Guest Editorial: A Special Issue on Low-Voltage Low-Power Analog Devices and Their Applications

Dear Readers,

It is well known that there is an increasing trend on the design of low-voltage low-power circuits due to the requirement of efficient portable electronic systems with long battery lifetime. For analog circuits, higher biasing current is needed to obtain the same performance with low supply voltages which, however, results in increasing the power consumption. On the other hand, lower biasing current restricts the dynamic range of the circuit, whereas with low supply voltages it is hard to keep all the transistors in saturation region. Thus, design techniques for low-voltage low-power operation are very important for analog circuit designers. In this Special Issue we deal with low-voltage low-power analog devices and their applications.

It is our great pleasure to introduce a collection of the best seven papers focusing on the design of low-voltage and/or low-power analog active circuits and their applications. Let us briefly introduce the published papers in this Special Issue.

The first paper in this Special Issue, written by *F. Khateb et al.*, presents the operation principle, advantages, and disadvantages of non-conventional techniques such as bulk-driven, floating-gate, and quasi-floating-gate transistors, enabling circuit designers to select between them depending on the application requirements. As an application example, three operational transconductance amplifiers (OTAs) are presented with supply voltages of ± 0.4 V and power consumption of 23.5 μW. PSpice simulation results using the 0.18 μm CMOS technology from TSMC are included to verify the design functionality and correspondence with the theory.

In the next paper, *S. A. Tekin et al.* proposed a low-voltage CMOS current-controlled floating resistor, designed by using a differential pair, which is convenient for integrated circuit implementation. The advantages of the proposed circuit consist in a wide tuning range of the resistance value, satisfactory frequency performance, and worthwhile dynamic range. As well as the proposed circuit is of a floating structure, it is able to be used as both positive and negative resistor. The proposed resistor requires ± 0.75 V power supply, with low-power dissipation of 0.41 mW. The circuit performance is simulated via SPICE.

In the third paper, *V. Stornelli and G. Ferri* present a current-mode low-voltage (1 V) and low-power (21 μW) differential difference second generation current conveyor (DDCCII). The circuit is developed by applying the current sensing technique to a fully balanced version of a differential difference amplifier. As a result, a low-voltage and low-power integrated version of the so-called DDCCII is designed. Post-layout results, using a 0.18 μm SMIC CMOS technology, have shown good general circuit performance, making the circuit suitable for a fully integration in battery portable systems, which can be, for example, fully differential Sallen-Key band-pass filter (BPF).

The paper by *S. Mahmoud and E. Soliman* designs a field programmable analog array (FPAA) consisting of seven configurable analog blocks (CABs) arranged in a hexagonal lattice such that the CABs are directly connected to each other. The CABs of the FPAA are based on a novel fully differential digitally programmable current conveyor (DPCCII), designed for ± 0.5 V supply voltages, having 0.6 mW power consumption. The programmability of the DPCCII is achieved using a digitally controlled three-bit MOS ladder current division network. A sixth-order Butterworth tunable low-pass filter suitable for WLAN/WiMAX receivers is mapped on the proposed FPAA. All the circuits are simulated using 90 nm CMOS technology from TSMC.

The fifth paper by *M. Kumngern et al.* deals with two voltage-mode multifunction biquadratic filters employing low-voltage ultra-low-power differential difference current conveyors (DDCCs). Each proposed circuit employs three DDCCs, two grounded capacitors, and two grounded resistors. By appropriate connection of the input and output terminals, the proposed filters can provide low-pass, band-pass, high-pass, band-stop, and all-pass voltage responses at high input impedance terminals, which is a desirable feature for voltage-mode operations. The natural frequency and the quality factor can be orthogonally set by adjusting the circuit components. The proposed circuits are simulated by using PSPICE simulators to confirm the presented theory.

The next paper by *A. Uygur and H. Kuntman* proposes an ultra low-voltage, ultra low-power voltage differencing transconductance amplifier (VDTA) employing dynamic threshold voltage MOS (DTMOS) transistors. The proposed VDTA is composed of two OTAs operating in the subthreshold region. Using TSMC 0.18 μm process technology parameters and with ± 0.2 V supply voltages, the total power consumption of the VDTA block is only 5.96 nW, and the transconductance –3 dB cutoff frequency is 3.3 kHz. As an application example, a fourth-order double-tuned BPF for processing real EEG data measurements is described. The filter dynamic range is cca 64 dB with 2 % THD and total power consumption of 12.7 nW.

In the last paper, written by *C. Muniz-Montero et al.*, a membership function generator circuit (MFGC) with bias supply of 1.5 V and independent DC-voltage programmable functionalities is presented. The realization is based on a programmable differential current mirror and three compact voltage-to-current converters, allowing continuous and quasi-linear adjustment of the center position, height, width, and slopes of the triangular/trapezoidal output waveforms. HSPICE simulation results of the proposed circuit using the parameters of a double-poly, three metal layers, 0.5 μm CMOS technology validate the functionality of the proposed architecture which exhibits a maximum deviation of the linearity in the programmability of 7 %.

We hope that the readers find the above papers interesting, inspiring, and motivating for their further research. Finally, we would like to thank all the anonymous reviewers who spent much of their precious time with reviewing the papers. Their timely reviews and comments greatly helped us in selecting the best papers for this Special Issue. We also thank all the authors who have submitted their papers for this issue. Special thanks go to the Editor-In-Chief, Assoc. Prof. Tomas Fryza, for his valuable support and for his assistance in the preparation of this volume.

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