A NEW DIFFERENTIAL CONFIGURATION SUITABLE FOR REALIZATION OF HIGH CMRR, ALL-PASS/NOTCH FILTERS

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Abstract: In this paper, a new configuration suitable for realization of differential input-differential output first order, second order all-pass and notch filters with high CMRR is given. The proposed configuration uses two negative type second-generation current conveyors (CCII-), and three admittances. Two first order and one second order all-pass filters and a notch filter (tunable if current controlled conveyor CCCII is used) are extracted from the proposed configuration. Tracking error, element mismatch, sensitivity analysis, simulation and experimental results are included.

1. INTRODUCTION

All-pass filters, also called phase equalizers are widely used for phase shifting while keeping the amplitude of input signal constant over the frequency range of interest. They can be used to equalize the undesired phase change as a result of processing the signal; they can also be used in the synthesis of multiphase oscillators. Notch filters on the other hand are used to eliminate a single frequency called the notch frequency.

Several all-pass and notch filter realizations using active elements are available in the literature [1-18]. These circuits use active elements such as second-generation current conveyors (CCII) [1-7, 9-11, 15, 17], operational amplifiers [12, 17], current differencing buffered amplifiers (CDBA) [13], four terminal floating nullors (FTFN) [8,14], third-generation current conveyors (CCIII) [16, 18] together with passive elements. However all of these phase equalizers are single input-single output structures [1-18].

Due to recent advances in integrated circuit technology it is possible to place analog as well as digital components on the same chip, thus obtaining mixed–mode signal processing circuits. Mixed-mode signal processing attracts increasing attention since it simplifies design, enables compactness and reduces cost. However signal interference from the digital to the analog part remains a serious problem to overcome; hence, for such circuits differential building blocks are accepted as a good solution. Therefore it is desired to process signals in differential form rather than simply as referenced to ground. Another advantage of differential operation over the single-ended case is that the amplitude of the signal increases by a factor of 2 [19].

An important parameter of differential active structures is the common-mode rejection ratio (CMRR). Differential signals have the advantage of canceling common-mode interference from unwanted signals and/or noise.

This paper presents a general configuration for realizing differential-input differential-output voltage-mode all-pass/notch filter circuits in Section 2; it consists of two CCIIs and three

admittances and, has very high CMRR, independent of matching element values. In Section 3, two first order, one second order all-pass and notch low sensitivity filter circuits are derived. In all of the filter circuits the CCIIs can be replaced by a current controlled conveyor (CCCII); one of these filter circuits has only external capacitors, which makes it much more feasible for IC implementation. For all the circuits the pole frequency can be controlled electronically by adjusting the bias currents of the CCCIIs without disturbing the unity gain of the filter. The advantages of the configuration are exhibited by considering the effects of the tracking error and element mismatch on the output, CMRR and differential gain, in Section 4. Section 5 contains comparative simulation results of all the filter circuits using transistor level implementation for the current conveyors. In Section 6 two of the proposed filters are constructed practically, while Section 7 concludes the paper.

2. THE PROPOSED CONFIGURATION

CCII has become very popular because of its high performance coupled with functional versatility. It has led to a wide application for implementation of high performance electronic functions operating in voltage mode or current mode [20].

The circuit symbol of CCII± is shown in Fig. 1 and its terminal relations in expression (1):

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{1}$$

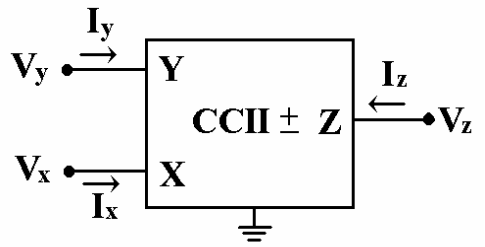

Figure 1. Circuit symbol of the CCII±.

The symbol of the CCCII± proposed in [21] is shown in Fig. 2 and is characterized by:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{2}$$

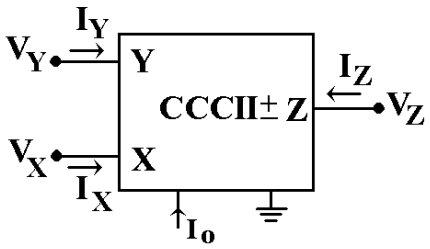

Figure 2. Circuit symbol of CCCII±.

Here the parasitic resistance R_x is the input resistance at terminal X and for BJT realizations it can be expressed as

$$R_x = \frac{V_T}{2I_o} \tag{3}$$

where V_T is the thermal voltage and I_0 is the bias current of the CCCII [21].

Conventionally the + or – signs of I_Z in equalities (1) and (2) denote the positive and negative type of current conveyors respectively.

The proposed general differential configuration is presented in Fig. 3. The differential input is connected to the Y terminals of the conveyors and the differential output voltage is taken across the Z terminals.

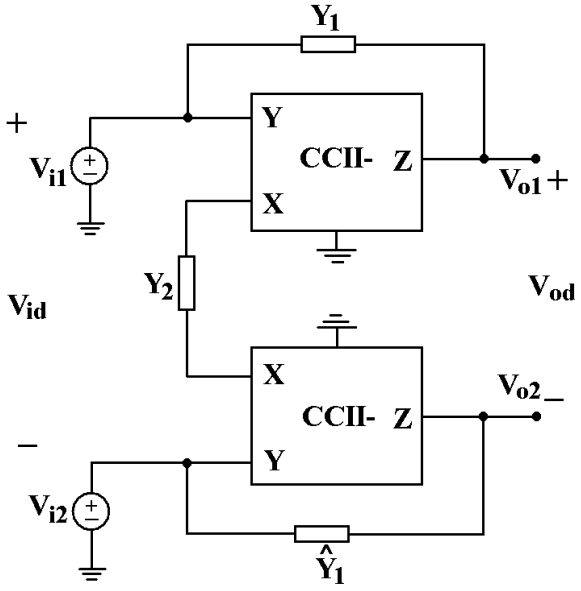

Figure 3. Proposed differential configuration.

Defining $V_{id} = V_{i1} - V_{i2}$, $V_{ic} = \frac{V_{i1} + V_{i2}}{2}$, and $V_{od} = V_{o1} - V_{o2}$, routine analysis of the circuit yields the outputs as:

$$V_{o1} = V_{ic} + (\frac{1}{2} - \frac{Y_2}{Y_1})V_{id} \tag{4}$$

$$V_{o2} = V_{ic} - (\frac{1}{2} - \frac{Y_2}{\hat{Y}_1})V_{id} \tag{5}$$

Then the differential output is:

$$V_{od} = V_{o1} - V_{o2} = \frac{Y_1\hat{Y}_1 - Y_2(Y_1 + \hat{Y}_1)}{Y_1\hat{Y}_1}V_{id} \tag{6}$$

If the output V_{od} is expressed in terms of V_{id} and V_{ic} as

$$V_{od} = A_{dm}V_{id} + A_{cm}V_{ic} \tag{7}$$

then,

$$A_{dm} = \frac{Y_1\hat{Y}_1 - Y_2(Y_1 + \hat{Y}_1)}{Y_1\hat{Y}_1} \tag{8}$$

and

$$A_{cm} = 0 \tag{9}$$

are obtained. Note that the common-mode gain (A_{cm}) of the circuit is equal to zero, independent of passive elements mismatches. Therefore the common-mode rejection ratio of the filter can be found theoretically as

$$CMRR = 20\log_{10}\left|\frac{A_{dm}}{A_{cm}}\right| \to \infty \tag{10}$$

which implies that the circuit has potentially high CMRR.

3. FILTER CIRCUITS DERIVED FROM THE CONFIGURATION

From the proposed differential configuration given in Fig. 3, different realizations for all-pass and notch filters can be extracted.

3.1. First Order All-Pass Sections

If in Fig. 3, the admittances are taken to be $Y_1 = 1/R_1$, $\hat{Y}_1 = 1/R_1$ and $Y_2 = \dfrac{1}{R_2 + 1/sC_2}$ then the configuration yields a first-order RC all-pass filter; the filter circuit is shown in Fig. 4.

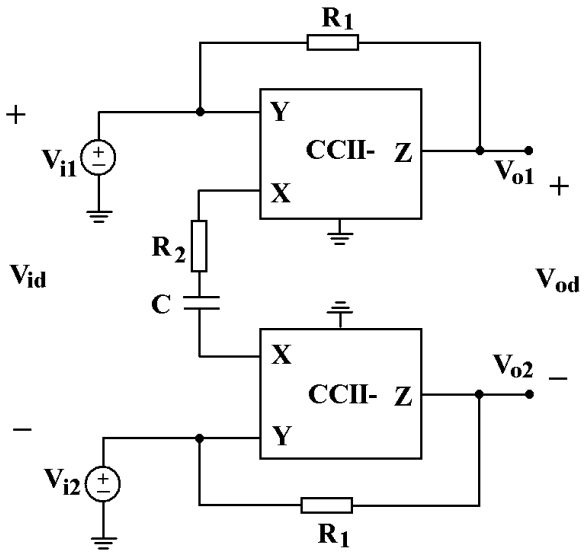

Figure 4. High CMRR first order RC All-Pass Filter.

Single ended and differential outputs of the circuit are obtained as:

$$V_{o1} = \frac{2(1+R_2Cs)V_{ic} + [1-(2R_1-R_2)Cs]V_{id}}{2(1+R_2Cs)} \tag{11}$$

$$V_{o2} = \frac{2(1+R_2Cs)V_{ic} - [1-(2R_1-R_2)Cs]V_{id}}{2(1+R_2Cs)} \tag{12}$$

$$V_{od} = \frac{1-(2R_1-R_2)Cs}{1+R_2Cs}V_{id} \tag{13}$$

By expressing the output V_{od} as given in (7)

$$A_{dm} = \frac{1-(2R_1-R_2)Cs}{1+R_2Cs} \tag{14}$$

and

$$A_{cm} = 0 \tag{15}$$

result. Selecting R_1=R_2=R the differential transfer function reduces to

$$\frac{V_{od}}{V_{id}} = \frac{1-RCs}{1+RCs} \tag{16}$$

and the filter has the following phase response

$$\varphi(\omega) = -2\arctan(\omega CR) \tag{17}$$

Equation (16) implies that the proposed circuit realizes transfer functions of a first order voltage mode all-pass filter with a gain of unity in magnitude. From equation (17) it can be seen that the circuit yields a phase shift from 0^o to -180^o.

By RC-CR transformation, namely letting $Y_1 = sC_1$, $\hat{Y}_1 = sC_1$ and $Y_2 = \dfrac{1}{R + 1/sC_2}$ in the configuration shown in Fig. 3, a new first-order all-pass filter can be obtained as shown in Fig. 5.

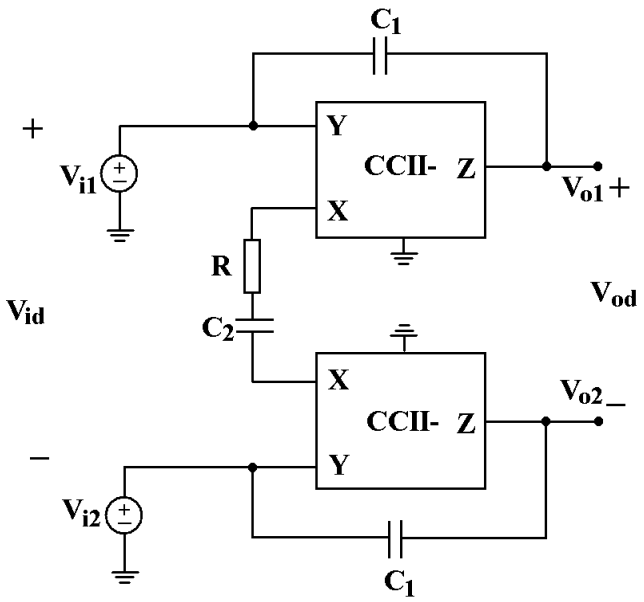

Figure 5. High CMRR first order filter after RC-CR transformation.

Routine analysis of the circuit shown in Fig. 5 yields for the outputs of the circuit

$$V_{o1} = \frac{2C_1(1+RC_2s)V_{ic} + [C_1 - 2C_2 + C_1C_2Rs]V_{id}}{2C_1(1+RC_2s)}, \tag{18}$$

$$V_{o2} = \frac{2C_1(1+RC_2s)V_{ic} - [C_1 - 2C_2 + C_1C_2Rs]V_{id}}{2C_1(1+RC_2s)}, \tag{19}$$

and

$$V_{od} = -\frac{\dfrac{2C_2}{C_1} - 1 - RC_2s}{1+RC_2s}V_{id} \tag{20}$$

for the differential output. Then differential and common mode gains are:

$$A_{dm} = -\frac{\dfrac{2C_2}{C_1} - 1 - RC_2s}{1+RC_2s} \tag{21}$$

and

$$A_{cm} = 0 \tag{22}$$

Note that the common-mode gain (A_{cm}) of the circuit is always equal to zero. Selecting C_1=C_2=C the differential transfer function reduces to

$$\frac{V_{od}}{V_{id}} = -\frac{1 - RCs}{1 + RCs} \tag{23}$$

and the filter has the following phase response

$$\varphi(\omega) = 180 - 2\arctan(\omega CR) \tag{24}$$

From (23) and (24) it can be seen that the circuit realizes a first order voltage mode all-pass filter with a gain of unity in magnitude and yields a phase shift from 180^o to 0^o.

The pole frequency for both circuits shown in Figs. 4 and 5 is found as:

$$f_p = \frac{1}{2\pi RC} \tag{25}$$

From equation (25) one can realize that the pole frequency can be adjusted by changing the value of the capacitor C or the resistor R without disturbing the unity gain of the phase equalizer. Moreover the sensitivity of the pole frequency is: $S_R^{f_p} = S_C^{f_p} = -1$.

In order to obtain a circuit more suitable for IC implementation, CCCII-s are used instead of CCII-s in the circuit of Fig. 5 resulting in a realization using only external capacitors as shown in Fig. 6. In fact in the circuit shown in Fig. 6, the parasitic resistances at terminals X of the CCCII-s replace the resistor R in the circuit shown in Fig. 5.

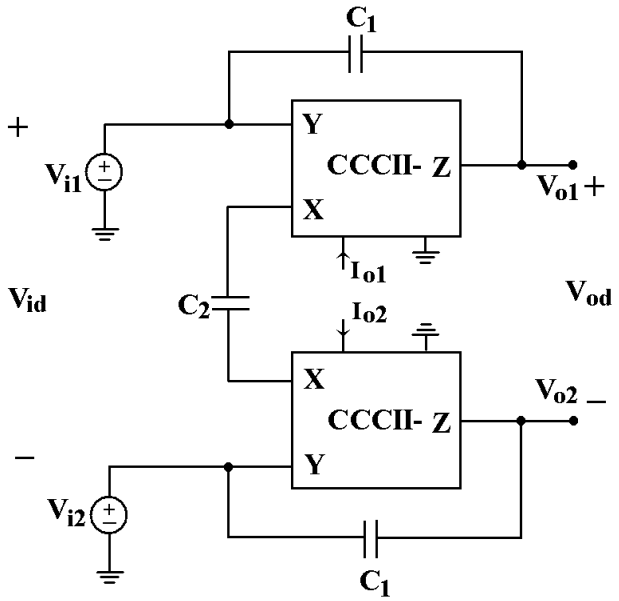

Figure 6. High CMRR first order only C all-pass filter.

All the equalities (18)-(25) are valid for the proposed circuit shown in Fig. 6 by replacing R with $R_{x1}+R_{x2}$; the transfer function becomes:

$$\frac{V_{od}}{V_{id}} = -\frac{1-(R_{x1}+R_{x2})Cs}{1+(R_{x1}+R_{x2})Cs} \tag{26}$$

with phase response

$$\varphi(\omega) = 180 - 2\arctan(\omega C(R_{x1}+R_{x2})) \tag{27}$$

and pole frequency

$$f_p = \frac{1}{2\pi(R_{x1}+R_{x2})C} \tag{28}$$

From equality (28) one can easily deduce that the pole frequency of the circuit can be adjusted by changing the value of the capacitor C and/or the electronically adjustable resistors R_{x1}, R_{x2} according to (3), without disturbing the unity gain property.

3.2. Second Order Realizations

The proposed configuration can be used for realizing second order filters. By choosing, $Y_1 = \hat{Y}_1 = \frac{1}{R_1} + sC_1$ and $Y_2 = \frac{1}{R_2 + 1/sC_2}$ for the admittances shown in Fig. 3 a second order all-pass/notch filter can be obtained as shown in Fig. 7.

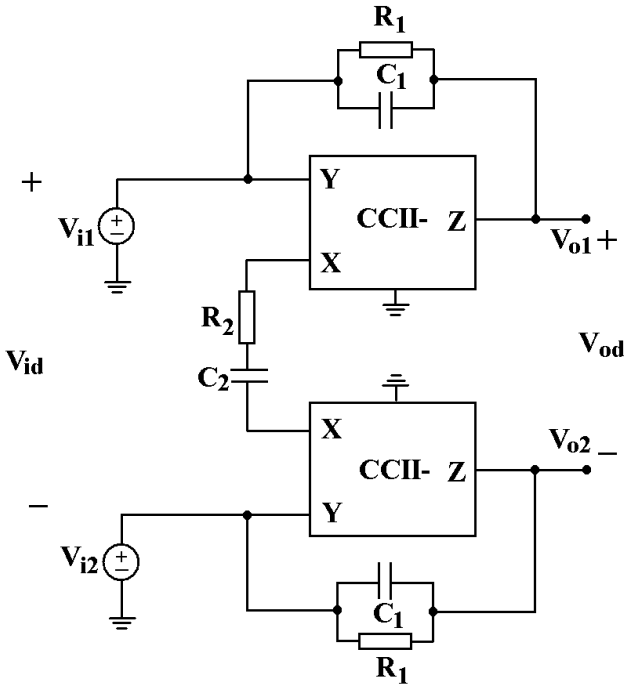

Figure 7. High CMRR second order All-Pass/Notch Filter.

The differential output voltage in this case is given by

$$V_{od} = V_{o1} - V_{o2} = \frac{s^2 - (\frac{2C_2 - C_1}{R_2 C_1 C_2} - \frac{1}{R_1 C_1})s + \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + (\frac{1}{R_2 C_2} + \frac{1}{R_1 C_1})s + \frac{1}{R_1 R_2 C_1 C_2}} V_{id} \tag{29}$$

By expressing the output V_{od} as given in (7)

$$A_{dm} = \frac{s^2 - (\frac{2C_2 - C_1}{R_2 C_1 C_2} - \frac{1}{R_1 C_1})s + \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + (\frac{1}{R_2 C_2} + \frac{1}{R_1 C_1})s + \frac{1}{R_1 R_2 C_1 C_2}} \tag{30}$$

and

$$A_{cm} = 0 \tag{31}$$

are obtained.

3.2.1. All-Pass-Section

For realizing the second order all-pass filter the following condition must be satisfied:

$$\frac{2C_2 - C_1}{R_2 C_1 C_2} - \frac{1}{R_1 C_1} = \frac{1}{R_2 C_2} + \frac{1}{R_1 C_1}, \tag{32}$$

which forces the following relation between resistor values

$$R_2 = (1 - \frac{C_1}{C_2}) R_1 \tag{33}$$

Then the filter has the phase response:

$$\varphi(\omega) = -2 \arctan \frac{(\frac{1}{R_2 C_2} + \frac{1}{R_1 C_1})\omega}{\frac{1}{R_1 R_2 C_1 C_2} - \omega^2} \tag{34}$$

As opposed to the first order realizations this circuit yields a phase shift from 0^o to -360^o and better pole frequency sensitivity. The pole frequency and the related sensitivities are:

$$f_p = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{35}$$

$S_{R_i}^{f_p} = S_{C_i}^{f_p} = -1/2$ for i=1,2.

3.2.2. Notch Filter

Another advantage of the circuit shown in Fig. 7 is its tunability by adjusting the value of resistor R_2 (via the bias current I_0 in the BJT implementation) to obtain a notch filter. Using:

$$R_2 = (2 - \frac{C_1}{C_2})R_1 \tag{36}$$

in the expression (30) for the gain yields:

$$A_{dm} = \frac{s^2 + \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + (\frac{1}{R_2 C_2} + \frac{1}{R_1 C_1})s + \frac{1}{R_1 R_2 C_1 C_2}} \tag{37}$$

As implied by (37) the notch frequency occurs at $f_n = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$ with same sensitivities.

4. TRACKING ERROR AND MISMATCH ANALYSIS

Taking into account the current conveyor non-idealities the terminal relations in (1) can be expressed as

$$I_Z = \alpha I_X \qquad V_X = \beta V_Y \qquad \text{and} \qquad I_Y = 0 \tag{36}$$

where α=1-ε_i and β=1-ε_v. Here ε_i and ε_v ($|\varepsilon_i|$<<1 and $|\varepsilon_v|$<<1) represent the current and voltage tracking errors of the current conveyors, respectively. Reanalyzing the proposed configuration shown in Fig. 3 and expressing the output in the form given in (7) yield:

$$V_{od} = V_{o1} - V_{o2} = \frac{(\beta_2 - \beta_1)(\alpha_2 Y_1 Y_2 + \alpha_1 \hat{Y}_1 Y_2)}{Y_1 \hat{Y}_1} \cdot V_{ic} + \left[1 - \frac{(\beta_1 + \beta_2)(\alpha_2 Y_1 Y_2 + \alpha_1 \hat{Y}_1 Y_2)}{2 Y_1 \hat{Y}_1}\right] \cdot V_{id} \tag{37}$$

$$A_{dm} = 1 - \frac{(\beta_1 + \beta_2)(\alpha_2 \hat{Z}_1 Y_2 + \alpha_1 Z_1 Y_2)}{2} \tag{38}$$

and

$$A_{cm} = (\beta_2 - \beta_1)(\alpha_2 \hat{Z}_1 Y_2 + \alpha_1 Z_1 Y_2) \tag{39}$$

where $Z=1/$Y. Note that:

i) Z_1, $\hat{Z}_1, Y_2$, being rational functions, the denominator in (38) therefore all pole frequencies are independent of tracking errors and the notch frequency is independent of voltage tracking errors β_1, β_2.

ii) in this case the common-mode gain (A_{cm}) of the configuration is not equal to zero. The common-mode rejection ratio of the filter can be found theoretically as:

$$CMRR = 20\log_{10}\left|\frac{A_{dm}}{A_{cm}}\right| = 20\log_{10}\left|\frac{2Y_1\hat{Y}_1 - (\beta_1+\beta_2)(\alpha_2 Y_1 Y_2 + \alpha_1\hat{Y}_1 Y_2)}{2(\beta_2-\beta_1)(\alpha_2 Y_1 Y_2 + \alpha_1\hat{Y}_1 Y_2)}\right| \tag{40}$$

which shows that the CMRR of the filter has a very high value because both of the parameters β_1 and β_2 are close to unity,

iii) for nominal values of all parameters V_{od} is related to V_{id} by:

$$V_{od} = (1 - 2Z_1Y_2)\, V_{id} \tag{41}$$

In the sequel $\beta_1 = \beta_2 = 1$ will be assumed to simplify the analysis and not without justification since the designer must exercise special care to ensure the rejection of the common mode voltage at the output as expressed in (37).

Letting $\hat{Z}_1 = Z_1 + \delta Z_1$ and $V_{od} + \delta V_{od}$ for the disturbed output,

$$V_{od} + \delta V_{od} = \left[1 - Z_1Y_2(1-\varepsilon_{i1}) - (Z_1+\delta Z_1)Y_2(1-\varepsilon_{i2})\right]V_{id} \tag{42}$$

and using (41) equality (43) is obtained for the deviation in the output.

$$\delta V_{od} = \left[(\varepsilon_{i1}+\varepsilon_{i2})Z_1 - (1-\varepsilon_{i2})\delta Z_1\right]Y_2 V_{id} \tag{43}$$

Neglecting second order terms and that $|1 - 2Z_1Y_2| = 1$, the expression for the relative error then becomes :

$$\left|\frac{\delta V_{od}}{V_{od}}\right| = \left|(\varepsilon_{i1}+\varepsilon_{i2}) - \frac{\delta Z_1}{Z_1}\right| \cdot \left|Z_1Y_2\right| \tag{44}$$

To get a feeling of what equality (44) means let $\varepsilon_{i1} = \varepsilon_{i2} = 0$, then $\left|\frac{\delta V_{od}}{V_{od}}\right| = \frac{|\delta Z_1|}{|R_2 + 1/j\omega C|}$ which decreases in the worst case to $\left|\frac{\delta V_{od}}{V_{od}}\right| = \frac{|\delta Z_1|}{R_2}$ as $\omega \to \infty$ e.g. for $R_2 = R_{x1} + R_{x2} = 1300\Omega$ (as is the case for only C all-pass filter simulation with $I_{o1} = I_{o2} = 20\mu A$ for CCCIIs), $\left|\frac{\delta V_{od}}{V_{od}}\right| = |\delta Z_1| / 1300$, a very small deviation at the output.

5. SIMULATION RESULTS

All the circuits have been simulated using the SPICE simulation program to verify the theoretical analysis.

5.1. First Order RC All-Pass Filter Simulation

For the conveyor CCII- in the first order all-pass filter the schematic implementation shown in Fig. 8 [22] with a DC supply voltage $= \pm 2.5$ V has been used.

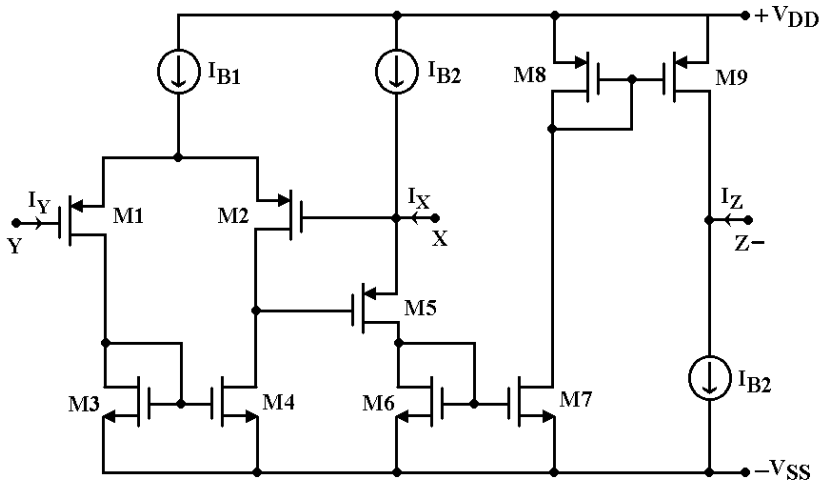

Figure 8. CMOS implementation of the CCII-.

Transistors are simulated using 0.35μm TSMC CMOS technology with parameters given in Table 1. and dimensions in Table 2. For the first order all-pass filter shown in Fig. 4 the element values are selected as: C=100pF and R_1=R_2=10kΩ, I_{B1}=200μA, I_{B2}=100μA which result in a 90^o phase shift at f_p=158.8 kHz and is very close to its ideal value (f_p=159.1 kHz).

The magnitude and phase characteristics of the simulated circuit are shown in Fig. 9 from which it can be seen that the simulation results agree quite well with the theoretical analysis.

Table 1. 0.35μm TSMC Model parameters of MOS transistors

```
.MODEL NM NMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17 GAMMA=0.5827871 PHI=0.7 VTO=0.5445549
+ DELTA=0 UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E-4 VMAX=8.309444E4
+ KAPPA=0.2574081 RSH=0.0559398 NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.046724E-8
+ CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3 PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10
+ MJSW=0.3508721)

.MODEL PM PMOS (LEVEL=3 TOX=7.9E-9 NSUB=1E17 GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674
+ DELTA=0 UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774 KP=6.733755E-5 VMAX=1.181551E5
+ KAPPA=1.5 RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13 WD=1.249872E-7
+ CGDO=3.09E-10 CGSO=3.09E-10 CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5
+ CJSW=4.813504E-10 MJSW=0.5)
```

Table 2. Transistor dimensions of the CCII-.

Transistor	W [μm]	L [μm]
M_1, M_2	24	0.35
M_3, M_4, M_6, M_7	10	1.5
M_5, M_8 M_9	15	1.5

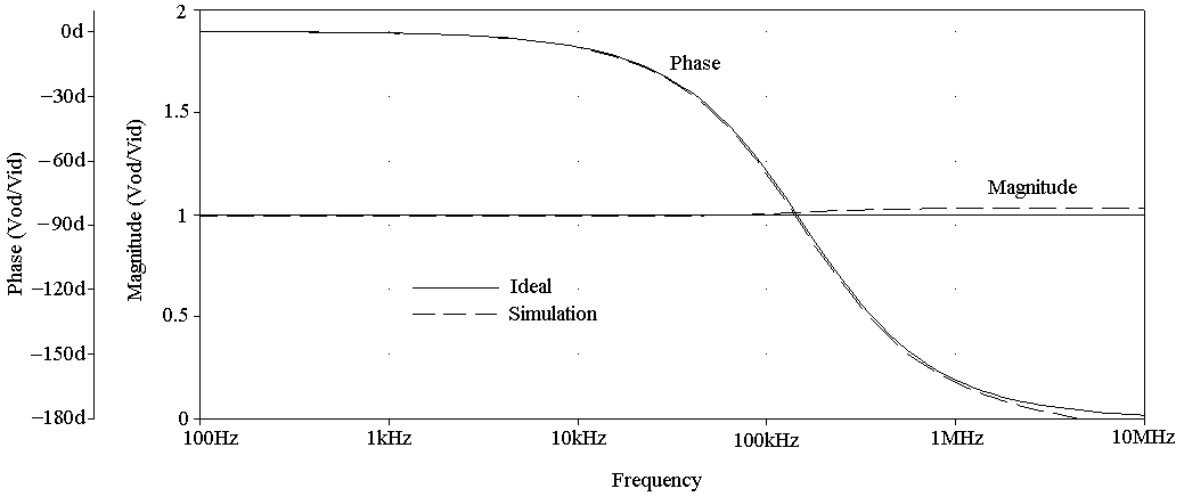

Figure 9. The magnitude and phase characteristics of the first order all-pass filter of Figure 4.

5.2 First order only C All-Pass Filter Simulation

The only C filter shown in Fig. 6 has been simulated using the CCCII- schematic implementation shown in Fig. 10 [21] with a DC supply voltage of ± 2.5 V.

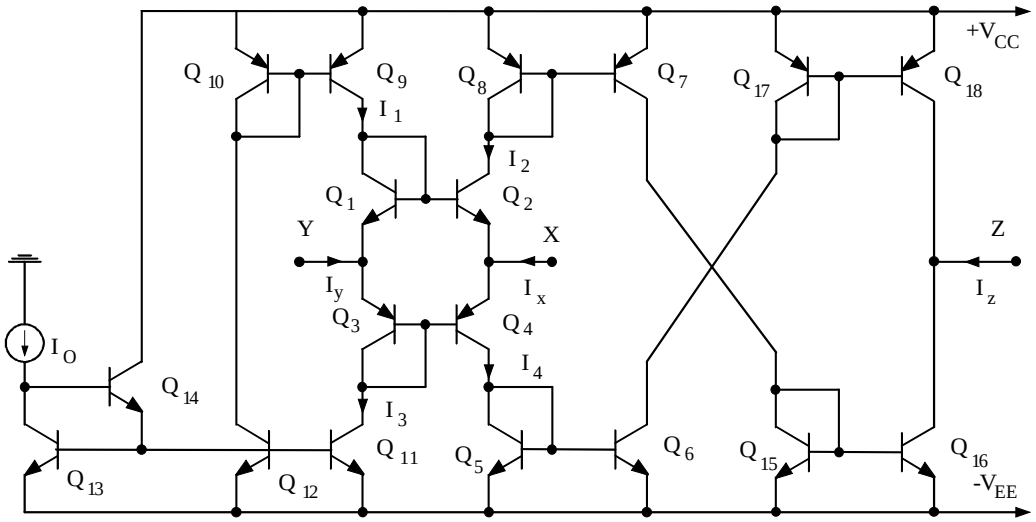

Figure 10. Schematic implementation for the CCCII–.

The PNP and the NPN transistors have been simulated using the parameters of the PR100N and NR100N bipolar transistors [23]; they are shown in Table 3.

Table 3. Model parameters of BJT's NR100N and PR100N

```
.MODEL NR100N NPN (IS=121E-018 BF=137.5 VAF=159.4 IKF=6.974E-3 ISE=36E-16
+ NE=1.713 BR=0.7258 VAR=10.73 IKR=2.198E-3 RE=1 RB=524.6 RBM=25 RC=50
+ CJE=0.214E-12 VJE=0.5 MJE=0.28 CJC=0.983E-13 VJC=0.5 MJC=0.3 XCJC=0.034
+ CJS=0.913E-12 VJS=0.64 MJS=0.4 FC=0.5 TF=0.425E-9 TR=0.425E-8 EG=1.206
+ XTB=1.538 XTI=2)

.MODEL PR100N PNP (IS=73.5E-018 BF=110 VAF=51.8 IKF=2.359E-3 ISE=25.1E-16
+ NE=1.650 BR=0.4745 VAR=9.96 IKR=6.478E-3 RE=3 RB=327 RBM=24.55 RC=50
+ CJE=0.180E-12 VJE=0.5 MJE=0.28 CJC=0.164E- 12 VJC=0.8 MJC=0.4 XCJC=0.037
+ CJS=1.03E-12 VJS=0.55 MJS=0.35 FC=0.5 TF=0.610E-9 TR=0.610E-8 EG=1.206 + XTB=1.866 XTI=1.7)
```

The element values are selected as: C=200pF, I_{o1}=I_{o2}=20μA (R_{x1}=R_{x2}=650Ω) which result in a 90^o phase shift at f_p=608 kHz and is very close to its ideal value (f_p=612.1kHz). Magnitude and phase characteristics of the simulated circuit are shown in Fig. 11 and the simulation results agree quite well with the theoretical analysis.

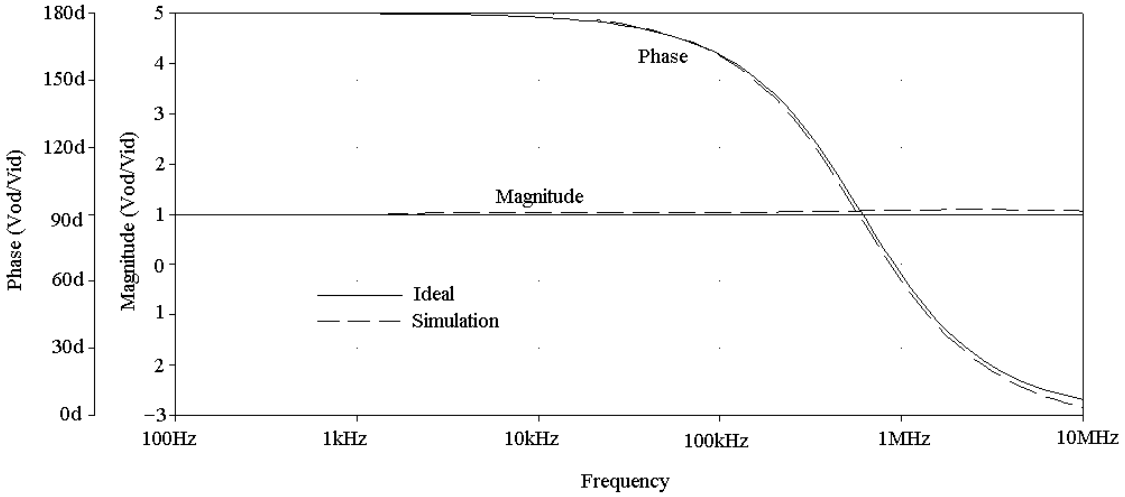

Figure 11. The magnitude and phase characteristics of the only C all-pass filter.

5.3 Second Order All-Pass Filter Simulation

The second order all-pass circuit shown in Fig. 7, has been simulated with the schematic implementation shown in Fig. 8 and MOS model parameters and dimensions given in Table 1 and 2, respectively. The element values are selected as: C_2=2C$_1$=100pF and R_1=2R_2=20kΩ, I_{B1}=200μA, I_{B2}=100μA which result in a 180^o phase shift at f_p=160 kHz and is very close to its ideal value (f_p=159.1 kHz). Magnitude and phase characteristics of the simulated circuit are shown in Fig. 12 and the simulation results agree quite well with the theoretical analysis.

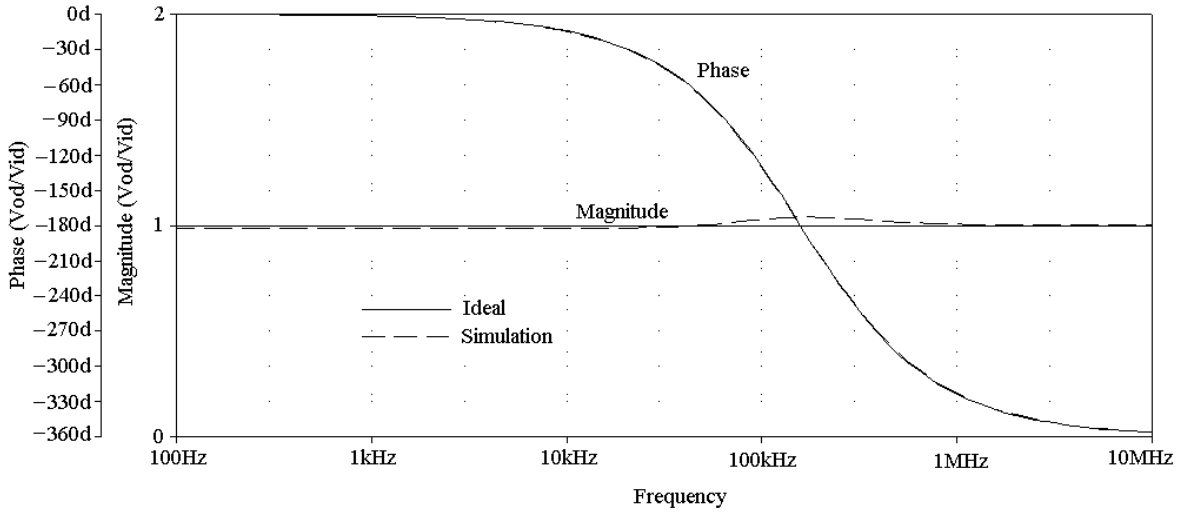

Figure 12. The Magnitude and Phase characteristics of the second-order all-pass filter.

5.4 Notch Filter Simulation

Keeping the same element values as for second order all-pass filter but changing R_2 to 30 kΩ the characteristic shown in Fig. 13 is obtained for the notch filter. The theoretical notch frequency being f_n=91.8 kHz, the simulated notch frequency was found to be f_n=90.2 kHz showing very good agreement.

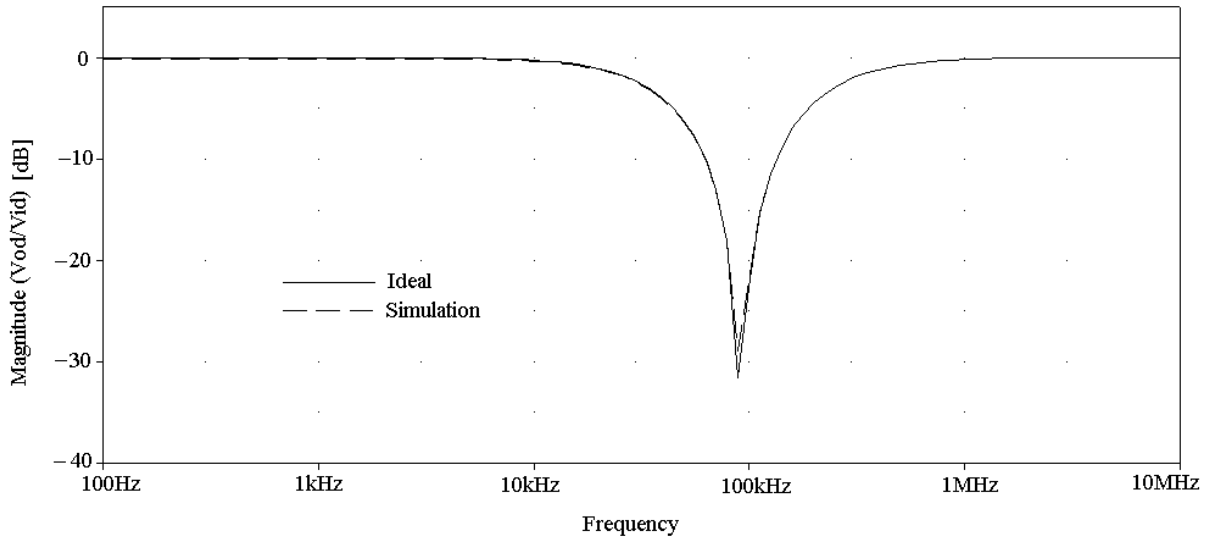

Figure 13. Magnitude characteristic of the notch filter.

6. EXPERIMENTAL RESULTS

The first and second order RC all-pass filters shown in Figs. 4 and 7 are constructed on National Instrument experimental board (Elvis) using AD844-type current conveyor (CCII+) IC of Analog Devices, 1% tolerance discrete resistors and polystyrene capacitors. The supply voltages are chosen as ±5V. To implement a CCII- , two CCII+ are used as shown in Fig. 14.

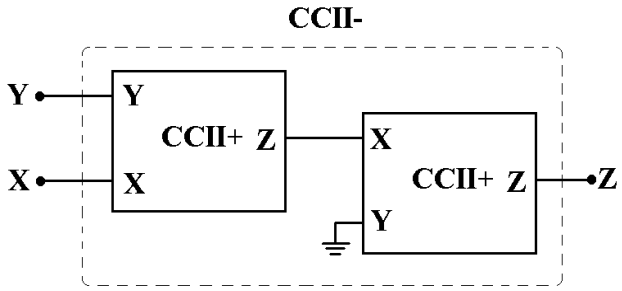

Figure 14. Implementation of a CCII- using two CCII+.

The circuit of Fig. 4 is constructed with R_1=R_2=10kΩ, C=10nF. The experimental result shows that the input and output signals are in 90^o phase difference at a pole frequency of 1.60 kHz as shown in Fig. 15.

Fig. 16 shows the experimental results for the circuit of Fig. 7 obtained with R_1=2R_2=20kΩ, C_2=2C_1= 10nF which results in a 180^o phase difference between input and output signals at the circuit pole frequency 1.60kHz.

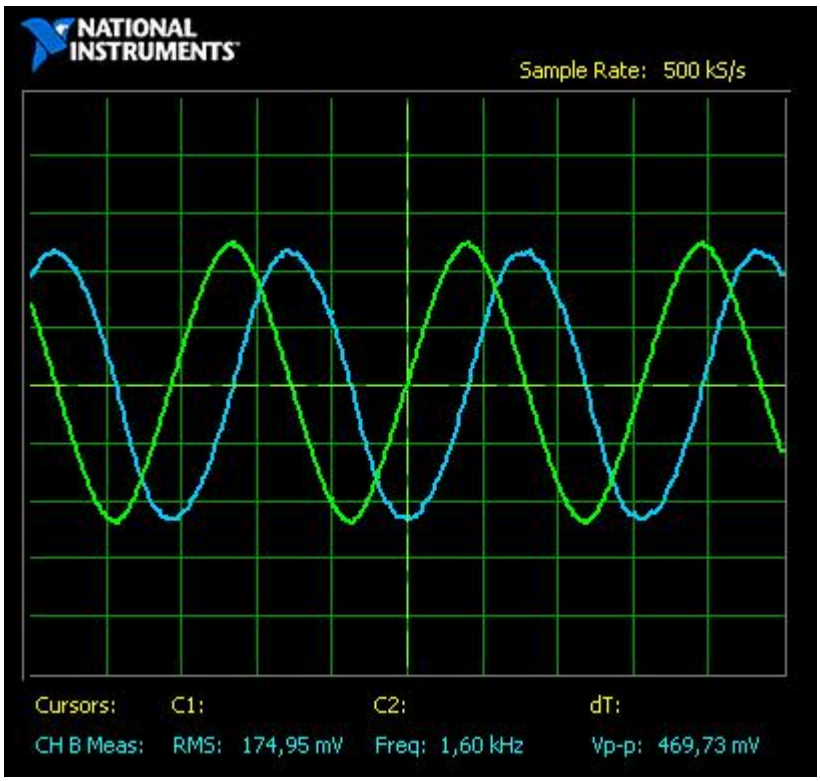

Figure 15. Experimental results of the first order RC all-pass filter (vertical scale: 100mV/divider, horizontal scale: 200μs/divider, blue color: output; green color: input).

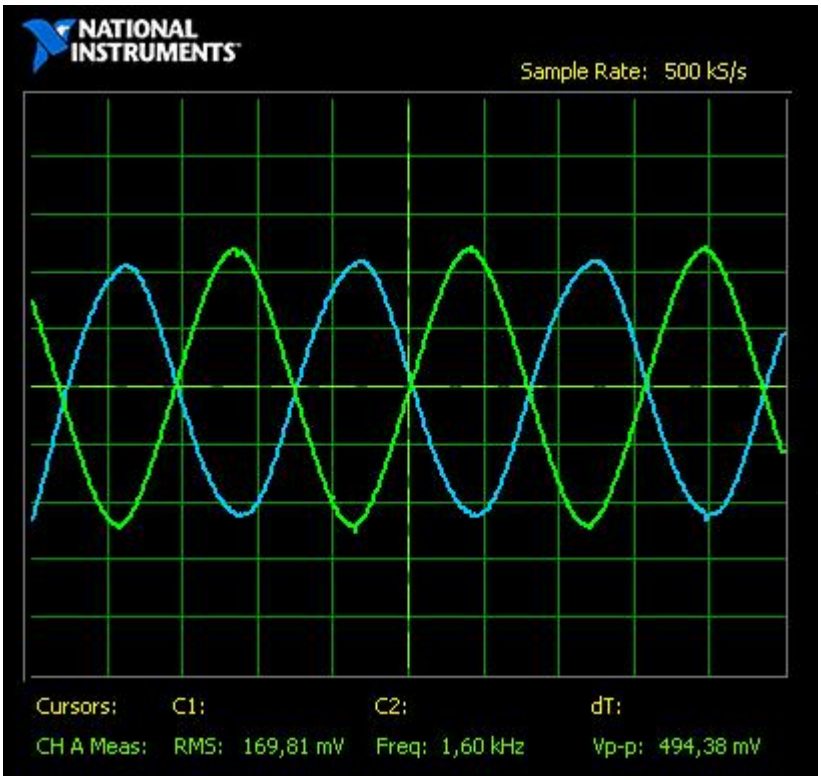

Figure 16. Experimental results of the second order all-pass filter (vertical scale: 100mV/divider, horizontal scale: 200μs/divider, blue color: output; green color: input).

7. CONCLUSION

In this paper a fully differential high CMRR general configuration for realizing first and second order all-pass and notch filters has been presented. The proposed configuration contains two CCII-s and three admittances. Two realizations for first order all-pass filter and one realization for second order all-pass filter have been given; it has been also shown that the second order filter can be tuned to behave like a notch filter. The pole frequency of the proposed filters and the notch frequency can be changed without disturbing the gain of the circuit. The non-ideality effects of current conveyors and element mismatches on the CMRR, voltage gains, pole and notch frequencies of the filters have been investigated and shown to be of negligible effect. The experimental and simulation results are given and shown to be in good agreement with theoretical analysis.

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