CMOS Realization of a Quantized-Output Classifier Circuit

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***Abstract*— In this paper a CMOS implementation of a multi-input data classifier with several output levels and a different architecture is presented. The proposed circuit operates in current-mode and can classify several types of analog vector data. The classifier circuit's new architecture consists of the interconnections of core cells each possessing a current-voltage converter, an inverter followed by a NOR gate and a voltage-current output stage. Using 0.35μm TSMC technology parameters, SPICE simulation results for a classifier with two inputs are included to verify the expected results.**

I. INTRODUCTION

The aim of classification is to assign an unknown object to a class containing similar objects. Classifier circuits can find applications in various fields of applied science such as automatic target recognition, real-time object recognition, pattern recognition, artificial intelligence, neural networks and statistics [1-5].

In this paper a one-dimensional classifier, called core circuit, shown in Fig. 1a with transfer characteristic as in Fig. 1b is used to realize an n-dimensional classifier as shown in Fig. 2 with an architecture resembling that of a 1-layer neural network. The current I_{in} is the 1-dimensional data for each core circuit and I_{out} is the output of the classifier; it should be observed that by grouping core circuits and adding the outputs in each group a multi-output classifier can be obtained as well. The transfer characteristic of the block in Fig. 1b is similar to a Trapezoidal Activation Function (TAF) [6] which is used in PWL approximation, high-speed folding analog-to-digital converters, fuzzy controllers, etc. The stability properties of neural networks with TAF have been investigated in [7] and a switched capacitor CMOS implementation of a cell with TAF has been proposed in [8]. Neurons with double threshold activation function have been investigated in literature and used to classify data separable by two parallel hyperplanes [9]. The primary aim of this paper is to develop a classifier circuit with n inputs and externally tunable decision regions and different amplitude in each region. In order to achieve this, an analog CMOS current-mode realization of a one-dimensional "classifier" circuit (core neuron) is realized. One-dimensional classifier can be used as a quantizer which in turn can be used for analog digital conversion.

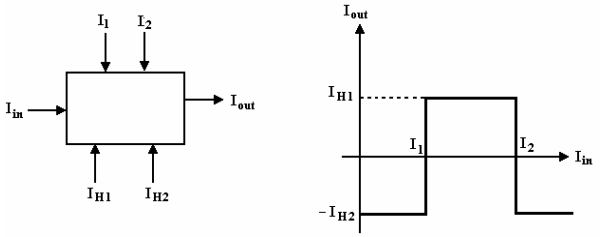

Figure 1.a. Core circuit block diagram. Figure 1.b. Transfer characteristic of the core circuit.

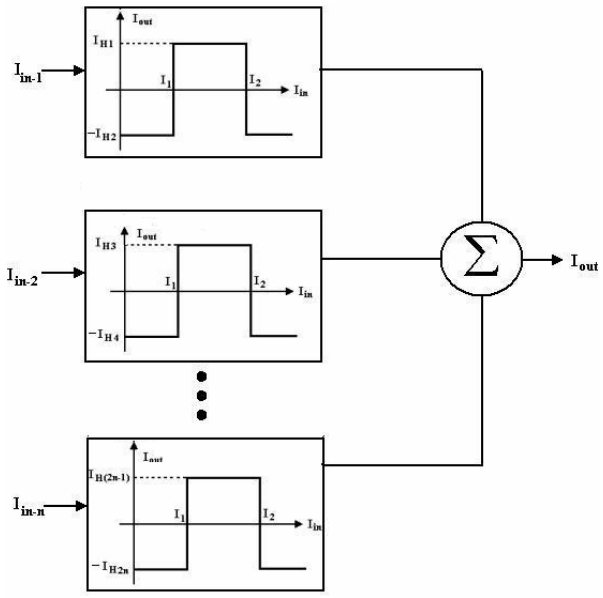

Figure 2. Block diagram of an n-dimensional classifier.

The classifier circuit has been simulated: *i)* with one input to illustrate the effects of quantization and *ii)* with two inputs to show the result of two-dimensional multilevel classification. As mentioned before the core neuron of the proposed circuit has a dc transfer characteristic as depicted in Fig. 1.b. The horizontal position, the width and the height of the transfer characteristic can be adjusted independently by means of external currents I_1, I_2 and I_{H1} and I_{H2}. Using several core circuits as shown in Fig. 2, a multi-dimensional, multi-level-output (each level corresponding to the coding of a data class) classifier is obtained.

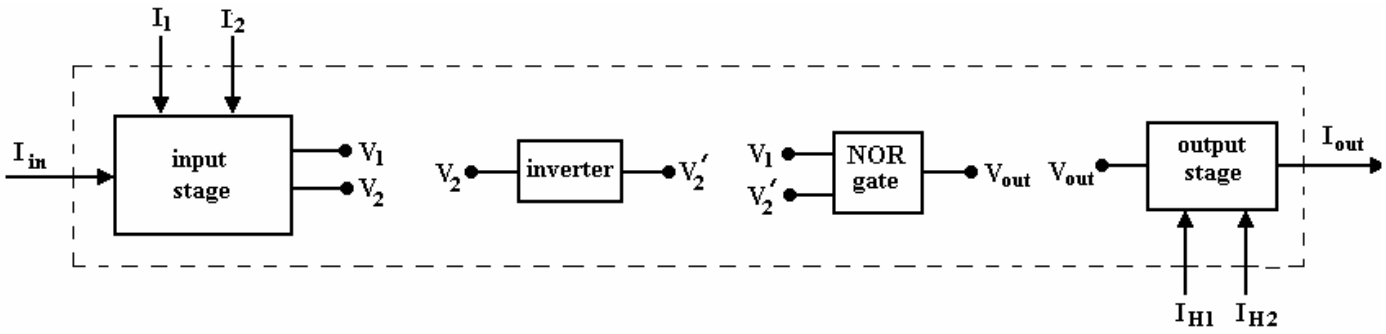

Figure 3. Block diagram of the core circuit.

II. CMOS REALIZATION OF THE CORE CIRCUIT

The input-output transfer characteristic shown in Fig. 1.b can be expressed as:

$$I_{out} = \begin{cases} I_{H1} & \text{for} \quad I_1 < I_{in} < I_2 \\ -I_{H2} & \text{otherwise} \end{cases} \tag{1}$$

The currents I_{H1} and I_{H2} as shown in Fig. 1.b are the positive and negative heights of the output current. The currents I_1 and I_2 are used to shift the horizontal position and adjust the width of the output current.

The proposed block diagram for realizing the core circuit with transfer characteristic of Fig. 1.b is shown in Fig. 3. It consists of a current-to-voltage input stage with two different outputs V_1 and V_2, an inverter, a NOR gate and a voltage-to-current output stage. The input stage and the inverter of the core circuit are shown in Fig. 4.

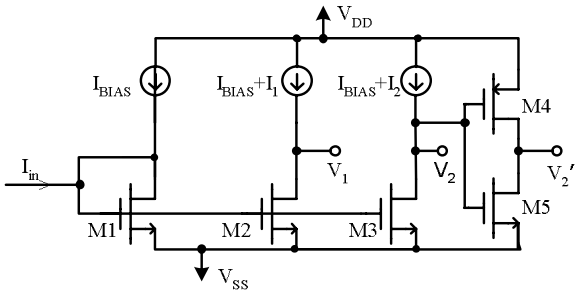

Figure 4. The input stage of the core circuit with the inverter.

The diode-connected transistor M_1 and the bias current I_{BIAS} form a current-to-voltage converter. The transistors M_2 and M_3 are biased with different currents $I_{BIAS}+I_1$ and $I_{BIAS}+I_2$ to form two different threshold currents of the transfer characteristic. The transistors M_1, M_2 and M_3 are matched. The transistors M_4 and M_5 constitute an inverter which is used to obtain an input-output characteristic with negative jump at threshold current I_2.

The NOR gate and the output stage of the proposed core circuit are shown in Fig. 5. The desired nonzero part of the transfer characteristics is obtained by the NOR gate (transistors M_6, M_7, M_8 and M_9) as follows: if both inputs of the NOR gate are at low level then the output of the gate is at high level, otherwise at low level. In fact V_{out} can be written as:

$$V_{out} = \begin{cases} V_{DD} & \text{for} \quad I_1 < I_{in} < I_2 \\ Vss & \text{otherwise} \end{cases} \tag{2}$$

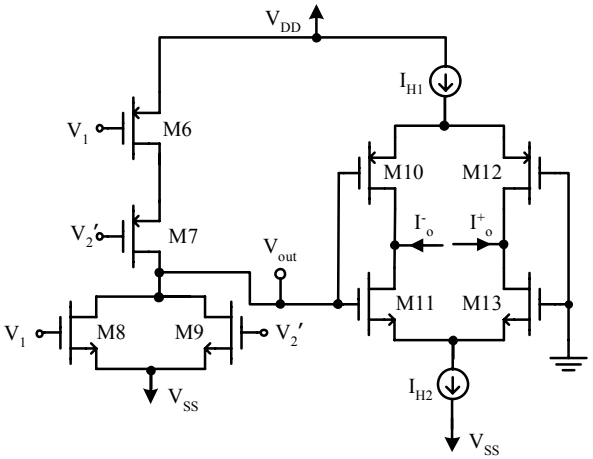

Figure 5. The NOR gate and the output stage of the core circuit.

The location of the nonzero portion of the output is fixed with the currents I_1 and I_2. This shift of the intercept points by adjusting the starting and ending boundary points of the specified decision region makes the device custom tunable. The currents I_{H1} and I_{H2} determine the peak values of the function. The current output stage of the circuit is obtained by connecting two complementary source-coupled pairs [10].

The current relations are $I_{DM10}+I_o^- = I_{DM11}$, $I_{DM12}+I_o^+ = I_{DM13}$, $I_{H1}=I_{DM10}+I_{DM12}$ and $I_{H2}=I_{DM11}+I_{DM13}$.

The output currents I_o^+ and I_o^- can be given in terms of V_{out} as follows:

$$I_o^+ = \begin{cases} I_{H1} & \text{for} \quad V_{out} = V_{DD} \\ -I_{H2} & \text{for} \quad V_{out} = V_{SS} \end{cases} \tag{3}$$

$$I_o^- = \begin{cases} -I_{H2} & \text{for} \quad V_{out} = V_{DD} \\ I_{H1} & \text{for} \quad V_{out} = V_{SS} \end{cases} \tag{4}$$

It should be noted that in the next section the current I_o^+ is used as the output current I_{out}, the current I_{H2} is chosen as 0 and the current I_{H1} denoted by I_H is used to change the height of the transfer characteristic.

III. Simulation of the Multilevel Classifier Circuit

To classify different types of data the proposed core circuits' outputs can be connected "in parallel" as shown in Fig. 2. In order to achieve the 1-D input-output characteristic shown in Fig. 6 the following constraints must be satisfied:

$$I_{in1} = I_{in2} = ... = I_{inn} = I_{in} \tag{5}$$

$$I_1 < I_2 < I_3 < ... < I_{(2n-1)} < I_{2n} \tag{6}$$

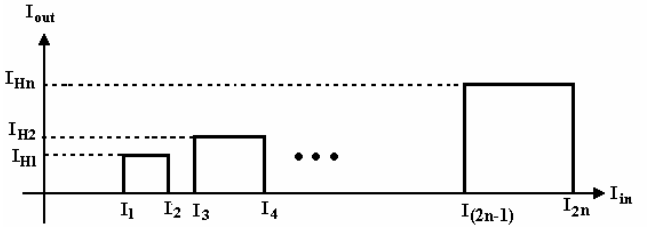

Figure 6. Desired Input-Output characteristic for the classifier.

Also the block diagram for realizing a 2-D multilevel classifier with two different input currents (I_{in1}, I_{in2}) is shown in Fig. 7.

The proposed core circuit is simulated using SPICE with 0.35μm TSMC MOSIS CMOS technology parameters. The voltage supply used in the proposed circuit is ± 1.25 V, the current I_{BIAS} is chosen as 0.1μA. The dimensions of the transistors are given in Table I.

The control currents and the power dissipation for the 2-D multilevel classifier block diagram of Fig. 7 are shown in Table II. The current I_{in1} is applied to core circuit-1 and core circuit-2, and the current I_{in2} is applied to core circuit-3 and core circuit-4.

SPICE simulation results for two different inputs to the classifier circuit are shown in Fig. 8. It can be seen from Fig. 8 that there are 8 different regions. So this kind of configuration can classify two-dimensional data into 8 different types of classes (9 if counting the I_{in1}-I_{in2} plane) each type being encoded with a different output current value.

To construct a quantizer circuit with eight quanta, eight core circuits need to be connected in parallel with the same input currents (I_{in}) and eight different sets of control currents. The selected classification parameters I_1, I_2 and the resolution parameter I_H for each core circuit are given in Table III.

To simulate the circuit as a quantizer a single triangular input waveform is applied to the input of the circuit and the input-output characteristic versus time is shown in Fig. 9. It should be observed that quanta width and peak value can be tuned at will thus providing further design flexibility.

TABLE I.

Dimensions of the MOS transistors

MOSFET	M_1, M_2, M_3, M_4, M_6, M_7, M_8, M_9,M_{10}, M_{11}	M_5	M_{12}, M_{13}
W [μm]	10	5	16
L [μm]	0.7	0.7	0.7

TABLE II.

Core Circuit Parameters (currents in μA)

Core Circuit-I			Power Dissipation	Core Circuit-II			Power Dissipation
I_1	I_2	I_{H1}	0.35mW	I_3	I_4	I_{H2}	0.77mW
70	140	60		210	280	120	
Core Circuit-III			**Power Dissipation**	**Core Circuit-IV**			**Power Dissipation**
I_5	I_6	I_{H3}	0.39mW	I_7	I_8	I_{H4}	0.91mW
60	140	100		280	360	80	

TABLE III

Core Circuit (CC) Parameters Used in Quantizer Circuit

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8
I_1 (μA)	0	5	10	15	20	25	30	35
I_2 (μA)	40	40	40	40	40	40	40	40
I_H (μA)	0.1	5	5	5	5	5	5	5

IV. Conclusion

In this paper, a current mode CMOS-only core circuit has been introduced and using this core circuit, a very flexible neural network like architecture has been designed and its abilities demonstrated. This circuit possessing a transfer characteristic with independently tunable heights, width and horizontal position, the proposed architecture can be used for a variety of purposes such as classification, quantization etc. Another advantage of the proposed circuit is its ability to operate at low supply voltages. Because of the parallel processing characteristic of the circuit, it is well-suited for real-world applications.

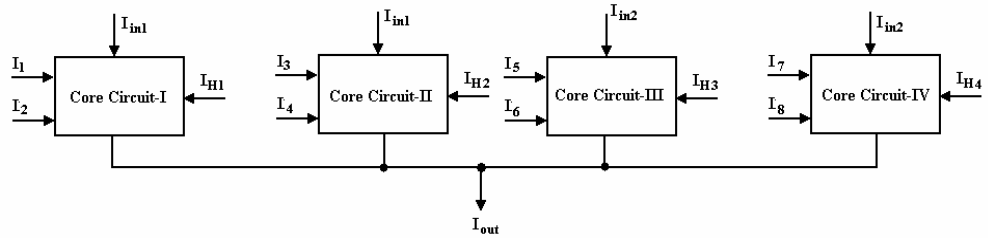

Figure 7. Block diagram of a two-dimensional multilevel classifier circuit.

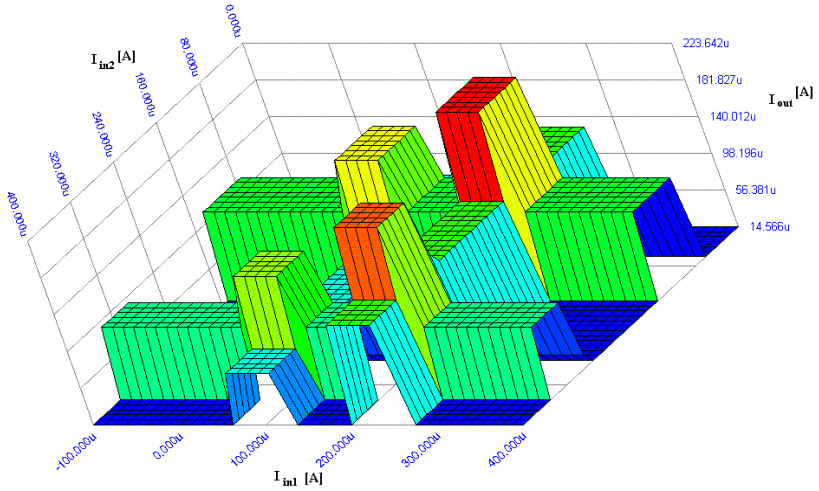

Figure 8. (I_{in1}-I_{in2})-I_{out} characteristic of the proposed two-dimensional multilevel classifier.

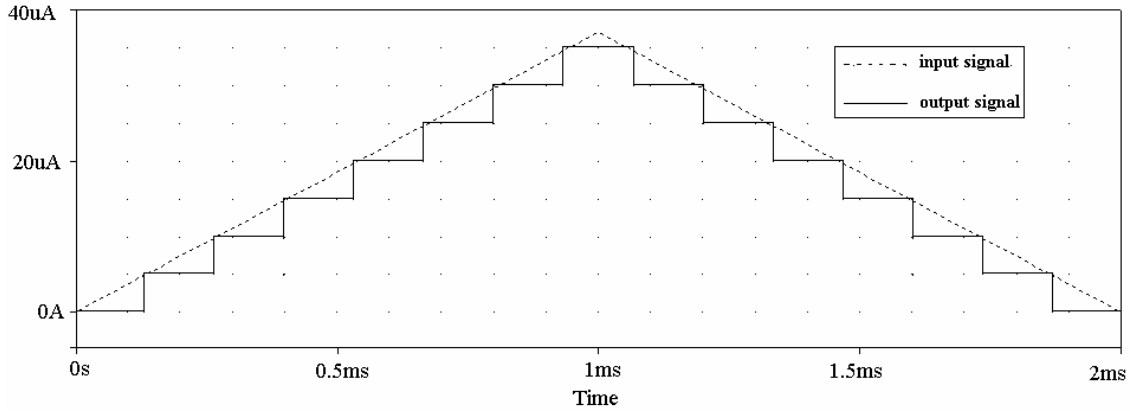

Figure 9. I_{in}-I_{out} characteristic of the eight level quantizer circuit.

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