ISTANBUL UNIVERSITY ENGINEERING FACULTY
JOURNAL OF ELECTRICAL & ELECTRONICS
YEAR : 2002 (547-553)
VOLUME : 2
NUMBER : 2

NEW HIGH PERFORMANCE REALIZATIONS FOR CURRENT-CONTROLLED CONVEYOR (CCCII)

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ABSTRACT

In this paper two new realizations, one CMOS and one bipolar, for current-controlled conveyor (CCCII) are proposed. The proposed circuits provide a good linearity, very high input impedance at port-y, high output impedance at port-z and good output/input current gain. SPICE simulation results using TUBITAK 3mCMOS process model are included to verify the expected values.

Keywords:*. *CMOS Circuits, CCCII

1. INTRODUCTION

Great interest has been devoted to the analysis and design of second generation current conveyor proposed by Sedra [1-2], mainly because it exhibits better performance, particularly higher speed and better bandwidth, than classic voltage-mode operational amplifiers, which are limited by a constant gain-bandwidth product [3-4]. On the other hand the recently introduced second-generation current-controlled conveyor (CCCII) [5-6] has the advantage of electronic adjustability over the current conveyor (CCII). Therefore there is a growing interest in the design of filters and oscillators using CCCIIs [7-11]. A number of circuit configurations for CCCIIs have been produced [5-6,12]. Although these circuits have a simple configuration, they suffer from low input impedance at port-y and low output impedance at port-z of the conveyor.

In this paper, two new circuits for realizing the CCCII are presented, each one with very small input impedance at port-x, a very high input impedance at port-y, a good linearity and high input/output gain ratio for current transfer. The resistances at port-x of the proposed CCCIIs, which can be controlled by adjusting the bias currents of the CCCIIs, are calculated theoretically. Simulation results, which confirm

Received Date : 6.2.2002
Accepted Date: 29.5.2002

the performance of the proposed CCCIIs, are included.

2. PROPOSED CIRCUITS

The port relations of an ideal CCCII, which is shown in Figure 1, can be given by

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \qquad (1)$$

where the positive and negative signs define a positive and negative current-controlled conveyor, respectively. The input resistance R_X at terminal x is proportional to $1/I_O$ for BJT realizations [5] and proportional to $1/\sqrt{I_O}$ for CMOS realizations [12] so that it is possible to control its value by changing the biasing current I_O.

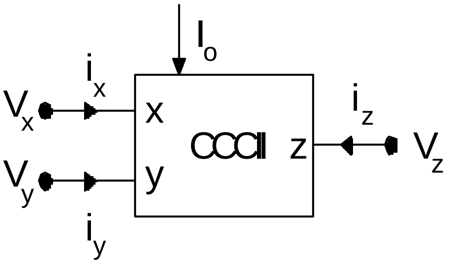


Figure 1. Electrical symbol of the CCCII.

The first proposed circuit, which is illustrated in Figure 2, is constructed with bipolar active feedback cascade current mirrors [13].

The conveyor x-input impedance is calculated as [5]

$$R_x = \frac{V_x - V_y}{I_x} = \frac{V_T}{2I_o} \qquad (2)$$

Thus, the x-input impedance can be controlled by the bias current I_o.

The z-output impedance of the proposed conveyor is calculated as

$$R_z = [g_{m36} \cdot g_{m37} \cdot r_{o38} . r_{o37} \cdot (r_{o36} \,//\, r_{o35})] \,//\, [g_{m23} \cdot g_{m24} \cdot r_{o21} . r_{o24} \cdot (r_{o23} \,//\, r_{o26})] \qquad (3)$$

where g_{mi} and r_{dsi} denote the transconductance and output resistance of the transistor numbered i, respectively. From Eqn (3) it can be seen that the proposed conveyor has a very high z-output impedance.

The second proposed circuit shown in Figure 3 is based on improved active feedback compact cascode current mirrors [14]. A major advantage of this circuit is that the output conductance and the feedback capacitance are lower 100 times than the standard current mirror circuit. The conveyor x-input impedance is calculated as

$$R_x = (g_{m102} + g_{m104} + g_{mbs102} + g_{mbs104})^{-1} \cong (g_{m102} + g_{m104})^{-1} \qquad (4)$$

and z-output impedance is calculated as

$$R_z \cong [g_{m23} \cdot g_{m2k} \cdot g_{msf22} \cdot r_{ds23} \cdot r_{ds24} \cdot (r_{ds2k} // r_{2c}) \cdot (r_{dsf22} // r_{osi})] // [g_{m33} \cdot g_{m3k} \cdot g_{msf32} \cdot r_{ds33} \cdot r_{ds34} \cdot (r_{ds3k} // r_{3c}) . (r_{dsf32} \,//\, r_{osi})] \qquad (5)$$

where g_{mi}, g_{mbsi}, and r_{dsi} denote the transconductance, body effect transconductance, output resistance of the MOS transistor numbered i, respectively. The r_{osi} is the input impedance of the current source I_{SF}.

Thus, the x-input impedance is very low and the z-output impedance is very high.

A current controlled conveyor with negative current transfer (CCCII-) can be obtained easily by adding two cross-coupled current mirror for the circuit shown in Figure 2 and two cross-coupled output stages for the circuit shown in Figure 3, in order to reveres the sign of current I_z.

3. SIMULATION RESULTS

The performance of the proposed circuits of CCCII+ is verified by SPICE simulation program using NR100N ve PR100N bipolar transistors parameters [15] for the first circuit and 3 µm TUBITAK CMOS transitor process model parameters for the second circuit. The dimensions of the MOS transistors used for SPICE simulations of the circuit in Figure 3 are given in Table 1. The voltage supply used for the CCCII given in Figure 2 is ±3.75 V with the bias current I_o =40µA. For the CMOS CCCII given in Figure 3 the supply voltage is ±5V and the bias current is I_o =50µA.

The basic dc and ac characteristics such as plots of V_x against V_y, plots of V_z against V_y and frequency response of I_z/I_x for the first and second circuits are obtained by SPICE simulations. The DC transfer characteristics of V_x against V_y (short circuited terminal z) for the both circuits are shown in Figure 4.

The voltage clipping limits at terminal-x are obtained as: V_{xmax}=2.84 V and V_{xmin}=-2.83 V for the first circuit and V_{xmax}=4.46 V and V_{xmin}=-4.36 V for the second circuit. Figure 5 shows the DC voltage transfer characteristic V_z-V_y from the input terminal y to the output terminal z for $R_z=\infty$ (open circuit) and short-circuited terminal x. The voltage clipping limits determined as: V_{zmax}=3.35 V V_{zmin}=-3.02 V for the first circuit and V_{zmax}=5 V and V_{zmin}=-5 V for the second circuit.

Table 1. Transistors aspect ratios

The second proposed circuit	
M101,M102,M2,M4, M22,M24,M4D	W=30μ L=3μ
M1,M3,M3D,M21, M23	W=450μ L=3μ
MSF1,MSF2,MSF21, MSF22	W=200μ L=3μ
MA,MB,MC,MK, M2A,M2B,M2C,M2K	W=300μ L=9μ
M103,M104,M12,M14, M32,M34	W=60μ L=3μ
M11,M13,M31,M33	W=900μ L=3μ
MSF11,MSF12,MSF31, MSF32	W=400μ L=3μ
M1A,M1B,M1C,M1K, M3A,M3B,M3C,M3K	W=600μ L=9μ

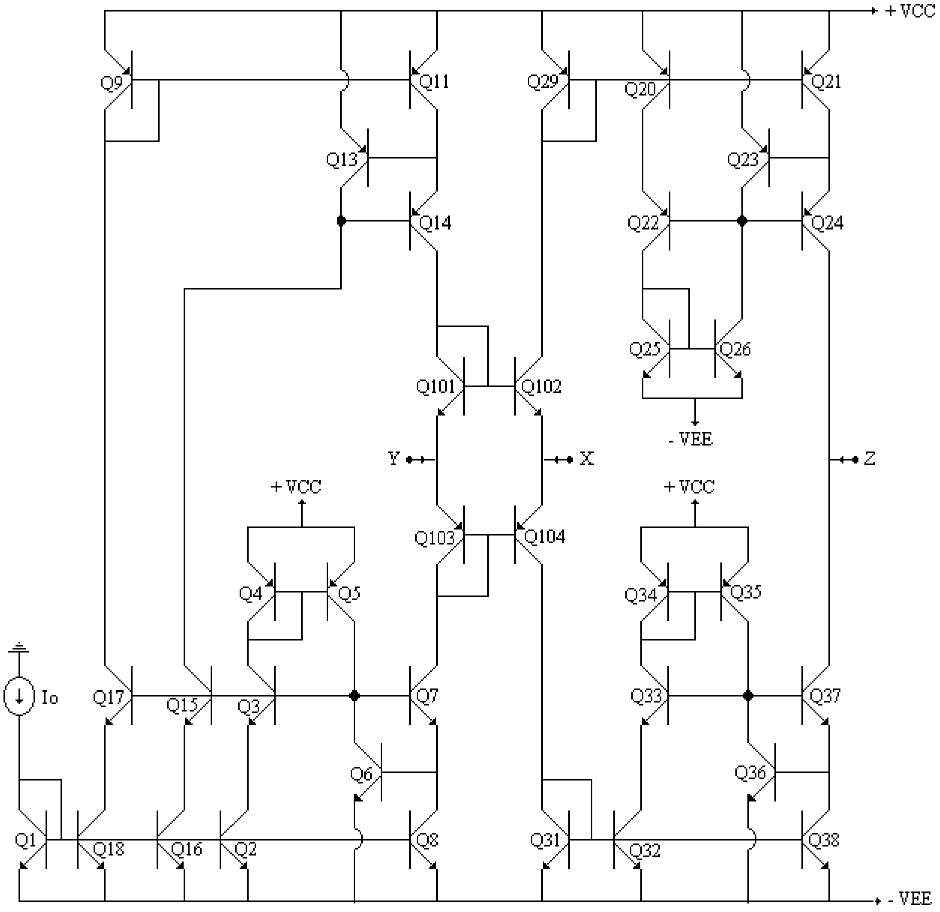


Figure 2. First proposed circuit for the CCCII.

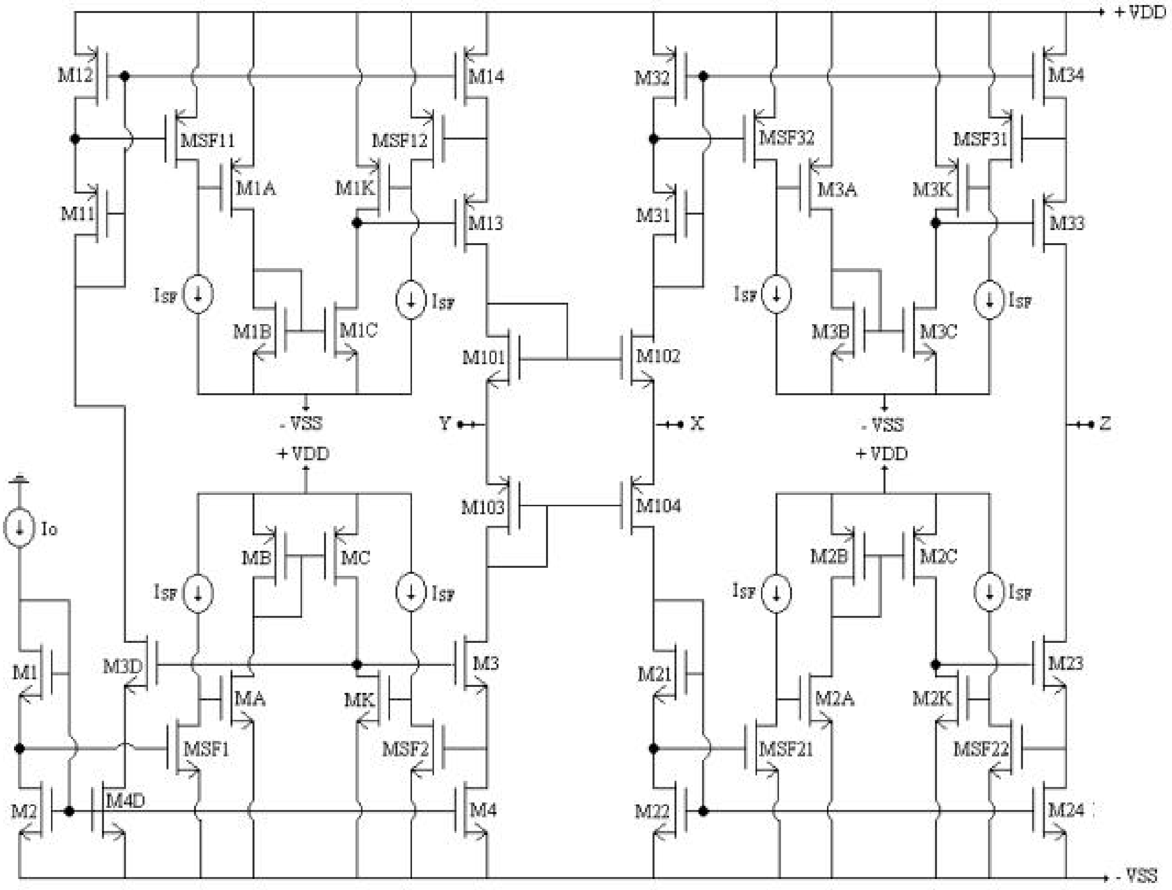
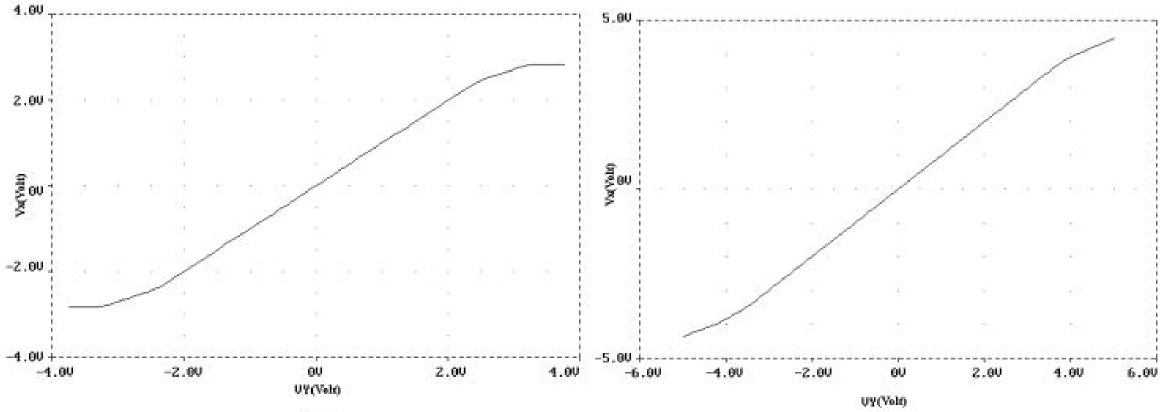
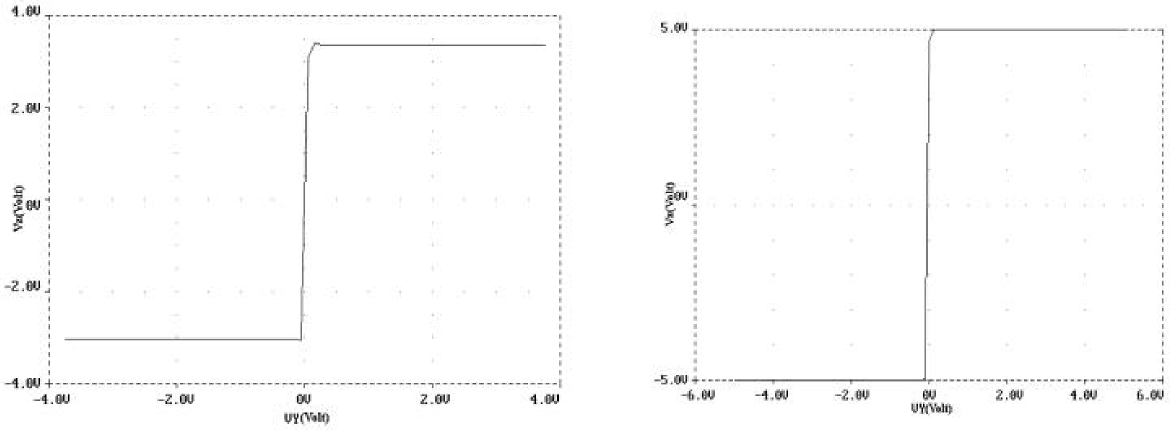


Figure 3. Second proposed circuit for the CCCII.



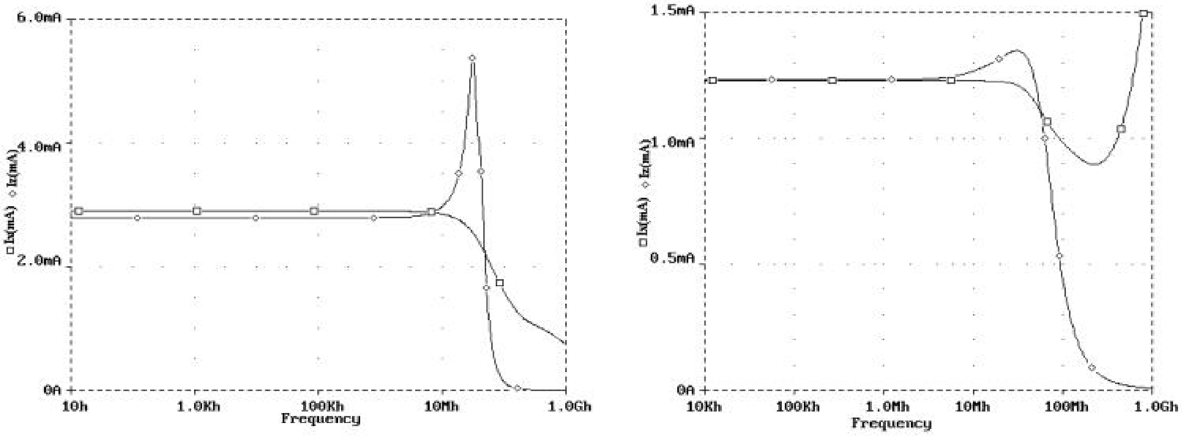
(a) (b)

Figure 4. The relation between V_x-V_y for (a) The first circuit (b) The second circuit.



(a) (b)

Figure 5. The relation between V_z-V_y for (a) The first circuit (b) The second circuit.



(a) (b)

Figure 6.The frequency response of the current follower (I_z and I_x) for (a) The first circuit (b) The second circuit.

The frequency responses of the current follower configuration of the proposed CCCIIs are shown in Figure 6. Table 2 gives the simulated results obtained from the voltage follower and the current follower configurations of the proposed CCCIIs. In this table, α_o and β_o are respectively the current and voltage transfer gains of the conveyor at low frequencies. w_a and w_b are the poles of the current and voltage transfer gains, respectively. The results confirm high performance of the proposed circuits.

Table 2. Simulation results

parameter	1st circuit	2nd circuit
R_y (Ω)	54.36×10^{6}	55.78×10^{6}
C_y (pF)	4.52	168×10^{-3}
R_z (Ω)	107.9×10^{6}	4.9×10^{9}
C_z (pF)	2.11	168×10^{-3}
R_x (Ω)	339	1.87×10^{3}
α_o	0.96	1
β_o	0.99	0.99
ω_α (r/s)	2.97×10^{8}	4.76×10^{8}
ω_β (r/s)	5.34×10^{8}	18.84×10^{8}

4. CONCLUSION

Two new realizations of the current-controlled conveyor are presented. The resistance values at port-x of the proposed circuits have been calculated. The simulation results confirm high performance of the circuits in terms of good linearity and wide bandwidths both in voltage and current operations.

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Hakan Kuntman: See Vol.2, Number 1, page 367.