OPERATION OF SILICON-GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS ON SILICON-ON-INSULATOR IN EXTREME ENVIRONMENTS
BY MARCO BELLINI

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I am a part of all that I have met;

Yet all experience is an arch wherethro'

Gleams that untravell'd world whose margin fades

For ever and for ever when I move.

Ulysses — Lord Tennyson

To my family

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Silicon-germanium heterojunction bipolar transistor (SiGe HBT) technology has recently become a viable competitor to III-V technologies for mixed-signal and RF through millimeter-wave circuit applications because it combines excellent transistor performance and compatibility with low-cost, conventional Si CMOS processes [25]. SiGe HBTs exhibit excellent gain, frequency response, low noise, high output resistance, and high transconductance per unit area [26].

Recently, several SiGe HBT devices fabricated on CMOS-compatible silicon on insulator(SOI) substrates (SiGe HBTs-on-SOI) have been demonstrated [14][28][4][83][65][34][51]. These transistors combine the well-known SiGe HBT performance with the advantages of SOI substrates: reduction in device parasitics and signal cross-talk, capability for high temperature operation, decreased vulnerability to radiation-induced soft errors, significant reduction of substrate capacitances, and elimination of latchup [16][51]. Moreover, these new devices are especially interesting in the context of extreme environments — highly challenging surroundings that lie outside commercial and even military electronics specifications [22]. However, fabricating HBTs on SOI substrates instead of traditional silicon bulk substrates requires extensive modifications to the structure of the transistors and results in significant trade-offs. Before this novel technology can be used in circuit applications, it is necessary to understand how SiGe HBTs-on-SOI differ from bulk SiGe HBTs in terms of device physics and operation both in normal and extreme environment conditions.

The present work investigates the performance and reliability of SiGe heterojunction bipolar transistors fabricated on silicon on insulator substrates with respect to operation in extreme environments such as at extremely low or extremely high temperatures or in the presence of radiation.

For example, high temperatures severely decrease the current gain and speed of SiGe

HBTs-on-SOI because of the adverse effects of the germanium fraction in the base. Moreover, the increased thermal resistance resulting from the SOI substrate may cause significant self-heating and further reduce the performance and reliability of the device.

Cryogenic temperature operation also poses concerns because the amount of impact ionization increases, potentially leading to reliability issues.

Operation of electronic devices of any kind in a radiation environment poses significant concerns from the points of view of total ionizing dose (TID) and single effect upset (SEU). While SiGe HBTs-on-SOI promise significant improvements in the TID and SEU response, these issues need to be carefully analyzed to ensure that the alterations necessary to accommodate the HBT on a SOI layer do not introduce new failure mechanisms and reliability concerns. For instance, the impact of the buried oxide and of the doping of the depleted collector on the TID response needs to be quantified. Studies of single event upsets are also necessary in order to understand the effects of substrate bias, collector doping, and device layout on the charge collected during an ion strike.

To conclude, this dissertation presents the results of investigations conducted along three different paths: the research of the effects of cryogenic temperatures, the analysis of operation at high temperatures, and the study of the impact of radiation on SiGe HBTs-on-SOI.

Chapter 1 introduces both extreme environments and SiGe HBTs, reviewing the state of the art of SiGe HBTs-on-SOI. The peculiar differences in behavior and performance resulting from the adoption of SOI substrates are explained.

Chapter 2 introduces Technology Computer Assisted Design (TCAD), also known as "device simulation". Simulation is an invaluable tool to investigate the microscopic behavior of a device and is used frequently in the present work. The particular challenges of simulating devices operating in extreme environments often require custom simulation or post-processing tools. Finally, a sophisticated example of custom post-processing — the 3-D regional transit time analysis — is presented [9].

Chapter 3 first presents an analysis of the *dc* performance of SiGe HBTs-on-SOI at cryogenic temperatures as low as 20 K [6]. In particular, the impact of collector doping in

thin-film SOI devices is analyzed. Then, the reliability of operation of SiGe HBTs-on-SOI at both room and cryogenic temperature is studied using different electrical stress techniques [13]. The implications of variations in the thermal resistance R_{TH} of the device on reliability at low temperatures are also discussed.

Chapter 4 analyzes the *dc* and *ac* performance of HBTs-on-SOI at temperatures as high as 330 °C [8]. Then, the impact of high temperatures on $1/f$ noise performance is also investigated [7].

Chapter 5 presents a comprehensive study of the radiation response of SiGe HBTs-on-SOI. Exposure to both x-ray and proton sources is used to understand the impact of total ionizing dose (TID) on the *dc* and *ac* figures of merit. The device investigated include complementary SiGe HBTs on thick-film SOI [11], fully and partially depleted SiGe HBTs on thin-film SOI (with conventional layout [10] and with $C_B E^B C$ layout [12]).

Finally, novel SEU phenomena are studied with the aid of 3-D TCAD simulations [12].

CHAPTER I

INTRODUCTION

This chapter provides a brief overview of SiGe HBTs-on-SOI, describing their device structure and commenting on their potential for operation in extreme environments.

The first section of this chapter introduces extreme environments of interest for SiGe HBTs-on-SOI. Then, the advantages of combining the SiGe HBT and SOI technologies are discussed. Subsequently, the device structure of conventional vertical (bulk) SiGe HBTs and of SiGe HBTs-on-SOI is compared. Examples of state-of-the-art SiGe HBTs-on-SOI are described. Finally, a brief review of the current understanding of device physics of SiGe HBTs-on-SOI is presented.

1.1 Extreme Environments

The term "extreme environments" (EE) identifies a small but very profitable niche market of electronics designed to operate in surroundings well outside commercial and even military specifications.

For example, EE applications may be characterized by extremely low or high temperature, pressure, vibration, and exposure to radiation or corrosive chemicals. This work focuses on the most relevant segments of EE from an application perspective: high and low temperatures and radiation.

An environment characterized by extreme temperatures can easily exceed the specifications of the commercial range (0 °C to 85 °C) or even of the military range (-55 °C to 125 °C) and reach extremes as low as 77.2 K (-196 °C) or even 4.2 K (-269 °C) on the cold side and as high 200 °C or 300 °C on the hot side [22]. Furthermore, numerous applications also impose challenging reliability requirements on cycling between high and low temperatures or on voltage stability over wide temperature ranges.

Examples of applications operating at cryogenic temperatures include orbital electronics,

systems for planetary and space missions, cryogenically cooled detectors and semiconductor-superconductor systems. High temperature electronics are often encountered in automotive applications (under-the-hood and engine electronics), aerospace applications, oil well logging, power switching, and radar systems [22].

Radiation is also a challenging environment: it poses significant threats to space and orbital electronics in the form of the following three failure mechanisms. The first is total ionizing dose (TID): x-rays, photons, and charged particles (such as protons and electrons) deposit significant amounts of positive charge inside the oxides of semiconductor devices. This charge significantly alters the electric fields and increases leakage currents [26].

A second failure mode is the formation of defects and the deactivation of dopants resulting from heavy mass particles causing displacement damage in the silicon volume.

Finally, high-energy particles create large amounts of electron-hole pairs in silicon, which may cause transient circuit malfunctions called single events upsets (SEUs) or may trigger destructive events such as single event latchup (SEL) [26].

As this work shows, despite these formidable challenges, SiGe HBTs-on-SOI have the potential to be ideal candidates for operation in extreme environments.

1.2 Advantages of SiGe HBTs-on-SOI

The original reason for interest in the silicon-on-insulator (SOI) technology was reducing vulnerability to single events effects (SEE) [67]. As explained in the previous section, a heavy ion strike on a semiconductor device generates a very large number of electron-hole pairs [69]. The generated charge separates because of either drift or diffusion and is collected at the contacts of the device, producing large current pulses that can significantly alter the circuit's behavior. For example, an ion-generated current pulse can drastically alter the charge stored in a capacitive node, altering information and leaving the circuit in an incorrect state. This is called single event upset (SEU) and is a common soft (i.e., recoverable) error.

An ion strike can also generate a large current, triggering a single event latchup (SEL), causing the complete destruction of the device [67].

In the context of SEE hardening, SOI devices possess a tremendous advantage over traditional bulk devices because the creation of electron-hole pairs is directly proportional to the silicon volume of the device. Therefore, SOI devices enable a dramatic reduction in collected charge because they have a silicon layer thickness of the order of hundreds of nm versus hundreds of μm for a bulk device [67]. Previous studies provide a clear comparison of the charge collected in SiGe HBTs fabricated on bulk silicon (with both high and low resistivity) and on thick-film SOI [62].

Interestingly, now SOI technology is mainly a focus of interest because it enhances performance rather than because it reduces SEE vulnerability [51]. The elimination of the substrate junction results in lower capacitances and in the elimination of substrate leakage. Importantly, the absence of substrate leakage translates in improved high-temperature operation and immunity to latchup [51][71]. The SiO_2 layer also dramatically reduces electromagnetic coupling between adjacent devices, suppressing crosstalk at low frequencies. It should be noted, however, that at frequencies higher than 1 GHz the buried oxide layer becomes essentially electromagnetically transparent. Consequently, the differences in crosstalk between SOI and bulk technologies disappear [64].

The advantages offered by SOI technology in terms of increased performances and reduced power consumption are particularly attractive to the CMOS digital logic market. According to [75], SOI wafers account for more than one third of the total revenues of the 300 mm wafer logic market. Taking into account the increasing commercial interest in SOI CMOS and the large popularity of BiCMOS platforms, it becomes natural to investigate the feasibility of the BiCMOS-on-SOI technology [54].

From the point of view of extreme environment applications, the combination of SiGe and SOI provides additional benefits [22]. At cryogenic temperatures, the presence of germanium in the base significantly increases both *dc* and *ac* performance [26]. At high temperatures the elimination of the substrate junction (absent in SOI devices) suppresses substrate leakage and latchup effect [16]. Also, SiGe HBTs-on-SOI share the same emitter-base stack and high base doping of bulk SiGe HBT and therefore benefit from reduced vulnerability to TID. Moreover, the adoption of a SOI substrate results in much smaller

silicon volumes and hence increased immunity to SEU, currently the Achilles' heel of bulk SiGe HBTs [22].

However, the benefits of SOI come at a price: the lower thermal conductivity of SiO_2 increases the thermal resistance R_{TH} and thus self-heating effects.

1.3 Introduction to bulk SiGe HBTs

This section describes the origins of SiGe heterojunction bipolar transistors, presents current state-of-the-art performance metrics, and gives a brief overview of the device structure of bulk SiGe HBTs.

The basic concepts behind SiGe HBTs are not recent. In fact, they were envisioned by W. Shockley in the very pioneer papers that laid the foundations for bipolar transistor devices [74][73] and were later refined by H. Kroemer in [44].

In silicon bipolar junction transistors (BJTs), the maximum current gain is limited by practical values of the doping in the emitter and in the base, but in SiGe HBTs the presence of germanium in the base effectively decouples base resistance (r_b), current gain β, and *ac* performance. The Gummel number in the base is reduced by the presence of germanium, which effectively weights the base doping, increasing the collector current I_C [26]. Consequently, it is possible to increase the base doping in order to reduce r_b and to improve the *ac* performance without sacrificing the current gain β. Furthermore, the presence of Ge grading across the base induces a drift field, which reduces the emitter-collector delay time τ_{ec} and thus increases the speed of the device.

Even though the basic principles of heterojunction bipolar transistors were well understood very early, fabrication challenges involved with producing high-quality, defect-free SiGe films were surmounted only in the mid-1980s with the advent of ultra-high vacuum chemical vapor deposition (UHV/CVD), opening up the path for commercial production of bulk SiGe HBTs [35].

Since the first demonstration of a SiGe HBT in December 1987, the interest in SiGe HBTs from both academia (in terms of paper published) and from industry (in terms of companies offering SiGe device technologies and applications) rose steadily through the

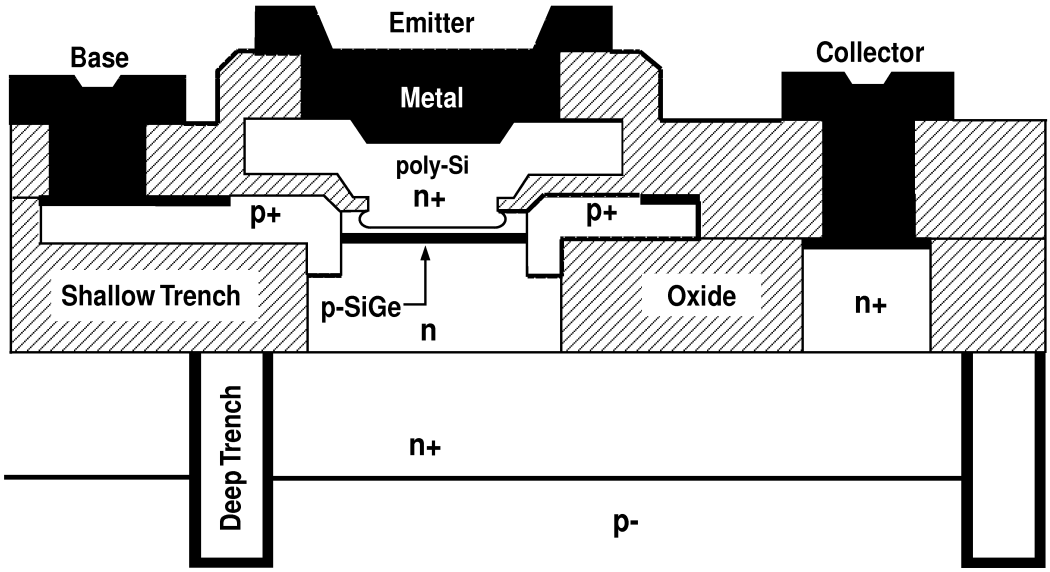


Figure 1: Schematic cross-section of a first generation SiGe HBT, after [26]. Drawing is not to scale.

years [26]. At the same time, figures of merit increased to reach current state-of-the-art levels such as the device described in [88], featuring a peak current gain β of 827, a f_T of 309 GHz, and a f_{max} of 343 GHz or the one reported in [20], reaching a peak β of 1900, a 240 GHz f_T, and a 300 GHz f_{max} at room temperature.

Figure 1 shows the cross-section of a first generation SiGe HBT, fabricated on a p^- substrate (with a typical resistivity of 10-15 $\Omega - cm$). A high n doping sub-collector (5-10 $\Omega/\square$) provides a low resistivity path from the collector to the top collector contact. A low doping n collector epi layer is grown on top. Shallow trenches are formed in order to isolate adjacent devices. Then, the reach-though connecting the sub-collector to the emitter contact is implanted. Subsequently, the emitter-base stack is grown with UHV/CVD, using a self-aligning process. The collector is then selectively implanted to trim breakdown and *ac* performance. Finally, the polysilicon extrinsic base and the emitter are formed [26].

1.4 Introduction to SiGe HBTs-on-SOI

This section introduces SiGe HBTs-on-SOI, underlining the differences in their device structure and fabrication with respect to traditional bulk devices. HBTs-on-SOI fall into two

Table 1: Figures of merit of C-SiGe HBTs on thick-film SOI. After [29].

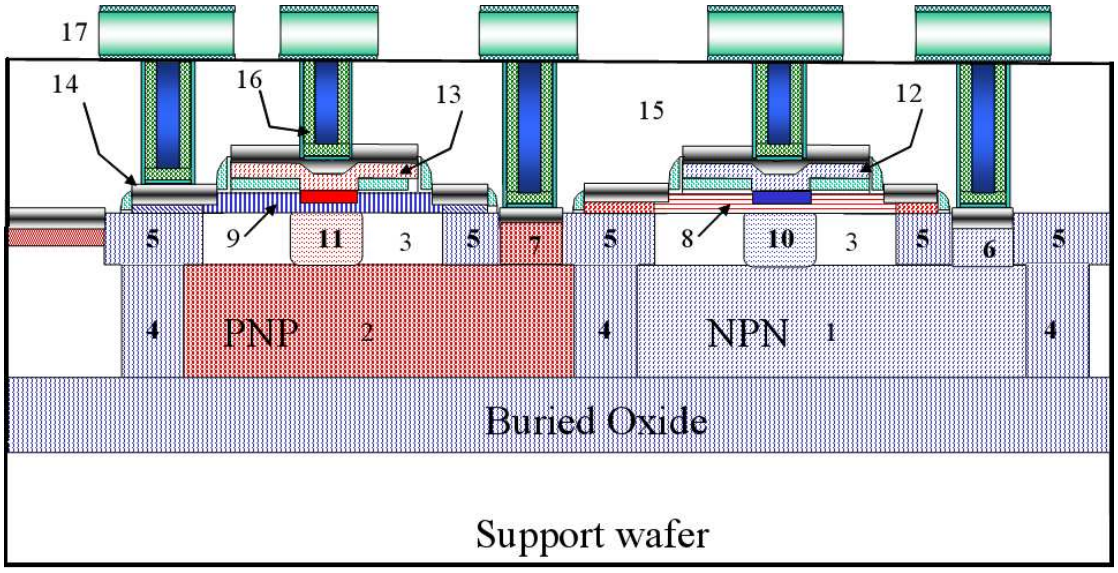
Figure of Merit (300K)	*npn*	*pnp*
β	200	200
V_A	150 V	100 V
f_T (V_{CE}=5 V)	25 GHz	25 GHz
f_{max} (V_{CE}=5 V)	90 GHz	60 GHz
B_{VCEO}	5.5 V	5.5 V
B_{VCBO}	7 V	6 V

main categories depending on the thickness of their SOI substrate. Examples of state-of-the-art SiGe HBTs on both thick- and thin-film SOI are presented to show the capabilities of these technologies.

1.4.1 SiGe HBTs on thick-film SOI

SiGe HBTs fabricated on thick-film SOI (typically $\approx$ 1-2 μm) can accommodate both collector and sub-collector and are characterized by a device structure very similar to bulk devices [28][29][83][65][34]. Therefore, their physical behavior is extremely close to a bulk device with the exception of the increase in thermal resistance R_{TH} caused by the lower thermal conductivity of SiO_2. A further disadvantage of these devices is that obviously they cannot be integrated with high performance CMOS SOI processes that have SOI layer thicknesses of the order of 0.1-0.2 μm. Also, deep trenches (DT) are needed to isolate transistors [14].

Figure 2 shows the schematic cross-section of a complementary-SiGe (C-SiGe) BiCMOS technology featuring both npn and pnp SiGe HBTs integrated on thick-film SOI. These devices have been designed for 5 V analog and mixed-signal applications and carefully optimized for balanced npn and pnp performance, low base resistance, low noise, and high βV_A product. The device performance is summarized in Table 1 [28][29]. The intended applications of this C-SiGe technology include a wide variety of low-power, high-frequency, precision analog/mixed-signal circuits such as data converters and amplifiers. A good example of the utility of this C-SiGe analog I_C platform includes a record-performance 12-bit, 500 MS/s C-SiGe analog-to-digital converter [79].



1: N-buried layer; 2: P-buried layer; 3: Collector epitaxy
4: Deep trench; 5: STI; 6: NPN sinker; 7: PNP sinker; 8:
NPN base; 9: PNP base; 10: NPN SIC; 11: PNP SIC; 12:
NEMIT POLY; 13: PEMIT POLY; 14: $CoSi_2$; 15: BPSG;
16: Contact; 17: 1^{st} metal (2^{nd}-4^{th} metal not shown).

Figure 2: Schematic cross-section of npn and pnp SiGe HBTs fabricated on thick-film SOI [29].

Table 2: Figures of merit of SiGe HBTs on thin-film SOI. After [15].

Figure of Merit (300 K)	Fully-Depleted (Low N_C)	Partially-Depleted (High N_C)
f_T (V_S=0 V)	30 GHz	45 GHz
f_T (V_S=20 V)	60 GHz	75 GHz
f_{max} (V_S=0 V)	45 GHz	55 GHz
f_{max} (V_S=20 V)	67 GHz	72 GHz
B_{VCEO} (V_S=0 V)	4.8 V	1.2 V
B_{VCEO} (V_S=20 V)	1.5 V	1.2 V
B_{VCBO}	13 V	4.5 V

This technology platform, commercially available from Texas Instruments under the name BiCOM3X, features a 1.5 μm thick-film SOI layer on top of a 0.145 μm buried oxide (BOX) insulating layer. Deep trenches are used to electrically insulate the devices. A boron-doped base is deposited for the npn SiGe HBT and an arsenic-doped base is used for the pnp SiGe HBT. An ultra-thin (< 10 $\mathring{A}$) IFO is grown before the emitter is deposited, followed by emitter polysilicon, which is implanted with either arsenic for the npn or BF_2 for the pnp.

1.4.2 SiGe HBTs on thin-film SOI

Fabricating a SiGe HBT on thin-film SOI layer is an even more challenging feat since it requires a completely different structure than a bulk SiGe HBT. The 0.1-0.2 μm SOI layer is too thin to accommodate the thick, heavily doped sub-collector needed in high-speed transistors to provide a low resistivity path from the CB junction to the top collector contact. Recently, however, a new "folded" SiGe HBT structure has been demonstrated [14][15][58], as shown in Figure 3. In this device, the emitter and base profiles are comparable to those in second-generation bulk SiGe HBTs, but the sub-collector is replaced by either a fully or partially depleted collector (by changing the doping N_C). As noted in [15][4] , the total transit time is limited by the $R \times C_{CjC}$ delay in the partially depleted SiGe HBT-on-SOI and by lateral drift in the fully depleted SiGe HBT-on-SOI.

This device shares the same substrate as a commercial IBM 130 nm SOI CMOS technology, featuring a 120 nm silicon layer on top of a 140 nm buried oxide layer. Through selective collector ion implantation both a fully depleted device with a collector doping

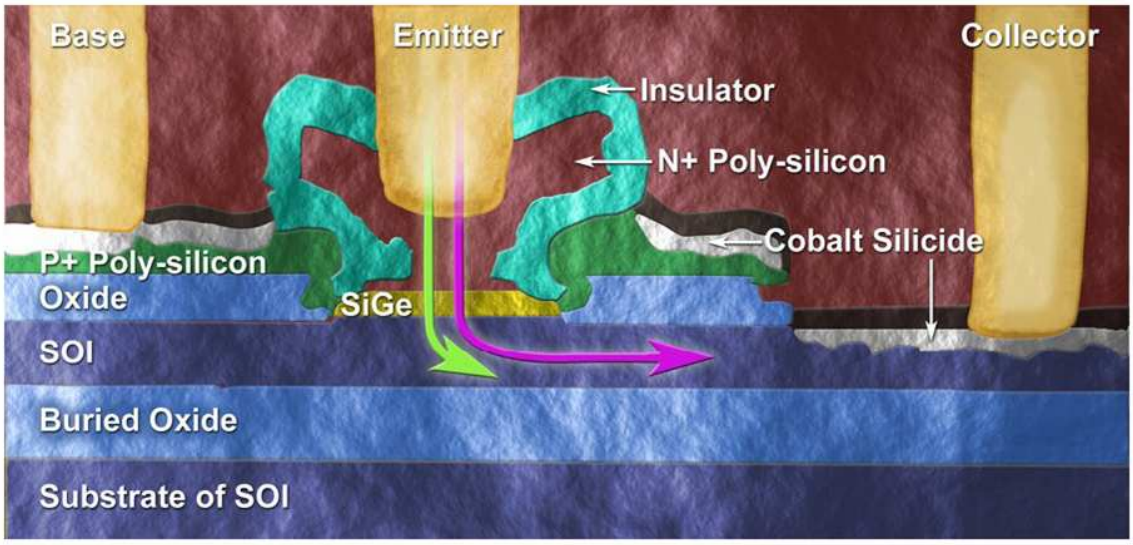


Figure 3: Cross-sectional SEM micrograph of a SiGe HBT on CMOS-compatible 120 nm thin-film SOI layer. From [14]

(N_C) of $1.5 \times 10^{17} cm^{-3}$ and a partially depleted device with N_C of $4.8 \times 10^{17} cm^{-3}$ can be fabricated. The device performance is summarized in Table 2.

The absence of the sub-collector results in significant differences in the device physics. The current flow is intrinsically 2-D and can be separated into a vertical path, directly under the emitter, and a lateral path along the buried oxide/SOI interface, as shown in Figure 3. In particular the applied substrate voltage V_S in fully depleted devices has a marked impact on the electric field inside the device, as explained in [15] and [16]. The change in the electric field alters the current flow within the collector, affecting significantly f_T, f_{max}, collector resistance (R_C), and avalanche multiplication [16].

The collector doping of a fully depleted device is carefully chosen so that when the substrate is floating or grounded, the built-in voltage is enough for the space charge region to extend in the whole collector area. However, the application of a positive substrate voltage V_S creates an accumulation layer at the silicon-on-insulator/Buried Oxide (SOI/BOX) interface as confirmed by the TCAD simulation of the electron density displayed in Figure 4 [16]. The accumulation layer acts as a low resistivity path to the top collector contact, creating a new preferential path for the carriers, as shown in Figure 5: when the substrate is grounded the current flows in the center of the SOI layer while at high substrate bias

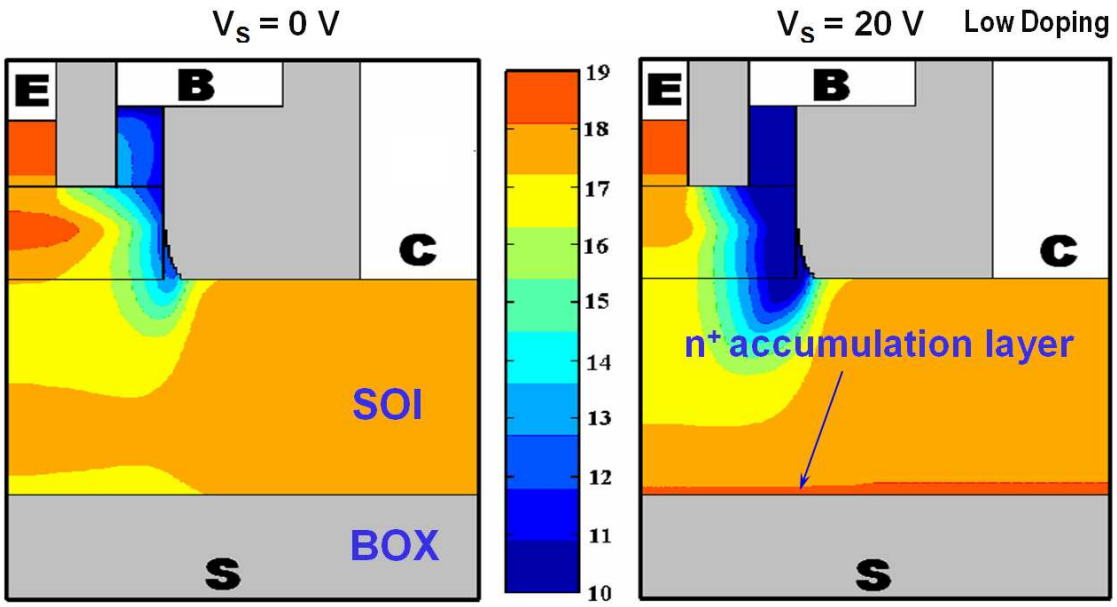


Figure 4: TCAD simulations of the electron density for a fully depleted HBT-on-SOI structure at a substrate voltage of $V_S = 0$ V and of $V_S = 20$ V. After [16]

the current flow occurs in proximity of the SOI/BOX interface. Thus, a positive substrate bias reduces the collector resistance R_C and hence the quasi-saturation effect — a forward biasing of the CB junction caused by the voltage drop on R_C [16].

It should also be noted that V_S deeply affects impact ionization in the device and hence M-1 — the avalanche multiplication factor. As shown in Figure 6, M-1 changes shape and increases significantly with V_S. At low V_S, V_{CB} completely depletes the collector and M-1 consequently saturates because the electric field is effectively pinned. This corresponds in Figure 6 to the $V_S = 0$ V curve, which shows little change in M-1 until V_{CB} surpasses 4 V because the collector is fully depleted. Any increase of V_{CB} will not change the voltage drop in the vertical path under the emitter. The excess voltage drop will fall across the lateral path and will contribute at large V_{CB} to the increase in M-1. This is confirmed by the TCAD simulations of impact ionization shown in Figure 7, which clearly display that the peak of impact ionization lies in the lateral path for $V_S = 0$ V.

However, when V_S is increased the electron accumulation layer forms, altering the potential in the collector and greatly reducing the voltage at the SOI/BOX interface. Most of the externally applied V_{CB} voltage will fall on the vertical path, leading to an increase of the

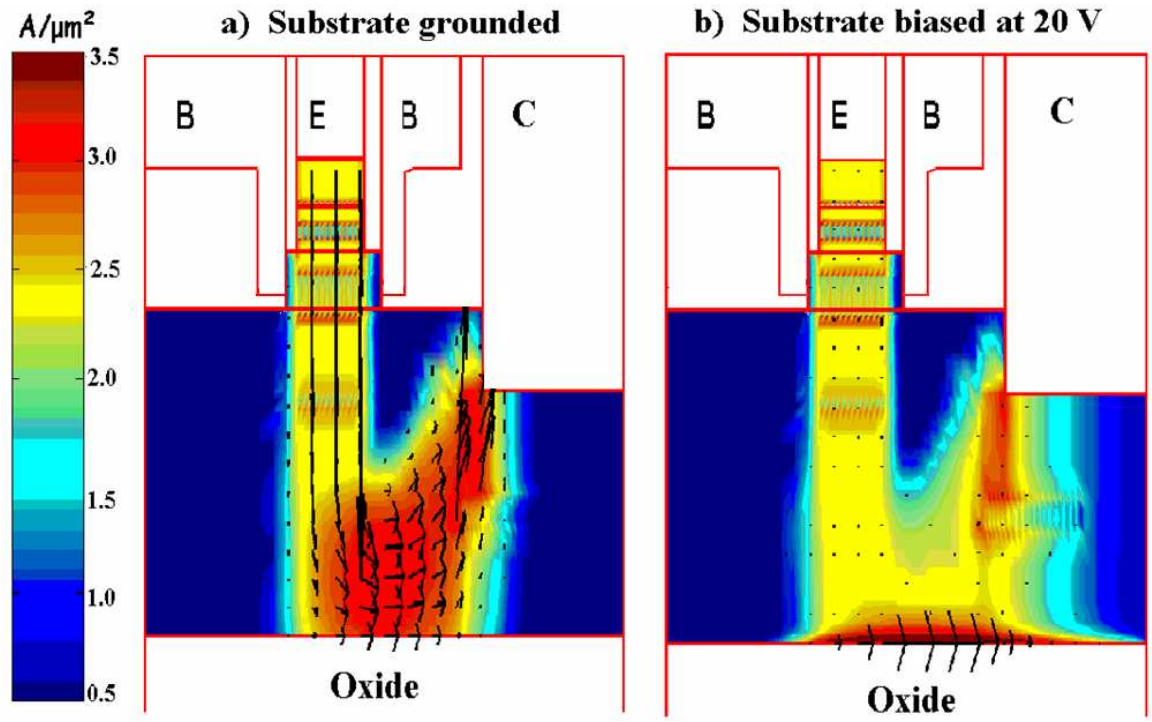


Figure 5: TCAD simulations of the current flow for a fully depleted HBT-on-SOI structure at a substrate voltage of $V_S = 0$ V and of $V_S = 20$ V. After [16]

electric field and consequently M-1 in the region directly under the emitter, as confirmed by Figure 7. This electrical field configuration is similar to the one of a conventional bulk (vertical) device. Not surprisingly, the M-1 curve for $V_S = 0$ V in Figure 6 closely resembles the one of a bulk device.

Also, the *ac* performance of SiGe HBTs-on-SOI is affected by the substrate effect. As shown in Figure 7, both f_T and f_{max} increase significantly with V_S because the substrate bias alters the electric fields inside the device, retarding the Kirk effect [18]. Interestingly, exposure to proton radiation also significantly *improves* f_T and f_{max}, as shown in Figure 8. This is consistent with previous findings because the positive charge created by radiation at the SOI/BOX interface is electrically equivalent to a higher substrate voltage. Obviously even an *enhancement* of *ac* performance can be a reliability issue for circuits operating in a radiation environment since it may cause malfunctions, suboptimal impedance matching, drift of bias points and increase in power consumption.

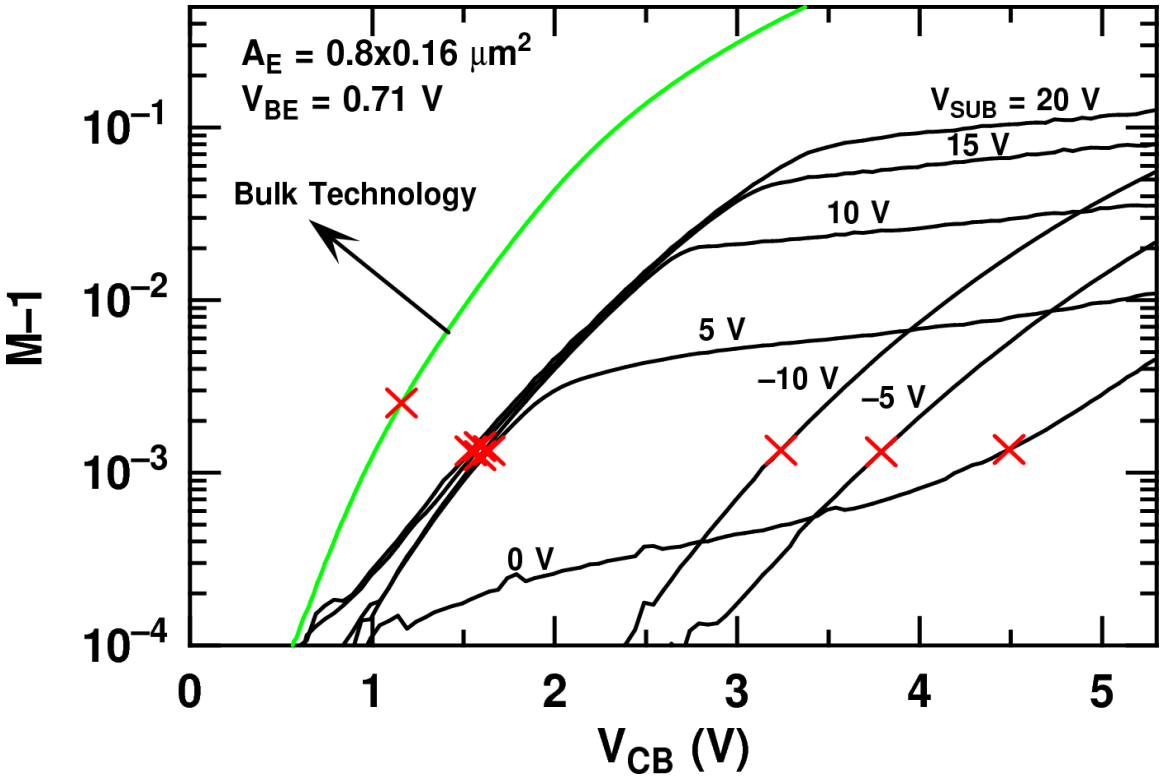


Figure 6: M-1 for a fully depleted HBT-on-SOI device at increasing substrate voltages (from V_S = -10 V to V_S = 20 V). The crosses indicate the base current reversal points. For comparison, the M-1 of a comparable bulk (vertical) SiGe HBT is shown. After [16]

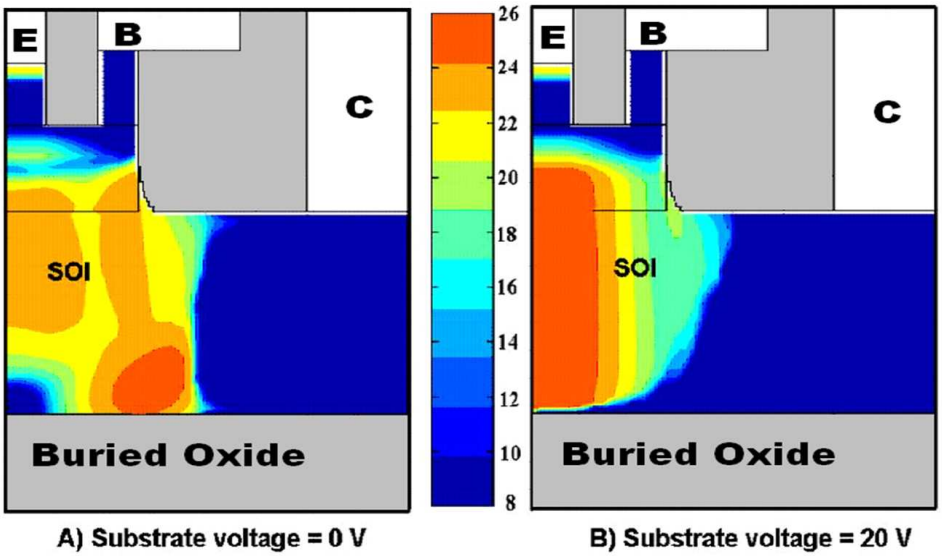


Figure 7: TCAD simulations of the avalanche multiplication coefficient for a fully depleted HBT-on-SOI structure at a substrate voltage of V_S = 0 V and of V_S = 20 V. After [16]

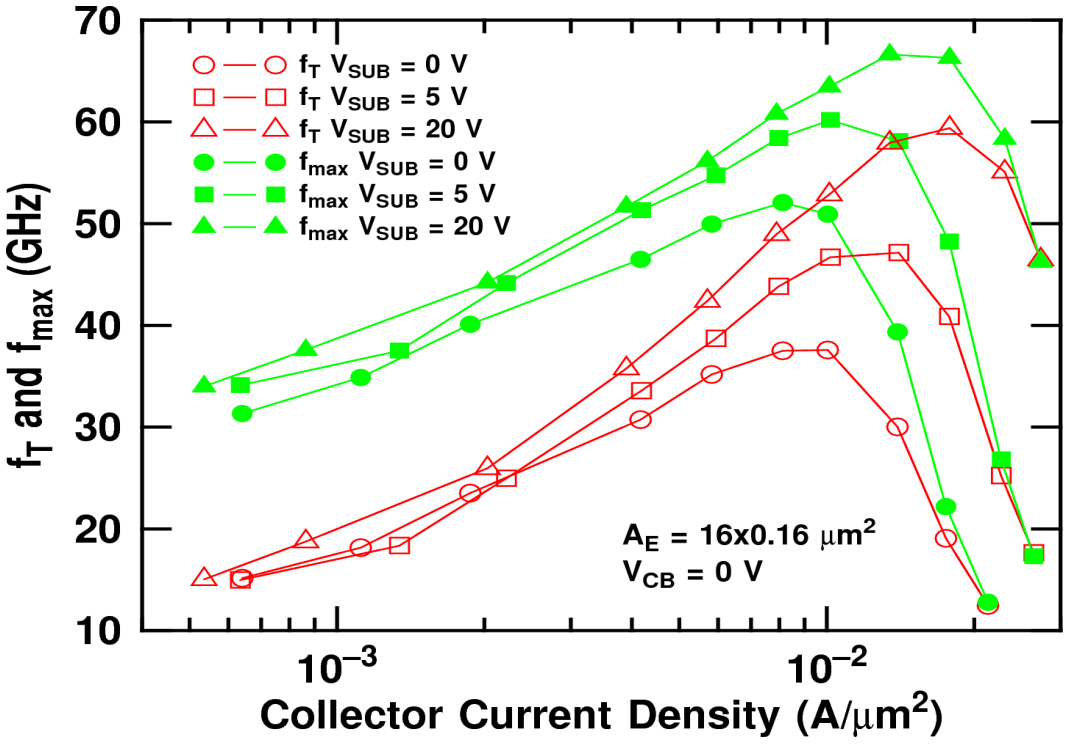


Figure 8: f_T and f_{max} versus collector current density for a fully depleted HBT-on-SOI structure at a substrate voltage of $V_S = 0$ V, $V_S = 5$ V, and of $V_S = 20$ V. After [18].

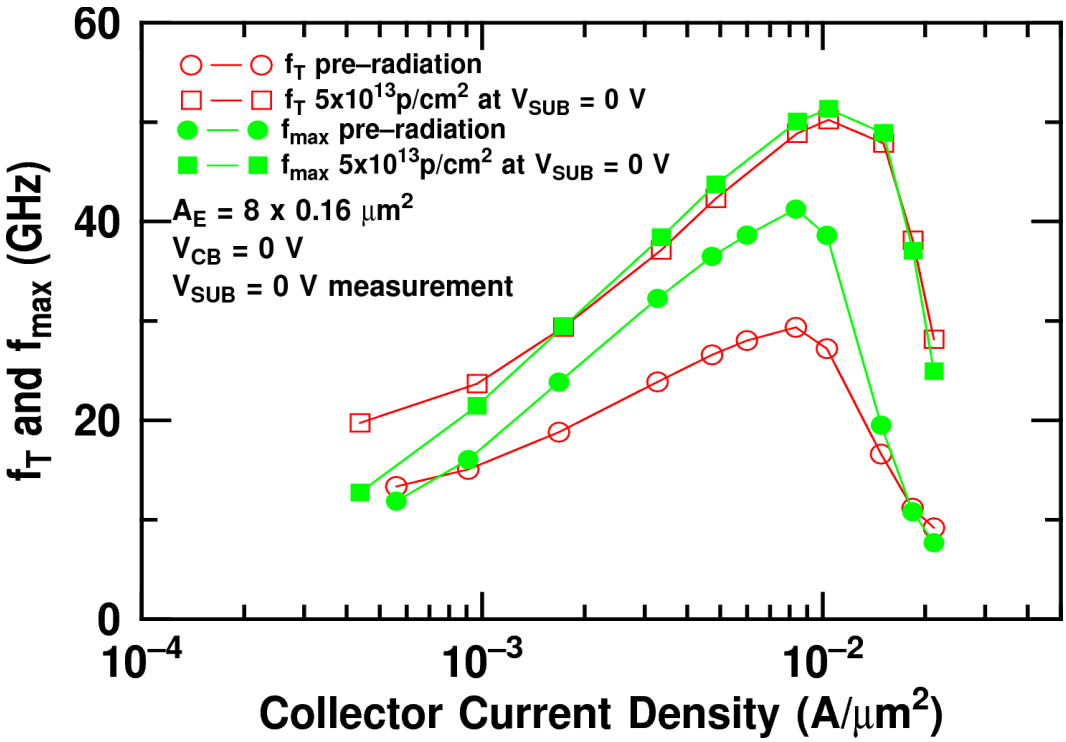


Figure 9: f_T and f_{max} versus collector current density for a fully depleted HBT-on-SOI structure with increasing proton fluence. After [18].

Table 3: Figures of merit of SiGe HBTs on thin-film SOI with C_BE^BC layout. After [4].

Figure of Merit	(300 K)
β	390
f_T (V_{CB}=0.5 V)	35 GHz
f_{max} (V_{CB}=0.5 V)	134 GHz
B_{VCEO}	5.4 V
B_{VCBO}	15 V

1.4.3 SiGe HBTs on thin-film SOI with C_BE^BC layout

Although the vertical cross-section of the devices discussed in this section is very similar to conventional SiGe HBTs-on-SOI described in section 1.4.2, the top layout is altered to optimize the *ac* performance, , as shown in the inset of Figure 10 [3]

In any HBTs-on-SOI, the emitter-collector distance limits the *ac* performance of the transistor because of the length of the drift path in the case of the fully depleted device or because of the $R \times C_{CJC}$ delay time in the case of the partially depleted device [15][4].

To minimize the *ac* performance degradation caused by the absence of the true sub-collector, these devices employ the novel C_BE^BC layout, reducing the distance L_C between emitter and collector (as shown in Figure 10) down to 0.4 μm [4][3]. This optimized layout, however, significantly alters the current flow inside the device. Interestingly, in a bulk SiGe HBT the current flow is essentially 1-D, vertical directly under the emitter, while in a SiGe HBT-on-SOI with a conventional CBEBC layout (with the base contacts between the emitter and the collector contacts) the current flow is 2-D, initially vertical under the emitter and then horizontal along the SOI/BOX interface [15]. Conversely, the current flow in a SiGe HBT-on-SOI with C_BE^BC layout is intrinsically 3-D in nature.

These HBTs are developed with the addition of only 4-mask layers on top of a 130 nm SOI CMOS process, and feature a 150 nm SOI layer on top of a 400 nm SiO_2 buried oxide (BOX), as shown in Figure 10 [3]. The layout optimization results in the figures of merit shown in Table 3.

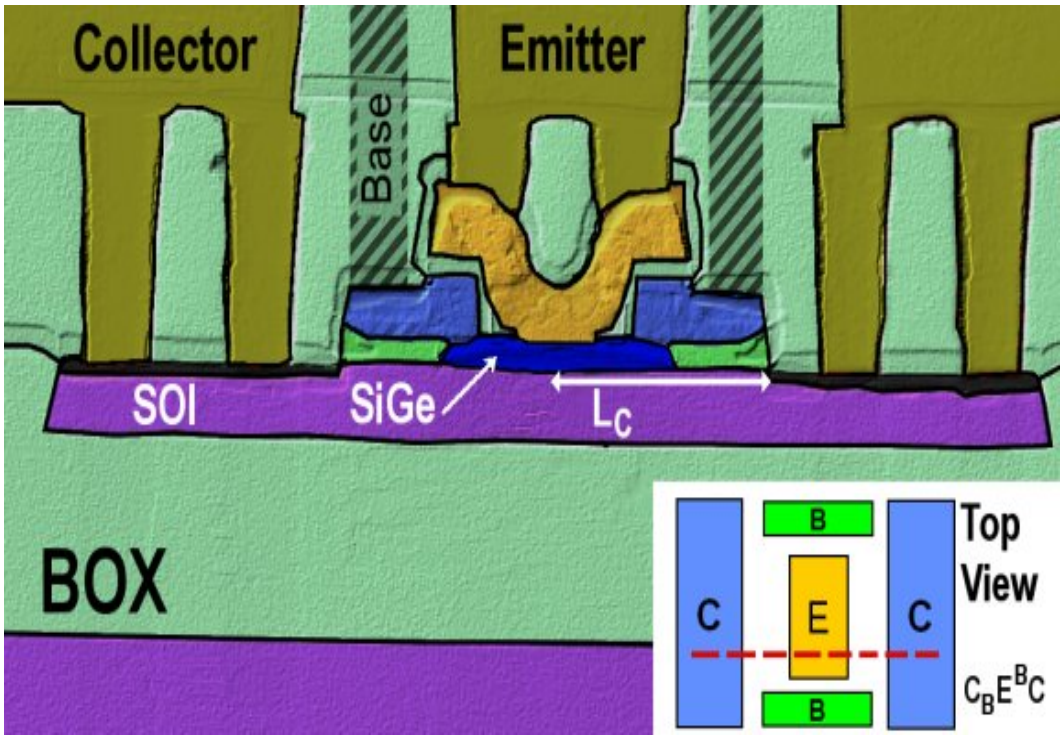


Figure 10: Cross-sectional TEM micrograph of the SiGe HBT-on-SOI with C_BE^BC layout, from [4].

CHAPTER II

DEVICE SIMULATION

In-depth understanding of modern semiconductor devices invariably requires the use of numerical analysis because often analytical techniques are limited to 1-D problems and require unrealistic assumption and approximations to reach a closed-form solution. In contrast, the numerical techniques known as "Technology Computer Assisted Design" (TCAD) can solve 2-D and 3-D non-homogeneous problems even when physical phenomena such as lattice heating, carrier drift and diffusion are tightly coupled. Since advanced numerical techniques are frequently used in the present work, this chapter introduces the fundamental concepts of device simulation. Then, the issues encountered in simulating devices operating in extreme environments are described. Finally, particular problems such as device optimization or simulation of radiation phenomena often require custom device simulation or post-processing techniques. An interesting example of a custom device simulation technique — the 3-D regional analysis of transit time — is presented. This technique is used to identify the regions of device that limit the *ac* performance at room temperature and it can easily be used to optimize the performance of a device operating in extreme environments.

2.1 Fundamentals of Device Simulation

TCAD is used to solve a numerical problem, defined as the set of equations describing semiconductor physics, the physical domain of simulation, and the boundary conditions at the extremes of the domain. The domain of simulation is approximated by a "grid" or "mesh" of connected elements: a 2-D domain is usually divided into triangles or rectangles and a 3-D domain into tetrahedra or prisms. In general, a finer grid with a larger number of elements produces a more accurate solution of the problem.

The set of equations most commonly used is the so-called "Hydrodynamic Transport Model" and comprises of the Poisson equation 1, the electron and hole continuity equations 2, the hole and electron current density equations 3, and the energy transport equations 4

[37][68].

$$\nabla \cdot \varepsilon \nabla \phi = -q\left(p - n + N_D - N_A\right) - \rho_{trap}, \tag{1}$$

$$\begin{aligned} \nabla \cdot \vec{J}_n &= qR_{net} + q\frac{\partial n}{\partial t}, \\ -\nabla \cdot \vec{J}_p &= qR_{net} + q\frac{\partial p}{\partial t}, \end{aligned} \tag{2}$$

$$\begin{aligned} \vec{J}_n &= q\mu_n \left(n\nabla E_C + kT_n\nabla n + f_n^{td}k_n\nabla T_n - \tfrac{3}{2}nkT_n\nabla ln\left(m_n\right)\right), \\ \vec{J}_p &= q\mu_p \left(n\nabla E_V - kT_p\nabla p - f_p^{td}k_p\nabla T_p - \tfrac{3}{2}pkT_p\nabla ln\left(m_p\right)\right), \end{aligned} \tag{3}$$

$$\begin{aligned} \vec{S}_n &= -\tfrac{5r_n}{2}\left(\tfrac{kT_n}{q}\vec{J}_n + f_n^{hf}\kappa_n\nabla T_n\right), \\ \vec{S}_p &= -\tfrac{5r_p}{2}\left(\tfrac{-kT_p}{q}\vec{J}_p + f_p^{hf}\kappa_p\nabla T_p\right), \\ \vec{S}_L &= -\kappa_L\nabla T_L, \end{aligned} \tag{4}$$

The unknowns n, p, ϕ, T_n, T_p, and T_L are respectively the electron and hole density, the electrostatic potential, the electron and hole carrier temperatures, and the lattice temperature. The other quantities are parameters function of the material, doping and of the unknowns.

The numerical simulator performs *dc*, *ac* and transient simulations of semiconductor devices and circuits, solving for the unknowns.

2.2 Use of TCAD in Simulations of Extreme Environments

Reaching the numerical solution of semiconductor problems even at room temperature is complex: the problems are intrinsically "ill-conditioned" because the electron and hole carrier concentrations n and p typically vary more ten orders of magnitude across a fraction of a micron [50]. This produces numerical instabilities that often prevent the solver to converge to a solution. Moreover, a typical 2-D device simulation typically features a grid with a number of elements between 50,000 and 100,000 resulting in very long computation times.

Simulation of devices operating in extreme environments can be even more challenging [21]. For example, simulations of transistors operating at cryogenic temperatures exhibit well-know convergence problems. A rule of thumb in creating a well-behaved grid is to ensure that the voltage drop at the opposite side of each element is small compared to kT/q. As the temperature decreases this rule is often violated to ensure that the number of elements doesn't become intractably large, resulting in degraded convergence [21].

Radiation studies are also plagued by numerical problems. Transient TCAD simulations can be used to reproduce total ionizing dose phenomena. Electron-hole pairs are deposited in the SiO_2 oxides according to equations 5, where D is the dose rate, g_0 is the generation rate of electron-hole pairs, and E_0 and E_1 account for the electric field-dependent yield [68]. Then, the Drift-Diffusion or the Hydrodynamic equations are solved both in silicon and in SiO_2 in order to evaluate the spatial distribution of positive charge trapped in the oxides. However, since the energy gap of SiO_2 is much larger than Si, the value of the holes quasi-Fermi levels will be very close to numerical precision and therefore convergence will be extremely slow.

$$\begin{aligned} G_r &= g_0 D Y(F) \\ Y(F) &= \left(\frac{F+E_0}{F+E_1}\right)^m \end{aligned} \tag{5}$$

TCAD simulations can also be used to study single event upset phenomena. In this case, the electron hole-pairs are deposited in the silicon volume and they are collected at the electrodes, generating transient current pulses. Since the SEU problem is intrinsically three-dimensional, accurate solutions require large 3-D grids which results in very long computation times.

In some cases it is possible to significantly shorten simulation times by using a quasi 3-D approximation. In this case the semiconductor transport equations are solved in the cylindrical coordinate system assuming rotational symmetry, as shown in Figure 11 [50]. Thus, the exact solution to the 3-D cylindrical problem is obtained at a 2-D computational cost.

The shortcomings of the quasi 3-D technique are obvious. First, it cannot be used for

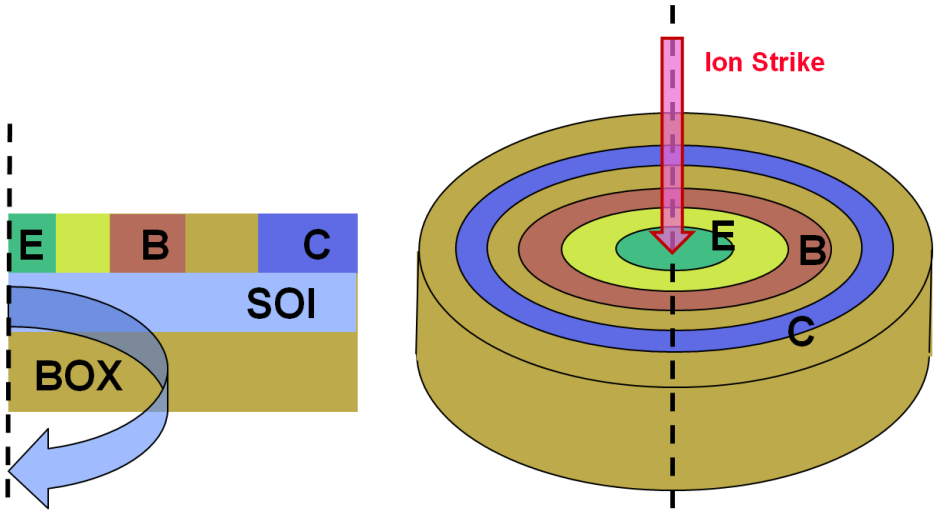


Figure 11: Schematic representation of a quasi 3-D simulation grid of a transistor with annular layout.

devices with complex layouts. Moreover, it can only accurately model ion strikes along the axis of symmetry. An ion strike outside the symmetry axis becomes a "ring" of ion strikes because of the use of rotational symmetry, as shown in Figure 12. The only way to correctly simulate arbitrary ion strikes is to use a 3-D grid.

2.3 3-D Regional Transit Time Analysis of SiGe HBTs on thin-film SOI

As mentioned in the previous section, 2-D TCAD simulation cannot be used for a number of analyses of devices with complex layouts, such as the one described in Section 1.4.3 [3]. In particular, *ac* analysis and optimization cannot be performed on this device using the conventional 2-D TCAD simulation approaches described in [72].

In this section the 1-D regional transit time technique from [76][80] is been extended to 3-D in order to better understand the impact of advanced layouts on device *ac* performance.

3-D device simulations of the SiGe HBT-on-SOI with $C_B E^B C$ layout have been performed with the NanoTCAD package [52], using a binary tree mesh with local refinement in the vicinity of the emitter-base (EB) and collector-base (CB) junctions as well as the SOI/BOX interface. The doping profiles obtained from secondary ion mass spectroscopy (SIMS) data are accurately reproduced with a truncated series of Gaussian functions. The

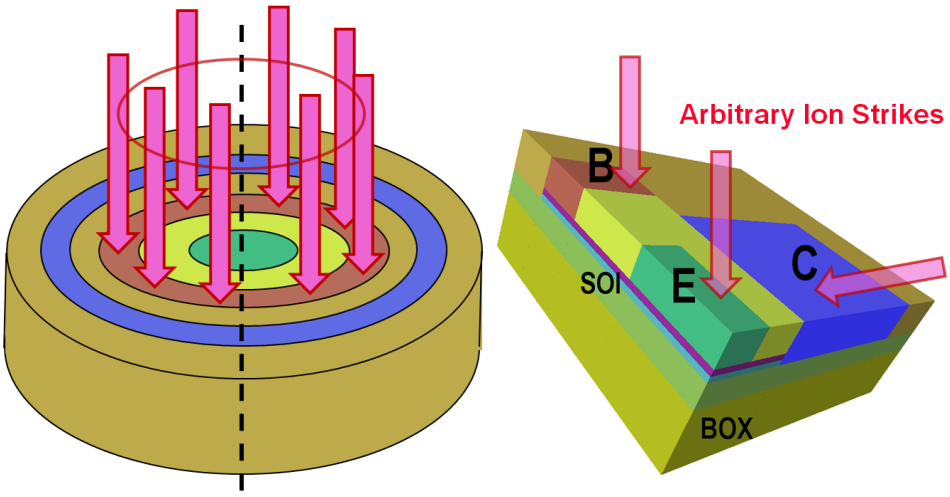


Figure 12: The schematic representation on the left illustrates the issues of simulating an arbitrary ion strike on a quasi 3-D simulation grid. Conversely, the 3-D grid shown on the right can be used to simulate arbitrary strikes.

semiconductor physics models employed include doping-dependent carrier lifetimes, SRH and Auger recombination, and mobility models featuring doping, electric field and carrier-carrier scattering dependence. The doping profiles were further calibrated to accurately simulate both forward and inverse Gummel characteristics, as shown by the close match between measured and simulated forward current gain β in Figure 13. The simulated cutoff frequency f_T, also displayed in Figure 13, is derived from the emitter-collector transit time τ_{ec} according to the expression $f_T = 1/2\pi_{ec}$.

The emitter-collector transit time τ_{ec} is calculated in the quasi-static approximation by performing a *dc* sweep on a discrete set of emitter-base voltages V_{BE}. The V_{BC} bias across the base-collector junction can be arbitrarily chosen to match measurement conditions. For each emitter-base voltage V_{BE} a small-signal perturbation ΔV of 1 mV – small enough for the quasi-static approximation to hold – is applied, resulting in an increase of the collector current I_C and in perturbations of the electron charge density n [76]. This approach enables to calculate f_T with a dramatic reduction in computation time with respect to a full *ac* simulation, which requires the estimation of the linearized admittance matrix $Y = G + j2\pi fC$ at each voltage step V_{BE} and at each frequency point f. Conversely, the transit time technique used here requires little more than the time needed for a single *dc*

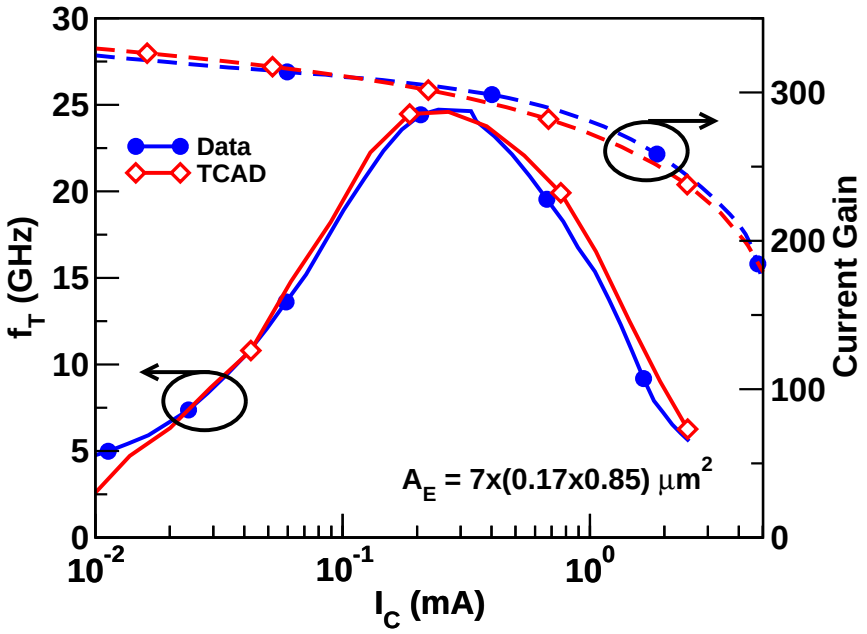


Figure 13: Simulated cut-off frequency f_T and current gain β compared to measured data for a SiGe HBT-on-SOI with emitter area A_E of $7\times(0.17\times0.85)$ μm^2.

sweep on the V_{BE} voltages. Since the perturbation ΔV is very small, the solutions for the voltage steps V_{BE} + ΔV converge in only a few iterations. This represents a dramatic advantage because the number of mesh elements in a 3-D simulation is very large (often more than 100,000) and consequently the computation time for a full *ac* simulation is extremely long. In addition, if V_{BC} is set to 0 V it is possible to simultaneously estimate the current gain β and the cutoff frequency f_T with the same *dc* simulation, significantly reducing device calibration and optimization times. However, a more time-consuming *ac* simulation provides the full set of s-parameters, enabling to extract other important figures of merit such as f_{max}. The emitter-to-collector transit time τ_{ec} is obtained by integrating over the volume of the device the ratio of the perturbations of electron charge and collector current caused by ΔV according to Equation 6. Obviously the challenge of extending the 1-D transit time analysis to 3-D lies in the numerical integration of Equation 6.

$$\tau_{ec} = \frac{\Delta Q}{\Delta I_C} = \iiint \frac{q\Delta n(\Delta\nu)}{\Delta I_C(\Delta\nu)} dxdydz, \tag{6}$$

At first, the NanoTCAD simulator processes the binary tree mesh representing the transistor geometry, the equations describing the physical problem and the boundary conditions and then solves the differential problem for the value of the electrostatic potential V, the electron density n, and the hole density p on the nodes of the mesh. The integrand of Equation 6 on the nodes of the mesh is obtained by simply subtracting the electron density n at voltage V_{BE} from n at voltage $V_{BE} + \Delta V$ and then multiplying by the quantity $q/\Delta I_C$. Next, the binary tree mesh structure is converted to a more simple tetrahedral mesh structure, as shown schematically in Figure 14. The binary tree mesh structure used by NanoTCAD is comprised of hexahedral elements (also known as "bricks") with orthogonal faces. As shown in Figure 14 a), some elements may feature extra points in addition to the 8 canonical vertexes because they are adjacent to "bricks" of smaller size. Once the vertices of the element are correctly identified, as shown in Figure 14 b), the hexahedron ABCDEFGH is split into 5 tetrahedra (ABCF, ADFH, AEGH, ACFH, and CGFH), as shown in Figure 14 c) and Figure 14 d). This mesh simplification permits the use of more convenient linear tetrahedral integration rules, as described in Equations 7.

$$\begin{aligned} &\iiint f(x,y,z)dxdydz \approx \sum_E \sum_{i=1}^{4} w_{i,E}\, f(x_i,y_i,z_i)|_E\,, \\ &w_{i,E} = \tfrac{1}{4} V_E, \end{aligned} \tag{7}$$

The contribution of each tetrahedral element E is evaluated using a first-order quadrature formula with equal weights (equal to 1/4 of the volume of the tetrahedron E) and nodes coinciding with the vertices of the tetrahedron. However, the most valuable result of this 3-D technique is not simply the evaluation of τ_{ec} and f_T (clearly useful) but especially the ability to identify the contributions of each region of the device to the total transit time.

Before introducing the regional analysis of transit time, it is necessary to understand the physical behavior of the SiGe HBT-on-SOI and in particular the current flow inside the device. A peculiarity of SiGe HBTs-on-SOI with a fully depleted collector is that substrate

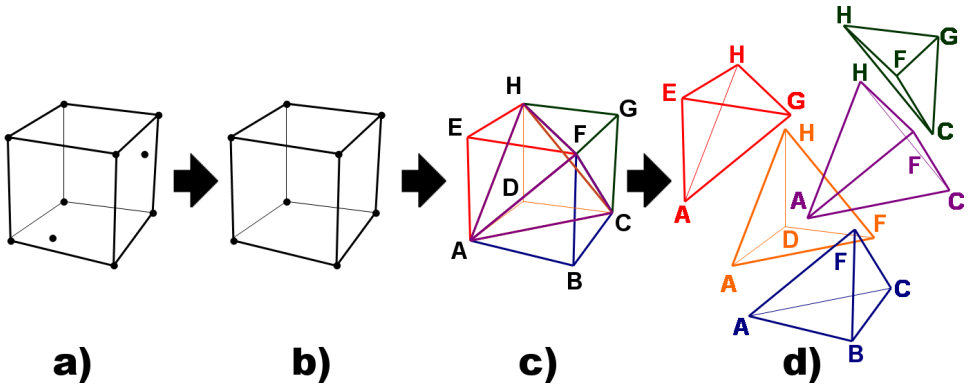


Figure 14: Graphical representation of the conversion from binary tree mesh to tetrahedral mesh.

bias V_S creates an electron accumulation layer at the SOI/BOX interface, providing a low resistivity path to the top collector contact, significantly reducing the collector resistance R_C and increasing f_T and f_{max} , as demonstrated in previous studies on devices with the conventional CBEBC layout [18]. Figure 15 and Figure 16 compare the effects of V_S on the current density in an HBT with $C_B E^B C$ layout biased at peak f_T collector current, plotting four 3-D isosurfaces corresponding to increasing $|J_N|$. At $V_S = 0$ V most of the current flow in the z direction occurs in the center of the SOI layer, as shown by the black arrow in Figure 15. Conversely, the current flow in the xy plane is confined to a narrow region between the emitter and the collector contact. However, at $V_S = 20$ V the accumulation layer results in a downward shift in the z direction of the current flow, closer to the SOI/BOX interface, as shown in Figure 16. Interestingly, the arrow in Figure 16 shows that the increased vertical electric field results also in a much larger spread of the current on the xy plane.

While isosurfaces are a great tool for obtaining an overall view of the variation of a scalar quantity in a three-dimensional space, visualization aids such as streamlines and 2-D cuts can provide a more focused insight on the device behavior, as shown in Figure 17 and Figure 18. In this situation the streamlines Σ represent the locus of points originating from the emitter contact and tangent to the vector field and help one visualize the path of the current flowing from emitter to collector. They are calculated through the simple Forward Euler integration method described in Equations 8.

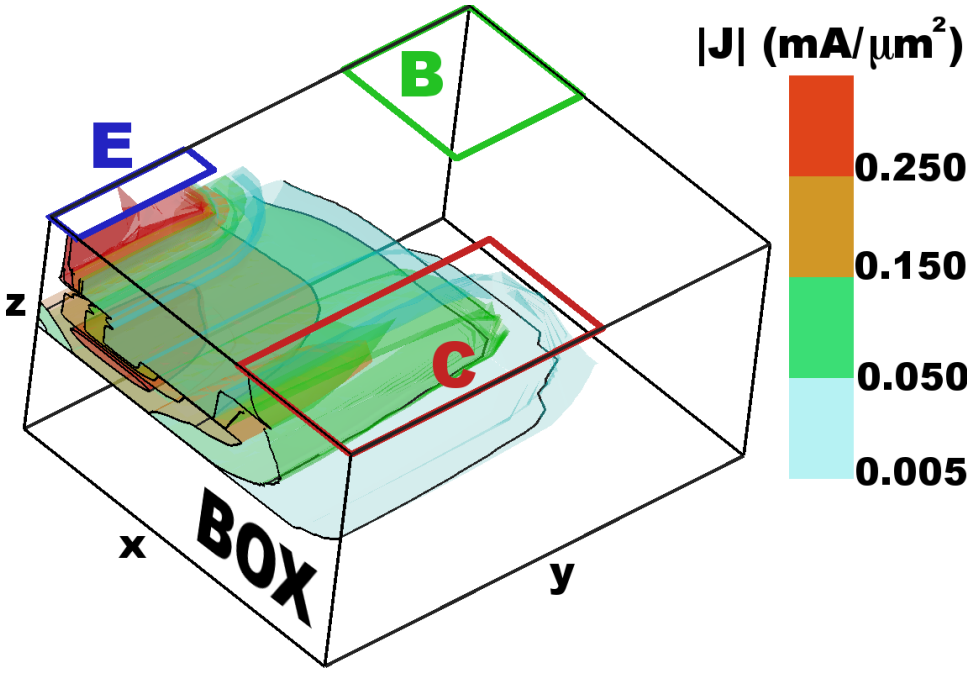


Figure 15: Isosurfaces of the electron current density $|J_N|$ for $V_S = 0$ V. The isosurfaces surround the volume in which $|J_N|$ is respectively greater than 0.25, 0.15, 0.05, and 0.005 $mA/\mu m^2$, as indicated by the legend.

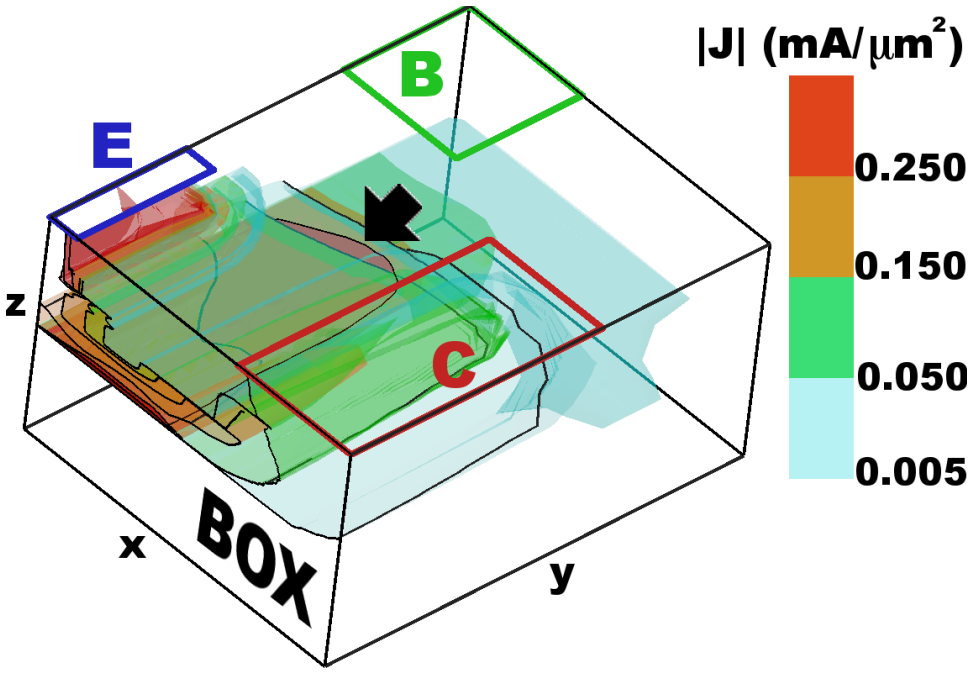


Figure 16: Isosurfaces of the electron current density $|J_N|$ for $V_S = 20$ V. The isosurfaces surround the volume in which $|J_N|$ is respectively greater than 0.25, 0.15, 0.05, and 0.005 $mA/\mu m^2$, as indicated by the legend.

$$\begin{aligned}
&\vec{p}(S) = x(S)\vec{i}_x + y(S)\vec{i}_y + z(S)\vec{i}_z, \\
&\vec{p}(S+dS) = \vec{p}(S) + \frac{\vec{J}_N}{|\vec{J}_N|} \cdot \left(dx\vec{i}_x + dy\vec{i}_y + dz\vec{i}_z \right),
\end{aligned} \tag{8}$$

Figure 17 and Figure 18 also show 2-D cuts of $|J_N|$ on the planes α, β, and γ parallel to the xz plane. The streamlines and the 2-D cut on plane α of Figure 17 suggest that at $V_S = 0$ V most of the current flows from the side of the emitter facing the collector contact and through the center of the SOI layer. The contribution of current flow from the center and from the side of the emitter facing the base is smaller because of the larger resistance encountered along these current paths. The 2-D cuts on planes β and γ show that the current flow in the xz plane widens as it approaches the high doping collector contact region. Conversely, Figure 18 shows that the streamlines noticeably shift downward in the z direction as V_S increases. In addition, the arrows in the 2-D cuts on planes α and β indicate how the current flow is spreading widely on the xy plane at the SOI/BOX interface, in accordance with Figure 16. The current flow becomes more uniform on plane γ because of the high doping of the collector contact region. Figure 18 also shows that the current at $V_S = 20$ V flows mainly from the center of the emitter contact towards the accumulation layer, rather than from the edges, in contrast with the behavior at $V_S = 0$ V.

Figure 19 introduces the plot of accumulated delay in the device, described in [72][76][80][60], which is a very powerful tool for analyzing the contribution of each region to τ_{ec} and for optimizing overall device performance. The line integral of $q\Delta n/\Delta J_C$ is evaluated along the streamlines Σ, according to Equation 9, yielding the accumulated delay D.

$$D\left(S\right) = \frac{q}{\Delta I_C} \int_0^S \Delta n \left(x(s), y(s), z(s)\right)|_\Sigma \, ds, \tag{9}$$

In the 1-D analysis the final value of D is obviously equal to τ_{ec} because there is only one streamline which coincides with the entire 1-D simulation domain. While this doesn't apply to the 3-D case because the streamline samples only a small part of the device, D is still a powerful tool for investigating what limits the overall ac performance. The color of the dots in Figure 19 represents the normalized accumulated delay D along the various paths from

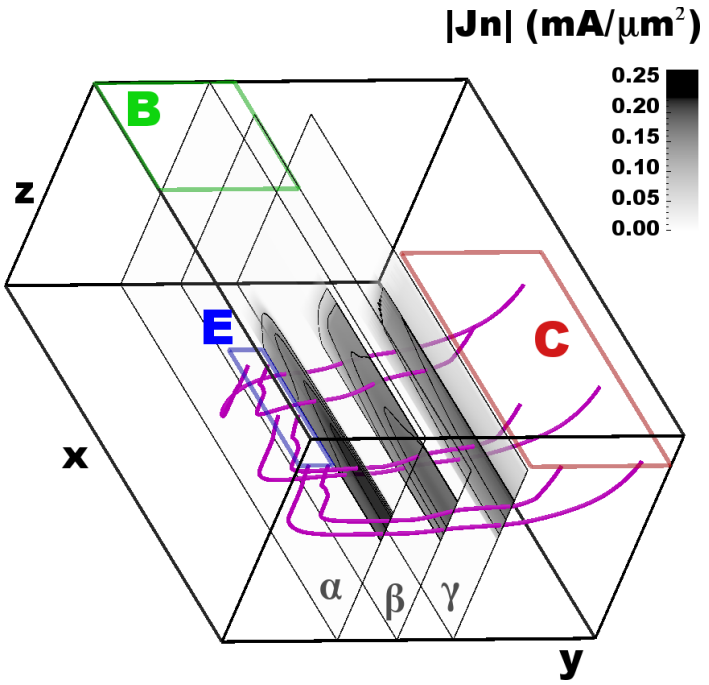


Figure 17: Streamlines and 2-D cuts of the electron current density $|J_N|$ at a substrate voltage $V_S = 0$ V.

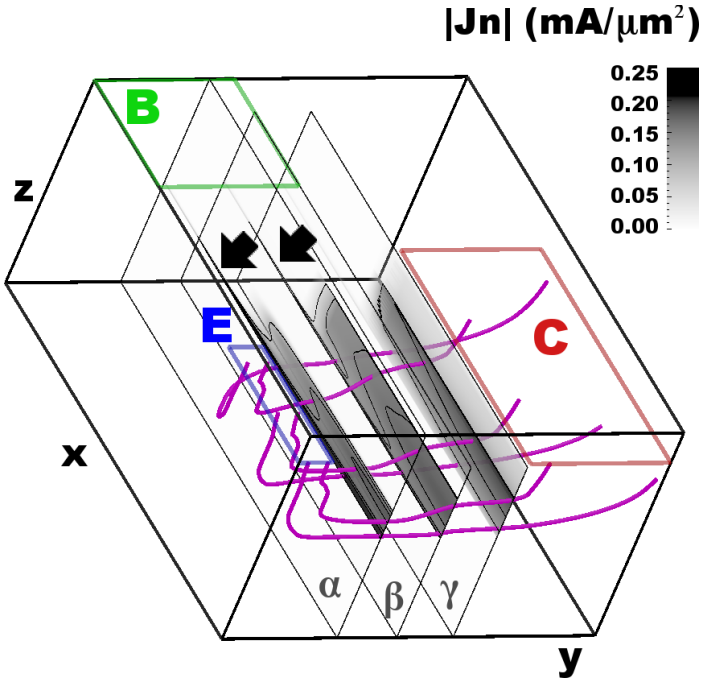


Figure 18: Streamlines and 2-D cuts of the electron current density $|J_N|$ at a substrate voltage $V_S = 20$ V.

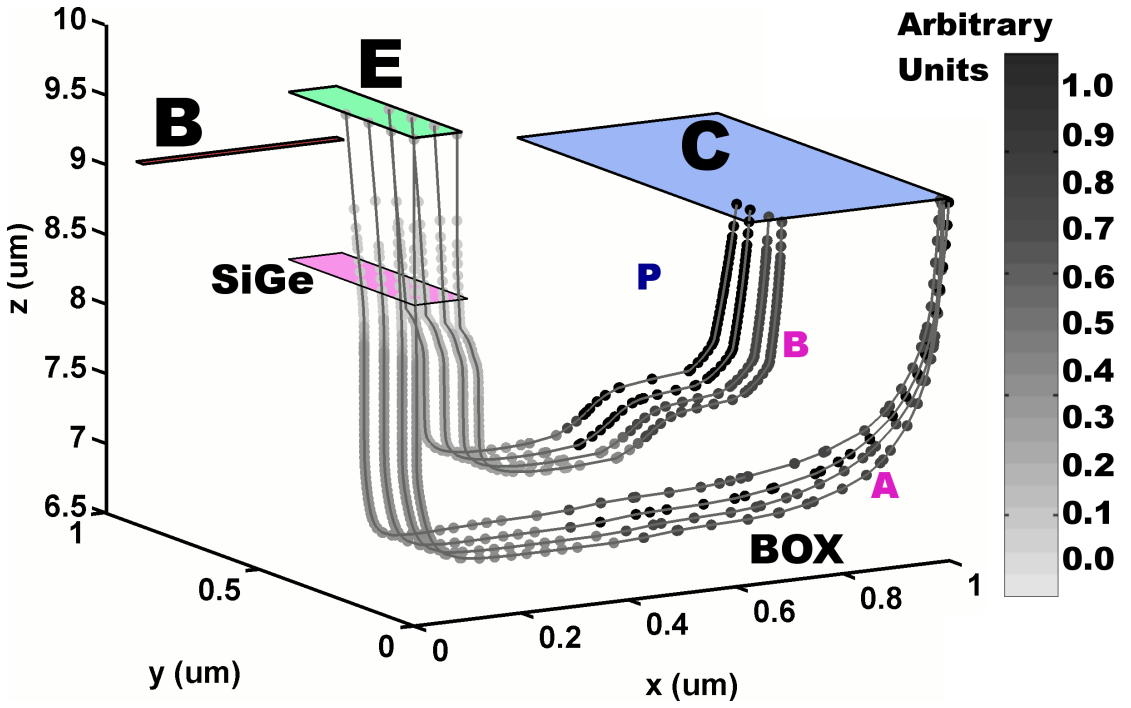


Figure 19: Cumulative transit time τ_{ec} integrated along various current streamlines from emitter to collector.

emitter to collector. To gain more quantitative insight, Figure 20 shows the accumulated delay D calculated along the paths A and B of Figure 19, versus the curvilinear abscissa s, for substrate voltages V_S equal to 0 V and to 20 V. The plot clearly shows how the delays resulting from the EB and CB space charge regions and from the transition between the depleted and neutral collector have the largest impact on τ_{ec} [60]. The increase of f_T with V_S from simulations agrees with measurements.

Finally, Figure 21 and Figure 22 show 2-D cuts of $q\Delta n/\Delta J_C$ on planes yz in the vicinity of the emitter contact (α), of high doping collector contact region (β) and on the plane xy close to the SOI/BOX interface (γ). As expected, the cross-section on plane α shows the delay contributions resulting from the proximity of the EB and CB junctions, while the cross-section on β visualizes delays related to the transition between depleted and neutral collector. In accordance with our previous findings, the value of the quantity $q\Delta n/\Delta J_C$ on plane γ decreases with increasing V_S because of the additional vertical electric field.

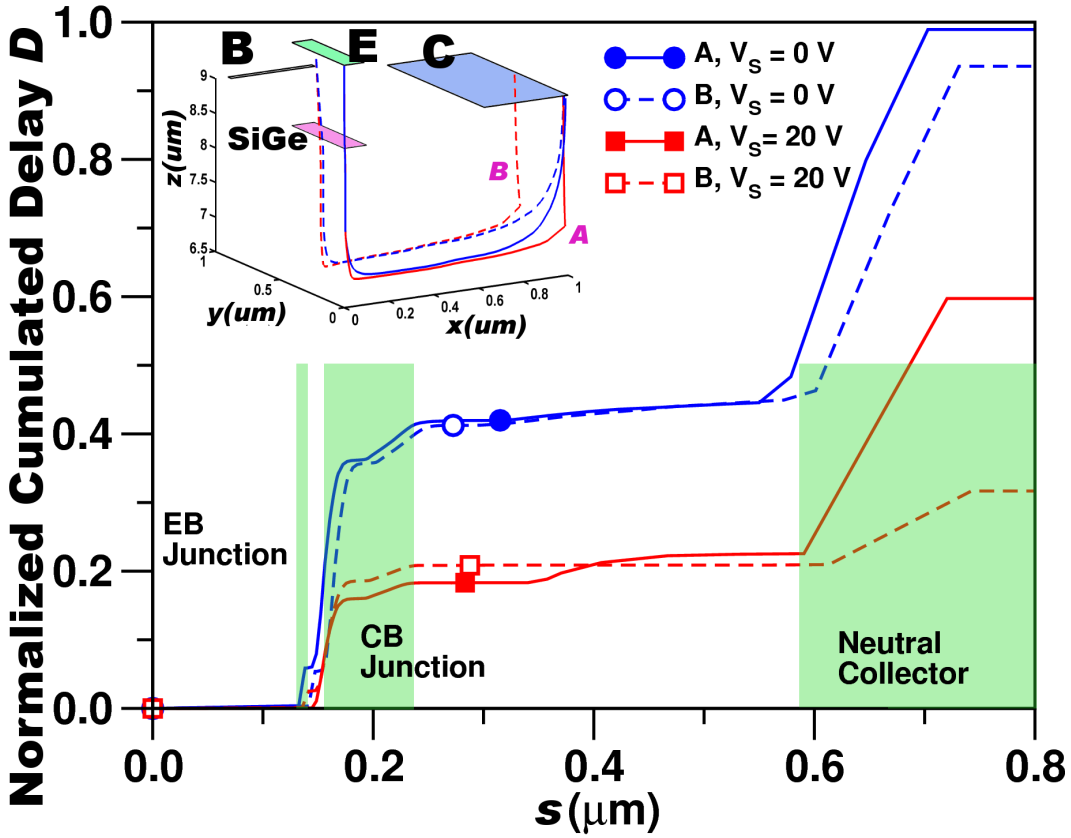


Figure 20: Normalized cumulated delay D along current streamlines A and B at $V_S = 0$ V and $V_S = 20$ V.

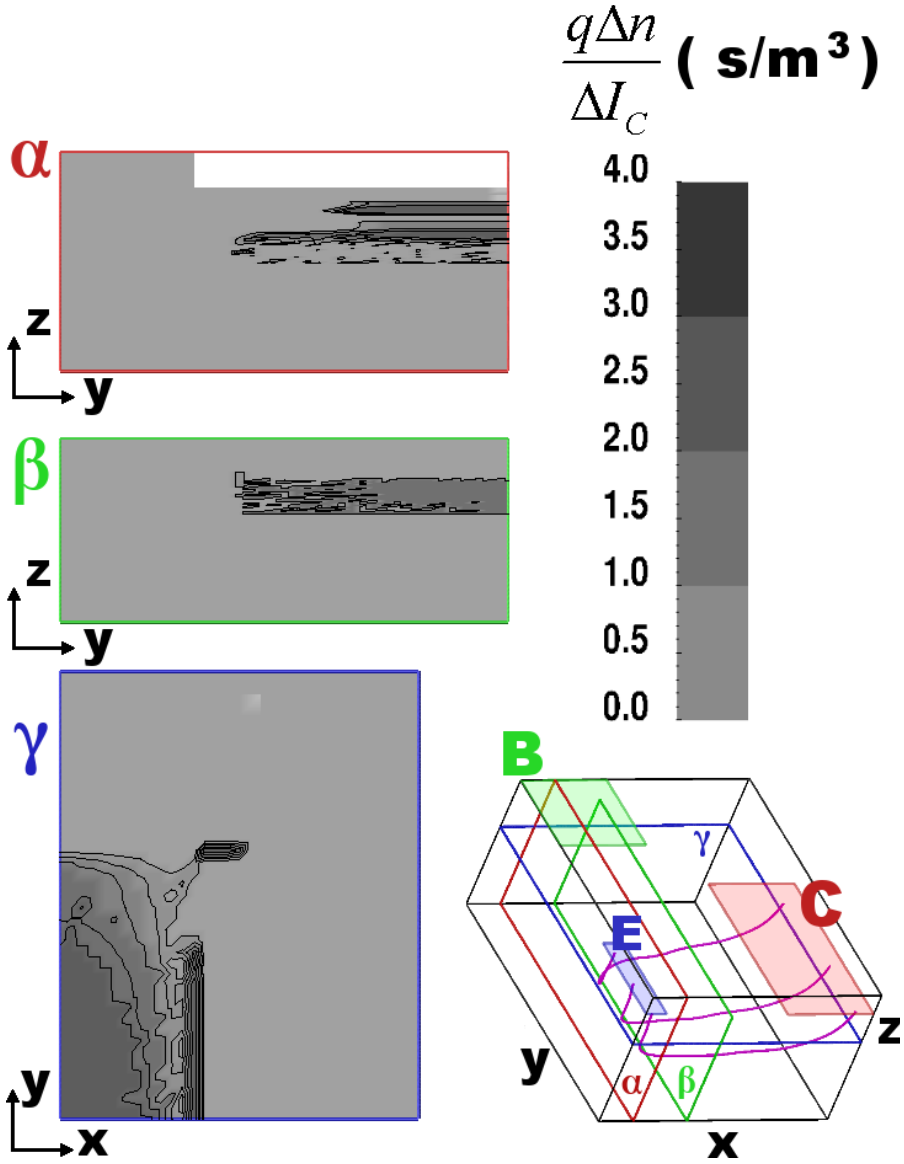


Figure 21: 2-D cuts of $q\Delta n/\Delta J_C$ on planes α, β, and γ for a SiGe HBT-on-SOI biased at peak f_T collector current and $V_S = 0$ V.

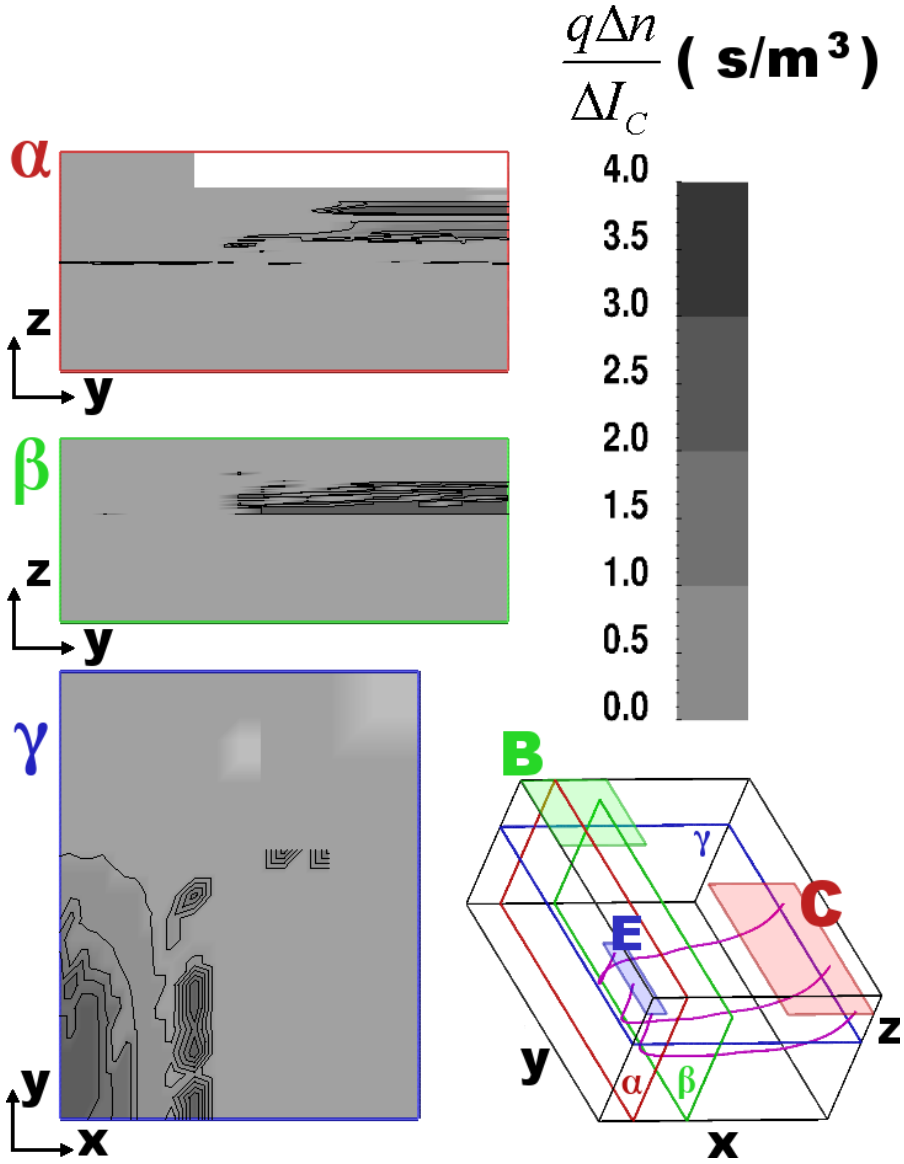


Figure 22: 2-D cuts of $q\Delta n/\Delta J_C$ on planes α, β, and γ for a SiGe HBT-on-SOI biased at peak f_T collector current and $V_S = 20$ V.

To conclude, the technique for the regional analysis of device transit time has been extended to 3-D and used to study a SiGe HBT-on-SOI with novel $C_B E^B C$ layout. The asymmetric device layout results in an intrinsically 3-D current flow so that the analysis and optimization of this transistor requires full 3-D TCAD simulations and advanced visualization techniques. The impact of the various regions of the device on the overall emitter-collector transit time has been studied at different substrate bias conditions.

CHAPTER III

OPERATION AT CRYOGENIC TEMPERATURES

Electronic circuits designed to operate at cryogenic temperatures are presently employed in satellite systems, space exploration, precision instrumentation, detector electronics, and very low noise receivers for astronomy. The volume of these applications is very small compared to the global semiconductor market but this niche fulfills important scientific, commercial, and military needs. Obviously, these circuits rely on high-performance and reliable electron devices and SiGe technology can potentially play a role in this field.

The performance of Si BJTs significantly degrades at cryogenic temperatures: the current gain β and the cutoff frequency f_T decrease and the base resistance increases. Conversely, the bandgap modulation introduced by the presence of germanium in the base has in general a positive impact on the figures of merit of SiGe HBTs operating at low temperatures [23][24].

This chapter covers the experimental studies of cryogenic temperature operation of SiGe HBTs-on-SOI presented in [6] and the analysis of reliability of SiGe HBTs-on-SOI at room and cryogenic temperature discussed in [13].

3.1 Cryogenic Temperature Operation of SiGe HBTs-on-SOI

This section describes how the performance of SiGe HBTs fabricated on SOI has been measured at cryogenic temperatures down to 20 K for the first time [6]. The device investigated is described in Section 1.4.2 and features a fully depleted collector with an average doping $N_C = 1.5 \times 10^{17} cm^{-3}$ and an emitter of area A_E of $0.16 \times 0.8\ \mu m^2$.

The devices were wirebonded to a dual-in-line package and placed in a custom Advanced Research Systems cryogenic test station with a Lakeshore 331 Temperature Controller. An Agilent 4155C Semiconductor Parameter Analyzer was employed for *dc* measurements.

Figure 23 shows the forward Gummel characteristics for a fully depleted HBT-on-SOI for the range of temperatures between 300 K and 20 K. Interestingly, even at very low

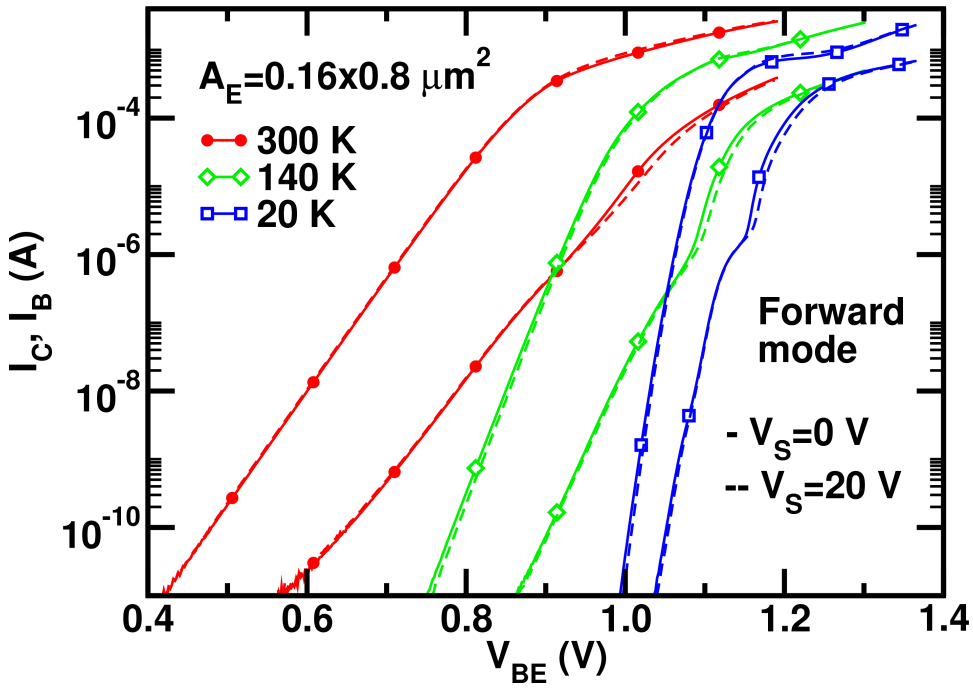


Figure 23: Forward Gummel characteristics in the temperature range between 20 K and 300 K for V_S equal to 0V and 20 V.

temperatures, the forward mode behavior of the transistor shows a remarkably ideal base current, despite the high peak base doping level (N_B $>5 \times 10^{18} cm^{-3}$). This low level of leakage can be explained by the use of a lightly doped epitaxial spacer layer between the base and emitter regions, which reduces parasitic recombination and field-assisted tunneling at low temperatures. Since the doping level of the emitter and base is well above the Mott transition, freeze-out at deep cryogenic temperatures produces limited impact on the base and emitter resistances.

Conversely, the light collector doping used by the fully depleted HBT-on-SOI increases the importance of quasi-saturation and heterojunction barrier effects (HBE) at low temperatures. The first phenomenon is caused by the voltage drop over the collector resistance R_C, which internally forward biases the CB junction, while the second phenomenon originates from the collector current exposing the valence band barrier at the collector-base heterojunction at high injection [45][39][41]. Both these effects result in a decrease in collector current and an increase in base current, which are then amplified by the reduction in temperature. In fact, the large increase in I_B at 20 K can be explained by an enhancement

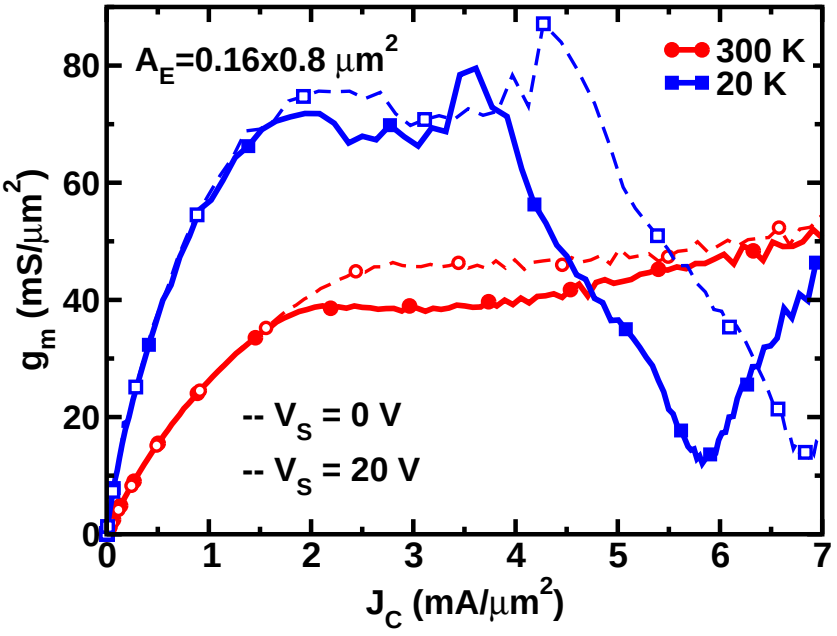


Figure 24: Transconductance per unit area versus collector current density J_C for a fully-depleted SiGe HBT-on-SOI in the temperature range between 20 K and 300 K.

of both quasi-saturation and HBE with cooling. According to [33], R_C should increase significantly below 50 K. Moreover, the increase in I_B resulting from HBE is exponentially coupled to the valence band barrier over kT [46]. It should also be noted that the increase of the substrate voltage V_S results in a slight reduction of the I_B increase and I_C decrease, as shown in Figure 23.

It should also be noted that the improvement in the analog figure-of-merit βV_A with cooling suggests that this device may be successfully employed for amplifier design at low temperatures. Moreover, the transconductance of the device, shown in Figure 24, increases with cooling from about 40 $mS/\mu m^2$ at room temperature to more than 70 $mS/\mu m^2$ at 20 K, as expected.

Such increase makes the device interesting for high-gain analog applications at cryogenic temperatures. Figure 24 also confirms the presence of HBE, which produces a sharp dip in the transconductance at low temperature and at high current densities. Interestingly, the current density J_{HBE} at which the dip occurs decreases with decreasing temperature, unlike that found in conventional vertical SiGe HBTs [39][41]. In bulk SiGe HBTs, the increase in

J_{HBE} with cooling can be explained by the enhancement of the saturation velocity at low temperatures, which leads also to a larger Kirk effect onset current. Since a comparable SiGe HBT-on-SOI featuring a high doping collector has shown the same trend of the bulk devices, it may be argued that the discrepancy in J_{HBE} behavior is resulting from collector doping and the difference in the electric field in the depleted collector region.

The Gummel characteristics in inverse mode (emitter and collector swapped) are not nearly as ideal as in forward mode: in particular the large amount of base leakage suggests that the collector-base junction is populated by a significant density of traps and that field-assisted tunneling is an important issue at low temperatures. Given that this device is fabricated on an SOI substrate, it is reasonable to wonder about the possible introduction of defects in the collector during the SOI fabrication itself. Neutral base recombination (NBR) measurements are used to investigate the presence of traps in the neutral base and in the collector-base space charge region. As displayed in Figure 25, the base current normalized with the value at $V_{CB} = 0$ V versus V_{CB} shows an increasing negative slope with lower temperatures — a telltale signature of the presence of NBR [70][40].

Furthermore, analysis of avalanche multiplication has been used to shed light on the effect of substrate bias V_S on electric field and on current flow across temperature.

Figure 26 plots collector current I_C versus V_{CB} at fixed emitter current I_E at 300 K and at 180 K, providing important insights into the behavior of M-1 at room and at cryogenic temperatures.

In agreement with the explanation presented in Section 1.4.2, Figure 26 a) shows that at room temperature for $V_S = 0$ V, an increase in V_{CB} up to roughly 5 V produces little change in the avalanche current because as the collector is fully depleted, the voltage across the collector-base junction is pinned. Further increases in V_{CB} increase the electric field in the lateral path and eventually M-1. Conversely, when V_S is increased the accumulation layer will alter the potential in the collector, applying most of the external V_{CB} voltage to the collector-base junction and significantly increasing the electric field in the vertical path and consequently M-1 [16].

Measurements on bulk devices at low temperatures have shown that when the substrate

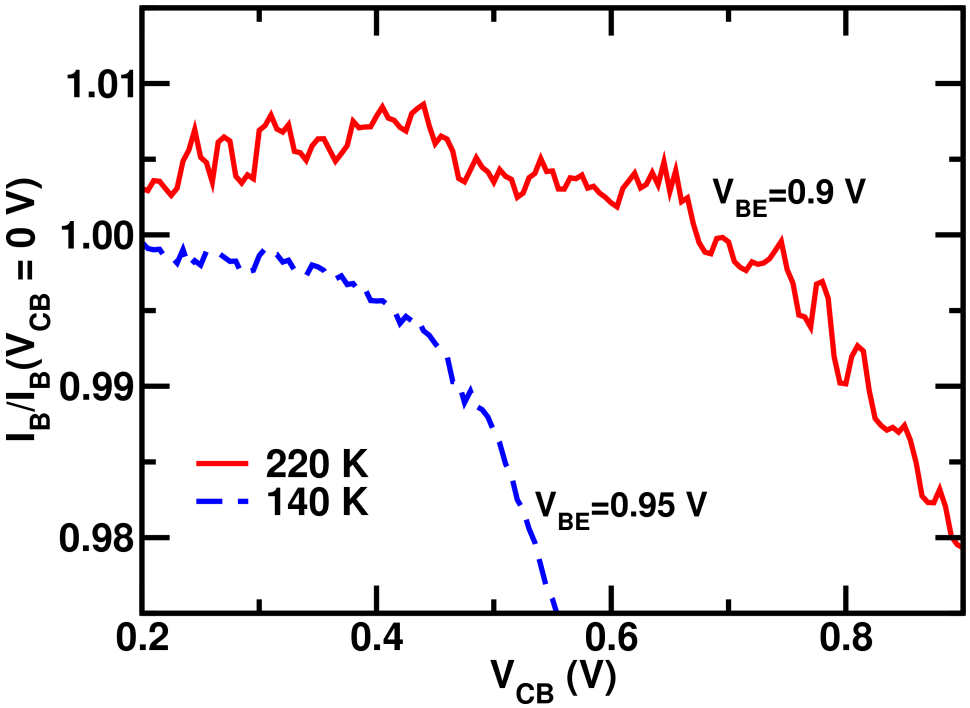


Figure 25: Base current I_B normalized with the I_B value at $V_{CB} = 0$ V versus V_{CB}, highlighting the presence of NBR.

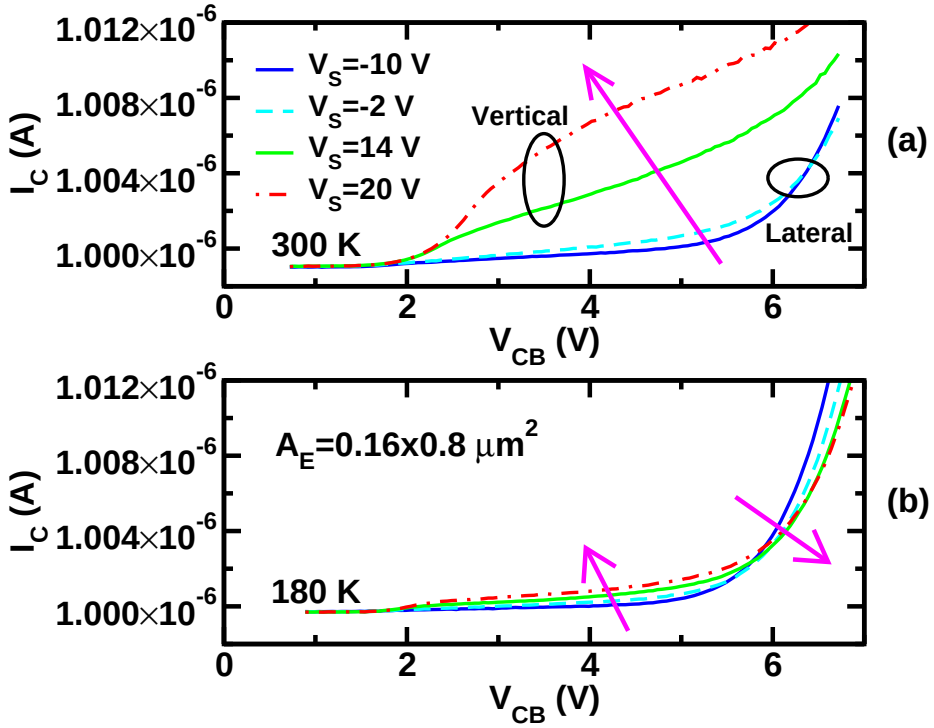


Figure 26: I_C versus V_{CB} for substrate bias V_S equal to -10 V, -2 V, 14 V, and 20 V at 300 K (a) and at 180 K (b).

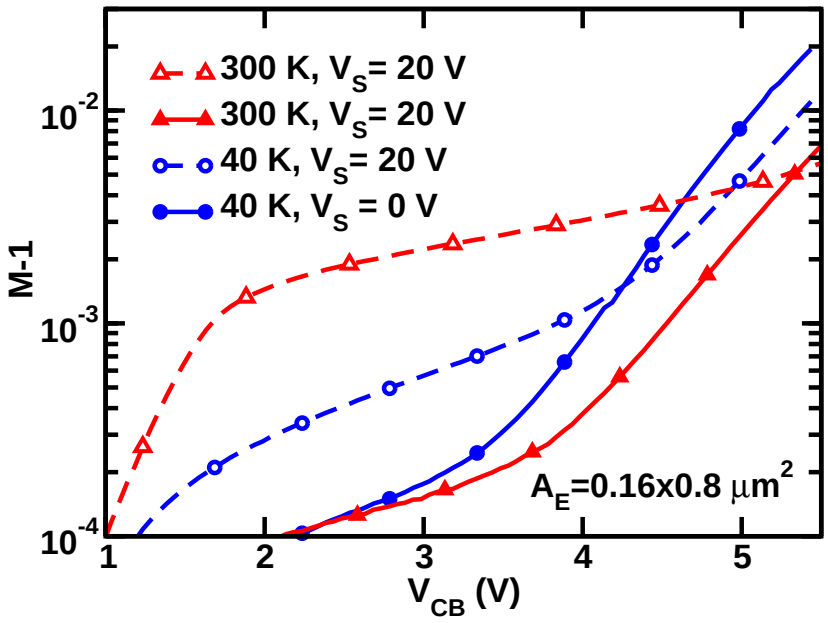


Figure 27: M-1 versus collector-base voltage V_{CB} for a fully depleted HBT-on-SOI at 40 K and 300 K for grounded substrate and for biased substrate with V_S equal to 20 V.

is grounded, M-1 increases monotonically at lower temperatures as a result of a longer mean free path. The impact of cryogenic temperatures on SOI devices is more complicated because the substrate voltage appears to have smaller effects than at room temperature, as shown in Figure 26 b), probably as a result of different current flow paths. In particular, the shape of I_C suggests that even at V_S equal to 20 V the electric field in the lateral path seems dominant in avalanche multiplication.

The extracted M-1 is shown in Figure 27, which displays behavior consistent with Figure 26. At low substrate bias V_S, the decrease in temperature enhances avalanche multiplication at higher collector bias, resulting in a higher M-1. Yet at high V_S, M-1 at low temperatures is smaller than at room temperature for low V_{CB}, but higher for high V_{CB}, in agreement with the data shown in Figure 26.

Although self-heating is obviously a concern for all SOI devices, at low temperatures the thermal conductivities of both silicon and SiO_2 naturally increase. As shown in Figure 28, the thermal resistance R_{TH}, extracted using the technique detailed in [81], decreases significantly with cooling. Even though R_{TH} is about five times that of a comparable bulk

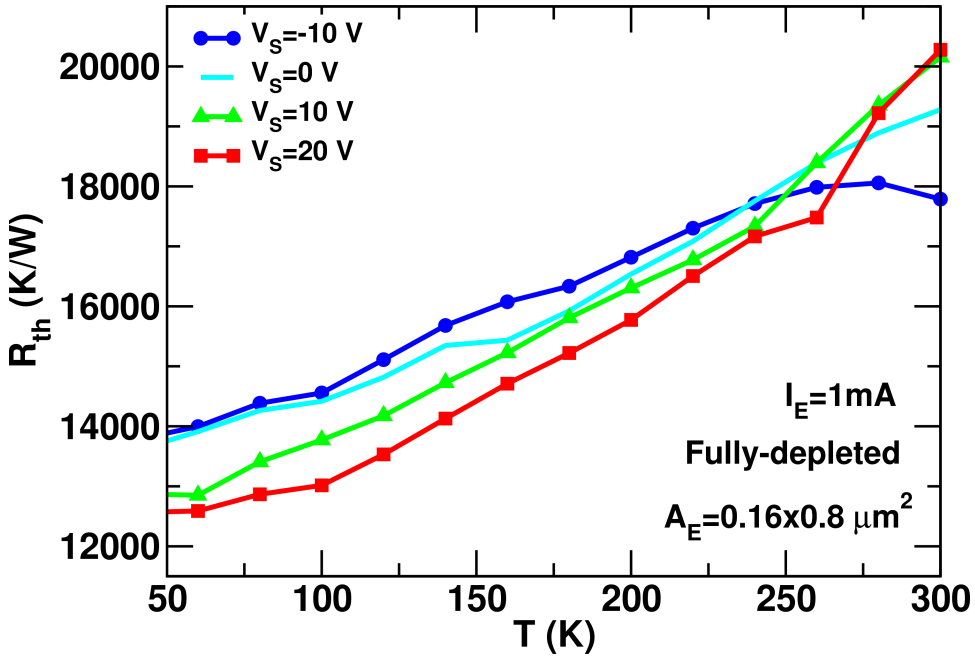


Figure 28: Thermal resistance of a fully depleted SiGe HBT-on-SOI in the temperature range between 50 K and 300 K.

device, we can expect some mitigation of any self-heating triggered reliability issues at low temperatures, clearly good news for cryogenic applications.

To conclude, the cryogenic operation of a fully depleted SiGe HBTs-on-SOI has been investigated for the first time by analyzing the behavior of *dc* parameters such as the current gain, the transconductance, and M-1 at low temperatures. The effects of the substrate bias have been examined as a tool to understand the current flow in the two-dimensional collector. The thermal resistance of the device was extracted in the range of temperatures between 50 K and 300 K. The high current gain and transconductance suggest that this device is suitable for the design of high-gain amplifiers at low temperatures.

3.2 Reliability at Room and Cryogenic Temperatures

Clearly, before any new technology can be used in any type of application, it must be proven reliable. For example, the effect of substrate bias during room temperature stress on fully depleted SiGe HBTs-on-SOI was discussed in [16], showing that a grounded substrate appears to be the worst-case stress condition. The present section describes how, for the first time, SiGe HBTs-on-SOI were stressed at 77 K and compared with stress applied at

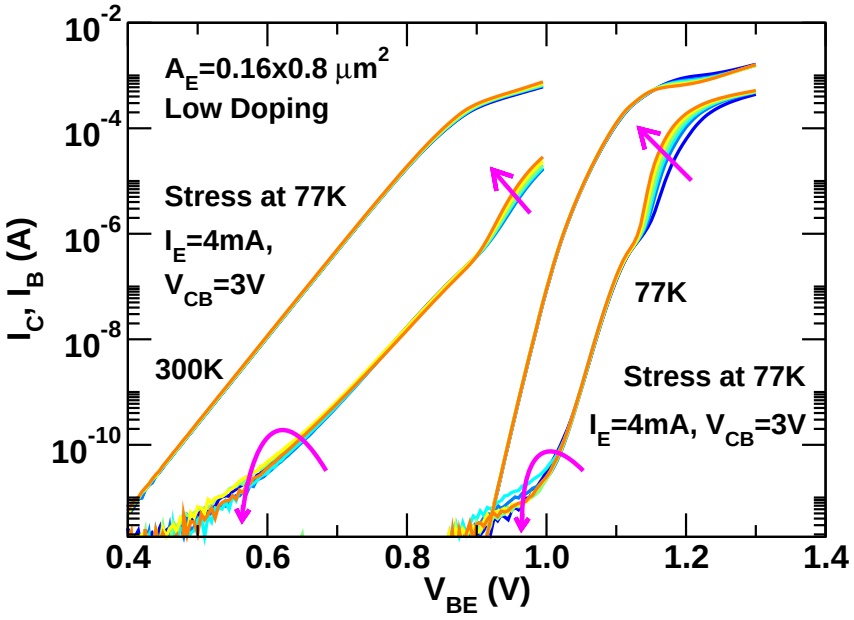


Figure 29: Effects of stress on the Gummel characteristics of a fully depleted SiGe HBT-on-SOI after a 4 hour stress sequence, at both 300 K and at 77 K.

300 K, noting the effects on I_B, current gain, and avalanche multiplication. The effects of stress on the *ac* characteristics are also investigated, and comparisons are made to more conventional reliability burn-in techniques [13].

The devices were subjected to mixed-mode stress [32][92]. This technique is based on simultaneous application of both high current density and collector-base voltage, and is thought to emulate actual mixed-signal circuit operation in a better way than more traditional stress techniques [82][53] . Measurements were performed with an Agilent 4155 Semiconductor Parameter Analyzer and a closed-cycle cryogenic test system. All devices showed negligible degradation until a current as high as $I_E = 4$ mA, which is about 20 times the peak f_T current, was applied. Overstressing was applied also in reliability studies of the bulk SiGe HBTs that share the same emitter and base profiles, but in that case the stress current needed was only 4-5 times the peak f_T current [92].

Figure 29 shows the effect of mixed-mode stress at $I_E = 4$ mA and $V_{CB} = 3$ V for the

fully depleted device at 300 K and at 77 K. The forward and inverse mode Gummel characteristics were measured at 40 logarithmically spaced points over a total stress time of 4 hours. The figure displays a small increase in the base current at low V_{BE} and the presence of significant spontaneous damage recovery. The other most notable effect is the increase in the quasi-saturation effect at high V_{BE}, resulting from an increase in collector resistance R_C. This degradation is especially relevant for the fully depleted SiGe HBT-on-SOI device, which is characterized by a larger R_C than a comparable bulk device because of lower collector doping. This damage shows no sign of recovery and becomes more significant at low temperatures resulting from additional collector freeze-out. The stress-induced base current of the partially depleted device behaves similarly; however, the increase in R_C appears more modest, resulting from its higher collector doping. The presence of spontaneous damage recovery has been consistently observed in multiple devices at different temperatures. Yet, interestingly, the amount of recovery is shown to vary substantially between samples. Although the exact amount of I_B degradation cannot be reliably predicted (this is in itself a potential reliability issue), the amount of leakage current is modest and confined to a low-current region rarely employed in actual circuit design. The presence of fluctuations in the excess base current such as those shown in Figure 30 was reported in [92] and attributed to a process of bond breaking and creation of a dangling silicon bond at the Si-SiO_2 interface, followed by re-passivation of such dangling bonds. The high junction temperature reached during mixed-mode stress because of the large R_{TH} of the device could enhance the re-passivation process, as suggested in [82].

As further argued in [82], fluctuations would be observed, especially if the number of interface traps is small and the rates of generation and annealing are slow. The inverse mode operation is similarly affected by both degradation and recovery. However, since the inverse mode Gummel characteristics already show a high base leakage current, possibly resulting from interface defects introduced by the SOI fabrication process, the relative degradation introduced by stress is negligible.

Given the limited impact of mixed-mode stress on this device (clearly good news from a reliability point of view), more traditional reverse emitter-base bias stress, as described

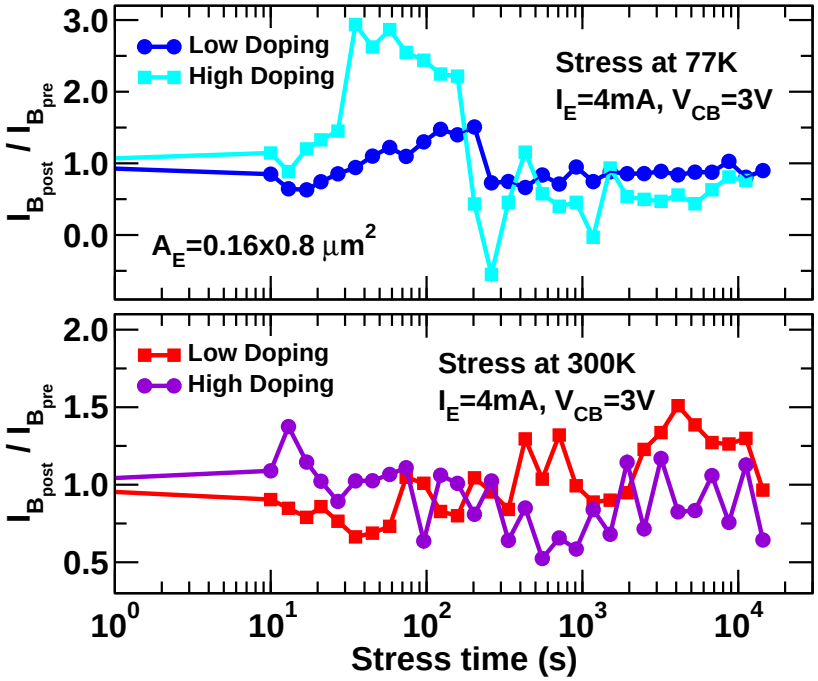


Figure 30: Ratio of post-stress and pre-stress base current extracted at a voltage V_{BE} such that $I_{B,pre}$ is 20 pA.

in [53], was also applied. By using an increasing V_{EB} the damage threshold to reverse EB bias stress was determined to be between 3 and 4 V, as shown in Figure 31. In direct contrast to mixed-mode stress, this stress mechanism results in large degradation without any sign of recovery, possibly because self-heating effects are less important during reverse emitter-base bias stress. Unlike for mixed-mode stress, no change in the collector resistance was observed. Interestingly, mixed-mode stress was applied after reverse EB bias stress, resulting in a sharp reduction of the non-ideal I_B component and confirming the presence of an underlying self-annealing mechanism.

Calibrated TCAD simulations were used to show that because of the reduced collector doping and of the nature of 2-D doping profile of the folded collector, the peak of the electric field is situated far from the emitter-base spacer in the case of mixed-mode stress, as shown in Figure 32, while it is obviously adjacent to the EB spacer for the reverse EB bias stress, consistent with our data.

Comparing simulations of these SiGe HBTs-on-SOI with those of a corresponding bulk

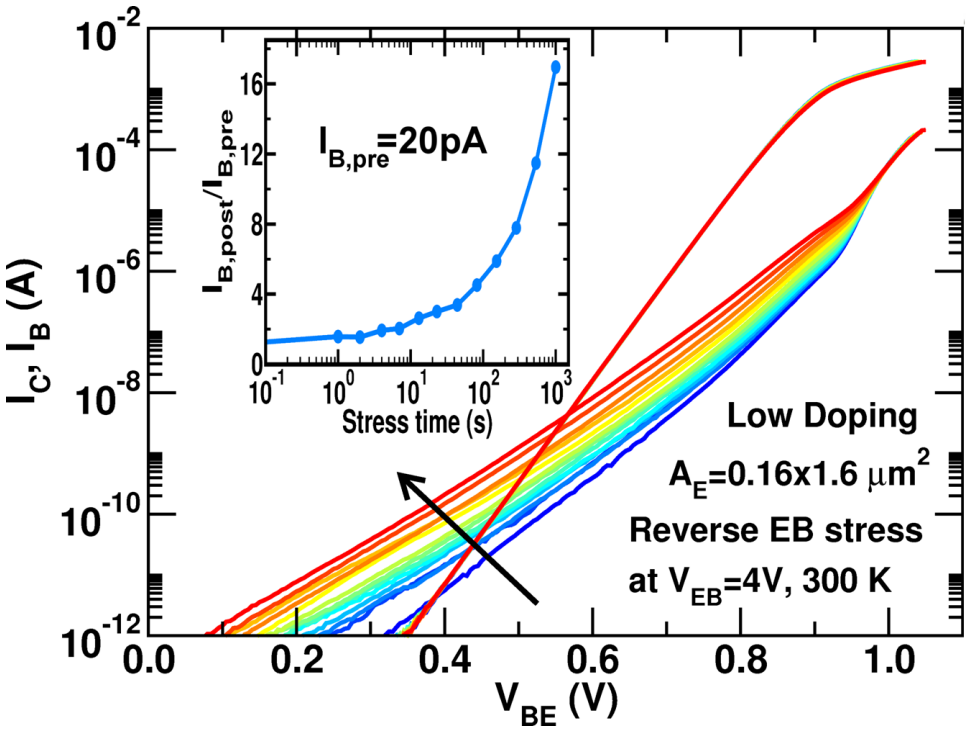


Figure 31: Excess base current of a fully depleted SiGe HBT-on-SOI stressed for 1000 seconds with V_{EB}=4 V.

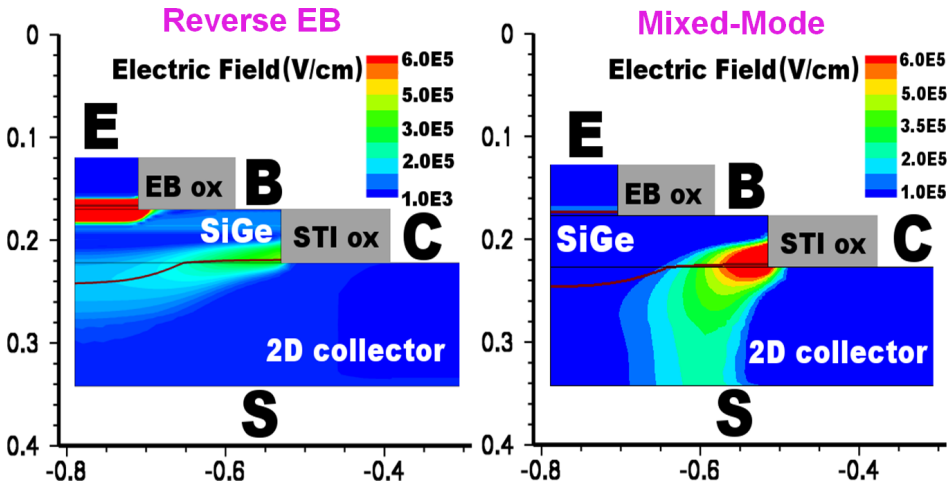


Figure 32: Electric field contour of a fully depleted SiGe HBT-on-SOI biased at I_E = 1 mA and V_{CB}=3 V.

device, as described in [92], one can easily observe that the electric field distribution and the position of its peak are significantly altered by the differences in the collector profiles. Since mixed-mode stress combines high current operation with large collector-base bias, it is not surprising that the collector doping affects the extent of the stress damage in a fundamentally different manner.

The effects of stress on *ac* performance have also been investigated under mixed-mode stress, using a fixed stress time of 1,000 seconds. As shown in Figure 33, an emitter current I_E of 8 mA (about four times the peak f_T current) and V_{CB} of 2 V result in negligible changes in both f_T and f_{max}. The increase of V_{CB} to 3 V with $I_E = 8$ mA results in a small but noticeable decrease in f_{max}, suggesting that the degradation process has a threshold situated between 2 V and 3 V. The increase of the emitter current to higher values results in only a slightly lower f_T and in a more noticeable reduction in f_{max}, indicating negligible damage in the intrinsic device [92]. The degradation of f_{max} for low J_C could be resulting from stress-induced changes in the base resistance r_{bb}, either in the extrinsic or intrinsic base region (or both). The slight change in f_{max} at high J_C is caused by the observed increase in the collector resistance R_C. The partially depleted device shows a similar behavior, with small decreases in f_T and f_{max}. Due to the higher doping of the collector, peak f_T is larger and occurs at a higher current density.

To conclude, both fully depleted and the partially depleted SiGe HBTs-on-SOI show little degradation under applied mixed-mode stress. The observed larger degradation shown by I_B under reverse emitter-base bias stress is expected, but is of less concern because this operational mode is seldom encountered in normal circuit operation. The effects of mixed-mode stress on M-1 and on *ac* performance have also been discussed.

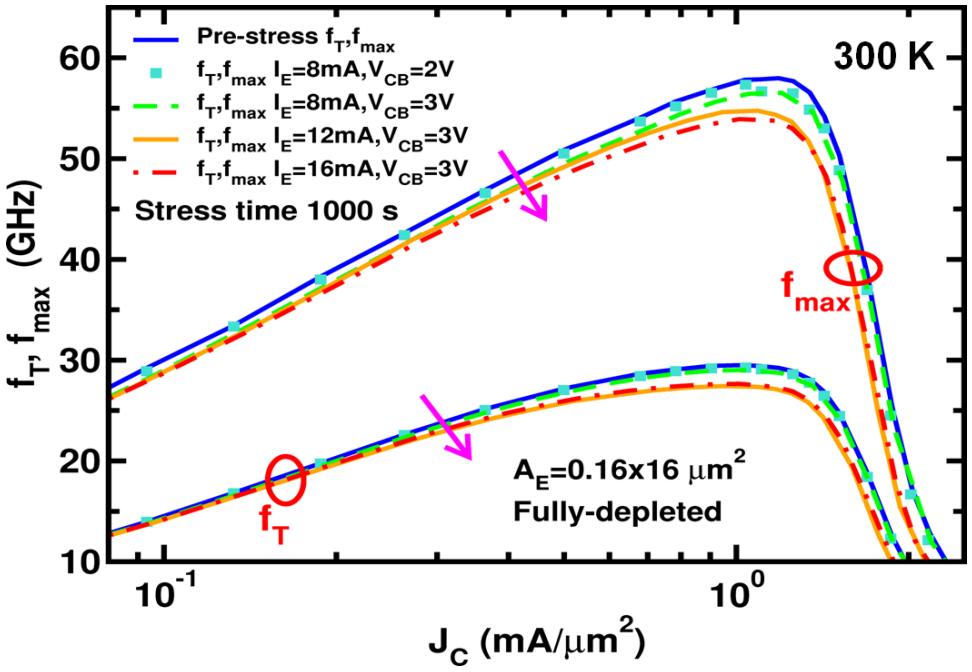


Figure 33: Effects of mixed-mode stress on f_T and f_{max} of a fully depleted SiGe HBT-on-SOI.

CHAPTER IV

OPERATION AT HIGH TEMPERATURES

Numerous emerging applications require IC operation above standard commercial or mil-spec temperatures (+85°C or +125°C, respectively), including: under-the-hood automotive electronics, all-electric-aircraft electronics for aerospace, power switching and control, nuclear power, radar systems, planetary exploration, and importantly these days, oil well logging and drilling [17]. In the latter case, disruptive innovations in the current practice of down-hole drill sensing could be provided by highly-integrated electronics packages robust to 200-300°C. This chapter investigates the impact of high temperatures on the *dc*, *ac*, [8] and $1/f$ noise performance of SiGe HBTs-on-SOI [7].

While bandgap engineering, as mentioned in Chapter 3, improves SiGe HBTs figures of merit at low temperatures, it necessarily degrades device performance at high temperatures. Moreover, the introduction of SOI substrates obviously raises self-heating concerns.

4.1 High Temperature Operation of SiGe HBTs-on-SOI

As mentioned in Section 1.1, high temperatures would intuitively seem to naturally disfavor the use of SiGe HBTs (for the same reason that their operation is favorably affected by cooling). Yet recent work has shown that operation of bulk SiGe HBTs at temperatures above 125 °C is potentially possible [17]. Clearly, however, bulk SiGe HBTs suffer from collector-substrate leakage at elevated temperatures, potentially compromising their usefulness for analog design. In the present section, we demonstrate that SiGe HBTs-on-SOI are in fact much better suited for a wide variety of high-temperature applications, to operating temperatures as high as 330 °C [8].

This section presents the first investigations on the high-temperature performance of SiGe HBTs-on-SOI, from both *dc* and *ac* points of view. All devices were measured on-wafer with an Agilent 4155C (for *dc*) and with an Agilent 8510 VNA (for *ac*), using a probe station capable of reaching 330 °C (for *dc*) and 200 °C (for *ac* limited by probes).

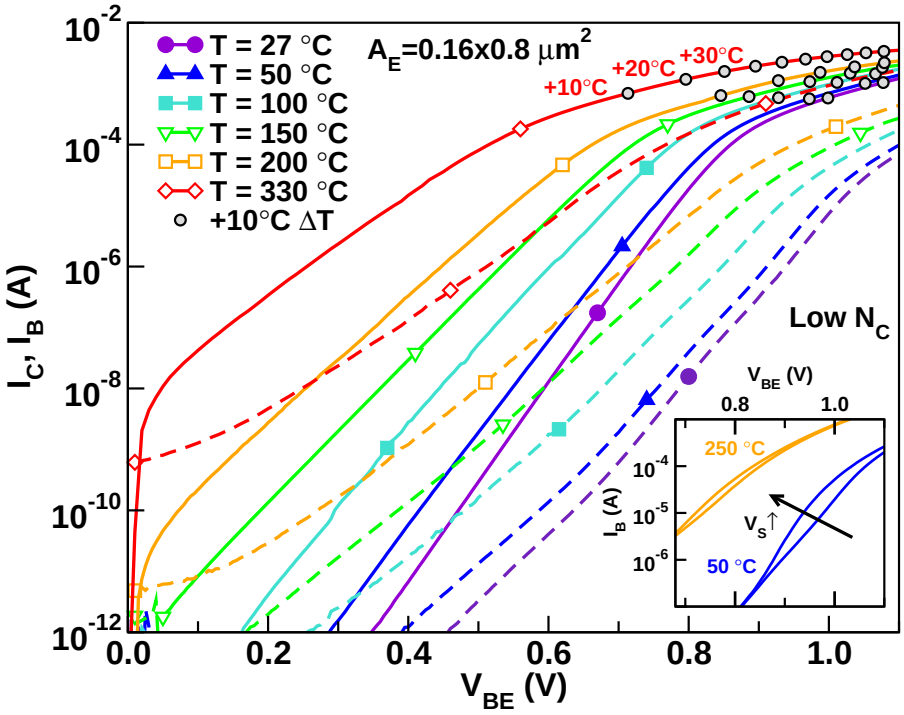


Figure 34: Forward Gummel plot of low N_C SiGe HBT-on-SOI. The inset shows I_B for $V_S = 0$ V and 20 V at 50 °C and 250 °C.

The forward Gummel characteristics of the fully depleted SiGe HBT-on-SOI, over the temperature range of 27 °C to 330 °C, are shown in Figure 34. Device temperature is estimated (based on extracted R_{TH} ranging from 16,000 K/W at 27 °C to 20,000 at 330 °C) and is shown in 10 °C increments in Figure 34. As expected, the turn-on voltage decreases at higher temperatures, because of the increase in intrinsic carrier density n_i. The large current drive achievable at 330 °C indicates that the impact of additional scattering at high temperatures on the mobility and hence on series resistances is negligible, clearly good news.

An applied V_S alters the current flow path [16], reducing the collector resistance R_C and partially mitigating quasi-saturation effects associated with the folded collector. But high temperatures, as shown in the insert of Figure 34, greatly decrease the impact of V_S on both the increase of I_B and the decrease of I_C. TCAD simulations confirm that the reduction of the substrate bias effect is caused by the large amount of the electron charge injected in the SOI layer at 330 °C, which effectively lowers R_C. The devices also showed

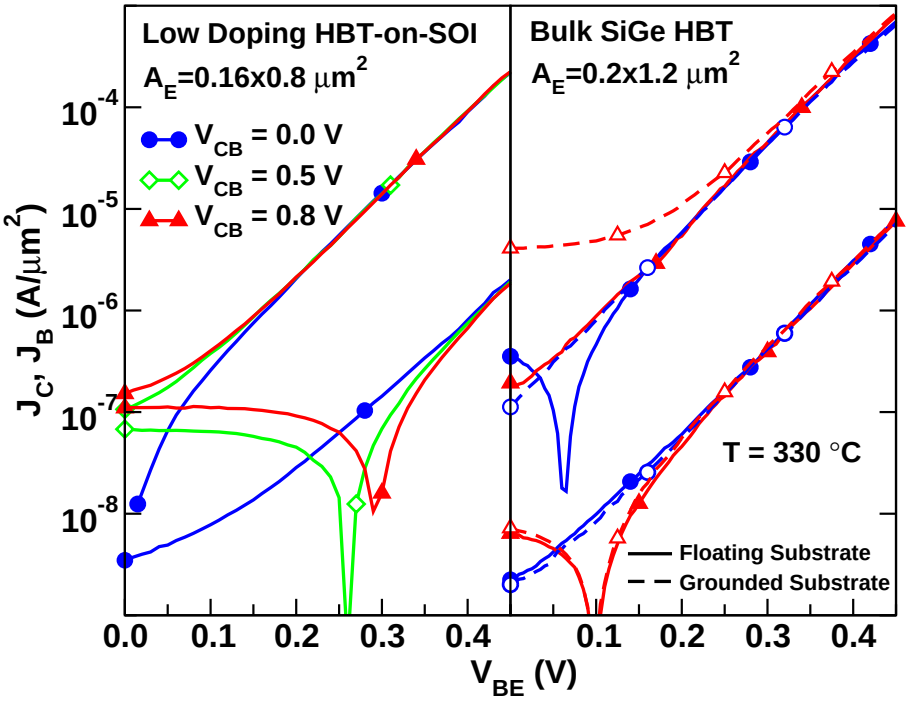


Figure 35: Forward Gummel plot of fully depleted SiGe HBT-on-SOI at 330 °C at V_{CB} = 0 V, 0.5 V, and 0.8 V compared to a bulk device.

no sign of metallization-failure-induced bias instabilities at high temperatures: the devices were operated under bias for 1 hour at 330 °C, and showed no changes.

Another advantage of the SOI device is the elimination of the collector-substrate junction leakage resulting from space-charge generation and from band-to-band thermal generation, which can be a serious concern for bulk devices in analog circuits [17]. As shown in Figure 35, I_C increases by only a small amount when the V_{CB} rises, in contrast with comparable bulk devices [17].

Figure 36 shows M-1 for the fully depleted device extracted using the technique from [55]. The measurement was taken at fixed $I_E = 4$ μA, which is large enough to minimize the impact of the leakage current I_{CBO}, as can be seen from Figure 35, but still small enough to avoid self-heating.

As discussed in [16], substrate voltage influences greatly M-1 in the low N_C device: as V_S increases, the peak of the electric field shifts laterally in the SOI layer, resulting at 27 °C in the characteristic change of shape of M-1 from V_S = -10 V to V_S = 20 V, which can

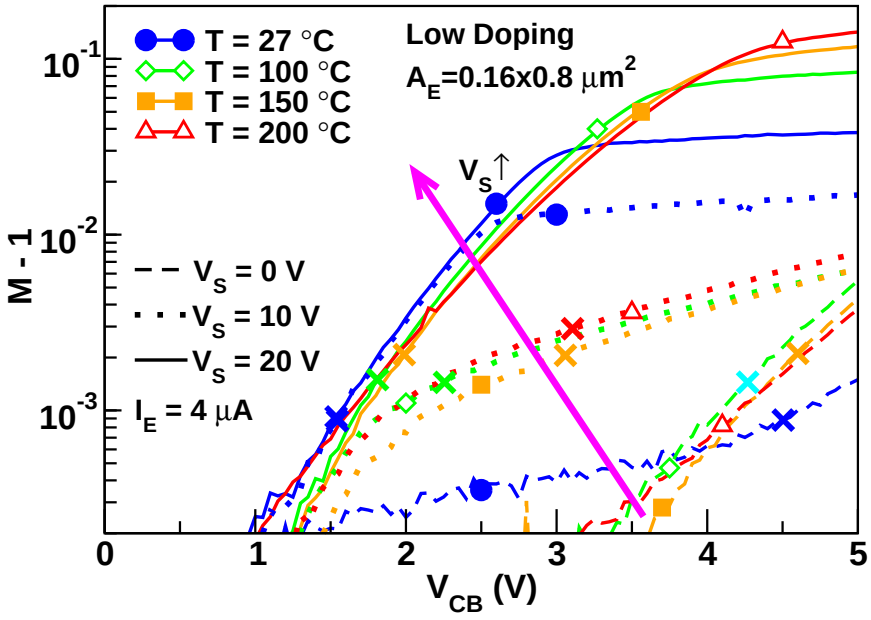


Figure 36: M-1 of low N_C SiGe HBT-on-SOI at 27 °C, 100 °C, 150 °C, and 200 °C. The crosses indicate base current reversal.

be seen in Figure 36 (circles). The temperature dependence of M-1 in the fully depleted device is extremely complicated because of the 2-D nature of the current flow. We note that for positive substrate bias, the external vertical electric field becomes dominant and M-1 first increases until it reaches the classic arc-shape typical of bulk SiGe HBTs. We can observe that temperature has two effects on M-1: 1) it reduces the amount of impact ionization, as confirmed in the TCAD simulation in Figure 37, and 2) it increases the effect of the substrate bias V_S, as can be inferred from the increase of M-1 at V_S = 20 V and V_{CB} = 5 V, leading to an M-1 shape similar to that of a bulk SiGe HBT.

Conversely, Figure 38 shows that the behavior of M-1 for the partially depleted device is similar to a vertical bulk device and decreases monotonically with temperature.

Figure 38 shows that since β decreases with temperature, the base current reversal point will occur at a higher M-1 to compensate for the reduction in current gain.

Figure 39 displays the breakdown voltages for both devices as a function of temperature and V_S, showing a very different behavior for the different collector doping levels. The

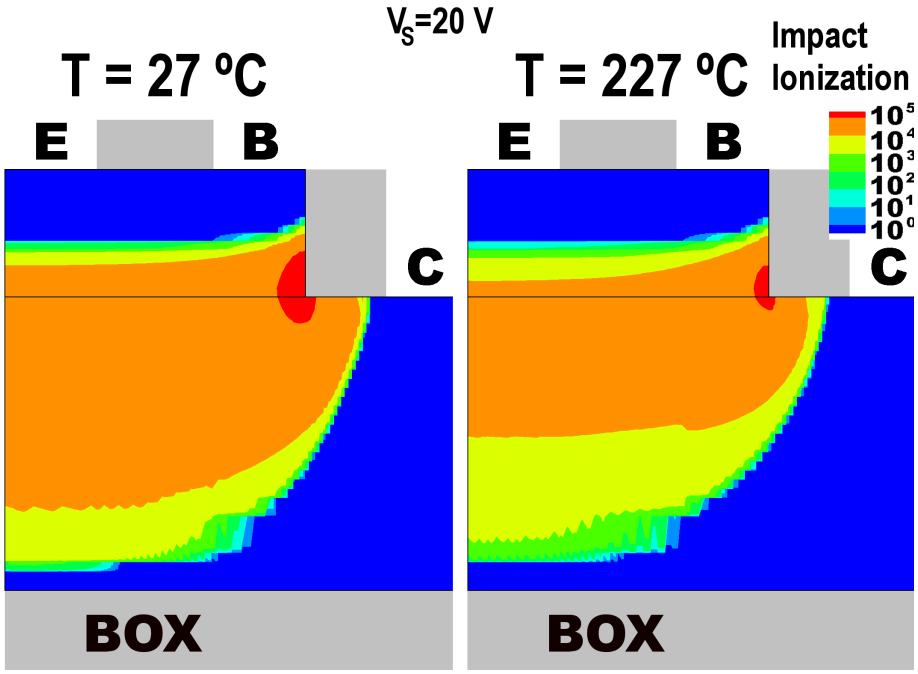


Figure 37: TCAD simulation of electron ionization coefficient in a low N_C HBT-on-SOI at temperature of 27 °C (300 K) and 227 °C (500 K) for a substrate voltage $V_S = 20$ V.

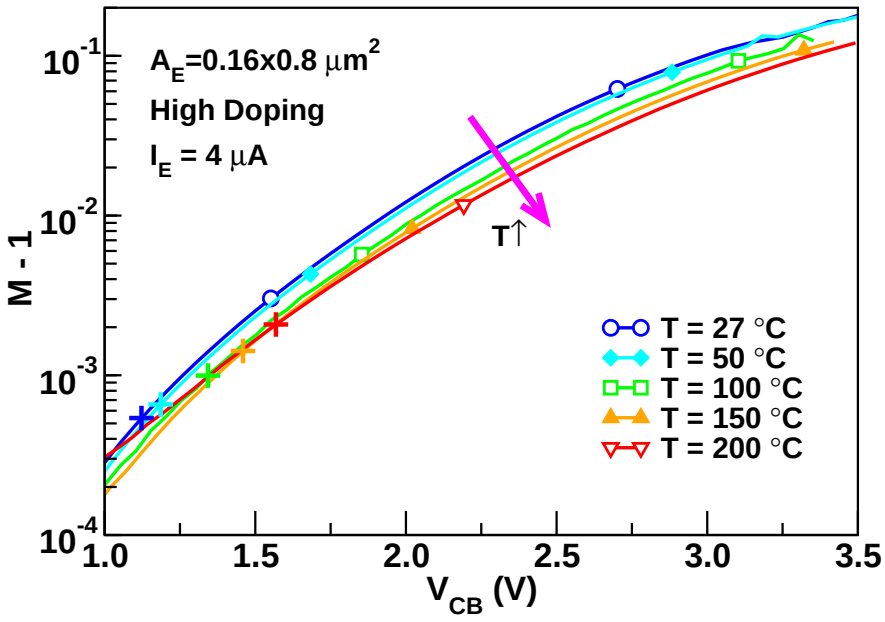


Figure 38: M-1 of high N_C SiGe HBT-on-SOI at 27 °C, 100 °C, 150 °C, and 200 °C. The crosses indicate base current reversal.

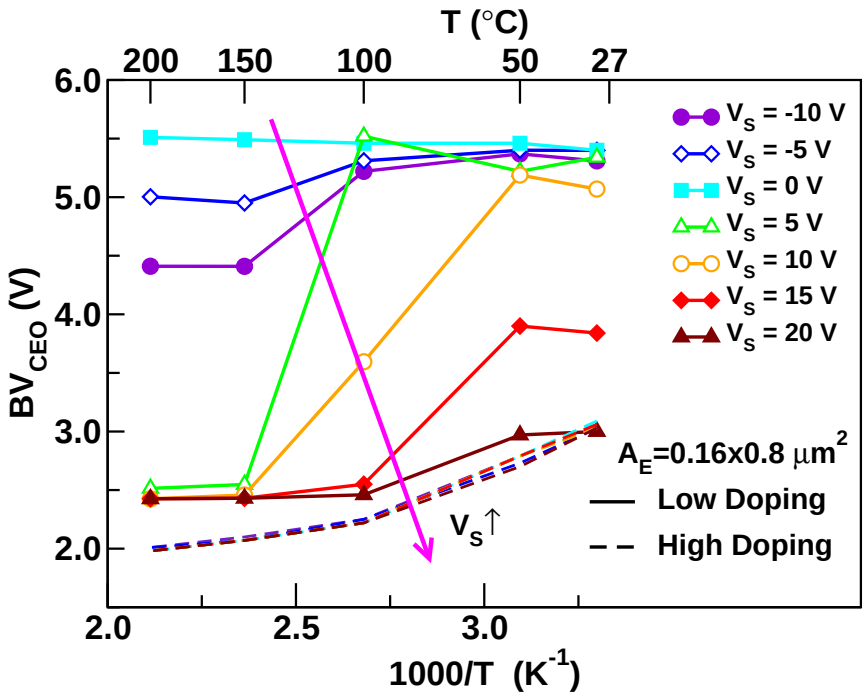


Figure 39: B_{VCEO} of fully and partially depleted SiGe HBT-on-SOI at 27 °C, 100 °C, 150 °C, and 200 °C.

higher N_C devices show a decreasing B_{VCEO} with temperature, in agreement with the previous studies on high-performance bulk SiGe HBTs [17]. In contrast, the low N_C devices show significant dependence on V_S. While at a V_S lower or equal to zero (depleted collector) B_{VCEO} decreases only slightly, at positive V_S (accumulated collector) the breakdown voltage reduces significantly, consistent with the typical behavior of partially depleted or bulk devices [17]. This is expected since in accumulation the external vertical electric field dominates the device behavior, in accord with findings in previous studies [16].

Finally, Figure 40 shows peak f_T and f_{max} in the temperature range between 27 °C and 200 °C for the fully depleted device. While positive substrate voltage V_S improves the *ac* performance of the device, temperature leads to a decrease in both f_T and f_{max}, consistent with data on bulk devices in [17]. Extraction of the forward transit time τ_F shows a significant increase at higher temperatures, which is likely caused by the degradation of τ_B resulting from enhanced scattering and the mobility degradation.

To conclude, the high-temperature operation of SiGe HBTs-on-SOI has been analyzed

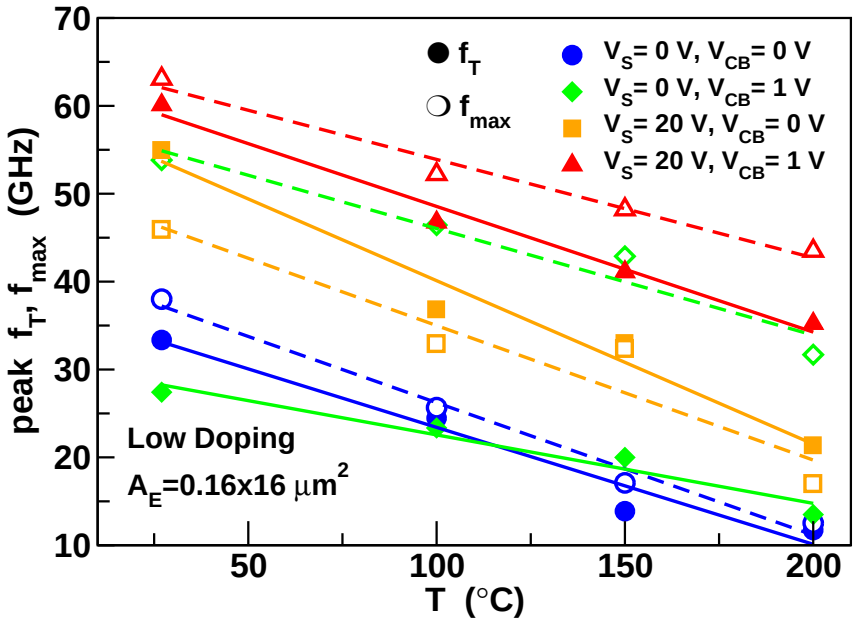


Figure 40: Transistor peak f_T and f_{max} of low N_C SiGe HBT-on-SOI in the temperature range between 27 °C and 200 °C.

from both an *ac* and *dc* perspective. The experimental data presented demonstrates that while operation at elevated temperatures yields an inevitable degradation in current gain, the resultant frequency response and breakdown voltages remain acceptable from a circuit perspective up to a temperature as high as 200 °C to 300 °C.

4.2 $1/f$ Noise at Room and High Temperatures

This section investigates in detail the $1/f$ noise performance of SiGe HBTs-on-SOI. For the first time, the low-frequency noise characteristics of both fully and partially depleted SiGe HBTs-on-SOI are measured both in forward and in inverse mode. To fully understand $1/f$ noise, the thin-film SOI devices are compared with bulk HBTs to evaluate how the different device structure affects $1/f$ noise performance. Furthermore, the impact of substrate voltage and collector doping and is analyzed. Finally, the impact of high temperatures on $1/f$ noise in the forward and inverse mode is studied [7].

Investigating the low-frequency noise characteristics of SiGe HBTs-on-SOI is important

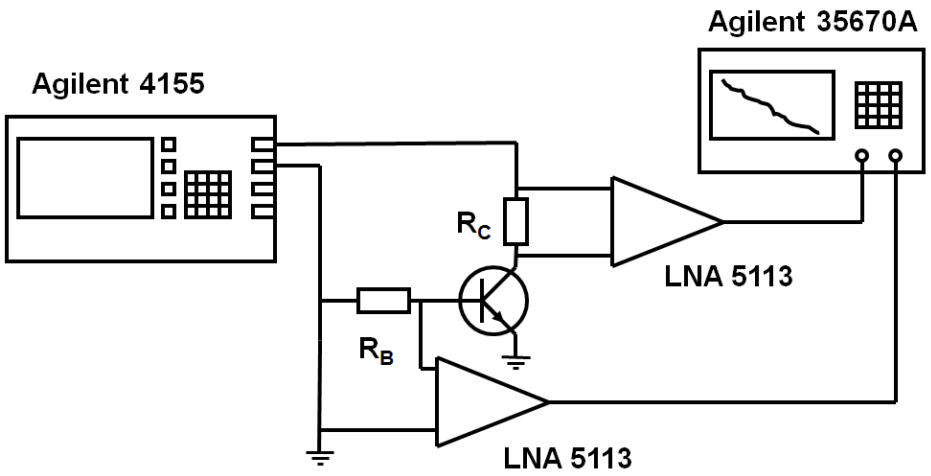


Figure 41: Dual channel low-frequency noise measurement setup. The noise voltage signals on the series resistors R_{BN} and R_{CN} is fed to Perkin Elmer low noise amplifiers model 5113 and measured by a dynamic signal spectrum analyzer Agilent 35670A. The device under test is biased by a semiconductor parameter analyzed Agilent 4155. All the instruments are computer-controlled [19].

not only from an application perspective (because of $1/f$ noise up-conversion at RF frequencies and the consequent detrimental effect on the spectral purity of the system), but also because it can shed light on the fundamental differences between SiGe HBTs-on-SOI and conventional bulk SiGe HBTs.

Both fully and partially depleted SiGe HBTs-on-SOI [15] are biased with a Agilent 4155 Semiconductor Parameter Analyzer and measured on a temperature controlled chuck capable of reaching 200 °C. Noise voltage signals on a metal film base series resistance R_{BN} of 500 $k\Omega$ and on a collector series resistance R_{CN} of 1 $k\Omega$ are amplified by Perkin Elmer low noise amplifiers model 5113 and fed to an Agilent 35670A Dynamic Signal Analyzer, covering the frequency range between 1 Hz and 52 kHz, as shown in Figure 41 [19].

In order to assess any possible degradation in low-frequency noise introduced by the folded collector structure, a fully depleted SiGe HBT-on-SOI with an emitter area $A_E = 0.16 \times 1.6\ \mu m^2$ is compared to an equivalent vertical SiGe HBT with $A_E = 0.2 \times 1.2\ \mu m^2$.

As shown in the inset of Figure 42, the Gummel plot normalized by area reveals significant discrepancies between the collector and base current of the devices, indicating that although the HBTs supposedly share the same emitter, base and germanium profiles, the

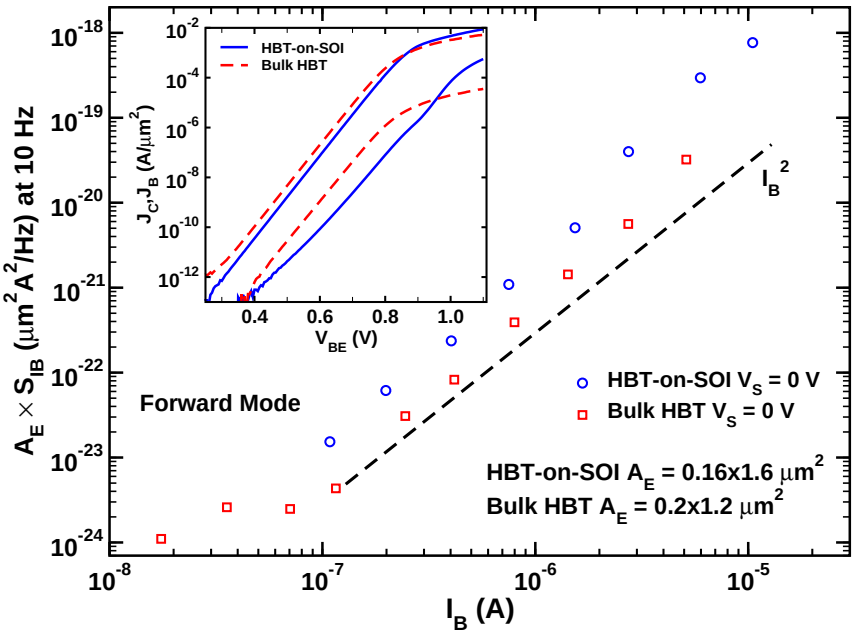


Figure 42: Base current noise power spectral density S_{IB} normalized by emitter area and interpolated at 10 Hz versus base current I_B for both a fully depleted HBT-on-SOI and a bulk (vertical) SiGe HBT, both measured at room temperature. The inset compares the Forward Gummel plots of the two devices.

different fabrication process introduces some unintended changes.

The reduced collector current I_C of the SOI device possibly suggests a slightly smaller germanium fraction at the side of the neutral base facing the emitter, which might be attributed to fabrication issues during the emitter formation process [86]. This is consistent with the significantly lower base current I_B which could be ascribed to a thicker undesired interfacial oxide (IFO). The inset also shows clearly that the SOI device exhibits a worse base current ideality compared to the bulk device whose base current is remarkably ideal. There are two factors which are responsible for the reduced non-ideality of the base current of the SOI device: the slight change of slope of I_B occurring in mid-injection condition and the small kink in I_B shown at a $V_{BE} = 0.8$ V before the onset of the quasi-saturation and HBE effects. Both these non-idealities could be explained by a thicker IFO, as reported in [86]. This hypothesis is confirmed in Figure 43 by the plot of the ratio of the base currents of the SOI device and the bulk HBT versus temperature. The noticeable increase in base current density at high temperature suggests the presence of a thicker IFO, according to

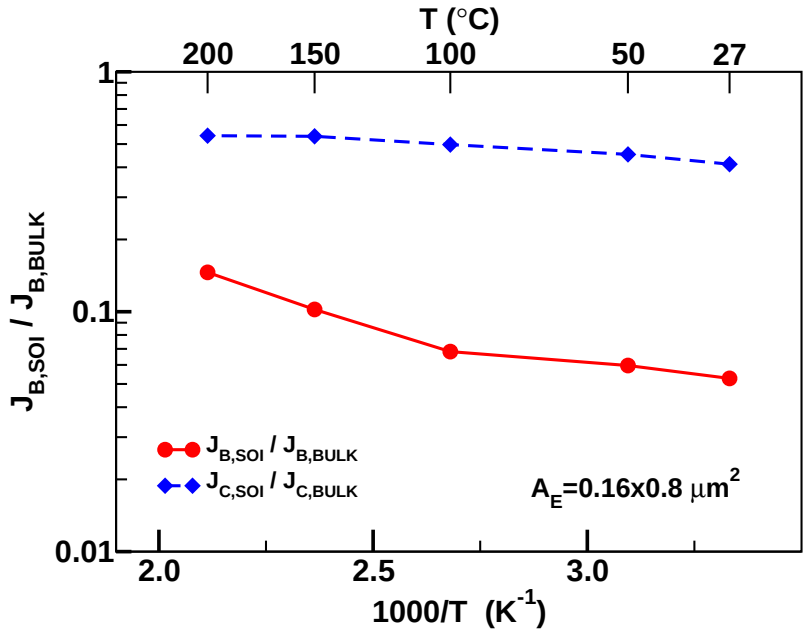


Figure 43: Comparison of the ratio of the collector and base currents of the HBT-on-SOI versus the bulk SiGe HBT as a function of temperature. The noticeable increase in the base current ratio suggests the presence of a thicker interfacial oxide at the emitter base interface of the SOI device.

the discussion presented in [2]. Furthermore, as reported in [89], $1/f$ noise has been proven to display a uniform exponential dependence on IFO thickness.

Given that previous studies have demonstrated how the substrate voltage V_S alters both *dc* and *ac* characteristics, it is relevant to investigate the possible impact of V_S on low-frequency noise. As shown in Figure 4, the substrate voltage shifts the current flow from the center of the device to the SOI/BOX interface. Thus, the collector current noise could potentially be affected by the presence of interfacial traps at the SOI/BOX interface, which could lead in principle to an increase in $1/f$ noise. As displayed in Figure 44, $1/f$ noise has been measured at different substrate bias V_S. Interestingly, the $1/f$ noise spectra reported show negligible variation for a range of V_S from -10 V (depletion) to 20 V (accumulation), which is clearly good news because the improvement in collector resistance, current gain roll-off and *ac* performance comes at no cost as long as $1/f$ noise is concerned. This result also suggests that the impact of traps at the substrate interface is inconsequential compared to traps in proximity of the EB junction.

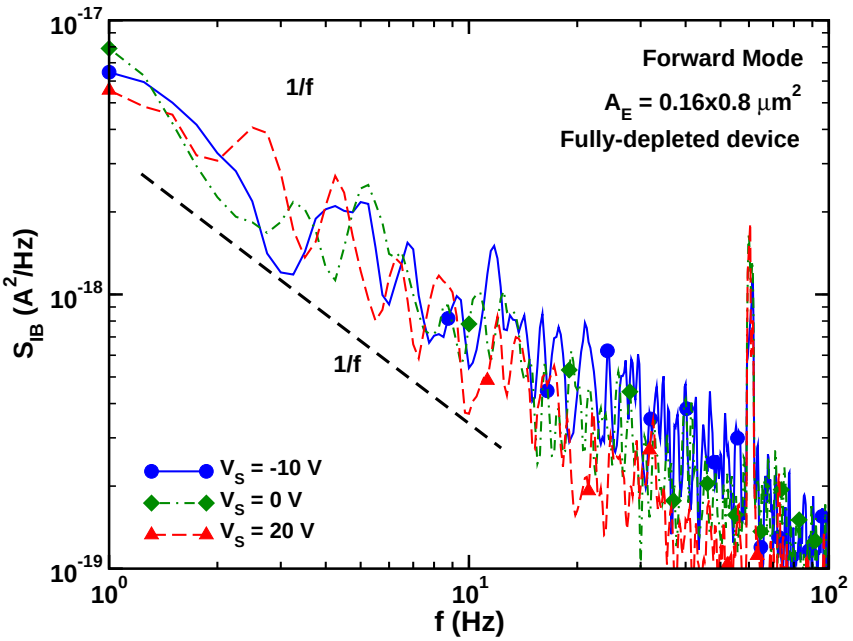


Figure 44: Noise spectra at room temperature of a fully depleted SiGe HBT-on-SOI at different substrate bias. As shown by the good overlap of the curves, V_S has negligible impact on the low-frequency noise of the device.

Figure 45 shows the base current noise power spectral density S_{IB} of fully depleted HBTs-on-SOI interpolated at 10 Hz versus emitter area A_E for increasing base current bias I_B. The data shows a reciprocal emitter area dependence which is typical of most SiGe HBTs, as reported in [89][27][38].

The temperature dependence of the $1/f$ noise in SiGe HBTs-on-SOI has also been investigated in the temperature range between 27 °C and 200 °C, as shown in Figure 46. Interestingly, although the S_{IB} noise spectrum maintains a I_B^2 dependence through the whole base current range, it increases noticeably for low temperatures at high current levels (I_B >1 μA), where the base current exhibits a hump because of the combination of the quasi-saturation and HBE effects. This behavior in S_{IB} disappears at 200 °C in accord with the fact that HBE is mitigated by higher temperatures. Finally, as displayed in the inset of Figure 46, S_{IB} extracted at high current levels (I_B = 20 μA) follows a $1/T$ trend.

Figure 47 compares the $1/f$ noise characteristics of fully depleted and partially depleted HBTs-on-SOI. As discussed in previous studies, the higher collector doping of partially

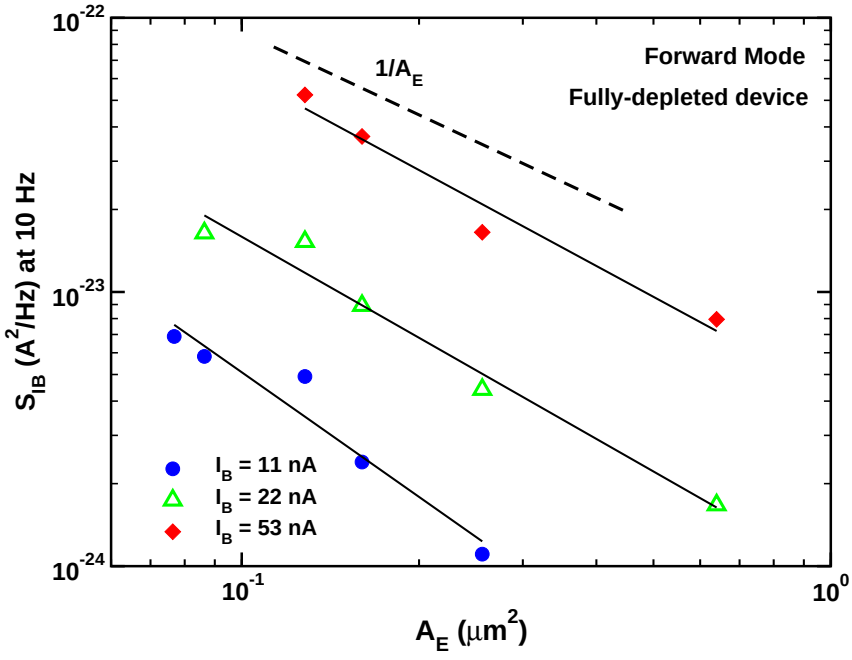


Figure 45: Base current noise power spectral density S_{IB} of fully depleted HBTs-on-SOI interpolated at 10 Hz versus emitter area A_E for increasing base current bias I_B, measured at room temperature. The measurement shows a $1/A_E$ dependence, as expected.

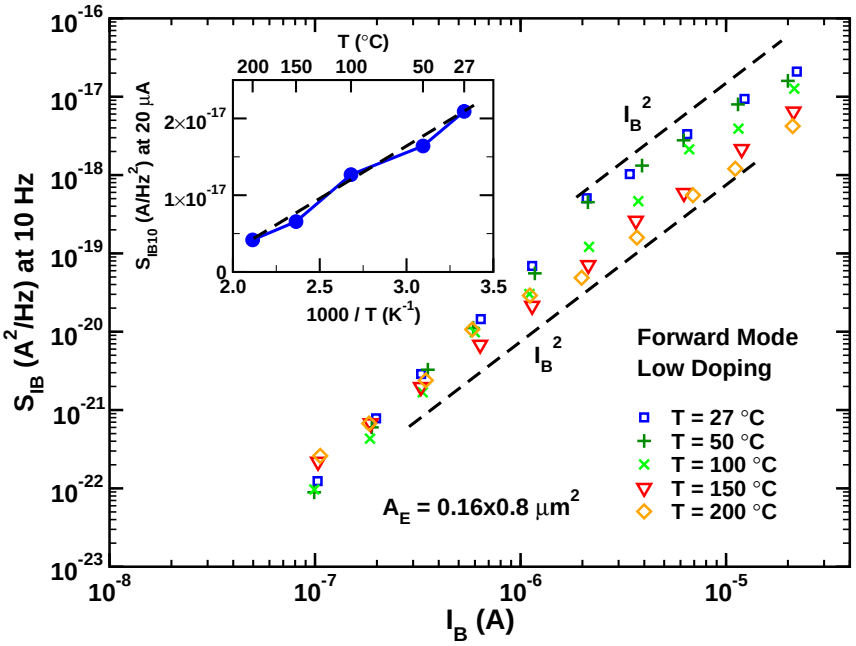


Figure 46: Base current noise power spectral density S_{IB} interpolated at 10 Hz versus base current I_B for a fully depleted HBT-on-SOI measured in the temperature range between 27 °C and 200 °C, showing a clear I_B^2 dependence. The inset shows that at high currents S_{IB} exhibits a $1/T$ trend.

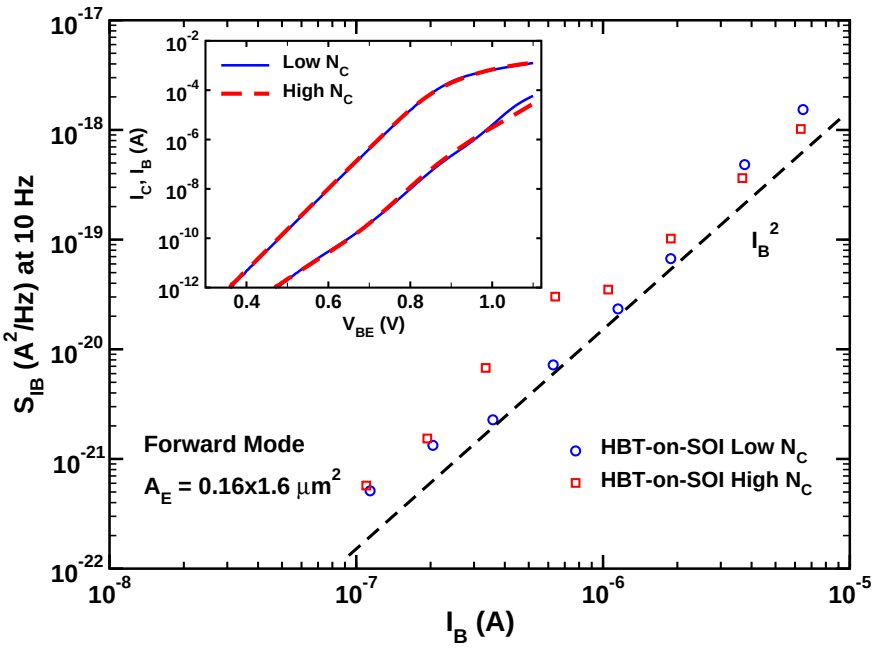


Figure 47: Base current noise power spectral density S_{IB} interpolated at 10 Hz versus base current I_B for a fully depleted (low N_C) and a partially depleted (high N_C) HBT-on-SOI measured at room temperature, showing a clear I_B^2 dependence. The inset compares the Forward Gummel plots of the two devices.

depleted devices results in lower collector resistance and lower quasi-saturation and HBE effect, as shown in the inset of Figure 47, in better *ac* performance but in higher impact ionization [16]. From an application perspective its very relevant to notice that the choice between fully and partially depleted collector comes with no tradeoff as long as $1/f$ noise performance is involved.

This result is consistent with the limited impact of substrate voltage on $1/f$ noise shown in Figure 44, and suggests that while care should be taken in the fabrication process to obtain the same EB interface quality as in the bulk devices, the adoption of a folded collector structure per se does not degrade low-frequency noise performance, which is good news.

Figure 48 shows the $1/f$ noise spectrum for the Inverse Gummel mode. Although the inverse mode operation of SiGe HBT has recently been analyzed in [1] for possible applications, our focus in this paper is limited to comparing the HBT-on-SOI and the bulk device to investigate the possible presence of defects caused by the different fabrication processes.

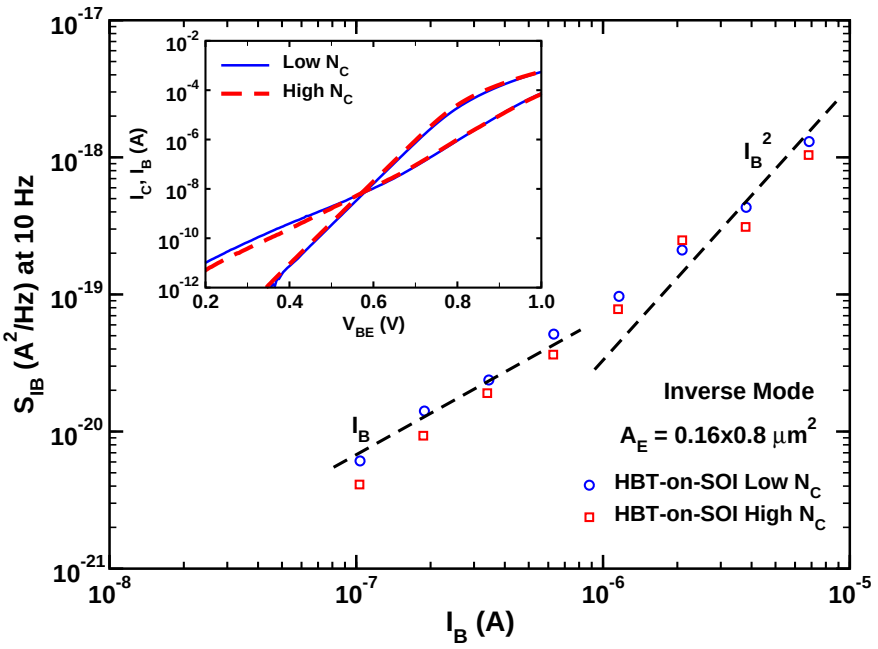


Figure 48: Base current noise power spectral density S_{IB} interpolated at 10 Hz versus base current I_B for a fully depleted HBT-on-SOI and a bulk HBT operated in the Inverse Mode (emitter and collector swapped) and measured at room temperature, showing different I_B dependences. The inset compares the Inverse Gummel plots of the two devices.

As shown by the inset, the inverse mode I_B shows a large leakage which is a telltale of significant presence of traps in proximity of the physical CB junction. Moreover, the inverse mode collector currents of the two devices do not match, which is expected given the different physical collector doping of the devices. The measured low noise spectra show a clear $1/f$ frequency dependence and since the devices possess a significant gain even in the inverse mode, S_{IB} and S_{IC} show very good coherence, proving the inverse mode base current is the dominant noise source. Since estimating the inverse mode "emitter areas" is no trivial task, the $1/f$ spectra could not be normalized by area. Although it would be preferable to have device with identical dimensions, its important to remark that the geometries of the two devices are quite similar, with a difference in forward mode emitter areas of only 6.25 %. Interestingly, the two devices exhibit a qualitatively different low-frequency noise behavior. While $1/f$ noise in the bulk device follows a clear I_B^2 dependence, the HBT-on-SOI shows a I_B^2 trend only at high I_B with a linear dependence on I_B at low base current suggesting that in this current range noise originates from carrier mobility fluctuations. The

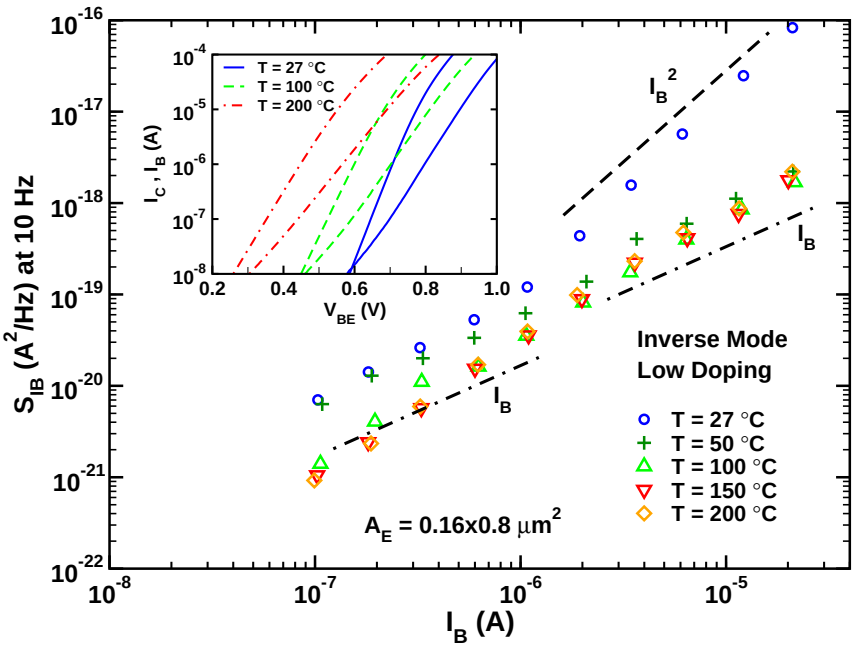


Figure 49: Base current noise power spectral density S_{IB} interpolated at 10 Hz versus base current I_B for a fully depleted (low N_C) HBT-on-SOI operated in the Inverse Mode (emitter and collector swapped) and measured in the range of temperatures between 27 °C and 200 °C. The inset compares the behavior of the Inverse Gummel plots with increasing temperature.

I_B dependent $1/f$ noise spectrum is consistent with the presence of a large leakage current resulting from space-charge region G/R recombination centers as observed in [42][36] and in previous studies on the proton irradiation response in bulk SiGe HBTs [89][38]. Finally, Figure 49 analyzes the temperature dependence of the inverse mode low-frequency noise in the fully depleted HBT-on-SOI in the temperature range between 27 °C and 200 °C.

The trend shown in Figure 48 changes significantly with temperature: S_{IB} shows a linear dependence with I_B in the whole I_B range, instead of showing a quadratic dependence at high I_B. This behavior can be explained observing the trend in the Inverse Gummel plot with temperature shown in the inset of Figure 49. As expected the leakage component of the base current increases significantly with temperature, leading to a linear I_B dependence in S_{IB}. Also, in accord with the behavior shown in the forward mode in Figure 48, the low-frequency noise decreases with temperature.

To conclude, the low-frequency noise characteristics of both fully and partially depleted

SiGe HBTs-on-SOI have been reported for the first time, comparing the novel folded collector structure with traditional vertical structure and analyzing the impact on $1/f$ noise of substrate voltage, collector doping and temperature. HBTs-on-SOI exhibit higher noise compared to bulk devices possibly because of the presence of a thicker interfacial oxide at the emitter-base junction. On the other hand, collector doping and substrate bias, which dramatically affect the *ac* and *dc* performance of SOI devices, are shown to have no impact on $1/f$ noise. As reported in literature, $1/f$ noise measured in the forward active mode shows a quadratic dependence on base current I_B and an inverse dependence on emitter area A_E. Finally, to gain more insight on the fabrication process, the low-frequency noise in the inverse mode is measured, showing that the large base leakage translates in a significant noise spectrum S_{IB} which follows an I_B dependence at low base currents followed by a I_B^2 dependence at high currents.

CHAPTER V

OPERATION IN RADIATION ENVIRONMENTS

Electronic devices and circuits requiring a high degree of radiation hardness are used for satellite navigation, telecommunication and instrumentation, for aerospace and planet exploration, for radiation detectors, for nuclear power plants, and for particle colliders. Radiation environments are characterized by exposure to γ-rays and x-rays, α particles, β particles, electrons, neutrons, and protons with varying levels of fluences.

Radiation affects electron device through three failure mechanisms: total ionizing dose (TID), displacement damage, and single events effects (SEE). Total Ionizing Dose is related to the amount of traps and positive charge created in SiO_2 by the amount of radiation and leads to increased leakage current in bipolar transistors. Displacement damage refers to the formation of defects and doping deactivation caused by the interaction of particles with heavy mass with the semiconductor lattice. Finally, single events effects include transient or permanent circuit malfunctions resulting from the generation of electron-hole pairs in silicon [26].

This chapter initially discusses the total ionizing dose hardness of SiGe HBTs fabricated on thick-film SOI and on thin-film SOI. Thin-film devices with both the conventional and the C_BE^BC layout are also investigated. Then, TCAD simulation studies of single event upset on thin-film devices with C_BE^BC layout are presented.

5.1 Total Ionizing Dose Response of HBTs on thick-film SOI

This section presents an analysis of the impact of radiation on the complementary SiGe HBTs fabricated on thick-film SOI introduced in Section 1.4.1 and compares the radiation response of SiGe HBTs fabricated on thick- and thin-film SOI substrates [11].

Previous studies of this complementary technology focused exclusively on the dependence of 1/f noise on transistor size and temperature and on the degradation of the low-frequency noise after 63.3 MeV proton irradiation [91][90].

The work presented in this section addresses more generally the impact of irradiation on the *ac* and *dc* device performance, particularly as it relates to analog circuit design, and inherent differences between npn and pnp device response. The pnp and npn SiGe HBTs have been irradiated at room temperature with 63.3 MeV protons, to a total fluence of 7.4×10^{12} p/cm^2 (equivalent to 2 Mrad(SiO_2)) and with 10 keV x-rays up to a total dose of 3.6 Mrad(SiO_2). The Gummel characteristics, output characteristics, and avalanche multiplication (breakdown voltage) have been measured as a function of total dose at room temperature for both proton and x-ray irradiated devices. Additionally, a complete *dc* characterization of the SiGe HBTs-on-SOI before and after 63.3 MeV proton irradiation has been performed down to cryogenic temperatures as low as 30 K, to better understand the device response and damage processes. The impact of irradiation on the *ac* performance has also been investigated up to 3 Mrad(SiO_2) for protons and 5.4 Mrad(SiO_2) for x-rays, measuring f_T and f_{max}.

In this experiment, pnp and npn SiGe HBTs with different emitter areas (1.2×2.0 μm^2 and 0.6×4.0 μm^2) were irradiated in de-lidded packages using both 63.3 MeV protons and 10 keV x-rays, up to a total dose of, respectively, 2 Mrad (SiO_2) and 3.6 Mrad(SiO_2), and immediately measured *in-situ*. Two different back substrate voltages V_S (0 V and 20 V) were applied during exposure (with the remaining terminals grounded), to evaluate the possible impact of substrate bias on the radiation response, considering that thin-film SiGe HBTs-on-SOI are significantly affected by V_S [15][16][18]. An additional package was irradiated with protons to a final dose of 3 Mrad(SiO_2) with all terminals grounded, and measured before and after irradiation across the temperature span ranging from 300 K to 30 K. Passive exposure (terminals floating) of *ac* test structures with an emitter geometry of 0.4×0.8 μm^2, and configured in a parallel array of 10×12 npn SiGe HBTs and 0.4×3.2 μm^2 in an array of 10×3 pnp SiGe HBTs, was performed to a dose of 3 Mrad(SiO_2) for protons and 5.4 Mrad(SiO_2) for x-rays. The devices were measured using an Agilent 4155 Semiconductor Parameter Analyzer (*dc*), an Agilent 8510 Vector Network Analyzer (*ac*) and a customized *dc* cryogenic probe station.

Figure 50 shows the radiation-induced degradation with increasing proton dose for the

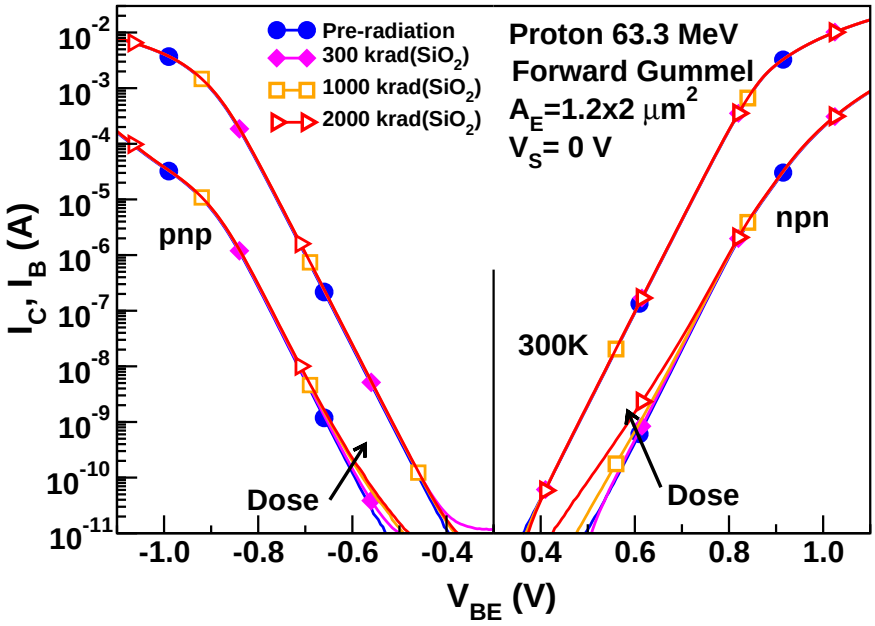


Figure 50: Forward Gummel characteristics of pnp (left) and npn (right) transistors as a function of cumulative proton dose in krad(SiO_2).

forward Gummel characteristics for both the pnp and the npn SiGe HBTs ($A_E = 1.2 \times 2.0$ μm^2).

When the concentrations of holes and electrons are comparable, recombination caused by interface traps is maximized [5][56][84]. In the case of a pnp device, however, positive charge trapped in the oxide accumulates the n-doped base, and the resulting higher electron concentration decreases the excess base current originating from surface recombination. Accumulation in the base also increases the electron current in the emitter, increasing the total base current and thus reducing the overall current gain [66]. Depletion actually occurs in the p-doped emitter, but its impact in this case is negligible because of the high emitter doping [5][66]. From a circuit perspective, the observed radiation-induced degradation in the *dc* characteristics of the transistors — 10% current gain reduction measured at the peak f_T collector current in the npn SiGe HBTs (only 5% in the pnp SiGe HBTs) after the final radiation dose — can be considered negligible for most circuit applications. The normalized excess current $\Delta I_B / I_{B0}$ exhibits a linear dependence on the perimeter-to-area

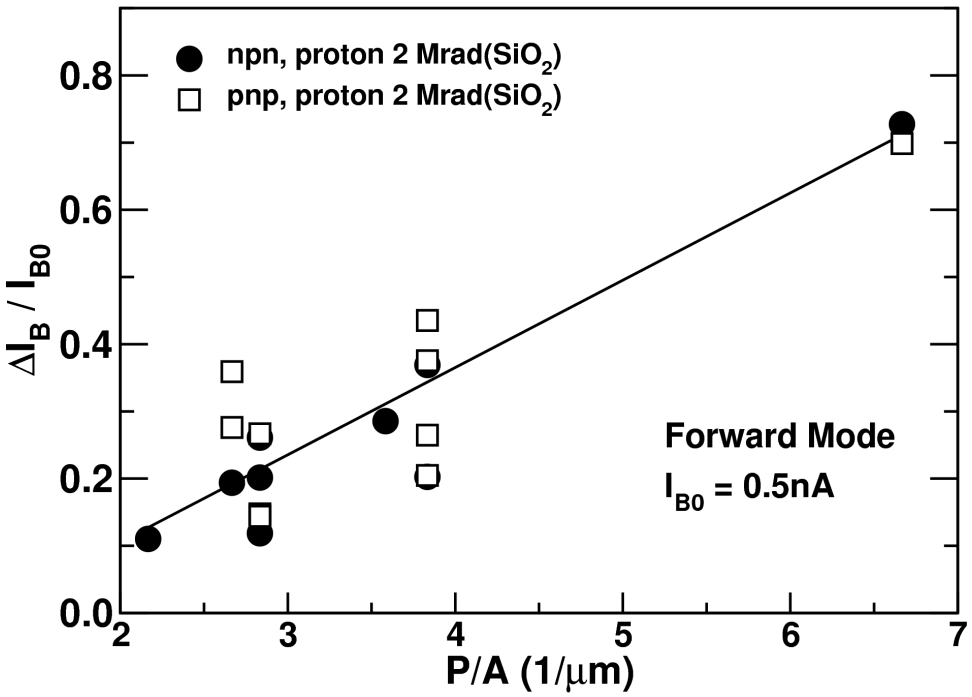


Figure 51: Excess normalized base current $\Delta I_B/I_{B0}$ versus emitter perimeter over area ratio of the thick-film SiGe HBT-on-SOI.

ratio P/A, as shown in Figure 51 and suggests the presence of recombination resulting from interface traps located at the Si/SiO_2 interface, surrounding the periphery of the EB junction [5][43][57][30]. Also, the radiation response of these thick-film SOI devices is much closer to that of a traditional bulk SiGe HBT than to a SiGe HBT on thin-film SOI, such as described in [16]. The thick SOI layer and the highly doped sub-collector result in a completely vertical current flow that is not affected by V_S or irradiation, as evidenced by the lack of substrate effect on I_B, I_C or on the collector resistance R_C [15][16][10].

The inverse mode (emitter and collector terminals swapped) Gummel characteristics, shown in Figure 52 for proton irradiation, show for both devices an excess base current ΔI_B larger than in the forward mode.

Surprisingly, the degradation in inverse mode is larger for devices irradiated with V_S = 0 V than for those irradiated with V_S = 20 V, while the forward mode shows no such substrate bias dependence (Figure 53).

This trend has been also confirmed with x-ray irradiation, as shown in Figure 54.

As can be seen in Figure 55, TCAD simulations employing ISE-DESSIS, as described in

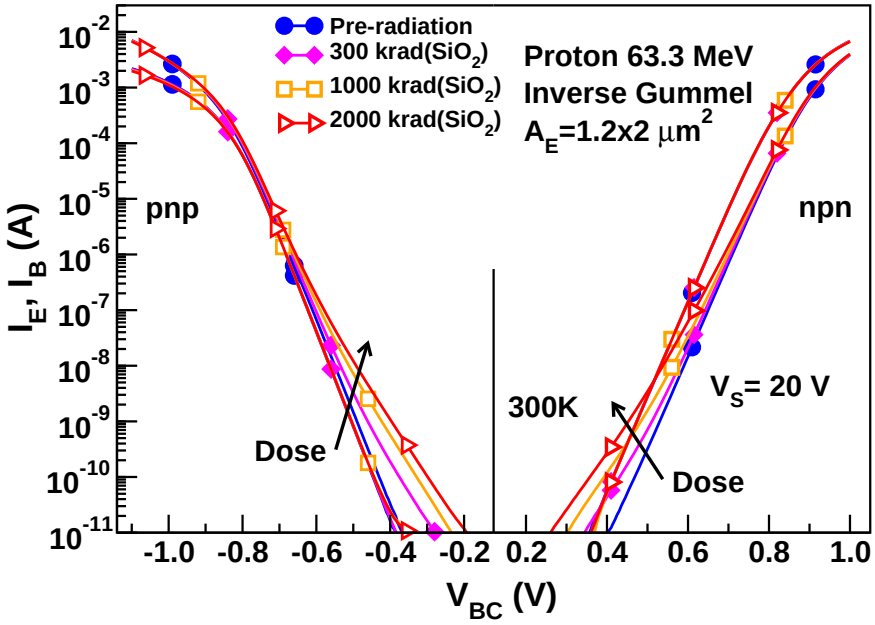


Figure 52: Inverse Gummel characteristics of pnp (left) and npn (right) transistors as a function of cumulative proton dose in krad(SiO_2).

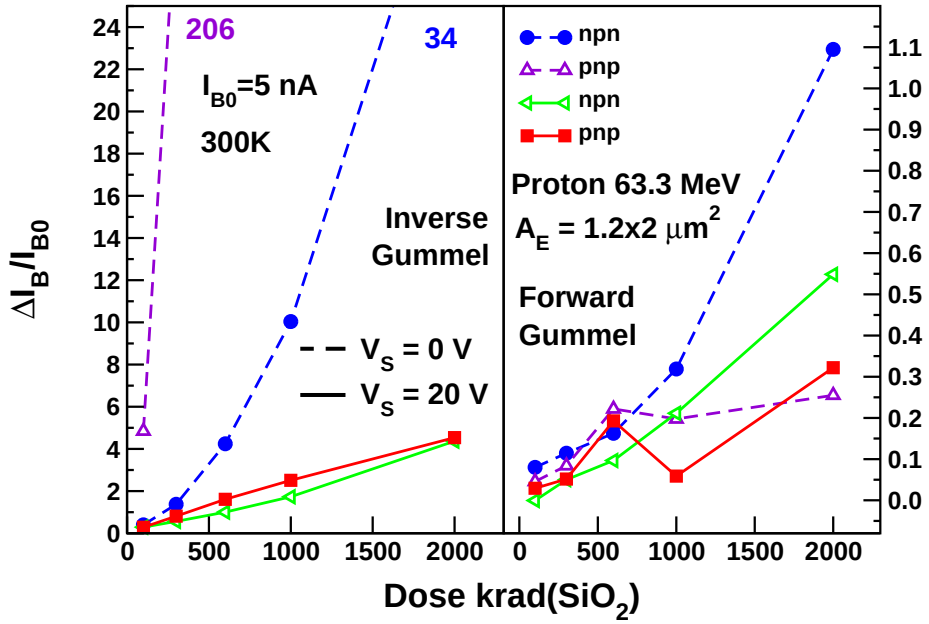


Figure 53: Excess normalized base current $\Delta I_B/I_{B0}$ versus cumulative proton radiation dose in krad(SiO_2) for both devices in forward and inverse mode operation.

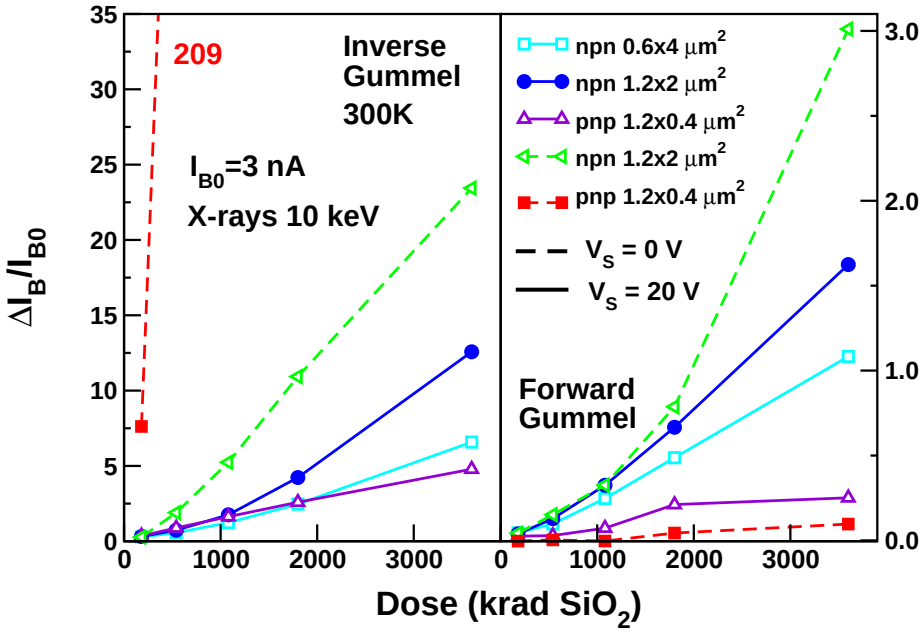


Figure 54: Excess normalized base current $\Delta I_B/I_{B0}$ versus cumulative x-ray radiation dose in krad(SiO_2), for both devices in forward and inverse mode operation.

[10][37], confirm that biasing the substrate results in a significantly larger positive charge in the BOX and DT with respect to a device irradiated with a grounded substrate.

The higher positive charge yield is caused by the applied electric field that more efficiently separates the electron-hole pairs generated in the oxide by the incident radiation [59], as confirmed by the electric field plot in Figure 56. In addition, simulations show no charge variation with changing substrate bias in the EB and STI oxides near the EB and CB junctions, respectively, which is consistent with the fact that substrate voltage has no effect on the *dc* and *ac* characteristics.

Given that temperature has a significant impact on SiGe HBT physics, the pre- and post-irradiation *dc* behavior of the devices was measured over a wide temperature range to gain better insight into the relevant damage mechanisms. Figure 57 shows the forward Gummel characteristics of the pnp and npn SiGe HBTs, both before and after irradiation, measured at temperatures of 300 K, 150 K, and 30 K. The base current of the pnp device shows a "hump" at moderately high $|V_{BE}|$, caused by the accumulation of holes in the base

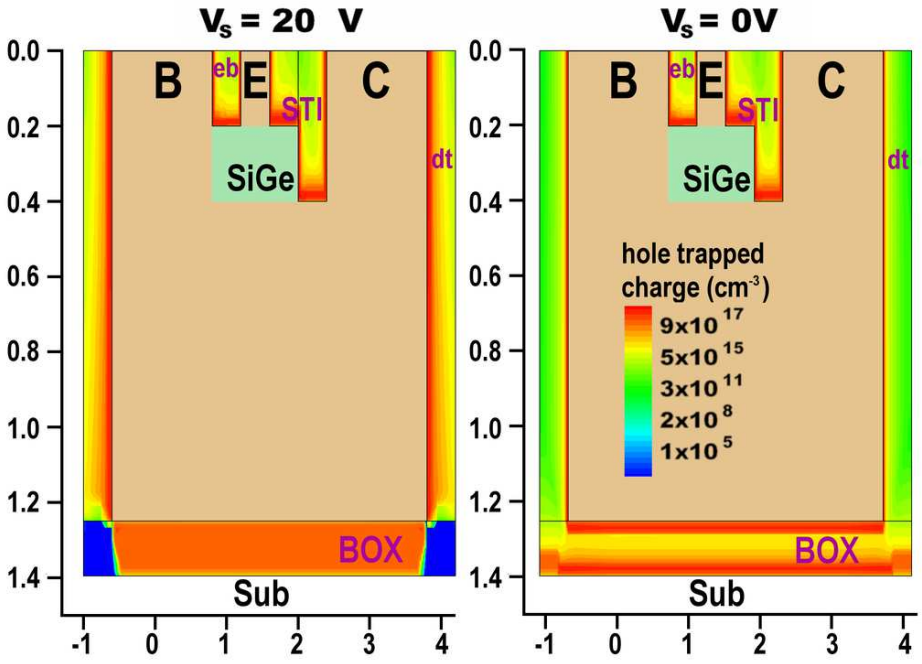


Figure 55: ISE-DESSIS TCAD simulation of oxide trapped charge in a npn transistor irradiated at a 2.1 Mrad(SiO_2) dose.

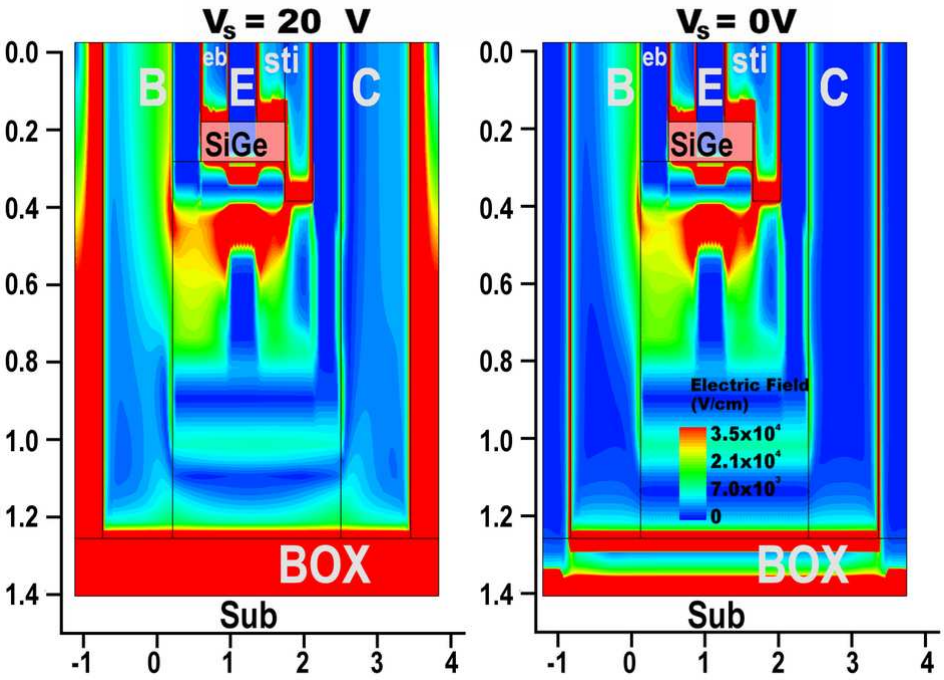


Figure 56: ISE-DESSIS TCAD simulation of electric field in a npn transistor irradiated at a 2.1 Mrad(SiO_2) dose.

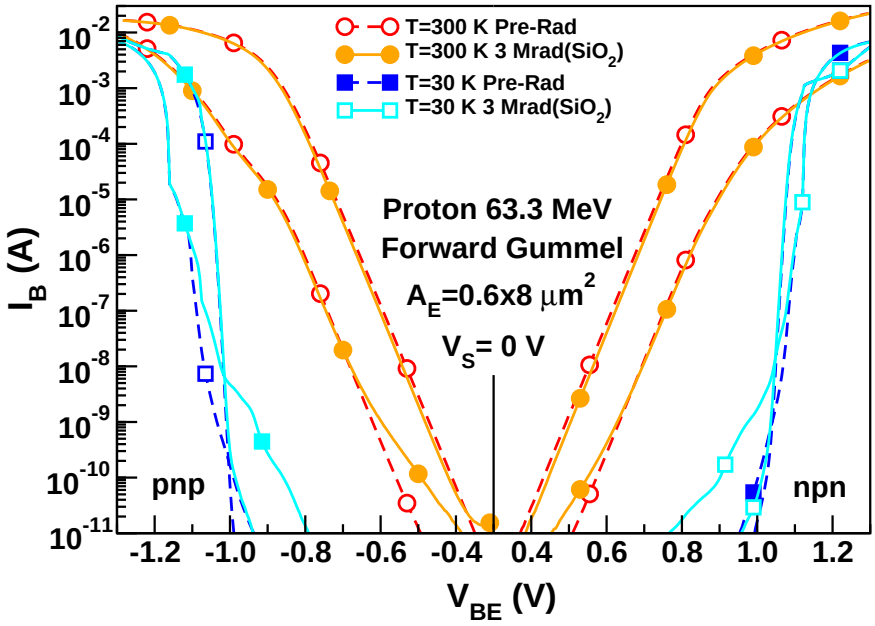


Figure 57: Forward Gummel plot of pnp and npn transistors before and after a 3 Mrad(SiO_2) proton dose at temperatures between 30 K and 300 K.

due to the heterojunction barrier effect (HBE) [26], which is magnified by the relatively low collector doping N_C. The I_C at which HBE occurs in the pnp SiGe HBTs is about 2.4 times higher than for the npn SiGe HBTs, possibly resulting from a higher local N_C. As shown by Figure 58, the ideality factor (n) of the excess base current ΔI_B is around 1.7 at 300 K, confirming an interface trap origin of ΔI_B at the Si/SiO_2 interface around the EB junction, as suggested also by Figure 51. At 150 K n rises to 3 and at 30 K it surpasses 10, implying that a trap-assisted tunneling mechanism is dominant at low temperatures [87]. It should be noted that a very high ideality factor n was observed also in the 300 K irradiation of a first generation npn bulk SiGe HBT when measured at 77 K, but not when the device was irradiated and measured at 77 K [63].

The forward current gain β at low temperatures is limited at high I_C by the HBE effect. The radiation-induced degradation in β, however, is negligible at collector currents used in most practical circuits. Interestingly, the inverse mode behavior at low temperatures

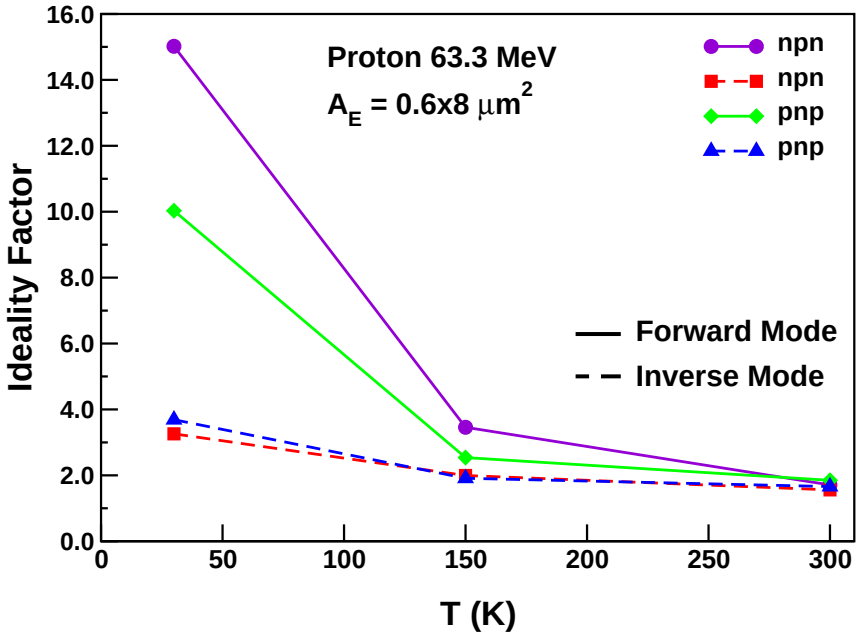


Figure 58: Ideality factor n of excess base current ΔI_B versus temperature for pnp and npn transistors.

displays an excess base current ΔI_B smaller than that for forward mode operation, suggesting that the degradation in forward mode I_B at low temperatures may be caused by traps generated in the IFO itself or at the IFO-silicon interface, consistent with [91]. The inverse mode excess I_B ideality factors n are about 1.5, 2, and 3 at 300 K, 150 K and 30 K, respectively.

Conversely, fully depleted SiGe HBTs on thin-film SOI are typically characterized by a significant change in M-1 with applied substrate bias or irradiation, and partially depleted SiGe HBTs on thin-film SOI by a small but noticeable change in M-1, as discussed in [16][10]. This suggests again that in SiGe HBTs on thick-film SOI, the current flow remains completely vertical, even after irradiation. Radiation has negligible effect on the M-1, B_{VCBO} and B_{VCEO}, similar to the vertical bulk devices. This is an important result, since one of the highlights of this technology is the large breakdown voltage ($>$ 5 V at 300 K), especially in comparison to fully depleted thin-film SiGe HBTs-on-SOI, in which radiation increases *ac* performance at the expense of avalanche multiplication, clearly a potential

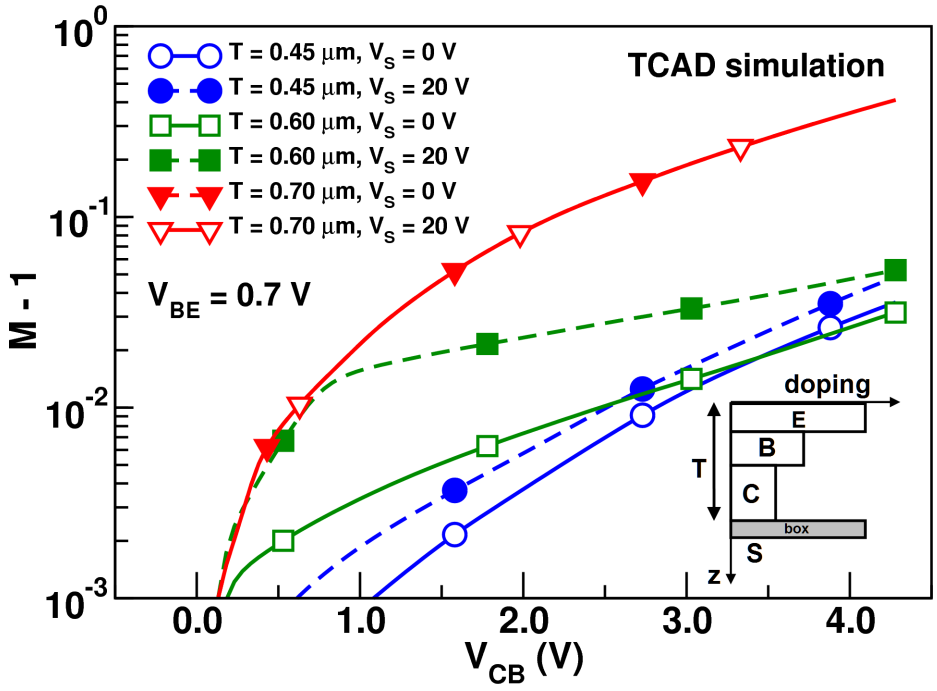


Figure 59: TCAD simulation of impact ionization at $V_{BE} = 0.7$ V and $V_S = 0$ V and $V_S = 20$ V at different SOI thicknesses (T).

reliability issue. TCAD simulations shown in Figure 59 indicate that the limited impact of substrate voltage and hence radiation-induced charge at the SOI/BOX interface is caused by the thickness of the SOI layer rather than by the collector doping N_C.

Finally, *ac* measurements of both npn SiGe HBTs (Figure 60 and 61) and pnp SiGe HBTs, before and after a 3 Mrad(SiO_2) 63.3 MeV proton dose and a 5.4 Mrad(SiO_2) 10 keV x-ray dose, show negligible degradation in f_T and f_{max}, within the measurement error of around $\pm 5\%$, clearly good news for use of this technology in circuit applications. The forward transit time τ_f and the total EB and CB capacitance per emitter area $C'\tau$, extracted according to [26] confirm that irradiation does not affect the intrinsic device performance. This conclusion is supported by the fact that the dynamic base resistance r_{bb} extracted from h_{11} using a "circle impedance" extraction technique [26] shows changes lying well within measurement and extraction error. Furthermore, the close agreement between τ_f, $C'\tau$ and r_{bb} from devices before and after irradiation and the negligible change in the f_T — I_C roll-off shown in Figure 60 and 61 suggest that displacement-induced acceptor deactivation in the

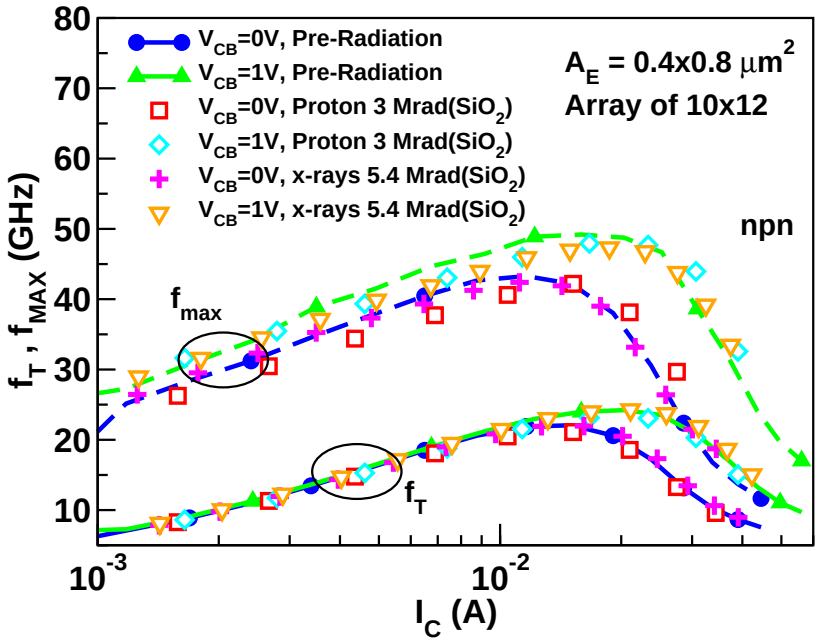


Figure 60: Plot of the *ac* performance of npn SiGe HBT before and after a 3 Mrad (SiO_2) proton and a 5.4 Mrad (SiO_2) x-ray dose measured with $V_{CB} = 0$ V and $V_{CB} = 1$ V.

base is not a concern in this technology [49].

To conclude, the work presented in this section provides a comprehensive analysis of proton and x-ray induced radiation response of the *ac* and *dc* characteristics of a complementary thick-film SiGe HBT-on-SOI technology. Substrate bias has been shown to affect the degradation in inverse mode but not in forward mode. Also, *dc* characterization of the devices down to cryogenic temperatures is used to highlight interface trap formation in different regions. TCAD simulations have been used to understand the differences between thick- and thin- film SiGe HBTs-on-SOI. In summary, these findings suggest that this C-SiGe HBT on thick-film SOI technology offers considerable potential in the context of analog/mixed-signal circuits found in space systems.

5.2 Total Ionizing Dose Response of HBTs on thin-film SOI with conventional layout

This section describes studies on total ionizing dose effects on both fully depleted and partially depleted SiGe HBTs-on-SOI described in Section 1.4.2 [10].

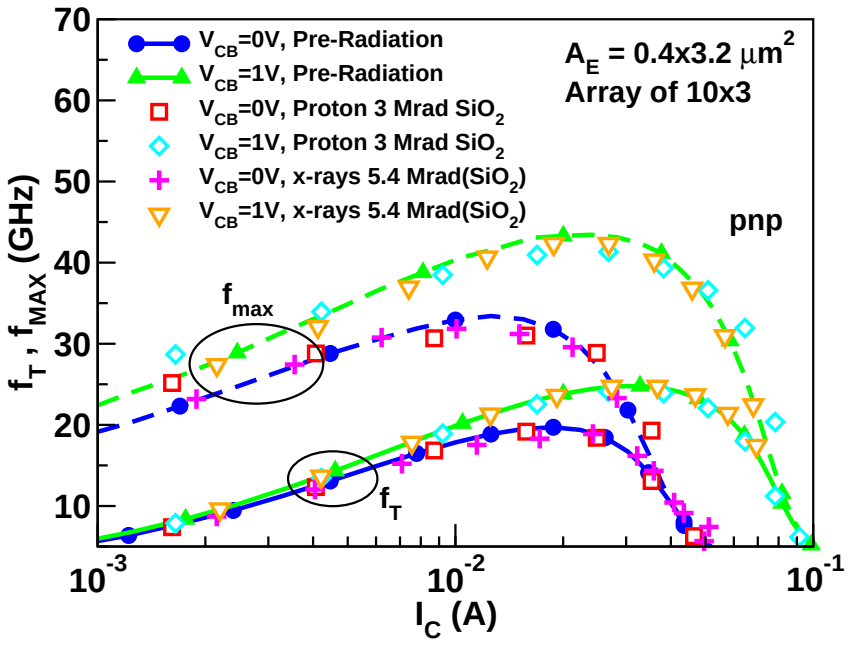


Figure 61: Plot of the *ac* performance of pnp SiGe HBT before and after a 3.15 Mrad (SiO_2) proton and a 5.4 Mrad (SiO_2) x-rays dose, measured with $V_{CB} = 0$ V and $V_{CB} = 1$ V.

The devices were irradiated at 300 K with 10 keV x-rays up to a total dose of 5.8 Mrad(SiO_2) which corresponds to 3.2 Mrad(Si). Gummel characteristics, output characteristics, and avalanche multiplication (which determines the breakdown properties) have been measured as a function of dose at room temperature. Measurements at cryogenic temperatures both prior to and subsequent to irradiation at a total dose of 1.3 Mrad(SiO_2) have been compared to aid in the analysis and understanding of the results. The two-dimensional nature of the electric field and current flow paths in the device are analyzed using advanced TCAD simulations.

In a previous study, the low collector doping SiGe HBT-on-SOI was exposed with grounded terminals to 63 MeV proton radiation with a fluence as high as 5×10^{13} p/cm^2 (6.8 Mrad(SiO_2)), showing that the positive trapped charge generated in the buried oxide (BOX) has an effect on quasi-saturation, R_C, and avalanche multiplication, which is electrically similar to an increase in V_S [18]. A significant improvement in f_T and f_{max} was also observed after proton radiation exposure (a radiation-induced improvement clearly atypical for most devices), and was explained by a delay of high injection effects in the collector. In this work, both the low and high collector doping devices are irradiated with grounded terminals, as well as under forward active bias. Although the literature shows that, for traditional bulk bipolar devices, the grounded terminal case usually shows worse degradation than the forward active mode [56][84][85][5], the two-dimensional nature of the electric field and current flow and their strong dependencies on both V_{CB} and V_S suggest the importance of investigating such bias effects in these SiGe HBTs-on-SOI. The spatial dependence of avalanche multiplication has also been used to as an experimental tool to understand the effects of bias on the electric field inside the 2-D collector region of the transistor.

Low- (fully depleted) and high-collector doping (partially depleted) SiGe HBT-on-SOI devices of different emitter areas (0.16×0.8 μm^2 and 0.16×1.6 μm^2), both grounded and in forward-active bias configuration ($V_{BE} = 0.8$ V, $V_{CB} = 0.5$ V), were irradiated with 10 keV x-rays, at doses of up to 5.8 Mrad(SiO_2) at a dose rate of 540 rad(SiO_2)/s. Radiation is known to increase the base leakage current because of two effects: creation of positive charge in the emitter-base (EB) oxide spacer and increase of the number of traps at the

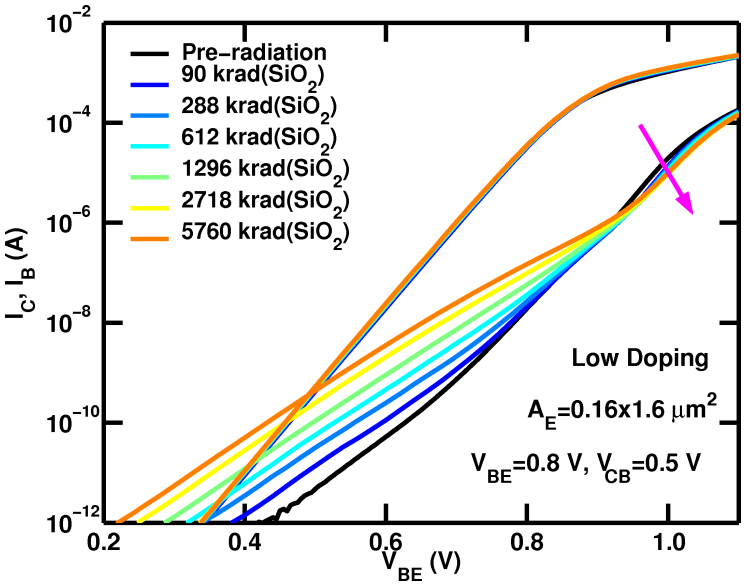


Figure 62: Gummel characteristics of fully depleted SiGe HBT-on-SOI as a function of cumulative x-rays dose in krad(SiO_2). The equilibrium dose in Si is 1.8 times lower. The device is irradiated in the forward active mode.

EB spacer oxide/silicon interface, which results in increased surface recombination velocity [56][84][85][5].

Figure 63 shows the increase in base current I_B in a low collector doping, biased device. Even at the highest dose, the device still exhibits a current peak gain of 400, clearly sufficient for most applications. The accumulation of positive charge in the buried oxide reduces the magnitude of quasi-saturation effects, consistent with the results of [16].

Figure 63 compares the degradation in excess base current density ΔJ_B versus total dose, for a measurement bias of $V_{BE} = 0.6$ V and both irradiation biases. The similarity of the curves suggests that bias during radiation exposure has little effect on the low doping devices, in agreement with the literature [56][84][85][5]. Interestingly, degradation resulting from 63 MeV proton irradiation seems to be about three times lower than observed here for x-rays, as observed also (and discussed) in [78]. However, for the high doping devices the differences in ΔJ_B between the grounded and forward-biased irradiation conditions are pronounced. ISE DESSIS v.10 [37] has been used to evaluate oxide trap charge buildup during irradiation, employing a detailed mesh structure with collector profiles obtained from process simulation, allowing for electron-hole pairs generation corresponding to a dose of 1.3

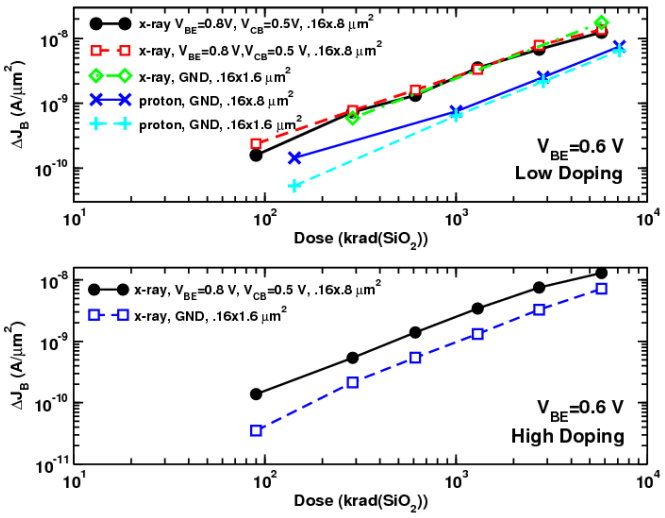


Figure 63: Excess base current density ΔJ_B versus cumulative radiation dose (proton and x-rays) for fully depleted (above) and partially depleted (below) SiGe HBT-on-SOI.

Mrad(SiO_2), and self-consistently solving the Poisson and drift-diffusion equations inside the oxides [37].

Figure 64 shows the simulated positive charge distribution in the oxides for the low N_C SiGe HBT-on-SOI both, for the biased and grounded cases. Observe that the biased device shows an amount of oxide charge in the EB spacer comparable to the grounded one, less charge in the shallow trench insulation (STI) oxide, but more charge in the buried oxide, leading to an alteration of the resultant electric field in the device. M-1 has been measured *in-situ*, using techniques described in [48] , and agrees well with previous experiments involving 63 MeV proton irradiation [16].

Figure 65 shows the effect of x-rays on M-1 for a given substrate voltage V_S, for the low N_C device. At $V_S = 10$ V, an increasing radiation dose reduces M-1, while for V_S=0 V, M-1 increases; for $V_S = 20$ V, M-1 decreases once more. The same trend can be observed for M-1 of the pre-irradiation device with increasing V_S. As explained before, this is caused by the creation of an accumulation layer, which alters the two-dimensional electric field and shifts its peak from the lateral current flow path to the vertical path [18]. The decrease of M-1 at $V_S = 20$ V after irradiation is possibly resulting from shielding effects associated with the accumulation layer [18].

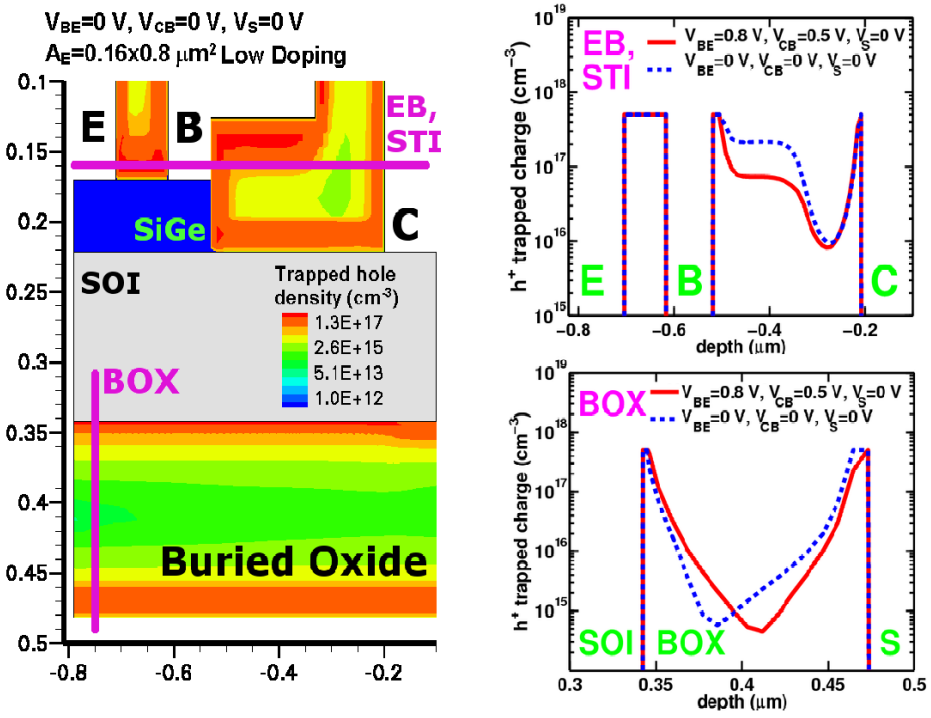


Figure 64: DESSIS simulation of accumulated positive charge in the isolation oxides for a fully depleted SiGe HBT-on-SOI.

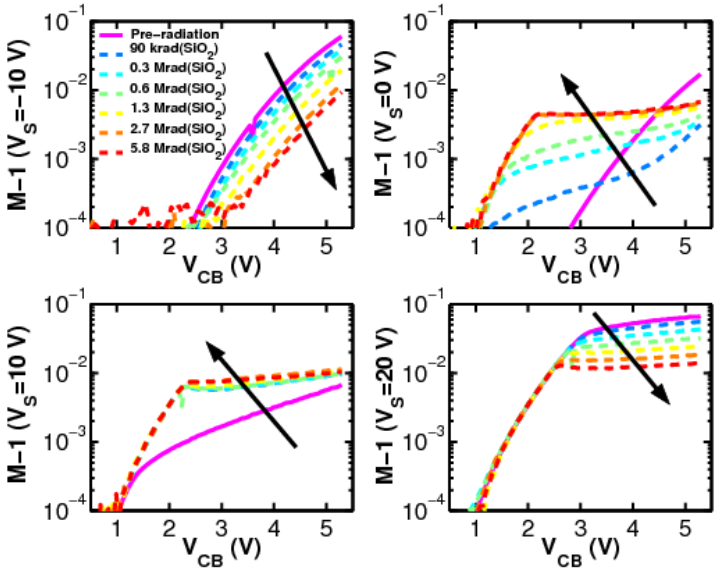


Figure 65: M-1 versus V_{CB} at different V_S for the fully depleted SiGe HBT-on-SOI as a function of cumulative dose.

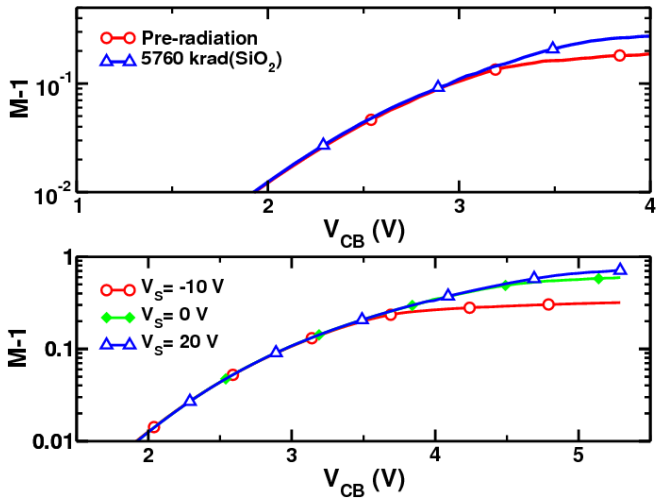


Figure 66: (a) M-1 versus V_{CB} for the partially depleted SiGe HBT-on-SOI before and after a total dose of 5.8 Mrad(SiO_2). (b) M-1 versus V_{CB} for the partially depleted SiGe HBT-on-SOI versus substrate voltage V_S.

The higher collector doping N_C of the partially depleted device results in little change of M-1 even after a total radiation dose of 5.8 Mrad(SiO_2), as displayed in Figure 66 (a). This is consistent with the small variations of M-1 with V_S, shown in Figure 66 (b), which result from the dominance of the vertical current flow path, as confirmed by TCAD simulations. The *dc* characteristics of a low doping SiGe HBT-on-SOI were measured, before and after a total radiation dose of 1.3 Mrad(SiO_2), using a custom *dc* cryogenic probe station.

Figure 67 shows the forward Gummel characteristics across the temperature range of 300 K to 60 K. The excess base current density ΔJ_B introduced by radiation is modest, especially at lower temperatures, because of the reduction of trap-induced generation processes. This results in a peak post-irradiation current gain β in excess of 2,500 at 60 K, compared to a pre-irradiation β of more than 9,000, as shown in Figure 68.

Although TCAD simulations indicate significant accumulation of positive oxide charge in the STI oxide with irradiation, the inverse mode Gummel characteristics exhibit a high base leakage current, even at low temperatures, making it hard to quantify the effects of radiation. Such leakage is probably resulting from interface defects introduced by the SOI fabrication process.

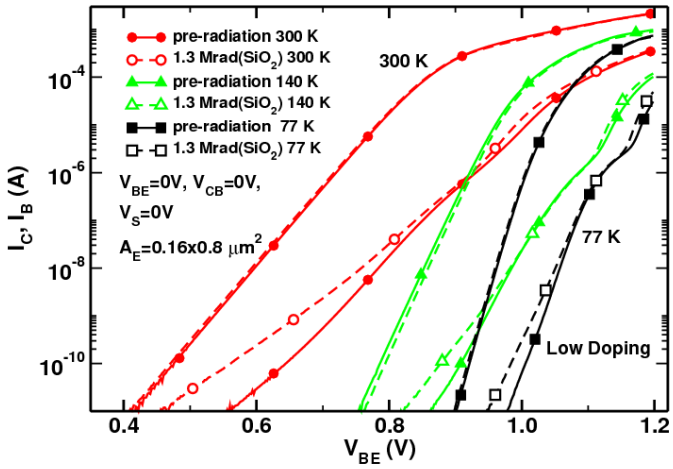


Figure 67: Forward Gummel characteristics of fully depleted SiGe HBT-on-SOI before and after a 1.3 Mrad(SiO_2) x-rays dose at temperatures of 300 K, 140 K, 77 K, and 60 K. The device is irradiated with grounded terminals.

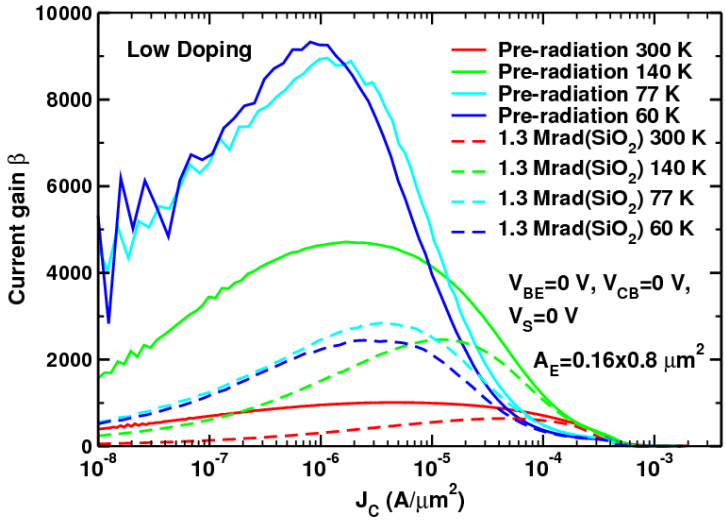


Figure 68: Current gain before and after a 1.3 Mrad(SiO_2) x-rays dose at temperatures of 300 K, 140 K, 77 K, and 60 K for a fully depleted SiGe HBT-on-SOI. The device is irradiated with grounded terminals.

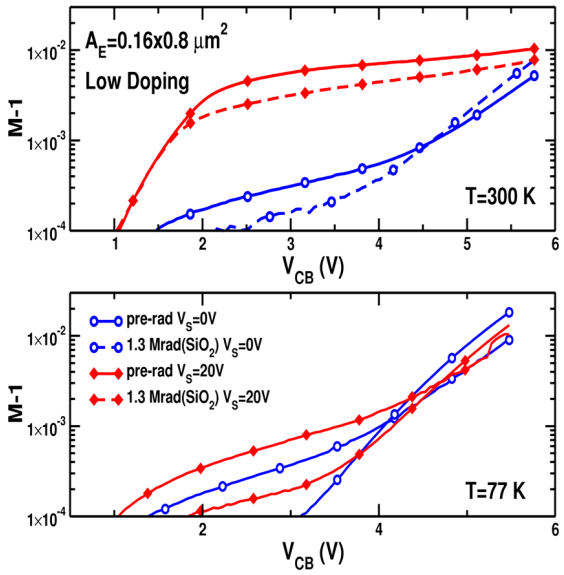


Figure 69: Avalanche multiplication for a fully depleted SiGe HBT-on-SOI before and after a 1.3 Mrad(SiO_2) x-rays dose at temperatures of 300 K and 77 K with a substrate voltage V_S of 0 V and 20 V. The device is irradiated in the forward active mode.

Figure 69 shows the avalanche multiplication for a fully depleted HBT-on-SOI at 300 K and at 77 K, for both the grounded substrate and the $V_S = 20$ V conditions. The shape of M-1 suggests that at low temperature avalanche multiplication occurs mainly in the lateral current path, even for high V_S, as confirmed by TCAD simulations. It should be noted that at low temperatures the effects of both substrate voltage V_S and of radiation on M-1 are much more modest than at room temperature.

Figure 70 shows the breakdown voltage B_{VCEO} extracted from the $I_B = 0$ point. Both pre-irradiation and post-irradiation B_{VCEO} decrease with decreasing temperature as a result of increased M-1, because of the longer carrier mean free path length and enhanced impact ionization at low temperatures [33]. Given the small change in the magnitude of M-1 with irradiation, the marked reduction in β can explain the increase of B_{VCEO} with radiation total dose.

To conclude, the comparison of the effects of proton and x-ray irradiation on a novel fully depleted SiGe HBT-on-SOI device shows that the amount of degradation introduced by protons is about three times lower than degradation caused by x-rays at similar doses. Partially-depleted SiGe HBT-on-SOI devices have been also investigated, displaying more

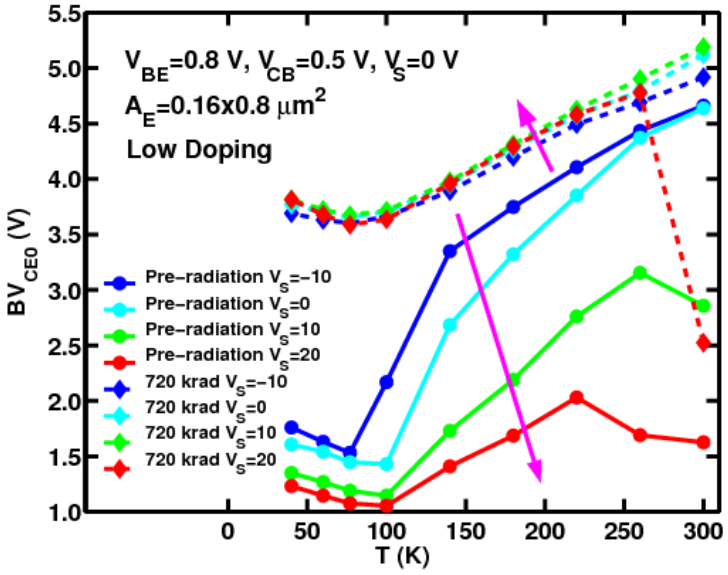


Figure 70: B_{VCEO} versus temperature before and after a 1.3 Mrad(SiO_2) x-rays dose for the fully depleted SiGe HBT-on-SOI. The device is irradiated in the forward active mode.

damage when irradiated with x-rays in the forward active mode than with grounded terminals. Finally, the *dc* characteristics of a fully depleted SiGe HBT-on-SOI have been compared before and after irradiation in the temperature range between 300 K and 60 K, highlighting the potential of this device for potential planetary exploration applications.

5.3 Total Ionizing Dose Response of HBTs on thick-film SOI with C_BE^BC layout

This section investigates radiation-induced effects on the *dc*, *ac* and thermal characteristics of the SiGe HBTs on thin-film SOI with advanced layout described in Section 1.4.3[3].

For the first time, the radiation response of this SiGe HBT-on-SOI is compared with that of a bulk SiGe HBT fabricated with an identical emitter-base structure. That is, the only differences between the devices are the substrate (bulk vs. SOI) and the collector doping. More importantly, the devices under study feature an innovative C_BE^BC layout (with off-plane base contacts, as shown in the inset of Figure 10) which significantly improves the *ac* performance. This section analyzes for the first time the impact of the novel C_BE^BC layout on total ionizing dose (TID). Experimental data and calibrated 3-D TCAD simulations demonstrate that, in the inverse mode, the current flow along the large oxide surface between

the collector and the base can be altered by substrate bias V_S, reducing the radiation-induced leakage.

Finally, for the first time, the thermal resistances (R_{TH}) of the bulk and SOI SiGe HBTs have been compared before and after irradiation over the temperature range from 300 K to 390 K, demonstrating that radiation exposure increases R_{TH} in SOI devices.

In this work both bulk SiGe HBTs and fully depleted SiGe HBTs-on-SOI of effective emitter areas (A_E) of 12×(0.17×0.5) μm^2 and 7×(0.17×0.85) μm^2 were irradiated in de-lidded packages with grounded pins using 63.3 MeV protons, up to a total dose of 2 Mrad (SiO_2), and immediately measured *in-situ*. Passive exposure (terminals floating) of *ac* test structures for both the bulk and SOI devices to a total dose of 4.2 Mrad(SiO_2) was used to quantify the impact of radiation on the *ac* performance.

Figure 71 shows the proton-induced degradation of the forward mode base current I_B with increasing radiation dose, for both a bulk and an SOI SiGe HBT with effective emitter area $A_E = 12\times(0.17\times0.5)\ \mu m^2$.

Figure 72 compares the normalized excess base current in forward and inverse mode. The radiation-induced degradation in the forward mode for both devices is similar, and expected because the transistors have identical emitter-base structures. However, in the case of the SOI device, $\Delta I_B/I_{B0}$ in the inverse mode (E and C swapped) is much larger compared to the forward mode, possibly because of the differences between the composition of the EB oxide and the pedestal oxide (used to separate the collector and the base), of the different emitter and collector doping and of the different geometrical dimensions of the Si/SiO_2 interfaces in both forward and inverse mode. Moreover, Figure 73 shows that applying a positive substrate voltage (V_S) to the SOI device after irradiation reduces the base leakage produced in the inverse mode. The NanoTCAD 3-D TCAD simulation package (previously used to investigate other advanced devices [52][77]) has been used to provide calibrated models of both the SOI and the bulk device in forward and inverse mode.

A trap concentration of roughly $10^{10}\ cm^{-2}$ (as suggested in [47]) was introduced at the pedestal oxide/SOI interface in order to reproduce the non-ideal base current in the inverse mode. The simulations correctly capture the impact of V_S and suggest that the current flow

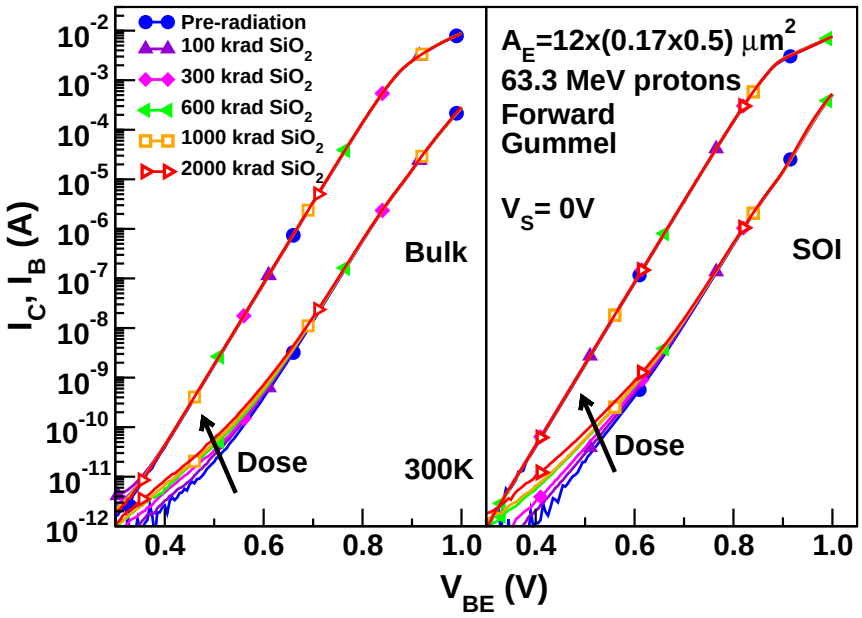


Figure 71: Forward Gummel characteristics of the bulk (left) and SOI (right) transistors as a function of proton dose in krad(SiO_2).

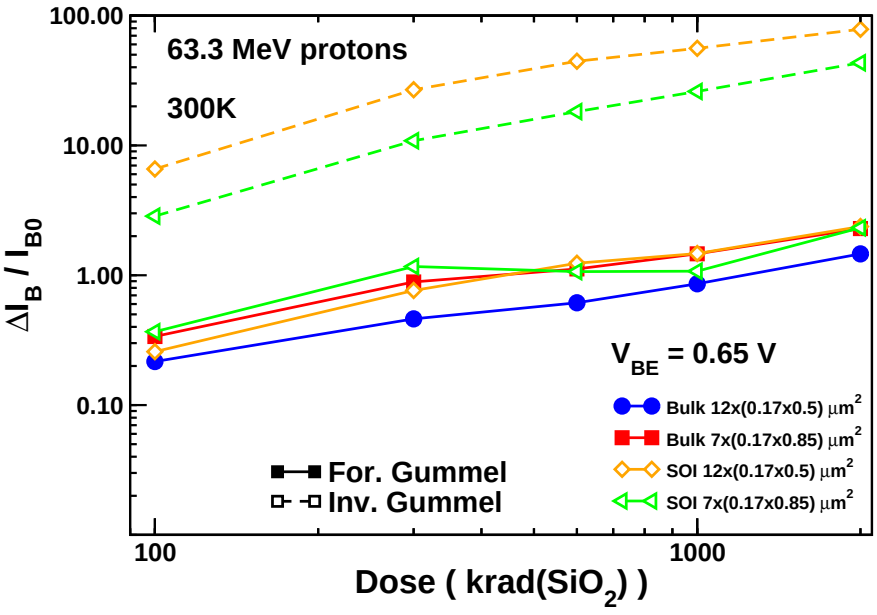


Figure 72: Excess normalized base current $\Delta I_B/I_{B0}$ versus total radiation dose in krad(SiO_2), in forward and inverse mode.

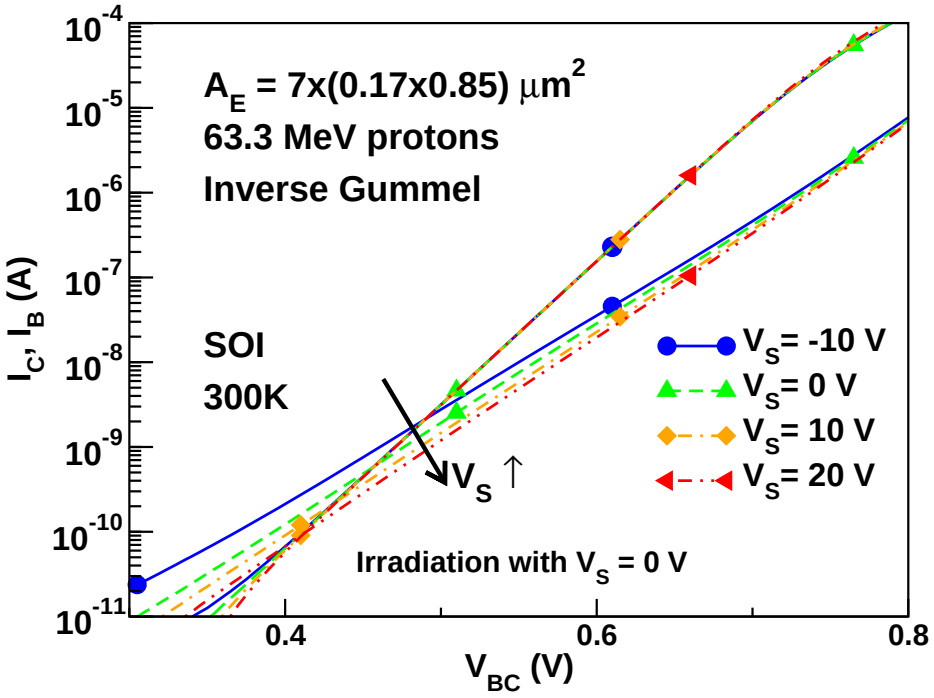


Figure 73: Inverse Gummel of a SiGe HBT-on-SOI after a proton dose of 2 Mrad(SiO_2) as a function of V_S during post-irradiation measurements.

is effectively pushed away from the Si/SiO_2 interface by the applied electric field, decreasing the generation/recombination (G/R)-induced leakage, as shown in Figure 74.

Since the performance of SiGe HBTs is strongly affected by temperature, a partially depleted device is measured before and after irradiation at a proton dose of 4.2 Mrad(SiO_2) in the range of temperatures between 30 K and 300 K, as shown in Figure 75. The pre-radiation forward-mode peak current gain increases from 250 at 300 K to more than 1500 at 77 K because of the presence of germanium in the base. Importantly, after the large 4.2 Mrad(SiO_2) dose, the gain degradation is less than 10% at peak current and is negligible at currents employed in most IC applications. The ideality factor of the excess base current increases significantly (from about 2 at room temperature to more than 40 at cryogenic temperatures), implying that a trap-assisted tunneling mechanism is dominant at low temperatures [87].

As far as *ac* performance is concerned, the bulk devices show no change in f_T and f_{max}. Conversely, Figure 76 shows a reproducible enhancement of the *ac* performance of the fully

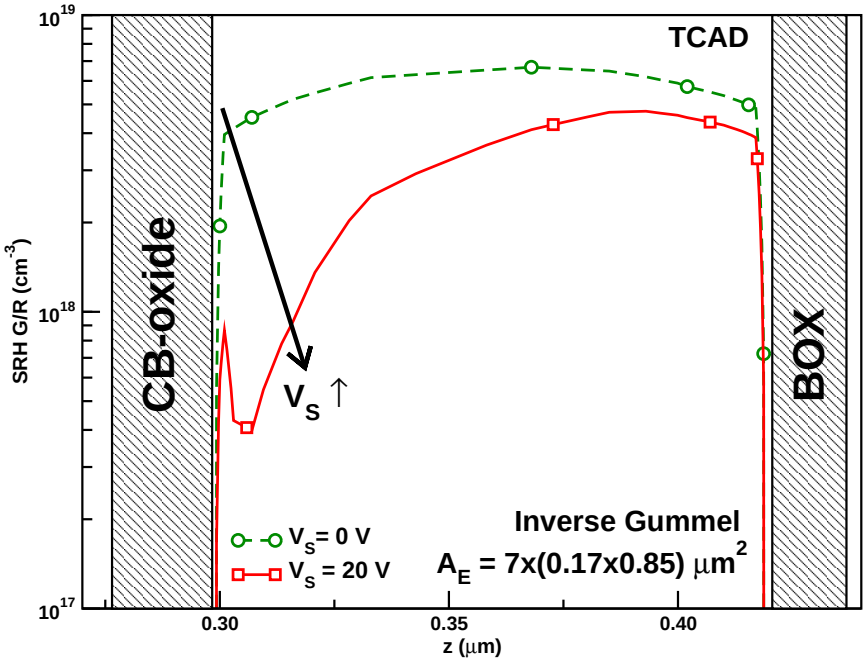


Figure 74: 1-D cut of SRH generation-recombination rate for $V_S = 0$ V and $V_S = 20$ V in the region between the base and the collector, as indicated in the inset.

depleted SiGe HBT-on-SOI after irradiation, in agreement with previous findings [16][18]. Radiation creates positive charge at the SOI/BOX interface, delaying the onset of the Kirk effect and thereby increasing f_T and f_{max} [16]. This is electrically equivalent to applying a higher substrate voltage V_S, as shown in Figure 76. The observed improvement in the *ac* performance is accompanied by a reduction in breakdown voltage, a potential concern for certain circuits.

Figure 77 compares the C_{BC} capacitance of the bulk and SOI devices with $A_E = 5\times(0.17\times1.2)\ \mu m^2$ and $L_C = 0.72\ \mu m$. The observed hump in the C_{BC} characteristic for the SOI device with $V_S = 0$ V has been reported in [31] and explained by the combined expansion of the space charge region in both the vertical and the horizontal directions. Interestingly, the application of substrate bias V_S affects the direction of expansion of the depletion region. As shown in Figure 77, positive V_S results in a predominance of the vertical component (as in the bulk HBTs) making the C_{BC} of the SOI device similar to that of a bulk device. The capacitance C_{BC} of the bulk HBT after irradiation shows a negligible

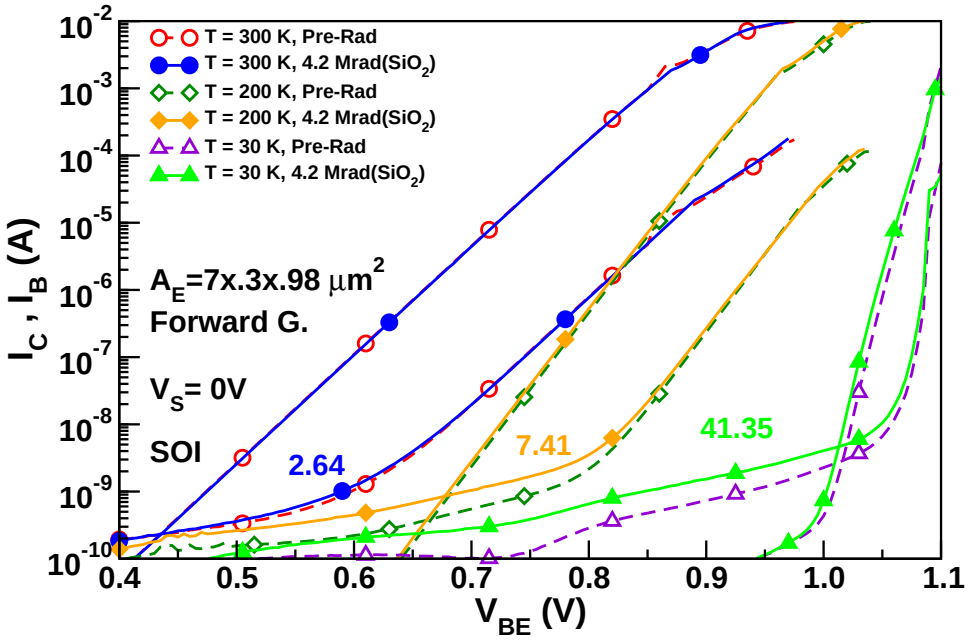


Figure 75: Forward Gummel characteristics of a partially depleted SiGe HBT-on-SOI as a function of temperature before and after a proton dose of 4.2 Mrad(SiO_2).

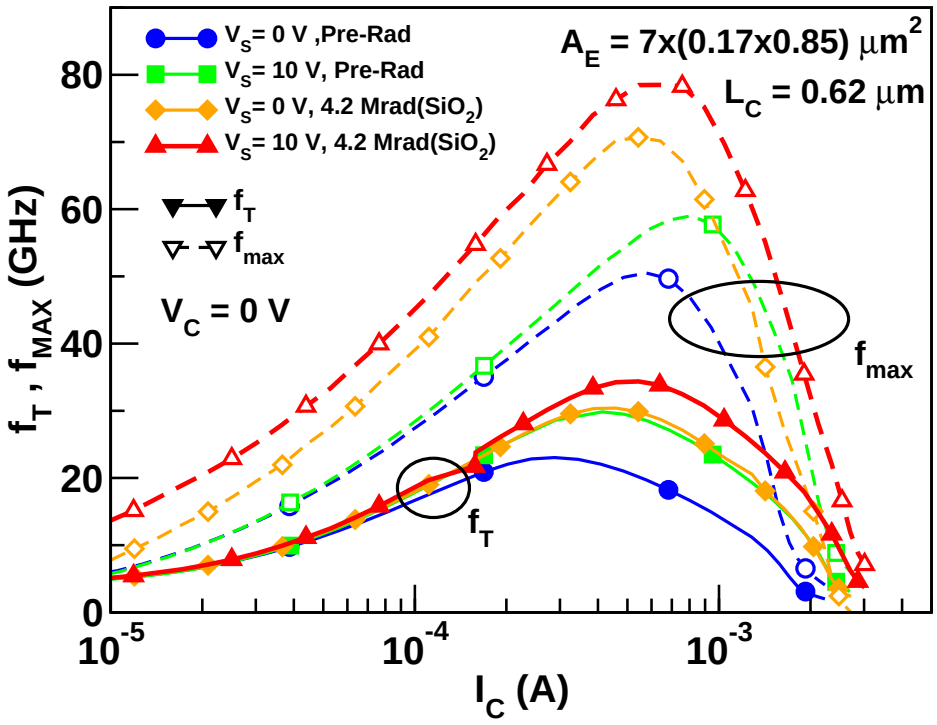


Figure 76: f_T and f_{max} for fully depleted SiGe HBT-on-SOI, before and after a 4.2 Mrad(SiO_2) dose, at different V_{CB} and V_S. The emitter area A_E is 7×(0.17×0.85) μm^2. L_C is 0.62 μm.

change, consistent with the observed small change of f_{max}. Conversely, proton irradiation of the SOI device leads to a dominance of the vertical component of the electric field in the depleted collector.

The impact of irradiation on the thermal resistance R_{TH} of both bulk and SOI HBTs is also examined using the technique described in [81]. Figure 78 shows that while bulk devices exhibit negligible change in thermal resistance, radiation in SOI devices has the same impact on R_{TH} as an increase in V_S. TCAD simulations have been used to compare the power density distributions in the SiGe HBT-on-SOI biased at V_{BE} = 0.7 V and V_{CB} = 2 V for substrate voltages of 0 V and 20 V. Figure 79 shows 1-D cuts of the power density P along the line z under the emitter for V_S = 0 V and 20 V while Figure 80 shows the 2-D cuts of P on the plane a from emitter to collector, as indicated in the inset of

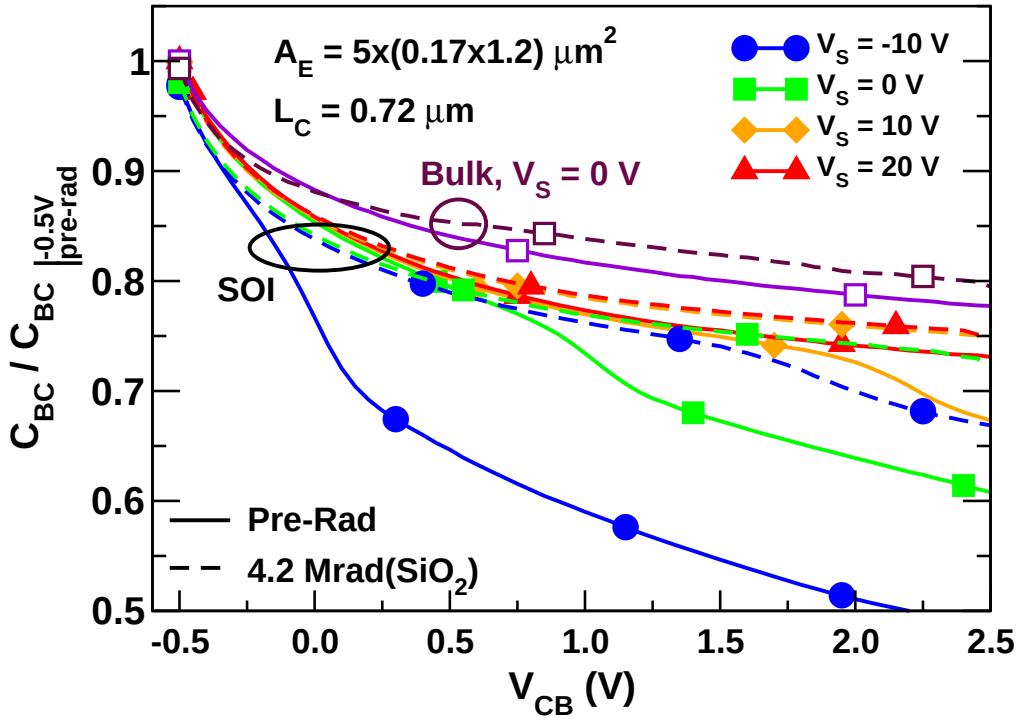


Figure 77: Normalized C_{BC} versus V_{CB} for both a bulk device ($V_S = 0$ V) and an HBT-on-SOI (V_S ranging from -10 V to 20 V, in 10 V steps), before and after a 4.2 Mrad(SiO_2) dose.

Figure 79. Since the thermal conductivity of SiO_2 is lower than for Si, the heat generated in the transistor flows mainly through the Si layer and through the top contacts, rather than through the SiO_2 BOX, as reported in [61]. Therefore, at $V_S = 20$ V the additional power dissipated at the SOI/BOX interface, as shown in Figure 79 and Figure 80 will flow through the whole SOI layer, resulting in a noticeable increase of the thermal resistance. Since large radiation doses result in both larger thermal resistance and impact ionization, the potential increase of self-heating can be a reliability concern for devices operating at large collector-base voltages in radiation environments.

To conclude, the impact of 63.3 MeV protons on SiGe HBTs on both SOI and bulk substrates fabricated with identical emitter-base structures is assessed by comparing the *dc* and *ac* performance and the thermal resistance. Although SOI devices exhibit larger degradation in the inverse mode than in the forward mode, the excess leakage can be reduced by increasing the substrate bias. Radiation also alters the current flow in the device, increasing R_{TH}. This constitutes a possible reliability concern for devices operating at large collector-base voltages.

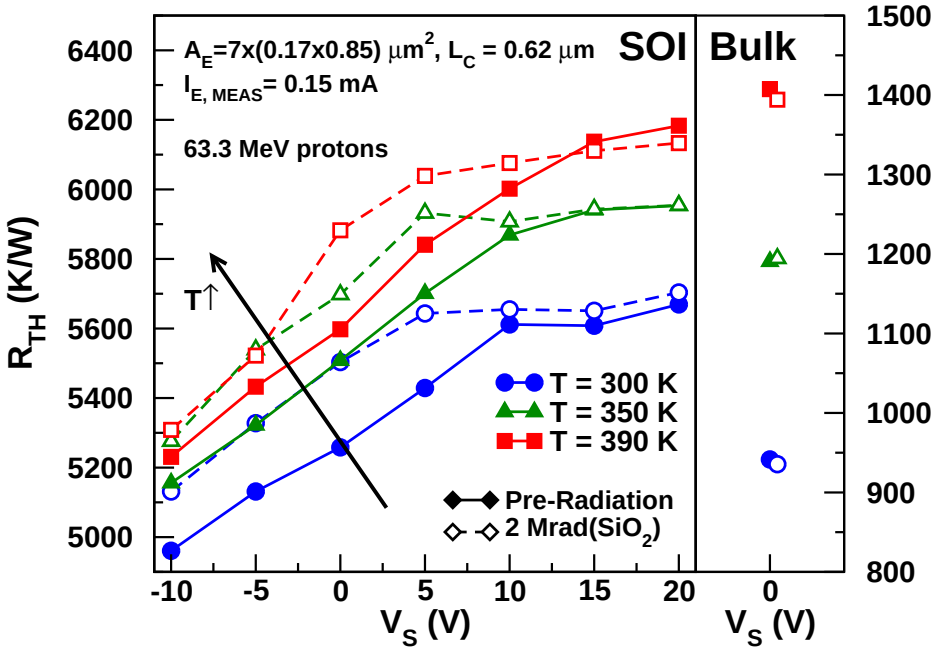


Figure 78: Thermal resistance R_{TH} of HBTs fabricated on bulk and SOI substrates as a function of V_S, before and after a 2 Mrad(SiO_2) dose, at temperatures of 300 K, 350 K and 390 K.

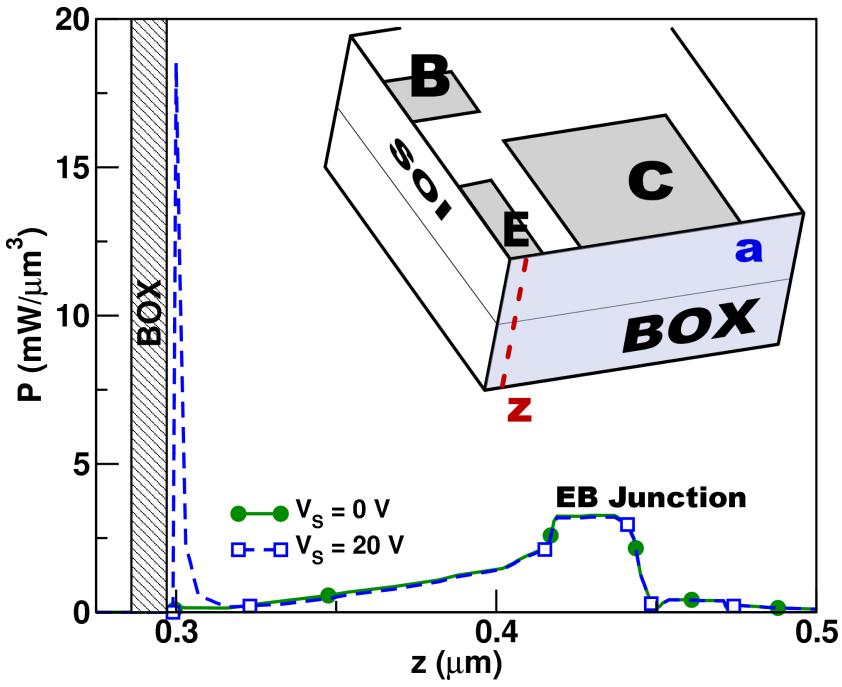


Figure 79: 1-D plots of power density in a SiGe HBT on SOI for $V_S = 0$ V and $V_S = 20$ V, along the line z indicated in the inset.

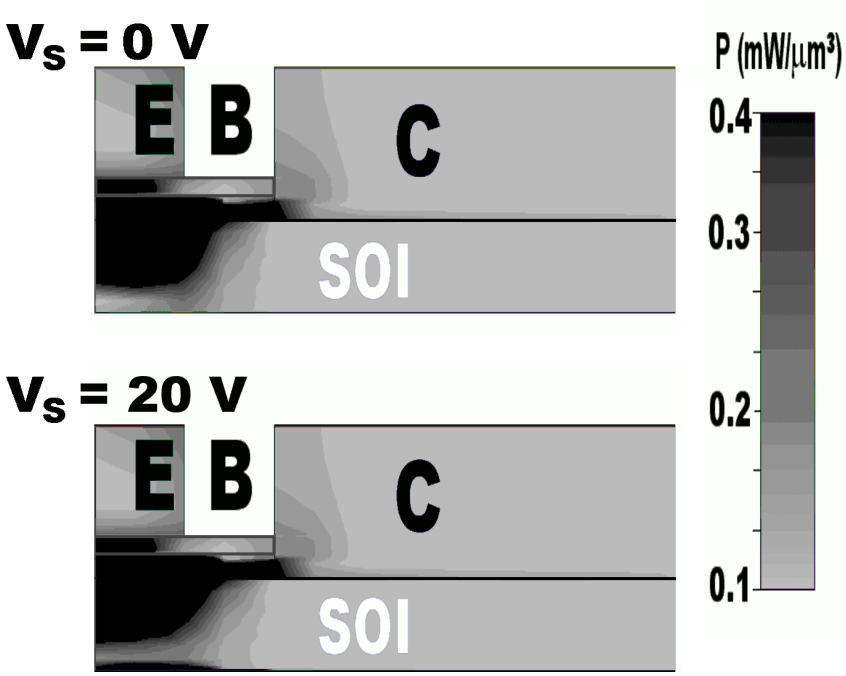


Figure 80: 2-D plots of power density in a SiGe HBT on SOI for $V_S = 0$ V and $V_S = 20$ V along the plane a indicated in Figure 79

5.4 Single Event Upset Response of HBTs on thick-film SOI with $C_B E^B C$ layout

Single event upset is considered the Achilles' heel of bulk SiGe HBTs: vertical devices are affected by SEU even when the strike occurs outside the deep trenches because of the bulk Si substrate.

While HBTs-on-SOI are obviously immune from this problem because they are completely surrounded by oxide, they may also exhibit position-dependent ion strike effects, especially in the case of advanced devices with optimized layouts. Although the smaller silicon volume of HBTs-on-SOI suggests that the amount of charge collected during an ion strike will be lower than in vertical HBTs, the difference in device geometry can potentially result in different collection phenomena. Especially in thin-film devices, the doping of the depleted collector and the substrate voltage exert significant influence on the electric fields in the region, possibly altering the SEU response.

Accurate studies of SEU transients in bulk devices require complex and lengthy 3-D TCAD simulations since the device mesh needs to be large enough to capture the complete

ion strike event without introducing unphysical approximations. Not only the vertical penetration of a heavy ion is in the order of tens of microns but also the boundaries of the mesh must be far enough from the strike site so that there is no artificial reflection of charge at the model boundaries. This leads to meshes with an extremely large number of elements and consequently to simulation times in the order of several days [25].

Importantly, the device geometry of SiGe HBTs-on-SOI is particularly advantageous for 3-D TCAD simulations because the devices are completely surrounded by SiO_2 and consequently the simulated Si volume is much smaller. Therefore, these devices present an opportunity to significantly reduce the overall number of mesh elements while at the same time to selectively increase the grid density in the EB junction and in the neutral base in order to improve the model accuracy.

This section describes calibrated 3-D ion strike simulations of the SiGe HBT-on-SOI device with $C_B E^B C$ layout [4] described in Section 1.4.3. Figure 81 shows the currents resulting from an ion strike in the center of the emitter of the device. The total collected charge is less than 0.025 pC, in contrast with about 1 pC for a comparable bulk device, resulting in an anticipated significant reduction in vulnerability to SEU [77].

Interestingly, the shape of the current pulses is remarkably different from an ion strike in the center of the emitter of a bulk device with a conventional CBEBC layout (with base contacts placed in-plane between emitter and collector). TCAD simulations indicate that initially I_B is negligible and that I_E and I_C have opposite signs. The negative I_B pulse is caused by excess holes leaving through the base and the positive I_E pulse is due to electrons leaving through the emitter, as shown by the arrows in Figure 82. The change of sign of the I_C pulse is caused by two distinct phenomena occurring at the times marked by A and B in Figure 81.

At time A, the ion strike creates a large number of electron-hole pairs, bringing the SOI layer out of equilibrium and causing a sudden increase in carrier recombination, as shown in Figure 82. The recombination peaks at the extremity of the high doping n-region, used to lower the collector resistance R_C, causing a large current flow from the collector contact which results in the negative I_C pulse.

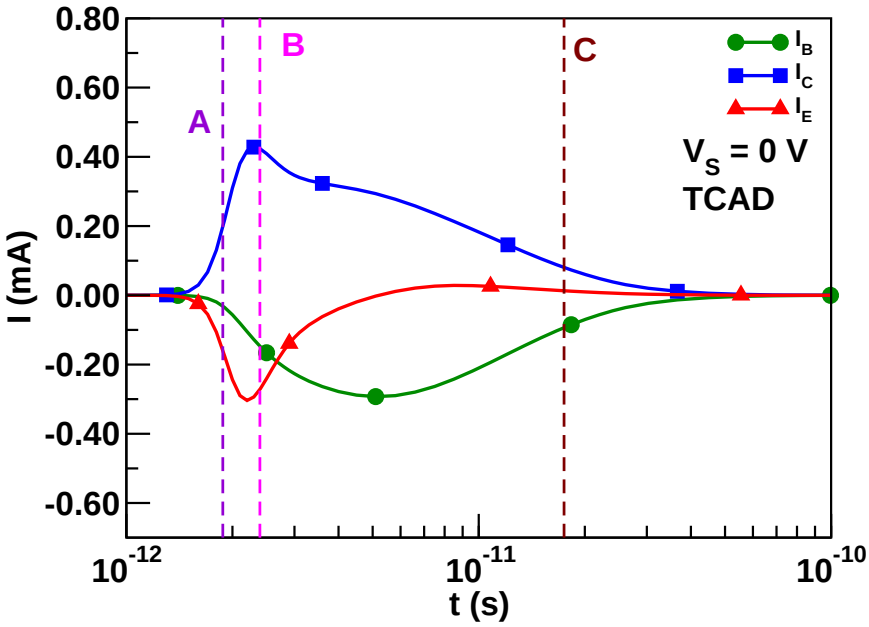


Figure 81: Collected charge at the terminals for an ion strike in the center of the emitter of a SiGe HBT-on-SOI.

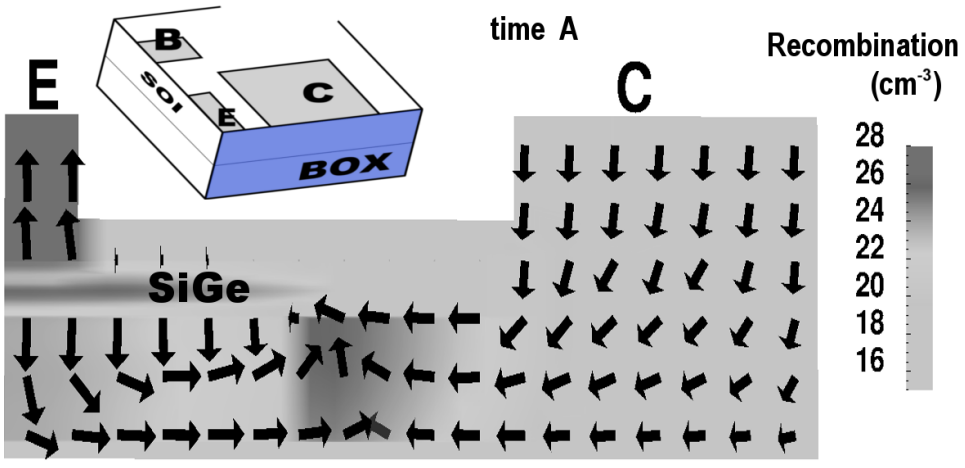


Figure 82: 2-D Plots of SRH recombination rate for the ion strike in the center of the emitter at time A, as indicated in Figure 81. The arrows visualize the electron flow. The inset shows the 2-D cut plane.

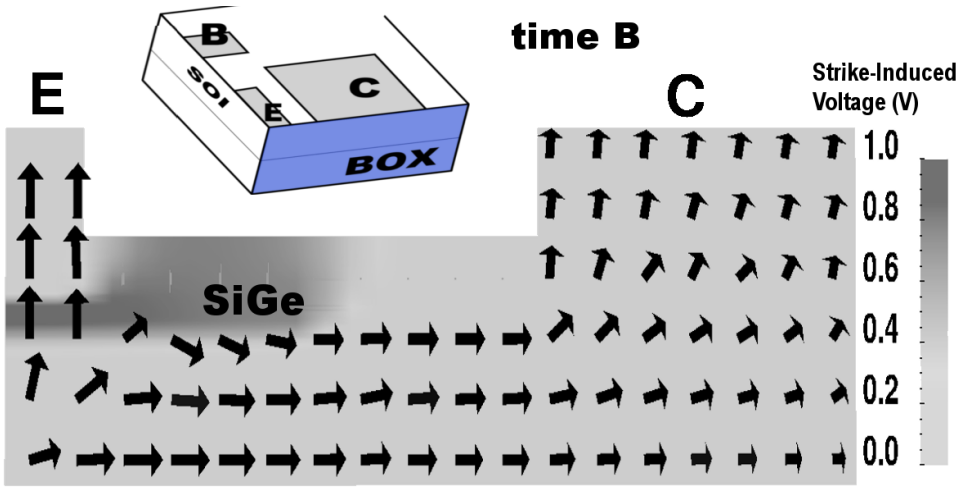


Figure 83: 2-D Plots of ion-strike induced electric potential for the strike in the center at time B, as indicated in Figure 81. The arrows visualize the electron flow. The inset shows the 2-D cut plane.

Then at time B, the ion strike significantly perturbs the electrostatic potential in the base of the device forward biasing the EB and CB junctions, as shown in Figure 83.

The positive I_C current component resulting from the forward-biased CB junction inverts the trend of the total collector current and results, as recombination subsides, in a positive I_C pulse at time C. Conversely the forward biasing of the EB junction decreases the total emitter current, as shown in Figure 81. At this time the transistor is operating in the saturation region, as shown by the large I_B current supporting both I_C and I_E.

Since the $C_B E^B C$ layout creates a significant asymmetry in the device geometry, it is reasonable to expect that the precise shape of the ion-induced currents will depend on the exact strike location within the device. This hypothesis is confirmed in Figure 84, which shows the currents generated by an ion strike between the emitter and base, as indicated in the inset. In this case, most of the electrons flow directly to the collector because it is the closest n-type contact. TCAD simulations suggest that an ion strike in this region is not able to significantly turn on the device, explaining why there is no change of sign in the strike-induced currents.

This analysis proves that studies of the effects of SEU on circuits featuring devices with $C_B E^B C$ layout require accurate 3-D TCAD simulations to correctly model the shape of

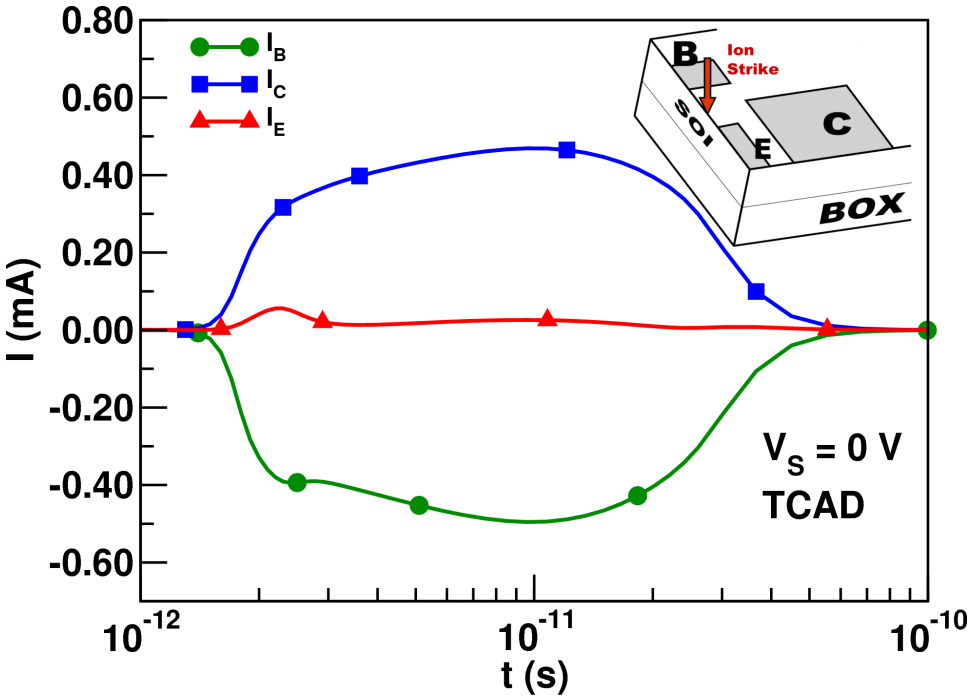


Figure 84: Collected charge at the terminals for an ion strike between the emitter and the base of a HBT-on-SOI, as shown by the inset.

current pulses resulting from heavy-ion strikes.

To conclude, 3-D TCAD simulations indicate that the novel $C_B E^B C$ layout used in these SiGe-on-SOI devices affects the shape of the current pulses induced by ion-strikes, potentially altering their SEU immunity.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

The contributions made by this work can be summarized as:

1. Implementation of a 3-D regional transit time analysis technique for the optimization of the *ac* performance of SiGe HBTs-on-SOI with advanced layouts.

2. First study of the cryogenic performance of SiGe HBTs-on-SOI at temperatures as low as 20 K. Discovery that the collector structure of these devices and the large thermal resistance significantly reduce the degradation caused by mixed mode stress.

3. First investigation of the *dc* and *ac* of SiGe HBTs-on-SOI at high temperatures. Analysis of 1/f noise in forward and inverse mode operation both at room and high temperature.

4. Comparison of the radiation response of SiGe HBTs fabricated on thick- and thin-film SOI substrates. Study of the impact of radiation on thermal resistance and collector base-capacitance of HBTs on thin-film SOI.

5. Simulation study of the impact of advanced layouts on the single event upset response of SiGe HBTs-on-SOI.

In the future, this work should be extended to study the use of SiGe HBTs in circuits operating in extreme environments and in particular to develop circuit techniques apt to mitigate the impact of the radiation-induced substrate effect on circuit performance and reliability.

APPENDIX A

PROGRAM LISTINGS

This appendix contains the code used for the 3-D regional transit time analysis described in Section 2.3.

The TCAD simulation is performed by the SDEVICE code A.1 The MATLAB code A.2 prepare_tecplot.m reads and converts the TCAD mesh and performs the transit time analysis. The auxiliary PERL script A.3 is called by the MATLAB file to quickly extract data from the TCAD mesh files.

```
# 3-D regional transit time analysis
# Sentaurus command file
# (c) Marco Bellini, marco.bellini.it@gmail.com
# 11/25/2008

Device HBT {



  Electrode {
    { Name="emitter" Voltage=0 }
    { Name="base" Voltage=0 }
    { Name="coll" Voltage=0 }
  }

  # input grid files
  File {
    Grid     = "npn_msh.grd"
    Doping   = "npn_msh.dat"

    Plot     = "tau_des.dat"
    Current  = "tau_des.plt"
    ACPlot   = "tau_des.acp"
```

```
    }

  Plot {
    Potential Electricfield
    eDensity hDensity
    eCurrent/Vector hCurrent/Vector
    TotalCurrent/Vector
    eMobility hMobility
    eQuasiFermi hQuasiFermi
    eGradQuasiFermi hGradQuasiFermi
    eEparallel hEparallel
    eMobility hMobility
    eVelocity hVelocity
    DonorConcentration Acceptorconcentration
    Doping SpaceCharge
    ConductionBand ValenceBand
    BandGap Affinity
    xMoleFraction
  }
}
File {
  Output  = "li_tau_hd"
  ACPlot  = "li_tau_acp"
  ACExtract  = "li_tau_axt"
}

Math {
  Extrapolate
  NotDamped=1000
  Iterations=20
  NewDiscretization
  Derivatives
  RelerrControl
  -CheckUndefinedModels
}
```

```
Physics {
  AreaFactor=2.0
  Temperature=295
  Hydrodynamic
  Mobility( PhuMob DopingDep HighFieldsat Enormal )
  EffectiveIntrinsicDensity (BandGapNarrowing( Slotboom) )
  Recombination ( SRH (DopingDependance)
  Auger
  )
}




System {
  HBT hbt (coll=c emitter=e  base=b)
  Vsource_pset vb (b 0)  {dc=0}
  Vsource_pset vc (c 0)  {dc=0}
  Vsource_pset ve (e 0)  {dc=0}
}

# initial voltage
# 0.70
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.7 }
    Goal { Parameter=vc.dc Voltage=0.7 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      }  }
  Plot( FilePrefix="t0700_" noOverwrite ) }
```

```
# initial voltage + 5 mV perturbation
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.705 }
    Goal { Parameter=vc.dc Voltage=0.705 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      }  }
  Plot( FilePrefix="t0705_" noOverwrite ) }

# 0.725
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.725 }
    Goal { Parameter=vc.dc Voltage=0.725 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      }  }
  Plot( FilePrefix="t0725_" noOverwrite ) }

Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.730 }
    Goal { Parameter=vc.dc Voltage=0.730 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      }  }
Plot( FilePrefix="t0730_" noOverwrite ) }

# 0.750
Solve {
```

```
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.75 }
    Goal { Parameter=vc.dc Voltage=0.75 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      }  }
Plot( FilePrefix="t0750_" noOverwrite ) }

Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.755 }
    Goal { Parameter=vc.dc Voltage=0.755 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      }  }
Plot( FilePrefix="t0755_" noOverwrite ) }

# 0.775
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.775 }
    Goal { Parameter=vc.dc Voltage=0.775 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0775_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.780 }
```

```
    Goal { Parameter=vc.dc Voltage=0.780 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0780_" noOverwrite )
}



# 0.80
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.8 }
    Goal { Parameter=vc.dc Voltage=0.8 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0800_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.805 }
    Goal { Parameter=vc.dc Voltage=0.805 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0805_" noOverwrite )
}
# 0.825
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.825 }
    Goal { Parameter=vc.dc Voltage=0.825 })
```

```
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0825_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.830 }
    Goal { Parameter=vc.dc Voltage=0.830 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0830_" noOverwrite )
}
# 0.850
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.85 }
    Goal { Parameter=vc.dc Voltage=0.85 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0850_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.855 }
    Goal { Parameter=vc.dc Voltage=0.855 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0855_" noOverwrite )
}
```

```
# 0.875
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.875 }
    Goal { Parameter=vc.dc Voltage=0.875 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0875_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.880 }
    Goal { Parameter=vc.dc Voltage=0.880 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0880_" noOverwrite )
}



# 0.90
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.9 }
    Goal { Parameter=vc.dc Voltage=0.9 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0900_" noOverwrite )
}
```

```
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.905 }
    Goal { Parameter=vc.dc Voltage=0.905 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0905_" noOverwrite )
}
# 0.925
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.925 }
    Goal { Parameter=vc.dc Voltage=0.925 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0925_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.930 }
    Goal { Parameter=vc.dc Voltage=0.930 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0930_" noOverwrite )
}
# 0.950
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
```

```
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.95 }
    Goal { Parameter=vc.dc Voltage=0.95 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0950_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.955 }
    Goal { Parameter=vc.dc Voltage=0.955 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0955_" noOverwrite )
}
# 0.975
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.975 }
    Goal { Parameter=vc.dc Voltage=0.975 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0975_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=0.980 }
    Goal { Parameter=vc.dc Voltage=0.980 })
```

```
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t0980_" noOverwrite )
}




# 1.00
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.0 }
    Goal { Parameter=vc.dc Voltage=1.0 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1000_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.005 }
    Goal { Parameter=vc.dc Voltage=1.005 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1005_" noOverwrite )
}
# 1.025
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.025 }
```

```
    Goal { Parameter=vc.dc Voltage=1.025 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1025_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.030 }
    Goal { Parameter=vc.dc Voltage=1.030 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1030_" noOverwrite )
}
# 1.050
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.05 }
    Goal { Parameter=vc.dc Voltage=1.05 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1050_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.055 }
    Goal { Parameter=vc.dc Voltage=1.055 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1055_" noOverwrite )
```

```
}
# 1.075
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.075 }
    Goal { Parameter=vc.dc Voltage=1.075 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1075_" noOverwrite )
}
Solve {
  Coupled ( Iterations=100 ) { Poisson Contact Circuit  }
  Quasistationary ( InitialStep=1e-2 Minstep=1e-6 MaxStep=0.05
    Increment=1.2
    Goal { Parameter=vb.dc Voltage=1.080 }
    Goal { Parameter=vc.dc Voltage=1.080 })
  { Coupled { Poisson Contact Circuit  Hole Electron eTemperature hTemperature
      } }
  Plot( FilePrefix="t1080_" noOverwrite )
}
```

Listing A.1: The **npn_tau_des.cmd** simulation file for the SDEVICE TCAD simulator.

```
%
% transit time extraction with tecplot
% (c) Marco Bellini, marco.bellini.it@gmail.com
% 11/25/2008
%
% requires:
% - Perl
% - Matlab or Octave (version >= 3.00, the one with the textread working with
    headerlines)
% - Synopsys Sentaurus
```

```
% SET UP

% index of X,Y,eDensity, hDensity variables
TDR_VARIABLES= '1,2,4,5';
% index of zones (we exclude the extracted zones: pn junction and
% depletion region )
% the zone index can be found on tecplot
TDR_ZONES= '1,2,3,4,5,6,7';

% carrier type
% 1 electrons
% 2 holes
CARRIERTYPE=1;

% plt file from simulation
% electrodes names must be: coll, base, emitter
PLT_NAME='hbt_tau_des.plt';

% grid file name
TDR_GRID='npn_msh.grd';
% dat file name will be tXXXX__hbt_des.dat
% where XXXX is the voltage bias

% optional script to set the SENTAURUS path at Georgia Tech
% leave blank if no script is required
SET_SENTAURUS_SCRIPT='source /tools/linsoft2/synopsys/sentaurus/cshrc.meta';
%SET_SENTAURUS_SCRIPT='';

% transit time plot Z scaling in Tecplot
% units are  s / (um)^2
TDR_MIN=-0.0001;
TDR_MAX= 0.005;
```

```
% batchmode
% 0 will open tecplot and display the fT for each bias step
%   the file EXTR_FT.txt will have VBE(V) IC(mA) and FT(GHz)
% 1 will just save the image PNG files but won't calculate fT
BATCHMODE=0;









% load gummel plt data

% prepare inspect
fid=fopen('plot_gummel_ins.cmd','wt');
fprintf(fid,'proj_load %s GU\n',PLT_NAME);
fprintf(fid,'cv_createDS "IB" "GU base OuterVoltage" "GU base TotalCurrent" y\
    n');
fprintf(fid,'cv_createDS "IC" "GU base OuterVoltage" "GU coll TotalCurrent" y\
    n');
fprintf(fid,'cv_write xgraph temp_IC.xgraph "IC"\n');
fprintf(fid,'cv_write xgraph temp_IB.xgraph "IB"\n');
fclose(fid);

% run inspect
str=sprintf('%s;inspect -batch -f plot_gummel_ins.cmd',SET_SENTAURUS_SCRIPT);
```

```
system(str);

% load data
[VBE,IB]=textread('temp_IB.xgraph','%f %f','headerlines',2);
[VBE,IC]=textread('temp_IC.xgraph','%f %f','headerlines',2);
base_OuterVoltage=abs(VBE);
coll_TotalCurrent=IC;
base_TotalCurrent=IB;
clear VBE IB IC fid;

save('./gummel_data.mat','base_OuterVoltage','coll_TotalCurrent','
    base_TotalCurrent');



% transit time

Q=1.6e-19;
SCALE_FACTOR=1e-4;



delete('EXTR_FT.txt');
% find data files
FN=dir('t*_des.dat');



% IC
%load('./gummel_data.mat');

for n=1:1:length(FN)
  bias(n)=str2num(FN(n).name(2:5));
end
bias=bias/1000;

for n=1:1:length(bias)
  pp=find(base_OuterVoltage==bias(n));
```

```
  IC(n)=coll_TotalCurrent(pp(end));
  VBE(n)=base_OuterVoltage(pp(end));

  clear pp;
end
IC=abs(IC);



% TDR conversion
for n=1:length(FN)
    tm=FN(n).name;
    tm(end-3:end)=[];
    OUTTDR=sprintf('%s.tdr',tm);
    OUTMCR=sprintf('EX_%s.mcr',tm);
  OUTSCR=sprintf('EX_%s.scr',tm);


  fid=fopen(OUTMCR,'wt');

  fprintf(fid,'#!MC 900\n');
  fprintf(fid,'$!INTERFACE AUTOREDRAWISACTIVE = NO\n');

  fprintf(fid,'$!VARSET |FNAME| = "%s"\n',FN(n).name);
  fprintf(fid,'$!READDATASET ''"./%s" "./|FNAME|" ''\n',TDR_GRID);
  fprintf(fid,'   DATASETREADER = ''SWB-Loader''\n');

  fprintf(fid,'$!WRITEDATASET "%s"\n',OUTTDR);
  fprintf(fid,'BINARY = FALSE\n');
  fprintf(fid,'INCLUDECUSTOMLABELS= FALSE\n');
  fprintf(fid,'VARPOSITIONLIST = [%s]\n', TDR_VARIABLES);
  fprintf(fid,'ZONELIST = [%s]\n', TDR_ZONES);

  fclose(fid);
```

```
  fid=fopen(OUTSCR,'wt');
  fprintf(fid,'%s\n',SET_SENTAURUS_SCRIPT);
  fprintf(fid,'tecplot_ise -batch -p %s\n',OUTMCR);
    fclose(fid);

    system(sprintf('source %s',OUTSCR));

end

system('rm EX_*');


% create difference data files

% find data files
FNT=dir('t*_des.tdr');

c=1;
for n=1:2:length(FN)

  % new file name
    tm=FNT(n).name;
    tm(end-3:end)=[];
    OUTDATA=sprintf('DELTA_%s.tdr',tm);
    OUTPNG=sprintf('DELTA_%s.png',tm);
    OUTMCR=sprintf('DELTA_%s.mcr',tm);

    str=sprintf('perl tec_tdr_extr.pl %s %s %s',FNT(n).name,FNT(n+1).name,
        OUTDATA );
  fprintf('%s\n',str);
    system(str);

    fprintf('BIAS POINT %d (%s - %s) \n',c, FNT(n+1).name,FNT(n).name);
```

```
   dIC(c)=(IC(n+1)-IC(n) )/2;% A/um correct for area factor = 2
   ic_t(c)=IC(n);
   vbe_t(c)=VBE(n);



   multiplier=Q*SCALE_FACTOR/dIC(c);

% creation of tecplot MCR files

fid=fopen(OUTMCR,'wt');

fprintf(fid,'#!MC 900\n');
fprintf(fid,'$!INTERFACE AUTOREDRAWISACTIVE = NO\n');
fprintf(fid,'$!READDATASET  "%s" \n',OUTDATA);
fprintf(fid,'  READDATAOPTION = NEW\n');
fprintf(fid,'  RESETSTYLE = YES\n');
fprintf(fid,'  INCLUDETEXT = NO\n');
fprintf(fid,'  INCLUDEGEOM = NO\n');
fprintf(fid,'  INCLUDECUSTOMLABELS = NO\n');
fprintf(fid,'  VARLOADMODE = BYNAME\n');
fprintf(fid,'  ASSIGNSTRANDIDS = YES\n');
fprintf(fid,'  INITIALPLOTTYPE = CARTESIAN2D\n');
fprintf(fid,'$!DROPDIALOG SLICES\n');
fprintf(fid,'$!ALTERDATA\n');

      if CARRIERTYPE==1
          fprintf(fid,'  EQUATION = "{INTEGR}={eDensity [cm^-3]}*%g" \n',
              multiplier);
      elseif CARRIERTYPE==2
          fprintf(fid,'  EQUATION = "{INTEGR}={hDensity [cm^-3]}*%g" \n',
              multiplier);
      end
fprintf(fid,'$!FIELDLAYERS\n');
fprintf(fid,'  SHOWMESH = NO\n');
```

```
fprintf(fid,'$!ADDONCOMMAND\n');
fprintf(fid,'  ADDONID = ''Sentaurus Workbench Add-on''\n');

      tstr='COMMAND = ''SET_CONTOUR VAR_NAME = "INTEGR"  NUM_LEVELS = 15
          SCALE = asinh';
  fprintf(fid,'%s RANGE_MIN = %g RANGE_MAX = %g  ''\n',tstr,TDR_MIN,TDR_MAX);
fprintf(fid,'$!FIELDMAP\n');
fprintf(fid,'  CONTOUR{\n');
    fprintf(fid,'COLOR = BLACK\n');
    fprintf(fid,'CONTOURTYPE = BOTHLINESANDFLOOD\n');
  fprintf(fid,'}\n');
fprintf(fid,'  EDGELAYER{\n');
fprintf(fid,'     COLOR = BLACK\n');
  fprintf(fid,'}\n');
fprintf(fid,'$!GLOBALCONTOUR\n');
  fprintf(fid,'LEGEND {\n');
    fprintf(fid,'SHOW = YES\n');
fprintf(fid,'  }\n');

fprintf(fid,'$!DRAWGRAPHICS TRUE\n');

      fprintf(fid,'$!EXPORTSETUP\n');
      fprintf(fid,'  EXPORTFNAME = ''%s''\n',OUTPNG);
      fprintf(fid,'  EXPORTFORMAT = PNG\n');
      fprintf(fid,'  IMAGEWIDTH = 800\n');
      fprintf(fid,'$!EXPORT        \n');

      fprintf(fid,'$!ADDONCOMMAND\n');
fprintf(fid,'  ADDONID = ''Sentaurus Workbench Add-on''\n');
  fprintf(fid,'COMMAND = ''INTEGRATE INTEGR  NAME = INT%d''\n',c);

      fprintf(fid,...
          '$!VARSET |FT| = ( (1/(2*3.141592653589793*|INTEGRAL|)) / 1e9)\n')
              ;
```

```
        fprintf(fid,...
          '$!SYSTEM "echo %g %g |FT%%12.6g| >> EXTR_FT.txt"\n',...
               vbe_t(c),ic_t(c)*1000 )
        fprintf(fid,'    WAIT = TRUE\n');

        fprintf(fid,'$!PAUSE "VBE= %gV, IC=%fmA, ft = |FT%%6.6g| GHz"\n',...
                 vbe_t(c),ic_t(c)*1000);

fclose(fid);


        % running tecplot
        if BATCHMODE
           str=sprintf('%s;tecplot_ise -batch -p %s &',SET_SENTAURUS_SCRIPT
               ,...
               OUTMCR);
        else
           str=sprintf('%s;tecplot_ise -p %s &',SET_SENTAURUS_SCRIPT,...
               OUTMCR);
        end
        system(str);

        % wait for user to close tecplot
        if ~BATCHMODE

           fprintf('Please press a key to terminate tecplot\n');
           pause;
           system('killall tecplot.shared');
           pause(3);

        end


c=c+1;
```

```
end
```

Listing A.2: The **prepare_tecplot.m** algorithm in MATLAB.

```
#!/usr/bin/perl
use POSIX;

# transit time extraction with tecplot
# Auxiliary perl program
# (c) Marco Bellini, marco.bellini.it@gmail.com
# 11/25/2008



if ( $#ARGV <0 )
{
  print "use with prepare_tecplot.m \n";
  print "perl tec_tdr_extr.pl doping1_xt.dat doping2_xt.dat outfile_xt.dat\n";
  exit 1;
}



$numberOfArgs = @ARGV;
      print "The number of arguments passed was $numberOfArgs \n";
      for($i=0;$i < $numberOfArgs ; $i++)
      {
       print "argv[$i] = $ARGV[$i]\n";
      }

$infile1 = $ARGV[0];
$infile2 = $ARGV[1];
$outfile = $ARGV[2];



# loading
print "\nSlurping file $infile1 ...";
# load all the file in memory
```

```
open(F,"$infile1") or die "\n\nCan't open $infile1 : $!\n\n";
@dtf1=<F>;
close(F);
print "Done\n";

print "\nSlurping file $infile2 ...";
# load all the file in memory
open(F,"$infile2") or die "\n\nCan't open $infile2 : $!\n\n";
@dtf2=<F>;
close(F);
print "Done\n";



$ ln=0;
$nregions=0;

# finds the position of the numerical variables
foreach $line (@dtf1)
{
  if ($line =~ m/^ Nodes/)
  {

      @ndtmp1 = split(/,/,$line);

      # NODES
      $ndtmp2=$ndtmp1[0];
      @ndtmp3 = split(/=/,$ndtmp2);
      $nodes[$nregions]=$ndtmp3[1];

      # FACES
      $ndtmp4=$ndtmp1[1];
      @ndtmp5 = split(/=/,$ndtmp4);
      $faces[$nregions]=$ndtmp5[1];
```

```
        $tr=$nregions+1;
        print "R$tr Nodes = $nodes[$nregions] Faces = $faces[$nregions] ";

    }

# DT + nodes is not accurate for the end
    if ($line =~ m/^ DT/)
    {
        $start_data[$nregions]= $ln+1;
    }

    if ($line =~ m/^USERREC/)
    {
        $end_data[$nregions]=   $ln - $faces[$nregions] -1 ;
        print " L = $start_data[$nregions] , $end_data[$nregions] \n";
        $nregions++;
    }
    # next line
    $ln++;
}


open (O, ">$outfile");

# Data extraction
for ($nr = 0; $nr < $nregions; $nr++)
{
    # copy file
    if ($nr == 0)
    {
    for ($i = 0 ; $i < $start_data[$nr];  $i++)
      { print O "$dtf2[$i]"; };
    }
    if ( ($nr > 0) && ($nr < $nregions) )
    {
```

```
  for ($i = $end_data[$nr-1]; $i < $start_data[$nr];  $i++)
  { print O "$dtf2[$i]" };
}
# X
for ($i = $start_data[$nr]; $i < $start_data[$nr] + 1*ceil($nodes[$nr]/4) ;
    $i++)
{
  print O "$dtf2[$i]";
}
# Flip Y
for ($i = $start_data[$nr] + 1*ceil($nodes[$nr]/4); $i < $start_data[$nr] +
    2*ceil($nodes[$nr]/4) ; $i++)
{
  $dat1=$dtf1[$i];
  @sdat1=split(/ /,$dtf1[$i]);
  for ($nn=1; $nn <= $#sdat1; $nn++)
  {
    $de=-@sdat1[$nn];
    printf O ' %.12E ', $de;
  }
  printf O "\n"
}
# e
for ($i = $start_data[$nr]+ 2*ceil($nodes[$nr]/4) ; $i < $start_data[$nr] +
    3*ceil($nodes[$nr]/4) ; $i++)
{
  $dat1=$dtf1[$i];
  @sdat1=split(/ /,$dtf1[$i]);
  $dat2=$dtf2[$i];
  @sdat2=split(/ /,$dtf2[$i]);
  for ($nn=1; $nn <= $#sdat2; $nn++)
  {
    $de=@sdat2[$nn]-@sdat1[$nn];
    printf O ' %.12E ', $de;
  }
```

```
    printf O "\n"
  }

  # h
  for ($i = $start_data[$nr]+ 3*ceil($nodes[$nr]/4) ; $i < $start_data[$nr] +
      4*ceil($nodes[$nr]/4) ; $i++)
  {
    $dat1=$dtf1[$i];
    @sdat1=split(/ /,$dtf1[$i]);
    $dat2=$dtf2[$i];
    @sdat2=split(/ /,$dtf2[$i]);

    for ($nn=1; $nn <= $#sdat2; $nn++)
    {
      $de=@sdat2[$nn]-@sdat1[$nn];
      printf O ' %.12E ', $de;
    }
    printf O "\n"
  }

}

for ($i = $end_data[$nregions-1] ; $i < $#dtf2 +2;    $i++)
  { print O "$dtf2[$i]"; };

close (O);

exit;
```

Listing A.3: The **tec_tdr_extr.pl** algorithm in PERL.

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