EFFECT OF DC TO DC CONVERTERS ON ORGANIC SOLAR CELL ARRAYS FOR POWERING DC LOADS

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EFFECT OF DC TO DC CONVERTERS ON ORGANIC SOLAR CELL ARRAYS FOR POWERING DC LOADS

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This thesis is dedicated

To Mom, Dad, B.C., and Mitch

For believing in me.

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SUMMARY

The objective of this research is to determine if it is possible to reduce the number of organic solar cells required to power a load using a DC to DC converter thereby reducing the cost of the organic solar array system. An organic solar power system designer may choose an organic implementation of a DC to DC converter to go along with the organic solar cell array. Common DC to DC converters include the buck converter, boost converter, buck/boost converter, and Cúk converter, all of which are not good candidates for organic implementation due to their use of inductors. Organic inductors are relatively lossier than organic capacitors. So, an inductor-less DC to DC converter, such as the Dickson charge pump, would be a better candidate for organic implementation.

Solar cells connected in an array configuration usually do not perform up to their full potential due to current and voltage mismatches between solar cells. These mismatches can be related to each solar cell's circuit model parameters such as the photon current density, diode ideality factor, diode reverse saturation current density, parallel resistance, and series resistance. This research varies these circuit model parameters as dependent variables, and observes the loads and power levels that make the Dickson charge pump a feasible option.

The results show that current mismatch does produce an opportunity to use a DC to DC converter to save the use of a few solar cells. However, the Dickson charge pump was found to be infeasible due to an input voltage requirement that could not be met using the tested organic solar cells.

CHAPTER I

INTRODUCTION

The objective of this work is to investigate what organic solar cell random circuit parameter tolerances, loads, and power are required to make a Dickson charge pump an economical solution for reducing the number of organic solar cells used in an organic solar cell array system. Background on common DC to DC converters is given first to compare the benefits and drawbacks of each. Next, the Dickson charge pump is analyzed extensively, and an original design methodology is presented. Then background on the basic solar cell circuit representation, current-voltage (I-V) curves, power-voltage (P-V) curves, and resistance-voltage (R-V) curves (hereafter called *cell curves*) is presented along with a method for finding the *array curves*. Lastly, simulation results are given that show how the standard deviation of the random circuit parameters affect array performance and how they affect the decision to use a DC to DC converter or Dickson charge pump.

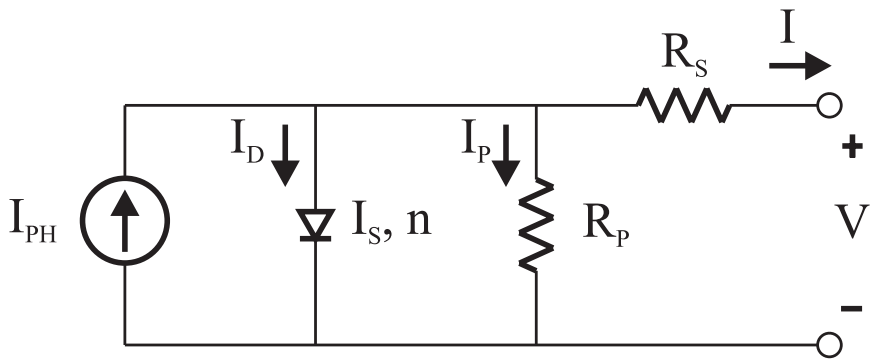


Figure 1: Basic solar cell circuit model.

1.1 Motivation: Reducing Solar PV Levelized Cost of Energy

Energy is essential for the human way of life. We, as a human society, have been looking for ways to produce more energy at lower cost for all of recorded history. Early methods of creating energy included burning wood, forced animal labor, and windmills. These forms of energy creation worked well for the time and capacity in which they were needed. However, populations grew and required cheaper and more powerful forms of energy creation. The burning of fossil fuels provided cheap and powerful energy and helped improve the infrastructures of developed countries. Automobiles, trains, and expanded manufacturing capabilities enabled developed countries to easily produce and distribute goods and services to its people.

The benefits of fossil fuel energy are its inexpensiveness, energy density, and portability while its drawbacks are pollution and limited supply. Renewable energy methods such as solar, wind, nuclear, hydro, fusion, and geothermal are being developed as inexpensive and powerful energy sources that do not share these drawbacks. All of these renewable energy methods would have a limitless supply and create less pollution than fossil fuels. One of the more attractive methods is solar energy because of wide availability of the sun, solar arrays available for the home, and absence of moving parts. These benefits for solar energy are a boon for the energy industry, but the preferred energy production method is still burning fossil fuels.

The reason energy companies use fossil fuels is its inexpensiveness despite its pollutive effects. On average, fossil fuel power is still less expensive than solar power. Table 1 shows the Levelized Cost of Energy (LCOE) of various forms of renewable and conventional energy. LCOE is a basic cost metric energy companies use to determine which form of energy is the most cost-effective to produce over the long term. It includes costs such as initial capital investment, expected future fuel costs, expected operation and maintenance, and expected taxes.

Table 1: Levelized Cost of Energy for Renewable and Conventional Energy [5]

Method	**Levelized Cost of Energy** ($/MWh)
Conventional Energy Methods	
Coal:	
Conventional Coal	$60.9
Advanced Coal	$63.9
Advanced Coal with CCS	$83.8
Natural Gas:	
Conventional Combined Cycle	$68.1
Advanced Combined Cycle	$64.8
Conventional Combustion Turbine	$113.4
Advanced Combustion Turbine	$100.6
Alternative Energy Methods	
Advanced Nuclear	$69.7
Geothermal	$72.9
Biomass	$79.8
Wind	$82.5
Solar Thermal	$154
Solar Photovoltaics	$287.9

There are two types of solar power listed in the table: solar thermal and solar photovoltaics (PV). Solar thermal refers to concentrating the sun's radiation to a point, which creates a large amount of heat. This heat is converted to electricity through a number of different methods including spinning a turbine with steam produced from boiling water [9]. Solar PV refers to converting photons from the sun's radiation to electricity. Solar cells made from semiconductors arranged into arrays capture the sun's radiation and use the photoelectric effect to convert photons into electricity [15].

Within solar PV, there are two main classes of solar cells: inorganic and organic. Inorganic solar cells are most commonly made (>80%) from crystalline silicon, but other semiconducting materials such as amorphous silicon have also been used [21]. The power-conversion efficiency of many common types of silicon solar cells have been reported between 9.8 and 24.7% [10]. Organic solar cells are distinguished from inorganic by their use of carbon-based semiconducting materials such as Buckminsterfullerine (C_{60}), [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM), and Zinc-Phthalocyanine (ZnPc) [11]. Organic solar cells have several advantages over inorganic solar cells. They are lighter in weight, more flexible, cheaper to manufacture, and more material-saving than inorganic solar cells [19] [22]. The disadvantage of organic solar cells is its poor power-conversion efficiency, which has been reported between 0.1 and 5.7% [8] [22]. The poor efficiency can be overcome by using more organic solar cells to meet a power specification, and the entire system may still be less expensive than an inorganic system. However, neither of these versions of solar PV has a cheaper LCOE than typical fossil fuel methods.

In order to get power companies to choose solar power more often, the LCOE of solar power must be driven down. Solar LCOE can be driven down in many different ways, but the most direct way is improving the amount of Watts generated per solar cell within a power generation system. The power generation system may

not necessarily be a grid-connected power plant designed to power neighborhoods. It may be a roof system placed on top of a house to power appliances and use net-metering, a medium-sized panel to power an electric motor, a small panel to power a streetlight, or a very small panel to illuminate Christmas light LEDs. Whichever the case, it would be beneficial to devise a way to reduce the number of solar cells needed to power a load.

One way to reduce the number of solar cells needed in a system is to improve the power efficiency of each solar cell individually. Another way is to analyze how solar cells behave when connected in an array together. It will be shown in this research that the manufacturing tolerances for solar cell parameters heavily affect the array performance. Some solar cells may be manufactured specifically to work best in a vertical array (more rows than columns), while others may work best in a horizontal array (more columns than rows). If a large load requires a large voltage, but the cells are made to work best in a horizontal array, then the best method of producing the voltage is to use a DC to DC converter.

The most common way of powering a DC load with inorganic solar cells is *bucking* or *boosting* the array output to the voltage and current needed for the load. A *buck* converter is a DC to DC converter that reduces DC voltage, while a *boost* converter increases DC voltage. Both of these circuits can be designed with efficiencies approaching 100% [16]. The reason buck or boost converters are used is because there are many different types of load applications, and it is more cost-effective for solar companies to design a few solar arrays and use many different converters to adjust the voltage and current accordingly.

Organic solar power system designers may decide to follow the same method as the inorganic designers, which is design a few flagship solar cell arrays and many different accommodating DC to DC converters. One difference is the organic designer may decide to build the buck or boost converter using organic components. In this case,

the organic designer should avoid using inductors, which are present in the buck and boost converters, because they are extremely lossy. There are other DC to DC converters that do not use inductors, and one of the most famous is the *Dickson charge pump*. The Dickson charge pump consists only of capacitors, diodes, and a clock, which makes it an excellent candidate for organic implementation.

In a general solar cell array power system, the DC to DC converter can be designed with an efficiency close to 100%, so it is not a limitation for powering the load. The solar cells in the solar array and the load are the factors that affect the power efficiency of the solar array.

This work investigates what solar cell manufacturing tolerances, loads, and power are required to make the charge pump option more economical than the array option. A little background on common DC to DC converters, Dickson charge pumps, and solar cell arrays is given first. Then, simulation results are given that show what conditions on the solar cell parameter tolerances produce situations that favor the charge pump option.

1.2 Survey of DC to DC converters

The simplest DC to DC converter is the voltage divider using resistors. However, there are not many voltage divider circuits in use because the non-load resistor dissipates power, lowering the overall power efficiency. Optimal DC to DC converters use switching techniques to move charge or current in such a way that creates a larger or smaller voltage or current on the output.

1.2.1 Buck Converter

The buck converter is used to lower the input voltage. The circuit diagram is shown in Figure 2. The waveform applied to the low-pass L-C filter, V_a is a square wave and has an average value of DV_{in}, where D is the duty cycle of the switch. The low-pass filter removes all the high frequency components in V_a, and the output becomes just

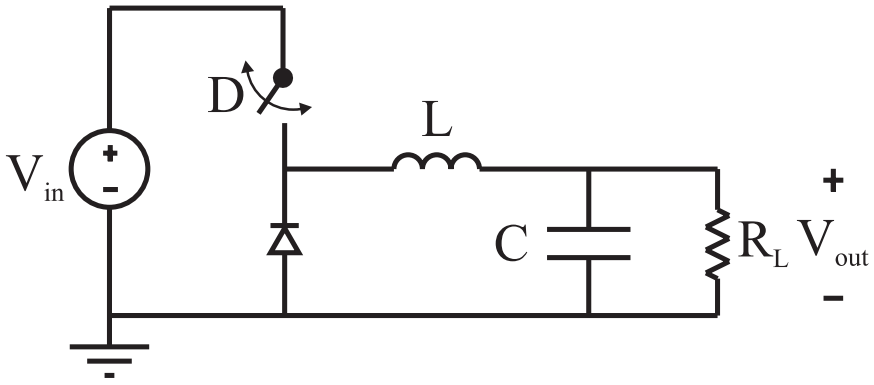


Figure 2: The buck converter uses a switch and low-pass filter to lower input voltage.

the DC component [16],

$$V_{out} = \bar{V_a} = DV_{in} \tag{1}$$

The gain equation is linear, so a feedback loop can be used to control or regulate the output.

1.2.2 Boost Converter

The boost converter is used to raise the input voltage. The circuit diagram is shown in Figure 3. The inductor is first charged when the switch is closed. When the switch opens, it discharges into the capacitor, which slowly discharges into the load. The gain equation is [16]:

$$V_{out} = \frac{1}{1-D} V_{in} \tag{2}$$

The gain equation is linear, so a feedback loop can also be used to control the output of the boost converter.

1.2.3 Buck-Boost Converter

The buck-boost converter is used to raise or lower the input voltage. The circuit diagram is shown in Figure 4. The buck-boost converter can be thought of as a buck and boost converter cascaded together. The peculiarity is that the output is inverted. The gain equation is the product of the buck and boost gain equations.

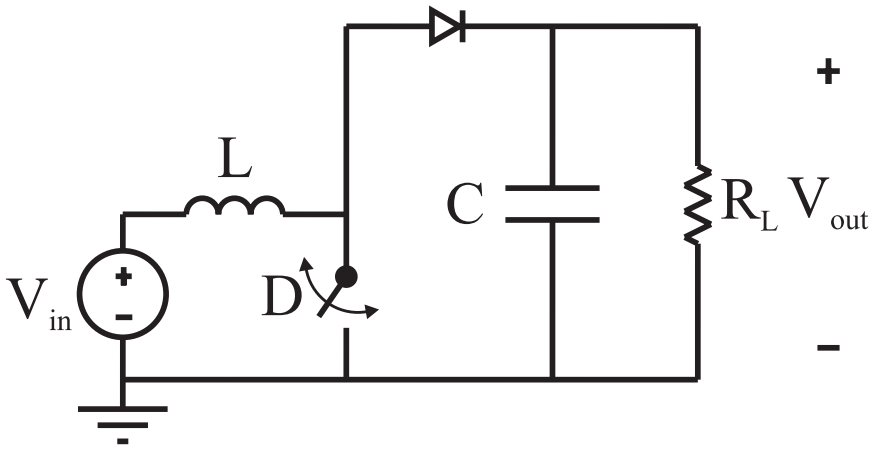


Figure 3: The boost converter uses a switched inductor and a ripple capacitor to raise input voltage.

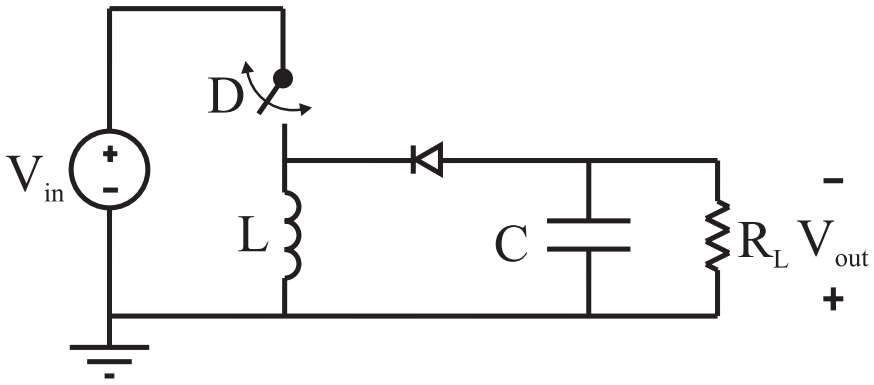


Figure 4: The buck-boost converter uses a switched inductor and a blocking diode to control how much power goes to the load.

From equations (1) and (2) [16],

$$V_{out} = \frac{D}{1-D} V_{in} \tag{3}$$

The gain equation is linear, so a feedback loop can be used to control the output.

1.2.4 Cúk Converter

The Cúk converter is used to raise or lower the input voltage just like the buck-boost converter. The circuit diagram is shown in Figure 5. This circuit was named after its inventor, Slobodan Cúk. The gain equation is the same as the buck-boost converter

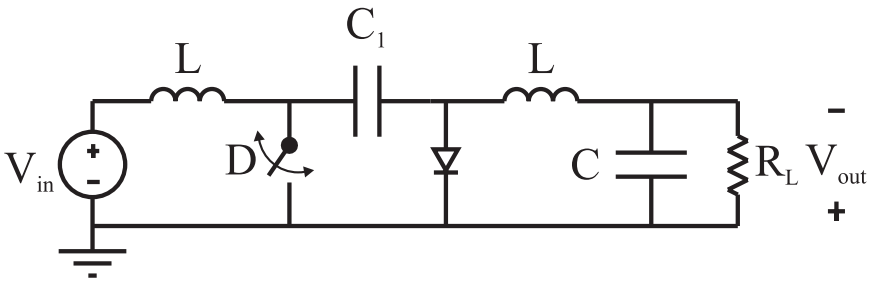


Figure 5: The Cúk converter uses a capacitor as its main energy storage device as opposed to an inductor like in the Buck, Boost, and Buck-Boost converters.

[16] [6]:

$$V_{out} = \frac{D}{1-D} V_{in} \tag{4}$$

The gain equation is linear, so a feedback loop can be used to control the output.

1.2.5 Cockcroft-Walton Voltage Multiplier

J. D. Cockcroft and E. T. S. Walton unveiled the predecessor to the Dickson charge pump in 1932. Their purpose was to accelerate protons to high speeds and conduct other experiments [4]. To do that, they needed an extremely large DC voltage (800 kV exactly) to create an extremely powerful electric field, which could accelerate protons from rest. The circuit they devised is shown in Figure 6. The basic idea behind the circuit was charging the lower-level capacitors on the right-hand column and then moving the switches up so that the higher left-hand capacitors could be charged. Then, the switches would be moved again to charge even higher-level right-hand column capacitors. This process continues until the circuit reaches steady-state, at which time the output voltage becomes [4]

$$V_{out} = NV_{in} \tag{5}$$

where N is the number of capacitors in the left-hand column. The maximum voltage across any individual capacitor is V_{in}. Even though the output voltage may be 800 kV, the individual capacitors do not need to be designed to withstand that much

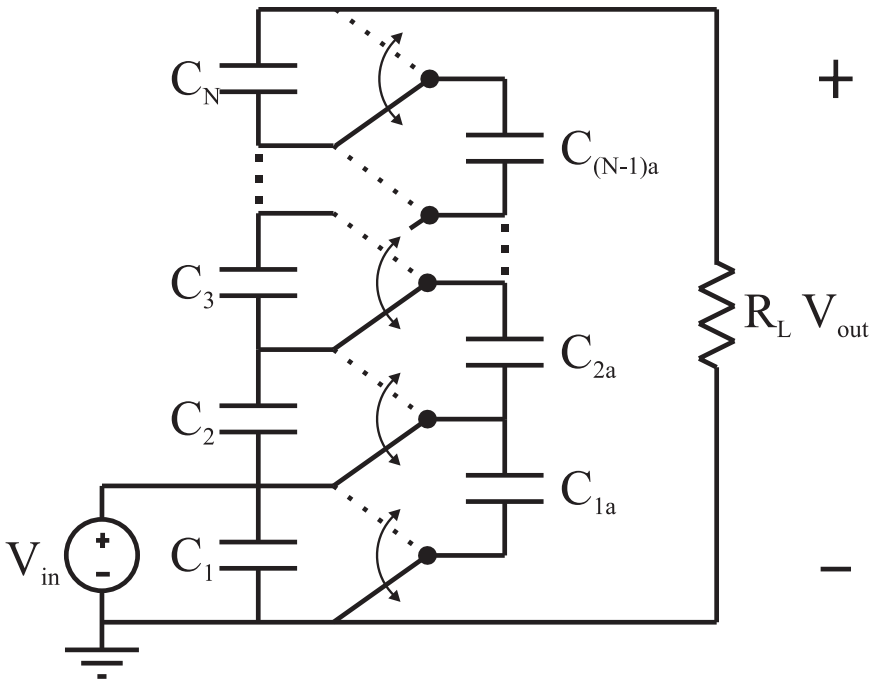


Figure 6: The Cockcroft-Walton voltage multiplier uses switched capacitors to step up the voltage.

voltage. This characteristic makes the Cockcroft-Walton voltage multiplier better suited for very high-voltage generation.

This DC to DC converter is different from the previous converters discussed because it does not use inductors. Thus, it is a reasonable candidate for organic component implementation. It would also be a good circuit to use for simulations in this research, but the Dickson charge pump uses almost half as many components to accomplish the same goal.

All of these DC to DC converters are used widely in other applications. Each has their own purpose. The buck, boost, buck-boost, and Cúk converters can have realistic power efficiencies above 0.9 [16]. These converters use inductors, which does not lend itself well to organic design. The Cockcroft-Walton voltage multiplier can have a power efficiency very close to 1.0 if operating at very high voltage and using large capacitors ($>$ mF). However, it suffers when stray capacitance becomes comparable to capacitors shown in the figure.

The Dickson charge pump overcomes many of the shortcomings of these converters. First, it does not use inductors. Second, it suffers only half as much from stray capacitance as does the Cockcroft-Walton voltage multiplier [7]. One downside is its nonlinear gain, which means a more complex feedback system needs to be designed in order to control the output.

CHAPTER II

DICKSON CHARGE PUMP OPERATION AND DESIGN

A common circuit used for boosting DC input voltage to larger DC output voltage is the Dickson charge pump [7] [1]. This type of charge pump circuit is a nonlinear, boosting DC-to-DC converter. The input is a DC voltage source, and the output is a DC voltage with ripple. It is nonlinear because a change in input voltage does not produce a proportional change in output voltage. It is a boosting converter because the circuit is generally used to create an output voltage that is larger than the input voltage.

The most common use of Dickson charge pumps is on-chip generation of large voltages for loads like flash memory and LCD displays in a systems-on-a-chip (SOC) [3]. A Dickson charge pump made with poly-silicon thin-film-transistors (TFTs) was designed to supply power for an LCD by Yoo and Lee [26]. Other uses include micro-electro-mechanical systems (MEMS) and high voltage varicap devices in tunable filters [2]. It can be used for larger power loads as well, but usage in power grid and high power transmission applications (> 1 MW) is uncommon.

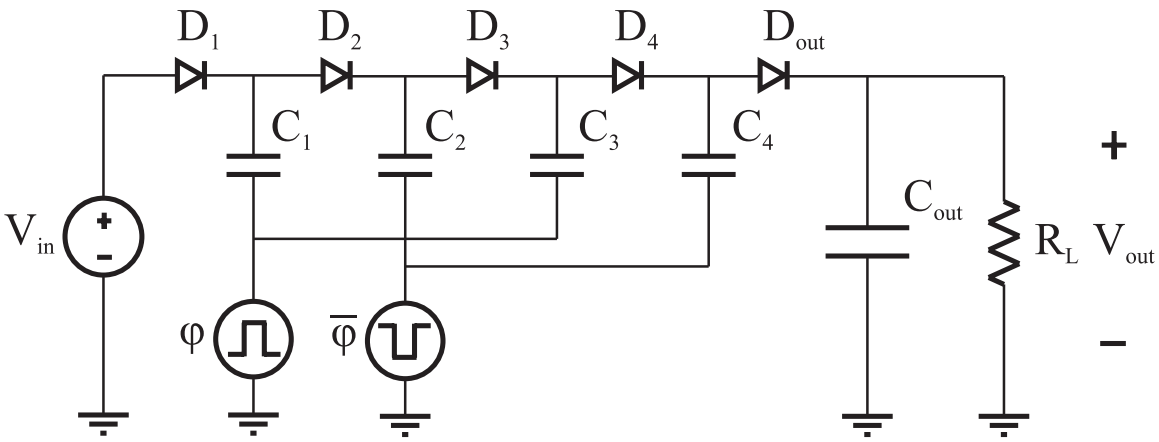


Figure 7: 4-stage Dickson charge pump circuit.

A circuit diagram of the Dickson charge pump is shown in Figure 7. A *stage* is defined as a capacitor connected between the preceding diode's cathode pin and one of the two clock sources. The Dickson charge pump in Figure 7 has $N =$ four stages. The diodes and capacitors in each stage are called *stage capacitors* and *stage diodes*, respectively. Each stage diode and stage capacitor has a subscript describing the stage to which they belong. Each stage capacitor has the same capacitance (i.e. $C_i = C_{i-1}$). The capacitor labeled C_{out} is called the *output capacitor*, and the diode labeled D_{out} is called the *output diode*. The output stage is not connected to a clock source and is connected in parallel with the load resistor, R_L. The clock sources, φ and $\bar{\varphi}$, are two complementary, non-overlapping, 50% duty cycle clocks with a maximum voltage of V_{in}. The clocks are 180 degrees out of phase, so when φ is high, $\bar{\varphi}$ is low and vice versa. The period of the clocks, T, is related to the clock frequency, f, by

$$f = \frac{1}{T} \tag{6}$$

2.1 Basic Circuit Operation

The Dickson charge pump operates in two modes: *transient* mode and *steady-state* mode, both of which are shown in Figure 8 [16]. Transient mode occurs when the charge pump is first turned on. Before being turned on, the stage capacitors and the output capacitor hold no charge. They must be charged up to reach steady-state mode. During transient mode, the DC source and clock sources provide much more current than during steady-state mode. This extra current is used to charge up the capacitors. Steady-state mode occurs when the capacitors operate under *charge balance*, which means the capacitors accumulate zero net charge during one complete clock cycle.

Pertinent equations such as input/output, power efficiency, input resistance, and ripple voltage equations are given for the steady-state mode in the following subsections. Detailed derivations are given in Appendix A.

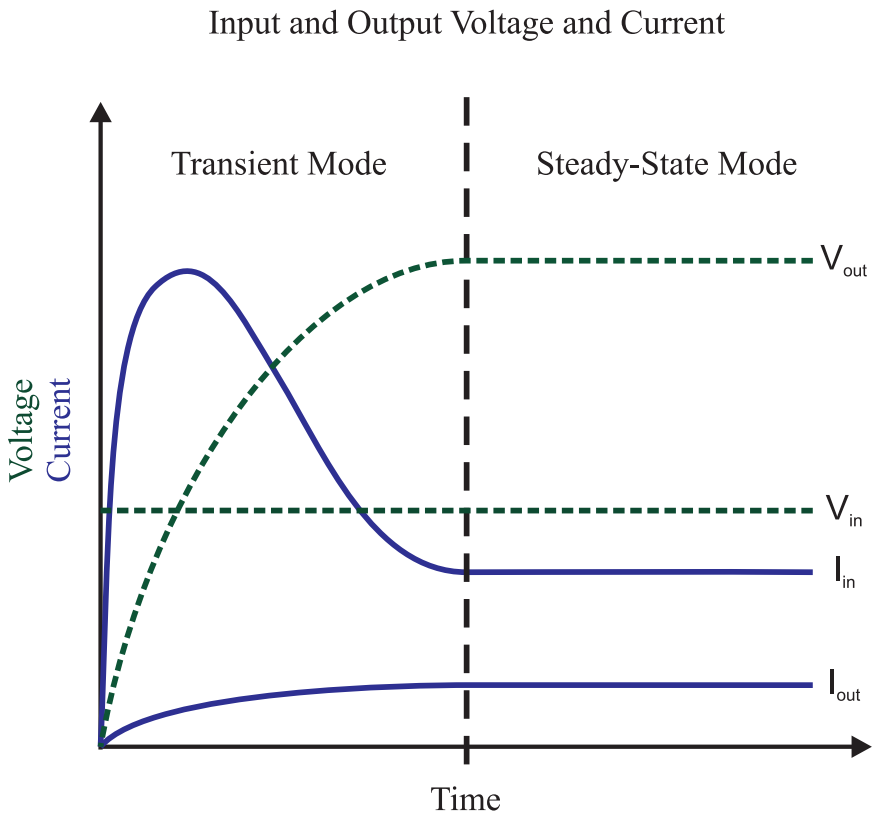


Figure 8: Difference between transient and steady-state modes.

2.1.1 Input/Output Equation

The most common form of the input/output equation was first presented by John F. Dickson [7]. For a general N-stage Dickson charge pump with clock voltage $V_\phi = V_{\bar{\phi}} = V_{in}$, this common output equation is

$$V_{out} = (N+1)(V_{in} - V_t) - \frac{NI_{out}}{fC} \tag{7}$$

This form is derived in detail in appendix section A.1, but is then rearranged to a simpler form:

$$V_{out} = \frac{(N+1)(V_{in} - V_t)}{1 + \frac{N}{fCR_L}} \tag{8}$$

This equation describes how the output behaves when design parameters are changed. Output voltage increases as more stages are added, but also loses V_t Volts as each stage is added. The fractional term in the denominator, N/fCR_L, is usually adds a small amount to the denominator, which means changes in the number of stages, frequency, capacitance, and load resistance do not affect the output voltage too heavily.

2.1.2 Power Efficiency

Power efficiency is defined as the ratio of power that makes it to the output without getting dissipated vs. the power supplied. It can be calculated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} \tag{9}$$

Efficiency η is easily found by substituting expressions for V_{out}, I_{out}, V_{in}, and I_{in}. Appendix section A.2 derives these expressions in detail and makes substitutions into equation (9). Two useful equations for power efficiency were derived. In terms of input and output voltage, power efficiency is

$$\eta = \frac{V_{out}}{V_{in}(N+1)} \tag{10}$$

If only input voltage is known, the efficiency has the following dependencies:

$$\eta = \frac{(1 - \frac{V_t}{V_{in}})}{1 + \frac{N}{fCR_L}} \tag{11}$$

These results have been verified through a different derivation technique by Tanzawa and Tanaka [23]. Equation (11) shows how the circuit parameters affect power efficiency. Increasing frequency, stage capacitance, and load resistance all increase efficiency as well as decreasing the number of stages. Efficiency becomes almost frequency independent for $f > N/(CR_L)$. Efficiency depends on input voltage. For large inputs, the V_t/V_{in} term is negligible, and efficiency becomes large. For small inputs, the V_t/V_{in} term dominates, and efficiency becomes small. This circuit is only useful for circuits with $V_{in} > V_t$.

The diodes are the only circuit components that dissipate power besides the load resistor, and their threshold voltage is fairly constant for any diode current. Reducing the current passing through the diodes for any given load resistance will increase power efficiency. Large loads require less current than small loads for the same output voltage. Large stage capacitors absorb less charge than small capacitors for constant frequency. Reducing the number of stages reduces the number of diodes. All of these things reduce the current through the diodes and increase power efficiency.

2.1.3 Output Ripple Voltage

The input/output equation gives a value for the maximum voltage the output can be. Output ripple voltage determines how far the output voltage drops from the final value given in equation (8). The load may require that voltage does not drop below 95% of its specification. If it does, the load device may turn off, break, or do something else that is undesired. So, it is important to determine what the output ripple voltage will be based on circuit parameters.

From appendix section A.2, The expression for output voltage ripple is

$$\frac{\Delta V_{out}}{V_{out}} = \frac{1}{R_L f C_{out}} \tag{12}$$

Ripple gets larger as load resistance gets smaller. Also, a faster frequency and a larger output capacitance will suppress ripple. Let the specification for percent ripple

voltage be called α:

$$\alpha = \frac{\Delta V_{out}}{V_{out}} \tag{13}$$

And let the ratio between output capacitance and stage capacitance be called β:

$$\beta = \frac{C_{out}}{C} \tag{14}$$

Then, according to the detailed derivation in appendix section A.2 , β and α are related by

$$\beta = \frac{1}{R_L f C \alpha} \tag{15}$$

This relationship implies capacitor ratio, β, and the ripple voltage specification, α, are inversely proportional to each other, which should make sense. Small ripple implies small α, which implies large β and large output capacitance. A large load resistance draws less charge from the output capacitor than a small load resistance, so a small output capacitor would suffice. Increasing frequency decreases β also, so along with the power efficiency equation (11), the designer can arbitrarily choose a large frequency to minimize capacitor size and maximize efficiency.

2.1.4 Input Resistance

Input resistance describes the equivalent resistance seen looking into the circuit. It is the same resistance the input solar cell array would see if connected to the input of the charge pump. The input resistance determines how large or small the input array needs to be in order to supply a certain input voltage and current.

Input resistance, R_{in}, is the resistance a Direct Current (DC) power source would see if connected to the input of the Dickson charge pump. It is defined as

$$R_{in} = \frac{V_{in}}{I_{in}} \tag{16}$$

The expression for I_{in} is derived in appendix A section A.2 as

$$I_{in} = (N+1) I_{out} \tag{17}$$

Substituting this expression into equation (16) and then replacing I_{out} with V_{out}/R_L, equation (16) becomes

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{(N+1)\, I_{out}} = \frac{V_{in} R_L}{(N+1)\, V_{out}} \tag{18}$$

V_{in}/V_{out} is the reciprocal of the the voltage gain, which is related simply to the power efficiency by equation (10):

$$\frac{V_{in}}{V_{out}} = \frac{1}{\eta\,(N+1)} \tag{19}$$

Substituting equation (19) into equation (18) yields

$$R_{in} = \frac{V_{in} R_L}{(N+1)\, V_{out}} = \frac{R_L}{\eta\,(N+1)^2} \tag{20}$$

This says input resistance decreases as the number of stages increases. This makes sense because more stages means more current is drawn at the same voltage. Also, load resistance determines the output current, which determines the input current as well.

2.2 Dickson Charge Pump Design

This section will discuss the basic design of a Dickson charge pump, special design cases, and the clock circuit used to drive the pump.

2.2.1 Basic Design

The common specifications for a DC-DC converter are:

- Output power
- Load resistance
- Input resistance
- Minimum power efficiency
- Percent ripple voltage

From these specifications, the designer must determine these circuit parameters:

- Stage diodes (threshold voltage)
- Number of stages
- Input power
- Input voltage
- Frequency
- Stage capacitance
- Output capacitance

The first parameter the designer must determine is the type of diode to use in circuit. There is no equation or method that finds the perfect diode threshold voltage, V_t, to use for the circuit. However, it will be shown later that low V_t minimizes the size of the capacitors. So, the designer should choose diodes that are cheap and have low V_t. Also, advanced techniques such as using body diode connections in silicon-on-insulator (SOI) MOSFETs can be used. In some cases, this technique increases power efficiency [12] [13], and it may be transferable to organic transistors as well.

The number of stages, N, is the next parameter to calculate. There are several ways to estimate N, including designer's preference; however, the simplest way is to rearrange the input resistance equation from (20):

$$R_{in} = \frac{R_L}{\eta\left(N+1\right)^2} \tag{21}$$

Solving for N, this becomes

$$N = \sqrt{\frac{R_L}{\eta R_{in}}} - 1 \tag{22}$$

N may not be an integer depending on the specifications for R_L, R_{in}, and η. N should be floored to the largest integer less than N (e.g. $\lfloor 5.724 \rfloor = 5$). Flooring N, rather

than simply rounding N, is beneficial because it reduces the number of components and helps increase the designed power efficiency (explained later).

Using $\lfloor N \rfloor$ instead of N, the next step is to recalculate efficiency η from $\lfloor N \rfloor$. Solving equation (21) for η results in

$$\eta_{recalc} = \frac{R_L}{R_{in}\left(\lfloor N \rfloor + 1\right)^2} \tag{23}$$

From this equation, it can be shown that $\eta_{recalc} \geq \eta$ since $\lfloor N \rfloor \leq N$.

The input power, P_{in}, and the input voltage, V_{in}, can be found using (23) and the specifications for output power, P_{out}, and input resistance, R_{in}. P_{in} is

$$P_{in} = \frac{P_{out}}{\eta_{recalc}} \tag{24}$$

And by definition,

$$V_{in} = \sqrt{P_{in}R_{in}} = \sqrt{\frac{P_{out}}{\eta_{recalc}}R_{in}} \tag{25}$$

The next few design parameters to calculate are stage capacitance, C, output capacitance, C_{out}, and frequency, f. In almost every equation derived so far, frequency and stage capacitance have always appeared together as the product (fC). The exceptions are in equations (6), (93), and (96), but those are not design equations. Solving for fC from the design equations derived in this chapter produces two equations:

$$fC = \frac{1}{\alpha\beta R_L} \tag{26}$$

$$fC = \frac{\lfloor N \rfloor}{R_L}\left[\frac{\eta_{recalc}}{1 - \eta_{recalc} - \frac{V_t}{V_{in}}}\right] \tag{27}$$

This is an under-determined system of equations, which produces infinite solutions for f and C. The set of solutions for f and C form the graph shown in Figure 9. Equation (27) will be used to determine the product (fC). Equation (27) contains variables that were specified or found earlier in the design process, whereas equation (26) contains β, which has not yet been found.

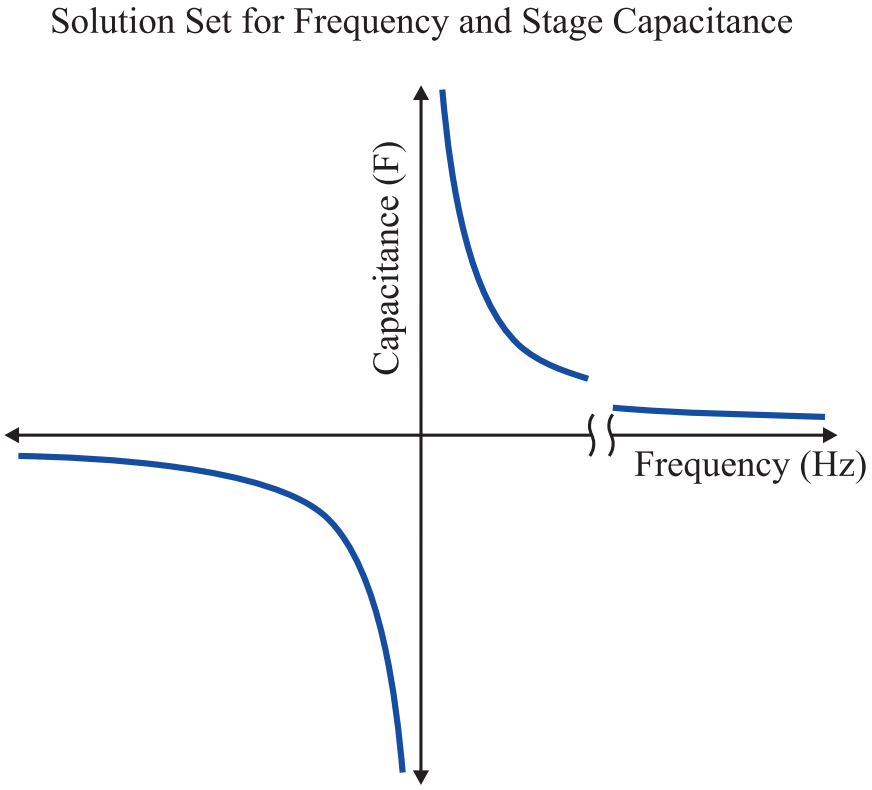


Figure 9: Solution set for f and C. Most Dickson charge pump designs have large f (∼MHz) and small C (∼nF), because those are the typical sizes available.

The set of infinite solutions, (f,C), allows the designer the freedom to choose f and C based on constraints such as component cost and size. Switch rise time and fall time are factors that affect which frequency should be chosen [14]. Output capacitance can be found using equation (26) and the equation for β in equation (119). First β is found using

$$\beta = \frac{1}{\alpha f C R_L} \tag{28}$$

Then, C_{out} is found using

$$C_{out} = \beta C \tag{29}$$

This finishes the basic design of the Dickson charge pump. The charge pump can be designed for almost any combination of input resistance, power efficiency, load resistance, and load power.

2.2.2 Special Cases

Sometimes, the constraint for η is too high for the given input resistance, and it is simply impossible to build. In these situations, a sacrifice of power efficiency should be made.

A large specification for η will sometimes call for $N < 1$. This situation occurs when R_{in} is specified to be too large ($R_{in} \geq R_L/\eta$ according to equation (22)). In this case, the designer should simply set $\lfloor N \rfloor = 1$ in the design equations above. Every specification can still be met except for the power efficiency: $\eta_{recalc} < \eta$ since $\lfloor N \rfloor > N$.

If the specifications call for a very small input voltage or a very high power efficiency, then the frequency-capacitance product will be negative ($fC < 0$). This produces the inequality

$$\eta_{recalc} + \frac{V_t}{V_{in}} > 1 \tag{30}$$

according to (27). The recalculated efficiency, η_{recalc}, was recalculated from the specifications, and input voltage, V_{in}, was found from the specifications. The only freedom

the designer has at this point is selection of a smaller V_t. If recalculated efficiency, $\eta_{recalc} \geq 1$, then even letting $V_t \to 0$ will not make fC positive. In this case, the designer should take the ceiling of N, which is rounding upward to the smallest integer greater than N (e.g. $\lceil 5.724 \rceil = 6$). Using $\lceil N \rceil$ will allow every specification to be met except for power efficiency just as before: $\eta_{recalc} < \eta$ since $\lceil N \rceil > N$.

2.3 Clock Design

The two clock phases, ϕ and $\bar{\phi}$, can be designed in a number of ways. This section discusses square-wave and sinusoidal clock designs.

2.3.1 Square-Wave Clock Design

A 555 timer chip is a circuit that can be configured to act as a 50% duty cycle switch that flips between V_{in} and ground. The output pin of the 555 timer would be one phase of the clock (ϕ). The other phase would be made using a complementary inverter with ϕ as the input and $\bar{\phi}$ as the output. This is a standard complementary inverter, or "NOT" gate, where a "high" input produces a "low" output and vice-versa. Figure 10 shows this clock circuit.

Another option for the clock signal generator is a ring oscillator, which consists of a NAND gate followed by an even number of NOT gates [25]. The output of the last NOT gate is connected to the input of the NAND gate. This is shown in Figure 11. Each MOSFET stage has a gate delay, τ_{delay}, and the square wave produced has a 50% duty cycle with period $T = 2(K+1)\tau_{delay}$. The last and next-to-last stages can be used as ϕ and $\bar{\phi}$.

The stage capacitors must be designed to withstand the large and fast current swings and large current amplitudes shown in Figure 33. The expression for that current curve can be found by

$$I_D(t) = C_1 \frac{dV_{C_1}(t)}{dt} = \frac{V_L}{R_D} e^{\frac{-t}{R_D(t)C}} \tag{31}$$

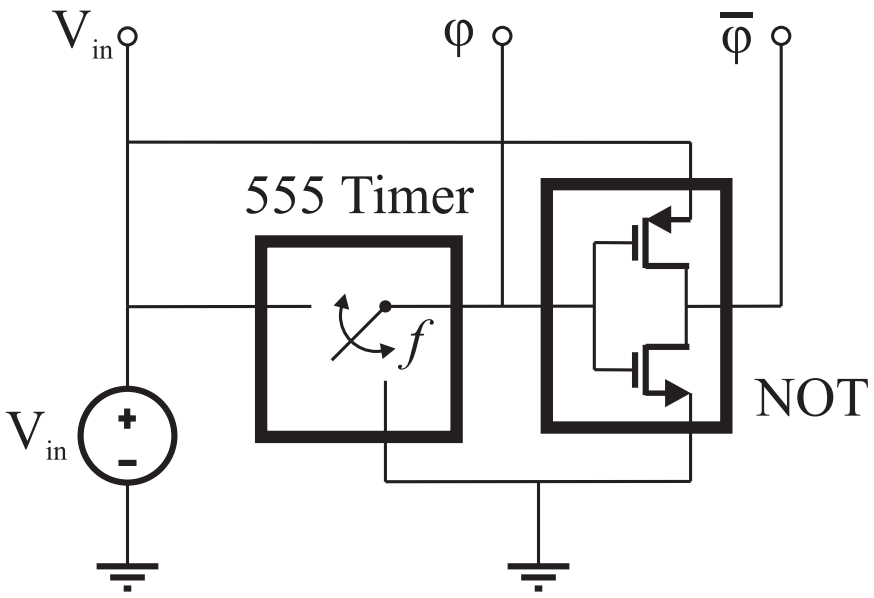


Figure 10: ϕ and $\bar{\phi}$ can be produced using a 555 timer and complementary inverter, or "'NOT"' logic gate.

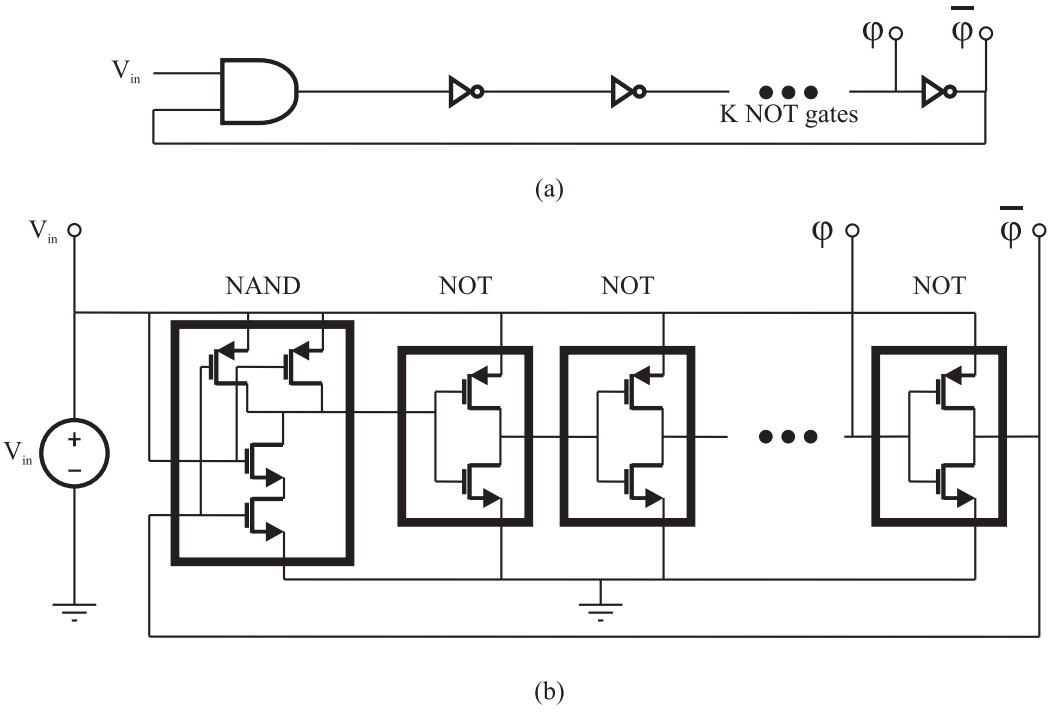


Figure 11: A ring oscillator circuit produces a square wave with period $T = 2(K + 1)\tau_{delay}$. (a) Digital logic symbol representation. (b) Transistor-level circuit.

The maximum diode current is V_L/R_D. At the beginning of each clock cycle, R_D is very small, so the current spike may be large.

An external clock may be used if the Dickson charge pump is used in a larger system. The only clock circuitry needed within the Dickson charge pump is a complementary inverter, buffers, and two NOR gates to prevent clock overlap [12].

2.3.2 Sinusoidal Clock Design

If a sinusoidal clock is desired instead of a square-wave clock, the designer could choose a crystal oscillator or any type of harmonic oscillator (Armstrong, Hartley, Colpitts, etc.). The circuit connections need to be modified as in Figure 12a. Instead of a separate $\bar{\phi}$-phase clock source connected to the even-numbered stages, these stages are simply connected to ground. This method works because charge is transferred from the even-numbered stages to the odd-numbered stages when the sinusoidal clock signal goes negative. So, the charge transfer action of the charge pump is still preserved even with a sinusoidal clock.

There are two benefits from using a sinusoidal clock over a square-wave clock. First, the sinusoidal clock imposes a gradual voltage change across the capacitors, which induces softer current transfer between the capacitors. The current no longer looks like unit-step decaying exponential functions with large current spikes as in Figure 33. Instead, the current looks like the curve in Figure 12b. In that graph, the maximum current can be found by comparing $I_C(t)$ to a triangular approximation as in the graph. The areas under $I_C(t)$ and the triangle curve must both be equal to charge transferred, Q_L:

$$Q_L = \frac{1}{2} t_L I_{max} = \int_{t_L} I_C(t) dt = C V_L \tag{32}$$

Then, I_{max} is found as

$$I_{max} = \frac{2 C V_L}{t_L} \tag{33}$$

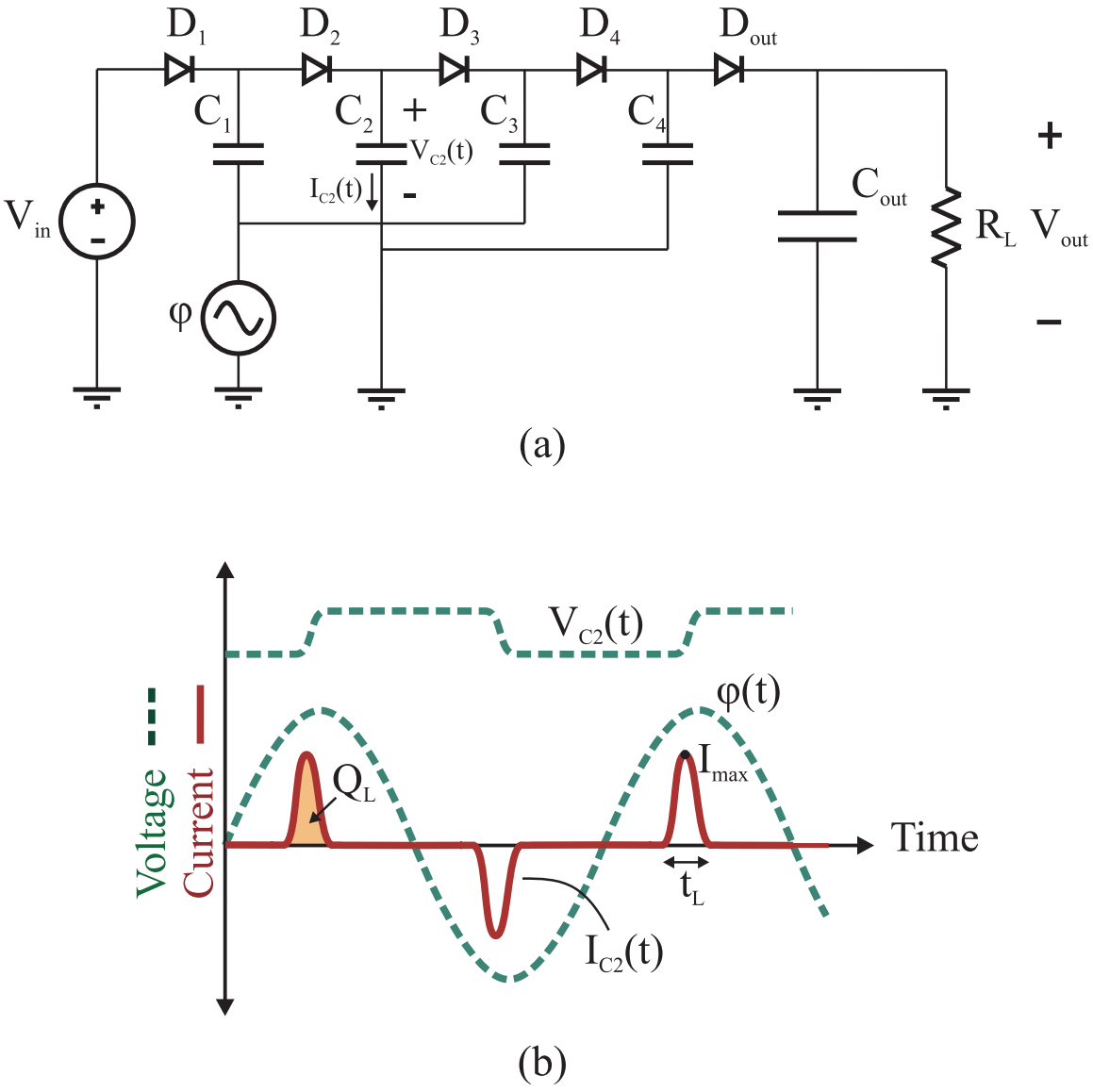


Figure 12: (a) Dickson charge pump with sinusoidal clock phases. (b) Clock and stage capacitor voltage and current curves.

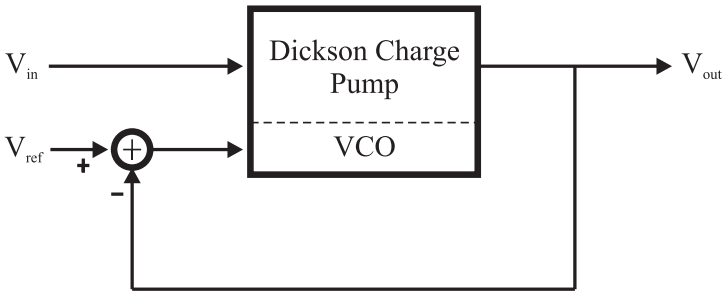


Figure 13: A VCO can provide output voltage regulation.

Making the substitution for V_L using (104), this becomes

$$I_{max} = \frac{2I_{out}}{ft_L} \tag{34}$$

where

$$t_L \propto \frac{V_{in}}{fV_{out}} \tag{35}$$

If the designer wishes to have control over the output voltage, a voltage-controlled oscillator (VCO) could be used. A VCO can be used in a control loop as shown in Figure 13 to regulate the output voltage in case the input voltage is not outputting a constant average DC voltage. The plant is the Dickson charge pump, which has a nonlinear gain with respect to frequency. Addition of a nonlinear control circuit would then provide voltage regulation. The VCO may be used in either the square-wave clock case or sinusoidal clock case.

Control over the output is useful when the input source experiences a sudden loss or gain in power. For solar cell arrays, this means partial shading or unusually high or low sun radiation, which causes a change in input voltage. The control system may need to be powered by a separate, more reliable power source to provide reliable reference voltages.

CHAPTER III

SOLAR CELL ARRAYS

Photovoltaics or *solar cell arrays* are collections of solar cells connected in series and/or parallel to provide DC electric power. The most common method of solar cell array connection is the rectangular form, where n columns of m series-connected solar cells are connected in parallel, which make the dimensions m rows by n columns. This chapter discusses the basic circuit model for both organic and inorganic solar cells, the effects of combining solar cells, and the effects of solar cell parameter mismatch.

3.1 The Solar Cell

Solar cells are characterized electrically by their current vs. voltage curve, or *I-V curve*. A typical I-V curve is shown in Figure 14. I_{SC} is the short-circuit current, which is the largest current the solar cell can produce. V_{OC} is the open-circuit voltage, which is the largest voltage the solar cell can produce in the first quadrant ($V > 0, I > 0$). P_k, I_k, and V_k are the power, current, and voltage the solar cell produces when operating at the *knee*, which is the operating point of maximum power production. The solar cell needs to be connected to the optimal resistance, R_k, in order to operate at the knee.

3.1.1 Basic Circuit Model for a Solar Cell

The typical solar cell can be represented by the circuit model shown in Figure 15. The current source, I_{PH}, represents the current produced from electron-hole pair recombination due to solar radiation. The diode represents the solar cell's P-N junction characteristics. Current will pass through the solar cell just like it would pass through

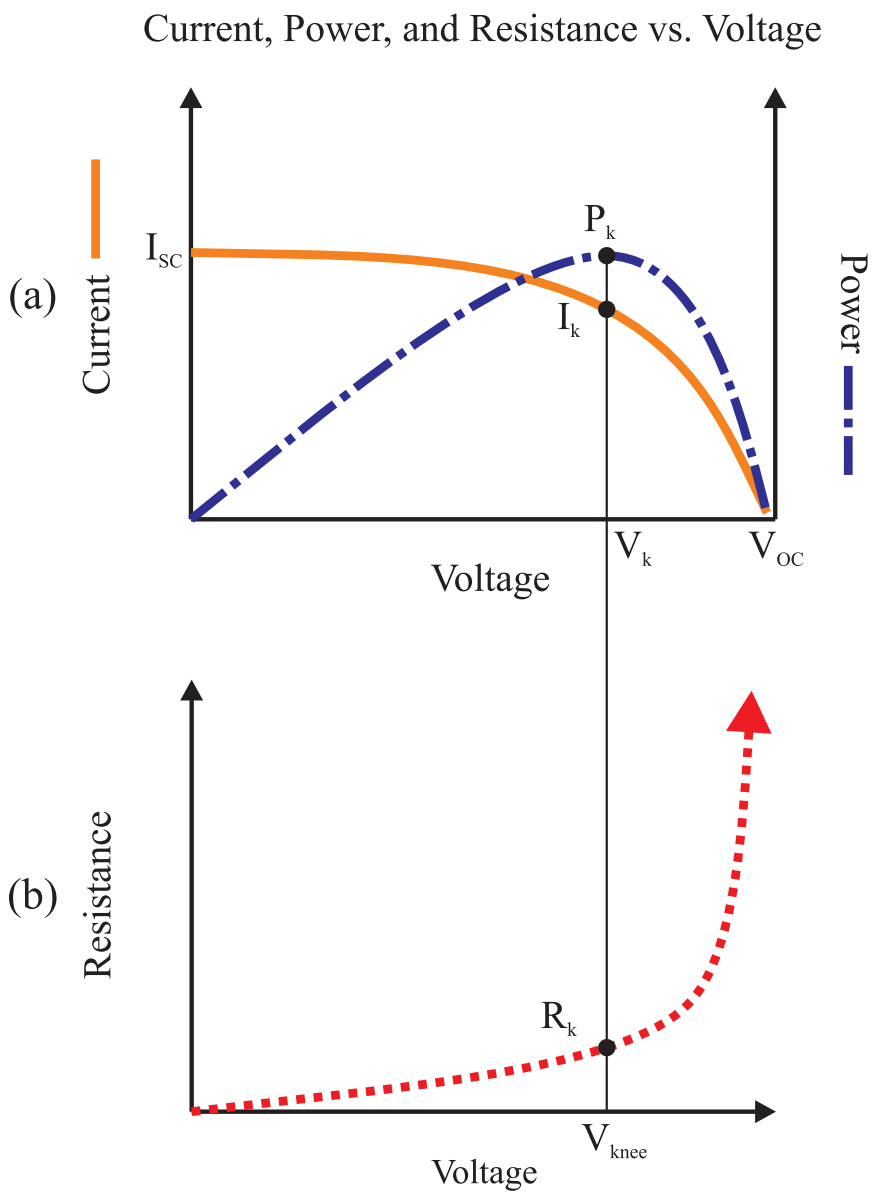


Figure 14: (a)Typical solar cell current and power vs. voltage curves. (b) Typical solar cell resistance vs. voltage curve.

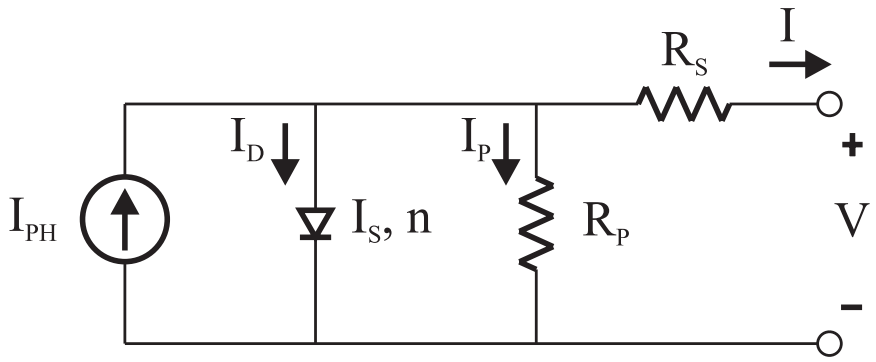


Figure 15: Solar cell circuit model used to find the I-V characteristic equation.

a diode when voltage is applied or produced across the terminals. The diode is characterized by its *ideality factor*, n, and its *reverse saturation current*, I_S. R_P is the parallel resistance of the semiconductor materials. R_S is the series resistance of the metals used in the solar cell leads and contacts. Typically, $R_P >> R_S$.

Figure 15 can be analyzed to find the I-V characteristic equation. A node equation will show

$$I = I_{PH} - I_D - I_P \tag{36}$$

I_{PH} is independent of V and I, so it will be left untouched in equation (36). However, I_D and I_P are dependent on I and V. The voltage across the diode is

$$V_D = V + IR_S \tag{37}$$

This is substituted into the diode current equation to find I_D:

$$I_D = I_S \left(e^{\frac{q(V+IR_S)}{nkT}} - 1 \right) \tag{38}$$

The voltage across the parallel resistor, R_P is also V_D, so the current can be found using Ohm's law:

$$I_P = \frac{V + IR_S}{R_P} \tag{39}$$

These expressions for I_D and I_P are plugged into equation (36) to get

$$I = I_{PH} - I_S \left(e^{\frac{q(V+IR_S)}{nkT}} - 1 \right) - \frac{V + IR_S}{R_P} \tag{40}$$

This is the generally accepted version of the current-voltage relationship for the solar cell model. The I-V equation is not in standard form as a function of voltage alone ($I(V)$), but is still practical to use and needs no further simplification. The basic shape of the I-V curve formed by this equation is the same as Figure 14, and can be thought of as simply a constant minus the diode curve. Making the solar cell more sensitive to light will increase I_{PH} and raise the curve to higher currents overall. Making the P-N junction diode less sensitive to voltage will decrease I_S and stretch the curve to higher voltages overall. The last term in the equation, $\frac{V+IR_S}{R_P}$, is small compared to the rest of the equation because the parallel resistance is large compared to voltage and series resistance. However, it is included to get an accurate measure of I_{SC} and V_{OC}.

3.1.2 Finding Short-Circuit Current and Open-Circuit Voltage

The simple method of finding short-circuit current and open-circuit voltage is to assume that the series resistance is very small and the parallel resistance is very large. With these assumptions, the current-voltage relationship for the circuit model becomes

$$I \approx I_{PH} - I_S \left(e^{\frac{qV}{nkT}} - 1 \right) \tag{41}$$

Shorting the terminals forces $V = 0$, which makes the diode current term drop out, and the current-voltage equation becomes

$$I_{SC} \approx I_{PH} \tag{42}$$

The total current produced by sunlight radiation is approximately the short-circuit current.

The open-circuit voltage is found by opening the cell terminals, which forces $I = 0$. Then, the current-voltage relationship becomes

$$0 \approx I_{PH} - I_S \left(e^{\frac{qV_{OC}}{nkT}} - 1 \right) \tag{43}$$

Solving this equation for V_{OC} results in

$$V_{OC} \approx \frac{nkT}{q} ln \left(\frac{I_{PH}}{I_S} + 1 \right) \tag{44}$$

This equation is the voltage produces across the diode when its current is I_{PH}. This has been verified by Nakayashiki [17]. For a detailed method of finding the short-circuit current and open-circuit voltage, refer to appendix section.

The *fill factor* (FF) is defined as the ratio of the knee power ($V_k I_k$) to the theoretical maximum attainable power ($V_{OC} I_{SC}$), and is related to the solar cell's power conversion efficiency (η_{cell}) by [28]:

$$FF = \frac{V_k I_k}{V_{OC} I_{SC}} = \frac{\eta_{cell} A E_L}{I_{SC} V_{OC}} \tag{45}$$

where A is the cell area (m^2) and I_L is the irradiance of the light incident on the solar cell (W/m^2).

3.2 The Solar Cell Array

The solar cell is a power generation device, but it does not produce much power by itself. Most conventional organic or inorganic solar cells produce power in the range of 10 nW to 10 mW, depending on semiconductor technology, illumination, and cell area exposed to light. Most devices that are commonly connected to solar cells, such as microcontrollers, battery banks, or DC to DC converters, have a wide variety of input resistances and require much more power than $10mW$. A single solar cell by itself will not be able to power a larger-power device, so designers use a solar cell array, such as the rectangular array shown in Figure 16. This section derives the I-V, P-V, and R-V relationships (called *the array curves* from now on) for a standard, rectangular solar cell array.

3.2.1 The Ideal Column Array

The array curves are found by first summing the cell curves to find the column curves, and then summing the column curves to find the array curves. For an *ideal solar cell*

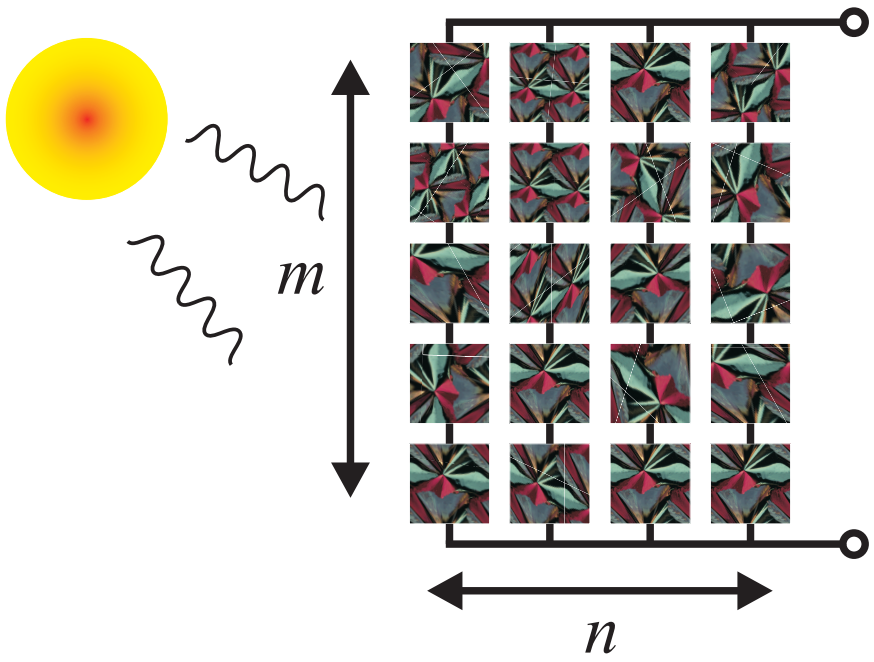


Figure 16: Rectangular array composed of $m \cdot n$ solar cells arranged in m rows and n columns.

array, which consists of m rows and n columns of identical solar cells, the column curves can be found by linearly scaling the cell curves in Figure 14. Cells connected in series share the same current, so for any arbitrary column current, I_{col}, the voltage across the column is

$$V_{col}(I_{col}) = \sum_{j=1}^{m} V_{cell,j}(I_{col}) = mV_{cell}(I_{col}) \tag{46}$$

where j is the j^{th} cell in the column. The summation is replaced with a multiplication by m because the voltage produced for each ideal cell is exactly the same for any current. Plugging in $I_{col} = 0$ in equation (46), we get the relationship for the column open circuit voltage, $V_{OC,col}$:

$$V_{OC,col} = mV_{cell}(0) = mV_{OC,cell} \tag{47}$$

Since current is the same through every cell in the column, the short circuit current for the column must be the same as the short circuit current of each cell:

$$I_{SC,col} = I_{SC,cell} \tag{48}$$

In addition, the knee current for the column, $I_{k,col}$, is the same as the knee current of each cell:

$$I_{k,col} = I_{k,cell} \tag{49}$$

This can be used in equation (46) to find $V_{k,col}$:

$$V_{k,col} = V_{col}(I_{k,col}) = mV_{cell}(I_{k,cell}) = mV_{k,cell} \tag{50}$$

Equations (49) and (50) show that the knee has moved only in voltage and not in current. This suggests that the P-V curve has moved with voltage and not current also.

The power produced by the column is just the column voltage times column current. Using this relationship and equation (46), we get

$$P_{col}(V_{col}) = V_{col}I_{col} = mV_{cell}I_{cell} = mP_{cell} \tag{51}$$

This says the power curve has been scaled by m, which implies the power at the knee has been scaled by m also. The power at the column's knee is

$$P_{k,col} = mP_{k,cell} \tag{52}$$

So a column of m identical, series-connected solar cells produces m times the power of one solar cell.

An array designer usually chooses the load resistance so that the solar cell operates at the knee. To get the R-V curve for the column, R_{col}, we just divide the column voltage by column current:

$$R_{col} = \frac{V_{col}}{I_{col}} = \frac{mV_{cell}}{I_{cell}} = mR_{cell} \tag{53}$$

This means the resistance required to operate at a specific I-V and P-V point is scaled up by m. So, the knee resistance has been scaled up by m also. In general, solar cell arrays with much more rows than columns ($m >> n$), called *vertical arrays*, can produce power for large load resistances.

3.2.2 The Ideal Row Array

The second step in finding the final array curves is summing the curves found from each individual column. In the ideal array case, where every cell is identical, each set of column curves is the same. In this section, the column curves can be treated like cell curves in case the solar cell array you are working with is just a single row. In other words, the subscripts 'col' and 'A' can be replaced with 'cell' and 'row', respectively, and the algebra would be exactly the same. This section uses the subscripts 'col' and 'A' to follow suit with the previous section.

The array current is the summation of currents produced by each column. So, for any arbitrary column voltage,

$$I_A(V_A) = \sum_{j=1}^{n} I_{col,j}(V_A) = nI_{col}(V_A) \tag{54}$$

where j is the j^{th} column in the array. The summation is replaced with a multiplication by n because the current produced by each ideal cell is exactly the same for any voltage. The short-circuit current is found by setting $V_A = 0$ in equation (54):

$$I_{SC,A} = nI_{col}(0) = nI_{SC,col} \tag{55}$$

Since the voltage across each column in the array is the same, the open circuit voltage of the array, $V_{OC,A}$, must be the same as the open circuit voltage of each column:

$$V_{OC,A} = V_{OC,col} \tag{56}$$

In addition, the knee voltage for the array, $V_{k,A}$ is the same as the knee voltage of each column:

$$V_{k,A} = V_{k,col} \tag{57}$$

This can be used in equation (54) to find the knee current for the array, $I_{k,A}$:

$$I_{k,A} = I_A(V_{k,A}) = nI_{col}(V_{k,col}) = nI_{k,col} \tag{58}$$

The previous two equations show that the knee has moved only with current and not with voltage. This suggests that the P-V curve has moved with current and not voltage also.

The power produced by the array is the array voltage times array current. Using this relationship and equation (54), the power curve is

$$P_A(I_A) = V_A I_A = V_{col} n I_{col} = n P_{col} \tag{59}$$

This says the power curve has been scaled by n, which implies the power at the knee has been scaled by n also. The array power at the knee is

$$P_{k,A} = V_{k,A} I_{k,A} = V_{k,col} n I_{k,col} = n P_{k,col} \tag{60}$$

So, an array of n identical, parallel-connected columns of solar cells produces n times the power of one column of solar cells.

An array designer usually chooses the load resistance so that the solar cell operates at the knee. To get the array resistance curve, R_A, the array voltage is divided by array current:

$$R_A = \frac{V_A}{I_A} = \frac{V_{col}}{n I_{col}} = \frac{R_{col}}{n} \tag{61}$$

This means the resistance required to operate at a specific I-V and P-V point is scaled down by n. So, the knee resistance has been scaled down by n also. In general, solar cell arrays with much more columns than rows ($n >> m$), called *horizontal arrays*, can produce power for small load resistances.

3.2.3 Combining Rows and Columns

Now the results of the previous two sections are combined to get the final array curves. The I-V curve was scaled by m in the voltage direction and scaled by n in the current direction. So, the set of I-V pairs, (I_{cell}, V_{cell}) that made up the solar cell I-V curve is scaled to make the new set of I-V pairs for the ideal solar cell array:

$$(I_A,\ V_A) = (n I_{cell},\ m V_{cell}) \tag{62}$$

This transformation is simple and intuitive. The voltage scales linearly upward with the number of series connections, and the current scales linearly upward with the number of parallel connections.

The power curve was scaled quadratically by m (equation (51)) and n (equation (59)), while voltage remained scaled up by m alone. The new set of P-V pairs, $(P_A,\ V_A)$ is

$$(P_A,\ V_A) = (mnP_{cell},\ mV_{cell})) \tag{63}$$

This transformation is also intuitive but not so simple. Since both voltage and current scale linearly, the power scales quadratically. This also says that the power scales linearly with the number of solar cells in the array. This trend is plotted in Figure 17. Notice that contour lines have been drawn on the m-n plane and that they follow constant L lines. This transformation is important in the design of solar cell arrays because there are many combinations of $(m,\ n)$ that create the same power. The designer may design a vertical array to power a large load or a horizontal array to power a small load both at the same power. So the power available from a solar cell array is not limited by the size of the load.

The resistance curve was first scaled up by m (equation (53)) and then scaled down by n (equation (61)), while voltage remained scaled up by m alone. The new set of R-V pairs, $(R_A,\ V_A)$ is

$$(R_A,\ V_A) = \left(\frac{m}{n}R_{cell},\ mV_{cell}\right) \tag{64}$$

Knee resistance gets large with increasing m and gets small with increasing n. This shows that $R_A >> R_{cell}$ for vertical arrays ($m >> n$), and $R_A << R_{cell}$ for horizontal arrays. This trend is plotted in Figure 18.

In an ideal situation, these transformations hold true. However, it is highly unlikely that any two solar cells are made exactly alike in reality because the fabrication process for solar cells is not exact. Fabrication processes such as screen printing,

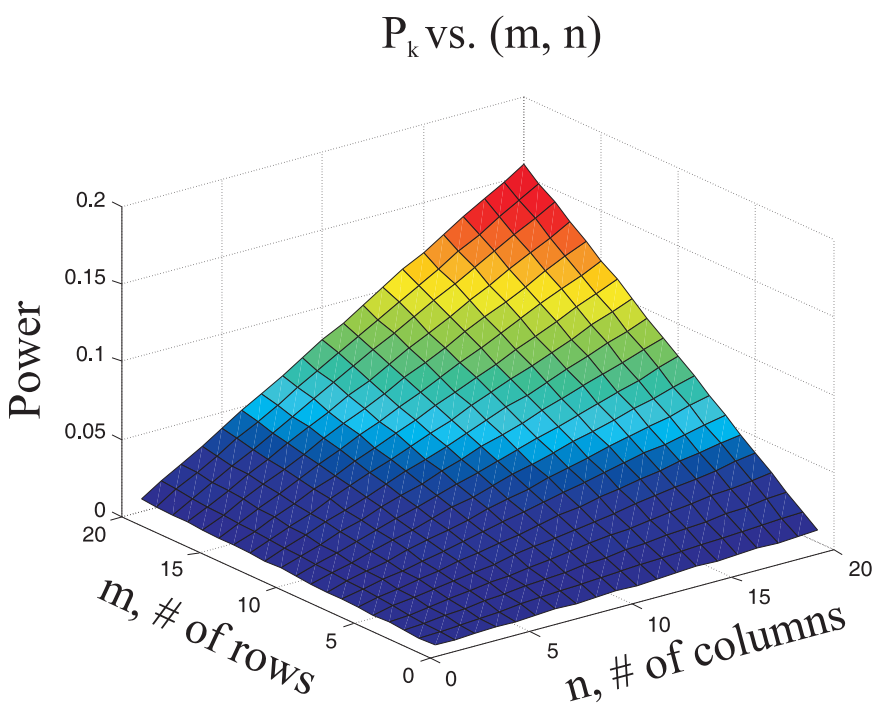


Figure 17: Knee power vs. (m, n). Knee power is proportional to the number of cells in the array.

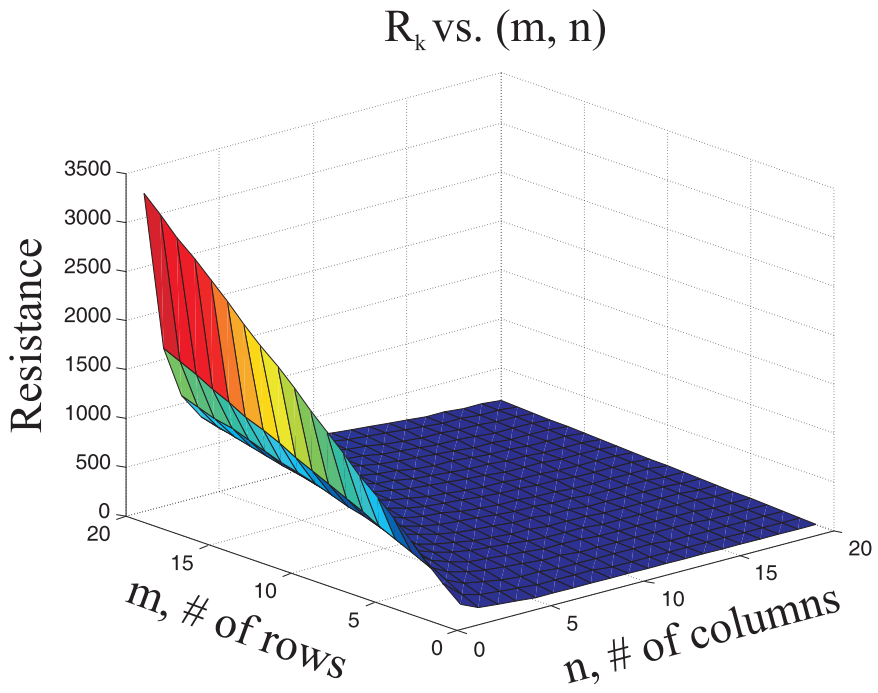


Figure 18: Knee resistance vs. (m, n). Solar cell arrays can be designed to power any kind of resistance.

thermal spraying, and chemical vapor deposition cannot consistently produce the same substrate thickness, length, and width due to limited precision [24] [20] [22]. In almost all solar cell arrays, the solar cells' circuit parameters, such as short-circuit current and open-circuit voltage, are not identical. The results derived for an ideal solar cell array are useful only for conceptual understanding and estimates of what a hypothetical solar cell array will produce. The next two sections discuss how array performance is changed when current and voltage mismatches are taken into account.

3.2.4 The Realistic Column Array

This section constructs column curves based on the individual cell curves comprising the column array. The voltage produced across the column is a summation of the voltages produced across each cell, which is dependent on the column current passing through the cells:

$$V_{col}(I_{col}) = \sum_{j=1}^{m} V_{cell,j}(I_{col}) \tag{65}$$

In the ideal array case, the summation is replaced with a multiplication by m. In the realistic case, the voltages produced across each cell are all different for any given column current, so the summation cannot be simplified.

The aggregation of these non-ideal voltages is illustrated graphically for three different I-V curves in Figure 19. To compute the column curve, the cell voltages are added along the constant current line, and the summation is plotted as a point on the column curve. This method of adding cell voltages is simple for constant current less than $I_{SC,1}$ because all voltages are in the first quadrant ($V > 0$, $I > 0$). However, the short circuit current of the column cannot be found unless the addition carries on beyond $I_{SC,1}$. The curves for cells one and two do not have current values in the first quadrant that go as high as the third cell's current values. So, information is needed about the current of cells one and two when large currents greater than their short circuit currents are forced through the column.

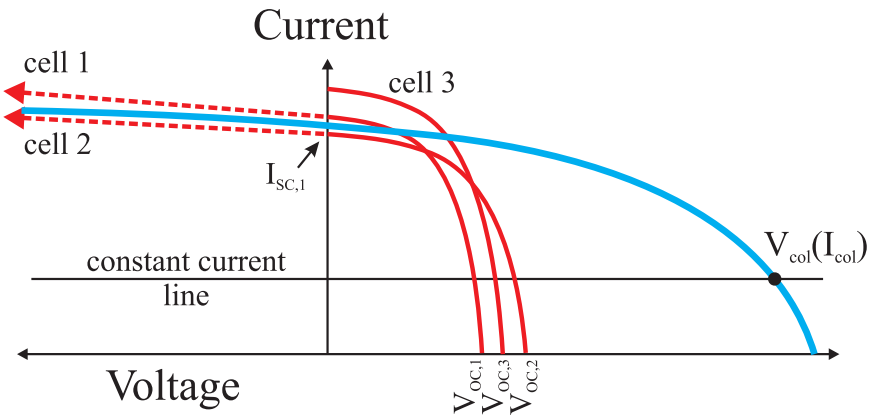


Figure 19: Graphical addition of the voltage of three, series-connected solar cells.

In fact, when the voltage across a solar cell goes negative, the current increases beyond its short circuit current. The approximate I-V equation from section 3.1.2 is

$$I \approx I_{PH} - I_S \left(e^{\frac{qV}{nkT}} - 1 \right) \tag{66}$$

From this equation, we can see that as V is negative, the exponential term gets smaller and I increases. So to get I-V values for cells one and two at the current levels of cell three, curves one and two must be extended into negative voltage.

This negative voltage region of cells one and two is a limitation on the column's power producing ability. If every cell in the column were identical to cell three, then the column would be able to produce more current at any voltage than in the realistic case. The resultant curve shows that the short circuit current of the column is very close to the short circuit current of cell two, which means the column current is limited by cell two for any column voltage.

The entire I-V curve of the random column appears limited in the current direction when compared to an ideal column's I-V curve. The random column voltage is expected to be unchanged from the ideal column voltage because the expected value of the open-circuit voltage of a random column is $mE[V_{cell}]$, where $E[V_{cell}]$ is the expected value of a random cell's voltage. The random column current is limited, and

can be related to the ideal column's current with

$$I_{col} = \kappa_c(m,n) I_{ideal\,col} \tag{67}$$

$\kappa_c(m,n)$ is a constant less than one and applies for current-limited columns. It is a function of m and n, but depends mostly on m. This substitution works for every point on the I-V curve, so the power curve of the realistic column can be written as

$$P_{col} = V_{col}\kappa_c(m,n) I_{ideal\,col} \tag{68}$$

And since $E[V_{col}] = V_{ideal\,col}$ and the column current is the same as the cell current, we can write the power as

$$P_{col} = \kappa_c(m,n) m V_{cell} I_{cell} = \kappa_c(m,n) m P_{cell} \tag{69}$$

This statement says that the power at any column voltage is smaller for a realistic column than for an ideal column.

In general, the weakest solar cell limits the total column current output [28]. However, the column voltage is not limited at all by any particular solar cell because the cell voltage across one cell does not affect the voltage across any other cell. So, the power produced by the column is only limited by the weakest cell's current capabilities. The converse will be true for the realistic row array. Instead of current limitations, the realistic row experiences voltage limitations.

3.2.5 The Realistic Row Array

This section finds row curves based on the individual cell curves comprising the row array. The current produced from the row is a summation of the currents produced through each cell, which is dependent on the row voltage across the cells:

$$I_{row}(V_{row}) = \sum_{j=1}^{n} I_{cell,j}(V_{row}) \tag{70}$$

In the ideal array case, the summation was replaced with a multiplication by n. In the realistic case, the currents produced through each cell are all different for any given row voltage, so the summation cannot be simplified.

This summation is illustrated graphically for three different I-V curves in Figure 20. The cell currents are added along a constant voltage line, and the summation is plotted as a point on the row curve. This method of adding cell currents is simple for constant voltage less than the open circuit voltage of the first cell because all voltages are in the first quadrant ($V > 0,\ I > 0$). However, the open circuit voltage of the row cannot be found unless the addition carries on beyond the open circuit voltage of cell one. The curves for the first and third cells do not have voltage values in the first quadrant that go as high as cell two's voltage values. So, we need to know what happens to the voltage of the first and third cells when large voltages greater than their open circuit voltages are forced across the row. In fact, when the current through a solar cell goes negative, the voltage increases beyond its open circuit voltage value. The I-V equation approximation from equation (66) can be rearranged to solve for V:

$$V = \frac{nkT}{q} \ln\left(\frac{I_{PH} - I}{I_S} + 1\right) \tag{71}$$

From this equation, the term inside the logarithm gets larger as I goes negative, which means V gets larger as well. The increase of V for $I < 0$ is very gradual, and appears to be almost linear compared to the I-V curvature in the first quadrant. Curves one and three must be extended into negative current to get I-V values for the first and third cells at the voltage levels of the second cell.

The random row I-V curve appears limited in the voltage direction, but not the current direction, when compared to an ideal row's I-V curve. The random row current is expected to be unchanged from the ideal row current because its the short-circuit current expected value of a random row is $nE[I_{cell}]$. The random row voltage

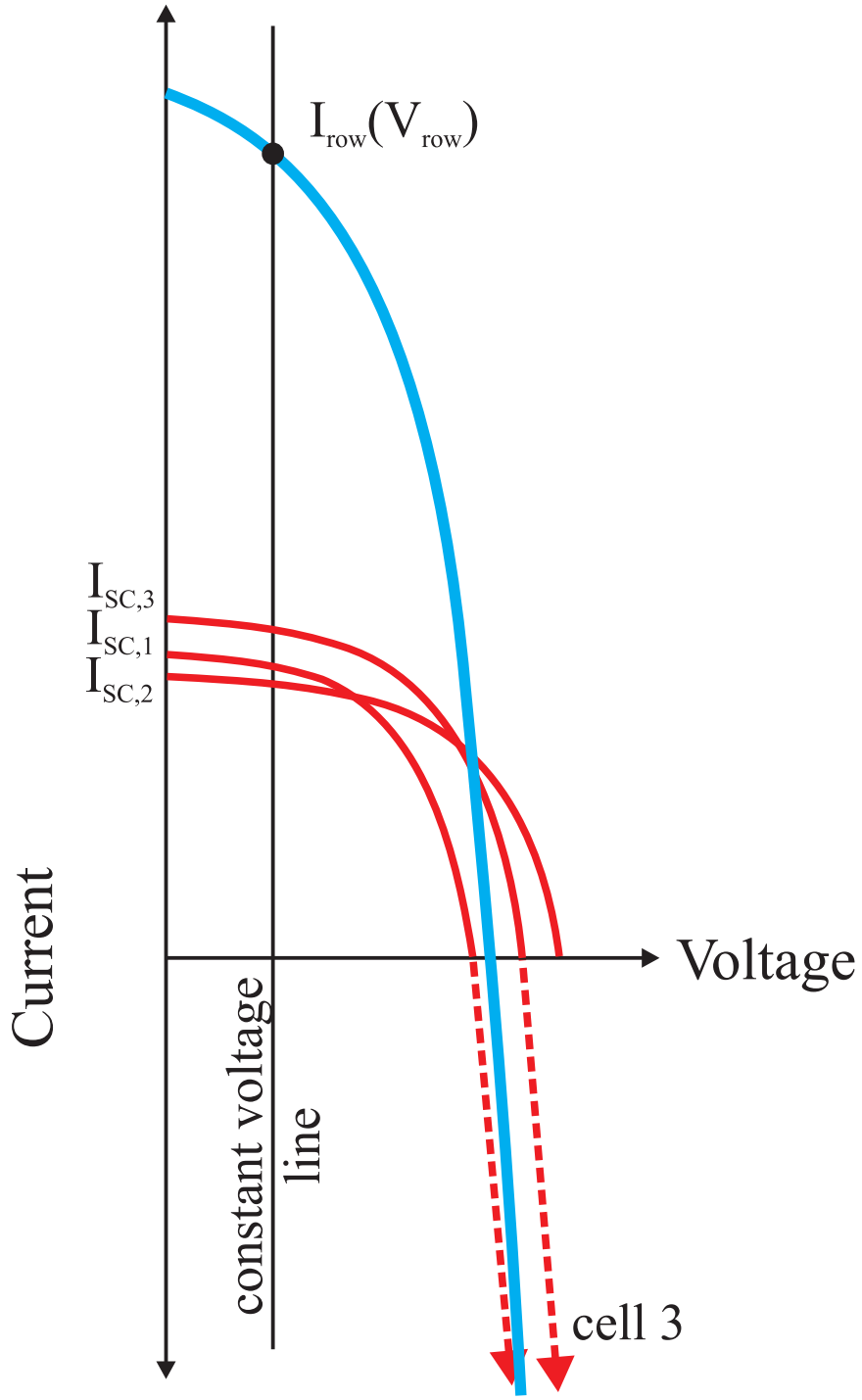


Figure 20: Graphical addition of the current of three, parallel-connected solar cells.

is limited, and can be related to the ideal row's voltage with

$$V_{row} = \kappa_r(m,n)V_{ideal\,row} \tag{72}$$

$\kappa_r(m,n)$ is a constant less than one and applies for voltage-limited rows. It is a function of m and n, but depends mostly on n. This substitution works for every point on the I-V curve, so the power curve of the realistic column can be written as

$$P_{col} = I_{col}\kappa_r(m,n)V_{ideal\,col} \tag{73}$$

And since $E[I_{row}] = I_{ideal\,row}$ and the row voltage is the same as the cell voltage, we can write the power as

$$P_{row} = \kappa_r(m,n)nV_{cell}I_{cell} = \kappa_r(m,n)nP_{cell} \tag{74}$$

This statement says the power at any row current is smaller for a realistic row than for an ideal row.

In general, the weakest solar cell limits the row voltage output. However, the row current is not limited at all by any particular solar cell because the current through one cell does not affect the current through any other cell. So, the power produced by the row is only limited by the weakest cell's voltage capabilities.

3.2.6 Combining Realistic Rows and Columns

Now, the results of the previous two sections are combined to get the total realistic array curves. In section 3.2.4, we found that the current was limited by the weakest cell in the column, and the voltage was scaled by $\kappa_c(m,n)m$. In section 3.2.5, we found that the voltage was limited by the weakest cell in the row, and the current was scaled by $\kappa_r(m,n)n$. So, the set of I-V pairs, $(I_{cell},\ V_{cell})$ that made up the solar cell I-V curve is scaled to make the new set of I-V pairs for the realistic solar cell array:

$$(I_A,\ V_A) = (\kappa_c(m,n)nI_{cell},\ \kappa_r(m,n)mV_{cell}) \tag{75}$$

This transformation is similar to the ideal solar cell array transformation except for the current and voltage limitations, $\kappa_c(m,n)$ and $\kappa_r(m,n)$.

The power curve was scaled quadratically by $\kappa_c(m,n)$ and m (equation (69)) and $\kappa_{col}(m,n)$ and n (equation (69)), while voltage remained scaled up by κ_c and m alone. As a result, the new set of P-V pairs, $(P_A,\ V_A)$ is

$$(P_A,\ V_A) = (\kappa_r(m,n)\kappa_c(m,n)mnP_{cell},\ \kappa_r(m,n)mV_{cell}) \tag{76}$$

This transformation says that the power is linearly proportional to the number of cells, mn, but also linearly proportional to the product of column and row limitation variables, $\kappa_{col}(m,n)\kappa_{row}(m,n)$.

The resistance curve is first scaled up by $\kappa_c(m,n)m$ and then scaled down by $\kappa_r(m,n)n$, while voltage remained scaled up by $\kappa_c(m,n)m$ alone. The new set of R-V pairs, $(R_A,\ V_A)$ is

$$(R_A,\ V_A) = \left(\frac{\kappa_r(m,n)m}{\kappa_c(m,n)n}R_{cell},\ \kappa_r(m,n)mV_{cell}\right) \tag{77}$$

Just like the voltage, current, and power transformations, the resistance transformation is affected by the array limitation variables.

3.3 Solar Cell Manufacturing

There are not many solar cells that are created equal, and this is due to manufacturing tolerances. The actual circuit parameters of each cell produced can be characterized as a normally-distributed random variable with a mean, μ, and standard deviation, σ.

The circuit parameters that are pertinent to this research are

- Photon Current Density $(J_{PH}) = N(\mu_{J_{PH}},\ \sigma^2_{J_{PH}})\ \left(\frac{A}{cm^2}\right)$
- Reverse Saturation Current Density $(J_S) = N(\mu_{J_S},\ \sigma^2_{J_S})\ \left(\frac{A}{cm^2}\right)$
- Cell Area $(A) = N(\mu_A,\ \sigma^2_A)\ (cm^2)$

- Ideality Factor $(n) = N(\mu_n,\, \sigma_n^2)$
- Parallel Resistance $(R_P) = N(\mu_{R_P},\, \sigma_{R_P}^2)\ \left(\frac{\Omega}{cm^2}\right)$
- Series Resistance $(R_S) = N(\mu_{R_S},\, \sigma_{R_S}^2)\ \left(\frac{\Omega}{cm^2}\right)$

Here, $N(\mu,\, \sigma^2)$ represents the normal distribution function with mean μ and variance σ^2. From these random cell parameters, the short-circuit current and open-circuit voltage variables can be found using equations (132) and (136) respectively. Short-circuit current density and open-circuit voltage are functions of random variables. The means and standard deviations of J_{SC} and V_{OC} are dependent from the means and standard deviations of the random cell parameters by equations (132) and (136).

These six random variables have an effect on the array limitation variables, $\kappa_r(m, n)$ and $\kappa_c(m, n)$. As shown in section 3.2.4, vertical arrays suffer if the short-circuit current density of each cell varies wildly. This would make $\kappa_c(m, n)$ smaller. So, a large $\sigma_{J_{SC}}$ creates a small $\kappa_c(m, n)$. Likewise, the same is true of open-circuit voltage and horizontal arrays: large $\sigma_{V_{OC}}$ creates a small κ_r.

The solar cells used in this research are the organic solar cells based on pentacene and C_{60} (also known as Buckminsterfullerene) from the paper by Yoo, Domercq, and Kippelen [27]. Typical values of the random cell parameters for these organic solar cells are:

- Photon Current Density $(J_{PH}) = N(0.015,\, 0.0014^2)\ \left(\frac{A}{cm^2}\right)$
- Reverse Saturation Current Density $(J_S) = N(54 \cdot 10^{-6},\, (8 \cdot 10^{-6})^2)\ \left(\frac{A}{cm^2}\right)$
- Cell Area $(A) = N(0.13,\, 0.01)\ (cm^2)$
- Ideality Factor $(n) = N(2.5,\, 0.075^2)$
- Parallel Resistance $(R_P) = N(328,\, 10^2)\ \left(\frac{\Omega}{cm^2}\right)$
- Series Resistance $(R_S) = N(2.04,\, 0.04^2)\ \left(\frac{\Omega}{cm^2}\right)$

These values were adapted from the paper. These will be the default values for a random solar cell for the analysis in the subsequent section.

CHAPTER IV

EXPERIMENTAL DESIGN

The basis for choosing either the array option (AO) or the charge pump option (CPO) is the number of solar cells required to power the load at the specified power. The hypothesis is manufacturing processes that result in cells of highly varied short-circuit current density (large $\sigma_{J_{SC}}$) will make the charge pump option more economical for large DC load resistances.

4.1 Array Option

The specified load resistance, R_L, and the specified load power, P_L, require a specially-sized solar cell array that produces knee resistance, R_k, approximately equal to load resistance and knee power, P_k, approximately equal to load power. The array limitation variables are used to find the dimensions of this array. The two variables are the array dimensions, m_1 and n_1. The voltage and current transformations from equation (75) are the two equations used to find m_1 and n_1. Adapted from section 3.2.6, the transformations are

$$(I_L,\ V_L) = (\kappa_c(m_1, n_1)n_1 I_{cell},\ \kappa_r(m_1, n_1)m_1 V_{cell}) \tag{78}$$

The load current, I_L, and load voltage, V_L, can be solved using load resistance and load power:

$$I_L = \sqrt{\frac{P_L}{R_L}} \tag{79}$$

$$V_L = \sqrt{P_L R_L} \tag{80}$$

Now, m_1 and n_1 can be solved rearranging the voltage and current transformations:

$$m_1 = \frac{1}{\kappa_r(m_1, n_1)} \frac{V_L}{V_{cell}} \tag{81}$$

$$n_1 = \frac{1}{\kappa_c(m_1, n_1)} \frac{I_L}{I_{cell}} \tag{82}$$

These two equations show how sensitive m_1 and n_1 are to the array limitation variables. A large current mismatch between solar cells makes κ_c small, and n_1 large. So, an array that produces limited current through its columns requires more columns to meet a specified load current. The total number of solar cells used in this option is $L_1 = m_1 n_1$. Comparing this total to the total in the charge pump option will determine which option to use.

4.2 Charge Pump Option

The same system of equations can be used to find the solar cell array dimensions, m_2 by n_2 for the charge pump option. The Dickson charge pump has an imperfect power efficiency ($\eta < 1$), so the knee power supplied by its input solar cell array is

$$P_k = P_{in} = \frac{P_L}{\eta} \tag{83}$$

This input power is larger than load power since the power efficiency is imperfect. The knee resistance for the input solar cell array can be found by using the expression for input resistance in a Dickson charge pump. This equation, adapted from section 2.1.4, is

$$R_k = R_{in} = \frac{R_L}{\eta\,(N+1)^2} \tag{84}$$

In most cases, input resistance is less than load resistance since power efficiency is usually greater than 25% and there is at least one stage ($N \geq 1$).

Now, input voltage and current to the Dickson charge pump can be found using these values of knee power and knee resistance:

$$I_{in} = \sqrt{\frac{P_{in}}{R_{in}}} \tag{85}$$

$$V_{in} = \sqrt{P_{in} R_{in}} \tag{86}$$

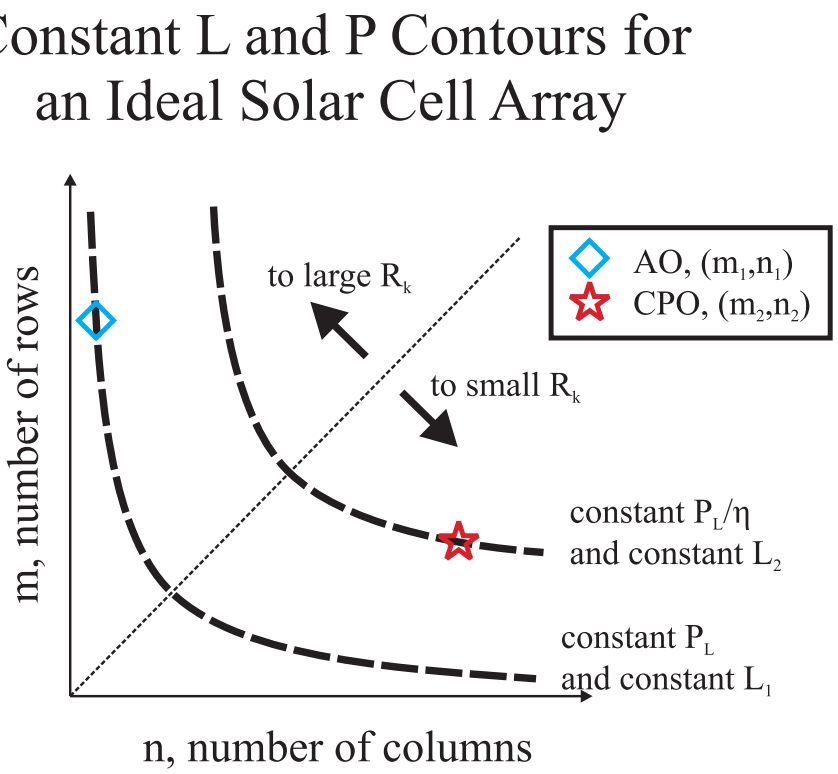


Figure 21: Contour plots of constant number-of-cells, L, and constant knee power, P_k.

Then, the dimensions m_2 and n_2 can be found using the same system of equations as before:

$$m_2 = \frac{1}{\kappa_r(m_2, n_2)} \frac{V_{in}}{V_{cell}} \tag{87}$$

$$n_2 = \frac{1}{\kappa_c(m_2, n_2)} \frac{I_{in}}{I_{cell}} \tag{88}$$

The total number of solar cells used in this array is $L_2 = m_2 n_2$. Comparing this total with L_1 will determine which option to choose.

In an ideal array, $\kappa_r = \kappa_c = 1$ for all (m, n). So, the comparison of L_1 with L_2 will look like the graph in Figure 21. Both sets of dimensions lie on constant power and constant number-of-cells curves, and $L_2 > L_1$ in the figure.

However, if a realistic solar cell array is analyzed, then the cell limitation variables, $\kappa_r(m, n)$ and $\kappa_c(m, n)$ are included. In this realistic case, the cell limitation variables may skew the constant power curves to look like Figure 22. In the graph, the constant

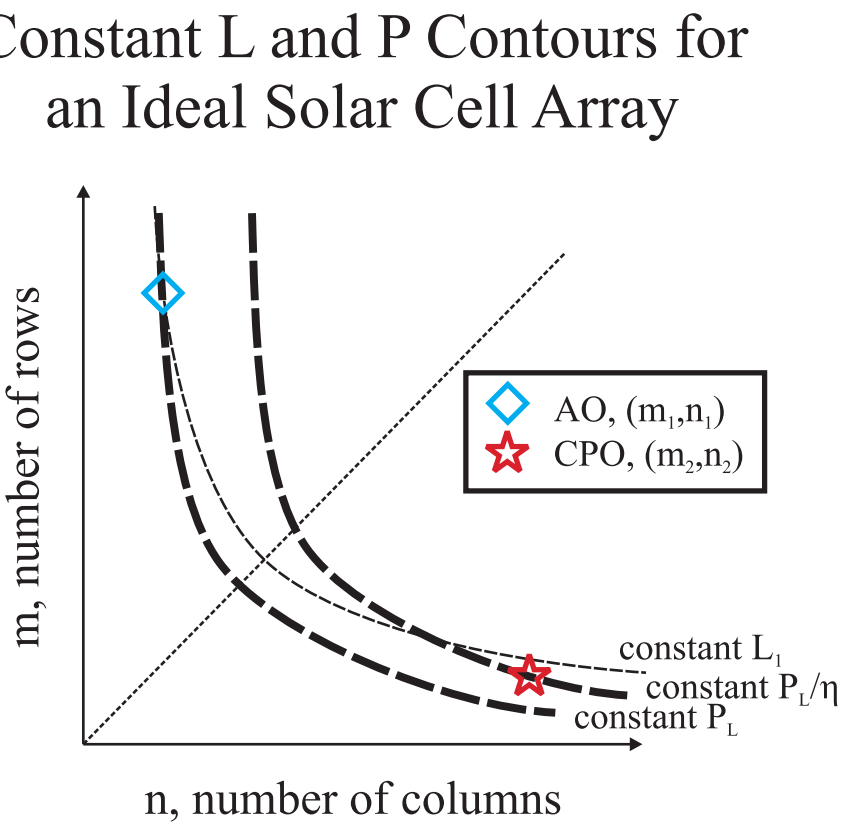


Figure 22: Skewed contour plots of constant knee power, P_k.

P_L/η curve dips below the constant L_1 curve, and the CPO dimensions are chosen so that $L_2 < L_1$.

The situation in Figure 22 is hypothetical, where horizontal arrays perform better than vertical arrays. In such a situation, the cell limitation variables are negligible for small m and large n, but significant for large m and small n. This situation should occur when the current produced by each solar cell varies significantly more than the voltage produced by each solar cell. So, solar cells with large $\sigma_{J_{SC}}$ should benefit by using the charge pump option.

4.3 Procedure

Simulations of solar cell arrays with random parameters are used to verify this hypothesis in the next chapter. The simulation procedure finds the cell limitation variables for a large sample of rows and columns, iterates over each dimension point as possible

AO dimensions, compares the AO dimensions to all corresponding CPO dimension points, and marks every dimension point that benefits from a Dickson charge pump.

4.3.1 Find the Cell Limitation Variables

The input variables to the simulation are:

- Photon Current Density standard deviation, $\sigma_{J_{PH}}$ $\left(\frac{A}{cm^2}\right)$
- Reverse Saturation Current Density standard deviation, σ_{J_S} $\left(\frac{A}{cm^2}\right)$
- Cell Area standard deviation, σ_A (cm^2)
- Ideality Factor standard deviation, σ_n
- Parallel Resistance standard deviation, σ_{R_P} $\left(\frac{\Omega}{cm^2}\right)$
- Series Resistance, σ_{R_S} $\left(\frac{\Omega}{cm^2}\right)$
- Dickson charge pump power efficiency, η

The expected values for each random cell parameter correspond to the values adapted from Yoo et. al. [27] and are coded within the simulation. For this simulation, the sample size of the dimension space, (m, n) is $1 \leq m \leq 75$ and $1 \leq n \leq 75$.

The first step in finding the array limitation variables, $\kappa_r(m, n)$ and $\kappa_c(m, n)$ for a large sample of (m, n) is finding the curves of an "ideal" solar cell, where the standard deviation of each random cell parameter is set to zero. The curves are cell current, I_{cell}, cell power, P_{cell}, and cell resistance, R_{cell}, which correspond to a domain of voltage, V_{cell}.

The second step is to find the expected values of the array I-V curves for every possible combination of (m, n). This is accomplished by finding many samples of the random I-V curves for each (m, n) and taking the average. In this simulation, the average was taken over 20 samples.

The final step is calculating the cell limitation variables using the average I-V curves, which are found using these equations:

$$\kappa_r(m,n) = \frac{1}{m}\frac{E[V_{array}]}{V_{cell}} \tag{89}$$

$$\kappa_c(m,n) = \frac{1}{n}\frac{E[I_{array}]}{I_{cell}} \tag{90}$$

Here, $E[\ ]$ denotes expected value. The simulation iterates over all combinations of (m,n) to find $\kappa_r(m,n)$ and $\kappa_c(m,n)$.

4.3.2 Compare Array Option to Charge Pump Option

Now, iterate over all combinations of (m,n), and make comparisons of the total number of cells used in the array option and in the charge pump option. For each iteration, treat the current dimensions as (m_1,n_1), the dimensions used in the array option.

First, find the corresponding load power for this iteration using:

$$P_L = \kappa_r(m_1,n_1)\kappa_c(m_1,n_1)m_1n_1P_{k,cell} \tag{91}$$

where $P_{k,cell}$ is the knee power of the "ideal" solar cell.

Second, find the corresponding P_L/η constant-power curve on which the charge pump option would operate. The knee power of each array along this constant-power curve should be at least P_L/η and not much larger than P_L/η. In this simulation, a window of $1.0P_L/\eta$ and $1.05P_L/\eta$ was used.

Third, find the points along the P_L/η constant-power curve that have fewer total number of cells. If at least one point exists that has fewer than m_1n_1 cells, then (m_1,n_1) is labeled as a *DC to DC point*. These points represent a load power and load resistance combination that would benefit from the use of a generic DC to DC converter, which does not have an input voltage requirement.

Fourth, find the points along the P_L/η constant-power curve that have fewer total number of cells and can realistically power a Dickson charge pump ($fC > 0$). It

is sometimes the case that the specifications for power efficiency, input voltage, and diode threshold voltage force $fC < 0$, which means a Dickson charge pump cannot be built. The design equation for the product fC is (from section 2.2.1):

$$fC = \frac{\lfloor N \rfloor}{R_L} \left[\frac{\eta_{recalc}}{1 - \eta_{recalc} - \frac{V_t}{V_{in}}} \right] \tag{92}$$

The denominator term, $1 - \eta_{recalc} - \frac{V_t}{V_{in}}$ determines the polarity of fC, and it is critical that V_{in} is large enough to make fC positive. So, for every point along the P_L/η constant-power curve that has fewer total solar cells, check the polarity of fC, and only record the points that have positive fC. If at least one of these points exists, then (m_1, n_1) is marked as a "CPO point".

All CPO points represent pairs of load resistances and load powers that could benefit from a properly designed Dickson charge pump. The hypothesis is that manufacturing processes that result in cells of highly varied short-circuit current density (large $\sigma_{J_{SC}}$) will make the charge pump option more economical for large DC load resistances (corresponding to vertical arrays).

CHAPTER V

RESULTS

The data shown in this section show how manufacturing tolerances on all of the solar cell basic circuit parameters affect the number of cells needed to power a DC load. In addition, for each case where solar cell savings are possible, the feasibility of the Dickson charge pump is presented. First, the cell limitation variables are presented for variances on each circuit parameter, which shows the effectiveness of each parameter on array power production. Then, the feasibility of designing a Dickson charge pump is presented for the parameters that significantly affect array power production. The Dickson charge pump is mostly infeasible for the organic solar cells analyzed in this research because of the minimum input voltage limitation. However, a generic DC to DC converter could be used if allowed to have a low input voltage on the order of a few Volts.

5.1 Array Limitation Variables

Overall, there are only two random circuit parameters that affected the number of solar cells needed to power a load: photon current density, J_{PH}, and cell area, A. The other random circuit parameters, series resistance, R_S, parallel resistance, R_P, diode ideality factor, n, and reverse saturation current density, J_S, all had a negligible effect.

The array limitation variables, $\kappa_r(m,n)$ and $\kappa_c(m,n)$ were found for large standard deviations of each random circuit parameter while the other random circuit parameters were held at zero standard deviation. Then, the multiplication of these two variables, $\kappa_r(m,n)\kappa_c(m,n)$, are plotted for the domain $(1 \leq m \leq 50, 1 \leq n \leq 50)$. Note that small values of $\kappa_r(m,n)\kappa_c(m,n)$ indicate an m by n sized array is heavily

limited in its power producing capabilities. Also note that an ideal array will have $\kappa_r(m,n)\kappa_c(m,n) = 1$ for all (m,n).

5.1.1 Array Limitation for Photon Current Density

Figure 23 shows the array limitation across the m-n plane for a standard deviation, $\sigma_{J_{PH}} = 0.0028\ \frac{A}{cm^2}$, which is double the default value of $\sigma_{J_{PH}} = 0.0014\ \frac{A}{cm^2}$. The array limitation surface in the figure is mostly related to m and unrelated to n.

For horizontal arrays, where $m < 5$ in the figure, the array is not hindered much by current mismatch. Arrays in this region perform comparatively well to an ideal array. However, there is a steep drop-off starting after $m = 1$, and the surface becomes more gentle for $m > 15$. The reason for the steep drop-off is large-row arrays are more likely to contain a weak-current solar cell, where J_{PH} is small, than small-row arrays. Large-row arrays are highly likely to have a weak-current solar cell. The array limitation is approximately the same (0.79) for arrays with $m > 15$.

Variations on photon current density heavily affect the performance of the array and may serve as a cell parameter that allows a Dickson charge pump to save the use of a few cells. A load resistance and load power that places the AO array dimensions in the large-row region ($m > 15$) will require more solar cells than a corresponding CPO array operating in the small-row region.

5.1.2 Array Limitation for Cell Area

Figure 24 shows the array limitation across the m-n plane for a standard deviation, $\sigma_A = 0.02\ cm^2$, which is double the default value of $\sigma_A = 0.01\ cm^2$. The shape of the array limitation surface is approximately the same as in the previous section for photon current density because photon current density is linearly dependent on cell area.

The same observations as in the previous section are made here. Arrays with $m < 5$ perform comparatively well to ideal arrays, and arrays with $m > 15$ are

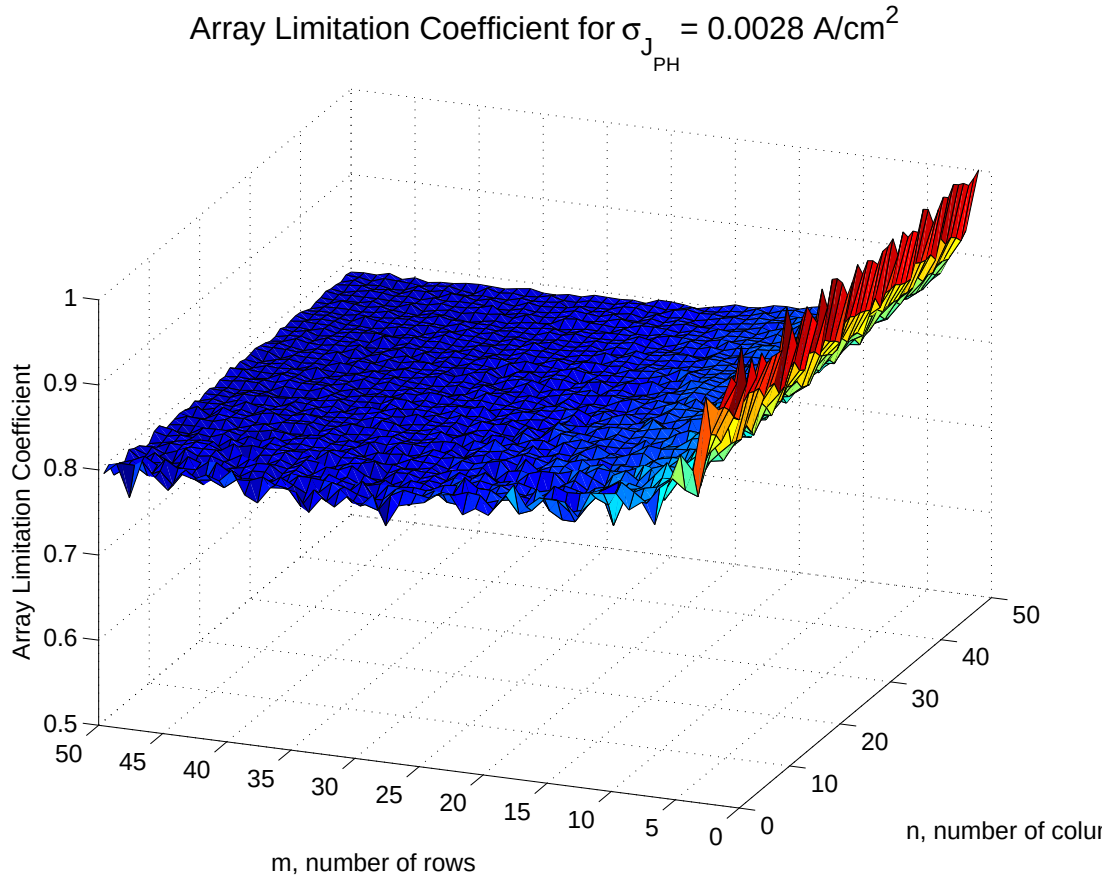


Figure 23: Array limitation for $\sigma_{J_{PH}} = 0.0028\ \frac{A}{cm^2}$. The surface appears almost flat for $m > 15$

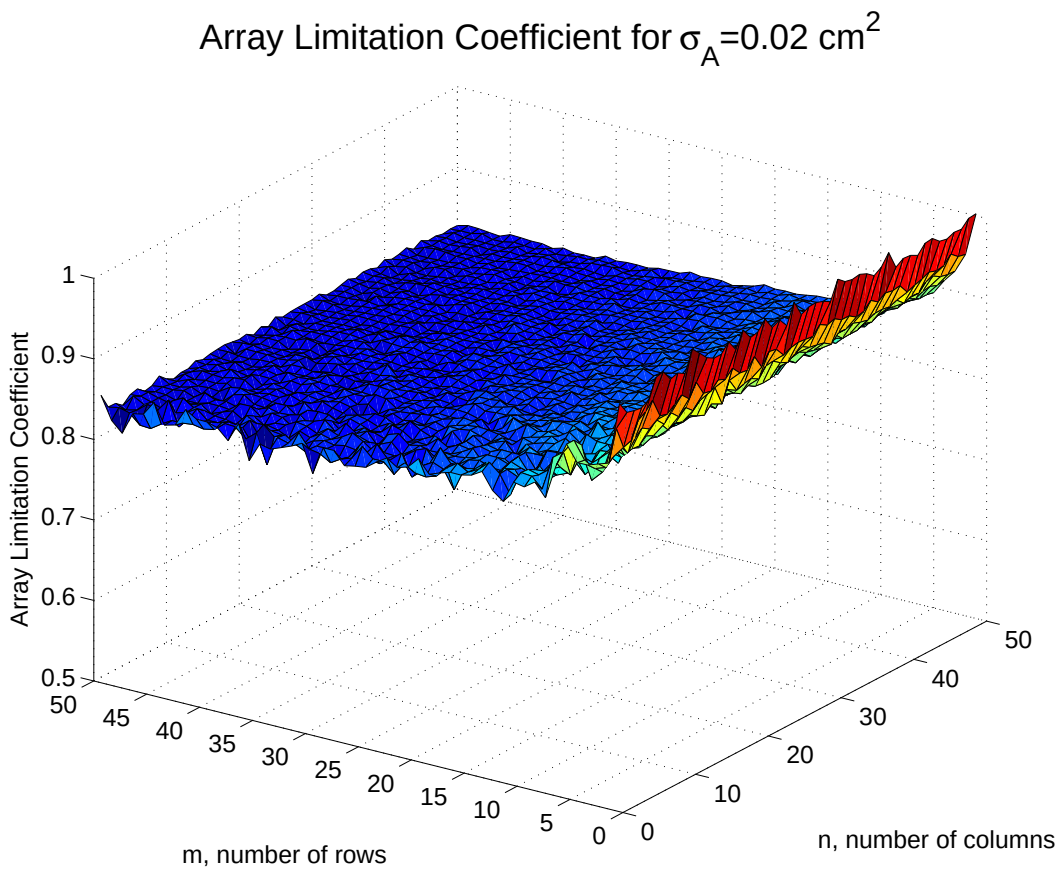


Figure 24: Array limitation for $\sigma_A = 0.02\ cm^2$. The surface appears almost flat for $m > 15$, similar to the case where $\sigma_{J_{PH}} = 0.0028\ \frac{A}{cm^2}$

limited by approximately the same amount (0.83). Variations on cell area heavily affect the performance of the array, so it may be a random cell parameter that allows a Dickson charge pump to save the use of a few solar cells.

5.1.3 Array Limitation for Other Basic Random Circuit Parameters

Figure 25 shows the array limitation across the m-n plane for standard deviations $\sigma_{R_S} = 0.16\ \frac{\Omega}{cm^2}$, $\sigma_{R_P} = 40\ \frac{\Omega}{cm^2}$, $\sigma_n = 0.3$, and $\sigma_{J_S} = 32 \cdot 10^{-6}\ \frac{A}{cm^2}$, which are quadruple their respective default values. These standard deviations are comparatively wider than that of photon current density and cell area, but it helps show how unrelated array performance is to variances these random parameters.

The array limitation surfaces in the figure are approximately the same as an ideal

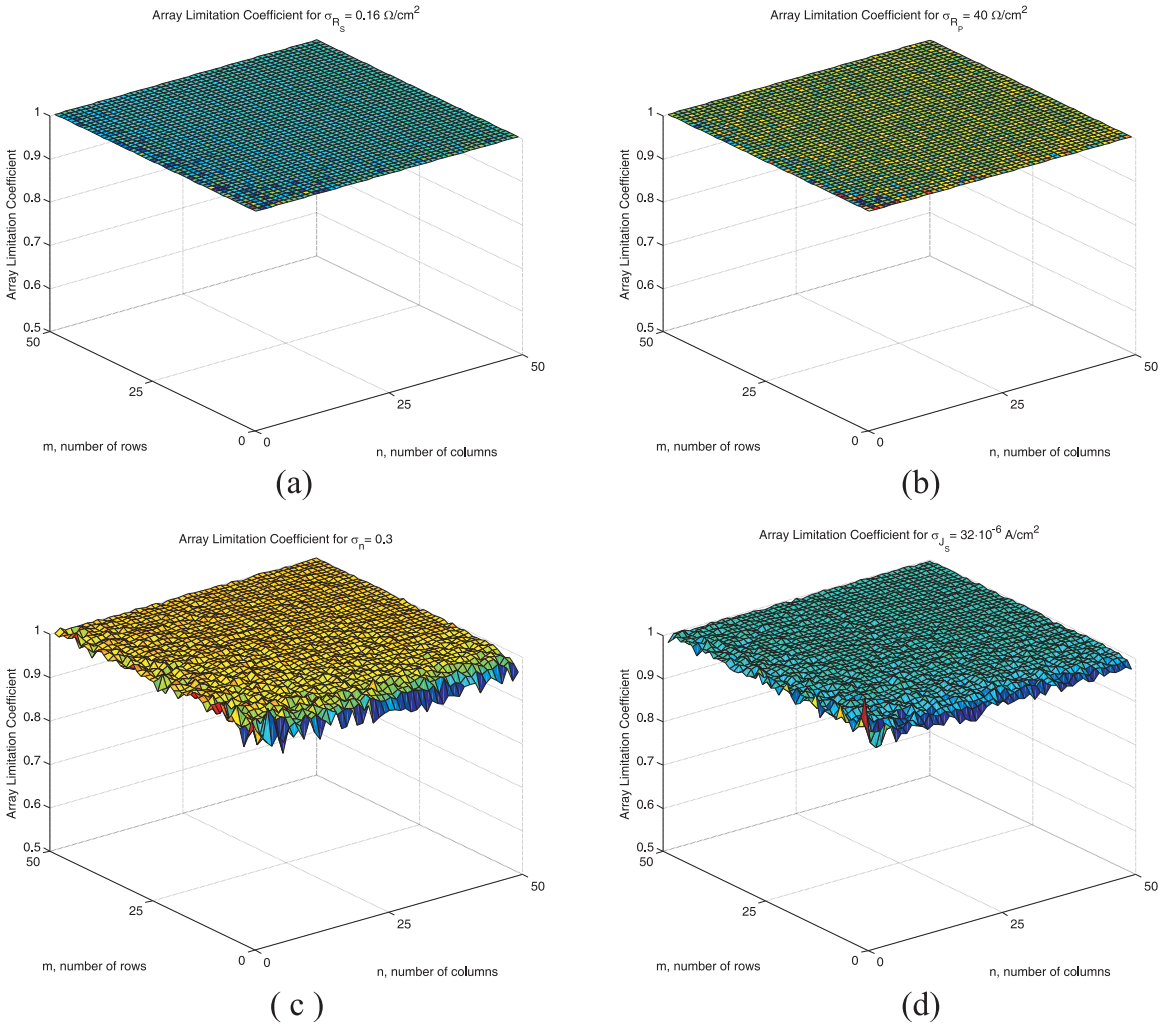


Figure 25: Array limitation for large standard deviations of (a) series resistance, R_S, (b) parallel resistance, R_P, (c) ideality factor, n, and (d) reverse saturation current density, J_S. These array limitations appear approximately the same as an ideal array.

array. Ideal arrays can never benefit from the use of a DC to DC converter because knee power is influenced only by the number of cells in the array and not the array limitation variables as explained in section 3.2.3. So a large variance on any of these random parameters would not promote the use of a Dickson charge pump to save the use of solar cells for powering a DC load.

5.2 DC to DC points and CPO points for Short-Circuit Current Density and Cell Array

Certain combinations of load resistance and load power coupled with a large standard deviation of short-circuit current density or cell area benefit from the use of a DC to DC converter or sometimes a Dickson charge pump. The results in this section show precisely what load resistance and load power combinations allow the CPO to be more cell-economical.

The first set of graphs in each sub-section show the load resistance and load power combinations that can be powered with fewer solar cells with a generic DC to DC converter at 90% power efficiency, (the DC to DC points). The second set of graphs in each sub-section show the load resistance and load power combinations that can be powered using a Dickson charge pump (the CPO points), if they exist. The CPO points are more restrictive than the generic DC to DC converter points because of the product fC limitation described in section 4.3.2.

5.2.1 Photon Current Density

Figures 26 and 27 show the DC to DC points for the double-default and triple-default standard deviation values of photon current density. A simulation for the default value of photon current density standard deviation was run, but no DC to DC points or CPO points were recorded. This is due to an insignificant array limitation coefficient, which has a minimum of 0.92 (92% of an ideal array power) for large-row arrays. There are no CPO points in any of these simulations because the minimum voltage

requirement for Dickson charge pumps could not be met.

Figure 26 shows the maximum power boundary is a load power of 91.7 mW, and the minimum load resistance boundary is 7 Ω for a standard deviation, $\sigma_{J_{PH}} = 0.0028$ $\frac{A}{cm^2}$. The colored region mostly covers the dimensions for vertical arrays, which supports the hypothesis that large cell-current variability allows a DC to DC converter to save the use of a few solar cells. The original hypothesis implies the use of the Dickson charge pump, but the input voltage requirement is too restrictive.

Figure 27 shows the maximum power boundary is a load power of 212 mW, and the minimum load resistance boundary is 3.4 Ω for a standard deviation, $\sigma_{J_{PH}} = 0.0042$ $\frac{A}{cm^2}$. The region increased in size from the double-default standard deviation simulation in Figure 26. The drawn boundaries do not closely hug the colored region on all sides mainly due to the random nature of the simulation.

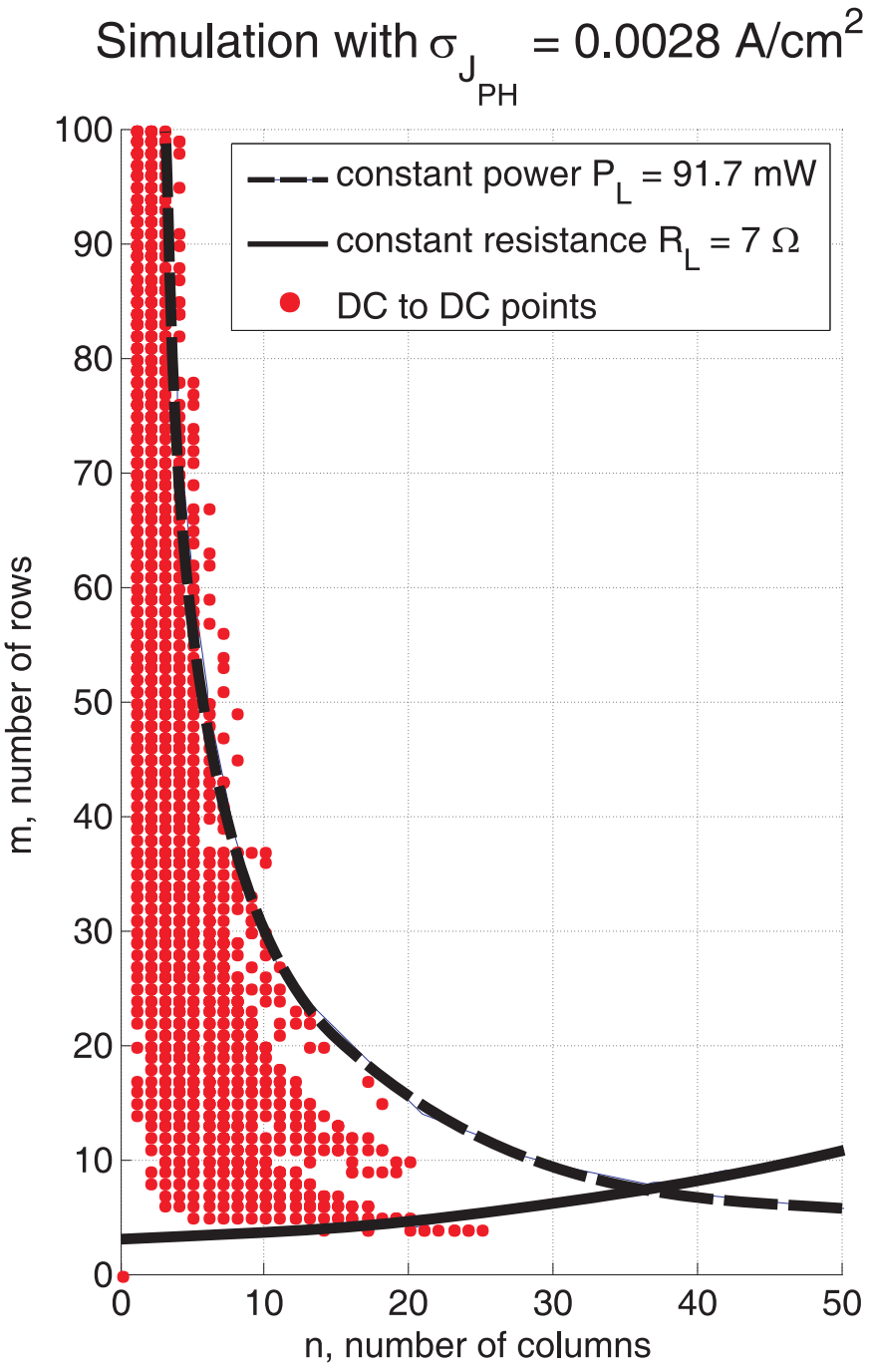


Figure 26: Minimum load resistance and maximum load power boundaries for double the default value of photon current density standard deviation.

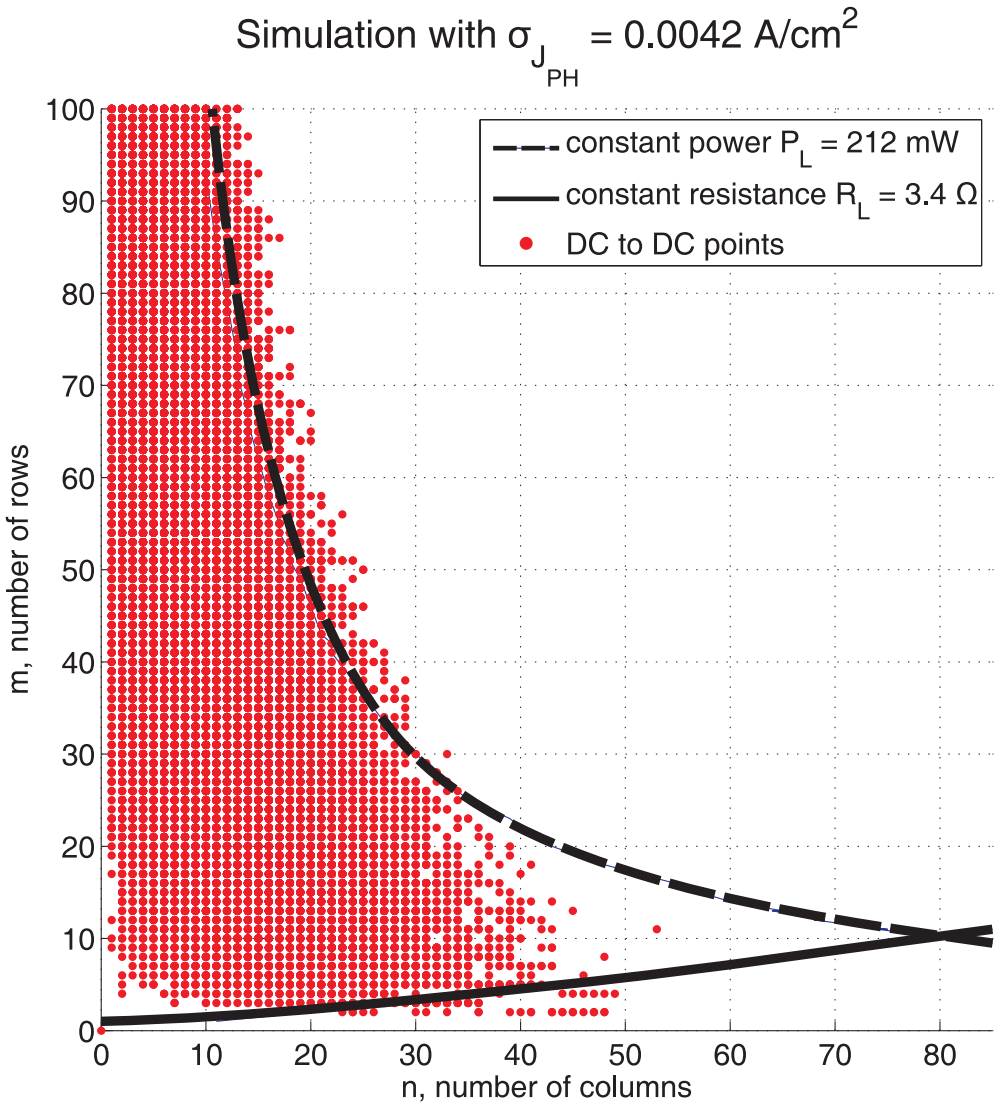


Figure 27: Minimum load resistance and maximum load power boundaries for triple the default value of photon current density standard deviation.

5.2.2 Cell Area

Figures 28 through 30 show the DC to DC points for the default, double-default, and triple-default standard deviation values of photon current density. Again, the minimum voltage requirement for the Dickson charge pump could not be met. Thus, there are no CPO points in these simulations.

The load power and load resistance boundaries for the DC to DC points region shows a similar outward progression as in the photon current density simulations. The load resistance boundary progresses from 31.3 Ω to 5.3 Ω, and the load power boundary progresses from 34.1 mW to 258.5 mW. The colored region again mostly covers the dimensions for vertical arrays, which supports the original hypothesis that large cell-current variability allows a DC to DC converter to save the use of a few solar cells.

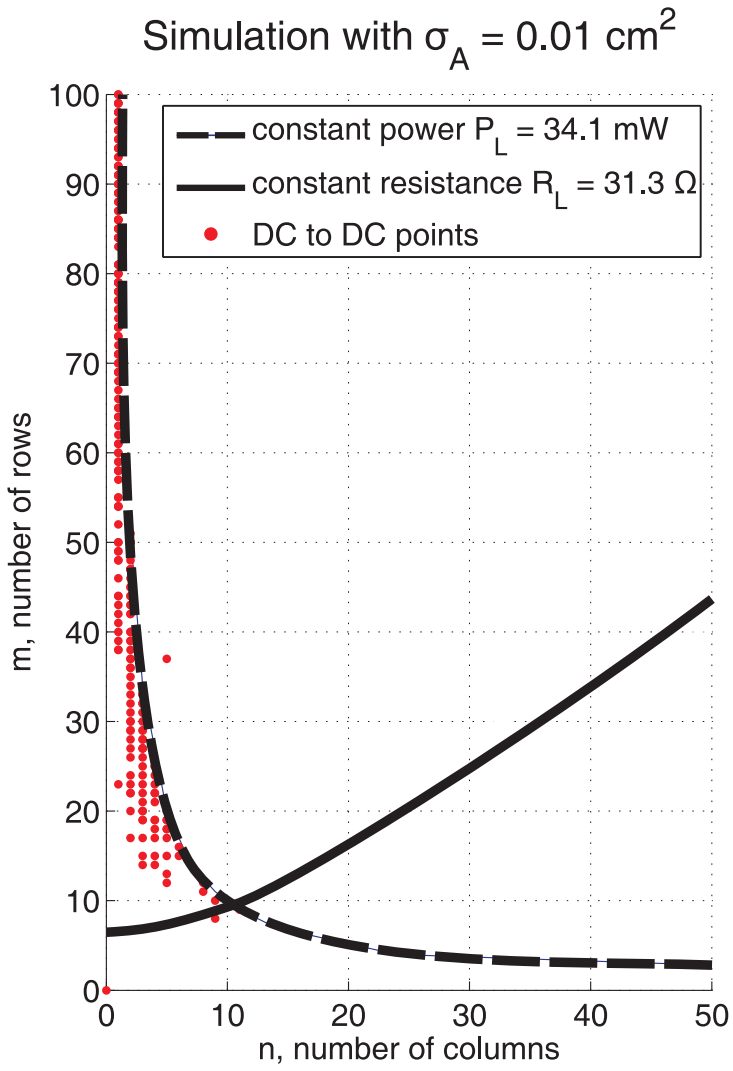


Figure 28: Minimum load resistance and maximum load power boundaries for the default value of cell area standard deviation.

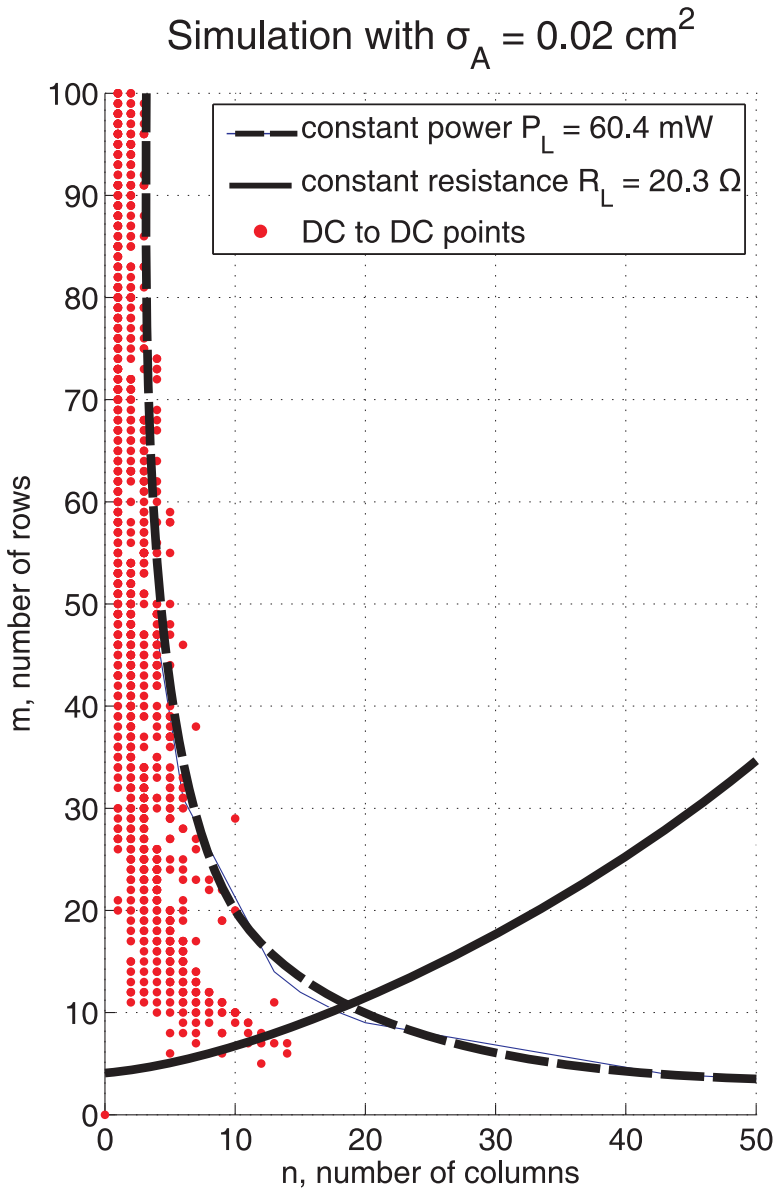


Figure 29: Minimum load resistance and maximum load power boundaries for double the default value of cell area standard deviation.

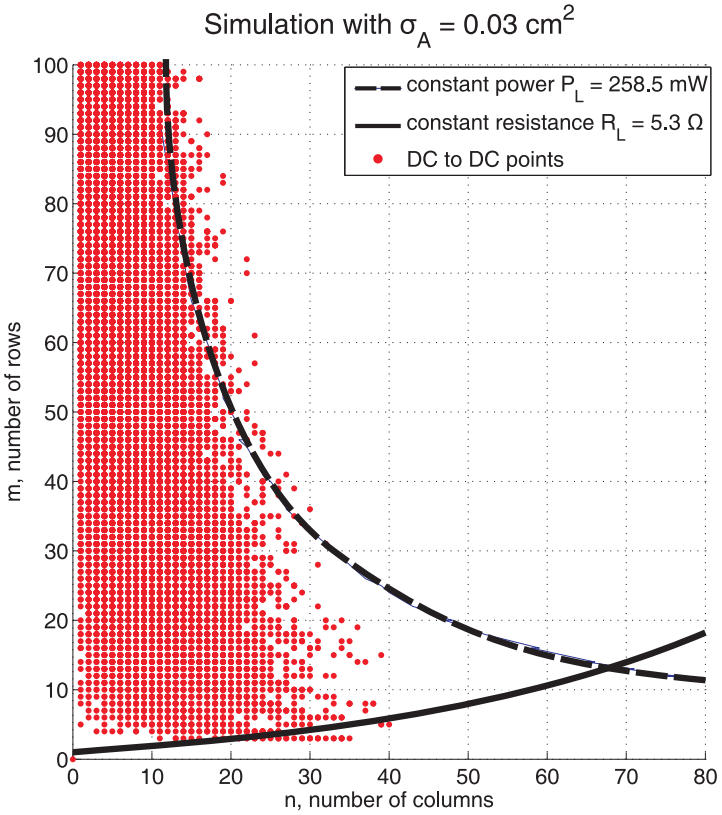
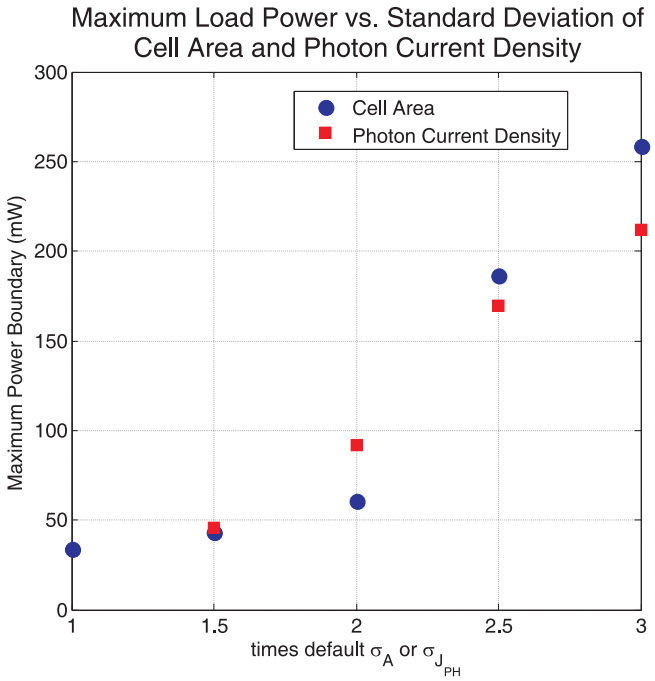


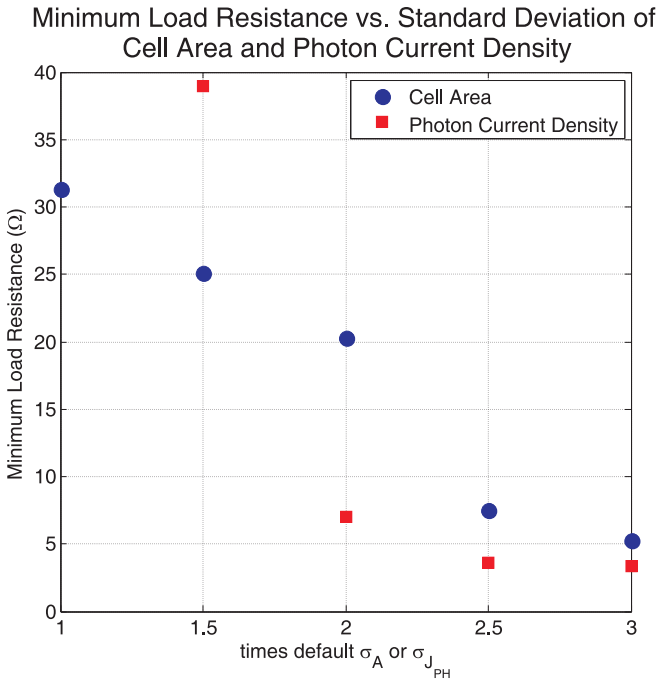
Figure 30: Minimum load resistance and maximum load power boundaries for triple the default value of cell area standard deviation.

5.3 Region of Savings vs. Current Mismatch

The results for load power and load resistance boundaries are compiled into two graphs in Figure 31. The load power and load resistance boundaries were simulated for intermediate points of photon current density standard deviation and cell area standard deviation. The trends show that the power boundary increases, and the resistance boundary decreases making the load conditions more inclusive as current variation widens. The plots basically imply that as the current mismatches within a solar cell array get larger, the load power and load resistance boundaries widen as well.



(a)



(b)

Figure 31: (a) The maximum power boundary increases with increasing $\sigma_{J_{PH}}$ and σ_A. (b) The minimum resistance boundary decreases with increasing $\sigma_{J_{PH}}$ and σ_A.

CHAPTER VI

CONCLUSIONS

The results show that the variability of the basic circuit parameters of organic solar cells presents an opportunity to use fewer solar cells to power a DC load by inserting a DC to DC converter between the solar cell array and the DC load. The range of minimum load resistance required to save a few cells is inversely proportional to the magnitude of the standard deviations of photon current density and cell area. Also, the range of maximum load power required to save a few cells is directly proportional to the standard deviations of photon current density and cell area. However, variance of circuit parameters such as series resistance, parallel resistance, diode ideality factor, and reverse saturation current density had a negligible effect on the minimum load resistance and maximum load power.

Organic solar cells based on C_{60} by Yoo et. al. [27] were used to show the values of load resistance and load power that would benefit from the use of a DC to DC converter. Most of the load resistance and load power combinations that allowed cell savings required a vertical array, and the cell-savings came from using a horizontal array with a DC to DC converter because current variability is the limiting factor in these simulations. The converse of this situation should also be true: Large voltage variability with little current variability should allow vertical arrays coupled with DC to DC converters to be more cell-saving than horizontal arrays.

Overall, the Dickson charge pump is infeasible even with low-threshold diodes ($V_t < 0.3$). The stage diode threshold voltage coupled with a large specified power efficiency presents a minimum voltage. The specified power efficiency can be reduced to reduce this minimum voltage, but then the constant P_L/η curve moves outward

from the constant P_L curve. Thus, the trade-off for low minimum input voltage is a reduced chance that a resized horizontal array will contain fewer solar cells.

6.1 Future Work

The converse of these simulations should be analyzed. Large voltage variability should produce situations where vertical arrays with DC to DC converters are favorable, but it has not yet been shown. The DC to DC converter to use in this situation is the converse of a boosting converter, which is a bucking converter. The two main circuit parameters that produce large voltages with solar cells are diode ideality factor and reverse saturation current. Increasing these parameters will increase the open-circuit voltage but decrease fill factor as well. This trade-off should be analyzed to determine whether using low-fill factor solar cells with a bucking converter is cheaper than using high-fill factor solar cells alone.

Research in inductor-less DC to DC converters of the bucking, boosting, or buck-boosting type is needed. Organic electronic circuits is a new field of research, and plenty of opportunities exist for more efficient DC to DC converters. Organic DC to DC converters probably won't surpass inorganic DC to DC converters in terms of efficiency and power handling capability, but the cost should be severely reduced for comparable converters.

APPENDIX A

DICKSON CHARGE PUMP THEORY

A.1 Input/Output Equation Derivation

The circuit's operation may be easily understood by analyzing the performance during steady-state mode. Figure 32 shows the circuit from Figure 7 operating during the two clock phases, the $T/2$ period when $\phi(t)$ is high and the $T/2$ period when $\bar{\phi}(t)$ is high. During $\bar{\phi}$, stage capacitor C_1 is being charged by the input DC source, V_{in}. A voltage loop equation will show that the expression for the voltage across C_1 is

$$V_{C_1}(t) = (V_{in} - V_{D_1}(t)) - \left[(V_{in} - V_{D_1}(t)) - V_{C_1}\left(\bar{\phi}_{begin}\right)\right] e^{\frac{-t}{R_{D1}(t)C_1}} \tag{93}$$

where $V_{D_1}(t)$ is the diode voltage, $V_{C_1}\left(\bar{\phi}_{begin}\right)$ is the voltage of capacitor C_1 at the beginning of the $\bar{\phi}$-phase, and $R_{D_1}(t)$ is the on-resistance of diode D_1. $V_{D_1}(t)$ is dependent on the diode current. For this analysis, we will assume that the current through every diode is within ranges that allow $V_{D_1}(t) \approx V_t$, where V_t is the diode threshold voltage. The term $V_{C_1}\left(\bar{\phi}_{begin}\right)$ is equal to the voltage at the end of the ϕ-phase, $V_{C_1}(\phi_{end})$. It is also true that $V_{C_1}(\phi_{begin}) = V_{C_1}\left(\bar{\phi}_{end}\right)$. These relationships hold for every capacitor in the circuit. $R_{D_1}(t)$ is found by taking the ratio of its voltage and current.

$$R_{D_1}(t) = \frac{V_{D_1}(t)}{I_{D_1}(t)} \approx \frac{V_t}{I_{D_1}(t)} \tag{94}$$

This is the same as the reciprocal of the slope to the diode's IV curve. $R_{D_1}(t)$ changes with current according to the diode equation. During the $\bar{\phi}$-phase, $I_{D_1}(t)$ is decreasing exponentially as shown in Figure 33, and $V_{D_1}(t)$ decreases exponentially with the same time constant but much more slowly. It stays approximately equal to the threshold voltage of the diode. This implies $R_{D_1}(t)$ is increasing almost linearly.

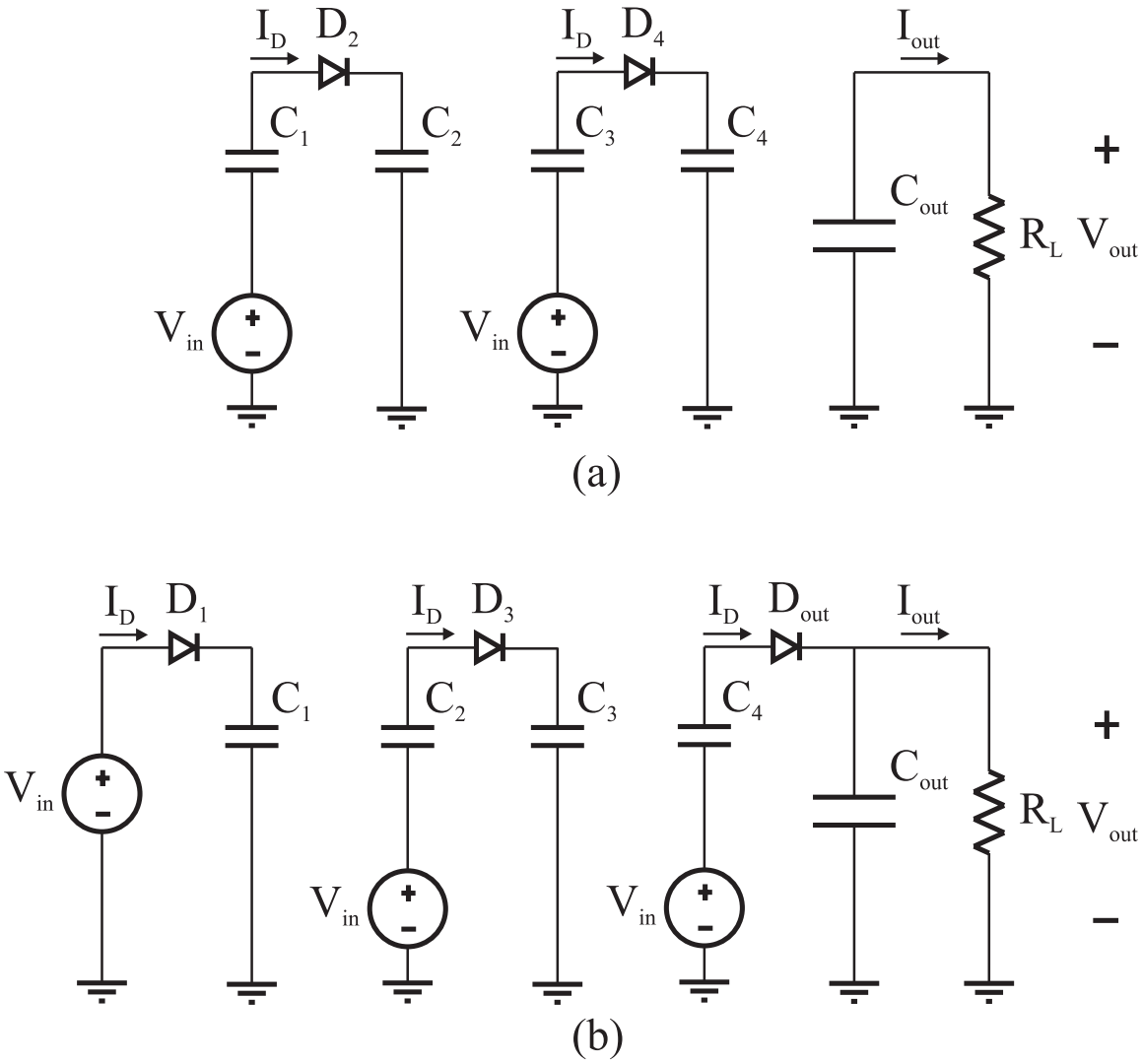


Figure 32: 4-Stage Dickson charge pump operating during (a) ϕ-phase and (b) $\bar{\phi}$-phase.

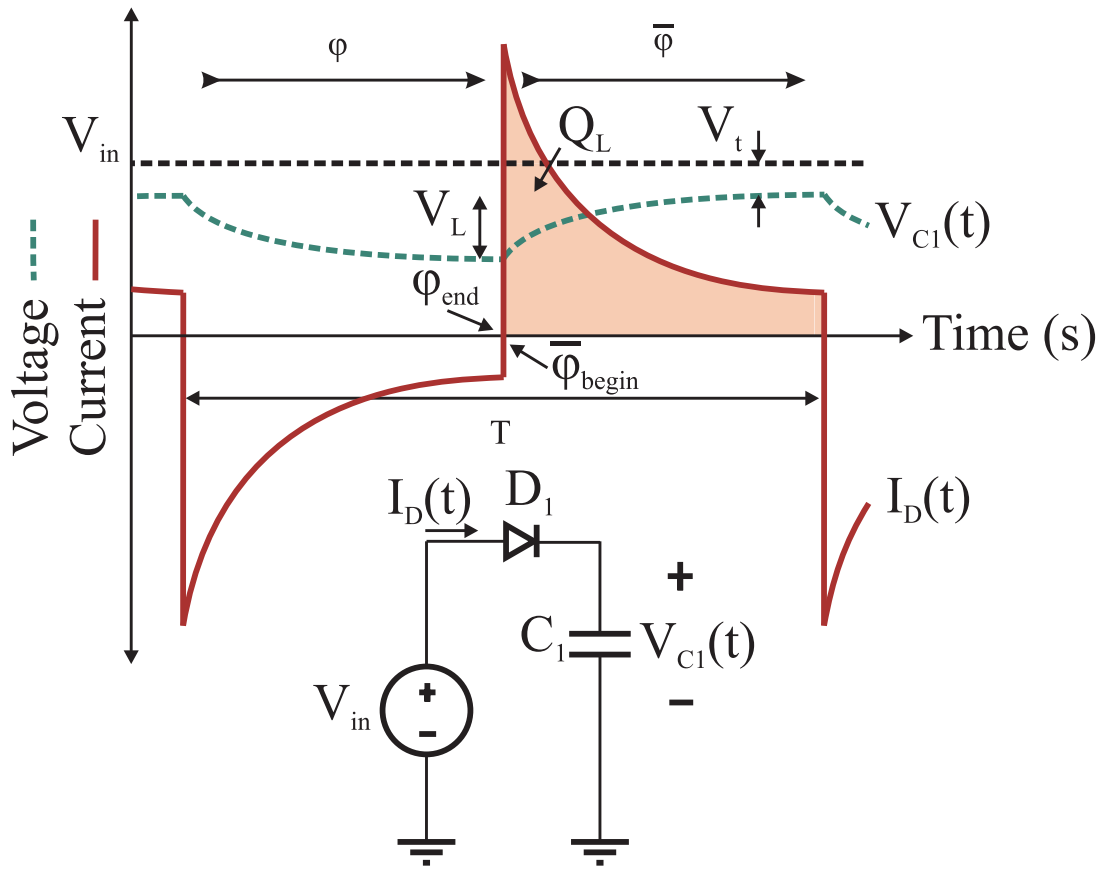


Figure 33: C_1 voltage and current and D_1 in steady-state.

When the $\bar{\phi}$-phase is just beginning, the capacitor draws a large amount of current, which makes the on-resistance very low. By the end of the $\bar{\phi}$-phase, most of the charge has been transferred to the capacitor, and the current drops to a low value, which makes the on-resistance high. Most silicon diodes have on-resistances in the range of 1 and 1000 $m\Omega$ [18]. This dynamic resistance behavior is shown in Figure 33.

We will assume that the clock period is long enough to allow the approximation

$$V_{C_1}\left(\bar{\phi}_{end}\right) \approx V_{C_1}(t \to \infty) = V_{in} - V_t \tag{95}$$

At the beginning of the next clock phase (shown in Figure 32a), the capacitor voltage should be continuous so that $V_{C_1}(\phi_{begin}) = V_{C_1}(\bar{\phi}_{end})$. The voltage presented to C_2 is the sum of V_{in}, $V_{C_1}(\phi_{begin})$ and $-V_t$. At this point, V_{C_2} is less than the sum of

these voltages, which means it begins to draw current (I_D in Figure 32a) from the input source. C_1 loses charge as I_D flows into C_2 and away from C_1, which means V_{C_1} decreases and V_{C_2} increases. The amount of charge lost from C_1 and gained by C_2 is

$$Q_L = \int_{\phi_{begin}}^{\phi_{end}} I_D(t)dt = C_1 V_L \tag{96}$$

where V_L is the voltage lost (or transferred) from C_1 to C_2 and the charge-voltage relationship $Q = CV$ was used. The integral equation is simply the area under the $I_D(t)$ curve in Figure 33. At the end of the ϕ-phase, V_{C_1} has decreased to

$$V_{C_1}(\phi_{end}) = V_{C_1}(\phi_{begin}) - V_L = V_{in} - V_t - V_L \tag{97}$$

as shown in Figure 33. And since C_2 can only charge up to the voltage to which it is excited, its end-of-stage value is given by

$$V_{C_2}(\phi_{end}) = V_{in} + V_{C_1}(\phi_{end}) - V_t = 2(V_{in} - V_t) - V_L \tag{98}$$

The process of analysis gets repetitive after this point. For the next phase, the capacitor voltage is continuous so that $\bar{\phi}$, $V_{C_2}(\bar{\phi}_{begin}) = V_{C_2}(\phi_{end})$. The circuit is in steady-state, so the charge gained by C_2, which is Q_L, during the ϕ-phase must be lost during the $\bar{\phi}$-phase. So, the same current I_D flows away from C_2 and into C_3, taking Q_L away from C_2 and into C_3. At the end of the $\bar{\phi}$-phase, V_{C_2} has dropped to

$$V_{C_2}(\bar{\phi}_{end}) = V_{C_2}(\bar{\phi}_{begin}) - V_L = 2(V_{in} - V_t) - 2V_L \tag{99}$$

And since C_3 can only charge up to the voltage to which it is excited, its end-of-stage value is given by

$$V_{C_3}(\bar{\phi}_{end}) = V_{in} + V_{C_2}(\phi_{end}) - V_t = 3(V_{in} - V_t) - 2V_L \tag{100}$$

The same process can be carried out for the k^{th} stage, and in general the voltage across the k^{th} stage capacitor, C_k, after ϕ (for even k) or $\bar{\phi}$ (for odd k) is

$$V_{C_k}(\phi_{end} \text{ or } \bar{\phi}_{end}) = V_{in} + V_{C_{k-1}}(\phi_{end} \text{ or } \bar{\phi}_{end}) - V_t = k(V_{in} - V_t) - (k-1)V_L \tag{101}$$

This equations shows how the voltage across the stage capacitors increases with the number of stages. The 4^{th} stage capacitor will have approximately four times the voltage of the 1^{st} stage capacitor. The designer should choose capacitors that can withstand this maximum voltage. This characteristic of the Dickson charge pump makes it difficult to design for extremely high voltages such as 800 kV as in the Cockcroft-Walton voltage multiplier.

The output capacitor in Figure 32 is charged during the $\bar{\phi}$-phase in the same way that the other stage capacitors are charged. The final equation for V_{out} can be found if C_{out} is viewed as a 5^{th} stage capacitor.

$$V_{out} = V_{C_5}(\bar{\phi}_{end}) = V_{in} + V_{C_4}(\bar{\phi}_{end}) - V_t = 5(V_{in} - V_t) - 4V_L \tag{102}$$

This expression provides V_{out}, but the V_L term is still present, which will depend on the load resistance.

The output current can be found by analyzing charge transfer. Capacitor C_4 loses charge Q_L, which is gained by C_{out}. The charge gained by C_{out} during $\bar{\phi}$ will be discharged into the resistor during $\bar{\phi}$ and ϕ because the resistor is always drawing current regardless of the clocks' phase. Since the circuit is operating in steady-state, the charge gained by C_{out} must be discharged before the next clock cycle. This implies that Q_L *Coulombs* is discharged by the load resistor during T *seconds*. This gives an expression for output current:

$$I_{out} = \frac{Q_L}{T} \tag{103}$$

By substituting equations (6) and (96), I_{out} can be expressed as

$$I_{out} = fC_1V_L \tag{104}$$

Now, equation (102) can be improved by using equation (104) to substitute for V_L in equation (102), which becomes

$$V_{out} = 5(V_{in} - V_t) - 4\frac{I_{out}}{fC_1} \tag{105}$$

This is the common output equation given for a 4-stage Dickson charge pump [7] [29], but it is not in proper form because of the I_{out} term that appears on the right hand side. If I_{out} is replaced with V_{out}/R_L and C_1 replaced with a common stage capacitance, C, then equation (105) becomes

$$V_{out} = 5(V_{in} - V_t) - 4\frac{V_{out}}{fCR_L} \tag{106}$$

Then, V_{out} can be solved as

$$V_{out} = \frac{5(V_{in} - V_t)}{1 + \frac{4}{fCR_L}} \tag{107}$$

This form of the equation is more proper and simpler than equation (105).

For a general N-stage Dickson charge pump with clock voltage $V_\phi = V_{\bar{\phi}} = V_{in}$, the output equation is

$$V_{out} = \frac{(N+1)(V_{in} - V_t)}{1 + \frac{N}{fCR_L}} \tag{108}$$

This equation describes how the output behaves when design parameters are changed. This form of the output equation will be used in the research.

A.2 Power Efficiency Derivation

Power efficiency is defined as the ratio of output power to input power:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} \tag{109}$$

Efficiency η is found by substituting expressions for V_{out}, I_{out}, V_{in}, and I_{in}.

The output voltage equation was derived in Section 2.1, equation (108). The output current equation was derived in Section 2.1, equation (104), and was found to be

$$I_{out} = \frac{Q_L}{T} = fCV_L = fC_{out}\Delta V_{out} \tag{110}$$

which has units *Coulombs/Second* or *Amperes* as expected.

Figure 32 is helpful in explaining the derivation of steady-state input current to the charge pump. Figure 33 shows the DC input source five times: once as the DC

input, and four times as a replacement for the clock sources. The input source supplies current I_D five times during once complete clock cycle. And since Q_L is defined by

$$Q_L = \int_{\phi_{begin}}^{\phi_{end}} I_D(t)dt \tag{111}$$

it must be true that the total charge supplied by the input source during one complete clock cycle is

$$Q_{in} = \int_{\phi_{begin}}^{\phi_{end}} 5I_D(t)dt = 5\int_{\phi_{begin}}^{\phi_{end}} I_D(t)dt = 5Q_L \tag{112}$$

Equations (111) and (112) were derived for a four-stage Dickson charge pump, so it makes sense that for an N-stage Dickson charge pump, the charge injected by the input source is

$$Q_{in} = (N+1)Q_L \tag{113}$$

Input current I_{in} can be found using (113) and (110) as

$$I_{in} = \frac{Q_{in}}{T} = (N+1)\frac{Q_L}{T} = (N+1)I_{out} \tag{114}$$

Now, V_{out}, I_{out}, and I_{in} are all clearly expressed in terms of Dickson charge pump circuit parameters. Equation (108) is augmented to formulate the power efficiency, η:

$$\frac{V_{out}}{V_{in}} = \frac{(N+1)(1-\frac{V_t}{V_{in}})}{1+\frac{N}{fCR_L}} \tag{115}$$

Now, multiplying (115) by I_{out}/I_{in} gives power efficiency as

$$\eta = \frac{V_{out}}{V_{in}}\frac{I_{out}}{I_{in}} = \frac{V_{out}}{V_{in}}\frac{I_{out}}{(N+1)I_{out}} = \frac{V_{out}}{V_{in}}\frac{1}{(N+1)} = \frac{(1-\frac{V_t}{V_{in}})}{1+\frac{N}{fCR_L}} \tag{116}$$

These two forms of the efficiency equation are useful at different stages of the design process. If the efficiency is specified, then equation (115) is used to find the input voltage. Then, equation (116) is used to find other circuit components like frequency, stage capacitance, or diode threshold voltage.

A.3 Output Voltage Ripple Derivation

The output capacitor usually has different capacitance than the stage capacitors because it directly influences the magnitude of the output ripple voltage, ΔV_{out}, whereas the stage capacitors directly influence V_{out}. Stage capacitance does affect ripple voltage indirectly. It is primarily chosen control output voltage. C_{out} is commonly designed to be large in order to reduce output ripple voltage. The difference in capacitor size affects the voltage gained by C_{out} during charge transfer. The relationship between ΔV_{out} and V_L is found by equating charge lost by the last stage capacitor with capacitance C and charge gained by C_{out}.

$$Q_L = CV_L = C_{out}\Delta V_{out} \tag{117}$$

$$\Rightarrow \Delta V_{out} = \frac{C}{C_{out}} V_L \tag{118}$$

The ratio of capacitor size is an important design parameter because it affects the size of the output ripple voltage. The ratio of output capacitance to stage capacitance is called β, and is defined as

$$\beta = \frac{C_{out}}{C} \tag{119}$$

Also, *percent ripple voltage*, or $\Delta V_{out}/V_{out}$ is a common specification for the output of a DC to DC converter. The percent ripple voltage is called α, and is defined as

$$\alpha = \frac{\Delta V_{out}}{V_{out}} \tag{120}$$

Equation (118) can be modified using equations (110), (119), and (120) to get a relationship between the ripple voltage specification, α, and the ratio of capacitance, β. First, equation (118) is rearranged to be

$$\frac{C_{out}}{C} = \frac{V_L}{\Delta V_{out}} \tag{121}$$

Then, a substitution for V_L is made, resulting in

$$\frac{C_{out}}{C} = \frac{I_{out}}{fC\Delta V_{out}} \tag{122}$$

Then, using Ohm's Law to replace I_{out}, (122) becomes

$$\frac{C_{out}}{C} = \frac{V_{out}}{R_L f C \Delta V_{out}} \tag{123}$$

Finally, the substitutions for β and α are made resulting in

$$\beta = \frac{1}{R_L f C \alpha} \tag{124}$$

Then, the expression for output voltage ripple is

$$\alpha = \frac{\Delta V_{out}}{V_{out}} = \frac{1}{R_L f C_{out}} \tag{125}$$

APPENDIX B

SOLAR CELL THEORY

This accurate method of finding short-circuit current and open-circuit voltage takes into account the series and parallel resistances. The final equations are more complex but also more accurate. These methods are used in the simulation for more credible results.

B.1 Accurately Finding Short-Circuit Current

The short circuit current can be found by setting $V = 0$ in the I-V equation, which becomes

$$I_{SC} = I_{PH} - I_S \left(e^{\frac{qI_{SC}R_S}{nkT}} - 1 \right) - I_{SC}\frac{R_S}{R_P} \tag{126}$$

The equation can be simplified by combining like terms and moving everything to the right hand side:

$$0 = I_{PH} - I_S \left(e^{\frac{qI_{SC}R_S}{nkT}} - 1 \right) - I_{SC} \left(\frac{R_S}{R_P} + 1 \right) \tag{127}$$

The next step is to remove the variable I_{SC} out of the exponential so the equation can be simplified. We can do this by using the infinite series representation of the exponential:

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots \tag{128}$$

In this expansion, let

$$x = \frac{qR_S}{nkT} I_{SC} = \beta_i I_{SC} \tag{129}$$

Using this substitution and the exponential series, equation (127) becomes

$$0 = I_{PH} - I_S \left(1 + \beta_i I_{SC} + \frac{(\beta_i I_{SC})^2}{2!} + \frac{(\beta_i I_{SC})^3}{3!} + \ldots - 1 \right) - I_{SC} \left(\frac{R_S}{R_P} + 1 \right) \tag{130}$$

The pair of ones within the parenthesis on the right hand side cancel each other. Then, rearranging the right hand side of this equation in terms of powers of I_{SC}, we get

$$0 = I_{PH} - \left(I_S\beta_i + \frac{R_S}{R_P} + 1\right) I_{SC} - \left(I_S\frac{\beta_i^2}{2!}\right) I_{SC}^2 - \left(I_S\frac{\beta_i^3}{3!}\right) I_{SC}^3 - \dots \tag{131}$$

Then, multiplying by -1, and dividing by I_S puts this equation in a standard polynomial form:

$$0 = -\frac{I_{PH}}{I_S} + \left(\beta_i + \frac{R_S}{I_S R_P} + \frac{1}{I_S}\right) I_{SC} + \frac{\beta_i^2}{2!} I_{SC}^2 + \frac{\beta_i^3}{3!} I_{SC}^3 + \cdots \tag{132}$$

With the equation in this form, I_{SC} can be approximated by truncating the infinite-degree polynomial to a large-, but finite-degree polynomial. Then, a computer program such as MATLAB could solve for I_{SC}. From this equation, we can see that I_{SC} is dependent on I_S, I_{PH}, and β, which is dependent on R_S, n and temperature, T (in Kelvin). I_{SC} is also slightly dependent on R_P. This makes sense because when the terminals of the cell are shorted, I_{SC} passes through R_S, which creates a voltage across R_P. This typically small voltage forces a current through R_P, which takes away from the short circuit current. This small voltage is also placed across the diode, and the diode draws some small current.

B.2 Accurately Finding Open-Circuit Voltage

A similar method is used to find the open circuit voltage. The first step is setting I = 0 in the I-V equation, which becomes

$$0 = I_{PH} - I_S\left(e^{\frac{qV_{OC}}{nkT}} - 1\right) - \frac{V_{OC}}{R_P} \tag{133}$$

Then, we use the exponential expansion from equation (128) and the substitution

$$x = \frac{q}{nkT} V_{OC} = \beta_v V_{OC} \tag{134}$$

With this substitution, equation (133) becomes

$$0 = I_{PH} - I_S\left(1 + \beta_v V_{OC} + \frac{(\beta_v V_{OC})^2}{2!} + \frac{(\beta_v V_{OC})^3}{3!} + \dots - 1\right) - \frac{V_{OC}}{R_P} \tag{135}$$

The pair of ones within the parenthesis cancel, and this equation can be rearranged in terms of powers of V_{OC}:

$$0 = I_{PH} - \left(I_S\beta_v + \frac{1}{R_P}\right)V_{OC} - \left(I_S\frac{\beta_v^2}{2!}\right)V_{OC}^2 - \left(I_S\frac{\beta_v^3}{3!}\right)V_{OC}^3 - \dots \tag{136}$$

Then, multiplying by -1 and dividing by I_S gives a simpler form of the polynomial

$$0 = -\frac{I_{PH}}{I_S} + \left(\beta_v + \frac{1}{I_S R_P}\right)V_{OC} + \frac{\beta_v^2}{2!}V_{OC}^2 + \frac{\beta_v^3}{3!}V_{OC}^3 + \dots \tag{137}$$

V_{OC} can be approximated by truncating this infinite-degree polynomial to a large, but finite-degree polynomial just like in the method for solving for I_{SC}. Then, a computer program like MATLAB can solve the equation quickly. From this equation, we can see that V_{OC} is dependent on I_{PH}, I_S, and β_v, which is dependent on ideality factor, n, and temperature, T. V_{OC} is only slightly dependent on R_P.

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