SIGNAL AND POWER INTEGRITY CO-SIMULATION USING THE MULTI-LAYER FINITE DIFFERENCE METHOD

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SIGNAL AND POWER INTEGRITY CO-SIMULATION USING THE MULTI-LAYER FINITE DIFFERENCE METHOD

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To my family.

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SUMMARY

Mixed signal system-on-package (SoP) technology is a key enabler for increasing functional integration, especially in mobile and wireless systems. SoP allows the integration of high speed digital, RF and passive components at a package level, thereby preserving performance at a lower cost compared to system-on-chip based solutions. Due to the presence of multiple dissimilar modules, each having unique power supply requirements, the design of the power distribution network (PDN) becomes critical.

Typically, this PDN is designed as alternating layers of power and ground planes with signal interconnects routed in between or on top of the planes. This arrangement serves two purposes - firstly, it allows a reduction in the package inductance, and secondly, signal lines on separate layers are isolated from each other due to the shielding effect of the planes.

In the case of a SoP module, to provide DC isolation between power supplies, the power and ground planes may be segmented into islands. In this case, electromagnetic (EM) coupling becomes a critical factor. Consider the SoP containing four modules shown in Figure 1. The digital module is the source of the simultaneous switching noise (SSN) containing harmonics at multiples of the clock frequency. For the case of a cell phone receiver, even relatively low levels of insertion loss between the digital and RF modules can significantly degrade the performance of the front-end low-noise amplifier. Also, decreasing supply voltages coupled with increasing power requirements tends to place stringent requirements on the target impedance [3] of the digital IC. Time-efficient and accurate signal and power integrity (SI/PI) simulation is therefore a critical component of the SoP design flow.

The goal for the simulation of multi-layer power/ground planes, is the following: Given a stack-up and other geometrical information, it is required to find the network parameters (S/Y/Z) between port locations. For simple structures, it is possible to
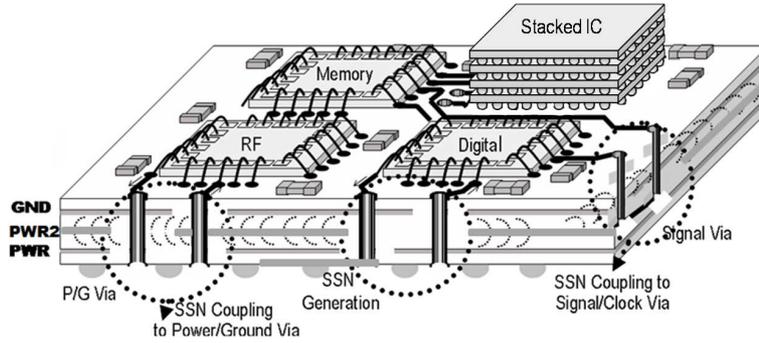
Figure 1. A System on Package Module (courtesy [2]).

use existing commercially available methods (full-wave EM solvers) to obtain the response of the PDN. However, commercial packages have extremely complicated stack-ups, and the trend to increasing integration at the package level only points to increasing complexity. It is computationally intractable to solve these problems using these existing methods.

The approach proposed in this thesis for obtaining the response of the PDN is the multi-layer finite difference method (M-FDM). A surface mesh / finite difference based approach is developed, which leads to a system matrix that is sparse and banded, and can be solved efficiently. The approach relies on approximating the electric field distribution in power/ground planes. Certain geometrical features may invalidate these approximations, which may lead to significant inaccuracy in simulation results. Thus, methods to update the system matrix to restore accuracy to M-FDM, while not adding significant computational overhead, have been considered. These methods are called the fringe augmentation (FA) and plane gap augmentation (PGA) methods.

While discussing the simulation of multi-layer packages, it is not possible to isolate the PDN from the signal traces routed between them. With increasing frequency, these signal traces behave as transmission lines, and hence, their distributed properties such as delay and phase become important. Also, signal traces use the PDN as their reference planes, and hence their characteristics cannot be decoupled from the PDN. Discontinuities in the PDN can manifest as signal integrity problems such as

reduction in eye height or increased jitter.

Finally, an application of M-FDM for the optimization of a PDN design using Genetic Algorithms (GA) is considered. From a design perspective, the requirement on the PDN is that it should represent a low impedance at all frequencies at which current transients exist. Traditionally, the solution to providing a low impedance power supply as seen by the device has been to place decoupling capacitors (decaps) across the power supply pins [4].

The impedance profile of the PDN can be optimized by carefully choosing the values and placement locations of the decaps. This is critical since the anti-resonances (or parallel-resonances) that occur between decaps and between the decap and the PDN can lead to an impedance maximum. If this impedance maximum occurs at a frequency at which current transients exist, the severity of the SSN can be exacerbated. This choice and placement of decoupling capacitors can be accomplished using an optimization engine based on a genetic algorithm (GA).

To summarize, the contributions of this research are the following:

1. The development of a PDN modeler for multi-layer packages and boards called the the multi-layer finite difference method.

2. The enhancement of M-FDM using multi-port connection networks to include the effect of fringe fields and gap coupling.

3. An adaptive triangular mesh based scheme called the multi-layer finite element method (MFEM) to address the limitations of M-FDM

4. The use of modal decomposition for the co-simulation of signal nets with the PDN.

5. The use of a robust GA-based optimizer for the selection and placement of decoupling capacitors in multi-layer geometries.

6. The implementation of these methods in a tool called MSDT 1.

CHAPTER 1

THEORETICAL BACKGROUND AND SUMMARY OF CONTRIBUTIONS

1.1   Electrical Bottlenecks in Microelectronic Packaging

An electronic package or board module is an electromechanical platform which has traditionally provided the following functions for an integrated circuit (IC)[5]:

1. Mechanical support and protection

2. Thermal dissipation

3. Geometric translations

4. Interfaces to the next level package

5. Electrical connectivity

However, modern packages are moving beyond these traditional roles. In a complex multi-functional device, system level integration occurs in stages, where the I/O pads of ICs are connected to individual packages or to multi-chip modules (MCM). This is the first level package, a few of which are integrated together onto daughter cards or printed wiring boards (PWB). These daughter cards may then be connected to backplanes, as shown in Figure 2.

While the reduction of size and corresponding increases in power and operating frequency have been key drivers for ICs, a corresponding scaling on package has not occurred, leading to the package being a significant electrical bottleneck in terms of supporting high frequency signalling. The solution to this problem has been to progressively integrate more functionality at lower levels of packaging. This has resulted in system integration strategies such as the system on package (SoP) approach, where multiple dissimilar components are integrated together.
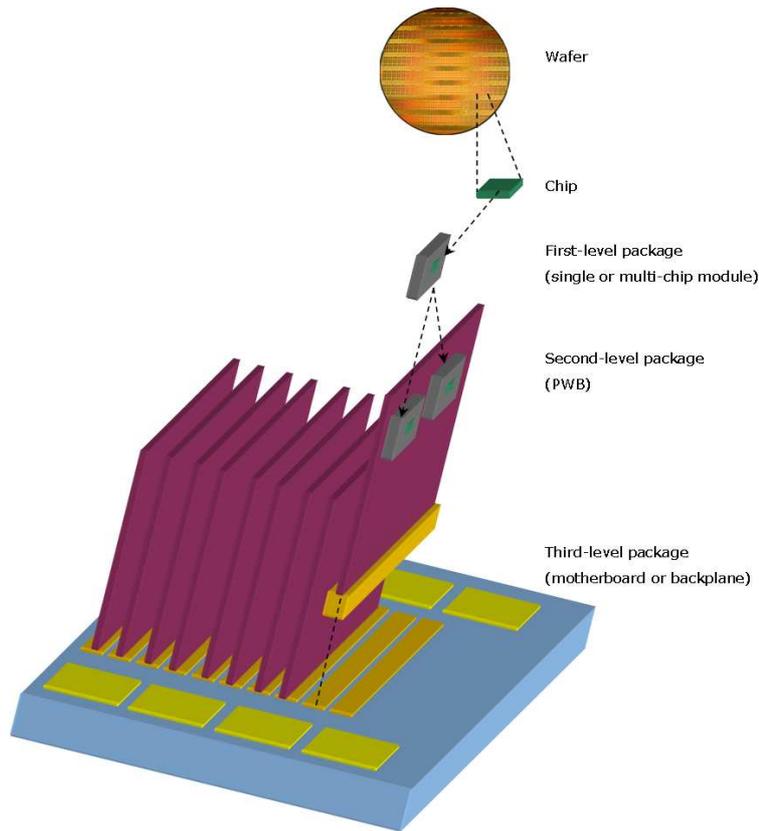
Figure 2. Package hierarchy.

Mixed signal SoP technology is a key enabler for increasing functional integration, especially in mobile and wireless systems. SoP allows the integration of high speed digital, RF and passive components in the first-level package, thereby preserving performance at a lower cost compared to system-on-chip based solutions. A conceptual SoP test bed is shown in Figure 3[2]. This illustration depicts the integration of different kinds of circuits on package. These circuits include embedded RF thin-film components such as resistors, inductors and antennas. To support high performance digital components, SoP also supports digital thin-film components such as embedded capacitors. Also, shown are optical waveguides with laser diodes for signaling, other packaged and bare modules, and a MEMS device.

While conceptually this integration scheme shows incredible promise in revolutionizing the electronics industry, there are still several challenges to be faced. One
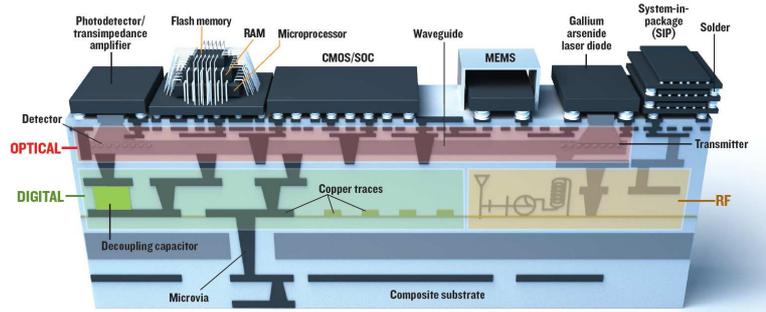
Figure 3. Schematic of a system on package (courtesy [2]).

of the key reasons for the success of past efforts in system integration (for example, the system-on-chip), is because of key advances in design automation technology [6]. Novel technology advances require support for the designer, and in this regard, Computer-aided-design (CAD) for SoP is still emerging.

The contributions of this work are aimed primarily at improving the state-of-the-art in design tools for conventional packages and boards, while also addressing some of the new challenges posed by SoP. The problem being considered is the design of the power distribution network (PDN). The challenge posed by SoP is primarily due to the integration of multiple dissimilar modules, each having unique power supply requirements. In traditional packaging, each of these dissimilar modules have power supplies that are relatively isolated from each other. This isolation is essential, because some modules are *noisy* (such as high-speed digital), while others are extremely sensitive to noise (such as RF-circuits). In this context, the noise is because of simultaneous switching of multiple circuits, a characteristic of synchronous digital circuits. The magnitude and impact of this noise is dependant on the design of the power supply, which in turn depends on accurate and efficient design tools capable of analyzing the complex and large problems posed by next generation package PDNs.

Typically, this PDN is designed as alternating layers of power and ground planes with signal interconnects routed in between or on top of the planes. This arrangement serves two purposes - firstly, it allows a reduction in the package inductance,

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and secondly, signal lines on separate layers are isolated from each other due to the shielding effect of the planes. The former, i.e., reduction in package inductance, is one of the design guidelines for the reduction of simultaneous switch noise (SSN).

1.2   Motivation: Increasing Efficiency of the Design Flow

A typical approach that is used in the industry for the design of printed circuit boards (PCBs) and packages is shown in Figure 4. This approach is called the partial-simulation approach to PCB/package design and involves making modifications to an original design layout based on rigorous simulations and analysis. In this approach a design engineer develops an initial layout of a system based on the design specifications of the product and the design rules of the fabrication process. The signal distribution network (SDN) and the PDN, which are a part of this layout are then analyzed using rigorous post-layout simulations. The simulation and analysis of the SDN, termed as signal integrity (SI), is typically carried out in the time domain and involves analyzing voltage drops on interconnects, conductor and substrate losses, reflections on electrically long interconnects, impedance mismatches, and transmission line discontinuities like vias and bends. On the other hand, the simulation and analysis of the PDN, termed as power integrity (PI), is performed in the frequency domain and primarily involves analyzing power/ground planes, decoupling capacitors, and simultaneous switching noise (SSN). The original layout is modified based on these SI and PI analyses to account for any design flaws. This process is often iterated through multiple times untill the SI and PI analysis are satisfactory. The layout is then sent for fabrication. The physical prototype obtained from fabrication is measured and analyzed in a laboratory. Design flaws arising due to parasitic effects that could not be captured in the simulation phase are accounted for here by performing the necessary layout modifications. This modified layout is then re-fabricated and re-measured till a working prototype of the required system is obtained.
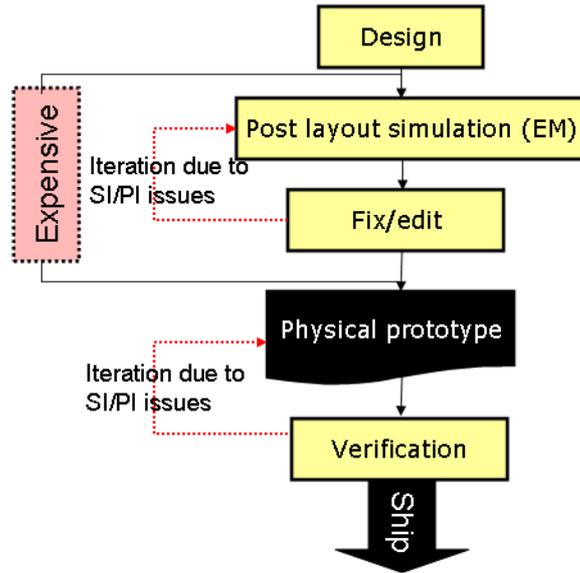
Figure 4. Current design flow.

The bottleneck of the above flow is the need to iteratively perform time expensive EM simulations for post-layout verification. Major design flaws, when detected post-layout, are costly and can cause significant delays.

The simulation method proposed in this research is called the multi-layer finite difference method (M-FDM).

The proposed design flow (Figure 5) adds an additional step, based on the computational efficiency of M-FDM. Since simulations with M-FDM, as will be shown, are relatively inexpensive, an iterated verification and re-design can be performed at the pre-layout stage. Catching major design flaws at this step can significantly reduce budget overruns. These simulations are used to guide the final layout process, which as before is validated using full-wave EM simulations, or M-FDM. This process leads to minimizing the number of EM iterations, reducing cost and time to market.

1.3 Simultaneous Switching Noise

The elaborate design of the PDN is required to provide a clean and stable power supply to the switching elements on-chip. These switching elements are primarily
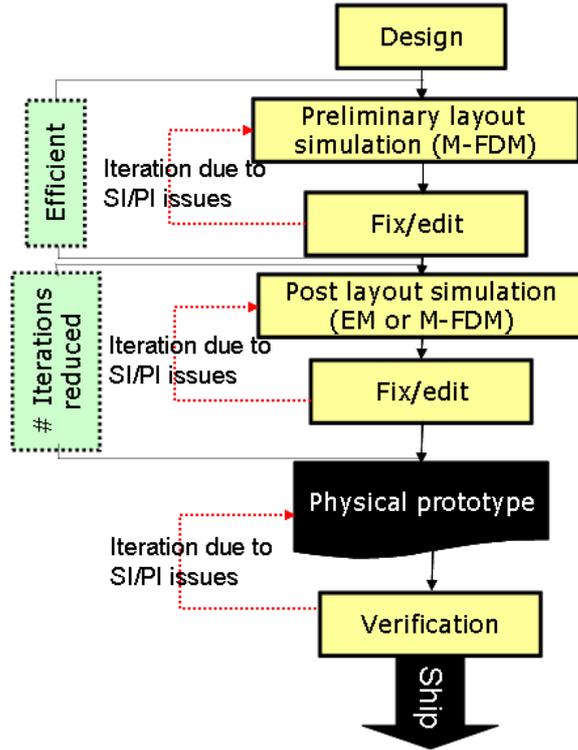
Figure 5. Efficient design flow.

CMOS drivers and other logic gates. Typical digital computers are synchronous circuits, with their various components synchronized by a clock. At each clock cycle, depending on the process being carried out, a significant portion of the circuits on-chip can switch, leading to simultaneous switching noise (SSN).

SSN is created as a consequence of Faraday's law, which can be stated as:

$$e = -L\frac{\mathrm{d}I}{\mathrm{d}t} \tag{1}$$

where e is the electromotive force, or the potential drop across an inductor, L, subjected to a time-varying current. In digital systems, this inductance is the effective inductance between the device ground (or power supply) and the system ground (or power supply). The direction of this induced electromotive force is determined by Lenz's law. The system ground is usually located on a voltage regulator module (VRM), off-chip, and the switching current required by the switching transistors on-chip follows a loop through the board and the package, which essentially constitutes

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this inductance.

In a digital device, there are usually two kinds of circuits that need to be powered, the core and the I/O circuits. The core circuits are entirely contained on an IC, while the I/O circuits allow communication between multiple ICs (for example, memory and CPU), which requires that the signal traces exit the chip, and traverse the package and board.

For a single core circuit, the maximum voltage dropped across the inductor can be shown[1] to be

$$\Delta v \approx \frac{L_c \times V_{dd}}{R t_r} \tag{2}$$

where t_r is the rise time of the switching signal, and R is the interconnection resistance, and L_c is the loop inductance associated with the core I/O circuits.

Since I/O circuits drive off-chip interconnections, which are typically much longer, these behave as transmission lines. Hence, the expression for the maximum voltage dropped across a I/O circuit is[1]:

$$\Delta v \approx \frac{L_{I/O} \times V_{dd}}{Z_0 t_r} \tag{3}$$

where Z_0 is the characteristic impedance of the transmission line and $L_{I/O}$ is the loop inductance of the I/O circuits.

1.3.1 SSN and Signal Integrity

Simultaneous switching noise causes transients on the DC power supply, as seen by the drivers. To see the effect of these transients on signaling, consider the voltage at the input end of a transmission line for a pulse with a rise time t_r, given by

$$v(t) = \begin{cases} \frac{Z_o V_{dd}}{L t_r} \left(\frac{L^2}{Z_0^2} \left[e^{\frac{-t}{(L/Z_0)}} - 1 \right] + \frac{L}{Z_0} t \right) & \text{for } t \leq t_r \\ A + B \left(1 - e^{\frac{-t}{L/Z_0}} \right) & \text{for } t > t_r \end{cases} \tag{4}$$

where

$$A = V_{dd} - [V_{dd} - v(t_r)] e^{\frac{t_r}{L/Z_0}} \quad B = [V_{dd} - v(t_r)] e^{\frac{t_r}{L/Z_0}} \tag{5}$$
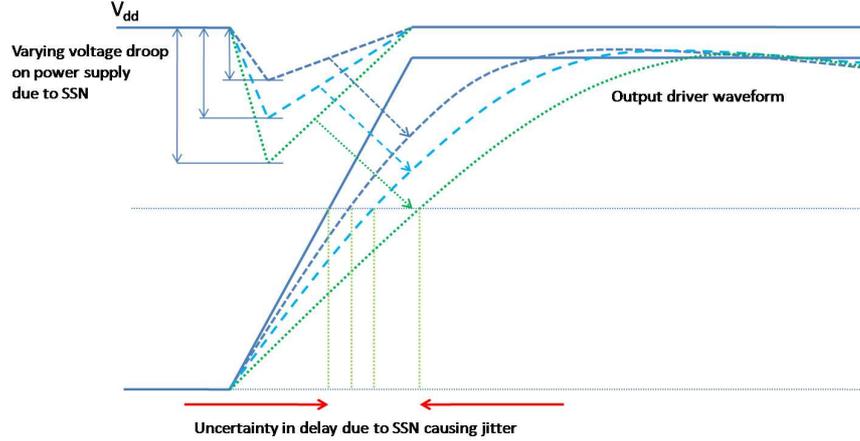
Figure 6. SSN induced jitter (courtesy [1]).

Clearly, transients on the power supply rail can lead to uncertainty in the rise time of the input pulse, causing jitter.

Figure 6, reproduced with modifications from [1], illustrates the impact of SSN on signal jitter. An increase in voltage droop on the the power supply strongly correlates with increasing rise times. For pseudo-random bit sequences, SSN (and hence voltage droop) is random, and hence there is uncertainty in the rise time of the signal. This uncertainty is the jitter caused due to SSN. Thus SSN can lead to delay and false switching.

1.3.2 Coupling in Package Structures

In the case of a SoP module, to provide DC isolation between power supplies, the power and ground planes may be segmented into islands. In this case, EM coupling becomes a critical factor. Consider an SoP containing four modules shown in Figure 1. The digital module is the source of the simultaneous switching noise (SSN) containing harmonics at multiples of the clock frequency. For the case of a cell phone receiver, a -60dB insertion loss between the digital and RF modules can significantly degrade the performance of the front-end low-noise amplifier.

Figure 7 shows a three layer package PDN supplying power to a mixed-signal IC. Multiple power supplies are typically required in modern SoPs due to the various
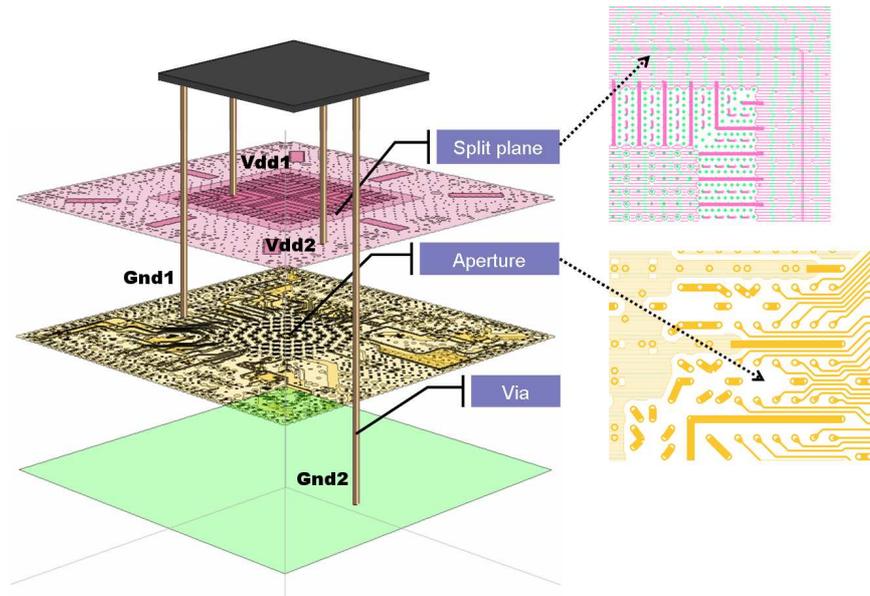
Figure 7. SSN coupling mechanisms in a realistic package.

integrated components. Split planes are required to provide DC isolation to the different supply voltages. Also, holes are created in the solid power/ground planes in order to route signals or to provide via anti-pads. The switching activity of digital circuitry causes a time varying current to be drawn from its power supply terminals, Vdd1-Gnd1. Due to the associated inductance of the loop, SSN is generated. SSN can couple horizontally across a plane pair and across power islands. Also, SSN couples vertically through vias, and through apertures. This can be regarded as a coupling by means of a wrap-around current on the edges of the planes. Through these mechanisms, ground bounce can occur across the Vdd2-Gnd2 planes in Figure 7. Thus, it becomes critical to model split planes and apertures.

1.3.3 Target Impedance

Digital components are broadband circuits whose switching circuits typically have energy concentrated in multiple discrete frequencies, which tend to be harmonics of the various clock frequencies that are employed. On the other hand, the transient behavior of the system depends on a large number of variables, including some high level considerations such as the program being executed.

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The PDN has a capacitive behavior at low frequencies and shows inductive behavior as we move towards the higher frequency range. However, this inductive trend is punctuated with a number of discrete resonances and anti-resonances. As far as a driver on-chip is concerned, the PDN must appear to be an ideal AC ground between its power and ground terminals. Therefore, the inductance of the PDN must be reduced to enable easy flow of charge to the required active circuits to mitigate the noise. The target impedance of the PDN is decided based on the core voltage and average current drawn by the processor. Based on the equations for voltage droop across the power supply impedance, it is possible to define a maximum allowed ripple. In practice, the maximum allowed ripple is assumed be 5% of the power supply voltage (Vdd)[3].

$$Z_{tar} = \frac{Vdd \times 5\%}{Id \times 50\%} \tag{6}$$

The current term in the denominator is $\frac{1}{2}$ the switching current in a clock cycle, which is assumed to be the current in each clock edge.

Decreasing supply voltages coupled with increasing power requirements tends to place stringent requirements on the target impedance [3] of the digital part. Clearly, time-efficient and accurate signal and power integrity (SI/PI) simulation will be a critical component of the SoP design flow.

1.4 Electrical Simulation of the Package

To meet the demands of high-performance packages, a simulation tool will have to capture the effects of the following geometrical features of the package:

1. Multiple power supply and signal layers

2. Apertures in power/ground planes

3. Slots in power/ground planes

4. Multiple signal line configurations (microstrip, stripline, CPW; single ended, differential)

5. Power/ground planes with necking (i.e. narrow strips)

6. Signal and power supply vias

7. Decoupling capacitors

The simulation methods for packages may be classified based on their formulation as circuit-based or EM-based, as well as a a third category which borrows conceptually from the two, and is labeled hybrid. These methods face a trade-off between their generality and CPU Time, as illustrated in Figure 8. Here, generality is meant to emphasize the class of problems for which a particular method can provide reasonably accurate results.

1.4.1 Circuit-based Methods

The simplest PDN model for packages is an equivalent inductance to model each ground pin. This has been used for quad flat packages (QFP) [7] and other lead-frame packages. However, for high speed micro-processors and ASICs, power/ground planes are routinely used to distribute power. These power/ground planes are electrically large and can support steady state cavity resonances. These resonance occur
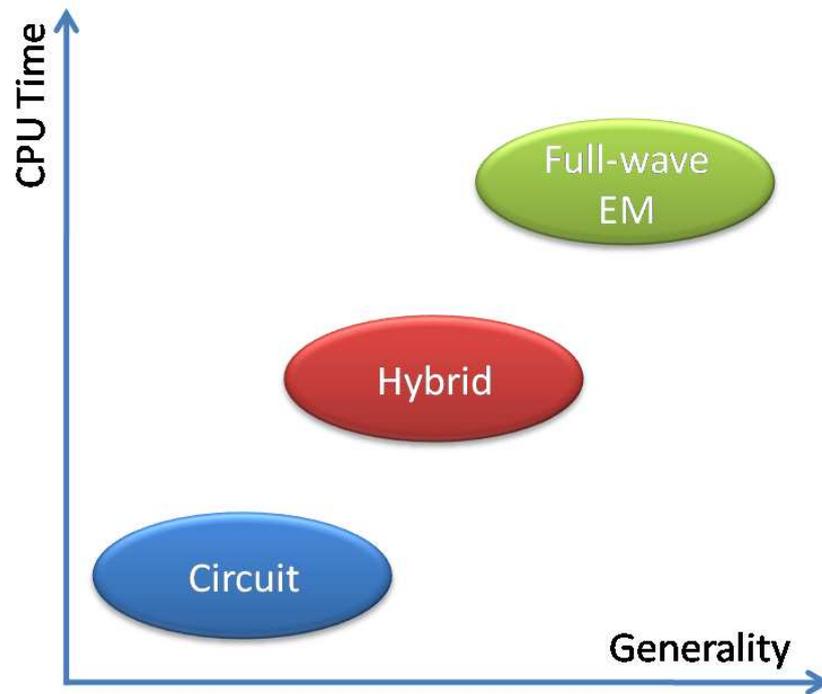
Figure 8. Trade-off between generality and CPU time for package simulation methods.

because the excitation port, for example, the I/O pin of a microprocessor can create noise which propagates in the lateral directions as a radial wave. This radial wave impinges upon what is effectively an open-circuit boundary at the edges of the package which causes reflections. Hence, circuit-based methods using partial inductance are applicable for low-frequency applications where the distributed effects of the PDN geometry can be neglected.

A circuit-based method which can be applied to package geometries is based on the transmission-line method (TLM). In this method, the power-plane is modeled as a 2D-grid of transmission line segments [8]. This method is applicable only for two-layer geometries, and is the basis for the transmission matrix method (to be discussed in Section 1.4.3.1).
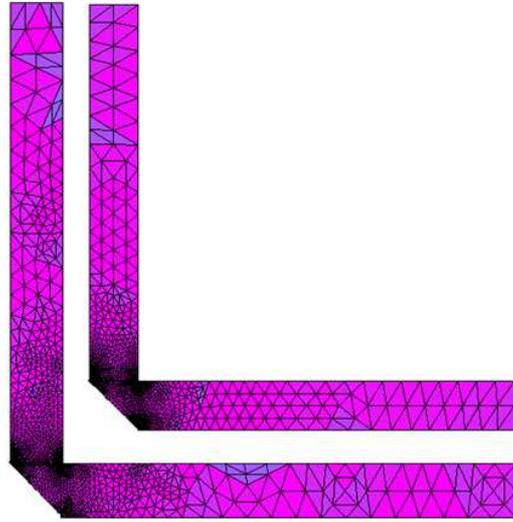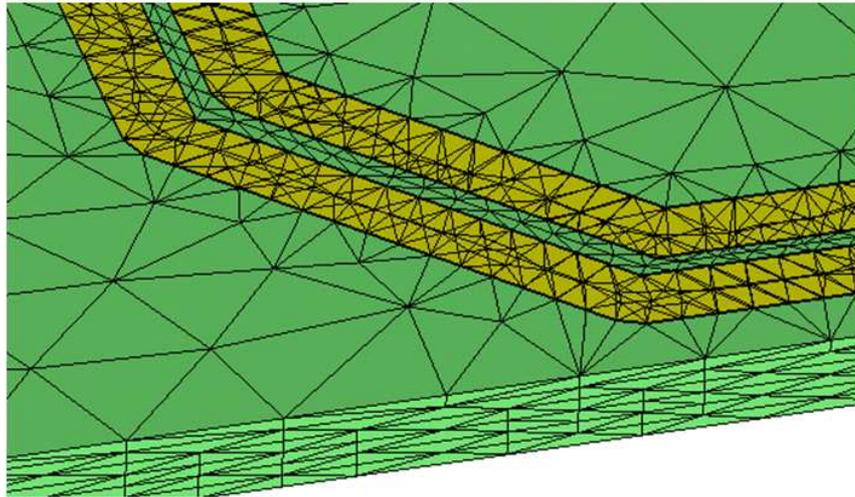
Figure 9. (a) Surface and (b) Volumetric mesh.

1.4.2 EM-based Methods

Of the full-wave EM methods available to simulate a package, the techniques resorted to are conventionally frequency domain methods. Packages are highly resonant low-loss structures. To completely characterize a package (in the time domain) requires simulating it for an impractically long period of time.

Full-wave frequency domain simulation methods can be broadly classified under the integral equation based method-of-moments (MoM) or differential equation based finite element method (FEM). These methods are accurate for the broadest class of problems. For package geometries, MoM methods are available [9][10] that use multi-layer Green's functions which enable it to use a surface mesh (Figure 9(a)). However, the resulting system matrix is dense. Hence, the computational complexity for such methods can be large, and the goal of full-package simulation is intractable. FEM-based techniques, on the other hand, lead to volumetric meshes (Figure 9(b)). Although the resultant system matrix is sparse, the use of a volumetric mesh results in rapid growth of the number of unknowns as problem size grows. Since packages are electrically large structures, only small subdomains of the package geometry can be simulated using FEM.

1.4.3 Hybrid Methods

A package can be described as a planar circuit. The concept of planar circuits was introduced in [11]. A planar circuit is a microwave structure in which one of the three dimensions, say z, is much smaller than the wavelength. Under this condition, it can be assumed that the field is invariant along the z-direction. Hence, $\frac{\partial}{\partial z} = 0$ and the Helmholtz wave equation can be reduced to 2 dimensions as follows:

$$\left(\nabla_t^2 + k^2\right)\mathrm{u} = j\omega\mu dJ \tag{7}$$
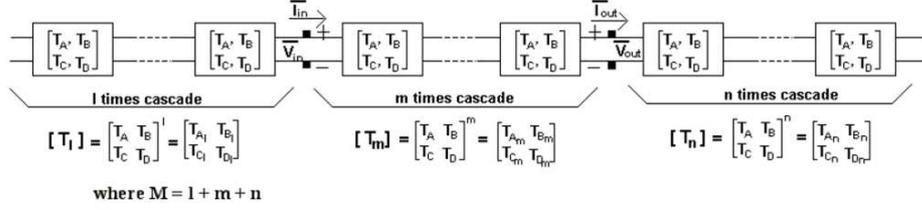
Figure 10. Cascade connection in TMM.

where

$$\nabla_t^2 = \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right)$$

$$k = j\omega\sqrt{\mu\varepsilon}$$

The open circuit at the boundary can be represented by a magnetic wall or Neumann boundary condition, which completes the problem formulation.

The two most prominent solutions in literature are the transmission matrix method (TMM)[12] and the Green's function based segmentation technique.

1.4.3.1   The Transmission Matrix Method

TMM is a technique used to solve the equivalent circuit representation that results under the finite difference solution of the wave equation. The equivalent circuit described in [8] can conventionally be solved using SPICE. However, the same equivalent circuit can also be reduced in terms of cascaded transmission matrices, as shown in Figure 10. Each of the cascaded T-matrices represents one column of cells in the discretized geometry. Thus, port to port ABCD parameters can be calculated which can in turn be used to calculate S-, Y-, or Z-parameters.

The advantage of this approach is that the overall system to be solved for a problem containing N cells is only of order $\sqrt{N}$, and with the ability to incorporate decoupling capacitors, this technique does have considerable advantages for single plane-pair geometries.

Using Gauss elimination, the equivalent circuit solved directly (resulting in a system containing N equations) will have a computational complexity of $O(N^3)$, while

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by employing TMM, the complexity reduces to $O(N^{1.5})$. Memory reduces from $O(N^2)$ to $O(N)$.

However, it must be noted that while the equivalent circuit when solved directly leads to a much larger matrix, this matrix is also sparse. Thus, by employing reordering techniques such as nested dissection [13], and by using an optimized sparse-solver, the computational complexity of direct solution can be reduced to $O(N^{1.5})$ and memory to $O(N \log N)$.

Thus, in terms of computational effort, TMM has a slight if not overwhelming advantage. This advantage needs to be reconciled with the limitations of the technique, which are:

1. TMM relies on identical columns of cells. The matrix-power operations that have to be performed while cascading the T-matrices requires a similarity transformation for each non-identical column. Thus, this technique works well for rectangular geometries, but is not as efficient for irregular geometries.

2. The matrix power operations lead to an ill-conditioned system.

3. The modeling of gap-coupling may require placing elements between columns of cells which are not neighbors. This cannot be done under TMM, as the cascading property is lost.

4. TMM cannot be applied for multiple plane-pair geometries with apertures, as this would require placing coupling elements between non adjacent layers.

1.4.3.2 The Segmentation Technique

The impedance matrix of a rectangular plane-pair of dimensions $a \times b$, with plane separation d and dielectric constant ε, with aribitrary port locations (x_i, y_i) and (x_j, y_j), can be derived as [11]:

$$Z_{ij}(\omega) = j\omega\mu d \sum_{n=0}^{n=\infty} \sum_{m=0}^{m=\infty} \frac{\varepsilon_n^2 \varepsilon_m^2}{(k_{mn}^2 - k^2)\, ab} f(x_i, y_i, x_j, y_j) \tag{8}$$
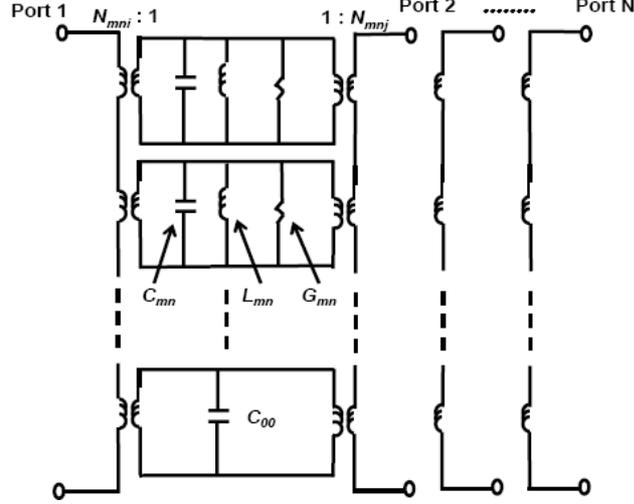
Figure 11. Equivalent circuit for a plane-pair.

where

$$f(x_i, y_i, x_j, y_j) = \left(\cos\frac{m\pi x_i}{a} \sin c\frac{m\pi t_{xi}}{2a}\right)\left(\cos\frac{n\pi y_i}{b} \sin c\frac{n\pi t_{yi}}{2b}\right)$$
$$\left(\cos\frac{m\pi x_j}{a} \sin c\frac{m\pi t_{xj}}{2a}\right)\left(\cos\frac{n\pi y_j}{b} \sin c\frac{n\pi t_{yj}}{2b}\right) \qquad (9)$$

Here $t_{x(i/j)}, t_{y(i/j)}$ is the size of the port, $k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2$ and k is the complex wavenumber. Further details can be found in [14][15][16].

While (9) provides a numerical technique for calculating the response of a rectangular plane-pair, this response cannot be directly used in a system-level simulation, containing other circuit elements such as non-linear circuitry and terminations. An intermediate step is required whereby the frequency response is used to synthesize a SPICE netlist. This macro-modeling step is not desirable because the synthesized equivalent circuit may not preserve passivity. Thus, to eliminate this step, (9) can be used to directly synthesize an equivalent circuit. This process is described in [17], and the equivalent circuit for a plane-pair is shown in Fig 11.

When irregular geometries are encountered, the structure is segmented into sections which are rectangular. The rectangular sections are then simulated separately and the boundaries between segments are stitched together using many "virtual

17
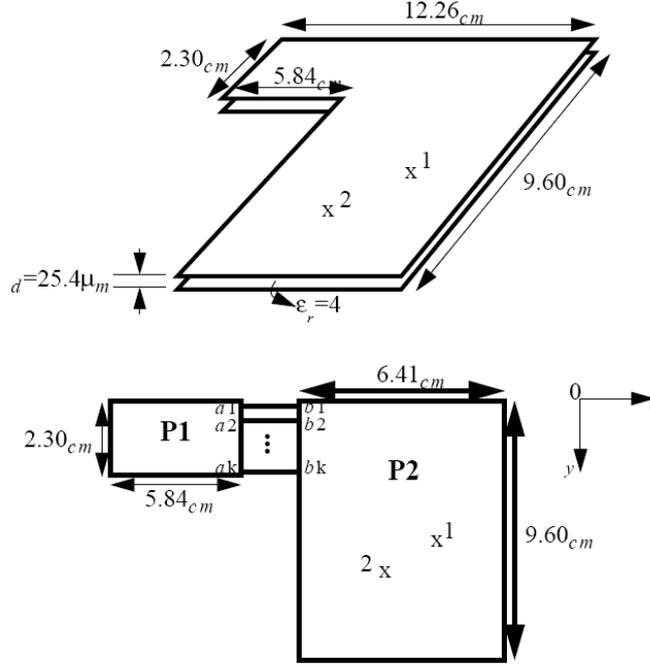
Figure 12. Segmentation of an L-shaped plane-pair.

ports". An example of this segmentation process is shown in Figure 12.

The limitations of this technique are:

1. Equation (9) requires a double infinite sum for all the modes that may exist in the structure. The convergence of the sum may be slow. However, an acceleration technique has been proposed in [18], which compromises on accuracy.

2. The technique is cumbersome for extremely irregular geometries, which requires several virtual ports between segments. Also, for multi-layered structures with apertures, the segmentation must be performed both horizontally and vertically.

1.5 Overview of the Proposed Hybrid Method

The methods developed in this thesis are based on a combination of insights from circuit theory and EM-field solvers, specifically tuned to modeling electrically large, multi-layer planar package geometries. The flow for the proposed method is shown in Figure 13.

18
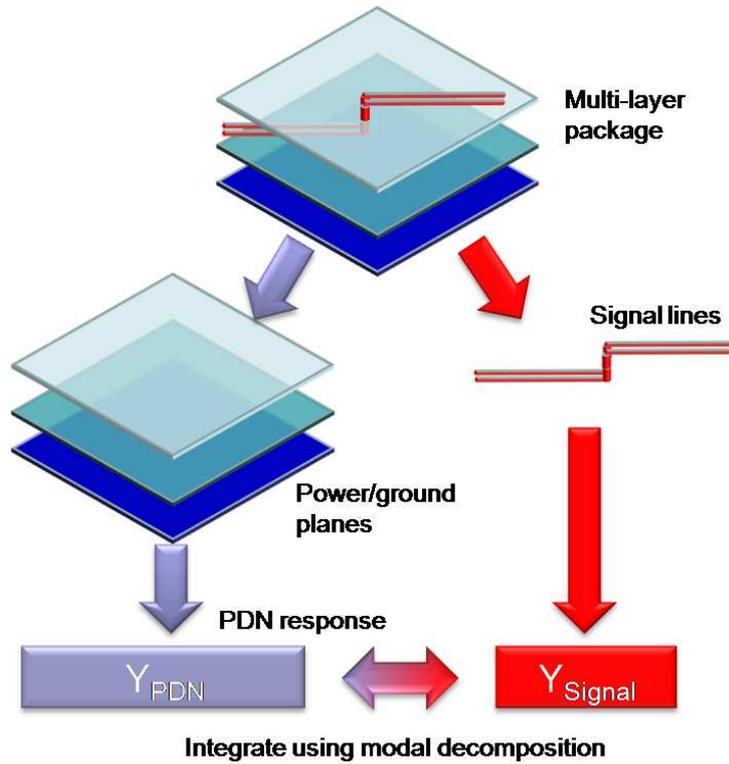
Figure 13. Overview of proposed hybrid method.

Modern packages consist of the PDN and the SDN. As can be expected, the response of the SDN is highly dependant on the design of the PDN. This is because the interconnects that form the SDN use the power/ground planes of the PDN as their reference planes. In this thesis, the complexity of the problem is reduced by decoupling the SDN and PDN problems. Thus the PDN and the SDN can be simulated in isolation, and the obtained response can finally be integrated together.

1. *Simulation of the PDN in isolation:*

   The PDN problem involves obtaining the frequency response of an irregular, electrically large, multi-layer power/ground planes containing apertures, vias and decoupling capacitors. This thesis focuses on the development of two methods, the second of which is an evolutionary development of the first. These methods are the multi-layer finite difference method (M-FDM) and the multi-layer finite element method (M-FEM). Both methods are based on the extraction of

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an equivalent circuit model for a two-layer geometry, which is then extended to multiple layers based on transformations of the admittance matrix (to be described in Section 1.6.

2. *Simulation of the SDN in isolation*

   The difficulty in using a full-wave method for co-simulating the SDN and the PDN is primarily because the interconnection width is much smaller than the lateral dimensions of the PDN. This leads to a dense mesh and a computationally intractable problem size. However, the interconnections can be divided into segments which can be considered to support a quasi transverse electromagnetic (TEM) mode. These segments can be analyzed as multi-conductor transmission lines (MTL). In this thesis, an electrostatic 2D solver is used to obtain the multi-conductor per unit length inductance and capacitance matrices, that characterize the interconnects.

3. *Integration of the PDN and SDN responses to obtain the system response*

   One of the solution techniques for the simulation of multi-conductor transmission structures is the theory of modal decomposition, to be described in Section 1.7. Modal decomposition enables the decoupling of the multi-conductor transmission line (MTL) equations, such that a system of n-conductors (including the reference conductor) can be represented in terms of a circuit containing $n - 1$ transmission-lines referenced to the system ground, and coupling networks containing controlled sources. This model can be shown to provide an exact solution to the MTL equations. Thus modal decomposition can be used to integrate the responses of the PDN and the SDN, that have been obtained in isolation.

1.6 Nodal Admittance Matrices and Shifting of Reference Nodes

The Helmholtz wave equation (7) is the governing equation for power/ground plane problems. The solution of this equation using finite methods leads to system of equations that can be expressed in terms of an equivalent circuit containing only passive elements and independent current sources. These equations hence are expressions of Kirchoff's current law (KCL).

Thus, the theory of indefinite admittance matrices can be applied to the solution of power/ground problems. Although the application of finite methods such as finite differences to (7) directly provides the admittance matrix for a simple two-layer problem, an understanding of the properties of admittance matrices is required to extend the method to multi-layer geometries, as well as for addition of components to the PDN. These components include decoupling capacitors, transmission lines referenced to power planes, as well as circuit models to capture second order effects, such as fringing fields.

The key advantage of using admittance matrices is that it can be assembled on a per-element basis, and the admittance matrices of individual components can simply be superpositioned to yield the total circuit admittance matrices. The contributions of these individual elements are referred to as *stamps*, and the rules for their inclusion in the system matrix are called stamp rules. Thus, element stamps can be directly included in the system matrix without the need to consider the rest of the circuit. The only required information are the node numbers of the terminals of the element and its stamp. Current sources do not contribute to the admittance matrix, but can similarly be superpositioned to yield the right hand side of the matrix equation. This superposition is valid as long as the reference node of the element under consideration is the same as the reference node of the complete circuit.

For example, consider the simple circuit containing three conductances G_1, G_2
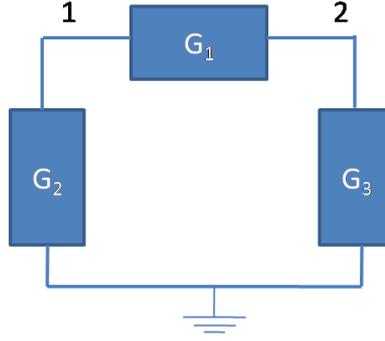
Figure 14. Simple circuit containing conductances.

and G_3, as shown in Figure 14.

The stamp for a conductance G is

$$\overline{\overline{\mathbf{Y}}}_{\mathbf{g}} = \begin{pmatrix} G & -G \\ -G & G \end{pmatrix} \tag{10}$$

Applying this stamp and the superposition principle, the admittance matrix of the circuit in Figure 14 can be obtained simply from inspection:

$$\overline{\overline{\mathbf{Y}}} = \begin{pmatrix} G_1 + G_2 & -G_1 \\ -G_1 & G_1 + G_3 \end{pmatrix} \tag{11}$$

A critical limitation of nodal analysis using indefinite admittance matrices is in the handling of voltage sources. This limitation is addressed by the modified nodal analysis method [19]. However, the formulations employed in this thesis do not require voltage sources, and hence, nodal analysis is sufficient.

An important application of admittance matrices in this thesis is in shifting references. Typically, the type of problem that is regularly faced is the following: the admittance matrix of a particular component (for example, a transmission line) is readily available. However, the reference node of this component is not the same as the reference node of the rest of the circuit. This can occur, for example, when a microstrip is routed on top of a power and ground plane-pair. The reference node of the overall circuit is the ground plane. However, the reference for the microstrip line is the power plane, on which the return current of the microstrip line flows.
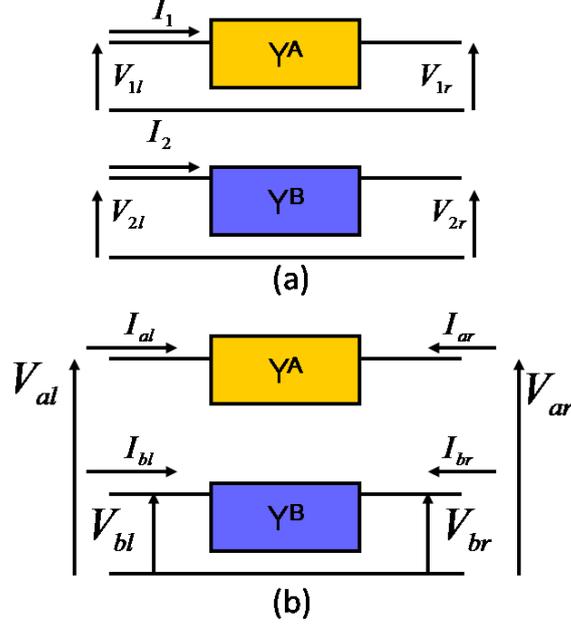
Figure 15. (a) Two-port networks with separate references (b) Combined four-port network with common reference.

Thus simply applying the element stamp will lead to an incorrect response. The reference of the component (in this case, the microstrip line) must be shifted to that of the system ground. This can be done using admittance matrices [20].

This is illustrated, without loss of generality, by using two-port networks with separate ground references, as shown in Figure 137(a). The four-port admittance matrix for the system with the common reference node can be derived as follows:

$$Y_{11}^A V_{1l} + Y_{12}^A V_{1r} = I_1 \tag{12}$$

$$Y_{11}^B V_{2l} + Y_{12}^B V_{2r} = I_2 \tag{13}$$

By noticing that

$$I_{bl} = I_2 - I_1, I_{al} = I_1,$$

$$V_{1l} = V_{al} - V_{bl}, V_{1r} = V_{ar} - V_{br},$$

$$V_{2l} = V_{bl} \text{ and } V_{2r} = V_{br},$$

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it is possible to write one row of the admittance matrix of the combined four-port.

$$Y_{11}^A(V_{al} - V_{bl}) + Y_{12}^A(V_{ar} - V_{br}) = I_{al} \qquad (14)$$

A similar approach can be used to obtain the complete system in the following form:

$$\begin{pmatrix} Y^A & -Y^A \\ -Y^A & Y^A + Y^B \end{pmatrix} \begin{pmatrix} V_{al} \\ V_{ar} \\ V_{bl} \\ V_{br} \end{pmatrix} = \begin{pmatrix} I_{al} \\ I_{ar} \\ I_{bl} \\ I_{br} \end{pmatrix} \qquad (15)$$

This approach of shifting reference nodes to accommodate local references of sub circuits will be repeatedly applied throughout this thesis.

1.7 Modeling the Interaction between Signal Lines and the Non-Ideal Power/Ground Planes

Signal lines placed on chip have small electrical lengths. Hence, it is possible to model these lines simply as lumped components. However, with increasing signaling frequency the signal lines routed on the package and board exhibit significant transmission line behavior, and must be modeled as transmission lines.

Traditionally, in packaged systems the analysis of the signal distribution network (SDN) and the power distribution network (PDN) have been carried out independently. Once the layout of a system is available, geometrical information is extracted to obtain models for the PDN and the SDN separately. However, it is known that effects like simultaneous switching noise (SSN) that occur in the PDN can affect the quality of the signal that propagates through the SDN. Analyzing the two networks separately fails to account for these effects accurately and hence compromises on the quality of the SI analysis.

Thus, most modeling approaches have simply considered the transmission lines
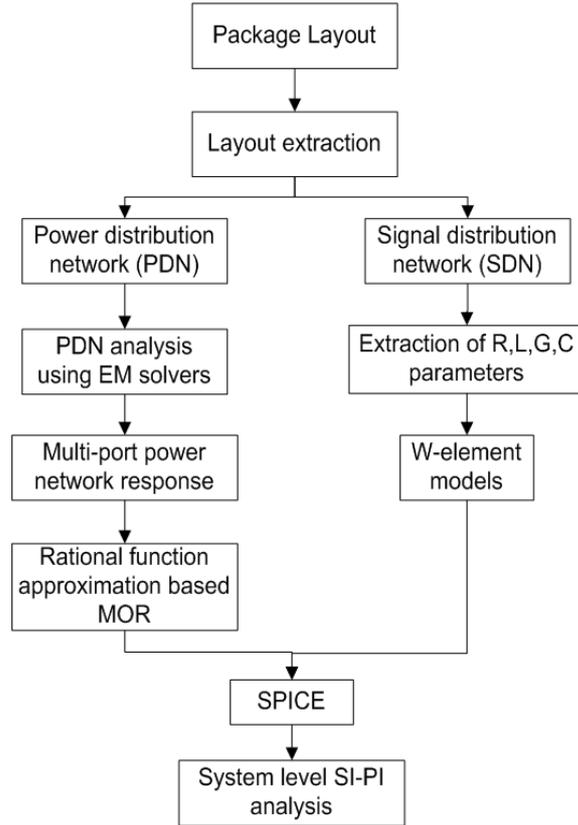
Figure 16. Flowchart for system level SI-PI analysis.

to be ideal without considering the effect of the return path. In reality, transmission structures on package experience significant coupling to the power distribution network. For example, an interconnect routed between a power and ground plane resembles a stripline; however, the power and ground planes need not be at the same AC potential. Hence, additional modes can be supported by the structure.

Transmission structures on package must be treated as a multi-conductor transmission line under the quasi transverse electromagnetic (TEM) field assumption[21]. The fields may not be pure TEM because the dielectric medium may not be homogenous (as in the case of microstrip). Also, the loss in the structure causes a non-zero field component in the direction of propagation. However, as long as this loss is small, the longitudanal component of the fields is small compared to the transverse component, and can be ignored. Thus, the methods of multi-conductor transmission line

(MTL) analysis can be applied.

The MTL equations are given by [4][21]

$$\frac{\partial}{\partial z}\overline{\mathbf{V}}(z,t) = -\overline{\overline{\mathbf{R}}}\overline{\mathbf{I}}(z,t) - \overline{\overline{\mathbf{L}}}\frac{\partial}{\partial t}\overline{\mathbf{I}}(z,t) \qquad (16)$$

$$\frac{\partial}{\partial z}\overline{\mathbf{I}}(z,t) = -\overline{\overline{\mathbf{G}}}\overline{\mathbf{V}}(z,t) - \overline{\overline{\mathbf{C}}}\frac{\partial}{\partial t}\overline{\mathbf{V}}(z,t) \qquad (17)$$

where $\overline{\overline{\mathbf{R}}}$, $\overline{\overline{\mathbf{L}}}$, $\overline{\overline{\mathbf{G}}}$ and $\overline{\overline{\mathbf{C}}}$ are the per-unit-length resistance, inductance, conductance and capacitance matrices, respectively. For $n+1$ conductors, these equations represent a set of coupled first-order partial differential equations. In the time harmonic case, it is possible to decouple the MTL equations and express them as second order ordinary differential equations in the frequency domain as

$$\frac{d^2}{dz^2}\overline{\mathbf{V}}(z) = (\overline{\overline{\mathbf{R}}} + j\omega\overline{\overline{\mathbf{L}}})(\overline{\overline{\mathbf{G}}} + j\omega\overline{\overline{\mathbf{C}}})\overline{\mathbf{V}}(z) \qquad (18)$$

$$\frac{d^2}{dz^2}\overline{\mathbf{I}}(z) = (\overline{\overline{\mathbf{G}}} + j\omega\overline{\overline{\mathbf{C}}})(\overline{\overline{\mathbf{R}}} + j\omega\overline{\overline{\mathbf{L}}})\overline{\mathbf{I}}(z) \qquad (19)$$

A general technique for solving these equations involves a similarity transformation and is often referred to as modal decomposition. The $n \times n$ complex matrices $\overline{\overline{\mathbf{T}}}_\mathbf{V}$ and $\overline{\overline{\mathbf{T}}}_\mathbf{I}$ are defined such that

$$\overline{\mathbf{V}}(z) = \overline{\overline{\mathbf{T}}}_\mathbf{V}\overline{\mathbf{V}}_\mathbf{m}(z) \qquad (20)$$

$$\overline{\mathbf{I}}(z) = \overline{\overline{\mathbf{T}}}_\mathbf{I}\overline{\mathbf{I}}_\mathbf{m}(z) \qquad (21)$$

$\overline{\overline{\mathbf{T}}}_\mathbf{V}$ and $\overline{\overline{\mathbf{T}}}_\mathbf{I}$ are similarity transformations that covert the actual phasor voltages and currents, $\overline{\mathbf{V}}$ and $\overline{\mathbf{I}}$ to the mode voltages and currents, $\overline{\mathbf{V}}_\mathbf{m}$ and $\overline{\mathbf{I}}_\mathbf{m}$.

Substituting the modal vectors in 18 and 19,

$$\frac{d^2}{dz^2}\overline{\mathbf{V}}_\mathbf{m}(z) = \overline{\overline{\mathbf{T}}}_\mathbf{V}^{-1}\overline{\overline{\mathbf{ZY}}}\overline{\overline{\mathbf{T}}}_\mathbf{V}\overline{\mathbf{V}}_\mathbf{m}(z) \qquad (22)$$

$$\frac{d^2}{dz^2}\overline{\mathbf{I}}_\mathbf{m}(z) = \overline{\overline{\mathbf{T}}}_\mathbf{I}^{-1}\overline{\overline{\mathbf{YZ}}}\overline{\overline{\mathbf{T}}}_\mathbf{I}\overline{\mathbf{I}}_\mathbf{m}(z) \qquad (23)$$

where $\overline{\overline{\mathbf{Z}}} = \overline{\overline{\mathbf{R}}} + j\omega\overline{\overline{\mathbf{L}}}$ and $\overline{\overline{\mathbf{Y}}} = \overline{\overline{\mathbf{G}}} + j\omega\overline{\overline{\mathbf{C}}}$. If $\overline{\overline{\mathbf{T}}}_\mathbf{V}$ and $\overline{\overline{\mathbf{T}}}_\mathbf{I}$ diagonalize the matrix product $\overline{\overline{\mathbf{ZY}}}$ and $\overline{\overline{\mathbf{YZ}}}$, respectively,

$$\overline{\overline{\mathbf{T}}}_\mathbf{V}^{-1}\overline{\overline{\mathbf{ZY}}}\overline{\overline{\mathbf{T}}}_\mathbf{V} = \overline{\overline{\mathbf{T}}}_\mathbf{I}^{-1}\overline{\overline{\mathbf{YZ}}}\overline{\overline{\mathbf{T}}}_\mathbf{I} = \overline{\overline{\lambda}} \qquad (24)$$

where $\bar{\bar{\lambda}}$ is a diagonal $n \times n$ matrix containing the eigenvalues of the matrix products $\overline{\overline{\mathbf{ZY}}}$ and $\overline{\overline{\mathbf{YZ}}}$. The columns of $\overline{\overline{\mathbf{T}}}_{\mathbf{V}}$ and $\overline{\overline{\mathbf{T}}}_{\mathbf{I}}$ contain the eigenvectors of the corresponding matrix products $\overline{\overline{\mathbf{ZY}}}$ and $\overline{\overline{\mathbf{YZ}}}$. If the multiplicity of all the eigenvalues is equal to one, then the transformation matrices simultaneously diagonalize both $\overline{\overline{\mathbf{Z}}}$ and $\overline{\overline{\mathbf{Y}}}$. Now, since the per-unit-length matrices are symmetric, $\left(\overline{\overline{\mathbf{ZY}}}\right)^T = \overline{\overline{\mathbf{YZ}}}$. Hence,

$$\left(\overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{-1}\overline{\overline{\mathbf{ZY}}}\overline{\overline{\mathbf{T}}}_{\mathbf{V}}\right)^T = \bar{\bar{\lambda}} \tag{25}$$

$$\text{Also, } \left(\overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{-1}\overline{\overline{\mathbf{ZY}}}\overline{\overline{\mathbf{T}}}_{\mathbf{V}}\right)^T = \overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{T}\overline{\overline{\mathbf{YZ}}}\left(\overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{-1}\right)^T \tag{26}$$

Comparing (26) with (24),

$$\overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{T} = \overline{\overline{\mathbf{T}}}_{\mathbf{I}}^{-1} \tag{27}$$

Thus it is sufficient to only find the transformation to diagonalize one of the matrix products, $\overline{\overline{\mathbf{ZY}}}$ or $\overline{\overline{\mathbf{YZ}}}$, to find the transformation to diagonalize the other. These transformation matrices allow us to solve the MTL equations as simply n single transmission line problems, to obtain the modal voltages and currents, $\overline{\mathbf{V}}_{\mathbf{m}}(z)$ and $\overline{\mathbf{I}}_{\mathbf{m}}(z)$. To illustrate this, consider (24) in the following form:

$$\overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{-1}\overline{\overline{\mathbf{Z}}}\left(\overline{\overline{\mathbf{T}}}_{\mathbf{I}}\overline{\overline{\mathbf{T}}}_{\mathbf{I}}^{-1}\right)\overline{\overline{\mathbf{Y}}}\overline{\overline{\mathbf{T}}}_{\mathbf{V}} = \overline{\overline{\mathbf{T}}}_{\mathbf{I}}^{-1}\overline{\overline{\mathbf{Y}}}\left(\overline{\overline{\mathbf{T}}}_{\mathbf{V}}\overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{-1}\right)\overline{\overline{\mathbf{Z}}}\overline{\overline{\mathbf{T}}}_{\mathbf{I}} = \bar{\bar{\lambda}} \tag{28}$$

Regrouping the matrix products in (28) and defining $\overline{\overline{\mathbf{T}}}_{\mathbf{V}}^{-1}\overline{\overline{\mathbf{Z}}}\overline{\overline{\mathbf{T}}}_{\mathbf{I}} = \overline{\overline{\mathbf{Z}}}_{\mathbf{m}}$ and $\overline{\overline{\mathbf{T}}}_{\mathbf{I}}^{-1}\overline{\overline{\mathbf{Y}}}\overline{\overline{\mathbf{T}}}_{\mathbf{V}} = \overline{\overline{\mathbf{Y}}}_{\mathbf{m}}$, (28) can be rewritten as

$$\overline{\overline{\mathbf{Z}}}_{\mathbf{m}}\overline{\overline{\mathbf{Y}}}_{\mathbf{m}} = \overline{\overline{\mathbf{Y}}}_{\mathbf{m}}\overline{\overline{\mathbf{Z}}}_{\mathbf{m}} = \bar{\bar{\lambda}} \tag{29}$$

$\overline{\overline{\mathbf{Z}}}_{\mathbf{m}}$ and $\overline{\overline{\mathbf{Y}}}_{\mathbf{m}}$ are called the modal per-unit-length impedance and admittance matrices, respectively. Also,

$$\bar{\bar{\lambda}}\overline{\overline{\mathbf{Z}}}_{\mathbf{m}} = \left(\overline{\overline{\mathbf{Z}}}_{\mathbf{m}}\overline{\overline{\mathbf{Y}}}_{\mathbf{m}}\right)\overline{\overline{\mathbf{Z}}}_{\mathbf{m}} = \overline{\overline{\mathbf{Z}}}_{\mathbf{m}}\bar{\bar{\lambda}} \tag{30}$$

Since $\bar{\bar{\lambda}}$ is diagonal, the above equation implies that so is $\overline{\overline{\mathbf{Z}}}_{\mathbf{m}}$. A similar approach can be used to show that $\overline{\overline{\mathbf{Y}}}_{\mathbf{m}}$ is also diagonal. This is only the case, however, if all

the eigenvalues have a multiplicity of one. If not, then $\overline{\overline{\mathbf{Z}}}_{\mathbf{m}}$ and $\overline{\overline{\mathbf{Y}}}_{\mathbf{m}}$ will be block diagonal.

Thus, it can be shown that

$$\frac{\partial}{\partial z}\overline{\mathbf{V}}_{\mathbf{m}}(z) = -\overline{\overline{\mathbf{Z}}}_{\mathbf{m}}\overline{\mathbf{I}}_{\mathbf{m}}(z) \tag{31}$$

$$\frac{\partial}{\partial z}\overline{\mathbf{I}}_{\mathbf{m}}(z) = -\overline{\overline{\mathbf{Y}}}_{\mathbf{m}}\overline{\mathbf{V}}_{\mathbf{m}}(z) \tag{32}$$

These equations represent a set of n single transmission line problems, whose solutions are the modal voltages and currents. To convert the modal parameters to the actual line voltages and currents is simple, and merely requires the application of the transformations given in (20) and (21). In a circuit simulation environment, this can be done by simulating the n modal transmission lines with modifications to their terminations, which essentially performs this transformation.

1.8 Contributions and Dissertation Outline

The motivation behind this thesis is the need to accurately model signal and power integrity problems in large packages and boards. **The main focus of this thesis is on the development of an EM-Circuit hybrid method called the multi-layer finite difference method (M-FDM).**

The contributions of this thesis are listed in Figure 17. The formulation for M-FDM is developed by applying the finite difference method to a single plane-pair package. It is assumed that, since the lateral dimensions of the board or package are much larger than the substrate height, the electric fields within the package are predominantly oriented along the direction of stacking. This assumption results in a surface finite difference mesh that is applied only to the metal layers. For single plane-pair geometries, the finite difference equations are treated as expressions of Kirchoff's current law, and hence an equivalent circuit is derived. For multiple plane-pair geometries, the equivalent circuit for each plane-pair is obtained individually.

EM/Circuit Hybrid

M-FDM
-Multi-layer structures with apertures
- $O(N^{1.5})$ time and $O(N\log_2 \sqrt{N})$ memory
-Circuit extraction compatible with SPICE
-Integration of T-lines with modal decomposition

Fringe and plane gap augmentations
-Modeling of fringe and gap fields using multiport coupling networks
-Obtained using 2D electrostatic simulation

Limitations of M-FDM
-Fringing fields not modeled at plane edges and slots in planes
-Square mesh leads to large number of unknowns due to presence of small features

MFEM
-Mesh is based on adaptive Delaunay triangulation
-Sparse system matrix
-Reduction in number of unknowns as compared to M-FDM
-Model is SPICE compatible

Figure 17. Contributions of this research.

These isolated network models are connected together by shifting the reference nodes to a common system ground. This approach is the underlying algorithm of M-FDM. The key contribution of this approach is the ability to model vertical coupling of SSN through apertures in the solid planes. Using efficient reordering and factorization techniques, the computational and memory complexity of the method are $O(N^{1.5})$ and $O(N \log_2 \sqrt{N})$, respectively.

One limitation of M-FDM stems from the inaccuracy induced because of modeling only the vertically directed electric field component. This scheme is sufficiently accurate for structures whose lateral dimensions are much larger than the dielectric thickness. When this condition is not met, the technique may not be accurate. However, using 2D electrostatic analysis, it is possible to obtain correction elements that can be used to update the M-FDM system matrix. These **fringe augmentation (FA)** elements can be represented in circuit form as inductances and capacitances. When applied to the edge cells of the M-FDM model, these circuit elements can correct the discrepancy due to neglecting the fringe fields.

Most PDNs are split into power islands which have been used to supply multiple devices with different power supply voltages. It is possible for these power islands to be coupled to each other across the slot. This coupling has been modeled by performing a 2D electrostatic analysis of the coupled structures. The results of the 2D analysis have been used to derive a multi-port coupling network. The approach is called **plane gap augmentation (PGA)**, and extends the capabilities of M-FDM to accurately modeling multilayered packages with slots.

Together, the FA and PGA methods form the second major contribution of this research.

The second limitation of M-FDM arises due to the meshing scheme. Since a square mesh is used, the dimensions of the mesh are controlled by the minimum feature size. This can lead to an extremely large number of unknowns for a practical geometry.

This problem has been addressed by the development of a promising novel approach called the multilayer finite element method (MFEM). An adaptive triangular mesh is applied to the geometry. The dimensions of the edge elements in this mesh are based on the wavelength at the maximum frequency of simulation. The mesh becomes dense only in the vicinity of small features. This enables MFEM to model realistic structures containing such small features with far fewer unknowns than M-FDM. Also, the model generated using MFEM is also SPICE compatible, and the resultant system matrix is sparse. Thus MFEM preserves the advantages of M-FDM, while overcoming the mesh density limitation. **MFEM is the third major contribution of this research.**

The response of a signal net is critically affected by its return path, which in packages/boards is constituted by a non-ideal power/ground plane. The integration of the signal nets with the PDN has been accomplished using modal decomposition techniques.

The selection and placement of decoupling capacitors on the PDN critically affects its impedance profile, that must be maintained below the target impedance over a wide frequency range. This process has been automatized using a GA-based optimizer. The location and description of the decaps have been used as the "chromosomes" on which the GA operates. At the end of each generation, solutions that will contribute to the next generation are selected based on relative success in meeting the objective function. The optimizer has been used to place decaps for meeting target impedance in multi-layer test structures as well as for maintaining signal integrity in structures with transmission lines.

The integration of the transmission lines with M-FDM using modal decomposition, and the GA-based optimization engine for the selection and placement of decoupling capacitors are the minor contributions of this research.

1.8.1   Summary of Contributions

The contributions of this research are summarized below:

Major Contributions:

1. The multi-layer finite difference method (M-FDM) for the modeling of arbitrary multi-layer power and ground planes of modern electronic packaging.

2. The fringe augmentation (FA) and plane gap augmentation (PGA) methods for modeling second order effects such as fringing fields at metal edges, and gap fields across slots in the metal planes

3. The multi-layer finite element method (MFEM) for modeling multi-layer power and ground planes with multi-scale geometries.

Minor Contributions:

1. Integration of transmission line structures with M-FDM using modal decomposition

2. A genetic algorithm based optimization method for the selection and placement of decoupling capacitors

3. The implementation of these methods in a tool called MSDT 1.

1.8.2 Dissertation Outline

The rest of this thesis is organized as follows:

1. The formulation of the multi-layer finite difference method (M-FDM) is discussed in Chapter 2. Initially, the discussion is confined to packages with two metal layers, and is then extended to multi-layer geometries. This extension is accomplished by shifting the reference node, as discussed in Section 1.6. The results from the method have been verified by comparisons with EM-simulations and measurements. A study of the scalability of M-FDM has also been undertaken.

2. The modeling of fringing fields at metal edges is considered in Chapter 3. The proposed method, called fringe augmentation (FA), is used to update the system matrix obtained from M-FDM.

3. The modeling of gap fields using the plane gap augmentation (PGA) method is the focus of Chapter 4. Both the FA (Chapter 2) and the PGA methods rely on a 2D electrostatic solution for obtaining the corrections to the M-FDM system matrix.

4. The simulation of signal nets in the context of their non-ideal return paths is discussed in Chapter 5.

5. The selection and placement of decoupling capacitors is critical to meeting target impedance requirements. This process has been automatized using a genetic algorithm, and is the focus of Chapter 6.

6. The ideas behind M-FDM can be applied to other finite methods as well. An adaptive triangular mesh based scheme, called the multi-layer finite element method (MFEM), has been developed to handle multi-scale geometries. The formulation for MFEM and some initial results are developed in Chapter 7.

7. The dissertation is concluded in Chapter 8.

CHAPTER 2

POWER INTEGRITY MODELING USING THE MULTI-LAYER FINITE DIFFERENCE METHOD

2.1   Introduction

Modern PCB and package power distribution networks (PDN) are designed using multiple layers of solid metal planes, which are alternatively assigned power and ground potentials. Since these power/ground planes are layered alternatively, a useful term to describe a stack-up containing multiple layers dedicated to the PDN is power/ground *plane-pair*. This arrangement reduces the effective inductance as seen by the power supply terminals of switching circuits on chip, which helps in mitigating simultaneous switching noise (SSN).

The use of power/ground planes in modern electronic packaging depends on the ability of design tools to characterize their behavior. SSN or voltage fluctuations on the planes are called *plane bounce*. These occur when the current transients in the PDN excite resonant modes, which can lead to signal integrity problems as well. For example, mode conversion at vias due to return-path discontinuities (RPD) is one of the main contributors to power/ground noise in packages. At the via hole, the parallel-plate mode gets excited due to switching signal currents, and conversely, the noise voltage between the planes gets coupled to the stripline mode.

Thus the problem of obtaining the response of a PDN is fundamental to solving power and signal integrity problems. Power/ground plane geometries can be separated into single plane-pair and multiple plane-pair structures.

2.1.1   Single Plane-Pair

The cross-section of a single plane-pair geometry is shown in Figure 18. In a single plane-pair, the fundamental noise coupling occurs in the horizontal direction between the two planes that constitute the plane pair. The source of this noise coupling can
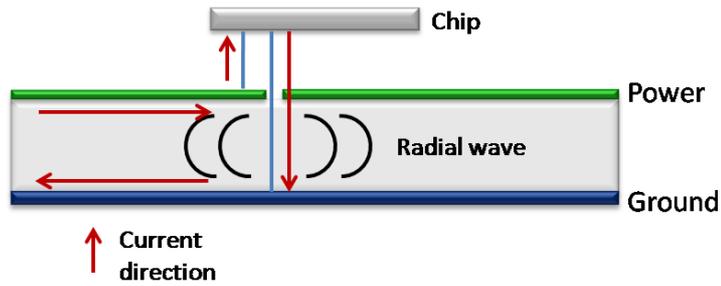
Figure 18. Single Plane-Pair Problem.
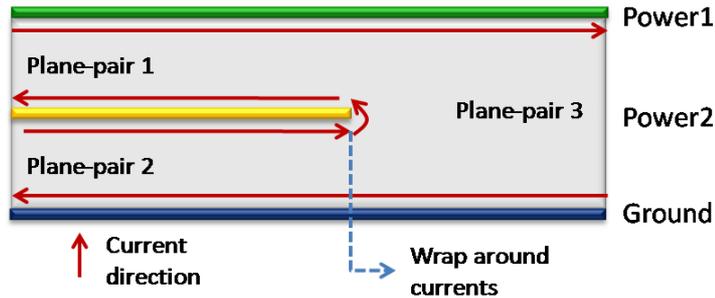
Figure 19. Multiple Plane-Pair Problem.

be modeled as a current source between the power and ground planes at the location of the power supply pins of the chip. The resulting noise propagates radially in the lateral directions, as shown in Figure 18. Also shown, assuming that the voltage regulator module (VRM) is connected to the left side of the cross-section, is the path of the current on the power plane and the corresponding return current on the ground plane.

2.1.2 Multiple Plane-Pair

Noise coupling occurs in the lateral directions in a single plane-pair structure. However, in a multilayered structure, like the example shown in Figure 19, there can be noise coupling in both the horizontal and vertical directions through the power/ground planes. Such a structure consists of multiple plane-pairs. The vertical coupling can then be considered as a coupling between these plane-pairs. Assuming a well developed skin effect, the vertical coupling through the conductors can be neglected. The major vertical coupling occurs through the interactions between these plane pairs at

their boundaries. This coupling mechanism can be described as the aperture coupling or the coupling due to the wrap-around currents as described in the following example.

For the 1D-example in Figure 19, the right half of the middle plane has been removed. For this example, there are three plane-pairs based on different combinations of the planes. Assume that there is a current on the middle plane with its return current on the bottom plane. These currents are confined inside the plane-pair 2 as shown in the figure. When this current arrives the right boundary of this plane pair, it can wrap-around the aperture. Hence this so-called wrap-around current can excite currents in plane-pair 1 and plane-pair 3 as shown in the figure. This is a direct current coupling path between the plane pairs and is critical for accurate estimation of coupling in multilayered planes.

The rest of this chapter is organized as follows. The formulation for the solution of the single plane-pair problem using the method of finite differences is provide in 2.2.

2.2 Formulation for Single Plane-Pair Geometries
2.2.1 Governing Equation

The voltage fluctuation that characterizes SSN propagates as a radial wave in a single plane-pair geometry. Thus, the underlying elliptic partial differential equation for the modeling of planes is a Helmholtz equation

$$\left(\nabla_t^2 + k^2\right) u = -j\omega\mu d J_z \tag{33}$$

where ∇_t^2 is the transverse Laplace operator parallel to the planar structures, k is the wave number, u is the voltage, ω is the angular frequency, μ is the permeability, d is the distance between the planes, and J_z is the current density injected normally to the planes [22].

The periphery of the plane-pair are typically left open. Hence, ignoring fringing
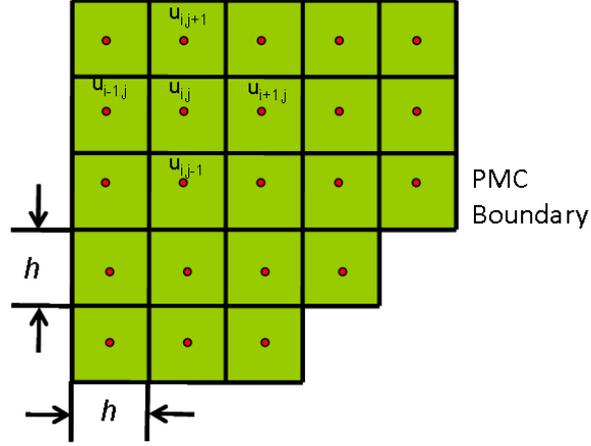
Figure 20. Discretization of the Laplace operator.

fields, the problem definition is completed by assigning homogenous Neumann boundary conditions, which correspond to assuming a magnetic wall, or an open circuit, on the periphery of the planes.

2.2.2 Application of the Finite Difference Method

One method to solve the Helmholtz equation is by applying the finite-difference scheme. The 2-dimensional Laplace operator can be approximated as

$$\nabla_t^2 u_{i,j} = \frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{h^2} \qquad (34)$$

where h is the mesh length and $u_{i,j}$ is the voltage at node (i,j) for the cell-centered discretization shown in Figure 20.

This discretization results in a well-known bedspring unit cell model [23] for a plane-pair consisting of inductors (L) between neighboring nodes, and capacitors (C) from each node to ground, as shown below:

$$\frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{h^2} + k^2 u_{i,j} = -j\omega\mu d J_z \qquad (35)$$

Applying $k = \omega\sqrt{\mu\varepsilon}$ and multiplying throughout by $\frac{h^2}{j\omega\mu d}$, we have,

$$\frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{j\omega\mu d} - j\omega\varepsilon\frac{h^2}{d}u_{i,j} = -h^2 J_z \qquad (36)$$

37
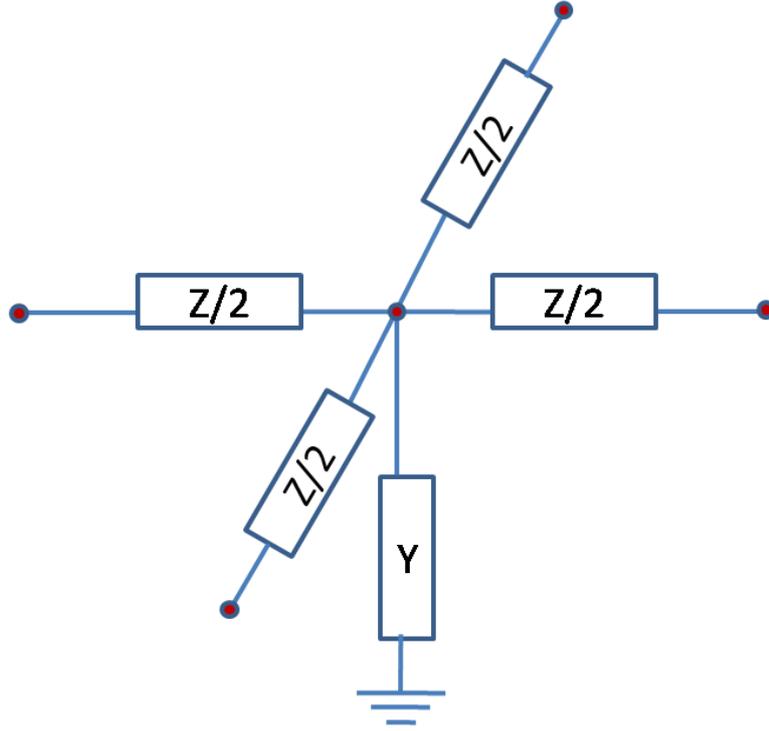
Figure 21. Unit-cell model using 5-Point Approximation (T-Unit cell).

Setting, $\mu d = L$ and $\varepsilon \frac{h^2}{d} = C$, we have the Kirchoff's current law

$$\frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{j\omega L} - j\omega C u_{i,j} + I = 0 \tag{37}$$

where I is the value of the current source placed at location (i, j). The above equations are equivalent to using a 5-point stencil function to approximate the Laplacian.

2.2.3 5- and 9- Point Approximations

The Laplacian in (34) can be represented in its stencil form as follows

$$\nabla_t^2 = \frac{1}{h^2} \begin{bmatrix} & 1 & \\ 1 & -4 & 1 \\ & 1 & \end{bmatrix} \tag{38}$$

The 5-point approximation can be represented as an equivalent circuit for each unit-cell, as shown in Figure 21. The resultant equivalent circuit is called the T-unit cell. Note that the impedances shown in the unit-cells are half of the total impedances

between two neighboring nodes. When unit cells are connected with each other, two half impedances from neighboring unit cells establish the correct impedance value. In the figure, the per unit cell impedance and admittance are represented as

$$Z = R + j\omega L \tag{39}$$

$$Y = G + j\omega C \tag{40}$$

where,

$$C = \varepsilon\frac{h^2}{d} \tag{41}$$

$$L = \mu d \tag{42}$$

$$R = \frac{2}{\sigma t} + 2\sqrt{\frac{j\omega\mu}{\sigma}} \tag{43}$$

$$G = \omega C \tan\delta \tag{44}$$

for a given permittivity ε, permeability μ, conductivity σ, conductor thickness t, loss tangent $\tan\delta$, and cell size h. Note that R in (43) represents the internal impedance, including both the dc and the skin effect resistance, as well as the contribution of the internal inductance.

Another finite-difference approximation that can be applied is the 9-point stencil form, which leads to the X-unit cell, shown in Figure 22. The 9-point stencil form of the Laplacian can be written as:

$$\nabla_t^2 = \frac{1}{h^2}\begin{bmatrix} \frac{1}{6} & \frac{2}{3} & \frac{1}{6} \\ \frac{2}{3} & -\frac{10}{3} & \frac{2}{3} \\ \frac{1}{6} & \frac{2}{3} & \frac{1}{6} \end{bmatrix} \tag{45}$$

The main difference between the T- and X-unit cells, is that the X-unit cell includes a direct inductive path to the diagonally neighboring cells in addition to the neighboring cells sharing a side. Note that the impedances shown in the unit-cells are half of the total impedances between two neighboring nodes. In this thesis, the T-unit cells have been used for the following two reasons.
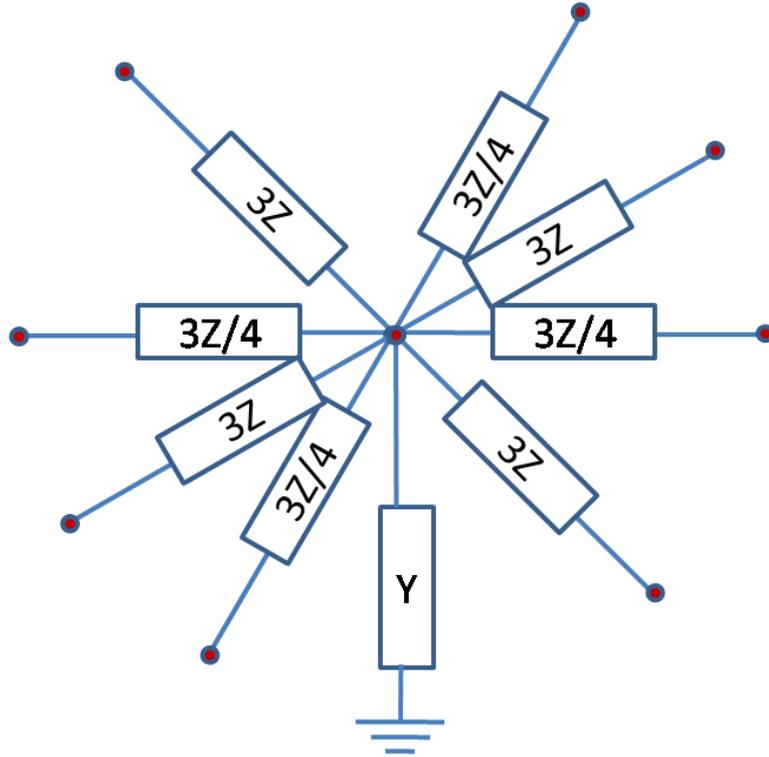
Figure 22. Unit-cell model using 9-Point Approximation (X-Unit cell).

1. The T- and X-unit cells are both derived from a second-order finite difference approximation of the Laplacian operator. As shown in [24], the difference in accuracy between the T- and X- unit cells is not significant.

2. The T-unit cell is simpler to implement.

2.2.4   Equivalent Circuit and Matrix Equation

Representing the unit-cells in a discretized single plane-pair problem in terms of T-unit cells allows the extraction of equivalent circuit such as the one shown in Figure 23.

This equivalent circuit model can be solved using a standard circuit solver based on the modified nodal analysis (MNA) approach[19]. However, direct solution of the finite difference equations using a linear equation solver can improve the memory requirements and speed, since the resulting admittance matrix is a sparse banded matrix. Based on the plane model in Figure 23, a linear equation system can be
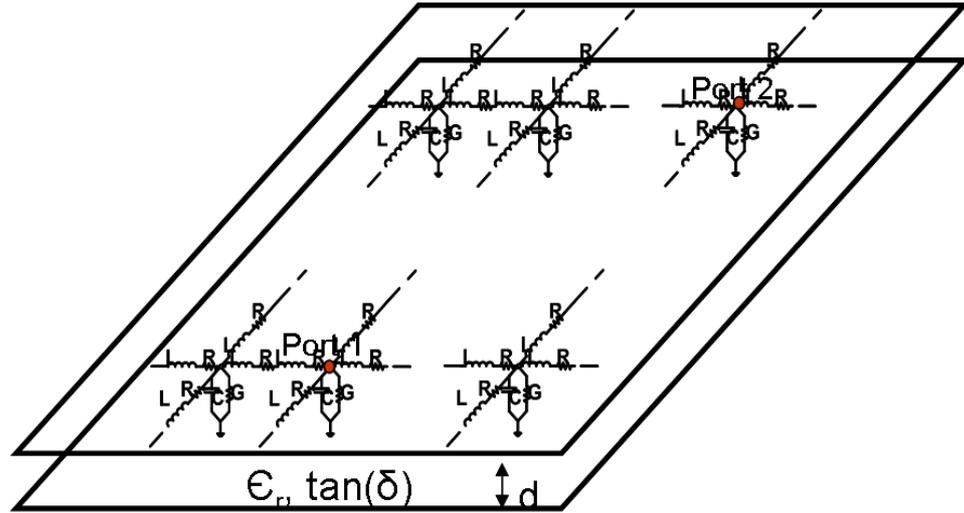
Figure 23. Electrical model for a plane-pair.

obtained which can be written in matrix form as:

$$\overline{\overline{\mathbf{Y}}}\bar{U} = \bar{I} \tag{46}$$

where $\bar{U}$ and $\bar{I}$ are the cell voltage and current vectors. The matrix $\overline{\overline{\mathbf{Y}}}$ is the nodal admittance matrix. If the unit cells are numbered using natural ordering, $\overline{\overline{\mathbf{Y}}}$ has the following form:

$$\overline{\overline{\mathbf{Y}}} = \begin{pmatrix} \bar{\bar{A}} & \bar{\bar{B}} & & & \\ \bar{\bar{B}} & \bar{\bar{A}} - \bar{\bar{B}} & \bar{\bar{B}} & & \\ & \bar{\bar{B}} & \ddots & \ddots & \\ & & \ddots & \ddots & \bar{\bar{B}} \\ & & & \bar{\bar{B}} & \bar{\bar{A}} \end{pmatrix} \tag{47}$$

where $\bar{\bar{A}} =$

$$
\begin{pmatrix}
Y_{uc} + 2Z_{uc}^{-1} & -Z_{uc}^{-1} & & & & & \\
-Z_{uc}^{-1} & Y_{uc} + 3Z_{uc}^{-1} & -Z_{uc}^{-1} & & & & \\
& -Z_{uc}^{-1} & Y_{uc} + 3Z_{uc}^{-1} & \ddots & & & \\
& & \ddots & \ddots & -Z_{uc}^{-1} & & \\
& & & -Z_{uc}^{-1} & Y_{uc} + 3Z_{uc}^{-1} & -Z_{uc}^{-1} & \\
& & & & -Z_{uc}^{-1} & Y_{uc} + 2Z_{uc}^{-1} &
\end{pmatrix}
\tag{48}
$$

and

$$
\bar{\bar{B}} =
\begin{pmatrix}
-Z_{uc}^{-1} & & \\
& \ddots & \\
& & -Z_{uc}^{-1}
\end{pmatrix}
\tag{49}
$$

Y_{uc} and Z_{uc} are the unit cell admittance and inductance terms, defined earlier in (40) and (39), respectively.

2.2.5 Computational Complexity

If the plane pair were to be discretized with M_1 cells horizontally and M_2 cells vertically, then the matrices $\bar{\bar{A}}$ and $\bar{\bar{B}}$ are of order $M_2 \times M_2$ and $\bar{\bar{\bar{Y}}}$ is $N \times N$ where $N = M_1 M_2$. If unit cells are numbered along columns, the bandwidth of $\bar{\bar{\bar{Y}}}$ is M_2. Using a direct solver, the computational complexity for equation 46 is $O(N \times M_2^2)$. For typical geometries, $M_1 \approx M_2 \approx \sqrt{N}$, resulting in a complexity of $O(N^2)$. Also, if sparse storage is used, memory required is $O(N^{1.5})$. The method can be further enhanced by the use of nested dissection, which is an asymptotically optimal node ordering method. This can improve the flop count to $O(N^{1.5})$ and memory to $O(N \log_2 \sqrt{N})$ [13].

2.2.6 Results

The finite difference method described in this chapter for the modeling of two layer geometries was implemented in a tool called Panswitch. The code was developed in

Figure 24. Geometry of test case.

Visual C++ and used the Intel math kernel library (MKL) for the linear equation solution.

The MKL library uses the PARDISO [25][26] linear equation solver. PARDISO is a robust thread safe parallel direct solver, and enables multi-threading.

The test case used to demonstrate the accuracy of the single plane pair formulation is a simple 2-layer 100 mm × 100 mm structure, with a 0.2 mm thick FR-4 dielectric separating the plates.

The structure is shown in Figure 24. The ports are located at the center of opposing edges. The structure was meshed using 10 mm, 5 mm, 2.5 mm and 0.5 mm meshes. It is expected that the impedance parameters Z_{11} and Z_{21} converge with increasing mesh refinement. This is substantiated by the self and transfer impedance plots shown in Figures 25 and 26 respectively. Also,the results have been compared with a commercial FEM-based simulation tool, which shows good agreement.

The structure in Figure 24 is one for which analytical calculation of the resonance frequencies is possible. The resonance frequencies of the $(m, n)^{th}$ TM-mode is given by:

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{50}$$

43
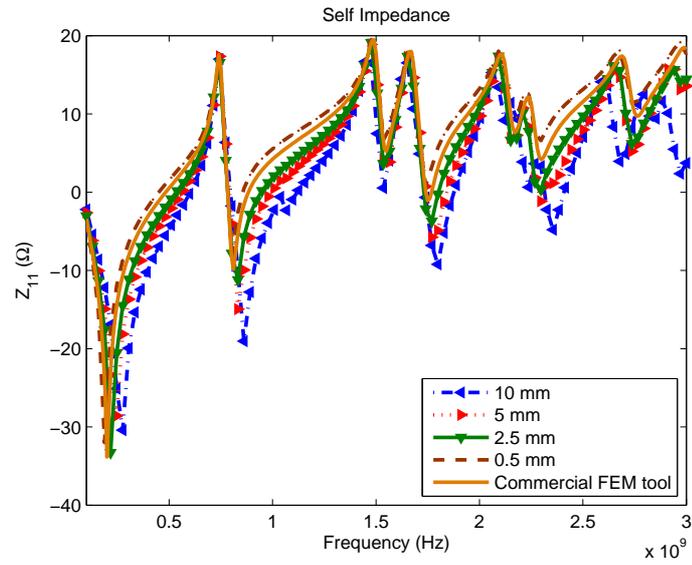
Figure 25. Self impedance, Z_{11}, with increasing mesh refinement.
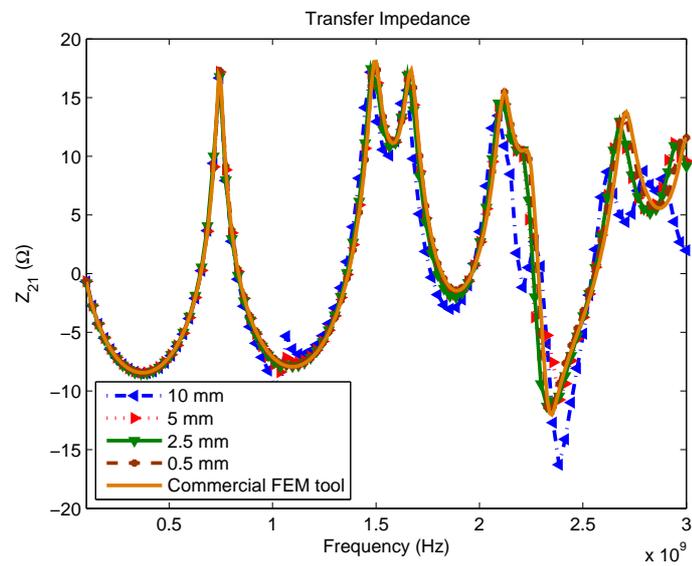
Figure 26. Transfer impedance, Z_{21}, with increasing mesh refinement.

44

Table 1. Theoretical and calculated resonance frequencies.

Mode	Theoretical (GHz)	Calculated (GHz)
$f_{10} = f_{01}$	0.74949	0.74
f_{11}	1.06	1.06
$f_{20} = f_{02}$	1.499	1.50
$f_{21} = f_{12}$	1.6759	1.67

Using $a = b = 100$ mm, the values of the first few resonance frequencies are tabulated in Table 1. There is good agreement between the theoretical and the numerically calculated values.
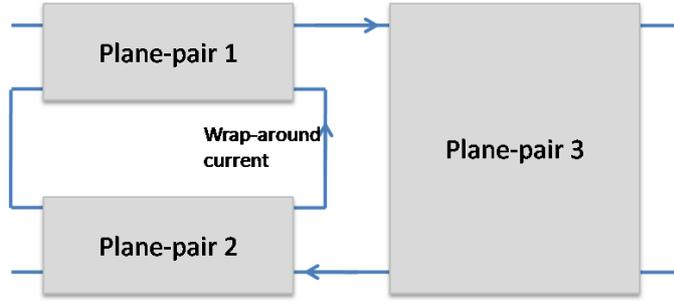
Figure 27. Equivalent network model of geometry in Figure 19.

2.3 Formulation for Multiple Plane-Pair Geometries

2.3.1 Aperture Coupling

The problem posed by the presence of apertures in multiple plane-pair geometries is illustrated in Figure 19, and was discussed briefly in Section 2.1.2. The vertical coupling of SSN can be described in terms of coupling as a result of interactions at the boundaries of the multiple plane-pairs formed due to the presence of apertures. The mechanism of coupling can be described in terms of wrap-around currents.

An equivalent model for such a problem can be developed by individually modeling each of the plane-pairs in the problem, and interconnecting them as shown in Figure 27. In this example, the network model for the 1D geometry in Figure 19 is built on a combination of three plane-pairs, which are formed between the three layers. This network model enforces the correct boundary conditions such that the wrap-around currents are taken into account. Since it is assumed that the electric-field has only one component (in the vertical direction, or direction of stacking), the fringing fields at the aperture are neglected, for the moment. The following sections will focus on a practical implementation of the model shown in Figure 27, using the finite difference scheme discussed earlier.

2.3.2 Formulation

The T-unitcell model of a single plane-pair geometry is shown in Figure 28(a). This model uses a common ground node. In a multilayered structure consisting of more
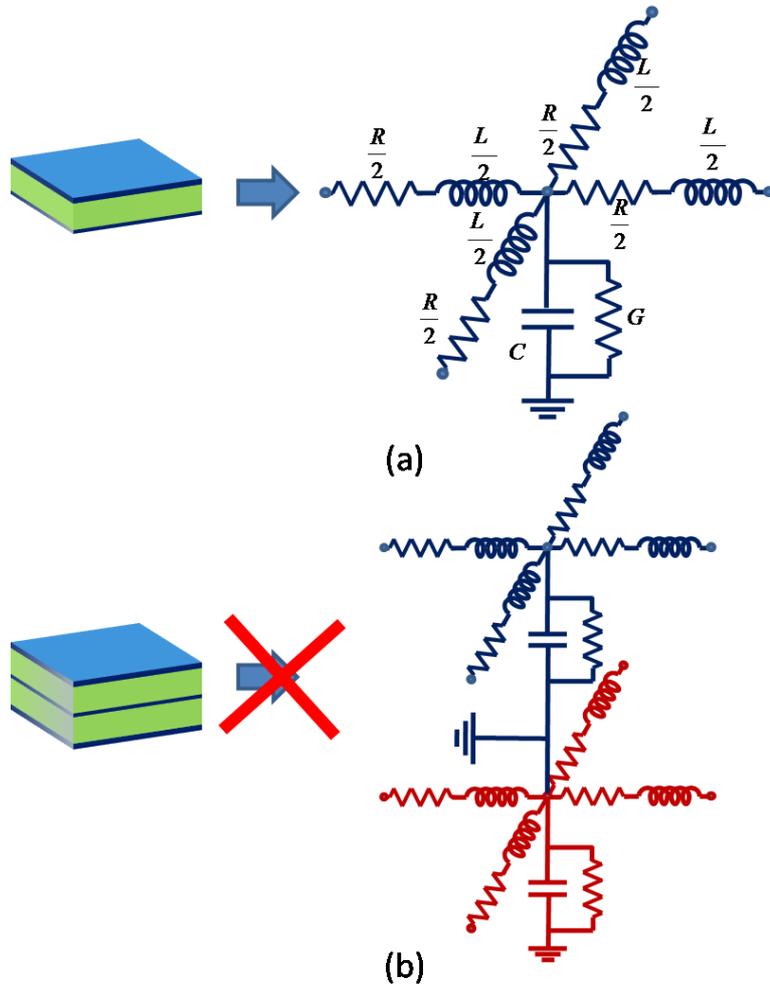
Figure 28. (a) T-unit cell for single plane-pair (b) Incorrect model for multiple plane-pairs based on stacking of individual T-unit cells.
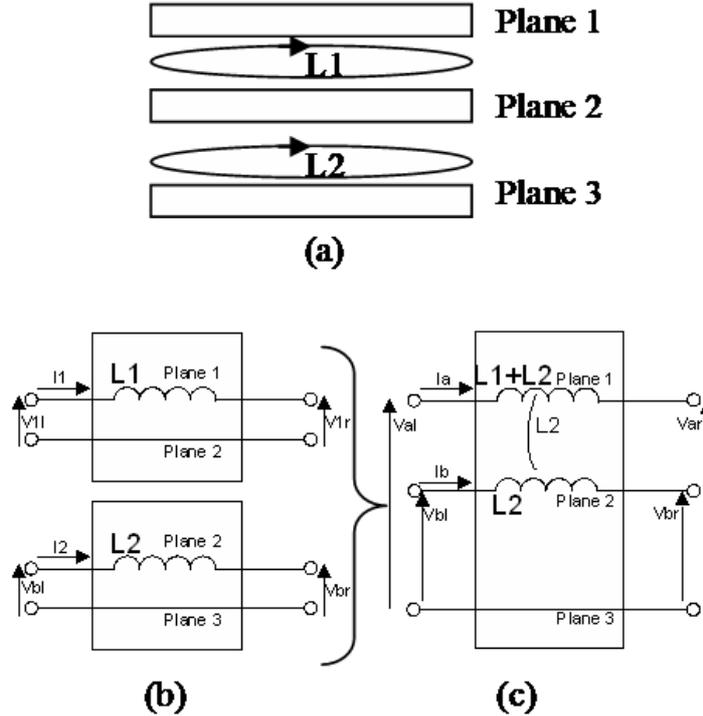
Figure 29. (a) Side view of a unit cell for a 3 plane structure showing the current loops associated with the p.u.c. inductances. (b) P.u.c. inductance of each plane pair. (c) Combining the p.u.c. inductances by changing the reference planes.

than two planes, unit cells of different plane pairs can assign this ground potential to different planes. Therefore, such unit cells cannot be stacked on top of each other without any modification to model a multilayered plane. A straightforward stacking, shown in Figure 28(b) would short-circuit the elements between two ground connections, resulting in a completely erroneous model.

2.3.2.1 Reference Node Assignment

Consider the unit-cell for a 3-layer structure. In the two plane-pairs (shown in Figuure 29(a)) that constitute this structure, it can be observed that when the excitation is confined within each plane-pair, the currents also form a loop. For example, a current flowing in the top layer return on the middle layer, while a current flowing in the middle layer returns on the bottom. This is simply another means of modeling the electric field confinement within a plane-pair.

To obtain a model for the combined unit cell representing all the planes in the structure, consider the inductor elements in a unit cell as shown in Figure 29(a). L1 is the per unit cell (p.u.c.) inductance between plane 1 and plane 2, whereas L2 is the inductance between plane 2 and 3. Hence, reference planes are different in both models in Figure 29(b) and L2 would be short-circuited if the same nodes on plane 2 were connected with each other. In order to avoid that, the p.u.c. inductances can be combined as shown in Figure 29(c) using a mutual inductance and assigning plane 3 as the reference plane. This model can be extended in a similar way to any number of planes. Physically, this model is based on the fact that there is a complete coupling of the magnetic field when the return current is on plane 3, as represented by the mutual inductance that is equal to L2.

This can be seen by calculating the per-unit-length inductance for the 3 plane structure, with the bottom layer assigned as the reference conductor. The capacitance in vacuum, for 3 planes of width w and spacing between planes d_1 and d_2, ignoring fringing fields is:

$$\overline{\overline{C}}_v = \varepsilon_0 \begin{pmatrix} \frac{w}{d_1} & -\frac{w}{d_1} \\ -\frac{w}{d_1} & \frac{w}{d_1} + \frac{w}{d_2} \end{pmatrix} \tag{51}$$

The inductance matrix can therefore be calculated as

$$\overline{\overline{L}} = \mu_0 \varepsilon_0 \overline{\overline{C}}_v^{-1} \tag{52}$$

$$= \mu_0 \begin{pmatrix} \frac{d_1+d_2}{w} & \frac{d_2}{w} \\ \frac{d_2}{w} & \frac{d_2}{w} \end{pmatrix} \tag{53}$$

Interestingly, this model can also be derived using the reference node assignment principle, discussed in Section 1.6.

Figure 30 is reproduced here for convenience. Recalling that the combined four-port admittance matrix, $\overline{\overline{Y}}$, for the 2 two-ports Y^A and Y^B in the figure is given
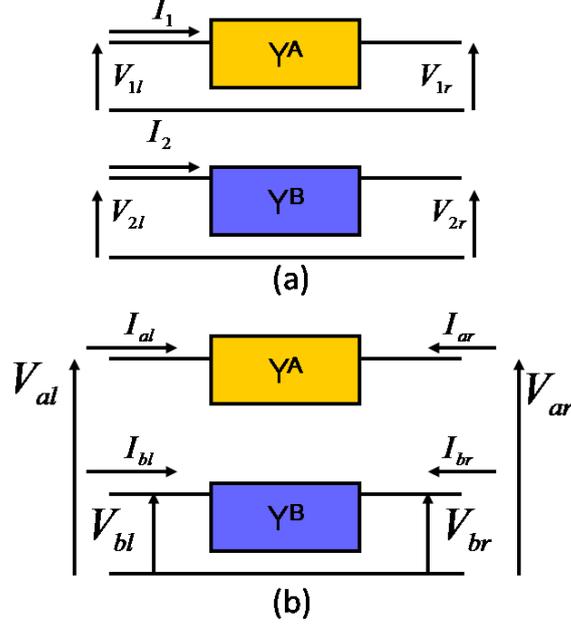
Figure 30. (a) Two-port networks with separate references (b) Combined four-port network with common reference.

by:

$$\overline{\overline{Y}} = \begin{pmatrix} Y^A & -Y^A \\ -Y^A & Y^A + Y^B \end{pmatrix} \tag{54}$$

Substituting for Y^A and Y^B

$$Y^A = \frac{1}{j\omega} \begin{pmatrix} \frac{1}{L_1} & -\frac{1}{L_1} \\ -\frac{1}{L_1} & \frac{1}{L_1} \end{pmatrix} \tag{55}$$

$$Y^B = \frac{1}{j\omega} \begin{pmatrix} \frac{1}{L_2} & -\frac{1}{L_2} \\ -\frac{1}{L_2} & \frac{1}{L_2} \end{pmatrix} \tag{56}$$

$$\tag{57}$$

Since L_1 and L_2 are the loop inductances of plane-pairs 1 and 2, respectively,

$$L_1 = \mu_0 \frac{d_1}{w} \tag{58}$$

$$L_2 = \mu_0 \frac{d_2}{w} \tag{59}$$

50

Substituting (58) and (59) in (55) and (56), (54) becomes

$$\overline{\overline{Y}} = \frac{1}{j\omega} \begin{pmatrix} \overline{\overline{L}}^{-1} & -\overline{\overline{L}}^{-1} \\ -\overline{\overline{L}}^{-1} & \overline{\overline{L}}^{-1} \end{pmatrix} \tag{60}$$

where $\overline{\overline{L}}$ is defined in (53).

2.3.3 Equivalent Circuit and Matrix Equation
2.3.3.1 Without Apertures

The total unit cell can be obtained as shown in Figure 31(b) for the example of three planes, where the bottom plane is chosen as the voltage reference plane. The equivalent circuit that would be obtained for a three layer geometry is shown in Figure 31(c).

2.3.3.2 With Apertures

An example for the equivalent circuit obtained from M-FDM when the structure to be modeled contains apertures is illustrated in Figure 32(a).

This is the same example with which the multiple plane-pair problem was introduced, in Figure 19. The equivalent circuit for this case is shown in Figure 32(b).

2.3.3.3 Matrix Equation

For solid multilayered rectangular planes, discretized with M_1 cells in the x-direction and with M_2 cells in the y-direction, the admittance matrix $\overline{\overline{Y}}$ can be written as

$$\overline{\overline{Y}} = \begin{pmatrix} \bar{\bar{A}} & \bar{\bar{B}} & & & \\ \bar{\bar{B}} & \bar{\bar{A}} - \bar{\bar{B}} & \bar{\bar{B}} & & \\ & \bar{\bar{B}} & \ddots & \ddots & \\ & & \ddots & \ddots & \bar{\bar{B}} \\ & & & \bar{\bar{B}} & \bar{\bar{A}} \end{pmatrix} \tag{61}$$

where $\bar{\bar{A}} =$

$$L_1 = \mu d_1 / 2, \quad C_1 = \varepsilon_1 \frac{h^2}{d_1}$$

$$L_2 = \mu d_2 / 2, \quad C_2 = \varepsilon_2 \frac{h^2}{d_2}$$

R_1, R_2, G_1, G_2 are the conductor and substrate losses at a given frequency

(a)   (b)

Figure 31. (a) Geometry and p.u.c. parameters. (b) Combined unit cell model for three planes. (c) Plane model consisting of multilayer unit cells.
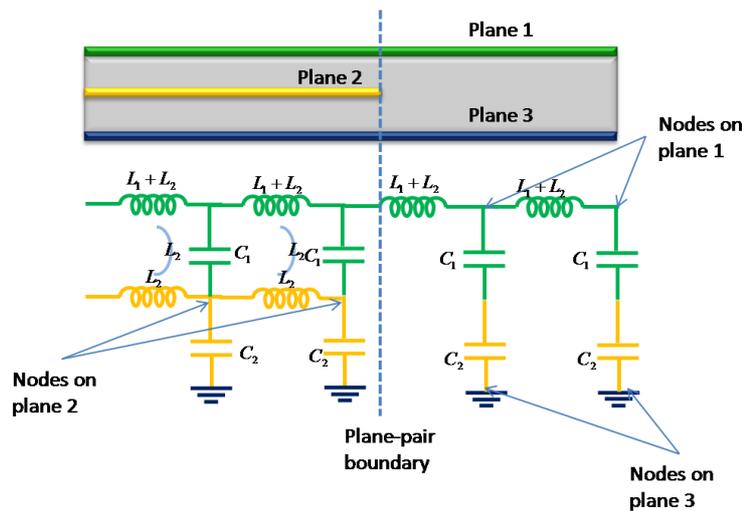
Figure 32. (a) Multiple plane-pair problem containing apertures. (b) 1D Equivalent Circuit.

52

$$
\begin{pmatrix}
\bar{\bar{Y}}_{uc} + 2\bar{\bar{Z}}_{uc}^{-1} & -\bar{\bar{Z}}_{uc}^{-1} \\
-\bar{\bar{Z}}_{uc}^{-1} & \bar{\bar{Y}}_{uc} + 3\bar{\bar{Z}}_{uc}^{-1} & -\bar{\bar{Z}}_{uc}^{-1} \\
& -\bar{\bar{Z}}_{uc}^{-1} & \bar{\bar{Y}}_{uc} + 3\bar{\bar{Z}}_{uc}^{-1} & \ddots \\
& & \ddots & \ddots & -\bar{\bar{Z}}_{uc}^{-1} \\
& & & -\bar{\bar{Z}}_{uc}^{-1} & \bar{\bar{Y}}_{uc} + 3\bar{\bar{Z}}_{uc}^{-1} & -\bar{\bar{Z}}_{uc}^{-1} \\
& & & & -\bar{\bar{Z}}_{uc}^{-1} & \bar{\bar{Y}}_{uc} + 2\bar{\bar{Z}}_{uc}^{-1}
\end{pmatrix} \tag{62}
$$

and

$$
\bar{\bar{B}} = \begin{pmatrix}
-\bar{\bar{Z}}_{uc}^{-1} \\
& \ddots \\
& & -\bar{\bar{Z}}_{uc}^{-1}
\end{pmatrix} \tag{63}
$$

Here, A and B are $kM_1 \times kM_1$ matrices for $(k+1)$ planes, assuming that the nodes are numbered starting from the top node in the lowest row, increasing in the vertical direction to the bottom node, then starting with the next cell in the x-direction until the last cell, and then starting with the next row. Hence, $\bar{\bar{\mathbf{Y}}}$ is a $(kM_1M_2) \times (kM_1M_2)$ matrix. The unit cell matrices, $\bar{\bar{Y}}_{uc}$ and $\bar{\bar{Z}}_{uc}^{-1}$ are tri-diagonal and are given by

$$
\bar{\bar{Y}}_{uc} = \begin{pmatrix}
Y_1 & -Y_1 \\
-Y_1 & Y_1 + Y_2 & -Y_2 \\
& -Y_2 & \ddots & \ddots \\
& & \ddots & \ddots & -Y_{k-2} \\
& & & -Y_k - 2\ Y_{k-2} + Y_{k-1} & -Y_{k-1} \\
& & & & -Y_{k-1} & Y_{k-1} + Y_k
\end{pmatrix} \tag{64}
$$

and

$$\bar{\bar{Z}}_{uc}^{-1} = \begin{pmatrix} \frac{1}{Z_1} & -\frac{1}{Z_1} & & & & & \\ -\frac{1}{Z_1} & \frac{1}{Z_1} + \frac{1}{Z_2} & -\frac{1}{Z_2} & & & & \\ & -\frac{1}{Z_2} & \ddots & \ddots & & & \\ & & \ddots & \ddots & -\frac{1}{Z_{k-2}} & & \\ & & & -\frac{1}{Z_{k-2}} & \frac{1}{Z_{k-2}} + \frac{1}{Z_{k-1}} & -\frac{1}{Z_{k-1}} & \\ & & & & -\frac{1}{Z_{k-1}} & \frac{1}{Z_{k-1}} + \frac{1}{Z_k} \end{pmatrix} \quad (65)$$

where Y_i and Z_i can be obtained similar to the unit cell parameters for a single plane pair structure as

$$Y_i = j\omega C_i + \omega C_i \tan \delta_i \quad (66)$$

$$Z_i = j\omega L_i + \frac{2}{\sigma t} + 2\sqrt{\frac{j\omega\mu}{\sigma}} \quad (67)$$

By an analysis similar to what was provided in the previous section, it can be shown that the computational complexity of M-FDM applied to $k+1$ layers is $O(N^2)$ where $N = (kM_1M_2)$. Using nested dissection [13] improves the flop count to $O(N^{1.5})$ and memory to $O(Nlog_2\sqrt{N})$. Typically in the presence of mutual inductor elements such as what has been shown in Figure 31, the unit cell inductance matrix $\bar{\bar{Z}}_{uc}^{-1}$ will be full-dense. However, the nature of the loop inductances considered lends to the tri-diagonal form shown in (65) and hence to the unique advantages of M-FDM.

2.3.4 Model to Hardware Correlation for Structures with Apertures

The following test cases were designed to demonstrate the capability to model vertical coupling through apertures in the metal planes. The geometries of the test cases are shown in Figures 33 and 36. In either case, the two ports were used to excite two different plane-pairs.

Ideally, if the metal-layers were all solid and contained no holes or apertures, then there will be no coupling between the ports, at the frequencies of interest. This is due

Figure 33. Test vehicle 1 (a) Geometry (b) Stack cross-section.

to the fact that the field penetration depth reduces with frequency. The skin-depth can be expressed as

$$\delta_s = \sqrt{\frac{1}{\pi f \mu \sigma}} \qquad (68)$$

where f is the frequency of operation, μ is the permittivity of the medium and σ is the conductivity of the metallization. At 100 MHz, for copper metallization, the skin-depth is approximately 7 μm (and 2 μm at 1 GHz). In these test cases, the copper used was 30 μm thick. Hence, field penetration will not play a major role over the frequencies of interest.

However, from the insertion loss results shown in Figures 35 and 38, there is significant coupling between ports. This is due to aperture coupling. Also, the results from M-FDM correlate well with simulations from Sonnet and with measurements, as can be seen from the insertion loss results mentioned above, and from the return loss results shown in Figures 34 and 37.

M-FDM required 3 MB of memory and 113.7 ms of simulation time per frequency point for Test vehicle 1, using 1 mm × 1 mm discretization. Using the same cell size, Sonnet required 95s of simulation time per frequency point. This represents a speedup of over 800X for comparable accuracy.
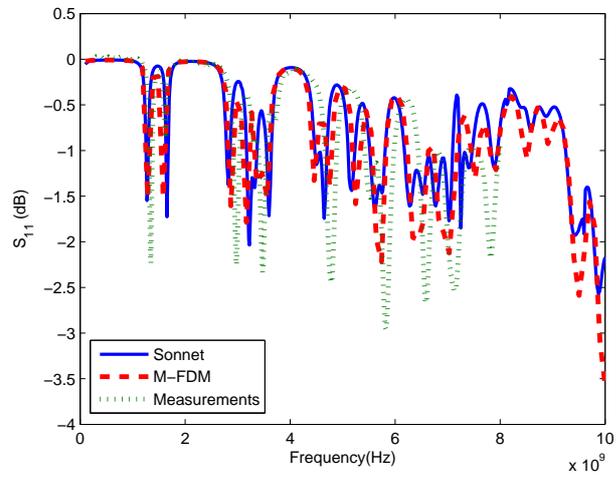
Figure 34. S_{11} (dB) (return loss) for test vehicle 1 (Fig 33).
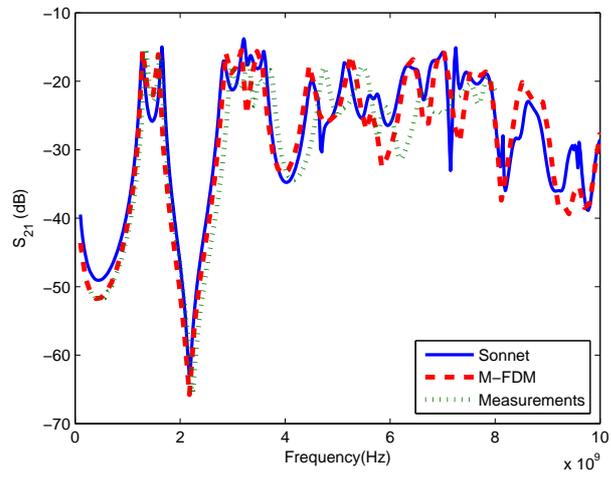
Figure 35. S_{21} (dB) (insertion loss) for test vehicle 1 (Fig 33).

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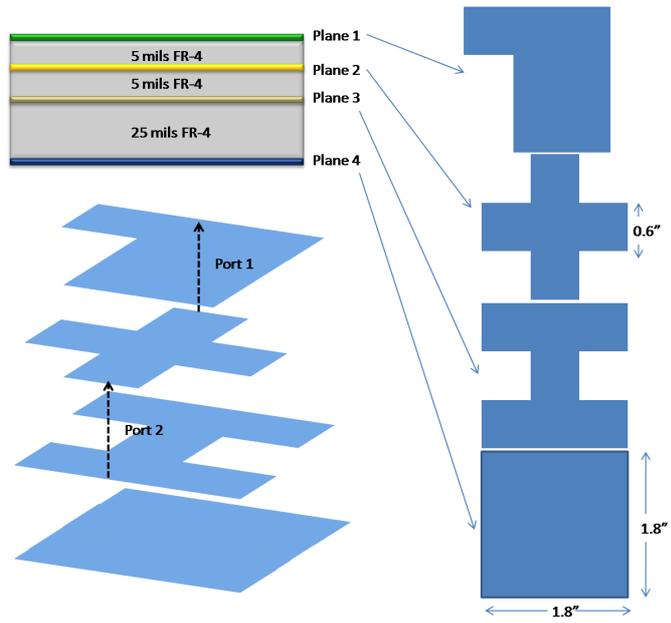
Figure 36. Test vehicle 2 (a) Geometry (b) Stack cross-section.
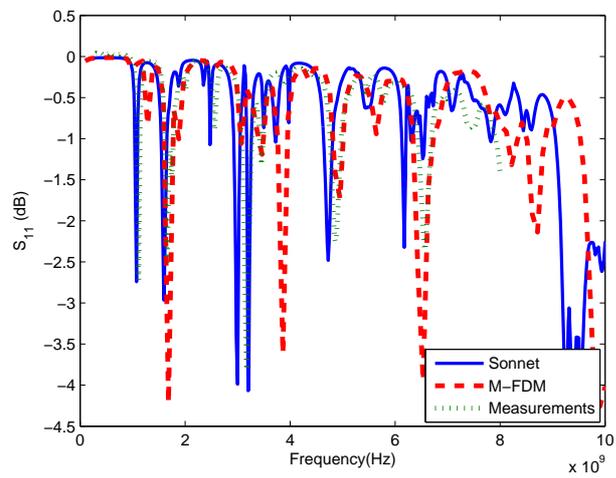
Figure 37. S_{11} (dB) (return loss) for test vehicle 2 (Fig 36).
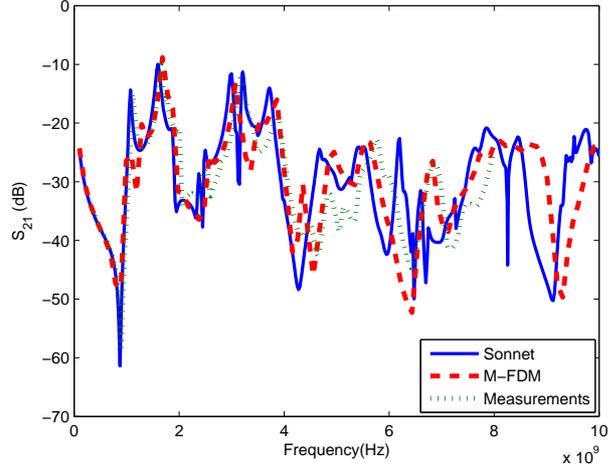
Figure 38. S_{21} (dB) (insertion loss) for test vehicle 2 (Fig 36).

Table 2. Simulation results for realistic package.

Layers	Nodes	Time/Freq Point (s)
2	38, 800	0.93
3	77, 600	1.78
4	116, 400	3.92
5	155, 200	6.8
6	194, 000	10.19
7	232, 800	16.33
8	271, 600	23.56
9	310, 400	32.99
10	349, 200	42.53

2.3.5   Results Demonstrating Scalability

The layout for two of the power distribution layers from a realistic package has been shown in Figure 39(a). The layers were discretized using a unit cell size of 0.185 mm, resulting in 38,800 nodes per layer. Table 2 shows the scalability of the simulation tool as the number of layers, and hence, the number of nodes is increased. By employing a sparse solver with nested dissection, it is possible to simulate a package with ten layers with 349, 200 nodes. For this case, the simulation time/frequency point was 33 s. In comparison, even the simulation of the two layer example was intractable with Sonnet due to insufficient memory available.

Further, consider the three layer case depicted by Figure 39. In this case, if the
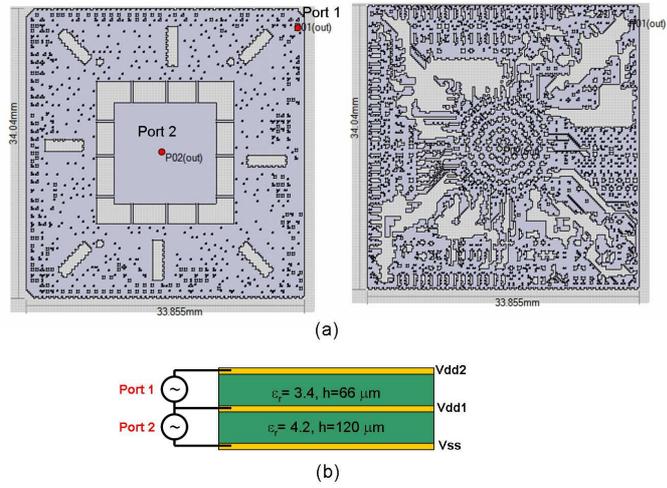
Figure 39. (a) Layouts for two package layers. Dimension is 34mm × 34mm. (b) Cross-section for the three layer example.
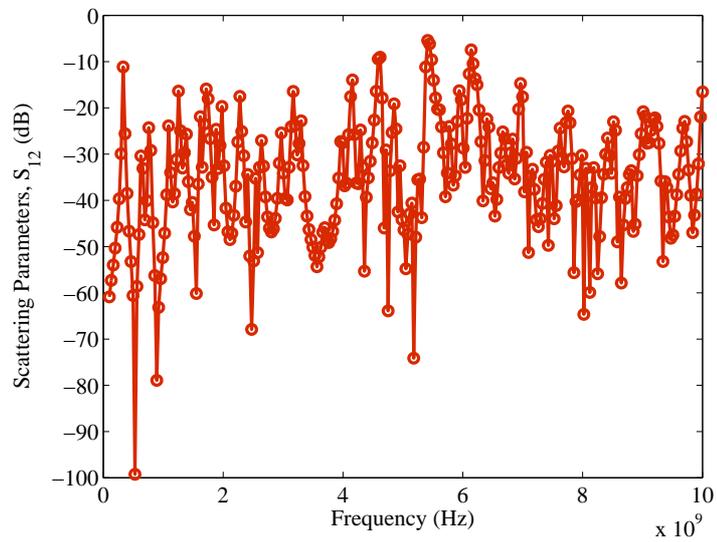
Figure 40. Insertion loss (dB).

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middle layer, Vdd1, were a solid plane, the two ports in the example would be isolated from each other. However, due to the apertures present in these layers, significant coupling can occur between the ports as shown in the insertion loss results shown in Figure 40. In particular, there is significant coupling at 2.4 GHz and 5 GHz (-20 dB). Consider a scenario where Vdd1 and Vdd2 supply power to a digital and an 802.11 transceiver module respectively. In this situation, the designer would have to incorporate decoupling techniques to isolate the ports in order to maintain the performance of the WiFi module. While this problem can be solved with M-FDM, it is intractable in commercial full-wave simulators.

2.4   Conclusions

In this chapter, the formulation for the multi-layer finite difference method (M-FDM) was developed. The formulation was developed by first discussing the finite difference method as applied to single plane-pair structures, using two different discretization schemes (the T- and X- unit cells). The discussion was later confined to the use of the T-unit cell which simplifies implementation without significant loss in accuracy.

The problem of extending this approach to multi-layer geometries was primarily one of handling the boundaries between plane-pairs, which occur due to the presence of apertures in multi-layer packages. This was solved by modeling each plane-pair individually, and later shifting the ground reference nodes to the common system ground, typically designated to be the bottom most layer in the package. This method completes the formulation of M-FDM and allows the modeling of wrap-around currents. Using nested dissection reordering [13] the method requires a flop count to $O(N^{1.5})$ and memory of $O(Nlog_2\sqrt{N})$.

M-FDM does have a couple of limitations. These arise primarily because of the simplifying assumption $\frac{\partial}{\partial z} = 0$, and assuming that the electric field does not have any components in the lateral direction. Physically, this implies that the fringing fields
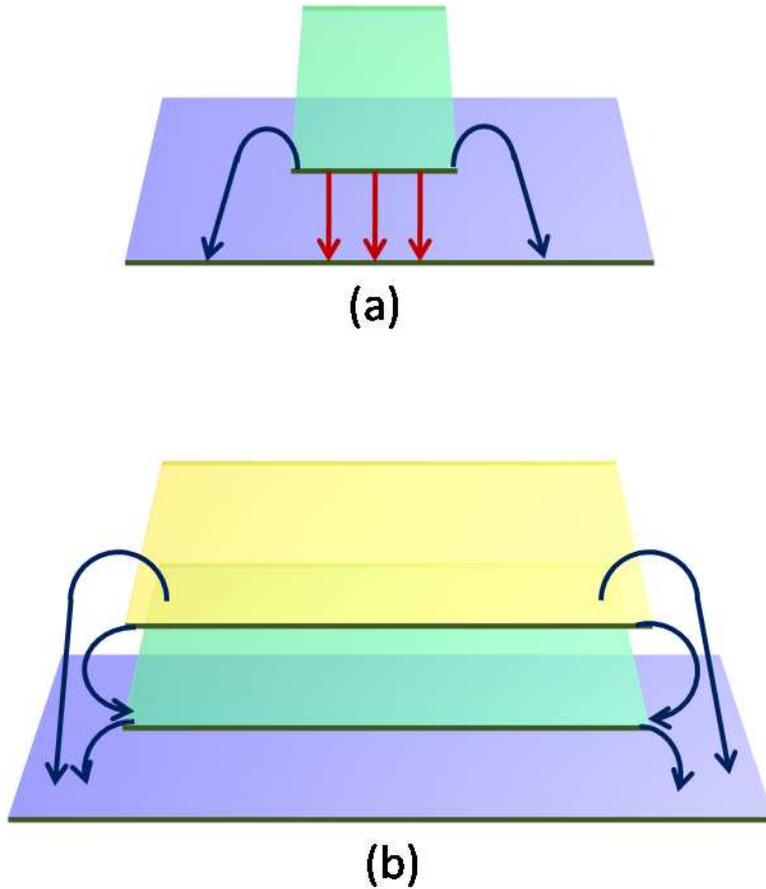
Figure 41. (a) Fringing fields due to narrowing of PDN (b)Fringing fields at edges in multi-layer geoemtries.

are not modeled. These fields are not critical when the ratio of the plane width to dielectric height is greater than 50. However, two situations where these fields cannot be neglected are the following:

1. A plane has a narrow section or a *neck*. This is illustrated in Figure 43(a).

2. In a multiple plane-pair structure, fringing fields at the boundaries of the plane-pairs can cause vertical coupling. This is illustrated in Figure 43(b). This coupling mechanism is typically not as significant as the coupling through wrap-around currents, which are modeled by M-FDM. However, in Figure 43(b), there are no apertures, and hence no wrap-around currents either.

The other critical effect in the context of package and board PDNs is the coupling
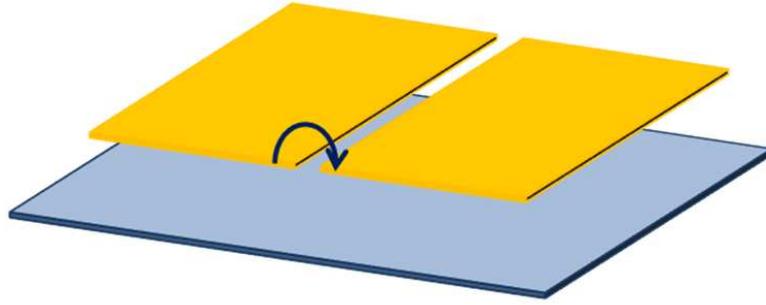
Figure 42. Gap coupling across slots in planes.

of energy across slots in metal planes. Slots are typically used to DC isolate two different supply voltages.

Thus, noise can coupling horizontally across the slots separating power islands, as shown in Figure 42.

The goal of forthcoming chapters is to use equivalent circuits to model the effect of the fringe (Chapter 3) and gap coupling (Chapter 4) fields. These equivalent circuit models are equivalent to updating the system admittance matrix with correction terms.

CHAPTER 3

MODELING OF FRINGING FIELDS IN M-FDM FOR MULTI-LAYERED PACKAGES

3.1 Introduction

The modeling of PDN geometries using techniques that employ the planar-circuit approximation (i.e., $\frac{\partial}{\partial z} = 0, E_x = E_y = 0$) is valid for large plane-pairs, where the ratio of the lateral dimensions of the planes to the dielectric height exceeds 50. However, in many PDNs, the presence of narrow lines (Figure 43(a)) implies that simulation results will be inaccurate. Also, even in the case when metal planes are wide compared to the substrate height, there can be significant coupling that can be associated with the fringing fields from plane edges (Figure 43(b)). This is because, in either case, the fringing fields contain E_x and E_y fields that are significant when compared to E_z. Hence, the planar circuit approximation can lead to unacceptable loss in accuracy.

3.1.1 Significance of the Fringing Fields

The error in ignoring the fringing fields can be illustrated by studying the resonance frequencies of a square plane pair geometry by varying the ratio of plane width W to substrate height h. The results from M-FDM, when compared with results from full-wave solver, can be used to quantify the error introduced by neglecting fringe fields.

In Figure 44, the relative percentage error in the first resonance frequency in S_{11} obtained from M-FDM (as compared to full-wave simulations[9]) are shown. Even for significantly wide planes, $\frac{W}{h} = 10$, the resonance frequency shift is large ($\sim 5.5\%$). Only for very wide planes, i.e. $\frac{W}{h} > 50$, does the error reduce to below 1%. As packages shrink to chip scale dimensions, the fringe effect, therefore, cannot be neglected.

Another example that amplifies the effect of fringing fields is a microstrip meander
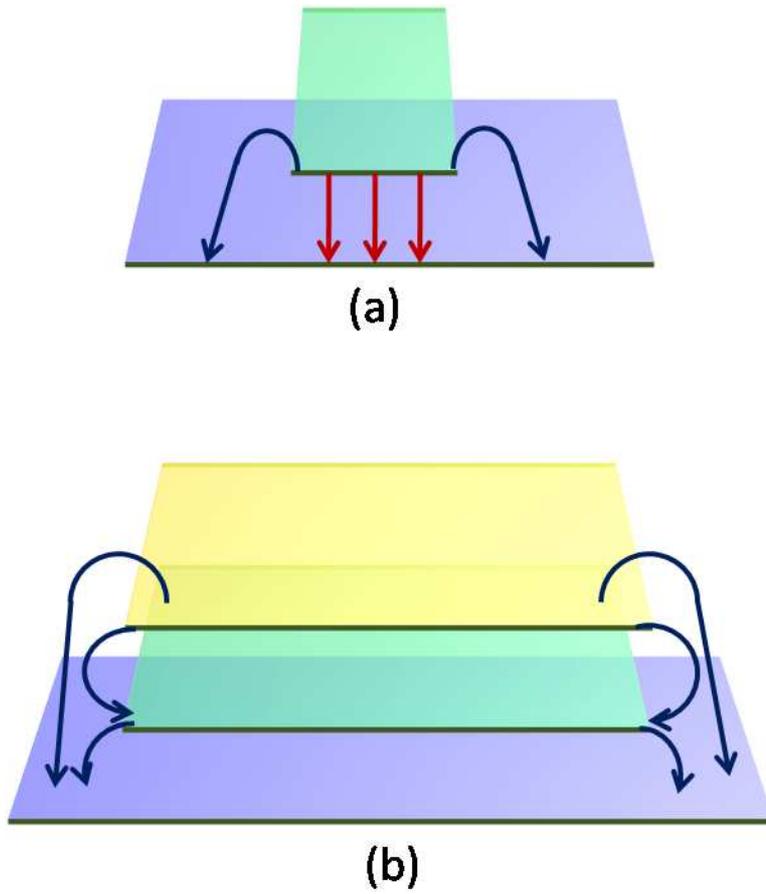
Figure 43. (a) Fringing fields due to narrowing of PDN (b)Fringing fields at edges in multi-layer geoemtries.
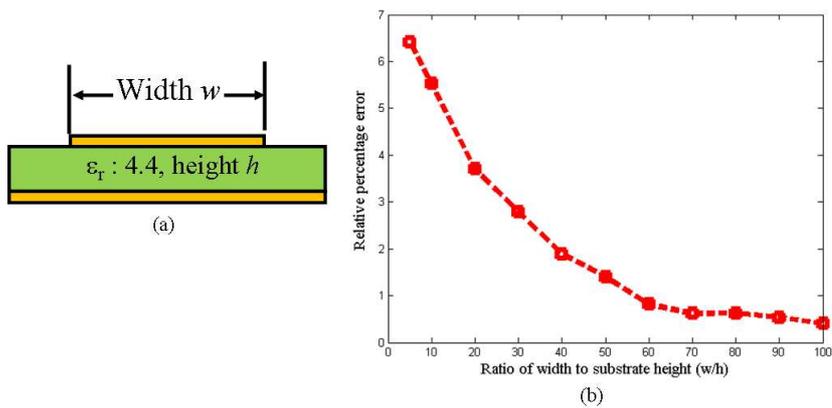
Figure 44. Relative percentage error in first resonance frequency (Return Loss, S_{11}.)
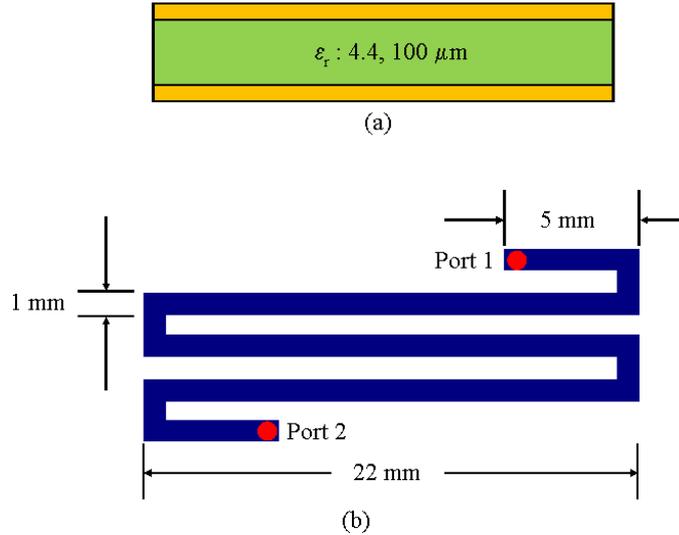
Figure 45. A microstrip meander line, (a) cross section (b) top view.

line, shown in Figure 45. The line width is 1mm and is placed over an FR-4 substrate of thickness 100μm. The return loss of this line, obtained from M-FDM and the full-wave solver Sonnet [9], is shown in Figure 46. Clearly, the M-FDM results show deviations in the resonance frequencies.

3.1.2   Prior Work in Modeling Fringing Fields

This problem has been considered recently in [27], where an extended segmentation approach was proposed. The segmentation approach is coupled with a 2D field solver, such that the effect of discontinuities such as vias can be extracted and included in the simulation. In this chapter, the M-FDM method is modified with a fringe augmentation (FA) technique, where the fringe elements are obtained from a 2D electrostatic solution, which is relatively inexpensive.

The addition of the capacitance and inductance elements associated with the fringe fields in this method is equivalent to modifying the material properties associated with the cells lying on metal edges, as developed in [28] for FDTD meshes. This technique enables the method to accurately characterize irregular multi-layered packages. Thus, the contribution of this work is the development of fringe corrections, for irregular
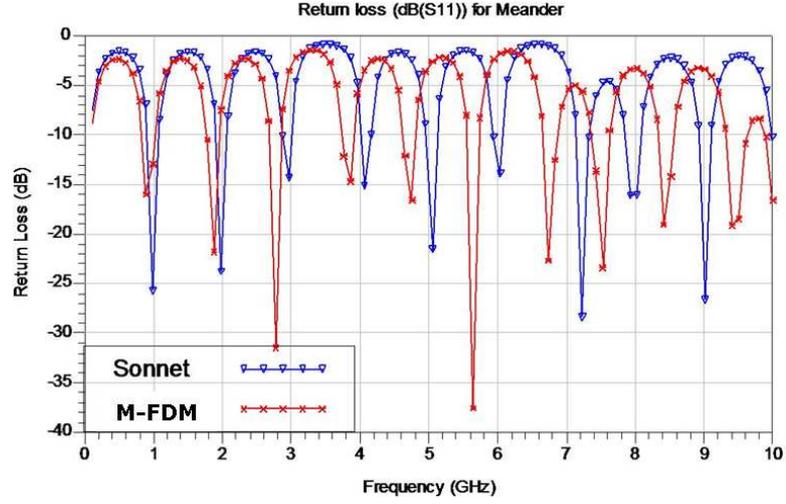
Figure 46. Return Loss (dB) of structure in Figure 45.

and multi-layered packages modeled using M-FDM.

The rest of this chapter is organized as follows. The formulation for obtaining the network model for the fringe augmentation elements is discussed in Section 3.2. In this section, the formulation for the 2D electrostatic solver, and its use to obtain the equivalent circuit model and matrix equations for single plane-pair and multiple plane-pair structures is also developed. The formulation is applied to single and multiple plane-pair geometries in 3.3, and the results from the FA method are compared with full-wave simulations and measurements. Finally, conclusion are presented in Section 3.4.

3.2 Addition of Fringe Elements to M-FDM
3.2.1 Simulation Flow

The effect of the fringing fields can be modeled by the fringe augmentation (FA) method coupled with the M-FDM formulation. The flowchart for the FA+M-FDM method is shown in Figure 47. The process involves the following steps:

1. The package geometry is segmented into cross-sections along each row and column of unit-cells. The cross-sections which are identical are grouped together.

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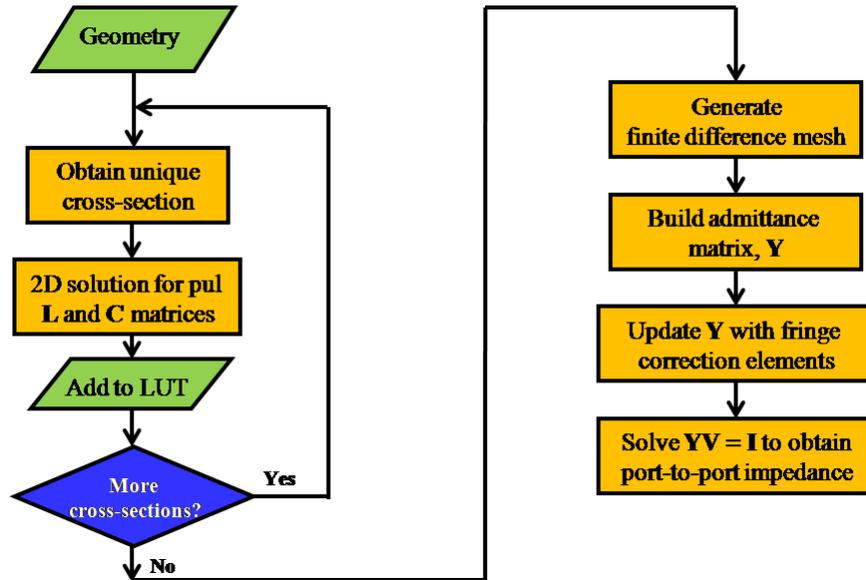
Figure 47. Flowchart for the addition of fringe augmentation elements.

2. Each unique cross-section is analyzed using a 2D electrostatic solver to obtain the per-unit-length (p.u.l) inductance and capacitance matrices, the values of which are stored in a look up table, to be retrieved while building the admittance matrix for the frequency sweep.

3. After pre-computing these p.u.l L and C matrices, M-FDM is applied to build the initial admittance matrix $\overline{\overline{\mathbf{Y}}}$.

4. $\overline{\overline{\mathbf{Y}}}$ is updated with the fringe correction elements that are calculated based on the stored 2D L and C matrices.

5. Equation 46 is solved to obtain the port-to-port impedance parameters as before.

3.2.2   2D Electrostatic Solver

A typical electrostatic problem involves the solution of Laplace's equation in a source free region to obtain the electric potential in the problem domain, Ω.

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Laplace's equation is given in differential form as:

$$\nabla \cdot (\epsilon \nabla u) = 0 \tag{69}$$

Here, u is the electric potential distribution in the dielectric domain where electrostatic fields exist.

In Cartesian coordinates, and in a homogenous medium, the equation becomes

$$\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) u = 0 \tag{70}$$

It is not possible to obtain an analytical solution to the above equation, in general. However a variety of numerical techniques are applicable, and a robust method-of-moments based 2D-solver, CZ2D [30], is commercially available.

A simple finite-element scheme has been used in this thesis. This scheme provides per-unit-length capacitance and high frequency inductance matrices of transmission structures.

The finite-element scheme uses a triangular mesh with N nodes and pyramid basis functions. The pyramid basis is described in Chapter 7.

We obtain and solve the system:

$$\sum_{j=1}^{N} \left(\int_{\Omega} (\epsilon \nabla \Phi_j) \cdot \nabla \Phi_i \right) U_j = 0, \, i, j = 1, 2 ... N \tag{71}$$

where Φ_i is the pyramid basis and U_i is the unknown potential, defined at node i.

The capacitance matrix, $\overline{\overline{C}}_{2D}$, can be obtained by applying Gauss' law:

$$C_{i,j} = \oint_{l_j} \epsilon \frac{\partial V}{\partial n} dl_j \tag{72}$$

where $C_{i,j}$ is the $(i,j)^{th}$ entry in the capacitance matrix, found by integrating the normal component of the potential gradient around a contour l_j enclosing the jth conductor with a 1V potential applied to the ith conductor.

The high frequency inductance matrix, $\overline{\overline{L}}_{2D}$, can be found to be $\sqrt{\mu_0 \epsilon_0} \overline{\overline{C}}_{2D0}^{-1}$, where $\overline{\overline{C}}_{2D0}^{-1}$ is the capacitance matrix of the same structure in vacuum.
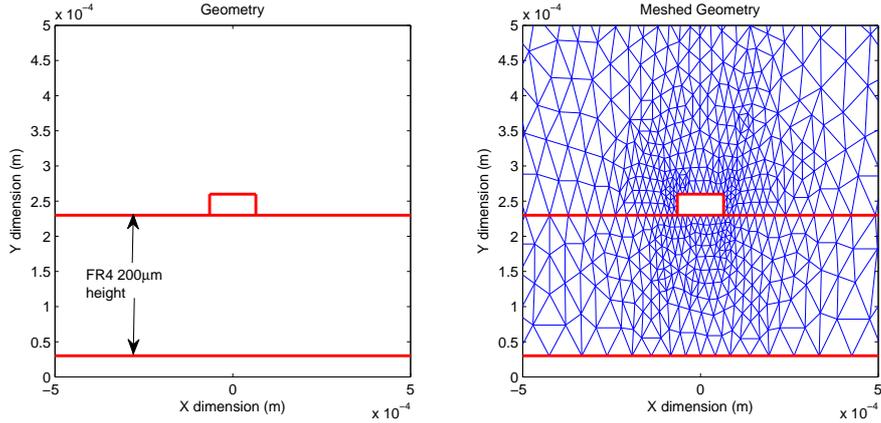
Figure 48. A microstrip line.

For example, consider the microstrip line of width 0.13 mm shown in Figure 48. The 2D potential distribution for this structure has been obtained and plotted in Figure 49. The characteristic impedance calculated from the obtained per-unit-length capacitance and inductance values is 86 Ω which agrees well with calculations from well know formulae [29].

3.2.3   Formulation

The cross-section of the geometry perpendicular to the edge under consideration is analyzed using a 2D-electrostatic solver to obtain the p.u.l capacitance and inductance matrices, $\overline{\overline{C}}_{2D}$ and $\overline{\overline{L}}_{2D}$, respectively. The formulation for the 2D solver is provided in Section 3.2.2.

While $\overline{\overline{C}}_{2D}$ and $\overline{\overline{L}}_{2D}$ represent the correct p.u.l capacitance and inductance of the structure, due to the approximation $\frac{\partial}{\partial z} = 0$ used by the formulation, as described earlier, the p.u.l inductance and capacitance of the M-FDM model represent only the contributions from the parallel plate fields. We denote these capacitance matrices as $\overline{\overline{C}}_{pp}$ and $\overline{\overline{L}}_{pp}$.

Once $\overline{\overline{C}}_{2D}$ and inductance $\overline{\overline{L}}_{2D}$ are obtained, they can be used to derive the fringe augmentation (FA) elements $\overline{\overline{C}}_f$ and $\overline{\overline{L}}_f$. $\overline{\overline{C}}_f$ represents the additional capacitive elements to be added to $\overline{\overline{Y}}$ to correctly model the fringe E-fields. $\overline{\overline{L}}_f$ represents

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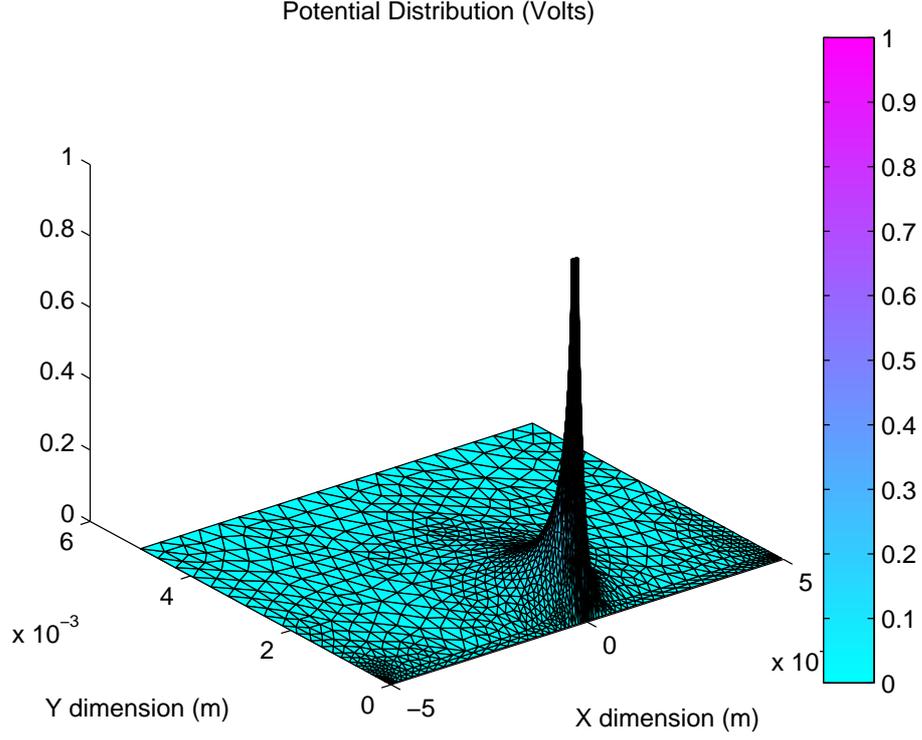
Figure 49. Potential distribution of microstrip in Figure 48.

additional inductive elements to be added between adjacent nodes that lie parallel to the edge being considered, to correctly model the fringe H-fields.

Given that $\overline{\overline{C}}_f$ and $\overline{\overline{L}}_f$ are added symmetrically on the two sides of the cross-section being considered, the following relations can be obtained.

$$\overline{\overline{C}}_{2D} = \overline{\overline{C}}_{pp} + 2\frac{\overline{\overline{C}}_f}{w}, \text{ where } w \text{ is the discretization width} \tag{73}$$

and

$$\overline{\overline{L}}_{2D}^{-1} = \overline{\overline{L}}_{pp}^{-1} + 2w\overline{\overline{L}}_f^{-1} \tag{74}$$

From the above equations, the expressions for $\overline{\overline{C}}_f$ and $\overline{\overline{L}}_f$ are:

$$\overline{\overline{C}}_f = \frac{1}{2}\left(\overline{\overline{C}}_{2D} - \overline{\overline{C}}_{pp}\right)w \tag{75}$$

and

$$\overline{\overline{L}}_f = 2\left(\overline{\overline{L}}_{2D}^{-1} - \overline{\overline{L}}_{pp}^{-1}\right)^{-1}w \tag{76}$$

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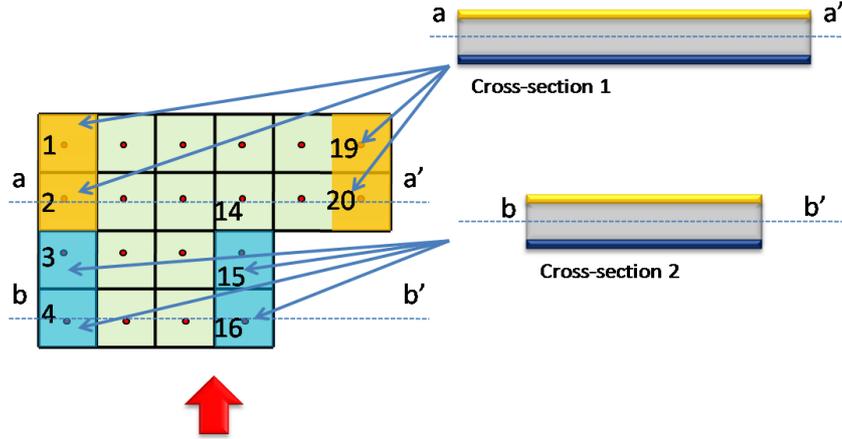
Figure 50. Two plane structure with two unique cross-sections.

3.2.4   Matrix Equation for Single Plane-Pair Geometries

Figure 50 shows the discretized top-view of an L-shaped two-layer structure. This structure can be segmented into two cross-sections, indicated by the dotted cutting planes $a - a'$ and $b - b'$, perpendicular to the axis indicated by the arrow. For these two cross-sections, the scalar fringe capacitance and inductance, C_{f1}, L_{f1}, C_{f2} and L_{f2}, can be obtained. In general, assuming that a geometry requires the analysis of k cross-sections, the fringe corrections will be $(C_{f1}, L_{f1}; C_{f2}, L_{f2}; \ldots; C_{fk}, L_{fk})$. In Figure 50, each of the cross-sections result in fringe corrections to several nodes. The formulation requires a list of nodes, S_{Ci}, be created for each of the capacitive corrections C_{fi}, indicating that an additional admittance of $j\omega C_{fi}$ needs to be added to each of the nodes in S_{Ci}. In the example shown in Figure 50, $S_{C1} = (1, 2, 19, 20)$ and $S_{C2} = (3, 4, 15, 16)$.

Similarly, another list is created containing (unordered) pairs of nodes S_{Li}, where the inductive element L_{fi} is added between each pair of nodes in S_{Li}. One implementation detail in the addition of fringe inductances needing additional clarification is in dealing with unit-cells lying at the boundary between two cross-sections, for example Nodes 2 and 3. For example, the fringe inductance to be added between Nodes 2 and 3 can be L_{f1}, L_{f2} or $\frac{1}{2}(L_{f1} + L_{f2})$. In this thesis, the implementation is simplified

by choosing the first option, while the last is more accurate. However, in practice, there is no significant loss in accuracy. In the example, $S_{L1} = \{(1,2); (2,3); (19,20)\}$ and $S_{L2} = \{(3,4); (15,16)\}$. Notice that Node 2 appears twice in S_{L1} and that the maximum number of fringe inductances connected to any given node is 2.

The ith capacitive fringe correction can be expressed in terms of the following equation:

$$\overline{\overline{\mathbf{Y}}}_{cf,i} = j\omega C_{fi} \overline{\overline{\mathbf{P}}}_i \tag{77}$$

where $\overline{\overline{\mathbf{P}}}_i$ is a diagonal matrix, whose diagonal entries are defined as

$$p_{m,m}^i = \begin{cases} 1, & \text{if } m \in S_{Ci} \\ 0, & \text{otherwise} \end{cases} \tag{78}$$

Similarly, the ith inductive fringe correction can be expressed as

$$\overline{\overline{\mathbf{Y}}}_{lf,i} = \frac{1}{j\omega L_{fi}} \overline{\overline{\mathbf{Q}}}_i \tag{79}$$

where $\overline{\overline{\mathbf{Q}}}_i$ is an incidence matrix whose elements are given by

$$q_{m,m}^i = \begin{cases} 2, & \text{if } m \text{ is present in } S_{Li} \text{ twice} \\ 1, & \text{if } m \text{ is present in } S_{Li} \text{ once} \\ 0, & \text{otherwise} \end{cases} \tag{80}$$

$$q_{m,n}^i = q_{n,m}^i = \begin{cases} -1, & \text{if } (m,n) \text{ is a pair in } S_{Li} \\ 0, & \text{otherwise} \end{cases} \tag{81}$$

Thus, the final admittance matrix including the fringe corrections can be written as

$$\overline{\overline{\mathbf{Y}}}_{FA} = \overline{\overline{\mathbf{Y}}} + \sum_{i=1}^{k} \left(\overline{\overline{\mathbf{Y}}}_{cf,i} + \overline{\overline{\mathbf{Y}}}_{lf,i} \right) \tag{82}$$

where $\overline{\overline{\mathbf{Y}}}$ is the admittance matrix from M-FDM given in (46). $\overline{\overline{\mathbf{Y}}}$ in (46) is now replaced with $\overline{\overline{\mathbf{Y}}}_{FA}$. It can be seen from this procedure that the number of non-zeros in and the structure of $\overline{\overline{\mathbf{Y}}}_{FA}$ is identical to that of $\overline{\overline{\mathbf{Y}}}$.
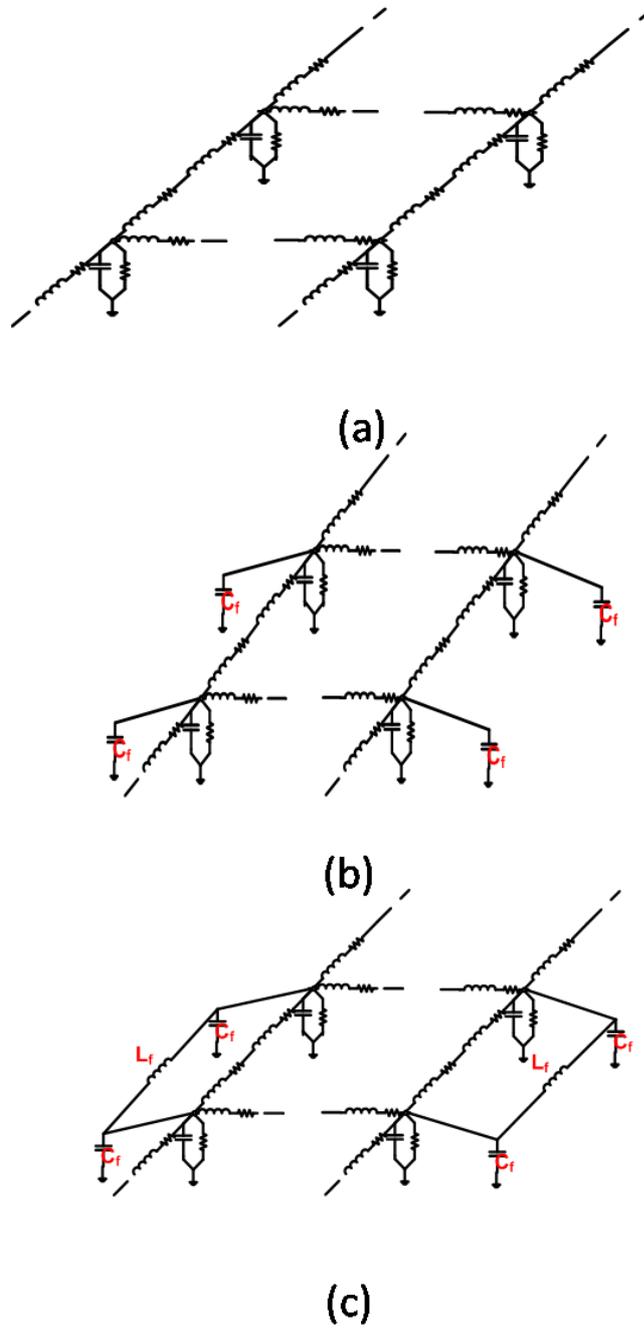
Figure 51. Addition of Fringe elements for single plane-pair structures. Equivalent circuit (a) from uncorrected M-FDM (b) upon addition of fringe capacitance (c) upon further addition of fringe inductance.
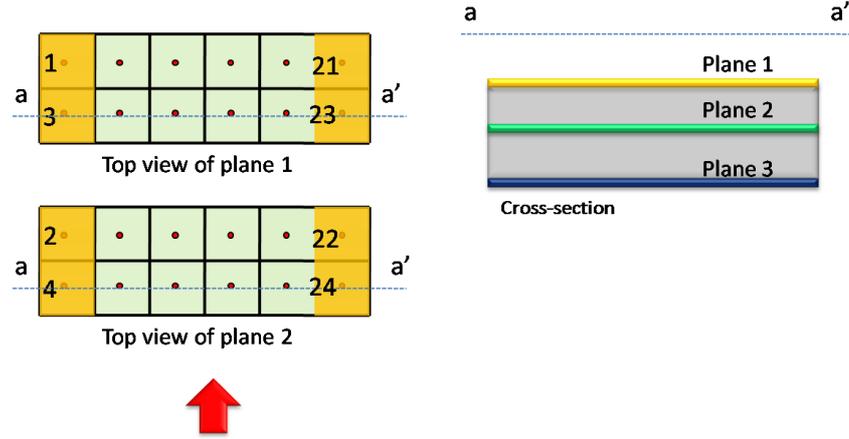
Figure 52. Three layer structure showing location of fringe nodes.

3.2.5 Equivalent Circuit for a Single Plane-Pair

The resultant equivalent circuit from the M-FDM + FA method when applied to two metal layer geometries is shown in Figure 51. Figure 51(a) shows the basic equivalent circuit from M-FDM. Upon updating the admittance matrix with the fringe capacitance, the equivalent circuit is modified as shown in Figure 51(b). Finally, the result of updating the admittance matrix with the fringe inductance elements is shown in Figure 51(c).

3.2.6 Matrix Equation for Multiple Plane-Pair Geometries

The FA method for multiple plane-pair geometries can be explained using Figure 52. The additional complexity posed by multiple plane-pairs is the reason for the choice of the simple example containing just one unique cross-section.

For this example, the 2×2 fringe capacitance and inductance matrices $\overline{\overline{C}}_f$ and $\overline{\overline{L}}_f$ can be obtained. In general, assuming that a geometry requires the analysis of k cross-sections, the fringe corrections will be $(\overline{\overline{C}}_{f1}, \overline{\overline{L}}_{f1}; \overline{\overline{C}}_{f2}, \overline{\overline{L}}_{f2}; \ldots; \overline{\overline{C}}_{fk}, \overline{\overline{L}}_{fk})$ Also, assuming that the geometry contains $L + 1$ layers, the fringe capacitance and inductance matrices will be $L \times L$.

The derivation of the matrix equation requires an understanding of the node numbering used in M-FDM. Assume also, that the geometry contains M rows and N

columns. The cell in row i, column j and layer l, (where numbering begins from the top left and from top to bottom) has the node number, $n_{i,j,l}$, given by

$$n_{i,j,l} = (j - 1) \times M + (i - 1) \times L + l \tag{83}$$

In the example, the node number for cell (2,1,2) calculated using the above formula is $n_{2,1,2} = (1 - 1) \times 2 + (2 - 1) \times 2 + 2 = 4$.

It can be seen that if a cell (i, j, l) in the top layer is marked as a cell to which fringe augmentation elements must be added, then so are $(i, j, l + 1)$, $(i, j, l + 2)$, ..., (i, j, L). Therefore, for convenience, only the number of a multi-layer unit cell needs to be considered. The formula for the multi-layer unit cell, $n_{i,j}^{uc}$ is

$$n_{i,j}^{uc} = (j - 1) \times M + i \tag{84}$$

The four multi-layer unit cells in the example have multi-layer unit cell numbers 1,2, 11 and 12.

As before, a list of nodes, S_{Ci}, is created for each of the capacitive corrections $\overline{\overline{C}}_{fi}$. However, this list is populated with the unit cell number and not the actual node numbers assigned to the unknowns in the system. In the example, there is only one list, S_{C1}, containing the aforementioned multi-layer unit cell numbers, (1,2,11,12).

The unordered list S_{Li} also contains the numbers of the multi-layer unit cells between which $\overline{\overline{L}}_{fi}$ must be added. In the example, $S_{L1} = \{(1, 2); (11, 12)\}$.

The ith capacitive fringe correction can be expressed in terms of the following equation:

$$\overline{\overline{Y}}_{cf,i} = j\omega \overline{\overline{P}}_i \otimes \overline{\overline{C}}_{fi} \tag{85}$$

where $\otimes$ represents the Kronecker matrix product. If $\overline{\overline{A}}$ is an $m \times n$ matrix and $\overline{\overline{B}}$ is a $p \times q$ matrix, then $\overline{\overline{A}} \otimes \overline{\overline{B}}$ is a $mp \times nq$ block matrix given by

$$\overline{\overline{A}} \otimes \overline{\overline{B}} = \begin{pmatrix} a_{11}\overline{\overline{B}} & \dots & a_{1n}\overline{\overline{B}} \\ \vdots & \ddots & \vdots \\ a_{m1}\overline{\overline{B}} & \dots & a_{mn}\overline{\overline{B}} \end{pmatrix} \tag{86}$$

The elements of $\overline{\overline{\mathrm{P}}}_i$ can be obtained using (78). $\overline{\overline{\mathrm{P}}}_i$ is an $MN \times MN$ matrix, and $\overline{\overline{C}}_{fi}$ is $L \times L$. Therefore, $\overline{\overline{\mathrm{Y}}}_{cf,i}$ is an $MNL \times MNL$ matrix, which is the same size as $\overline{\overline{\mathrm{Y}}}$. Also, the ith row in $\overline{\overline{\mathrm{Y}}}_{cf,i}$ corresponds to the ith unknown in $\overline{\overline{\mathrm{Y}}}$.

Similarly, the ith inductive fringe correction can be expressed as

$$\overline{\overline{\mathrm{Y}}}_{lf,i} = \frac{1}{j\omega}\overline{\overline{\mathrm{Q}}}_i \otimes \left(\overline{\overline{L}}_{fi}\right)^{-1} \tag{87}$$

where $\overline{\overline{\mathrm{Q}}}_i$ is the incidence matrix whose elements are defined in (80) and (81).

For the example in Figure 52,

$$\overline{\overline{\mathrm{Y}}}_{cf,1} = j\omega \begin{pmatrix} 1 & 0 & \ldots & & \ldots & 0 \\ 0 & 1 & & & & \vdots \\ \vdots & & 0 & & & \\ & & & \ddots & & \\ & & & & 0 & \vdots \\ \vdots & & & & 1 & 0 \\ 0 & \ldots & & \ldots & 0 & 1 \end{pmatrix} \otimes \overline{\overline{C}}_f \tag{88}$$

which can be expanded to

$$\overline{\overline{\mathrm{Y}}}_{cf,1} = j\omega \begin{pmatrix} \overline{\overline{C}}_f & 0 & \ldots & & \ldots & 0 \\ 0 & \overline{\overline{C}}_f & & & & \vdots \\ \vdots & & 0 & & & \\ & & & \ddots & & \\ & & & & 0 & \vdots \\ \vdots & & & & \overline{\overline{C}}_f & 0 \\ 0 & \ldots & & \ldots & 0 & \overline{\overline{C}}_f \end{pmatrix} \tag{89}$$

In the above equation, $\overline{\overline{\mathrm{Y}}}_{cf,1}$ is written in terms of 2×2 sub-matrices. Also, it is exactly the same matrix that will be obtained by explicitly adding the fringe capacitance $\overline{\overline{C}}_f$ on a cell by cell basis.

Similarly,

$$\overline{\overline{Y}}_{lf,1} = \frac{1}{j\omega} \begin{pmatrix} 1 & -1 & 0 & \ldots & & \ldots & 0 \\ -1 & 1 & & & & & \vdots \\ \vdots & & 0 & & & & \\ & & & \ddots & & & \vdots \\ & & & & 0 & 0 & \\ \vdots & & & & 1 & -1 \\ 0 & \ldots & & \ldots & 0 & -1 & 1 \end{pmatrix} \otimes \left(\overline{\overline{L}}_f\right)^{-1} \tag{90}$$

i.e,

$$\overline{\overline{\overline{Y}}}_{lf,1} = \frac{1}{j\omega} \begin{pmatrix} \left(\overline{\overline{L}}_f\right)^{-1} & -\left(\overline{\overline{L}}_f\right)^{-1} & 0 & \ldots & & \ldots & 0 \\ -\left(\overline{\overline{L}}_f\right)^{-1} & \left(\overline{\overline{L}}_f\right)^{-1} & & & & & \vdots \\ \vdots & & 0 & & & & \\ & & & \ddots & & & \vdots \\ & & & & 0 & & 0 \\ \vdots & & & & & \left(\overline{\overline{L}}_f\right)^{-1} & -\left(\overline{\overline{L}}_f\right)^{-1} \\ 0 & & \ldots & & \ldots & 0 & -\left(\overline{\overline{L}}_f\right)^{-1} & \left(\overline{\overline{L}}_f\right)^{-1} \end{pmatrix} \tag{91}$$

The above matrix, $\overline{\overline{\overline{Y}}}_{lf,1}$, can also be obtained by adding the fringe inductances on a cell by cell basis.

The use of the Kronecker product simplifies the formulation, provided that the node numbering discussed is used. For other node numbering schemes, $\overline{\overline{\overline{Y}}}_{cf,i}$ and $\overline{\overline{\overline{Y}}}_{lf,i}$ may have to be permuted to obtain the correct augmentation matrices.

The final system matrix including the fringe augmentation elements for multiple plane-pair geometries is obtained as before, using (82).

3.2.7 Equivalent Circuit for Multiple Plane-Pairs

The FA method leads to more complicated equivalent circuits when applied to multiple plane-pair geometries. As an illustration, consider a three metal layer geometry, the top view of which is shown in Figure 53(a). To provide a simple explanation of the FA method, only three nodes (A, B and C) in the finite difference mesh are considered. To include the matrix entries associated with the fringe field, the cross

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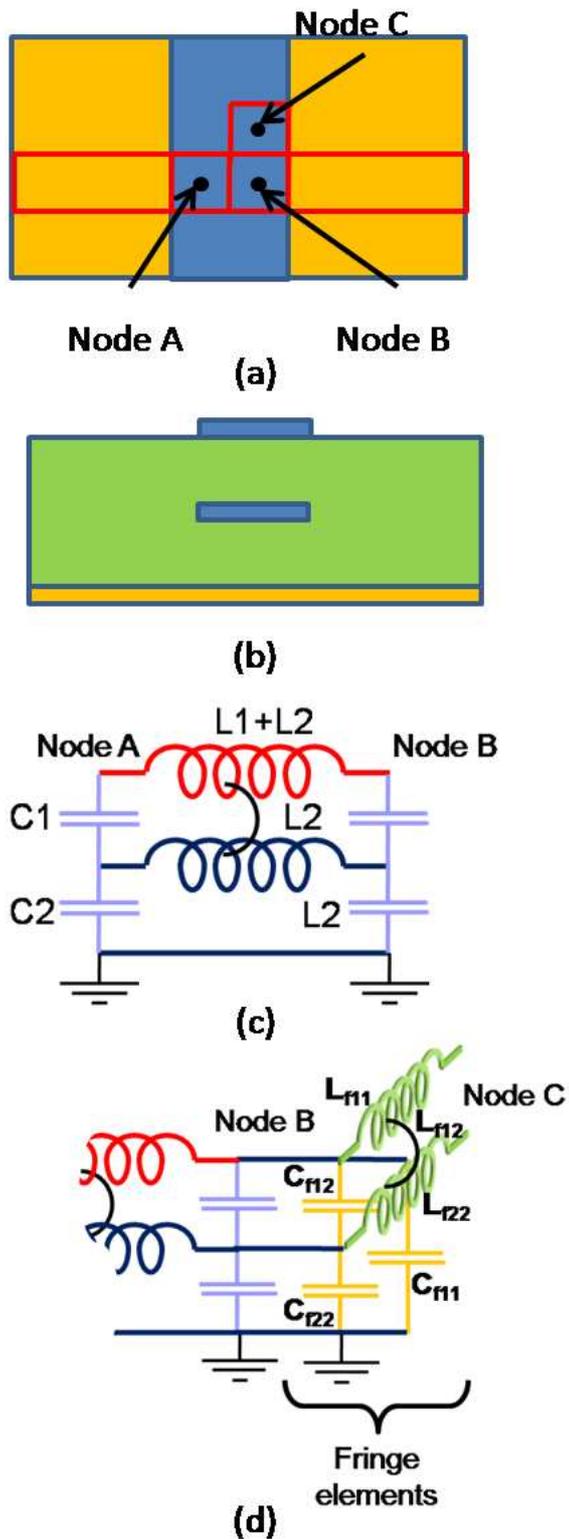
Figure 53. Addition of Fringe elements. (a) Top view of top and middle layers (b) Cross section (c) M-FDM circuit model between Nodes A and B (d) Circuit model as a result of fringe augmentation (FA).

section of the structure, as shown in Figure 53(b) is considered. In Figure 53(c), the circuit elements between Nodes A and B are shown, as derived from the M-FDM formulation. The correction of the system matrix, $\overline{\overline{Y}}$, with the elements from the FA matrix C_f and L_f results in the addition of new circuit elements as shown in Figure 53(d).

3.2.8 Computational Complexity

The fringe augmentation procedure requires the calculation of fringe elements for every non-unique cross-section in the geometry. However, once the metal strip is wide enough such that the edges do not significantly interact ($\frac{w}{h} > 10$), the fringe elements can be expected to remain unchanged, significantly reducing computational cost [28].

It can be noted that since no new non-zeros are being added to the admittance matrix, $\overline{\overline{Y}}$, the matrix structure remains identical to the form shown in (61). Hence, the factorization and solve time remain unchanged.

3.3 Results

The M-FDM technique with fringe augmentations was used to analyze three test structures. All simulations were carried out on an Intel dual-Xeon workstation with 3 GB of RAM. An Agilent four port, 40 GHz VNA was used for measurements. The full-wave method-of-moments based tools, EMSurf, which is part of the IBM EIP suite [30], and Sonnet, have also been used for correlation.

3.3.1 Microstrip Meander

The M-FDM + FA method was used to simulate the microstrip meander structure in Figure 45. The first step is to obtain the fringe augmentation elements from the 2D solver.

3.3.1.1 Results from 2D Simulation

The cross-section of the problem solved using the 2D solver is shown in Figure 45(a). Since this problem contains two layers, the fringe elements are scalars. The results from the 2D simulation are

$$C_{2D} = 435.13 \text{ pF/m} \tag{92}$$

$$L_{2D} = 101.97 \text{ nH/m} \tag{93}$$

The per-unit-length parallel-plate parameters are

$$C_{PP} = \varepsilon_0 \varepsilon_r \frac{1 \text{ mm}}{0.1 \text{mm}} = 389.58 \text{ pF/m} \tag{94}$$

$$L_{PP} = \mu \frac{0.1 \text{ mm}}{1 \text{mm}} = 125.66 \text{ nH/m} \tag{95}$$

From the above equations, and using a cell discretization, w, of 0.1 mm, the fringe augmentation elements can be calculated as:

$$C_f = \frac{1}{2} \left(C_{2D} - C_{PP} \right) w = 2.2775 \text{ pF p.u.c} \tag{96}$$

$$L_f = 2 \left(L_{2D}^{-1} - L_{PP}^{-1} \right)^{-1} w = 108.1769 \text{ nH p.u.c} \tag{97}$$

3.3.1.2 Comparisons with Full-wave Simulation

The microstrip meander line of Figure 45 was simulated using M-FDM with the fringe augmentations. The return loss results are shown in Figure 54. Clearly, the accuracy has improved significantly. Interestingly, in Figure 46, without the FA elements, the resonance frequencies obtained from M-FDM are consistently lower than the resonance frequencies from full-wave. The addition of the FA capacitance increases the per-unit-length capacitance, and so lowers the resonance frequencies further still. However, the FA inductance compensates for this by lowering the overall per-unit-length inductance, causing the results from M-FDM+FA to match with full-wave.

3.3.2 Three Layer Problem

The second test structure contains three metal layers with 30 mm wide planes in the top and middle layers. The top view of this structure is shown in Figure 55(a), with
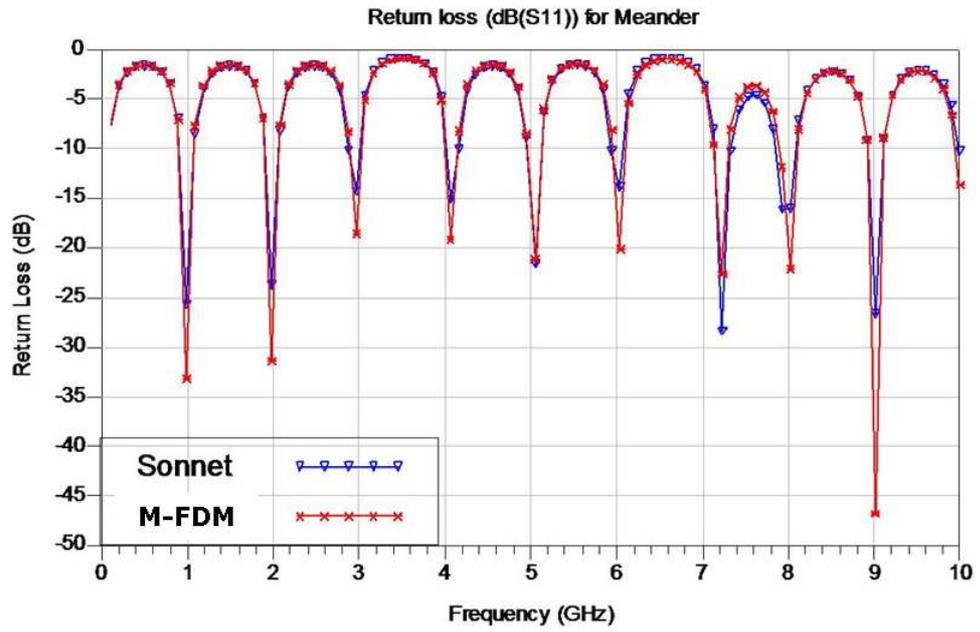
Figure 54. Return loss (dB) for structure in Figure 45 with fringe models.
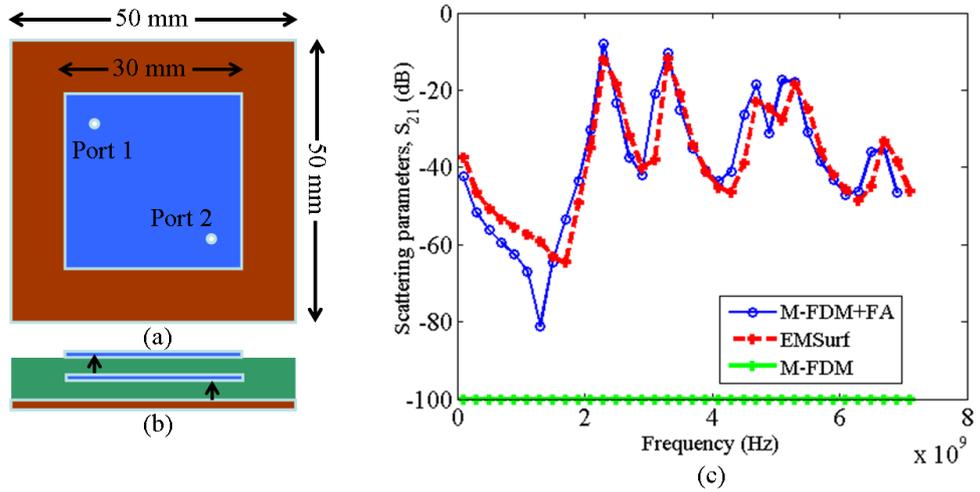
Figure 55. Geometry of multilayer test structure I. (a) Top view of top and middle layers (b) Cross section (c) Insertion Loss.
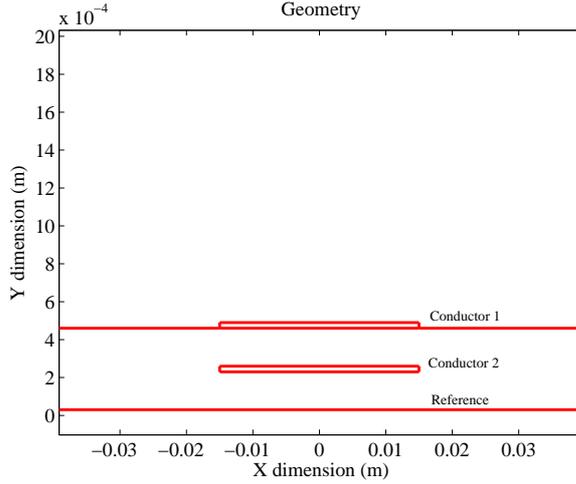
Figure 56. Geometry of electrostatic problem with cross-section from Figure 55(b).

the cross section in Figure 55(b). The dielectric was FR-4 with 200 μm thickness and $\tan \delta$ of 0.015. Port locations are indicated by the circles shown in Figure 55(a). Also, as can be seen by the arrows in Figure 55(b), the terminals of Port 1 are connected between the top and middle layers, while the terminals of Port 2 are connected between the middle and bottom layers.

3.3.2.1 Results from 2D Simulation

The cross-section of the structure, shown in Figure 55(b) was used as input to the 2D solver. The geometry of the problem analyzed with the 2D solver is shown in Figure 56. The potential distributions in the problem domain created due to excitations on the top and middle conductors are shown in Figure 57 and Figure 58 respectively. The per-unit-length capacitance and inductance obtained from 2D simulations are

$$\overline{\overline{C}}_{2D} = \begin{pmatrix} 5.915 & -5.8537 \\ -5.8537 & 11.727 \end{pmatrix} \text{ nF/m} \tag{98}$$

$$\overline{\overline{L}}_{2D} = \begin{pmatrix} 15.594 & 7.7825 \\ 7.7825 & 8.0521 \end{pmatrix} \text{ nH/m} \tag{99}$$

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Potential Distribution (Volts)
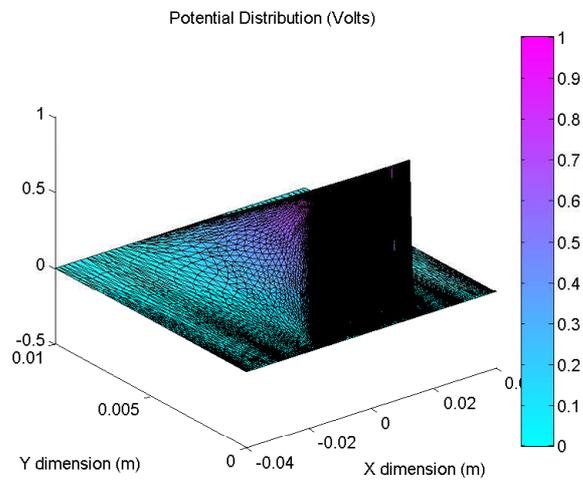
Figure 57. Potential distribution due to 1V excitation on top conductor.

Potential Distribution (Volts)
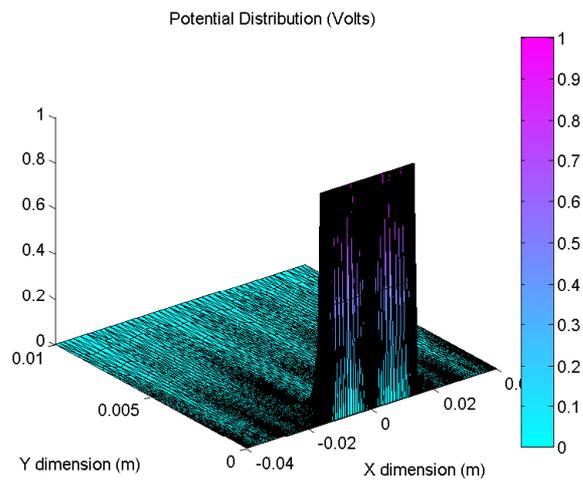
Figure 58. Potential distribution due to 1V excitation on middle conductor.

The per-unit-length parallel-plate parameters are

$$\overline{\overline{C}}_{PP} = \varepsilon_0 \varepsilon_r \frac{30 \text{ mm}}{0.2 \text{ mm}} \begin{pmatrix} 1 & -1 \\ -1 & 2 \end{pmatrix} = \begin{pmatrix} 5.84364 & 5.84364 \\ 5.84364 & 11.68728 \end{pmatrix} \text{nF/m} \qquad (100)$$

$$\overline{\overline{L}}_{PP} = \mu \frac{0.2 \text{ mm}}{30 \text{ mm}} \begin{pmatrix} 2 & 1 \\ 1 & 1 \end{pmatrix} = \begin{pmatrix} 16.7551 & 8.37758 \\ 8.37758 & 8.37758 \end{pmatrix} \text{nH/m} \qquad (101)$$

Using a unit-cell discretization of 0.5 mm, the FA elements are

$$\overline{\overline{C}}_f = \begin{pmatrix} 0.01784 & -0.002515 \\ -0.002515 & 0.00993 \end{pmatrix} \text{pF p.u.c} \qquad (102)$$

$$\overline{\overline{L}}_f = \begin{pmatrix} 0.22717 & 0.07073 \\ 0.07073 & 0.86593 \end{pmatrix} \text{nH p.u.c} \qquad (103)$$

From the above results, it can be seen that the additional fringing elements that are added between the top conductor and reference are the source of the coupling between the plane-pairs.

3.3.2.2 *Comparisons with Full-wave Simulation*

The insertion loss results are provided in Figure 55(c). When the fringe augmentations are not included, M-FDM [23] simulations indicate that the ports are uncoupled. Hence, the insertion loss between the ports is negligible. When the fringe augmentations are included, there is good agreement with the full-wave EM solution. Also, a significantly high S_{21} of -8dB at 2.4 GHz has been captured.

3.3.3 Model to Hardware Correlation

The third test case contains a cavity as shown in Figure 59. An application where such a structure is used is in the packaging of embedded active components. A chip is placed in the cavity, after the package has been completely fabricated. This approach to embedding actives inside a package is called the "chip last" approach, and is a means of reducing the stress placed on the IC during the fabrication process [31]. However, fringing fields occur along the edges of the apertures that are created in the power planes, and cause vertical electromagnetic coupling.
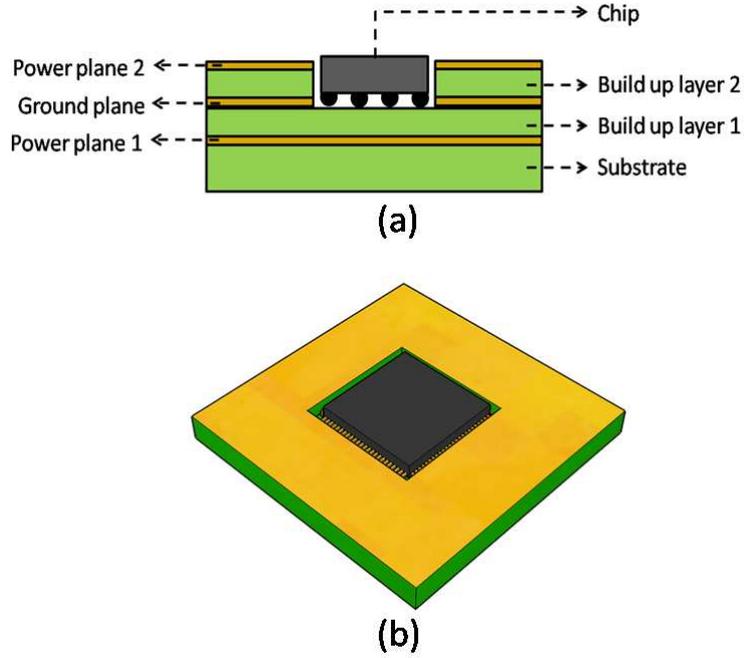
Figure 59. Model of package with embedded die in cavity (a)Stack-up (b)3D View.

The top view and cross section for the three layer test vehicle is shown in Figure 60(a) and 60(b), respectively. The dielectric layers are 50 μm thick with a relative permittivity of 3.4 and tan δ of 0.06, with 20 μm thick metal layers. Port locations are indicated by the circles shown in Figure 60(a), and as in the previous case, the terminals of Port 1 are connected between the top and middle layers, while the terminals of Port 2 are connected between the middle and bottom layers.

As before, when the fringe augmentations are not included, M-FDM simulations indicate that the ports are uncoupled. As seen from the insertion loss results shown in Figure 60(c), there is a good agreement between the M-FDM technique with fringe augmentations, the full-wave EM solution and measurement.

For this case, there are two non-unique cross sections to be considered for 2D analysis to obtain the fringe inductance and capacitance matrices. These simulations required about 10s each. The M-FDM simulations contained 14,400 cells and required 0.44s per frequency point.
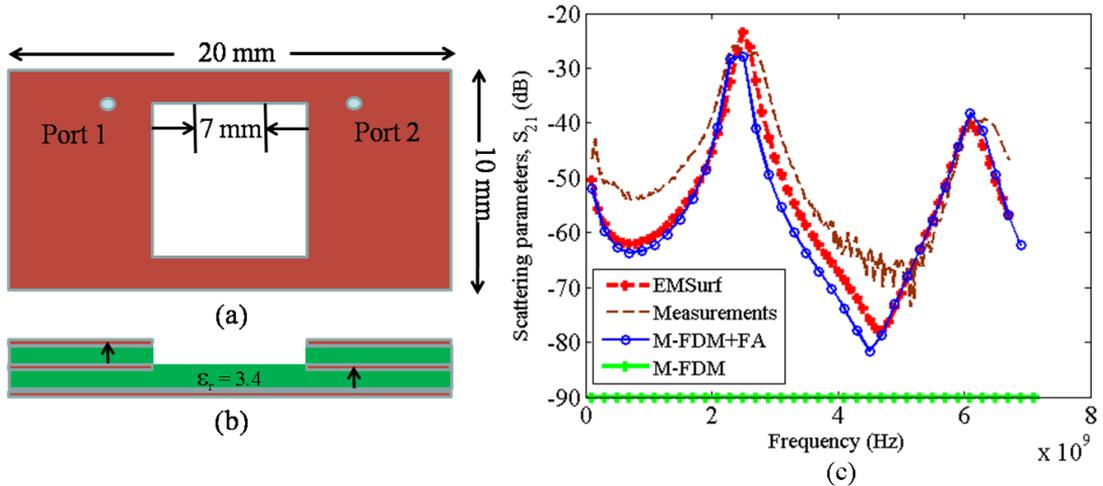
Figure 60. Geometry of multilayer test structure II. (a) Top view of top and middle layers (b) Cross section (c) Insertion Loss.

3.4   Conclusions

Fringing fields are significant at metal edges in a multi-layer power/ground network. In single plane-pair cases where the lateral dimensions of the plane exceed 50 times the height of the substrate, these fields can be neglected, without affecting the accuracy of the simulated response. However, for structures where the plane width is comparable to the height of the substrate, or where the edges of planes in a multi-layer package coincide, these fringing fields can be a significant source of coupling. In this chapter, a formulation has been developed to obtain a frequency independent network model for the fringing fields in multi-layer packages. This model is based on obtaining the per-unit-length capacitance and inductance of the structure being analyzed, using a 2D electrostatic solver whose formulation has also been developed. The FA elements do not increase the number of non-zeros in the system matrix. Thus the FA method does not cause an increase in the computational time required to factorize and solve the system. The additional increase in time is only due to the calculation of the 2D solutions of the cross-sections in the structure. These calculations are relatively cheap, and are only performed once for the entire frequency sweep. The FA method has been

employed to simulate single and multiple-plane pair structures and the results have been compared against full-wave simulations and measurements.

CHAPTER 4

MODELING OF GAPS IN M-FDM FOR MULTI-LAYERED PACKAGES

4.1 Introduction

In Chapter 3, the problem of fringing fields was considered. Fringing fields are ignored by the M-FDM formulation (or any other formulation that employs the planar-circuit approximation). This is because, according to this approximation, $\frac{\partial}{\partial z} = 0$.

This approximation can once again lead to errors in particular cases of power/ground planes containing slots. To support multiple DC levels, a PDN can be segmented into multiple galvanically unconnected planes. These are called split planes or power islands, depending on the layout geometry.

Electromagnetic fields in close proximity to the edges of the planes contain significant E_x and E_y fields, and these fields couple energy between power circuits that are not DC connected. Figure 61(a) and (b) shows split planes in two typical types of cases, which have been labeled microstrip type and stripline type, respectively.

The reason for labeling these types of structures based on types of transmission line configurations is this: the methodology that has been developed in this thesis
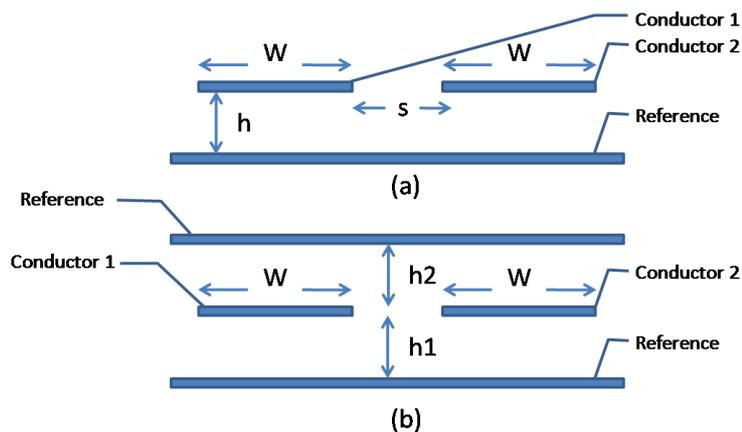
Figure 61. Gaps in Power Planes (a)Microstrip type gap (b)Stripline type gap.

relies on analyzing the cross-section of the structure, in a direction perpendicular to the slot axis, using the 2D-electrostatic solver developed in Section 3.2.2. These cross-sections are often analogous to low impedance transmission line configurations. However, the formulation is general and is not limited to these configurations alone.

As with the fringe augmentation (FA) procedure developed in Chapter 3, the 2D-electrostatic solution provides a per-unit-length (p.u.l) capacitance and inductance matrix, which is used to calculate additional circuit elements that enable the modeling of the EM-coupling between the galvanically unconnected metal patches. The proposed method for modeling the EM coupling across gaps in shapes is called the plane-gap augmentation (PGA) method. The contribution of this work is a formulation by which the M-FDM model can be corrected with a minimal number of additional circuit elements that couple nodes on either side of the slot.

The rest of this chapter is organized as follows. To motivate the need for including gap corrections, the results of M-FDM when applied to structures with prominent fringing fields are presented in Section 4.1.1. The modeling and inclusion of gap fields using the FA technique is discussed in Section 4.2. The accuracy of the technique is shown through model to hardware correlation in Section 4.3, followed by conclusions in Section 4.4.

4.1.1 Significance of Gap Effect

Split planes and power islands are increasingly being used to support multiple modules, with each module requiring a different power supply.

An example of this is that of a mixed signal board with split planes separating the digital module with an FPGA and an RF transceiver module. The board layout is shown in Figure 62. The dielectric thickness is 200 μm. Ports 1 and 2 are placed at the location of the FPGA and the RF transceiver respectively. Noise generated by the FPGA can couple through the PDN and cause degradation in the performance of the RF module. M-FDM without the gap models will not show any coupling between
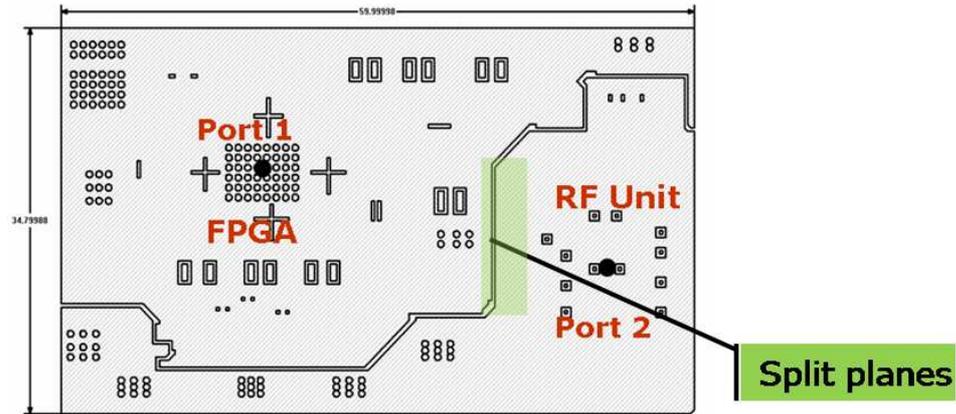
Figure 62. Mixed signal board.
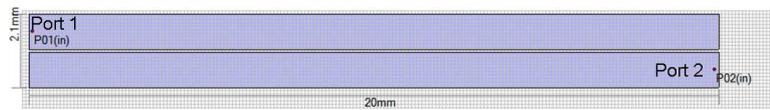
Figure 63. Top view of a power bus (20mm×1mm) with 100μm separation.

Ports 1 and 2.

Such PDN designs are only becoming more common as the integration of digital and analog/RF devices becomes more common. A simple split power bus is shown in Figure 63, using the same stack up shown in the previous example (Figure 45(a)). The insertion loss between the ports as obtained from M-FDM and from a schematic simulation of coupled lines in ADS are shown in Figure 64. Since M-FDM models the metal edges as PMC, there is no coupling between the two ports. Also, M-FDM with the fringe augmentations will not change the insertion loss behavior, since M-FDM+FA only models the effect of the fringing fields to layers above and below the metal edges.

Another instance where both the fringe and gap effects are critical is in the modeling of electromagnetic band gap (EBG) structures. An EBG is a periodic structure, that can be employed as a band-stop filter applied for noise suppression in modern packages and boards. An example *Alternating Impedance*-EBG (AI-EBG) [32][33] containing four 14mm×14mm *patches* connected together with 1mm×1mm *branches*
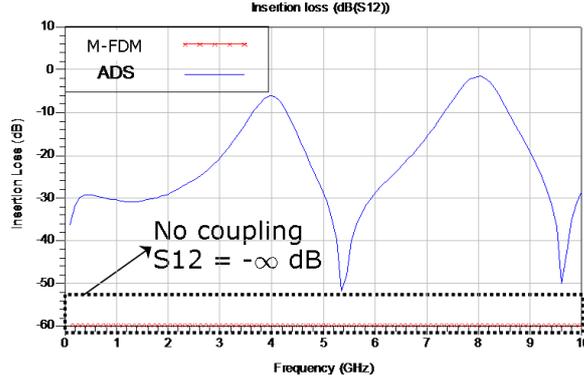
Figure 64. Insertion loss results for structure shown in Figure 63.

is shown in Figure 65(a), with the same stack up as in the previous examples. The fringe effect has a pronounced effect in the narrow-width metal patches, while the coupling across the slot between patches also has an effect in the bandwidth of the EBG. The insertion loss results shown in Figure 65(b) clearly show that the M-FDM approximation results in poor estimation of the bandwidth and isolation levels of the stop-band region.

It is possible to include the effects of gap coupling fields in the M-FDM model by using multi-port connection networks, the development of which is discussed next.

4.2 Inclusion of the Gap Effect using the Plane-Gap Augmentation Method

4.2.1 Simulation Flow

The flowchart of the M-FDM+PGA method has been illustrated in Figure 66. The process involves the following steps:

1. The package geometry is segmented into cross-sections along each row and column of unit-cells. The cross-sections containing gaps, and which are identical, are grouped together.

2. Each unique cross-section is analyzed using a 2D electrostatic solver to obtain the per-unit-length (p.u.l) inductance and capacitance matrices, the values of
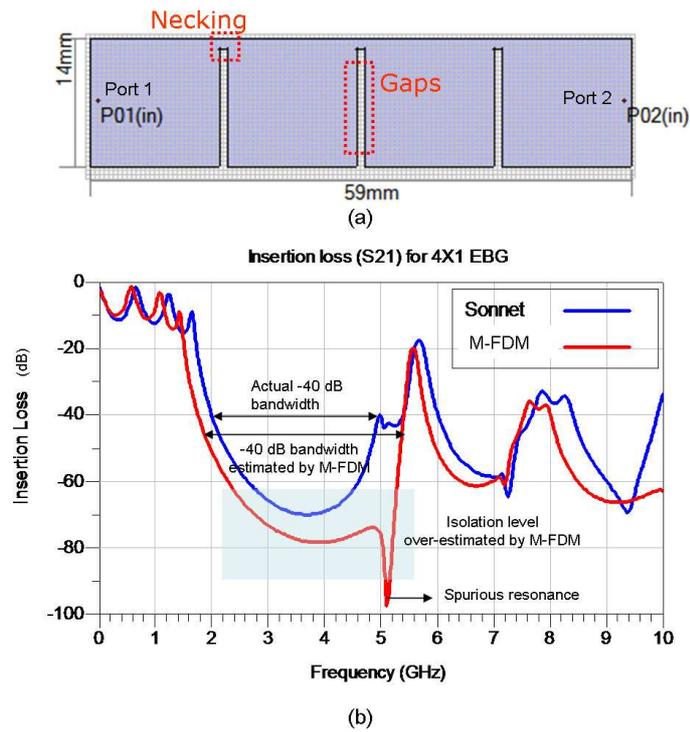
Figure 65. (a) Top view of the AI-EBG (b) Insertion loss of the AI-EBG.
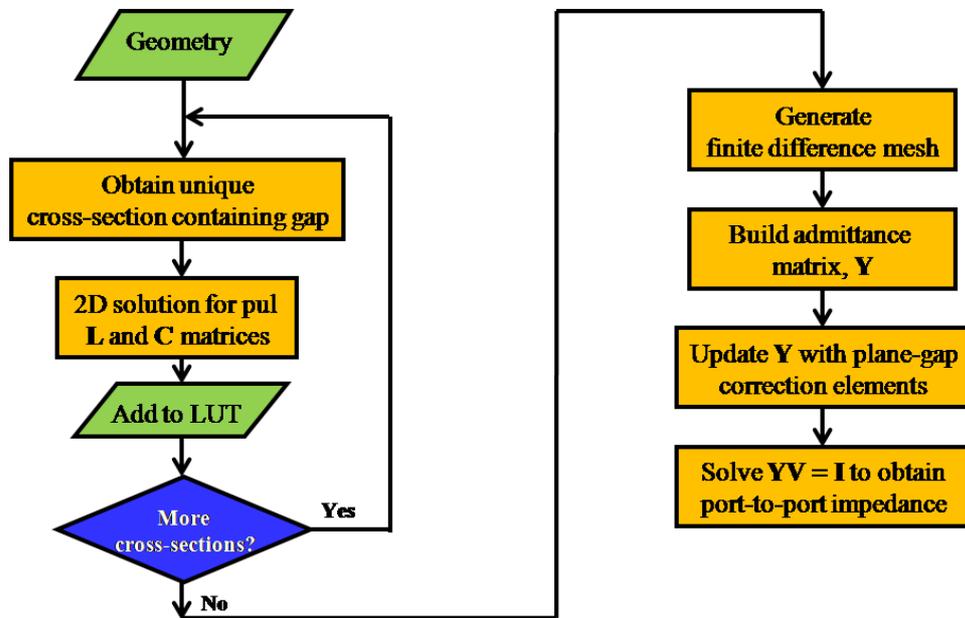
Figure 66. Flowchart for the addition of plane-gap augmentation elements.

which are stored in a look up table, to be retrieved while building the admittance matrix for the frequency sweep.

3. After pre-computing these p.u.l L and C matrices, M-FDM is applied to build the initial admittance matrix $\overline{\overline{\mathbf{Y}}}$.

4. $\overline{\overline{\mathbf{Y}}}$ is updated with the gap correction elements that are calculated based on the stored 2D L and C matrices.

5. Equation 46 is solved to obtain the port-to-port impedance parameters as before.

4.2.2 Formulation for Single Plane-Pair Structures

The cross-section of the geometry perpendicular to the gap under consideration is analyzed using a 2D-electrostatic solver to obtain the p.u.l capacitance and inductance matrices, $\overline{\overline{C}}_{2D}$ and $\overline{\overline{L}}_{2D}$, respectively. The formulation for the 2D solver is provided in Section 3.2.2.

$$\overline{\overline{C}}_{2D} = \begin{pmatrix} C_{11}^{2D} & C_{12}^{2D} \\ C_{12}^{2D} & C_{11}^{2D} \end{pmatrix} \tag{104}$$

$$\overline{\overline{L}}_{2D} = \begin{pmatrix} L_{11}^{2D} & L_{12}^{2D} \\ L_{12}^{2D} & L_{11}^{2D} \end{pmatrix} \tag{105}$$

For the two layer case, the only gap configuration that needs consideration is the microstrip type. The analysis of the microstrip type provides an intuitive understanding of the mechanism of the gap models being applied. The formulation for multiple plane pair gap models is an extension.

Consider the microstrip-type gap shown in Figure 61(a). The two planes on either side of the slot are considered to be symmetric, of width W. The substrate height is h with dielectric constant ε_r.

The top-view of a part of this structure with the FDM mesh is shown in Figure 67. The dotted rectangle picks out a row of unit cells. The M-FDM model can be
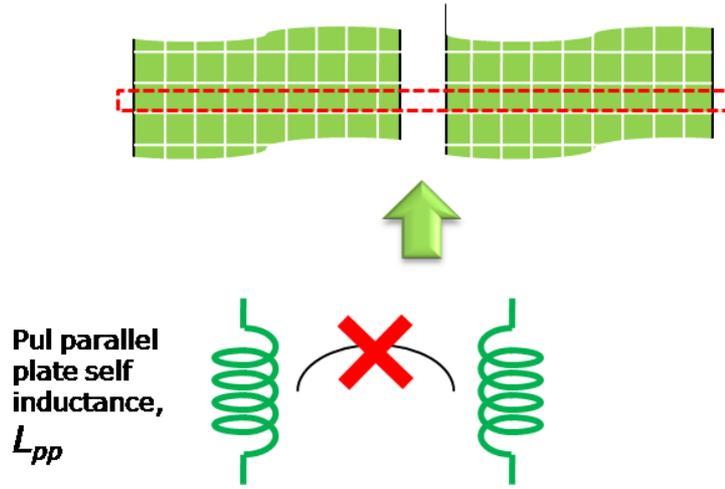
Figure 67. FDM mesh for the microstrip type slot shown in Figure 61(a).

considered to include an effective p.u.l inductance and capacitance for the structure. The equivalent per-unit-length inductance capacitance and inductance matrices are $\overline{\overline{C}}_{pp}$ and $\overline{\overline{L}}_{pp}$, respectively.

It can be seen that the p.u.l capacitance and inductance matrices, $\overline{\overline{C}}_{pp}$ and $\overline{\overline{L}}_{pp}$ are:

$$\overline{\overline{C}}_{pp} = \begin{pmatrix} \varepsilon_0 \varepsilon_r \frac{W}{h} & 0 \\ 0 & \varepsilon_0 \varepsilon_r \frac{W}{h} \end{pmatrix} \tag{106}$$

$$\overline{\overline{L}}_{pp} = \begin{pmatrix} \mu_0 \frac{h}{W} & 0 \\ 0 & \mu_0 \frac{h}{W} \end{pmatrix} \tag{107}$$

(106) and (107) have zeros in the off-diagonal entries because there are no coupling elements connecting the gap-separated conductors. By comparing (106) and (107) with (104) and (105), it is possible to derive the matrices for the circuit elements that form the gap model.

The gap capacitance matrix, $\overline{\overline{C}}_g$ is given by:

$$\overline{\overline{C}}_g = \overline{\overline{C}}_{2D} - \overline{\overline{C}}_{pp} \tag{108}$$
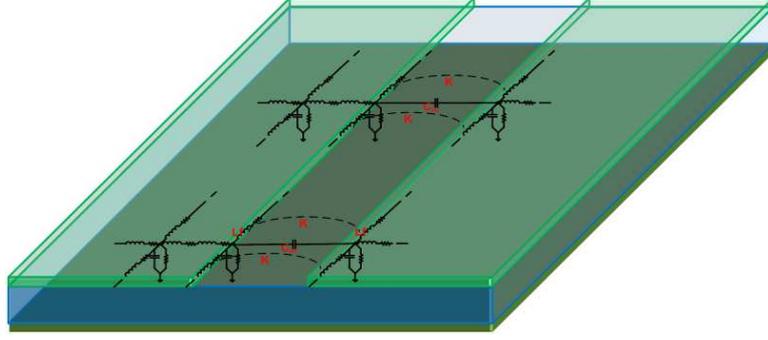
Figure 68. Equivalent circuit - M-FDM with PGA models for a microstrip case.

Therefore,

$$\overline{\overline{C}}_g = \begin{pmatrix} C_{11}^{2D} - \varepsilon_0\varepsilon_r\frac{W}{h} & C_{12}^{2D} \\ C_{12}^{2D} & C_{11}^{2D} - \varepsilon_0\varepsilon_r\frac{W}{h} \end{pmatrix} \tag{109}$$

The gap inductance matrix, $\overline{\overline{L}}_g$ is given by:

$$\overline{\overline{L}}_g = \left[\overline{\overline{L}}_{2D}^{-1} - \overline{\overline{L}}_{pp}^{-1} \right]^{-1} \tag{110}$$

Simplifying, the elements of the gap inductance matrix are:

$$L_{11}^g = -L_{11}^{pp}\frac{-L_{11}^{2D}L_{11}^{pp} + L_{11}^{2D^2} - L_{12}^{2D^2}}{L_{11}^{2D} - 2L_{11}^{2D}L_{11}^{pp} + L_{11}^{pp} - L_{12}^{2D^2}} \tag{111}$$

$$L_{12}^g = (L_{11}^{pp})^2\frac{L_{12}^{2D}}{L_{11}^{2D} - 2L_{11}^{2D}L_{11}^{pp} + L_{11}^{pp} - L_{12}^{2D^2}} \tag{112}$$

These equations are identical to those derived in [34], for the modeling of coupled microstrip lines using resonators.

The addition of the gap models results in an equivalent circuit of the form shown in Figure 68. In this figure, C_m and L_f represent the per-unit-cell self terms obtained from the gap matrices, and k represents the coupling coefficient of mutual inductance.

$$C_m = C_{12}^g w \tag{113}$$

$$L_f = L_{11}^g w \tag{114}$$

$$k = \frac{L_{12}^g}{L_{11}^g} \tag{115}$$

where, w is the unit cell width.
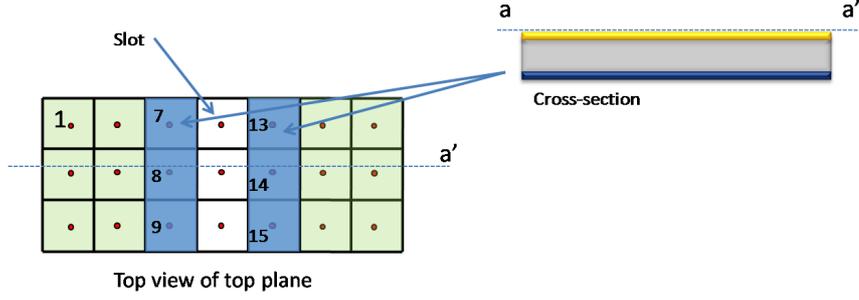
Figure 69. Two plane structure with a slot.

4.2.3 Matrix Equation for a Single Plane-Pair

Figure 69 shows the discretized top-view of a two-layer structure containing a slot. This structure can cross sectioned along the cutting plane $a - a'$.

In general, assuming that a geometry requires the analysis of k cross-sections, the gap corrections will be $(\overline{\overline{C}}_{g1}, \overline{\overline{L}}_{g1}; \overline{\overline{C}}_{g2}, \overline{\overline{L}}_{g2}; \ldots; \overline{\overline{C}}_{gk}, \overline{\overline{L}}_{gk})$. In Figure 69, each of the cross-sections result in gap corrections to several nodes. The formulation requires an ordered list of nodes, S_{Ci}, be created for each of the capacitive corrections $\overline{\overline{C}}_{gi}$, indicating that an additional admittance matrix of $j\omega\overline{\overline{C}}_{gi}$ needs to be added to each of the pairs of nodes in S_{Ci}. In the example shown in Figure 69, $S_{C1} = \{(7, 13); (8, 14); (9, 15)\}$. In this case, C_{11}^{gi} and C_{22}^{gi} can be thought of as modified fringing field capacitances added to each of the nodes in the list, while C_{12}^{gi} is the mutual coupling capacitance added in shunt to the pairs of nodes in the list.

For a single plane-pair geometry discretized with M rows and N columns, and if S_{Ci} contains r_i pairs of nodes, the ith capacitive gap correction can be expressed in terms of the following equation:

$$\overline{\overline{Y}}_{cg,i} = \overline{\overline{P}}_i \overline{\overline{Y}}_{cg,i}^P \overline{\overline{P}}_i^T \tag{116}$$

where $\overline{\overline{Y}}_{cg,i}^P$ is an $MN \times MN$ block-diagonal matrix whose first $2 \times r_i$ elements are given by:

$$\jmath\omega \begin{pmatrix} \overline{\overline{C}}_{gi} & & \\ & \ddots & \\ & & \overline{\overline{C}}_{gi} \end{pmatrix} \tag{117}$$

with zeros elsewhere.

$\overline{\overline{\mathrm{P}}}_i$ is a $MN \times MN$ permutation matrix. The entries of the permutation matrix are determined by the node numbers in S_{Ci}. The row corresponding to the node $S_{Ci}(m,n)$ is given by $e_{(m-1)+n}$, where $e_{(m-1)+n}$ is the $(m-1)+n^{th}$ row of the identity matrix. The purpose of $\overline{\overline{\mathrm{P}}}_i$ is to permute the rows and columns of $\overline{\overline{\mathrm{Y}}}_{cg,i}^{P}$ such that $\overline{\overline{\mathrm{Y}}}_{cg,i}$ results in the correct connection of the capacitve gap correction. The other rows of $\overline{\overline{\mathrm{P}}}_i$ are irrelevant since they will be multiplied with zeros.

Similarly, another list S_{Li} is created, with four ordered node numbers per row of the list. These four node numbers correspond to the node numbers of the cells on parallel to and on either side of the slot. In the example, S_{Li} contains 2 rows which are:

$$S_{L1} = \begin{pmatrix} 7 & 13 & 8 & 14 \\ 8 & 14 & 9 & 15 \end{pmatrix} \tag{118}$$

The four nodes in each row of S_{Li} are the nodes to which the inductive gap correction elements are to be connected. For the same discretization of M rows and N columns, with t_i rows in S_{Li}, the ith inductive gap correction can be expressed by the following equation:

$$\overline{\overline{\mathrm{Y}}}_{lg,i} = \overline{\overline{\mathrm{Q}}}_i \overline{\overline{\mathrm{Y}}}_{lg,i}^{P} \overline{\overline{\mathrm{Q}}}_i^{T} \tag{119}$$

Here, the first $2t_i$ rows of $\overline{\overline{\mathrm{Y}}}_{lg,i}^{P}$ are block tri-diagonal and are given by:

$$\frac{1}{j\omega} \begin{pmatrix} \overline{\overline{L}}_{gi}^{-1} & -\overline{\overline{L}}_{gi}^{-1} & & & \\ -\overline{\overline{L}}_{gi}^{-1} & 2*\overline{\overline{L}}_{gi}^{-1} & -\overline{\overline{L}}_{gi}^{-1} & & \\ & \ddots & \ddots & \ddots & \\ & & & -\overline{\overline{L}}_{gi}^{-1} & \overline{\overline{L}}_{gi}^{-1} \end{pmatrix} \tag{120}$$

with zeros elsewhere.
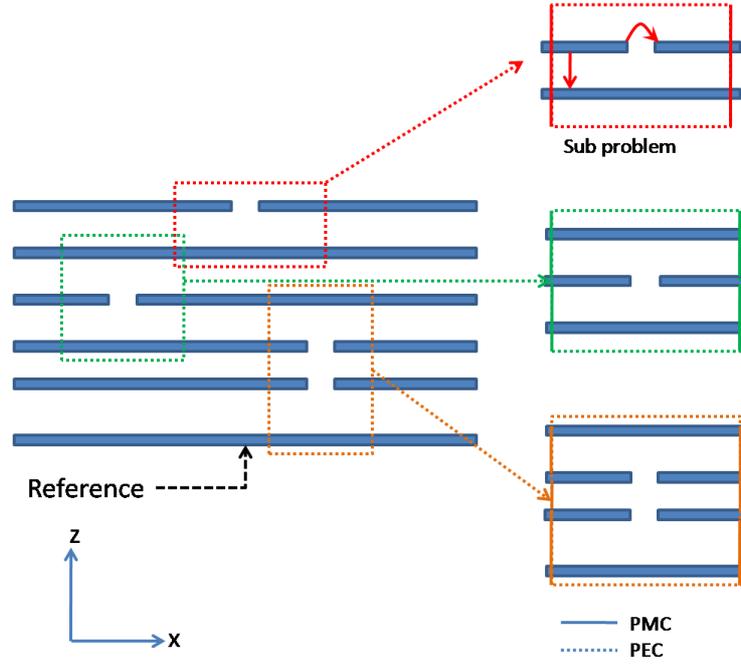
Figure 70. Multilayer geometry with multiple slots.

$\overline{\overline{Q}}_i$ is a $MN \times MN$ permutation matrix, the entries of which are determined by the node numbers in S_{Li}. The row corresponding to the node $S_{Li}(m, n)$ is given by $e_{(m-1)+n}$, which has been defined earlier.

Thus, the final admittance matrix including the gap corrections can be written as

$$\overline{\overline{Y}}_{PGA} = \overline{\overline{Y}} + \sum_{i=1}^{k} \left(\overline{\overline{Y}}_{cg,i} + \overline{\overline{Y}}_{lg,i} \right) \tag{121}$$

where $\overline{\overline{Y}}$ is the admittance matrix from M-FDM given in (46). $\overline{\overline{Y}}$ in (46) is now replaced with $\overline{\overline{Y}}_{PGA}$.

4.2.4 Formulation for Multiple Plane-Pairs

The cross-section of a multiple plane-pair geometry containing several arbitrary slots is shown in Figure 70. The formulation to obtain the circuit elements for modeling the gap involves the following steps. For each cross-section, the locations of all the slots are found. Each of these slots can be locally analyzed, thus reducing the size of the problem that needs to be considered. This is illustrated in Figure 70, where the

three slots are shown with their local references, each of which is a problem domain for a 2D-electrostatic simulation.

The width of the domain for each of these sub-problems is made large enough such that the electric fields between the planes, far away from the slot is $z-$ dominant. This allows for the problem domain to be terminated in the lateral (x) directions using an open circuit (PMC) boundary.

The 2D capacitance and inductance matrices, $\overline{\overline{C}}_{2D}$ and $\overline{\overline{L}}_{2D}$, for each of these domains can be obtained as before. However, the parallel plate capacitance and inductance matrices, are obtained with respect to the local sub-problem, and are denoted as $\overline{\overline{C'}}_{pp}$ and $\overline{\overline{L'}}_{pp}$, respectively.

The equations for the gap augmentation elements are:

$$\overline{\overline{C'}}_{g} = \overline{\overline{C}}_{2D} - \overline{\overline{C'}}_{pp} \tag{122}$$

$$\overline{\overline{L'}}_{g} = \left[\overline{\overline{L}}_{2D}^{-1} - \overline{\overline{L'}}_{pp}^{-1}\right]^{-1} \tag{123}$$

The elements represented by $\overline{\overline{C'}}_{g}$ and $\overline{\overline{L'}}_{g}$ are obtained with reference to a local ground. While adding these elements to the admittance matrix, this local ground node is shifted to the system ground, using the procedure described in Section 1.6.

4.2.5 Computational Complexity

There are two overheads involved in the use of the PGA method. First, the calculation of the PGA elements requires electrostatic simulations. Second, the inclusion of the PGA elements increases the number of non-zeros of the system admittance matrix.

The first overhead is addressed by the fact that the PGA elements are frequency independant, and involve a relatively low cost 2D simulation. The second overhead needs to be considered in more detail. The bandwidth of the admittance matrix of a two layer problem discretized with N cells, without the addition of the PGA elements, is $\sqrt{N}$. In the natural ordering scheme that is employed in M-FDM, cell (i, j) has

the node number $\sqrt{N}(j-1) + i$. Circuit elements are added that couple cell (i, j) with cells $(i \pm 1, j)$ and $(i, j \pm 1)$. Thus, the maximum bandwidth in the admittance matrix is $\sqrt{N}$.

However, with the addition of the PGA elements, cell (i, j) can be coupled, in the worst case, to cell (i, mj) where m is the number of cells required to discretize the slot. If S is the width of the slot, and w is the discretization width,

$$m = \frac{S}{w} \tag{124}$$

Thus, the computational complexity with the addition of the PGA models increases from $O(N^2)$ to $O(m^2 N^2)$, using a banded matrix solver, which is essentially the worst case. A mitigating factor is that m is likely to be small, given that PGA models need not be included for wide slots (slot width $> 10\times$ substrate height). In typical cases, m lies between 1 and 5. Recalling that with the nested dissection reordering algorithm, the computational complexity is $O(N^{1.5})$ for unaugmented case. This provides a lower bound.

4.3   Test Cases and Results
4.3.1   EBG Structure

The insertion loss results for the AI-EBG of Figure 65(a) are shown in Figure 71. The results from M-FDM are compared with results from a commectially available 2.5D Method-of-Moments (MoM) based solver and from measurements. Again, the application of the fringe and gap corrections clearly improves accuracy. In terms of simulation time, M-FDM was about 2700X faster than the commercial tool.

4.3.2   RF Type Examples

The PGA method uses significant insight from transmission line theory. One important step in the validation of the PGA method is to check the results obtained for structures which are commonly seen in RF circuits, such as coupled lines. The first example of this type that is being considered is a pair of coupled lines intersecting in
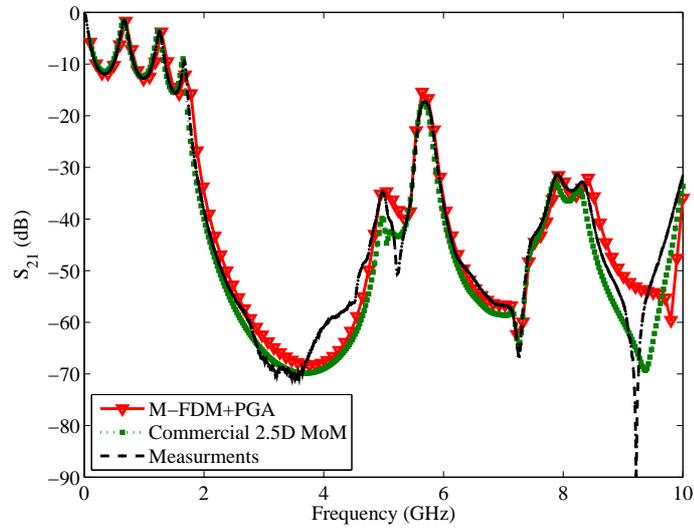
Figure 71. Insertion loss (dB) for structure in Figure 65(a) with fringe and gap models.
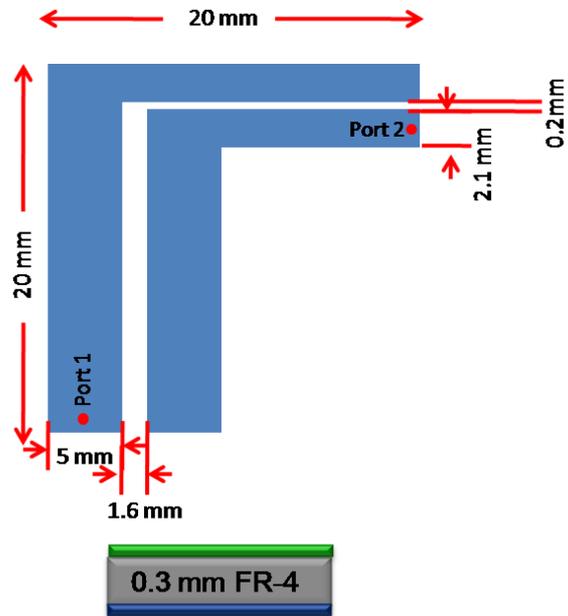
Figure 72. Geometry of coupled lines with a bend.
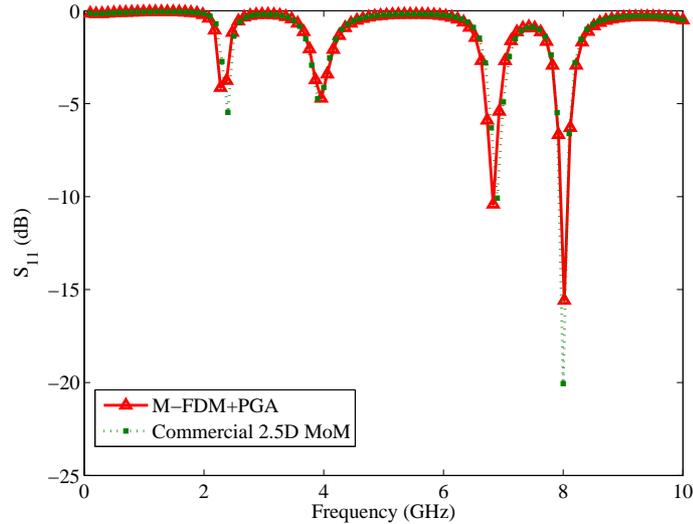
Figure 73. Return loss of structure in Figure 72.

a 90 degree bend, along wih a change in width of the lines, as shown in Figure 72. The return loss and insertion loss results obtained from the M-FDM + PGA method are plotted in Figures 73 and 74, and show good correlation to EM simulations. A critical difference between the PGA method and comparable equivalent circuit-based methods used in popular RF-oriented circuit simulators, such as ADS is that there is no requirement to to use a model for the bend.

The second RF-type example is a pair of coupled tapered lines. The reason for this choice is that the gap models need to be applicable over a wide range of gap separations. In this example, shown in Figure 75, the gap spacing varies from 0.3 mm (equal to the height of the substrate) all the way upto 5.4 mm (18 times the height of the substrate). The return loss and insertion loss are plotted in Figures 76 and 77. The M-FDM + PGA method shows good correlation to the results from the commercial MoM simulator.

4.3.3 Mixed Signal Board

Another test case is that of a mixed signal board with split planes separating the digital module with an FPGA and an RF transceiver module. The board layout is
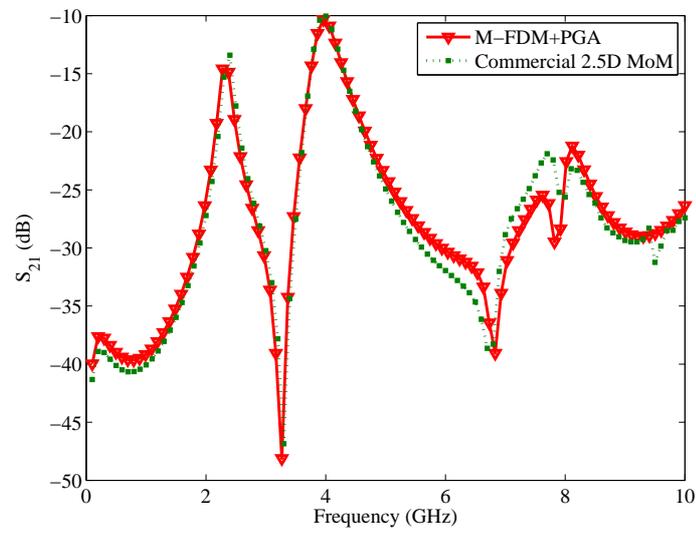
Figure 74. Insertion loss of structure in Figure 72.
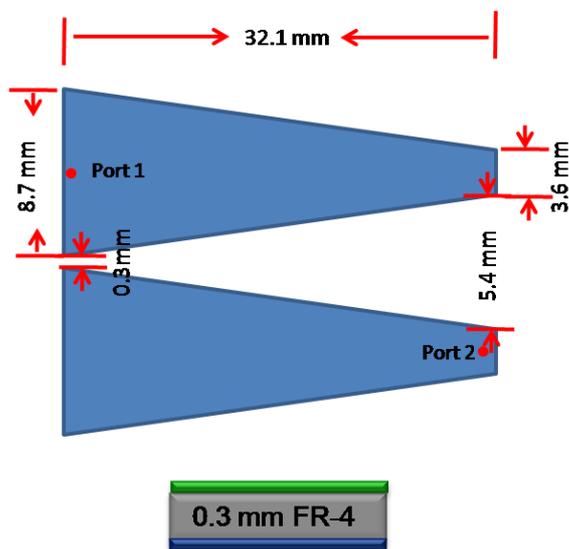
Figure 75. Geometry of coupled tapered lines.
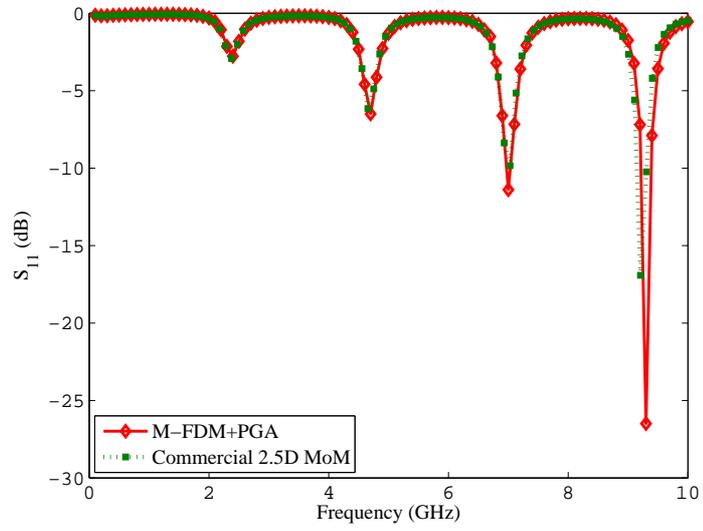
Figure 76. Return loss of structure in Figure 75.
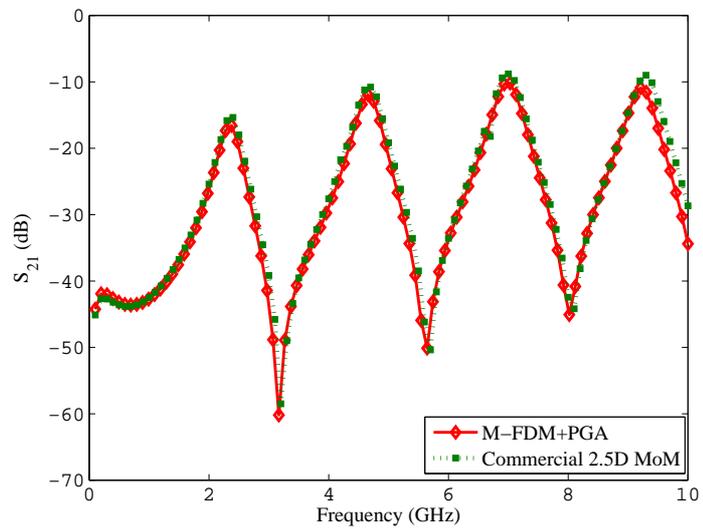
Figure 77. Insertion loss of structure in Figure 75.
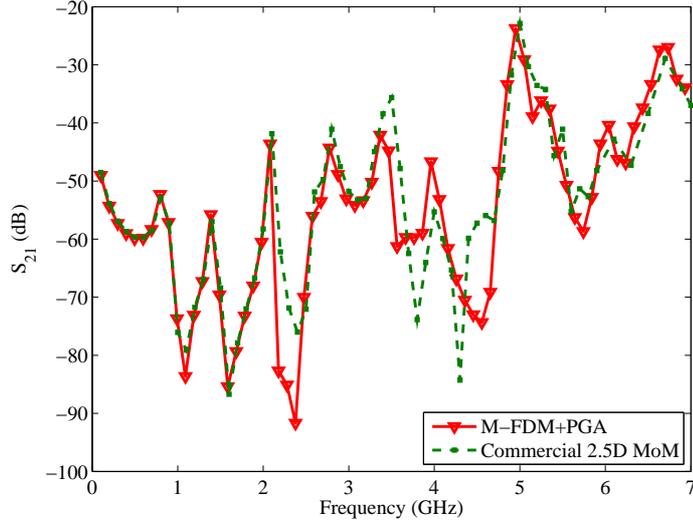
Figure 78. Insertion loss of structure in Figure 62.

shown in Figure 78(a). The dielectric thickness is 200 μm. Ports 1 and 2 are placed at the location of the FPGA and the RF transceiver respectively. Noise generated by the FPGA can couple through the PDN and cause degradation in the performance of the RF module. From the insertion loss result shown in Figure 78(b), it can be seen that significant coupling occurs at 2.1, 2.8, 3.5 and 5 GHz. Also, it can be seen from Figure 78(b) that the results from M-FDM and the commercial MoM tool are well correlated. The time per frequency sample for M-FDM was 3s as compared to 340s for the commercial tool, which represents a speed up of 113X.

4.3.4   Multilayered Examples

Three variations of a slot running through a $20mm \times 20mm$ multilayer package have been considered in Figure 79. Figures 79(a) - 79(c) show the cross-sections of the examples, also showing the location of the slot. The layout of the layer containing the slot is shown in Figure 79(d), along with the location of the ports.

In the first case, shown in Figure 79(a), the slot runs on the top layer, and is treated as a microstrip-type slot. The insertion loss of between the ports is shown in Figure 80, and has been compared with a commercially available FEM-based tool,

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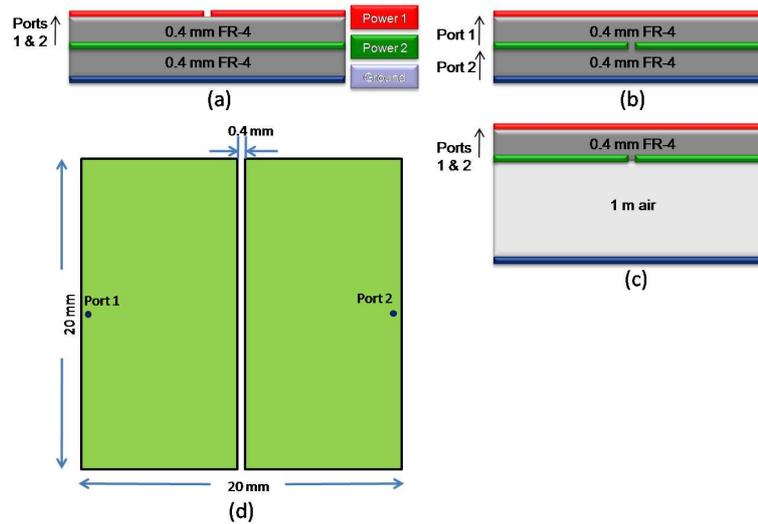
Figure 79. Cross-section (a)Microstrip type (b)Symmetric stripline (c)Asymmetric stripline, and (d)Layout.

and shows good correlation.

The slot is next placed on the middle layer, sandwiched symmetrically between two solid planes, as shown in Figure 79(b). The second port is now relocated between layers Power2 and Ground, and the insertion loss between the ports has been plotted in Figure 81. The results from M-FDM + PGA compare well with the results from the commercial tool.

An important test of the proposed M-FDM + PGA scheme is for the hypothetical case where the dielectric height between layers Power2 and Ground is made large (say 1m), and filled with air. For this case, shown in Figure 79(c), the insertion loss should approximate the results shown in Figure 80. This is what is observed, as shown in Figure 84.

The final multilayer test case contains overlapping slots on the top two layers. The cross-section and layout of the structure are shown in Figures 83. The magnitude of the insertion loss is shown in Figure 84, and shows good correlation as compared to the commercially available tool.
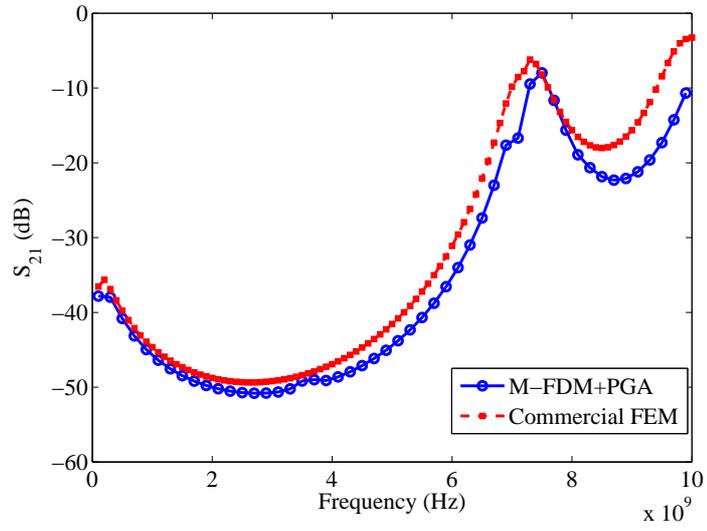
Figure 80. Insertion loss of structure in Figure 79(a).
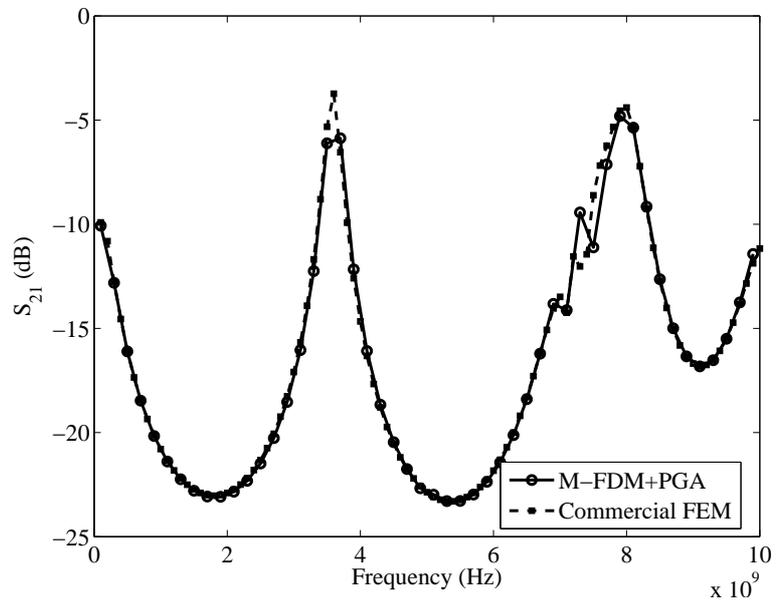
Figure 81. Insertion loss of structure in Figure 79(b).

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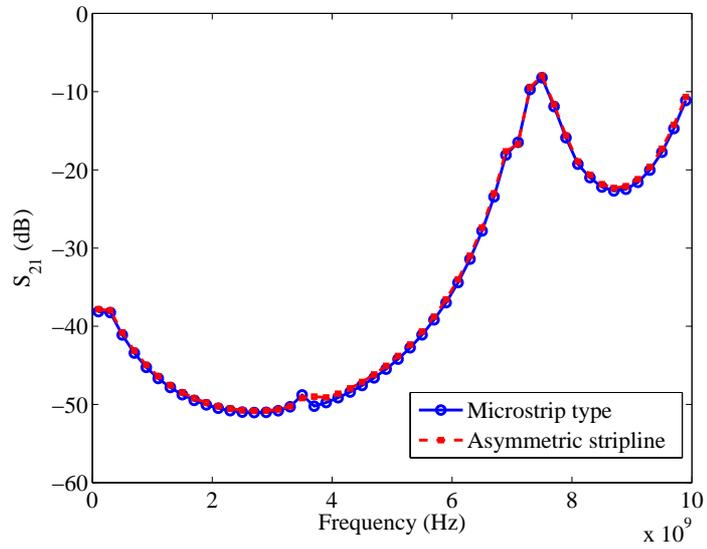
Figure 82. Insertion loss of structure in Figure 79(c).
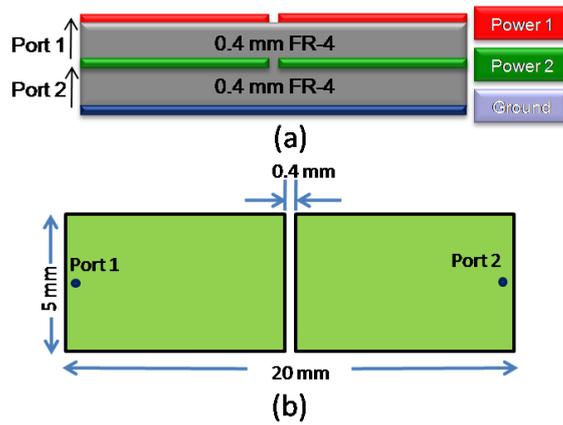
Figure 83. Test case containing overlapping slots (a) Cross-section (b)Layout.
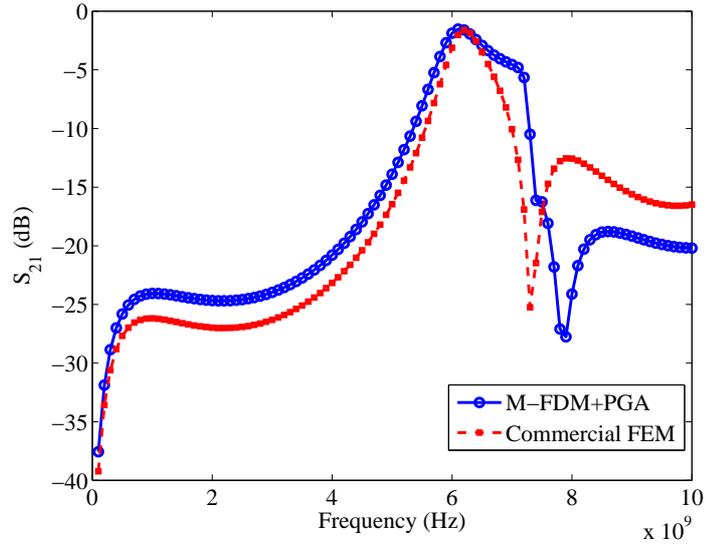
Figure 84. Insertion loss of structure in Figure 83.

4.3.5 Comparisons with Measurments

Test vehicles to validate the PGA method were manufactured by Panasonic. These test vehicles contained two metal layers with a solid ground plane, and a split plane on the top layer. The two types of test vehicles are shown in Figures 85(a) and 85(b), labeled Type 1 and Type 2, respectively.

The Type 1 structures had a slot that separated the top layer into two identical, rectangular, regions; The Type 2 structure, contained $x-$ and $y-$ directed slots. Three different slot widths were also fabricated in each type; these widths were 100 um, 200 um and 300 um.

The model to hardware correlation for the insertion loss for the resulting 3 variations of the Type 1 and Type 2 test vehicles are shown in Figures 86. As can be seen from the results, there is good model to hardware correlation.

4.4 Conclusions

As more and more devices are made multifunctional, it is necessary to design power distribution networks that can support multiple voltage levels. The most common
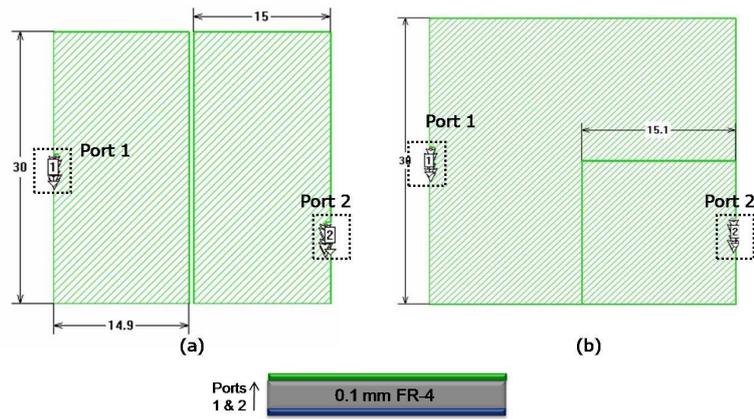
Figure 85. Manufactured test vehicles with variable slot widths (a)Type 1 and (b)Type 2.

method of isolating these multiple voltage domains is by the use of slots. These slots, while providing DC isolation, may not be able to isolate the voltage domains from high frequency noise coupling. To model this effect using M-FDM, the PGA method has been proposed. The method only couples unit cells adjacent to the slot. The resultant model provides a sufficient level of accuracy, as demonstrated by the various simulation and measurement results.
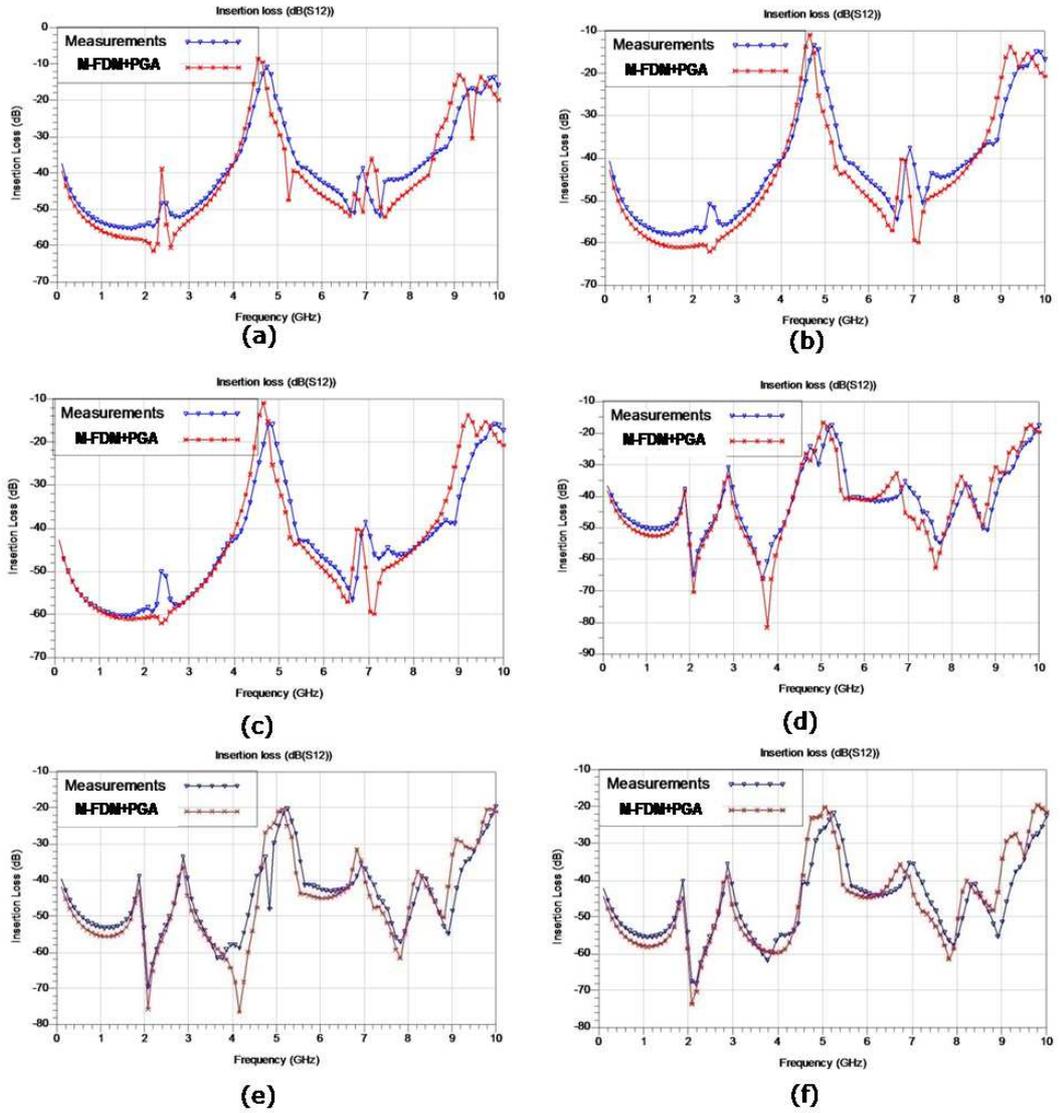
Figure 86. Insertion loss of structure in Figure 85; Type 1 with slot width (a)100 μm **(b)200** μm **(c)300** μm**; and Type 2 with slot width (a)100** μm **(b)200** μm **(c)300** μm**.**

CHAPTER 5

MODELING TRANSMISSION LINES WITH NON-IDEAL POWER/GROUND PLANES USING M-FDM

5.1 Introduction

Transmission structures on package are electrically long. Hence distributed effects such as delay need to be accounted for. Also, the return paths for the traces on package are the power and ground planes. It is incorrect to simply obtain the frequency response of the transmission line under the assumption that all of these return paths are at the same potential. For example, for a stripline sandwiched between a power and ground pair, the two return paths are not DC connected. Hence, it is essential to analyze the transmission line in the context of its non-ideal return paths.

5.1.1 Non-ideality of Return Paths

In Figure 87, a stripline is shown between two reference planes. While in general it is assumed that the reference planes are at the same potential, this may not necessarily be the case. In this figure, the potentials of the two reference planes are the same because of the via wall shorting the two references together. Thus, this is just a two conductor problem, and only one TEM mode of propagation exists. This *stripline mode* is visualized in the figure.

Shorting the two references is viable only if the planes are assigned the same DC potential. For example, the two planes both need to be assigned ground or VDD. If
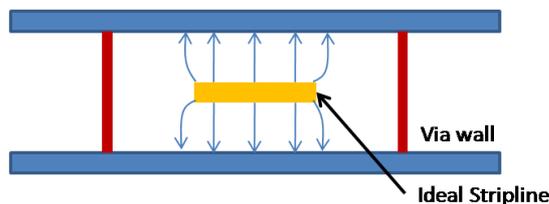
Figure 87. Ideal stripline mode.

Figure 88. Parallel plate mode of propagation in stripline with non-ideal references.

one is VDD and the other is ground, the situation results in a three conductor problem, as shown in Figure 88. In this case, in addition to the aforementioned stripline mode, another TEM mode called the *parallel plate mode*, visualized in Figure 88 may also propagate.

In general, for an $m+1$ conductor system, m TEM or quasi-TEM modes can exist. This can lead to significant signal integrity problems in high speed digital systems. This is because any actual wave propagating in the system can be expressed as a sum of the possible propagating modes. For the stripline in Figure 88, the returns currents of the stripline are distributed between the top and bottom planes. Since these planes are not forced to be at the same potential, this can excite a parallel-plate mode. This is called *mode conversion*, and in this case, mode conversion leads to ground bounce. Vice-versa, SSN in the system causes ground bounce, and this ground-bounce can be coupled to the stripline, corrupting the integrity of the signals in the system. Thus, simple transmission line models which do not model the effect of the non-ideality of the return paths will lead to incorrect simulation results, and are inadequate for performing a system level simulation.

The general method for solving this problem involves the theory of modal decomposition, which was discussed earlier, in Section 1.7. The contribution of this work is the extension of prior work [35][17][36][37][38][39] to allow the integration of transmission lines with M-FDM.

Figure 89. Four port transmission line model.

5.1.2 Prior Work with Transmission Line Referencing

The following transmission line configurations are the most common, on board, package and chip:

1. Microstrip

2. Stripline

3. Coplanar waveguide

In the past, an intuitive understanding of the return currents have been used to obtain equivalent circuit models [17]. These circuit models rely on a 4-port model of the transmission line. The input and output ports of the line are extended with two more ports, the input and output references as shown in Figure 89.

Models for the signal line referenced to the non-ideal power/ground planes are shown in Figure 90. The simplest case is that of the microstrip, shown in Figure 90(a). All of the return currents of the microstrip flow on the plane immediately below it. Thus, the reference ports of the transmission line model of the microstrip are connected to the nodes on the plane underneath the line, as shown in the figure.

However, for the stripline (Figure 90(b)), some of the return currents flow on the top reference, while the rest flows on the bottom. Thus the equivalent circuit representation is constructed by modeling the stripline by two transmission lines, whose input and output signal ports are shorted. The reference nodes of one of the transmission lines are connected to nodes on the top plane, while the reference nodes of the other are connected to nodes on the bottom plane (which in this case is
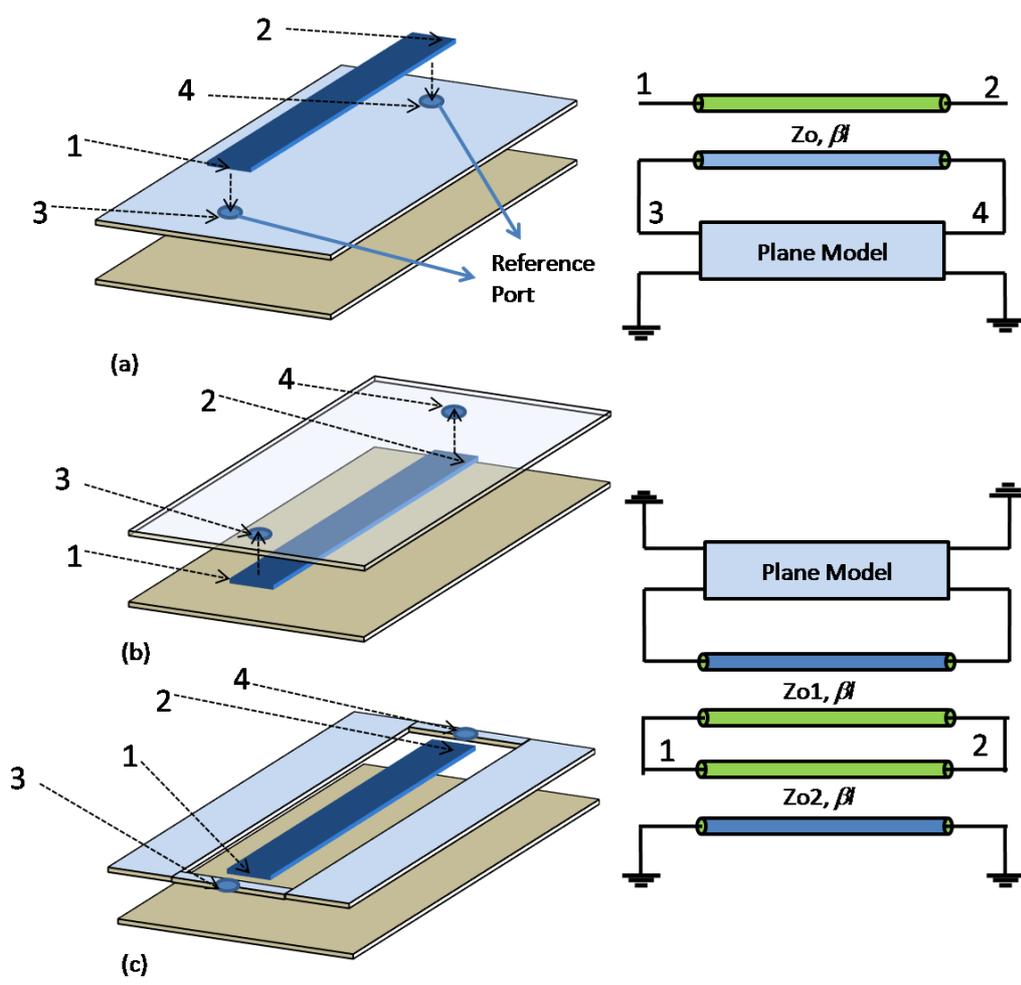
Figure 90. Transmission line models for (a) Microstrip (b) Stripline (c) Conductor-backed CPW with shorted side-grounds.
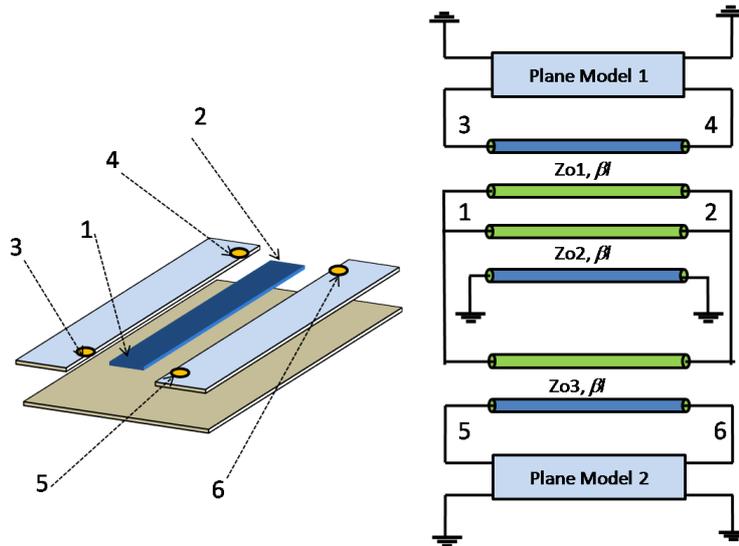
Figure 91. Transmission line models conductor backed CPW-line with shorted side grounds.

assumed to be an ideal ground). For the stripline, it is possible to analytically obtain the characteristic impedance of the two transmission lines in the model simply based on the ratio of the dielectric heights in the cross-section.

A conductor backed CPW line with shorted side grounds is shown in Figure 90(c). As in the stripline case, this configuration also consists of a signal conductor and two reference conductors, constituting a three conductor system. The two side grounds are grouped together and considered to be one conductor because they are shorted. Therefore, it is intuitive to consider that the return currents would divide between the bottom conductor and the side grounds. Hence, it should be possible to construct a model for this case which is identical in form to the model for the stripline. However, there are no analytical approaches available to obtain the characteristics of the two transmission lines in the model. The work in [40] requires a 2D-simulation to obtain a model equivalent to that shown in the figure.

If the side-grounds of the CPW line are not shorted, as is shown in Figure 91, then the resulting system contains four conductors, with three possible propagating modes. It may be possible, therefore, to obtain an equivalent circuit representation

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consisting of three transmission lines, each referenced to one of the three grounds. The derivation of this model is one of the goals of this chapter. The contributions of this chapter are the following:

1. Derivation of the equivalent circuit representation of the four conductor CPW-line with unconnected side-grounds.

2. Formulation for obtaining a model for different transmission line configurations and their non-ideal references, where the reference planes are modeled with M-FDM.

The rest of this chapter is organized as follows. A brief overview of the SI-PI co-simulation flow is discussed in Section 5.2. The equivalent network models for microstrip, stripline and CPW transmission line structures obtained using modal decomposition are described in Section 5.3. The integration of these equivalent circuit models and M-FDM is detailed in Section 5.5. This integrated method is applied to several test cases, the results of which are presented in Section 5.6, followed by conclusion in Section 5.7.

5.2 Simulation Flow

The methodology proposed in this thesis for the integration of the signal distribution network (SDN) and the PDN (shown in Figure 92) provides an efficient and reliable way of analyzing SiP structures by using novel modeling and simulation techniques. The initial steps in the methodology (shown using shaded boxes) are the same as those shown in Figure 16 and use existing techniques for layout extraction and interconnect modeling. However, the proposed methodology uses M-FDM for modeling the PDN. Modal decomposition is used for the integration of transmission line response with the PDN response from M-FDM. This ensures that all the coupling between the SDN and the PDN is accurately captured in the simulation. The integrated system response

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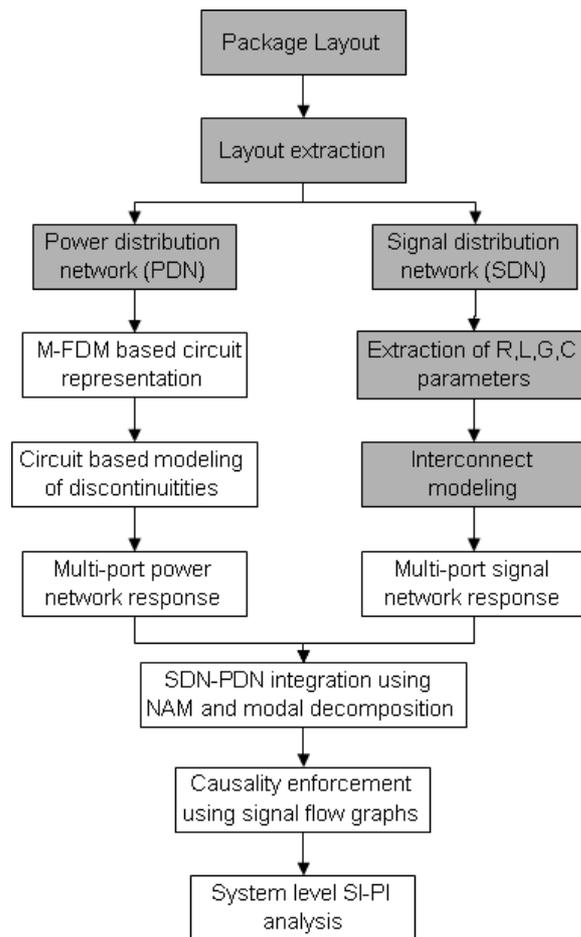
Figure 92. Proposed methodology for system level SI-PI analysis.

can then be transformed to obtain a reduced-order model of the system. This reduced order model captures all the system parasitics and can be efficient simulated in the time domain using signal flow graphs. The signal flow graph formulation includes a delay extraction technique that enables the enforcement of causality on the transient simulation [41][42][43].

Since separate analyses of the SDN and the PDN fails to account for the coupling between the two modules, the two responses need to be integrated to perform an accurate system level analysis. This integration can be performed using the admittance matrices of the two modules along with the stamp rule [44]. The process involves conversion of the SDN response into its equivalent model which is then stamped onto the admittance matrix of the PDN.

5.3 Modal Decomposition

All three types of configurations have similar modal representations. For a three conductor system consisting of two parallel plates (power/ground) and a signal conductor, there are two possible (quasi) TEM modes. Intuitively, one of these TEM modes is the parallel-plate mode. The other mode is the mode that propagates when the signal conductor sees ideal returns. For example, for the stripline case, the two TEM modes are the parallel plate mode and the stripline mode.

The first mode, the parallel-plate mode, is defined by no current in the signal line. All the current flows on one of the planes and returns on the other. In the second mode, the signal line sees ideal references. This implies that the planes are at the same potential. Setting the bottom plane to be the reference, it can be seen that

$$\bar{I}(z) = \begin{pmatrix} I_p(z) \\ I_s(z) \end{pmatrix} = \overline{\overline{T}}_I \bar{I}_m(z) = \begin{pmatrix} 1 & a \\ 0 & b \end{pmatrix} \begin{pmatrix} I_{par}(z) \\ I_{sig}(z) \end{pmatrix} \tag{125}$$

$$\overline{V}(z) = \begin{pmatrix} V_p(z) \\ V_s(z) \end{pmatrix} = \overline{\overline{T}}_V \overline{V}_m(z) = \begin{pmatrix} c & 0 \\ d & 1 \end{pmatrix} \begin{pmatrix} V_{par}(z) \\ V_{sig}(z) \end{pmatrix} \tag{126}$$

where the subscripts p and s represent the line parameters of the top plane and the

signal line, respectively. The subscripts *par* and *sig* represent the modal parameters of the top plane and the signal line.

Using the formulation from ([1]), it can be shown that to diagonalize the per unit length inductance and capacitance matrices, the following relations hold:

$$a = -\frac{L_{sp}}{L_{pp}} b \tag{127}$$

$$d = \frac{L_{sp}}{L_{pp}} c \tag{128}$$

These terms are obtained from the per-unit-length inductance matrix, $\overline{\overline{L}}$.

$$\overline{\overline{L}} = \begin{pmatrix} L_{pp} & L_{sp} \\ L_{sp} & L_{ss} \end{pmatrix} \tag{129}$$

L_{pp} is the self-inductance of the top plane, while L_{sp} is the mutual-inductance between the signal line and the top plane. Defining

$$k = -\frac{L_{sp}}{L_{pp}} \tag{130}$$

, and scaling the modal transformation matrices,

$$\overline{\overline{T}}_V(z) = \begin{pmatrix} 1 & 0 \\ -k & 1 \end{pmatrix} \tag{131}$$

$$\overline{\overline{T}}_I(z) = \begin{pmatrix} 1 & k \\ 0 & 1 \end{pmatrix} \tag{132}$$

The equivalent 4-port model of the signal line can be obtained as shown in Figure 93. Z_{par}^c and Z_{sig}^c are the characteristic impedances obtained from the modal per-unit-length impedance and admittance matrices $\overline{\overline{Z}}_{\mathbf{m}}$ and $\overline{\overline{Y}}_{\mathbf{m}}$, respectively. This electrical model can be derived in terms of the indefinite admittance matrix.

$$\overline{I} = \begin{pmatrix} I_p^i \\ I_p^o \\ I_s^i \\ I_s^o \end{pmatrix} = \begin{pmatrix} 1 & 0 & k & 0 \\ 0 & 1 & 0 & k \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} I_{par}^i \\ I_{par}^o \\ I_{sig}^i \\ I_{sig}^o \end{pmatrix} \tag{133}$$
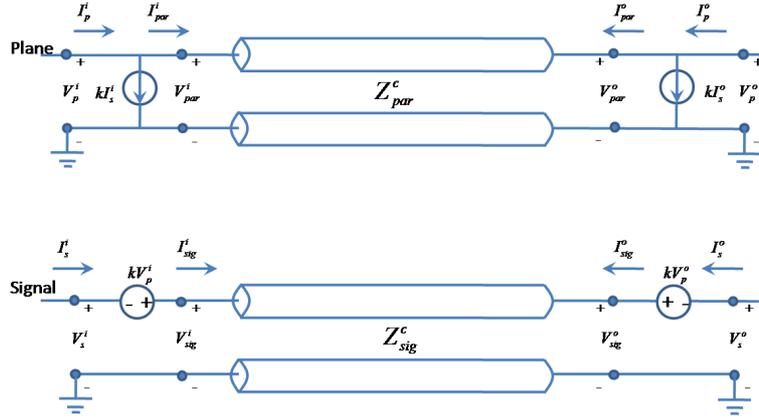
Figure 93. 4-port electrical model of signal line.

$$
\begin{pmatrix} I^i_{par} \\ I^o_{par} \\ I^i_{sig} \\ I^o_{sig} \end{pmatrix} = \begin{pmatrix} \overline{\overline{\mathbf{Y}}}_{\mathbf{par}} & 0 \\ 0 & \overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} \end{pmatrix} \begin{pmatrix} 1\ 0\ 0\ 0 \\ 0\ 1\ 0\ 0 \\ k\ 0\ 1\ 0 \\ 0\ k\ 0\ 1 \end{pmatrix} \begin{pmatrix} V^i_p \\ V^o_p \\ V^i_s \\ V^o_s \end{pmatrix}
\tag{134}
$$

Substituting (134) in (133),

$$
\begin{pmatrix} I^i_p \\ I^o_p \\ I^i_s \\ I^o_s \end{pmatrix} = \begin{pmatrix} k^2\overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} + \overline{\overline{\mathbf{Y}}}_{\mathbf{par}} & k\overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} \\ k\overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} & \overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} \end{pmatrix} \begin{pmatrix} V^i_p \\ V^o_p \\ V^i_s \\ V^o_s \end{pmatrix}
\tag{135}
$$

To summarize the formulation leading to the above equation, the response of the plane $\overline{\overline{\mathbf{Y}}}_{\mathbf{par}}$ is obtained using M-FDM. $\overline{\overline{\mathbf{Y}}}_{\mathbf{sig}}$ is obtained from the modal per-unit-length matrices $\overline{\overline{\mathbf{Z}}}_{\mathbf{m}}$ and $\overline{\overline{\mathbf{Y}}}_{\mathbf{m}}$. The transformation matrices $\overline{\overline{\mathbf{T}}}_{\mathrm{V}}$ and $\overline{\overline{\mathbf{T}}}_{\mathrm{I}}$ are obtained from the actual per-unit-length inductance matrix $\overline{\overline{\mathbf{L}}}$, which is in turn obtained from the 2D electrostatic solver described in Section 3.2.2.

5.3.1 Microstrip

The microstrip line configuration is the simplest to analyze because the power plane acts as a shield between the fields associated with the microstrip line and between the parallel plate conductors. The resultant inductance matrix satisfies the following relationship:

$$
L_{sp} \simeq L_{pp}
\tag{136}
$$
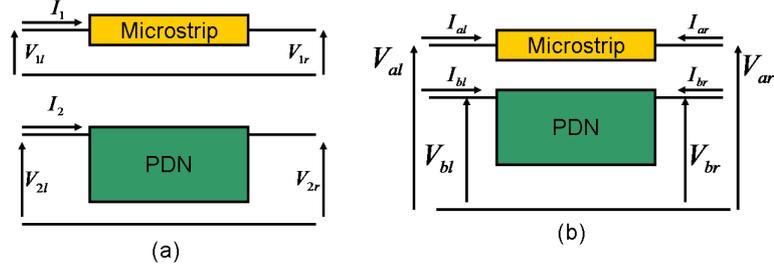
Figure 94. (a) Two-port model of microstrip over PDN (b) Equivalent four-port model with common ground reference.

where L_{sp} and L_{pp} are defined in (129). Thus, from (130), $k = -1$.

Hence, the indefinite admittance matrix representation for the microstrip configuration is given by:

$$
\begin{pmatrix} I_p^i \\ I_p^o \\ I_s^i \\ I_s^o \end{pmatrix} = \begin{pmatrix} \overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} + \overline{\overline{\mathbf{Y}}}_{\mathbf{par}} & -\overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} \\ -\overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} & \overline{\overline{\mathbf{Y}}}_{\mathbf{sig}} \end{pmatrix} \begin{pmatrix} V_p^i \\ V_p^o \\ V_s^i \\ V_s^o \end{pmatrix}
\tag{137}
$$

Interestingly, (137) can also be obtained by changing the reference plane of the microstrip line from the top-plane to the the bottom plane, as described in Section 1.6. In Figure 94(a), the two-port model of the microstrip line over a PDN is shown, with the combined four-port illustrated in Figure 94(b). The admittance matrix for the four-port is identical to admittance matrix derived using modal decomposition in (137).

5.3.2 Stripline

In the case of a stripline, the current on the signal line excites both the transmission line and parallel-plate modes. k can be obtained from the per-unit-length inductance matrix; However [35] has shown that the ratio $\frac{L_{sp}}{L_{pp}}$ can be obtained simply from geometrical parameters.

$$
\frac{L_{sp}}{L_{pp}} = \frac{h_1}{h_1 + h2}
\tag{138}
$$

where h_1 and h_2 are the substrate heights, as shown in Figure 95(a). This is true, however, only when the metal thickness is negligible when compared to the substrate
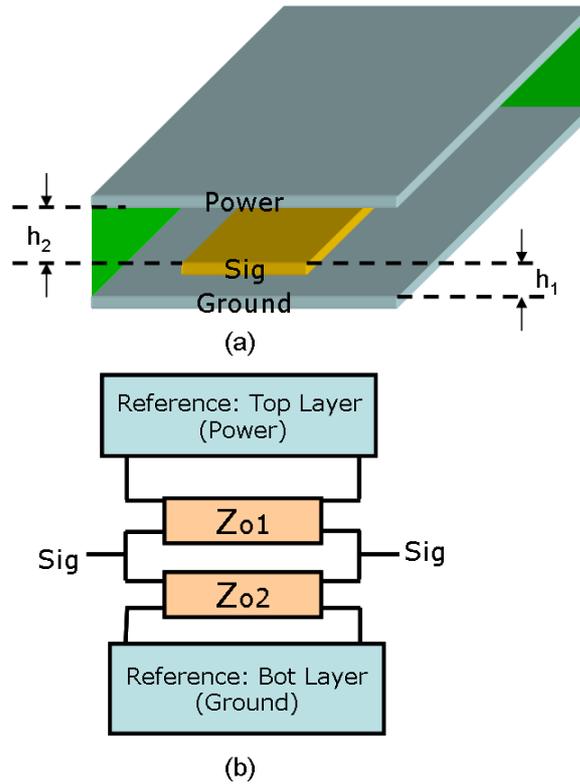
Figure 95. (a) 3D schematic of a stripline (b) Equivalent model.

Figure 96. Conductor backed co-planar waveguide cross section.

heights h_1 and h_2.

Substituting (138) in (135) leads to an admittance matrix which can be exactly represented in terms of the equivalent circuit model shown in Figure 95(b)[35].

5.3.3 Conductor Backed Co-planar Waveguide

The co-planar waveguide (CPW) structure is often used to reduce the coupling of noise in high speed bus structures. Also, due to high wiring density, it often becomes essential to route signal lines on power or ground layers. The cross-section of the CPW line is shown in Figure 96.

The starting point for the derivation of the equivalent circuit model for the CPW
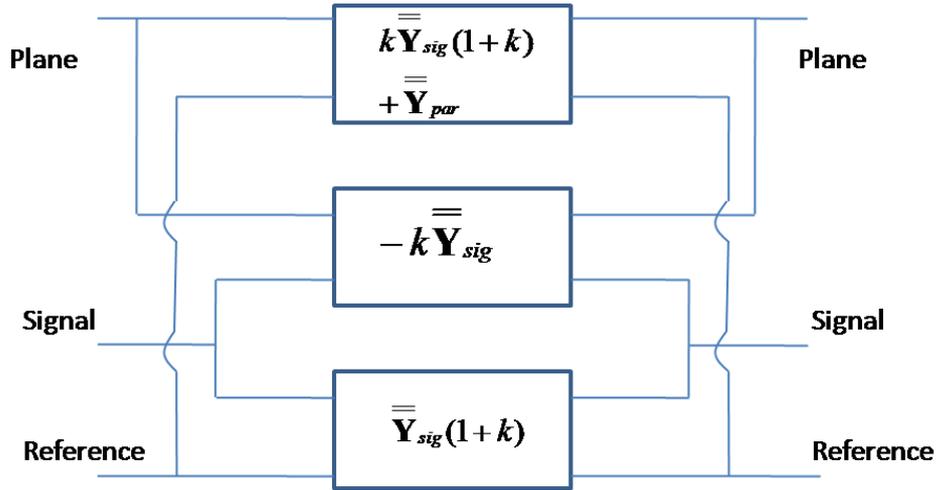
Figure 97. Four port equivalent circuit model for CPW line with shorted co-planar references.

line is (135). The work done in [40] assumes that the co-planar reference conductors (i.e. Power) are DC connected and are bridged at either end of the CPW line to ensure that there is no AC potential difference between them. However, this may not be the case. In such a case, it appears that the three conductor MTL equations that have been dealt with thus far may be insufficient, and the problem must be treated as a four conductor MTL. However, given the symmetry of the problem, a six-port model can be obtained.

The admittance matrix in (135) can be exactly represented in terms of the equivalent circuit shown in Figure 97. This model assumes that the co-planar references for the CPW line are at the same AC potential. From symmetry, the six-port model for the case of non-ideal co-planar returns can be constructed as shown in Figure 98.

5.3.4 Summary of Modal Decoposition Techniques

The equivalent circuit representation for the various transmission line configurations are controlled by the value of the coupling factor k. Figure 99 summarizes the results obtained thus far. The simplest cases are for the microstrip and stripline, where the value of k can be obtained analytically. For cases where the substrate may
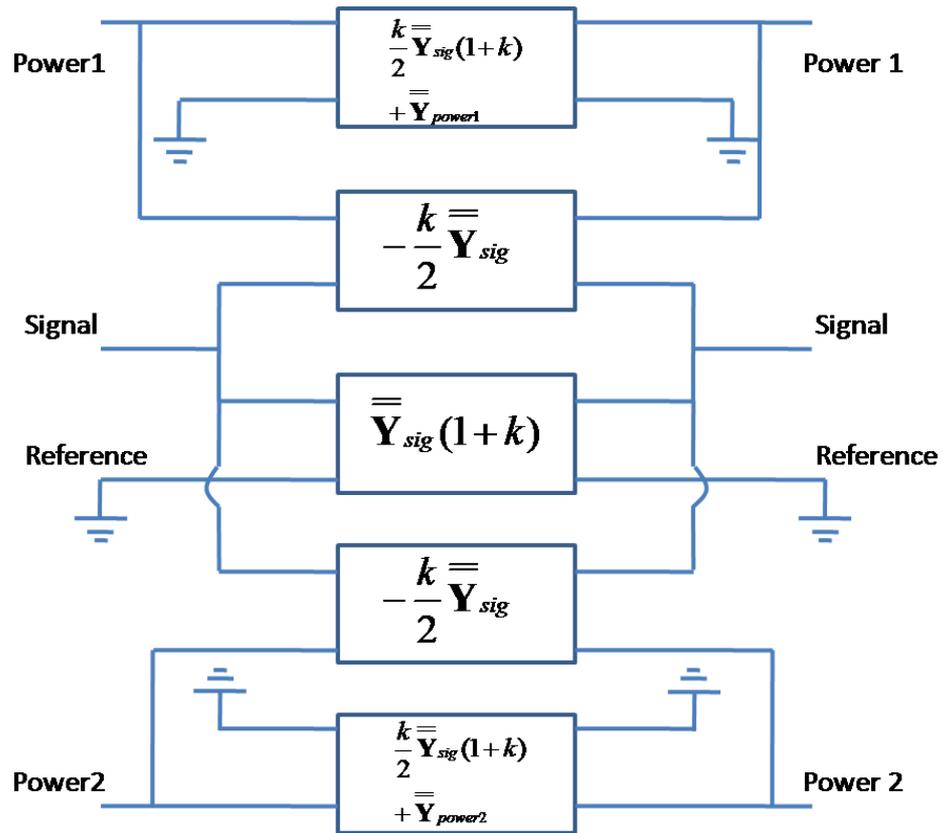
Figure 98. Six port equivalent circuit model for CPW line.

Transmission-line type	Coupling factor, k, $\varepsilon_1 = \varepsilon_2$	Coupling factor, k, $\varepsilon_1 \neq \varepsilon_2$
Microstrip	-1	2D solution required
Stripline	$-\dfrac{h_1}{h_1 + h_2}$	2D solution required
Conductor backed CPW with shorted side grounds	2D solution required	
Conductor backed CPW with unconnected side ground		
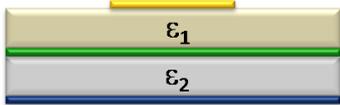
Figure 99. Summary of modal decomposition methods applied to different transmission-line configurations.

be inhomogeneous, however, the per-unit-length parameters of the line have to be calculated using a 2D electrostatic solver, like the formulation discussed in Section 3.2.2.

5.4 Port Reduction

Once the integration is complete, the line terminations and the other lumped components in the system can be added to the overall system matrix using the stamp rule. Since the transient response is often required only at particular locations in the system, the overall system matrix can be reduced to include ports only at those locations where the system is being excited or probed.

For a m-port overall system matrix that needs to be reduced to n (external) ports, the m-port Y-matrix is reordered such that the desired n-port locations appear in the top left corner of the matrix. This is shown in Equation 139 where Y_{ee} and Y_{ii} refer to the internal and external (required) ports respectively.

$$\begin{pmatrix} Y_{11} & \dots & Y_{m1} \\ \vdots & \ddots & \vdots \\ Y_{1m} & \dots & Y_{mm} \end{pmatrix} \rightarrow \begin{pmatrix} [Y_{ee}]_{n \times n} & [Y_{ei}]_{n \times (m-n)} \\ [Y_{ie}]_{(m-n) \times n} & [Y_{ii}]_{(m-n) \times (m-n)} \end{pmatrix} \tag{139}$$

From this reordered Y-matrix, the reduced n-port representation of the system is obtained using the equation:

$$[Y]_{n \times n} = Y_{ee} + Y_{ei} \left(-Y_{ii}^{-1} Y_{ie} \right) \tag{140}$$

5.5 Implementation Using M-FDM

The flowchart for the integration of transmission lines with M-FDM is shown in Figure 100. The initial steps are simply to mesh the geometry of the power/ground planes, and build the admittance matrix using M-FDM.

Next each transmission line in the geometry is broken up into segments which can be considered ideal, that is, the cross-section of the of the stack-up perpendicular to
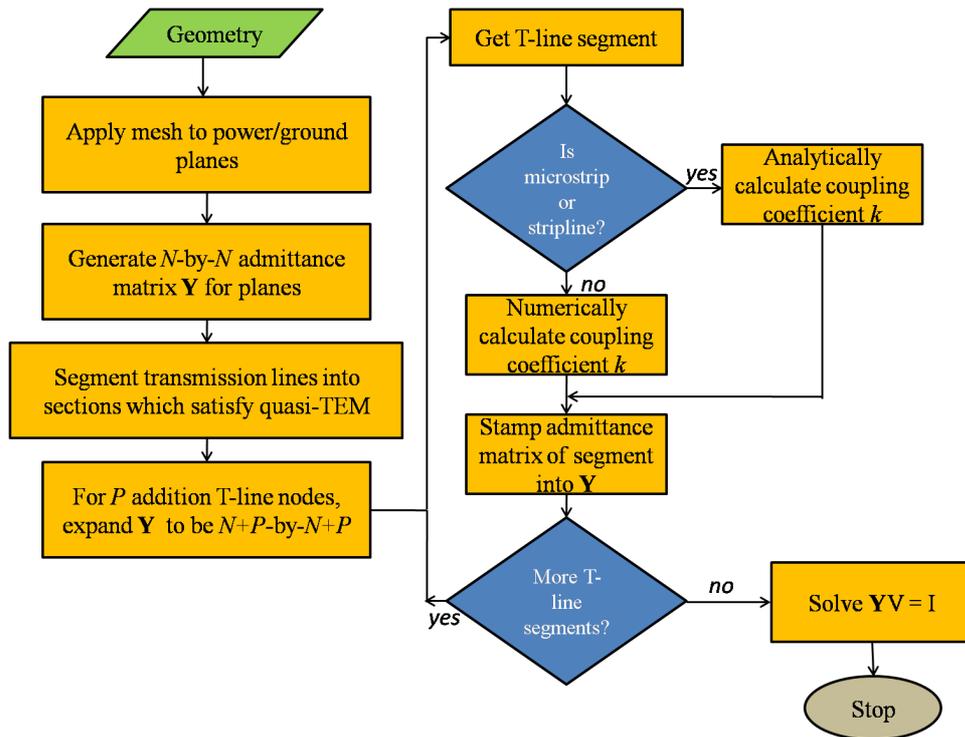
Figure 100. Flowchart for integrating transmission lines with M-FDM.
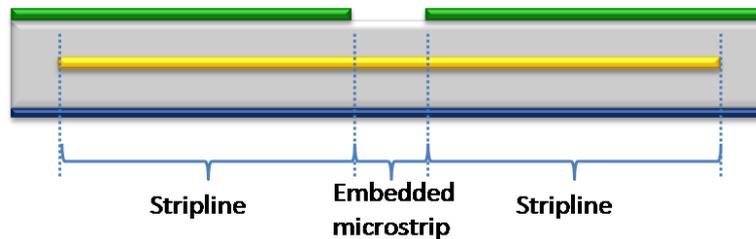
Figure 101. Stripline to embedded microstrip transition.

the direction of propagation must be the same within any given segment. This is required, for example, if one physical interconnect is routed as a stripline, as shown in Figure 101, but has a slot that removes a portion of the top plane.

The section of the line that is underneath the slot will have the characteristics of an embedded microstrip, and the location of the slot in the top plane is called a *return path discontinuity* or RPD. This RPD is important because the return currents for the stripline segments in the top plane will need to find another path across the discontinuity.

After obtaining the $N \times N$ admittance matrix $\overline{\overline{\mathbf{Y}}}$ from M-FDM, and if the interconnects in the structure can be segmented into q segments requiring P additional nodes, $\overline{\overline{\mathbf{Y}}}$ is expanded to be $(N + P) \times (N + P)$, where the nodes from $1 - P$ are allocated for the transmission line segments, and the nodes $(P+1) - (P+N)$ contain the original $N \times N$ admittance matrix of the PDN.

Element stamps are created for each of the transmission line segments. Each segment has two nodes representing the input and output nodes, and can have r nodes for the references. For microstrip, stripline, CPW with shorted side-grounds, and CPW with unconnected side-grounds, r can be 2, 4, 4 and 6, respectively.

The $r + 2$-port admittance stamp for each transmission line segment is added to the overall system matrix by inspection. For the example of a microstrip segment connected to the nodes $n1$ and $n2$ with reference nodes $n3$ and $n4$, the element stamp is given by the matrix in (137) after removal of $\overline{\overline{\mathbf{Y}}}_{\mathbf{par}}$ term from the second row and second column. Thus, using the stamp rule discussed in Section 1.6, the combined admittance matrix is given by

$$
\begin{pmatrix} \vdots \\ I_{n1} \\ \vdots \\ I_{n2} \\ \vdots \\ I_{n3} \\ \vdots \\ I_{n4} \\ \vdots \end{pmatrix}
=
\begin{pmatrix}
Y_{1,1}^{sig} & Y_{1,2}^{sig} & -Y_{1,1}^{sig} & -Y_{1,1}^{sig} \\
Y_{2,1}^{sig} & Y_{2,2}^{sig} & -Y_{2,1}^{sig} & -Y_{2,2}^{sig} \\
-Y_{1,1}^{sig} & -Y_{1,2}^{sig} & Y_{1,1}^{sig} + Y_{n1,n1}^{par} & Y_{1,2}^{sig} + Y_{n1,n2}^{par} \\
-Y_{2,1}^{sig} & -Y_{2,2}^{sig} & Y_{2,1}^{sig} + Y_{n2,n1}^{par} & Y_{2,2}^{sig} + Y_{n2,n2}^{par}
\end{pmatrix}
\begin{pmatrix} \vdots \\ V_{n1} \\ \vdots \\ V_{n2} \\ \vdots \\ V_{n3} \\ \vdots \\ V_{n4} \\ \vdots \end{pmatrix}
\tag{141}
$$

5.6 Test Cases and Results
5.6.1 Mixed Signal Board

The methodology described in prior sections has been implemented in a CAD tool. Simulations were performed to compare the methodology against full-wave simulations and measurements, and to demonstrate the scalability of the method. All simulations were performed on an Intel Xeon workstation with a 3.2 GHz processor and
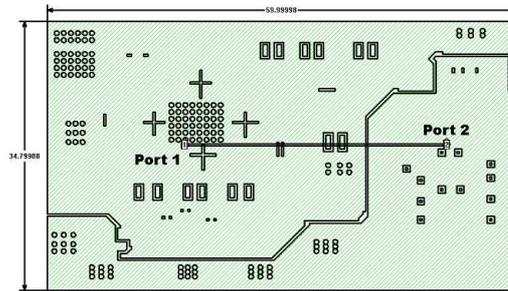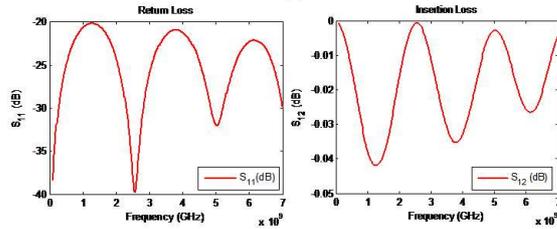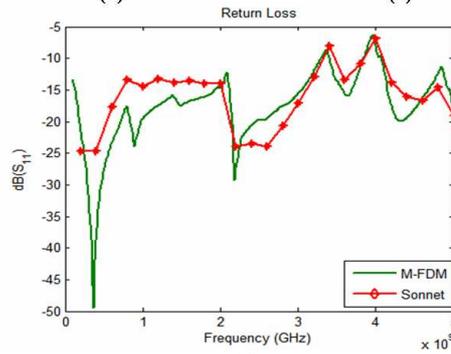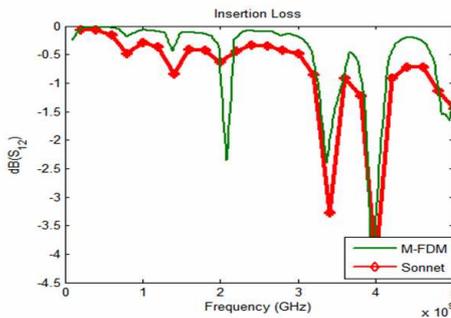
Figure 102. (a) Mixed signal board with transmission line traversing a slot (b) Return loss results - Ideal Microstrip (c) Insertion loss results - Ideal Microstrip (d) Return loss results (e) Insertion loss results.

3.5 GB of RAM. Full-wave simulations were performed with the method-of-moments based solver, Sonnet.

A mixed signal board of size 60mm × 34.8 mm is shown in Figure 102(a). A microstrip transmission line originates from an FPGA located near port 1, and connects to a low noise amplifier (LNA) at port 2. The microstrip, which is of length 34 mm, traverses over the slot separating the power islands of the two modules. The dielectric height between the power/ground planes was 300 μm, and between the signal and power planes is 200 μm. The dielectric was FR-4 with $\epsilon_r = 4.4$.

This example was simulated in Sonnet as well as M-FDM using a cell size of 0.3mm. In M-FDM, the PDN was simulated first. The transmission line was broken into three segments, with the first and last segment represented by a microstrip referenced to the power layer. The middle segment represents the section of the microstrip that is present above the slot and is hence reference to the ground layer. The results obtained from simulation are shown in Figures 102(b) - (e). Figures 102(b) and (c) show the case when the microstrip is assumed to be ideal. In this case, there are no discontinuities, and since the characteristic impedance is $\sim 54\Omega$, the dB(S_{12}) is very close to zero. However, when the microstrip is routed over the slot, the obtained return and insertion loss results are shown in Figures 102(d) and (e). In this case, the insertion loss is significantly higher.

As can be seen from the return loss and the insertion loss results, we are able to get good correlation between Sonnet and M-FDM. The Sonnet simulations required 800s per frequency point analyzed, while in M-FDM required 3.2s per frequency point. This represents a speedup of about 200X.

5.6.2 Microstrip Line Traversing a Slot

A 0.4 mm wide microstrip line traversing a 2.5 mm slot in the power plane is shown in Figure 103. The transmission line in this case is assumed to be an interconnect driven by a 533 MHz DDR II driver. In this case each power island is of size 125 mm
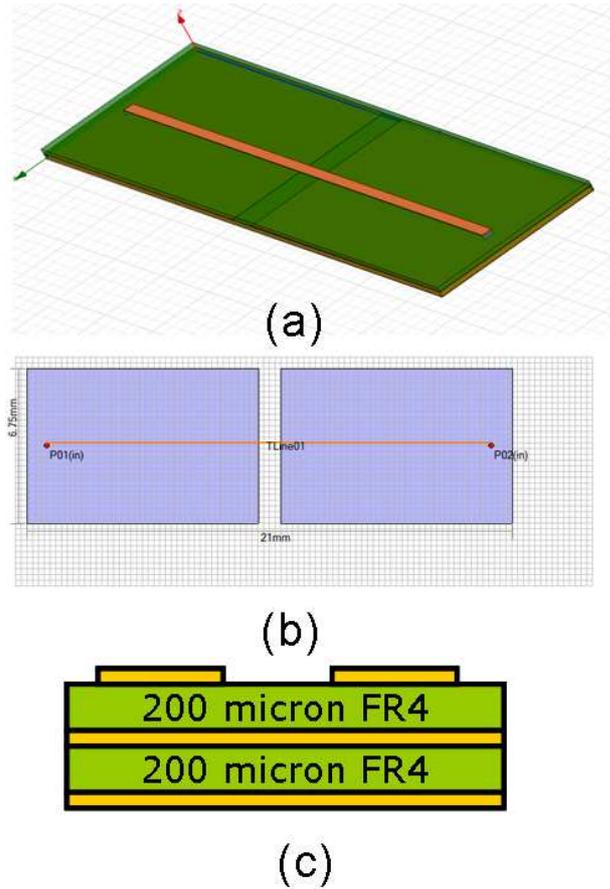
Figure 103. Top view of test case. Microstrip interconnects ports 1 and 2.

$\times$ 100 mm. The dielectric height between the microstrip line and the power plane is 0.2 mm. The dielectric height between the power and ground planes is 1 mm. A simple rectangular geometry is chosen since it is possible to analytically compute the resonant frequencies using the formula

$$f_{c_{m,n}} = \frac{1}{2\pi\sqrt{\mu\epsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{142}$$

where a and b represent the length and width of the rectangular geometry. Given a dielectric constant, ϵ_r, of 4.4, the first resonance occurs at 570 MHz. Figure 104 shows the insertion loss of the transmission line. It can clearly be seen that the resonance of the planes gives rise to significant insertion loss (-8dB). A method that can be used to suppress this resonance is by using decoupling capacitors with a self resonant frequency of around 570 MHz. Two such capacitors are placed at locations close to
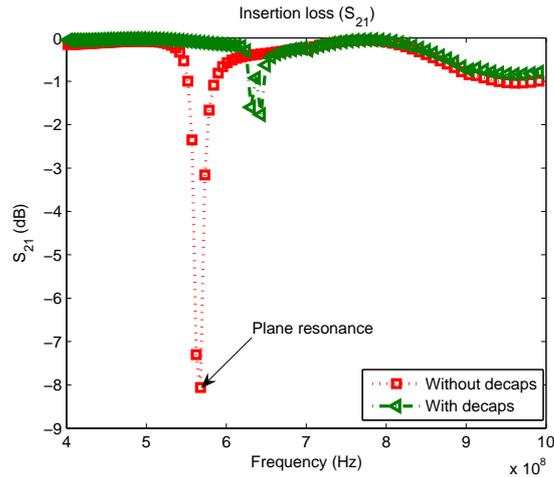
Figure 104. Insertion loss results for structure in Figure 103.

the gap as shown in Figure 103. The parasitic series resistance of the capacitor was 10 $m\Omega$, and its series inductance was around 0.8 nH. It can be seen from Figure 104 that after placement of the decaps, the insertion loss is significantly improved. The simulation time per frequency point using M-FDM was 100 ms, demonstrating how the method can be employed to efficiently co-simulate SI/PI problems.

5.6.3 Microprocessor Package

Another example is considered to demonstrate the importance of capturing the interaction between signal nets and the PDN. In this example, two uncoupled microstrip lines are routed over a patterned PDN layer. The central power island is assigned a DC voltage of Vdd, while the outer plane is connected to the lower Vss layer by means of 588 vias. The geometry and cross section of this example is shown in Figure 105. The 100 μm wide signal lines are designed to be close to 50 Ω. However, due to the transition over the slot separating the power islands, there is a return path discontinuity which causes the insertion loss of the the nets to deteriorate significantly, as shown in Figure 106.

Further, switching activity along the signal lines can cause SSN to couple to the PDN at several critical frequencies. In the following plots, a 1A A.C. noise source is

133
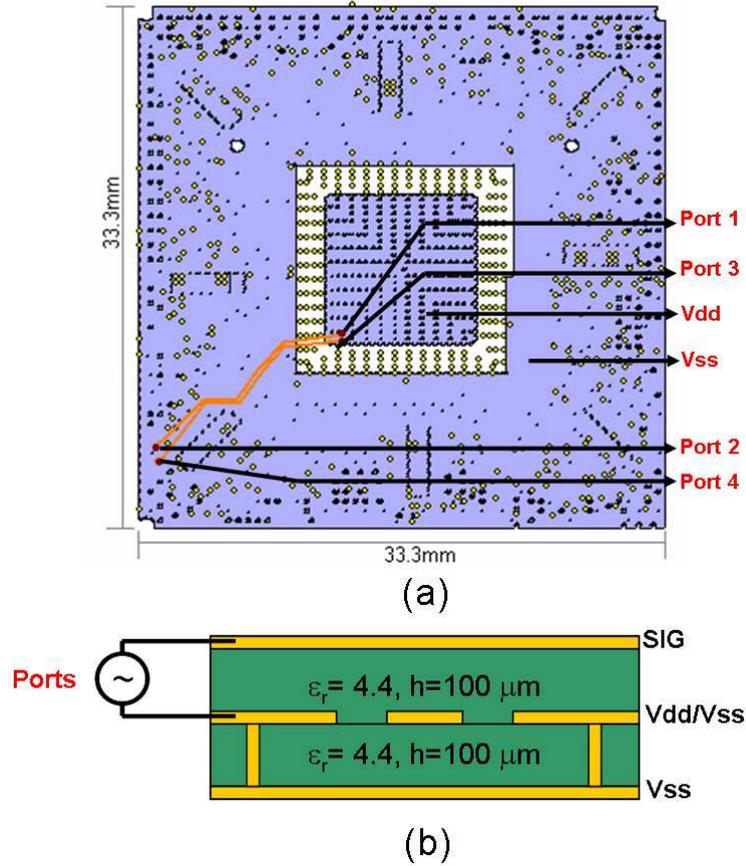
Figure 105. (a) Top view of example showing locations of ports (b) Cross section.

placed at the location of the ports in the example to determine a 2D voltage distribution. This provides a spatial distribution of noise "hot spots". Figure 107(a) and (b) show the voltage distribution at 2.4 GHz and 5.0 GHz respectively. These are the 802.11 a/b/g frequencies. Switching noise sources with harmonics containing energy at these frequencies could critically affect performance of a mixed-signal system. The locations of high noise voltage can be identified from the voltage distribution. Further, decoupling capacitors can be placed at these locations to reduce SSN.

5.6.4 Microstrip Via Transition

To verify the accuracy of the proposed SI/PI co-simulation technique, a structure containing a microstrip to microstrip via-transition was fabricated. The stack up of the structure and its layout are shown in Figures 108(a) and 108(b). The line is
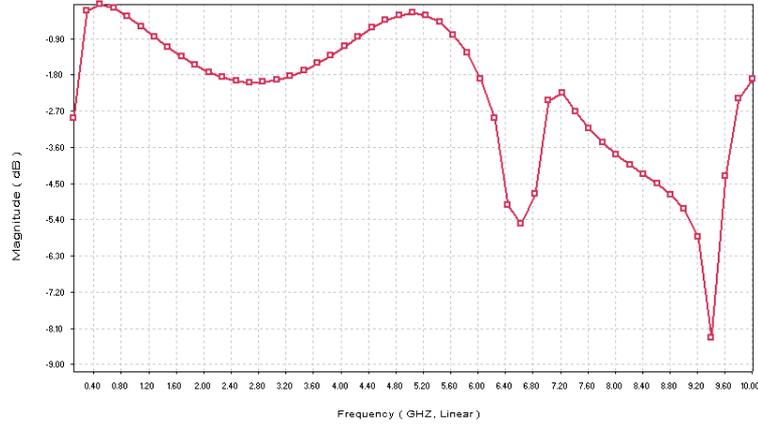
Figure 106. Insertion loss (dB).
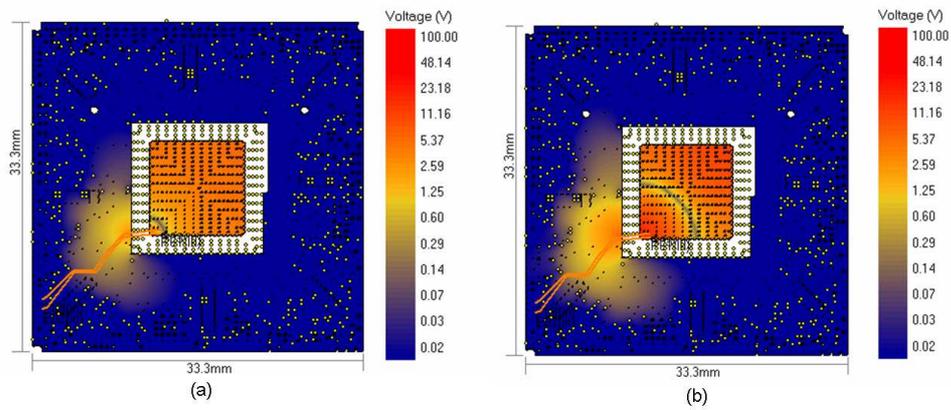
Figure 107. 2D voltage distribution plots. (a) 2.4 GHz (b) 5 GHz.

0.17mm wide and has a characteristic impedance of 50Ω, and has a total length of 30 mm. The two via transitions cause return path discontinuities (RPDs), the effects of which can be seen in the insertion loss and the return loss of the line, shown in Figures 109 and 110 respectively. The coupling between the line and the planes is shown in Figure 111. As can be seen from all three figures, there is good correlation between the simulated results and the measured data.

5.6.5   Stripline

The cross-section and layout of a test case containing a 0.2mm wide and 18mm long trace sandwiched between a power/ground pair is shown in Figure s112(a) and (b), respectively. This stripline in this case is symmetrically placed between the two
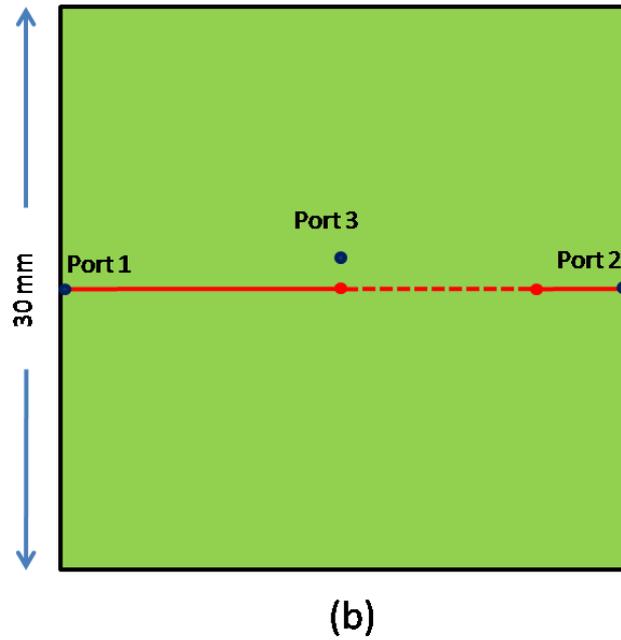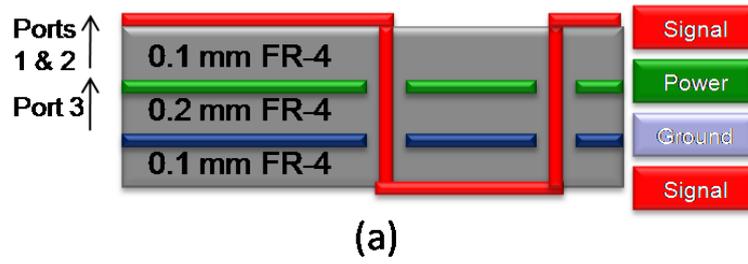
Figure 108. (a) Cross-section and (b) layout of microstrip transition.
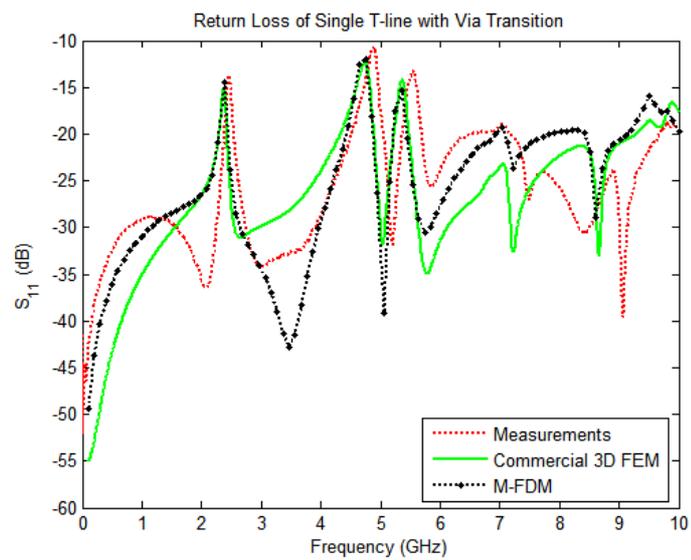
Figure 109. Return loss of microstrip transition shown in Figure 108.
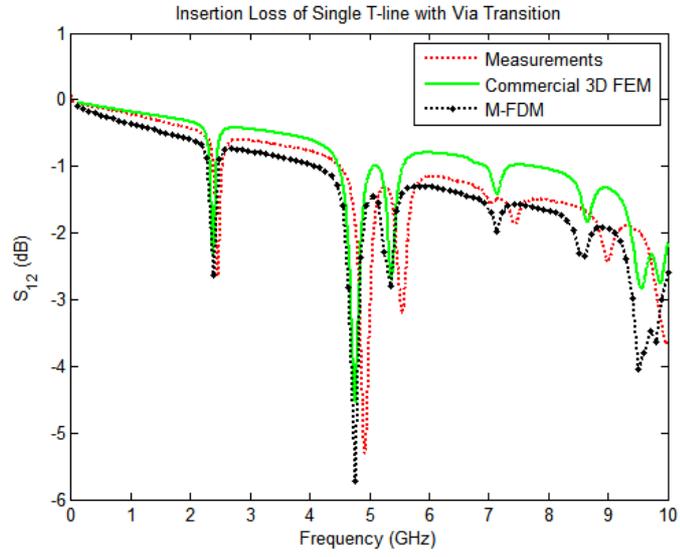
Figure 110. Insertion loss of microstrip transition shown in Figure 108.
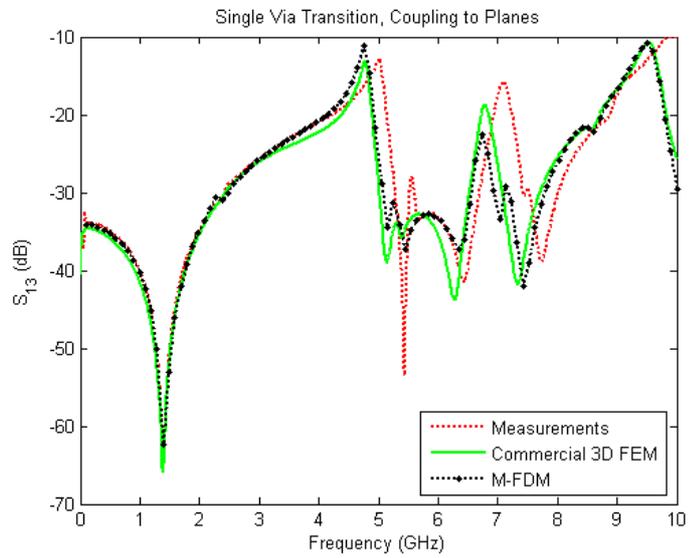
Figure 111. Coupling to PDN for microstrip transition shown in Figure 108.
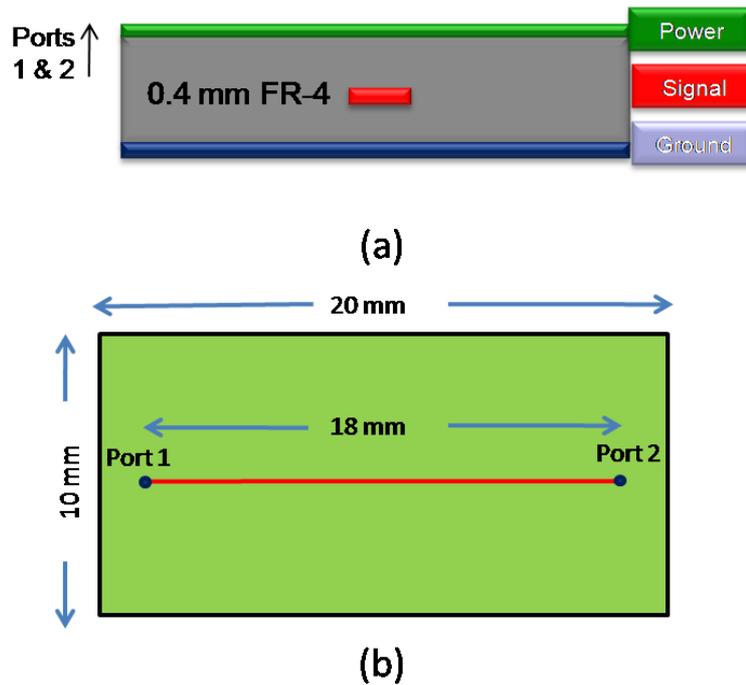
Figure 112. (a) Cross-section and (b) layout of stripline.

planes; however, the reference planes are not AC shorted with decoupling capacitors, which can cause parallel plate modes to be excited. This is clearly seen in Figure 113, in which the return loss of the stripline with an asymmetric excitation (with reference to power) are shown. The spikes at 3.6 GHz and 7.2 GHz clearly show the impact of the parallel plate modes. The benchmark simulation was performed on a commercial 3D finite integration technique (FIT) - based simulator, and shows good agreement with the M-FDM simulation.

5.6.6   CPW line

A 19 mm long, 0.36 mm wide conductor backed CPW line is shown in Figure 114. This line has two unconnected side grounds. The substrate used was FR-4 with a height of 0.4mm. Based on these dimensions, the line has a characteristic impedance of approximately 50 Ω. From 2D simulations, the calculated value of k was -0.72289. Simulations were performed in M-FDM using this value, and the return and insertion loss results as compared to a commercial power integrity tool are shown in Figures
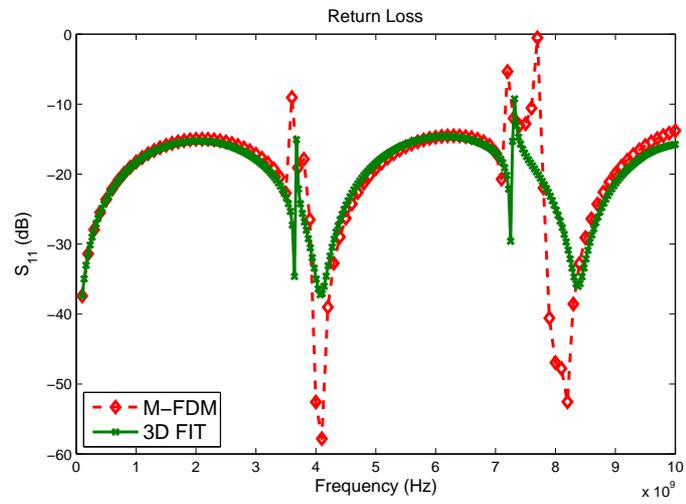
Figure 113. Return loss, S_{11}.
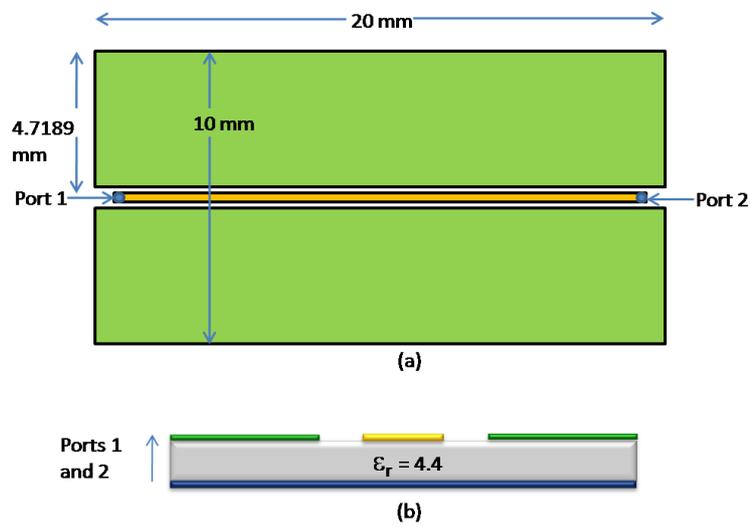
Figure 114. (a) Layout and (b)Cross-section of CPW line.
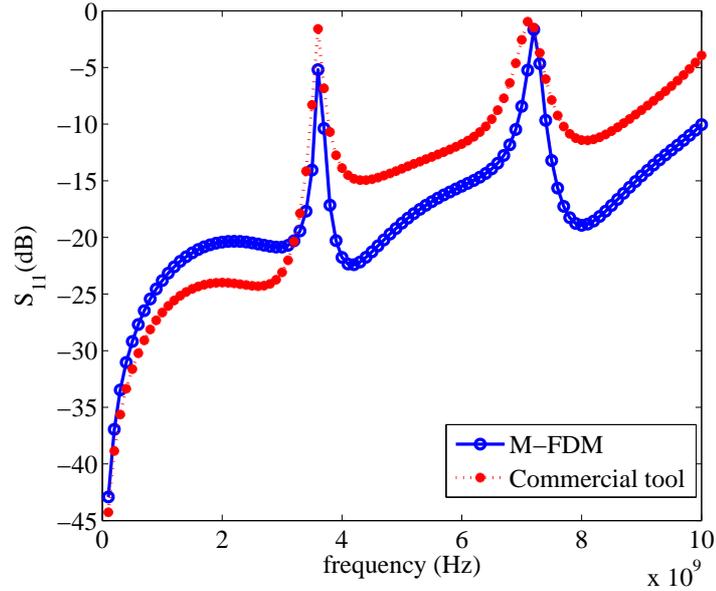
Figure 115. Return loss of structure in Figure 114.

115 and 116, showing good correlation.

5.7   Conclusion

The current in the signal lines return on the power and ground planes of the package. In configurations such as the stripline or CPW, this can lead to excitation of cavity modes in the power planes due to mode-conversion. These cavity modes appear as plane bounce in addition to SSN. Also, plane bounce caused by SSN can couple to the signal lines leading to signal integrity violations.

In this Chapter, modal decomposition based approaches have been used to integrate the response of signal lines in microstrip, stripline and CPW configurations with the admittance matrix obtained from M-FDM.

The approach has been validated by comparing the simulation results from M-FDM with commercial tools.
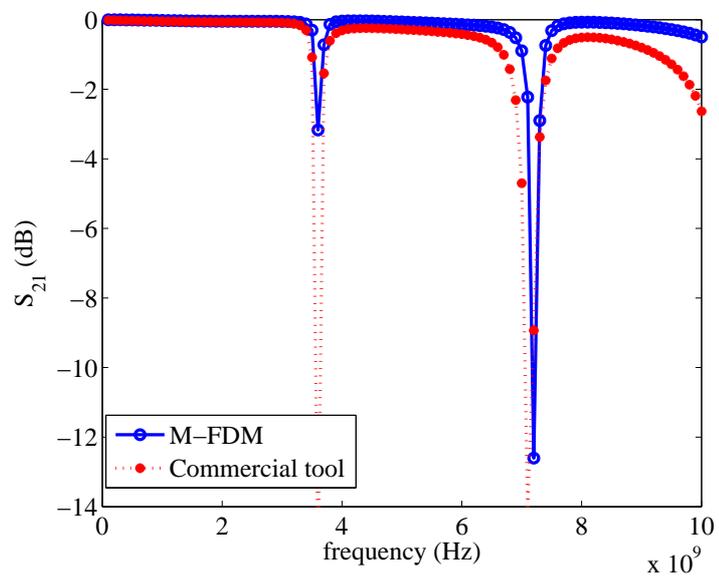
Figure 116. Return loss of structure in Figure 114.

CHAPTER 6

GENETIC ALGORITHM BASED OPTIMIZATION OF DECOUPLING CAPACITOR PLACEMENT

6.1 Introduction

In the design of complex power distribution networks (PDN) with multiple power islands, it is required that the PDN represents a low impedance as seen by the digital modules. This is to reduce the simultaneous switching noise (SSN), generated due to the switching activity of digital drivers. Typically this reduction in impedance is accomplished by placing decoupling capacitors between the power and ground planes of a package or board. However, achieving wide-band decoupling requires the placement of thousands of decoupling capacitors. This process requires a capacitor selection and placement methodology.

6.1.1 Role of Decoupling Capacitors

A typical decoupling capacitor or a *decap* can be represented in terms of its capacitance value in series with its parasitic inductance and capacitance. The frequency response of a capacitor resembles a V-shaped curve, which is a characteristic of a series resonant circuit. At the frequency where the capacitive impedance cancels out the inductive impedance, the resonant reaches its minimum impedance equal to its parasitic effective series resistance.

This frequency is called the self resonant frequency, f_{srf}, given by (143). For frequencies greater than the SRF, the decoupling capacitor behaves like an inductor.

$$f_{srf} = \frac{1}{2\pi\sqrt{LC}} \tag{143}$$

where, L is the inductance of ESL and C is the capacitance of the capacitor. The role of a decap is to provide a source of charge that can respond rapidly to the needs of switching circuits on the chip.

A switching system draws current from the power supply at multiple discrete frequencies which are harmonics of the clock frequency. If the impedance seen by the power supply terminals of drivers on chip is high at these frequencies, significant amount of SSN will be generated.

The role of decoupling capacitors is to reduce the power supply impedance to below a threshold, called the target impedance. Since decoupling capacitors are effective at performing this role around their SRF, multiple decoupling capacitors, with various SRFs may need to be placed.

6.1.2 Target Impedance

The number of capacitors required depends on the impedance level that must be reached, and this impedance level is called the target impedance.

The target impedance can be calculated as [3]:

$$Z_{tar} = \frac{Vdd \times \text{AllowedRipple}}{Current} \tag{144}$$

In practice, the maximum allowed ripple is assumed to 5% of the power supply voltage (Vdd). The current term in the denominator is $\frac{1}{2}$ the switching current in a clock cycle, which is assumed to be the current in each clock edge. Thus Equation 144 can be re-written as:

$$Z_{tar} = \frac{Vdd \times 5\%}{Id \times 50\%} \tag{145}$$

The target impedance trend as semiconductor manufacturing progresses from one technology node to the next has been shown in Table 3.

Table 3. Target impedance through technology nodes.

Year	Feature size(nm)	Power (W)	Vdd (V)	Current (A)	Target Impedance (mΩ)
2004	90	84	1.2	70	1.7
2007	65	103.6	0.9	115.11	0.7
2010	45	119	0.6	198.33	0.302

With reduction in rise time, the power supply impedance must be suppressed below the target impedance over an increased bandwidth. This implies that several different capacitors must be used to cover the frequency range. Bulk capacitors are used at low frequencies (1 kHz - 1 MHz), while ceramic surface mount and embedded capacitors are used upto 1 GHz. At frequencies higher than 1 GHz, the package power planes are used to provide decoupling. The frequency range over which a component can be employed for the suppression of power supply noise is shown in Figure 117.
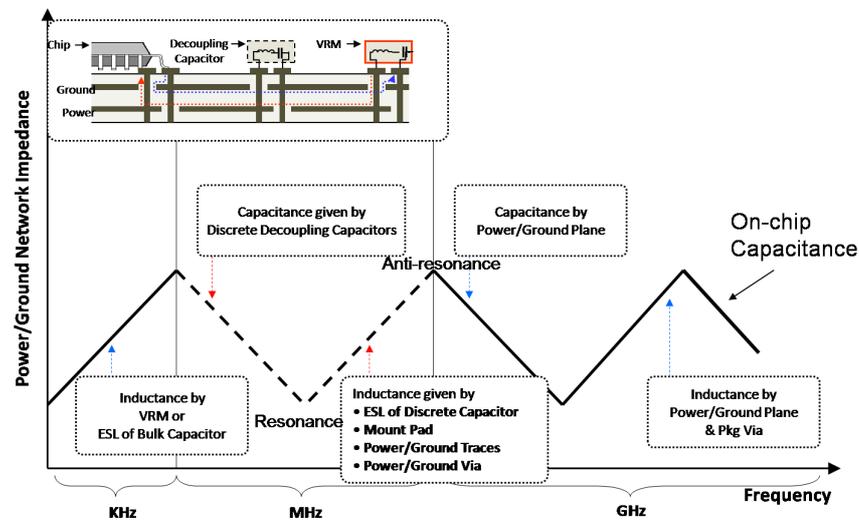
Figure 117. Typical PDN impedance profile due to interaction between various components of PDN (Courtesy [1])

6.1.3   Placement of Decoupling Capacitors

A PDN consisting of multiple decoupling capacitors and power/ground planes tailored to meet the target impedance requirements is challenging to design because of the following reasons:

1. **Parallel Resonances:**   The power/ground planes have multiple resonance and anti-resonance points as discussed earlier. To reduce the impedance at one of the anti-resonance points, a designer can place a decoupling capacitor with its SRF close to this anti-resonance point. This can create additional impedance maximums, however, due to parallel resonances created between the planes and

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the decap. Each decap can also interact with the others, leading to multiple impedance maximums due to parallel resonances between decaps.

2. **Proximity:** A decap creates an impedance null at its SRF as seen by the observation port only if it is placed close to the observation port. The radius of the circle within which the noise voltage is damped 50% or more is defined as R_{eff}. This R_{eff} is inversely proportional to frequency of operation [45].

3. **Signal Integrity:** Decaps may have to be placed to provide a path for the return current of a transmission line at a return path discontinuity (RPD). These include slots, via transitions, etc.

4. **Number:** A typical design may require thousands of decaps.

The solution space containing the values and locations of decoupling capacitors is extremely large, and manual placement based on an exhaustive search of this solution space is tedious. As a result, a stochastic search of design space is needed to determine optimal placement of decoupling capacitors in a power delivery network. This choice and placement of decoupling capacitors can be accomplished [18] using an optimization engine based on a genetic algorithm (GA)[46]. The GA is applied to search for the optimal locations of decoupling capacitors so as to minimize the input and transfer impedances over a desired range of frequencies.

However, the work in [18] relies on a cavity model for obtaining the PDN response. This is sufficient for simple rectangular two-layer geometries. However, for multilayer irregular geometries, the cavity model is inefficient. An in-depth discussion of the cavity method and its limitations can be found in Section 1.4.3.2.

6.2 Inclusion of Decoupling Capacitors in M-FDM

Decoupling capacitor are typically added to a system by populating the bare board or package with surface mount discrete components, as shown in Figure 118. These
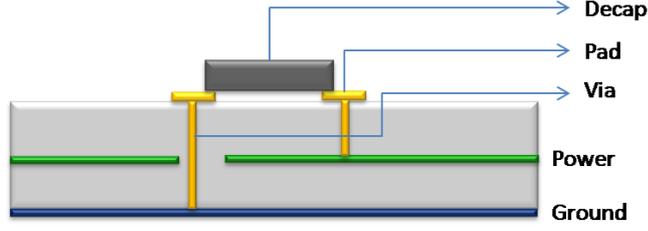
Figure 118. Surface mount decoupling capacitor mounted on power/ground pair.

components can be added to the M-FDM model for the PDN as follows:

The following quantities are assumed to be known:

$$Z_{cap} = ESR + j\omega L + \frac{1}{j\omega C} \tag{146}$$

$$Z_{via} = R_{via} + j\omega L_{via} \tag{147}$$

where, ESR is the effective series resistance of the capacitor, and L, C are defined in (143).

L_{via} and R_{via} are the self partial inductance of the via and its parasitic resistance, respectively.

If the decap is added between the unit-cell nodes n_1 and n_2 (corresponding to the pads) and the vias are connected between nodes n_1 and ground, and nodes n_2 and n_3 on the power plane, Z_{cap} and Z_{via} are added to the system matrix $\overline{\overline{\mathbf{Y}}}$ as follows:

$$\begin{pmatrix} \vdots \\ I_{n1} \\ \vdots \\ I_{n2} \\ \vdots \\ I_{n3} \\ \vdots \end{pmatrix} = \begin{pmatrix} y_{n1,n1} + Z_{via}^{-1} + Z_{cap}^{-1} & y_{n1,n2} - Z_{cap}^{-1} & \\ y_{n2,n1} - Z_{cap}^{-1} & y_{n2,n2} + Z_{via}^{-1} + Z_{cap}^{-1} & y_{n2,n3} - Z_{via}^{-1} \\ & y_{n3,n2} - Z_{via}^{-1} & y_{n3,n3} + Z_{via}^{-1} 1 \end{pmatrix} \begin{pmatrix} \vdots \\ V_{n1} \\ \vdots \\ V_{n2} \\ \vdots \\ V_{n3} \\ \vdots \end{pmatrix} \tag{148}$$

6.3 Optimization using the Genetic Algorithm

6.3.1 Formulation

The first step in the GA-based engine is the representation of the data as a set of *'genes'* that make up a *'chromosome'*. In this case, it is sufficient if the chromosome represents a particular choice of decaps and its placement (x- and y-locations, as well

as layer connectivity), with cost being an optional parameter. Hence, all the available decaps can be arranged and indexed in order of their resonance frequency. It is critical that the capacitors be arranged in order of their self resonance frequencies, as will be explained later in this chapter. Hence, a chromosome representing a particular decoupling solution is only dependant on the number of capacitors being placed.

The general flowchart of the optimization process is shown in Figure 119. The inputs to the algorithm are 1. The package or board layout, 2. The target impedance and the bandwidth, 3. The number of decaps to place, and 4. A library of SMD- and embedded-decaps. Other algorithm specific inputs include the size of the population (N), the probability that crossover (p_c) and mutations (p_m) occur and the maximum number of optimization iterations. Given these inputs, the engine generates a random initial population, with decoupling capacitors chosen from the library, and with random locations on the board or package.

Each of the potential solutions are evaluated using the M-FDM engine for their Z-parameters at multiple noise source locations. The *fitness* of the ith solution has been defined as

$$f_i = \sum_{j=1}^{N_{port}} \sum_{k=1}^{N_{freq}} (w_1[Z_{tar,j} - Z_{j,j}(k)] + w_2[Z_{tar,j} > Z_{j,j}(k)]) \qquad (149)$$

where w_1 and w_2 are weights chosen based on application, N_{port} is the total number of noise sources at which the target impedance criterion must be met and N_{freq} is the total number of frequency points in the simulation. Typically N_{freq} is chosen to adequately cover the frequency range. $Z_{tar,j}$ is the target impedance spec at the jth port, and $Z_{m,n}(k)$ is the (m,n) entry of the Z-matrix at the kth frequency point. Also, the logical operation in Equation 149 returns 1 if the condition is met, and 0 otherwise. An additional input to the fitness function may be cost of the capacitors used.

At this stage, the population is sorted in order of their fitness, and the best solution

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is checked to see if it satisfies the target impedance at all ports and at all frequencies, in which case the algorithm terminates successfully. Otherwise, the crossover and mutation steps are carried out.

A pair of individuals, *parents*, in the population are chosen. The key idea here is that the fitness of a solution is directly related to the probability that it will be selected as a parent. This selection pressure leads to cumulative improvement in the fitness of solutions over generations.

In the crossover phase, the chromosomes of the parent solutions are mixed together at a rate determined by the crossover rate, p_c. Essentially, a new solution is created by copying a portion of the solution from each parent, as shown in Figure 120. This is performed iteratively until a new population is generated.

This new population is now subjected to mutation. By mutation, small random changes are made to each solution at the mutation rate, p_m. It is critical that these changes be small, as the probability of the solution improving reduces with the magnitude of the mutation. Hence, a mutation to a particular decap will result in choosing a new decap which resonates at a slightly higher or lower frequency. Hence, the library of decaps is indexed according to its SRF. At this step, a new generation has been created and the algorithm goes back to the selection phase.

A few of the best solutions are preserved intact (*elitism*,[46]) over all iterations to prevent the solutions from becoming worse over generations.

Termination occurs when the GA converges to a solution that satisfies the target impedance requirements. However, in some cases, there may be no improvement in fitness, whereupon the algorithm is terminated, and may have to be run again with different input parameters.

6.3.2 Convergence

The GA is not guaranteed to converge to the best or most optimal solution. However, it is guaranteed to find solutions which are atleast as good (in terms of fitness) as the
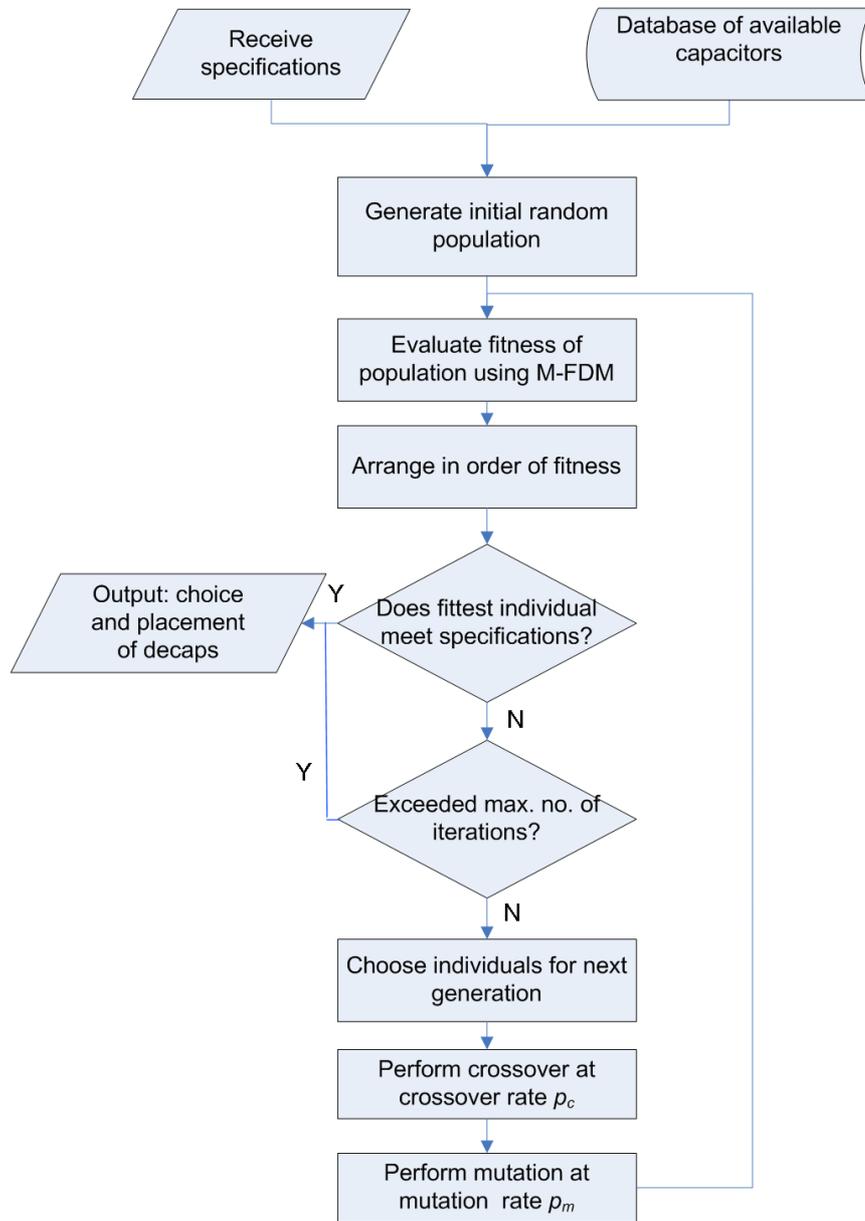
Figure 119. The flow of the GA based optimizer.
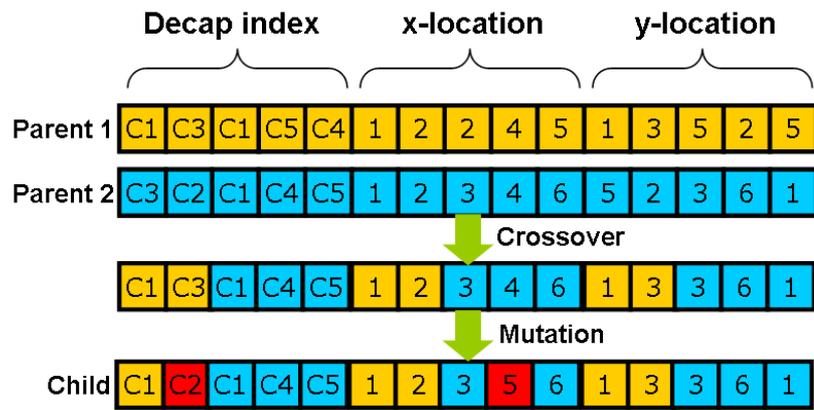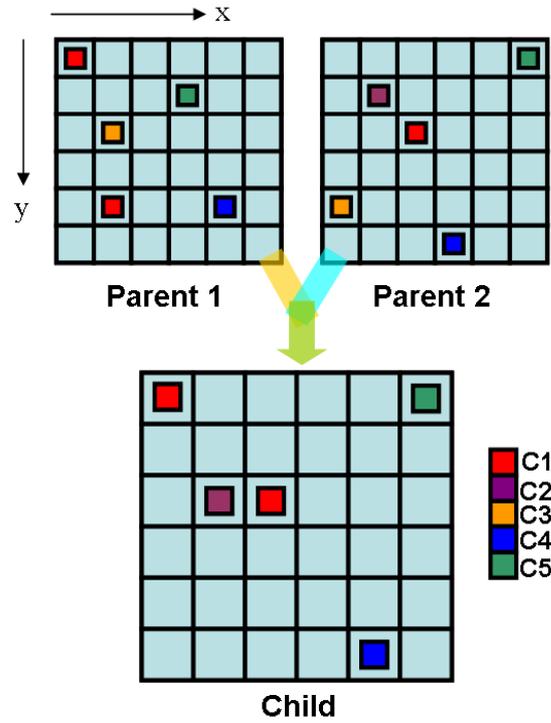
Figure 120. Schematic Illustration of Crossover and Mutation.

best solution in the current population.

The rapid convergence of the optimizer is strongly dependant on the choice of parameters such as the crossover and mutation rates, the population size, and the fitness function.

In this thesis, these parameters have been fixed to empirically determined values. However, the work in [47] has improved on the methods here by analyzing the impact of different fitness functions and initial non-random design driven capacitor placements.

6.3.3   Decoupling Capacitor Library

The decoupling capacitors used by the GA are listed in Table 4.

6.4   Test Cases and Results

All simulations were performed on a Intel dual-processor, 3GHz Xeon Workstation with 3 GB of RAM. The crossover rate was chosen to be 0.5 (i.e., 50% of the solutions that form the next generation will be created by crossover). The mutation rate was 0.1. This implies that each character in the chromosome has a 10% chance of undergoing a mutation. The maximum number of iterations was 100.

6.4.1   Test Case 1

The first example is a simple three layer package showing a transmission line traversing a slot in the power plane. The slot introduces a return path discontinuity as well as an impedance discontinuity. The stack up and the geometry are shown in Figure 103. The insertion loss of the transmission line is shown in Figure 121(a). Also, assuming that transmission line is terminated in digital modules, there will be a need to reduce the impedance looking into the PDN. The impedance profile at the two ports between the power and ground plane (identical, due to symmetry) is shown in Figure 121(b). The optimizer was required to meet a target impedance of 500 mΩ, using fewer than

Table 4. Library of decoupling capacitors (Courtesy [1]).

Cap	ESR mΩ	ESL nH	SRF (GHz)
27 pF	850	0.4	1.5315
33	700	0.4	1.3853
130	373.4	0.458	0.6523
174.4	313.1	0.509	0.5342
207.1	243.1	0.468	0.5112
304.7	148.6	0.413	0.4487
511.4	139.8	0.4	0.3519
598.5	120.0	0.432	0.3137
1.0 nF	75.0	0.370	0.2616
2.2	62.1	0.426	0.1644
2.9	203.8	0.533	0.1280
4.2	141.1	0.523	0.1074
8.2	88.9	0.519	0.0771
19.8	44.3	0.572	0.0473
41.1	25.7	0.435	0.0376
83	19.9	0.416	0.0271
179	15.9	0.548	0.0161
379	14.1	0.543	0.0111
0.81 uF	9.8	0.485	0.0080
1.93	6.7	0.686	0.0044
3.86	4.8	0.704	0.0031
7.87	5.5	0.876	0.0019
21.2	2.7	1.628	0.0009
81.2	2.5	2.834	0.0003

10 SMD capacitors, chosen from a library of 40 capacitors with an SRF ranging from 50 MHz upto 1 GHz. The parasitics of the SMD capacitors were included in the library. The optimizer converged in 16 iterations and with 9 decaps. The simulation required 8000 nodes, and the simulation time per frequency point in M-FDM was 140 ms (total time was 18 minutes). The top view of the placement is shown in Figure 122.

The optimized impedance profile is shown in Figure 123(b). The capacitor placement is asymmetric as seen by the ports, leading to differing impedance responses at
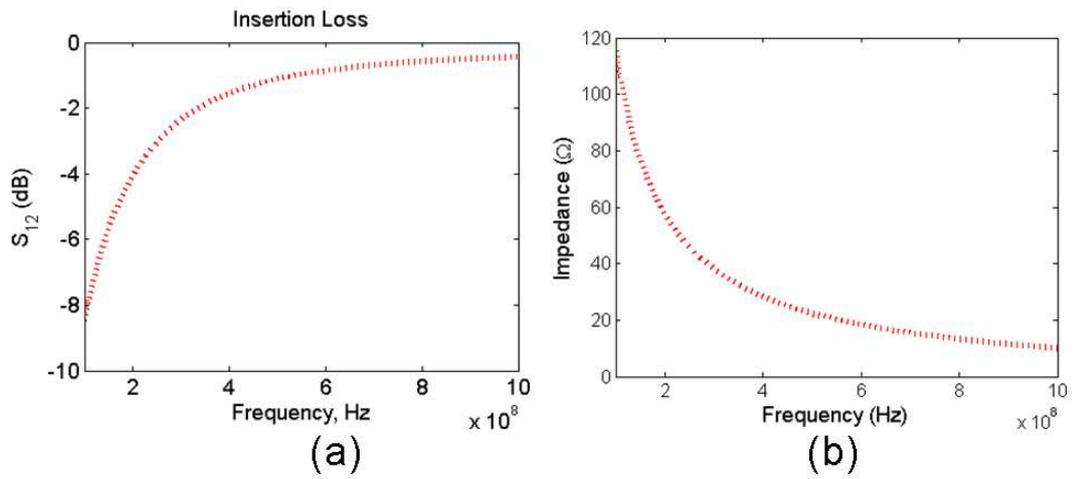
Figure 121. (a) Insertion loss of transmission line, and (b) Impedance looking into PDN at port locations in Figure 103.
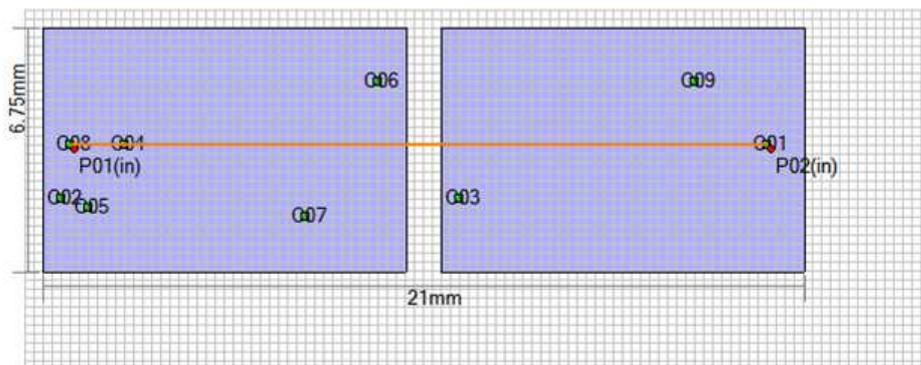
Figure 122. Top View of Optimized Capacitor Placement.
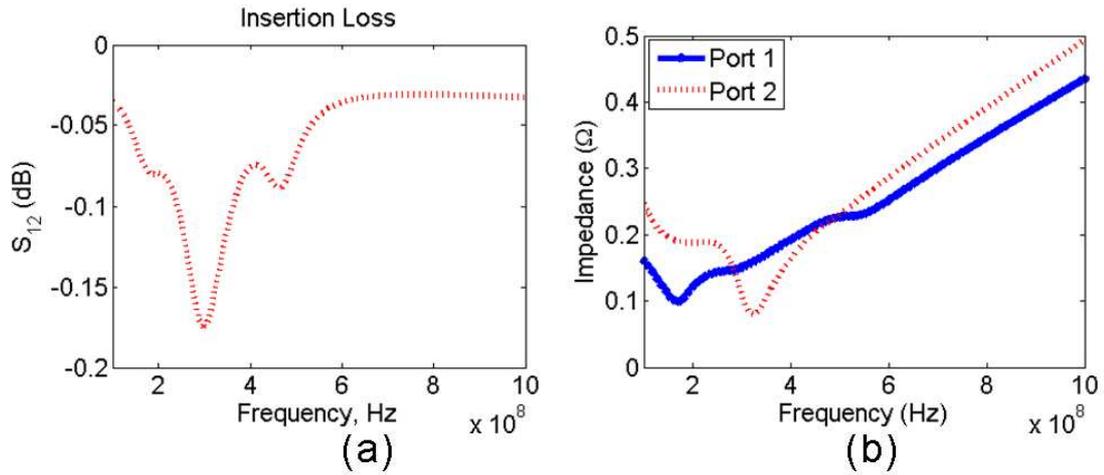
Figure 123. (a) Insertion loss of transmission line, and (b) Impedance looking into PDN at port locations in Figure 122.

the two ports. The impedance has been reduced from a maximum of 120 Ω to under 500 mΩ. The optimized design, while meeting the target impedance requirement, may also improve the effect of the return path discontinuity. This can indeed be observed in the optimized insertion loss of the transmission line, as shown in Figure 123(a).

6.4.2 Test Case 2

The second test case is a realistic three layer server backplane. While the top and the bottom layers are continuous, the middle layer is not. The geometry of the middle layer and the cross section of the structure is shown in Figure 124. The location of the ports has also been shown. The board dimensions are 112 mm $\times$ 97 mm. The impedance of the PDN looking into the planes is shown in Figure 125(a). Due to the discontinuous middle layer, although ports 1 and 2 are separated, they will still be coupled [48], as can be seen from the insertion loss, shown in Figure 125(b). The optimizer was required to place 200 decaps to achieve a target impedance of 200 mΩ, over a frequency range of 100 MHz - 1 GHz. The optimizer converged in 90 iterations, and the optimized impedance profile is shown in Figure 126(a). Also, by providing the decoupling, the vertical coupling between ports has also been reduced,

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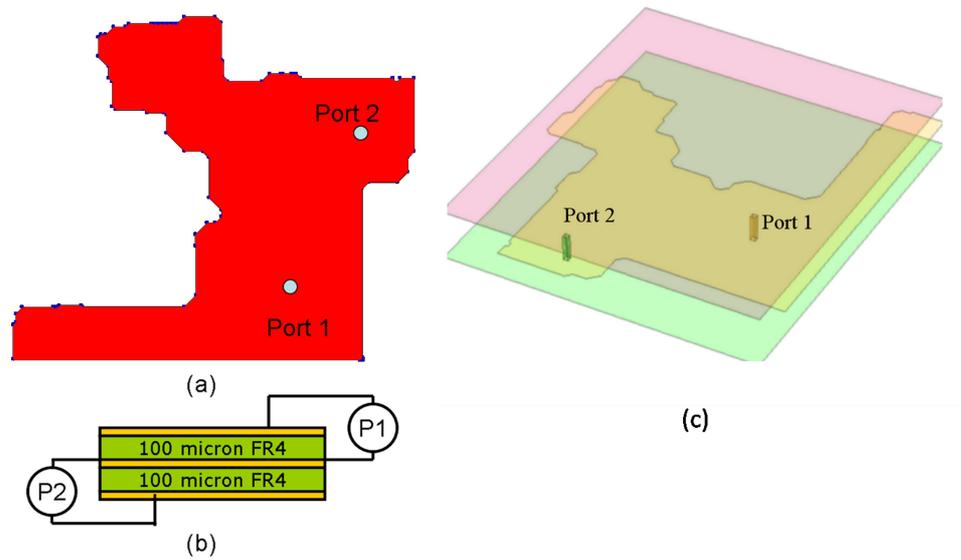
Figure 124. (a) Geometry of middle layer (b) Cross section (c) 3D view.
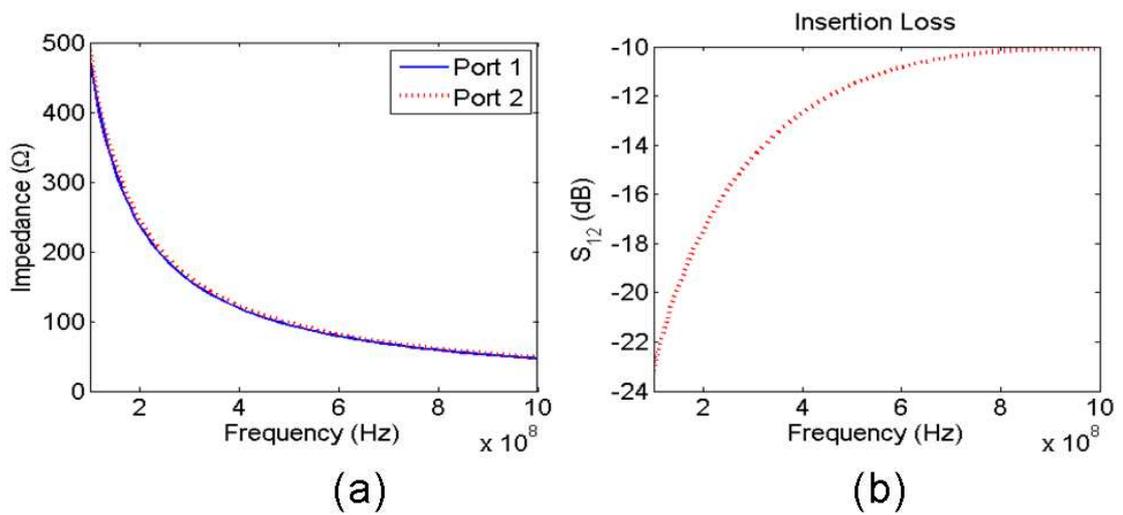
Figure 125. (a) Impedance looking into PDN at port locations and, (b) Insertion loss between ports (S_{12}) of structure in Figure 124.

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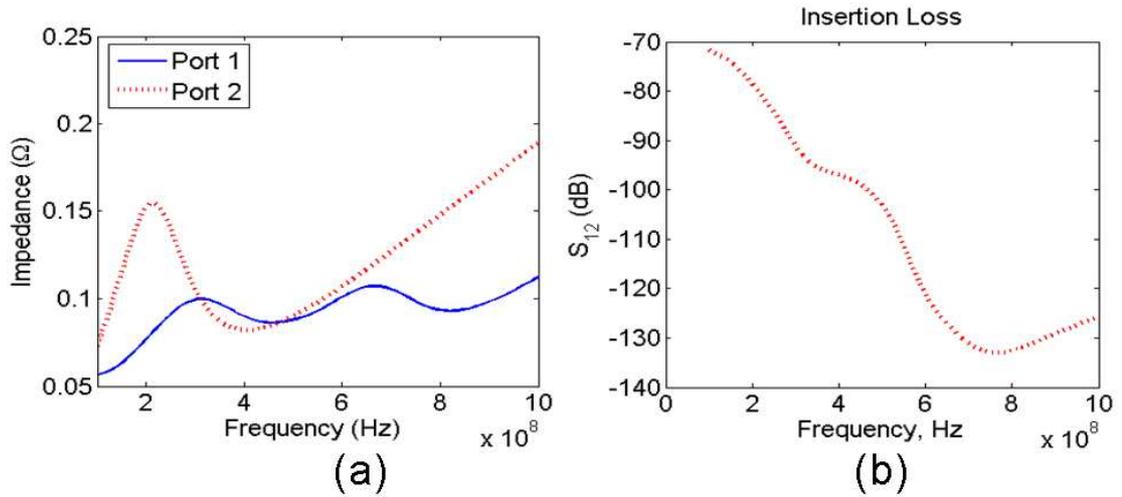
Figure 126. (a) Optimized impedance looking into PDN at port locations and, (b) Optimized insertion loss between ports (S_{12}).

as shown in Figure 126(b). The M-FDM model consisted of 89,000 nodes and required a simulation time of 2.5 sec/frequency point. The total time for convergence was 26 hours. This can be accelerated by seeding the initial population with reasonably good solutions rather than those generated at random.

6.4.3 Test Case 3

The final test case is an example to illustrate various trade-offs that can be made at an early stage in design, such as the impact of the choice of a substrate on the number of decoupling capacitors. Figure 127 shows a simple two-layer power/ground geometry of size 19.2 cm × 19.2 cm. The substrate used is an advanced thin-film planar capacitor laminate called Interra^{TM} HK-04 from Dupont [49]. This material is offered in three different substrate thicknesses - 50, 25 and 18 μm. The GA-optimizer was used to place decaps and optimize the impedance at Port 1 for a target impedance of 250 mΩ over the frequency range 500 MHz - 1GHz. The optimized self-impedance is shown in Figure 128. The benefit of using a thinner substrate is that it is now possible to reduce the number of decoupling capacitors required, as much of the decoupling comes from the capacitance between the parallel plates. This is shown in Figure

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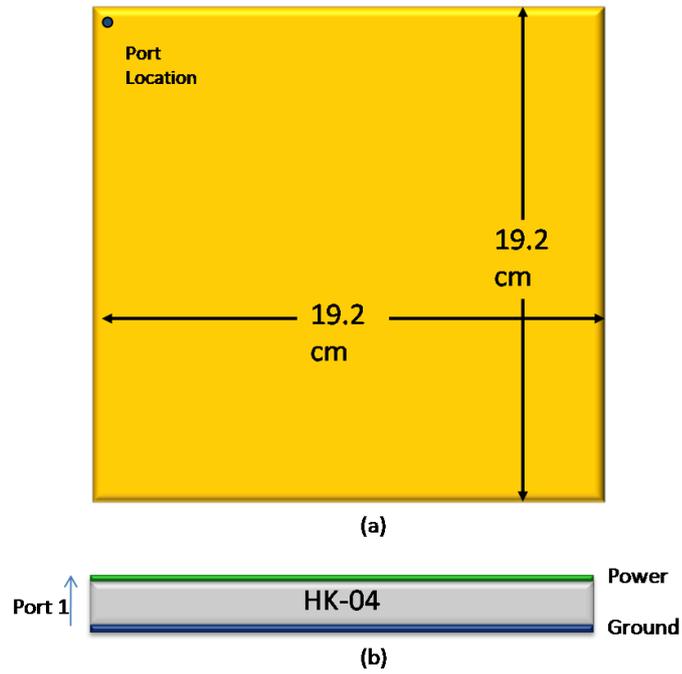
Figure 127. Structure of test case 3 (a) Top-view (b) Cross-section.
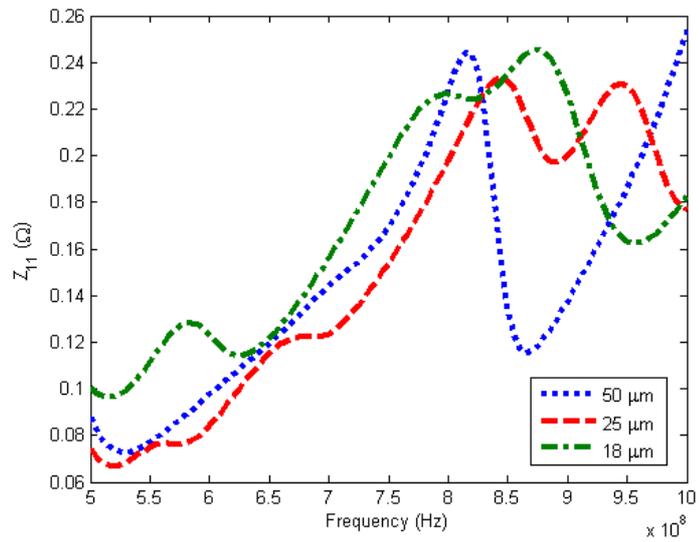
Figure 128. Self impedance at Port 1 after optimization.
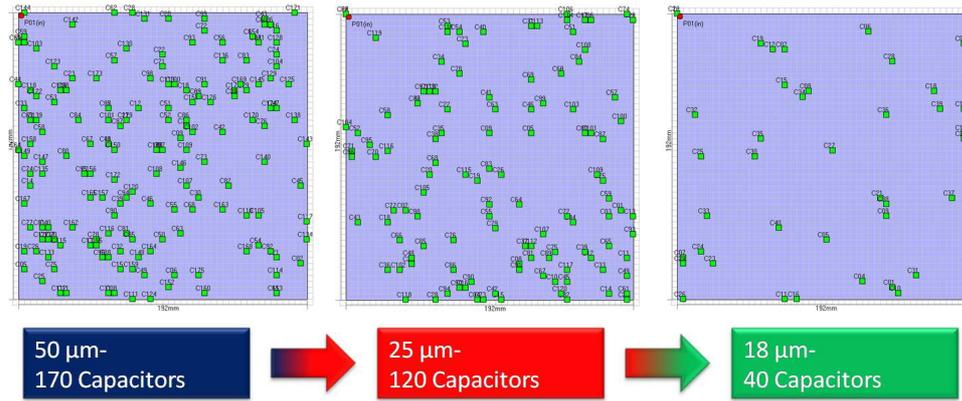
Figure 129. Locations of Decoupling Capacitors.

129, where the locations of the placed decaps are shown. The number of capacitors required for the 50, 25 and 18 μm substrates was 170, 120 and 40, respectively. Thus, it may be more cost effective to use a more expensive, but thinner, substrate as this results in the reduction of about 130 decaps.

6.4.4 Summary of Results for Test Cases 1 and 2

The simulation setup, runtime and convergence data are summarized in Table 6.4.4.

Table 5. Summary of results for automatic decap placement using GA.

Structure	No. of Decaps	Z_{tar} mΩ	CPU Time	Iterations
Test case 1	9	500	18 mins	16
Test case 2	200	200	26 hours	90

6.5 Conclusions

The signal and power integrity of high speed digital systems relies on the ability of PDN to provide charge instantaneously to switching circuits on chip. This is typically accomplished by placing decoupling capacitors on the package. This problem is hard to solve because thousands of capacitors may have to be placed to decouple a PDN from low frequencies (MHz) to high frequencies (GHz). These capacitors interact with each other and with the system, and the response of these capacitors is a function of

its placement. This problem cannot be solved deterministically. Thus, in this chapter a GA based approach was suggested to perform a stochastic search of the design space. The approach has been tested on two test cases.

CHAPTER 7

FUTURE WORK: INITIAL STUDY USING THE
MULTI-LAYER FINITE ELEMENT METHOD (M-FEM)

7.1   Introduction

As explained earlier, this method creates a sparse and banded admittance matrix and provides an efficient computational complexity of $O(N^{1.5})$.

7.1.1   Limitations of M-FDM

The methodology developed in this thesis, M-FDM, is a finite difference-based technique that can solve power plane problems using square-meshes. The limitation of the method is that it uses a rigid, square, grid. Typically, package PDNs are electrically large. Thus, for a large solid plane, like the one shown in Figure 130(a), the square mesh used by MFEM can use a cell size that is dependant on the maximum frequency of simulation. A good rule of thumb is to use a discretization width of $\lambda/20$. However, these PDNs also contain geometrically small features such as split planes and apertures. To capture very fine structures, the regular mesh becomes dense locally and globally, resulting in a large number of unknowns. This is demonstrated in Figure 130(b).

(a)   (b)
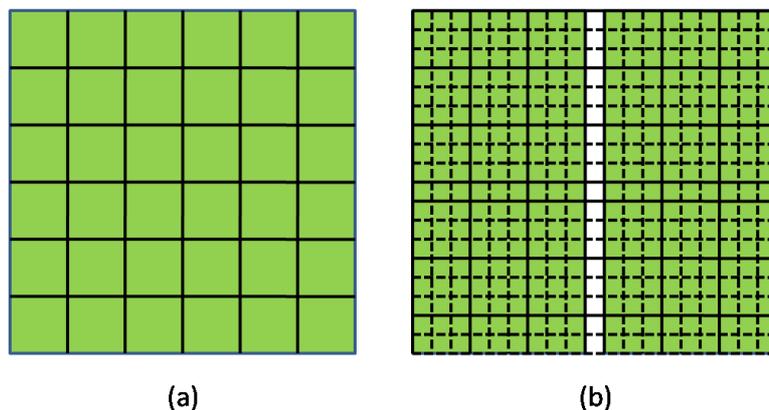
Figure 130. (a) Mesh generated based on maximum frequency (b) Mesh generated due to geometry.

In typical package geometries, the minimum feature size can easily be less that $100\mu m$ or 4 mils. Thus for a 50 mm $\times$ 50 mm package, the total number of cells required to model one solid plane-pair using a $100\mu m$ cell size is 250,000. Although M-FDM has been demonstrated in its current implementation for a maximum of 1 million unknowns, this only allows for the modeling of four plane-pairs. Given that the feature size on package and board are shrinking to allow for greater wiring density, the mesh is a serious limitation of M-FDM.

This problem can be solved by using a non-uniform rectangular mesh, which is also not optimal in the modeling of arbitrary geometries, such as circular voids and via-holes. Hence, techniques using non-uniform triangular meshes have been proposed in literature for two layer geometries with circuit extraction for SPICE compatibility [50]. However, FEM applied to multilayer geometries has typically used hexahedral or tetrahedral meshes [51].

Despite the limitations of M-FDM, there are some significant advantages as well. These advantages include the ease of implementation of a method that is capable of modeling a multi-layer power/ground network using a mesh that is applied only to the conductors. The formulation for M-FDM results in an admittance matrix that can be easily represented by an equivalent circuit.

The goal of this chapter is to obtain a formulation that can retain the advantages of M-FDM while overcoming its limitations. The proposed method is called the multilayer finite element method (MFEM), and initial results are promising.

In the method proposed, the multilayer finite element method (MFEM)[52], a Delaunay triangular mesh is applied to each metal layer. The potential distribution on each plane-pair is expanded in terms of pyramid basis functions. On simplification, the obtained matrix equation can be shown to represent an electrical network. This development of a triangular mesh based finite element technique can be applied to multi-layer geometries. As only a surface mesh is required, this approach requires far

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fewer unknowns than a general 3D FEM-based solution.

The rest of this chapter is organized as follows. The formulation for MFEM has been developed in detail in Section 7.2. A four-layer test case has been simulated and compared with existing techniques and these results have been discussed in Section III, with conclusions in Section IV.

7.2 Formulation for Single Plane-Pair Geometries

An efficient approximation that can be employed for package power planes is that of a planar circuit [11]. A planar circuit is a microwave structure in which one of the three dimensions, say z, is much smaller than the wavelength. Under this condition, it can be assumed that the field is invariant along the z-direction. Hence, $\frac{\delta}{\delta z} = 0$ and the governing equation reduces to the scalar 2D-Helmholtz wave equation:

$$\left(\nabla^2 + k^2\right)\mathrm{u} = j\omega\mu dJ_z, \; \nabla^2 = \left(\frac{\delta^2}{\delta x^2} + \frac{\delta^2}{\delta y^2}\right) \tag{150}$$

where ∇^2 is the transverse Laplace operator parallel to the planar structures, u is the voltage, d is the distance between the planes, k is the wave number, and J_z is the current density injected normally to the planes [22]. The open circuit at the boundary can be represented by a magnetic wall or Neumann boundary condition, which completes the problem formulation.

7.2.1 Basis Function

Using a standard finite-element approximation with a triangular mesh elements and linear pyramid or "hat"-basis functions [53], the weak form of the PDE in Equation (150) is:

$$\sum_{j=1}^{N} \int\int_{\Omega} \left[\nabla\phi_j \cdot \nabla\phi_i + \omega^2\mu\varepsilon\phi_j\phi_i + j\omega\mu dJ_z\phi_i\right] dxdy = 0 \tag{151}$$

where Ω is the problem domain. The triangular mesh and the hat function, ϕ are shown in Figure 131(a). The formulation of the matrix equation for 2D geometries is

well known, and is reproduced here from [54]. For convenience, simplex coordinates $\{L_1, L_2, L_3\}$ have been used, which can be related to the Cartesian coordinates:

$$x = L_1 x_1 + L_2 x_2 + L_3 x_3 \tag{152}$$

$$y = L_1 y_1 + L_2 y_2 + L_3 y_3 \tag{153}$$

$$L_1 + L_2 + L_3 = 1 \tag{154}$$

The equations above can be solved to obtain:

$$L_i = \frac{1}{2\triangle} (a_i + b_i x + c_i y) \tag{155}$$

$$a_i = x_{i+1} y_{i+2} - x_{i+2} y_{i+1}$$

$$b_i = y_{i+1} - y_{i-1}$$

$$c_i = x_{i-1} - y_{i+1}$$

and the subscripts are evaluated (modulo 3) $+ 1$. $\triangle$ is the area of the triangle with vertices at points $(P1, P2, P3)$. Within the cell, the pyramid basis functions are identical to the simplex coordinates themselves.

Hence, Equation (151) can be rewritten in matrix form as follows:

$$\left(\overline{\overline{\mathbf{K}}} + \overline{\overline{\mathbf{M}}} \right) \overline{\mathbf{U}} = \overline{\mathbf{F}} \tag{156}$$

where, $\overline{\overline{\mathbf{K}}}$ and $\overline{\overline{\mathbf{M}}}$ represent the stiffness and mass matrices, respectively, $\overline{\mathbf{U}}$ is the unknown potential, and $\overline{\mathbf{F}}$ contains the contributions from the current source excitation. The entries of $\overline{\overline{\mathbf{K}}}$, $\overline{\overline{\mathbf{M}}}$ and $\overline{\mathbf{F}}$ are:

$$k_{i,j} = \int\int_{\Omega} \frac{j}{\omega\mu d} \nabla\phi_i \cdot \nabla\phi_j \, dx dy \tag{157}$$

$$m_{i,j} = \int\int_{\Omega} \frac{-j\omega\varepsilon}{d} \phi_i \phi_j \, dx dy \tag{158}$$

$$f_i = \int\int_{\Omega} J_z \phi_i \, dx dy \tag{159}$$

The linear pyramid basis functions are equal to the simplex coordinates within the cell, i.e.

$$\phi_i(L_1, L_2, L_3) = L_i \tag{160}$$
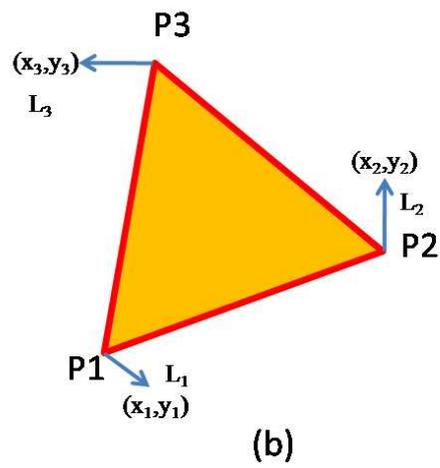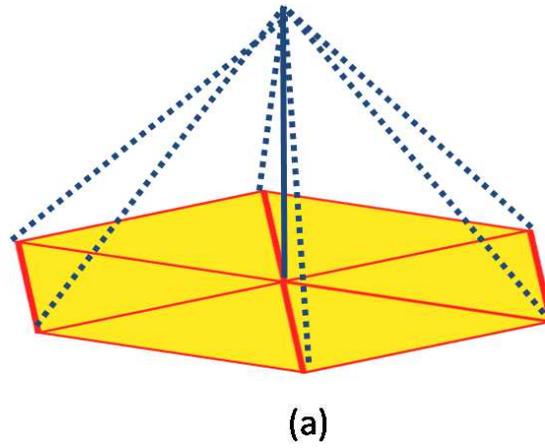
Figure 131. (a) Triangular mesh and pyramid basis function (b) Cartesian and Simplex coordinates.

Therefore,

$$\nabla\phi_i = \nabla L_i = \frac{1}{2\triangle}\left(\hat{x}b_i + \hat{y}c_i\right) \tag{161}$$

Substituting Equation 161 in Equation 157,

$$k_{i,j} = \frac{b_i b_j + c_i c_j}{4\triangle}\frac{j}{\omega\mu d} \tag{162}$$

The evaluation of the integral to obtain $m_{i,j}$ (Equation 158) and f_i (Equation 159) can be performed by transforming the coordinates from Cartesian to simplex using the Jacobian,

$$dxdy = dL_1 dL_2 \frac{\delta(x,y)}{\delta(L_1, L_2)} = 2\triangle dL_1 dL_2 \tag{163}$$

The integrals in Equations 158 - 159 are a special case of the general formula

$$I = \int\int_{\Omega} L_1^a L_2^b L_3^c dL_1 dL_2 = \frac{a!b!c!}{(a+b+c+2)!} \tag{164}$$

where a, b and c are integer powers. Therefore, substituting $a = 2, b = 0, c = 0$ when $i = j$ and $a = 1, b = 1, c = 0$ when $i \neq j$,

$$m_{i,j} = \frac{-j\omega\varepsilon}{d}\frac{\triangle}{12}\left(1 + \delta_{i,j}\right), \text{ where } \delta_{i,j} \text{ is the Kronecker delta function.} \tag{165}$$

Using $a = 1, b = 0, c = 0$,

$$f_i = J_z\frac{\triangle}{3} \tag{166}$$

7.2.2 Equivalent Circuit

$\overline{\overline{\mathbf{K}}}$ and $\overline{\overline{\mathbf{M}}}$ represent the admittance matrices of frequency-independant inductive and capacitive components, respectively. Specifically, $\overline{\overline{\mathbf{K}}}$ represents inductors connected between triangle vertices (i.e., along the triangle edges), and $\overline{\overline{\mathbf{M}}}$ represents capacitors connected between triangle vertices and to ground, as shown in Figure 132.

This can be shown by evaluating one row of the 3×3 local matrix corresponding to one triangle For example, the sum of the first row of this matrix is:

$$S = \sum_{j=1}^{3} \frac{b_1 b_j + c_1 c_j}{4\triangle}\frac{j}{\omega\mu d}$$
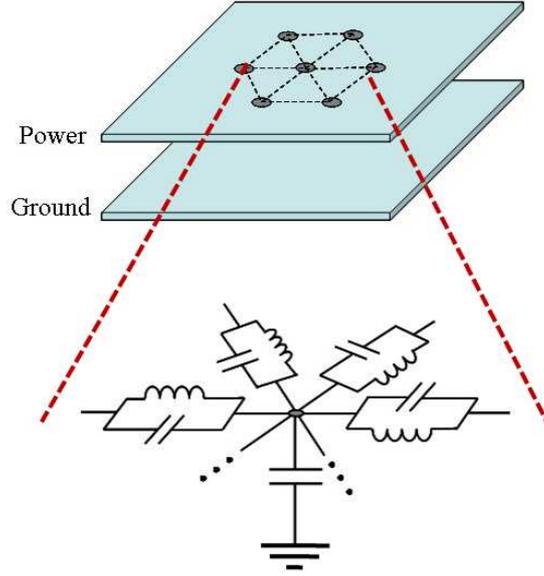
Figure 132. Topology of equivalent circuit for single plane-pair structures.

Consider the $b_1 b_j$ term for $j = 1, 2, 3$.

$$b_1^2 = (y_2 - y_3)^2 \text{ for } i = j = 1$$

$$b_1 b_2 = (y_2 - y_3)(y_3 - y_1) \text{ for } i = 1, j = 2$$

$$b_1 b_3 = (y_2 - y_3)(y_1 - y_2) \text{ for } i = 1, j = 3$$

$$\therefore b_1^2 + b_1 b_2 + b_1 b_3 = 0 \tag{167}$$

$$\text{Similarly, } c_1^2 + c_1 c_2 + c_1 c_3 = 0 \tag{168}$$

It can be shown that the other rows of the 3×3 local matrix also sum to zero. This implies that the rows (and by symmetry, the columns) of $\overline{\overline{\mathbf{K}}}$ sum to zero. This corresponds to circuit elements (in this case, inductances) connected between the triangle vertices, with no element to system ground. On the contrary, the row and column sums of $\overline{\overline{\mathbf{M}}}$ do not vanish, indicating capacitances to ground in addition to capacitive elements along edges.

Hence, the equivalent circuit for the single plane-pair case can be represented by the admittance matrix $\overline{\overline{\mathbf{Y}}}$, where $\overline{\overline{\mathbf{Y}}} = \overline{\overline{\mathbf{K}}} + \overline{\overline{\mathbf{M}}}$. This matrix is sparse and the solution to Equation (156) can be obtained using standard linear equation solvers. The ability

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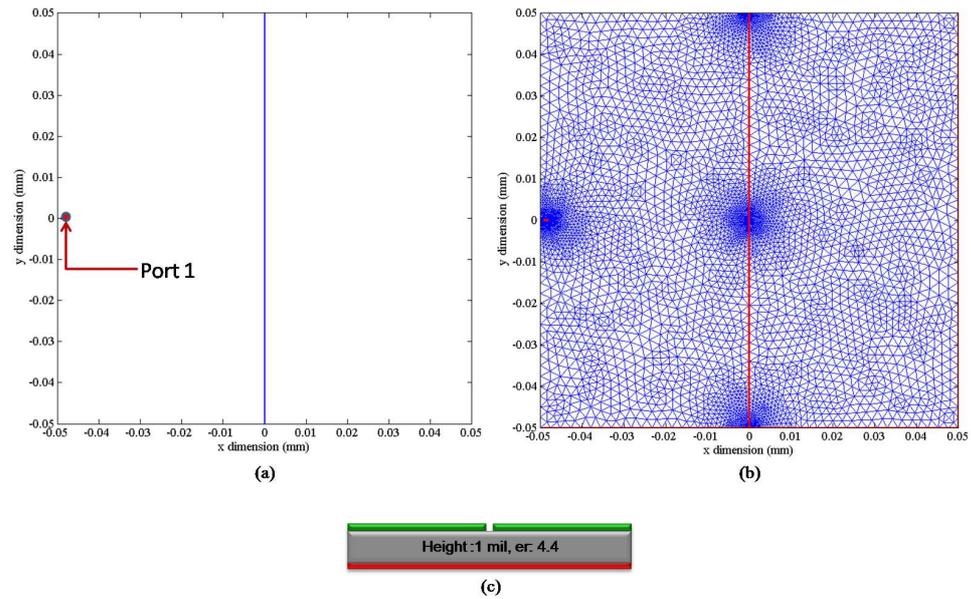
Figure 133. (a)Geometry of split-plane structure (b) Mesh (c) Cross-section.

to obtain an equivalent circuit enables the extension of the method to multiple plane pair geometries, without the need for using 3D-mesh elements (i.e. tetrahedral or hexahedral).

7.2.3 Results

The critical problem with finite difference methods such as MFDM is that in the presence of small features, the mesh becomes dense, as a result of which the number of unknowns in the system can be large. An example to illustrate this is a single plane-pair test case. The lower metal layer is a solid ground plane, while the top layer, of dimensions 100mm × 100mm contains a 0.2mm slot, dividing it into two 100mm×49.9mm islands. The geometry of the structure, the mesh, and the cross-section are shown in Figures 133(a), 133(b) and 133(c) respectively. The only port in the structure is placed on one of the power islands. The slot width (0.2 mm) is large enough when compared to the dielectric height (1 mil) that gap coupling can be ignored. As a consequence of the Delaunay mesh generation algorithm that has been used, the mesh is denser around small features and coarse elsewhere.
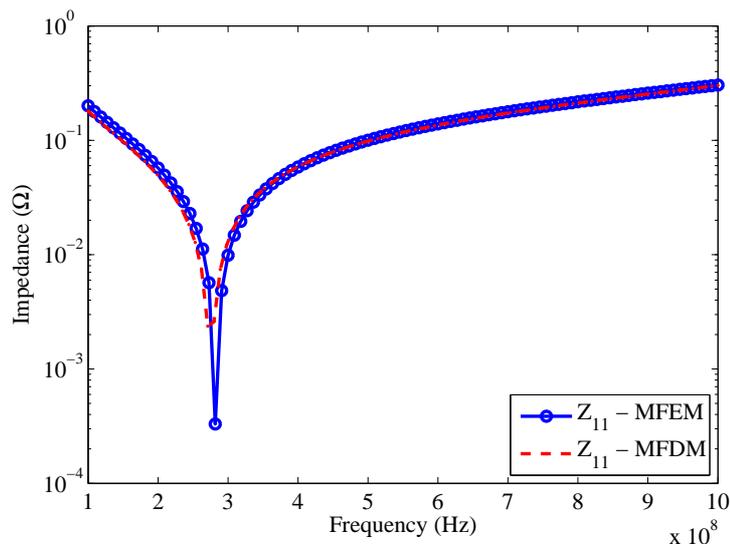
Figure 134. Self Impedance Z_{11}

Table 6. Summary of results for structure in Figure 134.

Method	Unknowns	Time / Freq Pt.	Code	MFEM Speed-up
MFEM	1,439	0.250 s	MATLAB	-
MFDM	250,000	10 s	C++	40X

The structure was simulated with MFEM, as well as MFDM. All simulations were performed on an Intel Core2 Duo 2.2 GHz workstation with 2.0 GB RAM. The impedance at Port 1, Z_{11} is shown in Figure 134, and there is good agreement between MFEM and MFDM. A summary of the computational requirements are listed in Table 6.

7.3   Formulation for Multiple Plane-Pairs

7.3.1   Meshing

As in the single plane-pair case, a triangular mesh is applied to each metal layer. As will be explained, the multi-layer formulation requires that the location of the mesh nodes be the same on every layer. This is done by flattening or collapsing the features on each metal layer on to one layer, on which triangulation is performed to obtain the mesh. The mesh thus obtained is used to discretize all layers. This is best explained
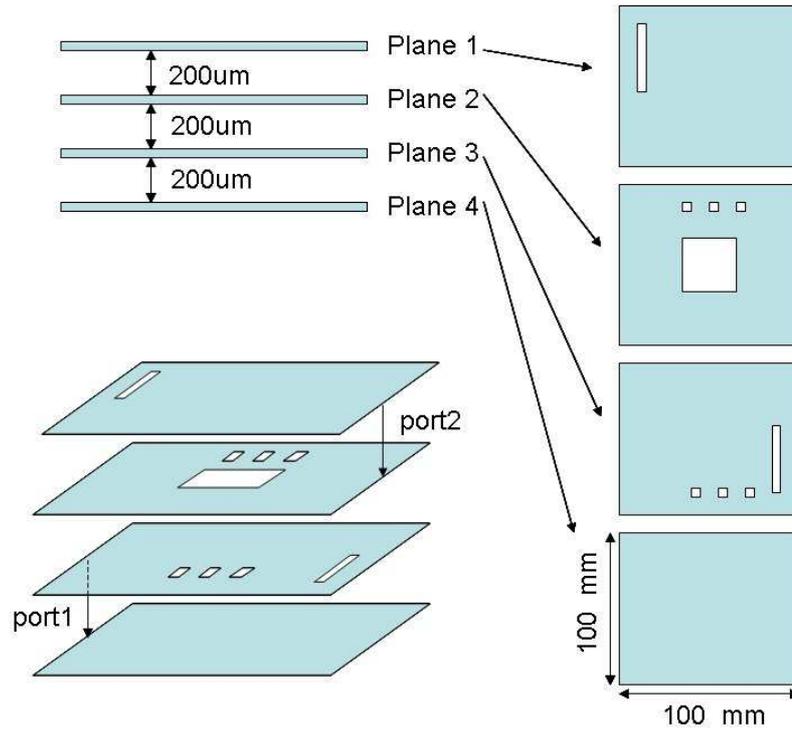
Figure 135. Four-plane test structure: cross section, location of ports, and top view of each plane.

using an example.

A four-layer structure containing apertures in each layer is shown in Figure 135. When all the features on the multiple layers is flattened onto one layer, the resulting 2D shape contains the outlines of the planes and all apertures. In Figure 136, this 2D shape with a triangular mesh is shown. This mesh can describe the geometrical features (polygon vertices and edges) in any of the layers. The method to obtain the admittance matrix for multiple plane-pair structures is described next.

7.3.2 Solid Planes without Apertures

In Section 7.2, the procedure to obtain an equivalent circuit for two-layer geometries with a common ground reference node has been described. For a multiple plane-pair structure containing more than two layers, it is possible to construct an equivalent circuit for each plane-pair. However, the equivalent circuit of different plane pairs
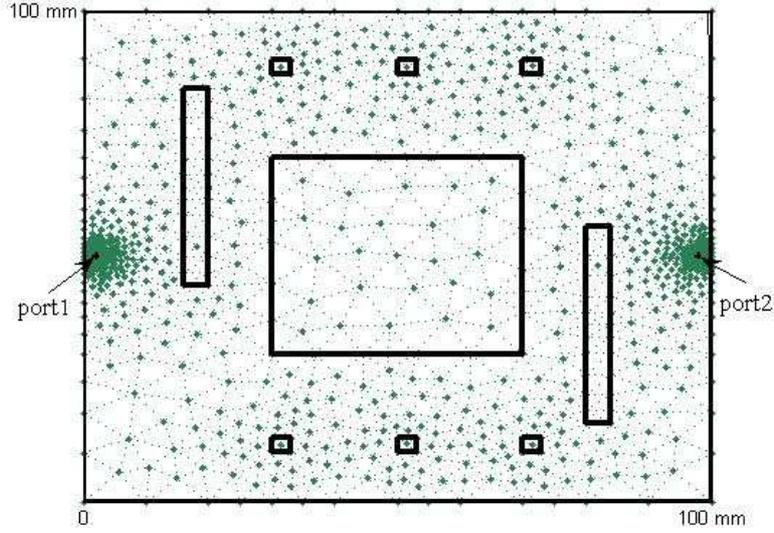
Figure 136. Top view of the meshed planes.

assign their respective ground reference node to different layers. Therefore, to obtain the model for the multi-layered plane requires shifting the different reference nodes to one common ground.

This shifting of ground reference nodes can be done using indefinite admittance matrices [20]. This is illustrated, without loss of generality, by using two-port networks with separate ground references, as shown in Figure 137(a). The four-port admittance matrix for the system with the common reference node can be derived as follows:

$$Y_{11}^A V_{1l} + Y_{12}^A V_{1r} = I_1 \tag{169}$$

$$Y_{11}^B V_{2l} + Y_{12}^B V_{2r} = I_2 \tag{170}$$

By noticing that

$$I_{bl} = I_2 - I_1, I_{al} = I_1,$$

$$V_{1l} = V_{al} - V_{bl}, V_{1r} = V_{ar} - V_{br},$$

$$V_{2l} = V_{bl} \text{ and } V_{2r} = V_{br},$$

Figure 137. (a) Two-port networks with separate references (b) Combined four-port network with common reference.

it is possible to write one row of the admittance matrix of the combined four-port.

$$Y_{11}^A(V_{al} - V_{bl}) + Y_{12}^A(V_{ar} - V_{br}) = I_{al} \tag{171}$$

A similar approach can be used to obtain the complete system in the following form:

$$\begin{pmatrix} Y^A & -Y^A \\ -Y^A & Y^A + Y^B \end{pmatrix} \begin{pmatrix} V_{al} \\ V_{ar} \\ V_{bl} \\ V_{br} \end{pmatrix} = \begin{pmatrix} I_{al} \\ I_{ar} \\ I_{bl} \\ I_{br} \end{pmatrix} \tag{172}$$

For an $M + 1$-layer (M plane-pair) package with solid power/ground planes on each layer, the system matrix, $\overline{\overline{Y}}$, is obtained as a simple extension of Equation 172.

$$\overline{\overline{Y}} = \begin{pmatrix} \overline{\overline{Y_1}} & -\overline{\overline{Y_1}} & & & \\ -\overline{\overline{Y_1}} & \overline{\overline{Y_1}} + \overline{\overline{Y_2}} & -\overline{\overline{Y_2}} & & \\ & \ddots & \ddots & \ddots & \\ & & & & -\overline{\overline{Y_{M-1}}} \\ & & & -\overline{\overline{Y_{M-1}}} & \overline{\overline{Y_{M-1}}} + \overline{\overline{Y_M}} \end{pmatrix} \tag{173}$$

where $\overline{\overline{Y}}_i$, $i = 1, 2, \ldots, M$ are admittance matrices obtained for the ith plane-pair counting from the top of the stack.

7.3.3 Inclusion of Apertures

Without apertures, the problem domain is simply a rectangle. In a more complex case with apertures, the flattened problem domain can be decomposed into a number of sub-domains, containing the solid metal planes and the apertures. To further explain this concept, an $M + 1$-layer package with an arbitrary number of apertures on each layer can be flattened into a rectangular problem domain containing N sub-domains. Each of these sub-domains represents one aperture or many overlapping apertures.

Thus, while adding the contributions of each layer i, $i = 1, 2, \ldots, M$, to the admittance matrix, the following cases are considered. As before, $i = 1$ is the top-most layer.

1. **Sub-domains $j_1, j_2, \ldots, j_P$ correspond to no apertures on layers i and $i + 1$:** This case is handled as in the previous sub-section. The contributions of the sub-domains $j_1, j_2, \ldots, j_P$ are added to $\overline{\overline{Y}}_i$ without alteration.

2. **Sub-domains $k_1, k_2, \ldots, k_Q$ correspond to apertures on layer i:** The contributions of sub-domains $k_1, k_2, \ldots, k_P$ are removed from $\overline{\overline{Y}}_i$.

3. **Sub-domains $l_1, l_2, \ldots, l_R$ correspond to apertures on layers $i + 1, i + 2, \ldots, i + X$:** The contributions of sub-domains $l_1, l_2, \ldots, l_R$ are removed from $\overline{\overline{Y}}_i$. Create admittance matrix M containing the contributions of the excluded sub-domains, with reference to corresponding nodes in layer $X + 1$.
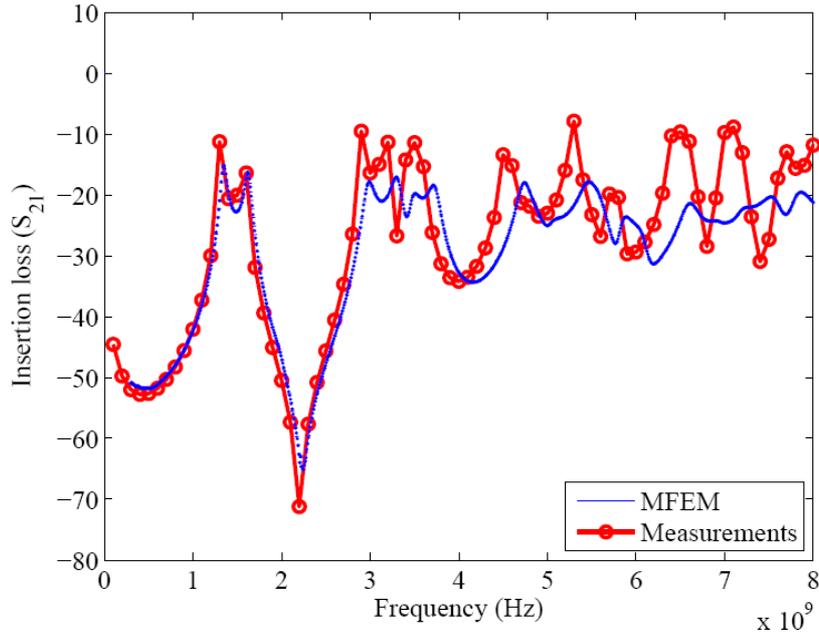
Figure 138. Insertion loss for structure in Figure 33.

7.3.4 Results

To validate MFEM, two test cases have been considered. The following test cases were designed to demonstrate the capability to model vertical coupling through apertures in the metal planes.

The geometry of the first test case is shown in Figure 33, along with the port locations.

However, from the insertion loss results shown in Figures 138, there is significant coupling between ports. This is due to aperture coupling. Also, the results from MFEM correlate well with measurements.

The second test case is the four-layer structure that was previously used to explain the meshing scheme, with plane dimensions of 100mm × 100mm. The differences in dimensions of each aperture was maximized to emphasize the meshing scheme employed by MFEM. Hence, the largest aperture size was 40×40 mm and the smallest was 3×3 mm. The minimum aperture size was chosen such that it still influenced the response of the structure at the maximum simulation frequency of 1GHz. Two ports
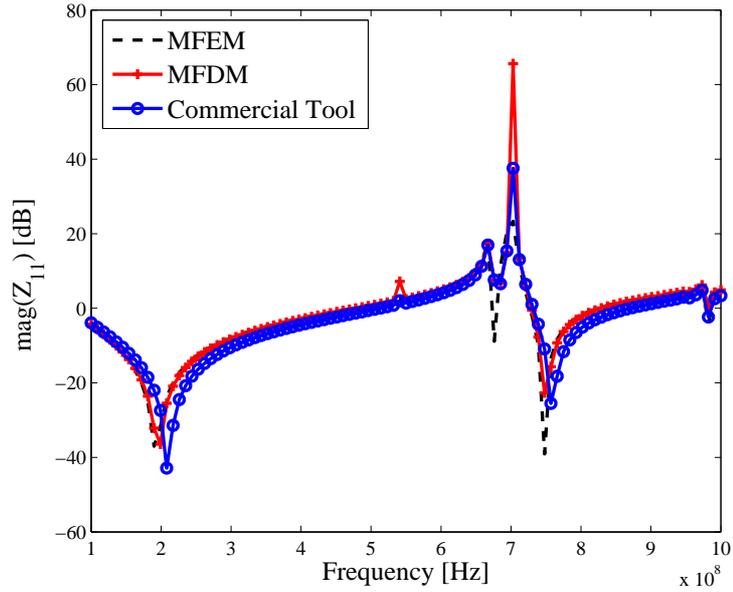
Figure 139. Magnitude of Self Impedance (Z_{11}).

Table 7. Summary of results for structure in Figure 135

Method	Unknowns	Time / Freq Pt.	Code	MFEM Speed-up
MFEM	3,594	0.350 s	MATLAB	-
MFDM	122,411	5.6 s	C++	16X
Comm. tool	71,204	2 s	Unknown	5.5X

are placed between the bottom plane (ground) and the second plane, and between the third plane and the top plane, respectively, as shown in Figure 135. The dielectric is FR-4 with $\epsilon_r = 4.4$.

The structure was simulated with MFEM, which has been implemented using MATLAB, and the results were compared with MFDM [55] and a commercial power integrity simulator. The commercial tool performs 2.5-D simulation using FEM. The self and transfer impedance results have been plotted in Figures 139 and 140. As can be seen from the results, there is good correlation between MFEM and the others methods. A summary of the results with timing information and implementation details has been provided in Table 7.
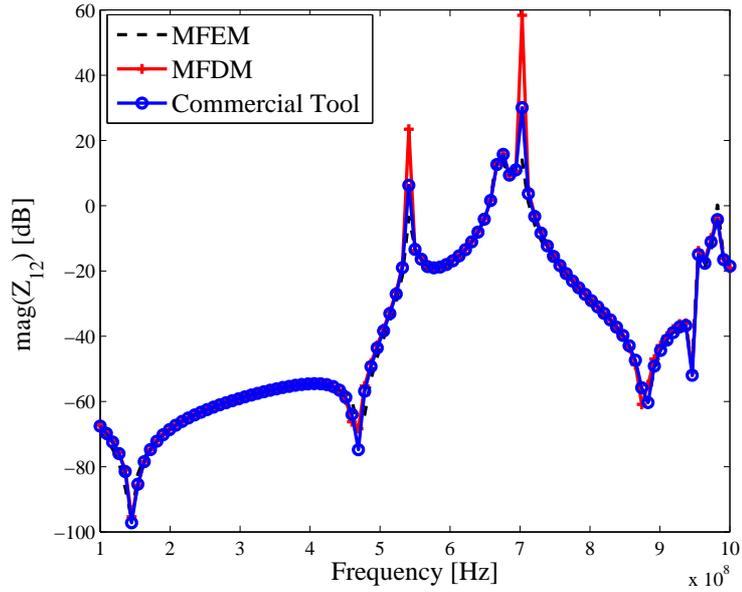
Figure 140. Magnitude of the transfer impedance (Z_{12}).

7.4 Summary

In this chapter, a novel modeling method to obtain the frequency response of multi-layer package power/ground planes has been proposed. This method, MFEM preserves several advantages of M-FDM. This includes a system that is sparse and a mesh that is applied only to the metal surfaces. Initial simulation results have demonstrated that MFEM requires significantly fewer unknowns while still providing accuracy comparable with other simulation methods. In the examples simulated in this chapter, the MFEM problem size is roughly in the thousands of unknowns, whereas the number of unknowns in M-FDM was in the hundred of thousands. This represents a reduction of around two orders of magnitude. Although this comparison must be treated cautiously, since the matrix structure of MFEM and M-FDM are not identical, MFEM has the potential to solve extremely large problems. Assuming that a maximum problem size of 500,000 unknowns (1/2 of M-FDM) can be solved using MFEM implemented with a direct solver, MFEM is capable of solving 50 - 500 layers. This is based on the assumption that each layer requires between 1,000 and 10,000

unknowns to discretize. A promising application of MFEM is in the simulation of multi-scale geometries or in the combined simulation of package and board.

CHAPTER 8

CONCLUSIONS

Typically, the power to ICs is supplied through a package power distribution network consisting of multiple stacked, electrically-large, metal planes which are assigned to different DC potentials. The management and mitigation of simultaneous switching noise (SSN) is the key design parameter goal intended to maintain a clean power supply on chip. To enable rapid design of these packages, modeling methods must be able to model arbitrarily shaped packages containing apertures in the metal planes, vias, decoupling capacitors, etc. Also, the signal lines are routed in between the stacked power/ground layers. These signal lines use the power/ground planes of the PDN as reference planes, and poor designs can cause coupling of energy between the PDN and the signal transmission lines, through mode conversion.

The objective of this research is the development of a signal and power integrity (SI/PI) modeling and co-simulation tool for package and board applications. The proposed method, which forms the main focus of this thesis, is called the multi-layer finite difference method (M-FDM).

M-FDM is a hybrid modeling approach that combines EM and network theory. The approach was developed by first applying a finite difference formulation to packages with two metal-layer or single plane-pair geometries. An equivalent circuit was extracted based on the finite difference equations. Using transformations of the indefinite admittance matrix, this method was extended to multiple plane-pair structures. This approach was capable of modeling the vertical coupling of SSN by means of a wrap-around current.

Also, the modal decomposition technique was used to integrate the response of transmission lines in microstrip, stripline and conductor backed CPW configurations with the model for the PDN from M-FDM.

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The key advantages of M-FDM are the following:

1. Mesh is applied only to the metal layers. Dielectrics are not meshed.

2. The model from M-FDM can be integrated with models for transmission lines based on modal decomposition.

3. The computational complexity of M-FDM is $O(N^{1.5})$ and the memory complexity is $O(N \log_2 \sqrt{N})$.

4. The model generated using M-FDM is a SPICE compatible equivalent circuit

The limitations of M-FDM are the following:

1. The modeling method is based on an assumption that only vertically directed electric field components exist in the package. Hence, fringing fields at metal edges and due to slots in the metal planes are neglected

2. The mesh applied to M-FDM consists of square unit-cells, the dimensions of which are determined by the minimum feature size in the geometry. Thus, the maximum number of layers that can be modeled for a practical package is limited.

This thesis addresses the limitations of M-FDM as well. To model the fringing fields at metal edges and near slots, methods called the fringe augmentation (FA) and the plane gap augmentation (PGA) were developed. These approaches are based on obtaining a multiport circuit model for a coupling network that can be represented as corrections to the admittance matrix obtained from M-FDM. These corrections are obtained by performing a 2D electrostatic simulation of the cross-section at the location of the discontinuity. In the case of the FA method, there is no increase in computational complexity required to solve the system containing the updated admittance matrix. For the PGA method, there is an increase in the number of

unknowns and the bandwidth of the system matrix, but the increase in computational complexity, which has been quantified, is small.

The second limitation, resulting from the use of the square mesh, has been solved based on initial results from a promising novel approach called the multi-layer finite element method (MFEM). An adaptive triangular mesh was applied to the geometry. The dimensions of the edge elements in this mesh are based on the wavelength at the maximum frequency of simulation. The mesh becomes dense only in the vicinity of small features. This enables MFEM to model realistic structures containing such small features with far fewer unknowns than M-FDM. Also, the model generated using MFEM is also SPICE compatible, and the resultant system matrix is sparse. Thus MFEM preserves the advantages of M-FDM, while overcoming the mesh density limitation.

However, the first limitation of M-FDM which was addressed with the FA and PGA techniques applies to MFEM as well. Since the model from MFEM can be expressed as an equivalent circuit, it is possible to conceptualize an approach similar to the FA and PGA methods that can be applied to MFEM. This has been left as future work.

The methods described in this thesis have been implemented in a tool called MSDT 1. These tools are currently in use by the commercial sponsors of this work, Panasonic, EPCOS, Infineon, NXP and Sameer. These tools are also made available to students of ECE 4460.

8.1 Papers Published

The following publications are a result of this work:

8.1.1 Journal Publications

1. A.E. Engin, K. Bharath and M. Swaminathan,"Multilayered Finite-Difference Method (M-FDM) for Modeling of Package and Printed Circuit Board Planes", in *IEEE Trans. on Electromag. Compat.*, Vol. 49, Issue 2, pp. 441–447, May 2007.

2. K. Bharath, N. Sankaran and M. Swaminathan, "Multi-Layer Fringe-Field Augmentations for the Efficient Modeling of Package Power Planes", submitted for review in *IEEE Trans. on Adv. Pkging.*

8.1.2 Conference Publications

1. K. Bharath, A. E. Engin and M. Swaminathan,"Modeling of EBG Structures using the Transmission Matrix Method," in *Proc. of PIERS*, 2006.

2. R. Mandrekar, K. Bharath, K. Srinivasan, A.E. Engin and M. Swaminathan, "System Level Signal and Power Integrity Analysis Methodology for System-In-Package Applications," in *Proc. of 43rd DAC*, pp. 1009 – 1012, July 2006.

3. K. Bharath, A. E. Engin, M. Swaminathan, K. Uriu and T. Yamada,"Efficient Modeling of Package Power Delivery Networks with Fringing Fields and Gap Coupling in Mixed Signal Systems," in *Proc. of the 14th IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 59 – 62, October 2006.

4. A.E. Engin, K. Bharath, K. Srinivasan and M. Swaminathan, "Modeling of Multilayered Packages and Boards using Modal Decomposition and Finite Difference Methods," in *Proc. of Electromagnetic Compatibility Symposium*, 2006.

5. A.E. Engin, K. Bharath, M. Swaminathan, et. al., "Finite-difference modeling

of noise coupling between power/ground planes in multilayered packages and boards," in *Proc. of 56th Electronic Components and Technology Conference*, pp. 1262 – 1267, June 2006.

6. K. Bharath, A.E. Engin, M. Swaminathan, K. Uriu and T. Yamada, "Simulation of Power/Ground Planes for SiP Applications," in *Proc. of 57th Electronic Components and Technology Conference* , pp. 1199 – 1205, May2007.

7. K. Bharath, A. E. Engin and M. Swaminathan, "Analysis for Signal and Power Integrity Using the Multilayered Finite Difference Method," in *Proc. Of IEEE International Symposium on Circuits and Systems*, pp. 1493 – 1496, May 2007.

8. K. Bharath, A.E. Engin, M. Swaminathan, K. Uriu and T. Yamada, "Signal and Power Integrity Co-Simulation for Multi-layered System on Package Modules," in *Proc. of Electromagnetic Compatibility Symposium Symposium*, pp. 1 – 6, July 2007.

9. K. Bharath, A.E. Engin, M. Swaminathan, K. Uriu and T. Yamada, "Computationally Efficient Power Integrity Simulation for System on Package Applications," in *Proc. of 44th Design Automation Conference*, pp. 612 – 617, June 2007.

10. K. Bharath, A.E. Engin and M. Swaminathan, "Automatic Package and Board Decoupling Capacitor Placement Using Genetic Algorithms and M-FDM", in *Proc. of 45th Design Automation Conference*, pp. 560 – 565 , June 2008.

11. K. Bharath, A.E. Engin, N. Sankaran and M. Swaminathan, "Multi-Layer Fringe-Field Augmentations for the Efficient Modeling of Package Power Planes", in *Proc. of 16th IEEE Conference on Electrical Performance of Electronic Packaging*, Oct 2008.

12. K. Bharath, J. Y. Choi and M. Swaminathan, "Use of the Finite Element Method for the Modeling of Multi-Layered Power/Ground Planes with Small Features", accepted for publication in *Proc. of 58th Electronic Components and Technology Conference*, June 2008.

13. K. Bharath, J. Y. Choi and M. Swaminathan, "Multi-Layer Finite Element Method (MFEM) for the Modeling of Package and PCB Power/Ground Planes", accepted for publication in *the 2009 International Symposium on Electromagnetic Compatibility*, July 2009.

8.2   Award

Received the best student paper award at the *16th IEEE Conference on Electrical Performance of Electronic Packaging* for the paper "Multi-Layer Fringe-Field Augmentations for the Efficient Modeling of Package Power Planes"

8.3   Invention Disclosure

K. Bharath and M. Swaminathan, Multi-layer finite element method (MFEM) for the modeling of package power/ground planes." US provisional patent 61/154,543, filed February 2009.

APPENDIX A

NETWORK DATA CONVERSIONS

The characteristic of an $n-$port network are typically represented in terms of 50 Ω S-parameters. This thesis primarily discusses methods which provide Z-parameters.

The relations between S- and Z-parameters are given by:

$$Z = \sqrt{Z_0}\,(I - S)^{-1}\,(I + S)^{-1}\,\sqrt{Z_0} \qquad (174)$$

$$S = (Z - Z_0)\,(Z + Z_0)^{-1} \qquad (175)$$

where I is an $n \times n$ identity matrix and Z_0 is an $n \times n$ diagonal matrix and $Z_0(i,i)$ contains the characteristic impedance of the ith port.

The conversions between Z and Y are given by,

$$Z = (Y)^{-1} \qquad (176)$$

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