

**ADVANCES IN ELECTRONIC PACKAGING TECHNOLOGIES BY ULTRA-
SMALL MICROVIAS, SUPER-FINE INTERCONNECTIONS AND LOW LOSS
POLYMER DIELECTRICS**

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The Academic Faculty

by

Venkatesh Sundaram

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Doctor of Philosophy in the

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**ADVANCES IN ELECTRONIC PACKAGING TECHNOLOGIES BY ULTRA-
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POLYMER DIELECTRICS**

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TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	iii
LIST OF TABLES	ix
LIST OF FIGURES	x
LIST OF SYMBOLS AND ABBREVIATIONS	xx
SUMMARY	xxi
<u>CHAPTER</u>	
1. Introduction And Objectives	1
1.1. Thesis Motivation: Bridge The Widening Interconnect Gap Between IC and Package Substrate	1
1.2. Research Objectives Driven by Wiring Gap	6
1.3. Historical Development & Current State of the Art Ultra High Density Wiring Substrates	7
1.3.1. Thin Film on Ceramic	10
1.3.2. Thin Film on Silicon	11
1.3.3. Sequential Build-Up Organic Substrates	14
1.4. Technical Barriers to Address the Wiring Gap	16
1.5. Research Outline to Address Barriers and Gaps	17
2. Low CTE Core Substrates	21
2.1. Property Requirements and Selection of Core Substrates	21
2.2. Core Substrate Materials Studied in this Research	24

2.3. Results and Discussion - Source of Surface Defects and Roughness In C-SiC Substrates	25
2.4. Results And Discussion - Surface Planarization For Ultra-Fine Line Conductors	27
3. Polymer Dielectrics Basics & Advanced Deposition Processes	32
3.1. Historical Trends In Polymer Dielectrics	32
3.2. Epoxy Dielectric: Chemistry, Processing-Structure-Property Relationship	34
3.3. Emerging Needs For Next Generation Of Polymer Dielectrics	37
3.4. Low Loss Polymer Dielectrics & Processes Explored In This Research	38
3.4.1. Benzocyclobutene (BCB) Dielectric Polymer Microstructure And Properties	39
3.4.2. Liquid Crystal Polymer (LCP) Structure And Properties	41
3.4.3. Low Loss Polymer Structure-Property Relationship And Processing Challenges	43
3.5. Ultra-Thin Polymer Dielectric Film Deposition Process-Structure-Property Relationship	46
4. Advanced, Ultra-Small Microvia Formation Processes	60
4.1. Photovia Process To Achieve 25 μ m Via Diameter In Epoxy Dielectric	61
4.2. Excimer And UV Laser Ablation Of Small Microvias – Photo Ablation By Nanosecond Excimer Laser And Downscaling Of Via Diameter (10-30 μ m) In Ultra-Thin (10-25 μ m Thickness) Low Loss Polymer Dielectrics	68
4.3. Nd-YAG Laser Ablation Of 30-40 μ m Diameter Microvias In RXP-4	73

4.4. Excimer Laser Ablation System And Process Fundamentals	77
4.5. Chemistry And Physics Of Polymer Ablation By Nanosecond Pulsed 308nm Excimer Lasers	83
4.6. Excimer Laser Ablation Of 25-50 μ m Diameter Microvias In LCP	85
4.6.1. Excimer Laser (308nm) Ablation Of 25 μ m Thick LCP Film	88
4.6.2. Discussion Of 25-50 μ m Microvia Ablation In 25 μ m Thick LCP Film	91
4.6.3. Effect Of Via Size And Fluence On Carbon Re-Deposition, Debris Removal And Cone Formation	95
4.7. Excimer Laser Ablation Of 10-40 μ m Diameter Microvias In BCB	100
4.8. Chapter Summary	110
5. Advanced Conductor Metallization And Plasma Surface Modification	111
Processes	
5.1. Major Challenges For Ultra-Fine Line Conductors	112
5.2. Dielectric-Copper Interface Control For Low Conductor Loss In The Multiple Ghz Frequency Range	114
5.2.1. Processing Techniques For Polymer Dielectric Surface Treatment	116
5.2.2. Chemical & RF Plasma Roughening Of Low Loss Polymers	121
5.2.3. Impact Of Dielectric Surface Roughness On Sub-10 μ m Copper Lines	128
5.3. Advanced Processes For <10 μ m Lines/Spaces And Extreme-Fine Line Copper Conductor Formation Using Low Cost Package Substrate Materials	130
5.3.1. Ultra-Fine Line Test Vehicle Design And Layout	130
5.3.2. Metallization Process Approaches For Ultra-Fine Lines And Spacing	131

5.3.3. Semi-Additive Plating (SAP) Process	132
5.3.4. Low Stress Electroless Plating	134
5.3.5. Low Cost And Ultra-Fine Line Photolithography	136
5.3.5.1.UV Lithography Methods	137
5.3.5.2.Principles For Resolution Of Proximity Photolithography	137
5.3.5.3.Experiments On Gap Effect	138
5.3.5.4.Calculations On Gap Effect	141
5.3.5.5. Photo Resist And Fine Line Formation Challenges	142
5.3.5.6.Electrolytic Plating Process And Sub-10 μ m Line/Space Results	143
5.3.5.7. Surface Irregularity Challenges For Sub-10 μ m Lines And Spaces	147
5.4. New Sub-10 μ m Copper Conductor Surface Treatment Process	153
5.4.1. Advanced Copper Surface Treatment Process Description	153
5.4.2. Copper Adhesion Process Testing Results	157
5.4.3. Advanced Silane Treatment Process For Sub-10 μ m Lines/Spaces	159
5.5. Chapter Summary	161
6. Next Generation Advanced Organic Substrate Integration Research	162
7. Summary and Conclusions, Future Work	168
8. Scientific And Technical Contributions	173
REFERENCES	177

LIST OF TABLES

		Page
Table 1.1	Microprocessor Performance Parameters for 2004 and 2010 from ITRS Roadmap	04
Table 1.2	Comparison of State-of-the-art and Proposed Research Parameters	20
Table 2.1	Comparison of Electrical and Mechanical Properties of SiC Composite Substrates with Carbon, Alumina and Glass Fiber Reinforcement	25
Table 3.1	Molar Polarization Comparison of Various Polymer Functional Groups	44
Table 3.2	Summary of Electrical and Thermo-mechanical Properties of Build-up Dielectrics	45
Table 4.1	Calculated Values of Y Scan Feed Rate (vs) for Various Repetition Rates (R in Hz) for a Dose (NAbl) of 500 pulses @ 200mJ/cm ² /pulse	90
Table 5.1	Summary of Wyko Surface Analysis of Chemical and Plasma Treated ABF GX-13 Epoxy Dielectric (all units in μm)	122
Table 5.2	Fabricated and calculated Lmin/Smin on 8μm thick photo resist in proximity mode lithography	142
Table 5.3	Secure™ HFz Process	155
Table 5.4	AFM Surface Analysis Before and After Copper Surface Treatment	158
Table 5.5	Line Width and Space Measurements of Untreated and Silane Treated Copper Fine Lines and Comparison to Bond Film etch based adhesion Treatment	160
Table 6.1	High Frequency Measurement Results for Embedded RF Capacitors in 50μm thick LCP	164

LIST OF FIGURES

	Page
Figure 1.1 Bridging the Widening Interconnect Gap Through Ultra-High Density Substrate Wiring Research	03
Figure 1.2 Component Integration Trends and Package Substrate Wiring Density Increase	08
Figure 1.3 Key Milestones in the Evolution of High Density Substrates	09
Figure 1.4 Dual Level Metal (DLM) Stacked Via Process for Cu-Polyimide on Ceramic Substrate by IBM	10
Figure 1.5 Cross-section schematic of thin film on silicon (TFOS) substrate technology by AT&T Bell Labs	12
Figure 1.6 Top View and Cross-Section of Fully Packaged Multi Chip Module using Cu-Polyimide TFOS Substrate	12
Figure 1.7 GE Chips-First HDI Substrate Technology with Cu-polyimide thin film multilayer wiring	13
Figure 1.8 Thick and Thin Film Organic Substrate Microvia Technologies Worldwide	15
Figure 1.9 Eight Major Research Elements in the Proposed SOP Substrate Research	18
Figure 2.1 Correlation of Substrate Warpage and Via-Pad Misalignment	22
Figure 2.2 Thermo-mechanical Modeling of Substrate Warpage Based on Modulus & Thin Film Build-up Process	23
Figure 2.3 Thermo-mechanical Properties of Core Substrates Explored in this Research	24
Figure 2.4 Fabrication Process for Carbon Fiber Reinforced SiC Composite	26

	Substrate	
Figure 2.5	Schematic of the surface roughness. Typically, pores of three size ranges can be seen (around 3-5 microns, 5-15 microns and 20-60 microns)	27
Figure 2.6	Effect of liquid coating process on the planarization of the C-SiC substrate (left) and photograph of coated and cured substrate showing surface defects (right)	28
Figure 2.7	Tenting of polyimide film over large pits on the surface of C-SiC substrate	29
Figure 2.8	(a) Complete flow and fill planarization of Carbon fiber bundles on the surface of C-SiC substrates by Speedboard lamination	30
	(b) Incomplete planarization of large pits due to insufficient resin	30
Figure 2.9	Profiles of C-SiC Substrate “Before” and “After” Planarization	31
Figure 2.10	Cross-section of C-SiC Substrate Planarized with Speedboard C prepreg	31
Figure 3.1	Historical evolution of dielectric materials	33
Figure 3.2	Structure of the Main Constituents of Epoxy Resins, (a) Bisphenol A, (b) Epichlorhydrin, and (c) Bromine functional side groups	34
Figure 3.3	Chemical Reaction in Polymerization of Epoxy Dielectric	34
Figure 3.4	Various Stages in the Cross-linking & Curing of Epoxy Dielectrics	35
Figure 3.5	Process for the Synthesis of BCB	40
Figure 3.6	Diels-Alder Reaction for Polymerization and Curing of BCB	41
Figure 3.7	Structure of Monomers used for the Synthesis of Vectra™ LCP	42
Figure 3.8	Structure of Aromatic Ester typical of Liquid Crystal Polymers	43
Figure 3.9	Dielectric Deposition Challenge for the Current Research Compared to State-of-the-Art	47
Figure 3.10	Conventional Melt Flow Extrusion Process for LCP results in Electrical and Mechanical Property Anisotropy	47

Figure 3.11 Counter-Rotating Die Concept for Producing LCP Dielectric Films with Biaxial In-Plane Property Isotropy	48
Figure 3.12 Uniaxial and Biaxial Orientation of LCP Films	49
Figure 3.13 Four, Six and Eight Metal Layer Thin All-LCP Substrate Cross-section Schematic	50
Figure 3.14 Drop in Modulus of LCP with Temperature as measured by DMA analysis	51
Figure 3.15 Lamination profiles optimized for multilayer LCP substrate shown in Figure 3.14	52
Figure 3.16 Distortion in Metal Traces during LCP Lamination at Temperature Much Above the Melting Point (280°C) as seen in (a) Microsection, and (b) X-Ray imaging	53
Figure 3.17 Delamination due to Insufficient Melting and Bonding of LCP at 260-270°C	54
Figure 3.18 Results from Optimized Lamination of LCP Core and LCP Bondply showing excellent layer to layer alignment, no distortion and good bonding as seen in X-ray image (left) and microsections (right)	54
Figure 3.19 Target Structure for BCB deposition on C-SiC (left) and low CTE laminate (right) core substrates	56
Figure 3.20 BCB Film Thickness after Curing and Plasma Surface Treatment plotted against Spin Speed	57
Figure 3.21 Planarization of BCB Thin Film after (a) spin coating and curing, and (b) using an intermediate planarization step before curing	58
Figure 3.22 Lamination Schematic for Thin Low Loss RXP-4 Thermoset Dielectric Film (left bottom) and excellent planarity achieved after optimized	59

	lamination of 18 μ m thick RXP-4 dielectric (right)	
Figure 4.1	Microvia Fabrication Technologies for Package Substrates	60
Figure 4.2	Process Sequence for Photo-Via Fabrication	62
Figure 4.3	Fundamental Polymer Reactions during Photo-Epoxy Via Processing	63
Figure 4.4	Microvia Daisy Chain Test Structures (Left), and Fabricated Substrate with Photo Microvias (Right)	65
Figure 4.5	Micro-sections of 25 μ m and 50 μ m Diameter Microvias in Photo-Epoxy that Survived after 2000 Thermal Shock Cycles	66
Figure 4.6	Micro-section of 50 μ m Diameter Microvia in Photo-Epoxy that Failed during Thermal Shock Testing	67
Figure 4.7	Photograph of Nd-YAG laser during ablation	68
Figure 4.8	Trends in Down Scaling of Microvias and Three Major Laser Technologies	70
Figure 4.9	Mechanism of Ablation	71
Figure 4.10	Typical Configuration of a Nd-YAG UV Laser for Point to Point Ablation	73
Figure 4.11	Two Step UV Laser Ablation Process to Improve Throughput for Dielectric Ablation and Precise Stopping on Copper Landing Pad	74
Figure 4.12	Damage to 8 μ m thick copper landing pad with 1W power setting for UV laser ablation of 18 μ m thick RXP-4 low loss dielectric (10 μ m dielectric via depth)	75
Figure 4.13	Optimized 30 μ m Top Diameter Microvias in RXP-4 by UV Laser Ablation at low power (<0.5W)	76
Figure 4.14	Top View of a 30 μ m Microvias in RXP-4 after Metallization (left) and Microsection Picture of Plated Microvia with Top Diameter of 40 μ m	77
Figure 4.15	Scanning projection lithography/ablation system with a 308nm excimer	78

laser	
Figure 4.16 Schematic of the various components of the Anvik 2150 SXE Excimer Laser Lithography/Ablation System at Georgia Tech PRC	80
Figure 4.17 Illustration of the seamless scanning technique used in the Anvik 2150 SXE Excimer laser system	82
Figure 4.18 Debris Removal System (DRS) using He & Vac to Remove Ablation Debris	83
Figure 4.19 Potential Bond Breaking Sites for Typical Polymers During 308nm Laser “Photo-chemical” Ablation	84
Figure 4.20 Ablation Depth vs. Dose for Various Fluences for LCP	85
Figure 4.21 Etch Rate vs. Fluence for LCP (threshold around 70 mJ/cm ²)	86
Figure 4.22 Extraction of Linear Absorption Coefficient from Etch Rates for LCP	87
Figure 4.23 Copper Window Etched in Foil on LCP (left) and Via after Ablation through 62.5μm diameter copper window (right) in 25μm LCP film	89
Figure 4.24 Top View of Ablated Feature (left) and Cross-section Schematic Illustrating Stalagmitic Cone Structures on the Floor of the Via Due to C and Cu Re-deposition	91
Figure 4.25 View of the etched copper window at the Cu-LCP interface	92
Figure 4.26 Top View of the Ablated Alignment Feature after Smoothing of the Copper Windows, Carbon re-deposition and cone formation can still be observed	93
Figure 4.27 Carbon re-deposits removed by O ₂ plasma clean (left) and after subsequent ablation (right)	94
Figure 4.28 Cross-section of “Cone” structure formed during laser ablation after electroless and electrolytic copper plating	95

Figure 4.29 Three Different Via Sizes Ablated at Identical Conditions showing correlation between via size and amount of cones formed	96
Figure 4.30 Evolution of Excimer Laser Ablation of LCP; top views after 250 pulses (top), and microsections (bottom)	97
Figure 4.31 Vias of 50, 37.5 and 25 μ m diameter after major steps in the via formation process	98
Figure 4.32 Scanning electron micrograph top view of a 50 μ m microvia in LCP	99
Figure 4.33 Demonstrated 25 μ m, 37.5 μ m, and 50 μ m Excimer Laser Ablated Microvias after Electroless and Electroplating of LCP	100
Figure 4.34 UV-vis absorption spectra for DVS-BCB compared to other common polymers used in microelectronics applications	102
Figure 4.35 Ablation Depth vs. Dose for BCB (Cyclotene 3022) at 200mJ/cm ² /pulse	103
Figure 4.36 Cross-section schematic of new conformal mask method using high resolution photoresist for BCB excimer laser ablation	104
Figure 4.37 Micrographs of Top Surface of Eagle NT-90 photoresist coated on BCB (underlying Cu patterns) at various ablation doses at 200mJ/cm ² /pulse and 200Hz	105
Figure 4.38 Surface profilometry scans of the NT-90/BCB/Cu structure before and after 308nm excimer laser ablation	106
Figure 4.39 Profilometry scans of BCB Microvia after laser ablation (left) and after plasma treatment (right) showing removal of 5 μ m NT-90 and roughening of BCB	107
Figure 4.40 Demonstration of 15-25 μ m Vias in BCB by 308nm Excimer Laser Ablation. 5-6 μ m wide ablated channels can also be seen in the picture	108
Figure 4.41 Electroless Cu plated and annealed hexagonal laser ablated areas in BCB	109

Figure 4.42	Microsections of 20 μ m Diameter Microvias in BCB after Electroless Cu seed layer deposition	110
Figure 5.1	Wiring Density in terms of Lines/Spaces and Via/Pad Dimensions Required for 20-100 μ m pitch area array flip-chip package substrates	112
Figure 5.2	Illustration of Critical Interfaces for ultra-fine line multilayer copper wiring: Cu-to-polymer (a) and polymer-to-Cu (b)	113
Figure 5.3	Skin depth at various frequencies (schematic – left) for common metals	115
Figure 5.4	Plasma Etching System (Plasma Etch BT-1) for 300mm x 300mm substrates	117
Figure 5.5	Plasma Etching Fundamentals (left) and Schematic and Equivalent Circuit for Capacitively Coupled RF Plasma	118
Figure 5.6	Wyko NT1100 Optical Interferometer and Operating Principle	121
Figure 5.7	Wyko Surface Scans at 25x Magnification for Chemical and Plasma Treated ABF GX-13 Epoxy Dielectric	123
Figure 5.8	Summary of Optical Interferometry Analysis of Surface Roughness for BCB	125
Figure 5.9	Surface Profile (\AA) of BCB after CF ₄ /O ₂ Plasma Treatment for 12 minutes	126
Figure 5.10	FESEM Images of BCB Surface Before and After CF ₄ /O ₂ Plasma	126
Figure 5.11	Summary of Optical Interferometry Analysis of Surface Roughness for LCP	128
Figure 5.12	High Magnification Optical Micrographs of Surface of Build-up Dielectric after (a) permanganate desmear, and (b) plasma desmear showing overlay of 10 μ m line	129
Figure 5.13	SEM micrograph of defects in 10 μ m lines due to deep pits from	129

chemical desmear	
Figure 5.14 Process test vehicle (TV) as designed (above images), and as fabricated (below) containing various test structures for fine line and space process Development	130
Figure 5.15 Fine Pitch Traces (20 μ m Line Width, 20 μ m Spacing) by Copper Etching (Top view and Micro-section) with Copper Thickness of 12 μ m (aspect ratio 1.6:1)	132
Figure 5.16 Process Flow for Semi-Additive Process (SAP)	132
Figure 5.17 Advanced Electroless Copper Plating System with Pd Activation	135
Figure 5.18 Electroless Plated Cu Uniformity Measurement by XRF for 1hr (front only) and 2hr plating time (front and back side) of 300mm x 300mm substrate	135
Figure 5.19 Principle of photolithography with UV light. Light diffraction becomes problematic when transparent area becomes smaller	138
Figure 5.20 UV Beam Intensity on the surface of photoresist. When Δ reaches $L/2$, the comb structure having equal line and space will not be resolved	138
Figure 5.21 Experimental Setup for UV exposure at different gap distances for studying the gap effect on the resolution of proximity mode photolithography	140
Figure 5.22 Optical micrograph of test comb structure with equal line width and space. 7 μ m line and space resolved on 8 μ m thick photo resist at a gap of 30 μ m by using i-line UV lithography	140
Figure 5.23 Calculated (lower) and fabricated minimum (upper) line and space with various gap distances between photo-mask and an 8 μ m thick photo resist	142
Figure 5.24 Feature Width Deviation from Designed Values for Dry Film Photoresist	144

Figure 5.25 Typical waveform for pulse reverse plating	145
Figure 5.26 Plated copper traces with line widths and space widths of 10/15/20/ 25 μ m on ABF/BT by using dry film photo resist provided by DuPont. The copper thickness measured is 18 μ m.	146
Figure 5.27 Ultra-fine line routing on ABF for 100 μ m pitch flip chip with 40 μ m pads. Line and space shown at 8.6 μ m for 3 lines/channel routing & Cu thickness of 8.5 μ m	147
Figure 5.28 Non-planar surface, due to thick copper trace under the dielectric layer, resulting in photolithography non-uniformity for 10 μ m lines/spaces in 15 μ m thick photoresist	149
Figure 5.29 “Bridge” effect showing very thin photoresist film remaining in the opening	150
Figure 5.30 Explanation for bridge effect in narrow photoresist spaces by UV light scattering between mask and resist under the opaque areas of the mask	151
Figure 5.31 (a) & (b) Fine line photoresist lifting caused by insufficient adhesion	151
Figure 5.32 Comparison of glass mask (left) and plated copper (right) for a structure with 5 μ m and 10 μ m lines/spaces on a epoxy build-up layer on FR-4	152
Figure 5.33 Microsection of high aspect ratio plated copper fine lines with 10 μ m line/space and 18 μ m copper thickness	152
Figure 5.34 Process Sequence from SAP to Subsequent Build-up Layer Fabrication	153
Figure 5.35 SEM micrograph of a 12 μ m wide copper conductor chemically treated with a conventional micro-roughening process for adhesion	154
Figure 5.36 12 μ m conductor before adhesion promotion treatment	157
Figure 5.37 SEM micrograph of 12 μ m line after treatment with silane filming process	158

Figure 5.38	SEM micrographs of 5-12 μ m lines/spaces after Sn-silane treatment	160
Figure 5.39	Conductor cross-section (left) and summary (right) of interface roughness measured for various materials and processes	161
Figure 6.1	Two Metal Layer High Density LCP Substrate with Embedded RF Passives	163
Figure 6.2	Capacitor Structures in Two Metal Layer LCP Substrate with Microvias	163
Figure 6.3	Low CTE Composite Substrate with Cu-Invar-Cu Core and LCP Dielectric (left) and after assembly of 200 μ m pitch flip chip IC (right)	165
Figure 6.4	All-LCP Substrate Panel (12"x18") with Six Metal Layer Test Structures	165
Figure 6.5	Top view of BCB coated on CIC-PTFE Core (left), and microsections of completed BCB build-up substrate on C-SiC (middle) and CIC-PTFE (right)	166
Figure 6.6	Ultra-Thin Four Metal Layer High Density and Low Loss RXP based Organic Substrate	167

LIST OF SYMBOLS AND ABBREVIATIONS

SOP	System on a Package
SOC	System on a Chip
SiP	System in Package
SiP	System in Package
MCM	Multi Chip Module
MEMS	Micro Electro Mechanical Systems
RF	Radio Frequency
MCM	Multi Chip Module
CTE or TCE	Coefficient of Thermal Expansion
3-D	Three Dimensional Package or Chip Stacking
ITRS	International Technology Roadmap for Semiconductors
NEMI	National Electronics Manufacturing Initiative
Gbps	Giga bits per second

SUMMARY

The fundamental motivation for this dissertation is to address the widening interconnect gap between integrated circuit (IC) demands and package substrates specifically for high frequency digital-RF systems applications. Moore's law for CMOS ICs predicts that transistor density on ICs will double approximately every 18 months. Packaging of ICs at the 32nm and 22nm nodes in the next few years will require 20 μ m (peripheral) and 80 μ m (area array) I/O pad pitch on the IC, which must be matched by flip-chip interconnection and substrate wiring pad pitch of the same 20-80 μ m dimension. System on a Package (SOP) technology pioneered by Georgia Tech PRC enables future "mega-function" electronic and bio-electronic systems through ultra-thin film component integration from the current 50/cm² to over 10000/cm². This puts added wiring density and performance demands on the substrate. The other driving force in this thesis research is the increasing adoption of high frequency wireless and wired communication pushing the need for package substrate materials that are stable into multiple GHz frequencies.

The current state-of-the-art in IC package substrates is at 20 μ m lines/spaces and 50-60 μ m microvia diameter using epoxy dielectrics with loss tangent above 0.01. The research targets are to overcome the barriers of current technologies and demonstrate a set of advanced materials and process technologies capable of 5-10 μ m lines and spaces, and 10-30 μ m diameter microvias in a multilayer 3-D wiring substrate using 10-25 μ m thin film dielectrics with loss tangent in the <0.005. The research elements are organized as follows with a clear focus on understanding and characterization of fundamental materials structure-processing-property relationships and interfaces to achieve the next generation targets.

1. Low CTE Core Substrate: Advanced low CTE and high modulus core substrates, consisting of composite materials, and processing challenges and solutions.
2. Low Loss Dielectrics with 25 μ m and smaller microvias: Advanced low loss, thin film polymers - liquid crystal polymer (LCP) and benzocyclobutene (BCB) and comparison to epoxies, with emphasis on polymer chemistry, effect of chemical processing on microstructure and properties, and exploration and demonstration of advanced processes for planarization, photolithographic via formation, and excimer/UV laser via ablation. Fundamental understanding of the laser-polymer interactions will be used to explain the experimental results from excimer laser photo-chemical ablation processes.
4. Sub-10 μ m Width Cu Conductors: Chemical and plasma surface modification to achieve sub- μ m polymer-to-Cu interfaces and correlation of surface characteristics to ultra-fine (<10 μ m) copper conductor formation processes, photolithography and semi-additive plating process demonstration of sub-10 μ m lines and spaces. Novel non-etch silane based surface treatment processes for Cu traces to enhance the bond strength of polymer – to – Cu interfaces.

The dissertation will conclude with research on integration of the various dielectric and conductor processes to demonstrate the 20-80 μ m pitch wiring in a low-cost, large area substrate platform.

CHAPTER 1

INTRODUCTION AND OBJECTIVES

1.1 Thesis Motivation: Bridge The Widening Interconnect Gap Between IC And Package Substrate

The fundamental motivation for this dissertation is to address the widening interconnect gap between integrated circuit (IC) demands and package substrate solutions while maintaining high performance. Moore's law for CMOS ICs predicts that transistor density on ICs will double approximately every 18 months. Based on this miniaturization curve, the International Technology Roadmap for Semiconductors (ITRS)¹ predicted the need for interconnecting ICs to systems at an I/O interconnect pitch of 200 μm in the year 2000 (for 250nm node) and 130 μm in 2005 (for 130nm node). However, due to limitations in package substrate wiring density, state-of-the-art solutions could only meet 225 μm I/O pitch flip-chip interconnects in 2000. By 2005, this gap of 25 μm between IC pad pitch and substrate pad pitch had increased to 50 μm based on leading edge substrate pad pitch capability of 180 μm . As shown in Figure 1-1, this IC-to-package interconnect gap is expected to increase further since ICs are following Moore's law and 45nm gate technology will migrate to 32nm and 22nm by 2010. Such transistor nodes will require 20-50 μm I/O pad pitch on the IC, which must be matched by flip-chip interconnection and substrate wiring pad pitch of the same 20-50 μm dimension. The wiring pitch on the substrate is determined by three important parameters, (i) line width and space, (ii) microvia diameter, and (iii) microvia capture and landing pad diameter. Substrate wiring pitch of 20-50 μm requires multiple layers of materials and high precision processes for

sub-10um lines/spaces and sub-25um diameter microvias. The National Electronics Manufacturing Initiative (iNEMI) roadmap also defines the need for 4-8 layers of 5-10um wiring for future system boards². However, current state-of-the-art microvia substrates are at 20um lines/spaces and 60-75um microvias. Higher levels of on-chip integration continue to increase the IC size and large System on Chip (SoC) ICs can be up to 20mm x 20mm with more than 5,000 I/Os at 50um pitch. This imposes stringent specifications on the flatness of the substrate (5-10um per inch) for flip chip assembly and reliability. Ultra fine pitch interconnects result in very low stand-off heights between the IC and substrate and poses severe challenges for underfill processing. Current package substrates fabricated using bis-maleamine triazide (BT) laminates with thermal coefficient of expansion (CTE) of 16-18ppm/°C and low modulus (15-20 GPa) need to be replaced by a new generation of low CTE and high modulus core substrates. High stiffness and low CTE lead to improved dimensional stability and less warpage, resulting in tighter layer to layer registration, important for smaller via pad diameters. Low CTE cores are needed for fine pitch flip chip interconnect reliability to reduce the expansion mismatch between IC and substrate. High modulus in the core substrate is especially critical in light of the drive towards thinner core substrates to reduce overall package height for mobile products.

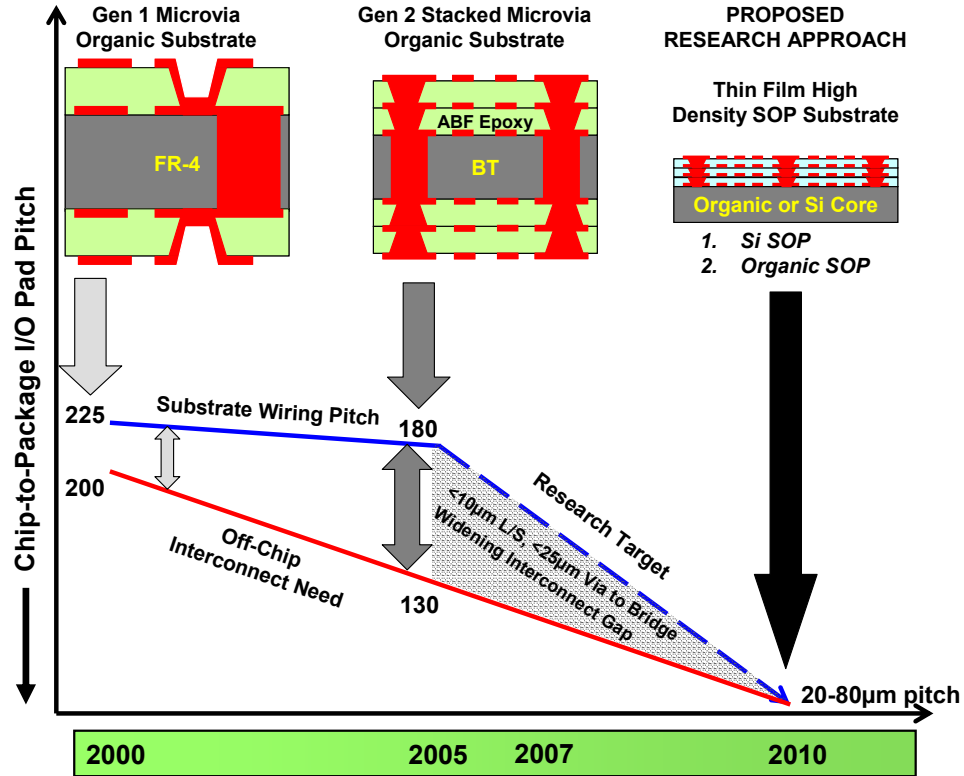


Figure 1.1 Bridging the Widening Interconnect Gap Through Ultra-High Density Substrate Wiring Research

Electrical Drivers for High Density Substrates: As on-chip clock speeds continue to increase, interconnect signal speed between the transistors need to keep up with the switching speed of transistors. On the contrary, it is widely recognized that interconnects have in fact become the bottleneck to semiconductor and system performance rather than the switching speed limitation of transistors. The ITRS roadmap translates IC performance to signal transmission speed required through the package substrate. Signal data rates of 5-10Gbps in the substrate drives the need for dielectric materials with loss tangent ~ 0.001 . Signal delay in global interconnects on ICs will dominate gate delay, and 5-10μm line/space in the substrate provides opportunity to off-load the longest global

wires from IC to substrate. Multi-core processor architectures, driven by the need to reduce power levels, increase the demand for signal I/O density and data bandwidth.

Table 1.1 Microprocessor Performance Parameters for 2004 and 2010 from ITRS
Roadmap

ITRS 2003:	2004	2010
Technology generation	90nm	45nm
Chip Frequency (local clock)	4GHz	15GHz
Number of package pins	500-1,600	780-2,782
Chip-Board I/O (narrow)	2.5Gb/s	9.5Gb/s
Chip size at production	140mm ²	140mm ²
Power (cost-performance)	84W	120W
Vdd(high)	1.2V	1.0V

Table 1.1 lists some of the attributes of microprocessors in 2004 and 2010 according to the ITRS roadmap. The signal data rate in the package substrate is expected to increase from 1-2 Gbps to about 10 Gbps per channel. At the same time, the voltage level is expected to decrease to 1V. These electrical needs translate to dielectric materials with low dielectric constant (<3.0) for higher signal speed in the substrate, and low loss tangent (<0.001) to minimize signal loss and maintain high signal-to-noise ratio at lower Vdd levels. Current state-of-the-art package substrates cannot match the performance of ICs primarily due to lossy epoxy based dielectrics that have been predominantly used for package substrates. The wiring gap described above must be bridged without any degradation in substrate electrical performance.

Added Wiring Demand from System on a Package (SOP) Technology: The research in this dissertation is a part of System-on-a-Package (SOP)³ technology that targets full system integration by embedded thin film components in a single multi-function, micro-miniaturized package or module. In the SOP concept, the “package is the system” and not

the bulky board. While systems of the past consisted of bulky boxes housing hundreds of components that perform one task such as computing or communications, the SOP concept consists of system functions to include computing, communication, consumer and other functions — all of these functions in a small system package no greater than the size of a Pentium processor package (35 mm in size). The SOP concept makes this possible by ultra-thin film integration of components in the substrate. A typical SOP package has a size of approximately 35 x 35 mm, with about four ICs for analog, digital and optical functions. Similar to a wafer-to-IC concept, the SOP packages will be fabricated on 600 x 600mm panels using low-cost processes used in high-density organic packages, and then diced — leading to tremendous size and cost reduction, functionality, performance and reliability.

The integration of multiple organic and inorganic materials for multiple functions into a high density substrate forms the core of SOP miniaturization. Embedding thin film passive and active components in the SOP substrate drives additional demand for substrate wiring density and performance as explained below.

- Embedded passive and active components in the substrate that used to compete for real estate on the package surface now compete for space with wiring inside the substrate.
- Interconnection of the embedded passive and active components buried inside the substrate requires additional wiring.

- Embedding and miniaturization of passives and actives brings them in close proximity, sometimes on the same substrate layer, and improved isolation between components by use of ultra-low loss dielectrics.

This research addresses to close the above wiring gap by:

- Low CTE Core Substrate for Minimizing Warpage During High Density Wiring Build-up and Flip Chip Reliability
- Low loss dielectric materials for high speed signal performance
- Thin Dielectric (10-25um thick) materials and microvia processes for 10-20um diameter
- Ultra-fine line and space conductor processes (5-10 μ m line/space) and multilayer high wiring density structures

As seen in Figure 1.1, these high density multilayer wiring structures can be integrated on dimensionally stable, flat and smooth organic or silicon based SOP substrates.

1.2 Research Objectives Driven By Wiring Gap

The primary objective of this research is to close the wiring gap through innovative new materials, processes and microstructures for ultra-fine line conductors and stacked ultra-small microvia interconnects. The specific objectives include:

1. Selection and exploration of new substrate core and dielectric materials consistent with the thermo-mechanical and electrical property requirements.
2. Fundamental understanding of materials, processes, interfaces and microstructures for future ultra-high density package substrates.

3. Research new low cost processes beyond current state-of-the-art to achieve 5-10 μ m conductor geometries and 10-20 μ m microvias.
4. Exploration of new process integration methods to demonstrate wiring pitch of 20-80 μ m in a large area organic substrate platform

The focus of this thesis research is to address each of the technical barriers related to new materials, substrate processes and structures by developing a fundamental understanding of the materials interactions including interface mechanical and chemical bonding, and novel process methods to achieve the target signal data rate and wiring density in the substrate.

1.3 Historical Development & Current State Of The Art Ultra High Density Wiring Substrates

The historical evolution of package substrates, as shown in Figure 1.2, started with big and bulky, low density boards with discrete passive components and packaged ICs in the 1970s and 1980s. The introduction of microvia build-up substrates in the early 1990s led to the concept of high density interposer package substrates to bridge the gap between sub-micron IC interconnects and milli-scale PWB interconnects. System in Package (SiP) technologies developed in the late 1990s further miniaturized IC packages through integration of small discrete passives (0201 and 01005) along with 3D stacked ICs into small form factor package substrates and package on package (POP) stacking. However, to fully leverage the scaling, integration and miniaturization advances of semiconductor technology, significant challenges remain in interconnect and wiring density enhancement and integration of passive and active components at the package substrate level. System-On-Package (SOP) technology pioneered by GT-PRC in the early

1990s aims to achieve miniaturization with ultra-high functional density by concentrating on the package as a whole rather than aim for miniaturization at the IC level alone.

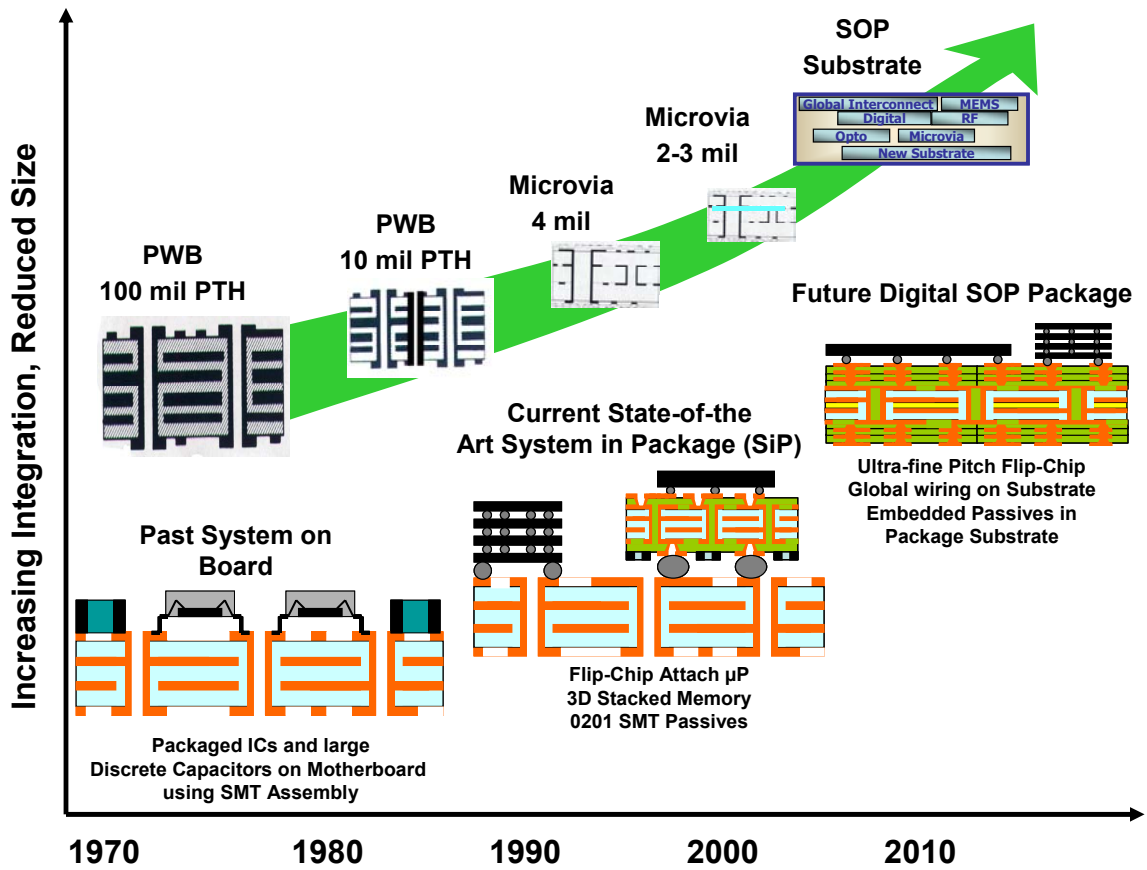


Figure 1.2 Component Integration Trends and Package Substrate Wiring Density Increase

Ultra-thin film wiring technology have been developed around the world on three primary platforms, namely, (i) thin film on ceramic substrates; (ii) sequential build-up organic substrates; and (ii) silicon redistribution and wafer level package processes. This section provides a summary of historical developments and current state-of-the-art technology for ultra-thin film multilayer wiring for SOP substrates. Figure 1.3 illustrates key historical milestones in these three platform technologies.

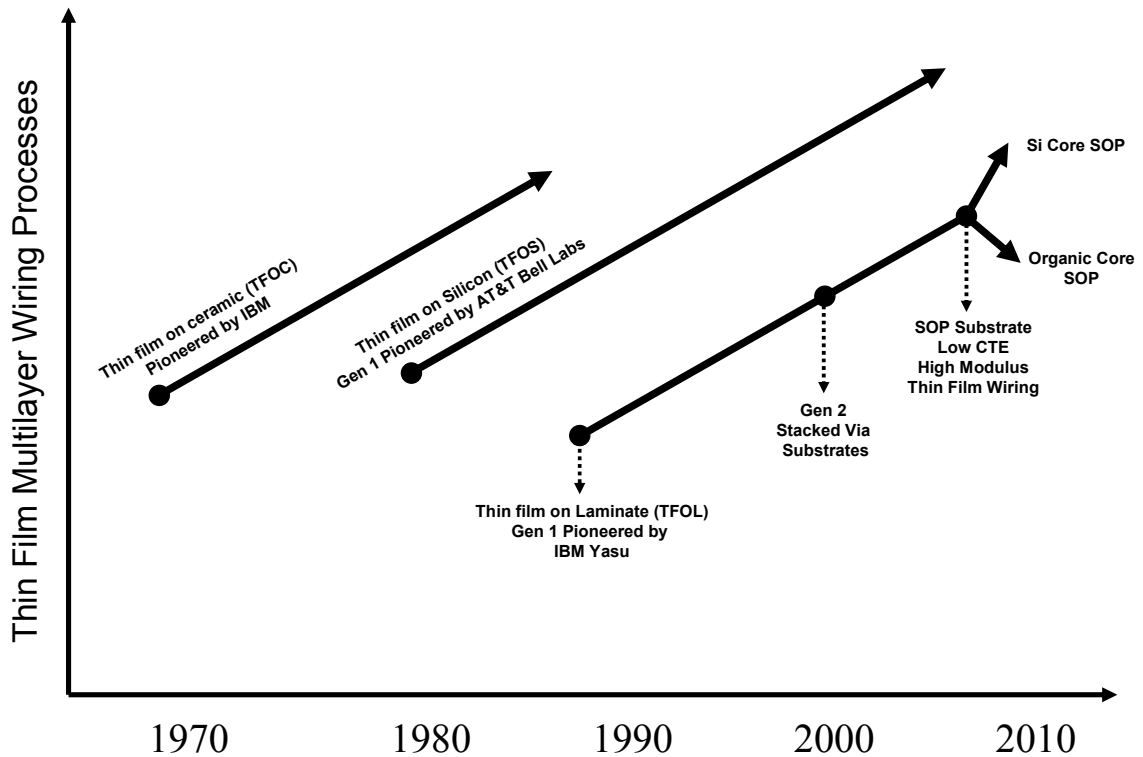


Figure 1.3 Key Milestones in the Evolution of High Density Substrates

The advent of thin film high density wiring, driven by the wiring demands of multi-chip modules (MCM), started in the 1970s with Cu-polyimide multilayer processing on low temperature co-fired ceramic (LTCC) substrates by IBM (MCM-C)⁴. A similar approach using spin-on polyimide dielectric was developed by Bell Labs on Silicon carrier substrates a few years later (MCM-D)⁵. Both of these substrate technologies were derived from semiconductor processing and utilized high cost processes such as chemical mechanical polishing (CMP) and sputter deposited metal seed layers. In the early 1990s, IBM Yasu in Japan adopted thin film build-up wiring on low cost FR-4 organic substrate cores using low cost epoxy dielectric materials and large area processes like electroless copper plated seed layers and photo-defined microvias (MCM-L). This technology, Surface Laminate Circuitry (SLC)⁶ is widely considered as the

pioneering high density build-up organic substrate solution that enabled the widespread use of flip-chip for mainstream IC packaging. In the late 90s and early 2000s, the density of microvia organic substrates was further enhanced by advancements in fine line conductor processes and filled/stacked microvias developed by many groups worldwide.

1.3.1 Thin Film on Ceramic (TFOC) Technology

Multilayer thin film wiring using polyimide-Cu was developed extensively by IBM in the 1970s and 80s on a variety of ceramic substrates for use in multi-chip module (MCM) packaging for high performance computing systems. The thin redistribution layers were developed on top of ceramic substrates including alumina, low temperature co-fired alumina (LTCC) and high temperature co-fired glass-ceramic (HTCC) materials in panel sizes from 125mm up to 150mm. Both conformal via and stacked via structures (process flow shown in Figure 1.4) were fabricated using spin-on liquid polyimide dielectric films from 5-12 μ m thickness per layer.

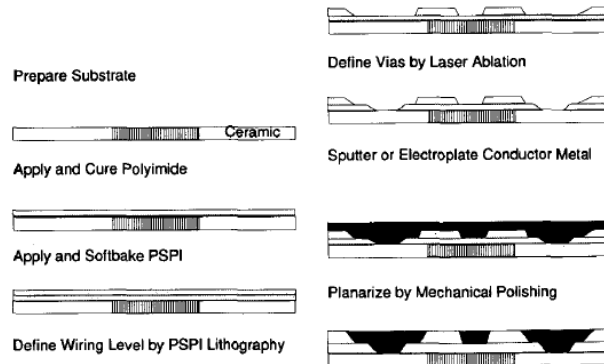


Figure 1.4 Dual Level Metal (DLM) Stacked Via Process for Cu-Polyimide on Ceramic Substrate by IBM⁴

One to four metal layers have been demonstrated in high volume production processes with minimum line widths of 10-25 μm and line pitch of $>50\mu\text{m}$. Photosensitive polyimide and laser ablation processes were used to define 1:1 aspect ratio vias to interconnect the metal levels. Cr-Cu seed layers were deposited on the cured polyimide using sputter deposition and additive electroplating or subtractive etching was used to pattern the metal circuits.

The primary limitations of thin film on ceramic substrate technology are the expensive processes and small panel sizes used, leading to high cost of the individual packages. For example, only two to four individual packages could be laid out on one ceramic panel of 50mm or 125mm, compared to the SOP targets of hundreds if not thousands of package substrates on one large manufacturing panel of 450mm or 600mm size. Also, the thin metal traces (1-3 μm thick) resulted in high conductor loss affecting high frequency performance for longer wires, which had to be routed through low density layers in the co-fired ceramic substrate core. Additional concerns are the high cure temperature of polyimide (350°C) and high diffusion rate of Cu into polyimide requiring barrier metal layers.

1.3.2 Thin Film on Silicon (TFOS) Technology

Thin film multilayer wiring on silicon wafers was first developed by AT&T Bell Labs in the 1980s with polyimide dielectric and thin film copper metallization, a process known as Polymer Hybrid Integrated Circuit (PolyHIC)⁷. This process initially used thin copper metallization on triazide polymer dielectrics on alumina substrates, and was later adapted to Cu-polyimide layers on Silicon wafers. Power and ground plane wiring levels

were integrated with higher density signal routing layers and dry etching processes defined the microvia interconnects (Figure 1.5)

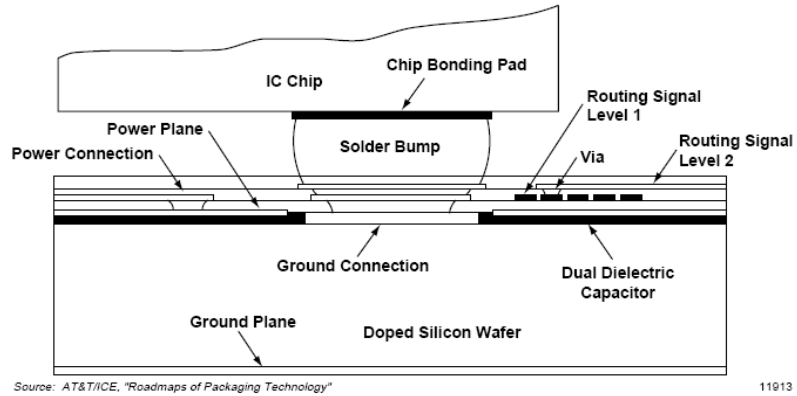


Figure 1.5 Cross-section schematic of thin film on silicon (TFOS) substrate technology by AT&T Bell Labs

The silicon substrates with thin film wiring was used to attach multiple ICs using eutectic solder bumps and external I/O connections were made using pin grid arrays. Figure 1.6 illustrates the top view and cross-section of the completely packaged MCM-D module with TFOS substrate.

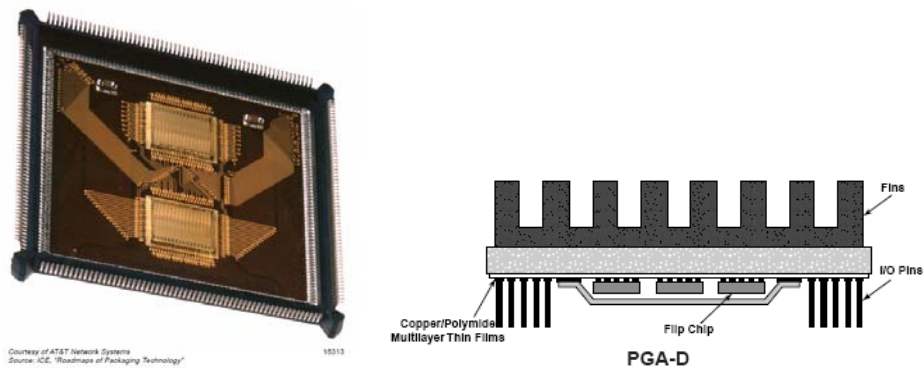


Figure 1.6. Top View and Cross-Section of Fully Packaged Multi Chip Module using Cu-Polyimide TFOS Substrate

Cu-polyimide thin film wiring was then applied to embedded chip in substrate technology pioneered by GE in the late 1980s and early 1990s as HDI or Chips-First build-up substrates. This concept is shown in Figure 1.7, and since then, several groups around the world have developed high density wiring technology on silicon substrates, by utilizing spin-on thin film polyimide or BCB dielectrics and back end of the line (BEOL) processes commonly used in wafer foundries⁸. Via interconnections were formed by photolithography or reactive ion etching (RIE) processes and sputter deposited metallization schemes were implemented in combination with lift-off processing or chemical mechanical polishing (CMP).

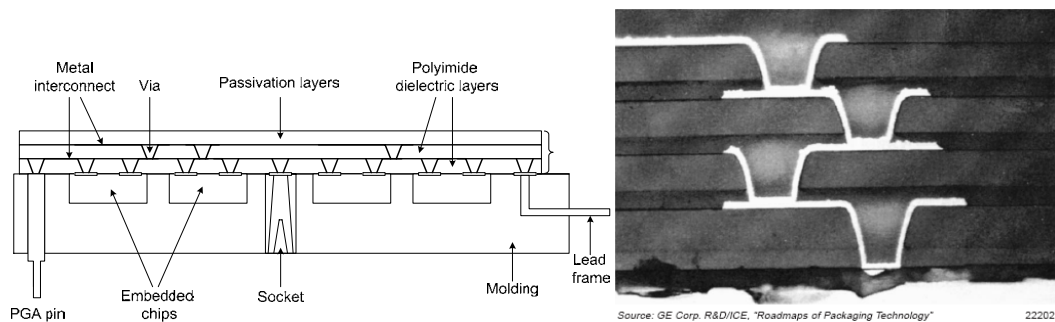


Figure 1.7 GE Chips-First HDI Substrate Technology with Cu-polyimide thin film multilayer wiring

Recent examples of silicon carrier for build-up wiring layers include PASSI technology by Philips/NXP, Redistributed Chip Package (RCP) by Freescale Semiconductor, and bumpless build-up layer (BBUL) by Intel. Similar high density package wiring have also been implemented on glass substrates, so called thin film on glass (TFOG), by ST Microelectronics. BCB-Cu multilayer wiring has also been fabricated on GaAs semiconductor wafers for high performance routing and embedded passives.

The common elements to the above silicon/glass based substrates are semiconductor-like processes such as Deep Reactive Ion Etching (DRIE) for dielectric patterning, chemical mechanical polishing (CMP) for planarization and vacuum metallization for conductors. These substrate techniques are limited by their high cost process methods, thin metallization layers (1-3 μm) affecting signal loss and lossy substrates in case of Si and other semiconducting materials that contribute to further signal degradation, especially when through vias in the core substrate are needed.

1.3.3 Sequential Build-up (SBU) Organic Substrates

The historical evolution of microvia technology on organic substrates is shown in Figure 1.8⁹. Microvia technologies, also called build-up substrates or boards were pioneered at IBM Japan in 1987 to replace ceramic substrates for area array flip-chip assembly of ICs. There are two main classes of organic microvia technologies, thin film and thick film. The first group is based on thin film technology combined with conventional PWB-cores with through hole plating such as SLC by Japan IBM⁶, IBSS/AAP10 by Ividen¹⁰, DYCOstrate by Dyconex¹¹, VIL by Japan Victor¹², CLLAVIS by CMK¹³ and others. These technologies are further classified by microvia formation processes as follows. SLC and IBSS/AAP10 are photo-via processes. DYCOstrate is by plasma via process and VIL and CLLAVIS are laser via processes. The second group is based on thick film technology combined with conventional through hole plating. These are ALIVH by Matsushita¹⁴ and B²ITTM by Toshiba/DTCT/DNP¹⁵. The ALIVH microvias are formed by laser drilling and subsequent filling with Cu thick film paste and the B²ITTM is formed by piercing prepreg by Ag filled thick film paste.

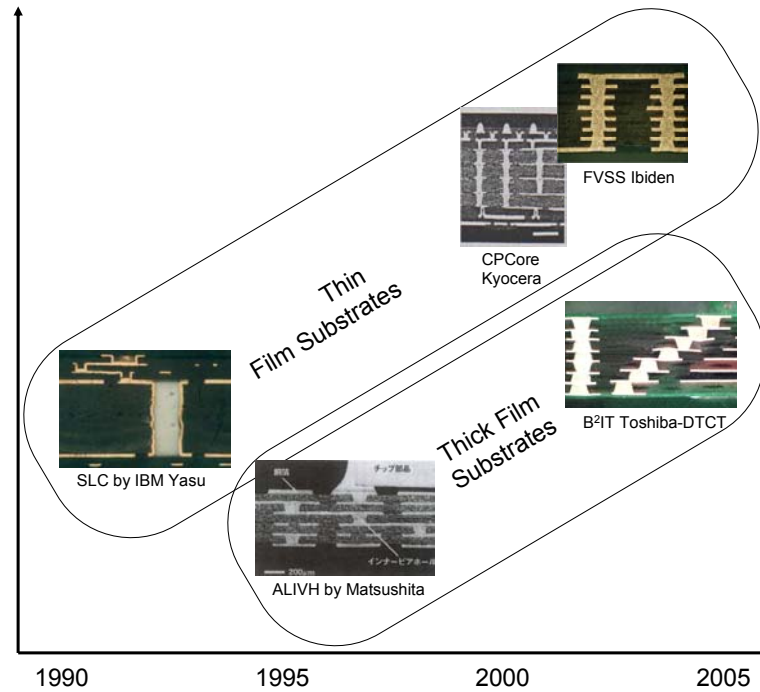


Figure 1.8 Thick and Thin Film Organic Substrate Microvia Technologies Worldwide

In order to meet lower cost and shorter-turn around time requirements, co-lamination technologies such as SSP-Multi and Full Via Stacked Structure (FVSS) by Ibsiden¹⁶, Parallel Lay-up (PALAP) by Denso¹⁷, CPCore by Kyocera¹⁸ and Core Printing Method of B²ITTM by DTCT¹⁵ have been developed since 1999. These technologies are called parallel build-up technologies because each layer is separately built and then laminated in one vacuum co-lamination press process using advanced manufacturing processes. To further extend the wiring density of these parallel build-up substrates, ultra high density multi-layer wiring using ultra small microvias has been developed using thin film technologies. Therefore, second generation build-up substrates are based on a combination of thin and thick film technologies, and are being developed by DNP/DTCT, Shinko and Kyocera in Japan and AMITEC¹⁹ in Israel. The progress in wiring density

enhancement in organic substrates has not kept pace with the wiring demand of ICs driven by Moore's law. The state of the art organic substrates have 20-30 μm lines/spaces and 50-75 μm microvia diameters. Additionally, the high expansion coefficient and low stiffness of BT and FR-4 laminates limits the size reduction of microvia pads due to poor layer to layer registration, and fine pitch flip-chip reliability concerns persist. Leading edge epoxy build-up dielectrics with film thickness of 35-40 μm and high moisture absorption are not conducive for high wiring density and high electrical performance. The latest organic substrates have wiring pitch of 150-180 μm compared to the IC pad pitch of 80-100 μm today reducing to 20-50 μm in the next five years.

1.4 Technical Barriers To Address The Wiring Gap

The objectives listed above and state-of-the-art review bring about a set of unique technical barriers and gaps in technology that must be overcome to meet the needs for SOP packages in the next 3-10 years. From a materials and process perspective, the critical barriers and technology gaps based on current state-of-the-art are as follows:

1. FR-4, BT and other laminate core substrates used in current package substrates limit flip chip interconnect down scaling due to their high CTE mismatch with silicon (18ppm/ $^{\circ}\text{C}$ vs. 3ppm/ $^{\circ}\text{C}$) and low elastic modulus (15-20GPa) resulting in excess warpage.
2. Current lossy (0.01-0.03) epoxies are limited in performance to 1-3 GHz and high cost thin film processes are a major barrier for available ultra-low loss (0.001) dielectrics.

3. Current dry film dielectrics limited to 30-50 μm thickness and a new set of dielectric materials and process integration is needed to achieve 10-25 μm thickness target.
4. Semi-additive and subtractive etch processes used today are limited to 20-50 μm lines/spaces. New processes for 5-10 μm lines and spaces are in all major roadmaps but no solutions exist or have been identified.
5. Current CO₂ and UV laser processes are limited to 25-100 μm via diameters and these “sequential” drilling processes not suited for very high via density (>10000 / cm²) and 10-20 μm microvia diameters.
6. Chemical surface treatment processes used for today’s epoxy dielectrics depend on mechanical locking and surface roughness of 1-3 μm for metal-polymer adhesion. Rough interfaces lead to high signal loss.
7. Chemical etching processes used for bond enhancement of copper conductors are not compatible with sub-10 μm lines due to excess copper etching resulting in damage to fine lines. A new set of non-etch processes are needed to treat ultra-fine copper conductors for multilayer adhesion and reliability.

1.5 Research Outline To Address Barriers

This research focuses on the fundamental microstructures and properties, novel process innovations and multilayer substrate integration necessary to address the barriers detailed above for three major materials — (i) low CTE and high modulus core substrate, (ii) ultra-low loss and low-stress thin film dielectrics, and (iii) ultra-fine line conductors; both for high speed, high density and high reliability wiring. These innovations are also

integrated into multilayer thin film build-up wiring with minimum via capture pads, on top of core substrates with ultra-high modulus and close to silicon CTE for improved solder joint reliability.

The key elements of the research are illustrated in Figure 1.9 in a cross-section schematic of the proposed ultra high density SOP substrate.

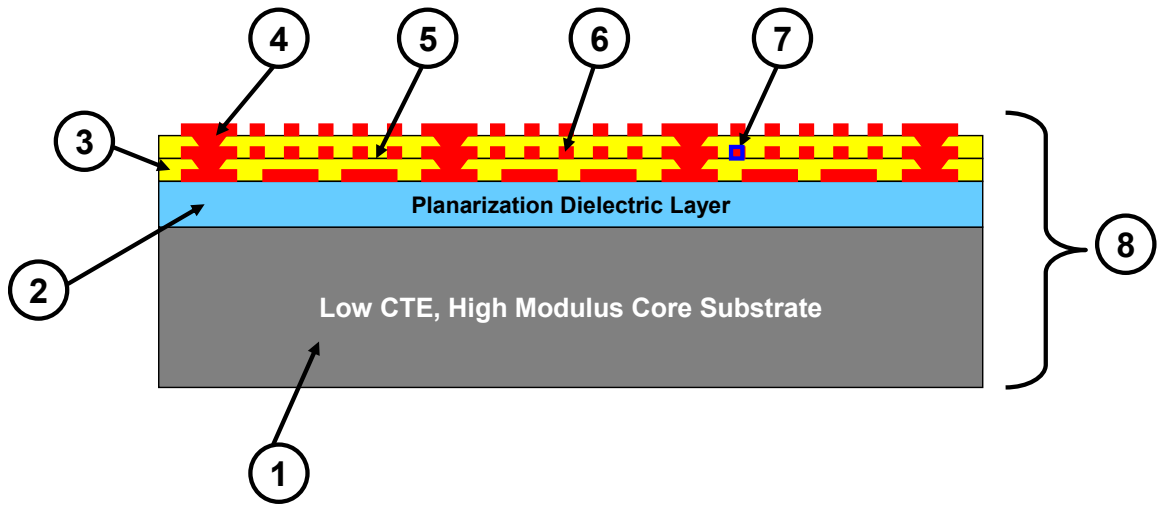


Figure 1.9 Eight Major Research Elements in the Proposed SOP Substrate
Research

Referring to Figure 1.9, the research elements are organized in the following chapters as follows. Chapter 2 presents materials, microstructure, processing and properties of core substrate. Low CTE and high modulus core substrates to replace FR-4 and BT. Metal (Cu-Invar-Cu), composite (SiC matrix) and new laminate (aramid reinforced) core materials and their processing are described.

Chapter 3 presents a background on current lossy and new low loss polymer dielectrics, including low loss and thin film polymer dielectric chemistry, and the effect

of chemical processing on microstructure and properties of epoxy, liquid crystal polymer (LCP) and benzocyclobutene (BCB) including thin film planarization processes.

Chapter 4 focuses on photovia, UV and excimer laser via ablation processes in BCB and LCP dielectrics for 10-30 μm diameter vias and fundamental analysis to overcome ablation process challenges. Via metallization results are also presented and discussed.

Chapter 5 presents the research addressing sub-10 μm conductor lines. It begins with surface treatment of dielectrics through plasma and chemical treatment processes to achieve sub- μm roughness including effect of polymer chemistry and surface analysis results. Following this are results and discussion of photolithography and semi-additive plating processes including effect of dielectric surface microstructures for copper conductor fine lines. The chapter ends with novel non-etch surface treatment processes for Cu traces to enhance the bond strength of polymer – to – Cu interfaces.

Chapter 6 presents the research into integration of the various dielectric and conductor processes to demonstrate high density SOP substrates to bridge the wiring gap and achieve 20-80 μm pitch wiring in a low-cost, large area substrate platform.

Table 1.2 shows the current state-of-the-art parameters and advanced research focus in this thesis.

Table 1.2 Comparison of State-of-the-art and Proposed Research Parameters

Parameter	Current State-of-the-art Package Substrate	Proposed Research
Core Substrate with low CTE and high modulus	CTE: 16-18ppm/°C Modulus: 20-30 GPa	CTE: 3-10ppm/°C Modulus: 100-200 GPa
Low Loss and Thin Film Dielectric	Epoxy Loss tangent: 0.01-0.02 Film Thickness per layer: 30-50µm	BCB or other thin film Loss tangent: 0.001-0.005 Film Thickness per layer: 10-25µm
IC & Substrate Wiring Pitch	150-180µm	20-80µm
Fine Lines and Spaces	20µm (Subtractive Etching)	5-10µm (Additive Plating)
Microvia Diameter	35-50µm (UV laser), 50-100µm (CO ₂ laser)	10-30µm (Excimer Laser)
Copper-Dielectric Interfaces	Chemical Treatment (1-3µm Ra) Microetch for Cu Roughening	Plasma Surface Modification (< 1µm Ra) Non-Etch Cu Treatment

CHAPTER 2

LOW CTE CORE SUBSTRATES

High density substrates require a stable and high modulus core substrate on which to build multiple layers of thin film dielectric and conductor wiring. The core must have dimensional stability of <10 microns per inch in order to achieve the required layer to layer alignment of build-up dielectric layers. The build-up dielectric films must also have low thermal coefficient of expansion (CTE) in order to match the low CTE core substrate and prevent additional warpage and dimensional change during multilayer processing. Thin polymer films with low processing temperature are important for ultra-small microvias and low process cost. Low loss tangent and low dielectric constant are also critical for the dielectric material for signal integrity. This chapter is organized into two major sections, (a) new low CTE, high modulus core substrate materials and processes, and (b) results and analysis from processes and microstructures for low loss thin film polymer dielectrics.

2.1. Property Requirements and Selection of Core Substrates

The main properties considered during the selection of core materials for ultra-high density SOP substrates include:

- Low to medium coefficient of thermal expansion (CTE) in the range of 3-10 ppm/°C matching Silicon CTE of 3ppm/°C for improved IC-to-substrate flip-chip interconnect reliability
- High elastic modulus (100-400 GPa) for minimum warpage during thin film build-up processing and flat substrates for ultra-fine pitch (20-80 μ m) flip-chip assembly

- Excellent dimensional stability with less than 10 μm /inch change in dimension across the 300mm panel during thermal excursions from room temperature to dielectric cure temperature (180-250 $^{\circ}\text{C}$) and back.
- High temperature stability to withstand dielectric processing and interconnect assembly processes up to 260 $^{\circ}\text{C}$
- Large area (300-600mm) and low-cost processing capabilities to allow for inexpensive and easy machinability for singulation into individual packages

The stringent need to process 10 or more layers of thin films, with via sizes of 10 μm and capture pads less than 50 μm , requires substrate materials with warpage in the few microns over 300-mm in size. As shown in Figure 2.1, via-to-pad misalignment of less than 10 μm requires warpage control to 5 to 10 μm /inch over 300 mm for 0.65-mm-thick substrates.

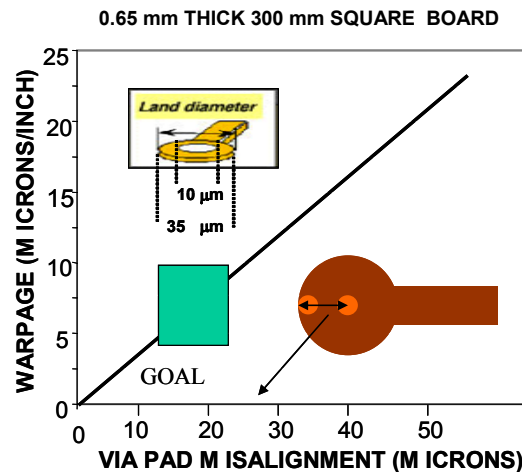


Figure 2.1. Correlation of Substrate Warpage and Via-Pad Misalignment

The warpage for a two layered structure consisting of a core and build-up film as given by Stoney's equation is:

$$\rho \propto E_s \Rightarrow \text{Warp} \propto \frac{1}{E_s}$$

where

ρ is the radius of curvature of the substrate

E_s is the elastic modulus of the substrate

It can be seen that a higher modulus results in a higher radius of curvature (and consequently lesser warpage). Figure 2.2 shows the relationship between substrate modulus and process-induced warpage for sequential buildup of 10 layers of 5 μm line/space wiring with 35 μm via pads. Based on thermomechanical modeling, the modulus required for the substrate is in excess of 400 GPa, represented by the acceptable warpage²⁰.

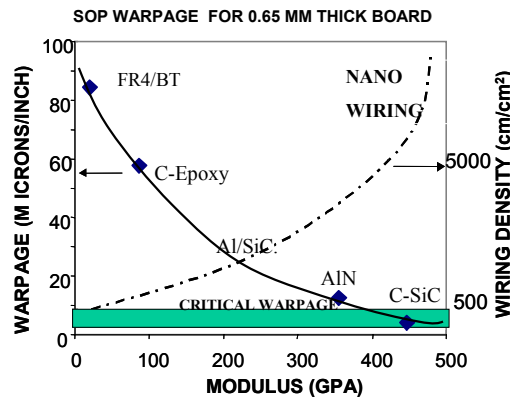


Figure 2.2. Thermo-mechanical Modeling of Substrate Warpage Based on Modulus & Thin Film Build-up Process

Current flip chip package solutions for 200- μm pitch area array use BT resin and high glass transition temperature (T_g) FR-4 laminates with a CTE of 18 ppm/ $^{\circ}\text{C}$. A silicon die has an approximate CTE of 2 to 3 ppm/ $^{\circ}\text{C}$, and thermomechanical stresses are induced in the package from the CTE mismatch between the die, the substrate and the buildup materials. These thermomechanical stresses result in solder joint failure, die

cracking, delamination of the solder bumps and cracking of the build-up layers - leading to failure of the assemblies^{21,22}.

2.2. Core Substrate Materials Studied in this Research

Based on the property requirements for the core substrate, several new materials were explored during this research and they are shown in chronological order in Figure 2.3.

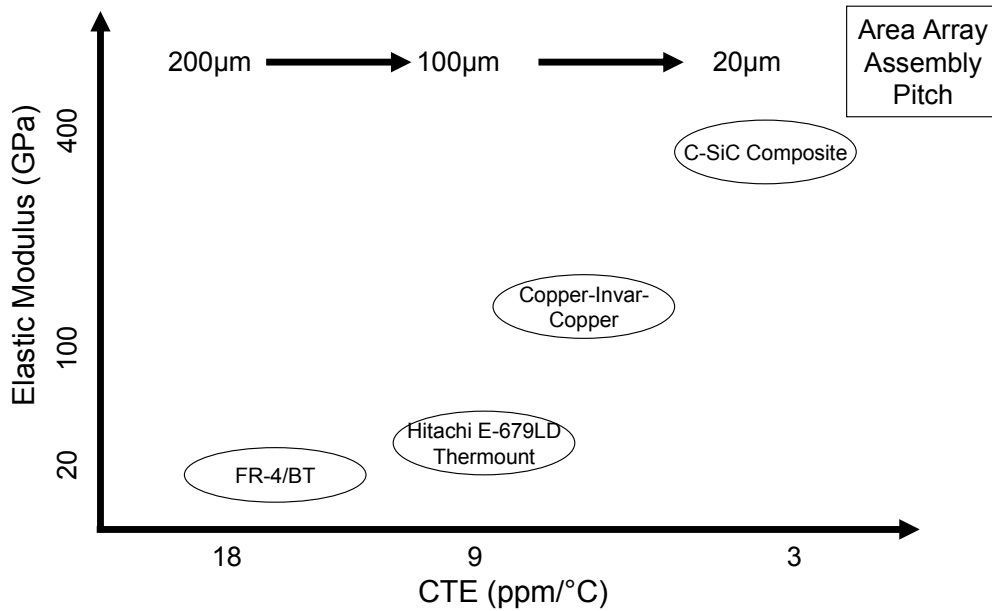


Figure 2.3 Thermo-mechanical Properties of Core Substrates Explored in this Research

Epoxy-based low CTE laminates from Hitachi Chemical have CTE of around 8-11 ppm/°C and modulus of 30 GPa²³. Laminates using thin Cu-invar-Cu cores (50-200µm thickness) and multilayer PTFE dielectric resulted in composite CTE of 6-8ppm/°C although they had low modulus (1-5 GPa)²⁴. The main focus of this research was on a novel Carbon fiber reinforced SiC composite substrate.

A manufacturing process (patented by Starfire Systems Inc., NY) has been demonstrated to yield large area, thin, carbon-silicon-carbide-based composite boards with the required stiffness and Si-matched CTE²⁵. Composite C-SiC cores with 2.5-

3ppm/°C CTE and 150-300GPa modulus was selected for further process development and integration. The C-SiC cores (Starboard™ C) have a CTE of 2.5ppm/°C to improve flip-chip reliability at 20-100µm pitch and modulus in excess of 200GPa to minimize warpage during single sided build-up processing. Alternate reinforcements in the SiC matrix have also been developed to tailor the substrate properties, such as low loss tangent using alumina (Starboard™ A - composite loss tangent of 0.03) and glass fibers (Starboard™ G - composite loss tangent <0.01). The key properties of the three SiC matrix composite substrates are shown in Table 2.1

Table 2.1 Comparison of Electrical and Mechanical Properties of SiC Composite Substrates with Carbon, Alumina and Glass Fiber Reinforcement

Substrate Properties			Material System		
Property	Level	Units	C	A	G
Glass Transition Temp.	DMA	°C	850	850	650
Flex Modulus	20 °C	GPa	300	115	35 – 55
	200 °C	GPa	300	115	35 – 55
CTE	20 °C	ppm/°C	2.5-3.5	4 - 5	3 – 4**
	240 °C	ppm/°C	2.5-3.5	4 - 5	3 – 4**
Relative Hardness	20 °C		300	200	150
	200 °C		300	200	150
Dielectric Constant	1.2GHz		-	7.55	3.9
Dissipation Factor	1.2GHz		-	.030	.001
Volume/surface resistivity		Ωcm	-	>10 ¹⁴	~10 ¹⁵

2.3. Results and Discussion - Source of Surface Defects and Roughness in C-SiC

Substrates

The unique chemical process used for fabricating the SiC matrix – Carbon fiber composite substrate is shown in Figure 2.4. This process has been used to demonstrate large area panels up to 300mm size, with scalability to 600mm square panels due to the molding process used for the fabrication.

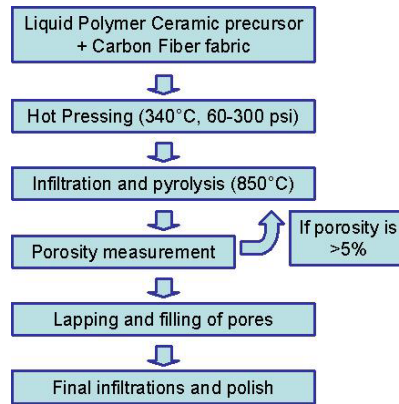


Figure 2.4 Fabrication Process for Carbon Fiber Reinforced SiC Composite Substrate

A schematic of the topography of C-SiC composite substrates is shown in Figure 2.5, which illustrates surface roughness, planarity and small and large porosity based surface defects that were encountered during processing. Contact profilometry (Veeco Dektak 30 profilometer) was used to characterize the surface topology and roughness of the C-SiC substrates. The pore dimensions were measured over a span of 10 mm. For simplicity, the roughness can be categorized into three ranges, (a) roughness of under $5\mu\text{m } R_z$, these are mainly from the roughness of the molding plate surface used and from carbon fiber bundles appearing close to the surface during grinding and polishing processes to achieve flat substrates; (b) small pits caused by surface and sub-surface porosity in the range of $5\text{-}15\mu\text{m}$ depth; and (c) large pits in the $20\text{-}30\mu\text{m}$ range with some as large as $60\mu\text{m}$ depth caused by the exposure of internal porosity related to knots in the carbon fiber fabric reinforcement.

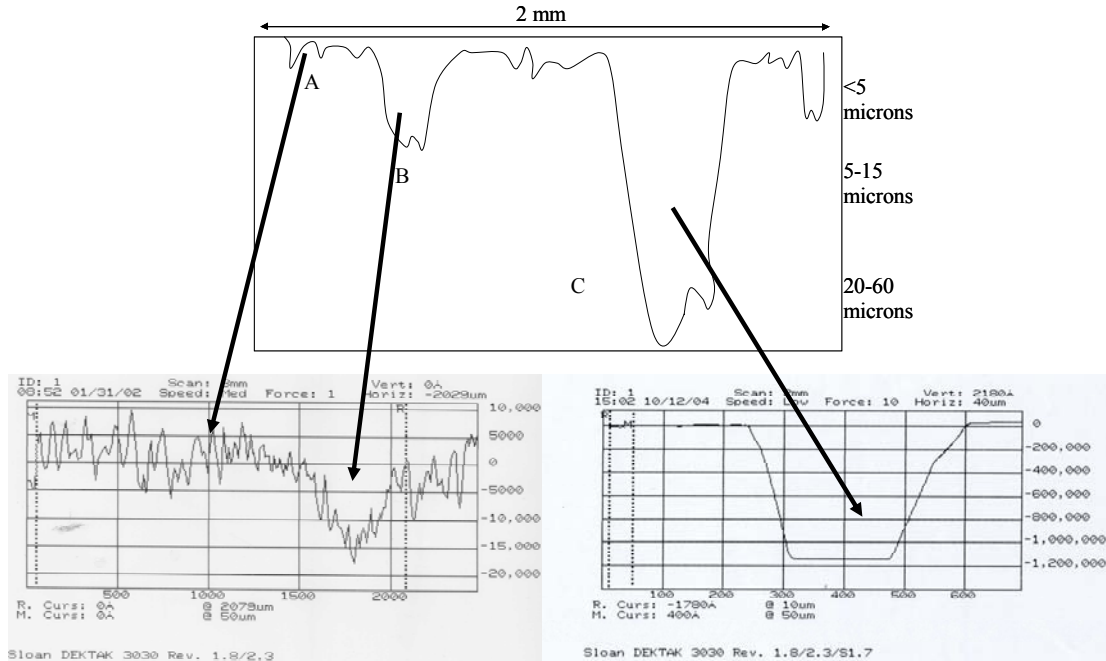


Figure 2.5: Schematic of the surface roughness. Typically, pores of three size ranges can be seen (around 3-5 microns, 5-15 microns and 20-60 microns).

Initially, 1mm and 2.5mm thick C-SiC substrates were obtained with minimum amount of the large pits. As the thickness of the substrate was reduced to 0.5mm, the incidence of large pits increased, and it was found to be related to the increasing volume percentage of carbon fiber reinforcement and knots in the carbon fiber fabric.

2.4 Results and Discussion - Surface Planarization for Ultra-Fine Line

Conductors

Due to the rough surface of the “as-fabricated” Starboard™ C carbon-SiC composite substrates, a planarization process was developed to achieve a smooth surface with a target smoothness below 1-2 μ m. The planarization layer also serves an electrical isolation function for build-up wiring layers since the C-SiC substrate is inherently partially conducting due to the conductive carbon fibers and semi-conducting SiC matrix. Several process options including direct liquid polymer coating, ceramic paint infiltration

and polishing, and polymer dry film lamination were explored. Three different phenomena were observed depending on the type of coatings used for planarization, namely, (a) conformal liquid coatings that did not planarize the rough surface of the substrate, (b) tented film lamination that resulted in planarization, but has concerns of out-gassing from trapped air in the pores, and (c) flow and fill planarization from high flow polymer films laminated on the surface.

Liquid Coating: Figure 2.6 illustrates the observed effect of liquid Benzocyclobutene (BCB) thin film coating (5-10 μ m layer thickness) on the rough surface of C-SiC substrates on the left, and a photograph of the processed substrate on the right. The BCB was deposited by spin coating followed by thermal curing in a nitrogen oven at 250°C for one hour. The liquid coating was not effective due to the conformal nature of the thin film coating, and also due to bubbles that formed on the medium and large pit locations due to out-gassing during polymer curing.

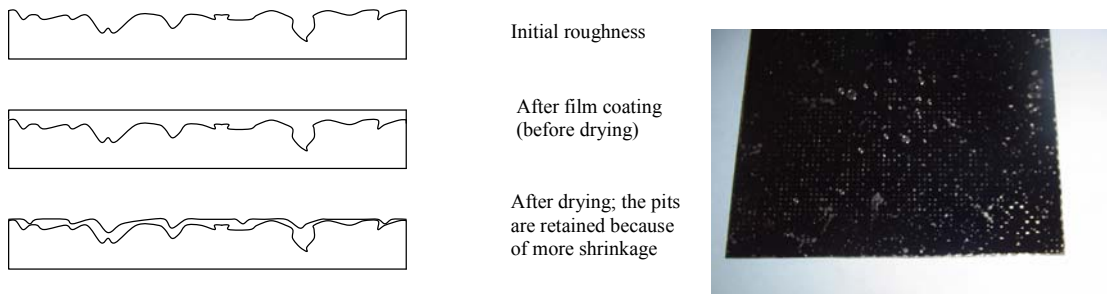


Figure 2.6 Effect of liquid coating process on the planarization of the C-SiC substrate (left) and photograph of coated and cured substrate showing surface defects (right)

Dry Film Lamination Process: Previous research has demonstrated that for reliable multilayer wiring, thin and low CTE polymer dielectrics (BCB, A-PPE) are compatible with C-SiC, whereas high CTE and thick epoxy films resulted in dielectric cracking and failures [Nitesh paper]. Low CTE polyimide (DuPont KaptonTM) and

Speedboard™ C prepreg (WL Gore) dielectric films were selected based on their compatibility with the low CTE C-SiC core substrates.

Planarization with polyimide: A new polyimide dielectric from DuPont Electronic Materials with low process temperatures of 200°C was deposited on the C-SiC substrate by hot pressing at 440°F temperature, and 400 psi pressure. This polyimide system is thermomechanically reliable because of its excellent properties such as high failure for elongation (15-30 %) and high-strength (200 MPa) inspite of its low stiffness. Figure 2.7 shows a microsection photograph of the laminated polyimide film on C-SiC core. As seen in the figure, the polyimide film “tented” over the large pits on the substrate surface. Even though a planarized surface was achieved for fine line fabrication, the trapped air in the pits is a potential source of out-gassing and failure during high temperature flip-chip assembly and reliability testing.

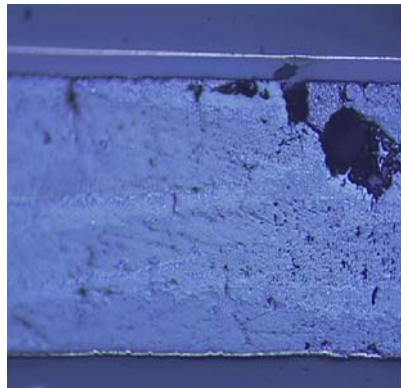


Figure 2.7 Tenting of poyimide film over large pits on the surface of C-SiC substrate

Planarization with Speedboard™ C Prepreg: Although epoxy and BT resins are brittle in un-supported film form, Speedboard™ materials are reinforced with a proprietary Teflon fabric reinforcement (courtesy of WL Gore) and the composite film has thermosetting and flow behavior of the BT resin matrix and good compliancy from

the ultra-low modulus Teflon fabric. Speedboard films with thickness in the 30-100 μm range were laminated in a vacuum hot press using 175-300 psi pressure and 175-200 $^{\circ}\text{C}$ cure temperature of the BT resin. This material had very high flow in the vertical direction causing good filling of the Type A (3-5 μm) and Type B (5-15 μm) surface roughness as illustrated by the planarization of surface carbon fiber bundles (Figure 2.8a). However, as seen in Figure 2.8b, the large pits could not be planarized completely due to insufficient resin volume, although the resin flowed and filled the pits. Lamination of very thick films can planarize the large pits, but thick films will introduce warpage from unbalanced stresses and also counter-act the thickness reduction critical to SOP substrates.

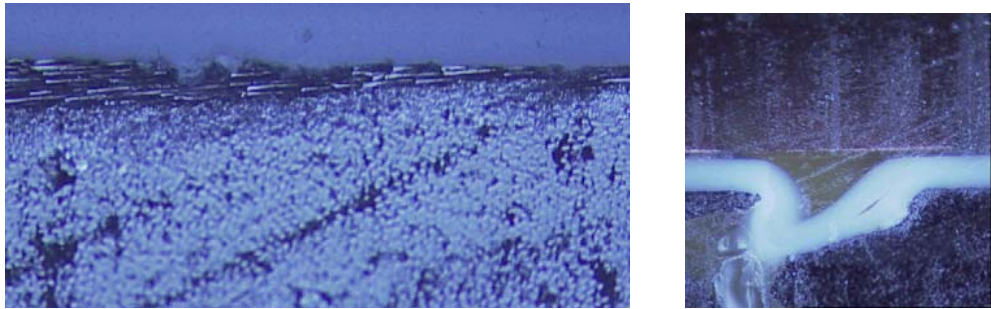


Figure 2.8 (a) Complete flow and fill planarization of Carbon fiber bundles on the surface of C-SiC substrates by Speedboard lamination; and (b) Incomplete planarization of large pits due to insufficient resin

A multiple infiltration and polish process using ceramic pre-cursors was used during the fabrication of the C-SiC substrates in order to minimize or eliminate the large pits (20-60 μm deep) from the “as-received” substrates. Once the large pits were eliminated, lamination based planarization was successfully applied using Speedboard C dry films of 38 μm and 100 μm thickness. Surface profiles of the substrate before and after planarization measured on a Veeco Dektak 30 system are shown in Figure 2.9. The

surface roughness of $1\mu\text{m}$ in the “after” scan is due to the roughness on the under side of copper foils used for the lamination. A cross-section of the planarized C-SiC substrate is shown in Figure 2.10 with $100\mu\text{m}$ thick Speedboard™ C on both sides. Complete planarization has also been achieved with one layer of $38\mu\text{m}$ thick Speedboard™ C prepreg and copper foil.

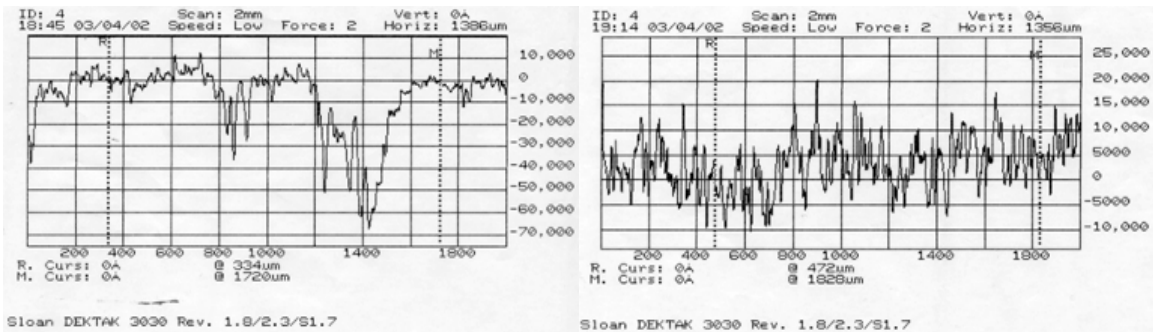


Figure 2.9: Surface Profiles of C-SiC Substrate “Before” and “After” Planarization

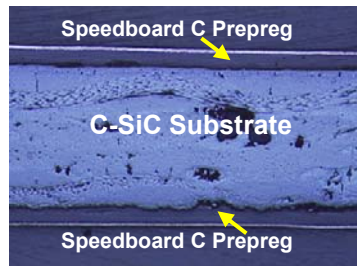


Figure 2.10: Cross-section of C-SiC Substrate Planarized with Speedboard C prepreg

CHAPTER 3

POLYMER DIELECTRICS BASICS & ADVANCED DEPOSITION PROCESSES

The polymer dielectrics in this chapter are meant to form insulating layers between multiple conducting layers on both sides of the low CTE core substrate presented above. This section describes a) the electrical, mechanical, thermal requirements for such dielectrics, (b) identifying emerging polymers that meet these requirements and (c) exploring and developing novel processes to form dielectric films to meet the above property needs. This is enabled, clearly, by a fundamental understanding of polymer chemistry-processing, microstructure development and property relationships, as well as interactions and interfaces with metallization.

3.1. Historical Trends in Polymer Dielectrics

The key build-up dielectric polymers used in this study are shown in chronological order in Figure 3.1 along with the evolution of dielectric materials during the last few decades. Initially, ceramic substrates with thick film technology were utilized resulting in bulky packages. They gave way to organic thin film technology in the 1980s which led to much better performance. Today, most high density packages use epoxy-based dry film dielectrics on low cost organic core substrates (e.g. FR4 epoxy fiberglass boards or BT resin laminates) [1]. Epoxies are thermosets which are widely used in substrates due to their excellent adhesion, good thermal stability, low processing temperature (<150°C), and low cost. However, epoxies also have high dielectric constants (3.5–5.0) and high water uptake (0.3-1.0 wt %).

The previously mentioned disadvantages of epoxy combined with their lossy nature, led to the development of a new class of advanced thermosetting polymers such as polyimide, BCB and polynorbornene. Around the same time PTFE (Teflon) also began to be used. PTFE is a thermoplastic with an extremely low dielectric constant of ~ 2.1 . However, it presents significant processing challenges due to its poor adhesion resulting in high cost. Another thermoplastic, LCP, started gaining acceptance in the late 1990s. However, the high processing temperature required was an issue. In recent years, several new polymer resins and dielectric films are being developed targeting an optimum set of electrical and mechanical properties, low processing cost and ease of processing, including polyphenyl ethers (A-PPE) and hydrocarbons filled with ceramics (e.g. Rogers RO 4000 series).

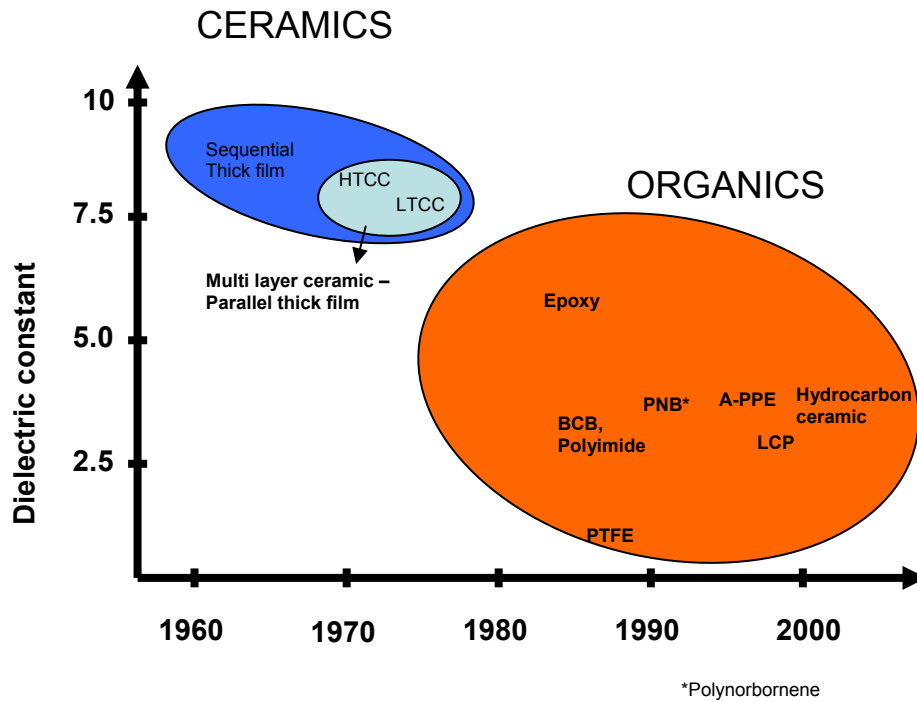


Figure 3.1 Historical Evolution of Dielectric Materials

3.2. Epoxy Dielectric: Chemistry, Processing-Structure-Property Relationship

The de-facto standard dielectric materials used in organic package substrates today are based on epoxy polymers. Epoxies are also widely used in packaging as moulding compounds, underfills, soldermasks and encapsulants. Traditional epoxy polymers for packaging are primarily a blend of Bisphenol A and epichlorhydrin, shown in Figure 3.2a and 3.2b²⁶. Bromine side group functionality (Figure 3.2c) is usually added for fire retardant properties necessary for package and circuit board applications.

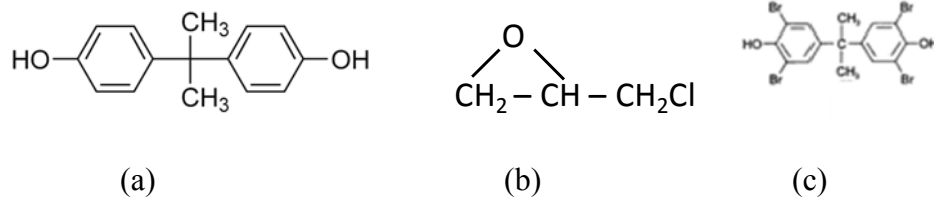


Figure 3.2 Structure of the Main Constituents of Epoxy Resins, (a) Bisphenol A, (b) Epichlorhydrin, and (c) Bromine functional side groups

In the past few years, most of the epoxy dielectric materials have been based on phenol or cresol novolac resins. The synthesis reaction of a typical multi-functional epoxy is shown in Figure 3.3.

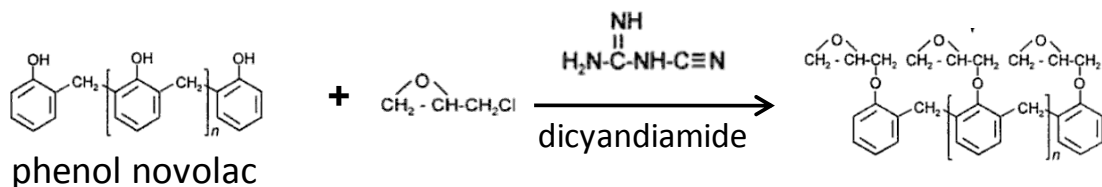


Figure 3.3 Chemical Reaction in Polymerization of Epoxy Dielectric

The most commonly used curing agent is amine based dicyandiamide (dicy) shown in Figure 3.3, which is mixed with the epoxy resin in typical ratio of 3-6 parts per

100 parts of resin. Epoxy resins are blended with the curing agents and dissolved in appropriate solvents to achieve optimum viscosity for flow during deposition processes. These prepared epoxy dielectrics are either spin cast or laminated as partially dried films on the substrate followed by a thermal curing process, which is typically done at 150-170°C for 1-2 hours. During the two-step condensation polymerization curing process, a 3D cross-linked network structure is obtained as shown in Figure 3.4, and this highly cross-linked structure is the source of the excellent thermal resistance and good mechanical properties of epoxy dielectrics. A typical example of epoxy build-up dielectric widely used in the industry is Ajinomoto Build-up Film (ABF).

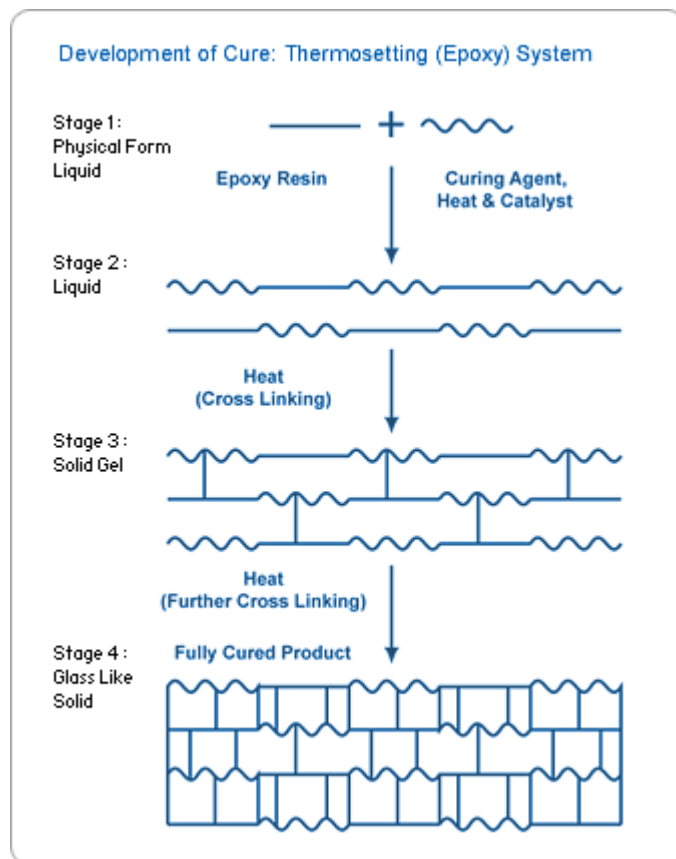


Figure 3.4 Various Stages in the Cross-linking & Curing of Epoxy Dielectrics²⁶

Epoxy polymers derive their unique combination of properties (high strength, good electrical insulation) from the “epoxide” or “oxirane” ring structure shown in Figure 3.2b. However, the characteristic epoxide structure allows moisture penetration into the epoxy dielectric due to available carbonyl (C=O) and hydroxyl (-H) bonding sites on the surface (which also contribute to the excellent adhesion of epoxy to metals such as copper). These bonds also have higher mobility and cause higher polarization in the dielectric resulting in higher energy loss and higher loss tangent. As the frequency of operation (and AC switching frequency) increases, the energy lost in dipole relaxation also increases and loss tangents of typical epoxies can go from 0.01 at 1 GHz up to 0.025 at 10 GHz. This increase in signal loss can limit the use of epoxy based package substrates for emerging RF-Digital mixed signal system applications.

There is a growing concern that there are major barriers for epoxy and other standard thermo-setting polymers for next generation packaging, primarily due to the following limitations:

- (a) High electrical loss, especially at GHz frequencies.
- (b) High moisture uptake of epoxies and resulting instability in electrical properties at GHz frequencies and adhesion to metals.
- (c) High CTE (60-80ppm/°C) of the neat resins, requiring loading of high volume % of ceramic fillers (e.g. SiO₂) to reduce the CTE of the dielectric film.
- (d) Bromination to provide fire retardant property (UL V-0 rating) to current epoxies and replacement by phosphorus and other elements which will require extensive study and re-certification.

3.3. Emerging Needs for Next Generation of Polymer Dielectrics

The choice of polymer dielectric for the next generation of microsystems packaging is driven primarily by the following technology trends and forces.

1. Move to higher temperature assembly processes due to elimination of lead for environmental benefits
2. Higher frequency and higher speed of electronics systems and emphasis on RF-digital mixed signal packaging with the advent of multi-communication devices with voice, video, and internet
3. Accelerating demand for miniaturization and high density interconnections with the shift to handheld consumer products

As seen in Figure 3.1, the primary driver for package substrate dielectrics until the end of the 20th century was the reduction of dielectric constant to keep up with the increasing signal speed for digital computing. The shift in systems drivers to mobile and wireless communication applications in recent years has led to a significant new requirement for dielectric materials, namely, low loss tangent and stable electrical properties into the multi-GHz frequency range. The next generation of build-up thin film dielectrics for packages will need a combination of low dielectric constant (for higher data rate digital signaling) and low loss tangent (for embedding RF signals and passive components).

These system drivers dictate property/process requirements for the build-up dielectric material and the main criteria used for selecting polymer dielectrics in this study were:

1. Electrical Properties: Low loss tangent and low dielectric constant for signal integrity at Gbps data rates and 1-80GHz RF performance. A major

need is for stable electrical properties with varying frequency, temperature and humidity conditions

2. Thermo-mechanical properties: Low CTE to achieve high reliability on top of low CTE core materials discussed in the previous section. High temperature stability and low moisture uptake for reliable flip-chip interconnect
3. Processability: Excellent flow properties for planar thin films (10-25um thickness per layer) without any polishing. Low process temperatures below 250°C. Ability to form sub-25um microvias for high density interconnections
4. Environmental: Pass all required fire retardant standards without the use of halogens.

3.4. Low Loss Polymer Dielectrics & Processes Explored in this Research

Based on the above property and processing requirements, two major dielectric materials were selected for extensive study,

(a) Benzocyclobutene (BCB), a low loss thin film dielectric commonly used in wafer level re-distribution layers (RDL), and

(b) Liquid Crystal Polymer, an emerging low loss dry film dielectric material.

The unique contribution from this research in each of these two materials is to: (a) explore, develop and demonstrate low cost package substrate processes on BCB to dramatically reduce the cost of processing BCB thin films at package substrate level, and (b) explore, develop and demonstrate package substrate processes on the new LCP materials for the first time. In both these cases, fundamental understanding of material

structure-process-property relationships to enable ultra-small microvias and is a critical element of this research. As a control material, the latest state-of-the-art epoxy dielectric was also explored for the fine via and line processes. During the final stage of this research, a new experimental low loss and thin film thermo-setting dielectric material from Rogers Corporation, named RXP, was used for the study. This material overcomes some of the barriers of BCB and LCP, is available as a thin dry film (10 μ m thick) and is more compatible with package substrate manufacturing than LCP and BCB.

The key dielectric processes explored in depth in this research are:

- (a) low-cost deposition and planarization methods for 10-25 μ m thick films,
- (b) excimer laser ablation of low loss polymers for ultra-small microvias in the 10-25 μ m diameter range, and
- (c) surface treatment of low loss polymers for optimum adhesion and ultra-fine line conductor formation.

3.4.1. Benzocyclobutene (BCB) Dielectric Polymer Microstructure and Properties

Benzocyclobutene is a low loss polymer used in high frequency applications. Most of the current uses of BCB in microelectronics are at the wafer level as a redistribution layer or other thin film passivation coatings. This research is focused on understanding the chemistry and properties of BCB, and exploring new low-cost package processes using low loss BCB dielectric. The BCB used in this research was CycloteneTM 3022 non-photo sensitive resin from Dow Chemical company. The polymer is based on divinylsiloxane bis(benzocyclobutene) (DVS-bis-BCB). The BCB hydrocarbon is produced by pyrolyzing alpha-chloro-o-xylene (Figure 3.5)²⁷. Treatment of the hydrocarbon with bromine provides 4-bromo-BCB in excellent yield. Palladium-

catalyzed coupling of 4-bromo-BCB with divinyltetramethylsiloxane produces the monomer DVS-bis-BCB. The monomer can be B-staged; that is, the curing reaction is started, then deliberately stopped before all of the monomer molecules are cross-linked. The resulting oligomer can be completely cured at a later time. The BCB four-membered ring opens thermally to produce o-quinodimethane (Figure 3.6). This very reactive intermediate readily undergoes Diels–Alder reactions with available dienophiles. The Diels–Alder reaction predominates in the B-staging of DVS-bis-BCB and in the subsequent step to generate the cured product.

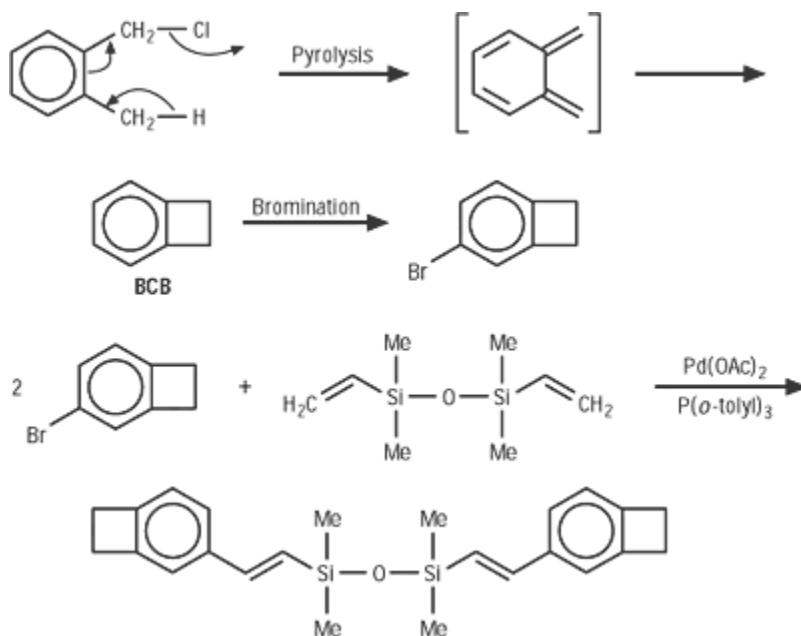


Figure 3.5 Process for the Synthesis of BCB

The process starts with a monomer. Pyrolyzing α -chloro-o-xylene produces the starting benzocyclobutene (BCB) hydrocarbon. A two-step reaction process yields the

divinylsiloxane (DVS)-based monomer DVS-bis-BCB, which can then be used to produce a variety of polymer formulations.

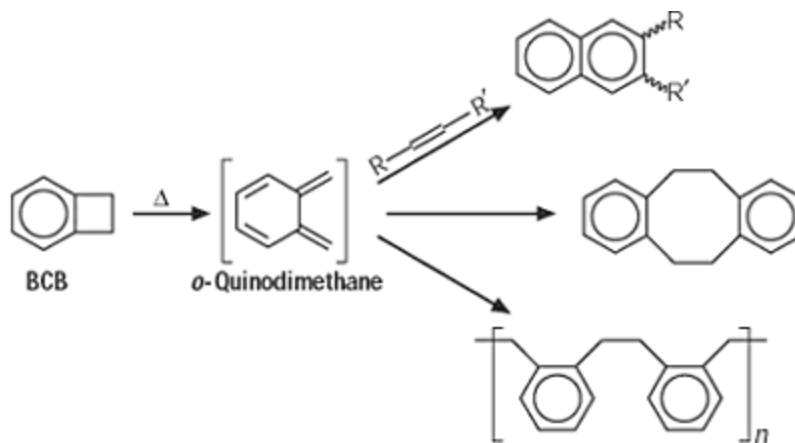


Figure 3.6 Diels-Alder Reaction for Polymerization and Curing of BCB

BCB serves as a starting point for a variety of other organic building blocks. If dienophiles are present in the reaction mixture, a Diels–Alder reaction predominates during the DVS-bis-BCB polymer curing process (top). If no dienophiles are present, the BCB entity can dimerize (middle) or polymerize (bottom). Because BCB polymers are hydrocarbons, and the ring opening polymerization process produces mostly non-polar groups, BCB has a very low dielectric constant, low loss tangent and low moisture uptake, consistent with the research targets outlined earlier.

3.4.2. Liquid Crystal Polymer (LCP) Structure and Properties

LCP is a thermoplastic polymer as opposed to thermo-setting epoxy and BCB polymers. Thermoplastics are melt processed and are compatible with recycling and more environmentally friendly compared to thermosets which are typically incinerated or buried in landfills. LCP is available as a high melting point (700-850F) polymer based on

bi-phenols (Xydar from Amoco) or lower melting point (545-640F) polymer based on naphthaline (Vectra from Hoechst Celanese). LCP has been a widely used high performance material in molded packages, connectors, and cables since the 1980s. However, process innovations in the 1990s led to the first viable dielectric films made from LCP. LCPs are wholly aromatic polyesters and Vectra resin used to make dielectric films is derived from 4-hydroxy benzoic acid (HBA) and 2,6 hydroxy naphthoic acid (HNA) monomers, shown in Figure 3.7.

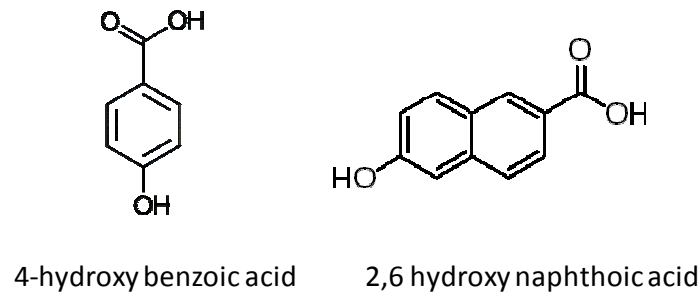


Figure 3.7 Structure of Monomers used for the Synthesis of Vectra™ LCP²⁸

LCP has a unique set of properties that combine the benefits of polymers and liquid crystals, derived from its polymer structure. LCPs are formed by introducing rigid “rod-like” elements (aromatic rings) into normally flexible polymer chains. During melt processing of the polymer, these rigid rods become fully oriented in the direction of shear forces. The structure of LCPs (Figure 3.8) consists of densely packed fibrous polymer "chains" that provide self-reinforcement almost to the melting point.

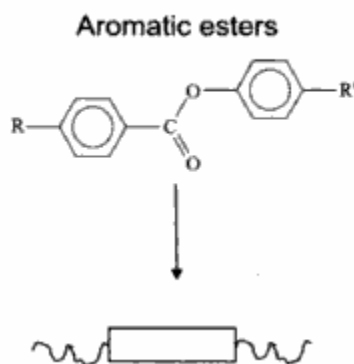





Figure 3.8 Structure of Aromatic Ester typical of Liquid Crystal Polymers

3.4.3. Low Loss Polymer Structure-Property Relationship, Processing Challenges

There is extensive literature on the study of polymer structure characterization and relationship to dielectric and mechanical properties of the three polymer systems described in this research. The beneficial properties of high performance polymer dielectrics such as BCB, LCP and the new RXP materials, including low loss tangent at high frequencies, low moisture uptake, and low CTE are derived essentially from their basic polymer chain structure, and the critical structural considerations are described below.

Polar Groups, Stiffeners and Reactive Sites in Main and Side Chains: Table 3.1 shows the molar polarization of some of the functional groups commonly found in dielectric polymers²⁹.

Table 3.1 Molar Polarization Comparison of Various Polymer Functional Groups

Functional Group	Molar Polarization (Φ)
-CH ₃	5.6
-CH ₂ -	4.7
	25.0
	15.0
	10.0
-O-	5.2
-OH	20.0

The availability of polar groups and reactive sites in the side chains of the polymer structure is a key determining factor in electrical properties and moisture absorption. The hydrocarbon based functional groups (C-H) have very low polarity and high bond energies, and this results in low dielectric loss and low reactivity. However, groups such as carbonyls (C=O) are more polar, and especially hydroxyl (-OH) groups commonly found in epoxies are among the most polar. Additional factors that are critical to electrical properties are the presence of rigid rods or stiffeners in the main chain of the polymer, such as phenyl rings, which limit mobility and contribute to slow dielectric relaxation and low loss, especially at GHz frequencies.

In the case of LCP, the rigid rod structure explained in the previous section is a major contributor to the low CTE of the dielectric film, and the lack of polar groups such as hydroxyls and reactive functional groups (-Na or other ionics) in the side chain contributes to stable and low loss tangent and very low moisture uptake into the polymer.

For BCB, water uptake is reduced due to the presence of the hydrophobic nature of the siloxane (Si-O-Si) segments. In both cases, the main chain phenyl rings result in fairly rigid structure and low thermal expansion, and the lack of molar side groups leads to low dielectric constant, low loss and low moisture uptake. The reason for the excellent properties of the RXP dielectric material is its predominantly hydrocarbon structure (C-H). However, the lack of phenyl rings or other stiffeners results in fairly high CTE for this material, and ceramic fillers are used in the RXP dielectric to reduce the CTE to acceptable levels for the substrate. Table 3.2 summarizes the key properties of these three high performance polymer dielectrics that form the basis of this research. The low moisture uptake is a very important characteristic of all three materials, since moisture coming into the dielectric can cause significant increase in dielectric loss at RF and microwave/millimeter wave frequencies.

Table 3.2 Summary of Electrical and Thermo-mechanical Properties of Build-up Dielectrics

Dielectric Polymer	Dielectric Constant	Dielectric Loss	CTE (ppm/C) No fillers	Moisture Uptake (wt%)
Epoxy	3.5-4.5	0.015-0.03	60-80	~1%
BCB	2.65	0.0008	52	~0.1%
LCP	2.9	0.002	6-18 (tailorable)	<0.04%
RXP	2.9	0.003-0.004	70-90	0.04%

However, the same polymer structure that results in the excellent properties of these advanced dielectric materials is also the root cause of major processing challenges. The lack of reactive and polar functional groups on the surface of these deposited films

leads to poor adhesion to copper. The strong 3-D bonding in the structure presents a challenge in terms of laser processing. The key process steps to integrate these materials into ultra-high density substrates are deposition/planarization, microvia formation, surface modification (for bonding) and copper metallization (surface & vias). The remainder of this chapter is dedicated to the process innovations explored and demonstrated on BCB, LCP and RXP dielectrics in these steps.

3.5. Ultra-Thin Polymer Dielectric Film Deposition Process-Structure-Property Relationship

The first major process challenge addressed was the deposition of thin dielectric films (10-25um thickness per layer) using low-cost package substrate compatible processes on the core substrate and copper metallization on the core surface. The main focus of this work was dry film lamination process (heat and pressure), although BCB is only available as a liquid and a low-wastage meniscus coating process was used as an alternative to conventional spin coating used for on-wafer BCB applications.

Since most of the high density IC substrates require multiple wiring layer build-up on the core, achieving near-100% degree of planarity (DOP) was a critical requirement. Although the current state-of-the-art organic substrates have excellent planarity, the dielectric thickness is close to 40um and copper thickness of 12-15um, compared to the more aggressive research targets as shown in Figure 3.9. It was important to understand the starting polymer structure and maintain the unique low-loss polymer structure through deposition process, so as to not impact the beneficial properties.

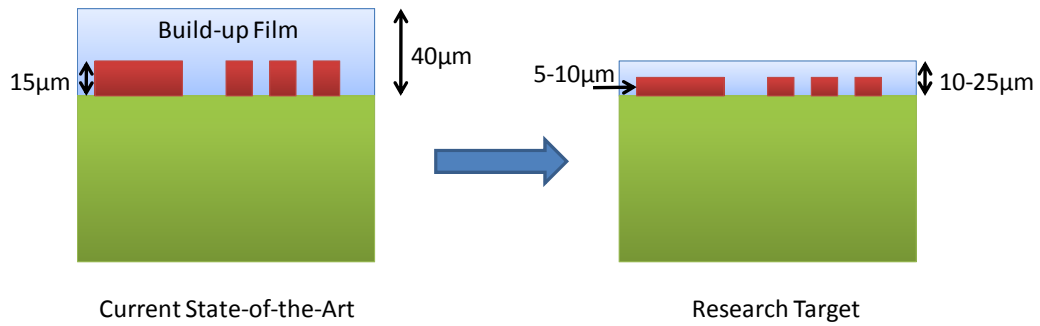


Figure 3.9 Dielectric Deposition Challenge for the Current Research Compared to State-of-the-Art

Thermoplastic LCP Dry Film Lamination Process

LCPs are typically processed into useful shapes via a melt extrusion process. The unique rigid-rod liquid crystal microstructure also leads to a uni-axial flow behavior and highly anisotropic properties using the conventional extrusion process (Figure 3.10). This is useful for achieving high melt flow and ease of extrusion; however, there are some property related problems for the resulting LCP dielectric, especially in dry film form. The issues arise from the alignment of the rigid rods in one direction during melt flow and are related to anisotropy of dielectric properties, and poor adhesion between layers in the Z direction.

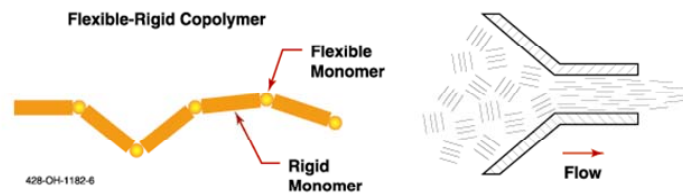


Figure 3.10 Conventional Melt Flow Extrusion Process for LCP results in Electrical and Mechanical Property Anisotropy

The major innovation in the 1990s that enabled the viability of LCPs as a dielectric film for package substrate applications was the use of counter-rotating die concept, pioneered by Kuraray in Japan, shown in Figure 3.11.

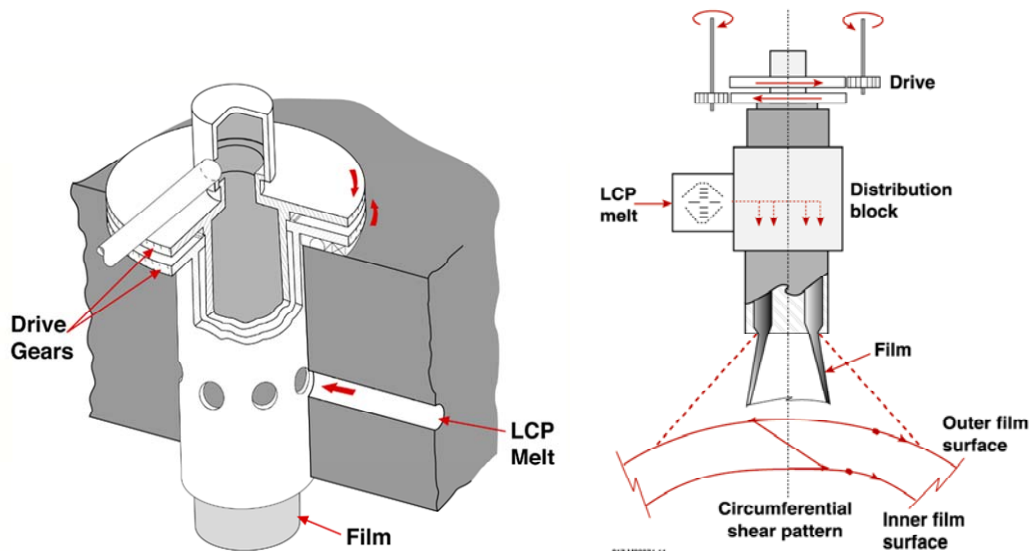


Figure 3.11 Counter-Rotating Die Concept for Producing LCP Dielectric Films with Biaxial In-Plane Property Isotropy³⁰

This process results in thin LCP dielectric films with alternating orientations of the rigid rod polymer chains, and the final composite film has much improved bi-axial property uniformity (Figure 3.12)³¹.

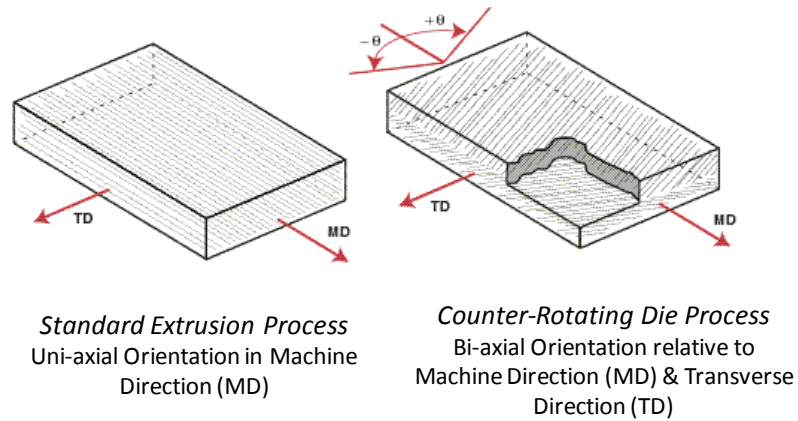


Figure 3-12. Uniaxial and Biaxial Orientation of LCP Films

Additional modifications have also been achieved by commercial dielectric film suppliers to improve the cohesive strength of LCP films. The melting temperature of the LCP film can also be controlled through the starting monomers and process. Two LCP films were used in this study from Rogers Corporation, one with a higher melting point of 325°C (called laminate in this study) and a second film with a lower melting point of 280°C (bond-ply).

A vacuum hot press was used to optimize the lamination process parameters (temperature, time, pressure) for multilayer LCP substrate structure shown in Figure 3.13.

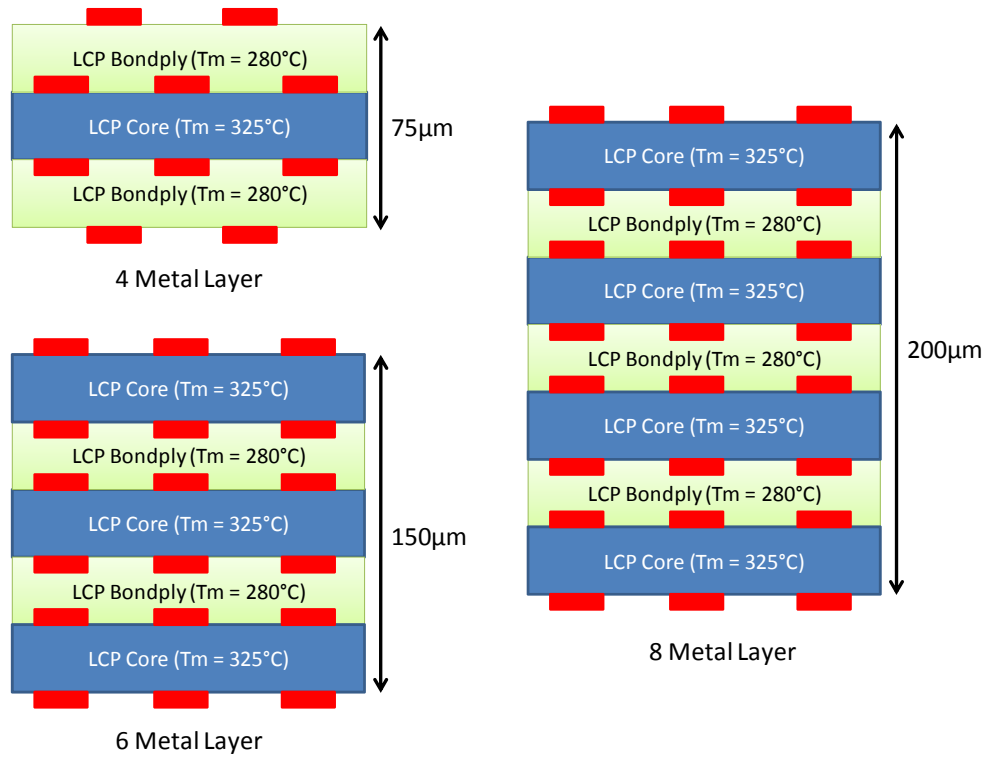


Figure 3.13 Four, Six and Eight Metal Layer Thin All-LCP Substrate Cross-section Schematic

The two main targets for the lamination process were (a) to achieve sufficient bonding of LCP to copper and LCP to LCP, and (b) obtain sufficient flow and fill to planarize the LCP dielectric over underlying copper traces. This was accomplished by leveraging the softening of LCP above 200°C and below its melting point of 280°C, as shown in Figure 3.14. Temperatures much higher than the melting point of the LCP during lamination with pressure can cause significant damage to the bi-axial in-place isotropy optimized by the counter-rotating die fabrication process.

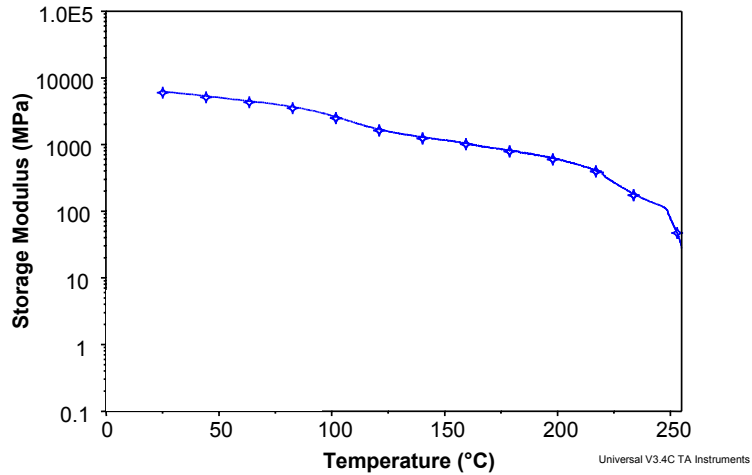


Figure 3.14 Drop in Modulus of LCP with Temperature as measured by DMA analysis³²

Based on this understanding of the LCP material behavior and impact on its microstructure with high temperature excursions, various temperatures were evaluated for the lamination process for 25µm thin film LCP dielectric. The lamination profiles down-selected for final evaluation are shown in Figure 3.15. These temperatures were selected based on initial design of experiments and around the melt point of 280°C for the lower melting LCP “bondply”.

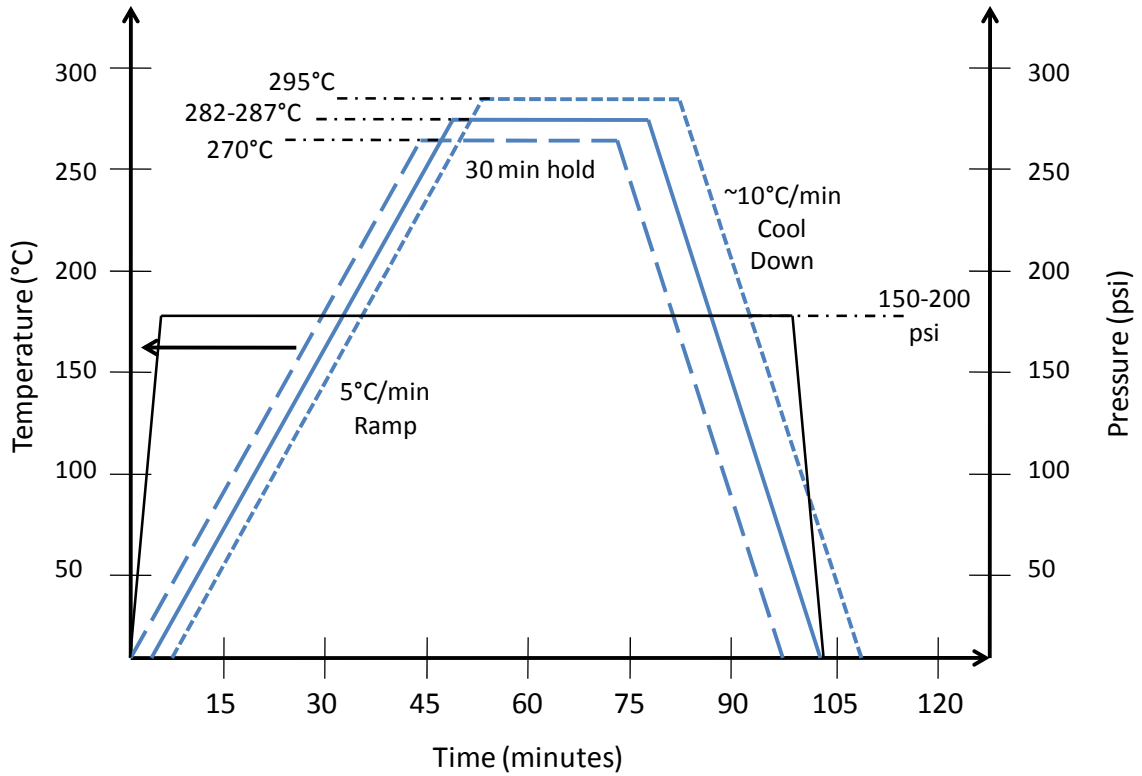


Figure 3.15 Lamination profiles optimized for multilayer LCP substrate shown in Figure 3.14

The heating ramp rate was maintained at 5°C per minute and hold time at peak temperature was optimized at 30 minutes to allow sufficient time for the entire 300mm substrate to reach an equilibrium lamination temperature. The pressure was applied during the heating ramp and maximum pressure of 175psi was found to be optimum to achieve planarization by flow and fill without excessive squeeze out of the dielectric from the edge of the substrate panel. This pressure was held through the hold cycle and entire cooling cycle, and the pressure was released only below temperature of 100°C.

The samples were analyzed by micro-sectioning, high resolution X-Ray imaging, and peel testing for layer to layer adhesion. The lamination at 295°C resulted in good bonding of the LCP bondply to Cu and to LCP core, however, the low melt viscosity and high pressure caused excessive flow of the LCP and distortion of the substrate structures as shown in Figure 3.16 (a – microsection, and b – X-ray images)

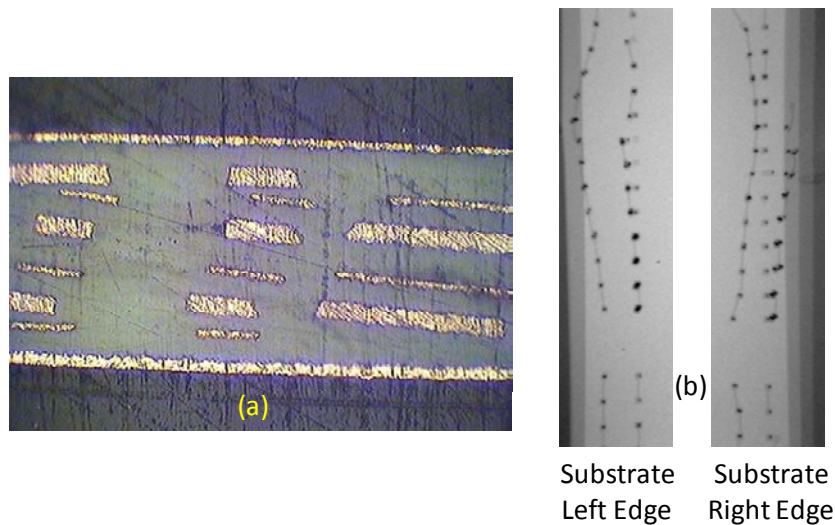


Figure 3.16 Distortion in Metal Traces during LCP Lamination at Temperature Much Above the Melting Point (280°C) as seen in (a) Microsection, and (b) X-Ray imaging

Figure 3.17 shows a micro-section of the sample laminated at 260-270°C range peak temperature. Although no distortion of metal traces were observed and layer to layer alignment was within 25µm, the bond strength of the LCP core to LCP bondply was insufficient and severe delamination was observed during peel testing. This was attributed to lack of melting of LCP at the interface to create good layer to layer bonding.



Figure 3-17. Delamination due to Insufficient Melting of LCP at 260-270°C

The optimum lamination profile that resulted in excellent bonding without any trace distortion was observed with peak temperature in the 282-287°C range for 15-30 minutes (depending on substrate size) and pressure of 150-175psi. The microsection and X-ray results from this lamination profile (from Figure 3.15) are shown in Figure 3.18 and this condition was used for all subsequent processes with the LCP dielectric.

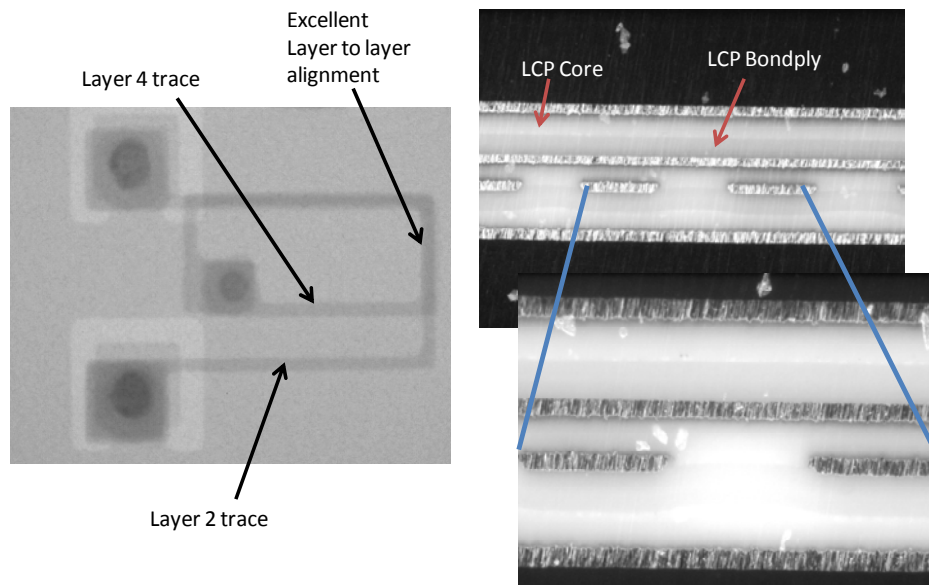


Figure 3.18 Results from Optimized Lamination of LCP Core and LCP Bondply showing excellent layer to layer alignment, no distortion and good bonding as seen in X-ray image (left) and microsections (right)

Thermosetting BCB and RXP Dielectric Film Deposition Process

In contrast to thermoplastic polymers such as LCP, thermo-setting polymers are deposited in the B-stage (partially cured) or as liquid resin (no cross-linking or curing). They undergo complete polymerization and curing after deposition by thermal treatment in a lamination press or in an oven. In this study, two low loss thermosetting polymers were explored:

- (i) BCB from Dow Chemical, a commonly used polymer in wafer level processes, with a focus on demonstrating laser microvia and wet metallization processes without any CMP polishing to reduce the cost of adopting this high performance material for low cost package substrates, and
- (ii) RXP, an emerging hydrocarbon based polymer system under development from Rogers Corporation, with unique combination of standard FR-4 like processing and low loss and low moisture uptake required for high frequency electrical performance.

BCB Deposition and Planarization Process: Cyclotene 3022-57 non-photosensitive resin was used to achieve the target film thickness of 9 μ m per layer. This liquid resin was processed via spin coating on 150mm C-SiC core substrates and 300mm low CTE laminate (Asahi Chemical A-PPE or Hitachi Chemical E-679LD) substrates as shown in the schematics in Figure 3.19.

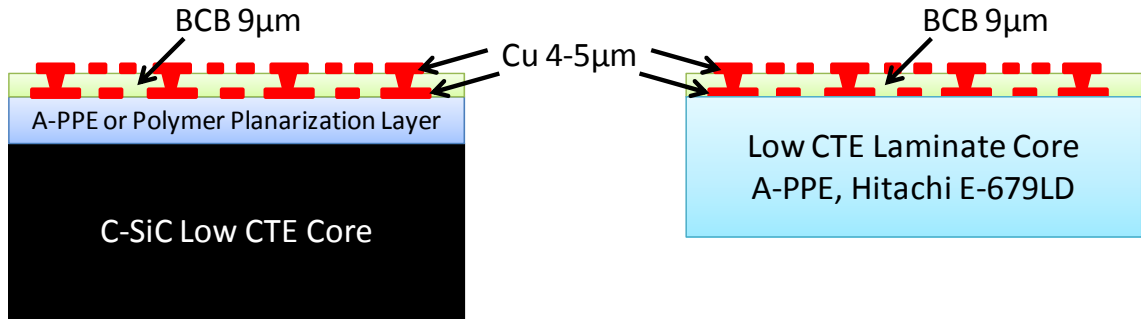


Figure 3.19 Target Structure for BCB deposition on C-SiC (left) and low CTE laminate (right) core substrates

The spin speed vs. film thickness guideline was taken from the Cyclotene data sheet, however, the process parameters had to re-optimized for the 300mm Karl-Suss RS16 spin coater used considering the viscosity of 259 cSt @ 25°C for the Cyclotene 3022-57 resin. Also, subsequent plasma roughening treatment for wet metallization reduced the thickness of the cured film by 1-2µm and this was taken into account during the spin coating process optimization. The as-deposited and cured film was targeted at 11µm to achieve the post-etching treatment thickness of 9µm used for the 50Ω transmission line design. The data for the spin speed vs. thickness is summarized in Figure 3.20, with linear and exponential curve fitting equations.

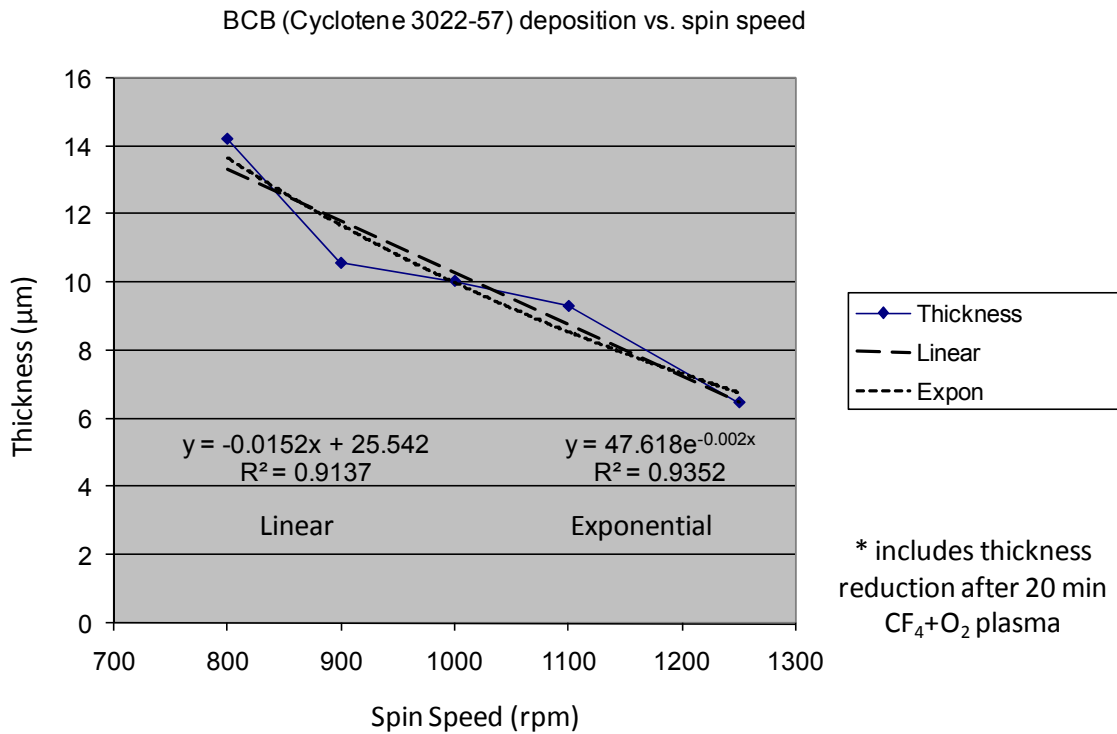


Figure 3.20 BCB Film Thickness after Curing and Plasma Surface Treatment plotted against Spin Speed

The degree of planarity (DOP) of the spin coated BCB films was analyzed by surface profilometry using a Veeco Dektak 3030 instrument. Test patterns with line widths and spaces from 25μm to 100μm were used as underlying copper structures with copper thickness of 4-5μm. For the larger line widths of 75 and 100μm, degree of planarity of ~90% was observed, while the degree of planarity for fine lines of 25 and 50μm decreased to ~80-85%. Figure 3.21a illustrates a microsection of 9μm BCB thin film coated and cured on top of 4-5μm thick wide copper traces. As explained in the next chapter on fine line fabrication, this level of DOP is not quite sufficient for low-cost imaging process to achieve ultra-fine lines <10μm.

Hence, an additional planarization step involving lamination with temperature and pressure and a polished steel plate as the planarizing surface was used after the coated BCB was baked at 90°C for 30-45 minutes to remove solvents. This planarization step was optimized at 150°C for 15 minutes at ~200psi, and the planarity of all the structures improved significantly and a microsection of the fully planarized BCB film after full thermal cure is shown in Figure 3.21b.

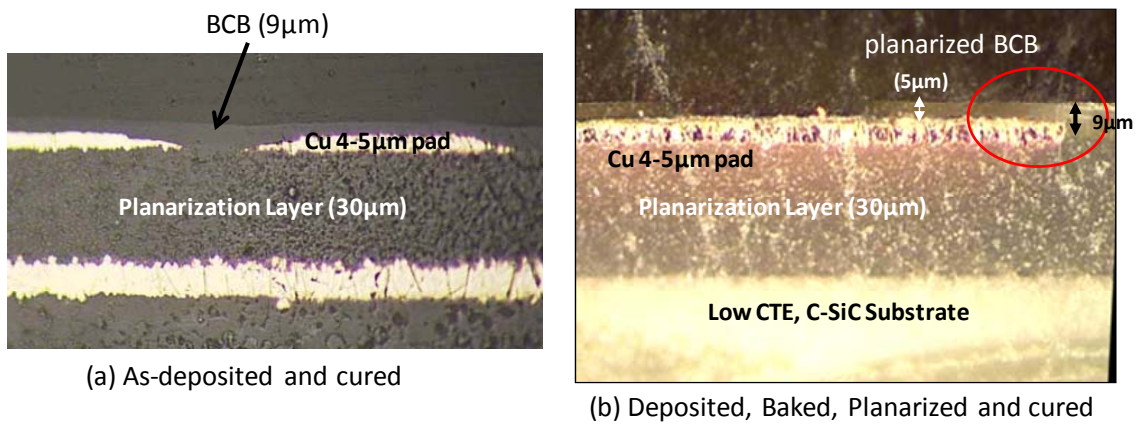
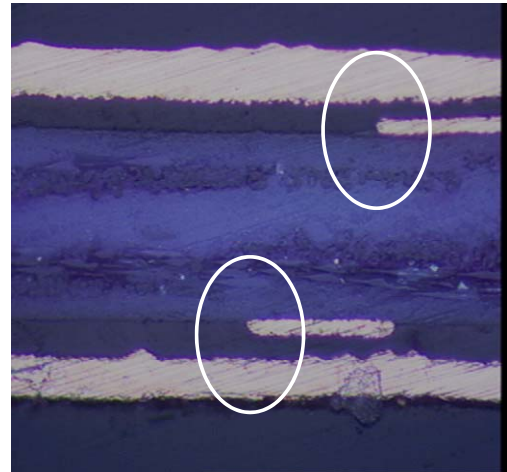
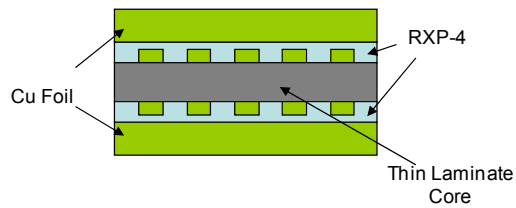


Figure 3.21 Planarization of BCB Thin Film after (a) spin coating and curing, and (b) using an intermediate planarization step before curing

RXP Dry Film Lamination and Planarization Process: Unlike BCB which is available as a liquid resin for thin film coating, RXP low loss dielectric was obtained as a dry film coated in copper foil (resin coated foil or RCF), or on mylar backer film. RXP dielectric was used in two thicknesses, 18µm and 9µm. The lamination conditions were optimized at 450°F for 60-90 minutes at 400 psi pressure. Figure 3.22 shows the excellent planarity achieved by high pressure lamination of RXP thin dry film.

5"x5" double sided hot press laminated RXP-4 with clad copper foil on RXP-1 Thin Low CTE Laminate Core



Excellent Degree of Planarization for 18µm Thick RXP-4 (Cu trace thickness under RXP-4 is 8µm)

Figure 3.22 Lamination Schematic for Thin Low Loss RXP-4 Thermoset Dielectric Film (left bottom) and excellent planarity achieved after optimized lamination of 18µm thick RXP-4 dielectric (right)

In summary, extensive process research was conducted to achieve thin film deposition with near 100% degree of planarity using low cost lamination and coating processes for three low loss dielectric polymers, namely, LCP, BCB and RXP-4.

CHAPTER 4

ADVANCED, ULTRA-SMALL MICROVIA FORMATION PROCESSES

This chapter presents the research on advanced processes for 10-30 μm diameter microvias in low loss BCB and LCP thin dielectrics using excimer laser scanning projection ablation technology. Additional research on photovia process for epoxy dielectrics and UV laser ablation process for an emerging thermosetting low loss dielectric (RXP-4) are also discussed. There is a clear emphasis on fundamental understanding of laser-polymer interaction mechanisms. Analysis of key findings during ultra-small microvia formation based on the polymer chemistry is included.

Figure 4.1 summarizes the various microvia formation techniques available for package substrates and their microvia size range for leading edge technology and standard manufacturing technology.

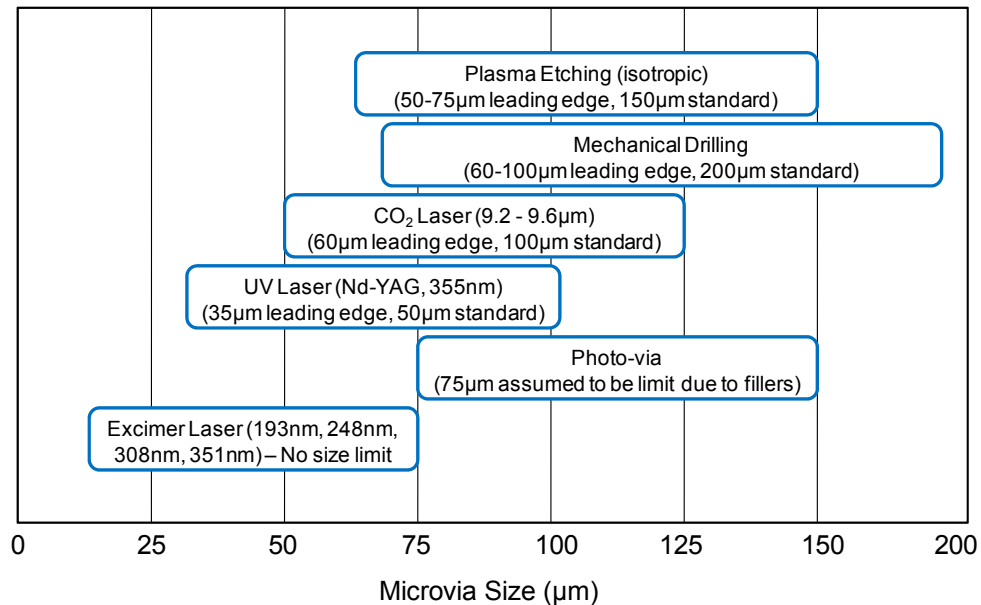


Figure 4.1 Microvia Fabrication Technologies for Package Substrates

The dominant approach to microvia fabrication in high volume manufacturing today is CO₂ laser ablation, mainly due to the process consistency, excellent reliability of resulting microvias, equipment stability and availability in industry infrastructure. However, the highly thermal CO₂ laser ablation process and difficulty in focusing the beam to small spot sizes limits the practical microvia sizes achievable to around 60µm diameter. The research target in this thesis was to explore and demonstrate 1:1 aspect ratio (diameter = thickness) microvias in the 10-30µm diameter range for the low loss dielectrics, LCP, BCB and RXP-4, well beyond the state-of-the-art and capable of meeting IC roadmap needs for the next few generations. The available options for reaching these microvia diameters were UV lasers and excimer lasers. Photovia technology was also explored for epoxy dielectrics, although this approach is not widely used due to limited photo-sensitive materials and difficult process control in volume manufacturing.

4.1. Photovia Process to Achieve 25µm Via Diameter in Epoxy Dielectric

In the initial phase of this research study, photo-sensitive epoxy dielectric materials in liquid resin (Ciba Specialty Chemicals ProbelecTM 81/7081), and dry film (DuPont VialuxTM) were used to explore the limits of photovia technology. Photovia processes use a photoimageable dielectric liquid or dry film which is processed using conventional photolithographic techniques with a typical process flow as shown in Figure 4.2. The major advantage of photovia technology is mass via formation in a single process which offers a cost effective alternative to laser ablation for very high via density substrates.

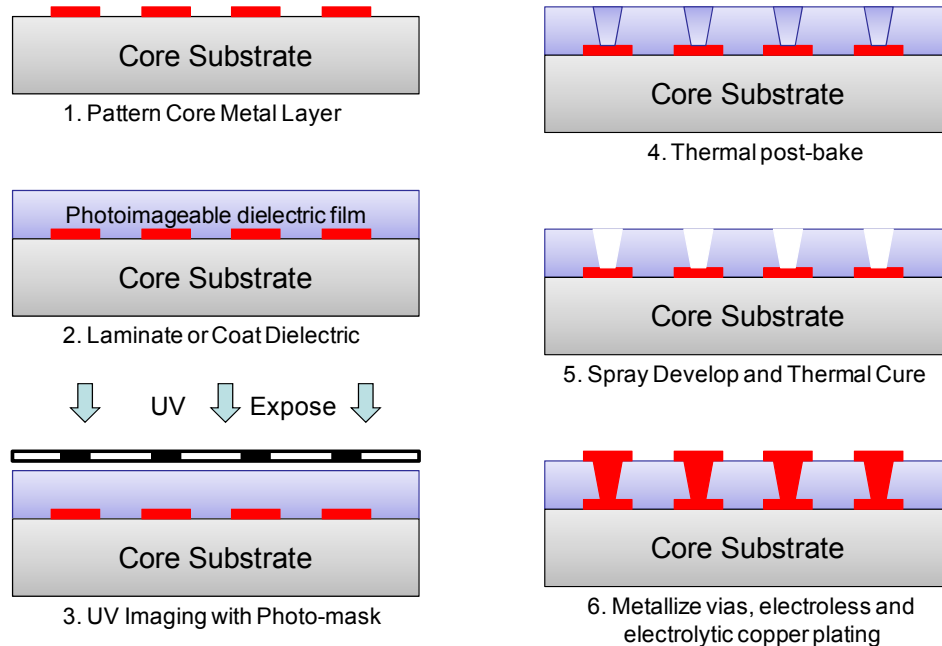


Figure 4.2 Process Sequence for Photo-Via Fabrication

For this study, one microvia layer was built up on top and bottom side of FR-4 or FR-5 core substrates using photodielectric dry film epoxy. The thickness of the photosensitive epoxy dielectric film was 25 μm . The dry film photoepoxy dielectric was vacuum laminated on the core metal layer pattern to achieve a planar surface. UV exposure was performed on the Tamarack 152R contact printer under vacuum hard contact with a Mylar phototool. Spray developing with Gamma Butyrolactone (GBL) solvent was used to create the vias. Registration was done using two cameras on target fiducials and a manual micro-alignment stage on the Tamarack 152R. The metallization process consisted of chemical roughing of the dielectric surface, and electroless copper plating followed by electrolytic copper pattern plating.

The fundamental polymer chemistry and reaction sequence for the photo-sensitive epoxy polymerization is shown in Figure 4.3, starting from monomers and curing agents mixture dissolved in appropriate solvent (propylene glycol mono methyl ether or PGMEA).

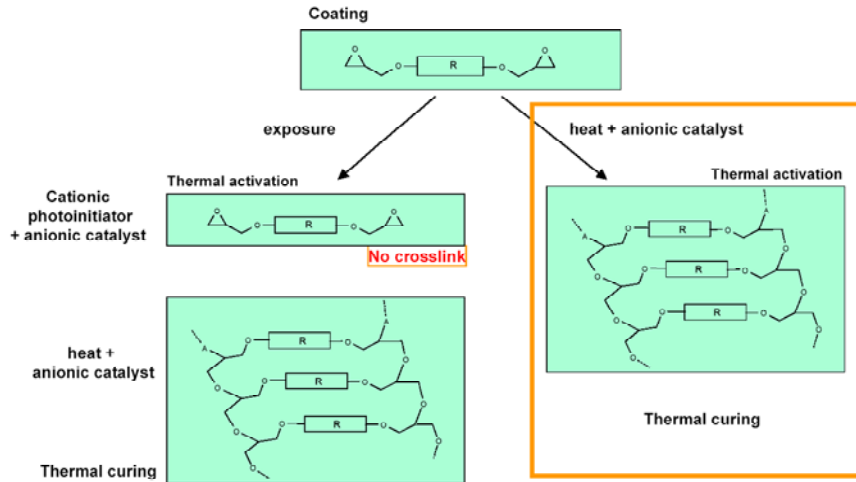


Figure 4.3 Fundamental Polymer Reactions during Photo-Epoxy Via Processing

The first step after coating the liquid epoxy into a thin film on the substrate involves thermal baking to remove all the solvent. In the case of dry film dielectric, most of the solvent is pre-baked out of the film by the material supplier. The UV exposure step illuminates selective regions of the dielectric, and since the epoxy used was negative acting, the cationic photoinitiator is released in the illuminated areas. The via diameter is a region where UV light is blocked and so there are no photoinitiators released in the via regions. An optimum UV dose of $300\text{-}500\text{mJ/cm}^2$ was determined through a series of experiments.

The thermal post-bake at 110°C for 60 minutes is a critical step which hardens the exposed areas by thermal activation while the blocked off areas remain in the as-deposited and dried condition. This difference also causes the UV exposed areas to be resistant to the solvent used for wet chemical spray developing of the microvia patterns. Gamma butyrolactone (GBL) was the solvent used for developing the microvias in the photo-epoxy dielectric film. After inspecting for completion of the developing process (2-4 minutes) and no residual dielectric in the bottom of the vias, the film is fully cured by a thermal process at 160-170°C for 60-90 minutes. The cross-linking of the epoxy polymer chains only takes place in this final step. After cure, the polymer was roughened by conventional wet chemical treatment with sodium permanganate etching solution. Then, a thin electroless copper seed layer was deposited, followed by photoresist lithography to define the via pads and line patterns on the top surface of the photo-epoxy dielectric. The final steps in the via metallization process were electrolytic pattern plating, photoresist stripping, and electroless copper seed layer etching (mild etch) to complete the via metallization process.

The microvia test structures consisted of daisy chain vias of 25, 50, 75 and 100 μm diameter as shown in Figure 4.4. The samples were subjected to liquid-to-liquid thermal shock cycles from -55°C to 125°C using an ESPEC Thermal Shock Chamber TSB-5. The chamber was set for automatic operation. One operation consisted of 100 thermal shock cycles and each cycle lasted 10 minutes. The transfer time from liquid to liquid was less than ten seconds. Resistance measurements were recorded after every 100 cycles and samples were cycled to 2,000 cycles.

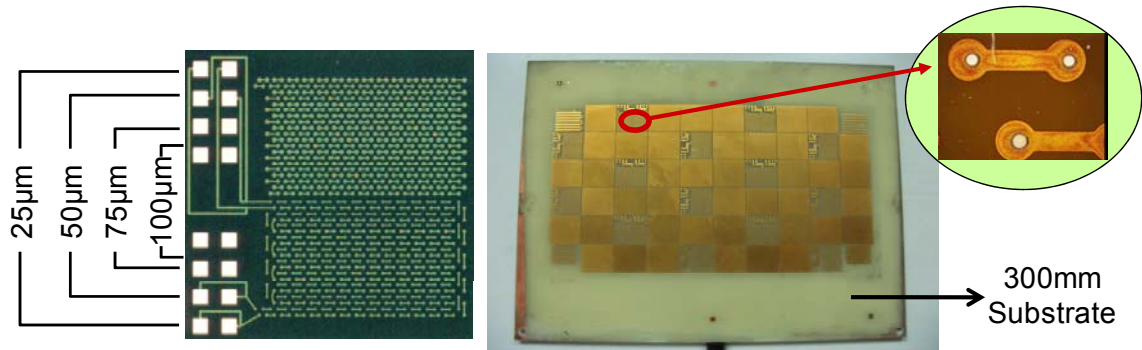


Figure 4.4 Microvia Daisy Chain Test Structures (Left), and Fabricated Substrate with Photo Microvias (Right)

The resistance R of microvias was measured using a four-point probe technique, and a 10% increase in resistance was considered a failure. Statistical failure rates were calculated and the reliability of the microvias formed with photo-epoxy dielectric was evaluated through electrical testing. Resistance R was measured with a LCR meter by probing every 10 vias connected in series. All resistances measured were the sum of the via resistance and the resistance from the lines and pads. The effective via resistance was deduced by subtracting the line and pad resistances as measured on the continuity test structures without any vias.

The average initial resistance of a 50 μm microvia was measured to be around 1 $\text{m}\Omega$. All other microvias having diameters of 75 μm and above had less than 1 $\text{m}\Omega$ resistance per via. The microvias demonstrated excellent robustness during the reliability test. Results from the thermal shock tests showed that all the microvias having diameters of 25, 50, 75, and 100 μm . fabricated using 25 μm thick dielectric passed 2,000 thermal shock cycles. No resistance changes were observed for all microvias tested on this sample set.

Figure 4.5 shows both the cross sections of the 25 μ m microvia and 50 μ m microvia that survived 2,000 thermal shock cycles.

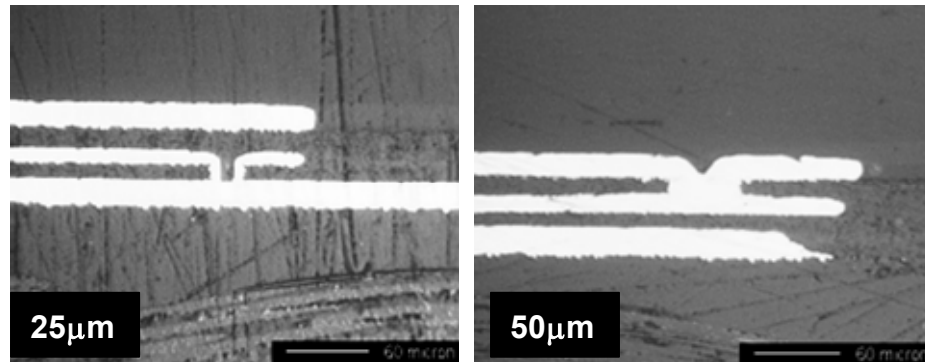


Figure 4.5 Micro-sections of 25 μ m and 50 μ m Diameter Microvias in Photo-Epoxy that Survived after 2000 Thermal Shock Cycles

This study showed that small photovias have potential for high reliability. It is well known that CTE mismatch between the dielectric film and the plated copper is one of the main causes of microvia interconnect failure. Thermal shock testing in liquid medium is a more stringent test of the thermo-mechanical reliability of a component than Air-to-Air testing. The liquid-to-liquid thermal shock testing method provides an accelerated test for microvia substrate failures.

During this study, it was also observed that incomplete cure of the polymer dielectric material was a potential source of failures and substrate rejects. Partially cured dielectric films may result in delamination and other instabilities during subsequent metallization and processing.

Curing processes need to be monitored to fully cure the interlayer dielectric based on the equipment used³³. Thinner dielectric films will enhance microvia reliability by making aspect ratios more favorable for via formation and metallization processes. This can be inferred from the current experiment on 25 μm diameter microvias using 25 μm thick dielectric film. Results from cross sectioning indicate that the failure mode for some of the 50 μm microvias that failed during thermal shock tests was identified to be cracks at the foot of the microvias as shown in Figure 4.6. Here the 50 μm via has nearly a 1:1 aspect ratio. The cracks are considered to be a result of the CTE mismatch between the copper and the higher expansion epoxy dielectric film. The thin copper metallization at the foot of the microvia only exacerbates the problem. With the extreme temperature changes from the liquid to liquid, thermal cycling the thin metal coverage in the microvia fatigues and subsequently cracks because it cannot support the induced thermal and interfacial stresses.

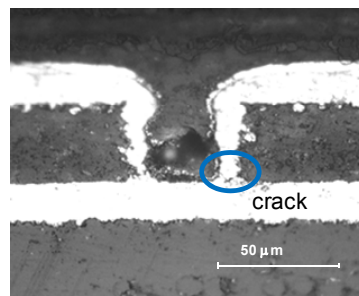


Figure 4.6 Micro-section of 50 μm Diameter Microvia in Photo-Epoxy that Failed during Thermal Shock Testing

In summary, although 25 μ m diameter microvias were demonstrated using photovia process, this approach has limitations due to mainly epoxy based photo-sensitive materials being available, and high cost and difficult process control for advanced dielectrics like photo-BCB. Also, filler loading in epoxies has a detrimental effect on the resolution of the photo-lithography process and this may limit the down-scaling of via diameters below 25 μ m. The next section focuses on the main approach in this research, namely UV and excimer laser ablation, for ultra-small microvia formation in low-loss dielectrics.

4.2. Excimer and UV Laser Ablation Of Small Microvias – Photo ablation by nanosecond excimer laser and downscaling of via diameter (10-30 μ m) in Ultra-Thin (10-25 μ m thickness) Low Loss Polymer Dielectrics

CO₂ lasers are widely used in the packaging industry today to drill microvias, but the wavelength range of 9.2-9.6 μ m for both RF-excited and TEA designs makes it challenging to focus the beam to diameters below 60 μ m. The next choice of lasers is the solid state Nd-doped (YAG and Vanadate) “UV” lasers with a first harmonic wavelength of 1.064 μ m and operate as frequency tripled (355nm) or frequency quadrupled (266nm).

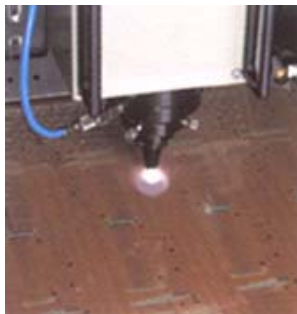


Figure 4.7 Photograph of Nd-YAG laser during ablation

In commercial UV laser systems, the beam can be typically focused down to 10-20 μm diameter (Figure 4.7) resulting in ablated spot sized in the 25-35 μm range. These lasers have high pulse repetition frequency (5 – 100 kHz) with highly coherent beams and power levels in the 1-10W range. The focused laser beam is used to ablate via patterns by computer controlled direct write method from design data. Either the laser beam spot can be optically scanned over the workpiece or the workpiece moved by precision XY tables.

For via diameters below 25-30 μm , the only viable option today is the excimer (short for excited dimer) laser with different wavelengths based on the gas mixture used, XeF₂ (351nm), XeCl (308nm), KrF (248nm) and ArF (193nm). The excimer laser produces low coherence beams with high pulse energies (0.01 – 1J), ns pulse widths, and relatively low pulse frequencies (<1kHz). This combination of parameters makes it ideally suited to the mask-imaging technique. The laser beam is first homogenized and then used to illuminate a mask. A high-quality lens is then used to project and image the mask pattern onto the substrate.

Similar to photo-via processes, excimer laser via ablation processes create all the vias on a substrate panel at one time, as opposed to single via at a time drilling for Nd-YAG and CO₂ lasers. As via densities in the package substrate escalate with increasing demand on I/O density from the ICs, mass via generation processes will eventually reach a break-even point where they are more economical compared to point-to-point drilling systems. Also, high power CO₂ lasers have the highest throughput for thick dielectric films (especially >50 μm film thickness and with glass or ceramic reinforcement). UV lasers have lower ablation rates and throughput than CO₂ lasers, however, they start to

become competitive for un-reinforced dielectrics in the 25-50 μm thickness range. If we extrapolate this technology trend in light of continuous reduction in package and dielectric thickness, excimer lasers hit the sweet spot when dielectric films are un-filled and approach thickness of 10 μm with extremely small vias at very high densities. Figure 4.8 illustrates the optimum technology nodes for the three different laser via ablation systems, and this forms the basis of the future focus in this research on excimer laser technology.

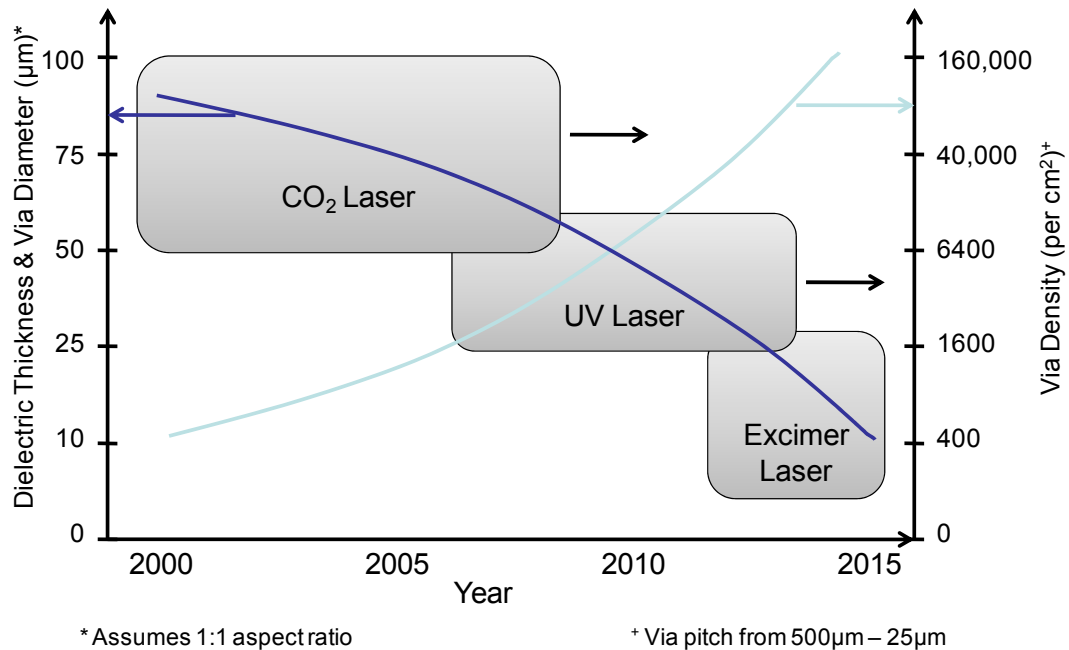


Figure 4.8 Trends in Down Scaling of Microvias and Three Major Laser Technologies

Fundamentals of UV and Excimer Laser Ablation: There are two primary modes of UV laser ablation; (i) photo-chemical which involves bond breaking and excitation and (ii) photo-thermal, which causes melting and vaporization of material. The sequence of events in photo-chemical and photo-thermal ablation are shown in Figure 4.9.

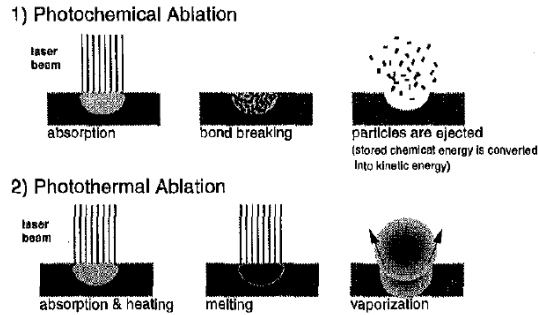


Figure 4.9 Mechanism of Ablation

Polymer ablation depends on two key conditions. First the polymer must absorb light strongly at the laser's wavelength. Clean, precise ablation usually requires linear absorption coefficients of at least 10^4 cm^{-1} . Second, ablation occurs only after the polymer has absorbed a minimum energy per unit volume, i.e., the laser intensity must exceed a threshold value.

The general features of UV laser ablation of polymers are summarized as follows:

- Polymer ablation takes place within 10 to 100 nanoseconds.
- The threshold energy fluence, defined as the fluence at which the etch depth is $0.05 \mu\text{m}$ per pulse, is low for polymers (typically in the range 10 to 100 mJ/cm^2).
- For fluences near or below the threshold, the etch depth follows Beer-Lambert's law (photo-chemical, linear absorption). In the photoablative regime (fluences just above the threshold and up to 10x ablation threshold) the ablative mechanism is well defined and can be used for controlled-depth ablation. For fluences well above the threshold, thermal effects contribute to the etch depth. In addition, the longer the wavelength, the stronger are the thermal effects.

- Wavelength affects absorption and threshold fluence. The etch depth per pulse (lower absorption coefficient) is larger for a weaker absorber than for a stronger absorber.

- The formation and expansion of the plasma plume during the laser pulse characterize the rapid etching process. The etch depth per pulse increases with energy fluence until the phenomenon of saturation is reached. "Saturation" is a mechanism involving the blocking of the trailing part of the laser pulse by both the plume and the excited polymer species generated by the leading part of the pulse. This occurs only at high energy densities and prevents additional material removal.

- The relaxation rate, the period of time in which the excited state of the polymer endures, affects the absorption of the laser light by the material. If the relaxation rate is too slow compared to the excitation rate, the bleaching or blocking effect occurs and reduces the absorption of laser energy.

- Ablation is accompanied by an acoustic signal that decreases with increasing laser wavelength.

- Ablation creates numerous products, including monomers, low-molecular-weight products, and fragments normal to the surface. The velocities of ablation products are high, in the range 101 to 101 m/s.

- Ablation takes place in the temperature range 400 to 800C (localized).

- The small absorption depth coupled with short laser pulses and low thermal conductivity of polymers restricts the extent of heat transfer, leading to precise material removal and a small heat-affected zone (HAZ).

4.3. Nd-YAG Laser Ablation of 30-40 μ m Diameter Microvias in RXP-4

The Nd-YAG laser used for this research was a Model 5210 from Electro Scientific Industries (ESI) operating at 355nm and power levels of 0.3-1.0W with pulse repetition rate range of 5-10 kHz. A schematic of the laser ablation system is shown in Figure 4.10, illustrating the laser source, and laser beam/substrate stage motion to achieve point-to-point ablation across the large RXP-1 substrate (300mm x 450mm). Nd-YAG laser ablation at 355nm occurs primarily through photo-thermal ablation mechanism, especially for metals. The ablation threshold of copper has been reported anywhere from 1 J/cm² for thin films to 3J/cm² for bulk copper at UV wavelengths. Since the energy fluence (energy density at dielectric surface) for 1-3W of laser power and 5-10 kHz repetition rate equals approximately 3-10 J/cm², the copper pad under the via, also called the landing pad, will get ablated while ablating the blind microvia.

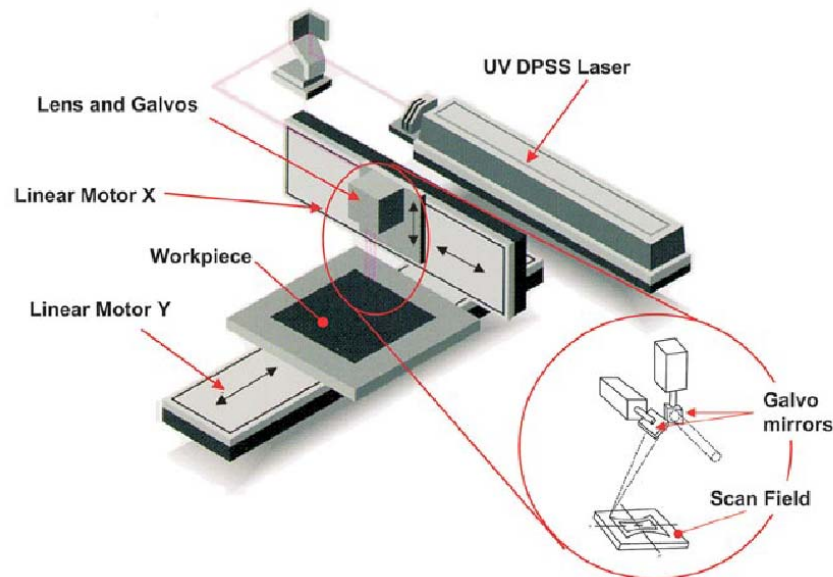


Figure 4.10 Typical Configuration of a Nd-YAG UV Laser for Point to Point Ablation³⁴

This effect is usually minimized by a two step drilling process as shown in Figure 4.11, in which the first step happens at a higher fluence to drill through a majority of the dielectric thickness, and the second step is done at a much lower fluence to be able to stop precisely on the copper landing pad without ablating too much copper from the pad.

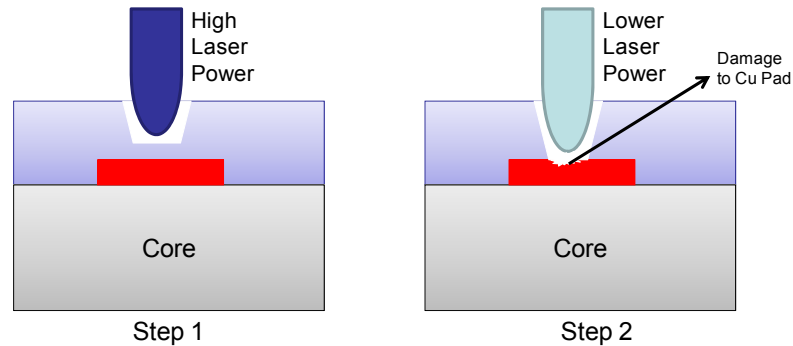


Figure 4.11 Two Step UV Laser Ablation Process to Improve Throughput for Dielectric Ablation and Precise Stopping on Copper Landing Pad

The results from Nd-YAG laser ablation of thin film RXP-4 low loss dielectric are discussed in the following section. The RXP-4 dielectric film thickness prior to lamination was around 18-20 μm and the copper pad under the dielectric was 8 μm thick with a tolerance of +/- 1-2 μm across the 150mm x 150mm substrate. The via depth in this case was the thickness of dielectric above the copper pad, and this was measured by micro-sectioning to be approximately 10 μm . The ultra-thin dielectric, consistent with semiconductor and package substrate roadmaps for 2010-2015, poses a significant challenge for Nd-YAG laser via ablation.

The two step process shown in Figure 4.11 cannot be optimized easily due to the very short travel depth of the laser beam below the dielectric surface before the copper pad surface is reached. Also, the thin and small (50 μm for 100 μm via pitch) copper pad has limited thermal diffusivity compared to thicker and larger landing pads, and is easily ablated with a high etch rate. Figure 4.12 illustrates the micro-section of a 40 μm microvia resulting from laser ablation at 1W power setting necessary for reasonable throughput ablation in volume manufacturing. The micro-sectioning was done after electroless and electrolytic copper plating of the vias. It can be seen that the laser beam, after ablating through the thin RXP-4 polymer dielectric, has ablated through most of the thickness of the copper landing pad. As seen in the figure, this structure can lead to potential yield loss due to difficulty in metallization.

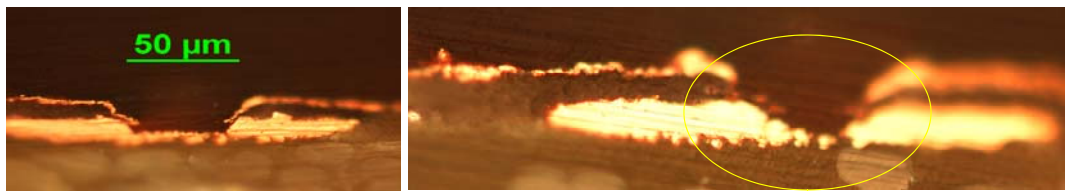


Figure 4.12 Damage to 8 μm thick copper landing pad with 1W power setting for UV laser ablation of 18 μm thick RXP-4 low loss dielectric (10 μm dielectric via depth)

To reduce the damage to the copper pads, the power was reduced to <0.5W and the ablated vias at this slower etch rate had good shape consistency and minimum “mouse bites” in the copper landing pad.

Figure 4.13 is the top view of a series of 30 μ m diameter microvias as observed in high resolution optical microscopy. The pictures with focus on the top surface and bottom surface of the vias at 500x magnification show the diameter of 32 μ m at the top and 20 μ m at the bottom of the via, with via depth of 10 μ m and wall angle of approximately 61 $^\circ$.

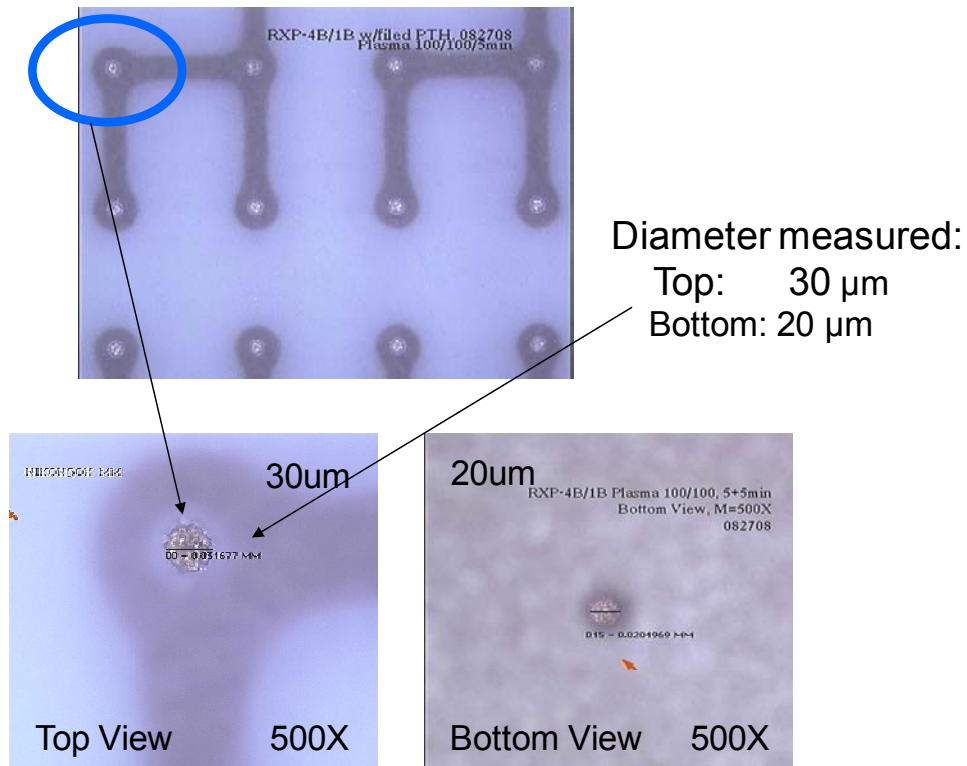


Figure 4.13 Optimized 30 μ m Top Diameter Microvias in RXP-4 by UV Laser Ablation at low power (<0.5W)

After an RF plasma cleaning step using a CF₄-O₂ gas mixture, any residues from the laser ablation were cleaned, followed by electroless copper seed layer deposition and electrolytic plating to build-up the final copper thickness. The top view and microsection of small microvias in RXP-4 low loss ceramic filled polymer dielectric indicate excellent microvia quality (Figure 4.14).

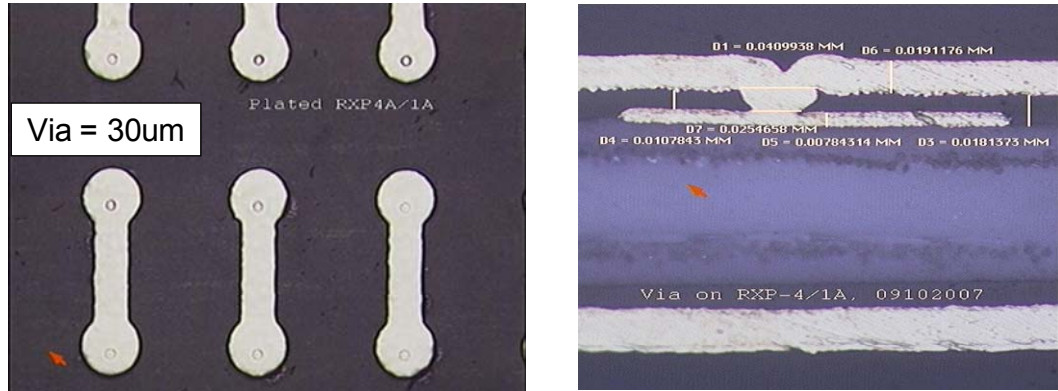


Figure 4.14 Top View of a 30 μ m Microvias in RXP-4 after Metallization (left) and Microsection Picture of Plated Microvia with Top Diameter of 40 μ m.

Inspection of the 30 μ m microvias across the entire large substrate indicated some variations in the etch depth and some microvias with residual polymer at the bottom of the via. This variability is caused by the thin film dielectric and difficulty in maintaining a tight process window across large substrate area. The fundamental limitations explained above could be a potential technical barrier for Nd-YAG lasers to shrink via diameters below 25 μ m, and more importantly ablate ultra-thin dielectric films (10 μ m) with copper pads of 5 μ m thickness. The next section focuses on the excimer laser ablation process to overcome these barriers.

4.4. Excimer Laser Ablation System and Process Fundamentals

Excimer lasers are ideally suited for mask projection ablation due to its low coherence and large size beams. Typical output from the laser source is a rectangular beam of roughly 25mm x 10mm. The beam is then shaped and homogenized using a set of optics.

For this research, a new scanning projection (1:1) via ablation/resist lithography system using a 50W Lumonics PM848 excimer laser source was used (Figure 4.15). The model was 2150SXE from Anvik Corporation, New York. The excimer laser was filled with XeCl with a characteristic emission wavelength of 308nm.



Figure 4.15 Scanning Projection Lithography/Ablation System with a 308nm Excimer Laser

There are several advantages to using 308nm wavelength. Most polymer dielectrics absorb strongly at this frequency, and hence high etch rates can be expected. Also, the wavelength is long enough to not damage optical components and ceramic dielectric coatings, providing longer life time for the expensive optics. The XeCl excimer laser is also a very stable system with prolonged gas lifetimes, thus reducing the number of gas changes required in production environments.

One of the challenges at 308nm as opposed to 351nm is the fact that mylar has a high ablation rate, and this eliminates the use of lowest cost mylar phototools. Expensive dielectric masks have been traditionally used in the past with 308nm excimer laser tools for lithography and other thin film applications. In this research, much lower cost aluminum on quartz phototools were optimized for use at 308nm. Aluminum also ablates at this wavelength in ultra-thin film form, but when the Al thickness exceeds 2 μ m, the thermal diffusivity of the metallic layer is sufficient to minimize heating related effects that cause damage to the Al. The Al on quartz photo-tools with 2-3 μ m Al thickness were successfully used for millions of pulses without any visible damage to even the finest features of sub-10 μ m dimensions.

A schematic of the major components in the via ablation system is shown in Figure 4.16. The XeCl excimer laser also has a constant energy mode known as StabiLASETM which maintains constant energy output from the laser by increasing the applied voltage from 27kV to a maximum of 33kV as the gas degrades. The maximum rated energy coming out of the laser was 250mJ although prolonged runs could only sustain ~225mJ of energy. The pulse repetition rate of the output could be adjusted up to a maximum of 200 Hz.

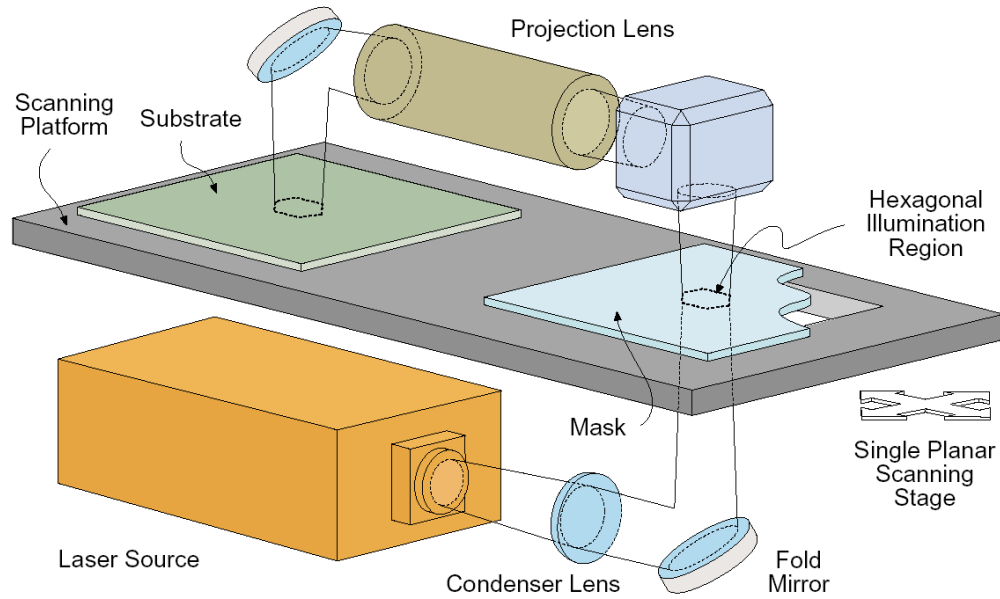


Figure 4.16 Schematic of the various components of the Anvik 2150 SXE Excimer Laser Lithography/Ablation System at Georgia Tech PRC³⁵

The laser beam is shaped with multiple optical elements into a hexagon, and then a fold mirror turns the beam upwards to hit the bottom surface of the mask loaded onto the stage. It was estimated that due to optical loss, only about 150 mJ of energy was incident on the mask plane. There are two modes in the system, one for photoresist lithography at lower fluences with a hexagonal beam with 50mm diameter, and via ablation mode with the highest energy fluence and a hexagonal beam diameter of 8.8mm. After the beam scans the images on the mask (open areas allow laser radiation to pass through), it is turned by a fold mirror and projected through a multi-element lens, followed by downward reflection onto the substrate using another fold mirror. It was estimated that the total energy loss from the laser to the substrate surface was approximately 50%, resulting in an incident energy maximum of ~125mJ.

The area of the hexagon in ablation mode is given by $3\sqrt{3}/2*t^2$ (t = length of the side = 4.4mm) and works out to $\sim 0.5\text{cm}^2$. Based on this focused incident beam size, the energy fluence at the substrate surface for a 250mJ output at the laser was calculated to be 200-250mJ/cm². This fluence is well above the threshold for most polymer dielectric films and is conducive to highly precise and near-100% photo-chemical ablation of microvias and patterns that can be transferred from the quartz mask onto substrates up to 350mm x 350mm (in the Georgia Tech PRC laser system).

The substrate and mask are loaded onto the same stage with fixed relative position, this minimizes the overlay and alignment errors caused by independently moving the mask and substrate. The area of the 350mm substrate/mask is covered by a seamless scanning technique illustrated in Figure 4.17. The three hexagons represent three successive scans along the X axis as indicated by the arrows on the left. The y-movement after each scan is also shown and the step is given by $w = 1.5 l_h$, where l_h is the hexagon side length. In scan 1, the region swept by the rectangular portion b-g-h-c of the hexagon is not overlapped by any portion of scan 2. However, the region swept by the triangular portion a-b-c in scan 1 is re-swept by the triangular portion d-e-f of the hexagon in scan 2. When the doses from the triangular segments are integrated, the cumulative dose anywhere in the overlapping region is the same as in the non-overlapping regions, thus producing a seamless uniform illumination across the entire substrate.

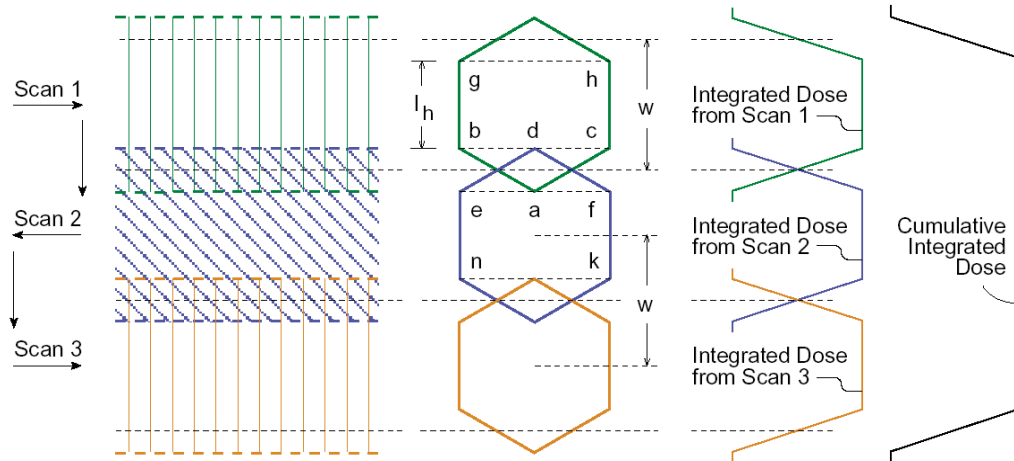


Figure 4.17 Illustration of the seamless scanning technique used in the Anvik 2150 SXE Excimer laser system³⁵

A unique feature of the laser ablation system was the debris removal system (DRS) to assist in removal of ablation debris away from the ablation region. Figure 4.18 shows a drawing of the DRS which consists of two nozzles in close proximity to each other on either side of the hexagonal laser beam and very close to the substrate surface. Helium gas is injected from one nozzle at a typical angle of 45° and vacuum is applied to the other nozzle also at a 45° angle. This configuration creates a sweeping flow of He (lightest gas other than hydrogen) across and just above the ablation site on the substrate which picks up most of the ablation ejectiles and delivers them into the vacuum system for removal away from the substrate. Since this system is fixed to the laser beam delivery frame, it is always active at the same position relative to the beam during ablation across the entire substrate.

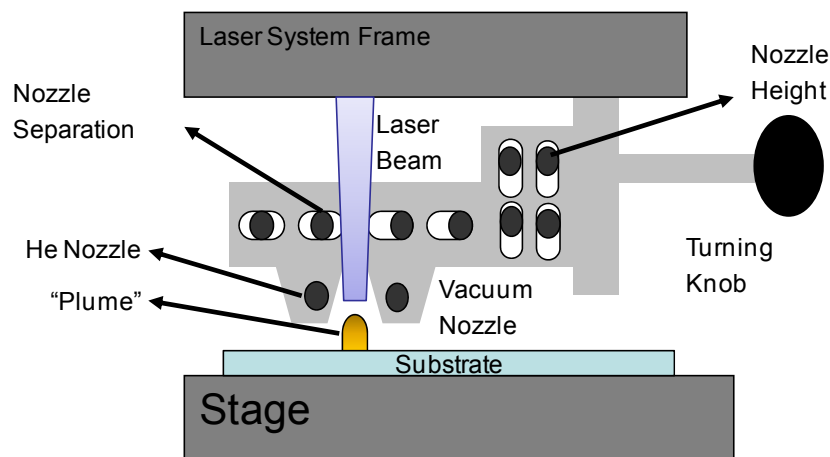


Figure 4.18 Debris Removal System (DRS) using He & Vac to Remove Ablation Debris

4.5. Chemistry and Physics of Polymer Ablation by nanosecond pulsed 308nm excimer lasers

When the nanosecond pulse of the excimer laser strikes the surface of the polymer (LCP or BCB in this case), a loud audible report is heard and, depending upon the wavelength, 0.01-0.1 μm of the material is etched away with a geometry that is defined by the light beam. The depth etched is a linear function of the number of pulses. The main advantage of using the XeCl excimer laser at 308nm is the fact that the photon energy at this wavelength is 4.02eV, which is above the bond energy for C-C bonds (3.59eV), C-O bonds (3.64eV), and close to that of carbonyls (C=O, 4.2eV @ 295nm)³⁵. The 308nm photon energy is also much higher than the bond energy of N-N (1.65eV) which is one of the main functional groups in many commercial photoresists and also in triazine polymers. As described in the earlier section on polymer chemistry, both LCP and BCB contain C-C, C-O and carbonyl groups and when the 308nm excimer laser energy (above the threshold fluence) strikes these polymers, the bond breaking follows along the above mentioned groups with bond energies lower than or close to 4.02eV.

Figure 4.19 shows potential bond breaking sites and low molecular weight groups that are formed as by-products.

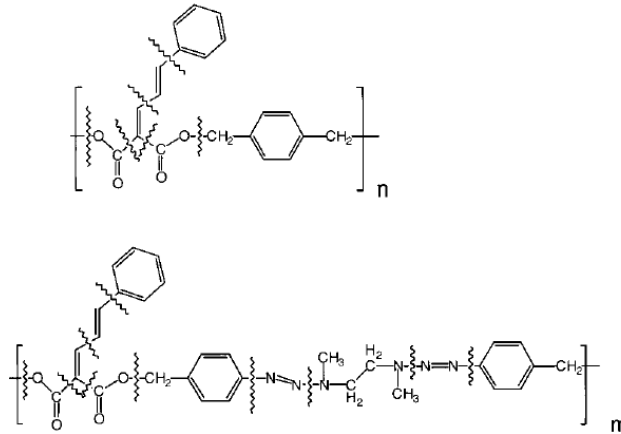


Figure 4.19 Potential Bond Breaking Sites for Typical Polymers During 308nm Laser “Photo-chemical” Ablation³⁶

The reaction which is termed 'ablative photodecomposition' results in the break up of the polymer chains to oligomers of much lower molecular weight along with the production of gases such as C₂, CO, CO₂, and small amount of monomers. The gaseous products are ejected from the surface (usually normal to the surface) at supersonic velocities and carry the solid particles of the polymer along. This chemical phenomenon along with the He flow and vacuum from the debris removal system in the Anvik 2150SXE laser system contributes to the elimination of most ablation products from the substrate surface, and in case of dielectric films below a certain thickness, it becomes possible to have a “clean” process without the need for any plasma or other post-laser cleaning step prior to metallization.

4.6. Excimer Laser Ablation of 25-50 μm Diameter Microvias in LCP

The first step in the research on excimer laser ablation of 25 μm and 50 μm thick LCP films was to characterize the threshold fluence and etch rate or ablation depth vs. energy fluence. This was done using stationary ablation mode, where the hexagonal beam was exposed on the substrate without any mask pattern, and LCP in the entire hexagon area was ablated at various energy densities and steps of number of pulses. The etch rate study was conducted on the 50 μm thick LCP film using a higher power laser system, Model 3000-308 XeCl excimer laser from Lambda Physik (Gottingen, Germany) operating at 308nm, with maximum energy output of $\sim 600\text{mJ}$, maximum repetition rate of 300Hz, and average power of 150W, much higher than the Lumonics laser at GT PRC. For the ablation rate study, all ablation was done in air atmosphere, with a low pulse repetition rate of 20Hz. Figure 4.20 summarizes the results of ablation depth vs. ablation dose in graphical format for various energy fluences adjusted at the laser source. The etch depths were measured using a Veeco Dektak surface profilometer.

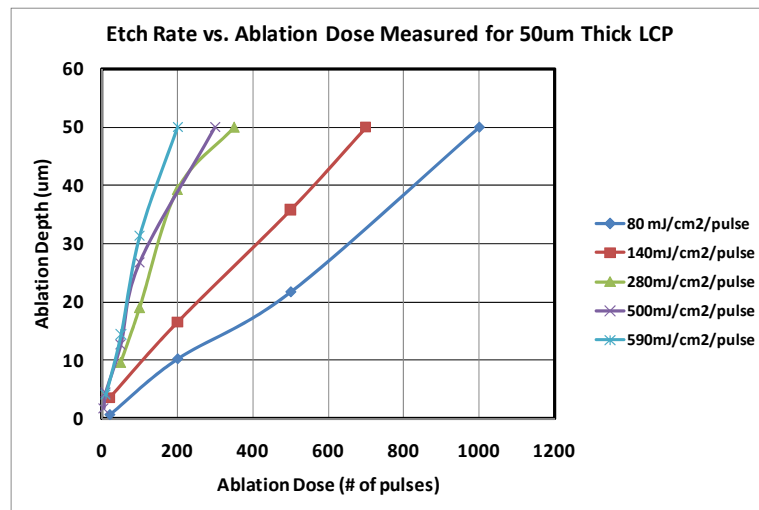


Figure 4.20 Ablation Depth vs. Dose for Various Fluences for LCP

The etch rates were extracted from the data shown in Figure 4.20 and the etch rate vs. fluence for LCP is plotted in Figure 4.21.

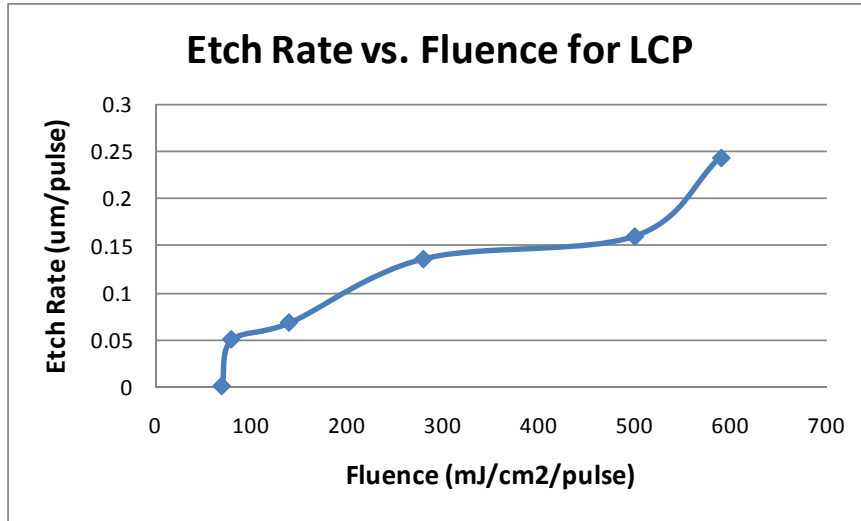


Figure 4.21 Etch Rate vs. Fluence for LCP (threshold around 70 mJ/cm²)

Consistent with reported literature for other polyesters, the ablation rate at low fluences just above the threshold fluence for LCP also showed an exponential dependence on the fluence, with deviations from the trendline appearing at higher fluence of 500mJ/cm²/pulse which is well above the threshold. The ablation of polymers is a function of the absorption of that polymer at the wavelength of incident radiation and can be derived experimentally from etch rate vs. fluence measurements. The equation relating ablation rate (L - μm/pulse) and fluence (F) is given by:

$$L \text{ (depth/pulse)} = \alpha^{-1} \ln (F/F_0)$$

where F_0 is the threshold fluence at which ablation is first observed. Figure 4.22 shows the same data from Figure 4.21 replotted as natural logarithmic values of F/F_0 with linear curve fitting.

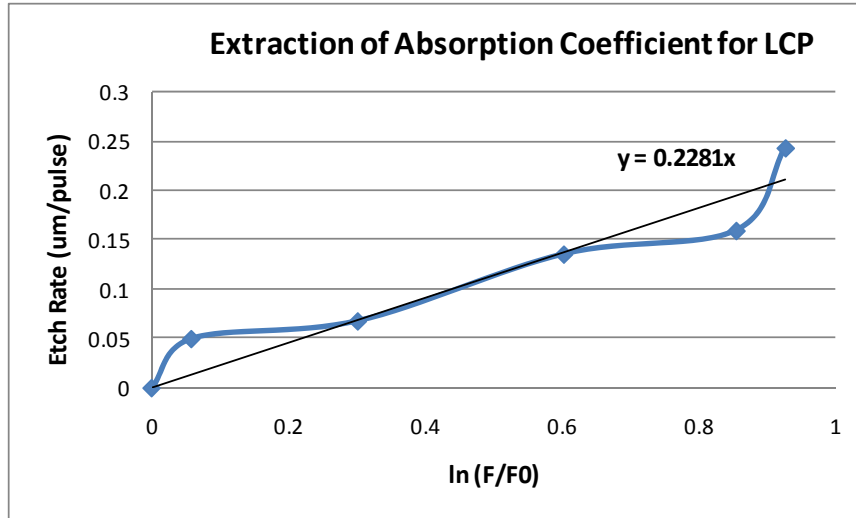


Figure 4.22 Extraction of Linear Absorption Coefficient from Etch Rates for LCP

The threshold was extrapolated to be the intercept where the etch rate approaches zero, and this value was calculated from the measured etch rates to be $\sim 70 \text{ mJ/cm}^2$. The slope of the curve was calculated as 0.2281 (for threshold of 70 mJ/cm^2), which results in experimentally derived absorption (α) for LCP of 4.4×10^4 at 308nm. This is consistent with the absorption of closely related polyesters reported to be around 5.1×10^4 in the literature.³⁷

The threshold fluence for LCP is a critical factor in being able to form small vias and other structuring in the micron range of dimensions. This is enabled mainly by the two unique characteristics of excimer laser ablation, (i) the precise and highly controlled depth etching, and (ii) lack of any thermal damage on the substrate. It has been established through numerous scientific studies in the past 20 years that an absorption of roughly 4000 cm^{-1} is essential for “neat” photo-chemical ablation.

Below the threshold fluence, significant etch rates could not be observed, and several thousand pulses were exposed at high repetition rate to measure the etch rate. However, there were significant thermal effects at these values below the threshold fluence through a process termed “incubation” in the literature, and damage to the LCP surface was noticed.

4.6.1. Excimer Laser (308nm) Ablation of 25 μ m Thick LCP Film

A series of experiments were designed to explore the excimer laser ablation of 25 μ m LCP films with thin copper foil laminated on both sides of the dielectric. The copper foil thickness available was 18 μ m and this was reduced to 9 μ m by chemical etch based thinning process which was optimized to achieve a tolerance of +/-2 μ m. The LCP film was flexible and the depth of field (focus) for the laser imaging system with 1:1 projection from a quartz mask was in the order of 150 μ m for feature sizes below 25 μ m. This was calculated based on a numerical aperture of 0.025 ($f/20$) for the projection lens used. This posed a potential problem for achieving consistent via ablation across large LCP flex film in the current setup.

A roll-to-roll handling system (available with most commercial laser tools) is required to hold the film in tension to prevent z-axis variance in the LCP surface position. It was decided to replace the projection imaging from a quartz mask with a conformal copper mask process creating the via openings in the thin copper foil laminated to the LCP. This changed the exposure mode to contact imaging, thus eliminating any depth of focus related variability.

For 9 μm thick copper, a spray etching process was developed to open circular via windows down to 25 μm diameter prior to ablation. For initial process establishment, a stationary ablation mode was used without any scanning motion of the substrate and mask stage. A cross-section of the as-etched LCP film prior to ablation is shown in Figure 4.23 which also shows a 62.5 μm microvia after ablation through the copper window.

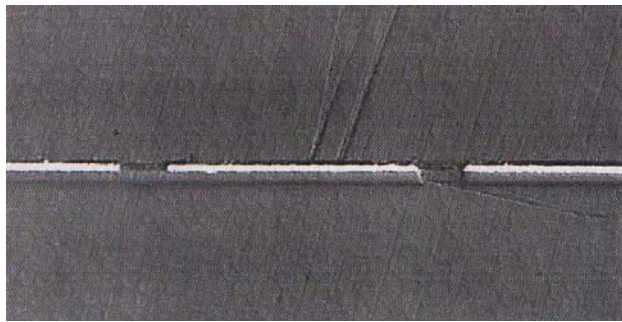


Figure 4.23 Copper Window Etched in Foil on LCP (left) and Via after Ablation through 62.5 μm diameter copper window (right) in 25 μm LCP film

Based on the etch rate data, and considering the high throughput requirements for high volume substrate processes, 200mJ energy level from the laser (close to the maximum fluence of the Anvik 2150SXE system at GT PRC) was selected for the scanning ablation experiments on 25 μm thick LCP dielectric. The equations to calculate the scan speed and relationship to the # of pulses, repetition rate and other parameters are shown in the following equations.

$$N = \# \text{Pulses / Pixel} = \frac{\sqrt{3}}{2} \cdot \frac{d_n R}{v_s}$$

$$N_{Exp} = \# \text{Pulses / Pixel(Exposure)} = \frac{\sqrt{3}}{2} \cdot \frac{50(\text{mm}) \cdot R(\text{Hz})}{v_s(\text{mm/min}) \cdot \frac{1}{60}(\text{min/sec})} = 2598 \cdot \frac{R(\text{Hz})}{v_s(\text{mm/min})} \quad \text{Exp mode}$$

$$N_{Abl} = \# \text{Pulses / Pixel(Ablation)} = \frac{\sqrt{3}}{2} \cdot \frac{8.8(\text{mm}) \cdot R(\text{Hz})}{v_s(\text{mm/min}) \cdot \frac{1}{60}(\text{min/sec})} = 457 \cdot \frac{R(\text{Hz})}{v_s(\text{mm/min})} \quad \text{Ablat. mode.}$$

where,

N (and N_{Exp} , N_{Abl}) are the dose or # of pulses required to ablate the entire film thickness,

v_s is the stage scan speed (Y scan rate), and R is the pulse repetition rate.

For the ablation of 25 μm thick LCP dielectric, N_{Abl} was selected to be 400, based on an etch rate @ 200mJ/cm² of 0.6-0.7 μm per pulse and an additional dose to ensure complete ablation of the film thickness over the large area substrate including any film thickness variations. For various repetition rates, the calculated values of v_s are shown in Table 4.1.

Table 4.1 Calculated Values of Y Scan Feed Rate (v_s) for Various Repetition Rates (R in Hz) for a Dose (N_{Abl}) of 500 pulses @ 200mJ/cm²/pulse

Repetition Rate (Hz)	Y Scan Rate (mm/min)
100	91.4
150	137.1
200	182.8

4.6.2. Discussion of 25-50 μm Microvia Ablation in 25 μm Thick LCP Film

A test structure with three via diameters, 25 μm , 37.5 μm , and 50 μm was used to evaluate the aspect ratio limits of the excimer laser ablation process. Additional structures for layer to layer alignment were included that were of the order of 1-1.5mm in size with 150 to 300 μm width. The process flow consisted of etching of the three via diameter patterns in the copper foil bonded to the LCP dielectric, followed by excimer laser scanning ablation and finally oxygen plasma cleaning to remove any by-product residues from the ablation. Finally, the vias were metalized by electroless copper seed layer plating and electrolytic plating to build up the final copper thickness.

Figure 4.24 is a top view micrograph of the large alignment structure after ablation at 200mJ/cm² and 200Hz repetition rate with 500 pulses.

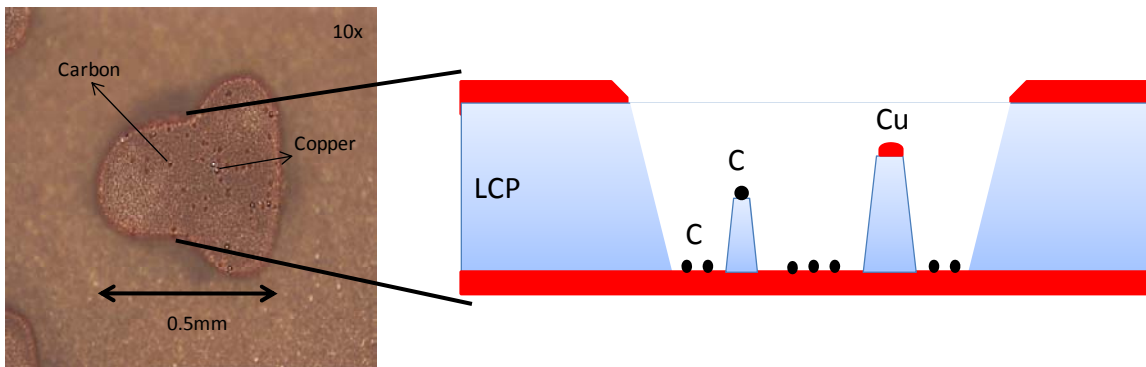


Figure 4.24 Top View of Ablated Feature (left) and Cross-section Schematic Illustrating Stalagmitic Cone Structures on the Floor of the Via Due to C and Cu Re-deposition

Stalagmitic cone structures were observed as shown in the photograph and schematic cross-section. Formation of such structures during excimer laser ablation at low fluences has been reported in literature³⁸.

However, some of the published data attributed this to impurities in the polymer that had high ablation thresholds and could not be removed, thus acting as a temporary “mask” for the polymer under these impurities. In comprehensive studies by Lippert et al. on polyimide ablation 308nm, nanosecond time-of-flight measurements confirmed the presence of fullerenes in the carbon clusters, which were a result of complete fragmentation to C_1 , C_2 , and C_3 fragments³⁹. In this research, it was observed that two types of debris were re-deposited midway through the ablation process causing a similar blocking effect. As confirmed by energy dispersive spectroscopy (EDS), the particles seen in Figure 4.24 were either carbonaceous (black spots) or copper (bright circular spots). Carbonaceous residue can also be seen on the base of the ablated feature. It is postulated that the carbonaceous particles forming the “cones” are larger by-products of the polymer bond breaking mechanism that could not be picked up and removed by the DRS and so re-deposited on the surface. The copper re-deposition has an interesting source as shown in Figure 4.25.

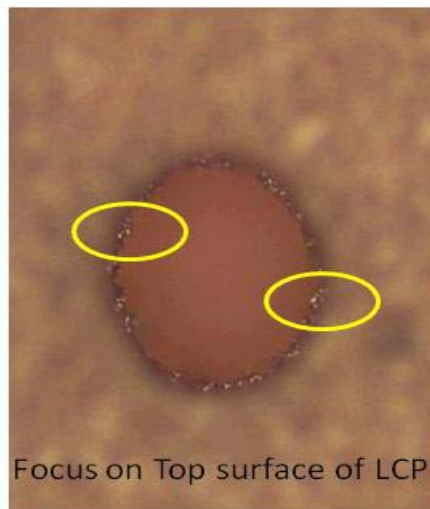


Figure 4.25 Top View of the Etched Copper Window at the Cu-LCP Interface

During the etching of the copper windows in the top copper foil, very small “overhangs” of copper could be seen at the inside edges of the via openings (seen as bright spots highlighted in the figure). Although bulk copper has a high ablation threshold much above the energy fluence used, it has been reported during studies of thin film Cu for use as a photo-mask pattern, that the damage threshold for copper reduce significantly into the mJ/cm^2 range of fluence when the film thickness approaches $1\text{-}2\mu\text{m}$ or lower. It is possible that the slivers of copper at the edge of the via openings in this case got dislodged due to localized thermal damage and re-deposited inside the via during polymer ablation and the particles of copper are large enough (few microns) to be above the ablation damage threshold for copper. To confirm this, an additional process step to microetch the copper windows prior to ablation was introduced. This resulted in etching of the copper slivers and smoothing of the copper windows and the ablated feature did not show any copper based cone structures at the same ablation conditions as before. A micrograph of the resulting feature is shown in Figure 4.26.

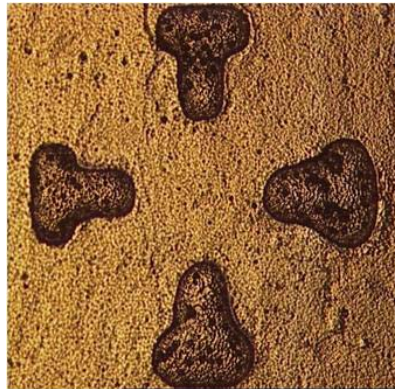


Figure 4.26 Top View of the Ablated Alignment Feature after Smoothing of the Copper Windows, Carbon re-deposition and cone formation can still be observed

To address the issue of carbonaceous re-deposits and cones of LCP formed as a result, an experiment was conducted to combine oxygen plasma cleaning (13.56MHz RF power 300W, 100 sccm O₂, 40-50mTorr vacuum under gas flow, 80°C, 10 minutes) with the laser ablation process. After the 500 pulse ablation step, the oxygen plasma cleaning was done and as seen in Figure 4.27 (left), the carbon on top of the cones as well as the via bottom copper pad were successfully removed. The sample was subjected to additional laser ablation for 250 pulses at 200 mJ/cm² and 200Hz repetition rate. The cones of LCP under the C residues were successfully ablated as shown in Figure 4.27 (right) where the Cu re-deposits can still be seen.



Figure 4.27 Carbon re-deposits removed by O₂ plasma clean (left) and after subsequent ablation (right)

An interesting photograph of the cone structures is shown in Figure 4.28 where the polymer cone is highlighted by the electroless and electroplated copper on top of and around the cone. In this sample, the additional ablation step after plasma cleaning was skipped, moving instead to the via metallization step. This confirms that the plasma cleaning process removed all the carbon residues from the cone surface and the plated copper has good adhesion to the small cone structure.

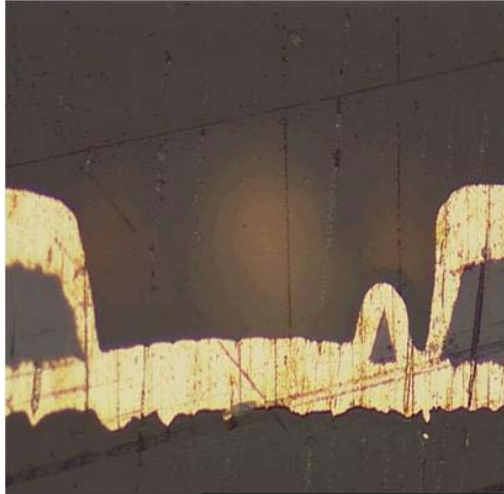


Figure 4.28 Cross-section of “Cone” structure formed during laser ablation after electroless and electrolytic copper plating

4.6.3. Effect of via size and fluence on carbon re-deposition, debris removal and cone formation

Figure 4.29 shows three different via sizes ablated using identical laser parameters, including fluence, scan speed, DRS setup.



Figure 4.29 Three Different Via Sizes Ablated at Identical Conditions showing correlation between via size and amount of cones formed

It was observed in several different samples that the density of carbon residues and cones formed decreased with decreasing via diameter. This can be attributed to the capacity of the debris removal system to sweep away the ejectile polymer fragments from the ablation site. Since the amount of ejectiles from a smaller via will be lower, it can be expected that the amount of larger fragments that cannot be removed by the DRS will also be less than those for larger features. It was also observed that the number of debris induced stalagmitic cones decreased for all via sizes when the Helium flow rate of the DRS was increased. This supports the explanation above for the via size dependence of the debris re-deposition. After optimization of the DRS nozzle angles, separation and He flow rates, the carbon debris related cone formation was eliminated for the three via sizes selected.

Once the process issues related to C and Cu re-deposition and cone formation were resolved, the vias of 25-50 μm diameter were ablated by laser scanning mode. To study the progress of via shape development during ablation, samples were microsectioned after 250, 350 and 500 pulses to compare the via shape and polymer thickness ablated. Figure 4.30 shows both top views and micro-sections, the top views are for ablating with 250 pulses, and the cross-sections were taken at the pulses indicated. As seen in the top views, there are no carbon deposits in the small microvias during ablation. This is explained by the small amount of material being removed and the capacity of the DRS system to be able to handle near-100% of the debris and ablation by-products.

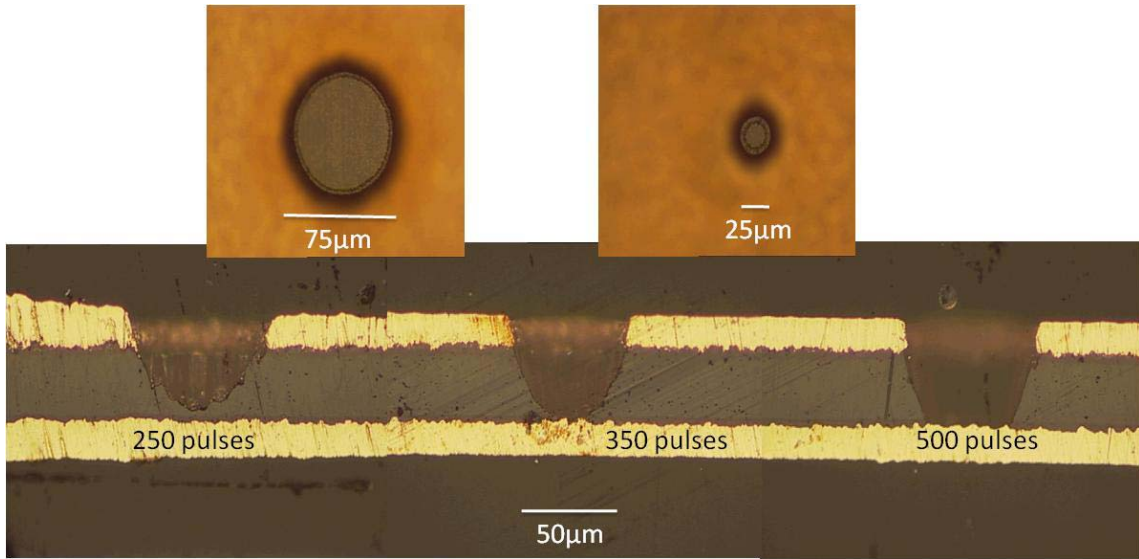


Figure 4.30 Evolution of Excimer Laser Ablation of LCP; top views after 250 pulses (top), and microsections (bottom)

The three different diameter vias at various stages of the LCP process are shown in Figure 4.31.

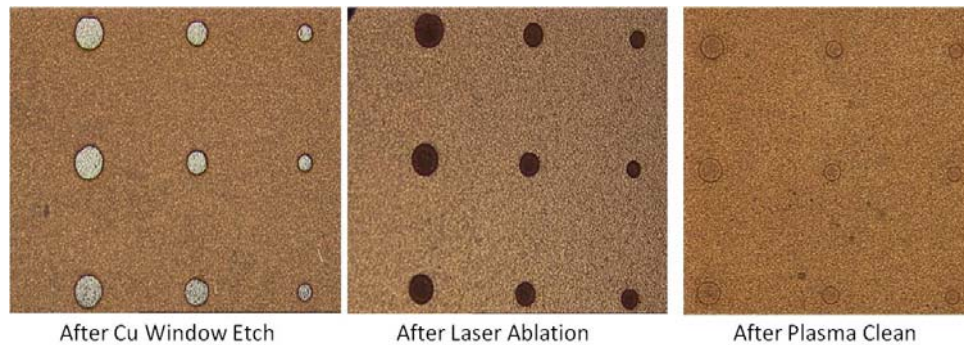


Figure 4.31 Vias of 50, 37.5 and 25µm diameter after major steps in the via formation process

The vias after etching of copper windows is shown on the left where the white colored polymer can be clearly seen through the Cu windows.

The middle photograph was taken after completion of 500 pulses. It was consistently seen that the appearance of dark black carbonaceous residues on the via bottoms was a very good indicator of 100% ablation with no LCP residual layer at the bottom of the vias. A possible reason for the inability of the DRS to remove this last thin layer of carbon debris could be the strong bonding of molten LCP at the LCP-Cu foil interface during lamination and also the LCP dielectric trapped in the crevices caused by the copper foil roughness. Finally, the picture on the right in Figure 4.31 shows the vias after an O₂ plasma clean to remove the carbonaceous residues.

The small microvias were examined by scanning electron microscopy to verify the completion of the ablation process. Figure 4.32 illustrates the top view SEM micrograph of a 50µm microvia in LCP with copper foil on both sides. The Cu window, and ablated via can be clearly seen. Also noticeable is the smooth and clean side wall of the via and transfer of very small etched imperfections in the Cu window onto the LCP. This indicates that with thinner LCP layers, the excimer laser process has the potential to achieve very small microvia diameters below 25µm.

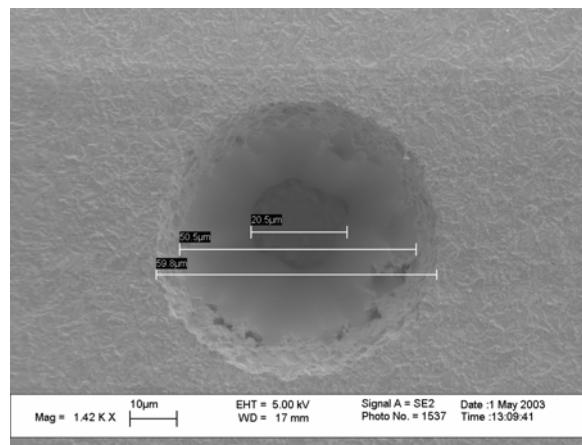


Figure 4.32 Scanning electron micrograph top view of a 50µm microvia in LCP

The three via sizes (25, 37.5 and 50 μm) were successfully demonstrated by excimer laser ablation of 25 μm thick LCP dielectric films, and the top views and microsections of the fabricated microvias after copper plating are shown in Figure 4.33.

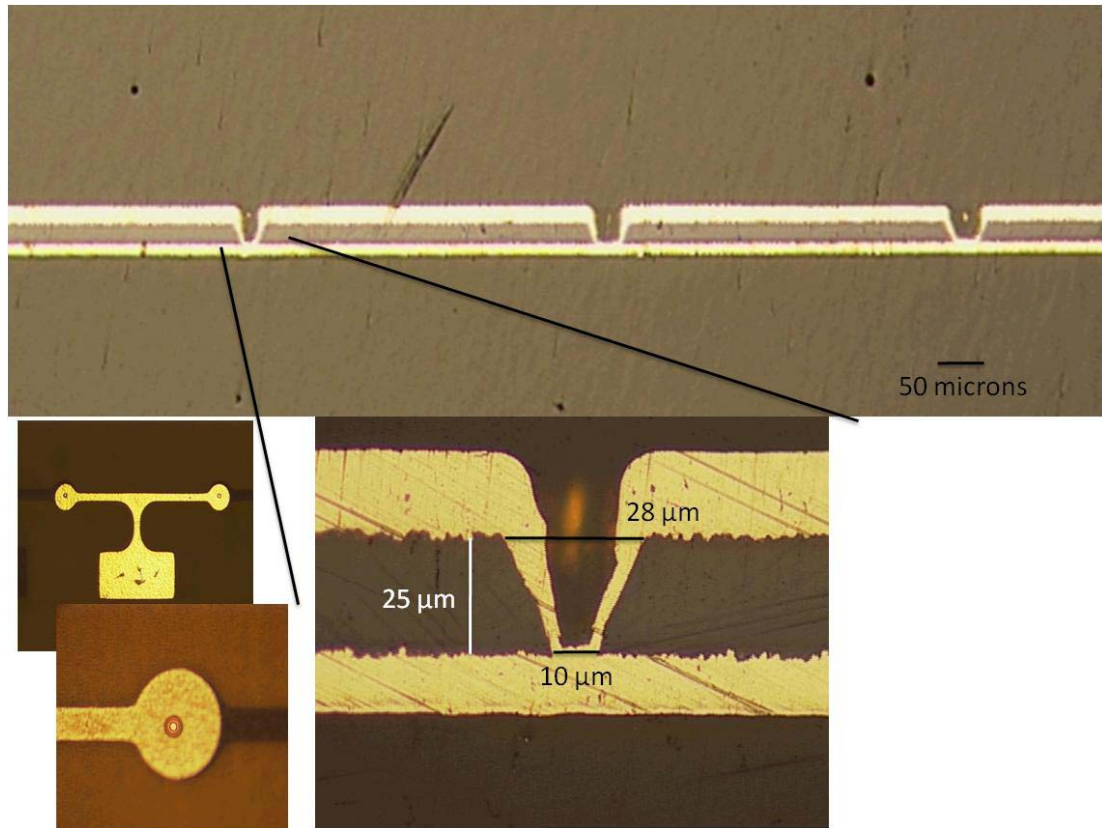


Figure 4.33 Demonstrated 25 μm , 37.5 μm , and 50 μm Excimer Laser Ablated Microvias after Electroless and Electroplating of LCP

4.7. Excimer Laser Ablation of 10-40 μm Diameter Microvias in BCB

Ultra-small microvias in BCB have been traditionally processed using photo-sensitive BCB or by reaction ion etching (RIE) of non-photosensitive BCB films. Preliminary experiments on 308nm excimer laser ablation of 50 μm and larger vias in BCB (Cyclotene 3022) for MCM-D applications has also been previously reported³⁸. The

focus of this research was to explore 308nm excimer laser ablation as a potential approach to achieving 30 μ m and smaller microvias in Cyclotene 3022-57 resin from Dow Chemical. The deposition and planarization process for BCB has been described in a previous section. Thin films of BCB (9 μ m total thickness, 5 μ m over underlying copper microvia landing pads) were deposited on three different substrates, (a) planarized C-SiC, (b) Cu-Invar-Cu metal core with PTFE laminated dielectric layers, and (c) high Tg glass reinforced organic laminates (specifically Asahi Chemical A-PPE, Hitachi Chemical MCL-E-679LD).

The Anvik 2150SXE system with 308nm XeCl excimer laser source attached to a scanning projection ablation/lithography system was used for the via formation. The test structures consisted of arrays of microvias with diameters of 40 μ m, 30 μ m, 20 μ m and 10 μ m. The discussion of polymer chemistry and laser-material interaction discussed in the previous section is also applicable to BCB ablation, since BCB also consists of phenyl groups, carbonyl groups, C-C and C=C bonds. In addition, BCB also has Si-O bonds due to the siloxane functionality in the main chain, however, the Si-O bond energy is 4.6eV which is higher than the carbon based bonds, and so it was not anticipated that the laser system used in this research would be able to break the Si-O bonds in BCB.

The UV-vis absorption spectrum for DVS-BCB has been previously reported and is shown in Figure 4.34 along with the curve for polyimide (PI2611) which is a polymer ideally suited for 308nm excimer laser ablation due to high absorption and etch rates (0.1 μ m/pulse at 100mJ/cm²).

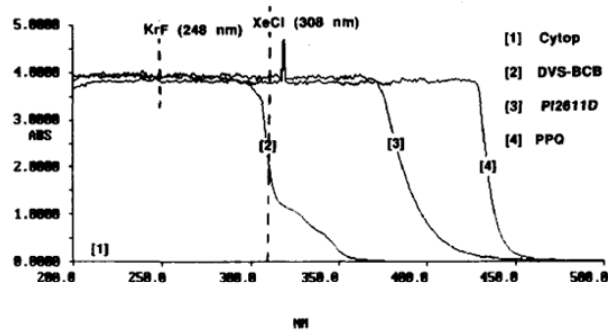


Figure 4.34 UV-vis absorption spectra for DVS-BCB compared to other common polymers used in microelectronics applications³⁸

The key observation from Figure 4.34 is that the absorption for polyimide (PI2611) at 308nm is still in the peak value region, however, for BCB, the absorption is on the downward slope at 308nm, which is the so-called “saturation” region where the light absorption in the polymer tends to dramatically decrease. Hence, the etch rate at fluences of 200mJ/cm² for BCB were expected to be lower than the etch rate established for LCP and reported previously by other groups for polyimide.

The only fluence that resulted in reasonable etch rates for BCB with the 308nm excimer laser system was 200mJ/cm²/pulse since lower fluence levels resulted in very low etch rates which were not considered feasible for manufacturing. Hence, the threshold fluence and absorption could not be established in this study for BCB. A BCB cured film thickness of 27μm was used for this set of experiments and etch depths were measured using a Veeco Dektak 30 surface profilometer. Figure 4.35 is a plot of ablation depth vs. dose (# of pulses) for Cyclotene 3022 at 200mJ/cm²/pulse fluence.

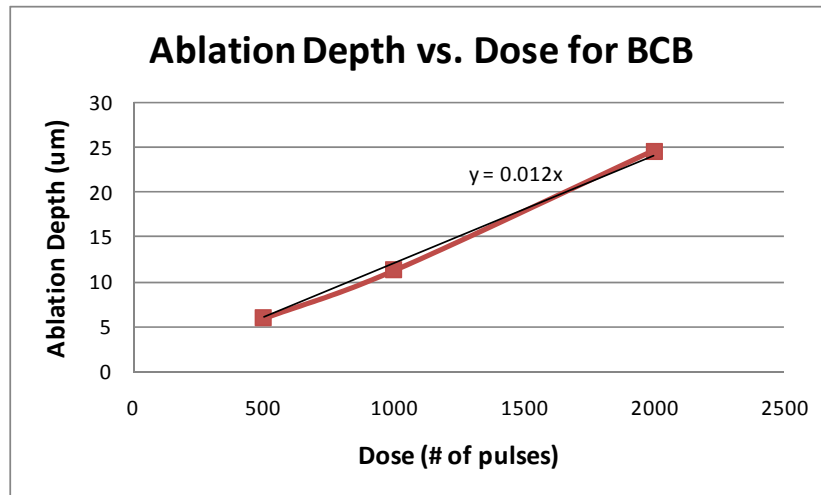


Figure 4.35 Ablation Depth vs. Dose for BCB (Cyclotene 3022) at 200mJ/cm²/pulse

The etch rate of 0.012μm/pulse at 200mJ/cm² is much lower than the etch rate measure for LCP at 200mJ/cm² of 0.08 μm/pulse, consistent with the UV absorption for these two materials at 308nm.

The cross-section of the BCB film that was optimized for ablation of small microvias consisted of total dielectric thickness of 9μm, with 4-5μm copper pad thickness for the landing pad, and 4-5μm BCB thickness above the pad (via depth). Since the BCB did not have any copper layer on top (unlike LCP with laminated copper foil), either projection ablation using a quartz mask or an alternate conformal metal mask are the main options that have been previously reported. Published work on conformal metal mask on BCB consisted of sputtering or other high cost vacuum deposition of multiple metals and atleast 2-3μm of copper to overcome the ablation damage threshold, followed by etching to define copper windows. This process has inherent cost barriers and also dimension limitations due to the etching process to define 10μm features. Hence, a new method to use a high resolution photoresist as a conformal mask for via ablation was

developed. The cross-section of the substrate structure with BCB and Eagle NT-90 negative photoresist is shown in Figure 4.36.

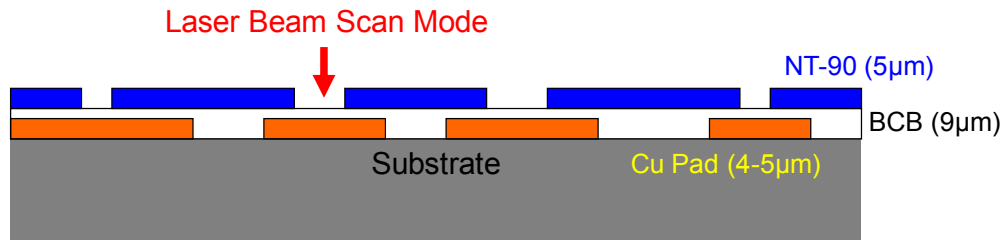


Figure 4.36 Cross-section schematic of new conformal mask method using high resolution photoresist for BCB excimer laser ablation

The Eagle NT-90 is a special photoresist tuned for high resolution i-line imaging (365nm peak wavelength) and due to the need for high spatial resolution, this and some other i-line resist polymer chemistry are tuned to have absorption bands in the 350-400nm range with steep fall-off in absorption immediately away from this band on both sides. Hence, the absorption of this type of i-line resist at 308nm wavelength is designed to be extremely low, and ideally suited for use in the current experiments as a conformal mask that does not undergo any photo-chemical ablation at 308nm. This resist was spin coated at 650rpm and bake dried at 90°C for 30 minutes to obtain a thickness of 4-5µm. The ablation characteristic (or lack thereof) at 308nm was confirmed by exposing the surface of the photoresist to the 308nm laser light at various doses. Figure 4.37 shows the surface of the Eagle NT-90 photoresist at 500, 1250 and 2000 pulses at 200mJ/cm²/pulse and 200Hz repetition rate.

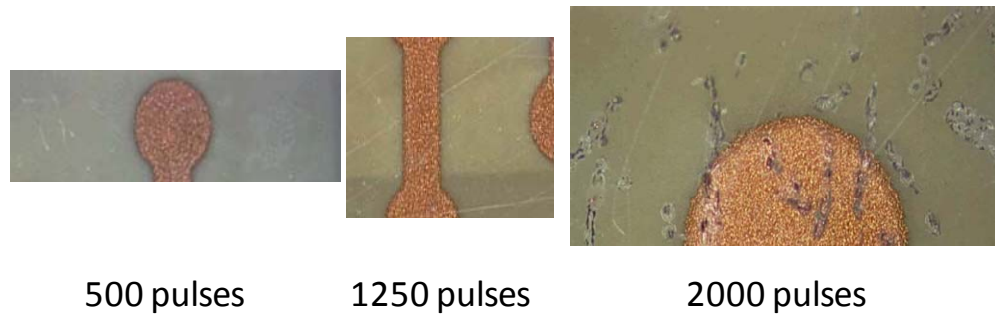


Figure 4.37 Micrographs of Top Surface of Eagle NT-90 photoresist coated on BCB (underlying Cu patterns) at various ablation doses at $200\text{mJ}/\text{cm}^2/\text{pulse}$ and 200Hz

At 500 pulses (picture at left), there was no visible effect on the photoresist, and it retained its light blue as-deposited color. At 1250 pulses (middle picture), there was a color change (yellowing) of the surface, however, the resist had no delamination or damage. When the dose was raised to 2000 pulses (picture at right), damage was seen on the photoresist surface. This is consistent with the mechanism of thermal damage in polymers during UV laser irradiation at fluences below the threshold fluence of the polymer.

The process flow for this novel and low-cost process with minimum number of process steps for laser ablation and metallization of BCB consisted of the following steps:

1. Copper pad layer patterning on substrate
2. BCB spin coating, planarization and soft cure (210°C , 1 hour)
3. NT-90 liquid photoresist spin coating and drying
4. UV imaging and spray developing of microvia windows in NT-90
5. Thermal bake to enhance photoresist adhesion to BCB and improve stability during laser ablation
6. Excimer laser scanning ablation of BCB through NT-90 conformal mask

7. One step plasma process for (a) removing NT-90, (b) cleaning via residues in BCB, and (c) surface roughening of BCB for metallization
8. Electroless copper seed layer plating and semi-additive electrolytic plating process to metalize BCB vias and define fine lines

The laser ablation parameters used for ultra-small microvia ablation in BCB were energy fluence of 200 mJ/cm²/pulse, pulse repetition rate (200 Hz), dose of 500-750 pulses translating to scan speeds of 150-200 mm/min. The depth of the ablated features was characterized by surface profilometry and the scans before and after ablation are shown in Figure 4.38, confirming the complete ablation of the BCB film thickness down to the copper pad without any surface damage to the NT-90 resist mask.

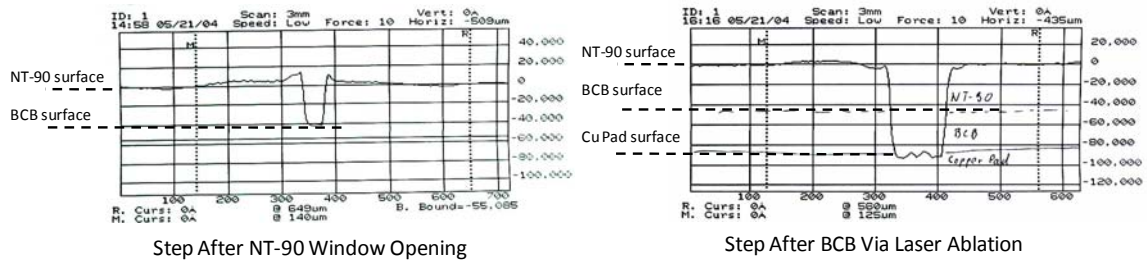


Figure 4.38 Surface profilometry scans of the NT-90/BCB/Cu structure before and after 308nm excimer laser ablation

The next major process innovation was the optimization of an integrated one-step approach to removing the NT-90 photoresist, clean any carbonaceous residues on the BCB via landing pads, and roughen the BCB surface for wet metallization. In MCM-D and wafer-level processing, the metallization process for the seed layer on BCB involved sputtering or other high-cost vacuum deposition of Cr-Cu or other metallization schemes. Special treatments in this process were required along with the adhesion or bonding

metals such as Cr or Ti to achieve acceptable Cu-to-BCB peel strength. The focus in this thesis research was on adopting low cost electroless copper plated seed layers widely available in the package substrate industry to significantly reduce the process cost of using a high performance dielectric such as BCB. A 13.56MHz RF plasma system (Plasma Etch BT-1) was used with gas mixtures optimized for BCB based on prior published literature by Dow Chemical Co. The gas mixture used for this study was CF₄-O₂ in a ratio of 0.27:0.73, with gas flow rates of 27sccm CF₄ and 73 sccm O₂ at a RF power of 300W. A series of time soaks in the plasma chamber were evaluated using the laser ablated BCB samples, and the results indicated that at times below nine minutes, the NT-90 resist (5μm thickness) was not completely removed. At times above 20 minutes, the NT-90 was removed, however, the BCB was etched down 2-3μm (total of 5μm thickness) and also the roughness on the BCB surface was excessive (>1μm average roughness). A time of 12-15 minutes was found to be the optimum condition and a successful process was demonstrated where the NT-90 was removed completely, the BCB surface was roughened to an average roughness of 0.5-1.0μm and all the carbonaceous residues were removed from the via pad, as shown in Figure 4.39.

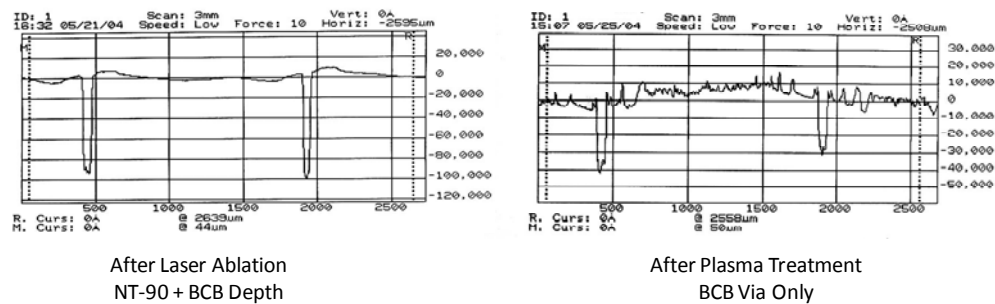


Figure 4.39 Profilometry scans of BCB Microvia after laser ablation (left) and after plasma treatment (right) showing removal of 5μm NT-90 and roughening of BCB.

Microvias as small as 15 μm diameter (or edge distance for square shapes) were achieved with consistent shape and no residual dielectric at the bottom of the via. The optimized microvias of 15 μm and 25 μm diameter in BCB are shown in Figure 4.40.

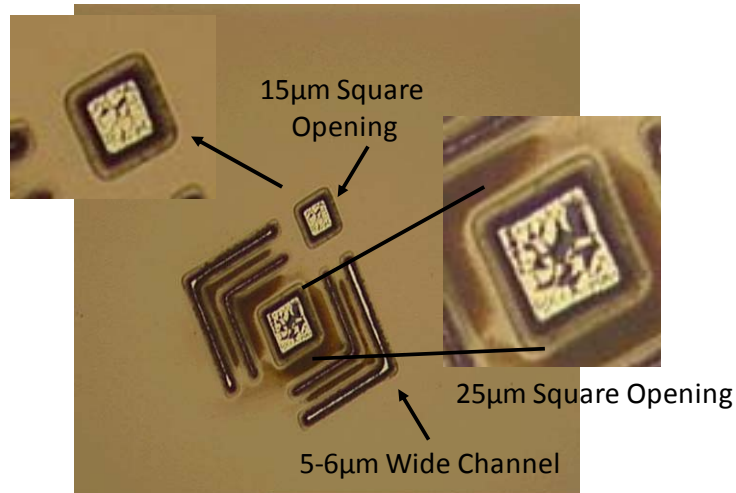


Figure 4.40 Demonstration of 15-25 μm Vias in BCB by 308nm Excimer Laser Ablation. 5-6 μm wide ablated channels can also be seen in the picture.

Unlike the cone formation and other residue problems encountered with LCP, there was no cone formation observed with the BCB. A small amount of carbonaceous residue deposited on the photoresist mask surface can be seen in the figure, and this was easily removed during photoresist stripping. There are two main differences between the LCP and BCB ablation that can explain this behavior. The film thickness of the BCB above the copper pads was much thinner than the LCP (4-5 μm BCB vs. 25 μm LCP) and also the via sizes in the BCB were smaller than those in LCP. This reduction in volume of ablated material for BCB microvias led to “debris-free” ablation similar to the behavior seen earlier for LCP with smaller via diameters.

The plasma cleaned vias and treated BCB surface was metalized with a metallic palladium activation system (Atotech Printoganth MV+ Activator) and low stress electroless copper plating (Atotech Printoganth MV+ chemistry). Electrolytic panel (subtractive etching) or pattern plating (semi-additive process) was used to build-up the final copper thickness of 5 μ m. Figure 4.41 shows the patterns ablated in BCB without using a mask, resulting in the 8.8mm hexagonal beam area being ablated at various locations on a 150mm x 150mm substrate after electroless copper metallization and annealing treatment. The adhesion of the electroless copper seed layer to BCB was confirmed by IPC standard scotch tape test method.

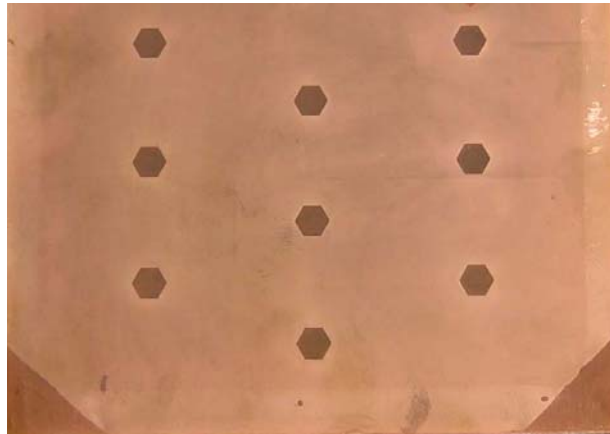


Figure 4.41 Electroless Cu plated and annealed hexagonal laser ablated areas in BCB

Figure 4.42 shows the micro-sections of a grid of vias of 20 μ m diameter (designed) with 40 μ m spacing between vias and a higher magnification image showing the top and bottom dimensions of the microvias after electroless copper seed layer metallization. For this sample, the BCB was coated on a blanket copper layer (laminated to A-PPE core) and the via depth was the same as the coating thickness of 9-10 μ m.

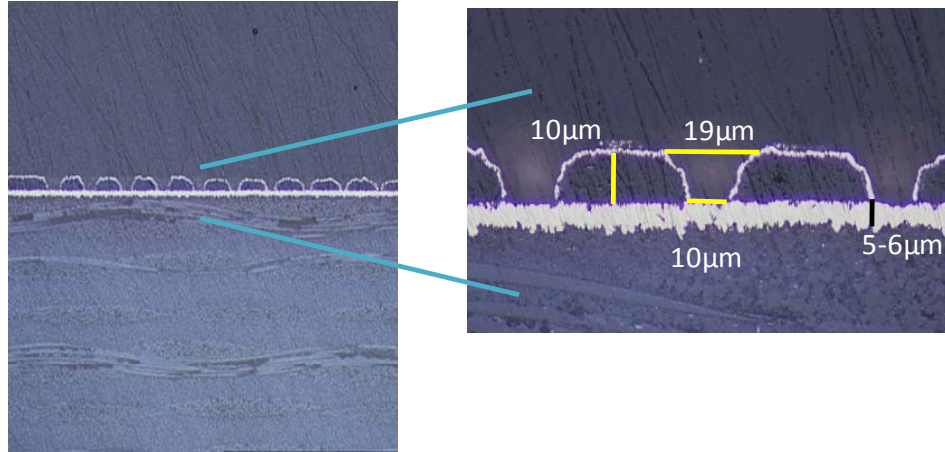


Figure 4.42 Microsections of 20µm Diameter Microvias in BCB after Electroless Cu seed layer deposition

4.8. Chapter Summary

The main objective of the research discussed in this chapter was to explore, develop and demonstrate ultra-small microvias in thin film low loss polymer dielectrics and benchmark epoxy dielectrics. A series of fundamental and experimental studies were conducted on photo-via, Nd-YAG laser, and excimer laser ablation processes, with major emphasis on highly scalable 308nm XeCl excimer laser ablation of LCP and BCB. The target via diameters of 25µm for LCP and sub-25µm for BCB were successfully demonstrated and a number of new fundamental knowledge was created along the way based on several materials and process analysis techniques.

CHAPTER 5

ADVANCED CONDUCTOR METALLIZATION AND PLASMA SURFACE

MODIFICATION PROCESSES

This chapter describes research in pushing the frontiers of ultra-fine line conductor formation processes for low-cost package substrates. The key processes addressed in this chapter are (a) plasma and chemical surface modification of low loss dielectric thin films, (b) semi-additive copper plating (electroless seed layer and electrolytic pattern plating), (c) ultra-fine line photolithography using low cost dry film and liquid photoresists, and (d) copper bond enhancement processes for reliability. All of the research described in this chapter targets sub-10 μm copper conductor widths and spacing.

Major IC and electronics systems roadmaps predict the need for sub-10 μm lines/spaces for package substrates in the next 2-5 years. The complexity of escape routing the next generation of high I/O density ICs is illustrated in Figure 5.1. The current state-of-the-art in IC substrates is around 150-200 μm I/O pad pitch for area array or depopulated area array flip-chip interconnects. Assuming an I/O pad pitch of 100 μm for next generation of high I/O count packaging, 12 μm lines/spaces would be required to escape only three rows of I/Os per signal wiring layer on the package substrate. When the pad pitch is reduced to 40 μm , line and space of 4 μm would be required for the same three row access. It is imperative to access multiple rows in each signal layer on the substrate since the layer count increase is a major factor in yield loss and higher substrate cost.

Package substrates for the next decade, whether built on an organic substrate or inorganic substrate (e.g. Si carrier) platform, will require precision and low cost processes for sub-10 μm lines/spaces.

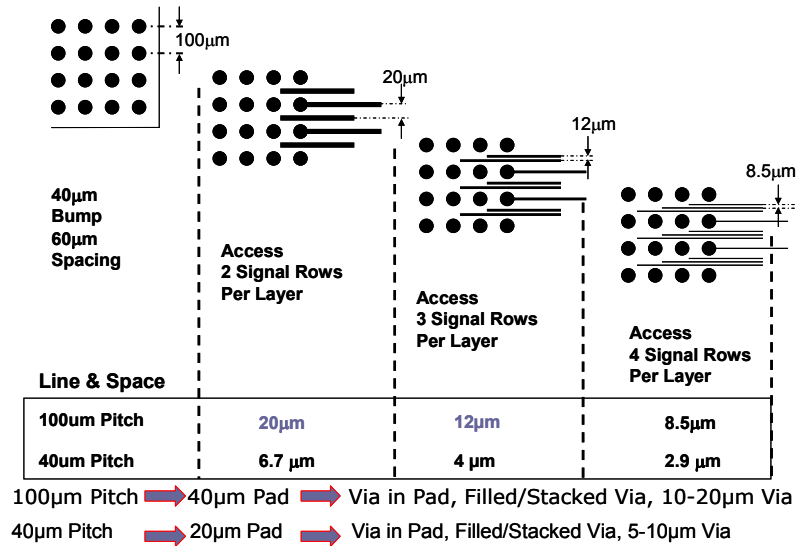


Figure 5.1 Wiring Density in terms of Lines/Spaces and Via/Pad Dimensions Required for 20-100 μm pitch area array flip-chip package substrates

5.1. Major Challenges for Ultra-Fine Line Conductors

The next major focus area of this thesis is the fabrication of ultra-fine line copper conductors (<10 μm lines/spaces) on epoxy and low loss BCB/LCP dielectrics using a low-cost package substrate compatible semi-additive process (SAP). Most of the prior work on sub-10 μm wide conductors has been on silicon wafers using semiconductor processes or on multi-chip modules (MCM-D) using high cost vacuum deposition and CMP processes. The need for low loss dielectrics for future high frequency SOP and package substrates requires new research in surface treatment processes. This is because

current industry standard chemical surface treatment processes have been designed for epoxy dielectrics and new materials like LCP, RXP-4, and adopting higher performance materials like BCB may need innovative new processes to achieve interface control for best electrical performance and thermo-mechanical reliability. The major technical challenges addressed in the conductor research to achieve the conductor geometries targeted can be seen from the following schematics (Figure 5.2) and are listed below.

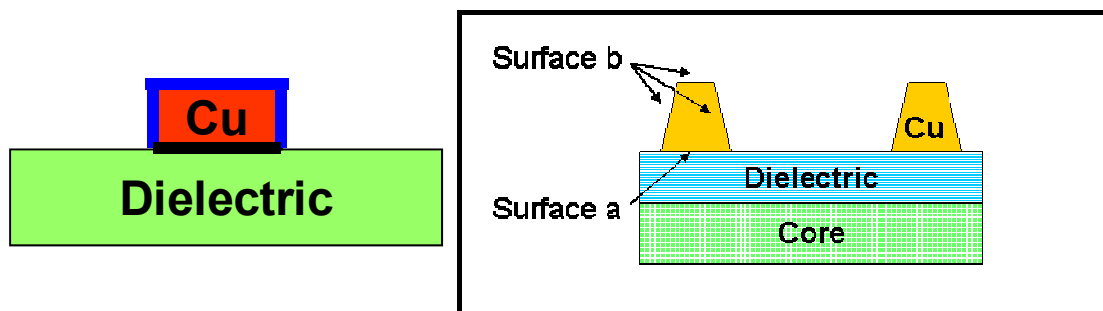


Figure 5.2 Illustration of Critical Interfaces for ultra-fine line multilayer copper wiring:
Cu-to-polymer (a) and polymer-to-Cu (b)

- Dielectric surface treatment and thin copper seed layer deposition by electroless plating and impact of seed layer thickness on achieving sub-10 μ m lines/spaces
- Photolithography and semi-additive plating process control using low-cost UV lithography tools, materials and processes compatible with package substrate manufacturing
- Reducing the interface profile of build-up dielectric to copper with sufficient adhesion and impact of surface roughness of dielectric on the fine line formation process

- Copper surface treatment of sub-10 μ m lines for polymer-to-Cu adhesion and bonding for multilayer wiring

5.2. Dielectric-Copper Interface Control for Low Conductor Loss in the multiple GHz Frequency Range

Background, Motivation and Literature Review

Multi-function package integration trends including SOP, 3D and other high density interconnect approaches continue to place demands on higher performance and lower loss at frequencies as high as 77 GHz. The increasing adoption of wireless communication in electronic and bio-electronic systems requires package substrates with very low signal loss and stable electrical performance at such high frequencies. The two main contributions to signal loss are dielectric loss and conductor loss. The focus on low loss tangent dielectrics (LCP, BCB, RXP-4) in previous chapters is an attempt to reduce the dielectric loss contribution. In this section, the research focus is on minimizing conductor loss by exploring surface treatment processes for LCP and BCB to achieve lower profile interfaces to plated copper while maintaining sufficient mechanical adhesion.

Skin depth is an important concept for GHz signaling and is defined as the thickness on the outer edge of the copper transmission line where the high frequency signals tend to be confined as shown in Figure 5.3. Also shown is the skin depth vs. frequency for copper and other metals used in micro systems packaging. The skin depth of copper decreases significantly with increasing frequency and falls to 1-2 μ m at 10GHz.

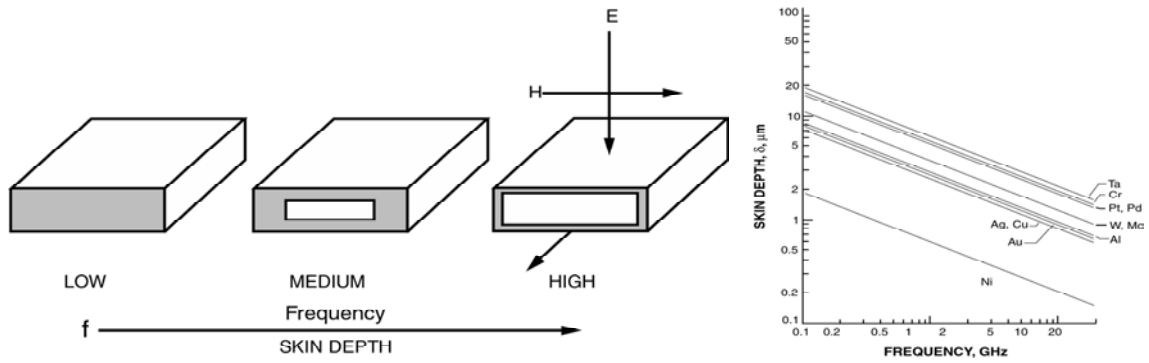


Figure 5.3 Skin depth at various frequencies (schematic – left) for common metals

As the conductor cross-section is reduced due to narrower lines required for higher routing density, the resistance of the transmission line increases and contributes to higher signal loss per unit length (dB/inch or dB/mm) compared to wider lines. The Cu conductor-dielectric polymer interface roughness contributes an additional amount of conductor loss. As the frequency increases and skin depth decreases, the contribution of the added roughness loss factor to overall conductor loss will increase. The reason is that the skin dominates the signal integrity and the average roughness of 1-1.5 μm for standard copper foils used in laminate substrates approaches 75-90% of the skin depth.

A recent study on effect of Cu-dielectric interface roughness quantified this problem by studying the roughness based added conductor loss factor for copper foils with different roughness profiles⁴⁰. Rolled copper foils without any bond enhancement treatment had an average roughness (R_a) of 0.4 μm and peak to peak roughness (R_z or R_t) of 3.2 μm . However, this foil does not have sufficient adhesion to polymers to meet reliability criteria.

The latest very low profile (VLP) grade foils used for high frequency substrates had R_a of $0.5\mu\text{m}$ and R_t of $3.8\mu\text{m}$. The standard profile foils most widely used in laminates today had R_a of $0.6\text{-}0.7\mu\text{m}$ and R_t of $5.1\text{-}7.9\mu\text{m}$ depending on measurement method (profilometry or optical interferometry). The roughest foils had R_a of $1\text{-}1.5\mu\text{m}$ and R_t of $8\text{-}11\mu\text{m}$. The study reported that compared to the untreated rolled copper foil, the VLP foils showed an additional conductor loss of $\sim 0.1\text{dB/inch}$ at 10GHz , while the highest profile foils showed as much as 0.4dB/inch added loss at 10GHz . Modeling and measured results were compared and the authors reported that the following equations accurately predicted the added loss factor from interface roughness.

$$\alpha_c' = \alpha_c * K_{sr} \quad K_{sr} = 1 + \frac{2}{\pi} \arctan[1.4(\frac{\Delta}{\delta})^2] \quad 10$$

where, α_c' is the added roughness loss, Δ is the average roughness, and δ the skin depth. It can be seen that as frequency increases and skin depth decreases, the contribution of roughness to the loss increases. It becomes more and more important to reduce the interface roughness between the build-up dielectric and plated copper traces as the frequency of the signals in the substrate increases. The target for the research on surface modification of low loss thin film dielectrics was $\ll 1\mu\text{m}$ R_a and $< 5\mu\text{m}$ R_z and demonstrating sufficient peel strength of electroless and electroplated copper.

5.2.1. Processing Techniques for Polymer Dielectric Surface Treatment

Chemical Desmear: The current process of record for high density organic package substrates is a chemical desmear process designed for epoxy dielectrics. This process consists of three steps:

- (i) solvent swell step, which creates a porous sub-surface structure in the cured epoxy polymer by a combination of caustic (NaOH) and low concentration of solvent,
- (ii) sodium or potassium permanganate etch step, which etches away selective regions of the “swelled” polymer by aggressive chemical attack in a highly caustic and high temperature environment, and
- (iii) neutralization step (hydrogen peroxide based), which converts the manganese residues from the etch step and renders the polymer surface clean and neutral in preparation for palladium activation and electroless copper plating.

The particular chemistries used in this study were Securiganth P and MV+ desmear systems from Atotech, Berlin, Germany.

13.56MHz RF Plasma Roughening Mechanism on Polymer Dielectrics: The other alternative explored in this research involves RF plasma treatment at 13.56MHz using a parallel plate system (Plasma Etch Model BT-1) shown in Figure 5.4.



Figure 5.4 Plasma Etching System (Plasma Etch BT-1) for 300mm x 300mm substrates

The plasma is generated by free electron collision with incoming gas molecules to partially or wholly ionize the gas mixture with roughly equal number of positive and negatively charge species including electron-hole pairs, free radicals and ions as shown in Figure 5.5. The parallel plate plasma “asher” operates as a capacitively coupled RF discharge and the 13.56MHz RF plasmas have higher concentrations of electronically charged particles than other types of plasmas. These plasmas have also been noted to have good uniformity across large area substrates, which is especially critical for surface treatment processes since the depth of the polymer surface being modified is in the order of tens of nanometers.

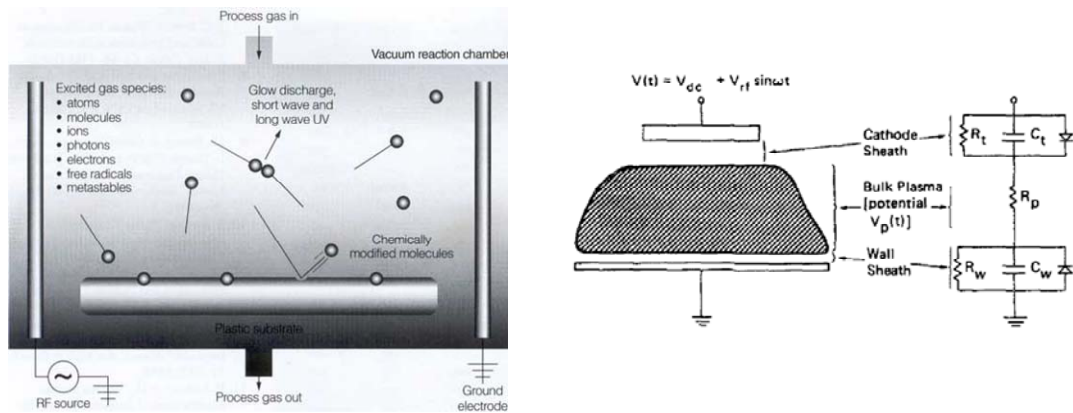


Figure 5.5 Plasma Etching Fundamentals (left) and Schematic and Equivalent Circuit for Capacitively Coupled RF Plasma⁴¹

The larger the bias voltage, the higher is the concentration and energy of the free radicals and electrons in the reactor. As seen in the voltage equation in the figure, at high frequencies like 13.56MHz, the contribution of the V_{rf} increases the $V(t)$ or time average which provides higher energy to the reactive species in the plasma chamber.

The BT-1 system consists of five parallel plates of 21"x20" size with 3" spacing, resulting in low DC bias voltage since the DC voltage increases when the ground electrode on which the substrate is placed is much larger in size than the power electrode (as is the case in RIE chambers). The other factors affecting the etch rate and uniformity are the pressure in the reaction chamber. The pressures used in the BT-1 system were in the 150-500mTorr range (compared to 10-100mTorr for RIE) and the concentration and energy levels of the reactive species in the plasma is much lower at these higher pressures. The plasma "asher" used here is ideal for very low etch rates and excellent uniformity required for shallow surface modification processes targeted in this research. The other influence on the bias voltage is the electronegativity of the gases used. Gases with low electronegativity, such as O₂ used in this study, result in much higher negative DC bias voltage, while Cl, Br and F are much more electronegative (F is highest) and CF₄ used here when injected in small doses does not have much influence on the DC voltage. Other parameters that can be controlled include the RF power and temperature which have a simple effect of higher energy and concentration of species at higher power and temperature and hence faster etch rates.

In general, plasma etching is a chemical etch process, not a physical etch, i.e. a chemical reaction takes place between the solid atom (from the polymer film to be etched) and gas atoms to form a molecule, which is removed from the substrate. For the large majority of etching processes, this physical etching component is so small it can be neglected.

In the current research, two main gases were used in various mixing ratios, CF₄ and O₂. In the 13.56MHz RF plasma glow, it has been reported that CF₄ forms CF₃⁺,

CF_2^+ , CF^+ , and F^+ , whereas oxygen forms (O) atoms, O^+ and O^- . However, in mixtures of $\text{CF}_4\text{-O}_2$, previous studies indicated the reaction of oxygen with CF_3^+ and other radicals to form CO , CO_2 , and COF_2 . The role of oxygen in the plasma etching of polymers is to form O-H, C-O or C=O bonds with the polymer chains and removal of reaction products. This is the reason oxygen plasma is a widely used and very effective process for cleaning all types of surfaces of organic impurities and contamination. CF_4 on the other hand is used mainly for etching or ablation due to the attack of polymer bonds by fluorine and related radicals.

Plasma interaction with the surface of polymers results in several effects, and the main effects for adhesion enhancement are listed below.

- (a) Organic removal: Organic contaminants are a primary reason for poor adhesion of plated copper to dielectric, and these contaminants may be in the form of residues, anti-oxidants, carbon residues or other organics.
- (b) Ablation: The etching of polymer surfaces can be accomplished in a plasma and the resulting mechanical roughness can play a significant role in improving the bond strength of the plated Cu to the polymer by increasing the total interface area. Etching or ablation can be accomplished by both reactive and inert gases, although no inert gas plasmas were explored in this research.
- (c) Surface re-structuring: Plasma modification of the polymer surface is actually the most promising effect to achieve smoother copper-dielectric interfaces and still achieve sufficient bond strength. By attaching polar functional groups to the surface of the polymer, the surface energy is increased significantly, and this can aid in adhesion enhancement.

5.2.2. Chemical & RF Plasma Roughening of Low Loss Polymers

Both chemical desmear and CF_4/O_2 plasma surface treatments were applied through a series of experiments to understand the mechanisms and adhesion improvements associated with these two approaches for a benchmark epoxy dielectric (ABF GX-13 from Ajinomoto Fine Tech), and three low loss dielectric polymers (BCB, LCP). Two different metrology techniques were used. The first method was contact surface profilometry using a Veeco Dektak 3030 tool. Data from this measurement technique has been presented in previous chapters. The second method was optical interferometry using a Veeco Wyko NT1100 tool shown in Figure 5.6. Also shown is a schematic of the operating principle of this approach.

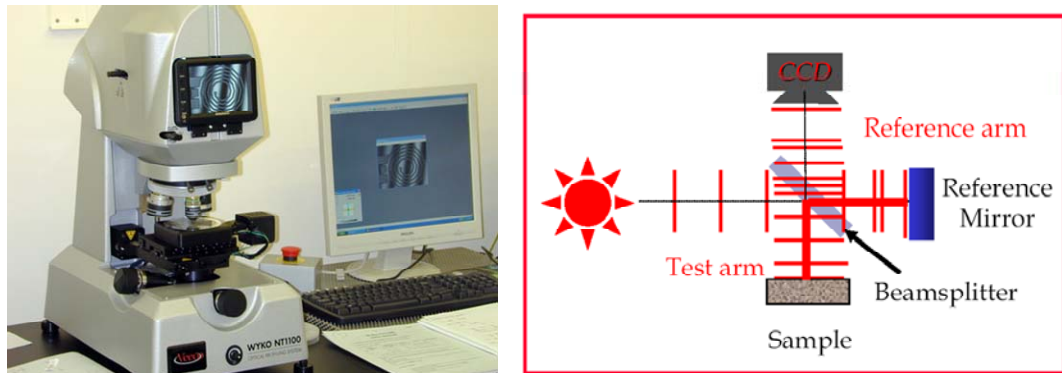


Figure 5.6 Veeco Wyko NT1100 Optical Interferometer and Operating Principle

The beam exiting from the light source is divided into two beams by the beam-splitter. One beam is reflected from the reference mirror and the other from the sample. The two beams are recombined by the beam-splitter to interfere and the CCD camera images the interferogram. Any change in tilt of the sample or the reference mirror causes a change in the light and dark fringes in terms of number of fringes and spacing. The surface topography of the polymer sample causes tilts at a micro and nano scale and the instrument is capable of resolving the changes in the fringe patterns to nanometer scale, thus measuring the roughness of the sample surface.

Epoxy Benchmark Dielectric: For ABF GX-13 epoxy dry film dielectric, the results of chemical desmear with two different conditions (7 min swell, 10 min etch) and (15 min swell, 20 min etch), along with CF₄/O₂ plasma treatment (400W, 100°C, 100sccm O₂, 25sccm CF₄, 10 minutes) and comparison to the untreated sample are summarized in Table 5.1 and Wyko images are shown in Figure 5.7.

Table 5.1 Summary of Wyko Surface Analysis of Chemical and Plasma Treated ABF GX-13 Epoxy Dielectric (all units in μm)

Sample	Ra	Rz
Chemical Desmear (D 15/20)	0.64	6.58
Chemical Desmear (D 7/10)	0.61	5.52
CF4/O2 Plasma	0.69	7.23
No Treatment	0.48	5.23

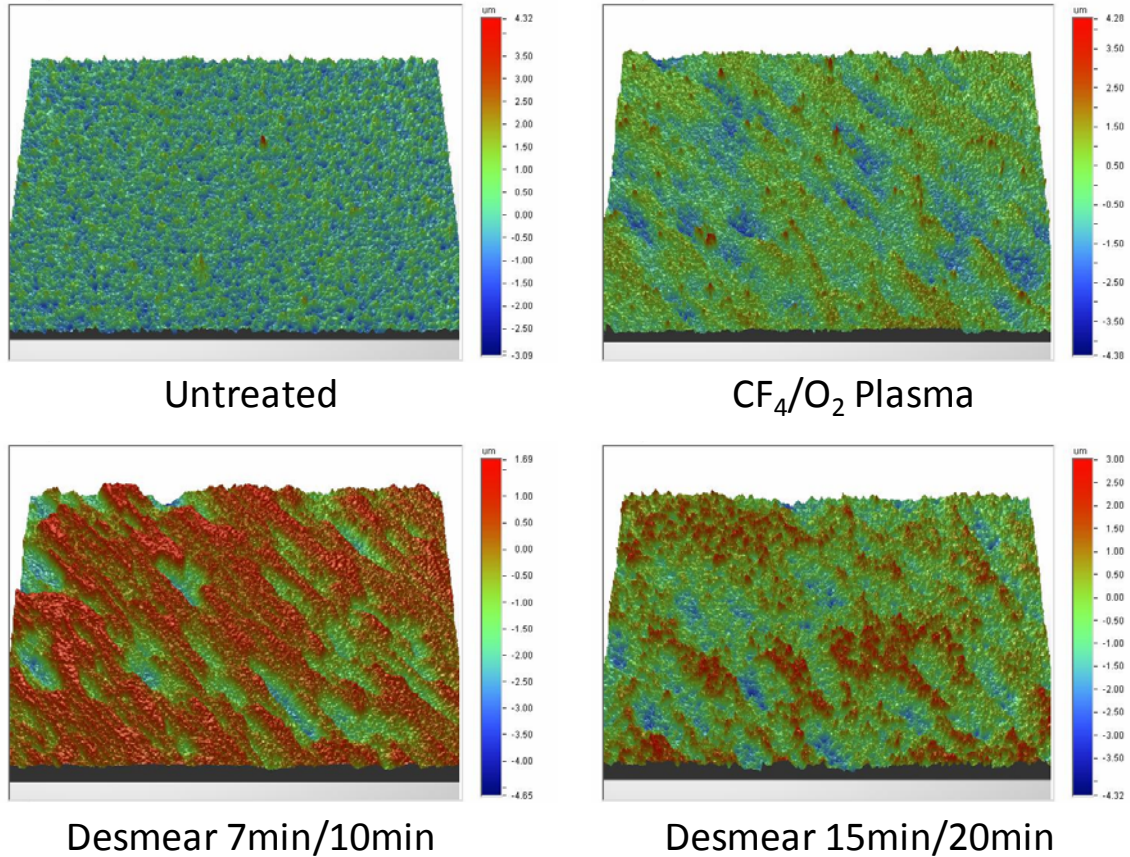


Figure 5.7 Wyko Surface Scans at 25x Magnification for Chemical and Plasma Treated ABF GX-13 Epoxy Dielectric

For the ABF epoxy dielectric, both the standard chemical desmear and plasma treatment resulted in primarily mechanical roughening as indicated by the increase in average roughness (R_a) and peak-to-peak roughness (R_z). However, even though the R_a was around $0.5\text{-}0.6\mu\text{m}$ for all the conditions, the R_z was higher than the research target ($<5\mu\text{m}$) mentioned earlier. It is also interesting to note that the R_z of the ABF without any treatment is greater than $5\mu\text{m}$. This is due to the presence of a high volume fraction of ceramic filler particles (some as large as $5\mu\text{m}$) in the epoxy dielectric for reducing the CTE of the material.

The fillers create significant topography on the surface of the untreated dielectric and although the polymer is etched during chemical and plasma desmear, the ceramic fillers are not attacked by either process and the filler driven topography is maintained after surface treatment. The additional roughness from the polymer treatment contributes to the slight increase in roughness with the chemical and plasma processing.

BCB and LCP Low Loss Dielectrics: LCP dry films (25 μ m thickness) and BCB spin-coated thin films (10 μ m thickness) were subjected to chemical desmear, O₂ plasma and CF₄/O₂ plasma surface treatments. In this case, oxygen plasma was added for BCB since it was a successfully established process for cleaning carbon residues from the excimer laser ablation described in Chapter 4.

The Wyko analysis results for BCB surface treatment are shown in Figure 5.8 for the following treatment conditions:

- Chemical desmear (6min swell + 10min etch),
- Chemical desmear (10min swell + 15min etch),
- O₂ plasma (300W, 100sccm O₂, 100°C, 10 minutes),
- CF₄/O₂ plasma (300W, 73sccm O₂, 27sccm CF₄, 100°C, 12 minutes)

and compared to the untreated sample.

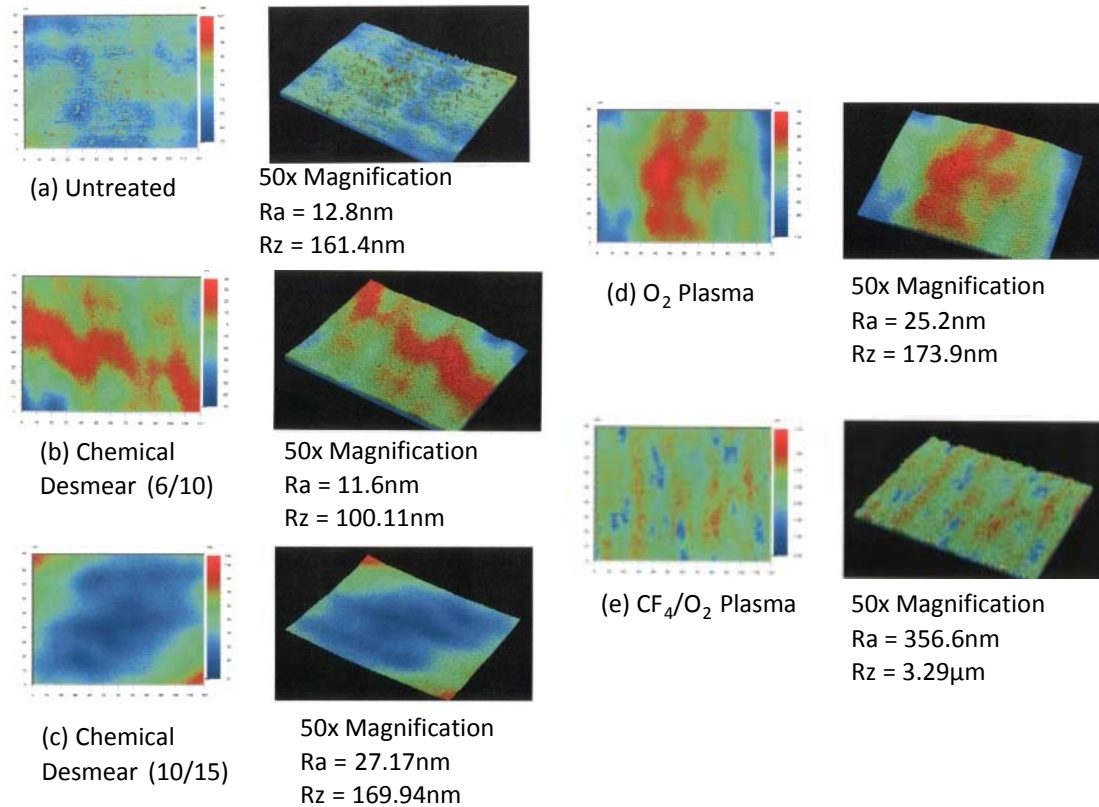


Figure 5.8 Summary of Optical Interferometry Analysis of Surface Roughness for BCB

It is clearly seen that the chemical desmear process designed for epoxy polymers did not have any effect on the BCB dielectric. In the case of epoxies, the highly caustic chemistry and hydroxyl groups can easily attack the epoxy polymer chain and break the C-H and C-O bonds in the presence of a strong oxidizer such as sodium permanganate. However, the polymer chains in BCB with the strong Si-O bonds and lack of hydryl side groups prevents chemical attack with the desmear chemistry. The optimized conditions from Chapter 4 for CF₄ + O₂ plasma ashing was highly effective and achieved the target roughness specifications. This is because of the highly energized fluorine based free radicals and ions in the plasma that can easily break the bonds and cause ablation in shallow depths on the surface of BCB.

The oxygen only plasma was also not effective, and this is consistent with reported literature on oxygen plasma etching of BCB, where unwanted oxidation of Si in the BCB chain causes surface passivation and very low etch rates. The CF_4/O_2 plasma modified BCB surfaces were also analyzed by surface profilometry to determine the local roughness (R_z and R_t) and presence of any deep pits similar to those in epoxies that can cause problems for ultra-fine line processing. The Dektak surface profilometry scan (Figure 5.9) confirms that the peak to peak roughness was less than $1.5\mu\text{m}$.

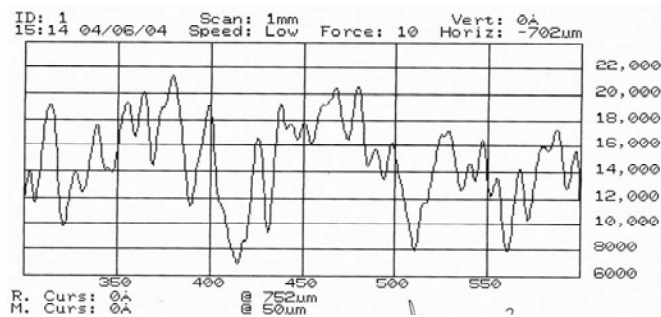


Figure 5.9. Surface Profile (\AA) of BCB after CF_4/O_2 Plasma Treatment for 12 minutes

Figure 5.10 shows the comparison of FESEM images at 10,000x magnification before and after the plasma treatment, and a uniform etching profile can be seen.

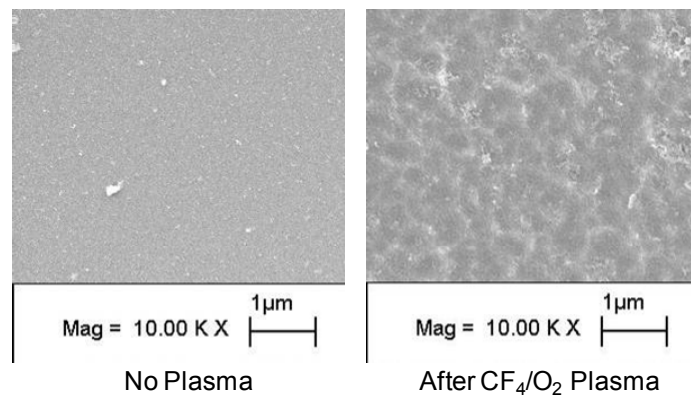


Figure 5.10 FESEM Images of BCB Surface Before and After CF_4/O_2 Plasma

Only plasma etching was explored for LCP since this polymer dielectric is known to be highly inert and resistant to chemical attack in harsh environments. In fact, this moisture and chemical barrier property of the LCP has made it a very attractive candidate for protective coatings, cable sheaths or molded packages for harsh environment applications. Figure 5.11 shows the optical interferometry measurements before and after $\text{CF}_4 + \text{O}_2$ plasma etching of LCP film. For this experiment, a single clad LCP film (copper foil laminated only on one side) was used and the un-clad exposed LCP surface was etched. The topography seen on the surface prior to etching is due to the melt flow behavior of LCP during single side copper lamination. Etch rates in the plasma were also established independently by Dektak surface profilometry and etch rates of 0.1-0.2 $\mu\text{m}/\text{minute}$ were observed for 300W RF power at 80°C and $\text{CF}_4:\text{O}_2$ flow of 125sccm:75sccm. This high flow rate resulted in higher reactor chamber pressure of ~500mTorr and resulted in much slower etch rates that could be well controlled. The roughness profile after this plasma etch process was quite uniform as seen in Figure 5.9 and none of the initial topography can be seen since the top 1-2 μm of the LCP film was completely etched.

For all the above materials, the optimized roughness profile and adhesion was confirmed by electroless and electrolytic copper plating with no blisters, followed by thermal annealing for stress relief at 150°C for 1-2 hours. The epoxy, BCB and LCP samples successfully passed IPC standard scotch tape test and further fine line processing and integration on low CTE core was done as discussed in the following sections.

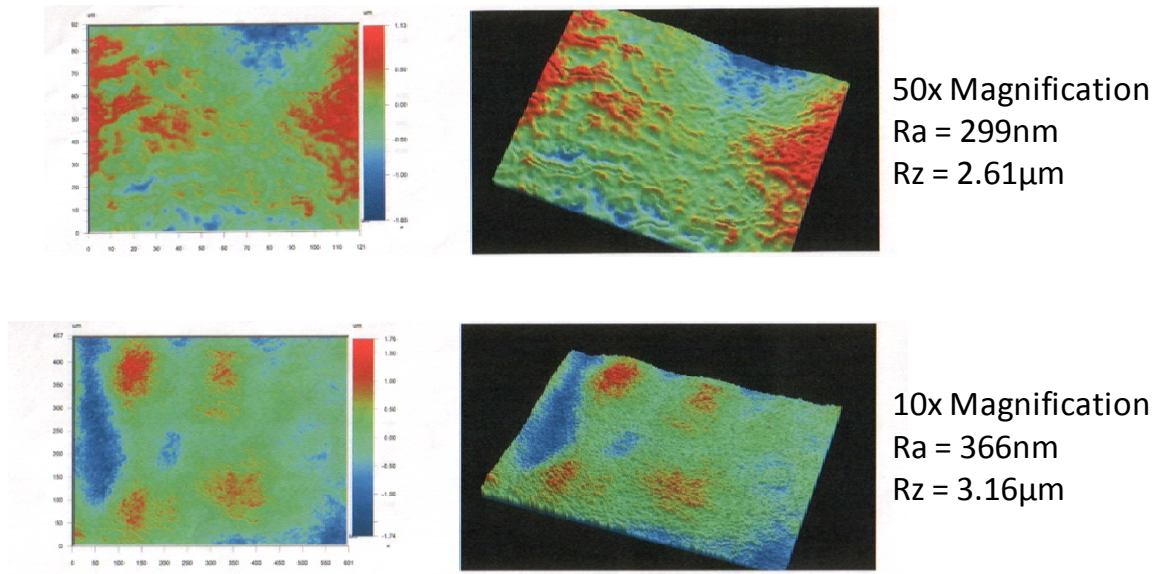


Figure 5.11 Summary of Optical Interferometry Analysis of Surface Roughness for LCP

5.2.3. Impact of Dielectric Surface Roughness on sub-10µm Copper Lines

Surface roughness is a critical factor for both fine line lithography and metallization. Comparisons of filled epoxy dielectric surface after permanganate desmear treatment and an unfilled epoxy surface after CF_4/O_2 plasma roughening is shown in Figure 5.10. A fine line width of $10\mu\text{m}$ is overlaid on these two surfaces to illustrate the scale of the surface roughness (R_z factor) against the ultra-fine line width dimension. As demonstrated earlier, permanganate desmear of a ceramic filled epoxy dielectric surface results in peak to peak roughness of $5\text{-}10\mu\text{m}$ ($2\text{-}4\mu\text{m}$ R_z even with the latest material and process) with lateral crevices and large pits measuring $\sim 2\text{-}3\mu\text{m}$ across as seen in Figure 5.12.

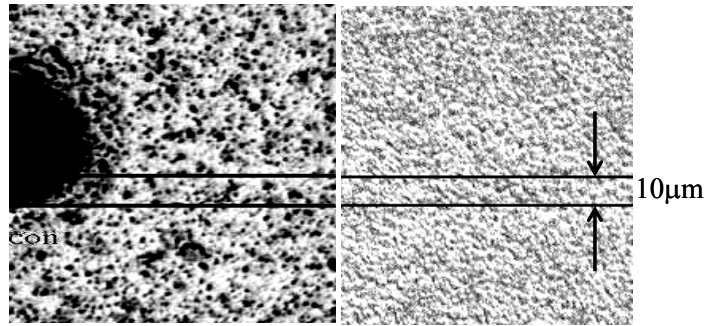


Figure 5.12 High Magnification Optical Micrographs of Surface of Build-up Dielectric after (a) permanganate desmear, and (b) plasma desmear showing overlay of 10µm line

Ultra-fine lines were fabricated on the epoxy surface shown at left in Figure 5.12 and this resulted in latent defects in the traces and inconsistent dielectric thickness between metal layers as shown in Figure 5.13. The plasma treatment on the other hand produces a fairly uniform roughness on the surface that can be <1µm deep. The plasma process has been successfully implemented to fabricate the ultra-fine lines as described in the next section.

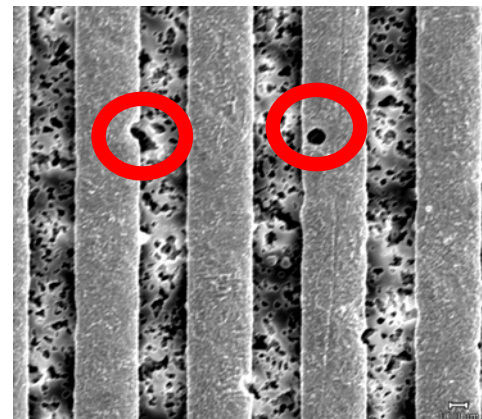


Figure 5.13 SEM micrograph of defects in 10µm lines due to deep pits from chemical desmear

Additionally, a planar surface is required for fabrication of fine lines on large substrates due to depth of field and contact limitations during lithography. The following sections describe the exploration and demonstration of low-cost package substrate compatible photo-lithography and fine line metallization processes for sub-10µm lines and spaces.

5.3. Advanced Processes for <math><10\mu\text{m}</math> Lines/Spaces and Extreme-Fine Line Copper Conductor Formation using Low Cost Package Substrate Materials

5.3.1. Ultra-Fine Line Test Vehicle Design and Layout

A process test vehicle (TV) was designed and fabricated to explore processing of ultra-fine copper lines to conventional epoxy and emerging build-up dielectrics. In addition, the test vehicle was designed to explore copper dielectric interfaces and ultimately multilayer reliability of the copper interconnections. The test vehicle design consisted of ultra-fine line challenge structures including; open serpentine structures, shorts combs, line/space, routing simulations, via stitch, and transmission lines – ranging from $25\ \mu\text{m}$ to $5\ \mu\text{m}$ in width and space (Figure 5.14).

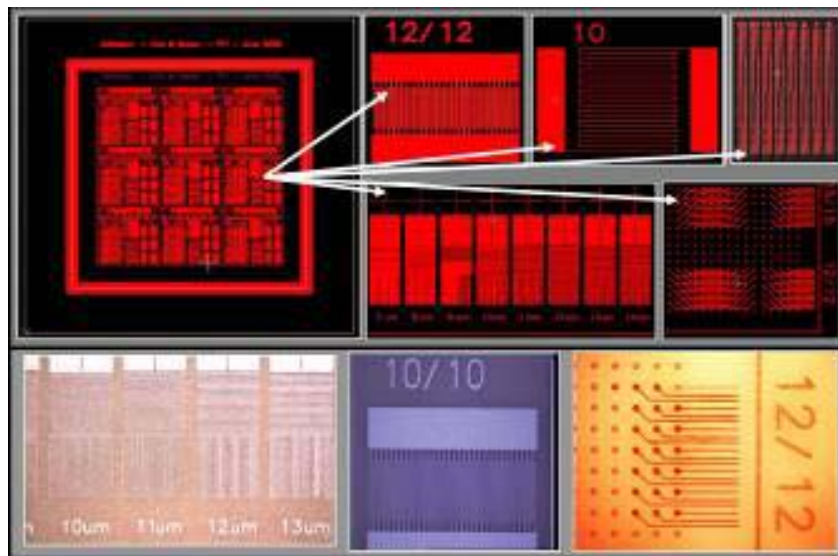


Figure 5.14 Process test vehicle (TV) as designed (above images), and as fabricated (below) containing various test structures for fine line and space process development.

5.3.2. Metallization Process Approaches for Ultra-Fine Lines and Spacing

There are two common techniques used for package substrate copper metallization: subtractive and semi-additive. The subtractive process uses wet chemical etching and has been used in printed circuit boards (PCB) for decades and is also used in HDI motherboards and low-cost mobile phone package substrates, while the semi-additive process (SAP) is a more recent development primarily used in high end and high density package substrates.

Limits of Fine Pitch Etching

Wet chemical etching is the most popular subtractive method in PCBs and substrates, and has resolution limits due to the isotropic nature of wet etching resulting in undercutting of traces. Current state-of-the-art processes can achieve 75 μm (3mils) to 125 μm (5mils) trace widths in a 35 μm thick (1oz) copper foil, and 20-30 μm line widths are emerging in production volumes using thinner copper foil (e.g. 9 μm or 12 μm thick). In the current research, the etch chemistry was fine tuned to minimize undercutting and 20 μm line and space was demonstrated on 12 μm foil with minimal undercut of the copper trace fabricated on glass reinforced epoxy FR-4 substrate. Figure 5.15 shows a cross section of 20 μm lines and spaces with near-vertical wall made by wet etching. Though the undercut effect can be reduced by modified etching, the aspect ratio of etched copper fine lines is limited by some amount of lateral etch during the process. It is believed that controlling the etch process across a large 300-600mm substrate panel in production will be a challenge for scaling etching processes to below 15 μm lines/spaces.

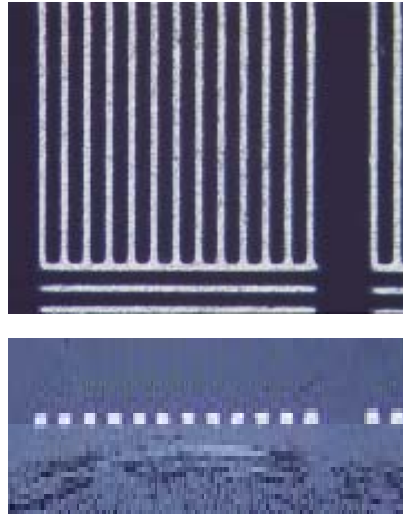


Figure 5.15 Fine Pitch Traces (20µm Line Width, 20µm Spacing) by Copper Etching (Top view and Micro-section) with Copper Thickness of 12µm (aspect ratio 1.6:1)

5.3.3. Semi-additive plating (SAP) process

To overcome the disadvantages of subtractive etching, the semi-additive plating process was designed. Figure 5.16 shows a process schematic of the key steps in semi-additive plating used in this research.

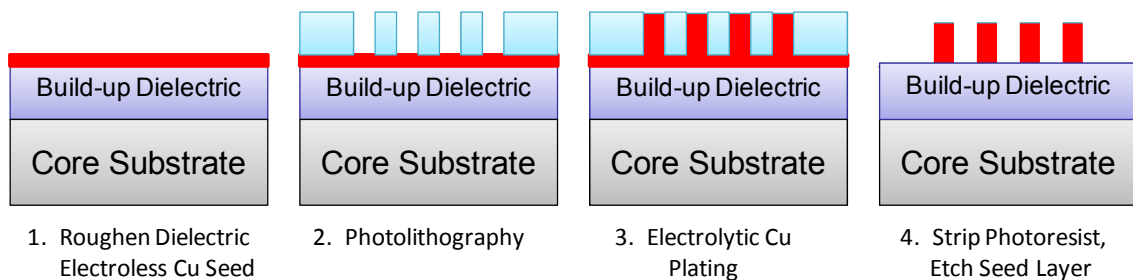


Figure 5.16 Process Flow for Semi-Additive Process (SAP)

A very thin seed layer of copper is plated on the dielectric using electroless plating after surface modification with chemical desmear or plasma etching and palladium activation. The function of the seed layer is to provide an electrically conductive surface for the higher throughput electroplating process. A dry film or liquid photoresist is deposited on the seed layer and patterned using photolithography. The final copper trace thickness is built up by DC or pulse reverse electroplating through the photoresist template. The photoresist is then stripped and the thin electroless copper seed layer etched away using a mild sodium persulfate or peroxide-sulfuric acid etchant. This will of course result in removal of copper from the electroplated traces as well and any reduction in line thickness or width has to be accounted for during process design. The formation of ultra-fine lines and spaces ($< 10\mu\text{m}$) requires strict control and optimization of all the SAP steps including interfacial roughness of dielectrics, seed layer formation, photolithography, electroplating and seed layer etch.

The research focus in this thesis was on advanced photolithography processes using next generation of low-cost dry film photoresist for $10\mu\text{m}$ lines/spaces, and liquid photoresist for $<10\mu\text{m}$ lines/spaces. Additional research focus was on understanding the critical interfacial issues and fundamentals of advanced materials/processes as they relate to achieving $<10\mu\text{m}$ lines. No new materials research was conducted in electroless and electrolytic copper plating chemistries, although the latest state-of-the-art process technologies from a leading high volume supply chain partner, Atotech, Germany were used to demonstrate the extreme-fine lines/spaces.

5.3.4. Low stress electroless plating

Electroless plating is a low cost and batch processing technique suited for high-volume manufacturing. Due to the smoother surface profile of plasma treated dielectrics, older colloidal based activation processes for copper plating do not work. A metallic palladium activation system was used for the low loss BCB, LCP and RXP-4 dielectrics. The palladium particles were small enough to occupy the tiny pores of plasma treated dielectrics and provide good activation. This is also important to provide a high density of closely spaced nucleation sites for the electroless copper redox reaction, which results in lower deposited film stress.

There is a strong need for smoother conductor surfaces for impedance control and less signal attenuation due to skin effect. But this results in poorer mechanical adhesion between the copper and dielectric. To counter adhesion problems and to obtain reliable SOP substrates, a low plating rate ($2\mu\text{m}/\text{hour}$) and low stress electroless plating process Printoganth MV+ from Atotech, Germany was used. This process produces fine grained deposits which have better adhesion than larger grain size copper deposits from higher plating rate processes. The deposits were blister free and had excellent coverage of the dielectric surface.

The thickness of the seed layer plays a critical role in determining the limit of fine line resolution. For $\leq 10\mu\text{m}$ lines, it is essential to deposit the thinnest seed layer that can meet the conductivity requirements for the panel size used. The minimum seed layer thickness is dictated by the amount of resistive loss from the edge of the panel to the center that can be tolerated during electrolytic plating. Since the seed layer etch (last step in SAP) is an isotropic wet etch, the top and side walls of the electroplated fine lines will

also undergo some etching leading to the formation of trapezoidal lines. For a 10 μ m copper line, a seed layer thickness of 1-2 μ m may result in line width variance of as much as 10-20%. The electroless copper plating system for 300mm x300mm substrates is shown in Figure 5.17.



Figure 5.17 Advanced Electroless Copper Plating System with Pd Activation

The plating was done at a controlled temperature of 34°C +/- 2°C for 15 minutes to deposit a seed layer of ~0.5 μ m average thickness. The uniformity of seed layer thickness was measured using XRay Fluorescence Spectroscopy (XRF) for several 300mm x 300mm substrates and the results are shown in Figure 5.18.

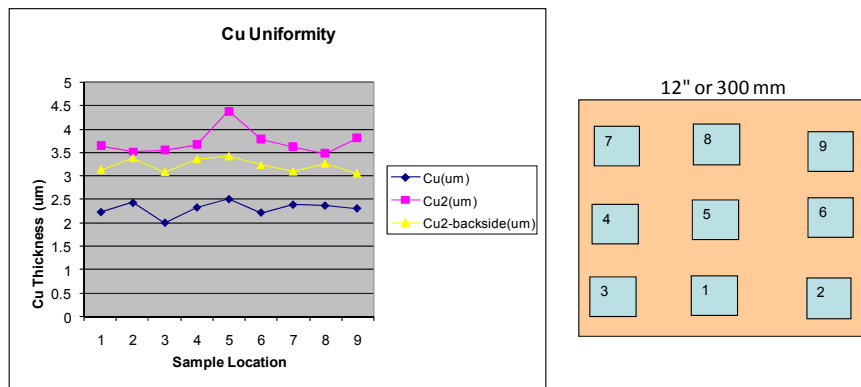


Figure 5.18 Electroless Plated Cu Uniformity Measurement by XRF for 1hr (front only) and 2hr plating time (front and back side) of 300mm x 300mm substrate

5.3.5. Low Cost and Ultra-Fine Line Photolithography

Photolithography has played a dominant role in the miniaturization of feature sizes at IC and package levels. The semiconductor industry has developed feature sizes less than 30nm for high performance microprocessors. However, the state-of-the-art package substrate technology is able to produce 15-20 μ m line and space. A technical gap of the order of 1000 exists between semiconductor and packaging. In order to keep the pace with semiconductor, a finer pitch wiring substrate is necessary. The key factors that hinder the finer feature size formation on package substrate are discussed in this section. Advanced solutions based on low cost materials and processes for fine line photolithography below 10 μ m were explored to determine the minimum lines and spaces based on the mercury i-line photolithography, both theoretically and practically.

Photolithography is the technology of reproducing images or patterns by using UV light. The designed patterns for constructing circuits are transferred onto a photosensitive thin or thick film by photolithographic method. This technology has been improving to produce smaller and smaller feature size on large panel substrate with high yield and low cost over the past decades. In semiconductor industry, deep UV beam is used for sub micron feature size ICs and x-ray and e-beam are used to make even finer structures. In order to maintain the lower cost, high pressure mercury lamp UV system with I-line is still the main tool for mass production in PCB industry. The photolithography dominates the process capability of producing fine line structure.

5.3.5.1. UV Lithography Methods

There are three basic UV light exposure models. They are proximity, contact, and projection imaging. Proximity and contact models are commonly used in package substrate and PCB fabrication while the projection model is used more in semiconductor and wafer-level processes. Figure 5.19 illustrates the principle of a collimated beam of UV light propagating through a transparent area in the photo-mask to a photo resist film on the substrate. From the figure, one can see that a UV beam illuminated on a photo resist is no longer collimated if there is a gap between the photo-mask and the photo resist. This is due to the nature of light diffraction. The photo resist beneath the opaque area of the mask could be illuminated by the UV beam. The beam intensities on the photo resist surface for contact mode ($d=0$) and proximity are shown in Figure 5.20. For contact mode, the beam intensity on resist is uniform and intensity outside of the opening area is zero. With the presence of a gap, the beam intensity becomes non-uniform and more dispersed. As the opening becomes narrower and the gap becomes larger, the effect becomes more problematic and the adjacent lines become un-resolvable.

5.3.5.2. Principles for Resolution of Proximity Photolithography

Proximity mode is commonly used for package substrates due to the elimination of mask damage risk from contact lithography. In proximity exposure mode, there is a small gap (typically of the order of tens of microns) between photo-mask and photo-resist. Assuming the opening on the photo-mask $0 \rightarrow L$ and the range of diffractive effect Δ , it can be seen that when Δ reaches $L/2$, a comb structure having equal lines and spaces

becomes closed since all the space is exposed. The photolithography reaches its limits of resolution. This is the minimum line and space that can be achieved by using this technology.

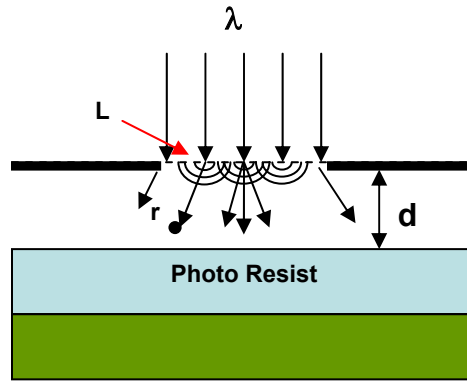


Figure 5.19 Principle of photolithography with UV light. Light diffraction becomes problematic when transparent area becomes smaller

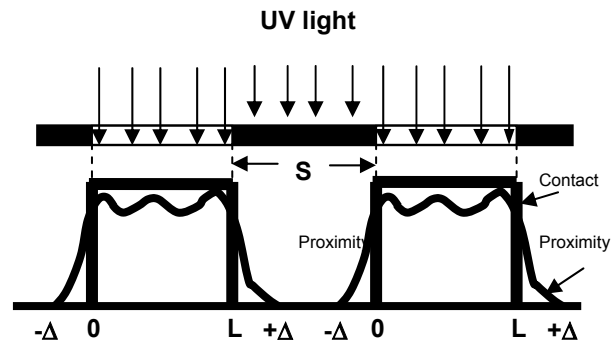


Figure 5.20 UV Beam Intensity on the surface of photoresist. When Δ reaches $L/2$, the comb structure having equal line and space will not be resolved.

5.3.5.3. Experiments on Gap Effect

In order to study the gap effect, it was very important to design a suitable experiment. Various groups of test samples with different thicknesses of photo resist

were prepared. All the samples in a group must have the same thickness according to the designed value. Extremely well controlled process conditions are necessary since the minimum lines and spaces are very sensitive to the process conditions, such as exposure dose, baking (temperature and time), development (solution concentrations, temperature and time) etc. Any difference in photo resist thickness, the distance of the gap, and process conditions will create significant errors in the experimental results.

A simple but effective way to guarantee control of these conditions was designed. The experiment is described as follows: (1) design a group of test comb structures having lines and spaces of 2 to 84 μm , (2) place the patterns at different positions (three positions in this experiment) on a photo-mask, (3) apply a uniform photo resist on a flat substrate, (4) place the photo mask onto the photo resist and tilt it at a small angle, (5) full field UV exposure, (6) develop, and (7) measure the minimum feature sizes and examine the image sharpness. The three test structures at different places on the photo-mask will have different gap distances to the photo resist, as shown in Figure 5.21. In this way the three patterns went through exposure and development simultaneously. Figure 5.21 also shows the details of the mask design and experimental setup. Three repeated groups of test patterns were on the mask. A layer of photoresist was spin coated on the substrate with a thickness of 8 μm . The gap distances between patterns and the photo resist were 30 μm (d1), 60 μm (d2), and 90 μm (d3). A high pressure mercury UV exposure lamp with collimated light (Tamarack Scientific Model 152R) was employed in the experiment. The minimum lines and spaces achieved were 7 μm , 10 μm and 12 μm for gaps at 30 μm , 60 μm and 90 μm respectively. Figure 5.22 shows a comb structure with lines and spaces of 7 μm photo resist at a gap of 30 μm . It was also found that the line edge became fuzzy or

unclear as the gap distance increased. When the photo-mask was laid down onto the photo resist in contact mode ($d=0$), $5\mu\text{m}$ line and space was achieved. Less than $6\mu\text{m}$ line and space was difficult to recognize under optical microscopy and high magnification SEM was required.

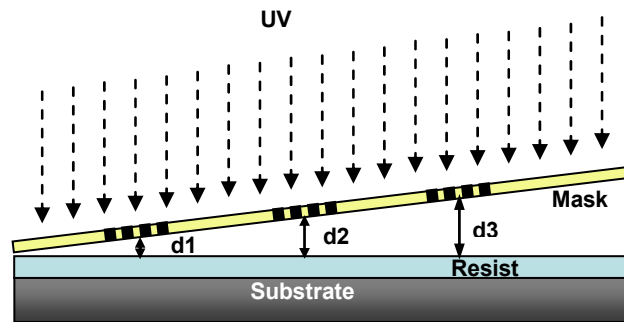


Figure 5.21 Experimental Setup for UV exposure at different gap distances for studying the gap effect on the resolution of proximity mode photolithography

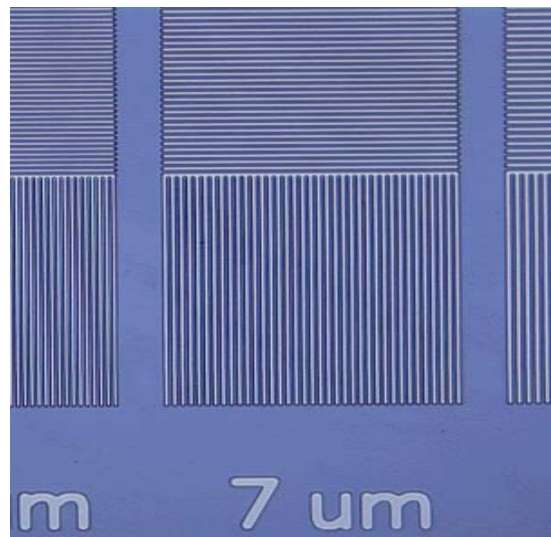


Figure 5.22 Optical micrograph of test comb structure with equal line width and space. $7\mu\text{m}$ line and space resolved on $8\mu\text{m}$ thick photo resist at a gap of $30\mu\text{m}$ by using i-line UV lithography

5.3.5.4. Calculations on Gap Effect

For a comb structure having equal line width and space, the minimum size L_{\min} can be calculated from the following equation⁴²

$$L_{\min} = 3/2 [\lambda(d+T/2)]^{1/2}$$

where λ is the wavelength of radiation, T is the film thickness and d is the gap between the photo-mask and the photo resist. For contact mode, the gap is zero. For i-line $\lambda = 365\text{nm}$ (i-line) and the resist thickness used in the experiment $T = 8\mu\text{m}$, the minimum L_{\min} was calculated at different gap distances from 0 to $100\mu\text{m}$. The calculated minimum L_{\min} was from $1.8\mu\text{m}$ to $9.5\mu\text{m}$ and the data is shown in Table 5.2 and plotted in a dotted line as shown in Figure 5.23. From the curve, it can be clearly seen that; (1) the best result is achieved at $d=0$, i.e. contact mode, (2) the gap greatly degrades the resolution. In the experiment described above, the best results with the fabricated test coupons were $5\mu\text{m}$. The experimental results were added to Figure 5.23 in a solid line marked “Fabricated”. Comparing the two curves, it can be seen that the fabricated feature size is about 2 to $3\mu\text{m}$ larger than calculated values. This difference may be caused by:

(1) Process effects: In general, the aspect ratio of features that can be developed for most resists is 1:1. In this experiment, the photo resist was $8\mu\text{m}$ thick. The aspect ratio will be 4:1 if $2\mu\text{m}$ line and space needs to be resolved and this aspect ratio was the limiting factor. The finest line and space obtained was $5\mu\text{m}$ and the aspect ratio was 1.6:1.

- (2) quality of UV light source, and
- (3) photo resist performance.

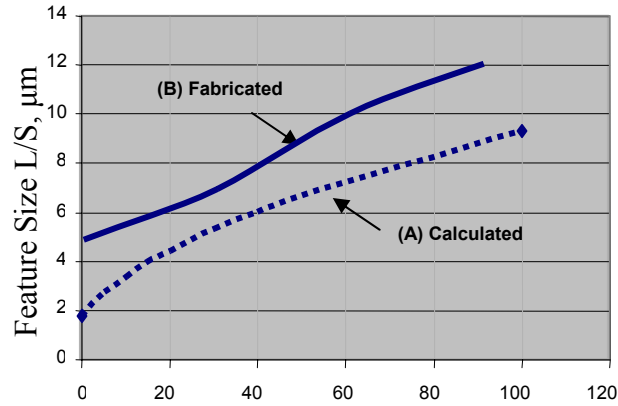


Figure 5.23 Calculated (lower) and fabricated minimum (upper) line and space with various gap distances between photo-mask and an $8\mu\text{m}$ thick photo resist.

Table 5.2 Fabricated and calculated L_{\min}/S_{\min} on $8\mu\text{m}$ thick photo resist in proximity mode lithography

Gap d , μm	90	60	30	0
Thickness T , μm	8.0			
Fabricated L_{\min} , μm	12	10	7	5
Calculated L_{\min} , μm	8.9	7.2	5.3	2

5.3.5.5. Photo Resist and Fine line formation challenges

Photo resists, dry film or liquid, are used for image transfer from photo-mask to the substrate. Dry film is supplied as a three-layer sandwich with a polyester cover layer and polyethylene separator sheet. This stack provides a reliable imaging system with a suitable resolution and a simple process for high volume production. The dry film has been the dominant process for the image formation in package substrate and PWB

manufacturing, mainly due to high yields, precise thickness control, and environmental friendliness by eliminating exposure to solvents in the substrate processing. The resolution of line and space (L/S) is related to the film thickness. In general, the minimum L/S that can be formed is about 1.5x-1.2x the thickness of the resist in a manufacturing environment and down to 1.0x-0.7x in the laboratory. The thinnest dry film resist currently available in production volume is 15 μ m (0.6mil). Therefore the finest circuit traces that can be fabricated by using dry film photo resist is about 18 μ m to 22 μ m in production and 15 μ m to 10 μ m in the laboratory. We have demonstrated 10 μ m line and space 15 μ m thick plated copper by using DuPont RistonTM JSF1C15 dry film photo resist in this research using advanced tools and processes compatible with organic substrate manufacturing infrastructure. A detailed analysis was performed on the uniformity of imaged fine line dimensions in four corners and one center location of a set of 150mm x 150mm substrates for JSF1C15 dry film photoresist using both immersion developing and spray developing processes. The results summarized in Figure 5.24 indicate that with optimized high pressure spray development process provided improved uniformity and process control over immersion developing. The R² value after spray development was 0.9995, very close to the ideal target of 1.0 and features down to 10 μ m width were imaged with very high tolerance across the entire 150mm substrate.

5.3.5.6. Electrolytic plating process and sub-10 μ m Line/Space Results

Both direct current (DC) electrolytic plating and pulse reverse plating using acid copper chemistries was used to metalize the fine line structures. The electrolyte

composition typically includes copper sulfate as the source of copper, sulfuric acid, and organic additives (brightener, carrier, leveler) to control the plating distribution, grain structure, and mechanical properties of the plated copper.

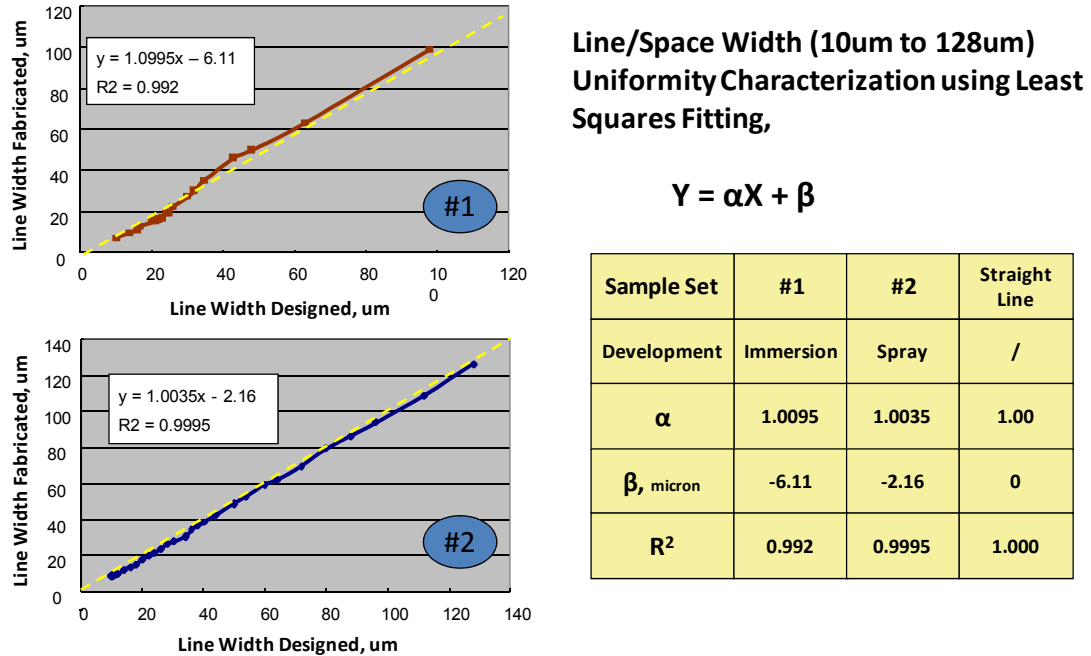


Figure 5.24 Feature Width Deviation from Designed Values for Dry Film Photoresist

Current density in the range of 10-25 A/sq. ft. (ASF) were used in DC plating mode for a plating rate of approximately 0.5 μ m per minute. Pulse reverse plating was primarily used for plating blind vias and fine lines with a high aspect ratio. In case of DC plating, there was significant non-uniformity in fine line plating thickness across the 300mm substrate, due to varying pattern density resulting in different current densities locally. Other causes of non-uniformity in plating distribution are the high aspect ratio vias where the depth of the via causes more copper to be deposited on the edges of the vias (high current density areas) than at the center (low current density areas) resulting in the so called ‘dogboning’ of the structure. To counter this problem, pulse reverse plating is used. DC plating can be used to plate such structures, but the current densities that

must be used are much lower resulting in higher processing time. In pulse reverse plating, instead of constant current, a waveform is used. A typical waveform is illustrated in Figure 5.25. The time ratio forward / reverse is about 20, but the reverse current density is about three times as high as the forward current density. The frequency is usually about 50 Hertz.

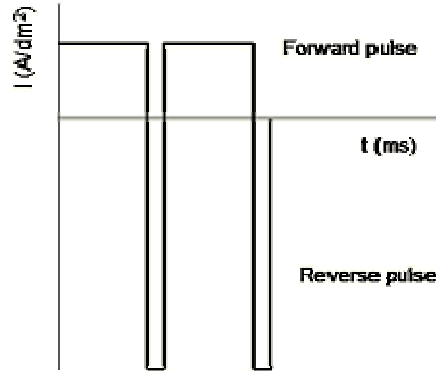


Figure 5.25 Typical waveform for pulse reverse plating

The effect of pulsed current is to provide time for relaxation and re-mixing of chemical components at the Helmholtz boundary layer typically formed adjacent to the substrate (cathode). Since fluid dynamics and surface tension make it difficult to exchange the plating solution into small features, the pulse waveform allows sufficient time between current supply cycles for the fluid to be exchanged in small and large features. During the forward pulse cycles, the substrate is the cathode and plating of copper takes place. During the reverse cycle, the substrate becomes the anode and de-plating occurs at the substrate. Since the reverse duty cycles are much smaller than the forward duty cycles, not much thickness of copper is etched, however, more equalization of plating thickness between large and small features and high and low metal density areas occurs. In this study, pulse reverse plating allowed for the use of at least 2x the

current density compared to DC plating for the same copper thickness uniformity for SAP processing.

Figure 5.26 shows 4 pairs of copper traces with lines and spaces of 10, 15, 20 and 25 μm on ABF/BT substrate by using the DuPont dry film photo resist. The copper thickness measured was 18 μm which was plated using semi-additive process (SAP). DC mode electrolytic plating was used to fill copper in the patterned photo resist.

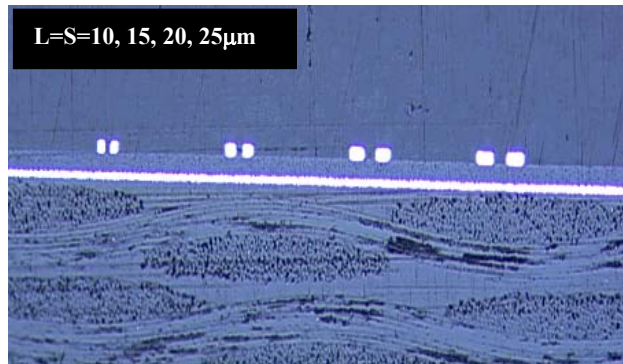


Figure 5.26 Plated copper traces with line widths and space widths of 10/15/20/25 μm on ABF/BT by using dry film photo resist provided by DuPont. The copper thickness measured is 18 μm .

Liquid photo-resist has higher imaging resolution ability and can be deposited in any thickness. As the advanced package moves towards higher pin counters, finer pitch, and thinner profile, liquid photo resist technology may be required. Figure 5.27 (top view – upper, microsection – lower) shows a flip chip mounting pad structure and routing lines on ABF on BT core substrate. The pad diameter in this case is 40 μm and the pitch is 100 μm . Also there are three metal lines routed in the channel between adjacent flip chip

pads with channel width of $60\mu\text{m}$. The minimum line width and space for this routing must be less than or equal to $8.6\mu\text{m}$. Copper thickness measured was $8.5\mu\text{m}$, resulting in an aspect ratio of 1:1. With the optimized process, it was possible to form line widths and spaces down to $5\text{-}6\mu\text{m}$ equal to routing capability of 4 rows/channel and $10,000\text{ I/O/cm}^2$.

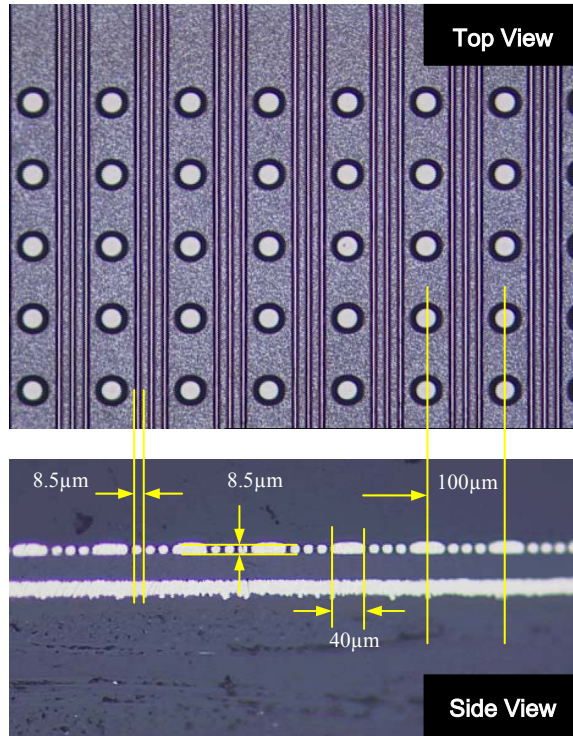


Figure 5.27 Ultra-fine line routing on ABF for $100\mu\text{m}$ pitch flip chip with $40\mu\text{m}$ pads. Line and space shown at $8.6\mu\text{m}$ for 3 lines/channel routing & Cu thickness of $8.5\mu\text{m}$.

5.3.5.7. Surface Irregularity Challenges for sub- $10\mu\text{m}$ lines and spaces

Fine line structures are usually formed on a planar and smooth surface. A non-planar, undulating, or rough surface will negatively impact fine line image formation. The physical characteristic of a surface can be distinguished by the following factors: warpage, global and local undulation, and roughness. Warpage is caused by the stress

induced during the build-up process. Warpage makes the entire panel non-planar. Periodically undulating surfaces are often seen in organic substrates with fiber reinforcement such as FR-4, FR-5, BT, etc. The woven glass fibers have knots and the epoxy resin has some amount of conformality to the waviness of the glass fabric making the substrate surface non-planar. The wavelength is in the millimeter range and the depth of the wave is about 2-3 μm for FR-4 or FR-5. Local undulation occurs in the build-up process when a dielectric film is applied on an underlying copper patterned circuit layer. The rough surface will impact the fine line formation but the roughness is necessary to ensure adhesion between the dielectric film and the copper trace.

Non-planar or undulating surface effect: Experiments showed that the undulating surface caused difficulties in fine line photo-resist patterning. This is shown in Figure 5.28, where the bottom layer is a comb structure with a 200- μm pitch coated with a layer of dielectric film. The top is a layer of developed dry film photo-resist with 10 μm line and space and 15 μm thickness. It can be seen from the figure that the removal of photo-resist is not uniform during the photo-resist developing. The photo-resist is opened very well on the top of copper traces while closed in the valleys between copper traces. The surface topography of such a surface, as measured by a Dektak-3030 Surface Profiler, was of the order of 5 μm .

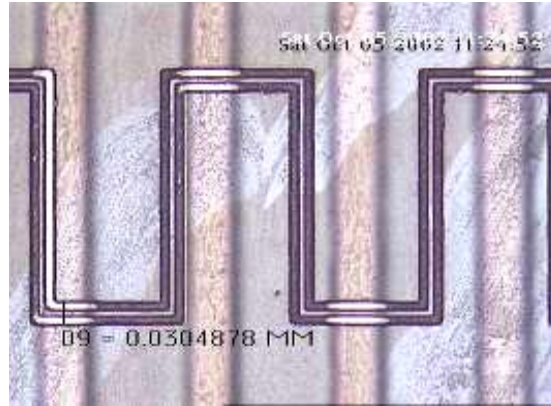


Figure 5.28 Non-planar surface, due to thick copper trace under the dielectric layer, resulting in photolithography non-uniformity for 10µm lines/spaces in 15µm thick photoresist.

Light Scattering and “Bridge” effect: There are two main causes of UV light scattering at the dielectric or substrate surface. One is the scattering at the edge of the fine line due to excessive local roughness in the dielectric surface. This can be caused by filler particles in the dielectric or by overetching during the chemical or plasma surface treatment process for electroless copper plating. The other cause of scattering is the lack of uniform mask-to-photoresist contact (in contact mode) or variation in mask-to-photoresist gap (in proximity mode). This effect can result from global warpage, and global or local undulations. As the photoresist opening dimension decreased, it was observed that there were some unexpected extremely thin resist film remaining in the spaces of resist relief after development. They look like a “bridge” as seen in Figure 5.29.

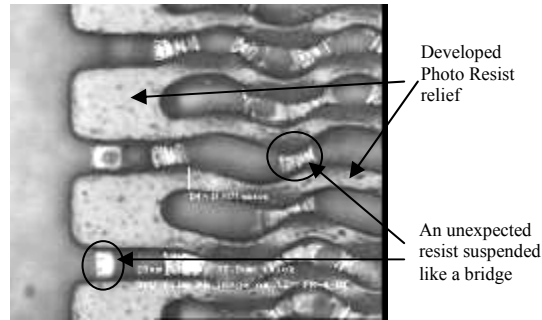


Figure 5.29 “Bridge” effect showing very thin photoresist film remaining in the opening

UV light was blocked by the opaque mask printed features in these areas and no photo resist should have been exposed and since a negative acting resist was used, the relief areas should be completely dissolved away in the developer. It is suspected that some of the scattered UV light may get trapped in the gap between photo mask and photo resist, as illustrated in Figure 5.30. When a beam 1 or 2 scatters near the opaque area, these scattered light may enter the gap beneath the opaque area and then propagate in the gap due to reflection. The light may cause a thin layer photo resist to be exposed, but the scattered light intensity was not strong enough to sufficiently cross-link all the resist down to the bottom. It in effect cross-linked very thin layers on the top of the resist, thus resulting in a piece of very thin film suspended across the resist relief like a bridge. In addition, these bridges were observed at much higher density in narrower spaces than in wider spaces. This is because either there was not sufficient scattered light to cross-link the larger resist gaps or the wider bridges were broken during development.

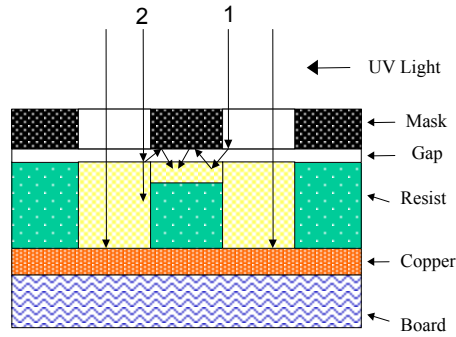


Figure 5.30 Explanation for bridge effect in narrow photoresist spaces by UV light scattering between mask and resist under the opaque areas of the mask

Adhesion related effects: The displacement of the photo resist pattern and the lift-off of photo resist strip from the seed layer due to poor adhesion are more prevalent when the width of the photoresist feature becomes smaller in geometry, as shown in Figure 5.31. This occurs due to the smaller contact area between the photo-resist feature and the seed layer resulting in weaker adhesion. Due to the same reason, plated copper lines tend to peel off from the dielectric film as they become finer. To counteract this, surface roughness treatments or chemical bond enhancement are necessary to improve the adhesion. The combination of smoother interface requirements for lower signal loss and finer lines/spaces for routing density will continue to present significant challenges to package substrate density improvements in the future.

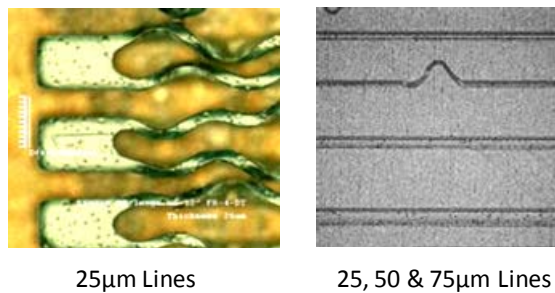


Figure 5.31 (a) & (b) Fine line photoresist lifting caused by insufficient adhesion

After careful optimization of the above mentioned processes, *i.e.* photolithography, interfacial roughness treatment, electroless and electrolytic plating, sub-10 μm lines and spaces with 1:1 and higher aspect ratios were demonstrated using Eagle NT-90 liquid photoresist on organic substrate as shown in Figure 5.32 (4 μm Cu thickness) and also shown earlier in Figures 5.26 and 5.27. Figure 5.33 illustrates a microsection of a series of 10 μm lines/spaces with high aspect ratio (18 μm plated copper thickness) fabricated using DuPont Riston JSF1C15 dry film.

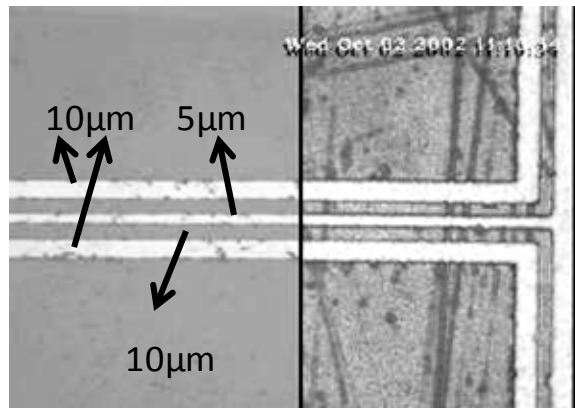


Figure 5.32 Comparison of glass mask (left) and plated copper (right) for a structure with 5 μm and 10 μm lines/spaces on a epoxy build-up layer on FR-4.

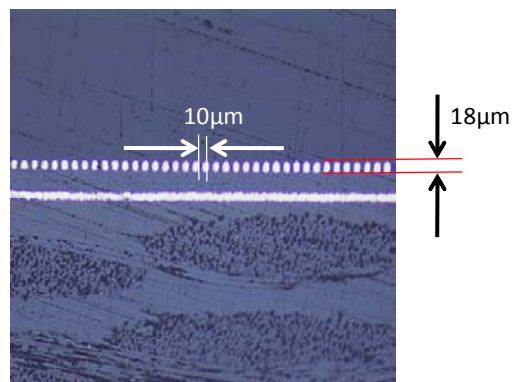


Figure 5.33 Microsection of high aspect ratio plated copper fine lines with 10 μm line/space and 18 μm copper thickness

5.4. New sub-10 μ m Copper Conductor Surface Treatment Process

Once the SAP process is completed, the substrate is ready for the next dielectric layer fabrication in the case of multilayer build-up substrates. Before the second build-up dielectric polymer is applied, the copper patterns must go through a surface treatment process for enhancement of the 2nd dielectric polymer to copper trace adhesion. This is required because the surface of the electroplated copper traces is very smooth due to organic additives in the plating bath, and without any roughening or bond enhancer, the multilayer structure will delaminate during reliability testing. The typical process steps after SAP prior to additional build-up layer processing are shown in Figure 5.34.

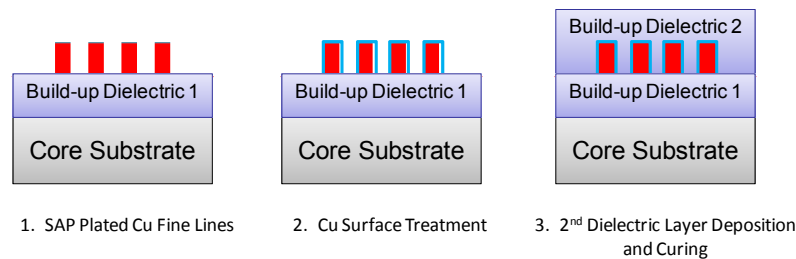


Figure 5.34 Process Sequence from SAP to Subsequent Build-up Layer Fabrication

The roughness of the copper has to be carefully controlled not only to ensure good reliability and peel strength, but also for best electrical performance.

5.4.1. Advanced Copper Surface Treatment Process Description

Traditional methods of microetching copper to achieve improved adhesion to build-up dielectrics are soon to be unsuitable for meeting the requirements of advanced IC-substrates. Figure 5.35 shows an example of conventional treatment to achieve such adhesion and to ensure reliability. However, because of concerns regarding signal

attenuation for high-frequency applications, such conventional methods are rapidly reaching their capability limits.

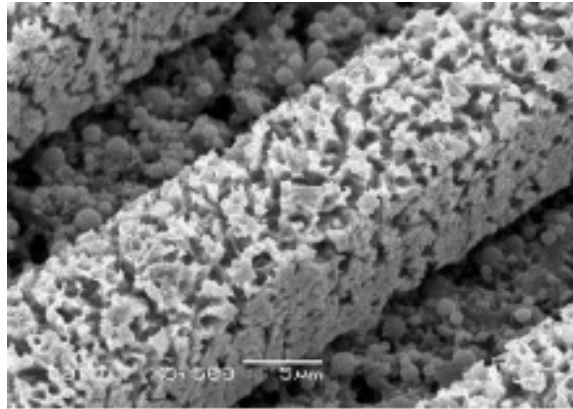


Figure 5.35 SEM micrograph of a 12µm wide copper conductor chemically treated with a conventional micro-roughening process for adhesion.

As line and space geometries are reduced to less than 10µm it is becoming a challenge to concurrently achieve excellent adhesion, ensure thermal performance, and minimize surface roughness. For fabrication of lines and spaces in dimensions below 10µm, a non-etching adhesion promotion process will be necessary. The Secure™ HFz process represents an innovative approach to enhancing the bonding of currently used build-up films and solder masks while not significantly altering the copper conductor to promote adhesion. Instead, the new process uses a silane-based chemical adhesion promoter to achieve the desired results. The Secure™ HFz process sequence and key process parameters are summarized in Table 5-3⁴³.

Table 5-3. Secure™ HFz Process

Process	Time	Temp
	(sec)	(°C)
Alkaline Clean	30	50
Rinse		RT
Acid Clean	30	40
Rinse		RT
Immersion Tin	30	30
Rinse		RT
Anti-Drag In		RT
Silane Filming	20	25
Drying		60

Alkaline Clean - This process step provides aggressive cleaning for the removal of organic residues (i.e. dry film photoresist) and fingerprints.

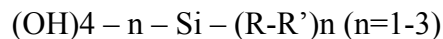
Acid Clean - This step provides removal of heavy oxides, anti-tarnishes or surfactants from the copper surface prior to immersion tin deposition.

Immersion Tin - The immersion tin step deposits 0.05 - 0.15µm of pure tin on the copper surface. Not strictly an immersion reaction, the process can be more accurately described as a blend of “immersion” and “electroless” processes, involving the use of a reducing agent to promote deposition of tin. Furthermore, the process is not strictly “non-etching”, although significantly less copper is removed in comparison to conventional etching processes.

The tin oxide/hydroxide represents a more suitable interface because stronger polar bonds can be formed between the oxide/hydroxide. The polar groups within the substrate and the tin hydroxide groups serve as a convenient anchor for further chemical modifications to build strong covalent bonds to the organic resins.

Silane Filming – Following the formation of an even tin-oxide layer, an aqueous solution of organosilanes is then applied and immediately dried.

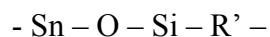
The organosilane adhesion promoter has the ability to form covalent bonds to the tin hydroxide (Sn-OH) as well as to the organic resin, which results in a strong interface linking copper and resin. The organosilanes of the following general structure have been found to be suitable couplers:



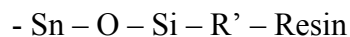
Where: R = Organic Bridge

R' = Functional Terminal Group

These organosilanes form strong bonds with the metal oxides:



During the lamination process, strong covalent bonds are formed between the silanes and the resin:



As described, all adhesion is derived from the organosilane mixture and no etching or roughening of the copper is required to achieve adhesion. Such a condition is ideal for high frequency applications by reducing signal losses and meeting more stringent controlled impedance requirement.

5.4.2. Copper Adhesion Process Testing Results

The surface roughness of 12 μ m wide copper lines were characterized by Atomic Force Microscopy (AFM) before and after the Secure HFzTM silane treatment. Figure 5.36 shows an SEM photo of a typical 12- μ m conductor prior to adhesion promotion treatment.

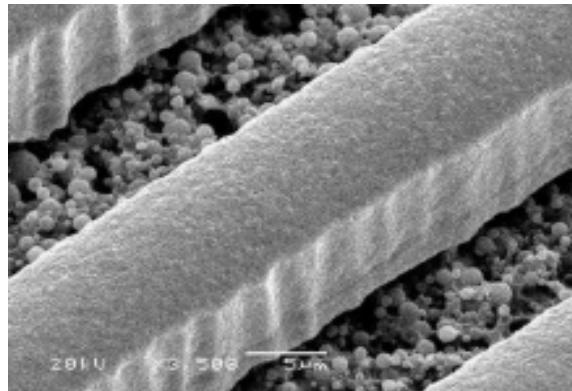


Figure 5.36 12- μ m conductor before adhesion promotion treatment

Roughness and Dimension Analysis: Table 5.4 presents the results of atomic force microscopy (AFM) surface analysis, showing changes in roughness before and after treatment, as well as for other surface treatment techniques. As shown, the surface roughening of the silane process is significantly less than that achieved with other methods.

Table 5.4 AFM Surface Analysis Before and After Copper Surface Treatment

Condition:	Roughness (in microns)		
Process	R _a	R _{ms}	R _z
Before Treatment (after SAP)	0.03	0.04	0.28
BondFilm® (Current Etch Based)	0.41	0.39	2.94
Secure™ HFz (New Silane Based)	0.05	0.06	0.30

Figure 5.37 shows an SEM photo of a typical 12- μ m conductor after adhesion promotion treatment using the silane process. Statistically, after treatment, the conductor surfaces are non-etched and maintain excellent shape characteristics for high-frequency applications.

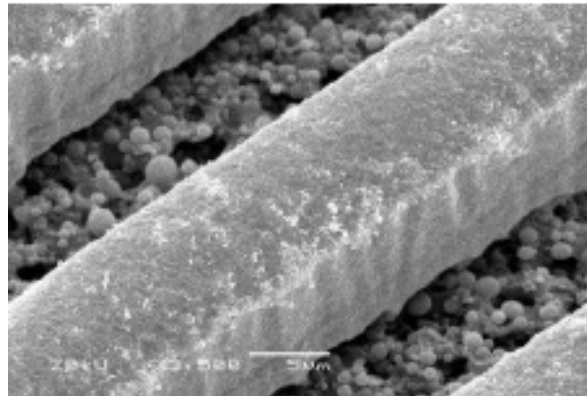


Figure 5.37 SEM micrograph of 12 μ m line after treatment with silane filming process

Adhesion Analysis: To measure adhesion, peel strength investigations were performed using lamination of Ajinomoto ABF GX13 epoxy dry film dielectric to copper conductors treated with the silane process. Peel strength measurements were performed both before and after highly accelerated stress testing (HAST). Peel strength of 0.8-

0.9kgf/cm was measured before and after the reliability testing. The adhesion characteristics of the epoxy dielectric to copper was very robust with excellent peel strength before and after HAST.

5.4.3. Advanced Silane Treatment Process for sub-10 μ m Lines/Spaces

The Sn-silane copper surface treatment process was applied to sub-10 μ m lines and spaces formed by SAP process described earlier for the first time to understand the impact on line dimension changes of super-fine lines. The SAP plated copper traces were approximately 6-7 μ m in thickness and were designed to target values of line and space from 5 μ m up to 12 μ m. There was some amount of deviation from designed line widths from the photomask fabrication process since a lower cost glass photomask with +/-1 μ m critical dimension (CD) was used for UV lithography of negative acting liquid photoresist. There was an additional dimensional variation introduced by the lithography and SAP seed layer etching process, most of the deviation coming from the microetch to remove the electroless copper seed layer of ~0.5 μ m thickness. The results from line width measurements using high resolution scanning electron microscopy are shown in Table 5-5, which also includes results from a conventional micro-etch based roughening treatment for lines and spaces below 10 μ m. The results indicate that the bond film etch treatment resulted in a line width reduction of at least 1-2 μ m and optical inspection also indicated that the line edges were quite rough and irregular for these ultra-fine lines. As seen in the table, the smallest lines of 5-6 μ m width were completely etched away during the microetching process. However, the silane non-etching treatment process resulted in minimum amount of dimensional change, and the deviations seen are within the error margin of the measurement technique.

Table 5-5. Line Width and Space Measurements of Untreated and Silane Treated Copper Fine Lines and Comparison to Bond Film etch based adhesion treatment

Process: (Line/Space)	Target 6/6	Target 8/8	Target 10/10	Target 12/12
Untreated	4.3/6.2	6.8/8.7	9.5/10.6	10.1/13.0
Sn/Silane (Secure HFz™)	4.3/6.8	7.4/9.3	9.3/10.6	10.5/12.8
Micro Etch (Bond Film™)	n/a	6.2/9.9	7.4/11.8	9.3/13.6
<i>Average of 3 measurements in microns (+/-0.5μm)</i>				

An advanced silane coupling agent based adhesion enhancement process for sub-10μm copper lines was successfully demonstrated down to 5μm line/space as shown in the SEM images in Figure 5.38.

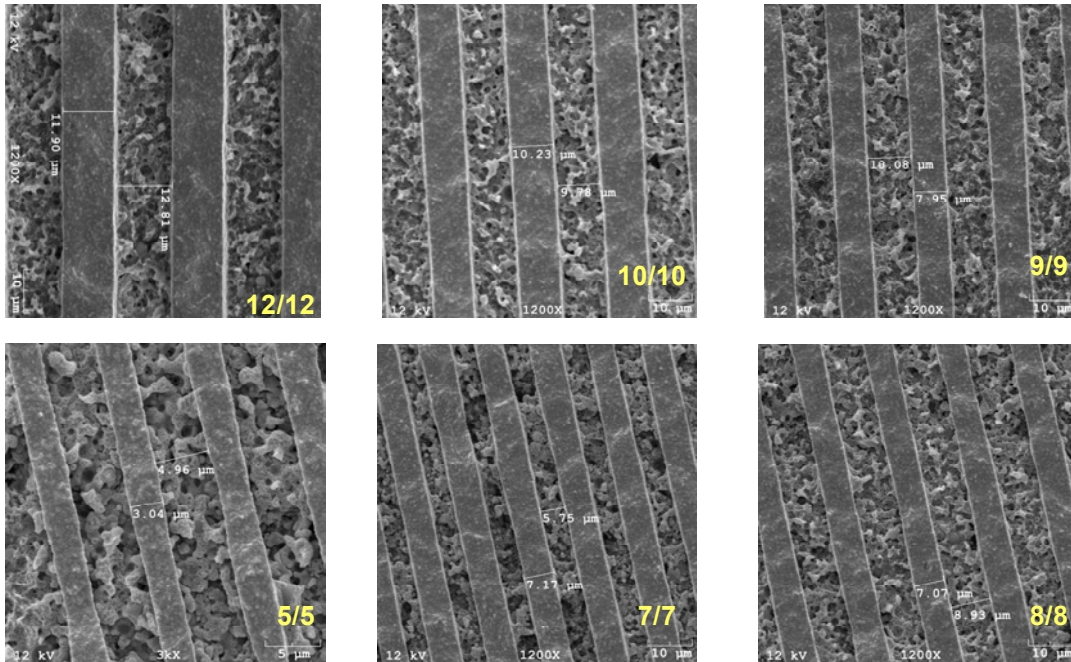


Figure 5.38 SEM micrographs of 5-12μm lines/spaces after Sn-silane treatment

5.5. Chapter Summary

The objectives for the research in this chapter were to explore and demonstrate sub-10 μm lines and spaces on epoxy and low loss build-up dielectrics. The control of the four interfaces of a rectangular cross-section of the copper fine line conductor was successfully demonstrated, with line widths and spaces from 10 μm down to 5 μm achieved via advanced next generation photoresists, lithography and semi-additive processes. A comparison of the surface profiles obtained from the various surface modification processes discussed in this chapter is shown in Figure 5.39. Based on these results, potential materials and processes have been identified to meet the needs for the next generation of high performance and high density SOP and package substrates.

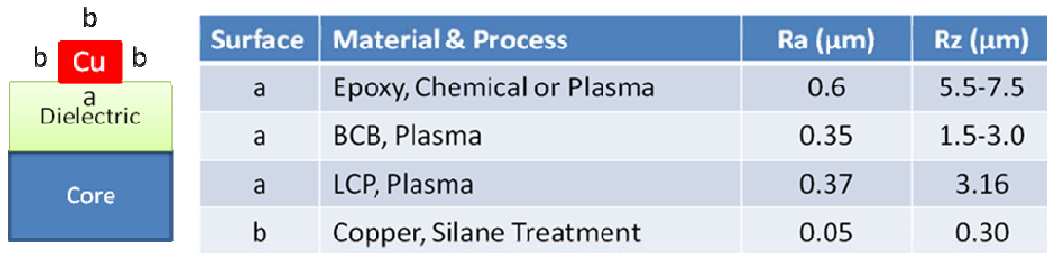


Figure 5.39 Conductor cross-section (left) and summary (right) of interface roughness measured for various materials and processes

CHAPTER 6
NEXT GENERATION ADVANCED ORGANIC SUBSTRATE INTEGRATION
RESEARCH

The starting point for the integration research was the completion of optimized baseline processes for each of the major process elements in the fabrication of multi-layer high density substrates. The integration focus was to bring together a combination of low CTE cores (C-SiC, Cu-Invar-Cu, low CTE laminate), low loss build-up dielectric (LCP, BCB, RXP-4) and excimer/UV laser via ablation and SAP metallization processes established in Chapters 2-5. During the course of the fundamental research involving advanced low loss dielectrics, ultra-small microvias and super-fine lines, several application specific test vehicles were fabricated for both high I/O density digital IC packages, and high frequency RF packages. The integration research summary is presented in this chapter in three sections on BCB, LCP and RXP low loss dielectric polymers either deposited on a variety of low CTE core substrates or as coreless/thin core organic substrates.

6.1. Coreless and Low CTE Core LCP Substrates

The first stage of the substrate process for LCP was the fabrication of two metal layer coreless and flexible substrates with embedded high quality factor RF passives. The process steps include excimer laser ablation of 25-100 μ m diameter microvias in 25-50 μ m thick LCP cores, followed by plasma surface treatment, electroless copper seed layer plating and SAP or subtractive etch process for defining fine lines.

Figure 6.1 shows the photographs of completed single LCP layer flexible substrates with microvia interconnects and a series of RF capacitor and inductor structures which were used to develop design library of these high quality factor components for wireless front end packages and modules.

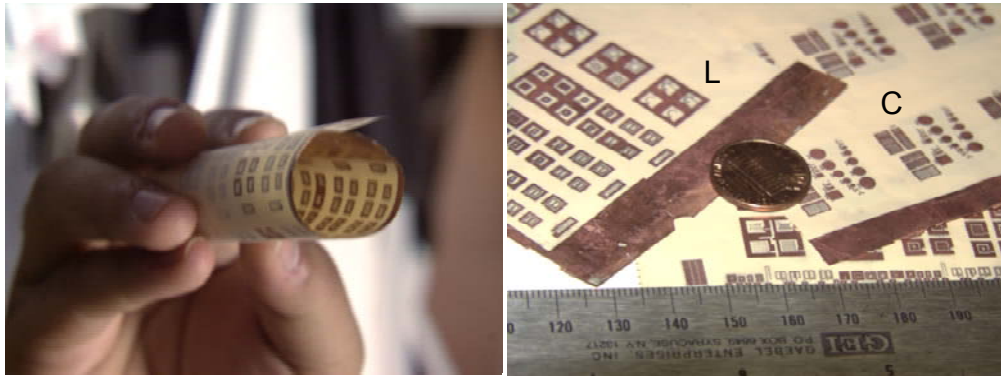


Figure 6.1 Two Metal Layer High Density LCP Substrate with Embedded RF Passives

The capacitor structures used for high frequency testing in the 1-10 GHz range are shown in Figure 6.2 including microvias for ground connections. High frequency vector network analyzer (VNA) measurements confirmed that the LCP substrates after all processes were completed still maintained the low loss properties of the starting dielectric and quality factors as high as 380 were measured as shown in Table 6.1.

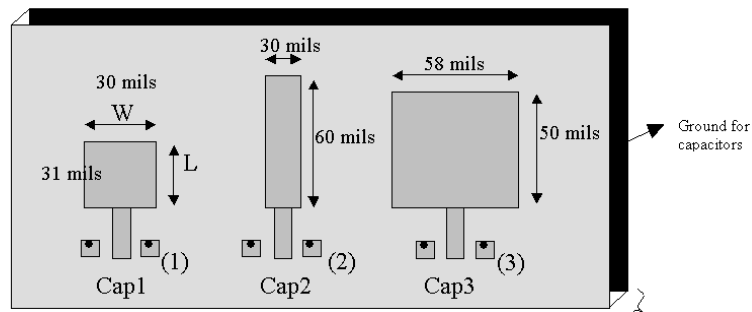


Figure 6.2 Capacitor Structures in Two Metal Layer LCP Substrate with Microvias

Table 6.1 High Frequency Measurement Results for Embedded RF Capacitors in 50 μ m thick LCP

Capacitor	Capacitance (pF) @1-2GHz	Q at 1 GHz	Q at 2 GHz
Cap 1	0.60	380	350
Cap 2	1.14	330	300
Cap 3	1.75	300	260

One of the beneficial mechanical properties of LCP is its low CTE without any fillers due to the self-reinforcing nature of the liquid crystal rigid rod structure. The typical CTE of LCP dielectric is around 17-20 ppm/ $^{\circ}$ C, and this enables the use of LCP as a build-up dielectric on low expansion rigid cores without significant CTE mis-match from core to build-up film. This concept was used to fabricate test substrates with a Cu-Invar-Cu low CTE (\sim 4-6ppm/ $^{\circ}$ C) core with thickness of 100 μ m and multiple layers of 50 μ m thick LCP dielectric laminated on both sides of the core at 282-287 $^{\circ}$ C. The composite CTE of this 1mm thick substrate was anticipated to be 8-12ppm/ $^{\circ}$ C, which is ideal for 1st level fine pitch flip chip and 2nd level BGA to FR-4 reliability. As shown in Figure 6.3, a flip chip test die with 200 μ m pitch solder based interconnects (PB-8) were assembled and working interconnects were shown on the low CTE substrate.

Figure 6.4 is a photograph of a 12"x18" six metal layer all-LCP coreless substrate fabricated using low and high melt LCP and test structure consisting of 25-100 μ m lines and spaces and microvias from 25-100 μ m diameter.

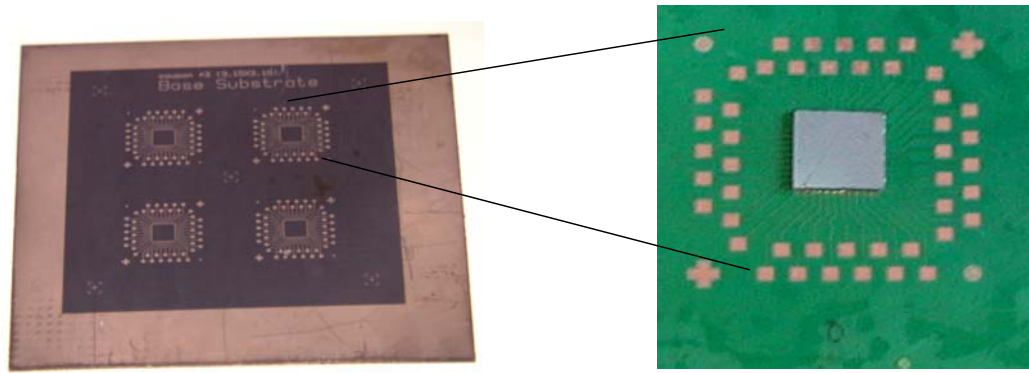


Figure 6.3 Low CTE Composite Substrate with Cu-Invar-Cu Core and LCP Dielectric (left) and after assembly of 200 μ m pitch flip chip IC (right)

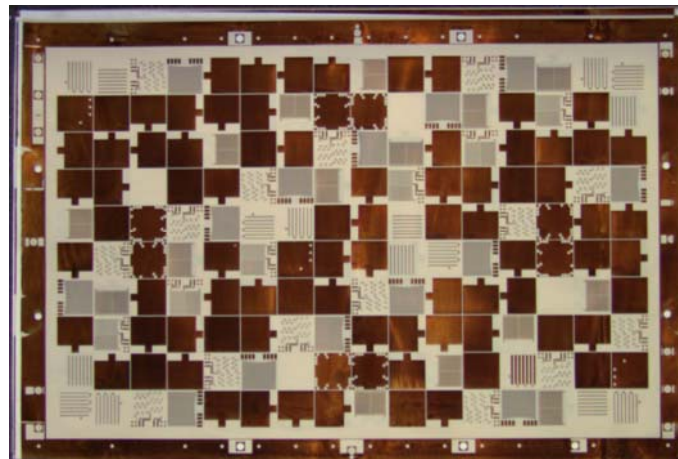


Figure 6.4 All-LCP Substrate Panel (12''x18'') with Six Metal Layer Test Structures

6.2. Thin Film BCB Build-Up on Low CTE Cores

Based on the fundamental research elements described earlier, two core substrates (Cu-Invar-Cu with PTFE laminated dielectric, and C-SiC) and BCB build-up dielectric processes were integrated using a two metal layer test vehicle with smallest dimensions of 6 μ m lines/spaces and 15-20 μ m microvias in th BCB layer. The process steps for this integration consisted of:

1. CIC-PTFE or C-SiC substrate planarization using polyimide or speedboard lamination
2. SAP process for first metal layer using electroless copper seed layer, liquid photoresist, and electroplated traces (4-5 μ m finished thickness)
3. BCB spin coating and curing for 9-10 μ m thickness
4. Excimer laser via ablation using NT-90 photoresist conformal mask
5. Plasma surface treatment and electroless copper plating on BCB
6. Semi-Additive plating process including photolithography for 5-10 μ m lines/spaces

Figure 6.5 shows a top view of the fabricated CIC-PTFE substrate with BCB build-up layers (left) and microsections of the completed BCB build-up layer structure on two core substrates, C-SiC with planarization layer (middle) and CIC-PTFE(right). Microvias of 20 μ m diameter and 6 μ m lines/spaces were demonstrated as part of this test vehicle.

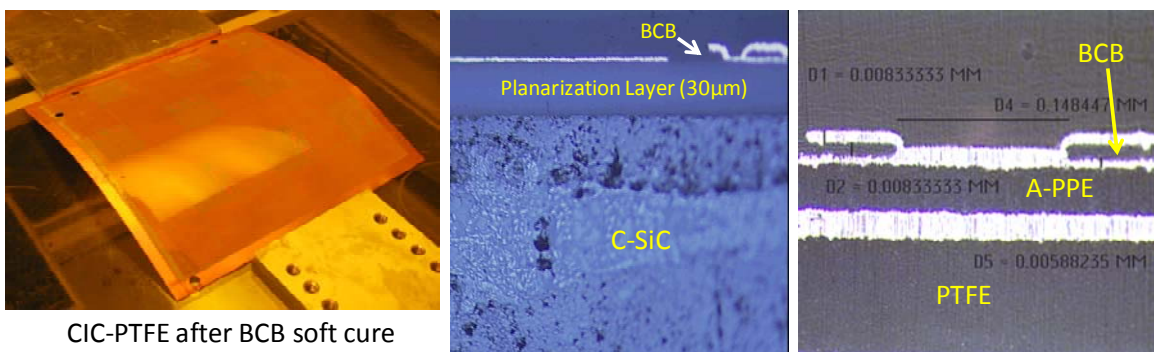


Figure 6.5 Top view of BCB coated on CIC-PTFE Core (left), and microsections of completed BCB build-up substrate on C-SiC (middle) and CIC-PTFE (right)

6.3. Ultra-Thin Low Loss Substrate with RXP Thermoset Core and Build-up Layer

The RXP-4 build-up dielectric process using UV laser ablation and electroless and electrolytic semi-additive process for metallization was integrated with a thin core (100 μm thickness) made of glass reinforced low loss resin (RXP-1 laminate) which is compatible with the build-up dielectric. Figure 6.6 is a leading edge demonstration of a four metal layer structure consisting of 50 μm diameter through vias in the core filled with electroplated copper, and 50 μm diameter blind microvias in RXP-4 dielectric (25 μm diameter vias were also successfully fabricated and tested).

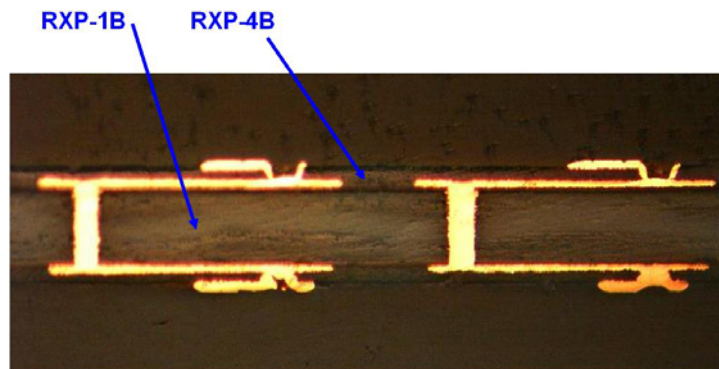


Figure 6.6 Ultra-Thin Four Metal Layer High Density and Low Loss RXP based Organic Substrate

CHAPTER 7

SUMMARY AND CONCLUSIONS, FUTURE WORK

The main objectives of this thesis were to bridge the IC to package interconnect gap by pushing a set of materials and process technologies on an organic substrate platform. A hybrid approach was used, combining fundamental understanding of materials-processing-structure-property relationships with the many constraints of “manufacturable” technologies to arrive at a unique set of solutions that have the potential to extend the reach of current low-cost organic substrates well into the next few generations of IC and systems packaging roadmaps. The highly integrated System-on-a-package (SOP) concept for multi-functional and micro-miniaturized systems packaging was a driving force behind the multi-faceted approach presented here.

This dissertation research started with the realization that the current set of industry standard polymer dielectrics and multilayer wiring organic substrate processes and structures could not keep up with the escalating density and performance demands of semiconductors driven by Moore’s law, and systems driven by component and function density increases. First, a new set of candidate materials and processes were identified based on long term roadmap target parameters for wiring density (lines/spaces, via diameter), high frequency performance (low dielectric constant, low loss tangent), and thermo-mechanical reliability (low CTE, high planarity). The core materials studied consisted of both existing (Cu-Invar-Cu), and emerging (C-SiC, low CTE laminates) materials with low CTE and high modulus. A brief discussion on planarization and other surface treatment processes for the new core materials in preparation for build-up processes was covered in Chapter 2.

The first major focus area of the thesis was on planarization, 10-30 μ m microvia formation and metallization of a set of low loss dielectric polymers (LCP, BCB, RXP-4) with properties (e.g. loss tangent <0.005) capable of significantly enhancing package and system performance. BCB has been used in microelectronics applications since the late 1980s and is a well studied polymer. Novel advanced processes were explored to be able to process BCB using industry infrastructure for low-cost organic package substrates, as opposed to wafer-scale processes that have been used widely for BCB. The first process was excimer laser microvia ablation using a 308nm XeCl laser source, and 20 μ m diameter vias in 10 μ m thick BCB films were successfully demonstrated. A fundamental understanding of the laser-polymer interaction mechanisms was key to achieving the targets and showed that the excimer laser process is highly scalable due to the purely photo-chemical nature of ablation. Although a minimum via diameter of 15 μ m was achieved, with the right set of optics and laser source, the excimer laser system can scale down to sub-10 μ m vias using mass via generation, which will become more viable over point-to-point drilling systems in the future if via densities continue to multiply at a high rate. The second unique contribution for BCB was to explore and demonstrate a wet seed layer metallization process for BCB using plasma modified surfaces and low stress electroless copper plating process.

The next material explored was liquid crystal polymer, a thermoplastic with enormous potential not only as flexible or rigid substrates for high frequency low loss packaging, but also environmentally friendly due to the ability to recycle and being naturally halogen free without the need for any flame retardants. Pioneering research in demonstrating all the major substrate processes including lamination/planarization, laser via ablation, and metallization were demonstrated and microvia diameters as small as 20-25 μm were demonstrated. The LCP substrate research in this thesis formed the basis of commercialization activities for RF SOP modules with embedded high Q passive components for wireless radio applications.

Finally, a new thermoset polymer, RXP-4, with unique low loss properties based on hydrocarbon backbones was explored and lamination, UV laser ablation and metallization processes were demonstrated for 25 μm diameter microvias in 9 μm and 18 μm dielectric thickness.

The second major contribution from this research was in the area of sub-10 μm copper super-fine line conductors. A comprehensive study of dielectric surface modification for epoxy, BCB and LCP was presented using chemical and plasma treatments. A detailed study of the effects of various global and local non-planarity common in organic substrates, on the ability to lithographically image sub-10 μm lines was presented, and this knowledge should assist in designing an improved set of materials and processes for future organic substrates. A novel copper surface treatment process using silane coupling agents was used for sub-10 μm lines and good adhesion enhancement was shown without any damage or line width change to the super-fine lines.

Finally, a set of baseline integration process flows were developed using various test structures and test vehicles, for the following integrated substrates: (a) multilayer LCP coreless and low CTE core substrates, (b) BCB thin film wiring on C-SiC and CIC cores, and (c) ultra-thin and low loss substrates with RXP-4 build-up on RXP thin core laminate.

7.1 Future Work

There were several challenges identified as an outcome of this dissertation for future microelectronics packaging. A major barrier for adoption of high performance and low loss polymer dielectrics continues to be the concern over the cost of synthesizing these complex polymer films. Environmental regulations including halogen free requirements are forcing the use of certain additives that adversely affect electrical properties. Additionally, dry films are the de-facto standard in high volume substrate manufacturing and miniaturization demands necessitate the availability of newer polymer dielectric thin films with low loss, low cost, ease of via and metal processing, and target thickness per layer of 5-10 μ m. Finally, with the migration to lower and lower CTE package substrate cores and towards coreless substrates, the polymer build-up films must have low CTE in the range of 10-25 ppm/ $^{\circ}$ C and there are very few polymers in production or R&D today that can achieve this without ceramic fillers.

The use of ceramic fillers and polymer roughening treatments for improving thermo-mechanical reliability continues to present unprecedented challenges as line widths move into the sub-10 μ m domain.

Although 5-10 μ m line widths were demonstrated in chapter 5, the increasing cost of higher resolution lithography materials (photoresists), litho tools and cleanroom costs pose a threat to dimensional scaling in packages. Since package substrates continue to remain much larger in form factor than ICs, the cost structure of semiconductor like processes like lithography may not be viable for package substrates for future nodes.

Finally, one of the barriers for organic substrates continues to be the poor dimensional stability and through via pitch limitations of current materials and processes. The emergence of through silicon via (TSV) technology and dramatic pace of infrastructure investments in TSV formation and metallization offers a major opportunity to leverage silicon as a substrate platform for future SiP, SOP and other miniaturized 3D packaging. However, a whole new set of package-friendly processes must be developed for thin silicon cores with fine pitch TSVs for Si substrates and interposers to be cost effective as a replacement for organic cores.

CHAPTER 8

SCIENTIFIC AND TECHNICAL CONTRIBUTIONS

The major fundamental scientific knowledge and new technology solutions generated as a result of this thesis research are shown in the following list.

8.1 Unique Basic Research Contributions

1. Fundamental evidence on excimer and UV laser interaction with current (BCB, epoxy) and new low loss polymer dielectrics (LCP, RXP-4) to enable sub-25 μm diameter microvias for future high density and high performance packages.
2. Chemical and plasma surface modification of low loss polymers (LCP, BCB) and surface analysis, including effect of fillers, to achieve $<0.5\mu\text{m}$ average roughness for simultaneously improving copper adhesion to low loss polymers and signal integrity at high frequencies.
3. Comprehensive analysis of impact of dielectric and substrate surface effects and photoresist materials/process parameters on low-cost Hg lamp UV lithography to push organic substrate wiring technology limits below 10 μm dimensions.
4. Explored the effect of copper super-fine line adhesion enhancement treatment processes for sub-10 μm geometries through surface analysis.

8.2 Pioneering Technical Innovations Demonstrated

1. Integration of low CTE cores and low loss, thin film build-up dielectrics for high density and high frequency package substrates with high reliability

2. BCB: Demonstrated low-cost process methods to enable the adoption of BCB for organic substrates as opposed to silicon substrates (prior art).
 - a. Developed a new process for excimer via ablation ($<20\mu\text{m}$ via diameters) in low loss BCB thin films
 - b. Developed a new process for non-vacuum metallization using electroless copper seed plating on BCB
3. LCP: Several new processes for multilayer RF substrates using LCP were developed for the first time.
 - a. Excimer laser ablation of $25\mu\text{m}$ microvias in LCP
 - b. Electroless copper (non-vacuum) metallization of LCP
 - c. Controlled lamination process for multilayer LCP substrates
4. Demonstrated for the first time super-fine lines and spaces ($5\text{-}10\mu\text{m}$) via low cost lithography and plating processes on several build-up dielectrics and a robust copper surface treatment process that maintains the line widths down to $5\mu\text{m}$.
5. Pushed the leading edge of organic package substrates by at least a factor of 2x in density in terms of line width and via size reduction.

8.3 Integration Research Contributions

1. Demonstrated an end-to-end baseline process for high density LCP substrates with microvias for RF substrates and commercialized the technology.

2. Demonstrated a BCB baseline process compatible with current industry infrastructure for organic substrates.
3. Demonstrated an ultra-high density and ultra-thin and high performance four metal layer substrate using RXP thermosetting low loss dielectric with substrate total thickness <math><200\mu\text{m}</math>, 25 μm microvias, 10 μm copper lines/spaces

8.4 Publications, Honors and Awards

- Lead Author, Chapter 7, SOP Substrate in “System on a Package Technology”, Book editors Rao Tummala, Madhavan Swaminathan
- 9 Peer-Reviewed Journal Papers
 - (REVIEW PAPER ON MICROVIA TECHNOLOGY) Sundaram, V.; Tummala, R.R.; Fuhan Liu; Kohl, P.A.; Jun Li; Bidstrup-Allen, S.A.; Fukuoka, Y.; “Next-generation microvia and global wiring technologies for SOP”, *IEEE Transactions on Advanced Packaging*, Volume: 27, Issue: 2, May 2004, Pages: 315 – 325.
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- Over 60 Conference Publications (some peer-reviewed)

- Invited Talks and Papers
 - Plenary Session Invited Talk: Venky Sundaram, Rao Tummala, “Recent Advances in Materials and Processes for SOP”, IEEE-CPMT Technical Committee on High Density Substrates, 54th ECTC Conference, Las Vegas, NV June 2, 2004
 - Rao R. Tummala, Kenichi Shintotani, Venky Sundaram, Swapan Bhattacharya, George White, Fuhan Liu, P.M. Raj, Lixi Wan, Seock Hee Lee, D. Ravi, “SOP vs. SOC at Georgia Tech PRC”, *Invited Paper* in *ICEP 2001 Conference*, Japan, April 2001.
- Five issued US Patents and Three US Patents Pending
- Eight Additional GT Invention Disclosures Submitted
- Best Paper Awards
 - Outstanding Poster Paper, 54th ECTC Conference, Orlando, FL, June 2005
 - 2004 IEEE Transactions on Advanced Packaging Commendable Paper Award from IEEE-CPMT Society
 - Best Student Paper Award, Asia-Pacific Microwave Conference, December 2005

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