

HIGH POWER-SUPPLY REJECTION CURRENT-MODE LOW-DROPOUT LINEAR REGULATOR

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**HIGH POWER-SUPPLY REJECTION CURRENT-MODE
LOW-DROPOUT LINEAR REGULATOR**

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To My Family

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS	iv
LIST OF TABLES	vii
LIST OF FIGURES	viii
LIST OF SYMBOLS AND ABBREVIATIONS	x
SUMMARY	xi
<u>CHAPTER</u>	
1 INTRODUCTION	1
1.1 Power Management Overview	1
1.2 Linear Regulators	3
1.3 Relevant LDO Characteristics	5
1.4 LDO Design Challenges	8
1.5 Research Objective	11
1.6 Synopsis	12
2 POWER SUPPLY REJECTION IN LDO REGULATORS	13
2.1 PSR Analysis	13
2.2 Supply Ripple vs. Spikes	16
2.3 State of the Art	17
2.4 Proposed Current-Mode Architecture	21
2.5 System-Level Current-Mode LDO Regulator	22
2.6 Synopsis	24

3	CURRENT-MODE LDO REGULATOR IC	25
3.1	Transistor-Level Implementation	25
3.2	Stability Analysis	26
3.3	PSR Analysis	32
3.4	Achieved Design Performance and Layout Challenges	36
3.5	Synopsis	37
4	EXPERIMENTAL RESULTS AND CONCLUSIONS	39
4.1	PCB Design and Testing Environment	39
4.2	PSR Measurement Results	40
4.3	Transient Measurement Results	42
4.4	Evaluation of the Proposed Architecture	45
4.5	Conclusions	47
4.6	Recommendation/Future Research	49
	APPENDIX A: MATHEMATICAL ANALYSIS OF DUAL-LOOP FEEDBACK SYSTEMS	50
	REFERENCES	52

LIST OF TABLES

Table 3.1: Current-mode LDO regulator's specification matrix	36
Table 4.1: Comparison of the proposed topology against the state of the art	47

LIST OF FIGURES

Figure 1.1: Conceptual step-down converters.	2
Figure 1.2: Comparison of different pass element structures.	3
Figure 1.3: A conventional LDO regulator.	5
Figure 1.4: (a) A conventional LDO regulator and (b) Its frequency response.	9
Figure 2.1: A conventional LDO regulator and (b) Its intuitive PSR model.	13
Figure 2.2: PSR response across wide frequency range.	15
Figure 2.3: Comparison between power-supply ripple and spikes.	16
Figure 2.4: (a) State-of-the-art techniques and (b) Their corresponding PSR response.	18
Figure 2.5: Feedforward ripple-cancellation technique.	20
Figure 2.6: System-level current-mode LDO regulator.	22
Figure 3.1: Transistor-level schematic of the proposed current-mode architecture.	26
Figure 3.2: Frequency response of the two feedback loops.	29
Figure 3.3: Frequency response of the current loop (LG_I) at 5mA load.	30
Figure 3.4: Frequency response of the voltage loop (LG_V) at 5mA load and 15nF output capacitor.	32
Figure 3.5: (a) Intuitive PSR model and (b) PSR analysis of current-mode regulator.	33
Figure 3.6: PSR response ($I_L=5mA$ and $C_O=68nF$) comparing current-mode vs. conventional regulator.	35
Figure 3.7: Micro photograph of the fabricated IC.	37
Figure 4.1: Measured PSR response of the proposed current-mode regulator with $C_O=15nF$.	40
Figure 4.2: Input ripple rejection at 2.4MHz using 15nF output capacitor.	41

Figure 4.3: PSR comparison with and without the current-feedback loop.	41
Figure 4.4: (a): PSR of current-mode LDO at 850kHz and (b) PSR of the regulator at 900kHz with the current loop disabled.	42
Figure 4.5: Positive and negative load transient response between full and no load.	43
Figure 4.6: Line transient response of the current-mode regulator.	44
Figure 4.7: Parasitic devices found in lateral PNP transistor.	45
Figure A.1: A basic dual-loop feedback control system.	50

LIST OF SYMBOLS AND ABBREVIATIONS

I_L	Load Current
R_L	Load Resistor
V_{REF}	Reference Voltage
V_{DO}	Dropout Voltage
R_{o-OL}	Open-Loop Output Resistance
C_O	Output Capacitor
A_{IN}	Supply Gain
A_{OL}	Open-Loop Gain
A_{CL}	Closed-Loop Gain
LG_I	Loop Gain of the Current Loop
A_{OL-I}	Open-Loop Gain of the Current Loop
A_{CL-I}	Closed-Loop Gain of the Current Loop
LG_{V-wI}	Loop Gain of the Voltage Loop with the Current Loop
LG_{V-woI}	Loop Gain of the Voltage Loop without the Current Loop
LDR	Load Regulation
LNR	Line Regulation
PSR	Power-Supply Rejection
UGF	Unity-Gain Frequency
IC	Integrated Circuit

SUMMARY

Power management components can be found in a host of different applications ranging from portable hand held gadgets to modern avionics to advanced medical instrumentations, among many other applications. Low-dropout (LDO) linear regulators are particularly popular owing to their: ease of use, low cost, high accuracy, low noise, and high bandwidth. With all its glory, however, it tends to underperform switched-mode power supplies (SMPS) when it comes to power conversion efficiency, although the latter generates a lot of ripple at its output. With the growing need to improve system efficiency (hence longer battery life) without degrading system performance, many high end (noise sensitive) applications such as data converters, RF transceivers, precision signal conditioning, among others, use high efficiency SMPS with LDO regulators as post-regulators for rejecting the ripple generated by SMPS. This attribute of LDO regulators is known as power supply rejection (PSR). With the trend towards increasing switching frequency for SMPS, to minimize PC board real estate, it is becoming ever more difficult for LDO regulators to suppress the associated high frequency ripple since at such high frequencies, different parasitic components of the LDO regulator start to deteriorate its PSR performance.

There have been a handful of different techniques suggested in the literature that can be used to achieve good PSR performance at higher frequencies. However, each of these techniques suffers from a number of drawbacks ranging from reduced efficiency to increased cost to increased solution size, and with the growing demand for higher efficiency and smaller power supplies, these techniques have their clear limitations. The

objective of this research project is to develop a novel current-mode LDO regulator that can achieve good high frequency PSR performance without suffering from the aforementioned drawbacks. The proposed architecture was fabricated using a proprietary 1.5 μm Bipolar process technology, and the measurement results show a PSR improvement of 20dB (at high frequencies) over conventional regulators. Moreover, the proposed LDO regulator can supply 5mA of load current at input voltages as low as 1.4V, and the regulator only requires a small 15nF output capacitor for stability, which is far smaller than some of the currently used techniques.

CHAPTER I

INTRODUCTION

With the drive towards better system performance and higher efficiency (longer battery life), power management ICs are proliferating in portable, industrial, medical, communications, and automotive applications. These feature rich devices incorporate a variety of electronic circuitries such as high-speed digital processors, high-precision analog circuitries, and low-noise RF circuitries, among others. Each of these blocks have different supply voltage requirements, ranging from low voltage, high efficiency, and fast transient response for digital cores to low noise, high power-supply rejection (PSR), and high accuracy requirements for analog/RF components; hence the need for multiple voltage regulators to meet these diverse power-supply requirements [1], [12].

1.1 Power Management Overview

Power management can broadly be divided into two categories: i) input power management which includes battery chargers among others, and ii) output power management which includes voltage regulators. Furthermore, there are a couple commonly used topologies of voltage regulators: i) linear regulators and ii) inductor based switched-mode power supplies (SMPS) [7], [16]. Linear regulators, as shown in Figure 1.1 (a), achieve regulation by linearly controlling the impedance between the input supply voltage and the output load. It is essentially a resistive voltage divider, whereby the upper impedance is actively controlled to achieve the desired output voltage, irrespective of any changes at the input supply voltage or the load current. Depending on

the operating conditions, significant power can be dissipated in the active resistor of linear regulators; and hence, they can potentially suffer from poor efficiency.

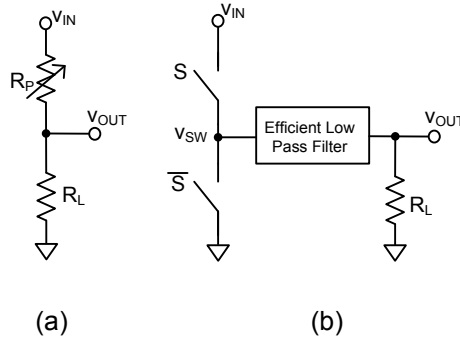


Figure 1.1: Conceptual step down converters: **(a)** Linear regulator and **(b)** Switched-mode converter.

SMPS, on the other hand, as shown in Figure 1.1(b), achieve voltage regulation by continuously turning switch S ON and OFF (at controlled duty cycles) to generate the desired output voltage. The average voltage at the v_{SW} node is a controlled fraction of the input supply voltage, and for Figure 1(b), it is given as follows:

$$V_{SW} = DV_{IN} \quad (1.1)$$

Because power is transferred to the output only when either S is completely turned OFF or is completely ON, no power is ideally lost in the conversion process. However, in order to efficiently generate a DC output voltage from v_{SW} , an efficient low-pass filter (hence inductive based) needs to be connected between v_{SW} and the output node. Although SMPS can ideally offer conversion efficiencies close to 100%, they exhibit inferior performance compared to linear regulators when it comes to noise, accuracy, bandwidth, cost, integration, and ease of use. These important reasons make linear regulators very attractive to a wide variety of applications [1], [7], [16].

1.2 Linear Regulators

A variety of different topologies of linear regulators, as shown in the figure below, can be obtained depending on how the active resistor (also known as the pass element/power transistor) is implemented. The choice and design of the pass element depends on the efficiency, maximum current, and bandwidth requirements, among others, of the application. Broadly speaking, based on process technology, the power transistor can be implemented either using a BJT transistor or a MOSFET transistor.

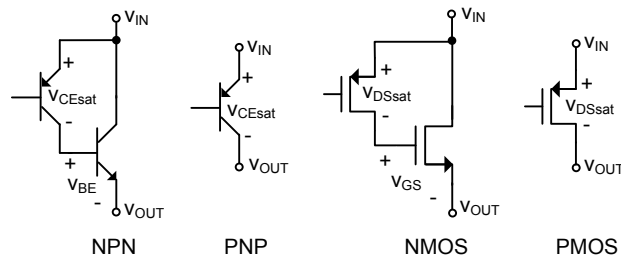


Figure 1.2: Comparison of different pass element structures.

One of the major benefits of using MOSFET based pass elements is that they do not require any gate drive current in steady state conditions. Moreover, due to the availability of advanced fine geometry CMOS process technologies, linear regulators implemented using MOSFET devices occupy smaller silicon real estate compared to their BJT counterparts. With all its glory, however, there are some drawbacks with MOSFET devices. One is that BJT devices offer higher bandwidth operation compared to their MOSFET counterparts. Secondly, bipolar power devices can be used for high voltage applications since diffusion breakdown is inherently higher than oxide breakdown, and finally, BJT based regulators can deliver higher load currents than their MOSFET counterparts [1], [14]. Based on these advantages of BJT devices and the availability of Linear Technology Corporation's (LTC) 1.5 μm Bipolar process technology, a BJT based

voltage regulator is used for this research project. Please note that although implementations using BJT transistors will be detailed in this literature, similar implementations using MOSFET devices can be readily extrapolated.

One way of implementing the active resistor is by using an NPN transistor in follower configuration. The collector and the emitter of the NPN transistor are respectively connected to the input and the output terminals of the regulator, and the resistance between the two terminals is modulated by changing the base current into the NPN. A major drawback of this implementation, however, is that the minimum required voltage (i.e. dropout voltage: V_{DO}) between the input and output terminals of the regulator to maintain regulation is fairly high, as shown below, therefore resulting in poor efficiency:

$$V_{DO\text{NPN}} = V_{BE} + V_{CEsat} \cdot \quad (1.2)$$

Referring to Figure 1.2, the efficiency of linear regulators can be improved by using a PNP pass transistor as it will lower the minimum (required) differential voltage between the input and output terminals of the regulator, as shown in the equation below:

$$V_{DO\text{PNP}} = V_{CEsat} \cdot \quad (1.3)$$

One of its demerits, though, is that the base current now flows to the ground (instead of the output as in NPN), which can lower the overall current efficiency of the regulator. However, depending on the current gain (β) of the PNP transistor, this downside can be minimized. Also, if PMOS devices are used instead, then this drawback is no longer an issue [1], [5], [6], [14].

Owing to their high popularity, such regulators are commonly referred to as low-dropout (LDO) linear regulators. Moreover, at low input-output voltage differentials,

LDO regulators offer sufficient conversion efficiency. In particular, as the supply voltages of digital circuitries continues to decrease, the demand for LDO regulators is projected to increase, as in this range, in addition to all their other benefits, they can offer efficiencies rivaling that offered by SMPS [8], [9].

1.3 Relevant LDO Characteristics

As shown in the figure below, a basic LDO regulator consists of a stable voltage reference, an error amplifier, and a pass element that controls the flow of power from the input to the output. Some of the most important parameters to consider when designing an LDO regulator are: dropout voltage, load and line regulation (accuracy), power-supply rejection (PSR), load transient response, and the overall solution size.

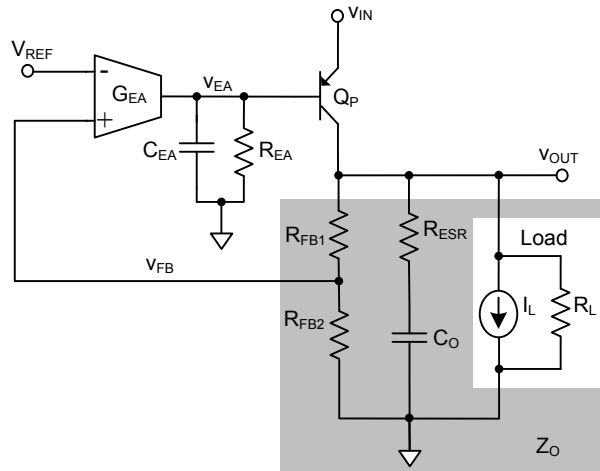


Figure 1.3: A conventional LDO regulator.

The dropout voltage, as mentioned earlier, is defined as the minimum difference between the input and the output voltages of the regulator before it ceases to regulate. The lower the dropout voltage, the more efficient the LDO regulator can become. Moreover, because of how PNP devices are physically implemented, as the regulator begins to operate near its dropout voltage, the effective current gain (β) of its power PNP

will degrade, and this needs to be addressed when designing PNP based LDO regulators [13], [27].

Load regulation (LDR) is another important specification for voltage regulators. It can be defined as the change in output voltage per unit change in load current, and it can be mathematically defined as follows:

$$\text{LDR} \equiv \frac{\Delta V_{\text{OUT}}}{\Delta I_{\text{L}}} = \frac{R_{\text{o-OL}}}{1 + \text{LG}} \quad (1.4)$$

and

$$R_{\text{o-OL}} = r_{\text{op}} \parallel (R_{\text{FB1}} + R_{\text{FB2}}) \parallel R_{\text{L}}, \quad (1.5)$$

where $R_{\text{o-OL}}$ is the open-loop output resistance of the regulator, r_{op} is the output resistance of the power device, and LG is the loop gain of the regulator. Thus, for a given set of operating conditions, as the regulator's loop gain is increased, its load regulation performance will improve [1].

Line regulation (LNR) is another important specification parameter for LDO regulators, and it can be defined as the change in output voltage per unit change in input voltage, and it can be mathematically described as follows:

$$\text{LNR} \equiv \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}}. \quad (1.6)$$

As the case with load regulation, line regulation is improved with increasing loop gain. It is important to note that although line and load regulations are both important parameters in determining the overall accuracy of LDO regulators, they are by no means the complete representation of regulator accuracy. Reference's temperature co-efficient, error amplifier's input-referred offset, and output voltage variation across process are some of the additional parameters that determine the regulator's accuracy [1], [14].

Power-supply rejection (PSR), also commonly known as power-supply ripple rejection, is another critical metric for LDO regulators, especially for high-performance noise-sensitive applications. Technically speaking, it is essentially the line regulation across frequency, and it can be mathematically represented as follows:

$$\text{PSR} \equiv \frac{1}{A_{\text{IN}}} \equiv \frac{V_{\text{in}}}{V_{\text{out}}} . \quad (1.7)$$

Qualitatively, the PSR transfer function of an LDO regulator can be thought of as a voltage divider due to the impedance between the input and output and the impedance between the output and ground [2], [17], [19]. PSR will be more rigorously treated in the following chapter.

Another parameter of particular importance to high speed digital loads powered using LDO regulators is the closed-loop bandwidth of the regulator. High speed digital circuits can switch from no-load (standby state) to full-load in a few tens of nano-seconds, consequently demanding a high speed regulator. The transient output voltage variation resulting from a sudden load dump can be anticipated using the regulator's bandwidth, output capacitor, and load current, as shown in the equation below:

$$\Delta v_{\text{O-tr}} = \left(\frac{\Delta I_{\text{L}}}{C_{\text{O}}} \right) \Delta t_{\text{BW}} + \Delta v_{\text{ESR}} + \Delta v_{\text{ESL}} , \quad (1.8)$$

where $\Delta v_{\text{O-tr}}$ is the change in the output voltage, ΔI_{L} is the maximum change in the load current, C_{O} is the output capacitor, Δt_{BW} is the regulator's response time, and Δv_{ESR} and Δv_{ESL} are the instantaneous changes in the output voltage due to parasitic series resistance and inductance, respectively, associated with the output capacitor. It is important to note that Δt_{BW} does not account for any slew rate limited delays, and it will further deteriorate the output voltage variation [1], [2], [4].

Finally, with the ever decreasing solution size of portable/handheld electronic devices, system designers are increasingly concerned about the PCB real estate occupied by power supply circuitries. As is typically the case, off-chip passive components usually end up consuming a large portion of the solution space, and this is particularly the case with large output capacitor (C_O) LDO regulators. A large output capacitor helps improve the high frequency PSR and load transient performance of LDO regulators, in addition to easing the task of stabilizing the regulator's control loop. As a consequence, however, a formidable challenge arises in designing LDO regulators with good PSR and transient performance while maintaining a smaller overall solution size by using a smaller output capacitor, for example.

1.4 LDO Design Challenges

Before going further into the objective of this research, it would be appropriate to gain a little perspective on some of the challenges involved in designing high performance LDO regulators. Although the challenges vary from application to application, one common difficulty found in designing most LDO regulators is maintaining stability across a wide range of load currents, which can span over six orders of magnitude, as well as across different types and sizes of output capacitors. As illustrated in Figure 1.3 above, and shown below for convenience, a basic LDO regulator consists of at least two poles.

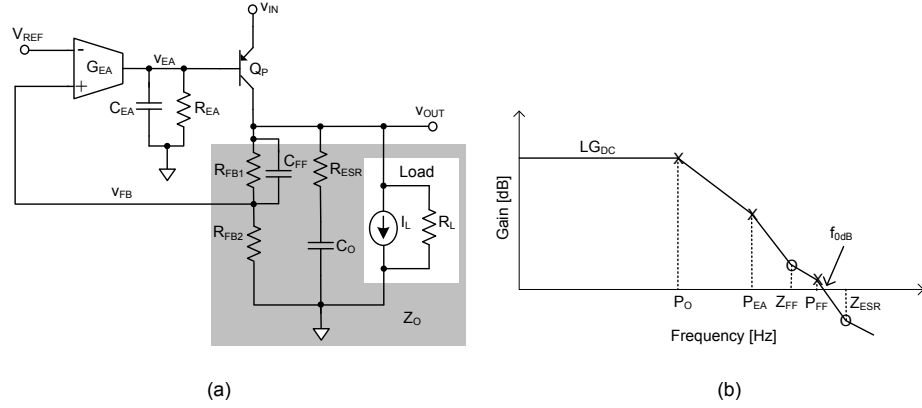


Figure 1.4: (a) A conventional LDO regulator and (b) Its frequency response.

The first pole, or the dominant pole, occurs at the output of the regulator, and it is formed by the parallel combination of the output capacitor and the equivalent open-loop resistance at the regulator's output (R_{o-OL}):

$$f_{PO} = \frac{1}{2\pi R_{o-OL} C_O}. \quad (1.8)$$

As the load current varies, however, R_{o-OL} varies with it and so does the output pole. The second pole (f_{p2}) occurs (as shown below) at the base of the power transistor, and it can get to quite low frequencies depending on the size of the power transistor, which is dictated by the maximum load current and the dropout voltage requirements of the regulator:

$$f_{PEA} = \frac{1}{2\pi R_{EA} C_{EA}}. \quad (1.9)$$

With the presence of two low-moderate frequency poles, an LDO is inherently unstable. To stabilize the regulator, at least one left-half-plane (LHP) zero is needed. Depending on the type of the output capacitor used, an LHP zero (f_{ESR}) can be obtained from the ESR (equivalent series resistance) of the output capacitor:

$$f_{\text{ZESR}} = \frac{1}{2\pi R_{\text{ESR}} C_{\text{O}}} . \quad (1.10)$$

However, the location of (f_{ESR}) can vary over a wide range, as ESR is not a well controlled parameter. Moreover, large values of ESR resistance can deteriorate the high frequency PSR performance of the regulator, as well as its transient response, as shown earlier [1], [5], [6], [14]. Another approach of generating an LHP zero (f_{ZFF}) is by placing a small feed-forward capacitor (C_{FF}) across the top resistor (R_{FB1}) in the feedback divider network [11]. However, as a by-product, it introduces a high frequency pole (f_{PFF}) located at the frequency shown in the equation below:

$$f_{\text{ZFF}} = \frac{1}{2\pi R_{\text{FB1}} C_{\text{FF}}} \quad (1.11)$$

and

$$f_{\text{PFF}} = \frac{1}{2\pi(R_{\text{FB1}} \parallel R_{\text{FB2}})C_{\text{FF}}} . \quad (1.12)$$

All of the major performance parameters of LDO regulators as stated above are affected by the stability of the regulator. For instance, achieving higher loop gain and stability under all conditions and at higher bandwidth may not be feasible, and thus tradeoffs involving the regulator's line regulation, load regulation, transient response, PSR performance, among others, are indispensable. In particular, achieving good high frequency PSR performance is especially challenging. As with any feedback system, the higher the loop gain of the system, the more effectively can the loop suppress any external disturbances. However, as the loop gain degrades at higher frequencies (i.e. bandwidth limited), the noise rejection performance of the system will deteriorate – and similar holds true with PSR for LDO regulators.

To achieve good PSR performance at lower frequencies, the DC loop gain (LG_{DC}) of the regulator needs to be high. However, with high LG_{DC} , as with any linear circuit, achieving wider bandwidth can become near impossible. Consequently, achieving good high frequency PSR performance, without trading-off other performance parameters, can quickly become challenging. Furthermore, LDO regulators with significantly lower dropout voltages often achieve so by considerably increasing the size of the power transistor, and thereby pushing the pole located at the base of the power device closer to the output pole, further deteriorating its stability. As a result, it becomes even more difficult to design LDO regulators with very low dropout voltages and good high frequency PSR performance.

1.5 Research Objective

To achieve longer battery life, many high performance applications such as data converters, RF transceivers, precision signal conditioning, among others, use switched-mode power supplies (SMPS) followed by LDO regulators (being low noise supplies) as post-regulators for noise suppression. However, with the increasing switching frequencies of SMPS (on the order of 10MHz), attenuating the associated high frequency ripple is proving increasingly difficult for LDO regulators since at such high frequencies, different parasitic components start deteriorating the regulator's PSR performance [3]. A handful of different techniques ranging from employing a simple low-pass filter at the regulator's input to connecting two regulators back-to-back to cascoding the regulator with an N-type transistor have been reported to improve the PSR performance of LDO regulators. However, as will be rigorously detailed in the following chapter, each of these techniques suffers from significant drawbacks ranging from large size to decreased

efficiency to increased circuit complexity, which diminishes their efficacy [17], [21], [22].

In power management, as in most facets of electronics, miniaturization is the rule rather than the exception. Large passive components, especially the capacitors, place a major bottle-neck in reducing the overall size of LDO regulator solutions. Nevertheless, a number of challenges come up with the use of smaller output capacitors. As had been stated earlier, it is difficult to achieve adequate phase margin, and even stability in some cases, with smaller output capacitors. Moreover, it becomes considerably more difficult to achieve good high frequency PSR performance with smaller output capacitors. With this in mind, it is the objective of this research project is to develop a high performance LDO regulator with good high frequency PSR performance without relying on large passive components or deteriorating the power conversion efficiency of the regulator.

1.6 Synopsis

In this chapter, different types of power supplies such as linear regulators and SMPS that can be used to power portable electronic devices have been presented. Although SMPS are more efficient than linear regulators, at low input-output voltage differentials, their efficiency benefit is not as impressive; moreover, many noise sensitive applications such as analog and RF circuitries require the use of linear regulators. In addition, a variety of different topologies of linear regulators can be obtained depending on how the pass element is implemented. The pass element of an LDO regulator can be implemented either using a PNP or a PMOS transistor. In the following chapter, the state-of-the-art in high PSR LDO regulators followed by an introduction to the proposed current-mode LDO regulators will be meticulously presented.

CHAPTER 2

POWER-SUPPLY REJECTION IN LDO REGULATORS

Power-supply rejection (PSR) is an important performance metric for low-dropout (LDO) linear regulators, especially for noise-sensitive applications that use switched-mode power supply (SMPS) for high efficiency with LDO regulator as a post-regulator for ripple suppression. A detailed PSR analysis of LDO regulators, followed by the state-of-the-art in high PSR regulators together with their drawbacks will be presented in this chapter. Finally, a brief overview addressing the benefits of the proposed current-mode LDO regulator compared to the state-of-the-art techniques will be presented.

1.1 PSR Analysis

The PSR transfer function of an LDO regulator can be modeled as shown in Figure 2.1 (b) below.

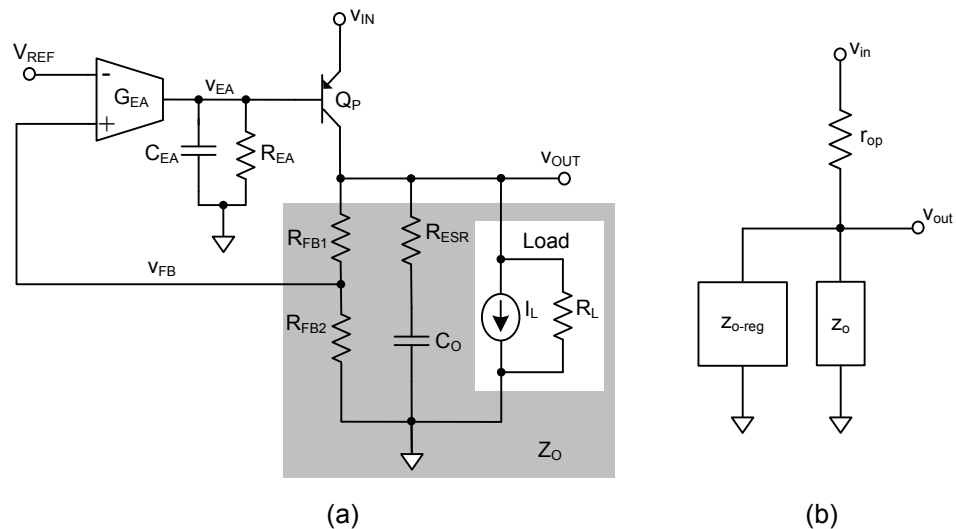


Figure 2.1: (a) Conventional LDO Regulator and (b) Its intuitive small-signal PSR model.

Based on this model, an LDO regulator's PSR response can be modeled of as a voltage divider resulting from the impedance between the input supply and the output and the impedance between the regulator's output and ground [2], [17], [19]. In addition, the PSR of an LDO regulator can be shown mathematically as follows:

$$\text{PSR} \equiv \frac{1}{A_{\text{IN}}} \quad (2.1)$$

and

$$A_{\text{IN}} \equiv \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{z_{\text{O}} \parallel z_{\text{o-reg}}}{r_{\text{oP}} + z_{\text{O}} \parallel z_{\text{o-reg}}}, \quad (2.2)$$

where r_{oP} is the output resistance of Q_{P} , and the effect of the regulator's feedback loop is embedded inside $z_{\text{o-reg}}$. As shown in the equation below, $z_{\text{o-reg}}$ decreases with increasing loop gain (LG):

$$z_{\text{o-reg}} = \frac{z_{\text{O}} \parallel r_{\text{oP}}}{\text{LG}} = \frac{z_{\text{O}} \parallel r_{\text{oP}}}{A_{\text{OL}}\beta}. \quad (2.3)$$

Combining the above three equations yield Equations 2.4 and 2.5 for PSR, respectively, at low-to-moderate frequencies and at high frequencies:

$$\text{PSR}_{\text{Low-to-mod. freq.}} \approx \frac{\text{LG} r_{\text{oP}}}{z_{\text{O}}} \quad (2.4)$$

and

$$\text{PSR}_{\text{High freq}} \approx \frac{r_{\text{oP}}}{z_{\text{O}}}. \quad (2.5)$$

Based on the intuitive model shown in the Figure 2.1 (b) and the above mathematical relationships, the PSR response of an externally compensated LDO (dominant output pole) across a wide range of frequencies is illustrated in Figure 2.2 below [2], [17], [19].

Around low frequencies, the feedback loop gain is significantly high, and so the regulator's output impedance is considerably low, therefore resulting in good PSR performance. Moreover, it is important to note that the occurrence of the output pole (P_{O})

does not deteriorate the PSR performance since both the numerator and the denominator in Equation 2.4 decrease at the same rate. However, as shown in the figure below, beyond the pole located at the error amplifier's output, P_{EA} , the feedback loop gain (in the numerator) starts decreasing at twice the rate as the term in the denominator (of Equation 2.4), and consequently the regulator's PSR starts to deteriorate.

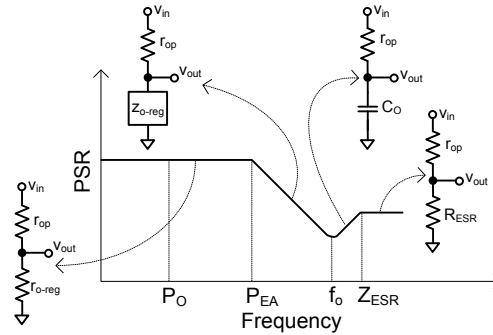


Figure 2.2: PSR response across wide frequency range.

The resulting PSR degradation continues until around the unity-gain bandwidth of the regulator, beyond which point, the LDO regulator's output impedance is essentially determined by the output capacitor. As the output capacitor's impedance is decreasing with increasing frequency, the LDO regulator's PSR starts to improve, and continues doing so until the parasitic components of the output capacitor (such as ESR) start to impede any further improvement in PSR [2], [17], [19]. In essence, the above analysis/illustration highlights the importance of higher loop gain and higher bandwidth in improving LDO regulator's PSR performance across wide frequency range.

Please note, however, that the above model assumes there is no ripple conduction through the transconductor of the pass transistor. Meaning that for an NPN device, there should be no ripple at the base of the power device, thereby resulting in no output ripple through the transconductor of the NPN transistor. On the other hand, for a PNP device, it

assumes there will be an equal amount of ripple present at the base of the PNP as it is at its emitter (regulator's input), and thus resulting in no output ripple through the transconductor of the PNP transistor [2], [17], [19].

2.2 Supply Ripple vs. Spikes

Before moving forward in to addressing the different techniques used to improve LDO regulator's PSR response, it is beneficial to understand the difference between supply ripple and spikes. As had been mentioned earlier, LDO regulators are commonly used as post-regulators, for noise suppression, after high efficiency switched-mode power supplies (SMPS). The LDO regulator's input ripple occurs at the switching frequency of the switching regulator, which can typically lie between 100kHz and 10MHz. However, as shown in the figure below, the input spikes caused by the pulsed energy delivery approach (fast turn-on and turn-off of the power switches) used in SMPS occur at much higher frequencies (around 100MHz) than the ripple frequency [25].

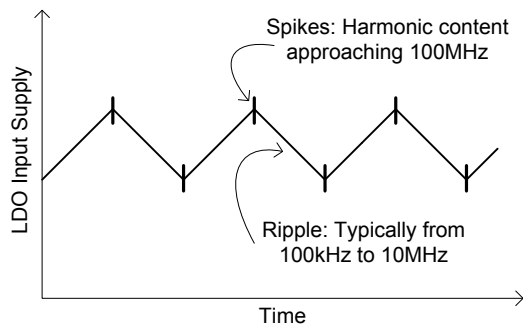


Figure 2.3: Comparison between power-supply ripple and spikes.

The rejection of ripple at the input of an LDO regulator can be improved by utilizing high speed process technologies and fancy control techniques, although it is by no means a simple problem. However, because spikes occur at much higher frequencies, well beyond the bandwidth of the regulator, it can only be improved by relying on

passive components. Capacitors generally tend to have limited benefit of attenuating spikes because they are constrained by parasitic ESR and ESL, which is present even in low ESR ceramic capacitors [25].

For better spike rejection, ferrite beads are used between the output of the LDO regulator and the load. Ferrite beads offer high impedance at higher frequencies, and thereby improving the high frequency PSR performance of LDO regulators. Moreover, because its impedance response is inductive, its low frequency impedance is low, thus it does not provide any PSR improvement at low frequencies where the PSR is already high due to the regulator's loop gain. It is important to note, however, that ferrite beads do exhibit small but non-zero impedance at DC; and therefore, they slightly deteriorate the regulator's overall efficiency. Furthermore, depending on how the regulator is compensated, they can also potentially impact the frequency response (stability) of the regulator [25].

2.3 State of the Art

Having looked at the fundamentals of PSR analysis in LDO regulators, we are now in a position to look at the state-of-the-art techniques used at improving PSR performance in LDO regulators. As shown in the figure below, a handful of different techniques can be applied to improve the PSR performance of LDO regulators. The simplest approach, as shown in Figure 2.4 (a) (i), is to employ a low-pass filter (e.g. an RC filter) in line with the power supply input to filter out the input supply ripple.

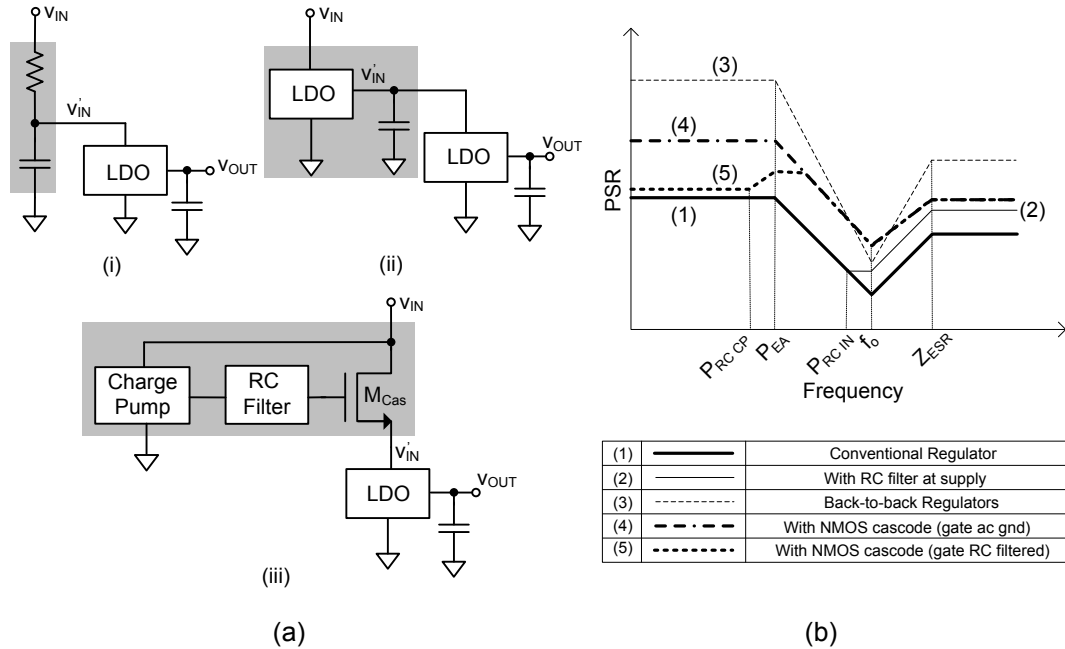


Figure 2.4: (a) State-of-the-art techniques and (b) Their corresponding PSR response.

As shown through curve (2) in the Figure 2.4 (b), depending on the corner frequency ($P_{RC\ in}$) location of the input filter, it can potentially filter out moderate to high frequency ripple at the input supply. However, this approach will significantly deteriorate the regulator's voltage headroom, as well as its efficiency, due to the presence of a relatively large series resistor between the input supply and the LDO regulator's input terminal [17], [20], [21].

Another approach, as shown in Figure 2.4 (a) (ii), is to connect two LDO regulators back-to-back. As shown through curve (3) in the Figure 2.4 (b), this will substantially attenuate the low frequency ripple at the output. However, at moderate frequencies, around the bandwidth of the regulators used, it is still difficult to achieve good PSR performance given that both regulators have similar limitations. Moreover, this approach has a number of other drawbacks: (a) it will dissipate substantially more power

as now the dropout voltage is twice that of a single regulator, (b) it will consume twice as much PCB real estate, and (c) it will considerably cost more [17], [20], [21].

The third approach, as shown in Figure 2.4 (a) (iii), is to connect an NMOS cascode transistor between the input supply and the input of the LDO regulator. The essential idea is to improve PSR by increasing the impedance between the input power supply and the LDO regulator's output. As shown through curve (4) in Figure 2.4 (b), the PSR response with the gate of the cascode device sitting at ac ground provides adequate PSR improvement at low frequencies as well as at higher frequencies. On the other hand, curve (5), with a more realistic ripple at the gate of the cascode device, shows very little PSR improvement at low frequencies. In fact, if the charge pump ripple is not properly filtered, the PSR of the regulator can potentially degrade. However, it does show moderate PSR improvement at higher frequencies [15], [17], [18], [20], [23], [24].

Nevertheless, as one can imagine, there are a number of drawbacks with this approach. Firstly, the regulator's dropout voltage essentially doubles, thereby substantially deteriorating the regulator's efficiency. Secondly, the silicon real estate (consequently the cost) drastically increases with this approach. The RC filter connected at the gate of M_{cas} needs to be carefully designed so that very little noise injection from the charge pumps heads to the gate of M_{cas} , otherwise the PSR performance could even degrade. This typically means large resistors and capacitors for filtering the gate signal of M_{cas} , thereby potentially increasing the overall solution size. Furthermore, given the fact that M_{cas} will be large in size (as it's a power transistor), the overall silicon real estate can become substantially larger, thereby increasing the die cost. Fourthly, the added cascode device markedly deteriorates the transient performance of the LDO regulator.

Finally, with the additional circuitries such as a clock and flying capacitors for the charge pump and the necessary filtering to attenuate the associated ripple due to the switching action, this strategy notably increases the circuit complexity of the regulator [17], [18], [20], [22]-[24].

Lastly, the high frequency PSR performance of LDO regulators can also be improved if the high frequency ripple at the source and gate of the power PMOS (for PMOS based regulators) is made common mode. This is essentially what the feedback loop accomplishes at lower frequencies (where it has adequate loop gain); however, because of limited bandwidth, it cannot achieve this at higher frequencies. The approach illustrated in the figure below claims to achieve this using a feedforward ripple-cancellation path which is higher bandwidth than the voltage regulation loop [22], [26].

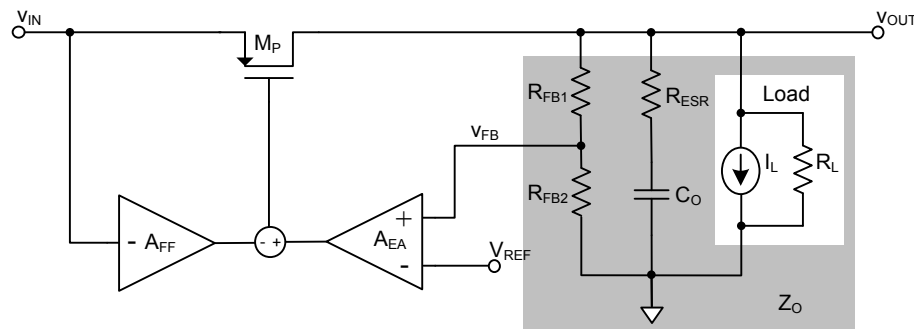


Figure 2.5: Feedforward ripple-cancellation technique.

The primary drawback with this approach, nevertheless, is that a substantially large output capacitor (4 μ F) is needed for stabilizing a 25mA regulator. As had been illustrated earlier, large output capacitors contribute significantly to the high frequency PSR performance of LDO regulators. Consequently, the benefits offered by the feedforward ripple-cancellation approach in [22] is not very clear.

Finally, at very high frequencies, each of the above mentioned approaches fails to provide good PSR performance as (at such high frequencies) it is primarily limited by the different parasitic components (ESR and ESL) of the output capacitor. This limitation is well illustrated in Figure 2.2 for further details. Moreover, at even higher frequencies, r_{OP} is no longer just resistive; its resistance actually starts rolling-off due to the equivalent emitter-collector capacitor (C_{CE}), which is basically determined by the parasitic base-collector capacitor (C_{CB}). However, since this deterioration occurs at much higher frequencies than the bandwidth of the regulator or the parasitic effects of the output capacitor, it can be neglected for simplicity [2].

2.4 Proposed Current-Mode Architecture

Having seen some of the major drawbacks of the different state-of-the-art approaches used to improve LDO regulator's PSR performance, it would be very useful to have an LDO regulator with improved high frequency PSR response without the afore mentioned drawbacks, namely poor efficiency, increased overall solution size, and increased cost. Particularly, if we step back and refer to the intuitive model for PSR analysis, we can readily see that PSR can be improved by either decreasing the equivalent impedance between the output and ground or by increasing the impedance between the input and output terminals of the regulator.

Furthermore, as had been shown in the previous section, the cascoding technique improves the regulator's PSR performance by essentially increasing the impedance between the input and output terminals of the regulator. It would be more useful, however, if the impedance between the input and output terminals of the regulator is increased without increasing its dropout voltage. In this literature, a current-mode LDO

regulator is proposed that increases the ac impedance between the input and output terminals of the regulator by utilizing a current-feedback loop. Because the proposed architecture does not increase the DC resistance between the input and output terminals of the LDO regulator, the regulator's efficiency is not compromised.

2.5 System-Level Current-Mode LDO Regulator

In a current-mode LDO regulator (as shown in the figure below) a current-feedback loop is implemented that allows for the power (PNP) transistor to be operated as a current-controlled current source; thereby, effectively increasing its input-output impedance by the loop gain of the current-feedback loop.

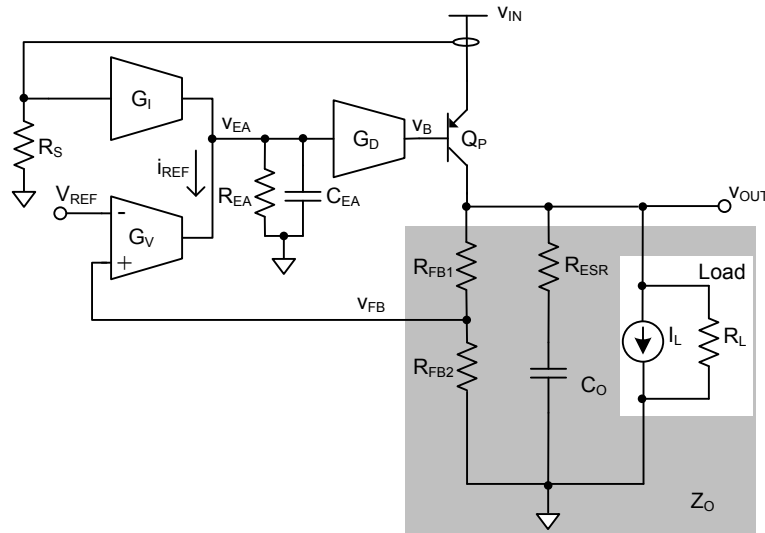


Figure 2.6: System-level current-mode LDO regulator.

As can be observed from the figure above, the main (voltage) loop sets a dynamic current reference for the faster current loop. During a transient condition, a load-dump for example, this reference point changes, and the current loop quickly drives (as it is higher bandwidth) the power transistor to the new current level.

One key requirement for proper operation of current-mode LDO regulators is that the bandwidth of the current-feedback loop needs to be higher than that of the voltage-feedback loop. This is not awfully difficult to achieve, however, since the dominant pole of the current loop occurs at that the base of the power transistor, which is at higher frequency than the dominant pole of the voltage loop that occurs at the output of the LDO due to the large output capacitor. Nevertheless, the current loop needs to be properly compensated to assure overall stability under different conditions of load, line, and output capacitors. For PNP power transistors, in particular, stability is somewhat more difficult to achieve since the pole located at the base of the power transistor moves as the load current changes. In addition, to make matters worse, the beta of the power transistor (β_P) also varies with the load current. More on stability of the proposed architecture will be discussed in the following chapter.

Another benefit of the proposed architecture is that the current-feedback loop being an internal sub-feedback loop (for the voltage loop), it effectively increases the bandwidth of the regulator's voltage loop by pushing out the pole located at the base of the power transistor to higher frequencies. This not only improves the regulator's transient response, but it further helps improve the PSR response, since with higher bandwidth, the voltage loop will maintain higher loop gain for wider range of frequencies, which in turn will keep the impedance between the regulator's output and ground low for a wider frequency range. The third benefit of the proposed architecture is that it offers better line transient response because any changes at the input line will be corrected by the current-feedback loop before any changes occur at the output voltage.

2.6 Synopsis

An intuitive, yet comprehensive, approach to analyze the PSR of LDO regulators has been presented in this chapter. Moreover, different state-of-the-art techniques that are used to improve LDO regulator's PSR response have also been presented, together with their respective drawbacks. Finally, we have glimpsed at the proposed current-mode architecture for improving the PSR performance of LDO regulators. More detailed analysis on the stability and PSR response of current-mode LDO regulators will be performed in the following chapter.

CHAPTER 3

CURRENT-MODE LDO REGULATOR IC

Before progressing further in to analyzing current-mode low-dropout (LDO) regulators, let us briefly recap some of the major benefits offered by current-mode LDO regulators over conventional regulators. Firstly, it offers better power-supply rejection (PSR) performance by increasing the impedance between the input and output terminals of the regulator by the loop gain of the current-feedback loop. Moreover, the bandwidth of the current-mode LDO is higher than that of conventional LDO regulators due to the feedback action of the internal current-feedback loop.

3.1 Transistor-Level Implementation

The proposed current-mode LDO regulator is implemented using Linear Technology Corporation's (LTC) 1.5 μm Bipolar process technology utilizing vertical NPN and lateral PNP devices. As can be observed from the transistor level schematic of the proposed LDO regulator, shown in the figure below, two main transconductance amplifiers are used: one for the current loop (G_I) and the other for the voltage loop (G_V).

Moreover, the circuit also contains a current mixer for combining the two loops. The output of the current mixing stage is used for compensating the two feedback loops – more on this in the next section. The current mixer's output, having high equivalent resistance, also serves as the gain node for the two feedback loops. Finally, there's the driver stage (consisting of Q_D) which can sink large amounts of current to be able to effectively drive the power PNP at heavy load levels.

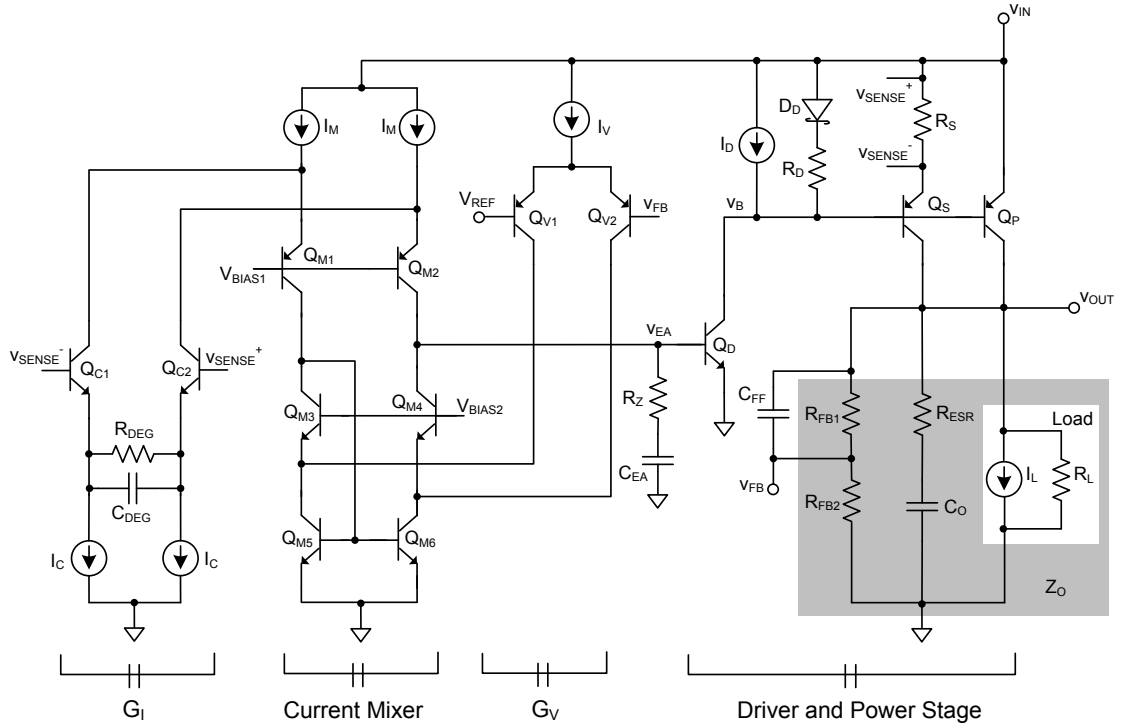


Figure 3.1: Transistor-level schematic of the proposed current-mode architecture.

The presence of multiple feedback loops make the design of the proposed architecture somewhat more complicated, and so it is imperative to analyze the stability of the regulator and understand how the two loops interact with each other.

3.2 Stability Analysis

Referring back to Figure 3.1, and assuming R_{DEG} is shorted for a moment, if there is a load change, for instance from no-load to heavy-load, then the voltage across the current sense resistor (ΔV_S), which is also the voltage difference between the two terminals of the current loop transconductor (G_I), will change by:

$$\Delta V_S = \Delta I_S R_S. \quad (3.1)$$

Since the transconductance of the current and voltage loop transconductors is roughly equal, this entire differential voltage (which can well be tens of millivolts) will manifest

at the feedback node (v_{FB}), consequently degrading the load regulation of the regulator, and hence the purpose of using R_{DEG} , as analyzed below.

This deterioration in load regulation can be remedied if the DC gain of the current loop is minimized without compromising its high frequency gain – which is needed for good high frequency PSR performance. This behavior can be achieved by frequency shaping, through R_{DEG} and C_{DEG} , the transconductor G_I . The large resistor, R_{DEG} , heavily degenerates the transconductance of G_I , and thus assures very low DC gain, and as the frequency increases, the capacitor (C_{DEG}) shunts away R_{DEG} , thereby increasing the transconductance of G_I , consequently increasing the loop gain of the current-feedback loop. A more qualitative way of thinking about the problem is: because we are interested in regulating the DC output voltage, and not the DC output current, the loop gain of the current loop is frequency shaped to achieve very low DC gain and adequate gain at higher frequencies.

The loop gain of the current-feedback loop (LG_I), at different frequencies, can be mathematically determined as shown in Equation 3.2 below:

$$\begin{aligned}
 LG_I &= (R_S G_I)(Z_{EA} g_{mD} R_B g_{mS}) = \beta_I A_{OL-I} \\
 &\approx \frac{R_{EA} g_{mD} R_B g_{mS} R_S}{R_{DEG}} \text{ (low frequency)} \quad , \quad (3.2) \\
 &\approx g_{C1} Z_{EA} g_{mD} R_B g_{mS} R_S \text{ (higher frequency)}
 \end{aligned}$$

where R_{EA} and R_B are the equivalent resistances at v_{EA} and v_B , respectively. Moreover, Z_{EA} is the equivalent impedance at v_{EA} , β_I is the feedback factor of the current loop, and A_{OL-I} is the open-loop gain (forward gain) of the current-feedback loop. All of the other

parameters have their normal meanings, as applied to analog circuits, with the subscript denoting the name of the device in Figure 3.1.

Furthermore, a pole-zero pair, as shown below, is also generated as a result of frequency shaping the transconductor G_I :

$$Z_D = \frac{1}{2\pi R_{DEG} C_{DEG}} \quad (3.3)$$

and

$$P_D \approx Z_D \frac{g_{mC1}}{(1/R_{DEG})} = Z_D g_{mC1} R_{DEG} . \quad (3.4)$$

In addition to these, as shown in the equations below, there are two other poles in the current loop. One of them occurs at v_{EA} since it is a high gain node and the other occurs at v_B , the base of the large power transistor (Q_P):

$$P_{EA} = \frac{1}{2\pi R_{EA} C_{EA}} \quad (3.5)$$

and

$$P_B = \frac{1}{2\pi R_B C_{\pi P}} . \quad (3.6)$$

As it can be inferred from this analysis, with three poles and one zero, the current loop is inherently unstable. An additional compensation zero is required to stabilize it, and it is achieved through the resistor (R_Z) in series with C_{EA} in the Figure 3.1:

$$Z_Z = \frac{1}{2\pi R_Z C_{EA}} . \quad (3.7)$$

With the additional zero used for compensating the pole (P_B) located the base of the power transistor, the overall frequency response can be approximated as having only two poles and one zero. Based on this analysis, curve (2) in the figure below shows the resulting frequency response of the current-feedback loop's loop gain.

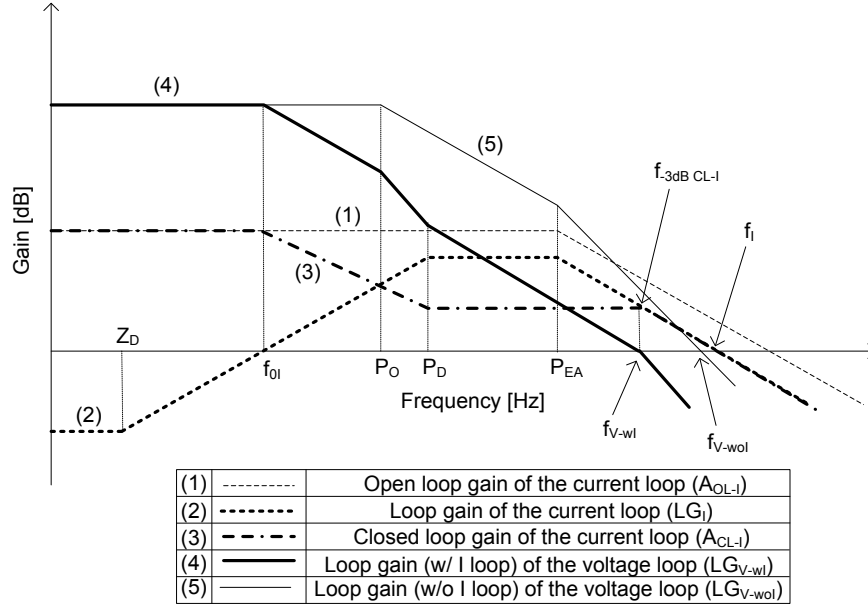


Figure 3.2: Frequency response of the two feedback loops.

The calculated loop gain of the current loop can then be used to determine the closed-loop gain of the current loop, which is essential for analyzing the voltage loop (as verified in Appendix A). The equation below mathematically shows the closed-loop gain of the current-feedback loop (A_{CL-I}):

$$\begin{aligned}
 A_{CL-I} &= \frac{A_{OL-I}}{1 + \beta_I A_{OL-I}} = \frac{R_{EA} g_{mD} R_B g_{mS}}{1 + (G_I R_S)(R_{EA} g_{mD} R_B g_{mS})} \\
 &\approx R_{EA} g_{mD} R_B g_{mS} \quad (\text{At lower freq.}) \\
 &\approx \frac{1}{G_I R_S} \quad (\text{At freq. where } LG_I \geq 1)
 \end{aligned} \tag{3.8}$$

As illustrated through curve (3) in the Figure 3.2 above, the closed-loop response accurately reflects the above relationships.

The loop gain of the current loop (through simulations) of the designed current-mode regulator is verified as shown in the figure below.

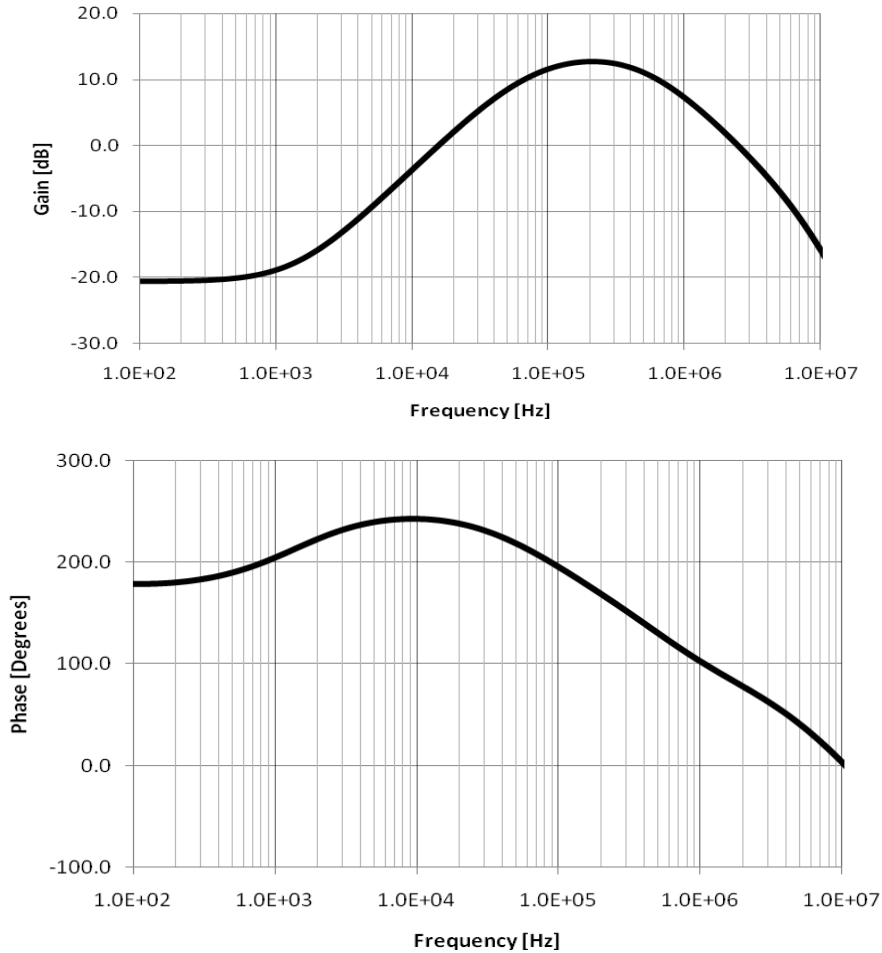


Figure 3.3: Frequency response of the current loop (LG_I) at 5mA load.

As we can see from the figure above, the current loop has practically no gain at low frequencies and acceptable gain at higher frequencies; hence, it is properly frequency shaped. Moreover, the loop is stable with close to 90° of phase margin – essentially the result of two poles and one zero. It can also be inferred from the figure above that the frequency response of the current loop is similar to what had been predicted based on the previous analysis and Figure 3.2.

Having determined the closed-loop gain of the current loop, we are now in a position to determine the loop gain of the voltage loop with and without the current-feedback loop, LG_{V-wI} and LG_{V-w0I} , respectively, which is illustrated as curves (4) and

(5), respectively, in Figure 3.2. Furthermore, LG_{V-wl} and LG_{V-wol} can be mathematically represented as follows:

$$LG_{V-wl} = G_V A_{CL-I} \frac{A_P}{A_S} Z_O \beta_V \quad (3.9),$$

and
$$LG_{V-wol} = G_V Z_{EA} g_{mD} R_B g_{mP} Z_O \beta_V, \quad (3.10)$$

where β_V is the feedback factor of the voltage loop, A_P is the emitter area of power PNP, and A_S is the emitter area of the sense PNP. It is important to note that based on Equations 3.8 and 3.9, the loop gain of the voltage loop (LG_{V-wl}) starts decreasing once the current loop's gain increases beyond unity (f_{0I} in Figure 3.2), and flattens out when the loop gain of the current loop flattens out (P_D).

The simulation results for the frequency response of the voltage loop in the actual design is shown in the Figure 3.4 below. The loop gain of the voltage loop is shown with (LG_{V-wl}) and without (LG_{V-wol}) the current-feedback loop. As anticipated from the above analysis and Figure 3.2, the loop gain of the voltage loop with the current-feedback loop (LG_{V-wl}) exhibits the output pole, another pole-zero pair as a result of frequency shaping the current loop, and slight effect from the -3dB bandwidth of A_{CL-I} ($f_{3dB\ CL-I}$) as it is around the same frequency as the unity-gain bandwidth of the voltage loop (f_{V-wl}); consequently, it is highly stable. On the other hand, due to the presence of three poles – the output pole, the pole located at the output of the error amplifier, and the pole at the base of the power PNP – and one zero at the output of the error amplifier, the loop gain of the voltage loop without the current-feedback loop (LG_{V-wol}) exhibits almost no phase margin.

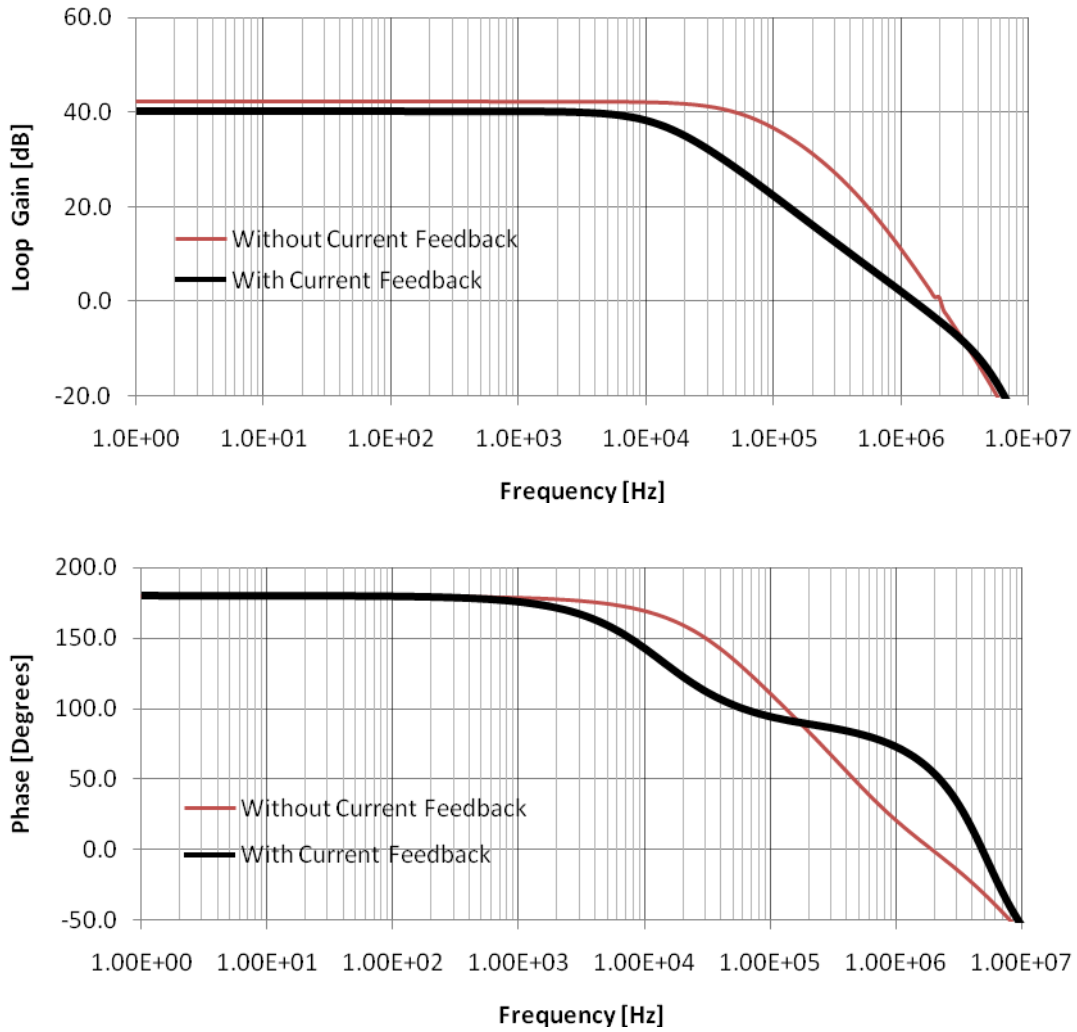


Figure 3.4: Frequency response of the voltage loop (LG_V) at 5mA load and 15nF output capacitor.

Having performed the detailed stability analysis of the two feedback loops and how the two loops interact with each other, we can now progress further into rigorously analyzing the PSR response of the proposed current-mode LDO regulator.

3.3 PSR Analysis

Attributed to the presence of dual feedback loops, the PSR analysis of current-mode LDO regulators is somewhat different from the approach/model used to analyze conventional LDO regulators. The conventional model (which was presented in Chapter

2) can be modified, as shown in the Figure 3.5 (a), to account for the additional feedback loop.

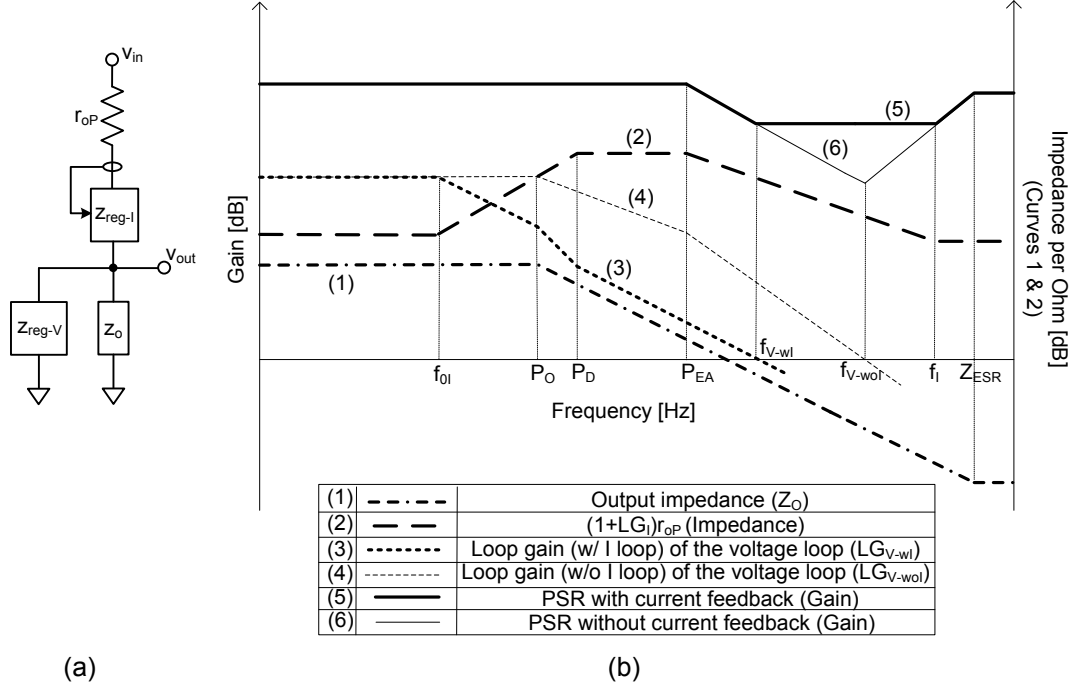


Figure 3.5: (a) Intuitive PSR model and (b) PSR analysis of current-mode LDO regulators.

The model shown in Figure 3.5 (a) incorporates an additional term (Z_{reg-I}) to model the increased impedance between the input and output terminals of the regulator due to the current feedback action. The PSR can be mathematically shown as follows:

$$\frac{1}{PSR} \equiv A_{IN} \equiv \frac{v_{out}}{v_{in}} = \frac{Z_O \parallel Z_{reg-V}}{(r_{oP} + Z_{reg-I}) + Z_O \parallel Z_{reg-V}}, \quad (3.11)$$

where Z_{reg-I} and Z_{reg-V} are defined as:

$$Z_{reg-I} = LG_I r_{oP} \quad (3.12)$$

and

$$Z_{reg-V} = \frac{Z_O \parallel (r_{oP} + Z_{reg-I})}{LG_V} \approx \frac{1}{\beta_V G_V A_{I-CL} (A_P/A_S)}. \quad (3.13)$$

Simplifying Equation 3.11 for low-to-moderate frequency range gives a more insightful perspective on PSR for this frequency band, as shown in the equation below:

$$\frac{1}{\text{PSR}_{\text{Low-to-mod. freq.}}} \approx \frac{z_o}{\text{LG}_V \text{LG}_I (1 + r_{oP})}. \quad (3.14)$$

For moderate-to-high frequency range, that is at frequencies beyond the bandwidth of the voltage loop but before the current loop's bandwidth, the PSR can be simplified as follows:

$$\frac{1}{\text{PSR}_{\text{Mod.-to-highfreq.}}} \approx \frac{z_o}{\text{LG}_I (1 + r_{oP}) + z_o} \approx \frac{z_o}{\text{LG}_I (1 + r_{oP})}. \quad (3.15)$$

This is the region, as shown in Figure 3.5 (b) through curves (5) and (6), where the proposed architecture provides better PSR response. Moreover, based on the analysis presented in the previous chapter, it really is in this region where the PSR of conventional regulators is worst; therefore, any improvement in this region will be incredible. Finally, the high frequency PSR response, i.e. at frequencies beyond the current loop's bandwidth, the PSR can be simplified as shown below, which is same as in conventional LDO regulators:

$$\frac{1}{\text{PSR}_{\text{High freq.}}} \approx \frac{z_o}{r_{oP}}. \quad (3.16)$$

Based on the above analysis, the PSR of current-mode LDO regulators can be qualitatively illustrated as shown through curve (5) in Figure 3.5 (b). In addition, the PSR of conventional regulators (i.e. without current-feedback loop) is illustrated as curve (6) in the same figure. As can be inferred from Figure 3.5 (b), although LG_V starts rolling-off when LG_I increases beyond unity, the PSR response remains unaffected since the product of the two remains constant. However, the benefit of the current-mode LDO regulator

becomes apparent after the unity-gain frequency of the voltage loop (f_{v-wl}) but before the unity-gain frequency of the current loop (f_i), which occurs around moderate-to-high frequencies, and it is typically in this frequency range where conventional LDO regulator's PSR deteriorates drastically.

The PSR response (through simulations) of the proposed current-mode regulator design is shown in the figure below. It is important to note that although the proposed current-mode LDO regulator is stable with 15nF of output capacitance (C_O), for comparison purposes, however, the PSR response shown below is with 68nF of output capacitance since the regulator with the current loop turned-off (essentially R_S shorted) is unstable with 15nF of output capacitance.

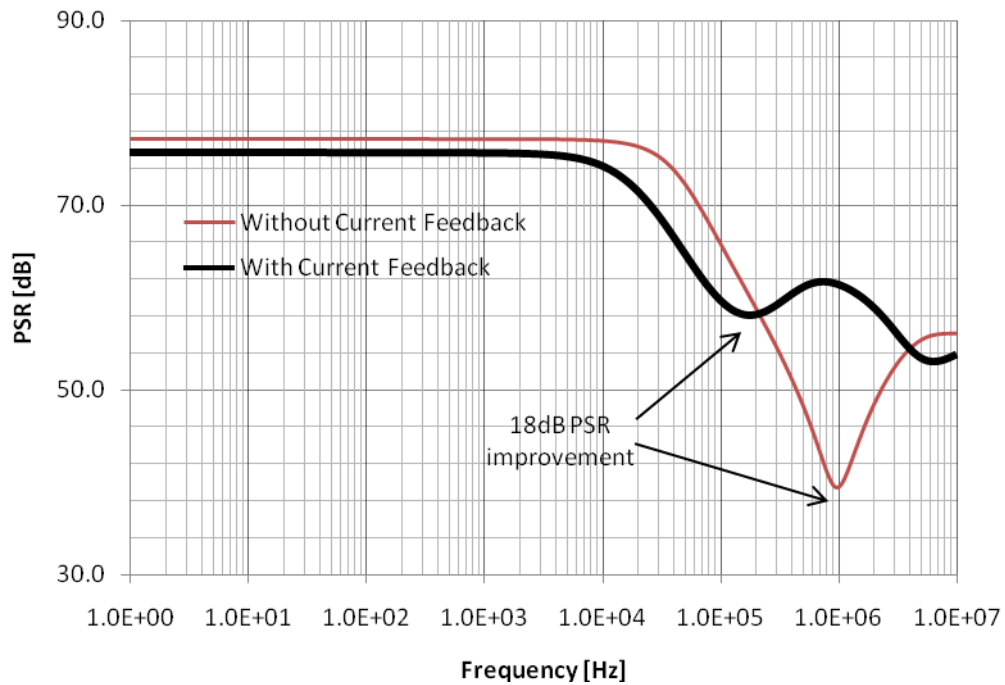


Figure 3.6: PSR response ($I_L=5\text{mA}$ and $C_O=68\text{nF}$) comparing current-mode vs. conventional regulator.

As can be seen from the above simulation results, the proposed architecture does provide significant PSR improvement over conventional regulators around moderate-to-

high frequencies. Although the PSR of the current-mode LDO regulator is slightly less than that of a conventional regulator at low-to-moderate frequencies (which is attributed to slightly lower LG_V due to non-ideal frequency shaping, i.e. non-zero LG_I at lower frequencies), it does provide significant PSR benefits at moderate-to-high frequencies. Moreover, since the PSR at lower frequencies is already high to begin with, slight deterioration in PSR will not be a major liability. On the other hand, since the lowest PSR occurs around moderate-to-high frequencies for conventional LDO regulators, any improvement in this region is really useful, and the fact that most switching regulators operate around moderate-to-high frequencies, this benefit is tremendous [3], [25].

3.4 Achieved Design Performance and Layout Challenges

The steady-state and transient performance (through simulations) achieved by the current-mode LDO regulator is summarized in the table shown below.

Table 3.1: Current-mode LDO regulator’s specification matrix.

Design Parameter	Simulation Results
Input Voltage Range	1.4V to 10V
Min. Output Voltage	0.6V
Stable Load Range	0 to 5mA
Dropout Voltage	200mV
Min. Output Capacitance	15nF
Load Regulation (0 to 5mA)	3.15mV
Line Regulation (2V to 6V)	0.6mV
Quiescent Current (no load/full load)	50 μ A/120 μ A
Bandwidth (at full load)	1.3MHz
Min. PSR up to 10MHz (at 5mA Load and 15nF C_{OUT})	43dB (at 3.7MHz)
Technology	1.5 μ m Bipolar

Before moving further into the experimental results, let us glance through some of the precautionary measures taken when laying out the circuitry. One is that the sense PNP is located very close to the power PNP for better thermal matching, as the V_{BE} of bipolar

transistors is sensitive to thermal gradients. It also helps against any mismatches attributed to process gradients. Furthermore, the power and sense PNPs share the same tub to minimize the tub-to-substrate capacitance at the common base terminal of the power and sense PNPs. Moreover, critically matched devices are placed far away from the power transistor so that there is little variation in temperature between the critically matched devices. Another precautionary measure taken was to separate common-tubed devices with deep P+ (plug) isolations to prevent latch-up issues in the event any device saturates and begins to inject minority-carriers into its neighboring devices [13]. The figure below shows the micrograph of the fabricated design.

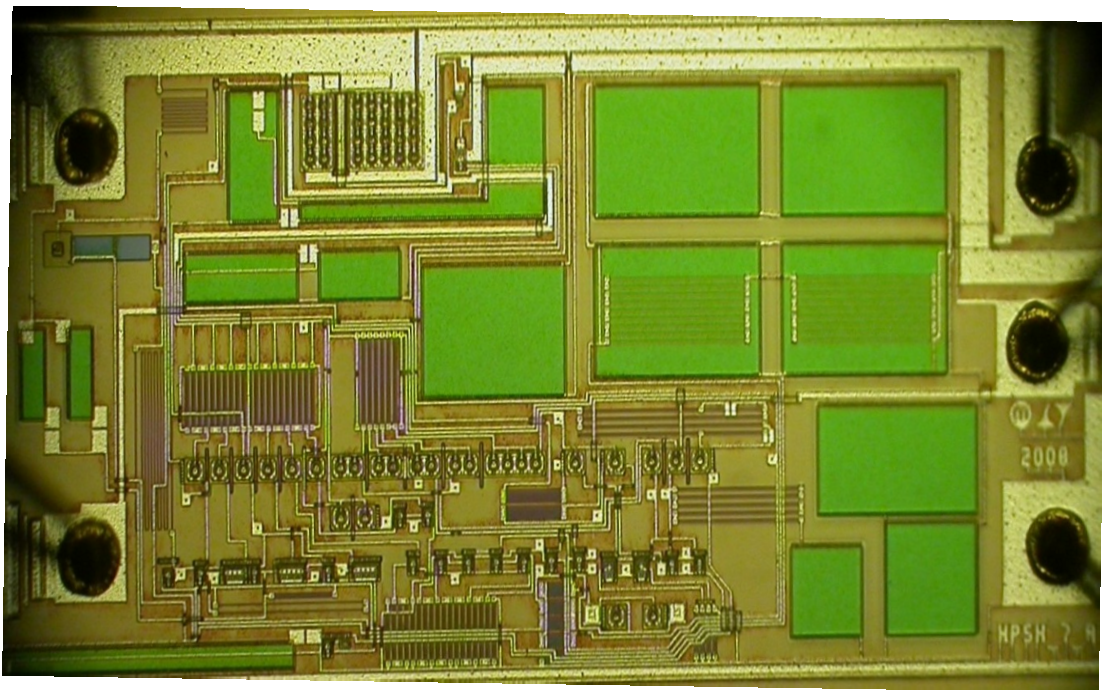


Figure 3.7: Micro photograph of the fabricated IC.

3.5 Synopsis

In the proposed regulator architecture, the high frequency impedance between the input and output terminals of the regulator is effectively increased by the loop gain of the current-feedback loop. Moreover, the outer loop is determined to be the voltage loop (and

not the current loop) since it is voltages (V_{REF} and v_{FB}) that are being mixed, and also because it is the output voltage (v_{OUT}) that is being sampled by the outer loop. With this in mind, the output current of the voltage loop's transconductor (G_V) sets the current reference signal based on the regulator's output voltage. The current loop will then try to drive the power PNP transistor such that the load current matches the current reference signal set by the outer voltage loop. In addition, the stability and PSR analysis of the proposed current-mode LDO regulator has been rigorously presented. The anticipated results from this analysis have been shown to agree with the simulation results.

CHAPTER 4

EXPERIMENTAL RESULTS AND CONCLUSIONS

The fabricated current-mode low-dropout (LDO) regulator is tested in the laboratory for actual performance measurement of all the different parameters simulated in the previous chapter, such as the input voltage range, dropout voltage, minimum (required) output capacitance, load regulation, line regulation, load transient response, PSR response, in addition to a few other measurements.

4.1 PCB Design and Testing Environment

Testing high frequency PSR performance requires some careful considerations when designing the PC board. Particularly, because of high ripple rejection exhibited by the regulator (around 75dB at lower frequencies), the output of the LDO will have very small amplitude; as a result, it can potentially be corrupted by external interference if care is not taken. This can be addressed, however, by using co-axial to co-axial cables to connect the output of the regulator to the oscilloscope while taking measurements. Moreover, since high frequency PSR is very important for this research, special attention is paid to minimize the parasitic resistances and inductances associated with PCB traces, especially the traces connecting the output capacitor to the ground plane.

In addition to the above considerations, generating a desired ripple at the input of the LDO regulator can be a non-trivial problem, especially since there is DC current flowing through the regulator to the output load. A power buffer circuitry is designed and built that can supply DC current as well as generate the desired ac ripple at the input of

the regulator. Current mixing is used (in the power buffer) for superimposing an ac ripple on top the DC signal at the input of the LDO regulator.

4.2 PSR Measurement Results

Two different LDO regulator designs were sent for fabrication: one with the current-feedback loop active and the other with the current-feedback loop de-activated (essentially by shorting the current sense resistor). The PSR results obtained by the proposed current-mode regulator was measured under a wide range of load currents, input voltages, and output capacitors. The figure below shows the PSR response of the current-mode LDO regulator at 5mA and using the minimum output capacitor of 15nF.

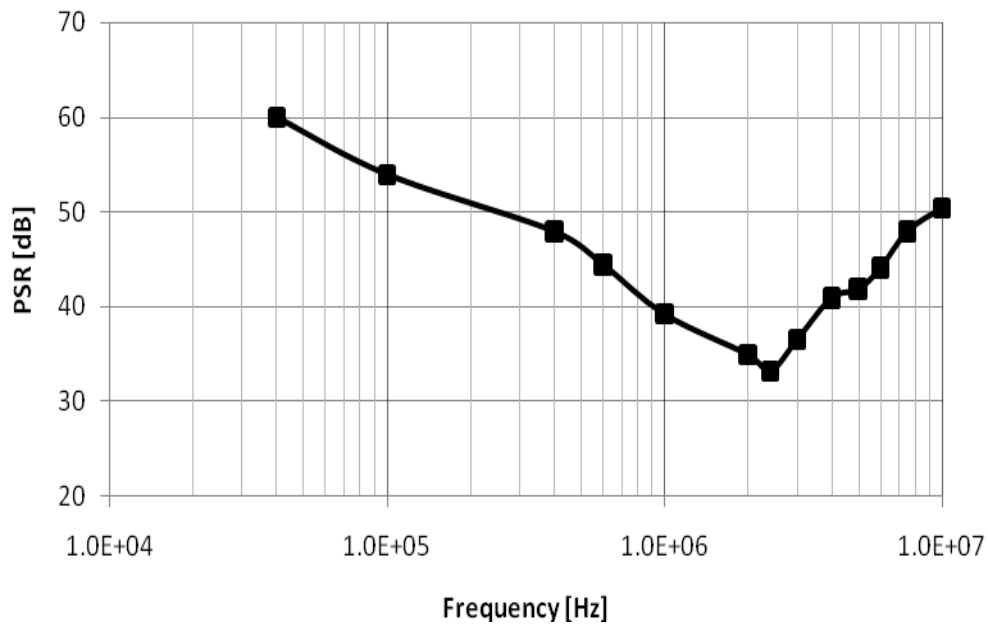


Figure 4.1: Measured PSR response of the proposed current-mode regulator with $C_O=15\text{nF}$.

As can be seen from the figure above, the lowest PSR (of 33dB) occurs around 2.4MHz, and the figure below details the PSR at this frequency, whereby channel 1 is the (ac) input signal and channel 2 is the (ac) output signal.

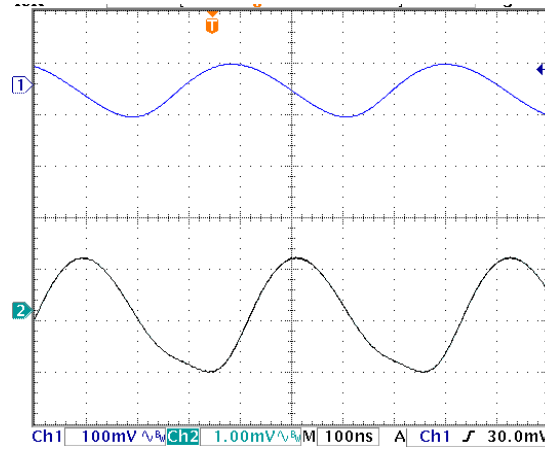


Figure 4.2: Input ripple rejection at 2.4MHz using 15nF output capacitor.

The PSR improvement when utilizing the current-feedback loop versus not using it is shown in the figure below.

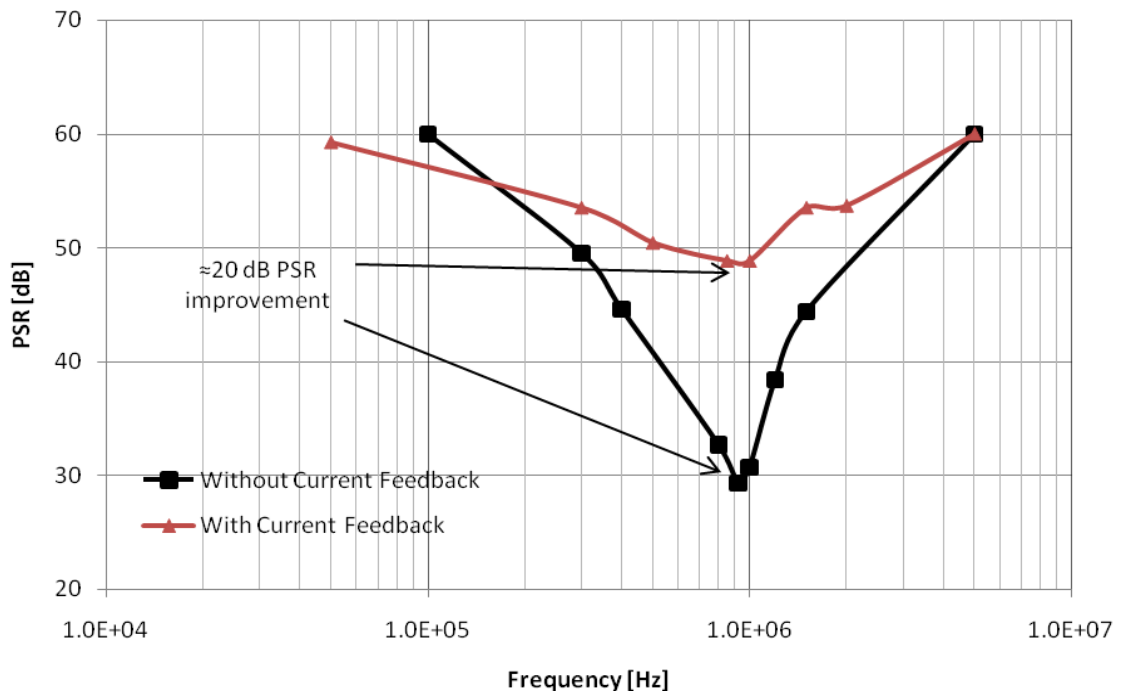


Figure 4.3: PSR comparison with and without the current-feedback loop.

Please note that 68nF of output capacitance (C_O) is used for this measurement since the regulator without the current-feedback loop becomes unstable with 15nF of C_O . Hence, both regulators (with and without the current-feedback loop) are tested at 5mA using

68nF of C_O . As we can observe from the figure above, the proposed current-mode regulator provides significant PSR improvement compared to when the current-feedback loop is de-activated, as had been predicted through simulations and mathematical analysis.

Furthermore, the lowest PSR for the current-mode regulator is about 49dB and occurs around 850kHz, and when the current loop is disabled, the lowest PSR is about 29dB, and it occurs around 900kHz. The PSR at this frequency is detailed in the figure below, whereby channel 1 is the (ac) input signal and channel 2 is the (ac) output signal.

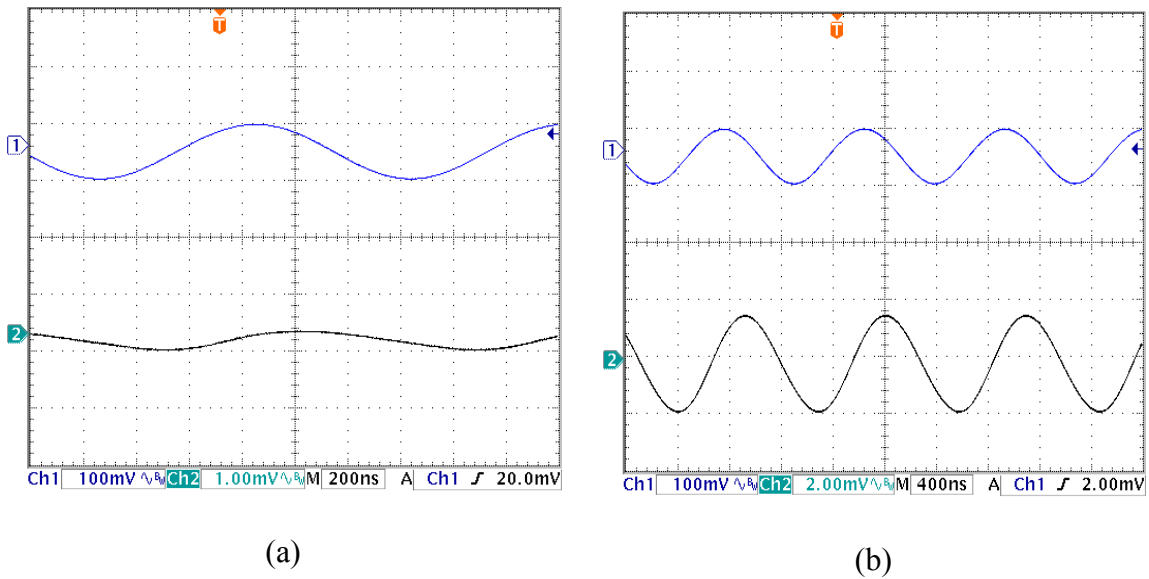


Figure 4.4: (a) PSR of current-mode LDO at 850kHz and (b) PSR of the regulator at 900kHz with the current loop disabled.

4.3 Transient Measurement Results

The load transient, no-load to full-load, response of the proposed current-mode regulator using a 15nF output capacitor is shown in the figure below, whereby channel 1 shows the load current and channel 2 shows the ac component of the output voltage. Moreover, the nominal output voltage is programmed at 0.6V.

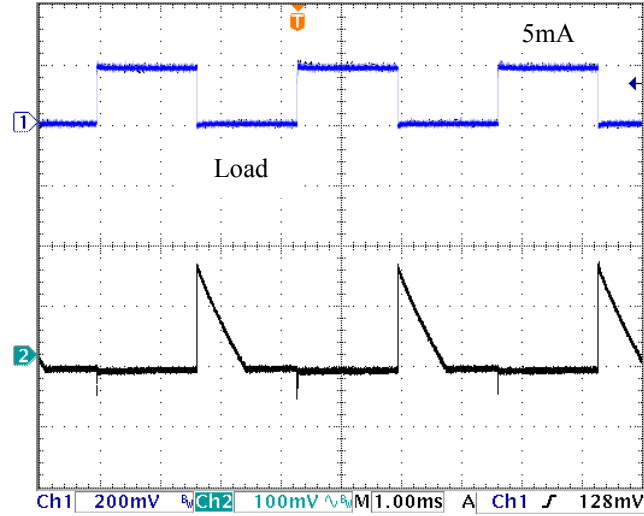


Figure 4.5: Positive and negative load transient response between full and no load.

The bandwidth of the regulator can be estimated based on its load transient response, such as the one shown in the figure above. Furthermore, since the load step's rise and fall time is about 50ns (although not clearly visible from the figure above), it can be assumed to be instantaneous (without significant error) to estimate the bandwidth of the regulator. Assuming very low ESR and ESL for the output capacitor, the response time (Δt_{BW}) of the regulator using the data from negative load dump, as it is apparently the worst case from the figure above, is given as:

$$\begin{aligned} \Delta t_{BW} &\approx \frac{\Delta V_{out} C_O}{\Delta I_L} \\ &= \frac{180\text{mV} \cdot 15\text{nF}}{5\text{mA}} = 0.54\mu\text{s} \end{aligned} \quad (4.1)$$

This implies the bandwidth (f_{BW}) of the regulator to be about 1.85MHz, similar to what had been predicted through simulations. Although it is difficult to discern from the figure above, the steady state change in the output voltage as the load is stepped from no-load to 5mA is about 4.6mV.

Another important transient test performed on the regulator is the line transient response of the current-mode LDO regulator with 15nF C_O operating at 5mA load current, and the output voltage is programmed at 0.6V. This response is shown in the figure below, where by channel 1 shows the input voltage and channel 2 shows the ac component of the output voltage.

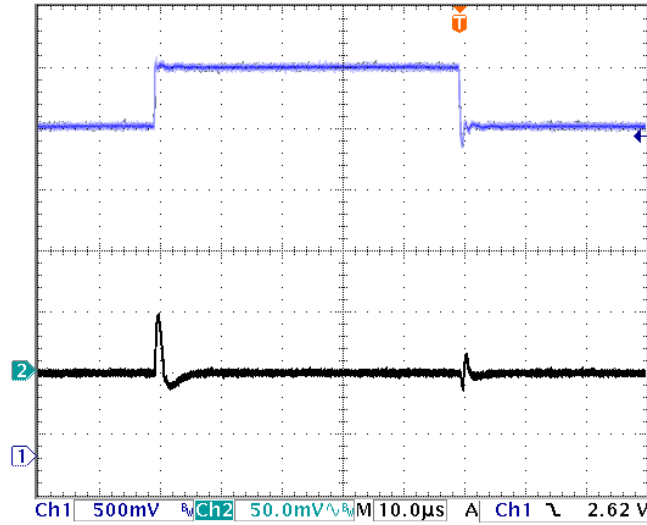


Figure 4.6: Line transient response of the current-mode regulator.

The input voltage is stepped between 2.7V and 3.2V. Moreover, the line regulation of the regulator was measured to be about 70dB.

The regulator has also been tested for a number of steady state parameters, in addition to line and load regulation. The dropout voltage of the regulator is measured to be about 205mV and the minimum input voltage of the regulator is found to be 1.4V. Moreover, the quiescent current (at no load) is measured to be 57µA, and at full load it is found to be 193µA. One explanation for the large discrepancy in quiescent current (at full load) between the measured results (193µA) and the simulation results (120µA) is that the leakage current to the substrate in the power PNP increases with load, and this was

not well accounted for in the simulations. As the schematic shown in the figure below illustrates, the parasitic PNP (Q_{PE}) is conducting whenever the power PNP is conducting.

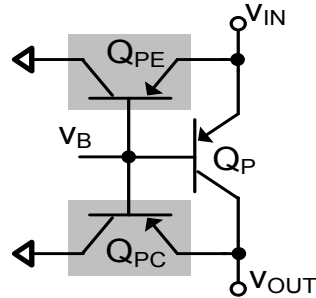


Figure 4.7: Parasitic devices found in lateral PNP transistors.

Although its current gain (β_{PE}) is made much lower through layout techniques, it still conducts some current, and it can become significant at higher load levels. Moreover, the parasitic Q_{PC} starts conducting when the main transistor (Q_P) enters into saturation, which is why the effective current gain (β) of PNP transistor deteriorates when in saturation [10], [13], [27].

4.4 Evaluation of the Proposed Architecture

As it has been shown through the measured results, the proposed architecture does provide significant PSR improvement (about 20dB) over conventional regulators at higher frequencies. Considering the fact that the PSR of a conventional LDO regulator significantly deteriorates around its unity-gain frequency, this improvement is a significant leap forward. Furthermore, with the drive towards energy efficiency without compromising system performance, many high-end analog and RF applications use switched-mode power supplies (SMPS) with LDO post-regulators to achieve high efficiency and low-noise power supplies. Nevertheless, with the trend towards increasing switching frequency of SMPS, typically around the unity-gain bandwidth of LDO regulators, the power-supply ripple suppression achieved by conventional LDO

regulators at such frequencies is not that impressive. This is where the benefits and applications of the proposed architecture really shine up.

Another benefit of the proposed architecture is that it can be stabilized with a smaller output capacitor than conventional LDO regulators. As had been mentioned earlier, in the regulator with the current loop disabled, a minimum of 68nF is needed to prevent oscillations at its output, where as only 15nF is needed to stabilize the proposed current-mode LDO regulator. Finally, the third benefit of the proposed architecture (as verified through the load transient response) is that it can achieve pretty high bandwidth (1.85MHz) while maintaining good phase margin.

Having seen the advantages of the proposed architecture, as with anything in engineering, trade-offs are involved. One is the increased complexity as a result of using two feedback loops and understanding their interactions. Guaranteeing stability for the two loops under different line, load, and output capacitor conditions is a non-trivial task. Another disadvantage of the proposed architecture is: owing to the non-ideal frequency shaping (i.e. non-zero loop gain of the current loop at DC) circuitry, there is slight deterioration in DC voltage gain, and thus in line regulation, load regulation, as well as in low frequency PSR performance.

There have been a few significant works in the area of high PSR LDO regulators, such as ([18], [22], [23], [24]). However, [18], [23], [24] rely on similar cascode strategy, and so the most recent and the most promising approach among the three, which is [18], is used for comparison against the proposed architecture. Table 4.1 compares the proposed approach against the state of the art. All the parameters shown are at full-load condition, as in this operating condition most regulators exhibit the worst performance.

Table 4.1: Comparison of the proposed topology against the state of the art.

Performance Parameter	[18]	[22]	Proposed Architecture
Strategy Used	Cascode	Feedforward Ripple-Cancellation	Current-Mode
Min. Input Voltage	1.8V	1.15V	1.4V
Max. Load Current	5mA	25mA	5mA
Dropout Voltage	450mV	150mV	200mV
Min. Output Capacitance	Integrated	4 μ F	15nF
Load Regulation	1.57mV/mA	0.048mV/mA	0.92mV/mA
I_Q	70 μ A	50 μ A	57 μ A@no load 193 μ A@full load $^\pm$
PSR at 100kHz (at full load)	61dB	62dB	57dB*
Lowest PSR up to 10MHz (at full load)	27dB	56dB	49dB*
Response Time	0.30 μ s	2.4 μ s	0.54 μ s
Technology	0.6 μ m CMOS	0.13 μ m CMOS	1.5 μ m Bipolar

*With 68nF C_O and $^\pm$ Reference is external.

Moreover, for the state-of-the-art techniques, the regulator's response time is estimated by taking the inverse of the regulator's bandwidth (if available) or by interpreting/computing from its load transient response.

As shown in the table above, although the cascode strategy used in [18] achieves good PSR performance, it suffers from poor efficiency due to its higher dropout voltage. Similarly, the feedforward ripple-cancellation strategy used in [22], achieves good high frequency PSR performance by relying on accurately matching the ripple at the gate of the power PMOS with that at its input; however, it suffers from significantly higher output capacitance (as shown in the table above) compared to the proposed topology.

4.5 Conclusions

The proposed architecture achieves high PSR by utilizing a current-feedback loop to increase the high frequency impedance between the input and output terminals of the

regulator, and thereby achieving improved high frequency PSR performance. The current-feedback loop essentially operates the pass transistor as a current-controlled current source, and the reference for the relatively faster current loop is set by the (outer) voltage loop. One of the additional benefits of the proposed architecture is that the current loop being an internal feedback loop to the outer voltage loop, the parasitic pole located at the output of the error amplifier is effectively pushed out in frequency, thereby enabling higher bandwidth and good phase margin for improved stability.

The proposed regulator was designed and fabricated using Linear Technology Corp.'s (LTC) 1.5 μ m Bipolar process technology. Experimental results demonstrating the benefits of the proposed architecture have shown a 20dB improvement (in the lowest PSR across wide frequency range up to 10MHz) over conventional LDO regulators. Moreover, the regulator has been able to achieve relatively high bandwidth of 1.85MHz using 15nF of output capacitor while maintaining good phase margin. In addition, the proposed regulator has also been shown to deliver 5mA of load current at input voltages as low as 1.4V.

Ultimately, a novel approach to achieve good high frequency (up to 10MHz) PSR performance has been presented. The proposed current-mode LDO regulator achieves high PSR without increasing the dropout voltage of the regulator; hence, without compromising its efficiency. Moreover, unlike other state-of-the-art techniques, the number and size of passive components required to achieve good PSR performance is minimal; in fact, only a small 15nF off-chip capacitor is needed for stability and good PSR performance. Finally, the proposed architecture will find a variety of applications in

future portable electronic devices, especially for low-noise applications that need to be powered using switched-mode power supplies (SMPS) for high efficiency.

4.6 Recommendation/Future Research

The ever increasing drive towards smaller solution size for electronic devices will inevitably push for more integrated power management solutions. Without relying on bulky magnetic components, LDO regulators are particularly well suited for such applications. With this in mind, the proposed current-mode architecture can be made into a system-on-chip (SoC) type of solution by integrating the relatively small output capacitor on the same silicon as the regulator. A variety of capacitor multiplier techniques have been studied, such as in [28], that be leveraged into integrating the 15nF output capacitor. Moreover, as had been seen from the PSR results shown earlier, the frequency-shaped transconductor used for the current loop does not have negligible gain at low frequencies, and this is another area that can be addressed in the future. Finally, a hybrid of the proposed topology and some of the state-of-the-art techniques, such as the active feedforward ripple-cancellation technique as used in [22], can be studied to find out if even better performance can be achieved.

APPENDIX A

MATHEMATICAL ANALYSIS OF DUAL-LOOP FEEDBACK

SYSTEMS

Dual-loop control systems are widely used in power converters, and although intuitive models are widely available while designing these circuits, it undoubtedly helps to rigorously analyze the internals of multiple feedback loops when leveraging more functionality out of it. This is especially true with frequency shaping the current-feedback loop in the proposed current-mode architecture. The figure below shows a general block level description of dual-loop control systems.

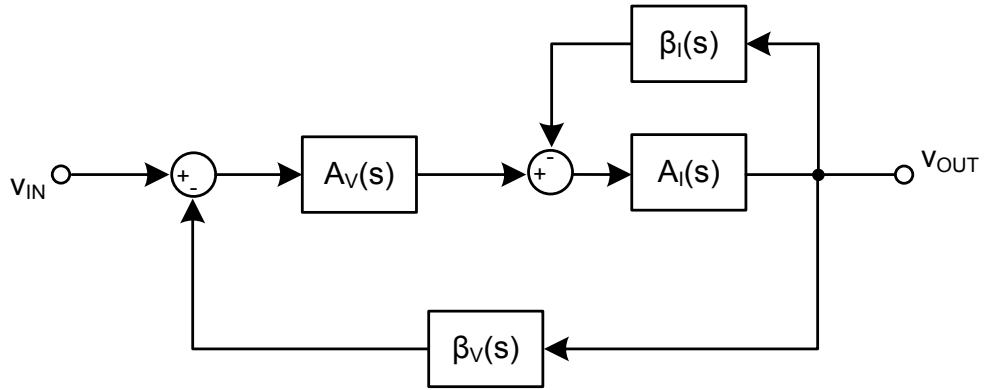


Figure A.1: A basic dual-loop feedback control system.

The transfer function from v_{IN} to v_{OUT} can be calculated as follows:

$$((v_{IN} - \beta_V v_{OUT})A_V - \beta_I v_{OUT})A_I = v_{OUT} \cdot \tag{A.1}$$

Re-arranging the terms in the above equation yields the following relationship between v_{IN} and v_{OUT} :

$$\frac{v_{OUT}}{v_{IN}} = \frac{A_I A_V}{1 + (A_I \beta_I + A_I A_V \beta_V)} \quad (A.2)$$

$$\Rightarrow \frac{v_{OUT}}{v_{IN}} = \frac{\frac{A_I}{1 + A_I \beta_I} A_V}{1 + \frac{A_I}{1 + A_I \beta_I} A_V \beta_V}$$

However, the above equation can be further simplified as follows:

$$\frac{A_I}{1 + A_I \beta_I} = A_{I-CL} \quad (A.3)$$

Hence,

$$\frac{v_{OUT}}{v_{IN}} = \frac{A_{I-CL} A_V}{1 + A_{I-CL} A_V \beta_V} \quad (A.4)$$

Equation A.4 represents the overall transfer function of the main loop (that is the voltage loop). However, when the current loop is frequency-shaped, as equation A.3 suggests, the overall transfer function from v_{IN} to v_{OUT} will subsequently change. Furthermore, based on the above equations, the loop gains LG_I and LG_V of the current and voltage loops, respectively, which is used to for stability analysis, is determined as follows:

$$LG_I = A_I \beta_I \quad (A.5)$$

and

$$LG_V = A_{I-CL} A_V \beta_V \quad (A.6)$$

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