Double-Layer No-Flow Underfill Process for Flip-Chip Applications

Zhuqing Zhang, Jicun Lu, and C. P. Wong, *Fellow, IEEE*

Abstract—No-flow underfill technology shows potential advantages over the conventional underfill technology toward a low-cost flip-chip underfill process. However, due to the filler entrapment in between solder bumps and contact pads on board, no-flow underfills are mostly unfilled or filled with very low filler loading. The high coefficient of thermal expansion (CTE) of the polymer material has significantly lowered the reliability of flip chip assembly and has limited its application to large chip assemblies. This paper presents a double-layer no-flow underfill process approach to incorporate silica filler into a no-flow underfill. Two layers of underfills are applied on to the substrate before chip placement. The bottom underfill layer facing the substrate is fluxed and unfilled; the upper layer facing the chip is filled with silica fillers. The total filler loading of the mixture is estimated to be around 55 wt%. The material properties of each layer of underfills, the underfill mixture, and a control unfilled underfill are characterized using differential scanning calorimeter (DCS), thermo-mechanical analyzer (TMA), dynamic mechanical analyzer (DMA), and a stress rheometer. FB250 daisy-chained test chips are assembled on FR-4 boards using the novel approach. A 100% assembly yield of solder interconnect is achieved with the double-layer no-flow underfill while in the single-layer no-flow underfill process, no solder joint yield is observed. Scanning electronic microscope (SEM) and optical microscope are used to investigate the cross-section of both assemblies. A US provisional patent has been filed for this invention.

Index Terms—Assembly yield, flip-chip, silica fillers, underfill.

I. INTRODUCTION

FLIP-CHIP technology is a first-level interconnection technique in which the active side of a silicon chip is faced down toward and mounted onto a substrate. Flip-chip has advantages over other interconnection methods including high I/O counts, better electrical performance, high throughput, and low profile, etc. [1]. Recently, the desire for low cost, mass production has resulted in the growing use of organic substrate instead of ceramics. Underfill technology has become one of the keys to the success of flip-chip on board since it alleviates the thermal stress on the solder joint caused by the mismatch in the coefficient of thermal expansion (CTE) between the silicon and the organic substrate, and hence enhances the package reliability significantly [2], [3]. However, the current flip-chip underfill process involves multiple steps including fluxing dispensing, chip placement, solder reflow, flux cleansing, under-

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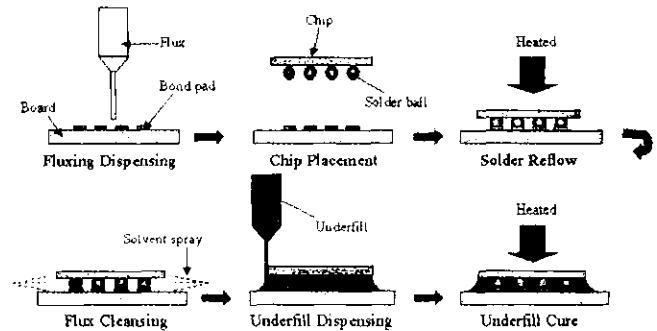
Fig. 1. Conventional flip-chip underfill process.

fill dispensing, and underfill curing (Fig. 1). The dispensing of underfill relies on capillary force to draw the liquid underfill into the gap between the chip and the substrate. The capillary flow is usually slow and can be incomplete, resulting in voids. It also produces nonhomogeneity in the resin/filler system. The curing of the underfill takes hours in the oven, consuming additional manufacturing time [4]. With increasing I/O counts and decreasing gap distance, flux cleansing becomes difficult, while the incompatibility between no-clean flux residues and underfill has caused reliability issues in flip-chip packages [5]. The time to underfilling a chip increases with the increase in chip dimension and the decrease in gap distance, which further aggravates the problems related to the conventional underfill [6].

In order to address these problems associated with conventional underfill, efforts have been made to modify the underfill process [7]–[10]. Several innovative approaches have been developed including no-flow underfill [11], [12], molded underfill [13], [14], and wafer-level underfill [15], [16]. No-flow underfill technology simplifies the underfill process by eliminating the capillary flow and combining the fluxing, solder reflow and underfill curing into one step. The process of no-flow underfill is illustrated in Fig. 2. The idea of integreted flux and encapsulant was proposed in the early 1990s [11]. The first successful underfill material was development and patented by Wong and Shi [17]. This process has been developed for several years, and it is evaluated and gaining acceptance in industrial. However, since the underfill is dispensed before the solder joints are made, there are chances that the silica fillers might be trapped in between the solder bumps and contact pads, and hence prevent the formation of solder joints during reflow [18]. So due to the interference of silica fillers with solder joint yield, no-flow underfills are mostly unfilled or of very low filler loading. The high CTE of the material limits the package reliability, especially in the case of large dies.

Fig. 2.　No-flow underfill process.

Fig. 3.　Double-layer no-flow underfill process.

TABLE I
PROCESSES AND UNDERFILL MATERIALS APPLIED IN ASSEMBLIES 1 AND 2

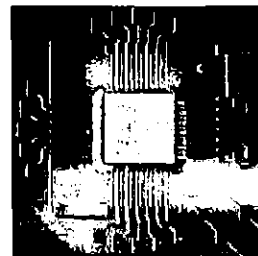|	Process	Underfill
Assembly 1	Double-layer	BL: Bottom layer (unfilled, with flux)
		UL: Upper layer (65 wt% silica-filled, without flux)
Assembly 2	Single layer	M: Mixture (1:1 volume ratio) of Underfills BL and UL

Fig. 4.　Picture of assembled chip and board.

This paper presents a novel double-layer no-flow underfill process to incorporate silica filler into the no-flow underfill to enable a high-yield, high-reliability flip-chip underfill packages.

II. PROCESS DESCRIPTION

The previous study has shown that in the filled no-flow underfill, the main cause of low assembly yield in assembly is the entrapment of silica fillers in between the solder bumps on the chip and the contact pads on the board [18]. If the fillers can be prevented from entering into the gap between the solder bumps and contact pads, the addition of fillers should not interfere with the formation of solder joint. In the present process, two layers of no-flow underfill are applied. The bottom layer underfill is relatively high in viscosity and is not filled with silica fillers. It is applied onto the substrate first. Then the upper layer underfill heavily filled with silica is applied on top of the first layer. The chip is then placed onto the substrate and reflowed, during which the solder joints are formed and the underfill is cured, or partially cured. The process flow is illustrated in Fig. 3. A U.S. provisional patent (GTRC ID 2485) has been filed for this invention [19].

III. ASSEMBLY

In order to investigate the feasibility of this process, FB250 bumped chips and FR-4 board with pads matching the bumps were used in this study. The chip was of 6.3 × 6.3 mm in size and had 48 peripheral bumps. The bump pitch was 457 μm (18 mil). All of the bumps were daisy chained for electric continuity testing. Each bump had a passivation opening of 102 μm, and height and diameter of 140 μm and 190 μm respectively. The solder mask on the FR-4 board was about 40 μm in thickness, and Cu trace about 20 μm. The Cu pads were finished with

Ni/Au to prevent surface oxidation and facilitate solder wetting. They were all designed to be solder-mask-defined in one direction, and pad-defined in the perpendicular direction. Prior to assembly, the boards were baked in an oven at a temperature of 125 °C for 2 h.

A number of dispensing approaches are capable of applying the bottom layer underfill on the board including coating, spray, printing, and laminating, etc. For simplicity, underfill was printed onto the solder mask opening using solder mask as a natural stencil. Then, a drop of the 65 wt% silica-filled underfill with prescribed quantity was dispensed on the center of chip site on the board. The average parameter of silica filler is 5 μm. The chip was placed on the board and reflowed with the same profile as that in the wetting test. Then the whole assembly was reflowed in an Electrovert Omniflo 5 convection reflow oven. The temperatures in the five zones of the oven were setup as 110 °C, 135 °C, 200 °C, 225 °C, and 150 °C respectively.

Two assemblies were compared in this study. Assembly 1 used the present double-layer underfill process, while Assembly 2 used the normal one-layer no-flow underfill process. The underfill materials applied in these two assemblies are described in Table I. In Assembly 1, Underfills BL and UL were applied in sequence according to the previous description. Underfill BL was the bottom layer underfill without silica fillers, and it had the fluxing capability. Underfill UL was the upper layer underfill filled with silica fillers up to 65 wt% but without fluxing capability. In Assembly 2, a mixture of Underfills BL and UL was applied as a single layer in a normal no-flow underfill process. The reason for the 1 : 1 volume ratio was that the thickness of the bottom layer was estimated to be 40–60 μm according to the measurement from a profilometer, and that the gap distance of the chip to the substrate was around 110 μm according to SEM observation. So Underfill M represented the underfill mixtures that were applied in Assembly 1.

Fig. 4 shows a picture of assembled chip. After the reflow, the electrical integrity of the solder joints was tested. Results showed that all the solder joints were interconnected in As-
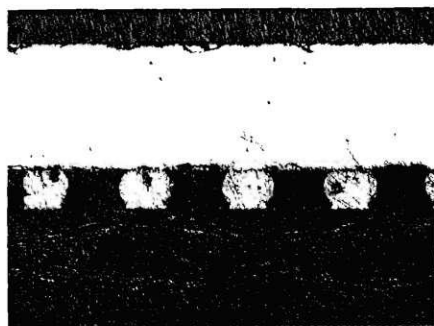
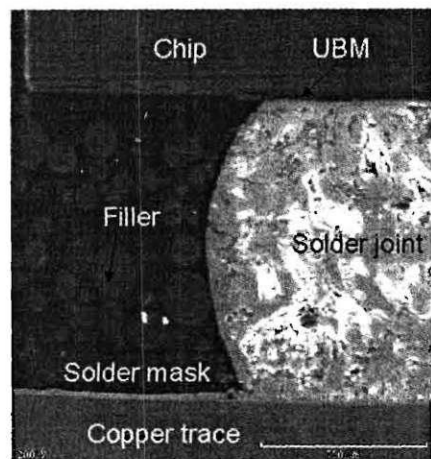Fig. 5 Optical microscope picture of the cross section of Assembly 1

Fig. 7. Optical microscope picture of cross section of Assembly 2.

Fig. 6. SEM picture of the cross section of Assembly 1.
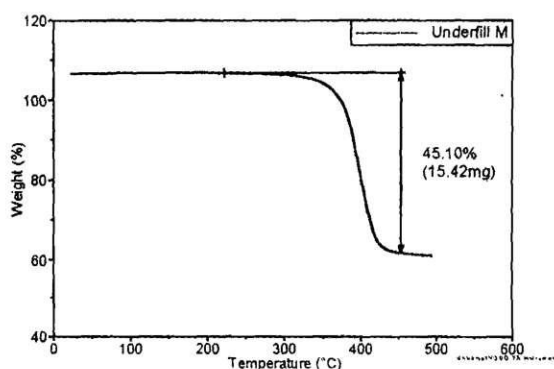
Fig. 8. Weight loss upon heating of Underfill M.

sembly 1, while in Assembly 2, none of the solder joints yielded. Although the materials applied as underfill in both assemblies were approximately the same, the double-layer underfill process had the advantage of high assembly yield, indicated by this result.

Optical microscope and SEM were used to confirm the solder joint integrity in Assembly 1 and the failure mechanism in Assembly 2. Fig. 5 shows the optical microscopic picture of the cross-section of Assembly 1. All the solder bumps wetted on the copper pad and formed the solder interconnects. Fig. 6 is a SEM picture of the Assembly 1 under high magnification. The observation on the silica fillers indicated that although two layers of underfills were applied prior to the solder reflow, after the reflow, there was no discernable separation of these two layers. These fillers tended to settle down at high reflow temperature when the viscosity of the underfill decreased. Since the upper layer Underfill UL does not contain fluxing agent, the results showed that the fluxing capability of the bottom layer Underfill BL was sufficient for solder wetting. Fig. 7 illustrates an optical microscope observation of a failed solder joint in Assembly 2. The fillers were trapped in between the solder bump and the contact pads, preventing the formation of a solder joint in the reflow process.

IV. MATERIAL CHARACTERIZATIONS

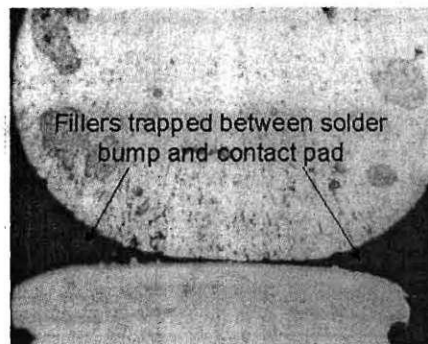In order to study the compatibility of the two underfill layers in Assembly 1 and to understand the relationship between the materials and process, the material properties of Underfills BL and UL in Assembly 1, and Underfill M in Assembly 2 were characterized and compared. A control sample, Underfill C, which was not filled with silica fillers but had fluxing agent incorporated, was also studied. Underfill C had the same curing system as Underfill UL, expect that it was not filled and had fluxing agent. Underfill C represents the normal, unfilled no-flow underfill material.

Filler Loading

The filler loading of Underfill M was estimated using Thermo-Gravimetric Analyzer (TGA) by TA Instruments, Model 2050. Fig. 8 presents the weight loss of Underfill M during heating in the TGA furnace at a heating rate of 5 °C/min under N_2 purge (77 ml/min in vertical direction and 12 ml/min in horizontal direction). The result suggests that the filler loading in Underfill M was about 55 wt%. Since Underfill M represented the mixture of Underfills BL and UL that were applied in Assembly 1, the actually filler loading of underfill in Assembly 1 was estimated to be around 55 wt%.

Curing Behavior

The curing behavior of the Underfills BL, UL, and M was investigated using a modulated Differential Scanning Calorimeter (DSC) by TA Instruments, Model 2920. A sample of about 10 mg was placed into a hermetic sample pan and heated in the DSC cell at 5 °C/min from room temperature to 300 °C under N_2 purge. The exothermic diagrams of Underfills BL, UL and M are shown in Fig. 9. It can be seen that Underfills BL and
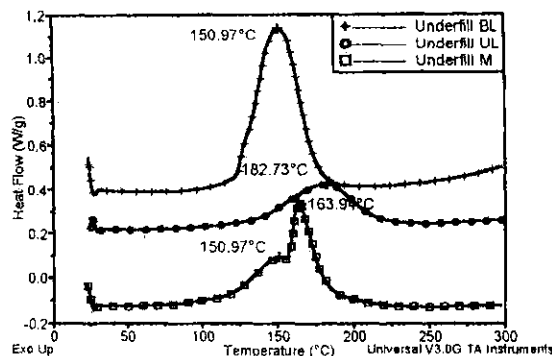
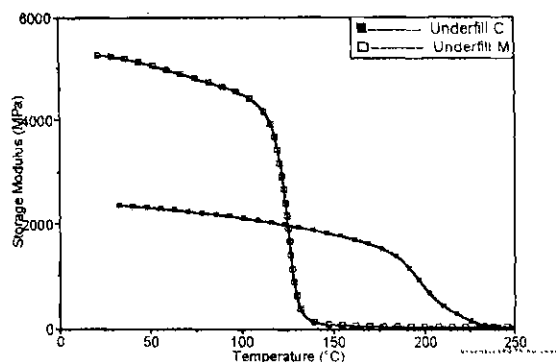Fig. 9. DSC curing behavior of Underfills BL, UL, and M.
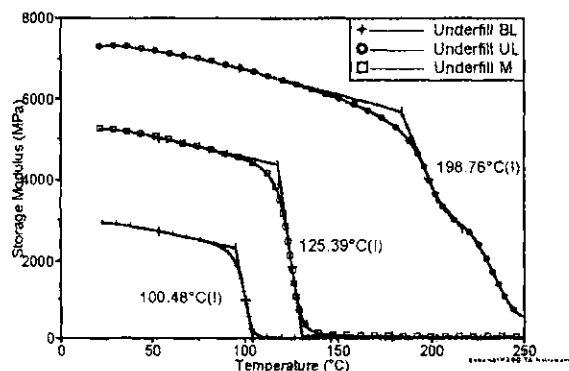

Fig. 10. Change of storage modulus of underfills BL, UL, and M.

Fig. 11. Change of storage modulus of Underfill M and Underfill C.

Fig. 12. Thermal expansion behavior of Underfill M and Underfill C

UL have different curing behavior since the two underfills were based on different epoxy curing systems. The mixture, Underfill M, displayed a two-step curing behavior.

Thermo-Mechanical Properties

In order to study the material properties of cured underfills, all the samples were placed in a convective oven, heated to 165 °C at a rate around 5 °C/min and continuously cured in the oven at 165 °C for an hour. Then the samples were immediately taken out to room temperature to cool down. Dynamic mechanical analyzer (DMA) by TA Instruments, Model 2980 was used to measure the dynamic moduli of the samples with respect to temperature. The sample dimension was about $18 \times 6 \times 2$ mm. The measurement was performed in a single cantilever mode under 1 Hz sinusoidal strain loading. The samples were heated at 3 °C/min in air to 250 °C. The coefficient of thermal expansion (CTE) of a cured sample was measured using a themo-mechanical analyzer (TMA) by TA Instruments, Model 2940. The dimension of the sample was about $5 \times 5 \times 2$ mm. The sample was heated in the TMA furnace to 250 °C at a rate of 5 °C/min.

Fig. 10 shows the change of storage modulus of Underfills BL, UL, and M with respect to temperature. It can be seen that although Underfill M displayed a two-step curing behavior illustrated by DSC, it only displayed a single Tg transition, indicating that there was no phase separation occurred. Fig. 11 compares the storage modulus of Underfill M with that of Underfill C. With fillers incorporated in the resin, Underfill M possessed
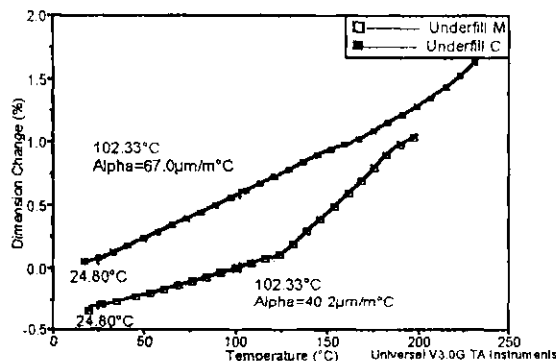
a much higher modulus at room temperature. The thermal expansion behaviors of Underfill M and Underfill C are illustrated in Fig. 12. The CTE of Underfill M was around 40 ppm/°C.

Moisture Absorption

The moisture absorption of cured materials of Underfill M and Underfill C was investigated. The samples were placed into an 85 °C/85% RH chamber after they were dried under vacuum at 125 °C over night. The weight changes at different time intervals were recorded and results are shown in Fig. 13. Due to the high filler loading in Underfill M, the moisture resistance has been improved significantly.

Rheology

The viscosity of Underfills BL, UL and M was studied using a stress rheometer by TA Instruments, Model AR 1000-N. The measurement was conducted under constant shear rate of 5.0 s^{-1}. The samples were heated from room temperature to 120 °C. The change of viscosity with respect to temperature is shown in Fig. 14. To maintain a viscosity difference between the upper and bottom layers is important for the success of the current approach, for the high viscosity of the bottom layer would prevent the fillers from settling down and entering into the gap between the solder bump and contact pad. As can be seen from Fig. 14, at room temperature, the viscosity of Underfill BL is much higher than that of Underfill UL. However, with the increase in temperature, Underfill UL showed a less dependence on temperature since it was heavily filled with

of fillers in between the solder bumps and contact pads. The solder joint integrity was examined by SEM and optical microscope observation. This double-layer no-flow underfill process showed a significant potential for a high-yield and high-reliability no-flow underfill process for large-die flip-chip applications. A US provisional patent has been filed for this invention.
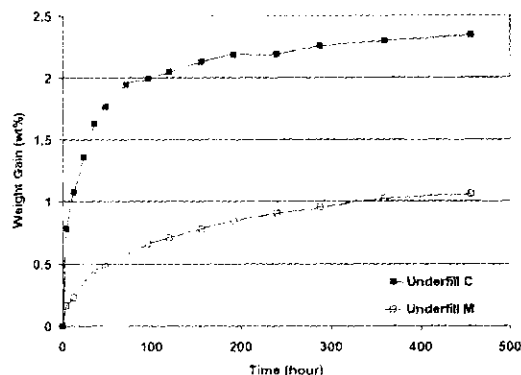

Fig. 13. Moisture absorption of Underfill M and Underfill C in an 85 °C/85% RH chamber.
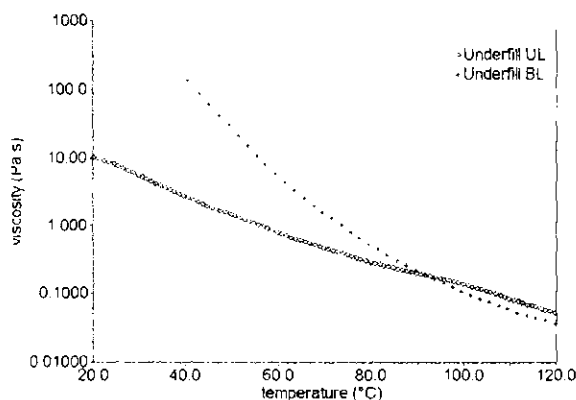

Fig. 14. Change of viscosity with temperature of Underfills BL and UL.

silica fillers. At temperature higher than 100 °C, the viscosity of Underfill BL became lower than that of Underfill UL, so fillers would tend to settle down. However, since solder reflow is a dynamic process, the wetting of solder on the pad will be determined by several simultaneous procedures including the decrease in underfill viscosity, the collapsing of the chip, the settling of the fillers, the curing of underfill, and the solder melting. As long as the chip can collapse onto the contact pad due to its own weight prior to the filler settling down onto the contact pad and forming a layer to prevent solder wetting, the chances of assembly yield would be much higher than in the case of a single-layer underfill process.

V. CONCLUSION

A novel double-layer no-flow underfill process for flip-chip applications has been developed and demonstrated. In this approach, two layers of underfills were applied onto the printed wiring board before the placement of the chip. The bottom layer was unfilled no-flow underfill and the upper layer was filled with silica fillers. The estimated total filler (in μm) loading was around 55 wt% and the CTE was 40 ppm/°C below Tg. Using FB250 bumped chips and FR4 board, high solder joint yield was achieved using the double-layer no-flow underfill process. The normal no-flow underfill process with silica fillers cannot achieve solder joint yield at the same filler loading due to the entrapment

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