A MULTI-CHANNEL NOISE DOSIMETER

A THESIS

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MULTICHANNEL NOISE DOSIMETER

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SUMMARY

In order to reduce industrial noise exposure the Occupational Safety and Health Act establishes the "Permissible Noise Exposure Levels". These are noise levels to which an individual can be exposed for certain limited periods of time without temporary or permanent auditory threshold shift.

Several manufacturers have developed lightweight integrating noise dosimeters that show directly or indirectly the percent of the allowable noise exposure. But the dosimeters are not provided with all the three frequency weighting networks as required by the American National Standard Institute (ANSI).

The purpose of this research is to design a portable multi-channel noise dosimeter that directly displays the cumulative noise exposure, and also meets the ANSI standard for sound level meters.

A four-channel dosimeter was designed and built to measure, respectively, the durations of noise levels equal to and above 85, 90, 95 and 100 dB.

The instrument consists principally of the noise detection system that detects and amplifies the noise signal, a root-mean-square (rms) circuit that determines the rms value of the signal, and four comparator circuits which independently drive four digital clocks after comparing the rms

voltage equivalent of the noise signal with four reference voltages. The reference voltages correspond with the rms voltage equivalent of 85, 90, 95 and 100 dB sound pressure levels.

The instrument was tested in the laboratory. It was found that the four channels respectively measure the durations of noise levels of (85 ± 1), (90 ± 1), (95 ± 1) and (100 ± 1) dB on A, B, C and F scales.

CHAPTER I

HISTORICAL INTRODUCTION

Physiological and other effects of excessive noise on people have been studied extensively and reported [1,2]. In most of these studies, losses in hearing sensitivity, both temporary and permanent, have been the concern of the researchers.

In 1831 Fosbroke [3] first recorded hearing losses in blacksmiths. Some thirty years later, E. H. Weber [3] reported hearing losses in boilermakers and railroad men. Since then there have been several reports of hearing difficulties in individuals from overexposure to intense noise [4,5].

In order to protect industrial employees from noise-induced hearing loss, the control of noise levels in industries has become necessary. Since the extent of hearing loss from noise exposure depends on many factors, such as the duration of the exposure and the intensity of the noise, it is necessary that permissible noise exposure limits be defined if industrial noise is to be controlled effectively.

The search for these permissible noise exposure limits has a long history. From the works of Glorig, Ward and Nixon [6], the CHABA* working group [7], Botsford [8] and

*CHABA is the abbreviation of "Committee on Hearing, Bioacoustics and Biomechanics."

others, a sound pressure level of 90 dB would be a widely acceptable criterion for eight hours of broadband steady state noise exposure. The Occupational Safety and Health Act [9] (OSHA) requires a halving of allowable exposure time for each 5 dB increase in noise level above 90 dB. Table 1 is a summary of the allowable noise exposure limits. These coincide with those given by the Walsh-Healy Act [10].

Table 1. Permissible Noise Exposures

Duration per Day in Hours	Noise Level in dB
16	85
8	90
4	95
2	100
1	105
1/2	110
1/4 or less	115

The Walsh-Healey Act requires that industrial noise levels in industries should be controlled by the employers so that the employees' exposure to noise do not exceed the limit values stated in Table 1. Secondly if the noise exposure is composed of two or more periods of noise exposure at different levels, their combined effect should be considered as follows: if

$$\frac{C_1}{T_1} + \frac{C_2}{T_2} + \ldots + \frac{C_N}{T_N}^{*} > 1$$

then the mixed exposure should be considered to exceed the limit value.

The preferred method of control is to reduce the noise at its source even though this method is expensive. A less expensive, but not very reliable noise reduction measure is the use of protective hearing equipment such as earplugs.

A third alternative method is an administrative control whereby an employee is not exposed to excessive noise for long periods of time.

In order to apply this method the employer has to measure the cumulative noise exposure experienced by his employees in order to insure that the limits listed in Table 1 are not exceeded.

If the noise level is constant in time or is not varying rapidly, then probably a clock and a sound level meter may be used to make the required measurements. However, industrial noise generally has a complex spectrum which varies rapidly with time. Obviously it would be impossible to use the simple technique mentioned above to measure the noise exposure levels. A suitable instrument would be one

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*C_N indicates the total time of exposure at a specified noise level, and T_N indicates the total time of exposure permitted at that level.

which displays the accumulated exposure without the necessity of an operator.

Several manufacturers have developed integrating dosimeters that compute the percent of the allowable noise exposure to which the individual has been exposed, the so called cumulative exposure factor. Current examples are: Conwed's Noise Exposure Integrator [11], the Personal Noise Dosimeter manufactured by Columbia Research Laboratories [12], Computer Electronic's Noise Dosimeter [13] and Du Pont E100 Audio Dosimeter [14].

All these instruments are lightweight and are worn by the workers. That is an advantage. The disadvantage is that the manufacturers have to omit some important features in order to make their instruments small enough to be worn by the employees. In the Noise Exposure Integrator and the Personal Noise Dosimeter, the cumulative noise factor is computed and displayed directly. However, their sound level meters are equipped with only the A frequency weighting* network. In the Computer Electronics and Du Pont E100 Dosimeters, not only are other weighting networks missing but also the readout units are not part of the dosimeter units. Thus a worker has to wait until the end of the work shift in order to read and compute the cumulative noise factor, in which case the person could have received an excessive exposure without warning.

*The frequency weighting networks are described fully in later sections.

The multi channel noise dosimeter of the present work is designed to avoid the serious drawback in the latter two instruments. At the same time, all the frequency weighting networks are built in the sound detection system as required by the American National Standard Institute.

CHAPTER II

GENERAL DESCRIPTION OF THE MULTI-CHANNEL NOISE DOSIMETER

The dosimeter as illustrated in Figure 1 is principally composed of a sound level detector, a root-mean-square circuit, four comparators, four transmission gates and five digital clocks.

The sound level detector consists of a microphone, a pre-amplifier, an attenuator, and four weighting networks, designated A, B, C, F. The microphone transduces the acoustic noise incident on it to an electrical signal. This electrical signal is then amplified and applied to the input of one of the weighting networks as determined by a selector switch. Simultaneously, the selector switch applies the output of the selected weighting network to the root-mean-square circuit which determines the root mean square value of the signal. Each comparator compares the dc output of the root mean square circuit with a stable reference voltage. The four reference voltages correspond respectively to the four noise exposure levels whose durations are to be measured, i.e. 85, 90, 95, and 100 dB. The output of each comparator is fed into one of the two inputs of an AND gate whose output drives a digital clock. Pulses at one second intervals are

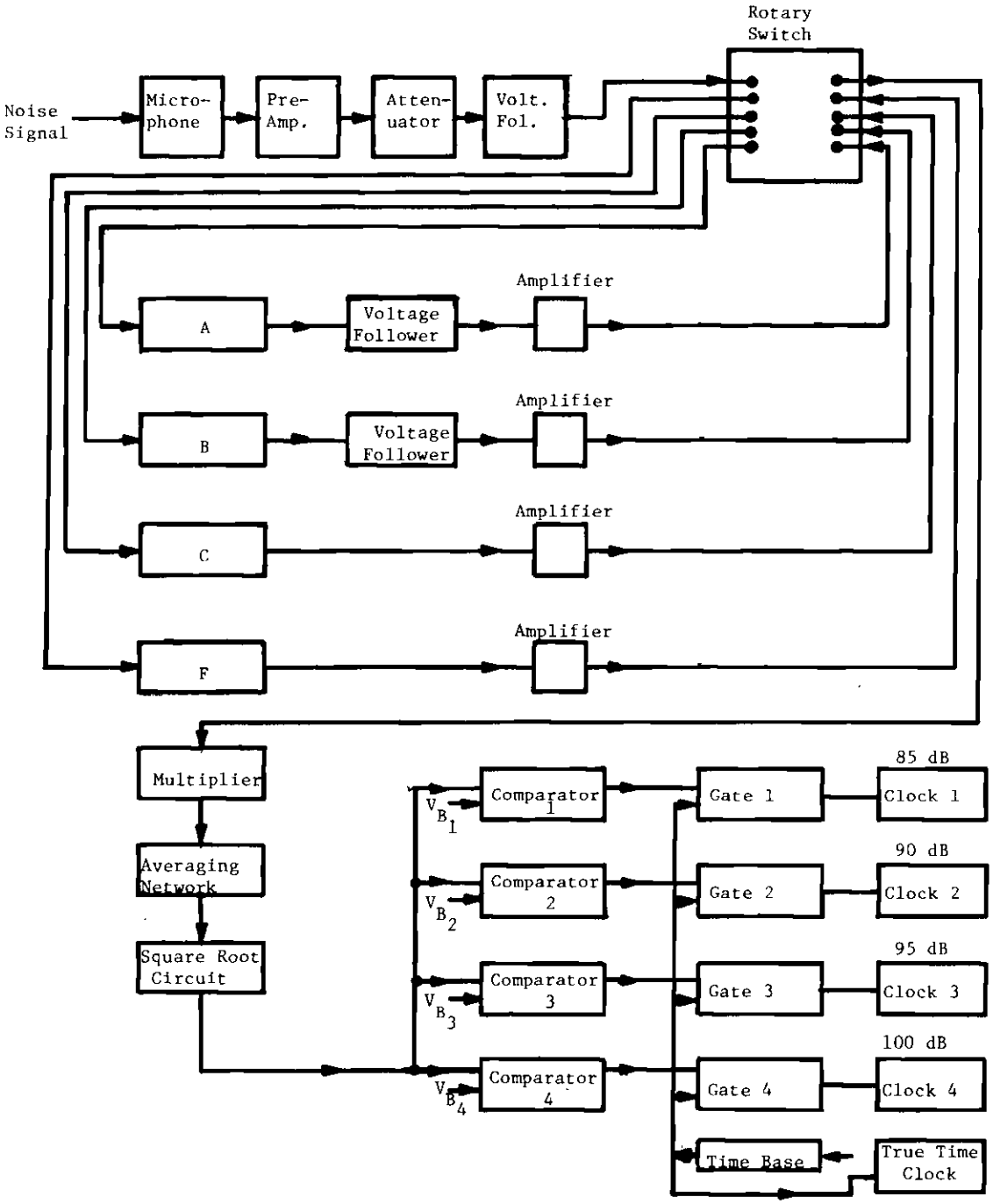

Figure 1. Block Diagram of the Multi-Channel Noise Dosimeter. (Frequency Weighting Networks are denoted by A, B, C and F.)

applied to the other input of the AND gates. When the noise level exceeds any of the reference levels the corresponding comparator's output registers logical 1. The AND gate then allows the clock pulses to be transmitted and recorded. The number of clocks in operation depends on the magnitude of noise level. For example if the noise level is equal to or exceeds 100 dB, all the clocks would record time; if it is less than 85 dB only the real time clock would record time.

There are other circuits which are shown in Figure 1 besides those mentioned above: an emitter follower is used as a buffer stage between the attenuator and the frequency weighting networks, amplifiers are added following the weighting networks to raise the level of the signal.

CHAPTER III

CIRCUIT DESIGNS

1. Pre-Amplifier Circuit

The pre-amplifier must have the following properties in order to accomplish its function in the noise dosimeter.

(a) The input impedance of the pre-amplifier should be high compared with the maximum output impedance of the microphone so that the voltage appearing across the input terminals of the pre-amplifier is essentially the open circuit voltage generated by the microphone.

(b) It must be able to deliver at least a voltage of one volt across a 1000 ohm load.

(c) The bandwidth of the pre-amplifier must exceed that of the microphone.

(d) The amplifier must have negative feedback to stabilize its gain and reduce distortion.

The General Radio 1560-85 microphone was employed in the design of the dosimeter. It has a sensitivity of -40 dB re 1 volt/N/m^2 which implies that the microphone generates a voltage of 10^{-2} volts, whenever the sound pressure is 1 N/m^2.

Now for the amplifier to produce at least 1 volt across 1000 ohm load, its voltage gain, G, as calculated

from equation (1) must be 40 dB

$$G = 20\text{dB} \log_{10} \frac{1 \text{ volt/N/m}^2}{V_p} \quad (1)$$

where V_p is the voltage generated at the output of the microphone which, as determined above, is equal to 10^{-2} V when the sound pressure level is 1 newton per meter squared.

Design of the Basic Amplifier

The number of stages required is determined by the minimum voltage gain per stage. The midband gain per stage, A_v, for a common emitter amplifier is given* approximately by

$$A_v = -h_{fe}R_L/h_{ie} \quad (2)$$

where h_{fe} and h_{ie} are the current gain and input impedance of the transistor respectively. R_L is the load impedance. Now for the transistor 2N3391A,

$$h_{fe} = 340$$

$$h_{ie} = 4.8 \times 10^3 \text{ ohm}$$

If R_L is equal to 1000 ohm, then

*See Appendix A.

$$|A_V| = 34 \text{ dB} \tag{3}$$

Since the minimum gain of the amplifier must be 40 dB, a two-stage amplifier will be sufficient to satisfy the voltage gain requirement.

In order to satisfy the high input impedance requirement, the first stage is a source follower bootstrapped to yield a high input impedance in the megohm range. Its voltage gain of approximately unity would not appreciably affect the overall voltage gain of the pre-amplifier.

The source follower and its equivalent circuit are shown in Figures 2 and 3. The design of the source follower involves choosing suitable values for R_g, R_1, R_2 and the supply voltage V_{DD}.

From the dc load line equation given by equation (4) and the loop equation at the input terminals given by equation (5), R_1, R_2 can be calculated if all other parameters are known. (Refer to Figure 2.)

$$I_D(R_1+R_2) = V_{DD} - V_{DS} \tag{4}$$

$$I_D R_1 + V_{gs} = I_G R_g \tag{5}$$

where I_D is the drain current

I_G is the gate current

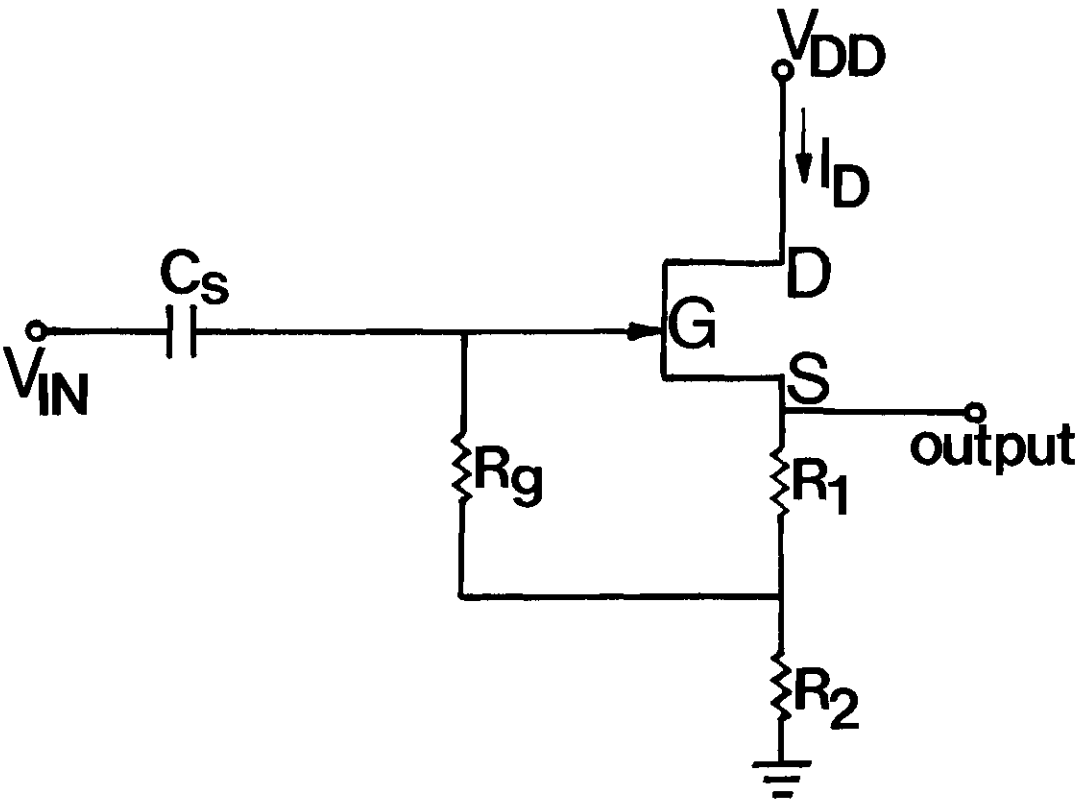

Figure 2. The Source Follower Circuit

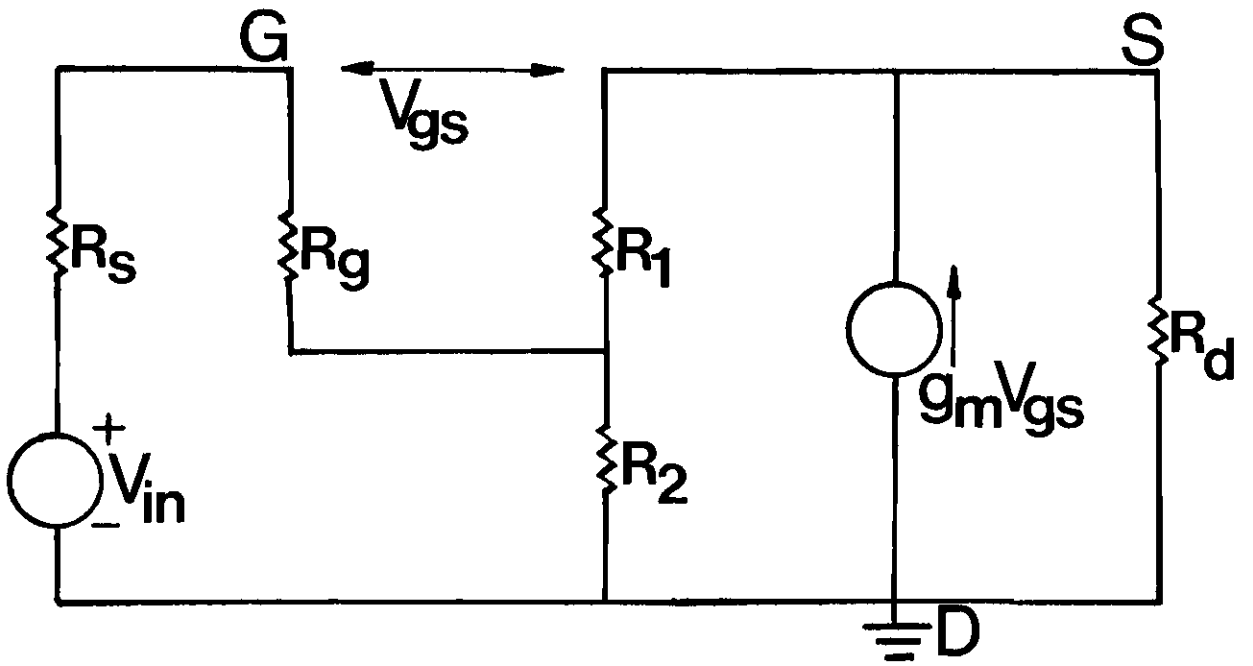

Figure 3. Mid-Frequency Equivalent Circuit of the Source Follower

V_{gs}, the gate to source voltage

V_{DS} is the drain to source voltage

The operating point conditions for the transistor 2N5459 are

$$I_{DQ} = 3mA$$

$$V_{DSQ} = 10\ V$$

V_{gs} at quiescent = -0.6 V

The size of R_g is obtained by applying the condition imposed on the input impedance, Z_i, of the source follower, i.e.

$$Z_i >> Z_m \tag{6}$$

where Z_m is the internal impedance of the microphone which is a capacitance C_m of 385 pF. Allowing 50 pF for the capacitance, C associated with the cable connecting the microphone to the amplifier, the total equivalent capacitance is 435 pF (see Figure 4). Hence the total maximum impedance Z_m' shunting the input impedance of the amplifier is given by

$$Z_m' = \frac{1}{2\pi f \times 435 \times 10^{-12}} \text{ ohms} \tag{7}$$

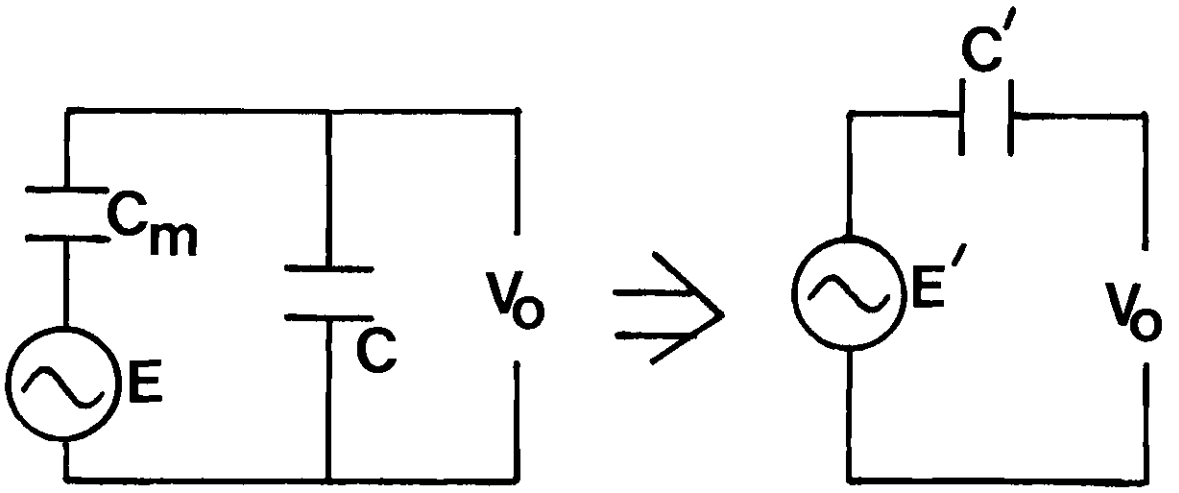

Figure 4. The Microphone's Equivalent Circuit

C_m represents the microphone

C is the capacitance associated with the connecting cable

C_m = 385 pF

C = 50 pF

C' = 435 pF

$$E' = \frac{1/50}{1/50 + 1/385} E$$

v_o = the output voltage

where f is the lowest frequency in the audio frequency spectrum which is 20 Hz. Substituting 20 Hz for f in equation (7).

$$Z_m' = 1.8 \times 10^7 \text{ ohms}$$

Referring to Figure 3, the input impedance, Z_i, of the source follower is given [15] by

$$Z_i = \frac{R_g}{1 - \frac{R_2}{R_1+R_2} K_v} \tag{8}$$

where K_v is the voltage gain of the source follower and is given [15] by equation (9)

$$K_v = \frac{g_m}{g_m + \frac{1}{R_d} + \frac{1}{R_1+R_2}} \tag{9}$$

$g_m \equiv$ transconductance = 4 mmho.

R_d is the drain resistance of the order of 30 kilohms for the transistor 2N5459. The quantity K_v of the source follower is approximately equal to unity. Hence the input impedance, Z_i, of the source follower will be large if $\frac{R_2}{R_1+R_2}$ is close to unity. Suppose

$$\frac{R_2}{R_1+R_2} = .95 \tag{10}$$

Then from equation (4)

$$R_1+R_2 = \frac{(15-10)\text{ volts}}{3\text{mA}}$$

$$= \frac{5}{3} \times 10^3 \text{ ohms} \qquad (11)$$

if the supply voltage V_{DD} is 15 volts. From equations (10) and (11),

$$R_2 = 1.55 \times 10^3 \text{ ohms}$$

$$R_1 = 0.1 \times 10^3 \text{ ohms}$$

The actual values selected for R_1 and R_2 were

$$R_2 = 1.5 \times 10^3 \text{ ohms}$$

$$R_1 = 100 \text{ ohms}$$

From equation (8), assuming that $K_v \approx 1$,

$$Z_i = 2 R_g$$

Now R_g is 10^9 ohms.

$$Z_i = 2 \times 10^9 \text{ ohms}$$

which is about 200 times the impedance Z_m'.

The output impedance, Z_o, of the unloaded source follower is given [16] by

$$Z_o = \frac{1}{g_m + \frac{1}{R_d} + \frac{1}{R_1+R_2}} \tag{12}$$

$$\approx 390 \text{ ohms}$$

Design of the Basic Amplifier

The basic amplifier circuit is shown in Figure 5. Operating point or quiescent conditions are:

$$I_{CQ} = 1.3 \text{ mA}$$

$$V_{CEQ} = 5 \text{ V}$$

$$V_{CC} = +15 \text{ V}$$

2N3391A transistor parameters are:

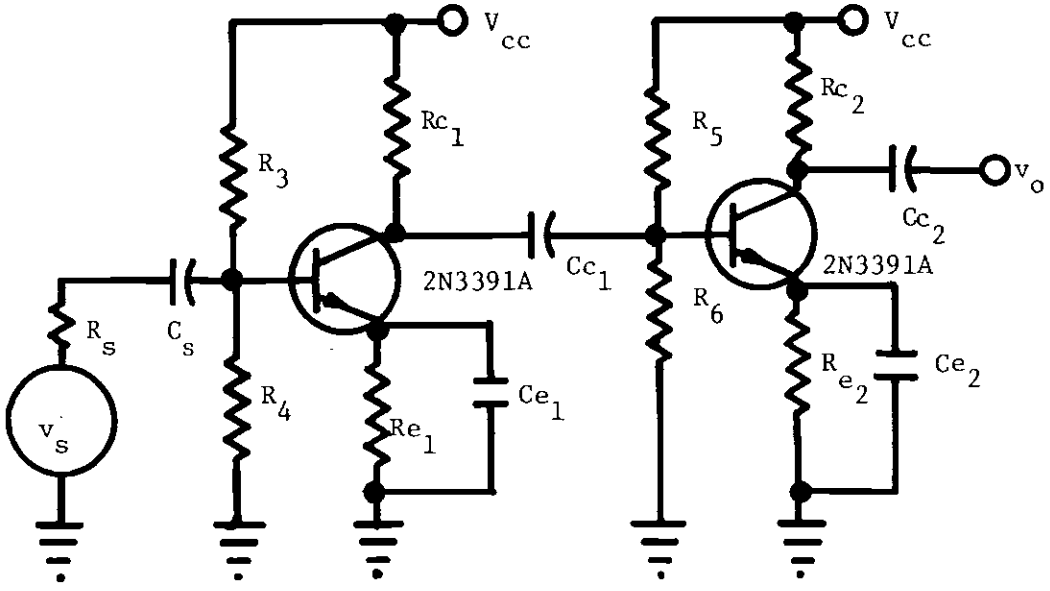

Figure 5. Basic Two-Stage Common Emitter Amplifier Circuit.

$$h_{fe}^{*} = 340$$

$$h_{ie} = 4.8 \times 10^{3} \text{ ohms}$$

$$h_{oe} = 36.4 \times 10^{-6} \text{ mho}$$

$$h_{re} = 4.1 \times 10^{-4}$$

Considering a single stage, the dc equivalent biasing circuit is shown in Figure 6.

Applying loop equations for the emitter-collector circuit and then base-emitter circuit, equations (13) and (14) can be written by inspection.

$$V_{CC} = R_c I_{CQ} + V_{CEQ} + R_e I_E \tag{13}$$

$$V_{BB} = (R_b + R_e)\, I_B + R_e I_E + V_{BE} \tag{14}$$

where R_b is the base bias resistance which is equal to $R_3 // R_4$.**

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*I_{CQ}, V_{CEQ} respectively denote the collector current and collector to emitter voltage at quiescent point.
h_{fe} is the small signal transistor current amplification factor.
h_{ie} is the input impedance of the transistor.
h_{oe} is the output admittance of the transistor.
h_{re} is the reverse voltage gain of the transistor.

** $R_3 // R_4$ means the parallel combination of R_3 and R_4.

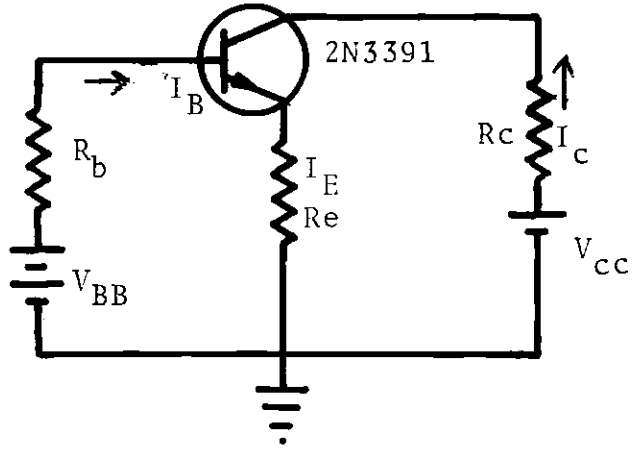

Figure 6. D.C. Equivalent Biasing Circuit. I_E is emitter current, I_B the base current and I_c the collector current. $R_b = R_3//R_4$

V_{BB} is the base bias voltage. Assuming that $I_E \simeq I_C$ for design purposes,

$$R_e + R_c = \frac{V_{CC}-V_{CEQ}}{I_{CQ}} \qquad (15)$$

$$= \frac{10}{1.3 \times 10^{-3}} \text{ ohms}$$

$$= 7.7 \times 10^3 \text{ ohms}$$

R_c, R_e were chosen to be 6.8×10^3 ohms and 500 ohms respectively. The actual collector current will then be about 1.37 mA. R_b should be much larger than the input impedance of the transistor which is approximately equal to h_{ie} ($= 4.8 \times 10^3$ ohms) in order to limit the loading effect of R_b.

R_b was chosen to be equal to 30×10^3 ohms, i.e.,

$$R_b = 6 \times h_{ie}$$

Hence from equation (14)

$$V_{BB} = (30 \times 10^3 + 0.5 \times 10^3)(1.37/340)\times 10^{-3} + 0.5 \times 1.37 + 0.6$$

$$= 1.40 \text{ volts}$$

where $I_B = \frac{I_c}{h_{fe}}$ is applied.

From Figure 4, the voltage divider resistances R_3 and R_4 are given by equation (16).

$$\frac{V_{BB}}{R_4} = \frac{V_{CC}}{R_3+R_4} \tag{16}$$

Equation (16) can be written as

$$V_{BB} = \frac{R_4 \ R_3}{R_3(R_3+R_4)} \ V_{CC} \tag{17}$$

$$V_{BB} = \frac{R_b \ V_{CC}}{R_3} \tag{18}$$

where

$$R_b = \frac{R_3 \ R_4}{R_3+R_4} \tag{19}$$

From equation (18)

$$R_3 = \frac{30 \times 10^3 \times 15}{1.4} \text{ ohms}$$

$$= 321 \times 10^3 \text{ ohms}$$

The actual value of R_3 selected was 330×10^3 ohms.

If $R_3 = 330 \times 10^3$ ohms

then $R_4 = 33 \times 10^3$ ohms

For simplicity, the stages were designed to be identical, hence

$$Re_1 = Re_2 = 500 \text{ ohms}$$

$$Rc_1 = Rc_2 = 6.8 \times 10^3 \text{ ohms}$$

$$R_3 = R_5 = 330 \times 10^3 \text{ ohms}$$

$$R_4 = R_6 = 33 \times 10^3 \text{ ohms}$$

Calculations of Coupling and Bypass Capacitors

The sizes of the coupling and bypass capacitors determine the lower cut off frequency of the amplifier which was set at 15 Hz.

Now the low frequency voltage gain $A_v'(s)$ of a single stage common emitter amplifier is given [16] by

$$A_v'(s) = A_v \frac{s^2(s+\omega_e)}{(s+\omega_c)(s+\omega_d)(s+\omega_m)} \tag{20}$$

where A_v is the midfrequency voltage gain, and

$$\omega_e = \frac{1}{R_e C_e} \tag{21}$$

$$\omega_c = \frac{1}{(R_c+R_b//h_{ie})C_c} \tag{22}$$

$$\omega_d = \omega_{ss} + \omega_{es} \tag{23}$$

$$\omega_{ss} = \frac{1}{R_{ss}\ C_s} \tag{24}$$

$$\omega_{es} = \frac{1 + h_{fe}}{R_{ss}\ C_e} \tag{25}$$

$$\omega_m = \frac{\omega_e\ \omega_{ss}}{\omega_d} \tag{26}$$

$$R_{ss} = R_s + h_{ie} \tag{27}$$

R_s is the source impedance. ω_d is the so-called dominant frequency which controls the lower half power frequency. Hence

$$\omega_d = 2\pi f_L$$

where f_L = 15 Hz.

$$\omega_d = \omega_{ss} + \omega_{es} = (2\pi \times 15) \text{ radians/sec} \tag{28}$$

If for simplicity ω_{ss} is made equal to ω_{es}, then from equation (25) the emitter bypass capacitor, C_e, can be calculated

$$C_e = \frac{1 + h_{fe}}{15\pi \times R_{ss}} \tag{29}$$

Now $R_{ss} = 390 \text{ ohms} + 4.8 \times 10^3 \text{ ohms}$

$h_{fe} = 340$

Then $C_e = 1340\ \mu F$

Now $C_s = \dfrac{1}{15\pi \times R_{ss}}$

$\tilde{=} 4\mu F$

C_s was chosen to be $5\mu F$ This reduces ω_{ss} and ω_{es} and increases C_e to $2000\mu F$.

$$C_s = 5\mu F$$

$$C_e = 2000\mu F$$

The capacitor, C_c, that couples the first stage to the second stage adds another break point as determined by ω_e at the low frequency end of the amplifier's frequency response. ω_c is therefore chosen less than ω_d, the dominant frequency.

Suppose

$$\omega_c = 10\pi \text{ radians/sec}$$

then $$C_c = \frac{10^{-3}}{10\pi\ (6.8 + 33//4.8)} \text{ farad} \qquad (30)$$

$$= 5.6\mu F$$

The practical choice for C_c was 5 μF. Summarizing,

$$C_s = C_{c_1} = 5\mu F$$

$$C_{c_1} = C_{c_2} = 5\mu F$$

$$C_{e_1} = C_{e_2} = 2000\mu F$$

Design of the Two-Stage Common Emitter Amplifier with Feedback

Two types of negative feedback circuits were applied to the basic amplifier circuit:

1. Unbypassed emitter resistor, R_7, that provides local negative feedback to the first stage.
2. Collector-Emitter feedback via R_f.

R_7 and R_f will be chosen such that the overall gain of the amplifier with feedback will be at least equal to 40 dB.

Voltage Gain of the Two-Stage Amplifier Without Feedback

The voltage gain, $A_v(s)$, of the two-stage amplifier is given by

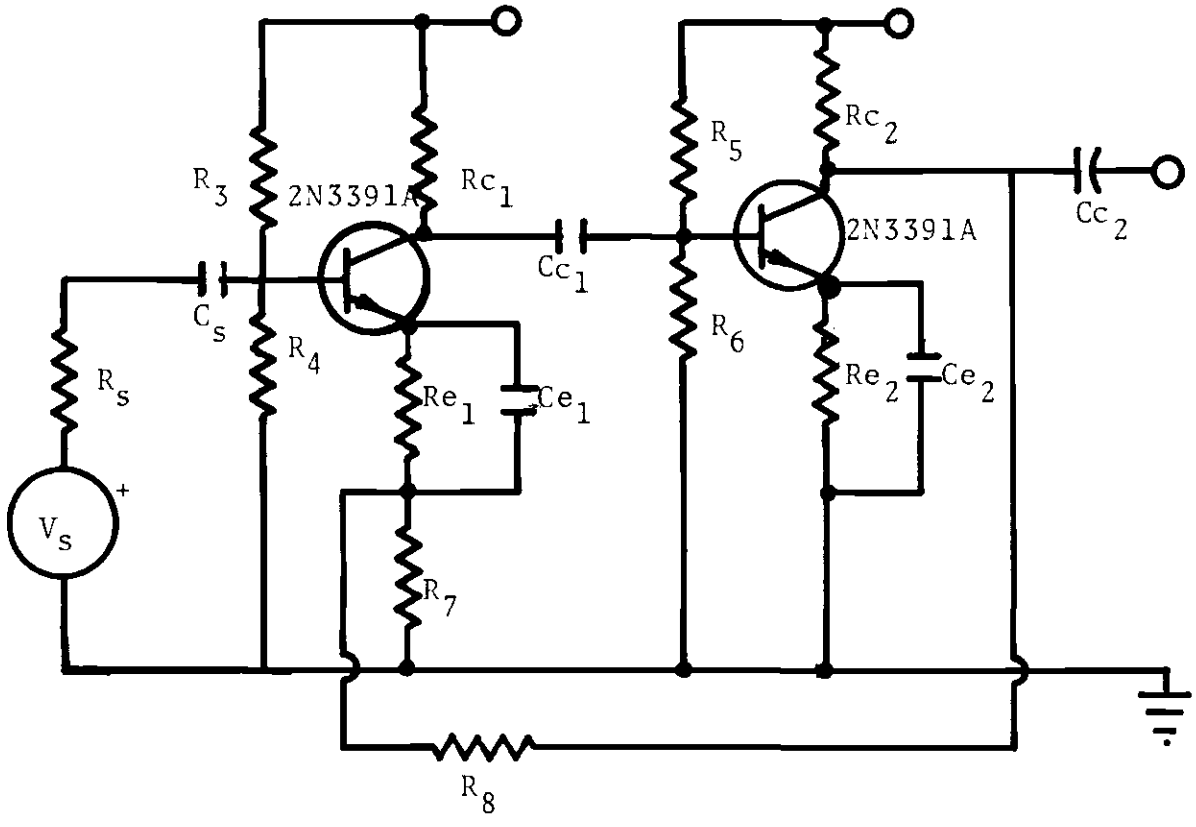

Figure 7. The Two-Stage Feedback Amplifier

$$A_v(s) = A_1(s) \times A_2(s) \tag{31}$$

where $A_1(s)$ and $A_2(s)$ are the voltage gains of the first and second stages, respectively. Now $A_1(s)$ and $A_2(s)$ are given [17] by equations (32) and (33), respectively.

$$A_1(s) = \frac{h_{fe_1} R_{o_1}}{h_{re_1} h_{fe_1} R_{o_1} - (1+h_{oe_1} R_{o_1})[(R_s+h_{ie_1})+(h_{fe_1}+1)R_f//R_7]} \tag{32}$$

$$A_2(s) = \frac{h_{fe_2} R_{o_2}}{h_{re_2} h_{fe_2} R_{o_2} - (1+h_{oe_2} R_{o_2})[R_s'+h_{ie_2}]} \tag{33}$$

R_s is the output impedance of the source follower which is equal to $.39 \times 10^3$ ohms. See Figure 8. R_s' is the output impedance of the first stage and is approximately given by

$$R_s' = \frac{1}{h_{oe_1}} // R_{o_1} \tag{34}$$

$$= 5.5 \times 10^3 \text{ ohms}$$

$$h_{oe} = 3.6 \times 10^{-5} \text{ mho}$$

$$h_{fe} = 340$$

$$h_{re} = 4.1 \times 10^{-4}$$

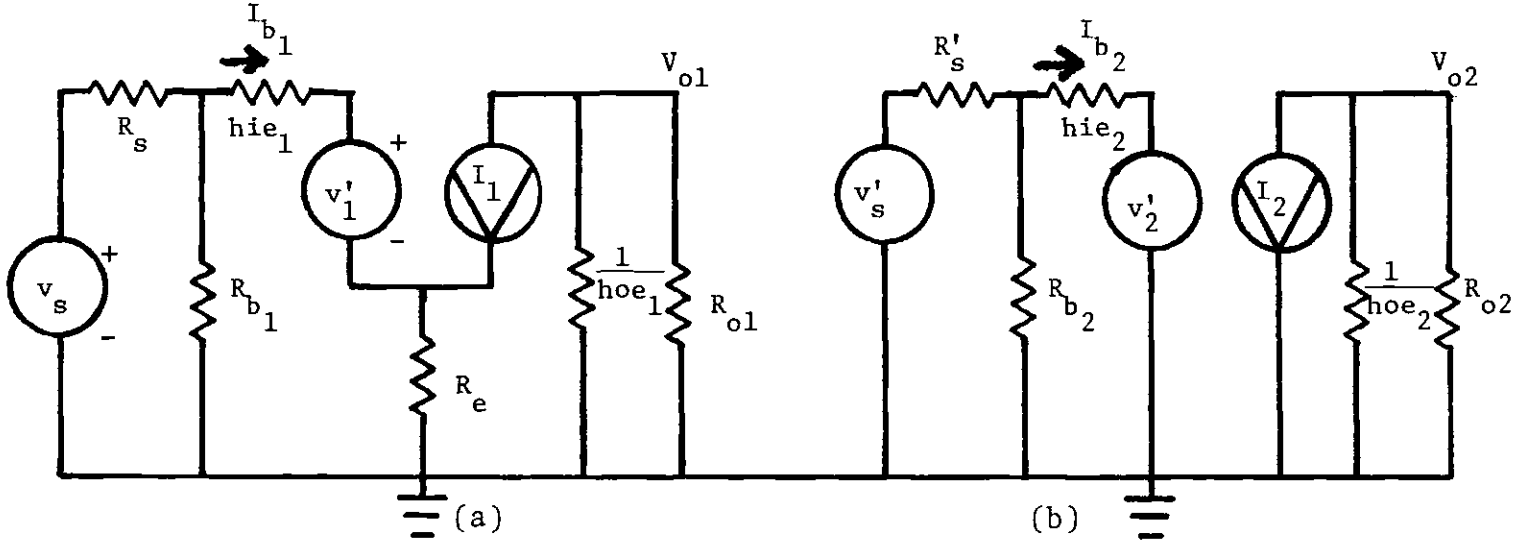

Figure 8. Mid Frequency Equivalent Circuits of the First and Second Stages, a and b

$I_1 = h_{fe_1} x I_{b_1}$, $I_2 = h_{fe_2} x I_{b_2}$; $v_1' = hre_1 v_{o1}$ $v_2' = hre_2 v_{o2}$

$R_{o1} = R_c // hie_2 // Rb_2$ $Re = R_7 // R_f$ $R_{o2} = Rc_2 // R_f // R_L$

$$h_{ie} = 4.8 \times 10^3 \text{ ohms}$$

and with

$$R_7 = 255 \text{ ohms}$$

$$R_f = 68 \times 10^3 \text{ ohms}$$

$$A_1(s) = -17$$

$$A_2(s) = -173$$

$$A_v(s) = 2941 \tag{35}$$

The Input Impedance, Z_i, the Output Impedance, Z_o, of the Two Stage Amplifier without Feedback

Referring to Figure 9, the input impedance, Z_i, of the two stage amplifier without feedback is approximately given [18] by

$$Z_i = h_{ie}//R_{b_1} \tag{36}$$

$$= 4.15 \times 10^3 \text{ ohms}$$

The output impedance, Z_o, of the two stage amplifier without feedback is approximately given [18] by

$$Z_o = \frac{1}{h_{oe_2}} //R_{o_2}$$

where

$$R_{o_2} = R_{c_2}//R_f//R_L$$

Now $R_f >> R_{c_2}$

and $R_L >> R_{c_2}$

$$Z_o \simeq \frac{1}{h_{oe_2}} //R_{c_2} \tag{37}$$

$$Z_o = 5.5 \times 10^3 \text{ ohms}$$

Voltage Gain, A_{vf}, Input Impedance, Z_{if}, and the Output Impedance, Z_{of}, of the Two Stage Amplifier with Feedback

When the feedback is applied, the voltage gain A_{vf} and input impedance, Z_{if}, and the output impedance, Z_{of}, are given [19] by equations (38, (39), and (40), respectively.

$$A_{vf} = \frac{A_v}{1 + \beta A_v} \tag{38}$$

$$Z_{if} = Z_i \ (1 + \beta A_v) \tag{39}$$

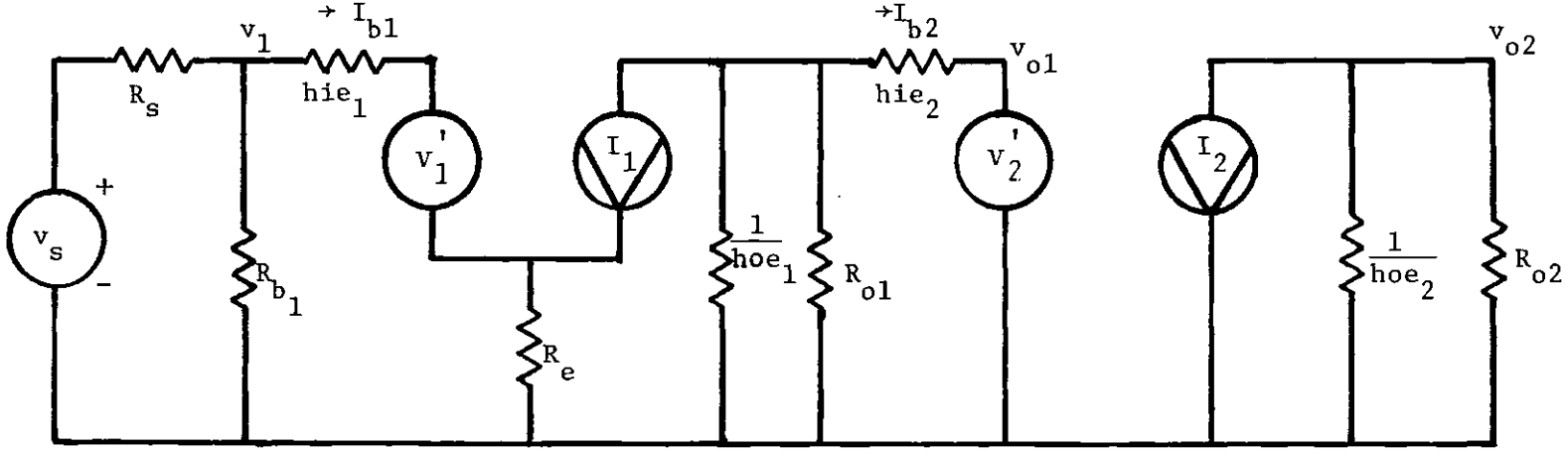

Figure 9. A.C. Equivalent for the Feedback Amplifier.

$I_1 = h_{fe_1} \times I_{b1}$ $I_2 = h_{fe_2} \times I_{b2}$ $Re = R_7//R_f$

$v'_1 = hre_1 v_{o1}$ $v'_2 = hre_2 v_{o2}$ $R_{o2} = Rc_2//R_f//R_L$

$R_{o1} = Rc_1//Rb_1$

$$Z_{of} = \frac{Z_o}{1 + \beta A_v} \tag{40}$$

where β, the feedback factor, is given by equation (41)

$$\beta = \frac{R_7}{R_7 + R_f} = \frac{1}{267} \tag{41}$$

since $R_7 = 255$ ohms and $R_f = 68 \times 10^3$ ohms

$$A_{vf} = 245$$

$$Z_{if} = 48.8 \times 10^3 \text{ ohms}$$

$$Z_{of} = 450 \text{ ohms}$$

The overall voltage gain of the amplifier (including the source follower whose measured voltage gain is 0.75)

$$A_T = 245 \times 75$$

$$= 183.75$$

The actual voltage gain measured was 180.

The Pre-Amplifier's Linearity, Dynamic Range and Frequency Response

Linearity and Dynamic Range. A 5 mV voltage signal

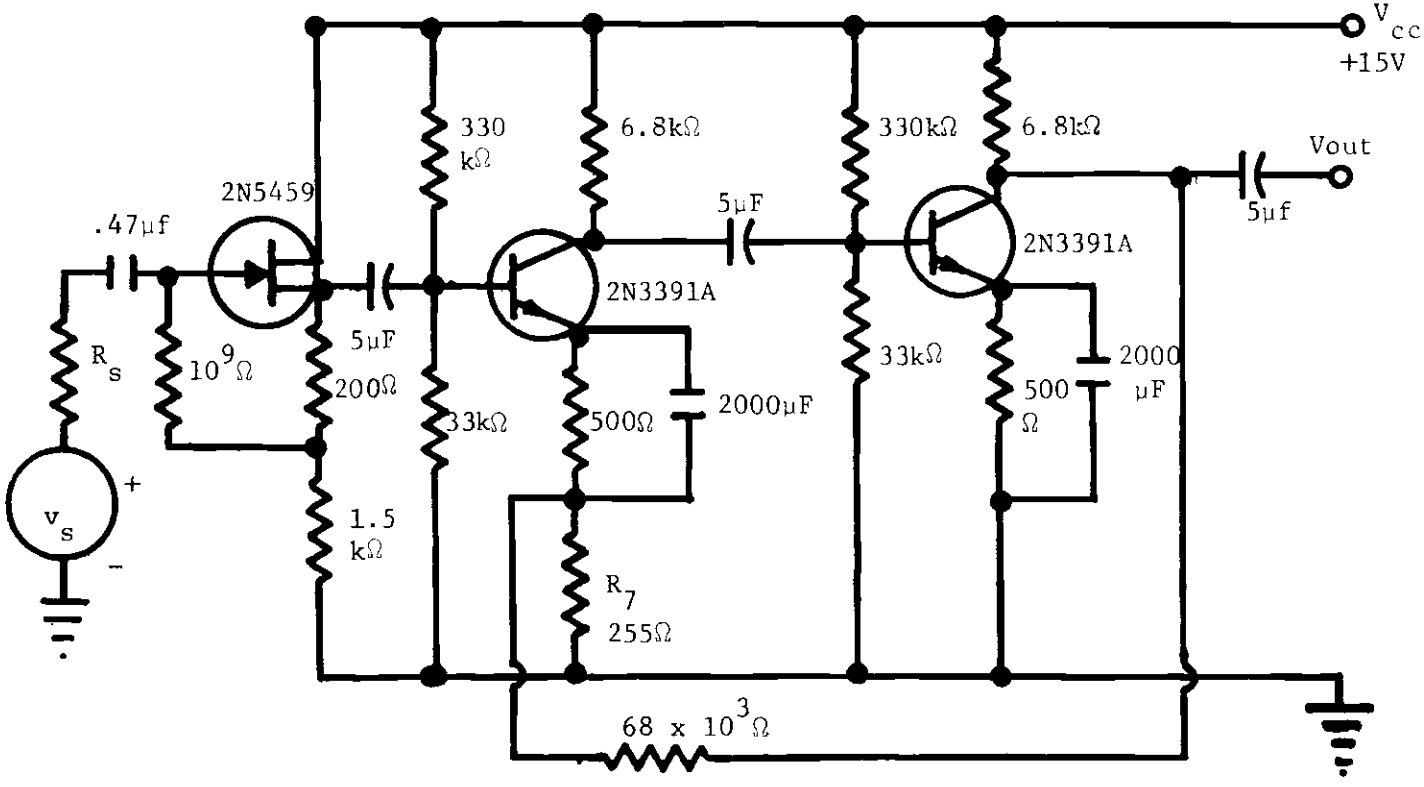

Figure 10. The Pre-Amplifier Circuit, Voltage Gain is 180 or 45 dB Input Impedance is 2000 m Ω Output Impedance is 450 Ω

at a frequency of 1000 Hz obtained from an audio signal generator was applied to the input of the pre-amplifier when loaded. Its corresponding output voltage was measured. The measurements were repeated at 5 mV increments.

The results are summarized in Table 2, and are shown graphically in Figure 11.

For input voltages above 54 mV, the output remains constant at 9.6 volts. Therefore the dynamic range of the amplifier is 54 mV. For inputs less than the dynamic range, the amplifier functions properly for all frequencies within the audio frequency spectrum.

Frequency Response

The gain, A, of the pre-amplifier is defined by equation (42),

$$A = 20 \text{ dB } \log_{10} \frac{V_{in}}{V_f} \qquad (42)$$

V_{in} is the input voltage obtainable from an audio signal generator, and V_f is the output voltage at frequency, f. With V_{in} set at 10 mV, V_f was measured for the various frequencies ranging from 10 Hz to 180,000 Hz. Using equation (42), the gain of the pre-amplifier was calculated for the respective frequencies f. The results are shown graphically in Figure 12.

The frequency response curve shows that the

Table 2. Input-Output Voltage Relationship of the Pre-Amplifier

V_{in} m Volts	V_{out} Volts
5	.9
10	1.8
15	2.7
20	3.6
25	4.5
30	5.4
40	7.2
45	8.1
50	9.0
52	9.4
55	9.6
60	9.6
65	9.6

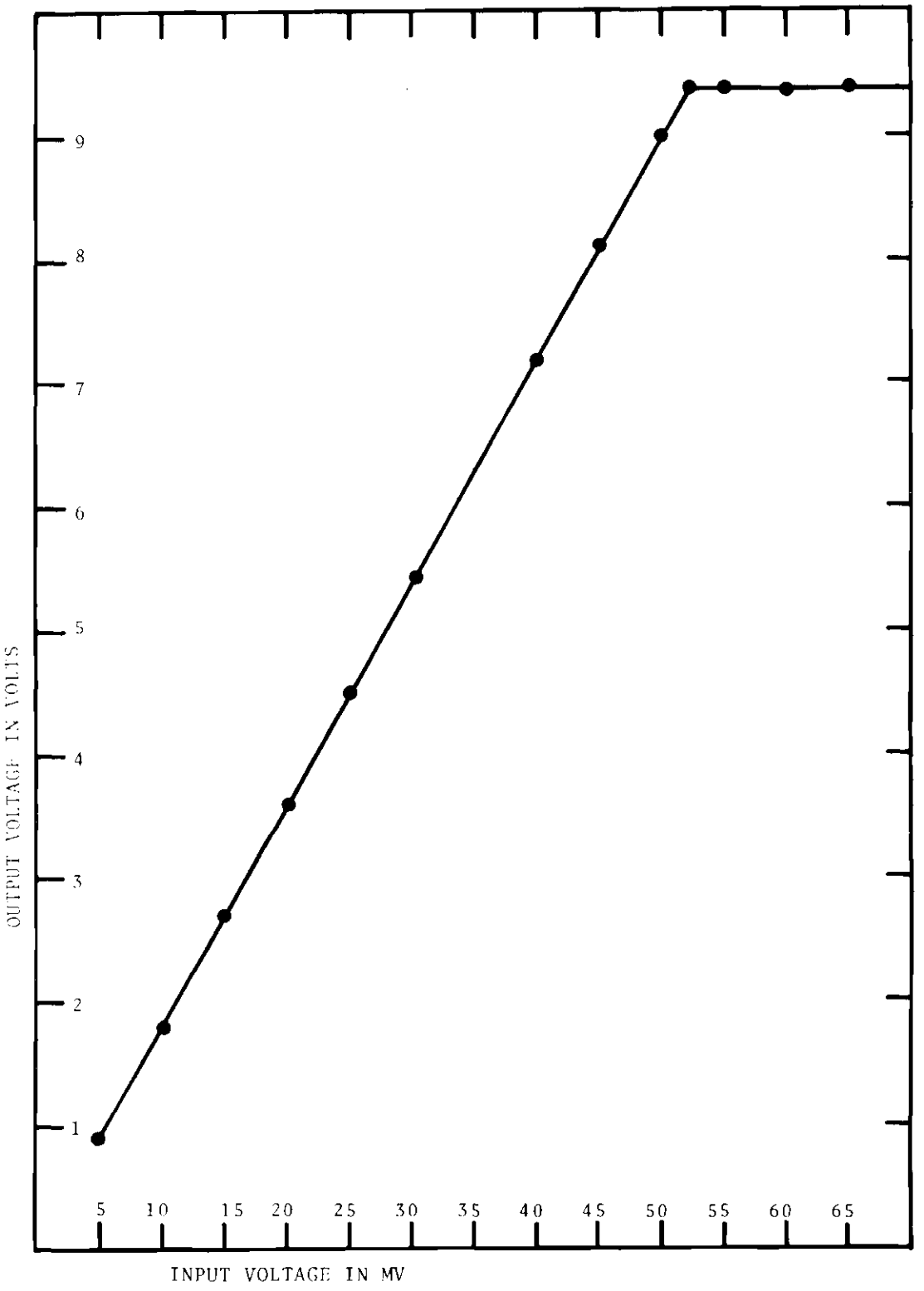

Figure 11. Input-Output Characteristics of the Pre-Amplifier

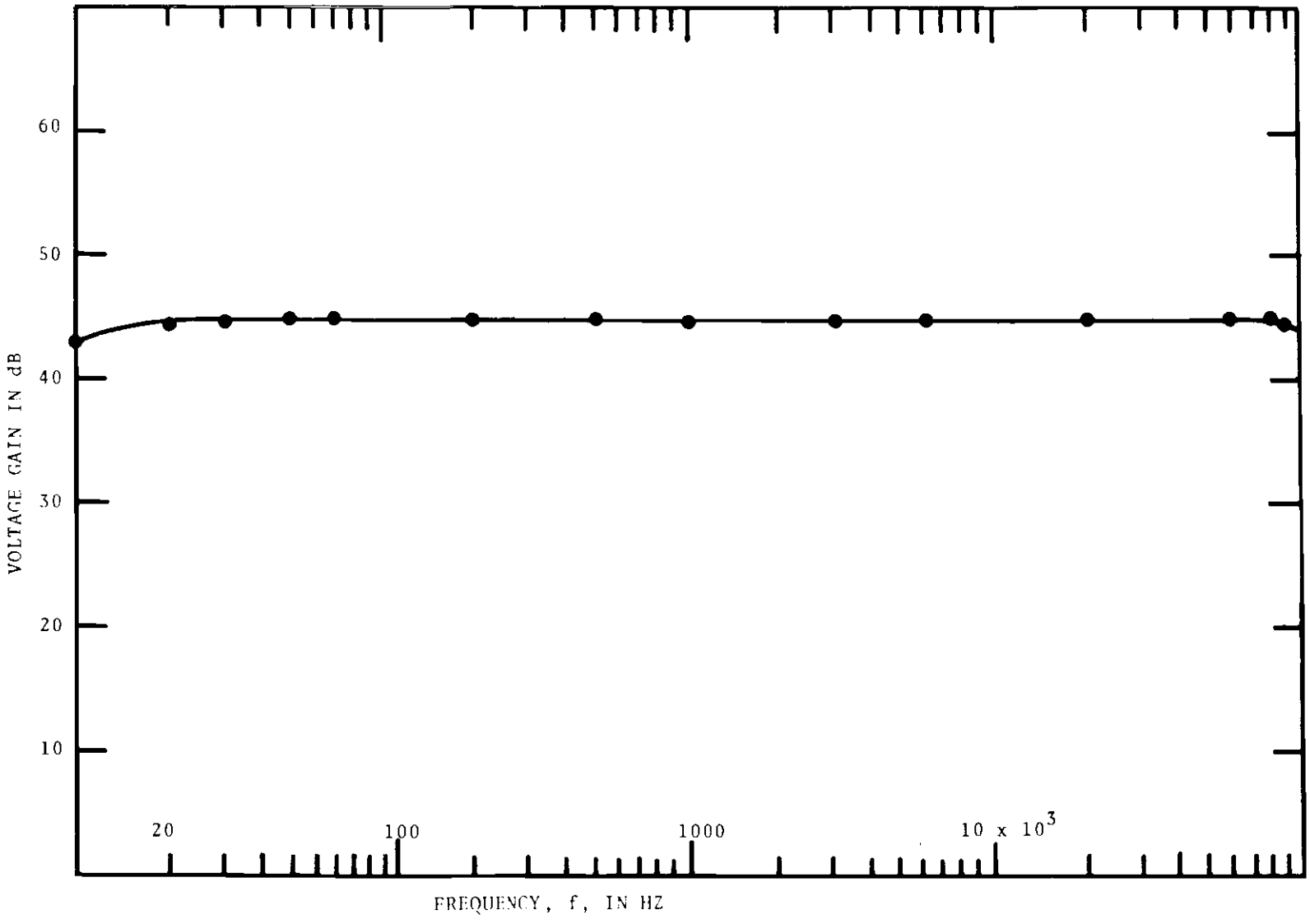

Figure 12. Frequency Response of the Pre-Amplifier

pre-amplifier has a completely flat response from about 20 Hz to 80,000 Hz. The -3 dB low and high frequency break points (not shown on graph) occur at 8 Hz and 180 x 10^3 Hz respectively.

2. Design of the Frequency Weighting Networks

Introduction

In 1933 H. Fletcher and W. A. Munson [20] drew the so-called Equal Loudness Contours by measuring the sound pressure levels of simple tones of various frequencies that sound just as loud to an observer as a 1000 Hz tone of a given sound pressure level. The shapes of the contours show that sounds at low and at very high frequencies in the audible frequency spectrum have to be higher in level than those at frequencies around 1000 Hz to 2000 Hz in order to be judged equally loud. A sound level meter therefore will need to reflect the frequency sensitivity of the ear. That is, the lower and the very high frequency components of the sound will have to be attenuated before they are added up to the mid-frequency components to obtain the overall sound intensity or sound pressure level. The resulting overall sound pressure level would be a "weighted" level.

So in 1961 the United States Standards Institute in collaboration with scientific and engineering societies throughout the world established three weighting networks characteristics which approximate the 40, 70 and 90 phon Fletcher-Munson frequency contours [21]. These networks are

designated A, B, C.

The A network is for weighting sound pressure levels up to 55 dB, B network is for weighting sound pressure levels between 55 dB and 85 dB and C network for levels above 85 dB.

The theoretical relative frequency responses of the A, B, C networks are shown [22] in Figure 13. The following designs for the A, B, C weighting networks meet the requirements. The optional flat response network, the F network, is added.

Design of the C Weighting Network

The C network is obtained* by a network designed to have its lower -3 dB point with respect to the 1000 Hz response at 31.62 Hz and to approach a roll off of 12 dB per octave below 10 dB. The high frequency -3 dB point is at 7942 Hz and approaches a roll off of at least 12 dB per octave above 20,000 Hz.

The requirements for this circuit can be met by cascading two differentiating circuits as shown in Figure 14.

The transfer function A(s) for the circuit is given** by

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*American National Standard S1.4-1971.

**See Appendix B.

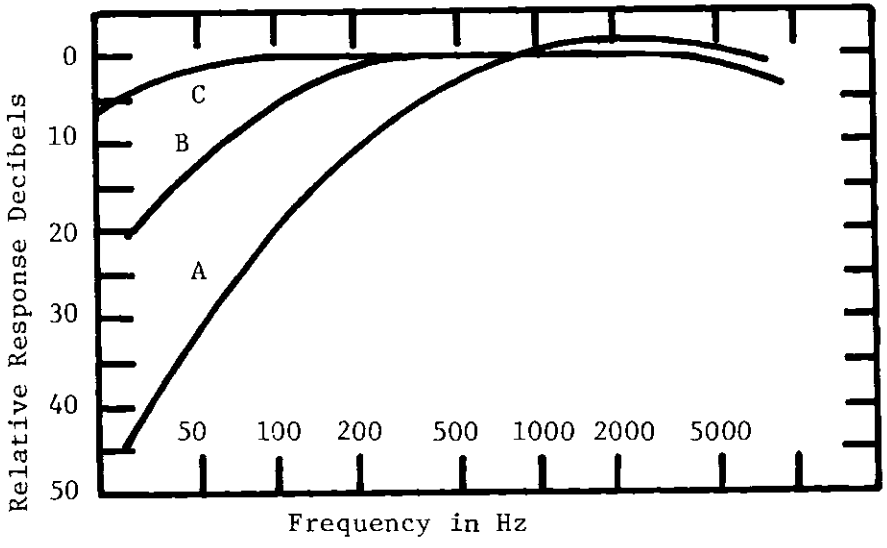

Figure 13. Theoretical Relative Frequency Response of the A, B, C Weighting Networks. General Radio Co. Handbook of Noise Measurement (1967).

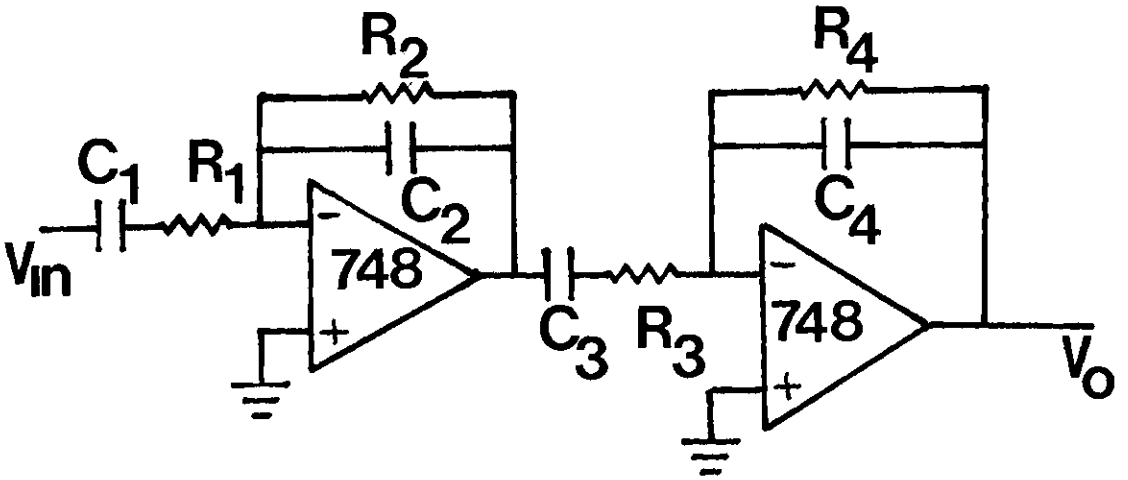

Figure 14. The C Network

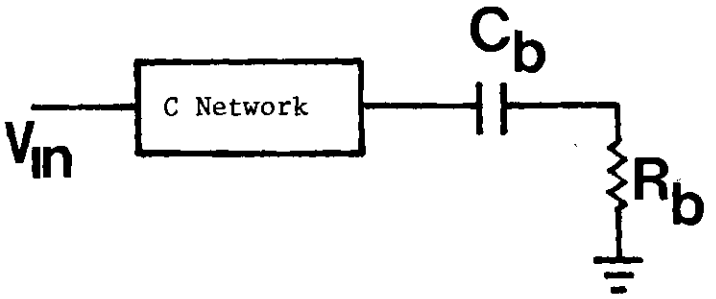

Figure 15. The B Network

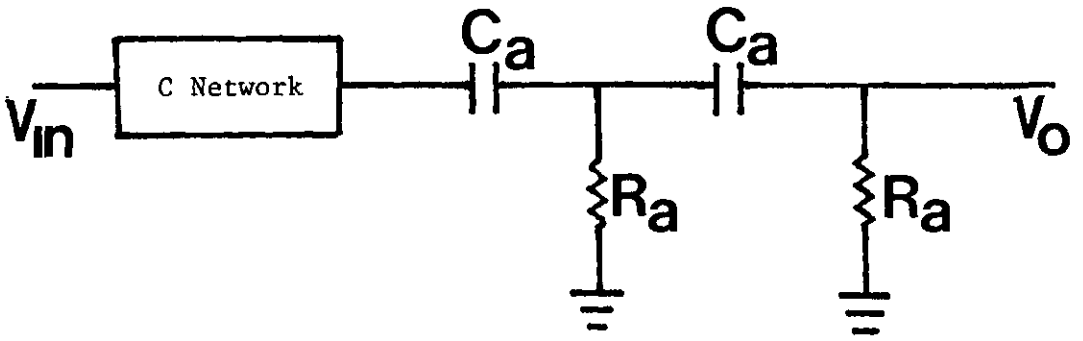

Figure 16. The A Network

$$A(s) = \frac{S^2}{R_1R_3C_2C_4(S + \frac{1}{R_1C_1})(S + \frac{1}{R_2C_2})(S + \frac{1}{R_3C_3})(S + \frac{1}{R_4C_4})} \quad (43)$$

If R_1, C_1 control the lower frequency -3 dB break point at 10 Hz, R_3, C_3 control the low -3 dB break point at 31.62 Hz, R_2, C_2 control the higher high frequency -3 dB break point at 20,000 Hz and R_4, C_4 control the high frequency -3 dB break point at 7942 Hz. Then

$$10 \text{ Hz} = \frac{1}{2\pi R_1C_1}$$

$$31.62 \text{ Hz} = \frac{1}{2\pi R_3C_3} \quad (44)$$

$$7942 \text{ Hz} = \frac{1}{2\pi R_4C_4}$$

$$20 \text{ kHz} = \frac{1}{2\pi R_2C_2}$$

R_1, R_3 were chosen to be 1000 ohms each; R_3, R_4 were chosen to be 1500 ohms each. Then

$C_1 = 15\mu F$, $C_4 = .01\mu F$ and

$C_3 = 7\mu F$

$C_2 = 4000$ pF

Design of B Network

The B weighting is obtained* by adding a network with a response that has the performance characteristics equivalent to a simple resistor-capacitor network. The R-C network is cascaded with and isolated from the C network as shown in Figure 15. The -3 dB point for the added network is 158.48 Hz

Therefore

$$\frac{1}{2\pi R_b C_b} = 154.48 \text{ Hz}$$

Choosing $C_b = .36\ \mu F$

then $R_b = 2.2 \times 10^3$ ohms.

It is noted that the low output impedance of the C network will provide an isolation between the C and the R-C networks.

Design of the A Network

The A weighting is obtained* by adding a network with a response that has the performance characteristics equivalent to two cascaded identical nonisolated resistor-capacitor networks, these are cascaded with and isolated from the C network. See Figure 16.

The -3 dB point for each of the identical added networks is at 281.84 Hz.

---

*See page 41.

Therefore,

$$\frac{1}{2\pi R_a C_a} = 281.84 \text{ Hz.}$$

If R_a is chosen to be 4.4×10^3 ohms, then

$$C_a \approx 0.11 \ \mu F$$

The F Frequency Response Network

The requirements for the F network are

(a) Low -3 dB point should occur at 20 Hz or lower

(b) High -3 dB point should fall at 20 kHz at least.

The F network is shown in Figure 17.

R_f, C_f, control the low frequency break point. A capacitor placed parallel to R_2 should control the high frequency -3 dB break point. Its omission implies that the upper frequency -3 dB point should fall at infinity. It will, however, be limited by circuit internal and stray capacitances of the order of 2 pF.

To calculate R_f, C_f, the transfer function is first computed. It is given [23] by

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = - \frac{Z_{out}}{Z_{in}} \qquad (45)$$

where $Z_{out} = R_2$ is the impedance in the feedback loop, and Z_{in} the input impedance.

$$Z_{in} = R_f + \frac{1}{SC_f}$$

$$A(s) = - \frac{R_2}{R_f + \frac{1}{SC_f}} = - \frac{S(R_2/R_f)}{S + \frac{1}{R_f C_f}}$$

$$A(s) = + \frac{A_o S}{S + \frac{1}{R_f C_f}} \tag{46}$$

$$A_o = - \frac{R_2}{R_f} \tag{47}$$

The low frequency -3 dB break point, f_L, is determined by the pole $f_L = \frac{1}{2\pi R_f C_f}$

If (48)

$$R_f = 5.1 \times 10^3 \text{ ohm}$$

then $C_f = 5\ \mu F$

for $f_L = 5$ Hz.

The value of R_2 was experimentally chosen such that at 1000 Hz the F network has a gain which is equal to that of the A, B and C network at 1000 Hz. R_2 was found to be $51X10^3$ ohms.

A. C. Amplifiers for A, B, and C Networks

Amplifiers following the weighting networks were needed to raise the level of the noise signal. The amplifier circuit diagram is shown in Figure 18.

The determining factors for choosing the components R_1, C_1, R_o are

(a) The low frequency break point should be chosen low such that it does not interfere with the frequency responses of the A, B, C networks at the low frequency end.

(b) At the reference frequency of 1000 Hz, the output voltage V_o should be the same for the A, B, C, F networks.

Calculations for R_1, C_1, R_o

The voltage gain A(s) can be expressed as*

$$A(s) = - \frac{SR_o/R_1}{(S + \frac{1}{R_1C_1})} \qquad (49)$$

where R_o/R_1 is the midband gain of the amplifier; and the low frequency -3 dB break point occurs at $f_L = \frac{1}{2\pi R_1C_1}$

*See equation 45.

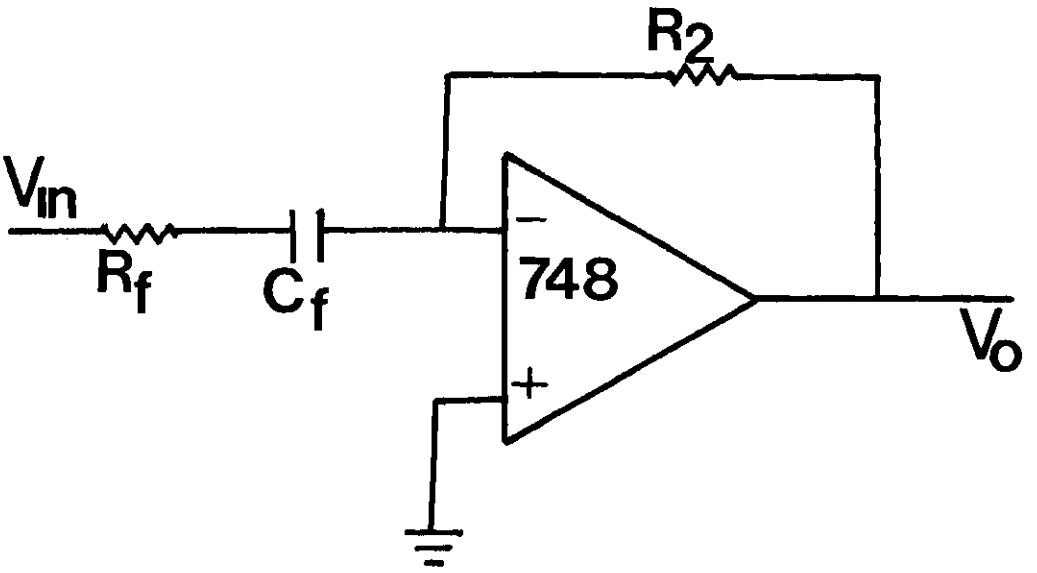

Figure 17. The F Network

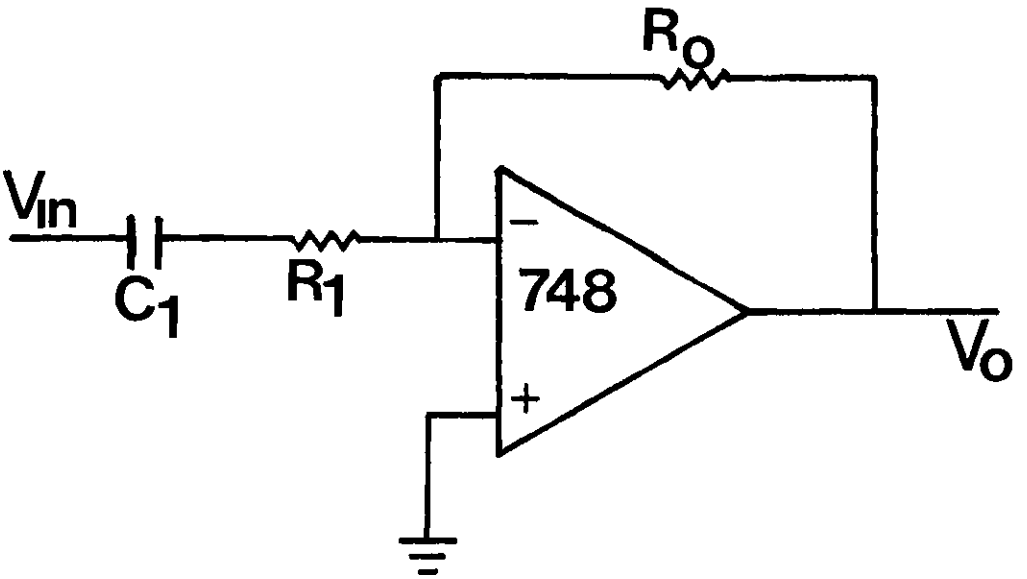

Figure 18. A.C. Amplifier Circuit. R_o Values for A,B,C Networks are 57kΩ, 47kΩ and 47kΩ respectively

with $R_1 = 5.1 \times 10^3$ ohms.

$C_1 = 5\mu F$

$f_L \approx 5$ Hz

R_o for each of the frequency response networks was chosen experimentally so that the requirement (b) stated above is satisfied.

The Relative Frequency Responses of the A, B, C and F Weighting Networks

The relative gain, A_{rel}, is defined by equation (50)

$$A_{rel} = 20 \text{ dB } \log_{10} \frac{A_f}{A_{1000}} \tag{50}$$

where A_f is the gain of the network at frequency f; A_{1000} is the gain at 1000 Hz.

Now

$$A_f = \frac{V_f}{V_{in}} \tag{51}$$

$$A_{1000} = \frac{V_{1000}}{V_{in}} \tag{52}$$

V_{1000} and V_f are respectively the output voltages at 1000 Hz and at frequency f when the input voltage is V_{in}.

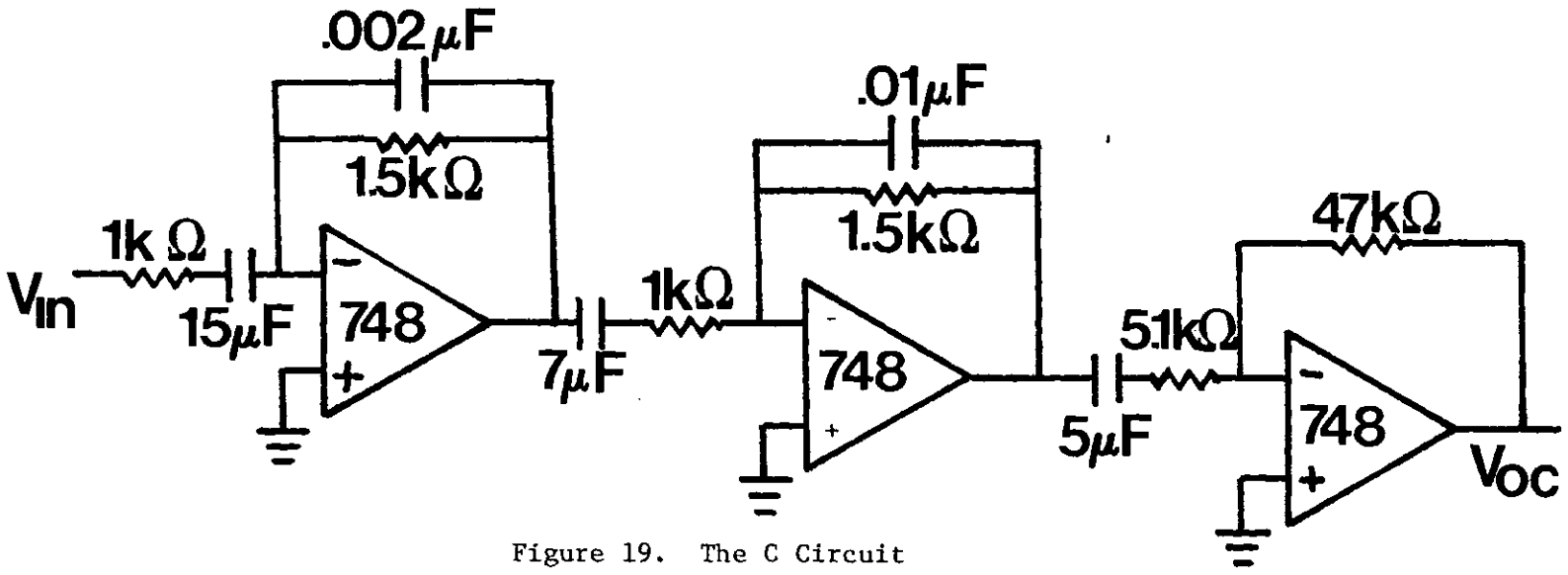

Figure 19. The C Circuit

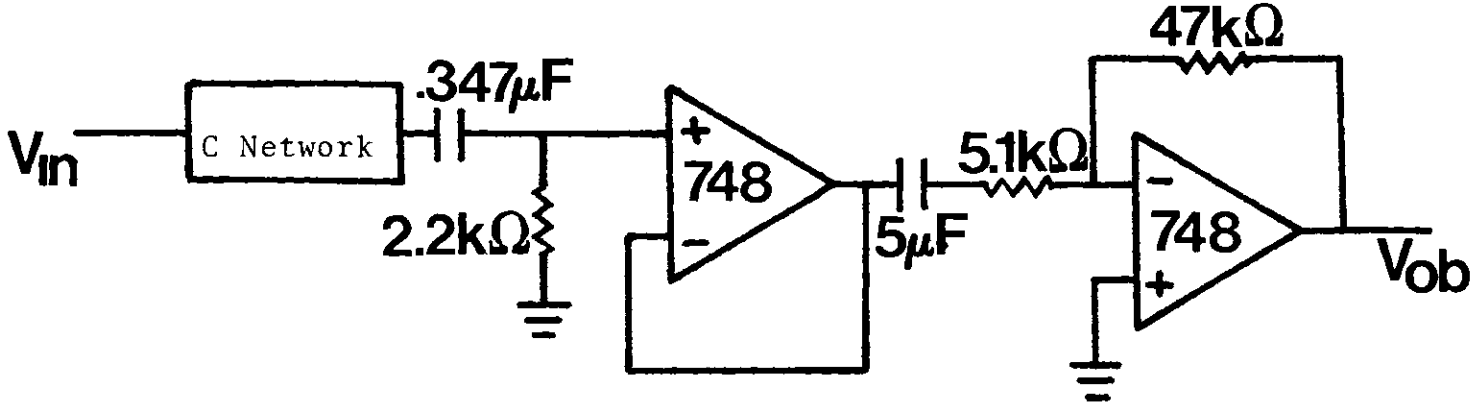

Figure 20. The B Circuit. The voltage follower isolates the B and the amplifier circuits.

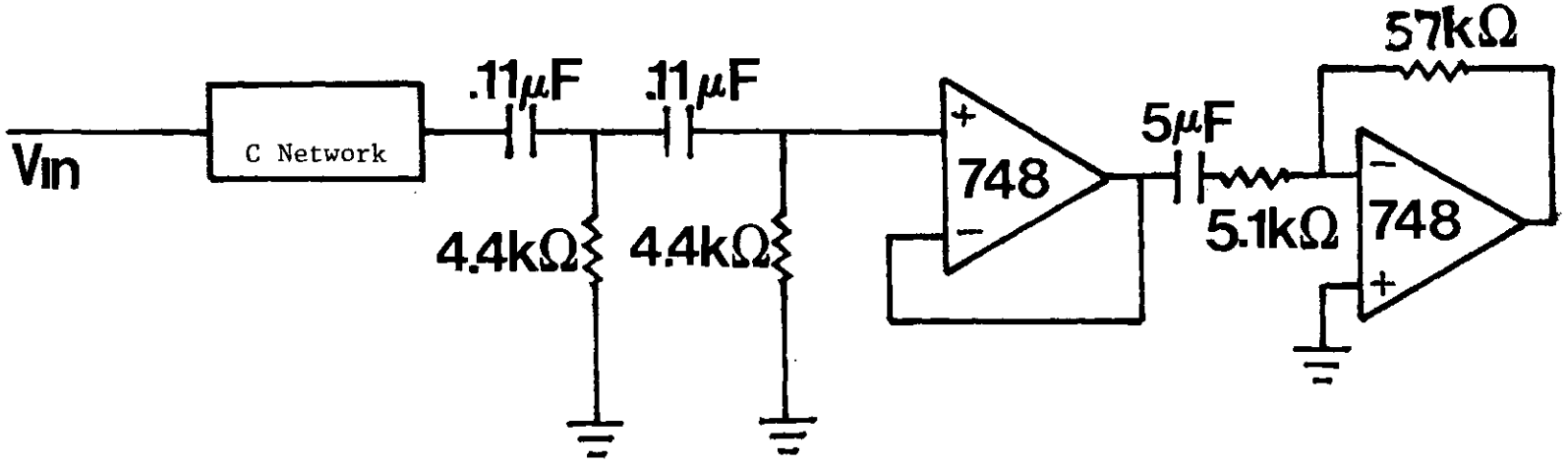

Figure 21. The A Circuit .

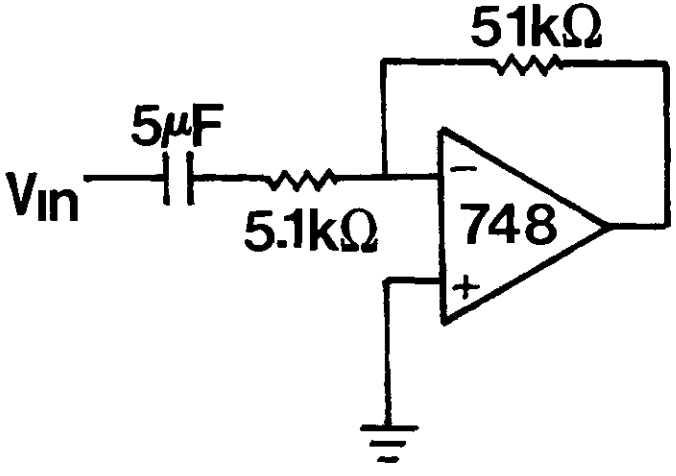

Figure 22. The F Network

From equations (50), (51), and (52) the relative gain can be defined as

$$A_{rel} = 20 \text{ dB } \log_{10} \frac{V_f}{V_{1000}} \tag{53}$$

With the input signal set at 10 mV, V_f for frequencies ranging from 10 Hz to 25,000 Hz were measured for the C network. V_{1000} was also measured. The measurements were repeated for A, B, and F networks. The relative gains for the networks were calculated. Tables 5, 6 and 7 summarize the results. Figure 23 graphically shows the relative frequency responses of the Weighting Networks.

Comparing Figures 13 and 23 it is seen that the theoretical and experimental frequency responses of the A, B and C networks are approximately the same. The closeness of the theoretical and experimental curves are summarized in Table 4.

The slight variations in the low and high -3 dB points are due to the tolerances associated with the resistors and capacitors used to build the circuits.

The F network is completely flat from 13 Hz to 22,000 Hz. Its low and high -3 dB points fall respectively at 10 Hz and 34,000 Hz.

Table3 . Relative Frequency Response of the C Network

Frequency, f, in Hz	Gain in dB with respect to 1000Hz
10	-14
16	-7.7
20	-6.2
31.5	-3.3
50	-1.94
100	-0.5
160	-0.1
200	0
250	0
315	0
400	0
630	0
800	0
1000	0
1250	0
1600	-0.1
2000	-0.2
2500	-0.3
3150	-0.5
4000	-0.85
5000	-1.3
6300	-2.0
8000	-3.0
10000	-4.4
12500	-6.1
16000	-8.5
20000	-11.2

Table 4. Relative Frequency Response of the B Network

Frequency, f, in Hz	Gain in dB with respect to 1000 Hz
10	-37.7
16	-27.6
20	-24.0
31.5	-17.2
50	-12.1
100	-5.8
160	-3.0
200	-2.0
250	-1.4
315	-0.8
400	-0.45
630	-1.04
800	0
1000	0
1250	0
1600	0
2000	-0.1
2500	-0.2
3150	-0.35
4000	-0.8
5000	-1.4
6300	-2.0
8000	-2.9
10000	-4.3
12500	-5.8
16000	-7.9
20000	-11.05

Table 5. Relative Frequency Response of the A Network

Frequency, f, in Hz	Gain in dB with respect to 1000 Hz
100	-19.2
125	-16.6
160	-13.6
200	-11.05
250	-8.8
315	-6.61
400	-4.8
500	-3.2
630	-2.05
800	-.82
1000	0
1250	0.6
1600	1.06
2000	1.21
3150	1.36
4000	1.21
5000	1.06
6300	0.51
8000	0.1
10000	-1.2
12500	-2.7
16000	-4.4
20000	-6.0

Table 6. Relative Frequency Response of the Flat (F) Network.

Frequency, f, in Hz	Gain in dB with respect to 1000 Hz
10	-3
12	-2
13	0
20	0
50	0
100	0
200	0
400	0
800	0
1000	0
2000	0
4000	0
8000	0
16000	0
20000	0
22000	0
30000	-1
34000	-3

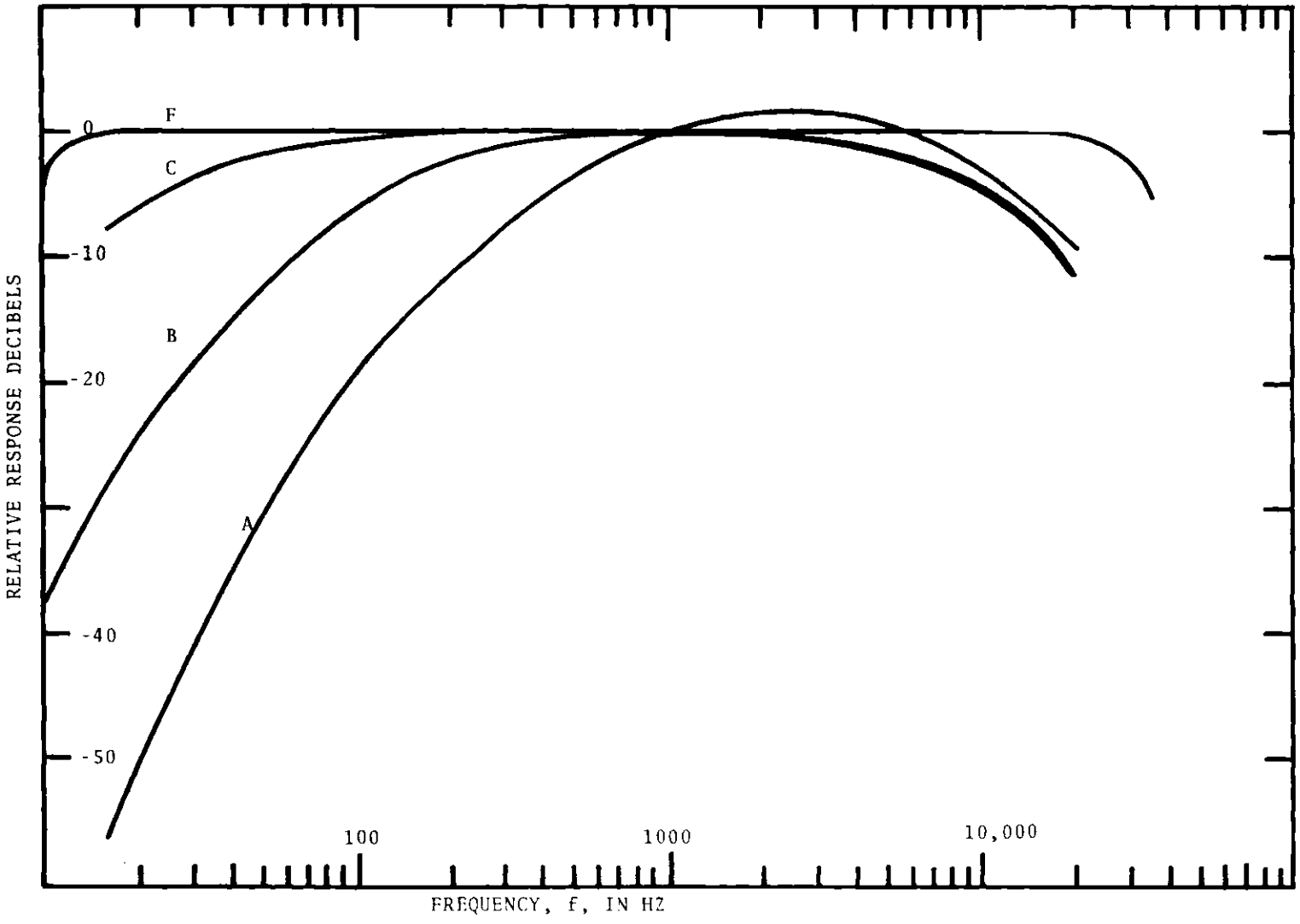

Figure 23. The Experimental Relative Frequency Responses of A, B, C and F Weighting Networks.

Table 7. Theoretical and Experimental Low and High -3 dB Points f_L, f_H in Hz

Theoretical		Experimental		Weighting Network
f_L	f_H	f_L	f_H	
31.5	7942	33	7900 ± 50	C
158.49	7942	160	7900 ± 50	B
563.68	10,300	552	10,200 ± 50	A

3. Root Mean Square (RMS) Circuit

The block diagram of the root mean square (rms) circuit is shown in Figure 26.

The Squarer

The squarer as shown in Figure 24 is a single integrated circuit RCA 3091D [24] multiplier, the output v_o of which is proportional to the square of the v_x and the v_y inputs, i.e.

$$v_o = kv_x v_y \tag{54}$$

where k is the scaling factor. Since in practical applications of the multiplier, slight current imbalances exist, RCA suggests the use of external potentiometers to null the imbalances. It is also recommended that the scaling factor, k, be made equal to $\frac{1}{10}$ for optimum accuracy.

The RCA 3091D together with its peripheral circuitry is shown in Figure 24. Prior to the use of the multiplier, the Y-balance, the X-balance, the Zero-adjust and the

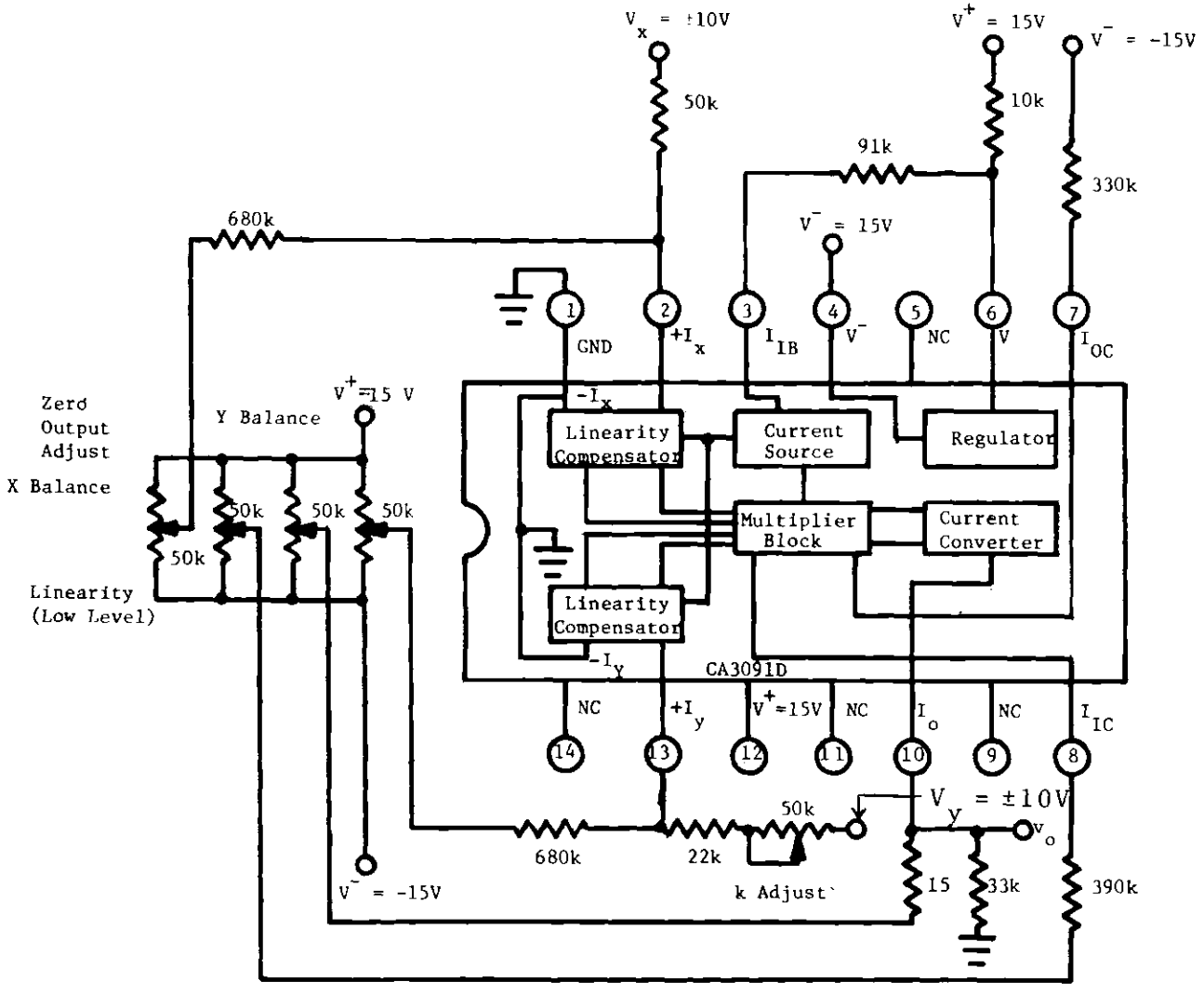

Figure 24. Functional Block Diagram of CA3091D with Typical Multiplier Outboard (Peripheral) Circuitry.

linearity potentiometers are adjusted according to the manufacturers specifications, such that for zero input the output is also zero.

To square the input signal, the v_x, v_y input terminals are connected together and the input signal is applied to the junction. The k-adjust potentiometer is then adjusted such that the output is equal to 2.5 V when the input is 5 V.

The maximum input voltage that can be applied to the multiplier circuit is 10 V. However, the maximum output voltage that each of the weighting networks can deliver to the multiplier is 9.8 V. Thus the multiplier's maximum rating for the input voltage cannot be exceeded.

The Averaging Circuit

The averaging circuit is shown in Figure 25. It is noted that the output of the squarer is a current source.

The current I_1 as shown in Figure 25 charges the capacitor, which has capacitance C, to a peak voltage v_2 as shown in Figure 26. Hence

$$v_2 = I_2R = \frac{1}{C} \int I_1 dt$$

$$= \frac{1}{C} \int I_o dt - \frac{1}{C} \int I_2 dt$$

since the driving current I_o is the sum of the currents I_1 and I_2.

$$\therefore \quad I_2 + \frac{1}{RC} \int I_2 dt = \frac{1}{RC} \int I_o dt \tag{55}$$

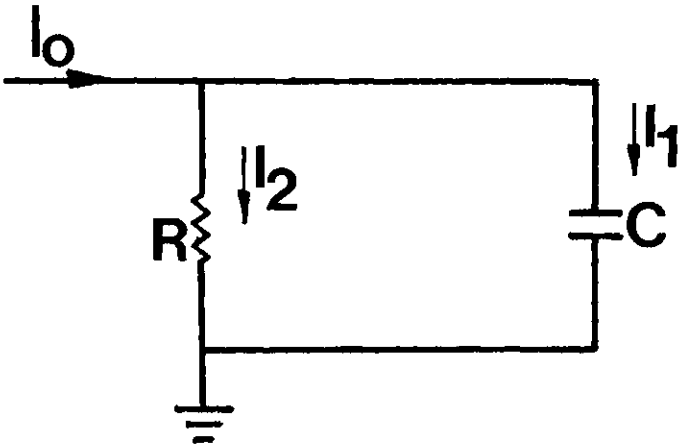

Figure 25. The Averaging Circuit

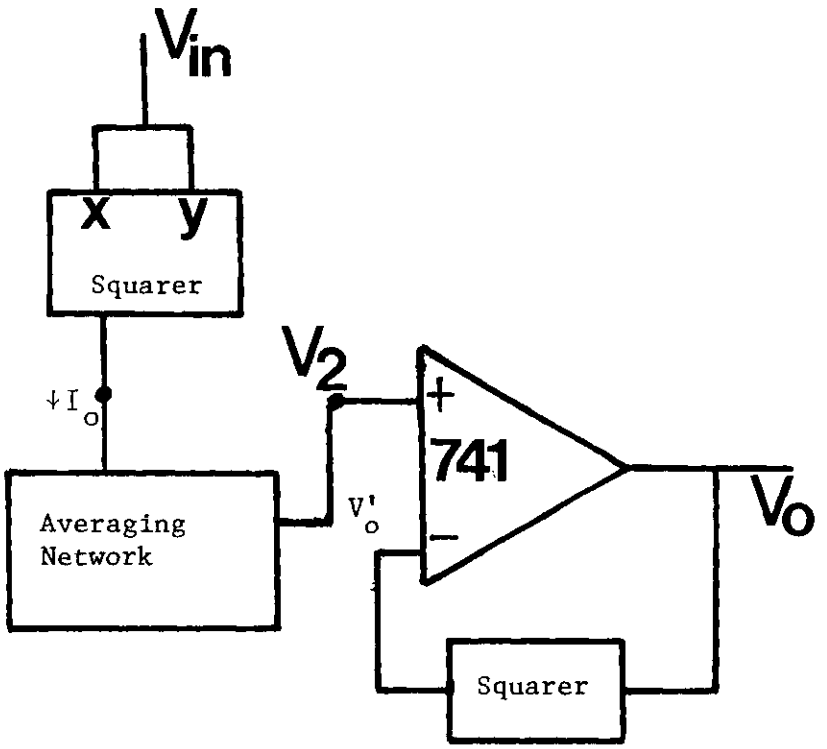

Figure 26. Block Diagram of the rms Circuit

If RC is large compared with the maximum period of the input signal, then the second term of the left hand side expression in equation (55) is small compared with I_2. Therefore

$$I_2 = \frac{1}{RC} \int I_o dt$$

Hence v_2 is proportional to the average value of the driving current

i.e. $$v_2 \propto \bar{I}_o$$

But $$I_o = kv_{in}^2$$

where k is the scaling factor.

Therefore v_2 is proportional to the average of the square of the input.

i.e. $$v_2 = k'\bar{v}_{in}^2$$

where k' is some normalization factor. The k-adjust potentiometer was adjusted such that k' = .1.

R, and C values were chosen to be 33×10^3 ohms and 15 μF respectively. Thus RC = 495 msec.
Since the minimum frequency of the signal is 20 Hz; the maximum period of the signal is 50 msec which is about a tenth of the time constant of the averaging circuit.

To obtain the square root of v_2, the squarer

is placed in the feedback loop of the 741 integrated circuit operational amplifier as shown in Figure 26.

v_o is the output voltage of the rms circuit. It is also the input to the squarer. Hence

$$v_o' = kv_o^2 \tag{56}$$

where k is the scaling factor which was normalized to 0.1. From the 741 operational amplifier,

$$v_o = A(v_2 - v_o')$$

where A is the open loop gain of the operational amplifier and v_2, v_o' are the non-inverting and the inverting inputs to the operational amplifier. Usually A is large. Hence as

$$A \to \infty, \quad v_2 = v_o'$$

Therefore from equation (56)

$$v_o = \sqrt{\frac{v_2}{k}} \tag{57}$$

So it is seen that the output v_o is proportional to the square root of the input v_2.

But $$v_2 = \overline{kv_{in}^2}$$

Since k and k' have the same numerical value, then

$$v_o = \sqrt{\overline{v_{in}^2}} \tag{58}$$

Thus the output voltage v_o is equal to the root-mean-square of the input voltage.

The Comparator Circuit

The comparator circuit is shown in Figure 27. It compares the rms value of the amplified noise signal with a reference voltage v_b. For the four channel noise dosimeter, four comparators are needed. The four reference voltages are respectively equal to the voltage equivalent of sound pressure levels of 85, 90, 95 and 100 dB as each appears at the negative input terminals of the comparators. The experimental determination of each reference voltage is discussed in a later section.

Transfer Characteristics of the Comparator

The voltage v_b is a superposition of v and v_o

$$v_b = \left(\frac{R_1}{R_1+R_2}\right)v + \left(\frac{R_2}{R_1+R_2}\right)v_o$$

$$= (1-\beta)v + \beta v_o$$

where $$\beta = \frac{R_2}{R_1+R_2}$$

is the feedback factor. The voltage v_o is determined by the inputs to the comparator as follows.

$$v_o = v(o) \text{ for } v_{in} > v_b$$

$$v_o = v(1) \text{ for } v_{in} < v_b$$

where v(o) is the logical zero output level and v(1) is the logical 1 output level. v(o) and v(1) for a 710 integrated circuit comparator are -0.5 V and 3.1 V respectively.

Thus when $v_{in} > v_b$

$$v_b' = (1-\beta)v + \beta v(o) \tag{59}$$

$$v_o = v(o) \text{ for } v_{in} > v_b$$

$$v_o = v(1) \text{ for } v_{in} < v_b$$

and when $v_{in} < v_b$

$$v_b'' = (1-\beta)v + \beta v(1) \tag{60}$$

$$v_h = v_b'' - v_b' = \beta[v(1)-v(o)] \tag{61}$$

The operation of the comparator introduces hysteresis into the transfer function of the comparator, but to an advantage which is the inherent self latching action of the hysteresis loop. Since the down and up switching levels are separated, the circuit has a built-in noise immunity equal to the width v_h (see Figure 28) of the hysteresis loop. Once the comparator registers an output, small perturbations will not cause reswitching and consequent erratic indications. However,

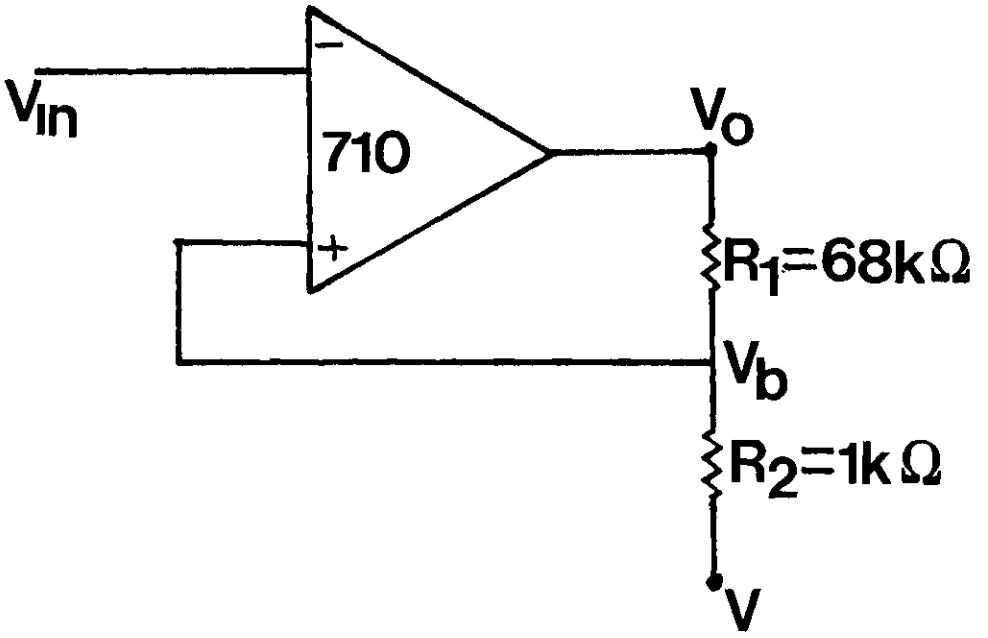

Figure 27. The Comparator Circuit

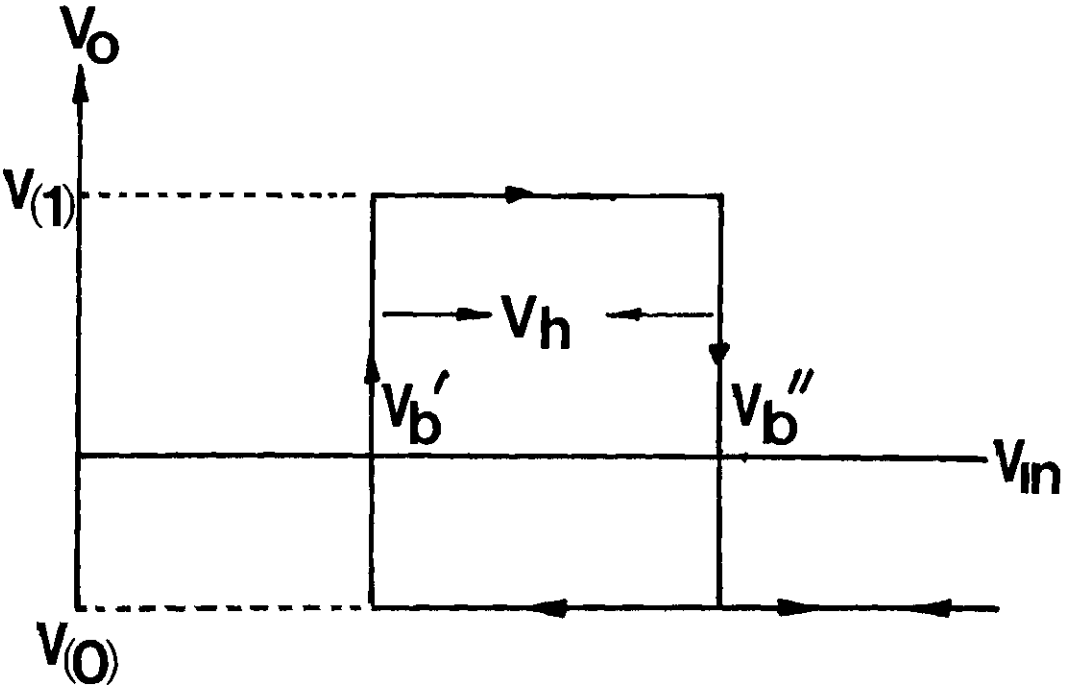

Figure 28. Transfer Characteristics of the Comparator

the input transition zone is broadened, hence a single voltage comparator level cannot be narrowly defined. But if the feedback factor β is chosen as small as possible, the width of the hysteresis loop can be decreased. For this design,

$$R_2 = 10^3 \text{ ohms}$$

$$R_1 = 68 \times 10^3 \text{ ohms}$$

then $$\beta = \frac{1}{69}$$

and the up and down switching levels were observed to be separated by approximately 1 dB sound pressure level.

The Inverter Circuit

Since the comparator is functioning in the inverting mode, the inverter stage, as shown in Figure 29, was added to it, so that

$$v_o = v_{cc} \quad \text{whenever} \quad v_{in} = v(o) = 0 \text{ V}$$

$$= 0 \quad \text{whenever} \quad v_{in} = v(1) = 3.1 \text{ V}$$

where v(1) and v(o) are respectively the high and low output levels of the comparator.

In the active or saturation region, the base-emitter

diode conducts and the base current, I, is given by

$$I = \frac{v_{in} - v_{BE}}{R} > 0 \qquad (62)$$

Assuming piecewise-linear approximation for the transfer function of the circuit v_{BE}, the base-emitter voltage, is constant and equal to 0.6 volt for the silicon transistor 2N2924.

Therefore when

$$v_{in} < 0.6 \text{ V}$$

the transistor is cut off and the output voltage, v_o, is equal to the supply voltage, v_{cc}. For $v_{in} > 0.6$V the base current increases linearly with v_{in}. The output voltage decreases from the cut-off voltage v_{cc} as

$$v_o = v_{cc} - I_c R_c$$

$$= v_{cc} - \beta I R_c$$

where $I_c = \beta I$. β is the current gain which is equal to 60 for the 2N2924. For saturation, $v_o = 0$ and

$$I \geq \frac{v_{cc}}{\beta R_c} = 0.23 \ \mu\text{A}$$

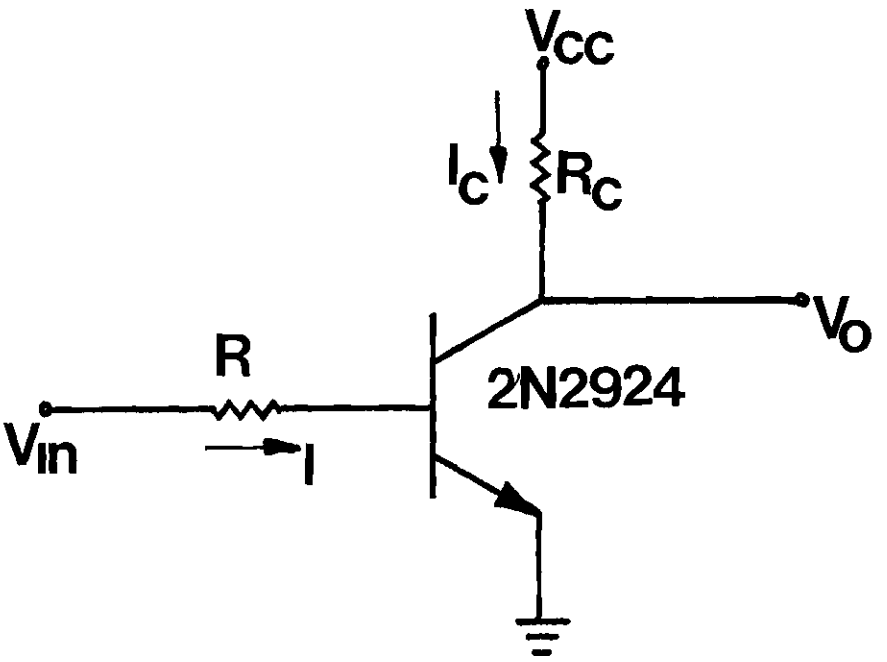

Figure 29. The Inverter Circuit

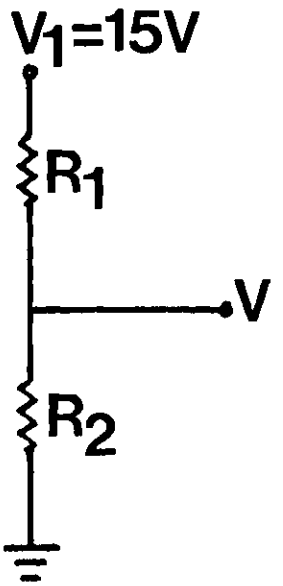

Figure 30. Voltage Divider Network $v = \frac{15R_2}{R_1+R_2}$ volts.

if $R_c = 2.2 \times 10^3$ ohms

then v_{cc} = 3 volts. From equation (62)

$$R \leq \frac{v_{in} - v_{BE}}{I}$$

For v_{in} = 3.1V, v_{BE} = 0.6V, I = .23 μA

$$R \leq 110 \times 10^3 \text{ ohms}$$

R was chosen to be 100×10^3 ohms.

Experimental Determination of v_b.

v shown in Figure 27 is a dc voltage obtained from a voltage divider network as shown in Figure 30. The R_2 value is fixed at 1000 ohms. R_1 is chosen such that for a noise level of 85 dB the v_a is of such magnitude that the reference voltage v_b for the first comparator is equal to the rms value of the amplified noise signal that is received at the negative input of the comparator. The procedure was repeated for noise pressure levels of 90, 95 and 100 dB. Table 8 summarizes the v_a values for which v_{b_1}, v_{b_2}, v_{b_3}, and v_{b_4} correspond respectively with 85, 90, 95 and 100 dB, sound pressure levels.

No actual noise source was used in the experiment. Instead the rms sound pressure, p, in newton/m^2 was calculated using equation (63) for the sound pressure levels of 85, 90, 95 and 100 in dB.

$$\text{SPL in dB} = 20 \text{ dB } \log_{10} \frac{p}{.00002} \tag{63}$$

Table 8. Noise Levels and Their Corresponding Reference Voltages

Noise Level in dB	p in N/m^2	v_{om} in mV	v in volts
85	.36	3.6	1.5
90	.63	6.3	2.7
95	1.1	11	4.9
100	2	20	8.8

Then using the sensitivity of the microphone which is 10^{-2} V for a sound pressure level of 1 newton/m^2 the p values were converted to voltages v_{om} as shown in Table 8. The equivalent v_{om} values were obtained from an audio signal generator.

The Timing System

Introduction. The timing system consists of

(a) The time base

(b) An "and" gate

(c) A clock

as shown in Figure 31. One input of the two input "and" gate is connected to the output of a time base which generates pulses at one second intervals. The other input of the gate is connected to the inverter output. When there is a signal at the inverter output, the pulses are transimitted and recorded by the clock. There are four clocks and four "and" gates corresponding to the four exposure levels whose durations are to be measured. In addition there is one clock that measures true time. All the clocks can record time up to ten hours.

The Time Base Circuit

The time base circuit is shown in Figure 32. The v_s is a 14 volts, 60 HZ signal that is obtained from the secondary of a transformer. Resistor, R, and diode D form a clipping circuit that transmits only the positive excursion of the signal. D_2 is a three volt zener diode which clamps the signal level at 3 volts. The 7490 and 7492 together divide the frequency of the signal by 60.

Calculation for Series Resistance, R

The optimum value for R, is obtained [26] from equation

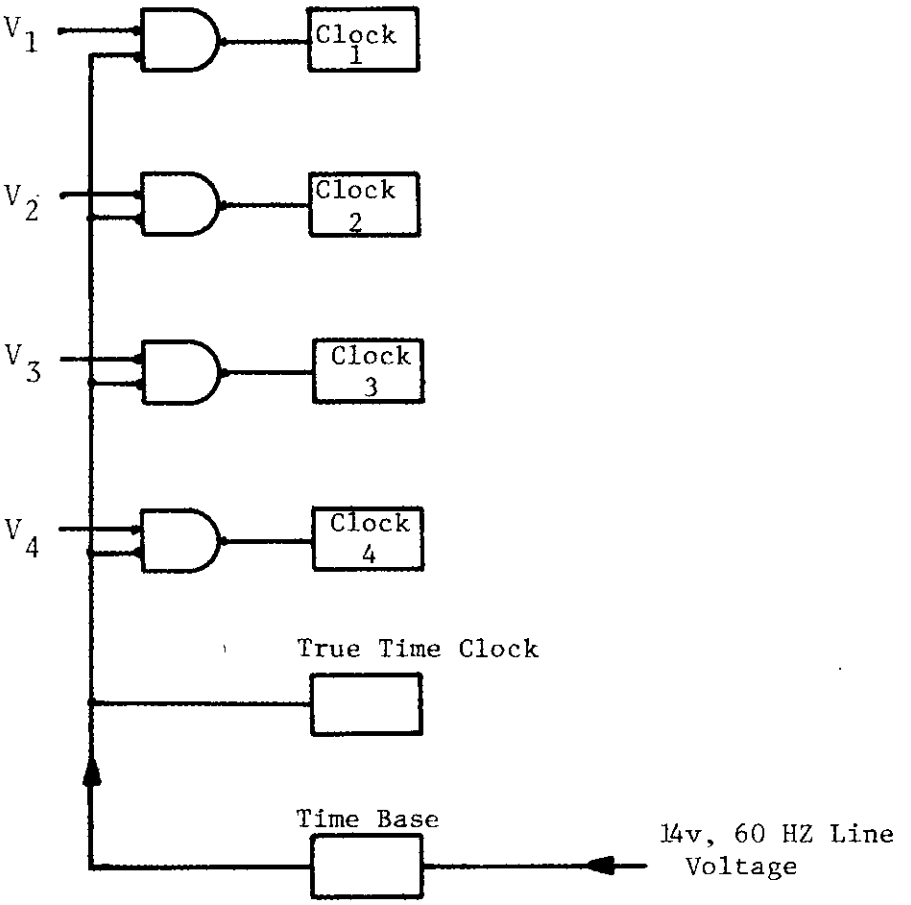

Figure 31. Timing System
V_1, V_2, V_3, V_4 are the outputs of the respective inverter stages

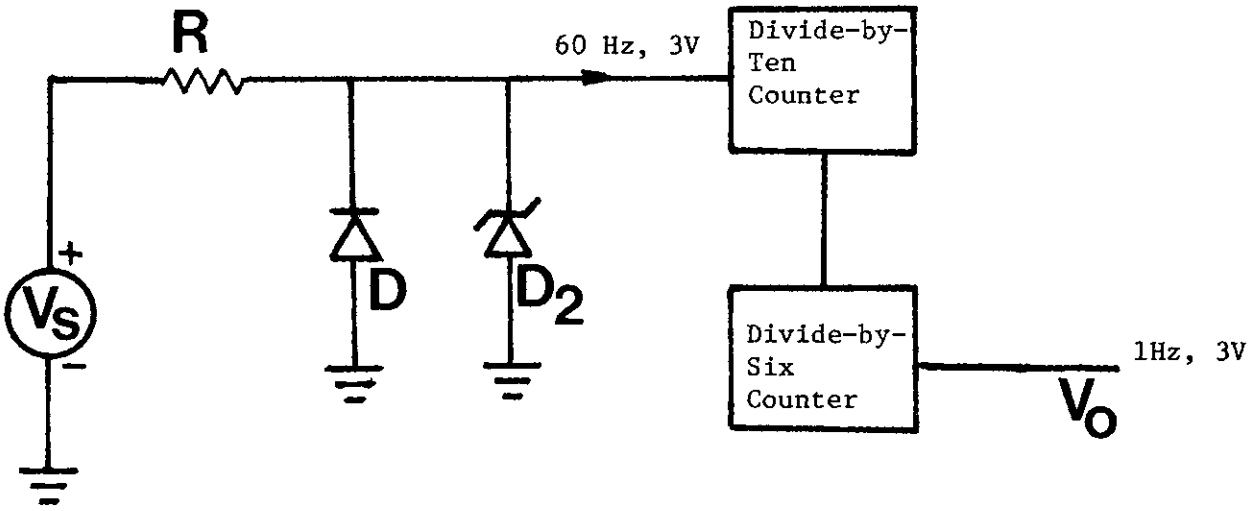

Figure 32. The Time Base Circuit

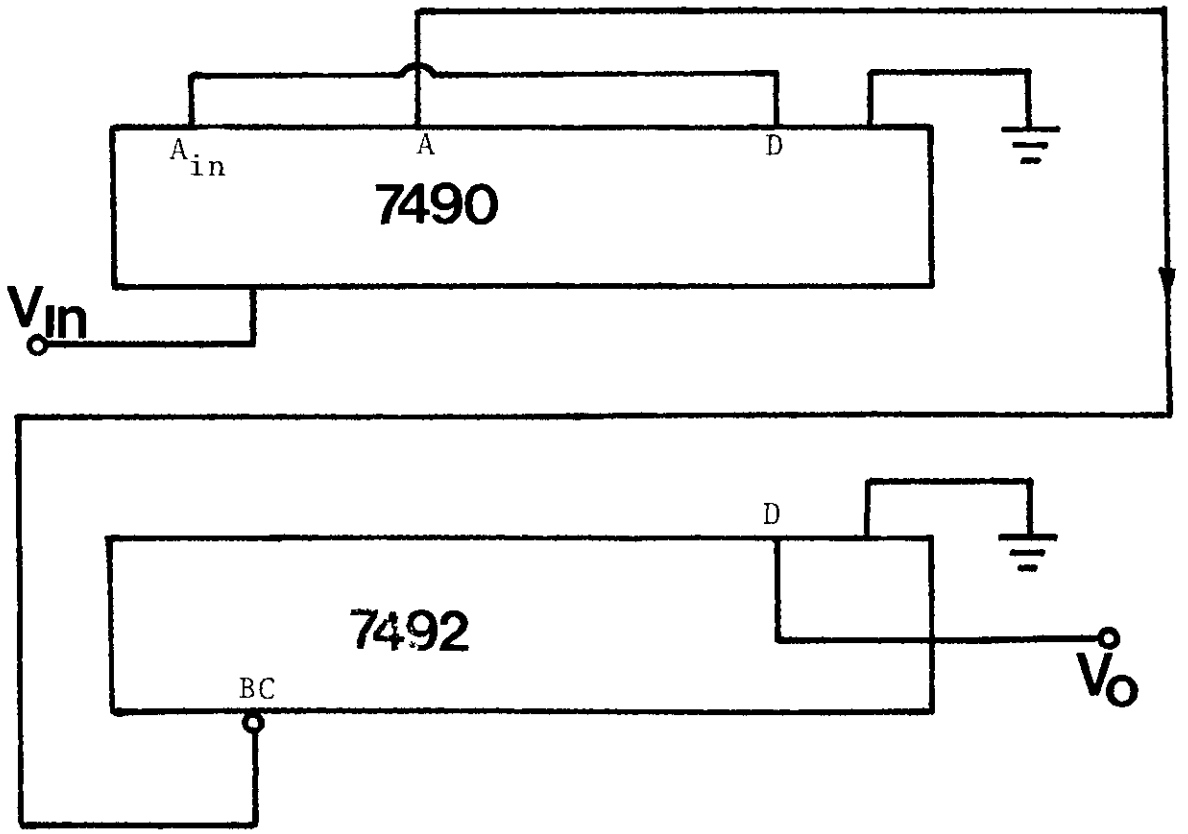

Figure 33. Frequency Divider Circuit

(64).

$$R = \sqrt{R_f R_r} \tag{64}$$

where R_f is the diode, D, forward resistance and R_r is the diode reverse resistance. R_f is of the order of a few tens of ohms or less. R_r is of the order of one hundred kilohms or more. This makes R large in the range of 10,000 ohms. R in this circuit was chosen to be 22 kilohms.

The Frequency Divider Circuit

The frequency divider circuit which divides the frequency of the 60 Hz signal by sixty consists of a cascade of a 7490 divide-by-ten counter and a 7492 divide-by-six counter as shown in Figure 33.

For the 7490 to operate in the symmetrical divide-by-ten mode the A input is connected to the D output, the input signal is then applied to the BD input. A square wave output (which is the input signal with the frequency divided by ten) appears at the A output.

For the 7492 to operate in the divide by six mode the input pulses are applied to the BC input. A frequency division of six is obtained at the D output.

The Ten Hour Clock

The ten hour clock is shown in Figure 34. Three decade counters (7490) and two divide-by-six (7492) counters

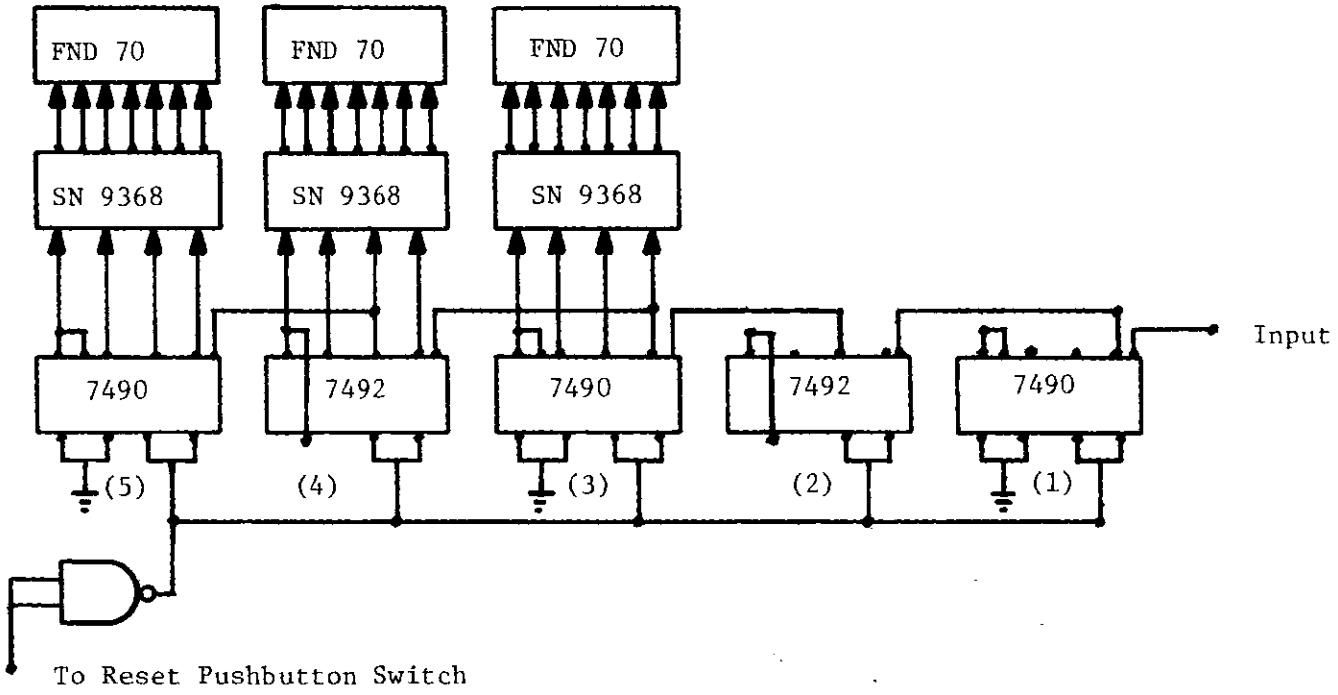

Figure 34. Block Diagram of the Ten Hour Clock. Seconds and Tens of Seconds Counts are not Displayed.

are connected in series. Counters 1 and 2 count the seconds and tens of seconds. Counters 3 and 4 count the minutes and tens of minutes. The 5th counter counts the hours up to 10 hours. The seconds count are not displayed.

When used as a BCD decade counter, the A output of the 7490 is externally connected to the BD input. The A input receives the incoming count and a count sequence is obtained at the D output in accordance with the BCD count sequence truth table shown by the count mode of Table 9. The counter counts from 0-9 and resets to zero to repeat the count.

Each of the three decoder/drivers are arranged parallel to counters 3, 4, 5. Each accepts the 4 bit binary code from the corresponding counter and produces the appropriate outputs for the selection of segments a, b, c, d, e, f, g in a 7-segment matrix display used for representing numbers 0-9.

Reset to Zero Circuit

To reset the counters to the count of zero, both reset 0 inputs of the 7490 and 7492 counters should be at logical "1" levels. The circuit to perform the operation is shown in Figure 35.

The two input nand gate with the two inputs tied together behaves like an inverter circuit. When the input is at logical "0" the output is at logical "1" and vice versa. Thus the push button switch connects the terminal marked 1 to ground when pushed in, thus setting the output of the gate (and also the counter reset zero inputs) to

Table 9. BCD Decade Count Mode Truth Table

A	B	C	D	Pulse Count
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9

Table 10. Scale-of-Six Count Mode Truth Table

A	B	C	D	Pulse Count
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5

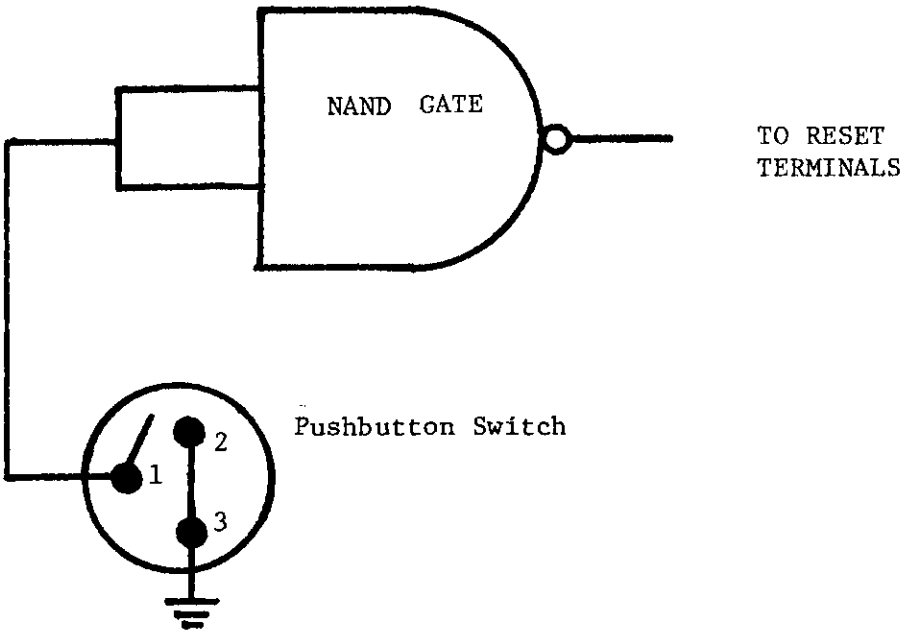

Figure 35. Reset-to-Zero Circuit

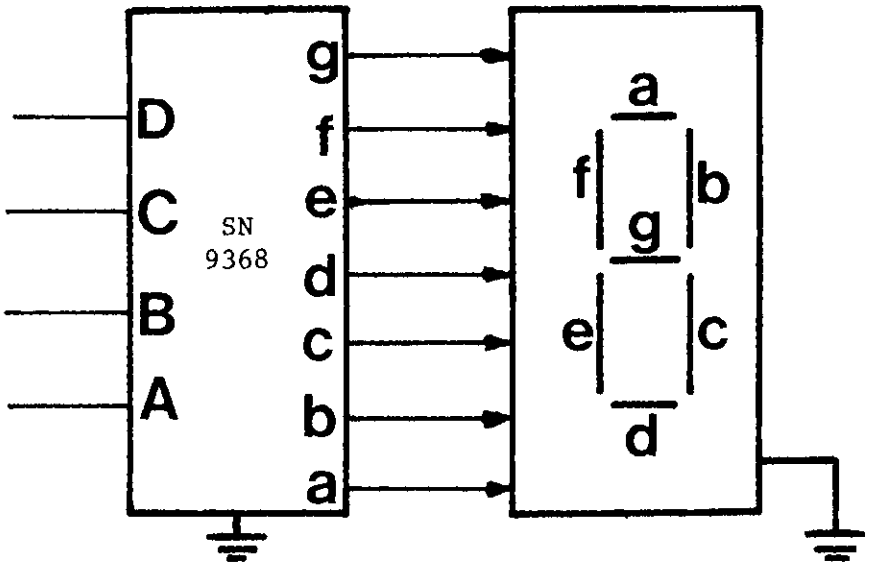

Figure 36. Block Diagram of Decoder/Driver-Display Arrangement. The 9368 decoder/driver sources exact current required by the FND 70 without external current limiting resistors.

logical "1." Consequently all the counters will be reset to zero.

When the switch is not pushed in terminal 1 is floating or at logical "1." The counters reset zero inputs will be then set at logical "0" and count operation is allowed.

CHAPTER IV

PERFORMANCE TEST OF THE NOISE DOSIMETER

The four-channel noise dosimeter was tested in the laboratory using the instruments listed below:

1. General Radio 1390-B Random Noise Generator
2. General Radio 1560-P5 Microphone
3. An Audio Amplifier
4. A Utah D8LA Loudspeaker
5. General Radio 1558 BP Octave Band Noise Analyzer

The Octave Band Analyzer has a built in sound level meter which meets the American Standard Association S-1.4 1961 standard for sound level meters.

The calibration of the microphone is traceable to the National Bureau of Standards.

The loudspeaker was housed in a chamber so as to exclude any interference from external noise sources.

Test Procedure

The amplified pink noise signal from the noise generator was applied to the loudspeaker which generated an audible sound. The amplifier's gain control was adjusted so as to produce a sound pressure level of 85 dB at the microphone as determined by the General Radio Octave Band Noise Analyzer.

The microphone was disconnected from the Noise Analyz-

er and connected to the Noise Dosimeter. The flat frequency response weighting was selected. The gain of the preamplifier circuit of the Noise Dosimeter was adjusted by means of an attenuator such that the channel 1 clock just began to count. This adjustment calibrates channel 1 to measure the duration of a sound pressure level of 85 dB or more.

Following the same procedure a noise level of 90 dB was produced. The microphone was again transferred to the Noise Dosimeter. Channel 1 clock counted continuously as expected. But channel 2 clock would count when the sound pressure level was increased slightly above 90 dB. This is due to the error involved in calibrating the first channel to respond to the 85 dB of sound pressure level. The maximum error observed was 1 dB of sound pressure level.

Proceeding as before it was found that to within an accuracy of 1 dB sound pressure level, the third and fourth channels, respectively, responded to sound pressure levels of at least 95 dB and 100 dB.

The whole process was repeated on the A and C frequency weighting scales of the Noise Analyzer and Dosimeter. The same observations were made as before.

The noise level was increased slightly above 100 dB and the Noise Dosimeter was left to operate for twenty four hours. At the end of the twenty four hour period it was observed that all the clocks on the four channels recorded the same time which corresponded with the time measured by

the true time clock. The test procedure was repeated. The results agreed with those obtained during the previous day.

CHAPTER V

CONCLUSIONS

A four channel Noise Dosimeter was designed to measure the durations of noise exposure levels of 85, 90, 95 and 100 dB cumulatively.

The instrument was tested in the laboratory with a pink noise source. It was observed that if the first channel is calibrated to respond to sound pressure level of at least 85 ± 1 dB, then to within an accuracy of 1 dB sound pressure level, the response of the adjacent channels are separated by 5 dB of sound pressure level on the frequency weighting (A, C and flat) scales.

Also if the sound pressure level is 85 dB none of the channel clocks will count. If the sound pressure level is slightly above 100 dB then all the four channels will respond. Therefore, the instrument measures the cumulative duration of sound pressure levels of 85, 90, 95 and 100 dB within a maximum error of 1 dB of sound pressure level.

The cumulative noise exposure factor, S, defined as the percent of the allowable noise exposure accumulated within a period of time can be calculated by using either equation (65a) or (65b).

$$S = \frac{C_1 - C_2}{16} + \frac{C_2 - C_3}{8} + \frac{C_3 - C_4}{4} + \frac{C_4}{2} \qquad (65a)$$

$$S = \frac{C_1 + C_2 + 2C_3 + 4C_4}{16} \qquad (65b)$$

C_1, C_2, C_3 and C_4 are, respectively, the time in hours that the clocks of channels 1, 2, 3 and 4 record. The figures 16, 8, 4, 2 are the time in hours that are allowed for exposure to noise levels of 85, 90, 95 and 100 dB.

To calculate the S factor, the C_N (N = 1, 2, 3, 4) values are read on the clocks and substituted in either equation (65a) or (65b). For efficient industrial noise control the cumulative noise exposure factor should not exceed unity according to the Walsh-Healey Act.

APPENDIX A

DERIVATION OF VOLTAGE GAIN OF SINGLE STAGE COMMON EMITTER AMPLIFIER

From Figure 38

$$v_s = v_1 + i_1 R_s \tag{66}$$

$$v_1 = h_{re} v_2 + i_b h_{ie} \tag{67}$$

$$i_2 = h_{fe} i_b + v_2 hoe \tag{68}$$

$$v_2 = - i_2 R_L' \tag{69}$$

$$\text{voltage gain } A_v = \frac{v_2}{v_1} \tag{70}$$

From equations (68) and (69) i_2 can be eliminated.

i.e.,

$$-\frac{v_2}{R_L'} = h_{fe} i_b + v_2 hoe \tag{71}$$

$$v_2 \left(hoe + \frac{1}{R_L'}\right) = - h_{fe} i_b \tag{72}$$

$$v_2 \left(\frac{R_L' \, hoe + 1}{R_L'}\right) = - h_{fe} \, i_b \tag{73}$$

$$v_2 = - \left(\frac{h_{fe} \, i_b}{R_L' \, hoe + 1}\right) R_L' \tag{74}$$

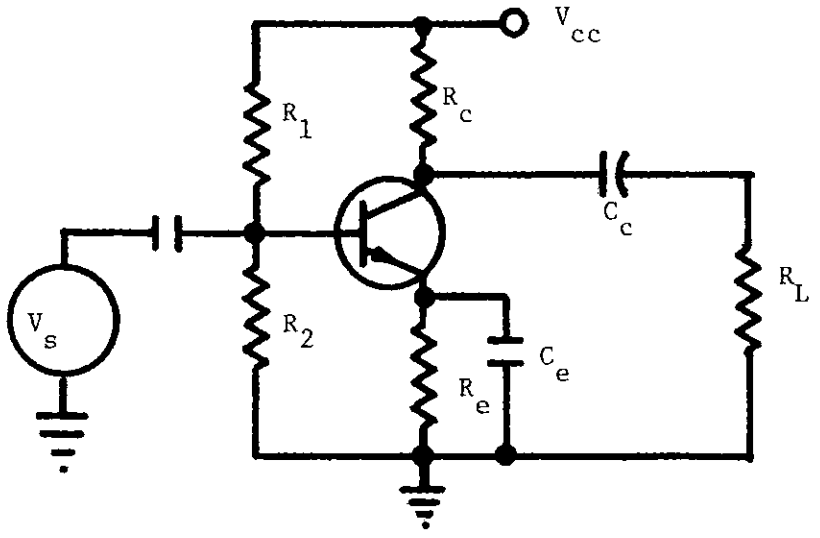

Figure 37. Basic Common Emitter Single Stage Amplifier

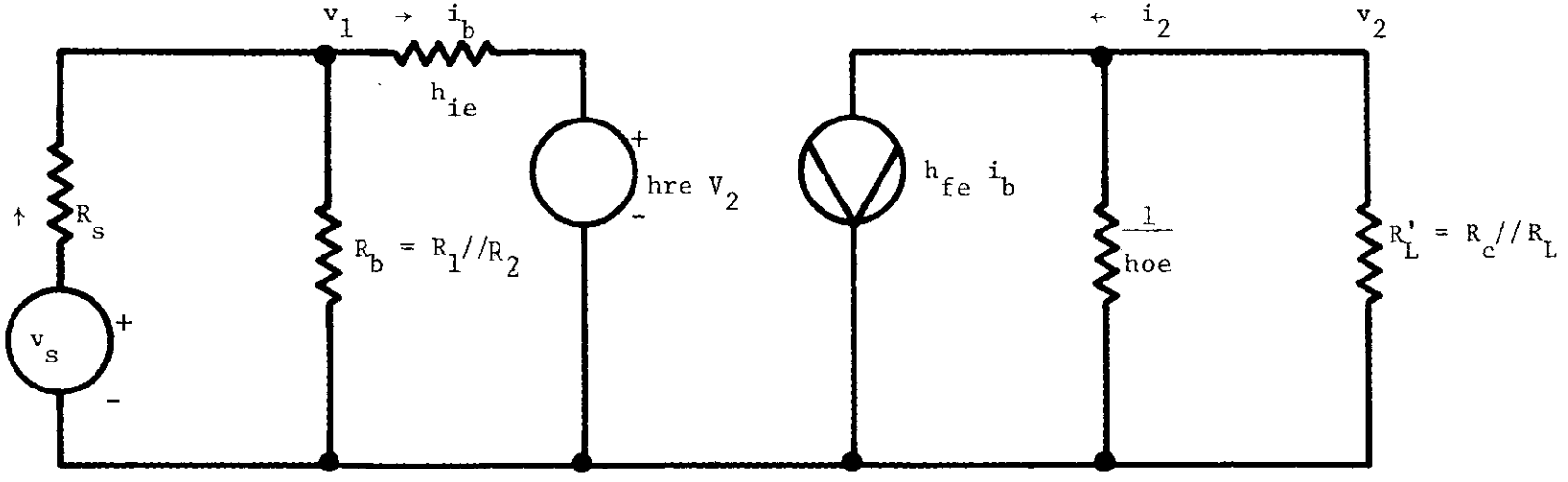

Figure 38. Mid-Frequency Equivalent Circuit of the Amplifier

or

$$i_b = - \frac{v_2 R_L' hoe + 1}{h_{fe} R_L'} \tag{75}$$

Substituting for i_b in equation (67).

$$v_1 = h_{re} v_2 - \frac{h_{ie} v_2 (R_L' hoe + 1)}{h_{fe} R_L'}$$

$$= v_2 \{h_{re} - \frac{h_{ie}}{h_{fe} R_L'} (R_L' hoe + 1)\} \tag{76}$$

$$\frac{v_2}{v_1} = A_v = \frac{h_{fe} R_L'}{h_{fe} h_{re} R_L' - (h_{ie} + R_s)(R_L' hoe + L)}$$

For 2N 3391A

$h_{fe} = 340$

$h_{re} = 4.1 \times 10^{-4}$

$hoe = 36.4 \times 10^{-6}$ mho

$h_{ie} = 4.8 \times 10^3$ ohm

For the first stage, the total load impedance, R_L, is the input impedance, h_{ie_2}, of the transistor paralleled by the base bias resistor R_{b_2} of the second stage.

i.e., $R_L = h_{ie_2} \; // \; R_{b_2}$

$= (4.8 \times 10^3 \; // \; 33 \times 10^3)$ ohms

$= 4.2 \times 10^3$ ohms

Now $R_L' = R_c \; // \; R_L$

$= (6.8 \times 10^3 \; // \; 4.2 \times 10^3)$ ohms

$R_L' = 2.6 \times 10^3$ ohms (78)

$$R_L' hoe = 2.6 \times 10^3 \times 36.4 \times 10^{-6}$$

$$= .095 \text{ ohm} \tag{79}$$

$$h_{fe} h_{re} R_L' = 363 \text{ ohms} \tag{80}$$

$$h_{ie}(R_L' hoe+1) = 5.28 \times 10^3 \text{ ohms} \tag{81}$$

From equation (80) and (81)

$$h_{ie} (R_L' hoe + 1) >> h_{fe} h_{re} R_L'$$

The factor $h_{fe}h_{re}R_L'$ can be neglected in equation (76). Hence the voltage gain per single stage, A_v, reduces to

$$A_v = -\frac{h_{fe}R_L'}{h_{ie}(R_L' hoe + 1)} \tag{82}$$

Since $R_L' hoe << 1$, A_v is approximately equal to

$$A_v = -\frac{h_{fe}R_L'}{h_{ie}} \tag{83}$$

APPENDIX B

DERIVATION OF THE TRANSFER FUNCTION OF THE C NETWORK

Refer to Figure 14.

The overall voltage given A(s) is the product of the voltage gains of the individual differentiators.

$$A(s) = A_1(s) \times A_2(s) \tag{84}$$

where $A_1(s)$ and $A_2(s)$ are the voltage gains of the first and second stages, respectively.

$$\text{Now } A_1^*(s) = -\frac{Z_F}{Z_1} \tag{85}$$

$$\text{where } Z_F = R_2 // \frac{1}{SC_2} \tag{86}$$

is the impedance in the feedback loop; and

$$Z_1 = R_1 + \frac{1}{SC_1} \tag{87}$$

is the series input impedance. Similarly

$$A_2(s) = -\frac{Z_F}{Z_1'} \tag{88}$$

$$Z_F' = R_4 // \frac{1}{SC_4} \tag{89}$$

*See equation (45)

$$Z_1' = R_3 + \frac{1}{SC_3} \tag{90}$$

From equations (85), (86), (88) and (89);

$$A(s) = \frac{R_4 // \frac{1}{SC_4}}{R_3 + \frac{1}{SC_3}} \quad \frac{R_2 // \frac{1}{SC_2}}{R_1 + \frac{1}{SC_1}} \tag{91}$$

$$= \frac{R_2C_1R_4C_3\ S^2}{(1 + R_4SC_4)(1 + R_3SC_3)(1 + R_2SC_2)(1 + R_1SC_1)}$$

$$= \frac{S^2}{R_1R_3C_2C_4(S + \frac{1}{R_1C_1})(S+\frac{1}{R_2C_2})(S+\frac{1}{R_3C_3})(S+\frac{1}{R_4C_4})}$$

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