LOW-POWER CMOS FRONT-ENDS FOR WIRELESS PERSONAL AREA NETWORKS

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LOW-POWER CMOS FRONT-ENDS FOR WIRELESS PERSONAL AREA NETWORKS

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To pappa, amma, achachen, and koche

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LIST OF ABBREVIATIONS AND SYMBOLS

ABBREVIATIONS:

1P6M: 1 Poly and 6 Metals

APDP: Anti Parallel Diode Pair

BiCMOS: Bipolar Complementary Metal Oxide Semiconductor

BLNA: Broadband Low Noise Amplifier

CMOS: Complementary Metal Oxide Semiconductor

IF: Intermediate Frequency

IIP3 or iIP3: Input Third Intercept Point

IP3: Third Intercept Point

L: Device Length

LNA: Low Noise Amplifier

LO: Local Oscillator

LR-PAN: Low-Rate Personal Area Network

LR-WPAN: Low-Rate Wireless Personal Area Network

MGTR: Multiple Gated Transistor

MIMO: Multiple-Input Multiple-Output

NF: Noise Figure

NMOS: N-Type Metal Oxide Semiconductor

OIP3 or oIP3: Output Third Intercept Point

P1dB: 1 dB Compression Point

PAN: Personal Area Network

PLL: Phase Locked Loop

PMOS: P-Type Metal Oxide Semiconductor

QVCO: Quadrature Voltage Controlled Oscillator

RF: Radio Frequency

SNR: Signal to Noise Ratio

TRFL: Tuned Resistive Feedback Low Noise Amplifier

VCO: Voltage Controlled Oscillator

VGA: Variable Gain Amplifier

W: Device Width

W/L: Device Aspect Ratio

WLAN: Wireless Local Area Network

WPAN: Wireless Personal Area Network

SYMBOLS:

β: Transconductance parameter

γ: Process dependent parameter in threshold voltage

μ_n: Electron mobility

ϕ_f: Fermi level

λ: Channel length modulation parameter

C_{js}: Depletion region capacitance

C_{ox}: Oxide capacitance per unit area

f_T: Transition frequency

g_{ds}: Output conductance of the transistor.

g_m: Transconductance

g_{m3}: $(\delta^3 I_D / \delta V^3_{GS})$

I_D: Drain current (DC bias)

I_{DO}: Process dependent parameter in subthreshold device equation

k: Boltzmann's constant

n: Subthreshold slope factor

NF_{min}: Minimum Noise Figure

q: Charge of an electron

T: Temperature in K

V_{DS}: Drain-source bias voltage

v_{DS}: Drain-source voltage (bias & small-signal)

V_{GS}: Gate-source bias voltage

v_{gs}: Gate-source small-signal voltage

v_{GS}: Gate-source voltage (bias & small-signal)

v_{LO}: LO signal amplitude

v_{SB}: Source-bulk voltage (bias & small-signal)

V_t: Threshold voltage at operating point.

v_t: Threshold voltage

v_{t0}: Threshold voltage with v_{SB} (source-bulk voltage) set to zero

SUMMARY

The potential of implementing subthreshold radio frequency circuits in deep sub-micron CMOS technology was investigated for developing low-power front-ends for wireless personal area network (WPAN) applications. It was found that the higher transconductance to bias current ratio in weak inversion could be exploited in developing low-power wireless front-ends, if circuit techniques are employed to mitigate the higher device noise in subthreshold region. The first fully integrated subthreshold low noise amplifier was demonstrated in the GHz frequency range requiring only 260 μW of power consumption. Novel subthreshold variable gain stages and down-conversion mixers were developed.

A 2.4 GHz receiver, consuming 540 μW of power, was implemented using a new subthreshold mixer by replacing the conventional active low noise amplifier by a series-resonant passive network that provides both input matching and voltage amplification. The first fully monolithic subthreshold CMOS receiver was also implemented with integrated subthreshold quadrature LO (Local Oscillator) chain for 2.4 GHz WPAN applications. Subthreshold operation, passive voltage amplification, and various low-power circuit techniques such as current reuse, stacking, and differential cross coupling were combined to lower the total power consumption to 2.6 mW.

Extremely compact resistive feedback CMOS low noise amplifiers were presented as a cost-effective alternative to narrow band LNAs using high-Q inductors. Techniques

to improve linearity and reduce power consumption were presented. The combination of high linearity, low noise figure, high broadband gain, extremely small die area and low power consumption made the proposed LNA architecture a compelling choice for many wireless applications.

Chapter 1
Introduction

1.1 Motivation

Mobile communication devices, powered by batteries, have stringent limitations on power consumption. Obviously, a wireless device consuming higher power will require more frequent battery recharge or replacement compared to another device using a similar battery. Higher power consumption can also have implications on equipment heating and form factor. Hence, low-power circuit design has always been extremely important in developing mobile communication devices.

Over the past decade, there has been a tremendous increase in the demand for wireless communication devices. However, most of this growth has mainly been in either cellular phone applications with large range or high data throughput applications like wireless local area networks (WLAN). Low data-rate systems requiring low-complexity wireless connectivity for home and industrial automation, control, and monitoring have been largely neglected until recently. Reducing power consumption and cost have higher priority over increasing data-throughput and range in these applications. A low-rate wireless personal area network (LR-WPAN) is a low-complexity network optimized for low-cost and low-power short-range wireless applications. Task Group 4 of the IEEE 802.15 Wireless Personal Area Network working group has now developed a wireless communication standard for such LR-WPANs [1], [2]. A consortium of semiconductor

companies, technology providers, OEMs, and end-users, called the ZigBee Alliance, has also been formed to develop a global specification for low-power, cost-effective wireless applications based on the IEEE 802.15.4 standard. Volume production of low-cost wireless nodes with lifetimes extending over years is expected to usher in a new generation of wireless applications that were inconceivable in the past.

Typical applications envisioned for low-rate WPANs [3] include the following:

- Lighting controls
- Air conditioning controls
- Remote meter reading
- Security
- Sensors for fire safety
- Residential and industrial automation
- Automotive control and monitoring
- Entertainment
- Health care

A wireless solution to the applications listed above is not practical if the high power consumption in wireless devices requires frequent battery replacement or recharge. Also vital is the cost of each node if a large-scale deployment is to be viable. Since these applications need only low-complexity wireless connectivity with low data-rate and range, a low-cost and low-power wireless solution is feasible. The IEEE 802.15.4 standard was developed specifically for these applications.

The power consumption in LR-WPAN front-ends is expected to be lower than that in other applications because of the relaxed specifications required to support a low data throughput [4]. Moreover, the extremely small transmitter duty cycle in these wireless nodes can also be exploited to guarantee a longer lifetime for the battery. However, novel circuit and system techniques are essential to further reduce power consumption and cost in LR-WPAN front-ends to cater to many new applications that call for even longer battery lives.

Ultra low-power wireless devices also have a myriad of biomedical applications such as patient monitoring and implants. Wireless endoscopy [5] and many other swallowable, body worn [6], [7], and implantable biomedical solutions are emerging today bringing about sweeping changes in the health care and medical fields.

The objective of this research is to develop circuit techniques to lower power consumption and cost of WPAN front-ends. Subthreshold CMOS operation, passive voltage amplification, and low-power techniques like stacking, current reuse, and differential cross coupling are explored to develop micro-power front-end circuits. Resistive feedback based impedance matching is also investigated to reduce the number of high-Q on-chip inductors required in low noise amplifiers so as to reduce die area and cost.

1.2 IEEE 802.15.4 (ZigBee) LR-WPAN Standard

Until recently, the main focus of the wireless industry has been high data throughput or large range systems. In many of these systems, the front-end power consumption needed to meet the specifications is high enough to require frequent battery recharge. However, there exists a range of control, monitoring, and automation applications that require a low-complexity wireless link supporting a low data rate. Unlike other systems, the power consumption of wireless nodes for such applications can be minimized at the cost of reduced data throughput and range. The power consumption in such wireless nodes can be further reduced by utilizing strict power management schemes, such as power-down and sleep modes.

The IEEE 802.15.4 standard was developed to cater to the automation, control, and monitoring applications that required low-complexity wireless connectivity with low data rate and smaller range. This standard is compared with other standards in Table 1.1 [8], [9]. Compared to others, LR-WPANs have relaxed performance specifications in order to make cost effective low-power implementations possible.

1.3 Challenges

As can be seen from Table 1.1, LR-WPAN devices have lower data throughput and range specifications but are required to have very long battery lives. Since the transmitter

duty cycle is extremely low in such applications, it is the receiver power consumption that determines the battery life of the wireless node. Typically, the receiver blocks having the highest power consumption are LNA, mixer, VCO, and VCO buffers. Novel circuit and system techniques are therefore required to significantly lower the power consumption [10] in these circuits.

Table 1.1: Comparison of IEEE 802.15.4 (ZigBee) LR-WPAN standard with other wireless standards.

Standard	**802.11b** (Wi-Fi)	GSM/GPRS CDMA/1xRTT	**802.15.1** (Bluetooth)	**802.15.4 (ZigBee)**
Focus	Large data-rate networking	Large range voice/data	Cable Replacement	**Control and Monitoring**
Frequency	2.4 GHz	900 MHz, 1800 MHz	2.4 GHz	**2.4 GHz, 915 MHz, 868 MHz**
System Resources	1 MB +	16 MB +	250 KB +	**4 – 32 KB**
Battery Life (Days)	0.5 - 5	1 – 7	1 – 7	**100 – 1,000 +**
Data-Rate (kbps)	11,000 +	64 – 128 +	720	**20 – 250**
Range (m)	1 – 100	1,000 +	1 – 10 +	**1 – 100 +**
Success Metrics	Speed, Flexibility	Reach, Quality	Cost, Convenience	**Reliability, Power, Cost**

Lowering the total cost of each wireless node is also vital to the success of such a network in volume applications. Hence, a fully integrated CMOS solution is desired that

requires minimal external components. Receiver circuits that utilize fewer high-Q, on-chip passives are required to reduce the overall die area and thus lower cost.

1.4 Organization of the Thesis

This dissertation is divided into seven chapters. After introducing the research objective and challenges in chapter 1, chapter 2 starts with a review of the basic wireless receiver architectures. The performance trade-offs involved in reducing power consumption in wireless receivers is discussed next. Chapter 2 ends with a review of existing low-power receiver front-end circuit techniques.

Chapter 3 discusses subthreshold CMOS operation including basic device equations. Device noise of subthreshold transistors is also reviewed. The higher transconductance to bias current ratio and other advantages provided by subthreshold circuits are discussed. Also presented are the challenges involved in extending the operation of subthreshold CMOS into the multi-GHz range.

Low-power wireless front-end blocks implemented in subthreshold CMOS are discussed next in chapter 4. A 1 GHz subthreshold low noise amplifier (LNA) implemented in a 0.18 μm CMOS process is presented. 1X and 2X mixers based on source/bulk LO (local oscillator) injection are discussed next including a mixer based on an active anti-parallel diode pair (APDP) requiring extremely low power consumption.

Also presented in this chapter are low-power variable gain blocks for base-band and IF (intermediate frequency).

Integrated subthreshold receivers are presented next in chapter 5. A micro power CMOS receiver utilizing a passive LNA and a subthreshold CMOS mixer is discussed first. The subthreshold mixer is a modified version of the APDP CMOS mixer explained in chapter 4, with a higher conversion gain and a lower noise figure. A 2.6 mW fully integrated subthreshold receiver is presented next. Included in this receiver are passive voltage amplifiers, subthreshold differential LNA, quadrature subthreshold mixers, subthreshold VGAs, and subthreshold LO signal generation blocks. Subthreshold operation, passive voltage amplification, and various low-power circuit techniques such as current reuse, stacking, and differential cross coupling have been combined to lower the total power consumption of the integrated subthreshold quadrature receiver.

Cost aspects of the wireless receiver implementation are discussed in chapter 6. Circuit techniques to reduce area requirement in receiver circuits are presented. Inductor-less CMOS LNA circuits are reviewed and the power consumption and linearity challenges involved are discussed. Linearity limitations in resistive feedback LNA circuits are analyzed and circuit techniques are presented to reduce non-linearity. Low-power techniques like current-reuse are also presented to reduce power consumption in these circuits. A tuned resistive feedback LNA, using a single compact low-Q on-chip inductor, is presented next achieving high gain, low noise figure, and high linearity while requiring low power consumption and extremely low die area.

The contributions of this research work are summarized in the final chapter. Potential future research opportunities are also discussed in the end.

Chapter 2
Wireless Receivers

Before data is transmitted over a wireless medium, its spectrum is shifted to the channel assigned for transmission by modulating an RF carrier signal. A wireless receiver front-end performs the frequency translation and demodulation to retrieve the data. The most vital specifications of an RF receiver are its sensitivity and selectivity. While the receiver sensitivity is defined as the weakest signal level that it can detect with acceptable signal-to-noise ratio, the selectivity is a measure of its immunity to interferers and blockers. Compared to other wireless applications, both sensitivity and selectivity requirements of WPAN systems are less stringent, making it possible to reduce both cost and power consumption.

Basic wireless receiver architectures are reviewed in this chapter. The factors determining the total power consumption in wireless receivers are discussed. Existing circuit techniques to lower power consumption in receiver front-ends are also reviewed.

2.1 Receiver Architectures

The receiver architecture chosen for implementation is extremely important in determining the power dissipation, cost, and complexity of the wireless transceiver [11]. The transmitter upconverts the baseband spectrum to the RF frequency and transmits it

across the wireless medium in the frequency channel allotted to the user. Often, strong interferers are present close to the spectrum of the desired signal that can corrupt the demodulation in the receiver. Band-selection and channel selection filters are required to limit the effects of the interferers. The frequency plan and architecture of the receiver is determined after considering the Q, in-band loss, and out-of-band rejection required in these filters.

2.1.1 Heterodyne Receivers

In heterodyne receivers, the signal is first down-converted to an intermediate frequency (IF). If the channel selection filter is implemented at the RF frequency, the required filter Q will be extremely high. The Q is significantly reduced when channel-selection is implemented at the IF frequency. The frequency translation is carried out by mixer circuits that usually have high noise figures. A low-noise amplifier (LNA) is used before the mixer so as to lower the overall noise figure of the receiver.

In heterodyne receivers, the frequency bands above and below the local oscillator (LO) signal are down-converter to the same IF. For example, if the desired signal frequency is f_{RF}, where $f_{RF}= f_{LO}+ f_{IF}$, then the signal at the frequency $f_{IMAGE}=f_{LO}-f_{IF}$ is also down-converted to f_{IF}. The signal at f_{IMAGE} is referred to as the image. The image has to be sufficiently suppressed before the down-conversion circuits for the proper operation of the heterodyne receiver. Expensive off-chip image-reject filters are therefore required in

heterodyne receivers making this architecture unsuitable for low-cost WPAN applications.

In heterodyne receivers, a low IF frequency makes channel-selection easier by lowering the Q of the channel-select filter. However, this makes image rejection more difficult because the desired signal spectrum and the image spectrum are close to each other. This trade-off between image rejection and channel-selection leads to dual-IF heterodyne implementation where the down-conversion is performed twice, as shown in the block diagram in Figure 2.1. Since the channel selection is done multiple times at progressively lower IF frequencies, the filter Qs required are significantly relaxed. However, the additional circuits required in this implementation increase both cost and power consumption of such receivers.

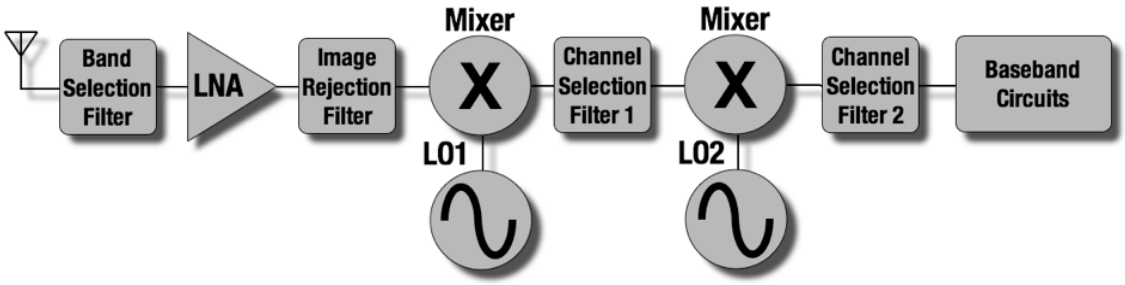


Figure 2.1: Block diagram of a dual-IF heterodyne receiver.

2.1.2 Homodyne Receivers

In homodyne or direct-conversion receivers, the RF signal is directly translated to baseband in a single down-conversion step. Hence, the LO frequency and the carrier

frequency are equal. The block diagram of a homodyne receiver is shown in Figure 2.2. Since there is no image frequency, no image rejection filter is needed. Direct-conversion receivers are significantly simpler than heterodyne receivers and are easier to integrate. They also have lower power consumption usually since the number of blocks required is lower.

The homodyne architecture suffers from a new set of issues because of its gain distribution. In a heterodyne receiver, the total gain of the receiver chain is distributed across the RF, IF, and baseband blocks. In a direct-conversion receiver, on the other hand, the gain preceding the baseband blocks is low and most of the gain is achieved after down-conversion in the baseband circuits. This significantly worsens the impact of DC offsets and flicker noise added by the baseband circuits.

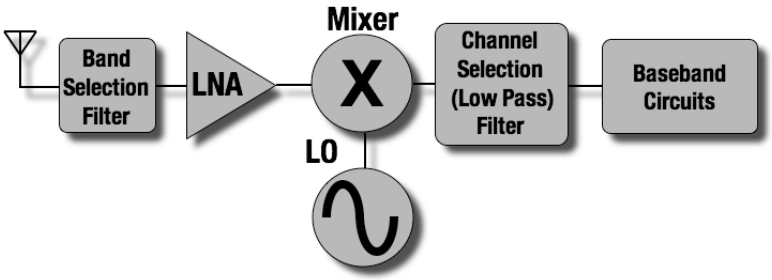


Figure 2.2: Block diagram of a direct conversion receiver.

DC offsets are created in receivers due to LO leakage and self-mixing in the down-conversion mixer. Flicker noise is the inherent low-frequency device noise present in all circuits. Since flicker noise is more dominant in devices associated with surface

phenomena, CMOS circuits exhibits high flicker noise [12]. Very large devices are usually used in baseband circuits to reduce flicker noise.

If the homodyne receiver is used for baseband signals without Hermitian symmetry in its spectrum, quadrature down-conversion is necessary to avoid loss of information. Unlike heterodyne receivers where the quadrature down-conversion can be done using a much lower LO frequency or even in the digital domain, direct-conversion receivers have to implement this down-conversion using the high LO frequency making it much more susceptible to I/Q mismatch issues. This effect is also exacerbated by the lower gain preceding the down-conversion as discussed before. Even-order distortion is another phenomena that is unimportant in heterodyne receivers, but can severely degrade homodyne performance. This is because the second-order distortion products of two interferers that are close to each other can corrupt the desired signal after down-conversion due to mixer feedthrough.

2.1.3 Low-IF Receivers

As the name suggests, the RF signal is down-converted to a low intermediate frequency in a low-IF receiver. The small frequency separation between the LO and RF carrier ensures that the DC offset, flicker noise and LO leakage issues are not severe in this architecture [13]. However, the problem of the image is more severe. Image-reject architectures like Hartley receiver [11] based on quadrature down-conversion can be used to suppress the image. The image rejection achieved is typically about 35 dB without

additional trimming due to device mismatch, which is sufficient for WPAN standards like IEEE 802.15.4 [14].

Low-IF architecture has emerged as the predominant choice for low-power, low-cost wireless receiver implementation today. It has the simplicity offered by direct-conversion architecture, but circumvents homodyne issues like DC offset, flicker noise, and LO leakage. However, it is not suitable for implementations requiring high image rejection.

2.2 Power Consumption in Wireless Front-ends

Lowering the total power consumption in battery powered wireless communication devices is critical so as to avoid frequent battery recharge or replacement. The total power consumption in a front-end is dependent on a multitude of factors. The sensitivity specification of the front-end determines the minimum gain and maximum noise figure of the receiver, both of which are dependent on the power consumption in receiver circuits. The output power requirement of the power amplifier is also extremely important in determining the total power consumption in typical wireless front-ends. In WPAN applications however, the power consumption in power amplifier and other transmitter blocks are not as critical since the transceiver is rarely in the transmit mode.

The carrier frequency and process technology also affect the total power consumption. For example, if high Q passives are available at the operating frequency in the process technology selected, power consumption in amplifiers and oscillators can lowered significantly without compromising gain and noise performance. However, such passives are not available in low-cost CMOS processes.

The power consumption in a wireless device is also dependent on the bandwidth and the supported data rate. Higher bandwidth and data rate generally requires higher transconductance in analog circuits and higher clock speeds in digital circuits, respectively, both of which increase power consumption. Complex modulation schemes requiring high processing power in the digital baseband section can also increase the total power consumption.

Another important factor in determining the total power consumption in front-ends is the blocker profile of the standard. If the receiver has to work in the presence of strong interferers close to the signal spectrum, the linearity and phase noise specifications become more stringent, potentially leading to significant increase in power consumption in the front-end circuits.

Extremely small duty cycle, in WPAN applications for example, help decrease the overall power consumption. The front-end is often in stand-by or off mode in such applications and the off state leakage power becomes vital. Circuit and system techniques

are required to further reduce power consumption and cost in LR-WPAN front-ends for low-power and low-cost wireless applications.

2.3 Low-Power RF Circuit Techniques

Bias current reuse, functional combination, controlled positive feedback, high impedance interfaces, technology scaling, and subthreshold biasing are common low power analog techniques. Many of these techniques have been used for reducing power consumption in wireless front-end circuits too. Previously reported circuit techniques to lower power consumption in wireless front-ends are reviewed in this section.

2.3.1 High-Q Passives

High-Q off-chip passive components have been used to reduce power consumption in wireless transceivers [15] - [17]. This technique is utilized in [16] to develop a 900 MHz CMOS receiver consuming 4.5 mW of power. The receiver had a noise figure of 7.4 dB. In [17], a high-Q off-chip inductor is combined with weak-inversion CMOS transistors to develop a micropower Colpitts voltage controlled oscillator for 400 MHz to 1 GHz. Consuming only 690 μW of power, it achieves –107 dBc/Hz phase noise at 100 kHz offset.

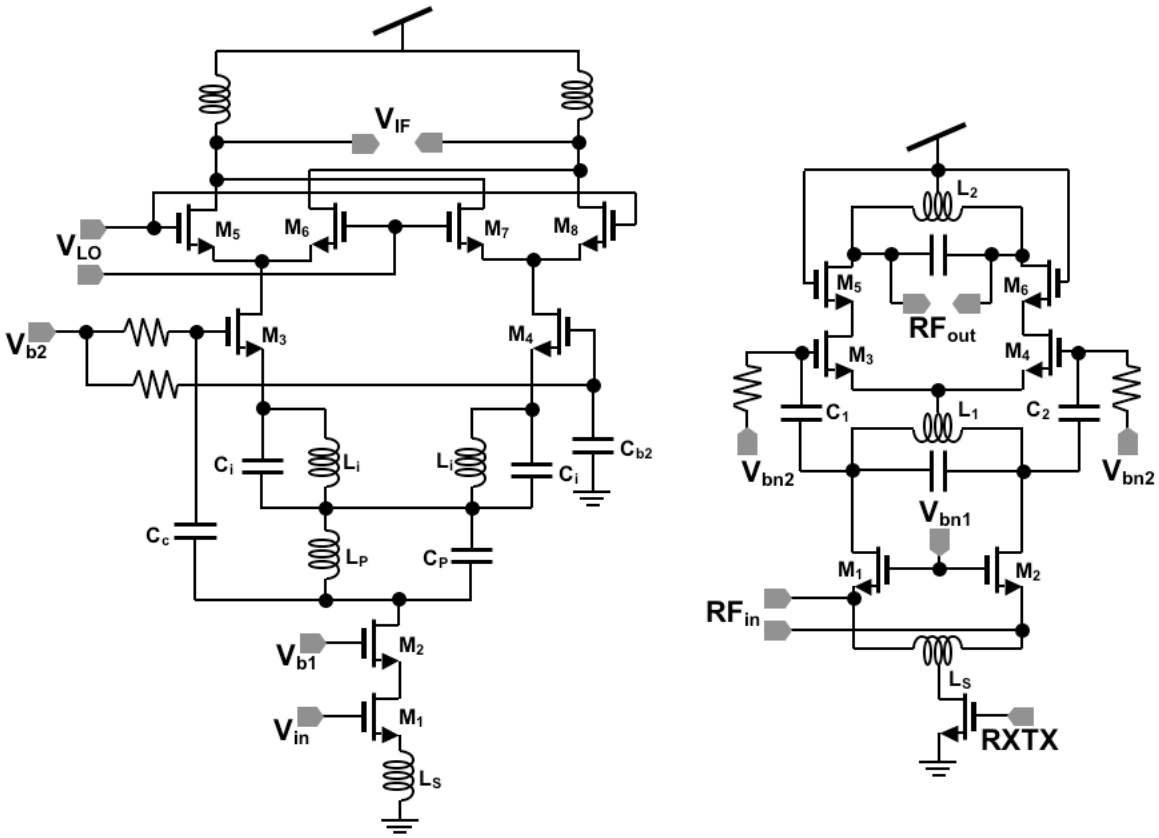
The advantage of using high-Q off-chip components is that it improves gain and noise performance in RF circuits even when the active devices are biased at very low currents [15] - [17]. However, the higher cost involved in using off-chip components usually makes this technique unattractive for LR-WPAN front-ends. When on-chip high-Q passives are integrated in the process technology, the additional processing steps and higher die area increase the cost.

2.3.2 Stacking And Current Reuse

The most commonly used circuit technique to reduce power consumption in RF front-ends has been stacking. The 2.4 GHz receiver described in [18] has the mixer stacked on top of the LNA to reuse bias currents. The LNA-mixer down conversion stack is shown in Figure 2.3a. The receiver achieves a voltage gain of 50 dB while consuming 17.5 mW of power. The noise figure of the receiver is 6 dB.

Stacking has also been used in [19] to increase the gain of the LNA by having a cascade of two stages reuse the same bias current as shown in Figure 2.3b. Transistors M_1 and M_2 form the first differential common-gate stage with load inductor L_1. The common-source cascode stage, formed by transistors M_3 to M_6 and load inductor L_2, is stacked on top of the first stage. This circuit achieves a voltage gain of 32 dB while consuming 10 mW of power.

The 1.6 GHz LMV (LNA-Mixer-VCO) cell in [20] utilizes the same current reuse technique to combine LNA, mixer, and VCO into a single stack. The 5.4 mW quadrature receiver in [20] achieves a gain of 36 dB and a noise figure of 4.8 dB. The schematic of the LMV cells in quadrature is shown in Figure 2.4.



(a) **(b)**

Figure 2.3: Schematics of front-ends using stacking: (a) LNA-Mixer in [18]. (b) 2 stage LNA in [19].

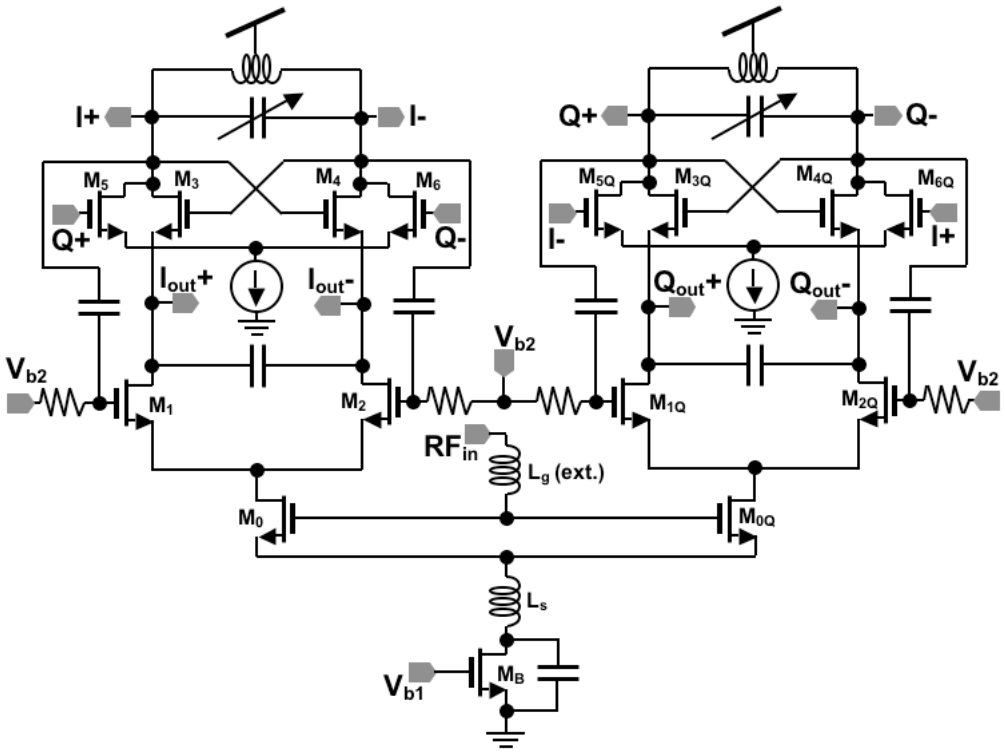


Figure 2.4: Schematic of the LNA-Mixer-VCO cells in quadrature from [20].

The disadvantage of the current reuse or stacking technique is the reduction of voltage headroom, which can lead to lower linearity. Another possible issue is higher signal leakage between the blocks stacked together.

2.3.3 Passive Mixing

Passive mixers can be used to reduce power consumption in wireless receivers. In [21], a 3.6 mW receiver is reported for 900 MHz with 30 dB voltage gain and 3 dB noise figure. It uses a cascode LNA with inductive source degeneration and a passive mixer. The schematic of the RF front-end in [21] is shown in Figure 2.5. Since passive mixing

cannot provide conversion gain, the LNA in the receiver chain is required to provide higher gain to compensate for the loss in the mixer.

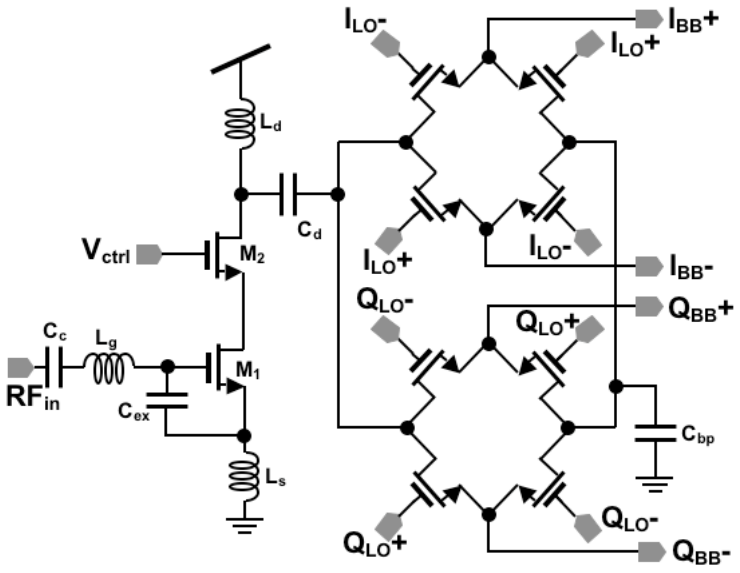


Figure 2.5: Schematic of the RF front-end in [21] with passive mixers.

A passive-only front-end described in [22] consumes 750 μW of power and has a noise figure of 5.1 dB. However, the gain achieved is limited since the only gain block in the front-end is a passive network. This can make the subsequent stages in the receiver chain dominate the overall noise figure.

2.3.4 Non-linearity Cancellation

Reducing power consumption can also make the receiver more non-linear. Linearity improvement techniques are often used to compensate for this effect. The receiver

reported in [23] consists of a cascode LNA and a mixer as shown in Figure 2.6. The mixer utilizes folded architecture and multiple gated transistor (MGTR) technique [24], also known as derivative superposition [25]. The folded structure helps both improve voltage headroom and implement a second-harmonic termination ($L_1||C_1$ in Figure 2.6) to reduce third-order harmonic components generated by second harmonic mixing. Derivative superposition works on the principle of non-linearity cancellation. In Figure 2.6, transistors M_3 and M_4 have gate-source voltages set such that the non-linearity in M_3 cancels the non-linearity in M_4.

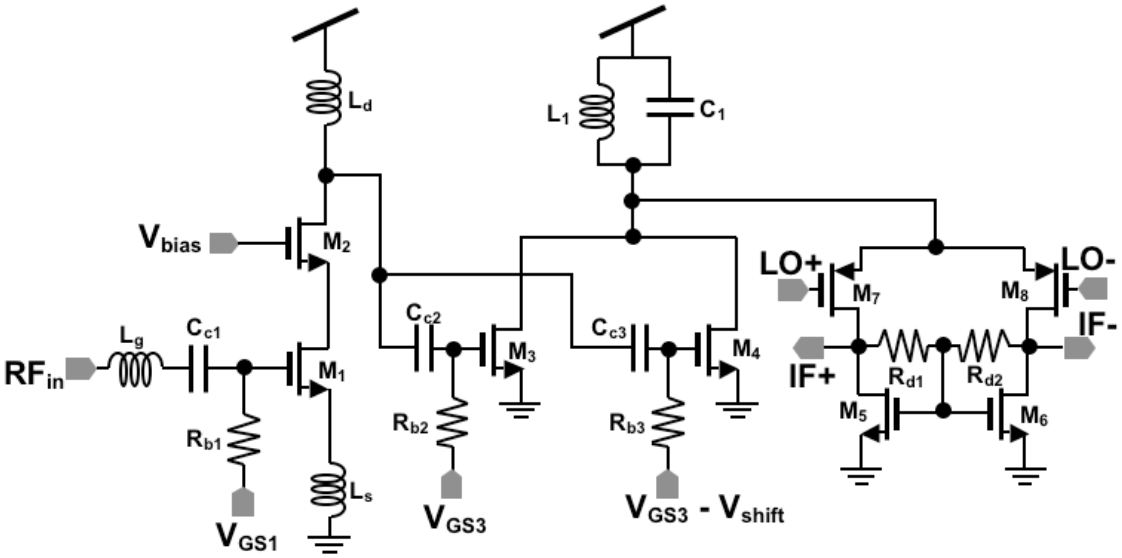


Figure 2.6: Receiver front-end in [23] showing folded mixer with MGTR.

The disadvantage of this technique is that it usually leads to a significant degradation of noise performance. Since this method is based on exact cancellation of

non-linearity, it will not be suitable for volume applications unless the cancellation is made temperature and process invariant.

2.3.5 Subthreshold Biasing

Subthreshold biasing has been used for a long time in low-frequency CMOS circuits for reducing power consumption. The same circuit technique was used for developing very low power voltage controlled oscillators in [17] and [26]. The disadvantage of this technique is the increase in phase noise in such VCOs. However, high-Q off-chip inductors can be used to improve noise performance as reported in [17]. A 45 μW mixer was also reported in [17] for 928 MHz based on subthreshold MOS transistors with a conversion gain of 12 dB. Subthreshold transistors and high-Q off-chip components were also used to develop a 450 MHz front-end in [27] consuming 110 μA of current from a 3 V supply. The receiver had a differential gain of 24 dB and a noise figure of 19.5 dB.

Subthreshold operation of CMOS transistors in multi-GHz frequency bands is explored in the next chapter with the objective of developing extremely low-power subthreshold RF front-ends.

2.4 Summary

Low IF receiver architecture offers the advantages of a direct conversion receiver while mitigating issues like DC offset, flicker noise, and LO leakage. Though the image problem reappears, image-reject quadrature down-conversion schemes can provide sufficient image rejection for many WPAN applications.

The power consumption in a wireless device is dependent on the center frequency, bandwidth, supported data rate, blocker profile, process technology, duty cycle, and digital baseband complexity. In extremely low duty cycle implementations, the off state leakage power becomes vital. Since a WPAN transceiver is rarely in the transmit mode, the power consumption in receive and sleep modes typically determines the overall power consumption of the wireless front-end. Circuit techniques like current re-use, stacking, non-linearity cancellation, passive mixing, and subthreshold biasing can be used to lower power consumption in wireless receivers.

Chapter 3
Subthreshold CMOS Circuits

While a CMOS transistor in strong inversion has square-law characteristics, a subthreshold CMOS transistor exhibits exponential characteristics similar to that of a bipolar transistor. Though extensively used in low-power analog circuits, subthreshold biasing has not been adequately explored at RF frequencies. The potential of implementing low-power RF circuits in subthreshold CMOS is investigated in this chapter.

3.1 Subthreshold MOS Operation

Subthreshold biasing is a standard circuit design technique used extensively in CMOS analog circuits to decrease power consumption [28], [29]. The main advantage of biasing a CMOS transistor in the subthreshold region is the significant increase in the transconductance to bias current ratio (g_m/I_D) when compared to the operation in strong inversion. Recently, subthreshold operation has been exploited in ultra low power digital circuits [30] - [32] by lowering the supply voltage below the threshold voltage of the transistors.

The drain current, i_D, of an NMOS transistor operating in weak inversion can be approximated by the following equation [28]:

Equation 3.1: $i_D = \frac{W}{L} I_{DO} \exp\left(\frac{v_{GS}}{n(kT/q)}\right)$,

where n is the subthreshold slope factor, I_{DO} is a process-dependent parameter, k is the Boltzmann's constant, T is the temperature (K), and q is the charge of an electron. Thus, the device characteristics change from square-law in saturation to exponential in sub-threshold. The gate-source voltage below which the transistor can be assumed to operate in subthreshold region is given approximately by:

Equation 3.2: $v_{gs,\ Subthreshold\ Limit} = V_t + n\frac{kT}{q}$

In subthreshold region, the drain current becomes relatively constant if V_{DS} is raised above 3kT/q (≈ 78 mV). The transconductance (g_m) of a transistor in strong inversion is given by:

Equation 3.3: $g_{m,strong\ inversion} = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$.

where μ_n is the electron mobility and C_{ox} is the oxide capacitance per unit area. The subthreshold transconductance, on the other hand, is independent of the aspect ratio and is given by:

Equation 3.4: $g_{m,subthreshold} = \frac{I_D}{nkT/q}$

Figure 3.1 shows the g_m of a 0.18 μm NMOS transistor when the transistor width is increased from 2.5 μm to 200 μm, with a constant bias current of 300 μA. The increase in g_m is significant as the device width is increased and one moves from the strong inversion region following Equation 3.3, to subthreshold region where Equation 3.4 is valid.

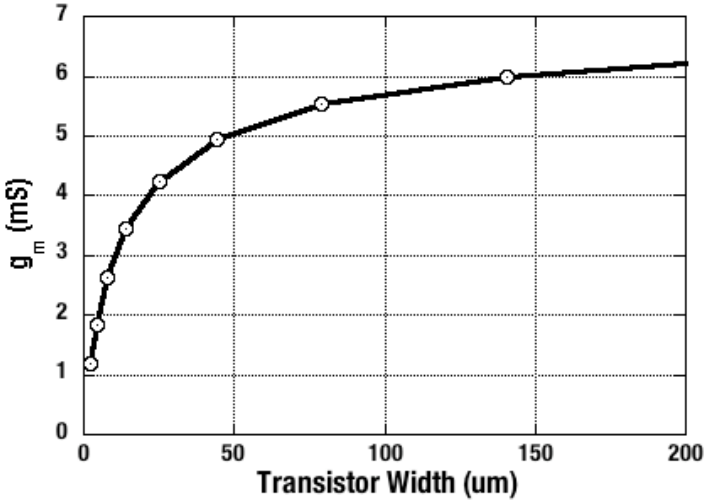


Figure 3.1: Transconductance of an NMOS transistor with 0.18 μm length (L) and a bias current of 300 μA.

The device characteristics of a subthreshold MOS transistor resemble that of a bipolar device. Hence, many of the bipolar design techniques (such as the translinear loop based current mode circuits) become relevant in subthreshold CMOS circuits. Subthreshold circuits also require lower voltage headroom, leading to easier stacking of blocks or lowering of supply voltage. The voltage swing required is also lower than that

in typical CMOS circuits: for instance, a differential pair requires only about 78 mV ($3kT/q$) for *hard switching*.

3.2 High Frequency Potential of Subthreshold Circuits in Deep Sub-micron CMOS

Technology scaling has made possible CMOS circuits operating at 100 GHz and beyond [33]. However, the improvement in subthreshold f_T with technology scaling has neither been adequately studied nor exploited. A deep sub-micron MOS device operating in weak inversion region can provide sufficient transconductance for many low power RF applications when used with suitable passive networks.

Though the g_m/I_D ratio is higher than that in strong inversion, the absolute value of transconductance is significantly lower. As can be seen from Equation 3.4, increasing W/L without changing I_D does not increase transconductance, unlike in strong inversion. However, if the current density is kept constant, g_m increases linearly with W/L. Hence, one can achieve the same transconductance for lower current by using a larger active device in the subthreshold region, resulting in extremely low-power consumption. On-chip inductors can then be used to resonate out the higher capacitances associated with the larger transistor. The higher output resistance of a subthreshold transistor can also help increase its voltage gain.

The transition frequency, f_T, is defined as the frequency at which the magnitude of the short-circuit common-source current gain falls to unity. The transition frequency of a subthreshold CMOS transistor is also much lower [34] than that of a CMOS transistor in strong inversion and is given by:

Equation 3.5: $$f_T = \frac{1}{2\pi}\frac{I_D}{(kT/q)}\frac{1}{WLC_{js}}.$$

where C_{js} is the depletion region capacitance.

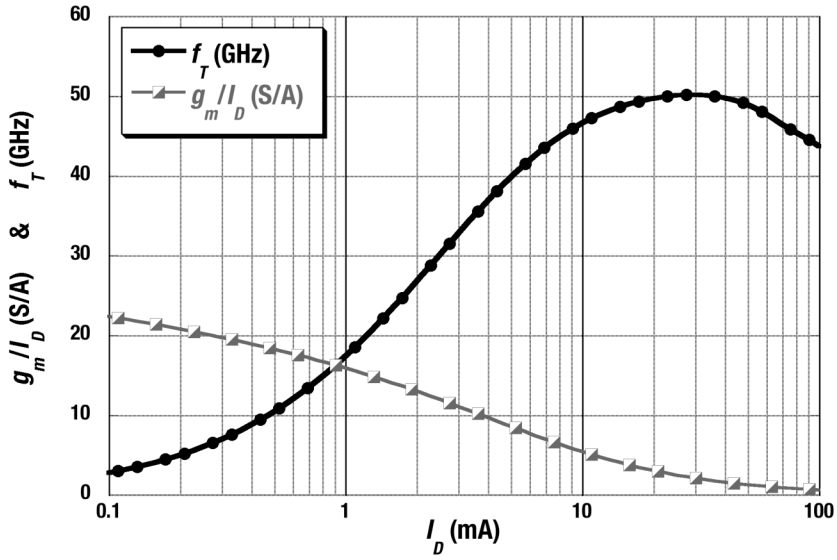


Figure 3.2: Plot of f_T and g_m/I_D of a 120 μm / 0.18 μm NMOS transistor.

The simulated f_T, and g_m/I_d are plotted in Figure 3.2 against the drain current I_D for a 120 μm / 0.18 μm NMOS transistor in a 0.18 μm process. The peak f_T of the device is 50 GHz at a bias current of 30 mA. The g_m/I_d ratio at this bias point is only 2.07. This

ratio is about an order of magnitude higher in the subthreshold region, where f_T is below 10 GHz.

Figure 3.3 shows the g_m, and r_{ds} of the same transistor plotted against the drain current I_D. The maximum transconductance of 61 mS is achieved with a bias current of 36 mA. The output resistance, r_{ds}, is about 430 Ω at this bias point. In subthreshold region, r_{ds} is in the order of 10 kΩ.

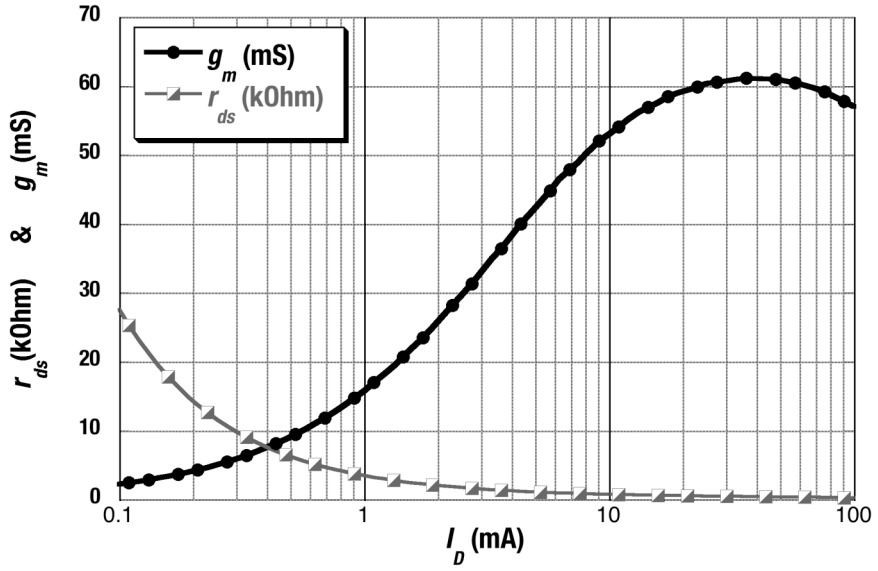


Figure 3.3: Plot of g_m and r_{ds} of a 120 µm / 0.18 µm NMOS transistor.

WPAN standards like 802.15.4 (ZigBee) operate in the 900 MHz and 2.4 GHz frequency bands and require extremely low power consumption. Subthreshold operation of deep sub-micron CMOS transistors is ideally suited for such applications. As shown in Figure 3.2, the subthreshold transition frequency is in the 5 GHz to 15 GHz range in 0.18

μm CMOS process. Technology scaling will further increase subthreshold f_T, making it possible to operate weak inversion devices in higher frequency bands like 5 GHz too.

Figure 3.4 shows the simulated transconductance to bias current ratio of NMOS transistors in 180 nm, 130 nm, 90 nm, and 65 nm CMOS processes. The simulated subthreshold transition frequencies of these devices are plotted in Figure 3.5.

Table 3.1 lists the device sizes and the V_{DS} used to generate Figure 3.4 and Figure 3.5. All the transistors are minimum length devices. However, the W/L ratios for all the devices are kept approximately equal. The drain-source voltages used are the rated supply voltages for these processes.

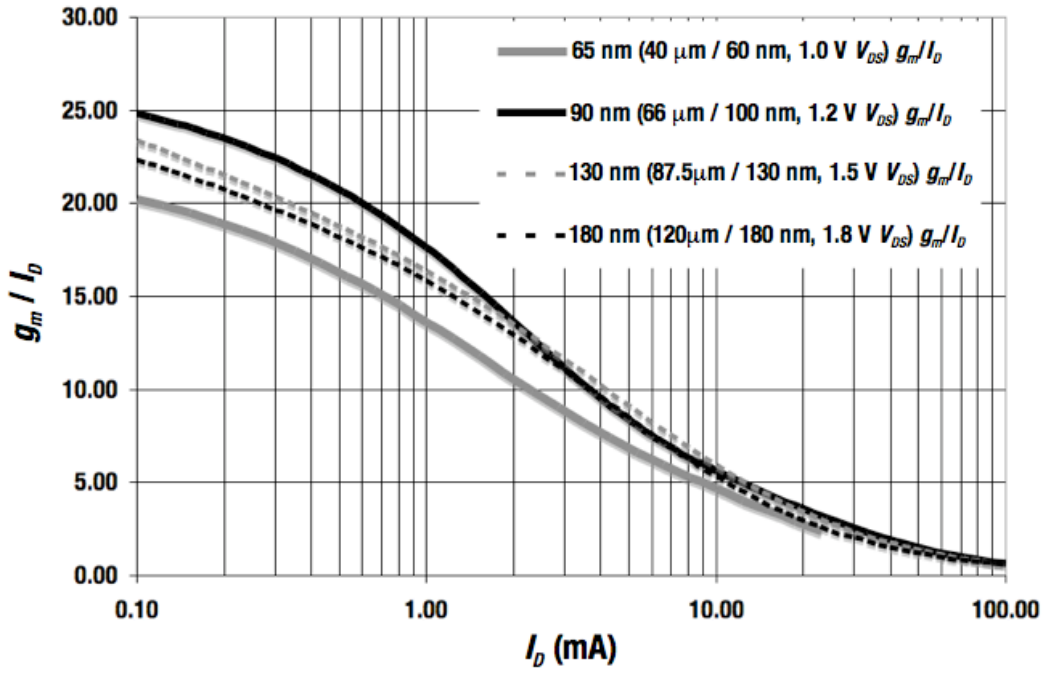


Figure 3.4: Transconductance to bias current ratio (g_m/I_D) in subthreshold and strong inversion regions across process technology nodes.

As seen in Figure 3.4, g_m/I_D increases by about an order of magnitude from strong inversion to weak inversion in all the process nodes. At a bias current of 600 μA, the subthreshold f_T of the 65 nm device is above 50 GHz, as shown in Figure 3.5. This is as high as the peak f_T of the 180 nm device in strong inversion shown in Figure 3.2.

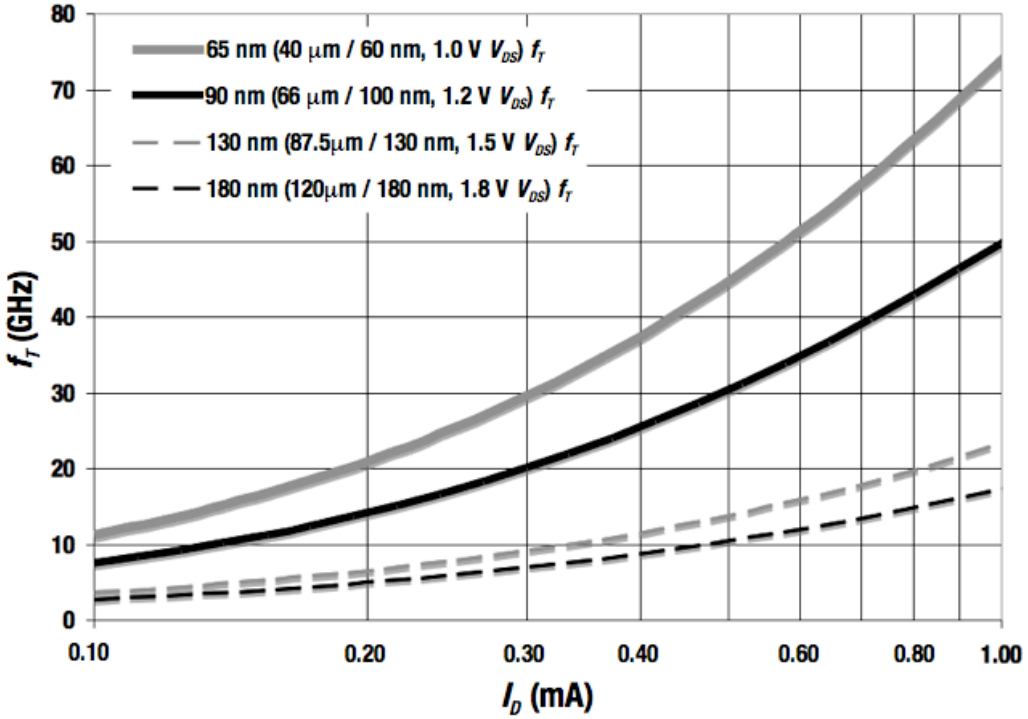


Figure 3.5: Transition frequency of subthreshold NMOS transistors across process technology nodes.

The high g_m/I_D ratio in subthreshold region can be potentially exploited to reduce the power consumption in wireless receivers in low-power applications in the future as the subthreshold f_T continues to increase with technology scaling. However, subthreshold devices have already been used in RF circuits for non-linearity cancellation [23]-[25]. Non-linearity cancellation is achieved by derivative superposition, when the g_{m3}

($\delta^3 I_D/\delta V^3_{GS}$) of an auxiliary subthreshold transistor cancels that of the main strong-inversion transistor.

Table 3.1: Device sizes and bias conditions used to generate Figure 3.4 and Figure 3.5.

Process	Device Width	Device Length	W/L	V_{DS}
180 nm CMOS	120 μm	180 nm	667	1.8 V
130 nm CMOS	87.5 μm	130 nm	673	1.5 V
90 nm CMOS	66 μm	100 nm	660	1.2 V
65 nm CMOS	40 μm	60 nm	667	1.0 V

3.3 Noise in Subthreshold CMOS Transistors

Besides the reduced transconductance, subthreshold CMOS transistors also suffer from higher device noise. However, circuit techniques like passive voltage amplification can be used to improve noise performance of subthreshold RF circuits. High frequency noise performance in subthreshold devices has not been studied extensively since the extremely low transition frequency in earlier process nodes made the implementation of high frequency subthreshold circuits virtually impossible. Widely used commercial models like BSIM4 [35] and Philips MOS11 [36] do not predict the noise in subthreshold devices accurately [37].

The channel noise, proportional to g_m, is the dominant device noise in strong inversion. As the gate-source voltage (v_{GS}) is lowered below the threshold voltage, the induced gate noise starts to dominate the overall device noise. NF_{min} is a few dB higher in subthreshold region due to the high induced gate noise [37]. Unlike what is predicted by most of the existing models, the subthreshold NF_{min} saturates after increasing by a few dB as v_{GS} is lowered below threshold voltage.

Circuit techniques like passive voltage pre-amplification will have to utilized to exploit the low-power potential of deep sub-micron subthreshold CMOS for WPAN receiver implementations without significantly compromising sensitivity.

3.4 Summary

Along with the strong-inversion f_T, the subthreshold f_T is also increasing with technology scaling and is now high enough to support numerous power-sensitive wireless applications. However, subthreshold biasing has not been adequately utilized in RF circuits yet. The high g_m/I_D ratio and the high output impedance can be exploited at RF frequencies to develop extremely low power wireless front-end blocks. Transistors in weak inversion have higher noise than in strong inversion. Circuit techniques like passive voltage pre-amplification can be used in conjunction with subthreshold devices to implement low-power receivers with sufficient sensitivity for WPAN applications.

Chapter 4

Micro-Power Wireless Front-End Blocks

4.1 Introduction

Low-power circuit techniques like subthreshold biasing and stacking are used to develop wireless front-end blocks requiring less than 1 mW of power consumption. A micro-power CMOS LNA [38] is presented based on subthreshold MOS operation in the GHz range. The LNA is fabricated in a 0.18 μm CMOS process and has a gain of 13.6 dB at 1 GHz while drawing 260 μA from a 1 V supply. An unrestrained bias technique, that automatically increases bias currents at high input power levels, is used to raise the input P1dB to –0.2 dBm. The LNA has a measured noise figure of 4.6 dB and an IIP3 of 7.2 dBm.

Novel subharmonic mixing techniques are presented next, based on threshold voltage modulation using signal injection at the bulk or source terminal of CMOS transistors. A 2.1 GHz subharmonic bulk-driven mixer [39] is designed by applying LO signals at the bulk terminal of PMOS transistors. The mixer has a measured conversion gain of 10.5 dB, an IIP3 of –3.5 dBm, and a noise figure of 17.7 dB while consuming 2.5 mW in each mixer core. The bulk-driven mixer architecture increases the second harmonic LO-to-RF isolation to above 67 dB and hence can mitigate LO leakage issues in wireless receivers. A micro-power mixer core based on shifted anti-symmetric transfer characteristics of an active anti-parallel diode pair is used to develop both 1X and 2X

mixers operating at less than 460 μW and having measured conversion gains of 9.7 dB and 7 dB, respectively, at 2.5 GHz.

A CMOS VGA cell is also implemented, combining two independent gain control circuits to obtain 40dB and 50dB (dB-linear) gain ranges at 250μW and 1.75mW power consumption, respectively [40].

4.2 Subthreshold Low Noise Amplifier

As explained in the last chapter, subthreshold CMOS transistors in deep sub-micron technologies can be utilized to develop extremely low-power RF circuits. However, subthreshold biasing of RF circuits has not been adequately explored in the past. A subthreshold LNA is designed for 1 GHz in 0.18 μm CMOS process to demonstrate micro-power RF circuit implementation using weak inversion devices.

4.2.1 Design and Implementation of 1 GHz Subthreshold LNA

Compared to the usual strong inversion operation, a MOS transistor operating in weak inversion has a lower transconductance and a lower f_T. In this design, transconductance is increased by using minimum length devices with larger width. The effect of the capacitances associated with such devices of large widths is reduced by using on-chip tuning networks so that adequate transconductance is obtained at 1 GHz. A

high impedance tuned load, obtained by parallel resonance of the load inductor with the total output node capacitance at the operating frequency, helps further improve the voltage gain to 13.6 dB.

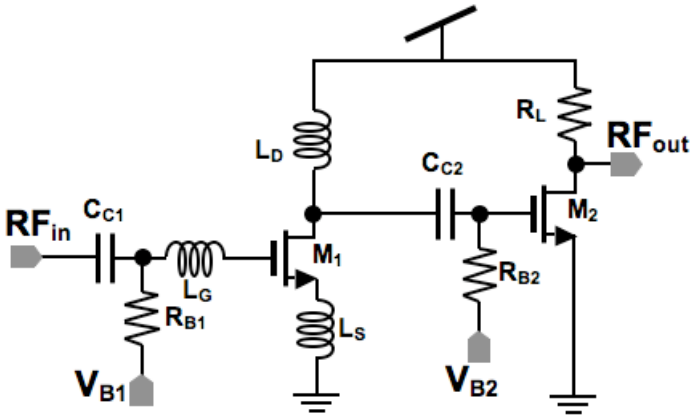


Figure 4.1: Schematic of the 1 GHz subthreshold LNA and output buffer.

Figure 4.1 shows the schematic of the 1 GHz subthreshold LNA. An output buffer is also included for facilitating characterization. Cascode architecture is avoided to operate at a low supply voltage. The 600-μm/0.18-μm NMOS device labeled M_1, operates in the weak inversion region and has a transconductance of 6.3 mS at 260 μA. The device size and bias point are so selected to obtain sufficient transconductance at minimal associated capacitances. The source degeneration inductor L_S and the inductor L_G provide input matching while inductor L_D is used as the high impedance resonant load.

As discussed earlier, transistor noise in weak inversion region is higher than that in strong inversion. Thus the noise figure of a subthreshold CMOS LNA is expected to be

higher than the strong inversion CMOS LNA. This effect is partially mitigated by having a significant voltage gain in the passive input matching network.

Circuits operating at very low bias currents are expected to have poor linearity. If the bias current was restrained, say by using a current sink in a differential LNA, then the subthreshold circuit would have a poor P1dB. However in the case of unrestrained bias, the bias current increases as the input power is increased. This is because the positive half cycle of the drain current is larger than the negative half cycle at higher input power levels. The increased current consumption compensates for gain compression, providing the same gain even at high input power levels, leading to higher linearity of the LNA. The effects of the drain current harmonics are reduced by using a tuned load.

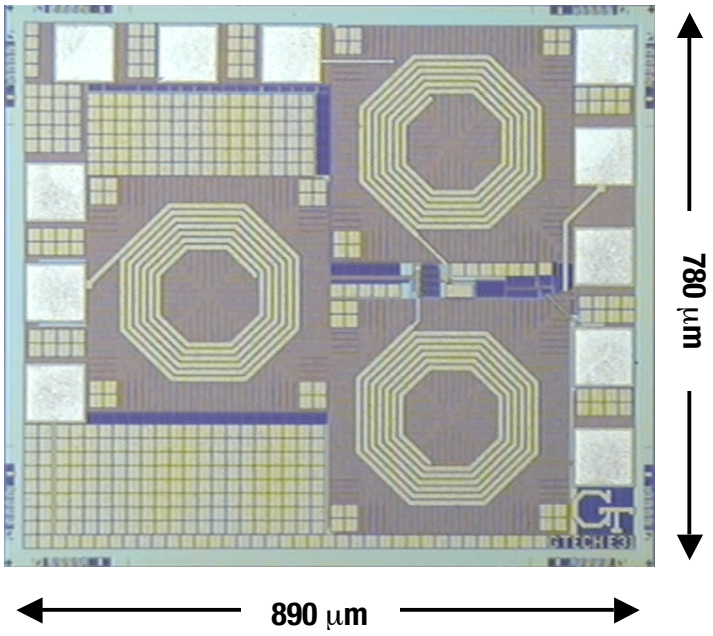


Figure 4.2: Die micrograph of the 1 GHz subthreshold LNA.

The LNA is fabricated in a standard digital 0.18 μm CMOS process. The microphotograph of the 890 μm x 780 μm chip is shown in Figure 4.2. The LNA uses on-chip inductors with patterned ground shield. These inductors have quality factors of approximately 4 at 1 GHz with self-resonant frequencies about 4 GHz. While the inductors are fabricated in the top metal layer with a thickness of 0.86 μm, the patterned ground shield is implemented in the first metal layer.

4.2.2 Measurement Results of the 1 GHz Subthreshold LNA

All measurements were performed using an on-wafer probe station. Since the output node of the LNA is a high impedance node, an output buffer was used for measurements. A simulation model of the buffer using its measured output impedance and bias settings was used to evaluate its gain, noise, and linearity performances so as to de-embed its effects on the LNA. The measured S-parameters are shown in Figure 4.3. The peak gain of 13.6 dB is obtained at 980 MHz with a 3-dB bandwidth of 160 MHz. S_{11} can be further improved by modifying the inductors used for input matching.

The noise figure of the LNA is 4.6 dB at 980 MHz. As shown in Figure 4.4, the noise figure values are evaluated using the measured noise figure of the LNA and the buffer, the LNA gain, and the buffer noise. The LNA and output buffer together has an IIP3 of –3 dBm as shown in Figure 4.5, and an input 1-dB compression point of –13 dBm as shown in Figure 4.6. The increase in current drawn from the supply with increase in input power is also plotted in Figure 4.6. After accounting for the non-linearity of the

output buffer, the input P1dB of the LNA is evaluated as –0.2 dBm and the IIP3 is evaluated as 7.2 dBm. The gain variation with supply voltage was also studied while maintaining the bias current at 260 μA. As plotted in Figure 4.7, this LNA has a gain above 12 dB with supply voltages as low as 0.5 V (130 μW power consumption).

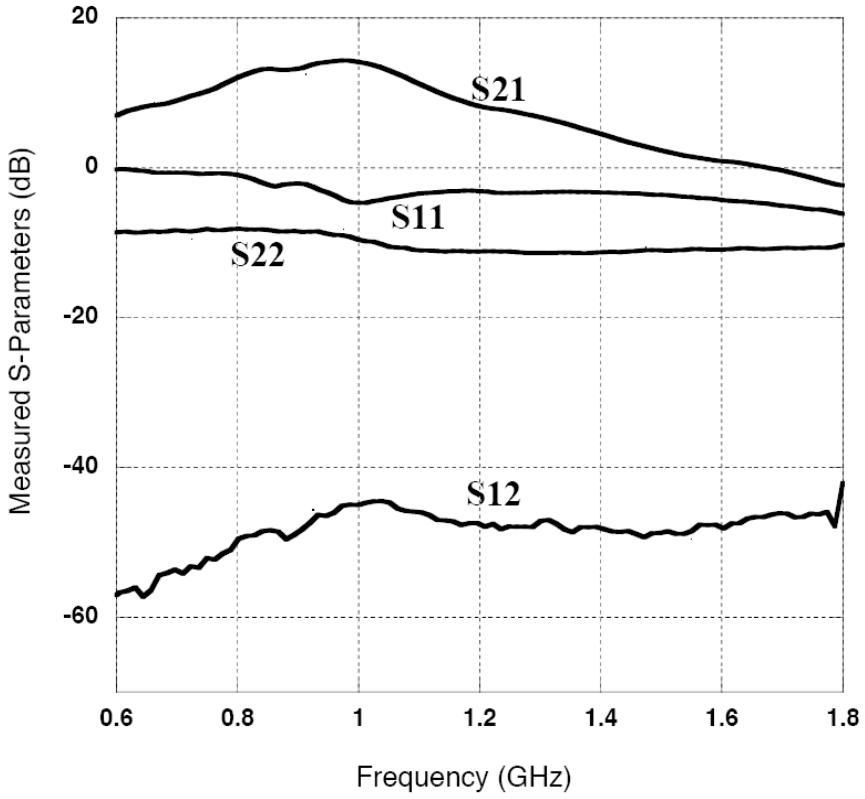


Figure 4.3: Measured S-parameters of the subthreshold LNA.

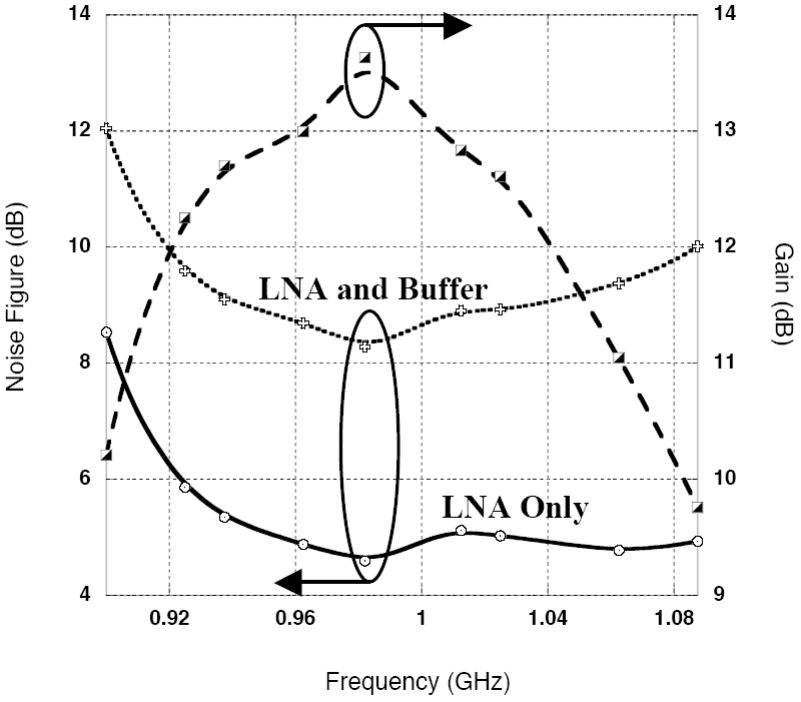


Figure 4.4: Measured noise figure of the LNA and output buffer.

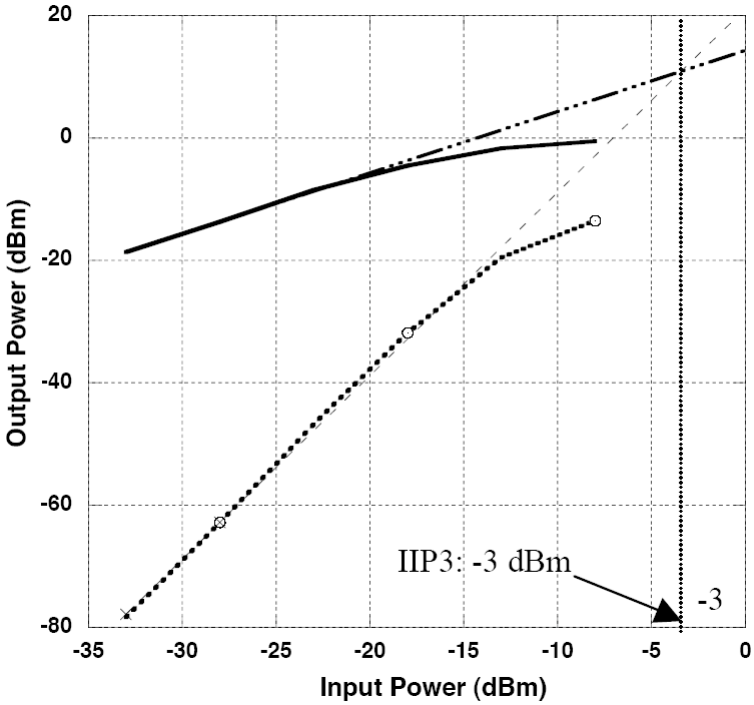


Figure 4.5: Measured input IP3 of the subthreshold LNA and output buffer.

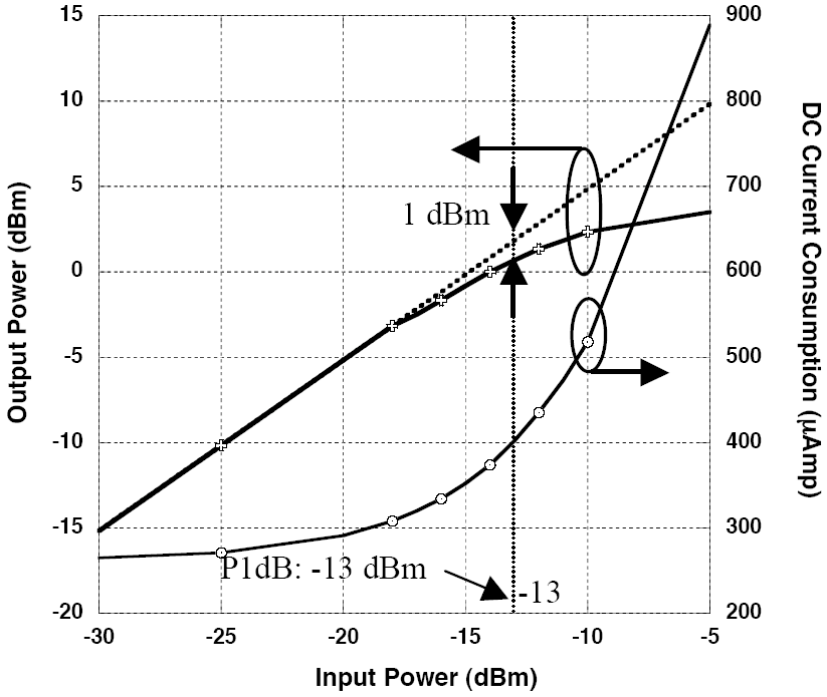


Figure 4.6: Measured input 1-dB compression point of the subthreshold LNA and output buffer. Also plotted is the increase in bias current with input power due to unrestrained biasing.

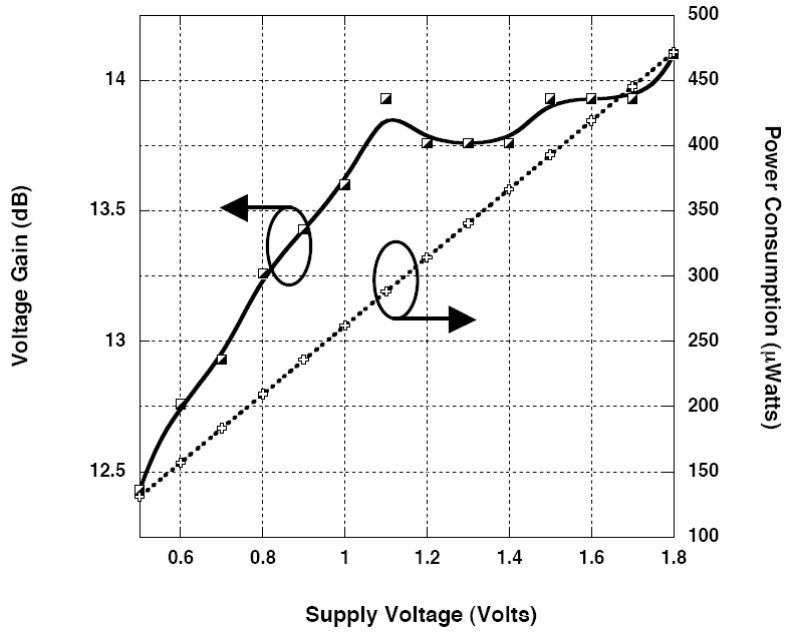


Figure 4.7: Gain and power consumption variation with supply voltage. Bias current is maintained at 260 μA.

4.3 CMOS Mixers for Low-Power Applications

Self-mixing, dc-offsets, and other local oscillator signal leakage issues in direct conversion receivers have led to a renewed interest in subharmonic mixers. Subharmonic mixer architectures use second or higher order harmonics of the LO signal for up or down conversion. In many cases, a lower LO frequency can significantly simplify transceiver design, especially of functional blocks such as frequency synthesizers, oscillators, and buffers. Hence sub-harmonic mixers can be used to build integrated RF front-ends for very high frequencies. These mixers can help make the transceiver less susceptible to LO pulling and are also suited for building multi-standard systems sharing a common LO signal generation scheme.

Numerous subharmonic mixers have been developed based on diode nonlinearity [41], [42]. However, such mixers do not have conversion gain and require high LO power, isolator blocks, and filters making them difficult to integrate. Subharmonic mixers have also been implemented based on poly-phase LO switching [43]-[45], but such circuits have lower voltage headroom and are not suited for supply voltage down scaling. Requirement of poly-phase LO signals with low phase mismatch is another disadvantage of these circuits. Two novel subharmonic CMOS mixers based on threshold voltage modulation are presented. While the anti-parallel diode pair (APDP) based mixer is suitable for very low-power applications, the bulk driven mixer using threshold voltage modulation provide higher LO-to-RF isolation and thus help mitigate LO leakage issues.

4.3.1 Subharmonic Mixing Using Threshold Voltage Modulation

The threshold voltage of a MOSFET can be modulated by signal injection in either the bulk or the source terminal. While the bulk terminal is used for applying LO signal in the bulk driven mixer, the active APDP mixer core involves signal injection in the source terminal. Both mixers essentially operate using threshold voltage modulation and have similar expressions for conversion gains as shown next.

Consider a single NMOS transistor with a grounded source and with v_G, v_D, and v_B as the voltages at gate, drain, and bulk, respectively. For simplicity, the device current in saturation region, i_D, can be expressed as

Equation 4.1: $i_D = \beta(v_{GS} - v_t)^2(1 + \lambda v_{DS})$,

where β is the transconductance parameter, v_{GS} is the gate-source voltage, v_t is the threshold voltage, λ is the channel length modulation parameter, and v_{DS} is the drain-source voltage. The threshold voltage, v_t, is given by

Equation 4.2: $v_t = v_{t0} + \gamma\left(\sqrt{2\phi_f + v_{sb}} - \sqrt{2\phi_f}\right)$,

where v_{t0} is the threshold voltage with v_{SB} (source-bulk voltage) set to zero, ϕ_f is the Fermi level, and γ is a process dependent parameter.

Using Equation 4.2, the following can be derived:

Equation 4.3: $$(v_{GS} - v_t)^2 = \left(v_{GS} - v_{t0} - \gamma\sqrt{2\phi_f}\left(\sqrt{1 + \frac{v_{SB}}{2\phi_f}} - 1\right)\right)^2 .$$

Using Taylor Series expansion for $\sqrt{1 + \frac{v_{SB}}{2\phi_f}}$, we get

Equation 4.4: $$(v_{GS} - v_t)^2 = \left(v_{GS} - v_{t0} - \gamma\sqrt{2\phi_f}\left(\begin{array}{l} \frac{1}{2}\left(\frac{v_{SB}}{2\phi_f}\right) - \frac{1}{8}\left(\frac{v_{SB}}{2\phi_f}\right)^2 \\ + \frac{1}{16}\left(\frac{v_{SB}}{2\phi_f}\right)^3 + \ldots \end{array}\right)\right)^2 .$$

Equation 4.4 is of the form $(\alpha - \beta)^2$ and it is the product term, $2\alpha\beta$, which is of interest since it represents mixing of the two signals.

Equation 4.5: $$\text{Product term} = 2(v_{GS} - v_{t0})\gamma\sqrt{2\phi_f}\left(\begin{array}{l} \frac{1}{2}\left(\frac{v_{SB}}{2\phi_f}\right) - \frac{1}{8}\left(\frac{v_{SB}}{2\phi_f}\right)^2 \\ + \frac{1}{16}\left(\frac{v_{SB}}{2\phi_f}\right)^3 - \ldots \end{array}\right)$$

Equation 4.5 shows that if a local oscillator signal is applied at the bulk, sub-harmonic mixing is easily achieved. The relative conversion gain levels for different harmonic mixing cases can be obtained from Equation 4.5.

Suppose the dc bias voltage of the gate is $A'_1 + v_t$, and the RF signal applied at the gate is $B'_1 \cos(\omega_{RF} t)$. Then

Equation 4.6: $\left(v_{GS} - v_t\right) = A'_1 + B'_1 \cos(\omega_{RF} t) = \dfrac{A_1 + B_1 \cos(\omega_{RF} t)}{2\gamma\sqrt{2\phi_f}}$,

where $A_1 = A'_1 \times (2\gamma\sqrt{2\phi_f})$, and $B_1 = B'_1 \times (2\gamma\sqrt{2\phi_f})$.

Similarly when the LO signal, $B'_2 \cos(\omega_{LO} t)$, is applied at the bulk with a dc bias voltage of A'_2,

Equation 4.7: $v_{SB} = -A'_2 - B'_2 \cos(\omega_{LO} t) = \left(A_2 + B_2 \cos(\omega_{LO} t)\right) 2\varphi_f$,

where $A_2 = -A'_2 / (2\phi_f)$, and $B_2 = -B'_2 / (2\phi_f)$.

Equation 4.5 to Equation 4.7 can be used to derive the following mixing terms:

Equation 4.8: $1X: \ \dfrac{1}{4} B_1 B_2 \cos\left\{(\omega_{RF} \pm \omega_{LO}) t\right\}$

Equation 4.9: $2X: \ \dfrac{1}{32} B_1 \left(B_2\right)^2 \cos\left\{(\omega_{RF} \pm 2\omega_{LO}) t\right\}$

Equation 4.10: $3X: \ \dfrac{1}{128} B_1 \left(B_2\right)^3 \cos\left\{(\omega_{RF} \pm 3\omega_{LO}) t\right\}$

The bulk driven subharmonic mixer design is based on Equation 4.9.

Threshold voltage modulation based on signal injection in the source terminal can also be used for subharmonic mixing. Consider an NMOS transistor biased in saturation region, having a signal at frequency ω_1 ($B_3'\cos(\omega_1 T)$ with dc bias voltage A'_3) applied to the gate and another signal at frequency ω_2 ($B_4'\cos(\omega_2 T)$ with dc bias voltage A'_4) applied to the source. Therefore,

Equation 4.11: $$v_G = A'_3 + B'_3\cos(\omega_1 t) = \frac{A_3 + B_3\cos(\omega_1 t)}{2\gamma\sqrt{2\phi_f}},$$

and

Equation 4.12: $$v_S = A'_4 + B'_4\cos(\omega_2 t) = \left(A_4 + B_4\cos(\omega_2 t)\right)2\phi_f,$$

where $A_3 = A'_3 \times (2\gamma\sqrt{2\phi_f})$, $B_3 = B'_3 \times (2\gamma\sqrt{2\phi_f})$, $A_4 = A'_4/(2\phi_f)$, and $B_4 = B'_4/(2\phi_f)$.

Using Equation 4.1 - Equation 4.3, and Taylor Series expansion as before, we get

Equation 4.13: $$(v_{GS} - v_t)^2 = \left(v_G - v_S - v_{t0} - \gamma\sqrt{2\phi_f}\left(\frac{1}{2}\left(\frac{v_S}{2\phi_f}\right) - \frac{1}{8}\left(\frac{v_S}{2\phi_f}\right)^2 + \frac{1}{16}\left(\frac{v_S}{2\phi_f}\right)^3 + \ldots\right)\right)^2.$$

Equation 4.13 is similar to Equation 4.4, and has the following product term representing mixing of the two signals.

Equation 4.14:

$$\text{Product terms} = 2v_G v_S + 2(v_G - v_S - v_{t0})\gamma\sqrt{2\phi_f}\left(\begin{array}{l}\frac{1}{2}\left(\frac{v_S}{2\phi_f}\right) - \frac{1}{8}\left(\frac{v_S}{2\phi_f}\right)^2 \\ + \frac{1}{16}\left(\frac{v_S}{2\phi_f}\right)^3 - \ldots\end{array}\right).$$

Substituting Equation 4.11 and Equation 4.12 in Equation 4.14 gives the following mixing terms:

Equation 4.15: $$1X: \left(\frac{\sqrt{2\phi_f}}{2\gamma} + \frac{1}{4}\right)B_3 B_4 \cos\{(\omega_1 \pm \omega_2)t\},$$

Equation 4.16: $$2X: \frac{1}{32}B_3(B_4)^2 \cos\{(\omega_1 \pm 2\omega_2)t\}, \text{ and}$$

Equation 4.17: $$3X: \frac{1}{128}B_3(B_4)^3 \cos\{(\omega_1 \pm 3\omega_2)t\}.$$

Equation 4.15 for 1X mixing has an additional term, $(\sqrt{2\phi_f}/(2\gamma))B_3 B_4 \cos\{(\omega_1 \pm \omega_2)t\}$, because, unlike the bulk driven mixer, the source terminal of the transistor is not at small signal ground. The active APDP mixer core operation is based on Equation 4.15 and Equation 4.16.

4.3.2 Bulk Driven Subharmonic Mixer

The bulk terminal in MOS transistors has been used earlier for designing low-voltage bulk driven circuits [46] - [48]. However the inherent non-linearity involved in such circuits has not been exploited for designing subharmonic mixers. As shown in Equation 4.8 - Equation 4.10, the device current will have components obtained as a result of mixing of the signal applied at gate with the harmonics of the signal applied at bulk. Hence the RF input is applied at the gate and the LO signal is applied at the bulk for subharmonic mixing.

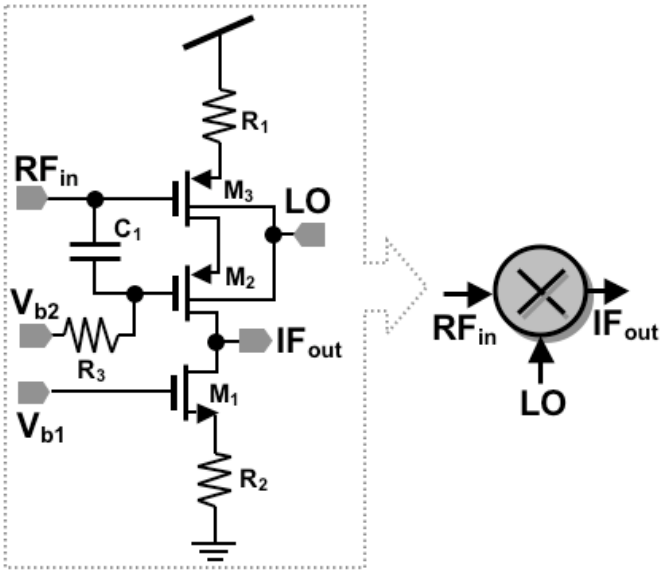


Figure 4.8: Schematic of the bulk driven mixer core.

Based on the theory described in the last section, a subharmonic bulk mixer is designed in a standard n-well CMOS process. In such a process, only PMOS transistors have isolated bodies and therefore only PMOS transistors are used for subharmonic

mixing. The schematic diagram of the basic subharmonic mixer core is shown in Figure 4.8. Resistor R2 and the cascode of PMOS transistors with resistor R1 increase output impedance and therefore improve conversion gain. Resistor R1 also improves linearity by resistive degeneration. Figure 4.9 shows the block diagram of the mixer. An output buffer is also included to facilitate measurements.

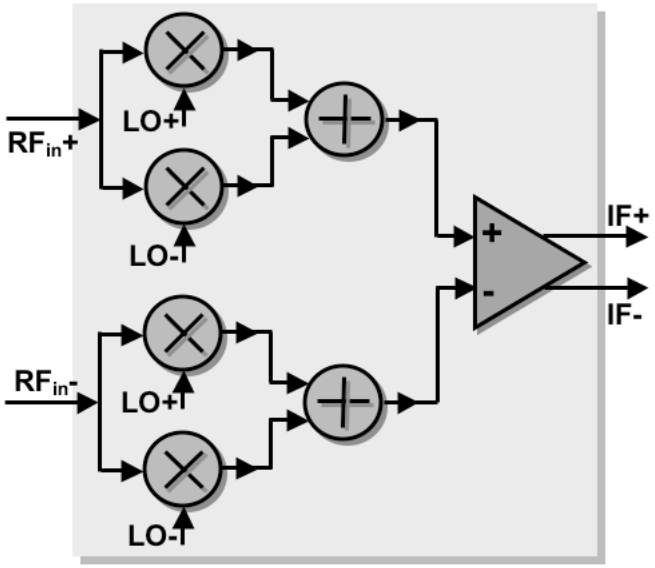


Figure 4.9: Block diagram of the subharmonic bulk mixer using the bulk mixer cores shown in Figure 4.8.

Since the LO signal is applied at the bulk, which has a lower capacitive coupling to the RF port, the LO-to-RF isolation is high. This is further improved by the architecture of the mixer, where the differential LO signals coupled to the RF port cancel each other. The LO fundamental is suppressed by more than 35 dB at the RF port while the vital second harmonic of the LO signal is suppressed by more than 67 dB in measurements.

The subharmonic mixer is fabricated in a standard digital 0.18 μm CMOS process. On-chip inductors are used to match the RF and LO ports to 50 Ω.

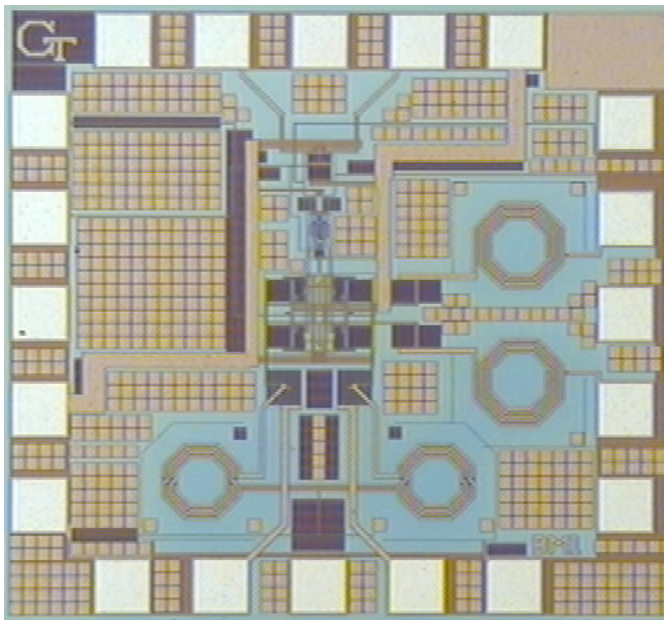


Figure 4.10: Die micrograph of the bulk driven mixer.

The microphotograph of the die is shown in Figure 4.10. All measurements of the bulk driven subharmonic mixer were performed using on-wafer probe stations. At the rated RF frequency of 2.1 GHz, the measured conversion gain is 10.5 dB. However, the peak conversion gain obtained was 13 dB at 2.9 GHz, with a 3-dB bandwidth of 1.5 GHz between 2 GHz and 3.5 GHz. The measured conversion gain is plotted across frequency in Figure 4.11. The conversion gain plotted in Figure 4.11 is obtained when the balanced LO signal powers are at 6 dBm each. The variation of conversion gain with LO power was measured and is plotted in Figure 4.12. As shown in Figure 4.12, the optimum LO power is 6 dBm.

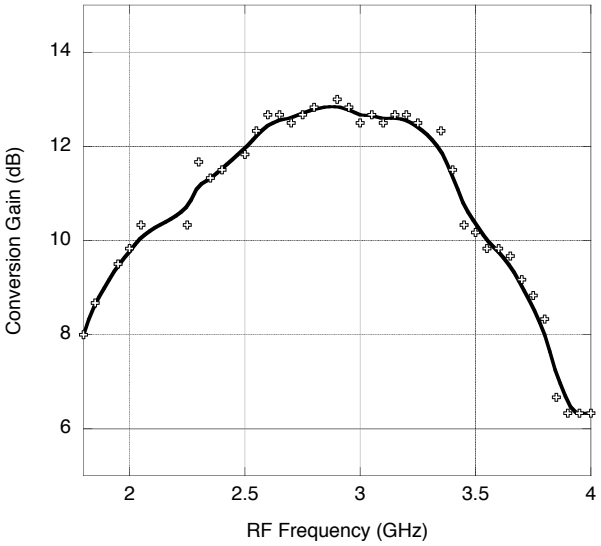


Figure 4.11: Measured conversion gain of the bulk driven subharmonic mixer.

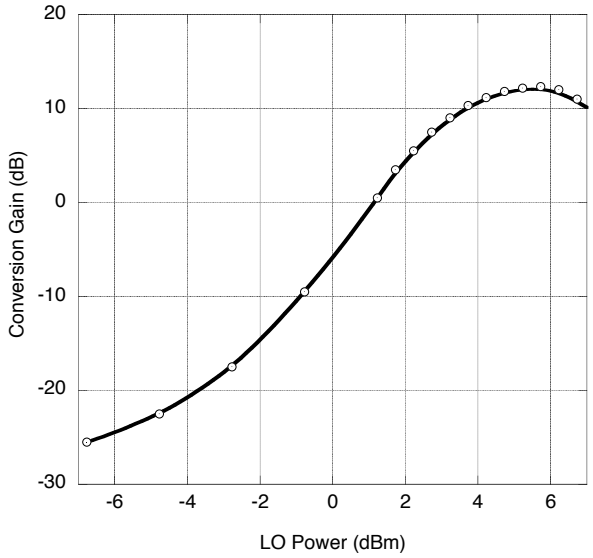


Figure 4.12: Conversion gain of the bulk mixer plotted against the LO power.

Each of the basic subharmonic mixer core, shown in Figure 4.8, operates at 1 mA. The total power consumed by the four mixer cores and the differential amplifier at the output is 12.5 mW. The mixer has a measured input 1-dB compression point of –12 dBm and an IIP3 of –3.5 dBm as shown in Figure 4.13 and Figure 4.14, respectively.

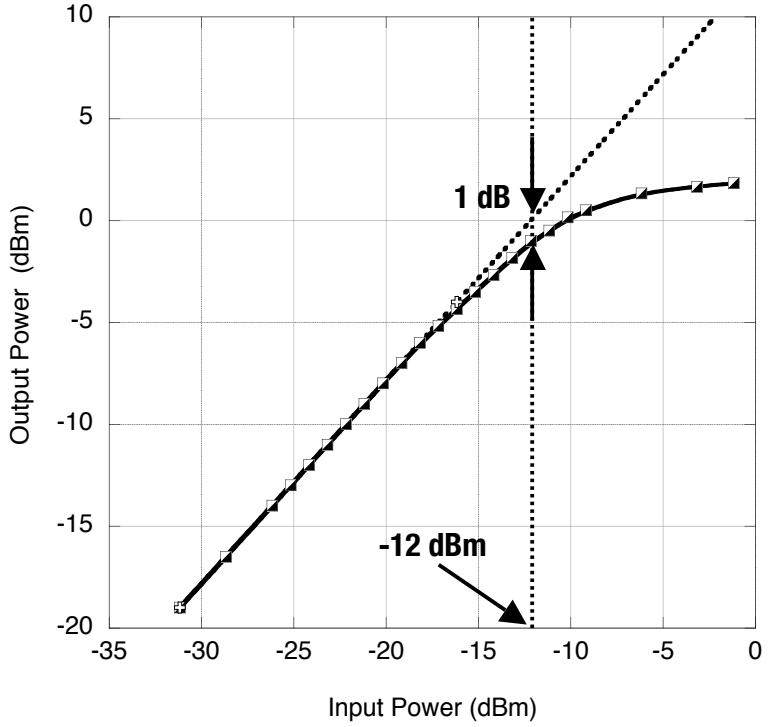


Figure 4.13: Input 1 dB compression point of the bulk mixer.

The measured noise figure of the subharmonic mixer and the output buffer is 19 dB as shown in Figure 4.15. After accounting for the noise added by the buffer, the noise figure of the subharmonic mixer is found to be 17.7 dB. The LO-to-RF isolation is also measured and found to be 35.2 dB for the fundamental (1.025GHz) and 67.1 dB for the more important second harmonic at 2.05 GHz. The novel mixer architecture presented here is suited for mitigating LO leakage issues especially in direct conversion receivers.

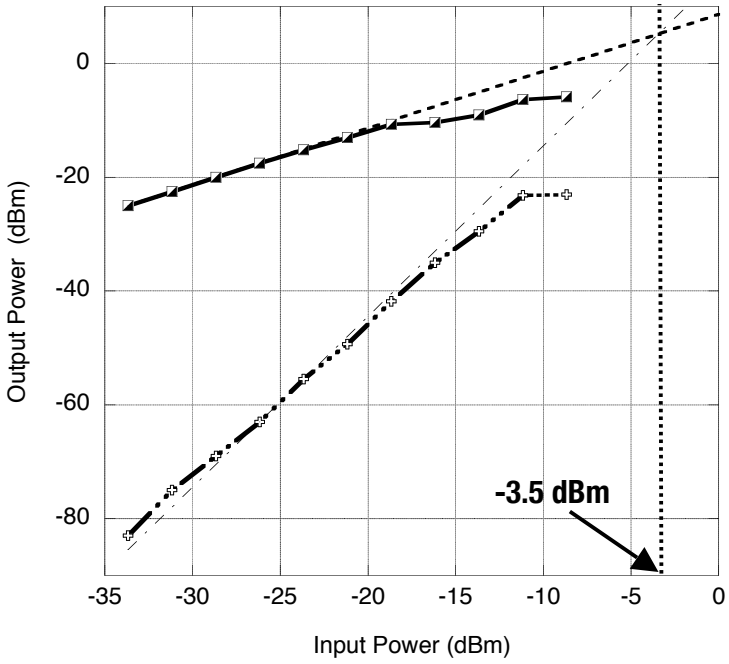


Figure 4.14: Input IP3 of the bulk driven mixer.

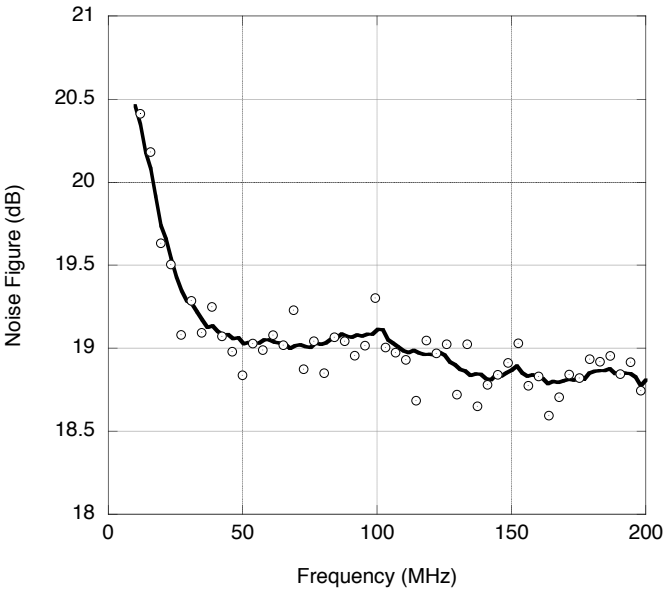


Figure 4.15: Measured noise figure of the bulk driven subharmonic mixer.

4.3.3 Active APDP Subharmonic Mixer

An APDP (anti-parallel diode pair) achieves harmonic mixing by using the non-linear characteristics of the anti-parallel diode pair. Similarly, the active APDP mixer core, shown in Figure 4.16, utilizes transistors connected in an anti-parallel scheme using coupling capacitors to perform 1X and 2X mixing using Equation 4.15 and Equation 4.16, respectively.

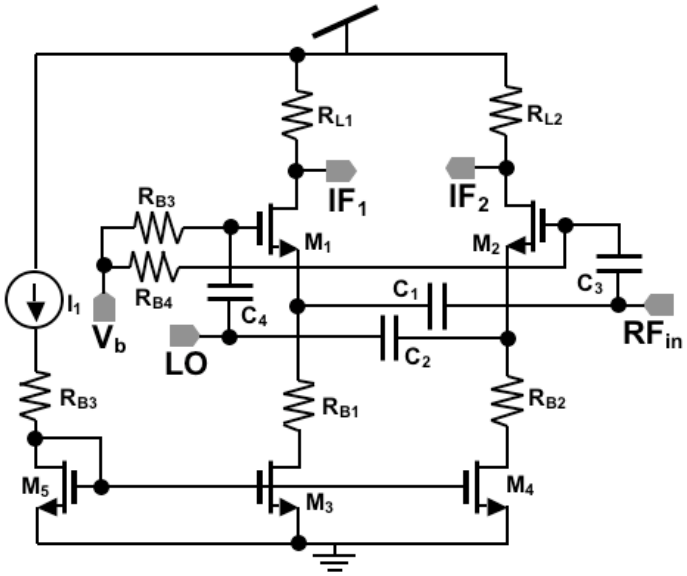


Figure 4.16: Schematic of the active APDP mixer.

In an active APDP, it is possible to connect the third terminal of the active devices to suitable load impedances and obtain conversion gain. The active APDP mixing technique avoids stacking of transistors and hence is suitable for low voltage operation. It alleviates the headroom issues associated with the supply voltage scaling that are prevalent in doubler based subharmonic mixers [43] - [45]. It does not require a large LO

drive and also provides conversion gain unlike passive mixers. The transistors in the mixer core are biased in the vicinity of the threshold level, which ensures very low power consumption. The mixer core can support higher order harmonic mixing as shown in section 4.3.1.

The transistors M_1 and M_2 form the active anti-parallel pair with anti-symmetric characteristics. In order to avoid loss of signal swing in the *dead-zone*, the transfer characteristics are shifted by using appropriate bias voltages as shown in Figure 4.16. This facilitates harmonic mixing at much lower LO voltage swing, implying a lower LO power requirement in the mixer core. On-chip matching networks are used to match the RF and LO ports to 50 Ω. The outputs IF_1 and IF_2 are summed using a summing buffer for 1X mixing while a differential buffer is used for 2X mixing. Capacitors C_1-C_4 are coupling capacitors that bring the LO and RF signals to the gate and source terminals of the transistors M_1 and M_2. The active APDP mixer is implemented in a standard digital 0.18 μm CMOS process. The microphotograph of the fully integrated active APDP based mixer is shown in Figure 4.17.

The conversion gain of the active APDP mixer is plotted against the LO power in Figure 4.18 for both 1X and 2X mixing cases. The variation of conversion gain and LO isolation with RF frequency is plotted in Figure 4.19. LO isolation is above 20 dB for both 1X and 2X mixers at 2.5 GHz. The input 1dB compression points of the active APDP mixers are found to be –9.5 dBm for 1X mixing and –6.5 dBm for 2X mixing as shown in Figure 4.20.

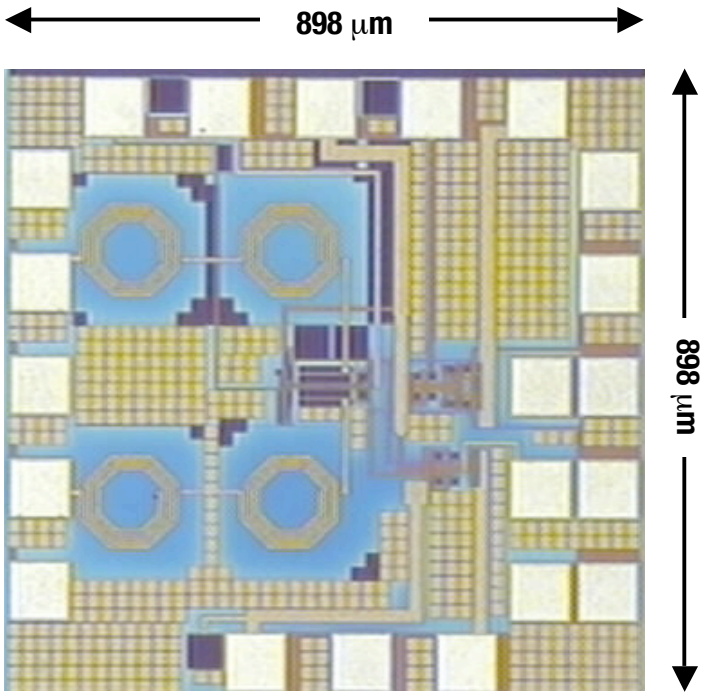


Figure 4.17: Die Micrograph of the active ADPD mixer.

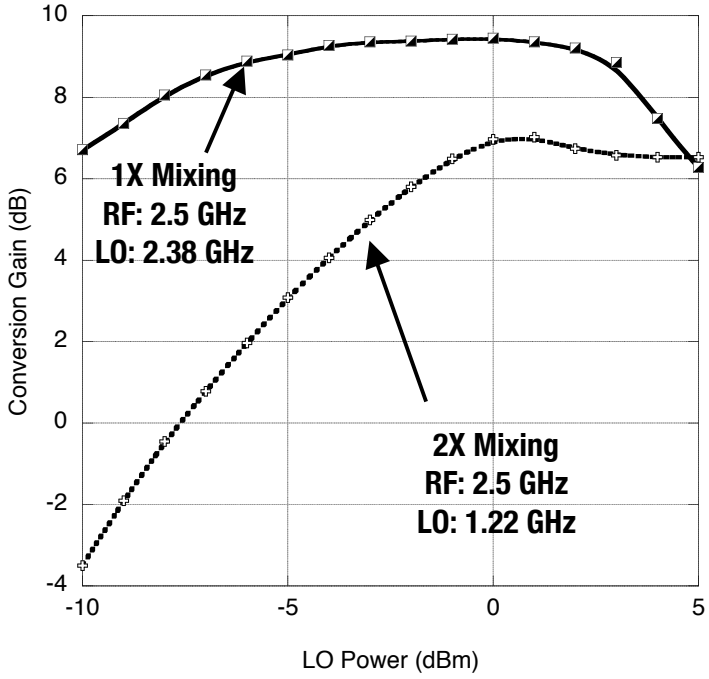


Figure 4.18: 1X and 2X conversion gain vs. LO power.

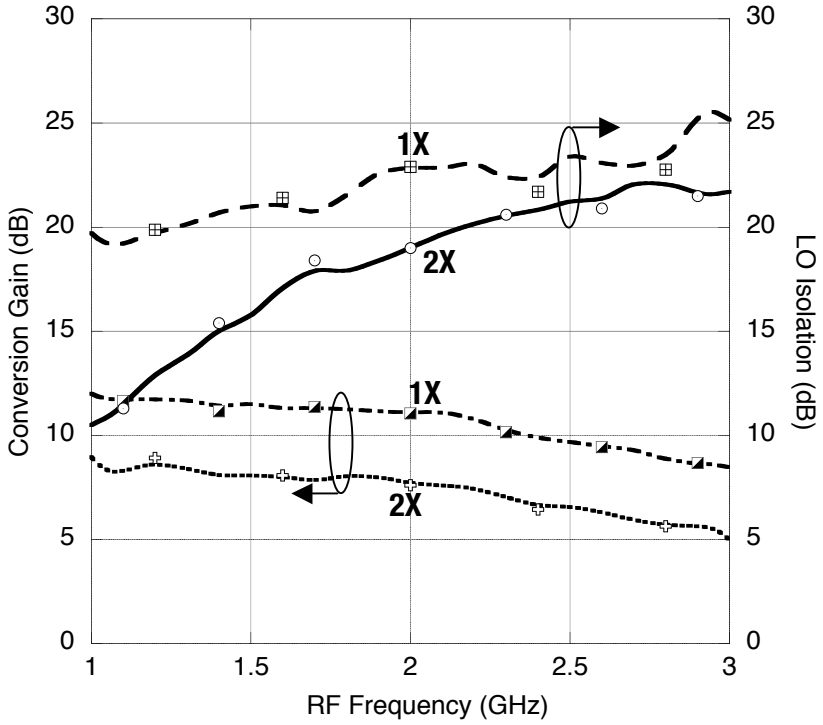


Figure 4.19: Conversion gain and LO isolation of the active APDP mixer.

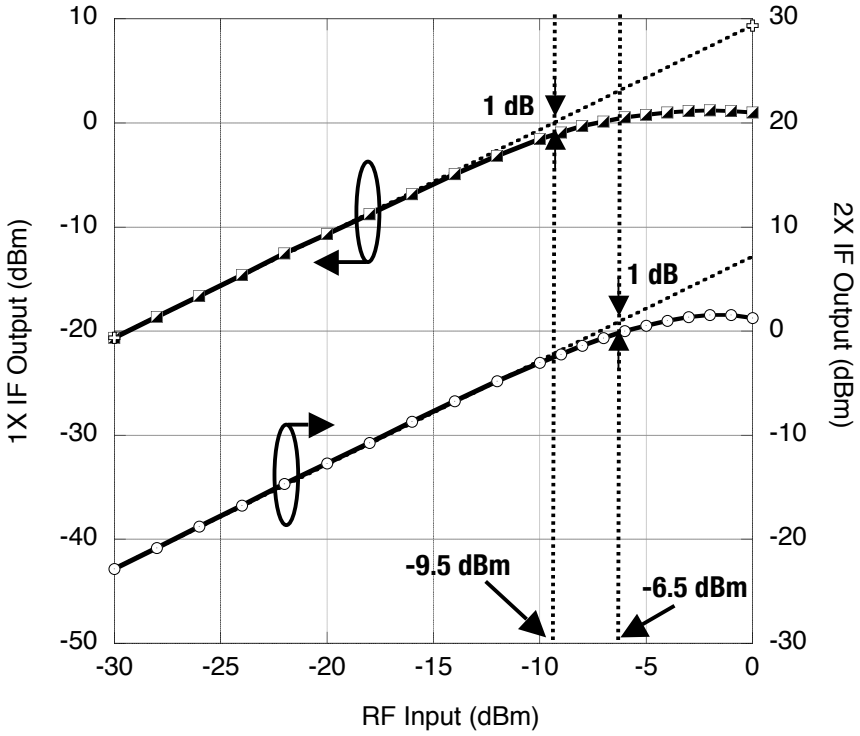
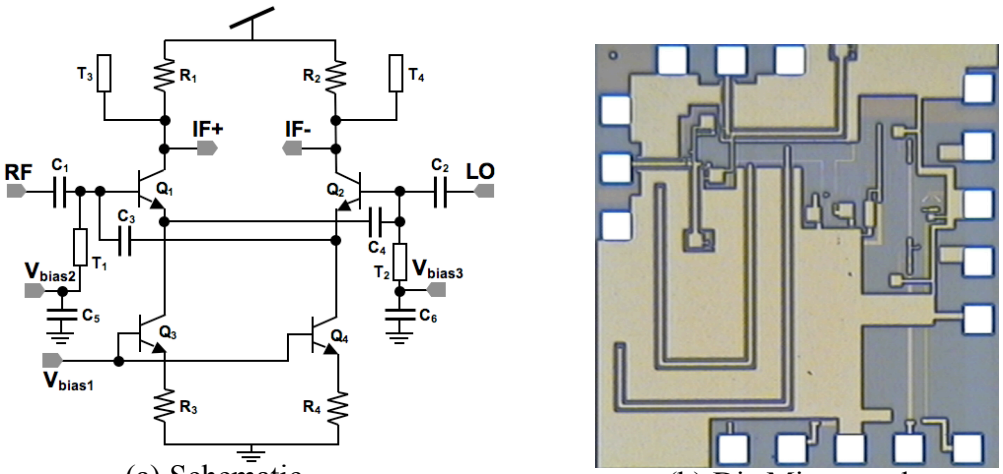


Figure 4.20: 1X and 2X input 1-dB compression point of the active APDP mixer.

The IIP3 of the mixer is -6.4 dBm for 1X mixing and -5.7 dBm for 2X mixing. The measured noise figure is 24.5 dB for 1X mixing and 25 dB for 2X mixing. Measured noise figure is higher than expected due to impedance mismatch at the RF input port.

The 1X and 2X mixers implemented using the active APDP mixer core consumes less than 460 μW of power and are thus useful for developing low power CMOS transceivers for wireless PAN and other applications. The same architecture can even help reduce conversion loss and lower the required local oscillator power in millimeter-wave WPAN receivers as demonstrated by the SiGe subharmonic mixer [50] shown in Figure 4.21. With an LO power of 0 dBm, the measured 2X conversion gain varies from -5 to -7.8 dB in the 50 to 65 GHz range. Compared to earlier reports of millimeter-wave SiGe and GaAs sub-harmonic mixers requiring 5 to 10 dBm of LO power [51] - [54], this circuit achieves similar conversion loss with an LO power as low as -7.5 dBm, while consuming only 0.5 mW of DC power.



(a) Schematic (b) Die Micrograph

Figure 4.21: Schematic and chip micrograph of the 60 GHz SiGe subharmonic mixer based on active APDP mixing core.

4.4 Micro-Power Variable Gain IF Amplifier

A CMOS VGA typically has a cascade of variable gain cells and an exponential voltage generator circuit for obtaining a wide dB-linear gain range [55]. A low-power variable gain amplifier is presented next where all the functions are performed by a single low-power block by combining two independent gain control circuits to obtain 50 dB dB-linear gain range at 1.75 mW power consumption in the nominal mode or 40 dB gain range at 250 μW power consumption in a micro-power mode.

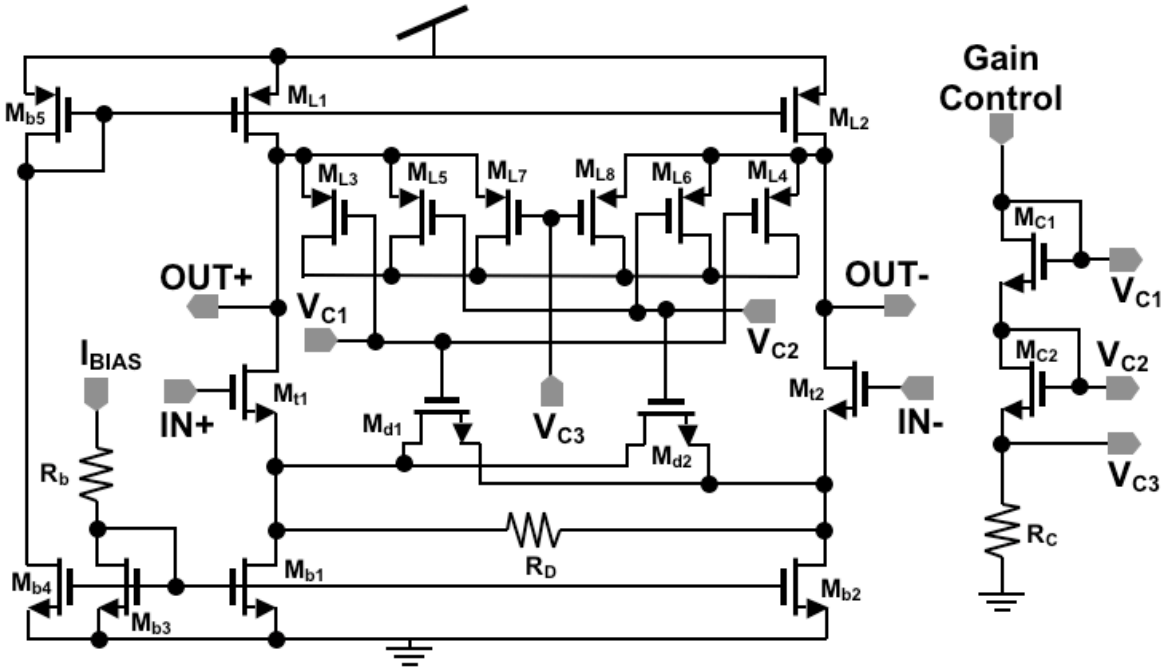


Figure 4.22: Schematic of the low-power VGA.

A wide dB-linear gain range is obtained by combining variable resistive degeneration and variable load gain control. The schematic of this VGA is shown in Figure 4.22. Transistors M_{t1} and M_{t2} form a differential transconductance pair degenerated by R_D, M_{d1}, and M_{d2}. Gain control by variable resistive degeneration provides high linearity [56]. Transistors $M_{L1} - M_{L8}$ form the load of this amplifier. The variable load and degeneration together provide a wide gain range. M_{C1}, M_{C2}, and R_C are used to generate gate voltages from the control voltage so as to combine the two gain control techniques to obtain 50 dB gain range that is approximately linear in the dB scale. The variable gain amplifier is implemented in a 0.25 μm BiCMOS process. The chip micrograph is shown in Figure 4.23.

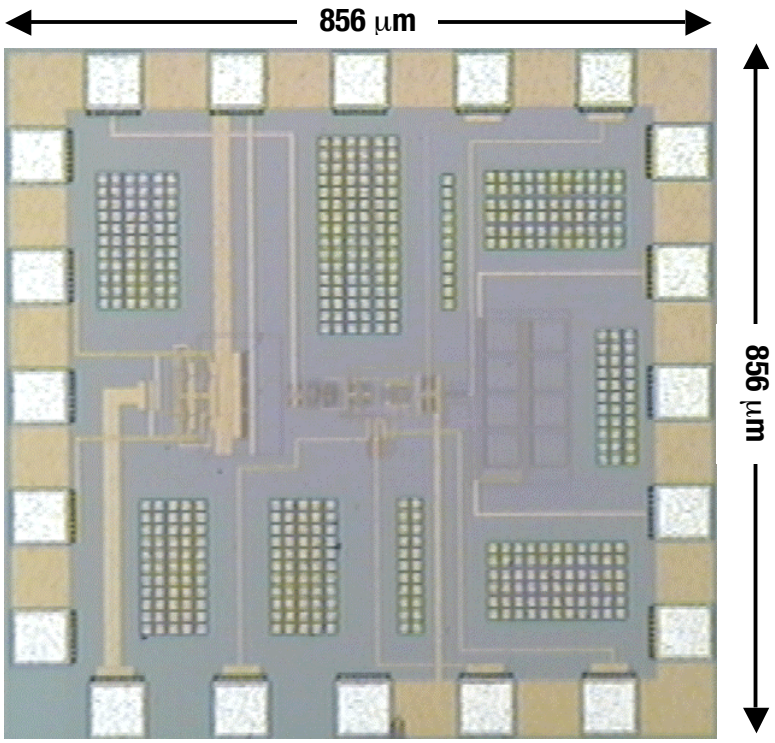


Figure 4.23: Die micrograph of the low-power IF VGA.

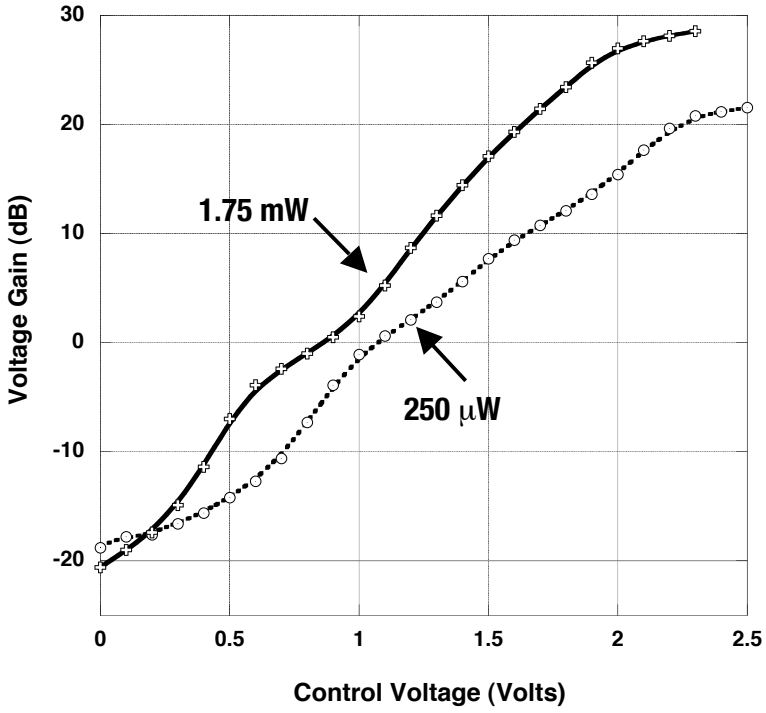


Figure 4.24: Measured gain variation in nominal and low-power modes of the low-power VGA

This VGA consumes 1.75 mW (2.5 V, 700 μA) of power and has an IIP3 of 13 dBm at minimum gain and –12.4 dBm at maximum gain. It has a bandwidth of 80 MHz and an equivalent input referred noise of 8.1 nV/√Hz at maximum gain and 83.8 nV/√Hz at minimum gain. The VGA can also be biased in a micro-power mode consuming only 250 μW of power with a gain-range above 40 dB as shown in the measured results plotted in Figure 4.24.

4.5 Summary

Several micro-power receiver blocks were presented for implementing low-power WPAN front-ends. Subthreshold CMOS operation is demonstrated at the GHz frequency range in the 260 μW subthreshold LNA. Subharmonic mixing techniques are explored as a method to lower the local oscillator frequency of the receiver and thus reduce complexity and power consumption in the LO generation blocks. Two novel mixing techniques based on threshold voltage modulation are presented. While the bulk driven mixer can mitigate LO leakage issues in direct conversion receivers, the active APDP mixer is suited for very low power wireless front-ends. A 250 μW variable gain amplifier is also presented with a gain-range above 40 dB. In the next chapter, these circuits are modified to improve noise performance and integrated together to develop fully monolithic wireless receivers. A subthreshold quadrature LO generation scheme is also presented.

Chapter 5
Integrated Subthreshold CMOS Wireless Receivers

5.1 Introduction

The potential of subthreshold CMOS in implementing extremely low power RF front-end blocks was discussed in section 3.2. Technology scaling has increased the subthreshold f_T and made the exploitation of the higher subthreshold transconductance to bias current ratio possible in RF circuits too. Several low-power circuits were presented in the last chapter operating in the subthreshold region. This chapter presents similar circuits with improved noise performance and higher levels of integration.

Cellular and WLAN wireless receivers have stringent sensitivity specifications and typically require an active low-noise amplifier stage prior to down-conversion. A different design methodology can be used for LR-WPAN front-ends where reducing power consumption is more critical than achieving the lowest sensitivity. A 2.4 GHz receiver is presented in this paper in which the active LNA is replaced by a passive series-resonant network. The passive network provides voltage amplification to reduce the effect of noise added by following stages. It also matches the input impedance of the receiver. The down-conversion mixer utilizes a subthreshold differential pair with LO signal injection at the common source node. It is based on the active APDP mixing core explained in section 4.3.3, but modified to improve conversion gain and noise performance. The LO power required for maximum conversion gain is only -10 dBm.

The receiver is implemented in a 0.18 μm CMOS process and consumes only 540-μW of power. It has a measured gain of 24.7 dB, a noise figure of 7 dB, and an output IP3 of 7.7 dBm.

The first fully integrated CMOS quadrature receiver is presented next using only subthreshold circuits for 2.4 GHz WPAN applications. The receiver is implemented in a 0.18 μm CMOS process and operates from a 1.2 V supply. The total power consumption in the subthreshold receiver chain, including the differential low-noise amplifier with gain switching, the quadrature mixer and the variable gain IF amplifiers, is only 1.4 mW. A series resonant passive network is used at the input of the LNA to provide both voltage gain and impedance matching. The maximum gain achieved by the receiver is 43 dB with 15 dB gain switching in LNA and a dB-linear range of 33 dB in the IF VGAs. The receiver has a measured noise figure of 5 dB and an output IP3 of 6.3 dBm at the maximum gain setting. A 1.2 mW subthreshold quadrature voltage controlled oscillator (QVCO) and buffer stack is also implemented for LO signal generation. The subthreshold QVCO buffer stack achieved a measured phase noise of -103.67 dBc/Hz at 1 MHz offset.

5.2 Micro-Power CMOS Receiver Using Passive LNA

5.2.1 Design and Implementation of the Micro-Power Receiver

Conventional LNAs provide both input matching and voltage gain without significantly degrading the signal-to-noise ratio. It thus reduces the effect of the following stages on the overall receiver noise figure. In this work, the active LNA is replaced by a series-resonant passive network as shown in Figure 5.1.

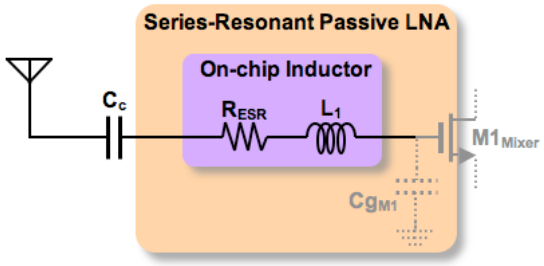


Figure 5.1: Schematic of the series-resonant passive network replacing the LNA.

In Figure 5.1, Cg_{M1} represents the effective capacitance to ground at the gate of $M1_{Mixer}$, the input transistor of the following down-conversion stage. C_c is the DC-blocking capacitor between the antenna and the integrated receiver. The on-chip spiral inductor L_1 resonates with Cg_{M1} at the operating frequency. Thus the input impedance of the LNA at the operating frequency is R_{ESR}, the equivalent series resistance of the on-chip inductor. The spiral inductor is designed to have an equivalent series resistance of 50 Ω at the operating frequency, thus achieving input impedance match at the cost of higher

noise figure. At the resonance frequency, ω_r, the passive network provides the following voltage gain:

Equation 5.1: $$\left|A_V(\omega_r)\right| = \frac{1}{\omega_r R_{ESR} C g_{M1}} = \frac{\omega_r L_{L_1}(\omega_r)}{R_{ESR}} = Q_{L_1}(\omega_r)$$

where $L_{L1}(\omega_r)$ and $Q_{L1}(\omega_r)$ are the inductance and Q of L_1 at the resonance frequency, ω_r, respectively.

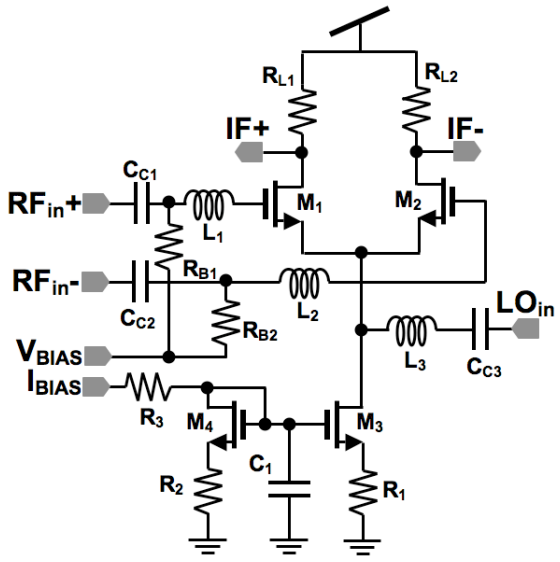


Figure 5.2: Schematic of the integrated micro-power receiver.

If the down-conversion mixer following the passive input stage cannot provide sufficient conversion gain, then the noise added by subsequent stages may dominate the overall noise figure [22]. A subthreshold mixer is used in this work to provide adequate conversion gain at extremely low power consumption. Subthreshold biasing not only

provides a higher g_m/I_D ratio but also increases the output impedance of the transistors compared to the operation in saturation region as explained in chapter 0. The schematic of the integrated receiver is shown in Figure 5.2.

Transistors M_1 and M_2 are biased in subthreshold region and together form a differential pair. The RF signal is amplified by the series-resonant passive networks (L_1 and L_2) and applied to the gates of these transistors. LO signal is injected at the common source node of the differential pair as shown in Figure 5.2. Down conversion is achieved by exploiting the exponential non-linearity of the transistors in subthreshold region. The voltage gain of this receiver is given by:

Equation 5.2: $$(Voltage\ Gain)_{\text{Receiver}} = \left(\frac{W}{L}\right)_{M_1} I_{DO}\left(\frac{1}{n(kT/q)}\right)^2 \left(\frac{v_{LO}}{2}\right)\left(\frac{Q_{L_1}(\omega_r)}{g_{ds1} + \frac{1}{R_{L1}}}\right),$$

where v_{LO} is the LO signal amplitude.

The LO power required for achieving the maximum conversion gain is about -10 dBm, leading to potential power savings in the LO signal generation and buffering circuits. If the current mirror (formed by transistors M_4 and M_3 in saturation) is replaced by a shunt resonant tank, one can lower the supply voltage to 1 V and further decrease the power consumption to 300-μW.

The integrated receiver is fabricated in a 1P6M 0.18 μm CMOS process. The on-chip inductors forming the series resonant network (L_1 and L_2) are about 13 nH each and are implemented as octagonal spiral inductors in the top metal layer. At the operating frequency of 2.45 GHz the inductor Q's are about 4 each. From Equation 5.1, the voltage gain of the passive network is 12 dB. The chip micrograph is shown in Figure 5.3. The chip dimensions are 1080 μm x 970 μm including the pads as indicated. Also marked in Figure 5.3 are the input RF pads, the LO pad, the output IF pads, and the three on-chip inductors L_1, L_2, and L_3.

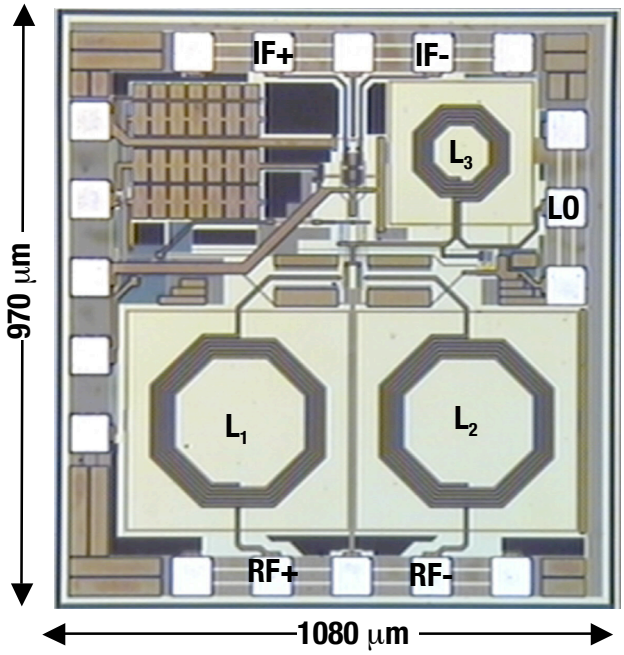


Figure 5.3: Die micrograph of the integrated micro-power receiver.

5.2.2 Micro-Power Receiver Measurement Results

Since the mixer is not designed to drive a 50 Ω load, a unity gain output buffer is used to facilitate measurements. A stand-alone output buffer is fabricated and characterized so as to de-embed its effects on the receiver measurements.

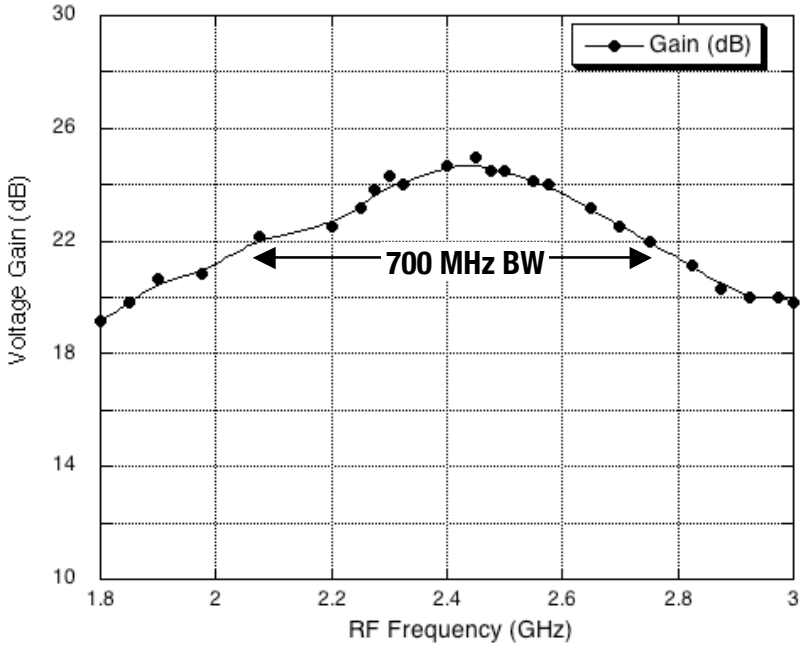


Figure 5.4: Measured voltage gain of the receiver.

All the measurements were performed by on-wafer probing. The integrated receiver consumes 540 μW of power, drawing 300 μA from the 1.8 V supply. The measured voltage gain of the receiver is plotted against RF frequency in Figure 5.4. It has a peak gain of about 25 dB at 2.45 GHz and a 3-dB bandwidth of about 700 MHz from 2.05 GHz to 2.75 GHz.

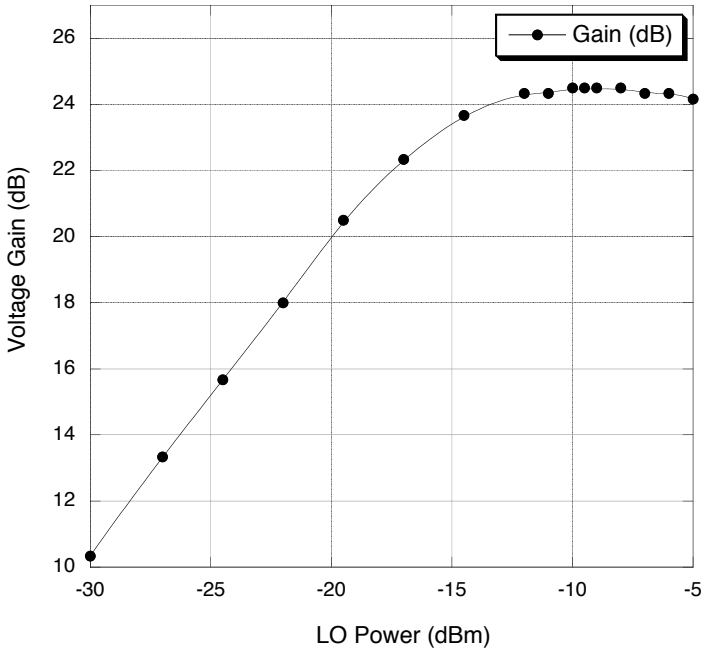


Figure 5.5: Measured gain of the receiver plotted against LO power.

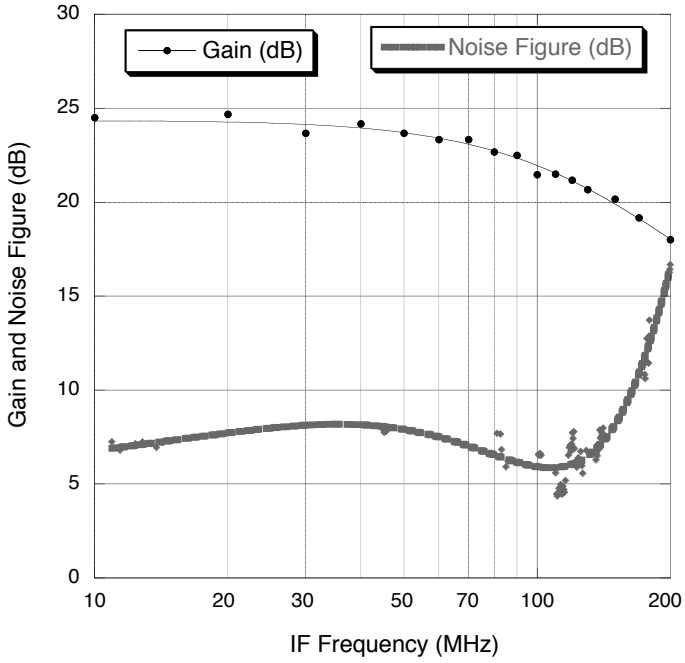


Figure 5.6: Measured gain and noise figure of the receiver.

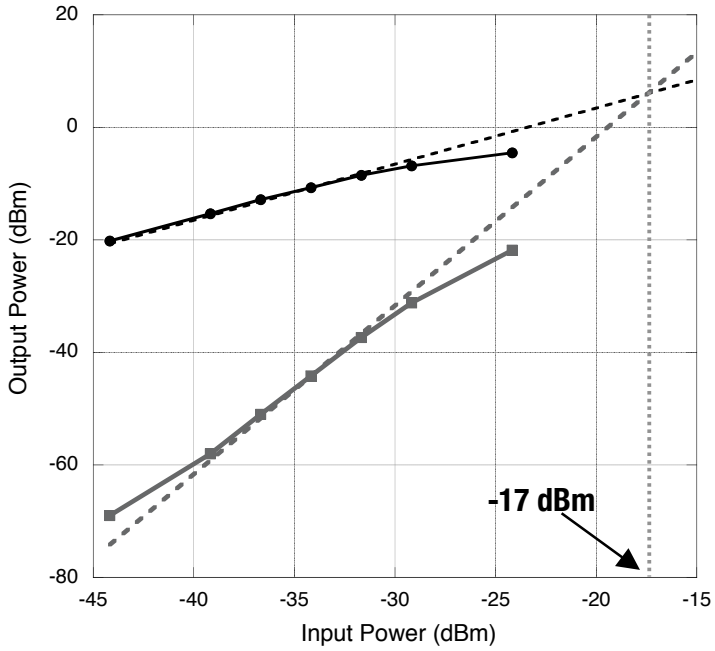


Figure 5.7: Input IP3 of the integrated receiver.

The variation of the receiver gain with LO power is plotted in Figure 5.5 for an RF frequency of 2.5 GHz and an LO frequency of 2.46 GHz. As discussed earlier, the LO power requirement of the receiver is very modest. The conversion gain is above 20 dB for LO power as low as -20 dBm.

The measured gain and noise figure of the receiver are plotted against the IF frequency in Figure 5.6. The noise figure is about 7 dB around 10 MHz IF and below 6 dB at 100 MHz IF. The measured input 1-dB compression point of the receiver is -27 dBm. The input IP3 plot is shown in Figure 5.7 with the two input tones at 2.5 GHz ± 10 kHz. The IIP3 of the receiver is -17 dBm.

5.3 Fully-Integrated Subthreshold Quadrature Receiver

Low-rate wireless PAN nodes require extremely low power front-ends with relaxed sensitivity specifications. Subthreshold circuits are hence ideally suited for this application as explained before. A subthreshold LNA can be added before the subthreshold mixer presented in section 5.2.1 to further lower the noise figure. Passive voltage gain blocks can be added before the subthreshold amplifier in the receiver chain to reduce the effect of the higher induced gate noise.

5.3.1 Implementation of the Subthreshold CMOS Quadrature Receiver

In this receiver, subthreshold CMOS circuits, passive voltage amplification, and low-power circuit techniques such as current reuse, stacking, and differential cross coupling are combined to reduce the total receiver power consumption without significantly degrading noise. The low-IF quadrature receiver topology implemented in this work is shown in Figure 5.8.

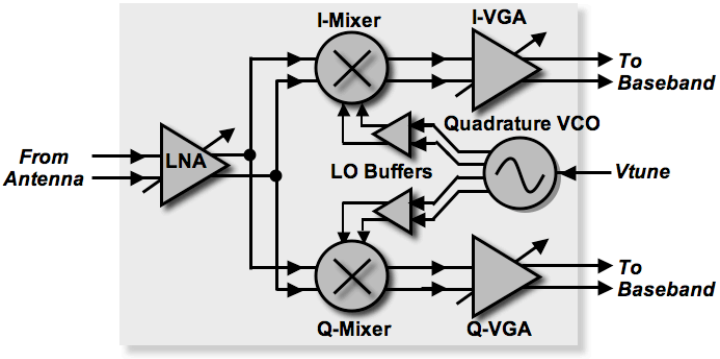


Figure 5.8: Block diagram of the low-IF quadrature receiver with integrated QVCO and LO buffers.

5.3.1.1 Differential Subthreshold LNA

As explained before, subthreshold circuits have higher noise figures due to the higher gate induced transistor noise. In this work, a series resonant passive network is used before the subthreshold LNA to provide both voltage gain and impedance matching simultaneously. The voltage gain provided by the passive network prevents subthreshold transistors in following stages from severely degrading the overall receiver noise figure as discussed before.

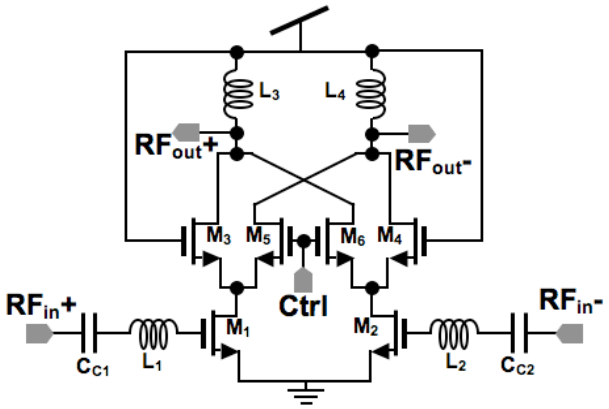


Figure 5.9: Schematic of the subthreshold low noise amplifier with gain switching. Biasing circuits are not shown.

A simplified schematic of the subthreshold LNA is shown in Figure 5.9. On-chip spiral inductors L_1 and L_2 (≈18 nH each) resonate with the gate capacitances of input transistors M_1 and M_2, Cg_{M1} and Cg_{M2}, respectively, at 2.4 GHz. Input impedance of the amplifier at the operating frequency is essentially the series resistance of the inductors, R_{ESR}, which is designed to be 50 Ω (Q≈5.5) to achieve impedance matching as explained

before. At the resonance frequency, ω_r, the passive network provides the same voltage gain given by Equation 5.1.

The cascode amplifier formed by subthreshold transistors M_1, M_2, M_3, and M_4 and load inductors L_3 and L_4 provides further gain while consuming 300 μA of current in each branch from a 1.2 V supply. The differential LNA provides a gain of 21 dB and a noise figure of 4.5 dB in simulations, while consuming only 720 μW of power. Separate test port has not been included in the integrated receiver test chip at the LNA/Mixer interface.

The overall voltage gain of the LNA is given:

Equation 5.3: $$(Voltage\ Gain)_{LNA} = Q_{L_1} g_{m1} \left(\frac{g_{m3} - g_{m5}}{g_{m3} + g_{m5}} \right) \omega_r L_3 \left(Q_{L_3} + \frac{1}{Q_{L_3}} \right),$$

where g_{mi} is the transconductance of transistor M_i. Transistors M_5 and M_6, when turned on, provide a 15 dB lower gain mode for the LNA. This is achieved by reducing the effective g_m of the cascode from g_{m1} (when $g_{m5} = 0$) to $g_{m1}(g_{m3}-g_{m5})/(g_{m3}+g_{m5})$ by current cancellation. The gain switching implemented in this LNA does not disturb impedance matching at the input.

5.3.1.2 Subthreshold Down-Conversion Mixers

The schematic of the subthreshold down-conversion mixer is shown in Figure 5.10. The double-balanced mixer is similar to the mixer presented in section 5.2.1, and is based on differential pairs M_3-M_5 and M_4-M_6 that are biased in weak inversion by the current mirrors formed by M_1, M_2, and M_7. Mixing is achieved by exploiting the nonlinear exponential characteristics of subthreshold transistors by applying RF signal at the gate and LO signal at the source as explained before.

The conversion gain of this mixer is given by:

Equation 5.4: $$(Conv.Gain)_{Mixer} = \left(\frac{W}{L}\right)_{M_3} I_{DO}\left(\frac{1}{n(kT/q)}\right)^2 v_{LO}\left(\frac{1}{2g_{ds3}+\frac{1}{R_{L1}}}\right).$$

The LO signal swing required in this architecture is low (about 100 mV-peak for maximum conversion gain). The input impedance of the LO port is also high, about 430 Ω single-ended. Thus the drive requirements on the VCO and LO buffers are modest, leading to significant power savings in the LO generation blocks too. The double-balanced mixer draws 150 μA of current from the 1.2V supply. The mixer provides a conversion gain of 9 dB and a noise figure of 11.8 dB (at 10 MHz IF), while consuming 180 μW of power.

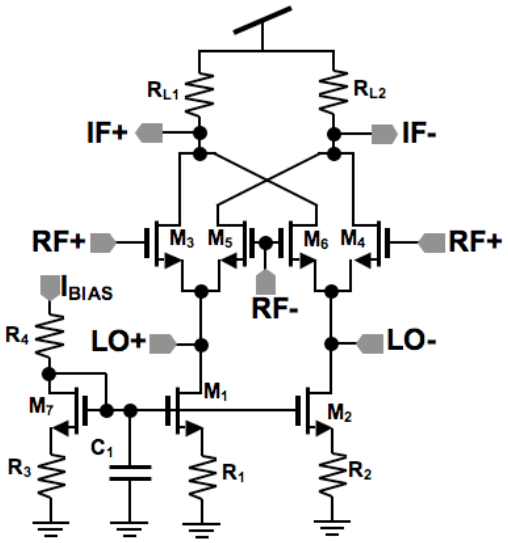


Figure 5.10: Schematic of the subthreshold down-conversion mixer.

5.3.1.3 Subthreshold Variable Gain Amplifier

Settling time specifications usually require the variable gain stages in a receiver to have a dB-linear gain variation with control voltage. This is achieved in a subthreshold VGA, similar to the one shown in Figure 4.22, by combining two independent gain control schemes as explained in section 4.4. When gain control by variable degeneration (formed by R_D, M_{d1}, and M_{d2}) is combined with that by variable load (M_{L1} through M_{L8}), an approximately dB-linear gain range of 33 dB is achieved at a current consumption of 150 μA from the 1.2 V supply.

5.3.2 Implementation of the Subthreshold LO Signal Generation Blocks

Low-rate WPAN systems have relaxed phase noise specifications and hence power consumption can be reduced at the cost of increased phase noise [57]. Circuit techniques like current-reuse [58], stacking [20], and transformer feedback [59] have been used to reduce the power consumption in the LO generation blocks. However, subthreshold biasing has not been utilized extensively for developing micro-power oscillators and LO buffers yet [60], [60].

5.3.2.1 Low-Power Differential Cross-coupled LO Buffer

In a fully integrated wireless transceiver, the LO buffers often consume significant amounts of power in order to provide the required LO amplitude to mixers. The design of the low-power LO buffers is as critical as the design of the VCO itself because the buffers cannot be allowed to limit the overall performance of the LO generation scheme [62]. The oscillator buffer should not significantly increase the loading of the VCO resonator. Excessive loading of the resonator may not only cause significant shift in oscillation frequency, but can also prevent oscillations from starting altogether. The buffer should supply the required LO power to the mixers without distortion and without consuming large amounts of power. These requirements make the design of low power LO buffer extremely challenging [63].

Commonly used CMOS buffers are based on the four topologies shown in Figure 5.11(a)-(d). Of these, common-source amplifier with resistive load and CMOS inverter generate positive input conductance in case of capacitive loading at its output terminals. The small-signal input admittance of an NMOS amplifier with a resistive load of R_{load} and a load capacitance of C_{load} is given by:

Equation 5.5:

$$\mathrm{Re}al[Y_{in}] = \frac{\omega^2 R_p C_{gd}\left[g_m R_p (C_l + C_{gd}) + C_{gd}\right]}{D_1} > 0,$$

$$\mathrm{Im}ag[Y_{in}] = \frac{\omega C_{gd}\left[1 + g_m R_p + \omega^2 R_p{}^2 C_l (C_l + C_{gd})\right]}{D_1} + \omega C_{gs},$$

where $R_p = R_{load} \parallel r_{ds}$, $C_l = C_{load} + C_{ds}$, and

$$D_1 = 1 + \omega^2 R_p{}^2 (C_l + C_{gd})^2.$$

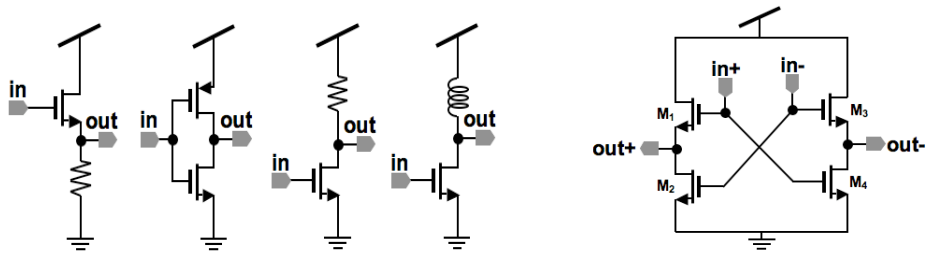


Figure 5.11: CMOS LO buffer circuits: (a) Source follower; (b) CMOS inverter; (c) Common-source amplifier with resistive load; (d) Common-source amplifer with inductive load; (e) Cross-coupled buffer

When designed to generate high output power, the device sizes need to be increased. Larger devices not only increase capacitive loading of the resonator that shifts the oscillation frequency, but also affect the oscillation start-up as described before. This

leads to a trade-off between the output signal power of the buffer and its loading on the VCO resonator. Hence, neither the CMOS inverter buffer nor the CS buffers (even with inductive peaking) are suitable for low-power and high frequency applications. The source follower based oscillator buffer, on the other hand, has negative input conductance when loaded with a capacitor at the output [62]. The small-signal input admittance of an NMOS source follower buffer with a load similar to that in Equation 5.5 is given by:

Equation 5.6:

$$\mathrm{Re}al\left[Y_{in}\right] = -\frac{\omega^2 R_l C_{gs}\left[g_m R_l\left(C_l + C_{gs}\right) - C_{gs}\right]}{D_2} < 0,$$

$$\mathrm{Im}ag\left[Y_{in}\right] = \frac{\omega C_{gs}\left[1 - g_m R_l + \omega^2 R_l^2 C_l\left(C_l + C_{gs}\right)\right]}{D_2} + \omega C_{gd},$$

$$\text{where } R_l = \frac{1}{g_m} \parallel R_{load} \parallel r_{ds},\ C_l = C_{load} + C_{ds}, \text{ and}$$

$$D_2 = 1 + \omega^2 R_l^2\left(C_l + C_{gs}\right)^2.$$

The negative input conductance helps the oscillator to startup instead of loading the resonator. However, a major drawback of the source follower buffer is the lack of an active pull-down device leading to asymmetric output voltage waveforms. Also, it does not provide any voltage gain. To avoid capacitive loading of the resonator, the device size has to be small, which further restricts the maximum output power even with a high bias current.

The differential cross-coupled transistors, in the LO buffer shown in Figure 5.11(e) [63], generate negative input conductance that helps in the start-up of oscillation as explained before. The differential input admittance of the cross-coupled buffer with a similar load is given by:

Equation 5.7:

$$\mathrm{Re}al\left[Y_{in}\right] = -\frac{\omega^2 C_1\left(G_m C_2 - G_o C_1\right)}{G_o^{\,2} + \omega^2 C_2^{\,2}} < 0,$$

$$\mathrm{Im}ag\left[Y_{in}\right] = \omega\left(C_3 - \frac{C_1\left(G_m G_o + \omega^2 C_1 C_2\right)}{G_o^{\,2} + \omega^2 C_2^{\,2}}\right),$$

where $C_1 = C_{gs1} - C_{gd2}$, $C_2 = C_{load} + C_{ds1} + C_{ds2} + C_{gs1} + C_{gd2}$,

$C_3 = C_{gs1} + C_{gd1} + C_{gs2} + C_{gd2}$, $G_o = \left(1/R_{load}\right) + g_{ds1} + g_{ds2} + g_{m1}$,

and $G_m = g_{m1} + g_{m2}$.

A major advantage of the differential cross-coupled buffer over the standard source follower buffer is that the former provides voltage gain greater than unity. The cross-coupled buffer has both active pull-up and pull-down capability which results in larger output current drive for the same power consumption as compared to that of the source follower buffer.

5.3.2.2 Subthreshold Quadrature LO Chain

The schematic of the quadrature LO generation block is shown in Figure 5.12. The differential cross-coupled buffer is stacked on top of the subthreshold oscillator for current re-use. Capacitors CG_i and CG_q provide ac ground for the VCO supply and the buffer ground. The total supply voltage for the front-end is 1.2 V while the supply voltage for the VCO is set to 0.45 V, which drives the cross-coupled devices of the oscillator into subthreshold region of operation. The transistors in the LO buffer are also biased to operate in the subthreshold region. Frequency tuning was implemented using a MOS varactor (for fine tuning) and a capacitor switch in order to achieve an overall tuning range of 2.26-2.52 GHz considering PVT variations. The PMOS transistors of the

LO buffers function not only as voltage amplifiers but also as current sources for the cross-coupled pair of the VCO. Thus, the tail current source for the VCO is eliminated which can help improve the phase noise performance of the VCO [63].

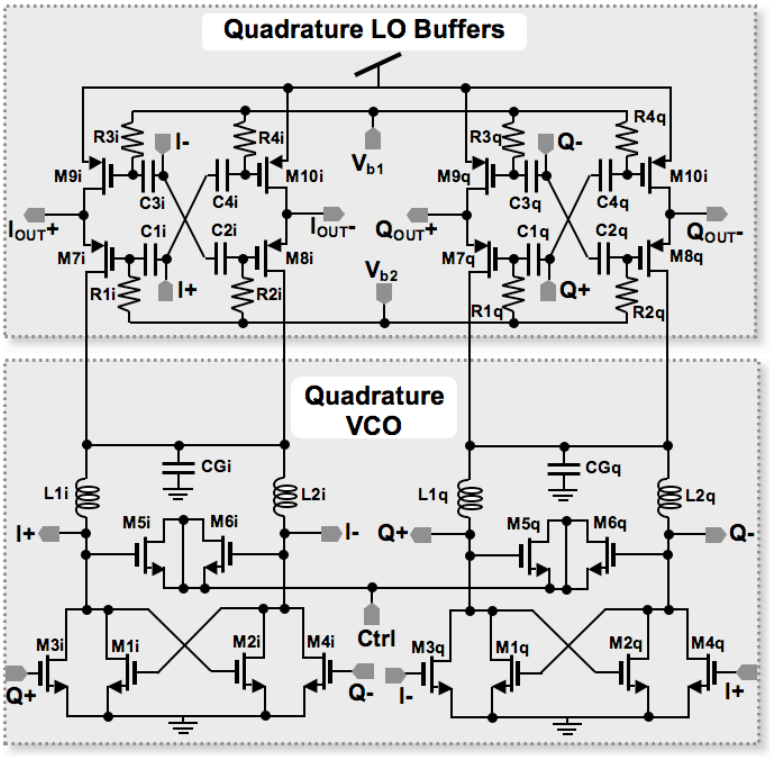


Figure 5.12: Schematic of the subthreshold QVCO-buffer stack.

In this implementation, the LO voltage requirement was 100 mV across the 430 Ω input impedance of the sub-threshold mixer. The subthreshold QVCO buffer stack could provide this amplitude while consuming only 1 mA of current from the 1.2 V supply, thus consuming a total power of only 1.2 mW for the entire quadrature LO chain.

5.3.3 Measurement Results of the Subthreshold CMOS Quadrature Receiver

The receiver was fabricated in a 1P6M 0.18 μm CMOS process. The chip micrograph is shown in Figure 5.13. The chip dimensions are 2 mm x 1.4 mm including the pads. Using differential inductors can significantly reduce the die area.

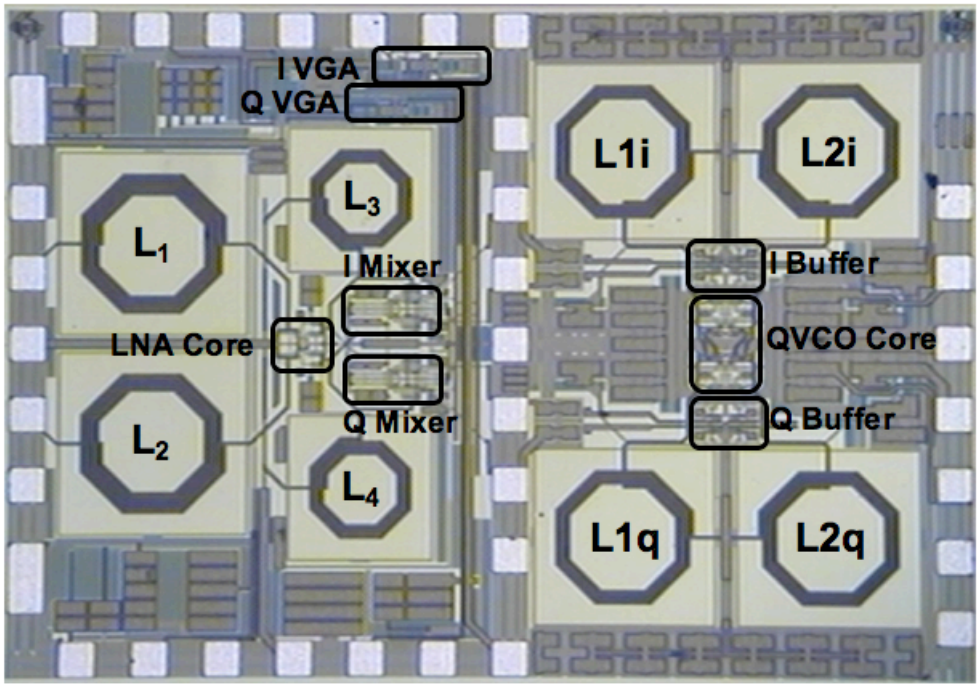


Figure 5.13: Chip micrograph of the subthreshold receiver.

All measurements were carried out by on-wafer probing. The receiver consumed a total power of 1.4 mW while the QVCO and buffers consumed 1.2 mW. The total receiver gain is plotted against RF frequency in Figure 5.14. This measurement was performed at the maximum gain setting of the receiver. As can be seen from Figure 5.14, the receiver has a maximum gain of 43 dB at 2.5 GHz, with a 3-dB RF bandwidth of 350

MHz (2.3 GHz - 2.65 GHz). The measured 3-dB IF bandwidth is 95 MHz leading to a processing efficiency of 27 μW/MHz.

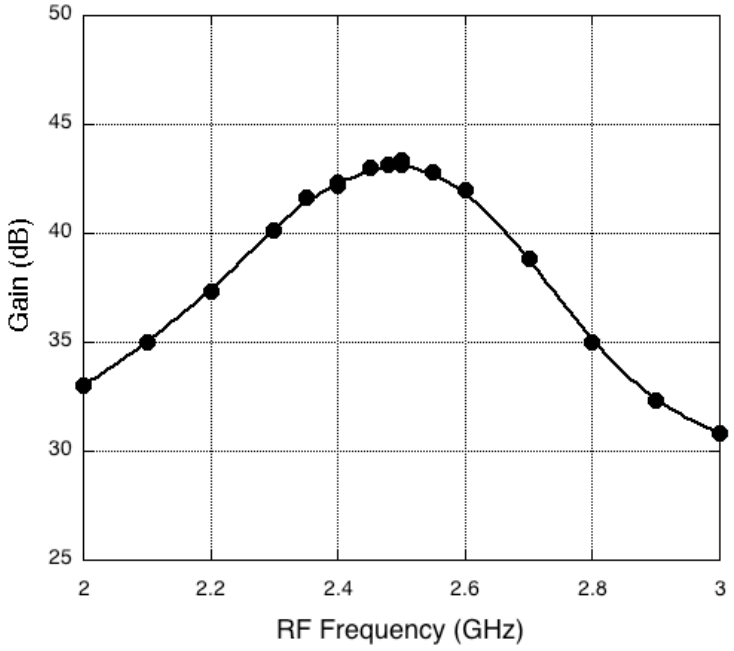


Figure 5.14: Measured gain of the subthreshold receiver at maximum gain setting.

Since the chip had a provision of using external LO too, the conversion gain was also measured for different LO signal powers. The maximum gain is achieved when the LO input is –10 dBm at each LO terminal as shown in Figure 5.15.

The input matching (S_{11}) of the receiver is plotted in Figure 5.16. Input matching is better than –26 dB at 2.5 GHz. Plotted against IF frequency in Figure 5.17 is the gain and noise figure measured using a noise figure meter. A noise figure of 5 dB is measured at 10 MHz, the lowest IF frequency limit in the measurement setup. The measured output IP3 of the receiver at maximum gain is 6.3 dBm. Measured gain control using VGA is

plotted in Figure 5.18. A dB-linear gain range of 33 dB is obtained with gain error less than 2 dB from an ideal dB-linear gain curve as shown in Figure 5.19.

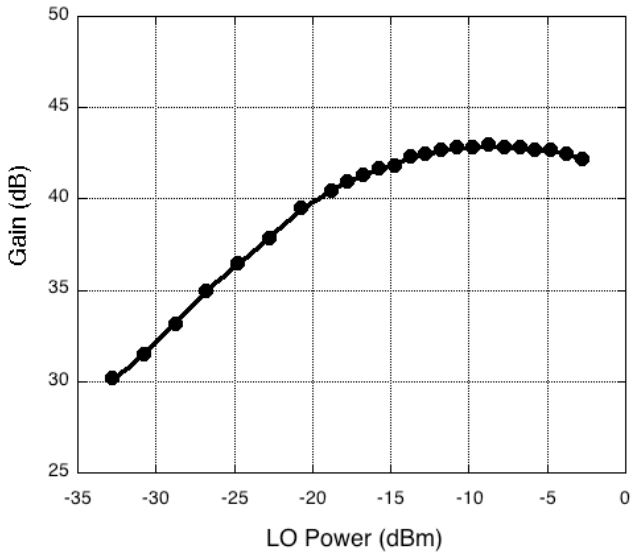


Figure 5.15: Measured gain of the receiver plotted against LO power.

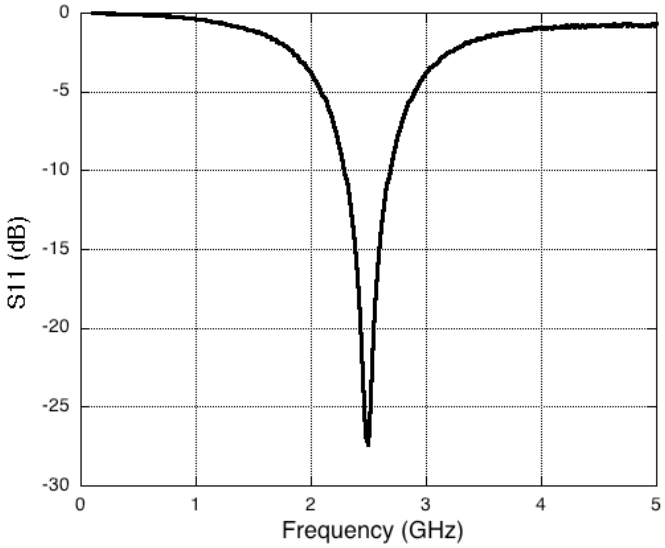


Figure 5.16: Measured input matching of the subthreshold receiver.

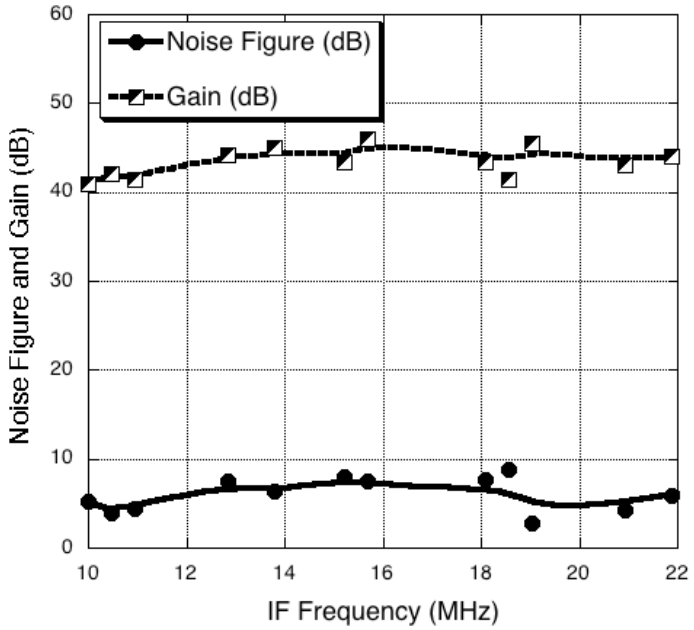


Figure 5.17: Measured noise figure and gain vs. IF.

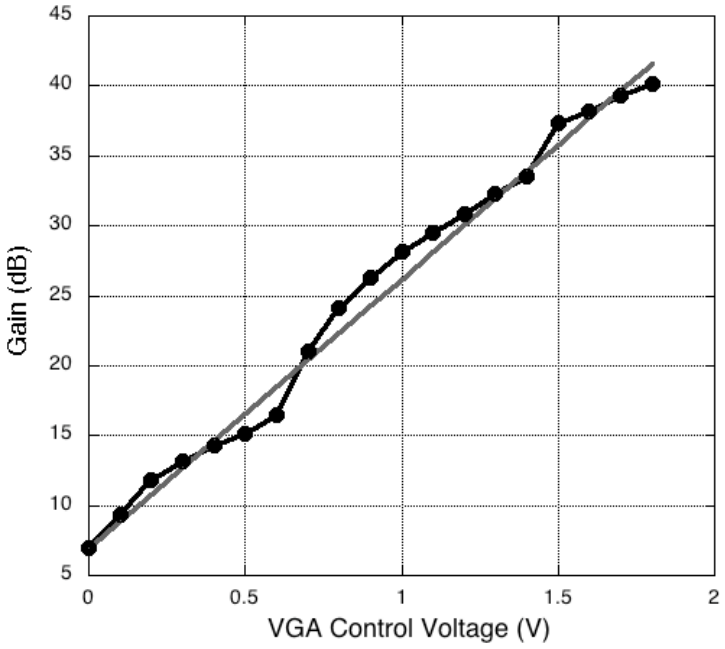


Figure 5.18: Measured gain control of the receiver using the IF VGA.

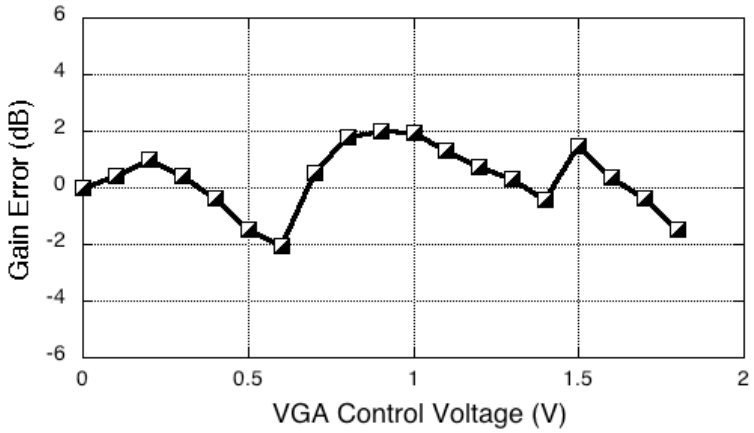


Figure 5.19: Measured gain control error of the receiver using the IF VGA.

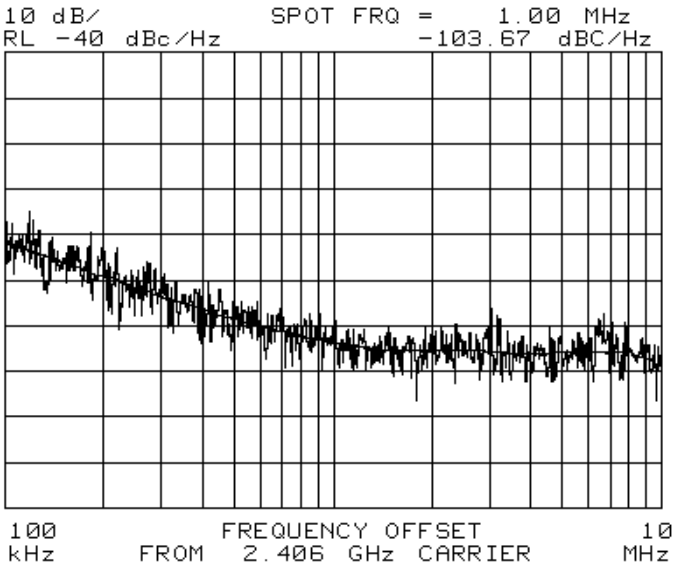


Figure 5.20: Measured phase noise of the subthreshold QVCO.

The measured phase noise of the QVCO [63] is –103.7 dBc/Hz at 1 MHz offset as shown in Figure 5.20. Shown in Figure 5.21 is the measured frequency range of the QVCO: 2.36 – 2.5 GHz.

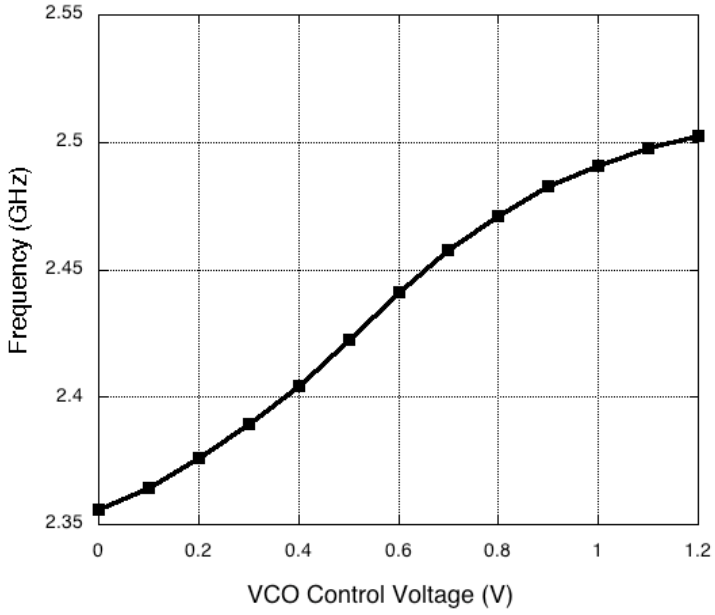


Figure 5.21: Measured frequency control of the subthreshold QVCO.

The performance of this receiver is summarized and compared with other reports in Table 5.1. The subthreshold receiver achieves 43 dB gain and 5 dB noise figure while consuming only 1.4 mW of power at the cost of reduced linearity (6.3 dBm OIP3). Earlier reports with similar power consumption have higher noise figures. For example, compared to the single ended LNA and single balanced mixer in [65] consuming 500 μW of power, the total power consumed by equivalent blocks in the subthreshold receiver is only 450 μW (360 μW in single ended LNA and 90 μW in single balanced mixer) while the noise figure is lower by more than 5 dB.

Table 5.1: Receiver Performance Comparison

	[14]	[18]	[20]	[64]	[65]	**This Work**
Process	180nm CMOS	250nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS	**180nm CMOS**
Freq. (GHz)	2.4	2.4	1.6	2.4	2.4	**2.5**
Supply Voltage (V)	1.8	2.5	1.2	1.8	1	**1.2**
Power (mW)	10.1	17.5	5.4*	6.48	0.5 (Single bal. LNA-mixer)	**1.4 (2.6*)**
Voltage Gain (dB)	< 32**	50	36	21.4	30.5	**43**
Noise Figure (dB)	5.7	6	4.8	13.9	10.1	**5**
OIP3 (dBm)	< 16**	-	17	-	9.5***	**6**

*VCO power consumption included.

**The voltage gain and OIP3 will be lowered by the total loss in the poly-phase filter and the passive mixer.

***OIP3 number estimated from 1-dB compression point by adding 10dB.

5.4 Summary

The circuits presented in chapter 0, were modified to improve noise performance and integrated with other subthreshold front-ends circuits to develop extremely low-

power wireless receivers for WPAN systems. A 2.4 GHz receiver is implemented for such applications in a 0.18 μm CMOS process requiring a current consumption of only 300 μA from a 1.8 V supply. It has a series-resonant passive network for input matching and voltage amplification instead of an active low noise amplifier. A novel subthreshold mixer, based on LO injection in the source, is used for down-conversion. The receiver achieves a voltage gain of 24.7 dB, a noise figure of 7 dB, and an output IP3 of +7.7 dBm. The LO power requirement of the receiver is extremely small, achieving more than 20 dB gain with LO power as low as -20 dBm.

The first fully integrated subthreshold CMOS receiver is presented for 2.4 GHz wireless personal area network applications. Power consumption is lowered without compromising noise performance by combining passive voltage amplification, subthreshold biasing, stacking, current reuse, and differential cross coupling. The subthreshold receiver implemented in 0.18 μm CMOS process achieves a gain of 43 dB, a noise figure of 5 dB, and an output IP3 of 6 dBm while consuming only 1.4 mW of power. The integrated 2.4 GHz QVCO and LO buffers consume 1.2 mW of power. The QVCO has a measured phase noise of -103.7 dBc/Hz at 1 MHz offset.

Chapter 6
Low-Cost Resistive Feedback RF Circuits

6.1 Introduction

Circuit techniques were presented in previous chapters to implement extremely low power wireless receivers for WPAN applications. Digital CMOS technology was chosen for implementation because of its cost advantages. However, cost is also determined by the area requirement of these circuits, which is dependent on the number of high-Q passive components. This chapter presents circuit techniques to eliminate high-Q inductors in LNA circuits. Though these extremely compact circuits are more critical in multi-band, multi-standard, and MIMO (multiple-input multiple-output) systems, they can also be used to lower the cost of WPAN front-ends if the power consumption is lowered. If sufficient gain is provided by the LNA, the down-conversion mixer can be a passive mixer as explained in section 2.3.3. In such an implementation, the only power consuming RF block in the receiver will be the LNA.

Low noise amplifiers occupy a significant percentage of the total die area in wireless front-ends today. This is because the performance of the LNA is dependent on the Qs of the multiple on-chip inductors. Because the area requirement of high-Q on-chip inductors is high, the die area occupied by the LNA is also high. Often, costly process steps are required to enhance the Q of the on-chip inductors to further improve the performance of RF circuits. The design of these circuits usually requires a higher number

of simulation and verification iterations. Cascode amplifiers with inductive source degeneration [65], the predominant low noise amplifier implementation used in CMOS wireless front-ends, require three high-Q inductors for achieving input impedance matching, high gain, and low noise figure. In spite of the high die area requirements, cascode LNAs have been used extensively in narrow-band wireless applications because they provide high gain, low noise, and high linearity at relatively low power consumption. With the advent of MIMO, multi-standard, and multi-band wireless systems, however, the use of the area intensive cascode LNAs is becoming increasingly expensive, leading to the pursuit of alternative LNA implementations.

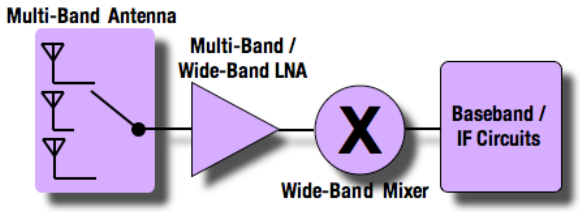


Figure 6.1: Multi-band receiver implementation using a multi-band/wide-band LNA.

A multi-band receiver can be implemented by using a single multi-band or wide-band LNA, as shown in Figure 6.1 Cascode LNAs based on inductive source degeneration are not suitable for this implementation since it is extremely difficult to switch the three on-chip inductors to make the same cascode LNA work across all the required frequency bands without compromising performance. Multi-band receivers can also be implemented by using multiple narrow-band LNAs, each designed for a different

frequency band, as shown in Figure 6.2. If cascode LNAs with inductive degeneration are used for this implementation, the die area and the cost will both be prohibitively high.

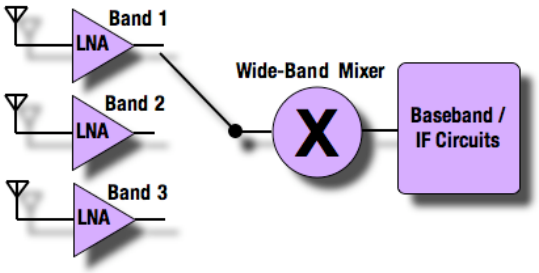


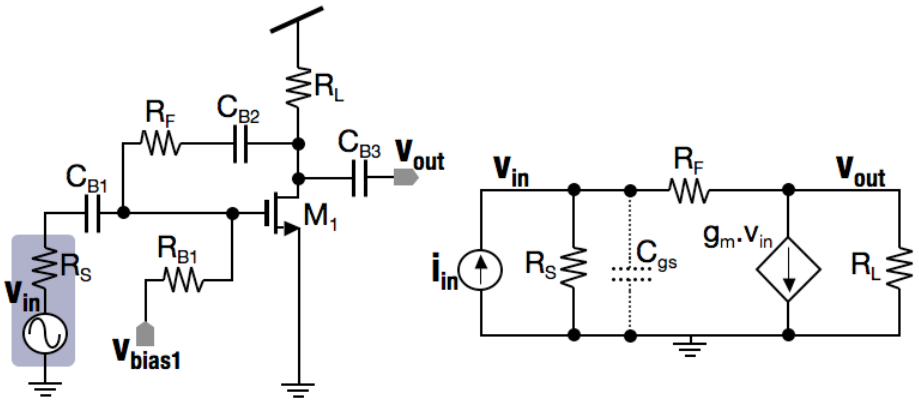
Figure 6.2: Multi-band receiver implementation using multiple narrow-band LNAs.

Inductor-less resistive feedback CMOS LNAs [67], [68] have been shown to be a viable option for implementing multi-band receivers as shown in Figure 6.1. These circuits require very small die area and can be implemented in a digital CMOS process without any additional RF enhancements. Hence, this approach can potentially reduce the cost of the wireless front-end implementation significantly. Resistive feedback LNAs achieve high gain and reasonably low noise figure [68]. However, novel circuit techniques are required to reduce power consumption and improve linearity.

6.2 Resistive Feedback LNA Theory

Consider a simplified resistive feedback amplifier, as shown in Figure 6.3(a). M_1 represents the input transconductance device, which could be a single transistor or a cascode pair. R_L represents the load resistance including the output resistance of the input

transconductance stage. R_F is the resistor implementing the shunt-shunt feedback. R_S is the source resistance and R_{B1} is used for biasing along with DC blocking capacitors C_{B1}, C_{B2}, and C_{B3}. The equivalent small-signal model of the transimpedance amplifier is shown in Figure 6.3(b) where g_m represents the transconductance of M_1. C_{gs} represents the capacitance to ground at the gate of M_1. For frequencies well below $1/(2\pi C_{gs}R_S)$, the effect of C_{gs} can be neglected.



(a) Schematic (b) Small-signal model

Figure 6.3: Simplified schematic and small-signal model of a shunt-shunt feedback amplifier.

6.2.1 Voltage Gain

Using the small-signal model in Figure 6.3(b), the voltage gain of the amplifier can be derived as:

Equation 6.1: $$A_v = \frac{v_{out}}{v_{in}} = -\left(g_m - \frac{1}{R_F}\right)\left(R_L \parallel R_F\right).$$

Feedback analysis [34] can be done by opening the loop, as shown in Figure 6.4, and determining the open-loop transresistance gain (a) and the feedback factor (f), as shown below.

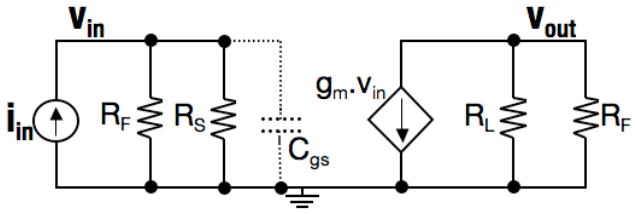


Figure 6.4: Open loop small-signal model of the shunt-shunt feedback amplifier.

Equation 6.2: $a = -(R_S \parallel R_F) g_m (R_L \parallel R_F)$

Equation 6.3: $f = -\dfrac{1}{R_F}$

The voltage gain given by feedback analysis is

Equation 6.4: $A_{v(Feedback\ Theory)} = -g_m (R_L \parallel R_F)$.

The discrepancy between Equation 6.1 and Equation 6.4 is because the feedforward path through R_F is ignored in the feedback analysis. This difference is negligible if $g_m >> 1/R_F$.

6.2.2 Input Impedance Matching

Shunt-shunt feedback reduces the input impedance of the amplifier by a factor of (1+*af*). The input resistance (R_{in}) of the amplifier is given by

Equation 6.5: $$R_{in} = \frac{(R_S \parallel R_F)}{1+af} \approx \frac{R_S}{1+af},$$

since $R_F >> R_S$ (for reasons, related to noise figure, explained later). For input impedance matching, R_{in} has to be equal to $R_S/2$. From Equation 6.5, input matching is achieved with a loop gain (*af*) just below 1, which also ensures circuit stability. Using Equation 6.3, the open-loop transresistance gain has to be approximately equal to the value of the feedback resistance for achieving input impedance matching.

Equation 6.6: ***Input Impedance Match Condition:*** $$|a| \approx R_F$$

6.2.3 Noise Figure

The contribution of each noise source to the total output noise is evaluated. Noise figure (*NF*) is then calculated by evaluating the ratio of the total output noise to the output noise due to R_S.

Equation 6.7: Output noise from source resistance, R_S: $\overline{v}_{out,R_S}{}^2 = \frac{4KT}{R_S} \bullet \left(\frac{a}{1+af} \right)^2$

Equation 6.8: Output noise due to M_1 $\overline{i}_d{}^2$:

$$\overline{v}_{out,M_1}{}^2 = 4KT \bullet \gamma_{g_m} \bullet g_m \bullet R_{out}{}^2 = 4KT \bullet \gamma_{g_m} \bullet g_m \bullet \left(\frac{R_L \parallel R_F}{1+af} \right)^2$$

where γ_{g_m} is the noise excess factor of M_1 [69].

Equation 6.9: Output noise from load resistance, R_L:

$$\overline{v}_{out,R_L}{}^2 = \frac{4KT}{R_L} R_{out}{}^2 = \frac{4KT}{R_L} \bullet \left(\frac{R_L \parallel R_F}{1+af} \right)^2$$

Equation 6.10: Output noise from feedback resistance, R_F:

$$\overline{v}_{out,R_F}{}^2 = 4KTR_F \bullet \left(A_{R_F \to Out} \right)^2$$

where $A_{R_F \to Out}$ is the voltage gain from the voltage noise source of R_F to the output given by:

Equation 6.11: $A_{R_F \to Out} = \frac{-\left(1+g_m R_S\right) \bullet R_L}{R_S + R_F + \left(1+g_m R_S\right) \bullet R_L} = \frac{-1}{1 + \frac{R_F + R_S}{\left(1+g_m R_S\right) \bullet R_L}}$.

Noise figure of this circuit can now be evaluated as shown below.

Equation 6.12: $NF = \frac{\overline{v}_{out,R_S}{}^2 + \overline{v}_{out,M_1}{}^2 + \overline{v}_{out,R_L}{}^2 + \overline{v}_{out,R_F}{}^2}{\overline{v}_{out,R_S}{}^2} = 1 + \frac{\overline{v}_{out,M_1}{}^2}{\overline{v}_{out,R_S}{}^2} + \frac{\overline{v}_{out,R_L}{}^2}{\overline{v}_{out,R_S}{}^2} + \frac{\overline{v}_{out,R_F}{}^2}{\overline{v}_{out,R_S}{}^2}$

Equation 6.8 ÷ Equation 6.7 and substituting Equation 6.2 give:

Equation 6.13: $$\frac{\bar{v}_{out,M_1}^{\ 2}}{\bar{v}_{out,R_S}^{\ 2}} = \frac{\gamma_{g_m} \bullet g_m \bullet \left(R_L \parallel R_F\right)^2 \bullet R_S}{\left(-\left(R_S \parallel R_F\right) \bullet g_m \bullet \left(R_L \parallel R_F\right)\right)^2} = \frac{\gamma_{g_m} \bullet R_S}{\left(R_S \parallel R_F\right)^2 \bullet g_m} \approx \frac{\gamma_{g_m}}{R_S g_m}$$

Equation 6.9 ÷ Equation 6.7 and substituting Equation 6.2 give:

Equation 6.14:
$$\frac{\bar{v}_{out,R_L}^{\ 2}}{\bar{v}_{out,R_S}^{\ 2}} = \frac{\left(R_L \parallel R_F\right)^2 \bullet R_S}{R_L \bullet \left(-\left(R_S \parallel R_F\right) \bullet g_m \bullet \left(R_L \parallel R_F\right)\right)^2} = \frac{R_S}{\left(R_S \parallel R_F\right)^2 \bullet g_m^{\ 2} R_L} \approx \frac{1}{R_S R_L g_m^{\ 2}}$$

Equation 6.10 ÷ Equation 6.7 gives:

Equation 6.15: $$\frac{\bar{v}_{out,R_F}^{\ 2}}{\bar{v}_{out,R_S}^{\ 2}} = R_F R_S \bullet \left(\frac{\left(1 + af\right) \bullet A_{R_F \to Out}}{a}\right)^2$$

Equation 6.15 can be further simplified by using Equation 6.6 as shown below.

Equation 6.16: $$\frac{\bar{v}_{out,R_F}^{\ 2}}{\bar{v}_{out,R_S}^{\ 2}} \approx \frac{4R_S}{R_F} \bullet \left(\frac{-1}{1 + \frac{R_F + R_S}{\left(1 + g_m R_S\right) \bullet R_L}}\right)^2$$

Substituting Equation 6.13, Equation 6.14, and Equation 6.16 into Equation 6.12 gives:

Equation 6.17:
$$NF \approx 1 + \frac{\gamma_{g_m}}{R_S g_m} + \frac{1}{R_S R_L g_m^{\,2}} + \frac{4R_S}{R_F}\left(\frac{-1}{1+\frac{R_F + R_S}{(1+g_m R_S)R_L}}\right)^2$$

Equation 6.17 shows that having a large feedback resistance can lower the noise figure. From Equation 6.6, a higher R_F requires a higher open-loop gain for input matching, usually leading to higher power consumption.

6.2.4 Linearity

Consider a non-linear amplifier modeled by the power series [69]:

Equation 6.18:
$$v_{out} = a_1 v_{in} + a_2 v_{in}^{\,2} + a_3 v_{in}^{\,3}$$

Negative feedback improves its input IP3 by the following factor:

Equation 6.19:
$$\frac{IP3\,|_{CL}}{IP3\,|_{OL}} = (1 + a_1 f)^2 \sqrt{\frac{a_3}{a_3(1 + a_1 f) - 2 f a_2^{\,2}}} \approx (1 + a_1 f)^{3/2}$$

where $2fa_2^{\,2} << a_3(1+a_1 f)$. $IP3|_{CL}$ and $IP3|_{OL}$ represent the close-loop IP3 and open-loop IP3, respectively. Equation 6.19 shows that linearity is not significantly improved by feedback at high frequencies if the open-loop gain of the amplifier rolls-off.

6.3 Inductorless Resistive Feedback LNAs with Improved Linearity

The linearity of a resistive feedback LNA can be improved by increasing its open loop bandwidth and by reducing component nonlinearities whenever possible. The resistive feedback LNAs in [68] had used positive feedback to increase bandwidth. These circuits also had DC blocking capacitors in the feedback path. The parasitic capacitance to substrate at the two terminals of this capacitor increased the loading of the source follower in the feedback path making it more non-linear.

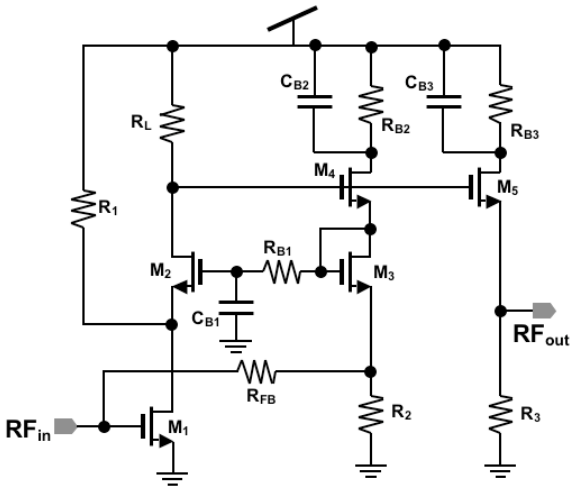
A resistive feedback broadband LNA (BLNA-1) with higher linearity is implemented as shown in Figure 6.5(a). It is based on a g_m-enhanced cascode formed by M_1, M_2, and R_1. While the source follower formed by M_4, M_3, and R_2 is part of the feedback loop, a separate source follower (M_5 and R_3) is used to improve reverse isolation and output drive capability. In order to obtain higher linearity without increasing power consumption the following modifications were made:

- DC feedback is implemented in the same small-signal feedback loop to avoid using blocking capacitor. The voltage across the diode-connected M_3 is used to bias M_1 and M_2.
- The open loop bandwidth is increased by reducing capacitive loading at the output node of the cascode.
- Positive feedback is avoided.

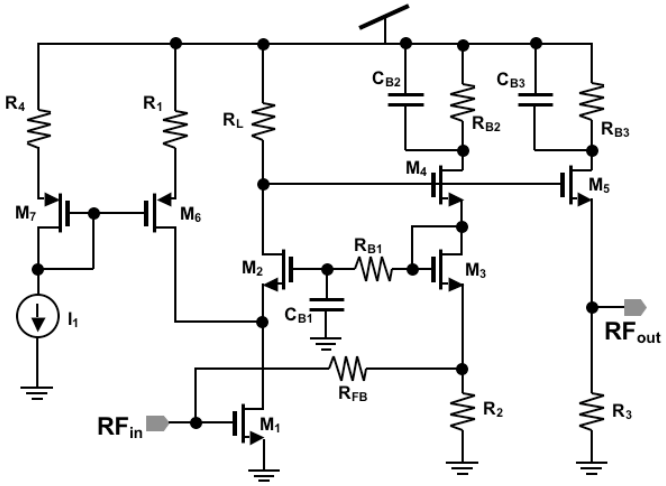
- Non-linear elements in the circuits are replaced whenever possible: for example, current sources are replaced by resistors.

In the resistive feedback LNA (BLNA-2) [70] in Figure 6.5(b), a current mirror, formed by M_6, M_7, R_1, and R_4, replaces the resistor R_1 in Figure 6.5(a). This increases the effective g_m of the cascode by reducing loss of small signal current through R_1 in BLNA-1. Hence, the load resistance can be lowered in BLNA-2 without sacrificing gain. This increases the open loop bandwidth and thus increases linearity as explained before. Reducing I_1 can lower the power consumption of the amplifier when necessary. The LNA can thus operate in either the nominal mode or a lower power mode. In the low power mode operation, a 50% power saving is achieved with only a slight performance degradation.

The modified super-source follower in [68] is used as a 50Ω-output buffer to facilitate measurements of the resistive feedback LNAs. These circuits are fabricated in a 90 nm, 7 metal CMOS process. While options like Metal-Insulator-Metal (MIM) capacitors are available in this process, the only RF enhancement option used in this implementation is the high resistivity substrate below RF signal paths. The capacitors are implemented as inter-digitated metal finger capacitors.



(a) BLNA-1



(b) BLNA-2

Figure 6.5: Schematics of the improved linearity resistive feedback LNAs.

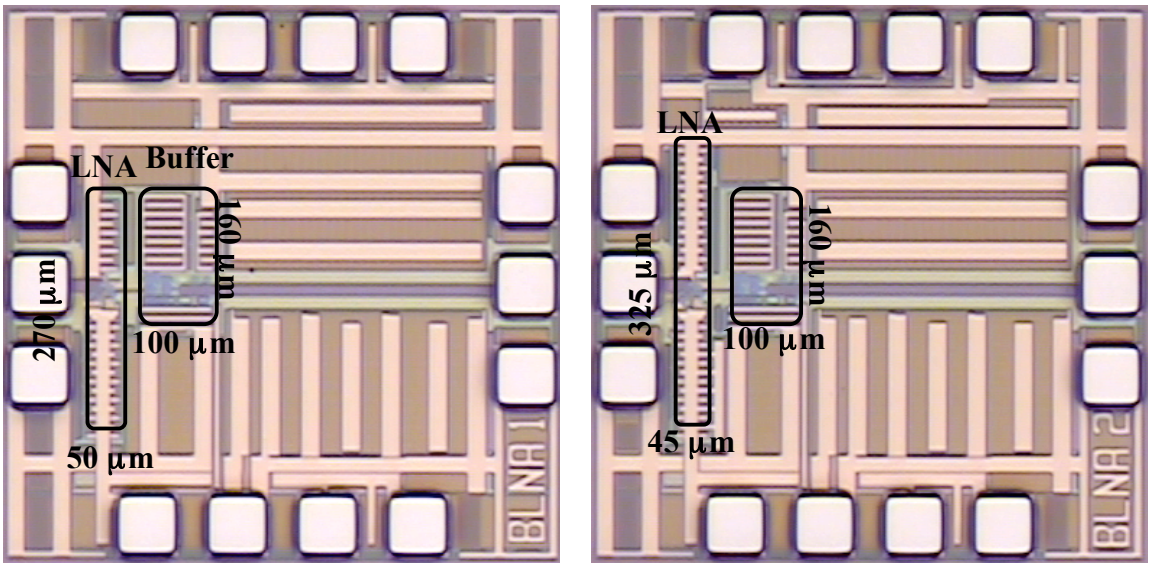


Figure 6.6: Chip micrographs of BLNA-1 and BLNA-2.

The chip micrographs of BLNA-1 and BLNA-2 are shown in Figure 6.6. All measurements are performed through on-wafer probing. A standalone output-buffer was also measured to de-embed the effects of the buffer on the LNA measurements. The buffer has an insertion loss of about 7 dB and its iIP3 is above 15 dBm from 500 MHz to 6 GHz.

Figure 6.7 - Figure 6.10 show the measured gain, input matching, noise figure, and input IP3 of BLNA-1. This LNA has a measured gain of 25.5 dB and a bandwidth of 7.93 GHz. At 5 GHz, it has a noise figure of 2.2 dB and an input IP3 of –7.7 dBm. This LNA occupies an active die area of 270 µm x 50 µm and consumes 16 mA from a 2.7 V supply.

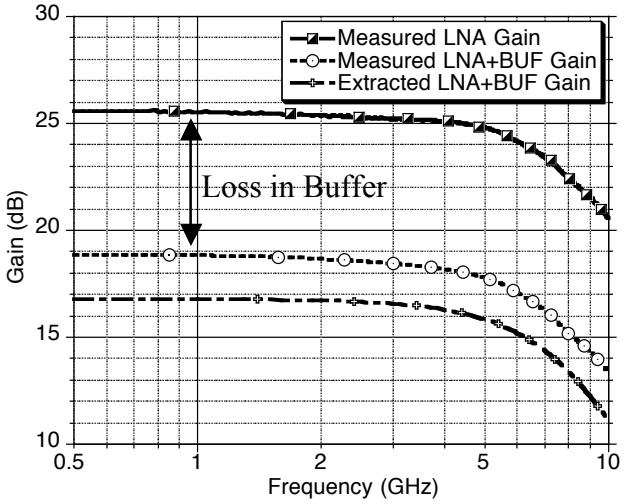


Figure 6.7: Measured gain of BLNA-1.

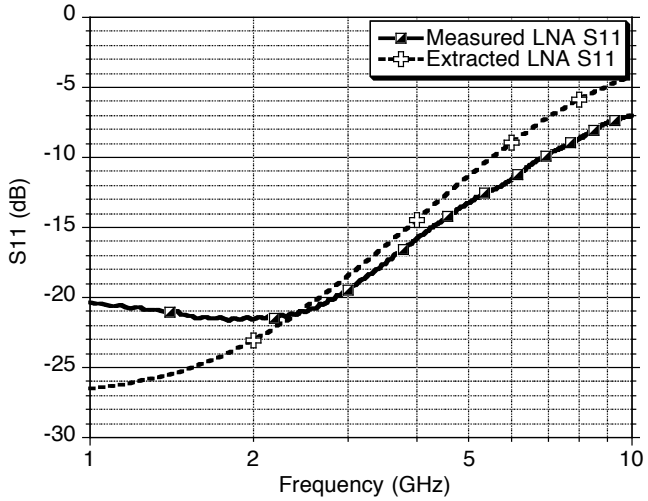


Figure 6.8: Input matching of BLNA-1

Also shown in Figure 6.7 - Figure 6.9 are the simulated gain, input matching, and noise figure after RC extraction. The measured gain performance is higher than the RC extracted simulation results due to slightly higher values of R_L and R_{FB}.

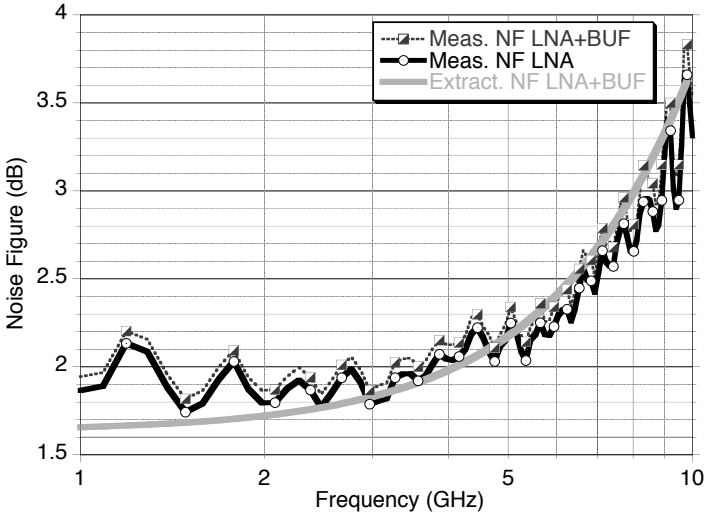


Figure 6.9: Measured noise figure of BLNA-1.

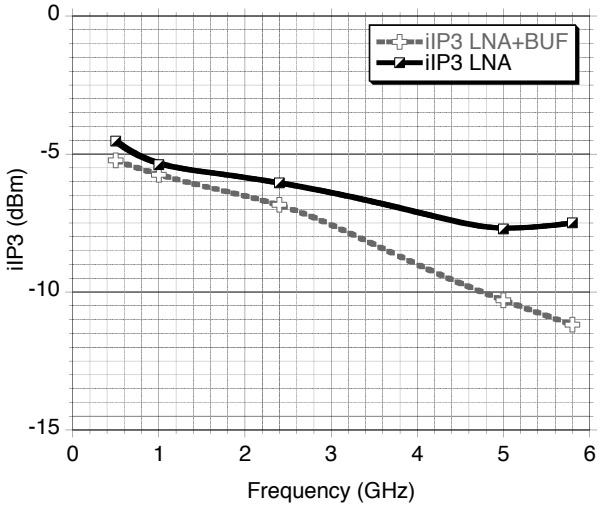


Figure 6.10: Input IP3 of BLNA-1.

The measured results of BLNA-2 are shown in Figure 6.11 - Figure 6.14. The results are plotted for both the nominal (15.5 mA, 2.7 V) and the low-power (8mA, 2.7 V) modes. BLNA-2 achieves a gain of 25.7 dB and 24.2 dB in the nominal and the low-power modes, respectively. At 5 GHz, it has a noise figure of 2.2 dB in the nominal mode

and 2.7 dB in the low-power mode. The input IP3 of BLNA-2 at 5 GHz is –8 dBm in the nominal mode and –6.1 dBm in the low-power mode.

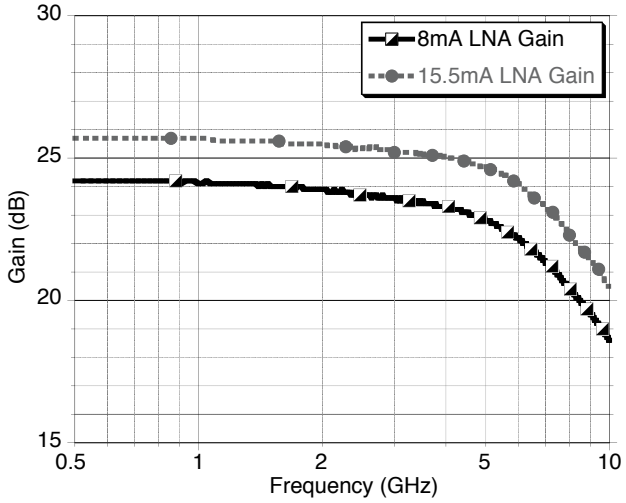


Figure 6.11: Measured gain of BLNA-2 for the nominal and low-power modes.

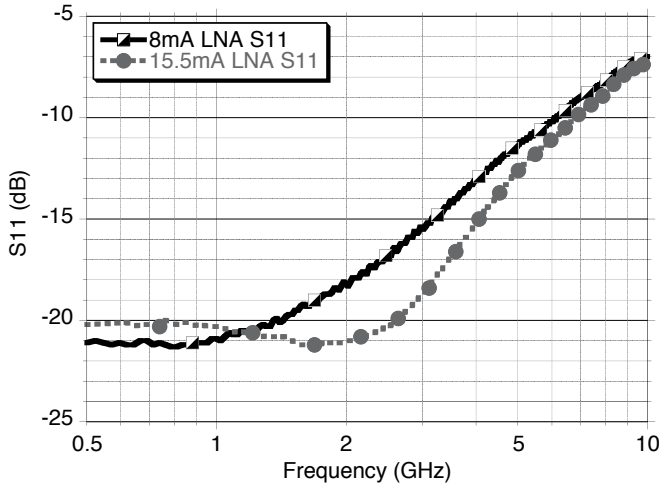


Figure 6.12: Input matching of BLNA-2.

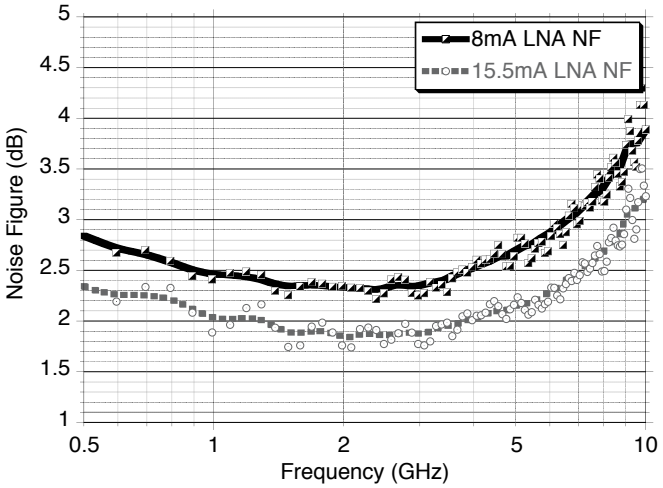


Figure 6.13: Measured noise figure of BLNA-2.

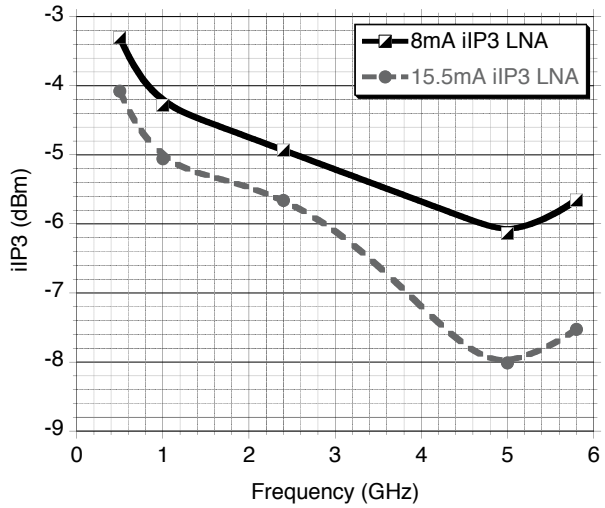


Figure 6.14: Measured input IP3 of BLNA-2.

The power consumption was lowered from 43.2 mW in BLNA-1 to 21.6 mW in the low-power mode of BLNA-2. When the input signal has sufficient SNR (signal to noise ratio), BLNA-2 can operate in the low power mode without sacrificing input matching,

gain or linearity. This is extremely important since in most LNA implementations, either the gain, linearity or input matching must be compromised in low power mode operation.

6.4 Low-Power Inductorless Resistive Feedback LNA

Current-reuse can be used to further reduce power consumption in inductorless LNAs. The schematic of a restive feedback LNA with current-reuse transconductance-boosting [72] is shown in Figure 6.15. Cascode transistors M_1 and M_3 form the input transconductance stage. A significant portion of the bias current in M_1 is diverted away from the load resistor R_L by transistor M_2. This reduces the DC voltage drop across R_L. Moreover, the transconductance generated by M_2 adds to that of M_1, increasing the effective g_m of the input stage. The current mirror formed by M_7 and M_8 controls the amount of current shunted away from R_L.

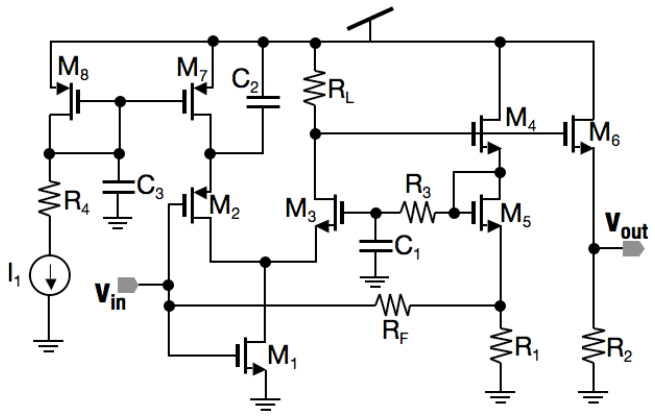


Figure 6.15: Schematic of the current-reuse transconductance-boosting resistive feedback LNA (BLNA-3).

The amplified signal is fed back to the input transconductance stage through feedback resistor R_F and the source follower formed by M_4, M_5, and R_1. The diode connected M_5 is used in the source follower to generate gate bias voltages for M_1, M_2, and M_3. The DC and AC feedback loops are combined as in BLNA-1 and BLNA-2, making it possible to remove the DC blocking capacitors required in earlier reports [68]. This reduces the total area requirement, and avoids loading of the source follower by the parasitic capacitance of the DC blocking capacitor to the substrate. The latter improves the LNA linearity as explained before.

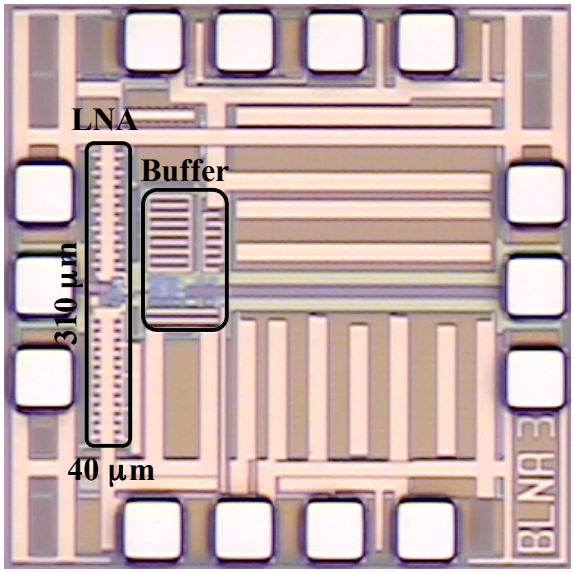


Figure 6.16: Chip micrograph of the current-reuse transconductance-boosting resistive feedback LNA.

The current-reuse transconductance-boosting resistive feedback LNA draws 6.7 mA from the 1.8 V supply, thus consuming 12 mW of power. The chip micrograph of this

LNA is shown in Figure 6.16. The chip is pad-limited and the actual LNA dimensions are 40 μm x 310 μm (Area: 0.012 mm^2).

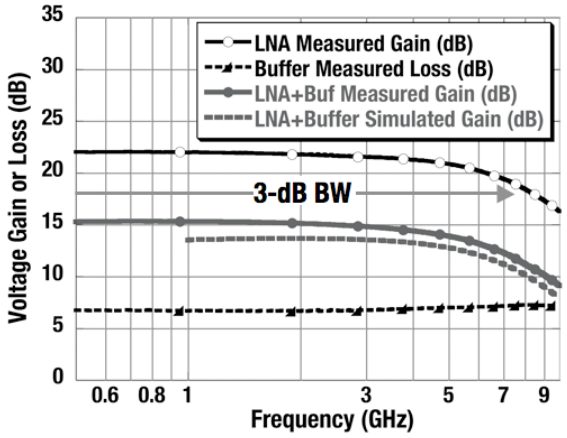


Figure 6.17: Measured and simulated gain of the current-reuse transconductance-boosting resistive feedback LNA and output buffer.

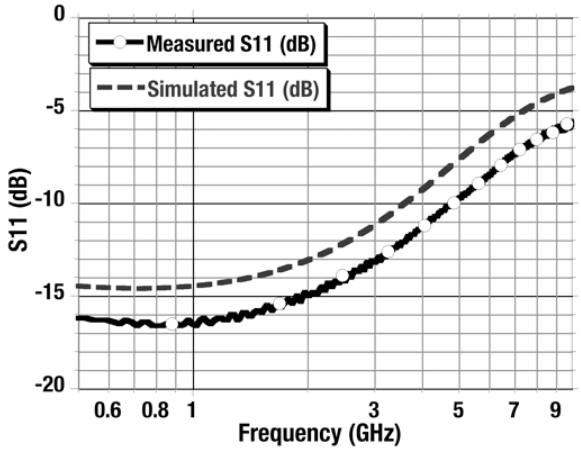


Figure 6.18: Measured and simulated input matching of the resistive feedback LNA.

The measured and simulated gain of the LNA and output buffer is shown in Figure 6.17. Also plotted in Figure 6.17 are the buffer loss and the de-embedded LNA gain. The gain falls from 22 dB at low frequencies to 21 dB at 5 GHz. The 3-dB bandwidth is 7.5 GHz. The measured and simulated input matching of the LNA are plotted in Figure 6.18. It is -10 dB at 5 GHz and better at lower frequencies.

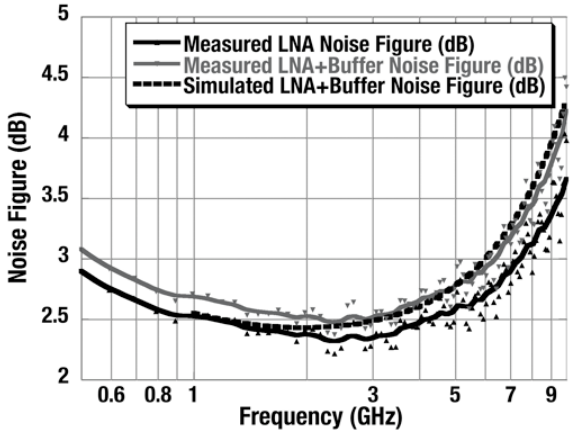


Figure 6.19: Measured and simulated noise figure of the LNA and output buffer.

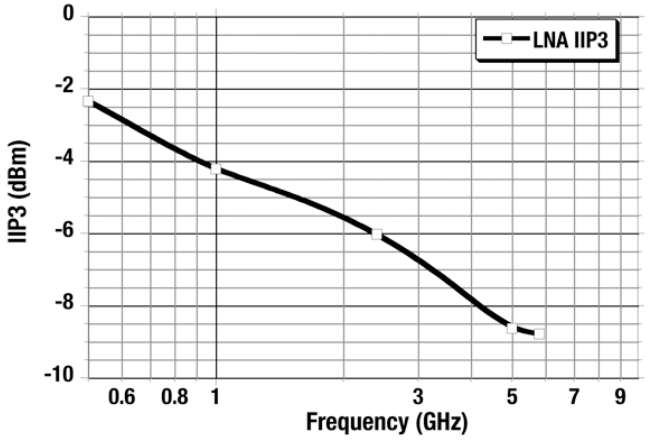


Figure 6.20: Measured input IP3 of the current-reuse transconductance-boosting LNA.

The measured noise figure is plotted against frequency in Figure 6.19. The noise figure is 2.6 dB at 5 GHz and varies between 2.3 dB and 2.9 dB from 500 MHz to 7 GHz. The 1.5 dB increase in gain in the measured results is due to slightly higher values for R_L and R_F. This increase in gain leads to improved input matching and noise performance compared to the simulated results. The input IP3 of the LNA is plotted in Figure 6.20 after de-embedding the effects of the output buffer. It varies from -2.3 dBm at 500 MHz to -8.8 dBm at 5.8 GHz. The degradation of linearity with frequency is due to the loop gain roll-off with frequency as explained before.

6.5 Resistive Feedback LNA with Nonlinearity Cancellation

In tuned LNAs based on inductive source degeneration, the main IP3 limitation is often due to the transconductance non-linearity in the input transistor. Several linearity improvement techniques like derivative superposition [25], modified derivative superposition [73], and active post-distortion [73] have been demonstrated for the cellular band (869-894 MHz). In these techniques, the cascode transistor is assumed to be linear.

In all resistive feedback LNAs with g_m-enhanced cascode structure, the W/L ratio of the cascode transistor is kept low to achieve a higher bandwidth. The cascode device also has a lower bias current than the input transistor so as to reduce the voltage drop across the load resistor as explained before. The lower W/L ratio and bias current makes the transconductance of the common-gate cascode transistor significantly lower than the

common-source input transistor. The gain of the common-source stage is the ratio of these transconductances. The high gain in the common-source input stage preceding the cascode stage makes the g_m non-linearity in the cascode stage limit the overall circuit linearity. This is because the IIP3 of the combined stages ($IIP3_{CS\text{-}CG}$) is related to the IIP3 of the common-source stage ($IIP3_{CS}$), its gain (G_{CS}), and the IIP3 of the common-gate stage ($IIP3_{CG}$) by the following equation:

Equation 6.20: $$\frac{1}{(IIP3_{CS-CG})^2} = \frac{1}{(IIP3_{CS})^2} + \left(\frac{G_{CS}}{IIP3_{CG}}\right)^2.$$

Hence, significant improvement in linearity can be obtained if the non-linearity of the cascode stage is reduced by non-linearity cancellation. This can be achieved by using derivative superposition [24], [25].

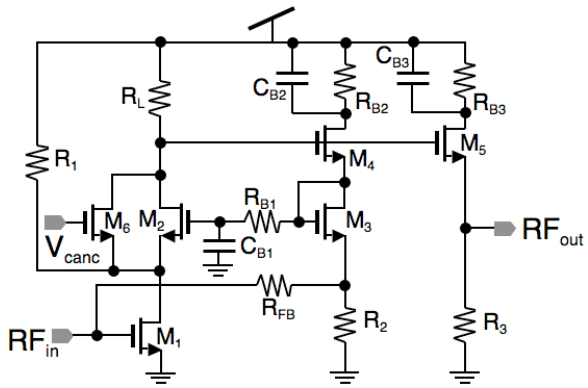


Figure 6.21: Schematic of the resistive feedback LNA with nonlinearity cancellation.

The schematic of the non-linearity cancellation resistive feedback LNA [74] is shown in Figure 6.21. Transistors M_1, M_2 and resistor R_1 form a g_m-enhanced cascode amplifier. The output at the load resistor R_L is fed back to the input through a source follower (M_4), a level shifter (M_3) and the feedback resistor R_{FB}. Another source follower (M_5 and R_3) is used to drive the 50-Ω output buffer as explained earlier. Resistors R_{B2} and R_{B3} protect the transistors in the two source followers from breakdown. The level shifter M_3 is used to bias the g_m-enhanced cascode by forming a DC feedback loop. The IP3 of the circuit is kept high even without cancellation by reducing non-linearities in the loop and by increasing the open-loop bandwidth as described before. Transistor M_6 is used to cancel the IP3 limiting non-linearity of the cascode transistor M_2 in the high-linearity mode. The cancellation is turned on and off by changing the gate voltage of M_6 with little effect on the gain and input matching of the LNA. Non-linearity cancellation is achieved when the g_{m3} ($\delta^3 I_D/\delta V^3_{GS}$) of M_6 cancels that of M_2 [25]. While M_6 is in weak-inversion for g_{m3} cancellation in the high-linearity mode, it is biased in strong-inversion region for the low-noise mode. The chip microphotograph is shown in Figure 6.22. It occupies an active die area of 325 μm x 50 μm.

This design is also implemented in a seven metal, 90 nm CMOS process. The LNA draws about 15.5 mA from a 2.7 V supply. The following measurement results are plotted after de-embedding the 50-Ω output stage, which was characterized separately. The gains of the LNA in the two modes are plotted in Figure 6.23. In the high-linearity mode, the LNA has a gain of 24.4 dB with 6.2 GHz of bandwidth. In the low-noise mode, it has a gain of 25.2 dB with 7.25 GHz of bandwidth. The input matching for the two

modes is shown in Figure 6.24. S_{11} is lower than –11 dB at 5 GHz and better at lower frequencies in both the modes.

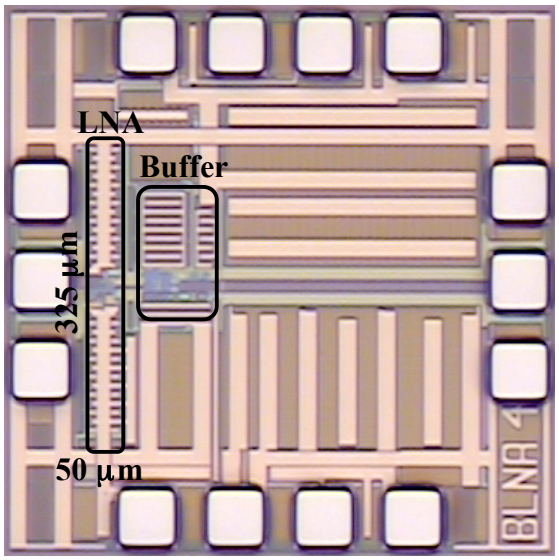


Figure 6.22: Chip micrograph of the nonlinearity cancellation LNA.

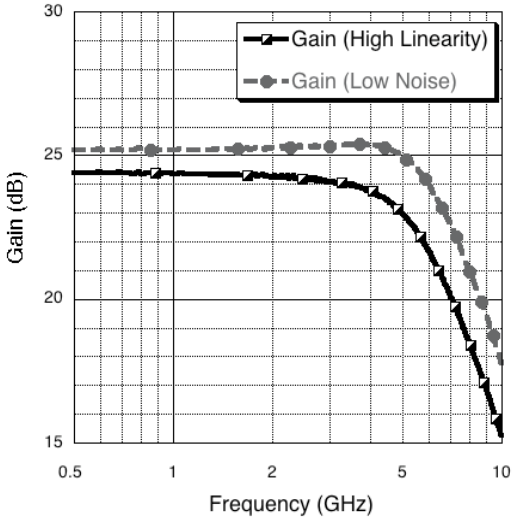


Figure 6.23: Measured gain of the LNA in high linearity and low noise modes.

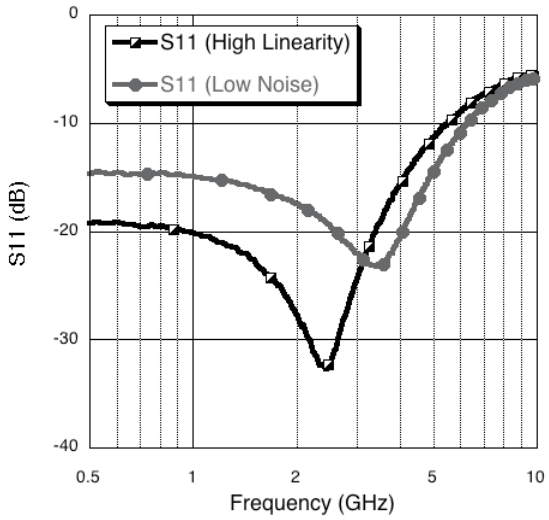


Figure 6.24: Measured input matching of the nonlinearity cancellation LNA.

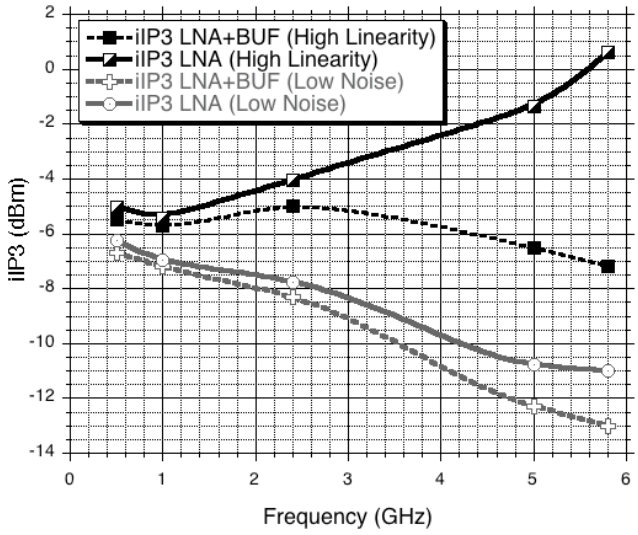


Figure 6.25: Measured input IP3 of the LNA.

The input-IP3s of the LNA in the two modes are plotted in Figure 6.25. Both the measured iIP3 and the de-embedded iIP3 are plotted. In the high-linearity mode, the measured iIP3 at high frequencies is limited by the non-linearity in the output buffer. While the iIP3 degrades with frequency in the low-noise mode, it improves with

frequency in the high-linearity mode showing that the cancellation achieved is frequency dependent. The variation of the IIP3 with the gate bias voltage of M_6 is plotted in Figure 6.26.

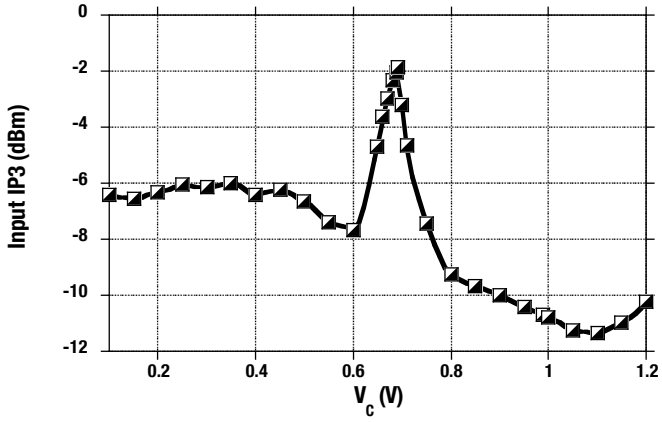


Figure 6.26: Measured input IP3 plotted against the gate bias voltage of M_6.

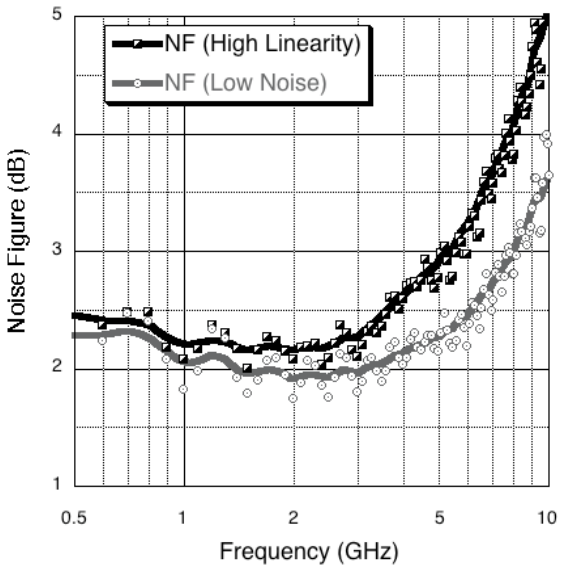


Figure 6.27: Measured noise figure of the LNA in the high linearity and low noise modes.

The noise figure of the LNA is plotted in Figure 6.27. There is little difference in the noise figures for the two modes at lower frequencies since the transistor biased in weak inversion is not placed directly at the input. However at higher frequencies, the noise penalty due to cancellation increases because of the faster gain roll-off in the high-linearity mode. At 5 GHz, for example, the noise figure increases from 2.3 dB to 2.9 dB when cancellation is applied.

6.6 Tuned Resistive Feedback LNA Using Compact Low-Q Inductive Load

Linearity issues due to the high gain in the common-source stage preceding the common-gate cascode stage can be avoided by replacing the load resistance with a low-Q resonant load, using a compact on-chip inductor. The bias current of the cascode device can be made equal to that of the input device because the DC voltage drop across the resonant load is negligible. Since all the capacitance at the output node can be resonated out with the inductive load, it is not necessary to make the W/L ratio of the cascode device small.

The schematic of a tuned resistive feedback LNA (TRFL) [76] is shown in Figure 6.28. Transistor M_1 is used as the common-source transconductance stage and M_2 as the cascode common-gate stage. A compact low-Q on-chip spiral inductor L_1 and the total capacitance at the output node form the resonant load. The parasitic capacitance of the DC block capacitors (C_{C2} and C_{C3}) to substrate and the drain capacitance of M_2 can

therefore be resonated out along with the load capacitance at the output node. Resistors R_{FB1}, R_{FB2}, and R_{FB3} form the shunt-shunt feedback path. Capacitors C_{B1} and C_{B2} and resistor R_{B1} are used for biasing the cascode transistors.

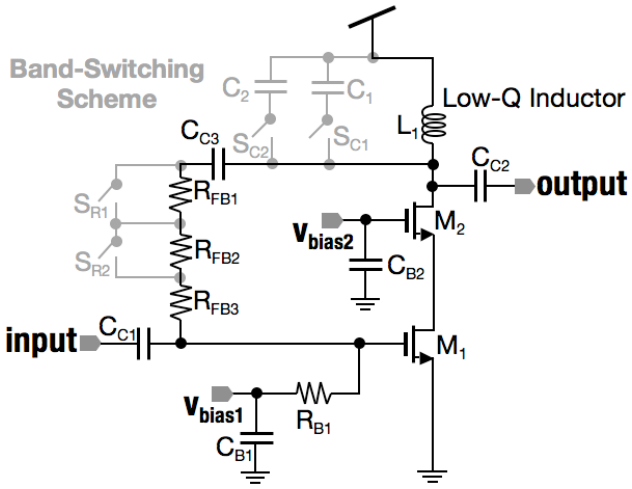


Figure 6.28: Schematic of the tuned resistive feedback LNA (TRFL) utilizing a compact low-Q load inductor.

Since this LNA utilizes only a single low-Q load inductor, it can be made extremely compact. Hence, low-cost multi-band receivers can be implemented by using multiple tuned resistive feedback LNAs each designed for a different frequency band, as shown in Figure 6.2.

This circuit can be easily modified to operate across different frequency bands for the multi-band receiver implementation shown in Figure 6.1. The band-switching scheme enabling this implementation is shown in Figure 6.28. The resonant frequency, f_r, can be

shifted by using the capacitors C_1 and C_2, and the switches S_{C1} and S_{C2}. At resonance, the load impedance is purely resistive and given by:

Equation 6.21: $$R_{L,fr} = 2\pi f_r L_{fr}\left(Q_{fr} + \frac{1}{Q_{fr}}\right).$$

Here, L_{fr} and Q_{fr} are the inductance and Q of the load inductor at the resonant frequency f_r. All the equations from section 6.2 are still valid if R_L is replaced by $R_{L,fr}$, and if g_m represents the effective transconductance of the cascode stage.

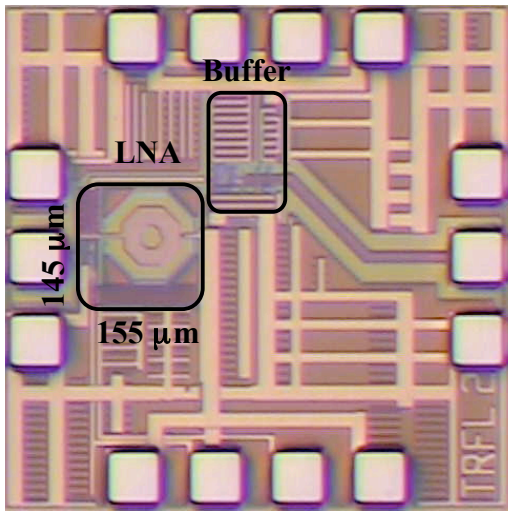


Figure 6.29: Chip micrograph of the tuned resistive feedback LNA.

If the switches S_{C1} and S_{C2} are used to shift f_r, the value of $R_{L,fr}$, given by Equation 6.21, will not be the same in different frequency bands. Thus the open-loop trans-impedance gain (a), given by Equation 6.2, will also vary from one frequency band to another. To satisfy the input matching condition in Equation 6.6 across all the frequency

bands, the feedback resistance R_{FB} will also have to be switched, as shown in Figure 6.28 using switches S_{R1} and S_{R2}.

The tuned resistive feedback LNA has a power consumption of 9.2 mW, drawing 7.7 mA from the 1.2 V supply. Band switching is not implemented and the LNA is designed to operate in a single frequency band around 5.5 GHz. The chip micrograph of this circuit is shown in Figure 6.29. The LNA dimensions are 155 μm x 145 μm (Area: 0.022 mm^2).

The stand-alone output buffer used with the tuned resistive feedback LNA is similar to the one used earlier for other measurements and has a loss of 8 dB, and a noise figure of 9.8 dB (including the noise added by the 50-Ω resistor at the input). The output buffer has an input 1-dB compression point of 6.5 dBm and an input IP3 of 18 dBm at 5.5 GHz.

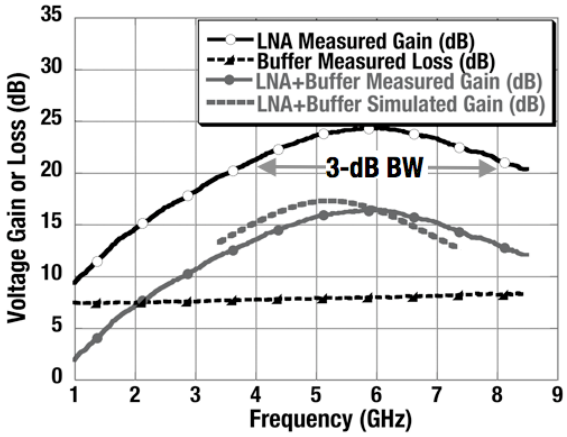


Figure 6.30: Measured and simulated gain of the tuned resistive feedback LNA and output buffer.

The measured and simulated gain of the LNA and output buffer is plotted in Figure 6.30. The buffer loss and the de-embedded gain of the LNA without the buffer are also plotted in Figure 6.30. The LNA has a maximum gain of 24.4 dB and a 3-dB bandwidth of 3.94 GHz from 4.04 GHz to 7.98 GHz. The measured input matching is plotted in Figure 6.31. The input matching is better than -10 dB from 5 GHz to 6.85 GHz.

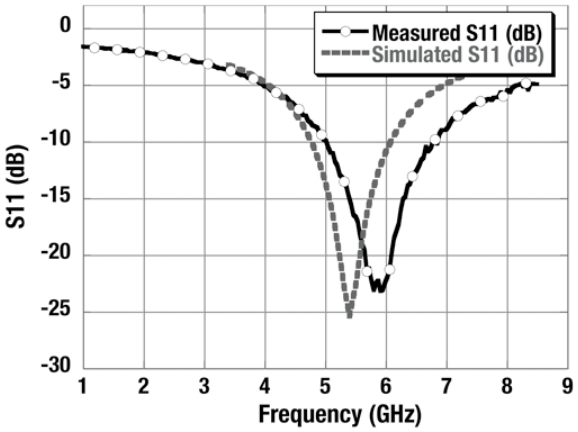


Figure 6.31: Measured and simulated input matching of the tuned resistive feedback LNA.

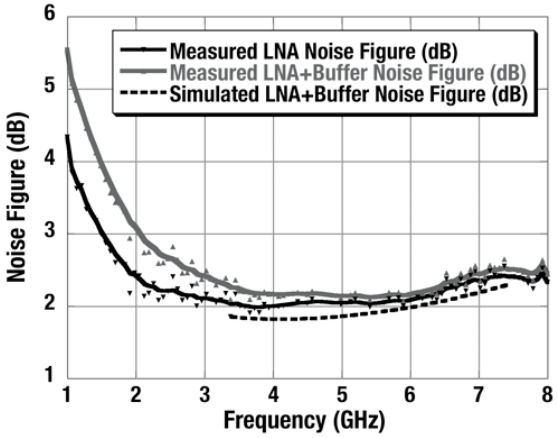


Figure 6.32: Measured and simulated noise figure of the TRFL and output buffer.

Figure 6.32 shows the measured and simulated noise figure of the tuned resistive feedback LNA and the output buffer. The de-embedded noise figure of the LNA without the output buffer is also plotted. The tuned resistive feedback LNA has a noise figure of about 2 dB between 4GHz and 6 GHz.

The IP3 of the LNA and output buffer is plotted in Figure 6.33. The input IP3 of the tuned resistive feedback LNA and output buffer is -7.7 dBm at 5.5 GHz. The IIP3 of the LNA is found to be -2.6 dBm after de-embedding the output buffer non-linearity using the IIP3 of the stand-alone buffer (18 dBm) and the gain of the LNA (24.1 dB). Therefore, the output IP3 of the LNA is 21.5 dBm. The measured input 1-dB compression point of the LNA and buffer is -18 dBm at 5.5 GHz. The input 1-dB compression point of the LNA without the output buffer is found to be -7.2 dBm after de-embedding.

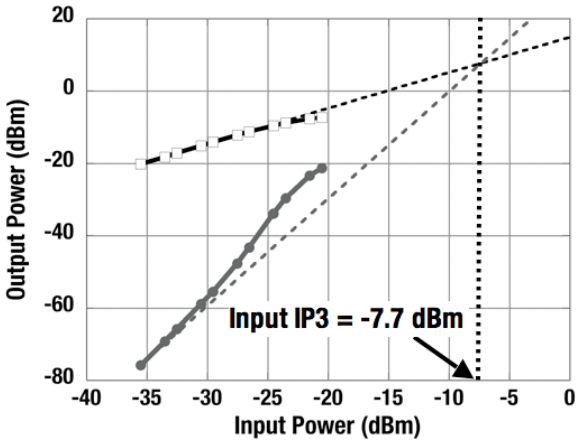


Figure 6.33: Measured input IP3 of the tuned resistive feedback LNA.

6.7 Summary

Extremely compact resistive feedback LNAs are presented as a cost-effective alternative to tuned LNAs using multiple high-Q inductors. Though these circuits are vital in reducing the area requirement in multi-band, multi-standard, and MIMO systems, these concepts can also be used in implementing very low-cost WPAN systems. The relationships between the feedback resistance, noise figure, input matching, and open-loop gain are presented. The effect of the open-loop bandwidth on the close-loop linearity is also explained.

A current-reuse transconductance boosting technique is used to reduce the power consumption in a resistive feedback LNA (BLNA-3) to 12 mW. The inductor-less LNA achieves a gain of 21 dB and a noise figure of 2.6 dB at 5 GHz. The roll-off of loop-gain and the non-linearities in the feedback loop are reduced to improve the output IP3 to 12.3 dBm at 5 GHz. The active die area of this LNA is only 0.012 mm^2. A tuned resistive feedback LNA (TRFL), using a compact resonant load, is also presented. It achieves a maximum gain of 24.4 dB and a 3-dB bandwidth of 3.94 GHz using a single low-Q on-chip inductor and consuming 9.2 mW of power. The LNA has an active die area of 0.022 mm^2. The noise figure of the tuned resistive feedback LNA is about 2 dB between 4 GHz and 6 GHz. At 5.5 GHz, the LNA has an output IP3 of 21.5 dBm. The combination of high linearity, low noise figure, high broadband gain, small die area and low power consumption makes this LNA architecture a compelling choice for low-cost, multi-standard wireless front-ends.

The performance of all the resistive feedback LNAs presented (BLNA-1 to BLNA-4, and TRFL) are summarized and compared with [68] in Table 6.1. The power consumption is reduced from above 40 mW to 9.2 mW and the output IP3 is increased by about 10 dB.

Table 6.1: Performance comparison of BLNA-1 to BLNA-4 and TRFL with [68].

Circuit	Bandwidth (GHz)	Gain (dB)	NF (dB) @ 5 GHz	OIP3 (dBm) @ 5 GHz	Supply (V)	Power (mW)	LNA Area (mm^2)
[68] ISSCC 2006 pp. 200	8.22	24.73	2.1	11.72	2.7	41.36	~0.025
BLNA-1	7.93	25.52	2.2	17.1	2.7	43.2	0.013
BLNA-2 Nominal	7.65	25.7	2.2	16.7	2.7	41.85	0.014
BLNA-2 Low-Power	7.15	24.2	2.7	16.7	2.7	21.6	
BLNA-3	**7.5**	**21.95**	**2.6**	**12.26**	**1.8**	**12.06**	**0.012**
BLNA-4 High Lin.	6.18	24.38	2.9	21.16	2.7	41.85	0.016
BLNA-4 Low Noise	7.25	25.19	2.3	14.27	2.7	40.5	
TRFL	**3.94**	**24.4**	**2.0**	**21.5 @ 5.5 GHz**	**1.2**	**9.2**	**0.022**

The performance of BLNA-3 and TRFL are tabulated and compared with others reported in Table 6.2. The current-reuse transconductance-boosting resistive feedback LNA (BLNA-3) provides comparable performance at lower power consumption while occupying very small die area. The tuned resistive feedback LNA (TRFL), though requiring slightly larger die area than the inductor-less LNA, provides very high linearity, low noise, and high gain while dissipating low power. This LNA presents a significantly improved trade-off between performance, power consumption, and cost, especially for multi-band, multi-standard wireless receivers.

Table 6.2: Wide-band low noise amplifier performance comparison.

	[68] ISSCC 2006 pp. 200	[77] ISSCC 2007 pp. 422	[78] RFIC 2006 pp. 41	[79] ESSCIRC 2005, pp. 219	This Work BLNA-3	This Work TRFL
Process	90-nm CMOS	90-nm CMOS	130-nm CMOS	130-nm CMOS	90-nm CMOS	90-nm CMOS
Freq. (GHz)	0.5 – 8.2	0 - 6	3.1 – 10.6	3 – 5	0.5 – 7	4 - 8
Power (mW)	42	9.8	9	45	12	9.2
Area (mm^2)	0.025	0.0017	~0.33	~0.5	0.012	0.022
Voltage Gain (dB)	25	17.4	15.1	25.8	22	24.4
Noise Figure (dB)	1.9 – 2.6	2.5 – 3.3	2.1 – 2.9	3.6 – 4.4	2.3 - 2.9	2 – 2.4
OIP3 (dBm)	8.8 (5.8 GHz)	7 (5 GHz)	6.6 - 10	12.8	11.5 (5.8 GHz)	21.5 (5.5 GHz)

Chapter 7
Conclusions

The final chapter lists the technical contributions of this research in developing low-power and low-cost wireless front-end circuits in CMOS. Potential research directions for future related to this work are also presented.

7.1 Technical Contributions

- The potential of implementing low-power RF circuits in subthreshold CMOS is investigated. It is found that the higher transconductance to bias current ratio could be exploited in high frequency subthreshold circuits in deep sub-micron CMOS technologies. The issue of higher device noise in subthreshold circuits is alleviated by using passive voltage gain stages before the subthreshold device.

- The first fully monolithic micro-power LNA using subthreshold MOS devices and on-chip inductors is implemented at 1 GHz. The subthreshold LNA, fabricated in a 0.18 μm CMOS process, has a gain above 12 dB with supply voltages as low as 0.5 V (130 μW power consumption) leading to a potential use of such circuits well into the GHz range when utilizing advanced technology nodes (65nm and beyond) that support only low voltage circuits.

- LO injection at the bulk terminal is utilized to develop a new subharmonic CMOS mixer. The LO-to-RF isolation is found to be 35.2 dB for the fundamental and 67.1 dB for the more important second harmonic. The novel mixer architecture is thus suited for mitigating LO leakage issues especially in direct conversion receivers.

- An active APDP based mixing core is developed to implement 1X and 2X CMOS mixers consuming less than 460 μW of power. The same architecture is utilized in SiGe millimeter-wave down-conversion circuits to significantly reduce LO power requirement and improve subharmonic conversion loss.

- A micro-power variable gain amplifier is developed by combining variable degeneration gain control and variable load gain control. It achieves about 40 dB of dB-linear gain range while consuming only 250 μW of power.

- A fully integrated 2.4 GHz receiver was implemented in 0.18 μm CMOS process for low-power wireless PAN applications by replacing the conventional active low noise amplifier by a series-resonant passive network. The passive network provides both input matching and voltage amplification. Down conversion is performed by a novel subthreshold mixer with LO injection at the common source node. The 540-μW receiver achieves a measured gain of 24.7 dB, a noise figure of 7 dB, and an output IP3 of 7.7 dBm. The current consumption of 300 μA is the lowest reported for wireless receivers at 2.4 GHz with similar gain.

- The first fully monolithic subthreshold CMOS receiver is implemented with integrated subthreshold quadrature LO chain for 2.4 GHz WPAN applications. Subthreshold operation, passive voltage amplification, and various low-power circuit techniques such as current reuse, stacking, and differential cross coupling have been combined to lower the total power consumption. The subthreshold receiver, consisting of the switched-gain low noise amplifier, the quadrature mixers, and the variable gain amplifiers, consumes only 1.4 mW of power and has a gain of 43 dB and a noise figure of 5 dB. The entire quadrature LO chain, including a stacked quadrature VCO and differential cross-coupled buffers, also operates in the subthreshold region and consumes a total power of 1.2 mW. The subthreshold receiver with integrated LO generation is implemented in a 0.18 μm CMOS process. The receiver has a 3-dB IF bandwidth of 95 MHz.

- Extremely compact resistive feedback CMOS low noise amplifiers are presented as a cost-effective alternative to multiple narrow band LNAs using high-Q inductors. Limited linearity and high power consumption of the inductor-less resistive feedback LNAs are analyzed and circuit techniques proposed to solve these issues. The relationships between the feedback resistance, noise figure, input matching, and open-loop gain are presented. The effect of the open-loop bandwidth on the close-loop linearity is also explained. The LNAs are implemented in a 90 nm CMOS process and do not require any costly RF

enhancement options. The output IP3 is increased by about 10 dB by using the circuit techniques proposed in this work.

- A 12 mW resistive feedback LNA, based on current-reuse transconductance-boosting is presented with a gain of 21 dB and a noise figure of 2.6 dB at 5 GHz. The LNA achieves an output IP3 of 12.3 dBm at 5 GHz by reducing loop-gain roll-off and by improving linearity of individual stages. The active die area of the LNA is only 0.012 mm^2.

- A 9.2 mW tuned resistive feedback LNA utilizing a single compact low-Q, on-chip inductor is presented showing an improved trade-off between performance, power consumption, and die area. At 5.5 GHz, the fully integrated LNA achieves a measured gain of 24 dB, a noise figure of 2 dB, and an output IP3 of 21.5 dBm. The LNA draws 7.7 mA from the 1.2 V supply and has a 3-dB bandwidth of 3.94 GHz (4.04 – 7.98 GHz). The LNA occupies a die area of 0.022 mm^2. The combination of high linearity, low noise figure, high broadband gain, small die area and low power consumption makes this LNA architecture a compelling choice for low-cost, multi-standard wireless front-ends.

7.2 Recommendations for Future Work

The potential of subthreshold high-speed circuits is immense as technology scaling pushes subthreshold f_T even higher. Hence, it is extremely critical that more accurate subthreshold models are developed for radio frequencies. High frequency noise models are especially important if subthreshold CMOS is to be extensively used in wireless front-end applications.

Besides the low noise amplifiers, mixers, local oscillators and LO buffers implemented in subthreshold CMOS in this work, the feasibility of other high frequency circuits should also be investigated in weak inversion. A vital front-end block that was not included in this work is the frequency synthesizer. Thus significant contributions can be made in developing low-power wireless transceivers by exploring subthreshold frequency dividers and other PLL (phase locked look) circuits.

In high data rate systems, baseband circuits have to support high bandwidth and therefore require high power. With increasing digital baseband complexity, the power consumption in digital circuits is also increasing. Thus reducing the power consumption in the RF front-end blocks does not imply that the total power consumption would remain low. System and circuit research is essential in analog-to-digital converters, pulse shaping circuits, and digital baseband circuits to develop extremely low-power wireless systems.

Many of the subthreshold circuits implemented in this work utilized high-Q passives to achieve reasonable gain and noise performance. To reduce area requirement and cost, it is necessary to reduce the number of area intensive high-Q passive components. With technology scaling, it will be possible to operate resistive feedback RF circuits without any high-Q components in subthreshold region. This can lead to extremely low-cost micro-power wireless front-ends that will have countless medical, control, and monitoring applications.

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Invention Disclosures

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VITA

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