Avionics Architectures and Components for Planetary Entry Probe Payloads and Systems

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TEC-ED, ESA-ESTEC

Presentation Overview

Overview

Drivers for Avionics Technology Development
ESA Strategy & Reference Avionics Architecture
Network Elements and Components
Processing Node Elements and Components
Ongoing and Future Developments
ESA's IP Core Service

Drivers for development

Key drivers for Avionics Architectures and Components

- Increasing data rates: more data means more science
- More demand for processing power: data reduction / compression essential due to higher sensor data rates and limited TM bandwidth
- Low power consumption: power is a scarce resource
- Low mass: miniaturization is essential in particular for exploration / science missions
- Low cost: standardization of interfaces and building blocks allows re-use of developments, low avionics mass and power consumption allows mass and cost savings in other areas which can lead to smaller, lower cost spacecraft and missions

Example: System on a Chip Study for a Jupiter Entry Probe

SoC CDF Study for JEP

A GSP-funded Assessment Study was performed in 2007 in the ESTEC CDF (Concurrent Design Facility) with the following goals:

- ⇒ **Analyze the impact of replacing the traditional separated subsystem architecture by a System On A Chip**
- ⇒ **Assess impact on mass, power, volume, operability, complexity, risk, cost of Jupiter Entry Probe (JEP) and Jupiter Europa Orbiter (JEO)**

Study results (JEP)

Jupiter Entry Probe (JEP)	SoC Technology	Option 1			Option 2		
		0.18 µm ASIC 1 Mrad rad-hard			Custom mixed signal.		
		Anti-fuse FPGA (300 krad)					
	Avionics Reduction	kg	W	Volume	Kg	-W	Volume
		- 4	- 10	- 75 %	- 8	- 20	- 85%
	System Reduction	22 kg			- 775 Wh		

- ⇒ **5kg mass saving on avionics translates into 20kg saving on launch mass or a 20% increase in payload mass**
- ⇒ **Smaller, lighter probe, no significant risk increase, estimated 4% saving in Phase B-CD cost**

ESA Strategy – Av.& P/L

ESA strategy for supporting European avionics & payload component developments

- Development of Application Specific Standard Products (ASSP)
  - That are capable of answering many on-board computing and control needs for the future decade
- Adopt new ASIC developments to ESA ASSP strategy to
  - reduce development time and recurring cost.
- Ensure SpW nodes developed by ESA to be
  - easily integrated in ESA On-Board Distributed Computing and Control System

Standardization / Hierarchy

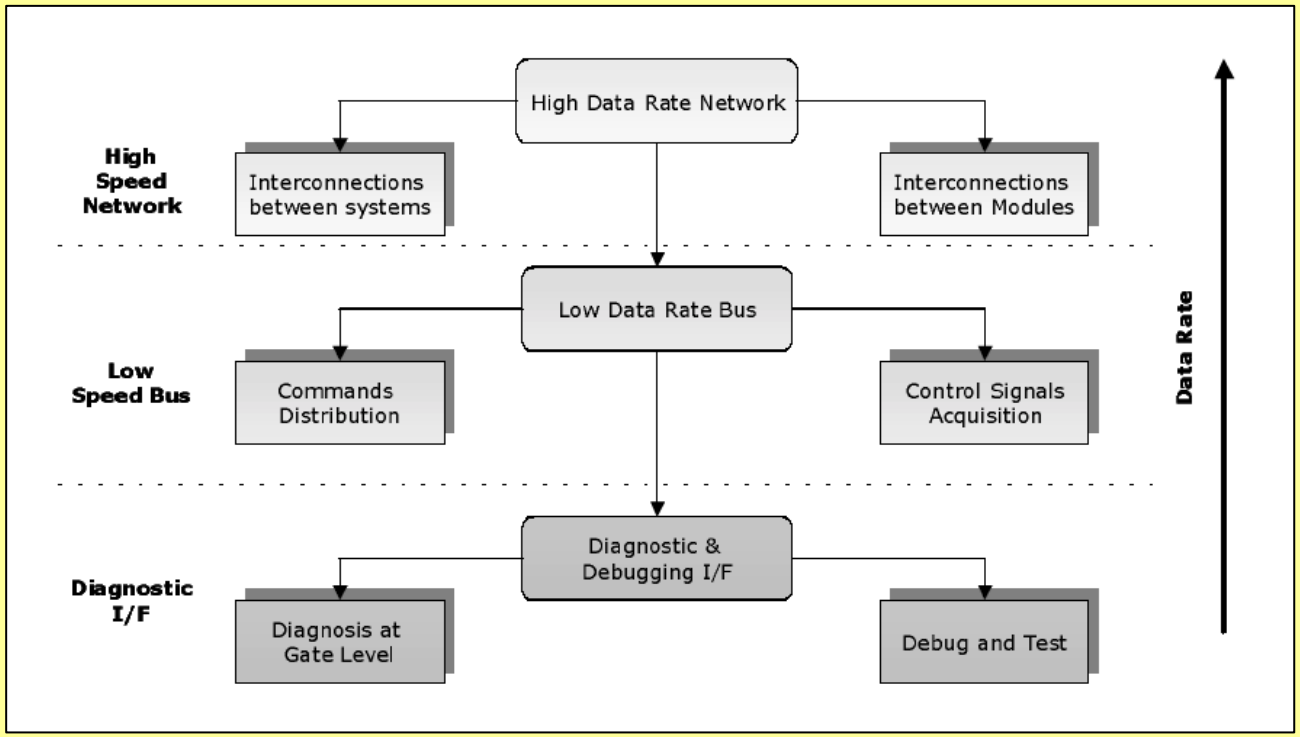
Hierarchical Avionics Network Architecture

- Need for several types of networks was identified, and solutions developed:

⇒ SpaceWire (SpW)

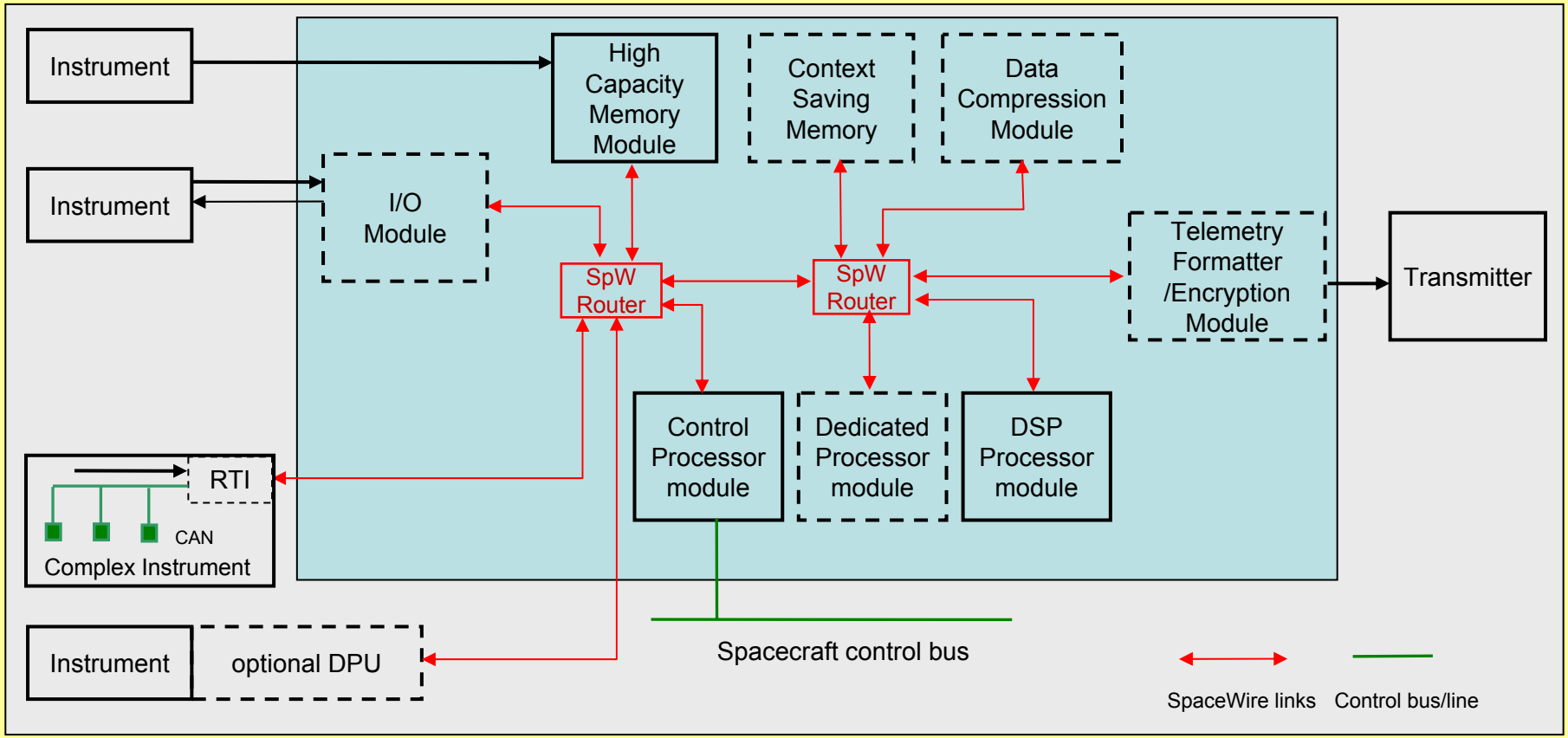
⇒ CAN Bus

⇒ Not defined yet / JTAG etc.



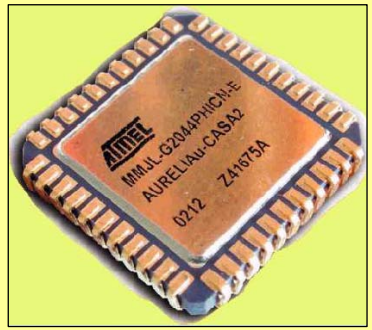
Networks & Nodes

Avionics Elements: Networks and Nodes

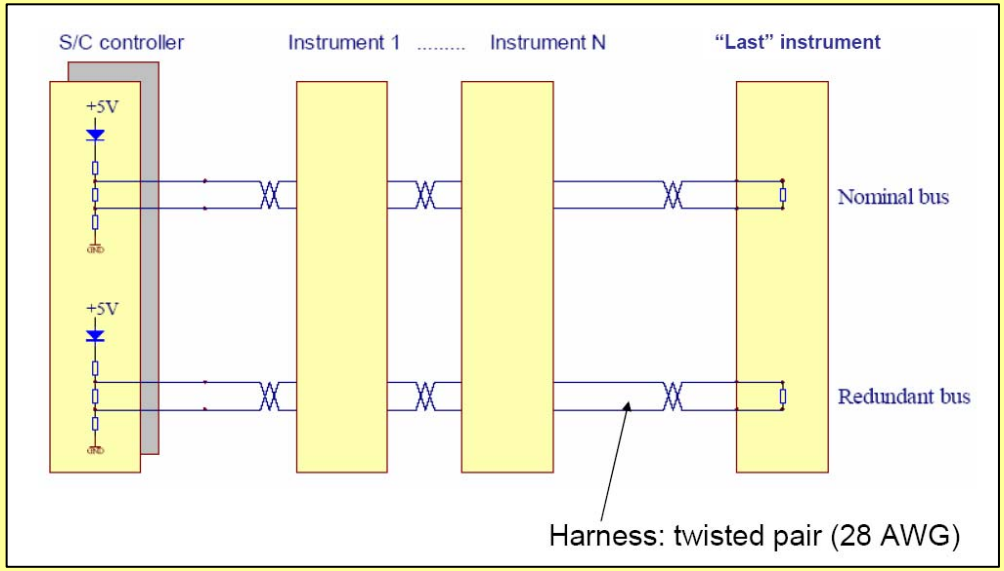


Networks: CAN Bus

Controller Area Network Bus



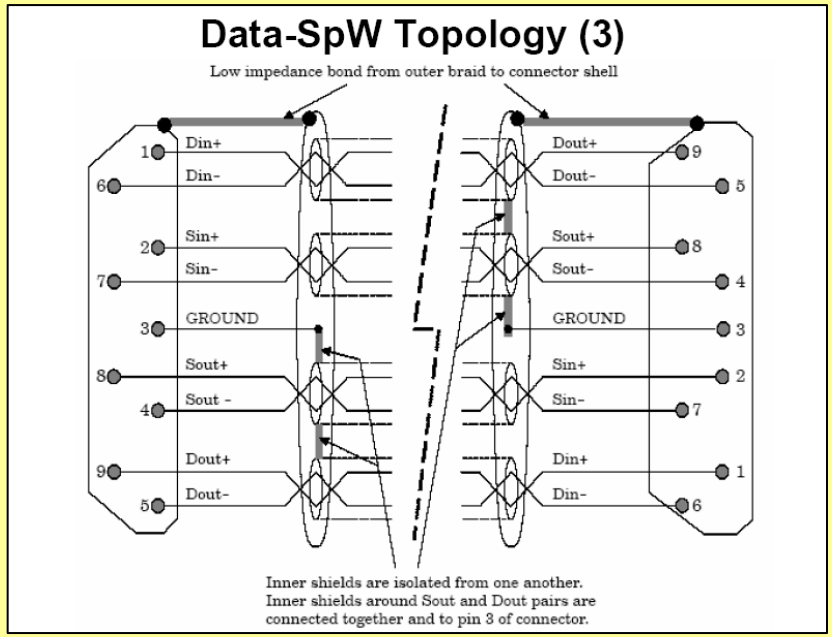
- Originates from automotive industry standard, soon adopted for space applications
- ESA IP core available (HurriCane)
  - includes features for SoC integration
- Rad-hard components available, based on ESA IP (ATMEL AT 7908E)
  - 1 Mbit max
  - 2-wire interface
  - P ~250 mW
  - uP interface



Networks: SpW

SpaceWire Key Features

- Up to 400 Mbps, 200 Mbps typical
- RMAP
- Simple, small IP (5-7 k logic gates)
- P2P or complex NW (routers)
- Routers use wormhole routing (low memory need)
- Fault isolation properties - LVDS
- Group adaptive routing for link failure management
- Supports time distribution with few µsec resolution
- More and more components (routers, nodes) becoming available
- SpW is now a well established standard for space avionics, networks, interfaces

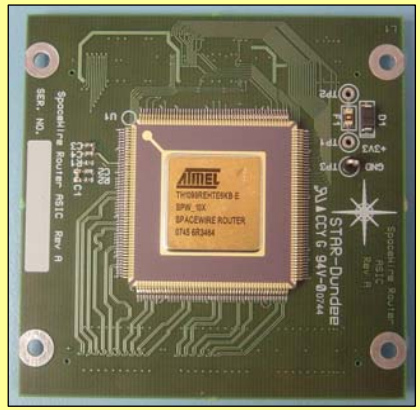


Physical specs

- 9-pin Micro-min D-type conn.
- Up to 10m Point 2 Point
- LVDS +/-350 mV typical
- 100 Ohm termination, power typically 50 mW per driver – receiver pair

SpW network components

SpaceWire Router

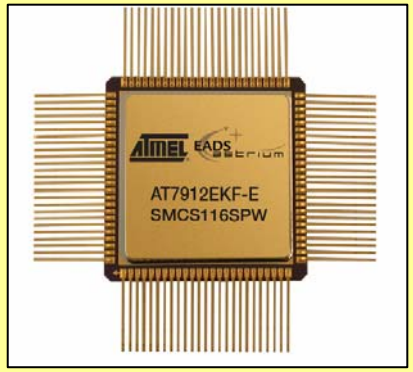


- compliant to standard ECSS-E50-12A,
- 8 full duplex serial links (2-200 Mbps) – LVDS
- offers external time-code and status signals
- 196 pin ceramic package
- 0.35um MH1RT (ATMEL): latch-up immunity 80 MeV/mg/cm2
- 2 external parallel ports,
- 1 internal configuration port (routing table, priority scheme) and (status and configuration registers),
- low latency, non-blocking, worm-hole, group adaptive routing,
- manages and distributes time-codes (network synchronization),
- Available NOW

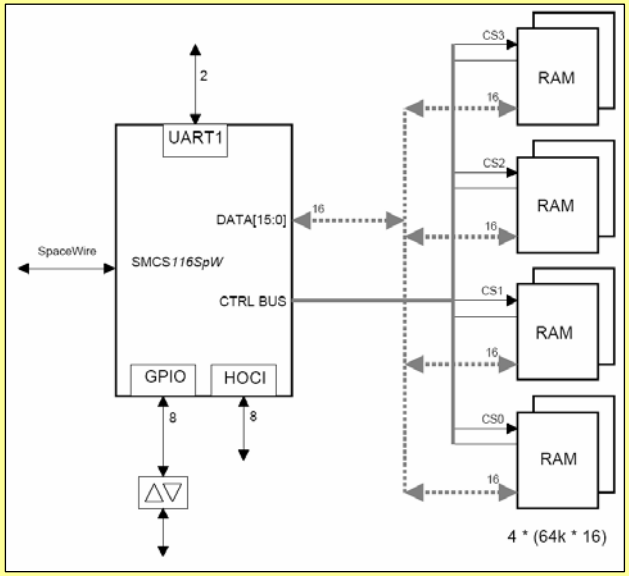
Nodes: SMCS116SpW

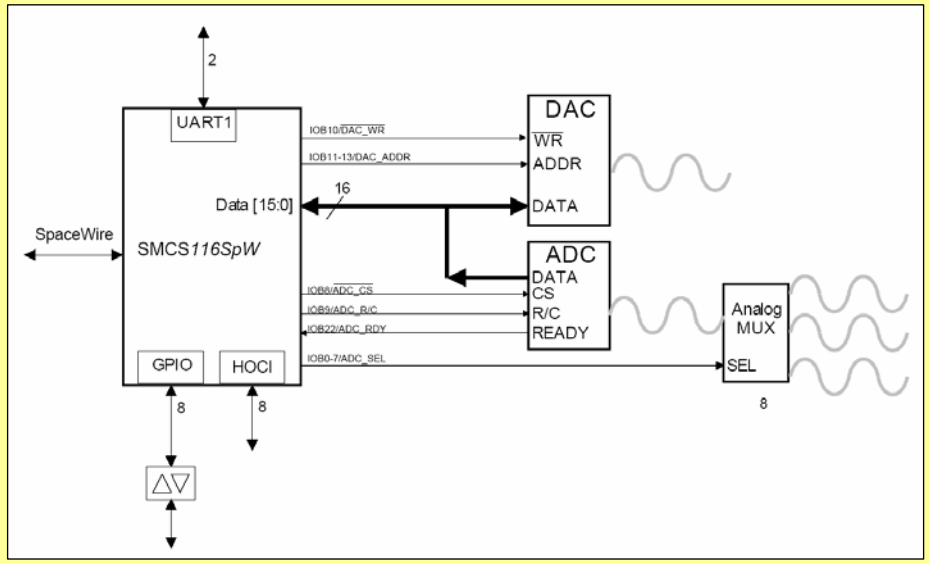
Scalable MultiChannel Communication Subsystem for SpW

- Connects one SpW link to various interfaces such as ADC/DAC, RAM, FIFOs, GPIOs and UARTS
- MQFP 100 pins package
- Supports both 5V and 3.3V operation
- SpW link speed: 200Mbps@5V, 100Mbps@3.3V
- Support Serial Universal Protocol (STUP)
  - Supports use in a SpaceWire network with distinct protocols
- Power consumption: 0.7W@5V, 0.4W@3.3V
- 0.5um MG2RT (ATMEL) CMOS technology
  - Total dose tested up to 50Krad
  - No SEL at 70 MeV/mg/cm2
  - SEU hardened flip-flops
- Engineering Models: Available
- Flight Models: order entry open



Typical Application Areas for the SMCS116SpW

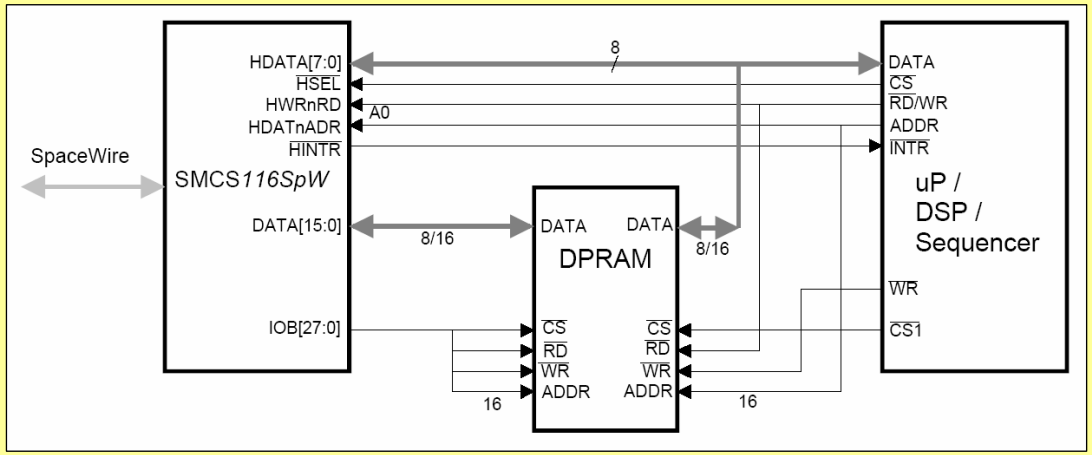




SpW - memory interface

Sensor interface

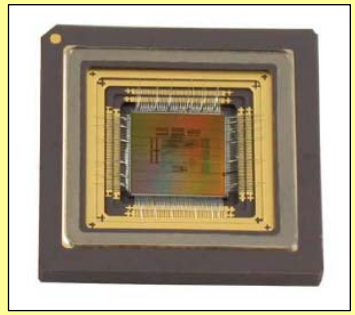
uP interface

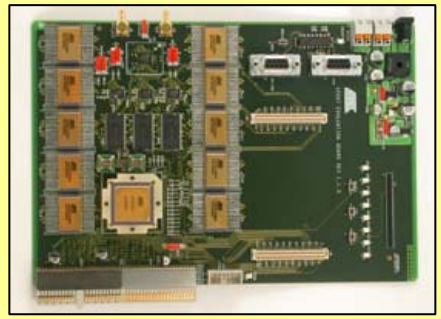


Nodes: LEON2 processor

AT697 CPU

- Sparc-V8 compliant
- 100 MIPS
- Radiation hardened chip
- Based on LEON2 FT IP core
- Developed under ESA contract
- Leon2 FT IP core used in several SoC developments
- Note: needs additional chip for SpW / CAN interface
- Companion chip by GR



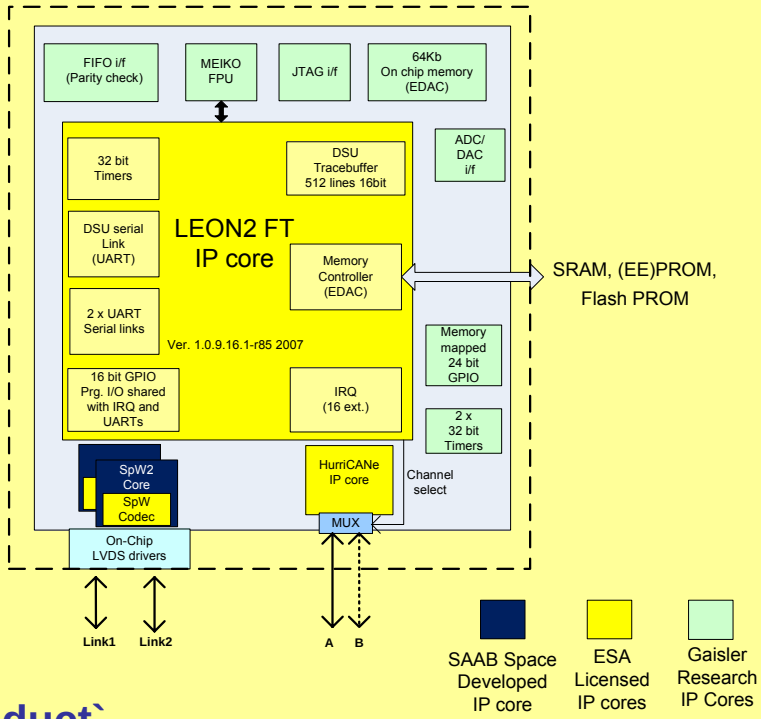


Manufacturer	ATMEL
Performance	0-100MHz / 100 MIPS @ 100 MHz, to 1GByte RAM
Radiation hardness	100 – 200 krads
Software	BCC/GCC compilers, RTEMS real time kernel, Linux supported
Mass	~ 1kg per processor board
Power (board)	Ca 10 Watts max (clock dependent)

Nodes: SpW-RTC

SpW Remote Terminal Controller (SpW-RTC) – AT7913E

- SPARC V8 LEON2-FT processor with FPU
- 50MHz core clock frequency
- Two 200Mbps SpW links (RMAP compliant)
- CAN controller (Support 2 links)
- Interfaces to ADC/DAC, SRAM, (EE)PROM, FIFOs, GPIOs, UARTS.
- 64Kbyte on-chip SRAM (EDAC protected)
- 3.3V for the I/Os, 1.8V for the core
- 0.6W power consumption
- 0.18um CMOS technology (ATMEL ATC18RHA)
- MCGA 349 pins package
- Available as Application Specific Standard Product`



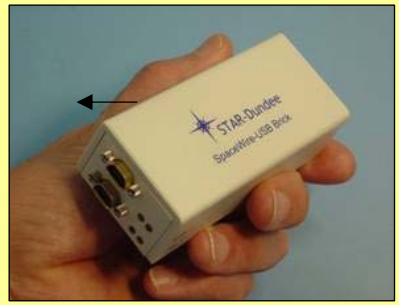
Network development

CAN

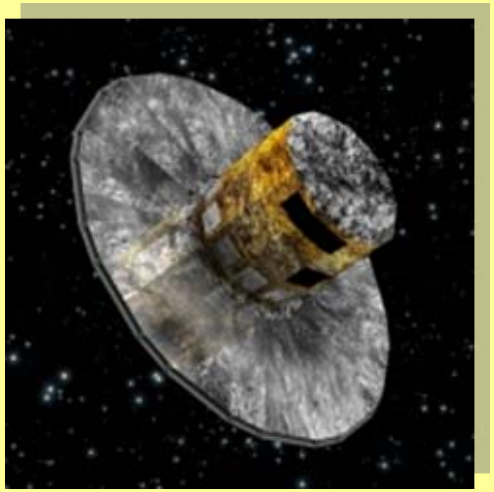
- Many commercial devices available supporting CAN interface
- Lots of documentation available / standard docs

SpW

- A range of development support equipment available
- SpW PCI / cPCI cards
- USB - SpW brick, USB router
- EtherSpaceLink
- SpW link monitor box
- Standard docs, web (SpW wiki)



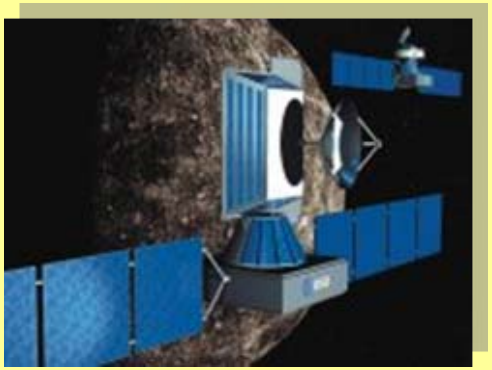
Missions using SpW devices



GAIA

EarthCare

ExoMars



BepiColombo
ESA/JAXA

James Webb
Telescope
ESA/NASA

Ongoing Developments

Some ongoing ESA development activities*

- SpaceWire activities
- SpaceFibre development

- Spacecraft Controller On a Chip (SCOC3)
- Next Generation Multipurpose Processor (NGMP)
- Next Generation Space DSP (NGDSP)
- Essential Telemetry Support ASIC (ETM)

- New IP Cores: SpW RMAP, massively parallel processors, & others

*** Examples with particularly high relevance to planetary entry probes**

Networks: SpW & SpFi

SpaceWire developments

- SpaceWire IP Tunnel: SpW networks connected via Internet
- SpW interface to be integrated in many new components & units

SpaceFibre developments

- SpW limitations: data rate, cable length & mass, galv. solation, etc:

=> Fiberoptic link is developed maintaining many SpW features

- 1-10 Gbps, 100m, galvanic isolation, mass few g / m
- Copper version for short distances (few 10 cm),
- TX of scalable number of virtual SpW links over SpF link
- Compliant to protocols and routing mechanisms defined in the SpW standard
- SpW/SpFi demonstrator available, work on definition and standardization ongoing

SpFi transceiver

SpW - SpFi router prototype

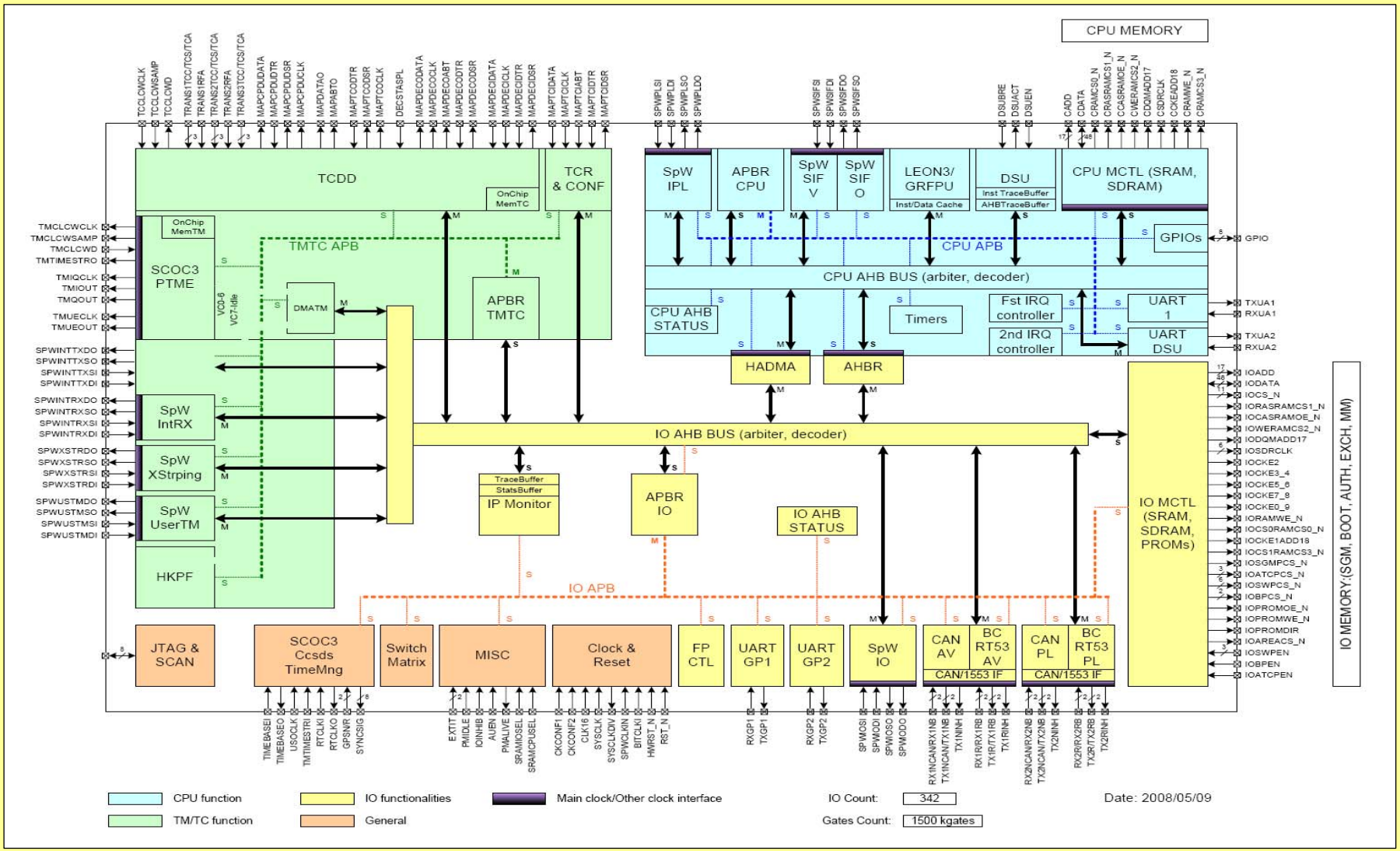
Nodes: SCOC3

Spacecraft Controller on a Chip 3

SCOC3 Specification

- **LEON3-FT with GRFPU-FT at 80 MHz+**
- **Dual AMBA-AHB bus architecture**
  - CPU bus and IO bus may operate at different frequencies
- **CCSDS TM/TC interfaces**
  - MAP interface for cross-strapping
- **OBDH interfaces**
  - 1553, SpaceWire, CAN, UART
- **Other resources**
  - CCSDS Time management, housekeeping telemetry packetiser
- **Power management**
- **Debug facilities**
  - IP Monitor: AMBA statistics and trace for peripheral bus
  - LEON DSU for CPU bus
- **Target technology: ATC18RHA, package BGA472**

Nodes: SCOC3


CPU MEMORY
TCDD
TCR & CONF
OnChip MemTC
SCOC3 PTME
OnChip MemTM
TMTC APB
DMATM
APBR TMTC
SpW IntRX
SpW XStrping
SpW UserTM
HKPF
SpW IPL
APBR CPU
SpW SIF V
SpW SIF O
LEON3/ GRFPU
Inst/Data Cache
DSU
Inst TraceBuffer
AHBTraceBuffer
CPU MCTL (SRAM, SDRAM)
CPU APB
GPIOs
CPU AHB BUS (arbiter, decoder)
CPU AHB STATUS
Timers
Fst IRQ controller
2nd IRQ controller
UART 1
UART DSU
HADMA
AHBR
IO AHB BUS (arbiter, decoder)
TraceBuffer
StatsBuffer
IP Monitor
APBR IO
IO AHB STATUS
IO APB
IO MCTL (SRAM, SDRAM, PROMs)
JTAG & SCAN
SCOC3 Ccsds TimeMng
Switch Matrix
MISC
Clock & Reset
FP CTL
UART GP1
UART GP2
SpW IO
CAN AV
BC RT53 AV
CAN/1553 IF
CAN PL
BC RT53 PL
CAN/1553 IF
IO MEMORY:(SGM, BOOT, AUTH, EXCH, MM)
CPU function
TM/TC function
IO functionalities
General
Main clock/Other clock interface
IO Count: 342
Gates Count: 1500 kgates
Date: 2008/05/09

Next Generation Multipurpose Processor

Requirements for Next Generation Multipurpose Processor:

- 400 MIPS minimum
- Standard Product
- Advanced generation silicon technology (90 nm or 65 nm)
- SPARC V8 (E) architecture
- Multi-core architecture
- Memory Management function (MMU) and debug support
- Large on-chip memory banks (16-32 MB), extended caches
- Standardised interfaces (SpW, MIL-STD-1553, CAN, RSS422)
- Interface for co-processors and/or companion devices

Ongoing ESA activities :

- Preliminary study done (GINA), final architecture to be defined
- Development and qualification 2009-2012, Chip availability planned 2013+

Next Generation Space Digital Signal Processor

Currently available space qualified DSPs are outdated (21020)

Requirements for next generation space DSP:

- 1 GFLOP+ performance
- Rad hardened design (int. memories, EDAC, registers), Small footprint, low power, space qualified
- Easy interfacing to standard DSP system components (RAM, ROM, ADC/DAC, bus, SpX networks, DSP arrays)
- Software development environment

Ongoing ESA activities :

- Next generation DSP tradeoff study 2008 / 2009
- Development and qualification 2010-2012, Chip availability planned 2013+

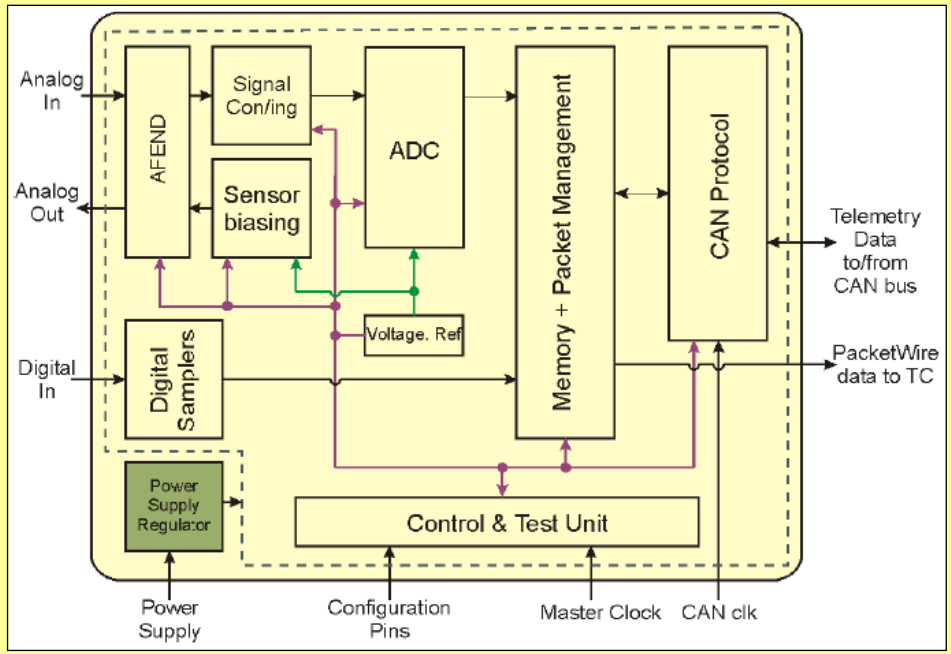
Bridging the gap:

- Dedicated ASICs
- Reconfigurable processors, FPGA + IP based solutions

Nodes: ETM ASIC

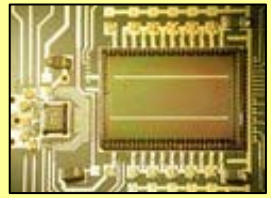
Essential Telemetry ASIC

- Device supporting TM acquisition from analogue and digital sources
- Up to 32 analogue channels
- 16 differential digital inputs
- 12 bit ADC
- Instrumentation amplifier
- Low power (~20 mW)
- Single power supply
- 20 mHz to 4 kHz f_s
- CAN and packetwire I/F
- Support for various temperature sensors
- Rad-hard, MIL temp range
- Standalone or cascaded



ESA IP Service

ESA/ESTEC maintains and distributes under ESA licenses a small catalog of IP Cores which comprise typical digital functions used in space applications (TMTC, EDAC, SpW, CAN, LEON2 ..). ESA/ESTEC provides this "IP Cores" service as an attempt to:



- counteract obsolescence and discontinuity of existing space standard ASICs, thus helping to guarantee the availability of some key functions in a technology independent format ("soft format").
- reduce costs of large IC developments (e.g. Systems-on-Chip) by re-using already designed and validated IC functions.
- promote and consolidate the use of standardized functions, protocols and/or architectures (e.g. SpaceWire, CAN, TMTC, etc).
- centralize IP users' feedback to improve quality of existing IPs and identify future needs.

The ESA VHDL IP cores can be licensed for space research and/or commercial use, under specific conditions (depending on the IP ownership) to companies based in ESA member and participant states.

* ESA IP Cores and ESA-funded Standard ASICs (as in ATMEL terminology for what you call ASSP), can only be licensed / sold to companies based on ESA member states. Requests from outside (even also for Participant states like Canada) have to be authorised by ESA Techn Transfer Board

Summary

Avionics elements supported by ESA

- Networks: CAN, SpW; IP cores; development support equipment
- Nodes: SMCS, RTC, Leon2, ….
- ESA IP service

Ongoing developments

- Networks: SpW & SpF
- Processors: NGMP, NGDSP, & more ..
- Systems on Chip: SCOC3
- ETM and others !

⇒ Only a subset of the actually ongoing developments was presented
⇒ Please check the ESA / TEC-ED web pages for more !

⇒ **http://www.esa.int/techresources/index.html**