Cost and Technology Roadmaps for Cost-Effective Silicon Photovoltaics

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The cost of photovoltaics (PV) is expected to decrease by a factor of two to four within the next two decades, making PV an integral part of the solution to the problems of fossil fuel depletion and growing energy demand. This paper describes cost and technology roadmaps for achieving 17–18%-efficient crystalline Si solar cells at a competitive manufacturing cost of less than $1/W.

I. INTRODUCTION

Crystalline Si has been the workhorse of the PV industry from its inception in the mid-1950s. Over the past two or three decades its cost has decreased by more than an order of magnitude, but still must drop by a factor of 2–4 further to compete with traditional energy sources. Efforts are being made to achieve this by using various materials and technologies. One approach involves high-cost, high-performance technologies using III-V materials, multiple junctions, and concentrator systems, which are currently too expensive for terrestrial applications. At the opposite end of the spectrum are low-cost thin-film technologies using materials like amorphous Si, CdTe, and CIS, but these suffer from low efficiency, poor stability, and scalability problems. Crystalline Si offers an intermediate path, striking a balance between cost and performance. This document demonstrates, through a combination of cost and technology roadmaps and recent developments, that crystalline Si PV is poised to simultaneously meet the cost and efficiency targets set by the US PV industry [1].

II. MANUFACTURING COST ANALYSIS AND ROADMAP FOR COST-EFFECTIVE SILICON PHOTOVOLTAICS

Even though laboratory Si cell efficiencies had reached 24.7% by the end of the 20th century, production cell efficiencies were struggling in the range of 12–15%. Laboratory cells were too expensive, but production cells were not efficient enough. Skepticism about the viability of silicon cells was building up, along with the competition from other PV materials and technologies. On a positive note, the PV market, which grew at an average rate of 13% per year during 1982–1996, exploded with an average annual growth rate of 30–35% per year during 1996–2002 [1]. Equally noteworthy is the fact that crystalline Si increased its dominance of the marketplace from 68% in 1990 to 93% in 2002, while annual module shipments increased from 47 MW to 560 MW during that period [2]. This was accomplished through successful scale-up of many different Si cell production lines. By 2002, there were about ten Si PV module manufacturers with production capacities in excess of 20 MW, with the largest exceeding 120 MW (Sharp). On the other hand,

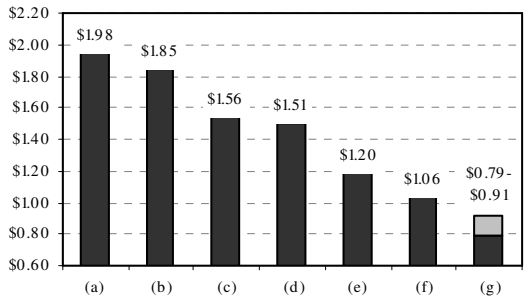

Fig. 1 PV module manufacturing cost analysis. Column (a) shows the current cost; the remaining columns show cost reductions due to (b) slurry recycling, (c) reduction of cell thickness to 200 μm, (d) reduction of feedstock costs to $20/kg, (e) increasing cell efficiency to 17%, (f) reductions in module materials costs, and (g) scaling up to 100–500 MW production capacity.

most competing materials and technologies experienced problems in scale-up and remained in the range of 1–10 MW. This once again proved the manufacturability, robustness, and stability of Si over other materials, endorsing that 200–500 MW Si PV plants will be built in the near future to take advantage of the significant cost reduction due to increased production volume.

Recently, a US PV Industry Roadmap was developed [1] that predicts an impressive ~25% annual growth rate in PV for the next 2–3 decades, resulting in an annual production capacity of ~17 GW/yr worldwide by 2020, with cumulative shipments approaching 88 GW. According to this roadmap, the installed system cost needs to come down from $6–8/W to ~$3/W by 2010 and approach $1.50/W by 2020 to compete with traditional energy sources. This implies that the long-term manufacturing cost of PV modules must drop below $1/W.

In order to establish the requirements for reducing the manufacturing cost of Si PV modules to below $1/W, we performed a detailed cost analysis using a spreadsheet developed at GT Solar for cast mc-Si. Many studies have been conducted in the past to assess the manufacturing cost of Si wafers, cells and module assembly using different basic assumptions [10–13]. Table I shows the key assumptions made in this study for the baseline technology describing the current status of module manufacturing. Our calculations in Fig. 1 show that the current module manufacturing cost is $1.98/W for 325-μm thick wafers, 13.5% efficient cells, $25/kg polysilicon, and 25 MW annual production capacity. Several cost sensitive factors were identified and implemented in the cost analysis sequentially to determine if their combination can reduce the manufacturing cost below $1/W using practically achievable parameters. Fig. 1 shows that: a) slurry recycling during wafer slicing will reduce the cost to $1.85/W; b) reduction of the cell thickness to 200 μm will then bring the cost down to $1.56/W; c) lowering the polysilicon cost to $20/kg will reduce the cost to $1.51/W; d) increasing the cell efficiency to 17% will lower the cost to $1.20/W. Due to economies of scale and increased competition between an increasing number of suppliers, the cost of materials (such as crucibles, aluminum, slurry, saw wire, etc.) will decline in the future, which will reduce the module cost to $1.06/W. The final cost reduction will come from the scale-up of the production line from 25 MW to 100–500 MW, which will bring the manufacturing cost to the range of $0.79/W–$0.91/W. Use of frameless modules can reduce the manufacturing cost by an additional $0.06/W. Scale-up in production reduces the materials, capital, labor, and overhead costs significantly, due to volume purchases, larger equipment, increased automation, and effective utilization of space and labor on a per watt basis. Haynes and Hill [3] reported 37% cost reduction, while Frantzis et al [4] reported 25% reduction in costs due to the scale-up from 10 to 100 MW. Alonso et al. [5] calculated a 14% cost reduction for the 25 MW to 250 MW expansion.

Table I. Key assumptions for baseline cost analysis of 25 MW mc-Si module production facility.

Cell thickness	325 μm	Depreciation	7 yr
Cell area	225 cm^2	Uptime	90%
Cell efficiency	13.5%	Working days	350/yr
Feedstock cost	$25/kg	Interest rate	8%
Wafering yield	92%	Labor	$11–30/hr
Cell yield	95%	Overhead	100%
Module yield	98%		

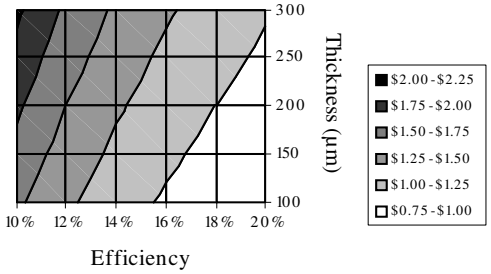

Fig. 2 Effect of cell efficiency and thickness on module manufacturing cost for fixed manufacturing yields shown in Table I.

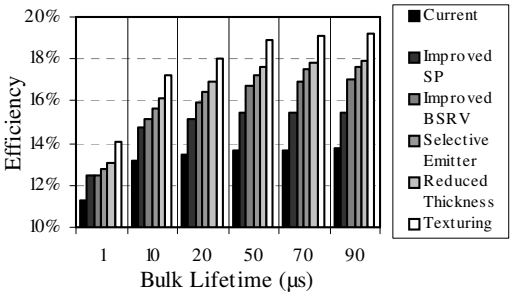

Fig. 3 Technology roadmap illustrating the steps required to achieve low-cost high-efficiency crystalline silicon solar cells.

Fig. 2 shows a contour plot for the synergistic effect of thickness and efficiency on cost for a 25 MW production line. The $1/W line in this figure indicates that either 200-µm thick, 18% cell or 160-µm thick, 17% cell can produce $1/W modules for a 25 MW production line. The scale-up of production lines from 25 MW to 100–500 MW will reduce the manufacturing cost appreciably below $1/W. A comprehensive cost study conducted under the European Photovoltaic Program [6] showed that for 500 MW production of screen-printed Czochralski, cast mc-Si, and ribbon Si cells with efficiencies of 16%, 15%, and 14.4% can reduce the manufacturing cost to €1.25/W, €0.91/W and €0.71/W, respectively. More recently [7] this study was revisited to validate the old assumptions and it was concluded, based on the progress in the past five years, that 150-µm thick, 17%-efficient screen-printed cast mc-Si cells are achievable in the future at a manufacturing cost of €0.77/W for 500 MW production.

The US Department of Energy (DOE) PVMaT project also estimates a current direct manufacturing cost of $2/W for crystalline Si modules and projects that it will drop to $1/W by 2008. Thus several cost studies have indicated that the direct manufacturing cost for crystalline Si PV modules has reached ~$2/W, with strong potential for reduction below $1/W.

Table II. Parameters for baseline solar cell used in PC1D and module manufacturing cost calculations.

Thickness	300 µm
Fill factor	0.74
Efficiency	13.5%
Bulk lifetime	20 µs
Bulk resistivity	1.3 Ω-cm
Sheet resistivity	40 Ω/sq.
Front surface recombination velocity	250,000 cm/s
Back surface recombination velocity	10^6 cm/s
Antireflection coating	SiN_x SLAR
Metallization coverage	8%

III. A TECHNOLOGY ROADMAP FOR ACHIEVING 17–18%-EFFICIENT MANUFACTURABLE CRYSTALLINE SILICON SOLAR CELLS

The cost analysis in the previous section revealed that 150–200-µm thick, 17–18% efficient crystalline Si cells at a 100–500 MW annual module production level will be required to achieve a direct module manufacturing cost below $1/W. Fig. 3 shows a technology roadmap for improving cell efficiency. A combination of PC1D and Sunrays simulation programs was used to perform efficiency calculations using a current industrial cell design with screen-printed contacts on 1.3 Ω-cm, p-type Si. Sunrays was used for modeling both planar and textured cells in order to maintain consistency in the optical model. All the pertinent material and device parameters are shown in Table II for the baseline cell which represents current industrial cells with a 20 µs bulk lifetime, 300 µm wafer thickness, and an efficiency of 13.5%. The roadmap shows that the following five technology improvements will be required to achieve 17–18% screen-printed cells:

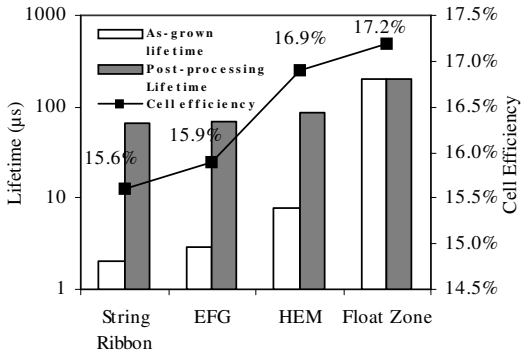

Fig. 4 Lifetime enhancement and highest manufacturable cell efficiencies (4-cm^2) achieved at Georgia Tech and verified by NREL.

a) fine-line screen-printed contacts with reduced shading losses from 8% to 5% along with improved fill factor from 0.74 to 0.78; b) an improved back surface field to reduce the back surface recombination velocity (BSRV) from 10^6 cm/s to 200 cm/s; c) a selective emitter design with an 80 Ω/sq sheet resistance and a front surface recombination velocity of 7500 cm/s; d) a reduction in the cell thickness from 300 to 200 μm; and e) surface texturing.

Model calculations in Fig. 3 show that the addition of all five technology improvements can raise the baseline cell efficiency from 13.5% to 18.0%. The roadmap in Fig. 3 also shows the impact of the above technology improvements on silicon materials of different quality with processed lifetimes ranging from 1–90 μs. Crystalline Si for PV generally comes in three forms: monocrystalline Czochralski (Cz) Si, cast or directionally solidified (DS) multicrystalline Si, and ribbon silicon. Thin film Si is also gaining momentum these days. Our research on the enhancement of the bulk lifetime has shown that the as-grown lifetime in most PV grade materials is quite low. However, the incorporation of appropriate gettering and defect passivation techniques as a part of cell processing can increase the lifetime to the range of 25–90 μs (Fig. 4). The lifetime enhancement is achieved at no additional cost because phosphorus diffusion for the emitter and Al alloying for the BSF are used for gettering, while the SiN_x AR coating and screen-printed contact firing are used for hydrogenation of defects. We have demonstrated that rapid firing of contacts not only can enhance throughput but also improves BSF, FF and hydrogenation of defects. Fig. 4 also shows that with those improvements we are able to raise the efficiency of screen-printed Cz, cast mc-Si, and ribbon materials to 15.5–16.9% without fine-line contact printing, selective emitter, reduced thickness, or surface texturing. Thus, there is still considerable room for improvement in manufacturable cell efficiencies on these materials.

The technology roadmap of Fig. 3 shows that with 200-μm thick, 50-μs processed lifetime Si, which is not uncommon today, it is possible to achieve 17.5% planar cell efficiencies and 19.0% textured cell efficiencies. The marginal benefits of lifetime enhancement beyond 50 μs decreases; at 90 μs, 18.0% planar and 19.3% textured cells can be achieved. It is important to recognize that it is easy to texture monocrystalline Si but texturing is a challenge for mc-Si, particularly ribbon Si.

Significant progress has been reported on the screen-printed Al-BSF, which has been shown to improve appreciably when a fast ramp-up rate is implemented during Al-Si alloying [8]. Effective BSRV values of 200 cm/s have already been reported [8] for screen-printed Al-BSFs formed on 2 Ω-cm float zone Si. However, as we move toward thinner wafers, the conventional Al-BSF formation may not be suitable as it warps thin wafers. There is a real need to develop a suitable Al-BSF, a good dielectric surface passivation scheme, or a cost-effective boron BSF. BSRV values in the range of 1–100 cm/s have been reported [9] for dielectric passivation of 1.3 Ω-cm single crystal Si, but a considerable challenge remains in achieving such low BSRV values for mc-Si due to defects at the silicon/dielectric and p-p^+ interface.

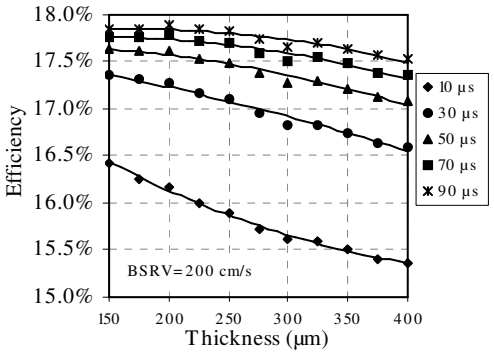

Fig. 5 Efficiency variation with thickness, illustrating increased efficiency and reduced variation in efficiency on thin substrates.

The next technology improvement on the roadmap calls for a reduced wafer thickness of ≤ 200 µm. Model calculations in Fig. 5 show that, with a good surface passivation, thinner wafers not only give higher efficiencies but also reduce the spread in efficiencies due to material quality or diffusion length variations. While thinner wafers reduce materials cost, higher efficiencies and a tighter distribution increase production capacity and reduce the area-related balance-of-systems costs. Model calculations in Fig. 3 and 5 show that it is possible to produce manufacturable screen-printed 17%–19%-efficient cells on 150–200-µm thick Si with a BSRV of 200 cm/s and bulk-lifetime in the range of 25–90 µs. It is important to note that a high BSRV or no rear passivation would hurt the efficiencies of thin Si cells. Thus, the challenges are to achieve very low BSRV, especially on multicrystalline materials, slice very thin wafers and process cells with high mechanical yield.

The development of Si ribbon cell technologies is progressing at a rapid pace with their market share reaching 3% in 2002. Ribbon technologies have the ability to grow very thin (≤ 150 µm) material directly from the Si melt. Ribbon Si offers more efficient use of the feedstock Si over ingot technologies, which require slicing and suffer from kerf losses. Thus ribbons can lead to even lower costs provided material yield and throughput per machine (m^2/yr) is maintained at high level. Edge-defined film-fed grown (EFG) Si from RWE Schott Solar (30 MW) and String Ribbon Si from Evergreen Solar (2 MW) are the industry leaders in this area with production cell efficiencies of about 14% for EFG and 13–13.5% for String Ribbon. We have fabricated screen-printed cells on EFG and String Ribbon Si at Georgia Tech with efficiencies as high as 15.9% and 15.6%, respectively (Fig. 4).

The last technology development in the roadmap (Fig. 3) involves surface texturing which can give ~1% increase in cell efficiency. The chemical texturing of (100) CZ wafers is routine in production today, but texturing of mc-Si poses a challenge. Several promising methods being explored include RIE texturing, porous Si texturing, acid isotropic texturing, and mechanical grooving. At least one high-throughput isotropic texturing system is now commercially available.

In addition to the reports on low-cost high-performance technology developments detailed above, now there are several examples of manufacturable cell designs and technologies leading to 16–18% crystalline Si cells in the laboratories or pilot production lines. As discussed earlier, Münzer et al. achieved a large area 18.2% efficient cells on Cz Si, Duerinckx et al. reported 16.5–17.0% efficient cells on mc-Si, and Georgia Tech [10] and the University of Konstanz [11] have reported ribbon Si cell efficiencies approaching 16%, all using screen-printed contacts. Besides screen printing, there are two other manufacturable crystalline Si technologies that have reported 18% efficiency cells on Cz Si. BP Solar recently announced [12] an 18.3% efficient large area LGBG cell, an improvement of 11% over previous cells. Lately, HIT (heterojunction with intrinsic thin-layer) cells from the Sanyo Electric Company [13] have attracted considerable attention because they have already achieved 17–18% efficiency in production on 200-µm thick Si while laboratory efficiencies have exceeded 20%.

Both the cost and technology roadmaps presented in this paper, along with the rapid development of manufacturable cell designs and technologies indicate that it is not a question of whether but it is only a question of when

crystalline Si PV will become cost-effective and compete with traditional energy sources. Indications are that module manufacturing costs will reach ~$1/W by 2010, and fall appreciably lower by 2020.

IV. CONCLUSIONS

The silent revolution in crystalline Si solar cell technology continues in spite of economic, technical, and political hurdles and competition from other promising PV materials. Silicon PV has demonstrated most of the major attributes for commercial success, namely efficiency, stability, manufacturability, high yield, and scalability. Cost analysis shows that the current direct manufacturing cost of Si modules has reached $1.98/W and can go below $1/W to compete with traditional energy sources. This will require 150–200-μm thick, 17–18% efficient cells with 100–500 MW production lines. The technology roadmap shows that this cost reduction can be achieved with thinner Si substrates, modest bulk lifetime, better back surface passivation, improved screen printing, and surface texturing. Considerable progress has been made in each of these areas and efficiencies approaching 17–18% have been recently achieved in the laboratories for single crystal Si-based screen-printed cells, laser grooved buried contact cells, and HIT cells. In addition, cast and ribbon multicrystalline-based screen-printed cell efficiencies have reached 15.5–17% in the laboratories. Furthermore, the scalability of Si technologies has exceeded 100 MW with a proven track record of decades of reliable service. Thus, crystalline Si is a safe bet for cost-effective PV.

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