Effective Interfaces in Silicon Heterojunction Solar Cells

T.H. Wang,[1] E. Iwaniczko,[1] M.R. Page,[1] D.H. Levi,[1] Y. Yan,[1]
V. Yelundur,[2] H.M. Branz,[1] A. Rohatgi,[2] and Q. Wang,[1]
[1]National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401, USA
[2]Georgia Institute of Technology, 777 Atlantic Dr., Atlanta, GA 30332, USA

ABSTRACT

Thin hydrogenated amorphous silicon (a-Si:H) layers deposited by hot-wire chemical vapor deposition (HWCVD) are investigated for use in silicon heterojunction (SHJ) solar cells on p-type crystalline silicon wafers. A requirement for excellent emitter quality is minimization of interface recombination. Best results necessitate immediate a-Si:H deposition and an abrupt and flat interface to the c-Si substrate. We obtain a record planar HJ efficiency of 16.9% with a high V_{oc} of 652 mV on p-type float-zone (FZ) silicon substrates with HWCVD a-Si:H(n) emitters and screen-printed Al-BSF contacts. H pretreatment by HWCVD is beneficial when limited to a very short period prior to emitter deposition.

INTRODUCTION

The a-Si:H/c-Si heterojunction solar cell is a good solution to the problems associated with high-temperature junction formation because a-Si:H can be deposited at temperatures below 250ºC. The simple planar structure of the SHJ may also help control processing costs. Applied to the full device area of a n-type crystal silicon wafer as both the emitter and back-surface-field (BSF) contact, thin intrinsic and doped hydrogenated amorphous silicon (a-Si:H) double layers have demonstrated superior passivation capability as well as adequate carrier transport ability in high-efficiency silicon heterojunction solar cells in Sanyo's HIT structure [1]. The amorphous layers used in these n-type wafer-based HIT cells are deposited by plasma-enhanced chemical vapor deposition (PECVD). In principle, HWCVD could be superior to PECVD for silicon heterojunction solar cells because of higher deposition rates, reduced ion bombardment of the base wafer, and high densities of atomic hydrogen (H) generation that may passivate the wafer interface region. However, obtaining high performance of heterojunction solar cells by using either PECVD or HWCVD, by groups other than Sanyo, has been a challenge. Efficiencies on the more commonly used and less expensive p-type silicon wafers have not been as high as on n-type wafers.

In this paper, we report our work on the silicon heterojunction solar cells based on p-type silicon wafers, using HWCVD for the entire emitter deposition process. To eliminate complications of the backside heterojunctions [2], a standard Al-BSF is used, so that we may focus on understanding and optimizing the front interface passivation. We study the effects of various gas treatments and deposition conditions prior to and during HWCVD deposition of the a-Si:H emitter. Some of the findings from HWCVD should apply to a-Si:H emitter deposition in general, including PECVD.

Effective a-Si:H/c-Si interfaces that allow efficient transport of charge carriers with minimal recombination loss is a prerequisite for high-performance heterojunction solar cells, in which a thin (~5 nm) intrinsic hydrogenated a-Si:H layer is generally interposed between the base wafer and the heavily doped emitter. This i-layer likely has a far lower density of defects and possibly a slightly larger energy gap than doped a-Si:H layers. If epitaxy extends through the i-layer, the defective interface will be contacted by the doped a-Si:H which is a less effective passivant than the intrinsic layer. Partial epitaxy, highly defective epitaxy, or a mixed phase i-layer can all cause detrimental high dark currents, because the a-Si:H/c-Si interface area or defect density will be large and the bandgap will be smaller. The additional dark-current path through inadequately passivated interface states in a heterojunction solar cell reduces the open-circuit voltage (V_{oc}) to well below its potential value given by the higher total band bending. Therefore, we use V_{oc} and the interface recombination velocity (S) as the indicators of the effectiveness of an a-Si:H/c-Si heterointerface.

EXPERIMENTAL

The material evolution and phase change are closely monitored by real-time spectroscopic ellipsometry (RTSE) [3] with post-deposition data analysis, and samples are examined by high-resolution transmission electron microscopy (HRTEM). The interface recombination velocity (S) is measured using a photoconductive decay lifetime measurement on an a-Si:H/c-Si/a-Si:H symmetric "sandwich". V_{oc} and other device parameters are characterized on a mesa-etched grid/ITO/a-Si:H/c-Si/Al solar cell structure. Surface cleaning, Si film deposition, front contact/ITO, Al-BSF fabrication on Czochralski silicon (CZ-Si) wafers, and characterizations are carried out at NREL. Details of the NREL device fabrication process are described elsewhere [4]. Standard diffused-junction solar cells as well as screen-printed and belt-furnace fired Al-BSF on float-zoned (FZ) Si are processed at Georgia Tech.

0-7803-8707-4/05/$20.00 ©2005 IEEE.

RESULTS AND DISCUSSIONS

Effect of deposition temperature

The crystallinity of the deposited Si layer is found to be very sensitive to the deposition temperature and crystal orientation of the substrate. Crystallinity, in turn, affects an SHJ solar cell's performance dramatically. In one set of experiments, RTSE clearly indicates epitaxial growth up to 30 nm in thickness on a (100) substrate at 200°C. On a (111) substrate at the same temperature, however, RTSE shows the film to be essentially a-Si:H as soon as the deposition starts. When the substrate temperature is higher, epitaxial growth can also be observed on (111) substrates. In Figure 1, through HRTEM imaging, one can see that epitaxy persists for ~15 nm at 375°C on a (111) wafer, encompassing the i-layer (5 nm) and extending well into the n-layer. As a result, the open-circuit voltage (V_{oc}) of this device is only 487 mV. When we lower the substrate temperature to 100°C for both the i- and n-layer deposition, abrupt amorphous-silicon growth is obtained, even on a (100) wafer, and a V_{oc} greater than 620 mV is obtained (Figure 2). Because of this tendency to grow epitaxial Si at higher HWCVD temperatures, V_{oc} decreases with increasing emitter deposition temperature. Figure 3 illustrates V_{oc} as a function of the i- and n-layer deposition temperatures (same for both layers) for 1.0 and 0.4 Ω·cm (111) substrates. The best V_{oc} and lowest S are obtained at substrate temperatures of 100° to 150°C. When an epitaxial film grows through the intrinsic layer and into the doped layer, V_{oc} is limited to 600 mV or lower, depending on the a-Si/c-Si interface roughness and quality of the epitaxy [5]. With carefully chosen conditions to avoid epitaxial growth, we have achieved V_{oc} values as high as 640 mV on p-type CZ-Si.

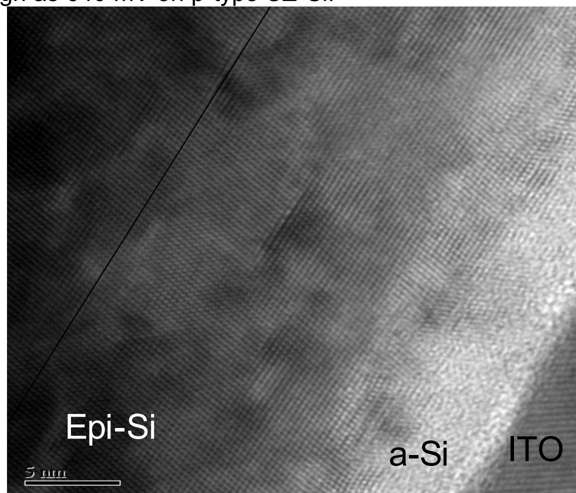

Fig. 1. Cross-sectional HRTEM image of Si deposition on a (111) wafer at 375°C. Line shows the wafer surface.

The beneficial effect of an abrupt interface is shown in interface recombination velocity (S), also. Figure 4 shows S as a function of i-layer deposition temperature. For passivations the n-layer temperature was fixed at 300°C to activate the n-layer dopants. Reducing the i-layer temperature reduces S as Si epitaxy is suppressed.

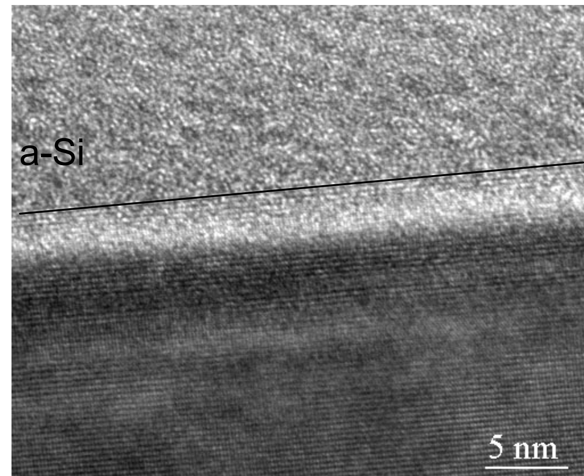

Fig. 2. Cross-sectional HRTEM image of Si deposition on a (100) wafer at 100°C. Line shows the wafer surface.

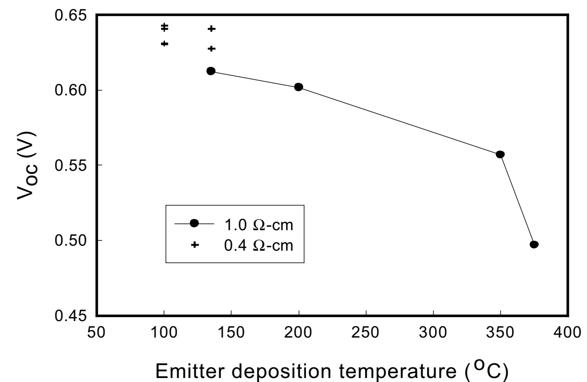

Fig. 3. V_{oc} vs. the i- and n-layer temperature.

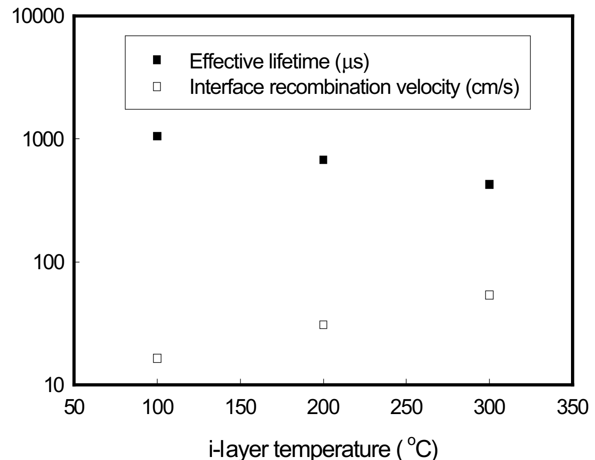

Fig. 4. S vs. i-layer temperature (T) (n-layer at T=300°C).

Effect of hot-wire pretreatment with H_2

With the expectation that exposure to atomic hydrogen before i- and n-layer deposition would help clean the wafer surface, remove residual oxide, and passivate surface defects, we tried exposing the wafer to cracked H_2 gas before film growth. However, HRTEM indicated that

prolonged pretreatment caused strain and defects in the Si wafer (Figure 5) and RTSE showed increased roughness at the interface. However, we find that a short atomic H pretreatment of the wafer (~10 sec) improved dark current and V_{oc}, as shown in Figures 6 and 7. There has been some speculation that H pretreatment passivates p-type dopants near the wafer surface [6]; this may be another reason that prolonged H exposure is detrimental to the solar cell performance.

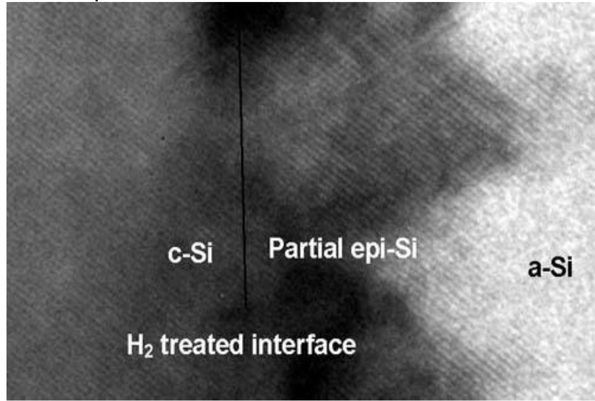

Fig. 5. Partial epitaxy and rough interface as a result of a 3-minute H pretreatment on (100) silicon.

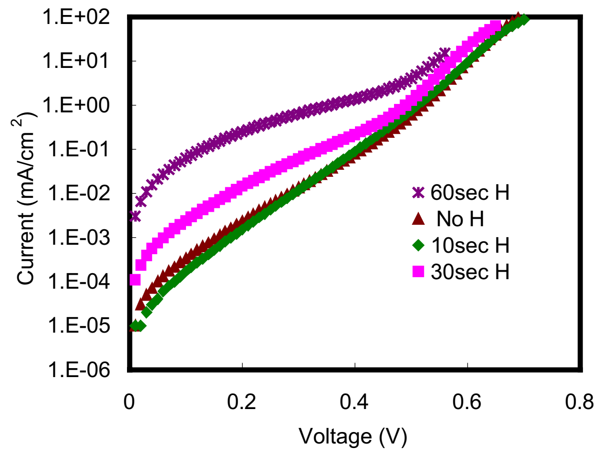

Fig. 6. H pretreatment vs. dark current.

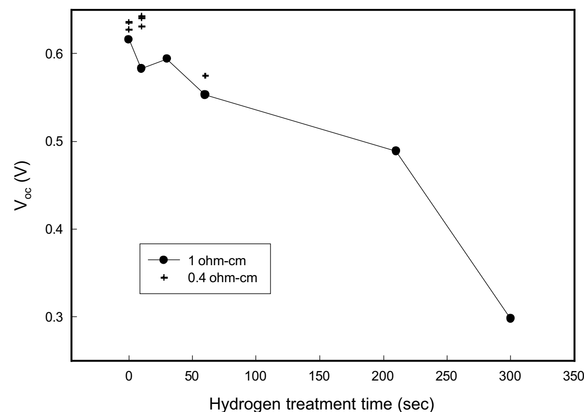

Fig. 7. Dependence of V_{oc} on H pretreatment time.

Remarkably, a short atomic H pretreatment can replace the undoped a-Si:H layer in heterojunction devices on p-type wafers. Figure 8 shows that without H pretreatment, a thin intrinsic a-Si:H (i-layer) is critical to obtain good cell performance. On the other hand, Figure 9 indicates no clear advantage by using the i-layer in cells that are subjected to H pretreatment. However, these voltages are slightly lower (but better J_{sc}) due to the higher resistivity wafers used in the experiment.

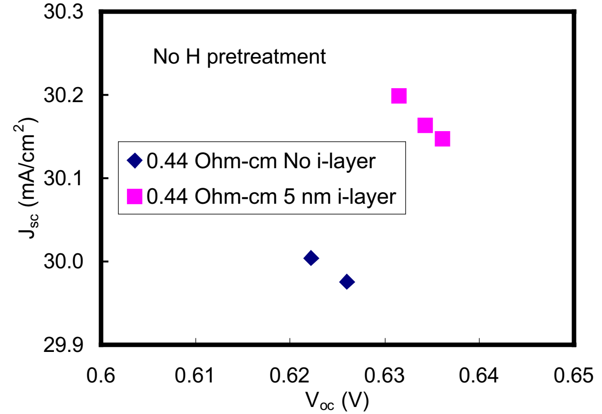

Fig. 8. Solar cell parameters with and without an undoped a-Si:H layer in heterojunction cells without H pretreatment.

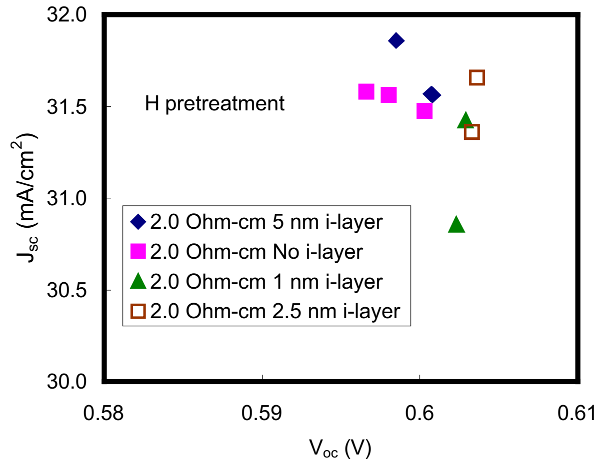

Fig. 9. Solar cell parameters with and without an undoped a-Si:H layer in heterojunction cells with a 10-sec H pretreatment.

Heterojunction vs. diffused junction

Using the same FZ wafers with an identical screen-printed and belt-furnace fired Al-BSF, we fabricated both the heterojunction (HJ) and diffused-junction (DJ) solar cells. Our heterojunction solar cells employing the optimized a-Si:H emitter structure exhibit the highest reported efficiency (16.9%), so far, for a flat-surface heterojuncton (Figure 10). The results listed in Table 1 show that V_{oc} of the HJ devices is higher by about 15 mV than that of the DJ devices for both the 1.0 and 0.5 Ω·cm substrates. This again indicates the excellent interface passivation provided by the a-Si:H emitter. J_{sc}, however, is about 5% less than the DJ devices. Spectral response

measurements (Figure 11) show that most of this current loss is due to poor blue response. Absorption measurements in our ITO and a-Si:H layers suggest that most of this loss is due to parasitic blue absorption in the a-Si:H emitter.

Table 1. 1-cm^2 ITO/a-Si:H/c-Si/Al-BSF HJ solar cells in comparison with the standard 4-cm^2 SiN_x:H/c-Si/Al-BSF DJ solar cells (NREL independently verified)

ID	emitter	V_{oc} (V)	J_{sc} (mA/cm^2)	F.F. (%)	Eff. (%)	Substrate flat FZ(p)
16C	HJ	0.645	33.11	79.2	16.9	1.0 Ω·cm
65C	HJ	0.652	32.16	80.5	16.9	0.5 Ω·cm
5-5	DJ	0.630	34.90	78.1	17.2	1.0 Ω·cm
3-40	DJ	0.636	33.82	78.9	17.0	0.5 Ω·cm

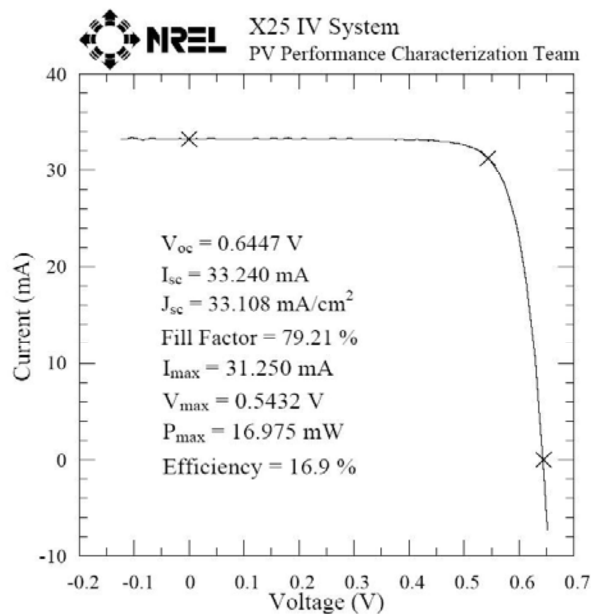

Fig. 10. I-V curve of solar cell 16C.

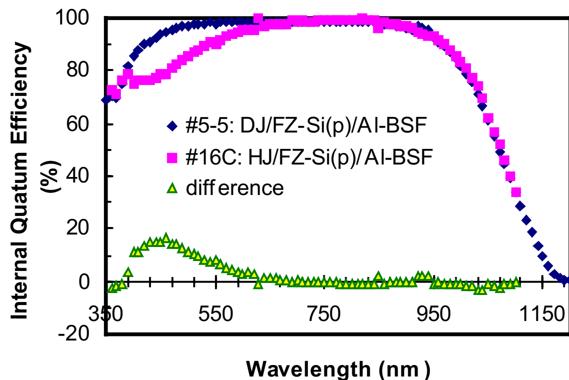

Fig. 11. Spectral responses of the DJ solar cell and the HJ solar cell, excluding the front reflective loss.

SUMMARY

Effective a-Si:H/c-Si heterointerfaces that allow efficient transport of charge carriers with minimal recombination loss can be obtained with immediate a-Si:H deposition and an abrupt and flat interface to the crystalline-silicon substrate. An abrupt and flat interface means that the a-Si:H/c-Si interface area is minimal, defect density stays low, and the bandgap on the amorphous side of the interface is large. This is accomplished by low-temperature deposition (<150°C for (100) and <200°C for (111)) of the thin silicon layers. A planar HJ record efficiency of 16.9% with a high V_{oc} of 652 mV is achieved using screen-printed Al-BSF on untextured FZ-Si. Beneficial H pretreatment by HWCVD is limited to a very short period prior to emitter deposition. With adequate H pretreatment, an undoped a-Si:H thin layer does not seem to be necessary for the p-type wafer-based HWCVD heterojunction solar cells. Higher V_{oc} exhibited by heterojunction cells compared to similar diffused-junction cells indicates excellent interface passivation by the a-Si:H emitter. Minimization of parasitic absorption in the emitter, as well as front surface texturing, should increase J_{sc} significantly.

ACKNOWLEDGEMENTS

The authors would like to thank Charles Teplin, Yueqin Xu, Scott Ward, Anna Duda, Richard Crandall, and Pauls Stradins for their valuable technical assistance and discussion. This work is supported by the U.S. DOE under Contract #DE-AC36-99G010337.

REFERENCES

[1] M. Taguchi, K. Kawamoto, S. Tsuge, T. Baba, H. Sakata, M. Morizane, K. Uchihashi, N. Nakamura, S. Kiyama, and O. Oota, *Prog. PV Res. Appl.* **8,** 2000, p. 503.

[2] T.H. Wang, M.R. Page, E. Iwaniczko, D.H. Levi, Y. Yan, H.M. Branz, V. Yelundur, A. Rohatgi, G. Bunea, A. Terao, and Q. Wang, *14th Workshop on c-Silicon*, Winter Park, CO, August 8-11, 2004; NREL/BK-520-36622, p. 74.

[3] D.H. Levi, C.W. Teplin, E. Iwaniczko, R.K. Ahrenkiel, H.M. Branz, M.R. Page, Y. Yan, Q. Wang, and T.H. Wang, *Materials Research Society Symposium Proceedings Vol. 808*, 2004, p. 239.

[4] M.R. Page, E. Iwaniczko, Q. Wang, D.H. Levi, Y. Yan, H.M. Branz, V. Yelundur, A. Rohatgi, and T.H. Wang, *14th Workshop on c-Silicon,* Winter Park, CO, August 8-11, 2004; NREL/BK-520-36622, p. 246.

[5] T.H. Wang, Q. Wang, E. Iwaniczko, M.R. Page, D.H. Levi, Y. Yan, C.W. Teplin, Y. Xu, X.Z. Wu, and H.M. Branz, *19th European PV Solar Energy Conf.,* Paris, France, June 7-11, 2004. p.1296.

[6] F. Roca, J. Cárabe, A. Jäger-Waldau, *19th European PV Solar Energy Conf.,* Paris, France, June 7-11, 2004, p.1321.