DEVELOPMENT OF MICROMACHINED MILLIMETER-WAVE MODULES FOR NEXT-GENERATION WIRELESS TRANSCEIVER FRONT-ENDS

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DEVELOPMENT OF MICROMACHINED MILLIMETER-WAVE MODULES FOR NEXT-GENERATION WIRELESS TRANSCEIVER FRONT-ENDS

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To my beloved family

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LIST OF SYMBOLS AND ABBREVIATIONS

$\sim$	approximately equal to
$>$	greater than
$<$	less than
DUT	device-under-test
C	centigrade
CB-CPW	conductor backed coplanar waveguide
CPW	coplanar waveguide
CMOS	complementary-metal-oxide-semiconductor
CTE	coefficient of thermal expansion
Cu	copper
dB	decibel
dpi	dots per inch
E-plane	electric plane
ϵ_r	dielectric constant
$\circ$	degrees
FBW	fractional bandwidth
FET	field-effect transistor
f_o	center frequency or cut-off frequency or resonant frequency
ft	foot
GaAs	gallium-arsenide
GHz	gigahertz = 10^9 cycles per second
H-plane	magnetic plane
LCP	liquid crystal polymer
LTCC	low-temperature co-fired ceramic
M	coupling matrix

M_{xy}	coupling coefficient between nodes x and y
MEMS	micro-electro-mechanical-system
μm	microns = 10^{-6} meter
mm	millimeter = 10^{-3} meter
MMIC	monolithic microwave integrated circuit
NASA	National Aeronautics and Space Administration
pF	pico farads = 10^{-12} farads
Q_e	external quality factor
Q_L	loaded quality factor
Q_u	unloaded quality factor
RIE	reactive ion etch
RF	radio-frequency
Si	silicon
SoC	system-on-a-chip
SOLT	short, open, load, and thru
SoP	system-on-a-package
$tan\ \delta$	loss tangent
TRL	through-reflect-line
TZ	transmission zero
WLAN	wireless local area network

SUMMARY

This thesis discusses the design, fabrication, integration and characterization of millimeter wave passive components using polymer-core-conductor surface micromachining technologies.

The first several chapters present the development of a W-band broadband micromachined monopole antenna on a lossy glass substrate, a Ka-band elevated patch antenna, and a V-band micromachined horn antenna. A simple CPW feeding scheme is used for each of them. The design methodology is described and the antenna performance is documented. All antennas have advantages such as a broad operating band and high efficiency.

Next, a low-loss broadband coupler is presented. By elevating a microstrip coupler in the air, broadband coupling and reduced attenuation can be achieved. Meanwhile, a high-Q cavity for millimeter-wave applications, using surface micromachining technologies is reported.

There are two chapters focused on the development of low-loss all-pole band-pass filters and transmission-zero filters, respectively. Both are implemented using polymer-core conductor surface micromachining technologies. By combining 3-D structures and planar transmission lines, novel coupling structures can be designed to create transmission zeros. Superior simulation and measurement results show that polymer-core conductor surface micromachining is a powerful technology for the integration of high-performance filters.

Finally, integration of high performance millimeter-wave transceiver front-end using polymer-core-conductor surface micromachining technology is presented for the first time. By elevating a cavity-filter-based duplexer and a horn antenna on top of the substrate and using air as the filler, the dielectric loss can be eliminated. A full-duplex transceiver front-end integrated with amplifiers are designed, fabricated, and comprehensively characterized to demonstrate advantages brought by this surface micromachining technology. It is a low loss and substrate-independent solution for millimeter-wave transceiver integration.

CHAPTER I

INTRODUCTION

1.1 Background

Increasing system performance and reducing fabrication cost are both imperative with the growing demand for high data rate and affordable communication modules for next-generation communication systems, especially in the millimeter-wave frequency range [70][35].

The lower-band frequency spectrum is already jammed. However, there is still a large amount of unused bandwidth in the millimeter-wave spectrum. In some countries, there is up to 7 GHz unlicensed bandwidth at the vicinity of 60 GHz, which can be used to support high-speed multimedia data transmission. Therefore, much research activity is taking place in millimeter-wave wireless communications.

Millimeter-wave active circuitries, such as amplifiers and oscillators, are fabricated using semiconductor micro-fabrication processes. However, high-performance millimeter-wave three-dimensional (3-D) passive modules such as parabolic antennas and cavity-based waveguide filters are mainly manufactured using traditional mechanical methods. They are usually stand-alone components, available for hybrid board-level integration. The millimeter-wave passive components can also be printed on top of semiconductor substrates to facilitate a monolithic integration with active devices.

In the past several decades, the introduction of planar transmission lines such as microstrip, stripline, or coplanar-waveguide has provided great flexibility and compatibility with active devices. However, there are quite a few disadvantages associated with these planar geometries. These include parasitic coupling, radiation, dramatically increased ohmic loss at the higher frequency, dielectric loss, and frequency dispersion. These effects seriously deteriorate electrical performance and lead to costly and time-intensive design cycles . Furthermore, for a planar antenna directly printed on those semiconductor substrates such as Si, GaAs, and SiGe, it is easy to trigger surface wave propagation and distort the radiation

pattern because of the high substrate dielectric constant. The antenna bandwidth is very narrow and cannot support well high-speed data transmission.

Suppressing some of these electromagnetic mechanisms, such as parasitic radiation and coupling, has led to improved performance, but requires very sophisticated design, which adds considerably to the volume, weight, and cost of the circuit [27][73][72]. This has put the monolithic integration of the whole system in a dilemma.

The advances in semiconductor-processing techniques offer an historic opportunity to provide integration along all the directions of three-dimensional space. The capability to use one more dimension and a few more parameters in the circuit design has led to revolutionary geometries. This makes it possible to integrate complicated 3-D components on the same wafer that carries planar active circuitries. These 3-D components are inherently high-performance compared with their planar counterparts. This helps reduce ohmic loss and eliminate electromagnetic-parasitic effects without affecting the monolithic character. This has dramatically increased the system performance and lowered the manufacturing cost.

1.2 Micromachining Technologies

This enabling technology is called micromachining. According to Wikipedia [1], micromachinery is fabricating mechanical objects in the same general manner as integrated circuits, such as photolithography, etching, and thin-film deposition. Micromachining technology, by utilizing the modern microelectronic processes to realize the function of traditional mechanical machining in a smaller scale, offers both the superior electrical performance coming from the 3-D structures and the process compatibility with the standard semiconductor technology. It has been extensively studied and used in both academia and industry. Many types of micromachining technologies have been developed and studied. These include silicon bulk micromachining, thin-film surface micromachining, polymer/ceramic micromachining and metal micromachining. All of these technologies have their own pros and cons. The details are discussed in the following paragraphs.

Micromachining technology for RF/microwave electronics was pioneered by research

groups at the Univerisity of Michigan almost 20 years ago[11]. Membrane-supported millimeter-wave components, fabricated using wet etching silicon bulk micromachining technologies were extensively studied there, as well as by other researchers later on. A variety of monolithic, quasi-planar transmission-line geometries, which will support transverse-electromagnetic (TEM) wave propagation, can be developed using semiconductor micromachining. Other passive components such as membrane-supported microstrip filters, high-performance microstrip patch antennas by partially removing the silicon substrate, and horn-backed dipole arrays for W-band imaging applications have also been studied [58][57][36]. Most of the work involves using KOH to anisotropically etch silicon wafer. It generates a slope rather than vertical sidewall [9]. Thus, deep RIE dry etching is used since it provides a vertical sidewall. It was used first in optical device fabrication such as for optical waveguides. Then the research was extended to THz applications and micromechanical devices to form a vertical deep trench. The major limitation is the requirement to stack several wafers to build microwave/millimeter-wave components because the corresponding wavelength is on the order of several millimeters and a single wafer with the thickness of several hundred microns is not enough [45].

A via-based multi-layer technology, so-called EBG filters, a substrate waveguide, and the LTCC process [29][43] can achieve a two-and-a-half-dimension (2.5 D) integration. However, the component performance fabricated by these processes relies heavily on the substrate properties. This is because the components are built in the substrate. The dielectric constant and loss tangent associated with the substrate directly affects component performance. Usually, low-loss materials such as ceramics are widely used. However, ceramics generally have high permittivity, which is a disadvantage for antenna integration.

Surface micromachining is another technology that has been developed for high-performance passives integration. Unlike bulk micromachining, surface micromachining is substrate-independent. It usually builds complicated micromechanical components by utilizing sacrificial layers. It has been widely used in RF MEMS switches [39][53]. Other than MEMS switches, most surface micromachined components usually emphasize mechanical functions [5][8]. As for other RF applications, several Korean researchers have successfully utilized

thin-film polymer sacrificial layers and developed an elevated microstrip transmission line, coplanar waveguide, and demonstrated their applications in hybrids and filters [38][37]. The maximal elevation of the structure is less than tens of microns.

Microstrip-based components can actually benefit from this order of elevation since the dielectric loss is removed. However, this order of elevation is not enough for a broadband antenna. Jeong-Geun Kim reported a V-band patch antenna [36] elevated by 200 microns. This was achieved by spinning photoresist twice and electroplating for an extremely long time . This reaches the limitation of thin-film polymer micromachining, but the performance improvement did not completely pay off with this timely and costly process.

A laser-based photo-curable polymer stereo-lithography method has been extensively studied in recent years [22]. In the stereo-lithography process, a 3-D solid part is created using a laser beam to scan on a liquid monomer and cure it into polymer in a line-by-line and layer-by-layer sequence. It is an additive process, which requires no mask, no molding, and no special tooling. Researchers have demonstrated a lot of 3-D microwave stand-alone components such as cavities, filters, and 3-D antennas. They demonstrate the process to be a repeatable, accurate manufacturing method. The tolerance, surface roughness, and metallization techniques have been investigated. However, the metallization scheme is very complicated and consists of two steps: the first one is coating the entire structure with a conductive ink and the second one is electroplating the entire surface. If patterning the metal is needed, laser ablation must be used to rip off metal from the specific region. This process is not compatible with CMOS processes. Furthermore, if the metal has to be removed from inside the cavity, a laser beam cannot reach it easily. Another big issue is the difficulty of integrating with other planar components. The formation of those complicated 3-D structures needs a separate setup. The structure is held on a special platform and immersed into the resin tank. After one layer is patterned and cured, the platform is lowered and a new layer of resin is coated and dispensed by a re-coater blade. This is not a compatible approach for monolithic integration with other planar components.

1.3 *Enabling technology: concept of Polymer-core conductor*

In this dissertation, one specific micromachining technology and its applications in millimeter-wave transceiver front-ends are systematically studied. This technology is the so-called thick-film polymer surface micromachining. This dissertation mainly discusses research efforts on developing various millimeter-wave components using this technology.

The invention of thick-film negative photo-curable resin SU-8 is revolutionary for thick-film polymer micromachining. With its excellent optical and mechanical properties, SU-8 has gained popularity [16]. High-aspect ratio 3-D structures based on SU-8 can be made on top of the substrate up to 1 2 mm with almost vertical sidewalls [79][80]. With this advance, 3-D structures that cannot be built using the aforesaid thin-film technology can now be explored using thick-film polymer micromachining. These include a vertical monopole antenna, a completely air-lifted patch antenna, waveguide-based structures such as a cavity filter and a duplexer, as well as other microwave/millimeter-wave components that require high elevation.

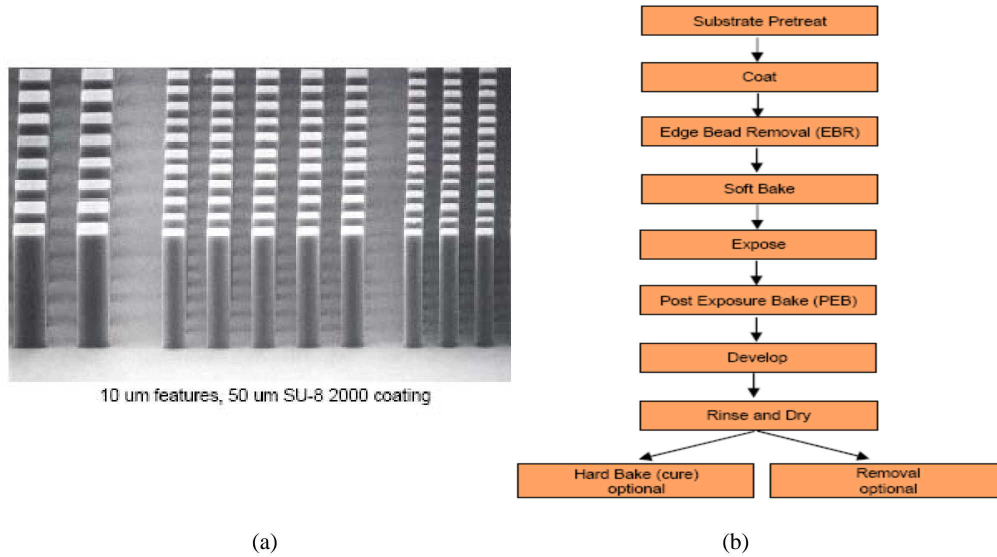
Basically, SU-8 is a photo-definable polymer resist. The following section describes its physical properties and handling techniques.

1.3.1 Properties of SU-8

Based on the processing guidelines on Microchem's web site [2], SU-8 is "a high contrast, epoxy based photoresist designed for micromachining and other microelectronic applications, where a thick, chemically and thermally stable image is desired. Film thicknesses of 0.5 to 200 microns can be achieved with a single coat process. The exposed and subsequently thermally cross-linked portions of the film are rendered insoluble to liquid developers. SU-8 is capable of producing very high aspect ratio structures and is best suited for permanent applications where it is imaged, cured and left on the device." Figure 1.1 shows an image of high-aspect ratio SU-8 pillar arrays to demonstrate its unique capability.

The following table summarizes SU-8's important physical properties related to our millimeter-wave integration research:

Compared with other negative-tone photoresists, SU-8 is far more sticky and viscous.



(a) (b)

Figure 1.1: (a)vertical sidewall pillars SU-8 pillars, demonstrating its capability of building high aspect-ratio structures (b)general fabrication flow of SU-8.(Courtesy of MicroChem)

Table 1.1: SU-8 physical properties.

Physical property	value
Adhesion Strength (mPa) Silicon/Glass/Glass with HMDS	38/35/35
Coeff. of Thermal Expansion (CTE ppm)	52
Youngs Modulus (Gpa)	2.0
Dielectric Constant (10MHz)	3.2

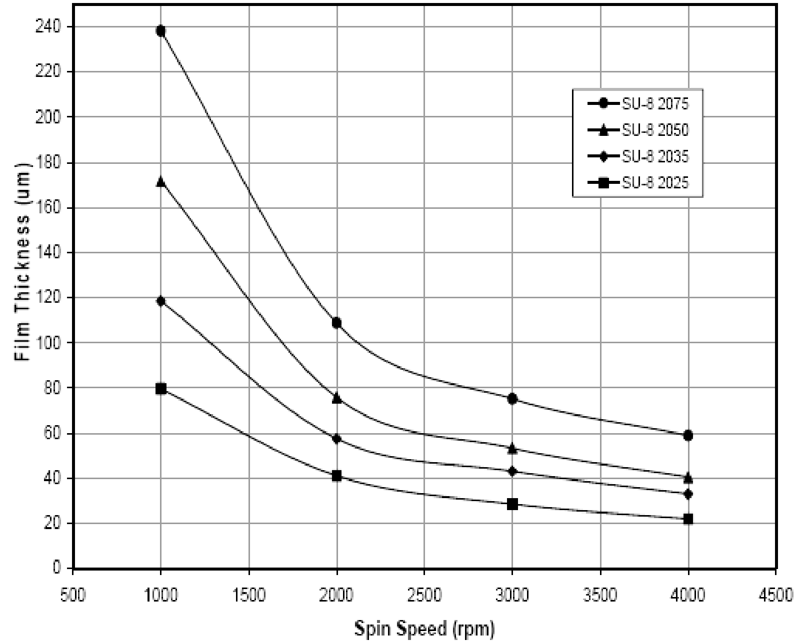


Figure 1.2: SU-8 2000 spin speed versus thickness.

It is hard to handle but can a create thicker coating than other photoresists. Figure 1.2 shows SU-8 coating thickness versus spinning speed. As can be seen, a coating of several hundred microns of SU-8 can be easily achieved.

1.3.2 Fabrication flow for a polymer-core conductor

A polymer-core metal-coated conductor based on the SU-8 resin was proposed in [80]. Using the cured SU-8 as a mold and then selectively covering its surface with the metal whose thickness is 3-5 times the skin depth at the interested frequency, one can get a polymer-core metal-coated conductor that acts electrically as a solid conduct sheet/rod/wire. Figure 1.3 demonstrates this concept and shows the cross-section of a CPW-fed polymer-core conductor.

In this dissertation, a number of millimeter-wave transceiver front-end modules have been designed, fabricated, and characterized based on this polymer-core conductor concept. The integration of these modules into a substrate independent transceiver front-end is also explored.

Before discussing details of the electrical designs of these components, we first present a

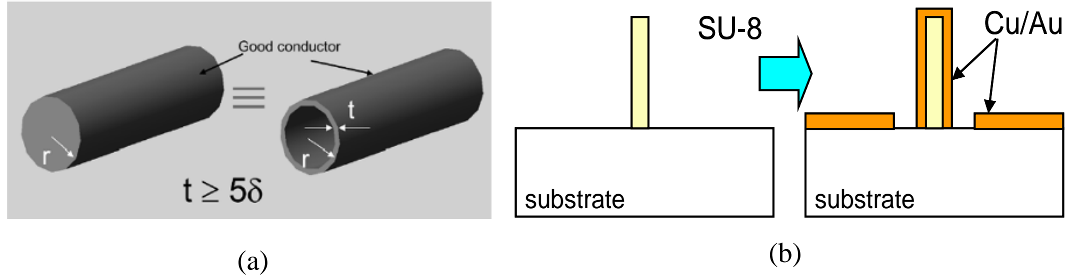


Figure 1.3: (a) The solid conductor vs. hollow conductor (b) polymer core of the conductor vs. after metallization (Courtesy of Y. K. Yoon [80]).

standard fabrication flow for a CPW-fed polymer-core conductor pillar in this chapter. The CPW-fed polymer-core conductor pillar with conformal metal coverage is the basic building cell for other complicated components in this dissertation. Unique steps and variations from this stand fabrication flow for a specific component are covered in other chapters.

There are many versions of fabrication flow to make a polymer-core conductor in terms of choosing metallization schemes, photo-resists, and photolithography methods. Figure 5.6 shows the one we have used for our applications.

Most structures discussed in this dissertation are higher than 300 microns. Great side-wall metal coverage is required. Although SU-8 patterning can create a virtually vertical sidewall, it is not purely vertical when the height is above several hundred microns. Back-side exposure is preferred for these high structures although front-side exposure also works; backside exposure gives better mechanical robustness and gains better metal coverage in a DC sputterer.

For back-side exposure, a transparent substrate such as glass can be used. By simply covering the wafer with a UV-blocking material such as Cr and Ag, leaving openings only for SU-8 pillars, nice SU-8 pillars can be created using back-side exposure. To metalize these pillars, a DC sputterer is used because it can give better sidewall coverage.

Now another mask is used to remove the metal at CPW slot regions. To prevent the metal on the pillar sidewall being removed, photoresist has to be used to protect the metal on the sidewall . However, it is not easy for photoresist to climb up several hundred microns to conformally cover pillars. So etching is not feasible here to remove metal at the slot region.

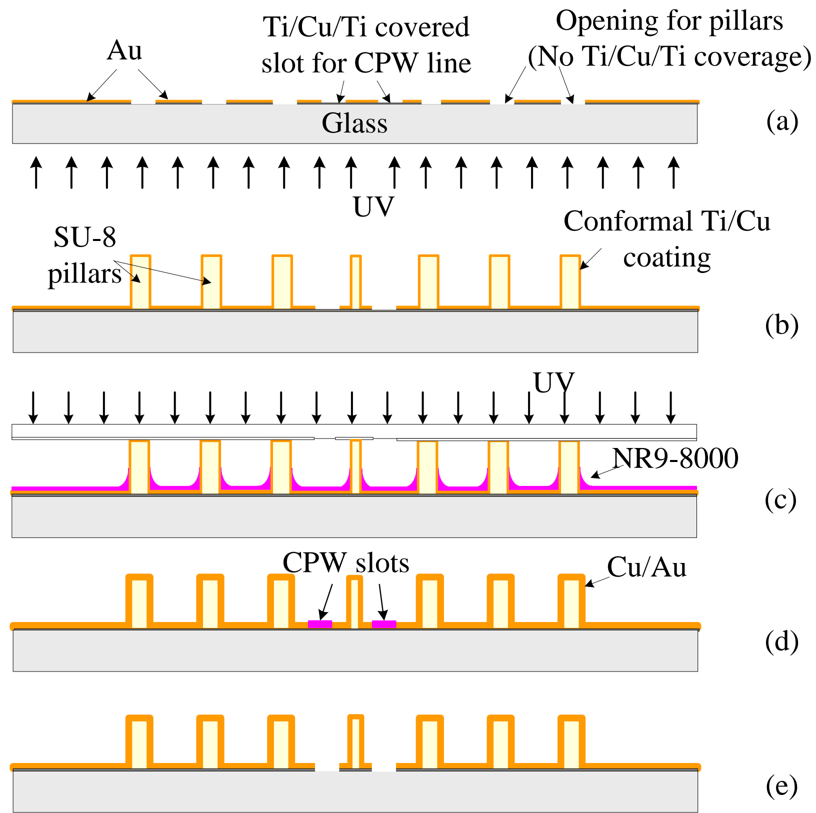


Figure 1.4: A general fabrication flow for polymer-core conductor with a CPW feeding line

One possible scheme to solve this problem is to first cover the slot region with photoresist and then electroplate the uncovered region with another type of metal. After electroplating, a specific metal etchant is used to remove the seed layer metal only, without attacking plated sidewall metal. Negative tone photoresist with a dark-field mask is used to protect the slot region. Positive tone photoresist with a clear-field mask is not a practical combination here. This is because photoresist will climb up and accumulate at the bottom of the SU-8 pillars and is much thicker than other regions. It needs an extremely large optical dose to decompose photoresist at this region. Over-exposure will ruin the patterns that cover CPW slot regions.

Even if the combination of negative-tone photoresist and a dark-field mask is a feasible scheme, there are other issues. Because of the existence of SU-8 pillars, coverage of the negative-tone photoresist is not uniform across the wafer. When photoresist passes the vicinity of pillars, its thickness changes. Although the same amount of optical power density is measured across the whole wafer, different line widths are generated when the thickness is not uniform. This eventually leads to a width-varying CPW-slot, and the characteristic line impedance is no longer constant. Consequently, we can no longer trust the measured electrical performance of these 3-D structures.

One solution to this problem is pre-patterning a CPW line before patterning the SU-8 pillars. In a back-side exposure scenario, SU-8 patterns will also appear on top of the slots if the slot regions are not covered by a UV-blocking material. So, additional steps are needed to cover the slot regions.

The fabrication steps depicted in Figure 5.6 are an optimized process flow that addresses the above concerns.

In (a), a seeding layer of Ti/Cu/Ti is sputtered onto a transparent glass wafer. The bottom Ti layer is for adhesion enhancement. Cu is used as the seed layer for gold electroplating to create CPW lines and slots. Based on our experiments, Cu is a very good seed layer for gold plating. Although gold can also be used as a seed layer, Cu is used instead. It is not just cheaper, but more importantly, it can be easily removed at the last step. The copper etchant will not etch electroplated gold that covers the SU-8 pillar surface in the

following steps.

A layer of positive photoresist is coated and patterned to prevent CPW slots and openings for SU8 pillars being plated. CPW dimensions are also determined in this step. Compared with a proximity alignment scheme in which CPW dimensions are defined after SU-8 pillars are created, this contact-mode alignment gives more accurate CPW dimensions.

Gold electroplating follows and another mask is used to etch Ti/Cu/Ti away from the place where there will be SU-8 pillars. CPW slots are protected in this step and Ti/Cu/Ti in that regions remains.

In (b), a certain thickness of SU8 is coated onto the substrate. Both gold and Ti/Cu/Ti can effectively block UV exposure, so only SU-8 on top of the unmetalized openings gets exposure and is cross-linked. SU-8 pillars are created and another layer of Ti/Cu/Ti is sputtered to conformally cover the whole structure. Again, Ti is used for adhesion enhancement and Cu is used as the seed layer for gold plating. Cu is used because during gold plating, plated gold on the sidewall is thinner than the one on the substrate, especially at the bottom of SU-8 pillars. If a gold seed layer is used, the gold etchant to remove the seed layer later in the last step will also etch the sidewall gold at the same time. As a result, sidewall gold coverage will not be great. Although increasing gold plating time leads to better sidewall coverage, the thickness of photoresist used to cover slot regions is not thick enough to support over-plating. In our experiment, we have observed that when a CPW line photoresist pattern passes between two pillars that are very close to each other, the thickness is less than the one on other regions. The electroplated gold thickness will first exceed the thickness of photoresist covering CPW slots at these regions. So, simply increasing gold plating time does not always help. On the contrary, since the copper etchant usually does not attack sidewall gold, we don't need to use over-plating.

In (c), a layer of negative-tone photoresist NR9-8000 is used to cover CPW slots. NR9-8000 is chosen because it can reach 17 microns with a single coating and is thick enough for electroplating. Also, it is relatively easy to remove after electroplating. Diluted SU-8 resin can also be used here to cover CPW slots but is very hard to remove after UV exposure.

Photoresist patterns to cover CPW slots still have distortion because a proximity exposure is used and SU-8 pillars still affect the profile of photoresist coating; nevertheless, CPW dimensions have already been determined in step (a). As long as NR9-8000 patterns are larger than the predetermined CPW slots, slot widths remain unchanged.

In (d), the top Ti layer is removed after NR9-8000 is patterned and electroplated gold deposits directly on Cu seed layer. After electroplated gold achieves a thickness of several microns, NR9-8000 is washed away. Except for the layer of Ti/Cu/Ti/Cu/Ti on CPW slot regions, a layer of gold covers the whole structure.

In (e), all of the seed layers are removed from CPW slots region and the structure is released.

1.3.3 Advantages of a polymer-core conductor

From the above fabrication flow, one can easily see that there is no high-temperature process step. Only standard semiconductor micro-fabrication techniques are used, such as photolithography and metal deposition. All process conditions are CMOS-technology compatible. In other words, 3-D millimeter-wave structures can be fabricated together with low-cost CMOS circuitry. It can build 3-D and planar structures at the same time. This will eventually bring a monolithic integration solution to solve all issues discussed earlier in this chapter.

This method is capable of building high-performance millimeter-wave components. Except for feeding lines, various structures are elevated into air to eliminate substrate loss, which is always a big concern for millimeter-wave transceiver integration.

This is also a substrate-independent method. Since in this method, a substrate only provides mechanical support for elevated structures, its electrical properties only have a very minor impact on elevated component performance.

1.4 Contributions and organization

In this dissertation, we have developed a whole library of millimeter-wave passive components using thick-film polymer surface micromachining technology. We have also investigated various issues involved in integrating these individual modules to a fully duplex

transceiver front-end.

The contributions of this thesis are related to the design, fabrication and characterization of multiple novel passive component prototypes, as well as the demonstration of the feasibility and advantages in a fully integrated subsystem.

Chapter 2 focuses on the design, fabrication, and characterization of a micromachined W-band monopole with superior performance. This is the first demonstration of using this polymer-core conductor approach to build a high-performance millimeter-wave radiator. This research has led to a number of peer-reviewed publications and opened the possibility of using such technology to build more complicated 3-D structures.

In Chapter 3, a fully elevated patch antenna has been reported for the first time. Compared with its planar counterpart, it achieves great electrical performance because of the elevation. Full characterization data has been presented both in conferences and journals.

In Chapter 4, the development of a CPW-fed micromachined horn antenna structure is presented for the first time. A prototype horn has been implemented for V-band applications.

A super-broadband elevated microstrip coupler and a high-Q micromachined cavity are presented in Chapters 5 and 6, respectively.

Chapters 7 and 8 present our systematic exploration of various filters using micromachining technologies. Four filter topologies, including two all-pole filters and two transmission-zero filters, have been implemented and discussed in detail in these two chapters. The most advanced filter design theories and methods have been used, along with several novel coupling structures in our work. All of them have been published in the most prestigious microwave conferences and journals.

Chapter 9 summarizes experiences and tricks gained in the integration of various individual functions such as antennas, duplexer, and amplifiers into a fully duplex transceiver front-end for V-band short range wireless applications. The performance of these integrated modules confirms the potential and feasibility of using this technology as a substrate-independent approach for high-performance system integration.

Chapter 10 concludes this dissertation, summarizing its contributions.

CHAPTER II

A W-BAND MICROMACHINED MONOPOLE

2.1 Motivation

Traditionally, planar antennas are widely used in compact millimeter-wave systems as a low-cost solution. Planar antennas and transmission lines are fabricated at the same time since they both use the standard printed circuit board process. Nevertheless, it is well known that printed microstrip patch antennas often suffer from low bandwidth, high loss and radiation pattern perturbation caused by surface wave. All of these drawbacks set limit to use patch antennas in broadband modules and have led to various bandwidth improvement techniques.

On the contrary, cylindrical monopoles and dipoles have broad impedance bandwidths and are better candidates for broadband radiation. The major roadblock for their wide application is these 3-D radiating structures, as well as feeding structures are more complicated than those of printed circuits counterparts and thus hard to be implemented in an integrated manner. It is well known, that in a low-frequency system, a cylindrical monopole is usually fed by a coaxial cable whose outer conductor is attached to the ground and the inner one connects the monopole. A via has to be used. In a low-cost compact millimeter-wave system, this process should be avoided for cost reduction. Therefore, a transition from a planar transmission line to a three dimensional monopole, on the same side to the substrate, is essential to the effective realization of this concept. In our work, a transition from a coplanar waveguide to a vertical monopole is designed and optimized.

A cylindrical dipole antenna is simple to design. Design curves and equations are well documented. The total physical length is around the half-wave length at the operating frequency. A dipole antenna working at 100 GHz has a physical length close to 1.5 mm. As mentioned briefly in the previous chapter, our enabling technology, the thick-film photo-definable SU-8 polymer conductor is capable of making high-aspect-ration 3-D structures

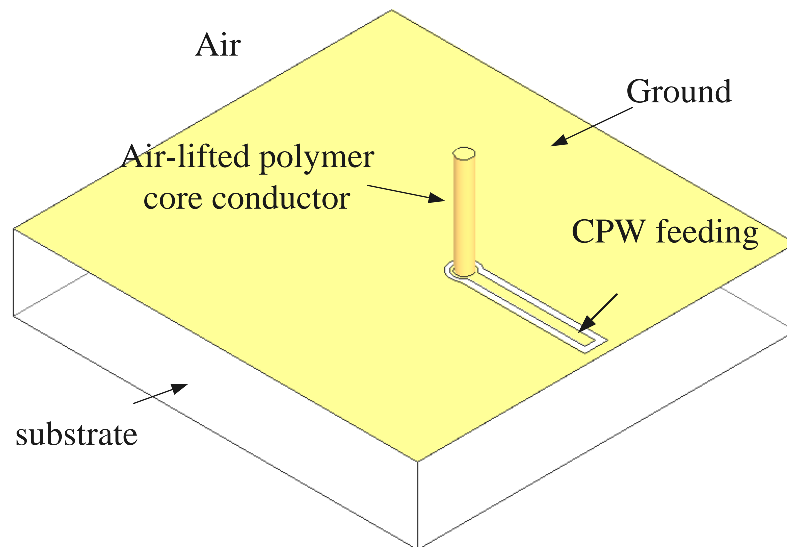


Figure 2.1: Schematic of a CPW-fed micromachined monopole antenna.

on top of the wafer up to 1 mm. Coating SU-8 thicker than 1 mm is possible but the optical energy for exposure cannot penetrate when SU-8 is too thick and most dose is absorbed, preventing it reaches deeper into SU-8. The patterned structure can no longer have a vertical sidewall and will have an exaggerated lateral profile resulted from UV exposure diffraction. Another challenge for integration of a dipole antenna is the need of a balun which complicates integration process and thus increases the cost.

Instead, a monopole antenna is investigated in our work. For a cylindrical monopole antenna, the physical length is usually a quarter wave length of the operating frequency in the free space. This is only half of the dipole length. So, making a vertical W-band monopole on top of the wafer using the idea of the polymer core conductor is more feasible.

2.2 W-band monopole

Figure 2.1 shows the micromachined monopole investigated in our research. The quarter-wavelength monopole stands vertically at the end of the CPW line center conductor. The CPW line is configured as an open-end stub. The two sides of the ground plane are connected radially to enclose the monopole bottom.

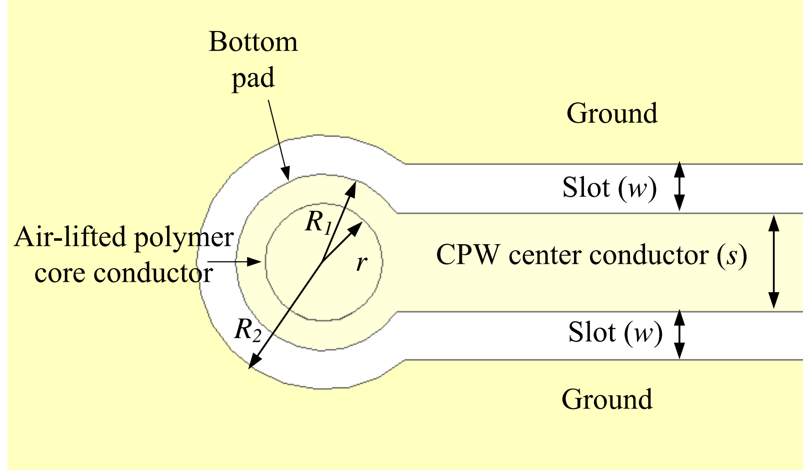


Figure 2.2: Top view of a CPW-fed micromachined monopole antenna.

2.2.1 monopole design

The top view and the illustration of key geometrical parameters are shown in Figure 2.2. The radius of the monopole r, the radius of the bottom pad $R1$, the radius of the ground aperture R, the center conductor line width s, and the gap width w between CPW ground and the center conductor have been optimized with Ansoft HFSS 9.0. The gap width w is fixed to 50 μm because of the limitation of fabrication accuracy at the time when this project was done. The minimum diameter of the monopole is set to be 80 μm after considering the aspect-ratio constraint for SU-8. The bottom pad radius $R1$ should be larger than the radius of the monopole r. This constraint is for the fabrication feasibility; the bottom part of the monopole sidewall cannot be electroplated if there is no space between the CPW slot and the monopole since the slot is covered by photo-resist during the electroplating.

The theoretical input impedance of the quarter-wave length monopole is 36.5 Ω at resonance. At the time when the project was done, the measurement system was calibrated to 50 Ω using an SOLT calibration kit. The input line impedance is thus designed to be 50 Ω using Agilent ADS LineCal for various substrates, as shown in Figure 2.3. There is an obvious mismatch between 50 Ω and 36.5 Ω.

To minimize reflection, an impedance transformer needs to be designed. A quarter-wavelength impedance transformer, and a parallel single matching stub matching have been considered. However, they introduce discontinuities to the feeding line and thus cause

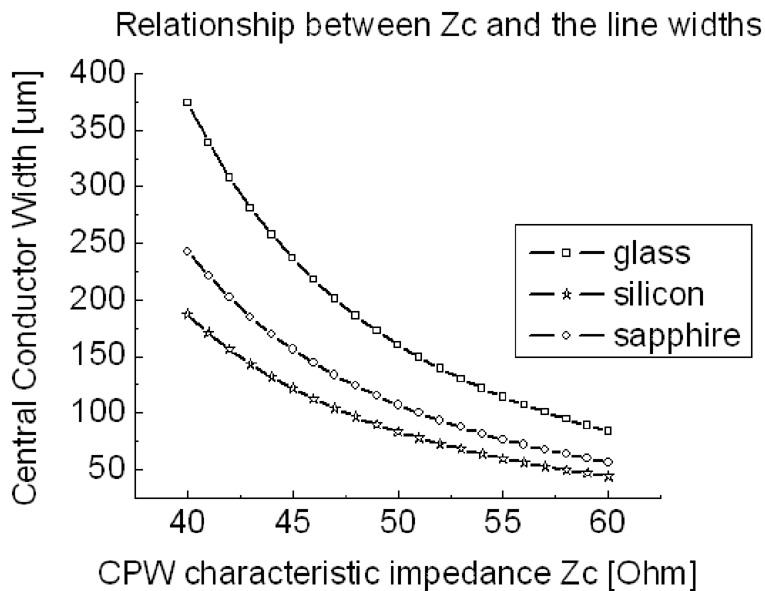


Figure 2.3: Optimization of CPW line dimensions for different substrates.

radiation loss in W-band. The maximum directivity of a quarter-wave length monopole is not high, thus parasitic radiation can easily perturb the desired monopole radiation pattern.

Directly feeding the monopole using a 50 Ω line, while carefully designing the transition at the bottom of the monopole, however, gives a good matching both in simulations and measurements. It has been found that the transition itself functions as an impedance transformer. This is because that the ground pad of the monopole is larger than the diameter of the monopole itself. The parasitic capacitance and the inductance associated with the transition form a simple impedance matching network. Figure 2.4 plots the simulation results of the return loss for a CPW-fed monopole on silicon and sapphire substrate. As can be seen, good matching is achieved with the center frequency is set as 85 GHz when the height of the monopole is chosen as 800 μm.

2.2.2 monopole fabrication and testing results

The fabrication was done on a chromium coated soda-lime glass (Telic Co.) substrate. The glass substrate was chosen because it is low-cost and readily available in the cleanroom when this project was done. It is not an ideal millimeter-wave substrate since there are lots of impurities in this kind of glass. The CPW line attenuation is thus high, as plotted

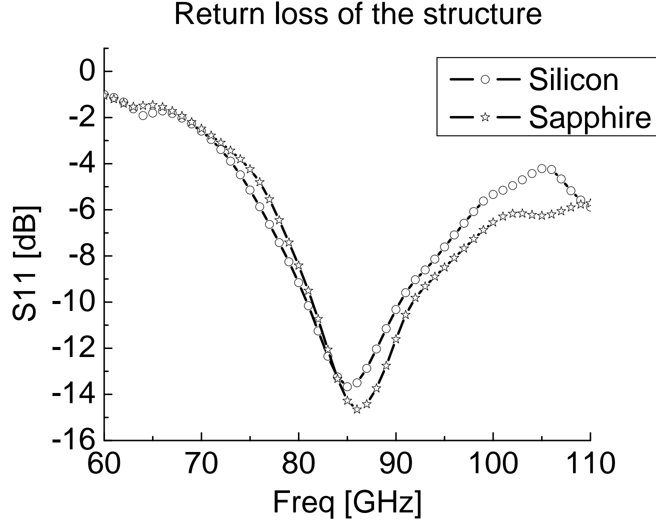


Figure 2.4: Full-wave simulated return loss performance of the micromachined monopole on silicon and sapphire substrates.

in Figure 2.5. As can be seen, the attenuation is larger than 10 dB/cm at the interested frequency. Additionally, based on our characterization result, this type of glass has a ϵ_r of 8.1. Directly printing a microstrip antenna on this high-ϵ_r electrically-thick substrate (1.6 mm here) will definitely bring surface wave and lower radiation efficiency.

However, our proposed method is a substrate-independent solution and the only part lying directly on the substrate is CPW feeding line which can be kept very short in an integrated front-end when a chip can be directly put at the monopole bottom. Here, to test the antenna, we have to keep certain length between probing pads and the monopole itself. We chose 1 mm as a separation. This length approximately introduces 1 dB loss and does not greatly affect the monopole return loss measurement. Since the monopole antenna is built on top of the substrate and a ground metallization blocks the substrate loss, it is inherently a high-efficiency radiator.

Another advantage brought by a glass substrate is it allows for backside exposure. This provides a better mechanical robustness when the monopole is high. When SU-8 coating is thin, the top and bottom get almost same exposure intensity and an ideal vertical structure can be defined. However, when SU-8 is very thick, the bottom gets much higher exposure intensity than the top; a cone shape is created by backside exposure. If a front-side exposure

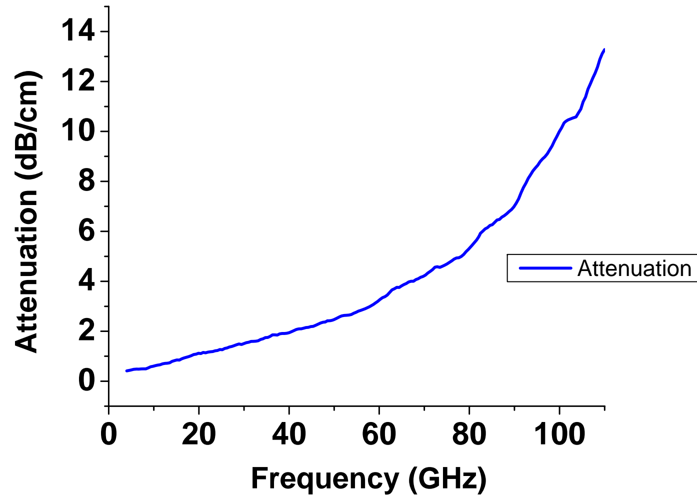


Figure 2.5: CPW line attenuation versus frequency on a soda-lime glass substrate.

is used instead, a reverse-cone is expected and it is very fragile.

Figure 2.6 details the fabrication process. Chromium is patterned for the monopole column definition using a standard photolithography (a). A layer of 800 μm-thick SU-8 is coated on the substrate. This thickness defines the monopole height ultimately. A UV source exposed from the substrate backside to get a mechanically strong column pattern. Metal deposition of titanium and copper using a DC sputterer is performed to have a conformal seed layer. Thin SU-8 (a thickness of 5 μm) is spin-coated on it and patterned for the definition of signal path as well as ground pads (c). Up to 2 μm gold is electroplated through the bottom mold as well as pillar surface uniformly. The thin layer of SU-8, the seed layer and the bottom chromium layer are removed sequentially to complete the process by using plasma etching and metal etchant respectively (d). Figure 2.7-2.9 show SEM pictures of fabricated monopole antennas and a 3 by 3 array respectively.

An Agilent vector network analyzer 8510XF connected to a Cascade GSG 150 probe station that was calibrated with a standard SOLT scheme between 50GHz and 110GHz.

Measurements are performed on two samples and the results are shown in Figure 2.10 and 2.11, where good agreement with simulation can be observed. The structure demonstrates broadband impedance matching and symmetry radiation pattern in W-band. Greater than 10 dB return loss over 19 GHz bandwidth is measured on the soda-lime glass

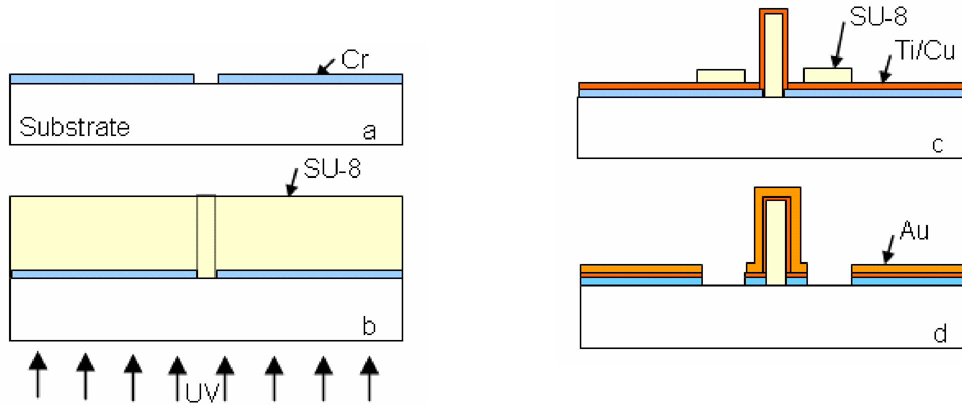


Figure 2.6: fabrication flow of a CPW-fed monopole.

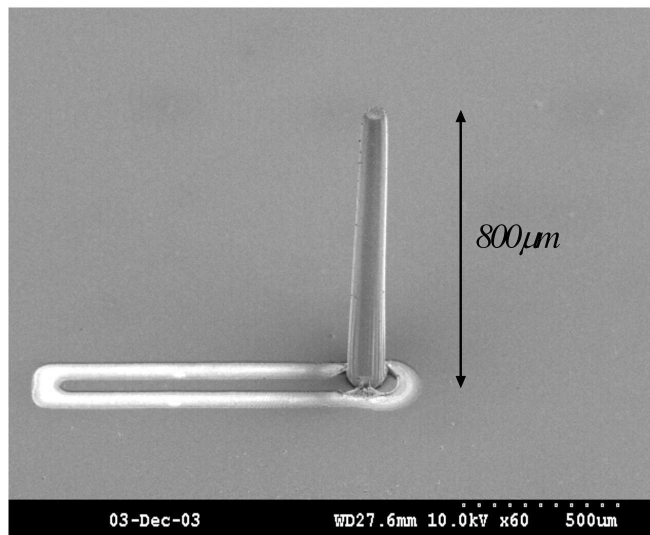


Figure 2.7: SEM picture of the micromachined monopole.

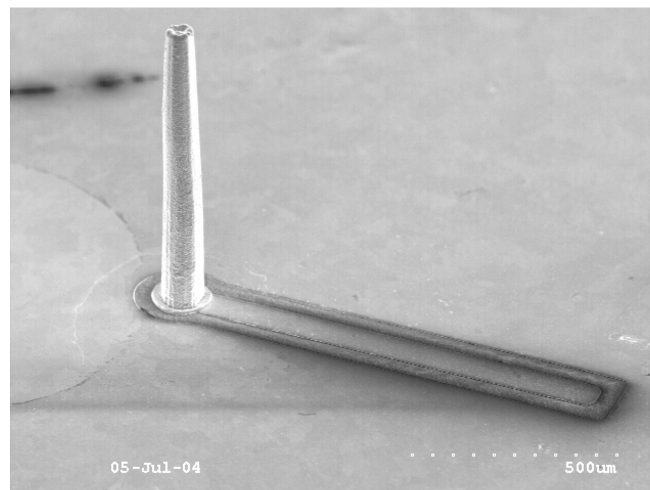


Figure 2.8: SEM picture of the micromachined monopole.

Figure 2.9: 3 by 3 monopole arrays on a glass wafer.

substrate. As can be seen, the resonating frequency is decided by the height of a monopole. Compared with a planar antenna directly printed on the same substrate, the bandwidth improvement is quite significant.

2.2.3 Effects of ground bridge

CPW discontinuities can convert slot mode propagation from the normal CPW mode, resulting in radiation leakage from two slots, especially when the center metal strip is wide and two slots are separated far away. Air bridges to connect the ground are widely used to reduce the slot-mode leakage. Here, since we use a CPW open-end stub to connect the vertical monopole, we studied the effects for ground bridge over a CPW line. Bonding wires can be used to connect two separate grounds. Alternatively, air-bridges can be fabricated. This needs several new masks and thus increases fabrication cost. Wedge bonding wires were used. Figure 2.12 shows an SEM image of a wire-bonded monopole. Measurement shows the same result compared with the one before wire-bonding. This is because of the symmetric nature of the structure and feeding. With this observation, a wire-bonding step can be skipped to simplify the process.

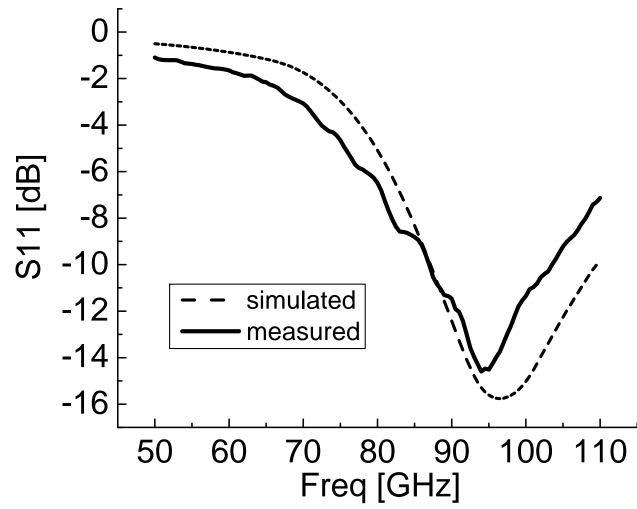


Figure 2.10: Return loss simulation and measurement result for a 700 micron-high monopole

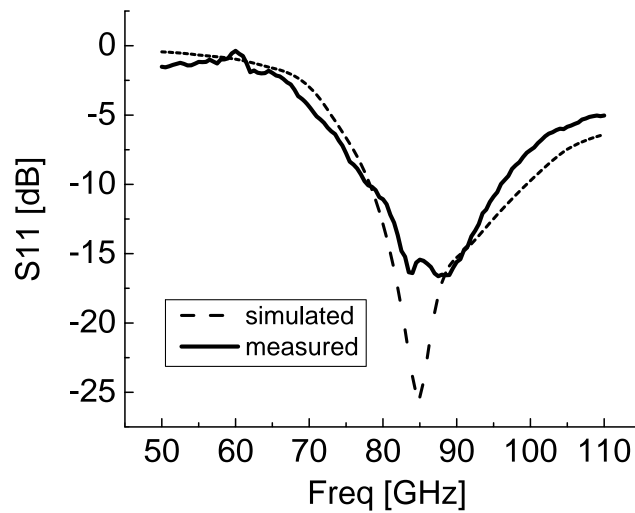


Figure 2.11: Return loss simulation and measurement result for a 800 micron-high monopole

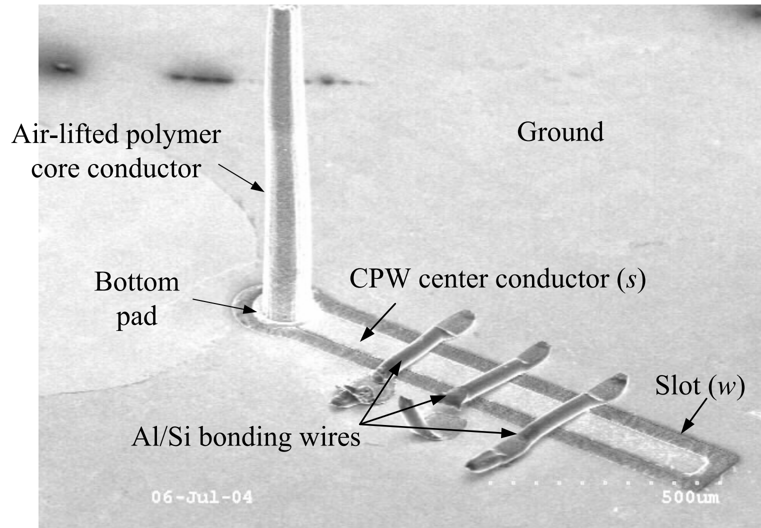


Figure 2.12: SEM picture of a CPW-fed monopole with CPW ground connected using bonding wires

2.3 Chapter summary

In this chapter, we present the development of a broadband micromachined monopole antenna on a lossy glass substrate. A simple CPW feeding scheme is used. The design methodology is described and the antenna performance is documented. A 19 GHz bandwidth has been measured at 85 GHz, confirming the advantages of micromachining technology. In addition, the impact of adding ground bridges to connect CPW grounds are investigated .

This is the first time a high-efficiency vertical micromachined monopole is investigated for W-band operation. Its CPW feeding scheme makes it possible to integrate planar components in a simply manner.

CHAPTER III

A MICROMACHINED PATCH ANTENNA

A patch antenna provides broadside radiation and is widely used in low-cost microwave transceivers. In our research, we have investigated the feasibility of elevating a patch antenna into air by using the surface micromachining technology.

3.1 Background

One limitation of the monopole antenna structure discussed in the previous section is the operating frequency can not be further lowered due to the constraint that the SU-8 thickness can only go up to 1~2 mm. Theoretically, a quarter-wavelength monopole antenna that resonates down to 37.5 GHz can be made using this surface micromachining technology. However, practically, a SU-8 post of 2 mm high is not mechanically strong. It is fragile and prone to fail. Another limitation, in terms of the antenna performance, is that the gain of the monopole is quite limited since it is an omni-directional radiator. So other antenna designs need to be considered. An alternative radiator that outperforms a monopole is a microstrip antenna. Because of low manufacturing cost, good antenna performance and mature optimization tools, microstrip antennas have gained popularity in the emerging wireless communication and sensor applications in the RF/Microwave/millimeter wave regimes. However, there is one big drawback associated with the traditional printed microstrip patch antenna without employing the micromachining techniques. That is, a microstrip antenna shows significant performance degradation due to the excitation of surface waves in high-ϵ_r materials, resulting to lower efficiency, reduced bandwidth, degraded radiation pattern and undesired coupling between the various elements in array configurations. Nevertheless, integrating antennas to a high-ε_r substrate is a must when a high degree of system-level integration is needed for the consideration of compactness and antennas are expected to be easily integrated with other RF parts on a single substrate.

Many efforts have been put forth to integrate quasi microstrip patch antenna by using

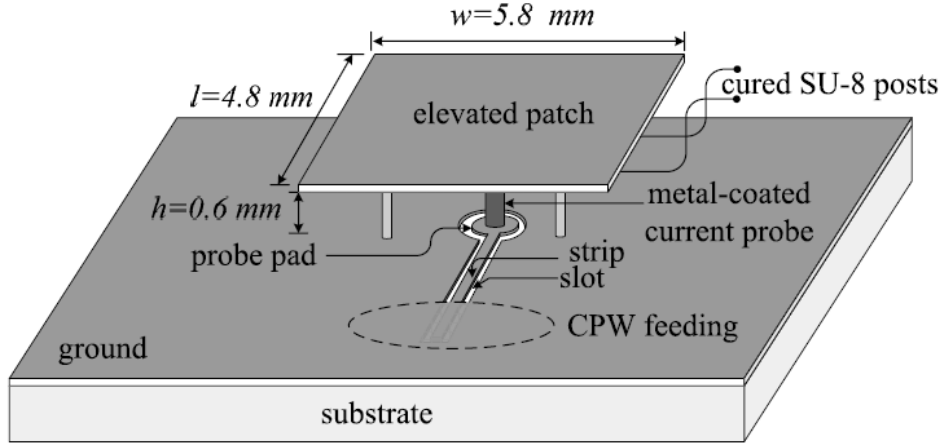


Figure 3.1: Schematic of the proposed elevated patch antenna fed by a CPW-connected micromachined current probe.

micromachining techniques and alleviate the problem caused by surface waves at the same time. Among them, authors of [57] use wetting etching to partially remove the silicon underneath the patch to lower the effective dielectric constant. Authors of [24] use metal posts to lift the patch into air and use proximity coupling method to feed the patch. For both [57] and [24], the effective substrate of patch antenna is a mixture of air and high-ϵ_r materials, so compared to a completely air filled elevated patch proposed in our research, antenna performance is not fully optimized in these work. It has also been demonstrated in [36] that fabricating a 200 microns elevated 60 GHz 2×1 patch array supported by three metal posts is feasible. Since these metal pins are electroplated and it takes extremely long time to complete the fabrication process, it is not cost-effective. Also, it is hard to get more elevation using this method.

In our research, completely lifting the patch antenna into the air by the surface micromachining has been studied. Figure 3.1 shows our elevated patch antenna structure.

The patch is fed by a CPW-connected vertical metal-coated polymer-core probe that we developed in the previous section as a radiator, but now, it is seen rather as a vertical current probe. The probe is connected with the central conductor of a coplanar waveguide on top of substrate using the 3D transition in [36]. The coplanar waveguide feeding scheme is preferred since it is compatible with the assembly of MMIC surface-mount devices and

the ground metal of a CPW line is shared by the elevated patch antenna. This helps remove the air-dielectric interface. Unlike metal posts in [24], several polymer posts are used underneath the patch to support the structure. This can avoid coupling between the supporting posts and the radiating structure. This design offers several advantages. First, this topology effectively creates a low-ϵ_r substrate since the substrate is essentially air (the lowest possible dielectric constant). This will help increase radiation efficiency, directivity, and radiation bandwidth. In addition, for traditional patch antennas integrated with other components, once the substrate specifications are chosen for the whole module, the thickness is a universal variable for each component on this substrate and it cannot be tailored freely and thus optimized for antenna design. However, for the air-elevated patch antenna presented in this section, the height of the vertical probe and polymer posts can be specified in the process and changed from several microns up to 1 mm, regardless of the substrate that is used. This can be used to further enhance the patch bandwidth when we cannot change the substrate thickness for the sake of the rest of the module circuits. Thus, a air-elevated patch can meet different application requirements and be utilized as a substrate-independent solution. Last, but not least, the CPW ground on top of the wafer will totally shield the antenna from the underlying elements and vice versa.

3.2 Antenna design

The elevated patch is designed and optimized to resonate at the LMDS band of 26˜28 GHz. The final size of a prototype patch is 4.8 mm $\times$ 5.8 mm. The patch is elevated by 600 μm. This height is chosen after considering the following factors: first, the more elevation, the more bandwidth the antenna has. secondly, the more elevation, the more difficult the fabrication is and the more fragile the micromachined structure will be. A height of 600 μm is a good choice taking all of these concerns into account.

The structure is simulated using the FEM-based Ansoft HFSS V9.1 software tool and verified using TLM-based Microstripes 6.5. To expedite the simulation, a coaxial feeding scheme is used in simulations to find the optimal probe position and then a CPW section is introduced to connect the probe. Another useful note found here to optimize the patch

Table 3.1: Dimensions of the micromachined patch antenna.

	patch length l	patch width w	patch thickness t	patch elevation h
value	4.8 mm	5.8 mm	0.1 mm	0.6 mm
	substrate ϵ_r	substrate thickness	probe location off edge	probe diameter d
value	8.1	0.6 mm	1 mm	0.2 mm

antenna is to check the real/imaginary parts of the input impedance at the bottom of the current probe instead of using S11 directly. This is because a CPW line, along with parasitic discontinuities at the bottom of the current probe, can create a matching point on S11 plot but that point may not be the resonance frequency of the patch itself since these parasitics also contribute to the imaginary part. The measured antenna gain and the fractional bandwidth provide false characterization information. Instead, from the reading of real/imaginary parts of input impedance, especially the imaginary part, it is easier to find the resonating frequency and tell how different factors affects the antenna properties at resonance.

The design parameters summarized in Table 3.1. Simulation results predict a 7.8% fractional bandwidth around 27 GHz and nearly frequency-independent radiation patterns from 25 GHz to 32 GHz with a maximum directivity of 10.2 dBi observed at 27 GHz (As shown in Figure 3.2). The main beam is along the normal direction of the patch, and the 3-dB beam-width is 62 degree in the E-plane. Also, the simulated 3-D radiation pattern has very low-level side-lobes and back-side radiation (below -20 dB), indicating an improved radiation efficiency because of elimination of surface waves.

3.3 Fabrication and measurement

The proposed patch antenna was fabricated on top of soda-lime glass with a thickness of 0.6 mm. The polymer core of metalized feeding probe was defined with a layer of 600 μm thick SU-8 (MicroChem SU-8 2100). A conformal seed layer of Ti/Cu/Ti was deposited using a DC sputterer. Negative-tone photoresist NR-9 8000 was spun on top of the Ti layer and patterned to cover the slot of the feeding CPW-line and copper was electro-plated to

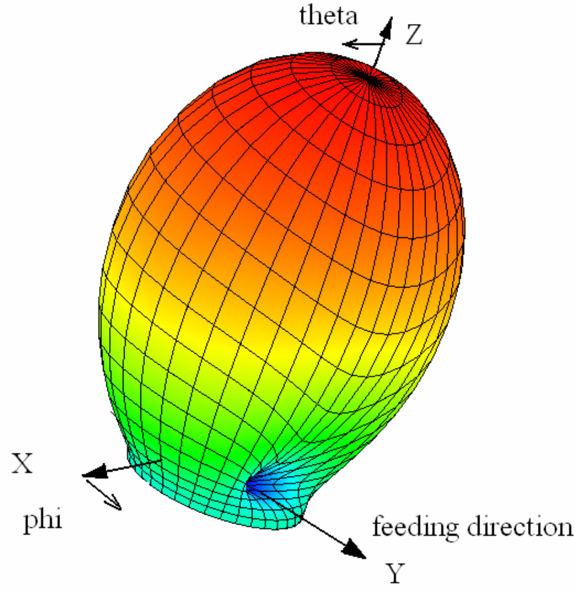


Figure 3.2: Simulated radiation pattern for the elevated patch antenna.

metalize the current probe and ground pattern. A layer of 600 μm thick SU-8 was dispensed and patterned for the second time to define the supporting polymer posts. After all posts had been formed, the assembly of the top patch with the supporting structure was done by flipping the whole structure to align with the vacuum-stuck patch on the bench. The relative positioning was realized with the aid of marker on the ground plane. Silver paste was pre-applied to the post contact areas on the patch using a tiny tip to guarantee good electrical contact between the current probe and the patch. The whole structure was then treated by electroplating bonding techniques described in [37]. At this stage, NR9-8000 was removed and Ti/Cu/Ti on the slot region was etched away. The structure was then released. In the future, batch processing of the elevated patch antenna may be performed using flip chip processing with predefined solder bumps for positioning to the posts.

The fabricated elevated microstrip patch antenna (as shown in Figures 3.3) and 4.6 was characterized by a 2-port Agilent 8510C vector network analyzer with a probe station. The NIST Multical TRL algorithm was used to calibrate the measurement system [48]. The reference plane was set to the bottom of metal-coated epoxy core probe.

Several prototypes were built and characterized. The measured return loss of an elevated microstrip patch antenna, with the parameters given in Table 3.1, is plotted along with the

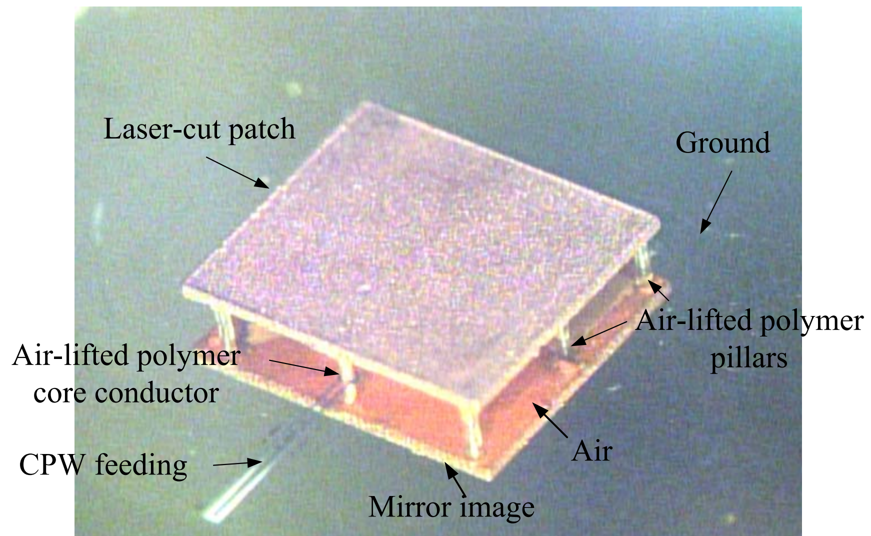


Figure 3.3: A picture of a fabricated micromachined patch with its image on the metal ground also shown.

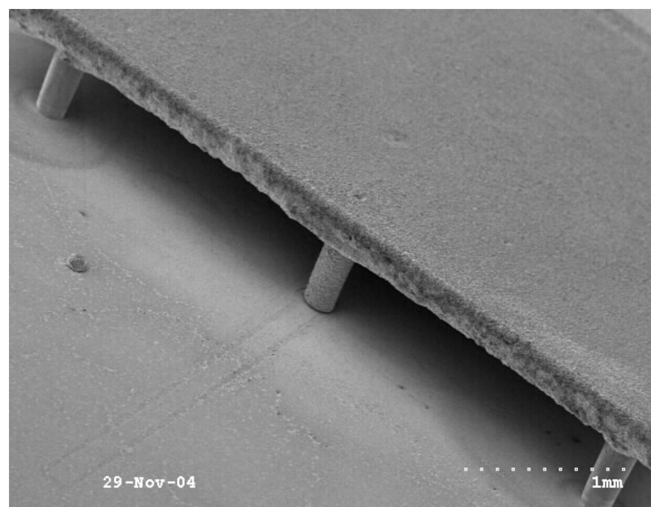


Figure 3.4: A SEM picture that shows the patch edge and pillars.

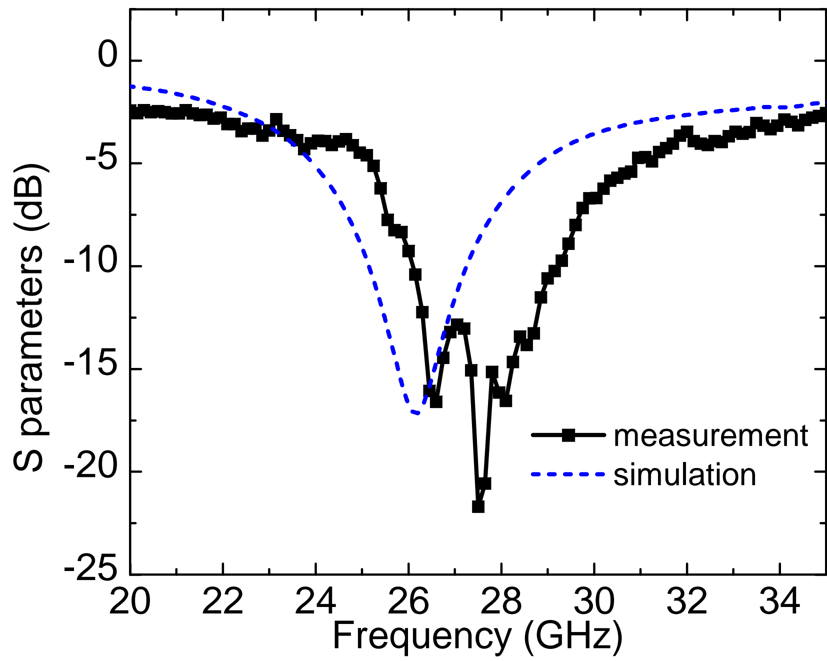


Figure 3.5: Return loss measurement result for one elevated patch sample, together with simulation result.

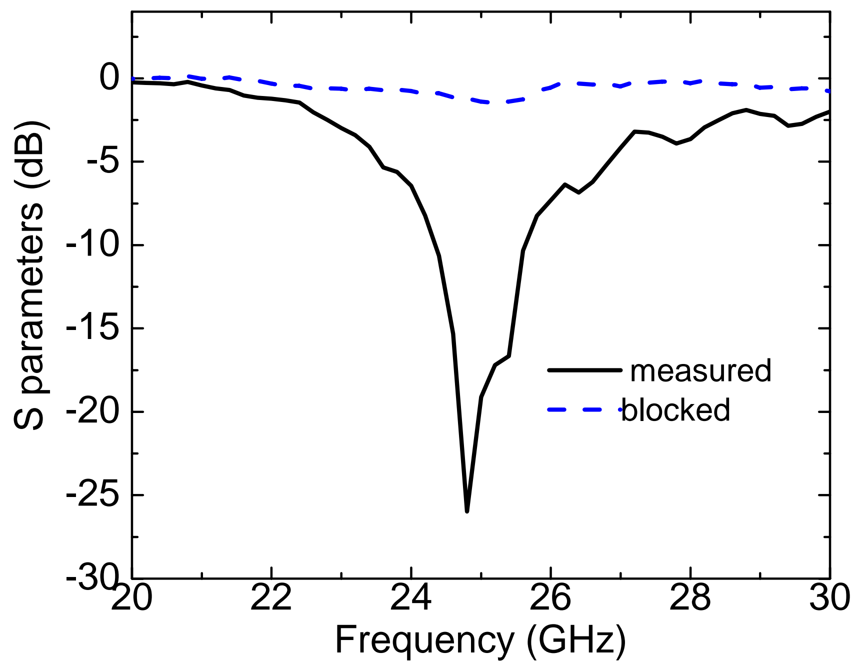


Figure 3.6: Return loss measurement result for another elevated patch sample, together with measured return loss when radiation is blocked by metal.

simulation results in Figure 3.5. A fraction bandwidth of 10.5 % (10-dB bandwidth) is observed in the measurements (26.2 GHz to 29.1 GHz). This bandwidth is slightly higher than the simulated one, which is 9.6%. This is believed to come from various losses that is hard to be accurately modeled in numerical simulations; these losses will pull down the reflection coefficient curve in measurement. The central frequency is shifted up by 2 % from 27.2 GHz to 27.7 GHz, which can be attributed to accumulated fabrication dimension variations and tolerances.

More specifically, the metal patch piece is made by laser-cutting and there is dimension variation from piece to piece. Figure 3.6 shows the measured return loss of another sample using different metal patches. As can be seen, the center frequency shifts to 25 GHz.

To further proof existence of radiation, metal housing is used to cover the whole structure and measured return loss shows a clear reflection to the input port and indicates radiation blockage. It is also plotted in Figure 3.6.

As a comparison, the traditional patch antenna directly printed on top of this kind of soda-lime glass (600 micron thick, ϵ_r=8.1) gives a narrower fractional bandwidth of 2.6% according to simulations. Its efficiency is low because of the lossy substrate.

The radiation pattern is characterized with an on-wafer radiation pattern probing system that has been modified from the original system [68]. In the new system, the microwave probe station is replaced by a plexiglass pedestal that holds a microwave probe head and a 3.8 cm thick Styrofoam cantilever upon which the antenna sets. Furthermore, a modified GGB Industries Picoprobe with a microcoax length of 2.54 cm is used to reduce the interaction of the probe head with the antenna under test. With this new on-wafer radiation pattern measurement system, the only metal structure near the antenna is the probe head, which after being covered by a piece of absorber, results in smooth radiation plots. However, even this small structure prevents the E-plane radiation pattern across the full 180 degree sweep. During the test, the elevated microstrip antenna is the transmitting antenna and a Ka-Band, 15 dB gain horn is used as the receiving antenna with a separation of 27 cm between them. Before measurements, the diode power detector is calibrated and all measurements are corrected by this calibration factor and the gain factor of the standard

Table 3.2: Performance comparison for antennas with and without elevation.

	Max directivity	E-plane 3-dB beamwidth (degree)	H-plane 3-dB beamwidth (degree)	fractional bandwidth
Elevated patch	9.5	75	90	9.6%
No elevation	4.9	N/A	N/A	2.6%

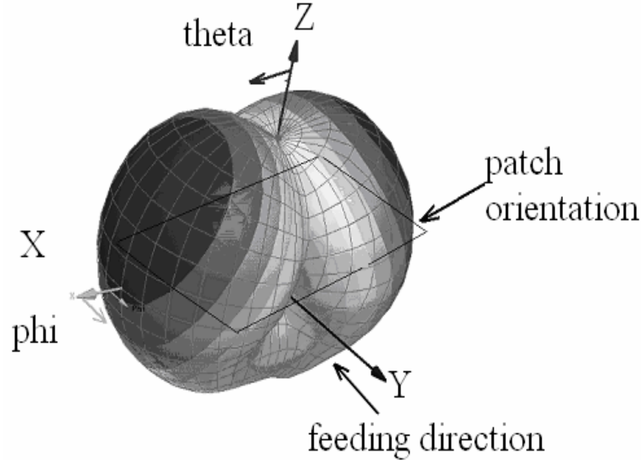


Figure 3.7: Radiation pattern of a patch antenna directly printed on the same substrate.

gain horn used during calibration. The proposed antenna has demonstrated a significantly improved radiation performance than the traditional patch antenna directly printed on top of the same type of soda-lime glass. The comparison is shown in Table 3.2. The maximum predicted directivity for the elevated patch is 9.5 dBi and the antenna efficiency is 94%.

A non-elevated patch on the same substrate gives a maximum predicted directivity of 4.9 dBi, but no longer at the broadside direction as a consequence of surface wave triggered in this electrically thick, high-ϵ_r substrate. (As in Figure 3.7) It can be clearly observed from Figure 3.7 that there is a deep drop in the z-direction for the antenna without elevation due to the diffraction of surface waves at the edge of the substrate. Elevated patch have a clear main beam in the z-direction. The E-plane and H-plane patterns at the measured central frequency of 27.7 GHz are plotted in Figure 3.8 and Figure 3.9 respectively. The simulation results predicted by Zeland IE3D and Ansoft HFSS are plotted in the same figure for comparing. They agree very well with each other.

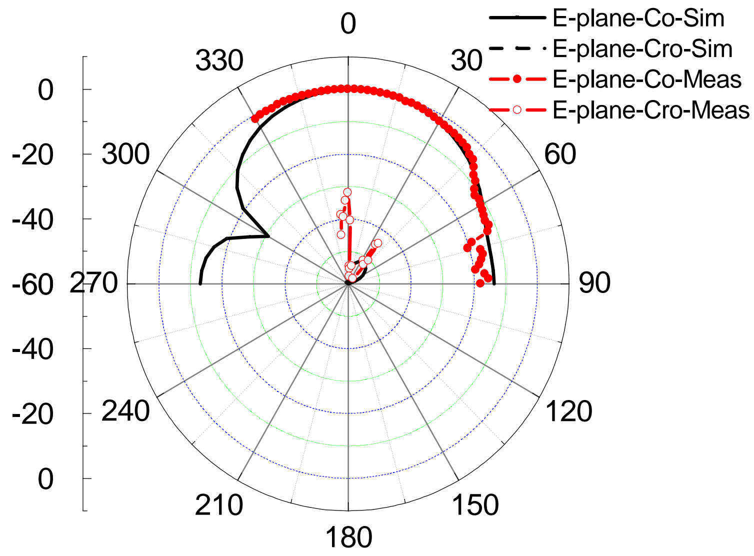


Figure 3.8: Simulated and measured radiation pattern on the E-plane.

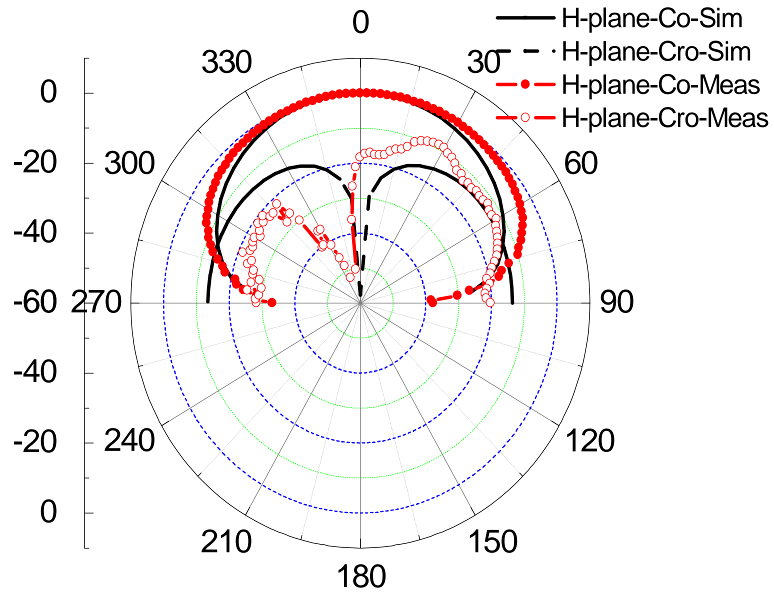


Figure 3.9: Simulated and measured radiation pattern on the H-plane.

For the E-plane co-polarization field, simulations predict a null in the direction of the feeding CPW-probe transition; this effect is believed to be a consequence of the electromagnetic field perturbation due to the existence of the transition. There is no such phenomenon for traditional probe-fed patch antenna since the ground is continuous and does not have a CPW slot cut. The maximum simulated and measured E-plane cross-polarization levels are -52 dB and -31 dB respectively. For H-plane, these values are -13.5 dB and -8.8 dB. E-plane cross-polarization level is lower than H-plane because the mode that generates the cross-polarization level is mainly the TE_{02} [31], which is also why the H-plane cross-polarization field yields a null at the broadside direction. Notice that a clear null is observed for the H-plane cross polarization at θ=0 in simulation and the same null shifts slightly to -10 degrees in measurements. A possible reason for the higher level of the cross-polarization level on the right side of the measured diagram could be that the prototype probe is not exactly on the middle line of the patch due to the assembly process.

3.4 Discussion

Parametric analysis for various geometrical parameters has been performed and among these parameters, the current probe radius plays a very important role. Since the probe is implemented using the polymer-core conductor, it does not have to use the standardized center pin diameter of the traditional coaxial connector. Its diameter can be optimized to get optimal performance.

In this design, the reference plane to calculate the input impedance of the proposed structure is set right before the CPW-fed probe transition, thus the imaginary part of the Z_{in} comes from the antenna itself, as well as the feeding probe, that can be modeled as a series inductor in the equivalent circuit. Various values of the diameter of the probe have been simulated and compared using Ansoft HFSS. Figure 3.10 shows the S-parameters locus when the other geometric parameters are as specified in Table 3.1. When increasing the probe diameter from 100 μm to 300 μm, wire inductance associated with the probe decreases. Thus for Z_{in}, the slope of the reactance becomes less steep, as in Figure 3.11. Consequently, more frequency points will fall within the $SWR = 2$ circle and more bandwidth can be

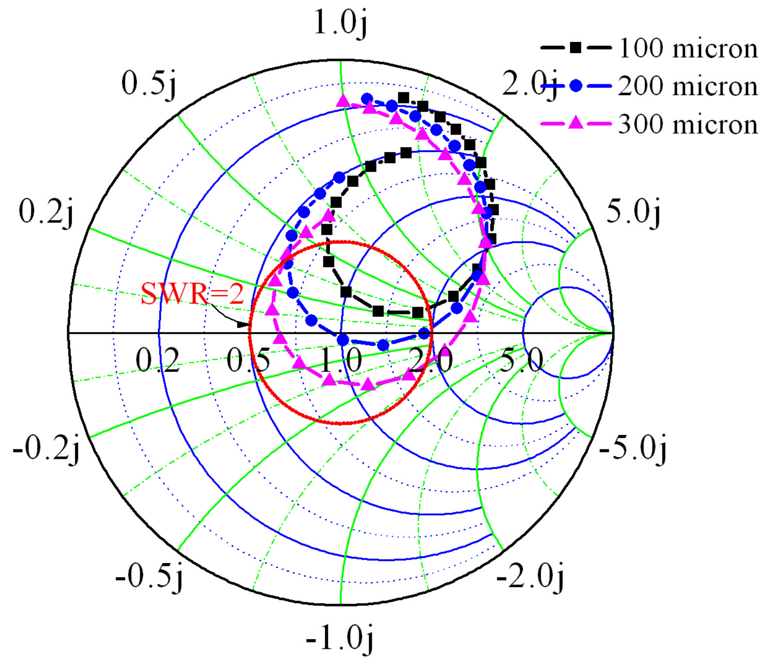


Figure 3.10: Input matching contours for different probe radius.

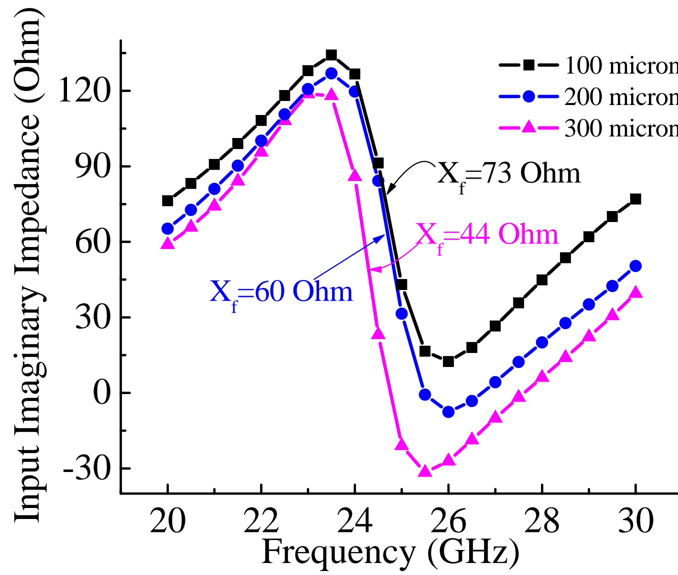


Figure 3.11: The imaginary part of the input impedance versus probe radius.

achieved. On the other hand, increasing the probe diameter will enlarge the probe pad and thus the perimeter of the circular slot around the probe pad; at the same time, the CPW line signal/slot widths also need to be increased to achieve smooth impedance transition to the probe. This introduces more ground opening and disturbs the radiation pattern. Because of this finding, 200 μm probe diameter is chosen to balance the bandwidth, compactness, and radiation pattern. Similar as other classical probe-fed antennas, the probe location was chosen as 1 mm away from the patch front edge to make the real part of the input impedance close to 50 Ω.

Simulated data for the geometries with and without epoxy (ϵ_r=4) posts demonstrate no significant difference in terms of bandwidth, radiation pattern and electrical/magnetic field distribution, as it is evident from Figure 3.12 that shows the surface current distribution on the patch. A large number of posts would offer a more rigid mechanical performance at the expense of an increased dielectric loading of the patch, and thus of a higher dielectric loss. In this design, the smallest possible number of posts, while maintaining mechanical robustness, is decided as eight; one polymer supporting post is used for each patch vertex and one for each middle point of the patch edge. Since the current probe is very close to the front edge, the one at that edge has been removed. One polymer post is also placed in the center of patch. These eight polymer posts account for 0.8% of the cavity volume underneath the patch. Thus, the loss and the dielectric loading of the supporting posts only play a minor role and can be omitted. Mechanical analysis was also performed to evaluate the mechanical properties of the proposed geometry. Simulation results by the FEM-based mechanical simulation tool ABAQUS(TM) indicate that the structure is both mechanically and electrically robust under vertical pressure, but fragile to shear stress. Thus operation under the latter circumstance should be avoided.

3.5 Chapter summary

In this chapter, we presented an elevated patch antenna that is fabricated using thick-film surface micromachining technology. The antenna is completely elevated in the air. It is fed by a CPW-connected probe. It demonstrates broader bandwidth and increased radiation

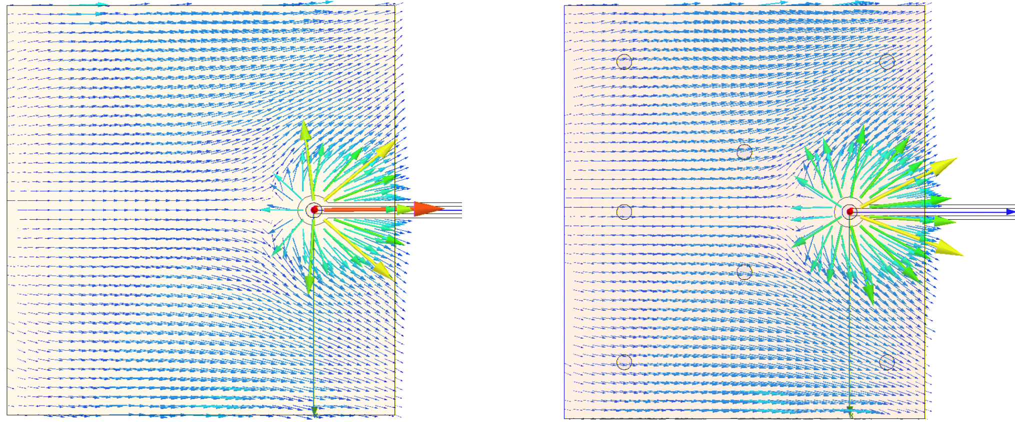


Figure 3.12: Surface current distribution on an elevated patch with and without polymer supporting posts underneath.

efficiency compared with its planar counterpart on the same substrate.

CHAPTER IV

A MICROMACHINED HORN ANTENNAS

This chapter presents an integrated horn antenna with a very simple feeding scheme for 60 GHz applications. This H-plane horn is elevated over the top of the substrate. It is excited using an integrated vertical current probe connected with a coplanar-waveguide (CPW) using surface micromachining technologies. The lower part of the horn is rows of metallized pillars. The upper part and the top wall is built by stacking two layers of micromachined silicon wafers. The horn bottom is the ground metal on the substrate's top surface. A prototype antenna is designed, fabricated and characterized. Simulation and measurement results have shown wide input matching and radiation bandwidth. A 14.6 dBi gain is projected by multiple full-wave simulators and a 14.4 dBi gain is measured.

4.1 Background

With the ever-increasing demand for high performance, low cost, low-power wireless communication systems in the millimeter wave regime, such as Wireless Personal Area Network (WPAN) applications, the need for integrating all function modules (digital, RF, optical, etc) on a single chip or into a single package becomes more pronounced [70]. The simplest way to integrate a millimeter-wave antenna is to use a microstrip wire/patch. However, a microstrip antenna poses the opposite substrate requirements with respect to the rest of substrate requirements (such as ϵ_r and thickness) other than the rest of the integrated functions and circuits since it prefers low-ϵ_r, thick substrates to suppress the substrate modes (higher efficiency), achieve a wider bandwidth, undisturbed radiation patterns, and reduced undesired coupling between the various elements in array configurations.This is not compatible with the rest of the RF components/passives that need high-ϵ_r and thin materials for the sake of compactness and thermal dissipation.

To overcome these limitations, integrated horns were introduced in [20] and have caught extensive interest because of their high gain, high efficiency and wide bandwidth. Several

millimeter-wave and sub-millimeter-wave receivers that integrate mixers with horn antennas have been reported and shown superior performances [10]-[17], where a couple of silicon wafers are wet-etched along a certain crystal orientation and stacked to form the horn flare. In most cases, the horn axis is aligned perpendicular to the substrate surface. The number of layers needed for a good gain is still practical for THz and sub-millimeter wave for the broadside radiation [32], [28]. It is not feasible though for lower frequencies since a significant number of silicon pieces have to be used with different opening for different layers to generate a stepped tapering profile. Integrated horns designed for end-fire radiation were also reported, as the ones in [67] and [28]. Fewer layers are needed for this configuration. This reduces fabrication cost and is adopted in this paper.

However, another important issue with all these designs is their relatively complicated feeding schemes. A microstrip probe, a dipole or a slot ring can be used to excite the horn [20]-[18]. However, almost all these excitation structures need to be fabricated separately on another substrate (silicon, quartz or a thin film dielectric substrate) and inserted into an individual microstrip channel. This complicates the fabrication and assembly steps, thus increases the fabrication cost.

In our research, a CPW-connected vertical probe is used to excite an integrated waveguide which tapers linearly to a horn antenna. The lower part of the sidewall consists rows of metalized pillars. The upper part and the top wall is built by stacking two layers of micromachined silicon wafers. The horn bottom is formed by metalizing the substrate's top surface. The horn axis is along the surface's tangential direction. Although an E-plane flare is also achievable by using multiple stepped wafers, the fabricated horn is flared only in the H-plane for simplicity.

Several advantages are claimed for the proposed horn structure, including a simple integrated feeding structure, a CMOS-compatible monolithic integration scheme, and wide bandwidth.

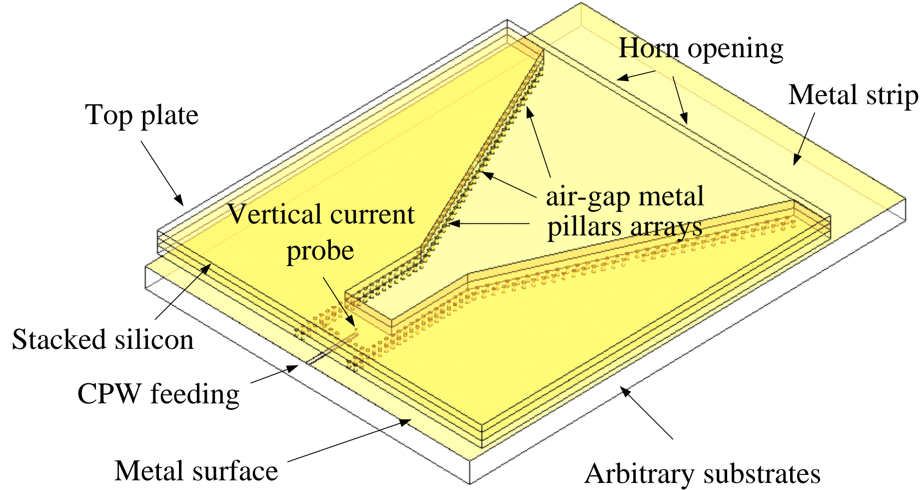


Figure 4.1: 3-D view of the proposed micromachined horn.

4.2 Design and optimization

4.2.1 Design of the feeding and transition

Figure 8.12 shows the proposed horn structure. It starts from a coplanar-to-rectangular waveguide transition. After the waveguide mode is established, the waveguide tapers out in the H-plane to form the horn. The transition reported in [46] can be used to excite the waveguide in a non-contact way. However, it needs to extend approximately halfway into the waveguide to fully excite the required TE_{10} propagation mode. For a standard WR-15 waveguide whose height is 1.88 mm and operating at 60 GHz, the total length of the whole probe will be larger than 1 mm, taking into account the transition length. This is not quite feasible in our fabrication by using SU-8. Besides, a separate silicon piece as the transition layer would have to be etched to form a quasi-coaxial structure (as was used in [46]), using an additional mask. This would result in a significantly higher fabrication cost.

A novel and simple feeding scheme for the 60 GHz horn is developed in our research. Figure 8.13 depicts the proposed feeding scheme. Figure 4.3 shows the top and side view of the horn. A current probe with a height of 350 μm, along with 350 μm high pillar sidewalls are fabricated using SU-8 surface micromachining technologies on top of the substrate. Cores of pillars are formed through patterning a thick photo-definable polymer SU-8, and then plating their outer surface up to several microns. Although it is possible to directly

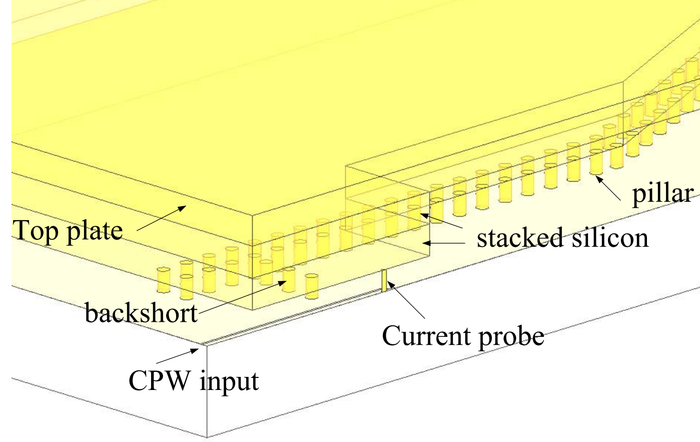


Figure 4.2: The close-up schematic for the feeding structure (splitted along the symmetry plane).

pattern solid walls, pillar fences are used instead due to the fabrication feasibility concern, which has been discussed in [56]. The lower part of the waveguide/horn cavity is formed in this way. Two identical pieces of 525 μm-thick micromachined silicon wafers are etched through to form the upper hollow part of the horn. These two pieces have a recession for backshort different with the one formed by pillar arrays (in other words, $d_2 > 0$ in Fig. 4.3; otherwise, there is no contact between the probe and the silicon layer). As can be seen from the cross-section view in Figures 8.13& 4.3, a step profile is formed. The top plate is lowered in the transition region to contact the current probe and comes back to its regular height for the waveguide and horn to achieve a high gain operation. The length of the backshort (d_1 in Figure 4.3)and the distance from the current probe to the step edge (d_2 in Figure 4.3) are critical for impedance matching.

4.2.2 Design of the horn

After TE_{10} mode is established in the waveguide, the waveguide flares out in the H-plane to increase the effective radiation aperture, and thus gain. A narrow beamwidth in the H-plane is expected. Flaring-out in the E-plane is also possible using more stepped silicon pieces to further increase the gain and narrow down the E-plane beam. Another possible solution to reduce the E-plane beamwidth is to use a tapering slot on the top plate [17]. These techniques increase the fabrication complexity and are not considered in our research.

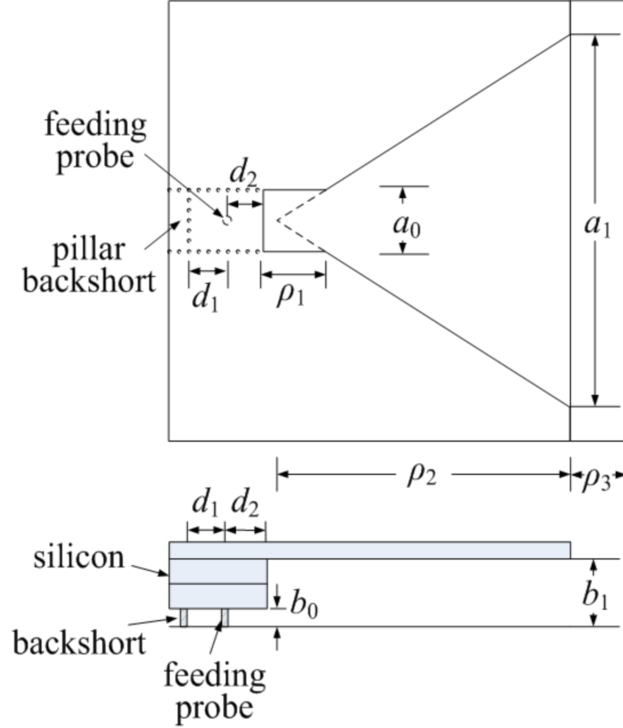


Figure 4.3: Illustration of horn dimensions (top and side views).

A linear flaring is used and the dimensions of the horn are found, following the guidelines provided in [7] to maximize the gain. Table 4.1 summarizes the horn's physical dimensions, while their physical meanings are shown in Figure 4.3. A solid wall version is designed first to save full-wave simulation time. After the horn performance is optimized, the lower part of the sidewall is replaced with rows of pillars using the following equations [15]:

$$a_{eff} = a - d^2/0.95b \tag{4.1}$$

Where a_{eff} is the width of the equivalent solid-wall waveguide that has the same characteristic impedance and a is the measured center to center distance between the two inner rows of pillars. d is the diameter of the pillar and b is the pitch between two adjacent pillars. d and b were chosen to minimize the EM-wave leakage while meeting the fabrication constrains [15].

Further adjustments are made with the aid of the full wave simulator.

Return loss larger than 10 dB is observed to cover the 56-63 GHz frequency band (Fig.

Table 4.1: Optimized horn dimensions with transition(Units: mm).

Dimensions	Value	Dimensions	Value	Dimensions	Value
a_0	3.7	a_1	20.0	d_1	1.0
b_0	0.35	b_1	1.4	d_2	0.9
ρ_1	6.1	ρ_2	18.0	ρ_3	6.0

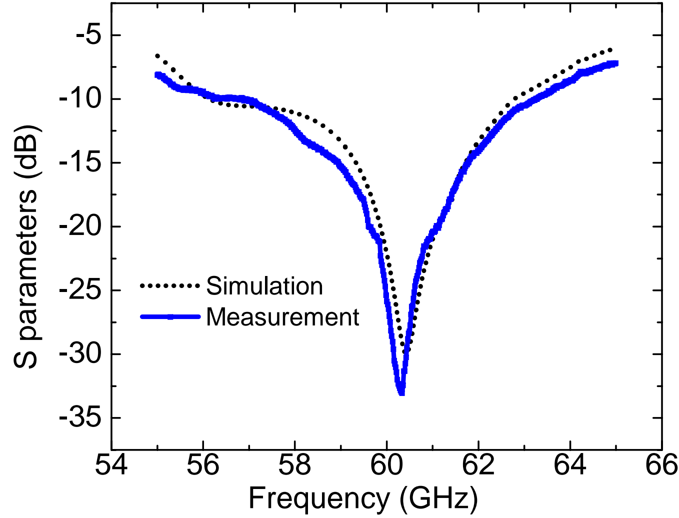


Figure 4.4: Simulated and measured return loss of the proposed horn.

4.4). It can cover the whole V-band from 50 to 75 GHz if more steps for the top plate are used.

A 14.6 dB gain is projected by multiple full wave simulation tools including Ansoft HFSS and Flomerics Microstripes. The main radiation beam is tilted to the upper space due to the 6 mm metal strip. Simulation finds the maximal beam is pointed to $\theta = 60°$ direction. To better describe the radiation beamwidth, a tilted H-plane is defined as shown in Figure 4.5 since a regular H-plane is less meaningful when the radiation beam is tilted. 3-dB beamwidth on E-plane and this tilted H-plane is $44°(38°\sim82°)$and $20°(-10°\sim10°)$ respectively. Beamwidth on the tilted H-plane is obviously narrower than the one on E-plane since this is a H-plane horn.

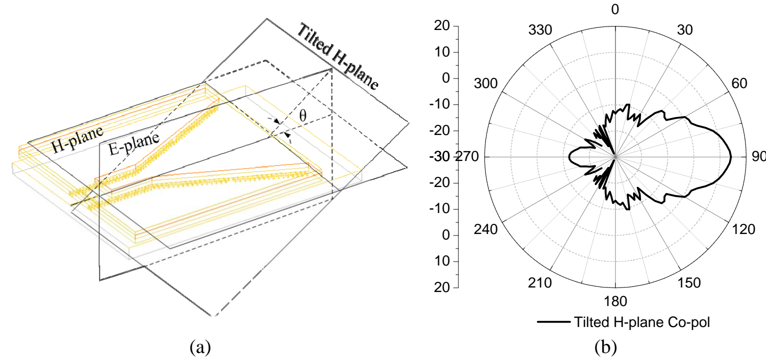


Figure 4.5: Simulated radiation pattern on E- and tilted H- planes.

4.3 Fabrication and measurement

As for the fabrication process steps for SU-8 layer [80][56]: a thin Ti layer was sputtered to improve the SU-8's adhesion to the glass. A negative photo-definable epoxy SU-8 2035 350 μm thick was dispensed and patterned to define the cores of the pillar fences. Ti/Cu/Ti was then sputtered as the seed layer to cover the pillars, as well as the substrate in a conformal manner. Negative photo-resist NR9-8000 was coated and patterned in a non-contact way to cover the CPW slot region, preventing the metal coverage on the slot in the following electroplating step. Electroplating of copper and gold covers the sidewall of the pillars and the exposed feeding structures.

The fabrication of micromachined silicon pieces starts from the cleaning process. A silicon dioxide layer with 0.5 μm thickness is deposited on the silicon wafer using Unaxis PECVD as a stop layer. Then, the silicon wafer is flipped over and the photoresist (PR), SRP 220 is spun on it. After the soft baking, the wafer is patterned using MA6 mask aligner and etched through using STS ICP with DRIE process until the stop layer. Once the PR remnants and the stop layer are removed, the metals, Ti/Cu/Au, with the thickness of 20 nm/3 μm/20 nm are sputtered on the silicon sample using DC Sputter.

The assembly flow to further illustrate how this horn antenna is built is shown in Figure 4.7. Alignment between different layers is achieved with the aid of an acrylic fixture. Figure 4.8 shows picture before and after the acrylic fixture cover is closed.

The fabricated sample on a glass substrate is measured by an Agilent 8510XF vector

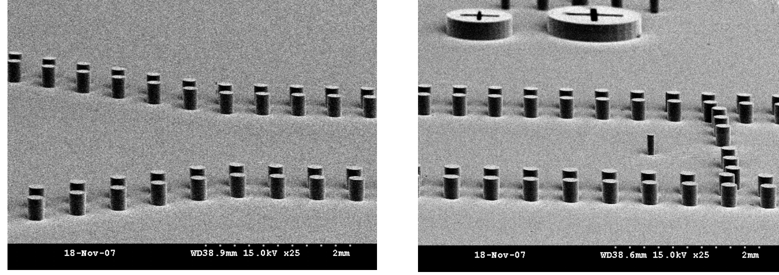


Figure 4.6: (SEM pictures for the micromachined horn showing the feeding probe and the horn flare pillar sidewall.

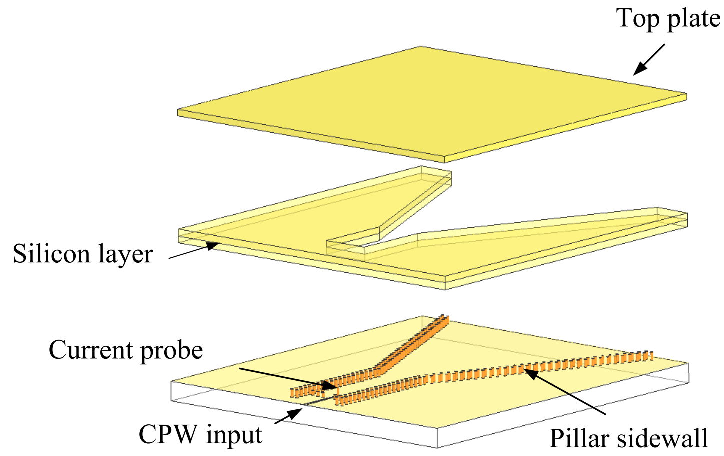


Figure 4.7: The assembly scheme for the horn structure layer by layer.

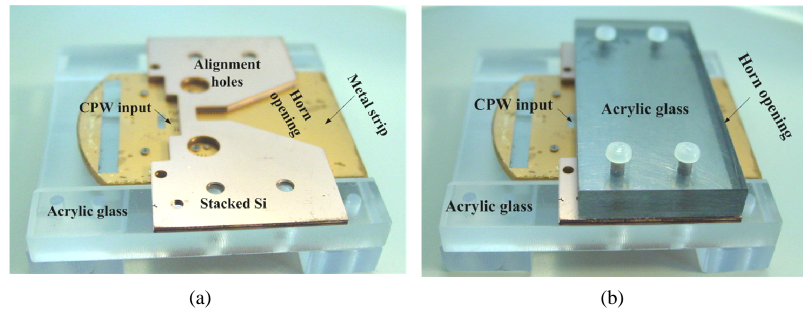


Figure 4.8: Pictures of the horn antenna assembly.

network analyzer station connected with GSG probes of a 250 μm pitch. The system is calibrated with WinCal SOLT scheme between 55 GHz and 65 GHz .The reference plane is set to the probe tips. The measurement results are plotted in Fig. 4.4 (along with the HFSS full-wave simulation result). Good agreement between simulation and measurement is observed. Larger than 10 dB return loss was observed from 56.9 GHz to 63.2 GHz. The discrepancy is within fabrication tolerance. It might also be attributed to misalignment between metalized SU-8 pillars and silicon pieces. A 100 μm misalignment between pillars and silicon pieces was found. This can be corrected by using a micromachined alignment piece in the future.

Pattern measurement is taken using an on-wafer pattern measurement setup in the NASA Glenn research center. Figure 4.9 shows a picture of the on-wafer pattern measurement to characterize this antenna. The measured E-plane co-polarization gain pattern, E-plane cross-polarization gain pattern, and the simulated E-plane co-polarization gain pattern, are plotted together in Figure 4.10. Agreement is great except null depth and backside diffraction. This is expected due to the existence of the metal probe head and bulky millimeter-wave mixer module. The measured gain is 14.4 dBi and slightly lower than the simulated 14.6 dBi. Simulated and measured H-plane gain patterns are separately plotted in Figure 4.11 (a) and (b) for clarity. Since the main radiation beam is tilted to the upper space, H-plane radiation patterns are less informative than the E-plane pattern. Still, agreement between simulation and measurement is great and a narrower beam width can be observed on the H-plane.

4.4 Chapter summary

In this chapter, a novel approach to integrate high performance millimeter-wave horn antennas using micromachining technologies is presented. By combining thick-film surface micromachining and silicon bulk micromachining technologies, a CPW-fed air-filled horn antenna is developed and characterized for 60 GHz applications. A wide bandwidth and a measured high gain of 14.4 dBi is observed in simulations and measurements. The proposed method also offers an easy integration platform of both planar components and 3-D

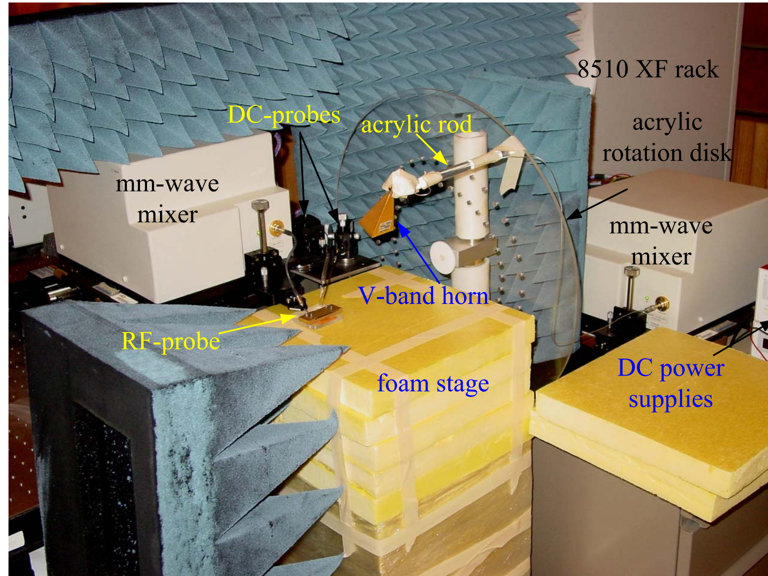


Figure 4.9: On-wafer pattern measurement setup.

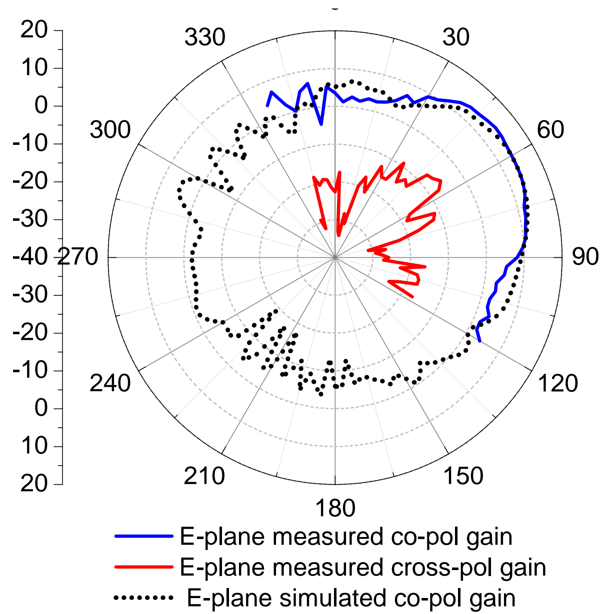


Figure 4.10: Simulated and measured E-plane gain patterns

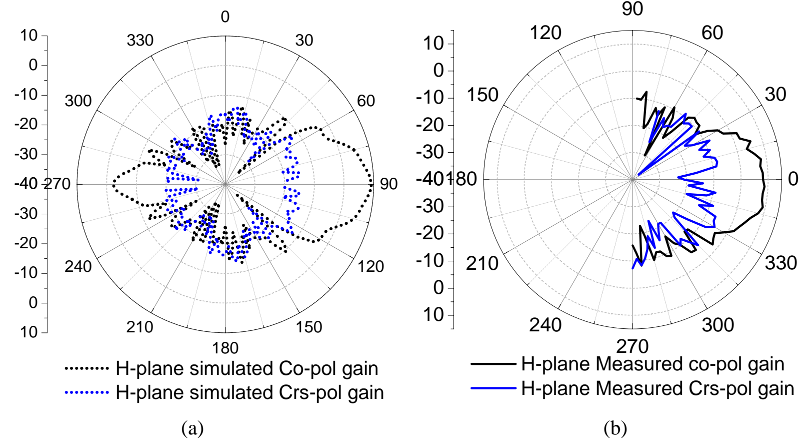


Figure 4.11: (a) Simulated and (b) measured H-plane gain patterns.

integrated modules on top of the substrate.

CHAPTER V

A BROADBAND ELEVATED MICROSTRIP COUPLER

A broadband elevated microstrip coupler has been designed and implemented on a soda-lime glass substrate using surface micromachining technology. The coupler is elevated by 200 μm and fed by CPW-connected vertical probes. This scheme helps eliminate the conventional air/dielectric interface problems. By using this method, frequency dispersion and attenuation due to the substrate can be effectively reduced. A return loss of 10 dB and a coupling of 12.5 dB is measured in our experiment over 15-45 GHz. The proposed structure can be implemented on very lossy substrates, such as doped silicon in a standard CMOS technology and thus can be applied into the integration of high performance RF components with digital or optical functions/subsystems on low-cost low-resistivity silicon wafers.

5.1 Background

Considering fabricating a microstrip directional coupler on lossy substrates such as a standard CMOS substrate, the loss of the substrate and the non-TEM nature of the propagating wave along the air/dielectric interface sets limitations to the coupler performance in several aspects. The coupling bandwidth and the isolation are limited by the different mode phase velocities caused by the air/dielectric interface.

Figure 5.1 shows how different air/dielectric interfaces affect the frequency dispersion for even/odd mode transmission. The ratio of even-mode wavelength to odd-mode wavelength among air (ϵ_r=1), LCP (ϵ_r=3.1), LTCC (ϵ_r=5.4) and silicon (ϵ_r=11.9) substrates is compared in this figure. Apparently, there is no frequency dispersion for air filling, which is exactly our investigated structure.

Most important of all, high substrate loss will severely degrade coupler performance. Various methods have been investigated to improve the performance by compensating non-TEM mode transmission and eliminating substrate losses. A multi-layer overlapped structure in [34] was designed to compensate non-TEM mode transmission, but substrate loss

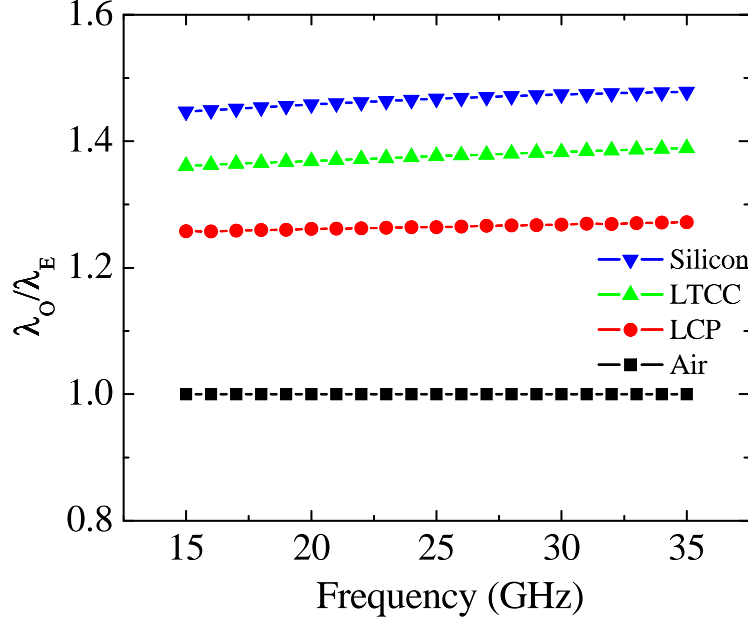


Figure 5.1: Comparison of dispersion properties of different substrates for a microstrip coupler.

is a drawback since the line is embedded in the substrate. A coplanar waveguide coupler can be used [74] to get near-identical dielectric loading for both even and odd modes, and thus have less severe frequency dispersion. However, it still can not completely eliminate the substrate loss. Other technologies include the deposition of low-loss thin-film polyimide on top of the silicon substrate [60][61] to decrease the loss associated with the substrate.

In our research, the polymer-core conductor approach is used to diminish both substrate loss and non-TEM mode wave propogation. The coupler is elevated to a height of several hundred microns by supporting posts. The structure is fed using a vertical polymer-core conductor probe that is connected with coplanar waveguide on the top surface of the lossy substrate. The substrate is, thus, covered by a ground metal on top. Electromagnetic field of the coupler itself will not leak into the lossy substrate. The elimination of the dielectric/air interface helps reduce the mode dispersion and associated problems such as poor isolation. A thick metal electroplating scheme for the elevated microstrip line is used to enhance coupling by introducing vertical coupling from the side walls.

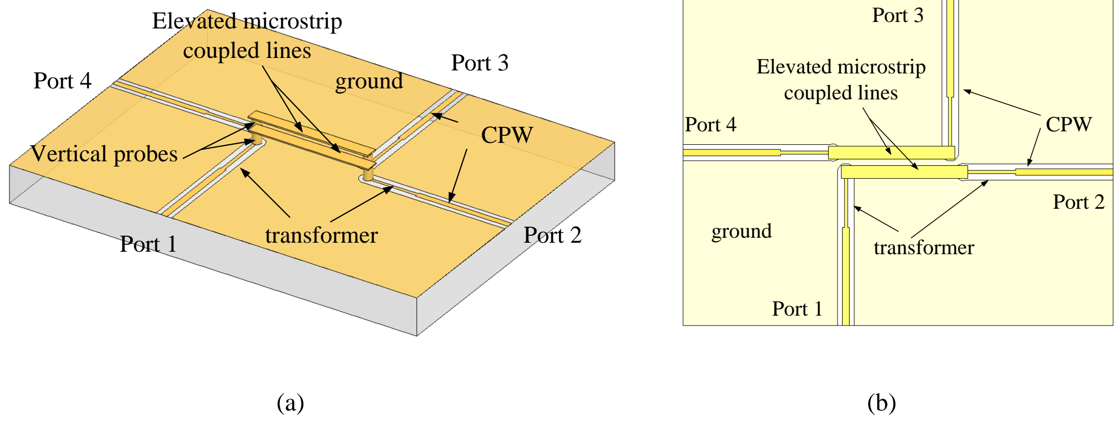


Figure 5.2: Schematic of a micromachined elevated microstrip coupler (a)3-D view (b)top view.

5.2 Elevated coupler design

In our work, a microstrip directional coupler prototype with an elevation of 200 μm is fabricated on a soda-lime glass that has an ϵ_r of 8.1.

The configuration of the proposed elevated microstrip coupler is shown in Figure 9.2. The elevated microstrip line is supported and fed at the end by metal-coated epoxy core probes that we have discussed in previous sections.

The metal probe is directly connected with a quarter wavelength CPW impedance transformer to convert input impedance of the coupler to standard 50 Ω at the input ports.

The feeding CPW lines and the coupler share the ground plane in a simple and natural way which makes air the only dielectric between the coupler and the ground plane. This helps eliminate substrate loss, as well as frequency dispersion caused by the air/dielectric interface.

There are several variables that need optimization in the coupler design:

- w- the width of the elevated microstrip line
- s-the gap between the two lines
- H- the height of the elevation
- T- the metal thickness of the coupler

The following equations guide the optimization of w and s:

C_e=C_{11}=C_{22}, C_o=C_{11}+2C_{12}=C_{22}+2C_{12}

Z_e=1/$v_e C_e$, Z_o=1/$v_o C_o$

$c = \frac{Z_e - Z_o}{Z_e + Z_o}$

where C_e (also C_{11},C_{22}) is the even-mode capacitance which is determined mainly by the separation from the ground, C_o is the odd- mode line capacitance which is determined by both the separation from the ground and the gap between the two lines. v_e is the even-mode wave propagation velocity and v_o is the odd-mode velocity. c is the mid-band voltage coupling coefficient.

Here, since there is no air/dieletric interface, the even-mode and odd-mode velocities are same. Otherwise,frequency dispersion results in two different propagation velocities for even-mode and odd-mode. The frequency-dependent even- and odd-mode voltage distribution along the line shows faster variation than the one without frequency dispersion. Even- and odd-mode voltage cancellation at the isolation port is more frequency-dependent and leads to a narrower band coupling and reduced directivity.

Furthermore, the w and s will affect Z_o and Z_e. As a simple rule, the narrower the lines, the higher Z_e, the smaller the gap, the lower Z_o can be achieved. Also, if the coupler is terminated with an impedance of Z_0=$\sqrt{Z_o Z_e}$, the input impedance will also be

Z_{in}=Z_0

In our design, a width of 200 μm and a gap of 100 μm lead to a Z_e of 150 Ω and Z_o of 75 Ω, and we need a Z_0 of 108 Ω. It is true that a wider line w and a narrower gap s can achieve lower input impedance. However, a tradeoff should be made to try to avoid infeasible gap values or line widths. Large line widths introduce more parasitic radiation from the edge of the line. Narrow line gaps are hard to implement in our fabrication. Another important design parameter is thickness elevated microstrip line. As simulated results show in Figure 5.3, the thicker the metal, the stronger the coupling we can achieve. A thicker metal makes vertical wall coupling stronger (the vertical walls functions as a parallel-plate capacitor). A thicker metal also results in a slight reduced attenuation as shown in Figure 5.3.

The final variable is the height of the elevation. As can be observed from Figure 5.4, a

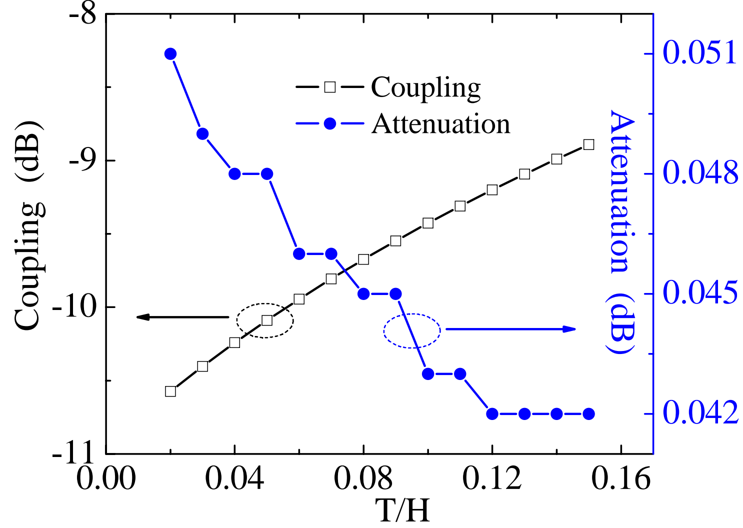


Figure 5.3: Attenuation and coupling versus metal thickness.

Table 5.1: Dimensions of the optimized elevated coupler.

	w	s	T	H
value (μm)	200	100	10	200

low elevation leads to higher odd mode impedance and loose coupling because the electrical field is more constrained between elevated lines and the ground. On the contrary, a high elevation results in lower odd mode impedance and tight coupling because more electrical field can be concentrated between lines.

On the other hand, the higher the structure, the higher parasitic radiation is generated. However, elevating the coupler to a height up to a few hundred microns does not introduce a significant radiation loss, while makes it possible to electroplate several tens of microns of microstrip line which is beneficial to the vertical coupling. Compared to the air-bridges used in MEMS switches, the use of a metal post makes it possible to vary the height of the structure from several tens of microns up to one millimeter. This introduces another design variable for optimization. The final optimized values of the coupler are summarized in Table 5.1.

The structure is simulated using the FEM-based Ansoft HFSS V9.1 software tool. The simulation results showing through, coupling, matching, and isolation performance of the

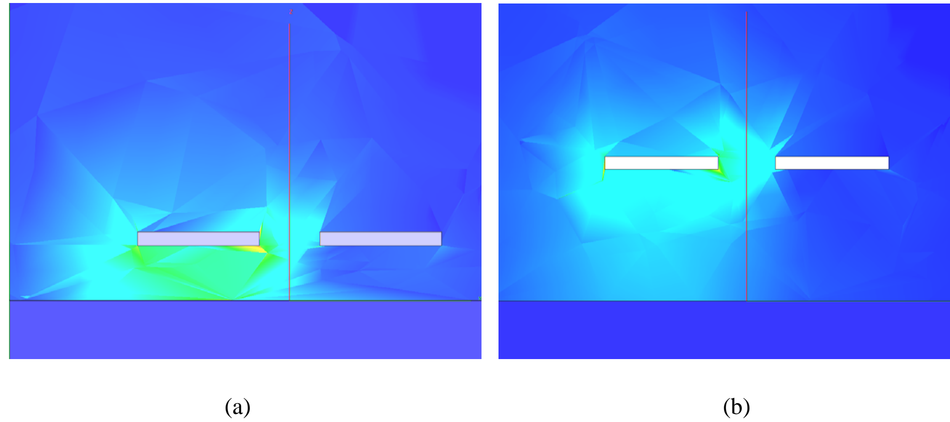


Figure 5.4: Elevation effects on field distribution of a pair of coupled lines on top of ground (a)low elevation (b) high elevation.

coupler are shown below.

From the simulation, a coupling of 11 dB, return loss larger than 10 dB for all ports and an isolation larger than w for the isolated port have been observed over 15- 45 GHz. The broadband nature resulted from elimination of the air/dielectric interface is well demonstrated.

5.3 Fabrication and measurement

As shown in Figure 5.6, fabricating the coupler uses the following steps: a) The coplanar waveguide (CPW) and the ground planes are patterned on top of the soda-lime glass substrate with ϵ_r of 8.1 by means of standard lift-off process using chromium and gold (Cr / Au; 30 nm / 1.5 μm). b) Photo-definable epoxy SU-8 (Microchem, Inc.) is spin-cast and patterned for the post definition to the desired height, by which the substrate coupling is minimized. In this coupler implementation, feeding posts have the height of 190 μm. c) Conformal seed layers of titanium and copper (Ti / Cu; 30 nm / 300 nm) have been deposited using a DC sputterer. Negative-tone photo resist NR9-8000 (Futurrex, Inc.) is spin-coated and lithographically patterned, letting copper selectively cover the posts with a thickness of 15 μm. d) A thick layer of sacrificial polymer (NR9-8000) has been used as a mechanical support for the lateral bridge patterning. e) Seed layers of Ti / Cu for the bridge pattering are deposited, followed by photoresist (NR9-8000) casting and patterning on it.

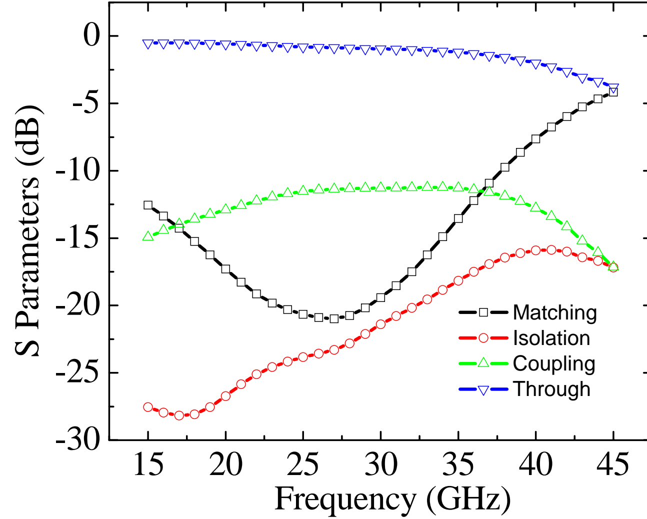


Figure 5.5: Simulated 4-port scatter parameters for the elevated coupler.

After copper electrodeposition with a thickness of 10 μm has been performed, removal of molding polymer, seed layers, and sacrificial layers follows to complete the process.

The fabricated prototype that is shown in Figure 5.7 was characterized by a 2-port Agilent 8510C vector network analyzer with a probe station. The NIST Multical TRL algorithm [48] was used to calibrate the measurement system. Five lines were used. The reference plane was set to the step discontinuity where the quarter wavelength transformer is connected with the input coplanar waveguide. During characterization, two of the four ports were terminated with RF probes integrated with broadband 50 Ω terminations.

As shown in Figure 5.8, the coupler demonstrates a very broadband measured coupling of 12.5 dB and a matching of 10 dB over 15-45 GHz. It also shows a through transmission of 0.015-1.85 dB over 15-45 GHz, which agrees well with the simulation. Multi-section transformer can be used in future to get better return loss performance. It is believed that the disparities between the simulated and measured matching and coupling are caused by the imperfection of the 50 Ω termination impedance as well as the parasitics associated with the probes that are connected with those termination impedances. The calibration was not performed on those unused ports.

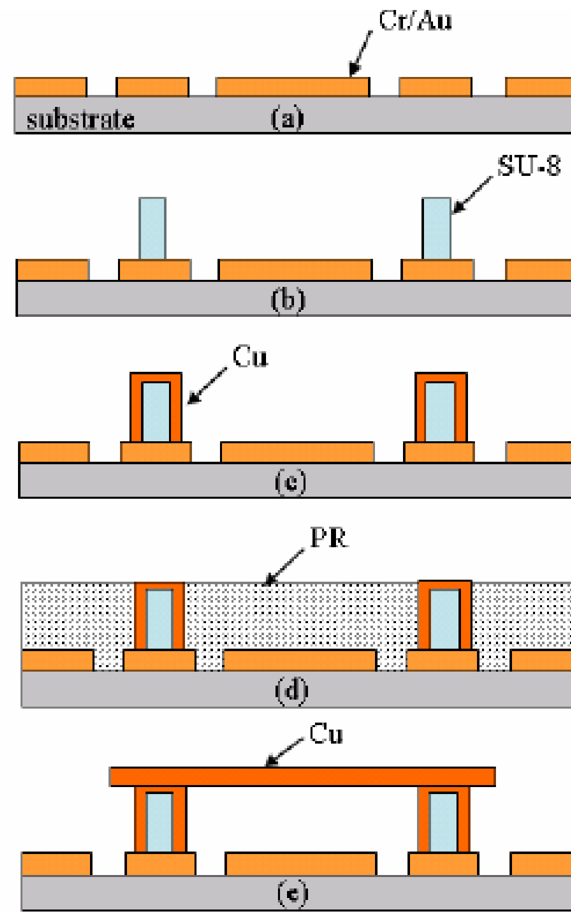
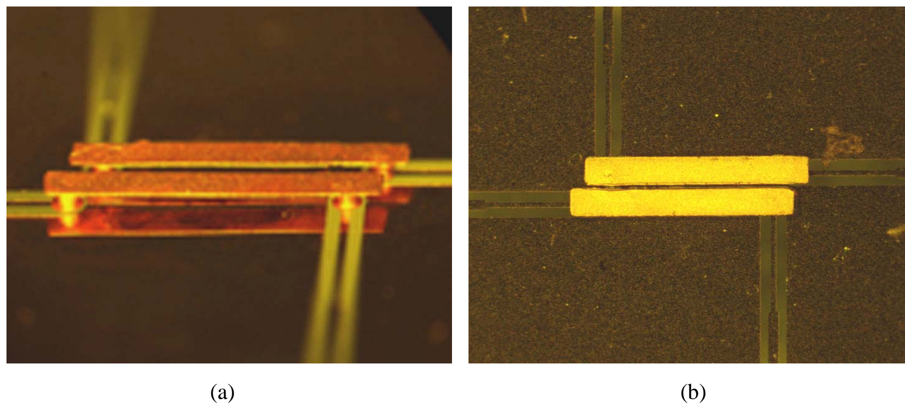


Figure 5.6: Process flow for the elevated coupler.



(a) (b)

Figure 5.7: Pictures of a fabricated coupler prototype (a)3-D view (b)top view.

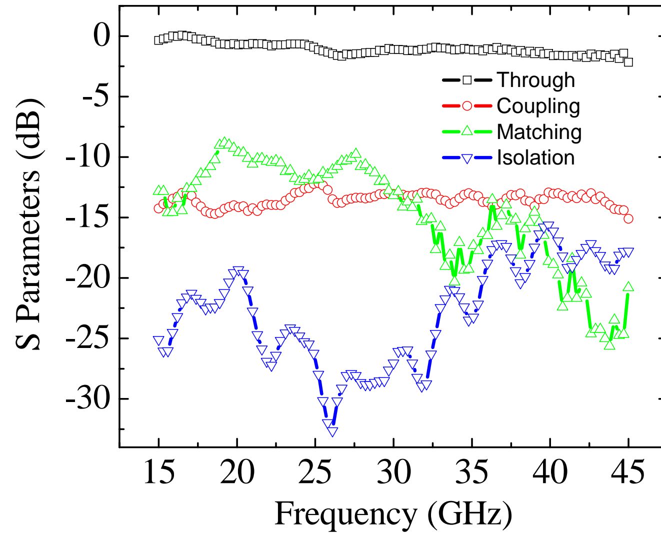


Figure 5.8: Measured 4-port scattering parameters for the elevated coupler.

5.4 Chapter summary

This chapter focused on the development of a low-loss broadband coupler using thick-film surface micromachining technologies. By elevating a microstrip coupler in air, broadband coupling and reduced attenuation can be achieved.

CHAPTER VI

MICROMACHINED CAVITY RESONATOR

6.1 Background

High-Q resonators are widely used in the design of high-selectivity filters and duplexers. However, the conventional resonators made in the form of metallic rectangular or cylindrical waveguides [12] are bulky and not allowing for an easy integration with the monolithic integrated circuits. At the other hand, high-Q planar resonators are also widely used due to their simplicity and the low fabrication cost [77], but usually requires high-ϵ_r and low-loss substrates. In the past several years, several 3-D high-Q cavity resonators have been implemented using either bulk micromachining technologies or standard PCB drilling processes ([58], [43] and [19]), offering the advantage of the simple integration with other components on the same substrate. However, these cavity resonators require a substrate that is low loss and easily micro-machined by either dry/wet etching or drilling, thus limiting its applications in certain substrates. The stereo-lithography method has also been explored and used to build waveguide structures [22]. It builds both the substrate and elevated parts layer by layer, using the same type of resin. This is a good technique to form stand-alone complicated structures. But selectively metalizing the surface of a 3-D structure requires laser ablation, posting a challenge.

In this chapter, a 30 GHz rectangular elevated cavity resonator was designed, fabricated and characterized on a very lossy soda-lime glass with the loss tangent of 0.06 at 10 GHz. It demonstrates a measured quality factor of at least 219 by utilizing the surface micromachining technology. (A CPW planar half-wave open-end stub resonator on this substrate gives a Q of about 23.2). Furthermore, this quality factor can be easily controlled by adjusting the height of the cavity from several micron up to 1 2 mm in the fabrication process.

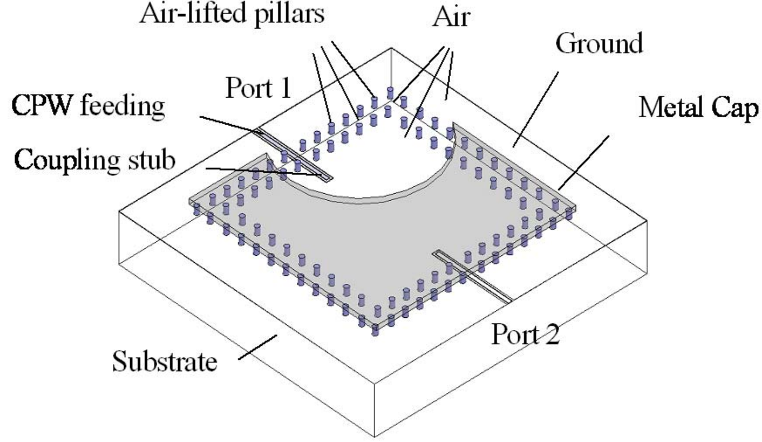


Figure 6.1: A micromachined cavity using surface micromachining technology.

6.2 Design and optmization

Figure 6.1 shows the proposed micromachined cavity resonator. The four side walls are composed of two rows of polymer-core conductor pillars with air gaps between them. The pillar fences instead of solid walls are used due to the fabrication feasibility concern, which is discussed later in this section. When the pitch between the pillars satisfy the rule given in [15], the pillar fence will block the outgoing electromagnetic waves inside the cavity and will act effectively as four solid metal walls [29]. These rules can be expressed mathematically using the following equations:

$$p > d \tag{6.1}$$

$$\frac{p}{\lambda_c} < 0.25 \tag{6.2}$$

$$\frac{\alpha_l}{k_0} < 10^{-4} \tag{6.3}$$

where p is the pitch between pillars, d is the pillar diameter,λ_c is the wavelength for an electromagnetic wave whose frequency is just equal to the cut-off frequency of a waveguide, k_0 is the free-space wave-number, and α_l is leakage loss. Equation 6.1 states the pitch must be larger than the diameter so that the waveguide is physically realizable. Equation 6.2is to avoid any bandgap in the operating bandwidth. Finally, Equation 6.3 is the condition when leakage loss can be neglected. Curves to read α_l/k_0 can be found in [15].

The bottom wall of the cavity is the metallization on top of the soda-lime glass substrate. This configuration offers two advantages: First, it allows for the easy integration of the resonator with other planar microwave components (CPW-fed components) located on the substrate surface; secondly, this metalized ground blocks most undesired substrate effects such as the dielectric loss and the frequency dispersion. In Figure 6.1, the top cover is partially removed purposely to reveal the side wall detail and the feeding scheme which is used to determine the resonator quality factor.

An open-end CPW stub is inserted into the air cavity through the gap between two adjacent pillars to excite the cavity. This feeding scheme is for the sole purpose of determining the quality factor of the cavity, as it introduces a weak coupling mechanism. In the filter application which is discussed later, a CPW-fed vertical probe can be used to contact the top wall of the cavity and introduce a strong coupling.

The equations to extract the unloaded quality factor are listed below:

$$Q_l = \frac{f_{res}}{\triangle f} \tag{6.4}$$

$$S_{21}(dB) = 20log_{10}(\frac{Q_l}{Q_{ext}}) \tag{6.5}$$

$$Q_u = (\frac{1}{Q_l} - \frac{1}{Q_{ext}})^{-1} \tag{6.6}$$

where Q_l is the loaded quality factor, f_{res} is the resonate frequency of the cavity,$\triangle f$ is 3-dB bandwidth, Q_{ext} is the external quality factor, and Q_u is the unloaded quality factor. Using weak coupling is to avoid overloading the cavity. When S_{21} is small, Q_{ext} is much larger than Q_l and reading for Q_l is more accurate. Considering an extreme case when S_{21} is close to 0 dB, Q_u calculated from Equations 6.5 and 6.6 is numerically sensitive and is hard to reflect the actual value.

In our research, a square cavity with a height of 300 μm is designed to resonate at 30 GHz with the dimensions shown in Table 4.

For a conventional solid-sidewall cavity with this height, the quality factor can be calculated as 607 at 30 GHz. However, pillar fences are used, leading to additional radiation leakage. More important, the inserted open-end CPW stub inside the cavity couples some

Table 6.1: Dimensions of the micromachined cavity.

	length	width	height	pillar diameter	pitch
units (μm)	7120	7120	300	160	600

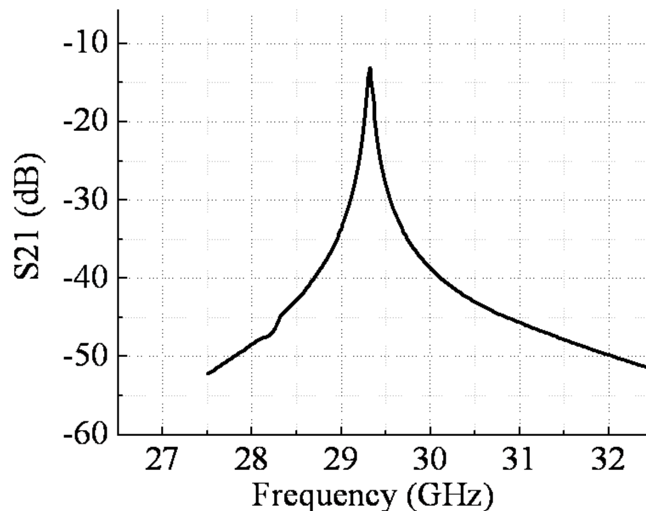


Figure 6.2: Simulated weak coupling response for the micromachined cavity.

electromagnetic energy into the substrate, thus introducing additional loss. These effects degrade the cavity quality factor and are difficult to predict analytically but are taken into account by using the FEM-based Ansoft HFSS 10.1 full -wave simulation, which also helps optimize the positions of the cylindrical pillars. The simulated weak coupling response is given in Figure 6.2. By considering the conductor/dielectric loss, as well as the radiation leakage from the feeding line, an unloaded Q of 280 is observed in simulation.

6.3 Fabrication and measurement

A specific type of soda-lime glass (Telic Co.) is chosen as the substrate to validate the proposed concept. The soda-lime glass is not optimized for high frequency applications since it has numerous impurities. The CPW line attenuation is extracted up to 110 GHz and it gives a 2.45 dB/cm attenuation at 30 GHz. This high dielectric attenuation severely degrades the performance of planar or in-substrate cavities.

As mentioned earlier, using solid metal side walls is not feasible in the fabrication;

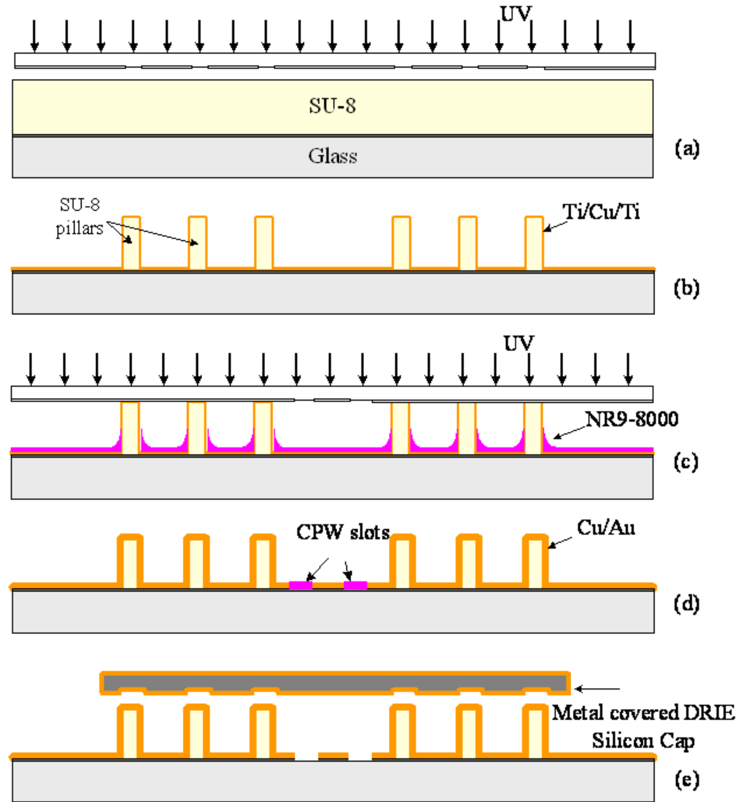


Figure 6.3: Process flow for the micromachined cavity.

plating the metal up to several hundred microns takes extremely long time and is costly. Instead, polymer-core conductor pillars are used. Even so, it is still unfavorable to make the whole sidewall using a single polymer-core since SU-8 has thermal property that is not same as the substrate. When there is a long SU-8 wall on the substrate, the accumulated tension causes severe delamination, thus damaging the structure.

On the contrary, a cylindrical pillar only has a limited foot-print and has a very good mechanical adhesion to the substrate. Rows of pillars exhibit similar electrical properties while not having mechanical problems.

Figure 6.3 shows fabrication steps: A thin Ti layer was sputtered to improve the SU-8 adhesion to the glass. A layer of 300 μm negative-tone photo-definable epoxy SU-8 2075 was dispensed and patterned to define the mold of pillar-fence side-walls. Ti/Cu/Ti was sputtered as the seed layer to cover the pillars, as well as the substrate in a conformal manner. Negative photo-resist NR9-8000 was coated and patterned in a non-contact way

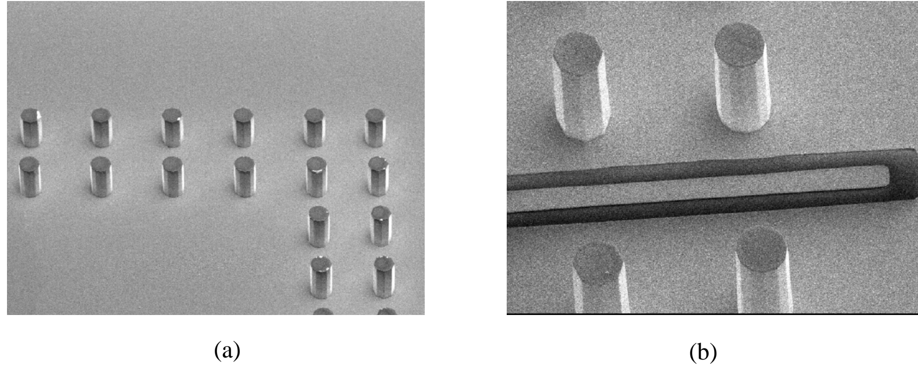


Figure 6.4: SEM pictures of the fabricated cavity (a)pillar arrays at the corner of the cavity (b) An open-end CPW stub passes between two adjacent pillars.

Table 6.2: Comparison of simulated and measured cavity performance.

	f_{res}	S_{12} dB	Unloaded Q
Simulation	29.23 GHz	-12.6	280
Measurement	29.65 GHz	-20.27	219

to cover the CPW slot region, preventing the metal coverage on the slot in the following electroplating step. Electroplating of 6 μm copper and 2 μm gold was done to cover pillars sidewall and uncovered feeding structures. At the same time, on a silicon wafer, rows of shallow pits were etched into the wafer at the exactly same position of the pillar fences and were metalized to be used as a top cap of the cavity. This is achieved by flipping the patterned silicon wafer piece and latching the released structure into the pre-defined pits.

The fabricated prototype (SEM pictures are shown in Figure 6.4.) was characterized using a two-port Agilent 8510C vector network analyzer with a probe station. The reference plane was set to be located at the outer surface of the rear pillar fences. The weak-coupled cavity resonates at 29.65 GHz with a 3-dB bandwidth from 29.6 GHz to 29.75 GHz (Figure 6.5). The peak coupling level from port 1 to port 2 is -20.27 dB. Using the Equations 6.4,6.5,and 6.6, Q_l is calculated as 197.7 and Q_u is calculated to be 218.9. The comparison between simulation and measurement is listed in Table 6.2 to demonstrate the difference.

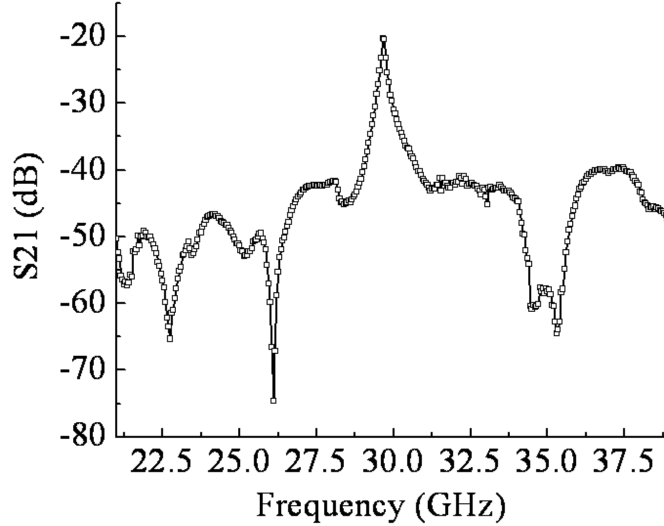


Figure 6.5: Measured weak-coupling response of the fabricated cavity prototype.

6.4 Discussion

The reason of getting a value lower than the one of a conventional solid wall cavity, with the same dimensions and resonating frequency, is mainly due to the loss from the inserted open-end CPW short stub. By using the excitation described in this section, even if the insertion loss of the line itself could be calibrated out by moving the reference plane into the cavity to the end of the CPW stub, the perturbation introduced by the lossy CPW stub could not be isolated from intrinsic cavity performance. The total response looked into the reference point would be the combination of the cavity resonator itself, whose intrinsic quality factor could be even higher, plus the lossy part of the series resonating stub. Non-uniform metal coverage for the vertical structures in the sputtering and electro-plating step caused an anisotropic deposition profile and a thinner coverage of the pillar bottom, which introduced more conductor loss. This might help explain the difference between the simulation and the measurement.

However, a planar CPW or microstrip resonator on the same substrate and at the same frequency would have a equal to 23.2 according to Equation 6.7, where α is the line attenuation as 2.45 dB/cm at 30 GHz and equals to 28.21 Np/m to be used in the above equation. β is the propagation constant of the line and λ_e is the guided wavelength. Comparing 23.2 with the value of 219, it can be easily seen that the Q_u of the proposed

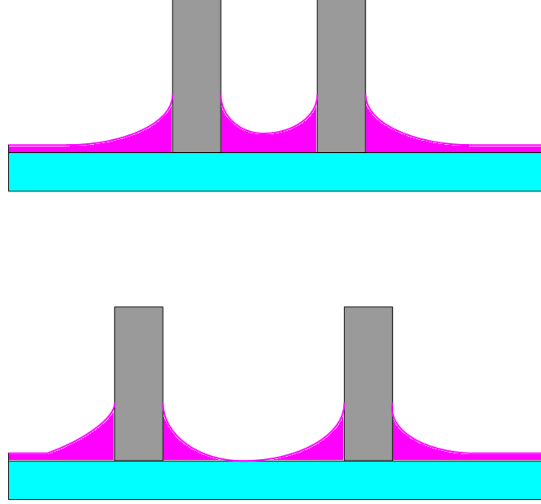


Figure 6.6: Photoresist thickness variation because of the existence of pillars.

resonator is significantly increased almost by an order of magnitude.

$$Q \approx \frac{\beta}{2\alpha} = \frac{\pi}{\lambda_e \cdot \alpha} \tag{6.7}$$

An interesting observation during cavity fabrication is photoresist distribution is greatly affected by the pillars. As the sketch shown in Figure 6.6, the photoresist thickness is no longer uniform when pillars exist. It is very easy to understand photoresist accumulates at the pillar bottom region. But it is not quite straight-forward to find out that the thickness between two adjacent pillars can be either thicker or thinner than other regions. As can be seen in Figure 6.6, when two pillars are very close to each other, photoresist is thicker than other regions; when two pillars are placed a little apart from each other, surface tension from the accumulated photoresist at the bottom will drag photoresist in the middle away and leaves a thinner coverage. When two pillars are apart far away from each other, the region between them has coating similar to other regions.

This finding is important to optimize the pitch between the two pillars that let a CPW feeding line to pass through. When photoresist is too thin and it cannot support long-time electroplating, leading to poor metal coverage of pillar sidewalls. Also, a thinner layer of photoresist leads to an over-exposed pattern to cover CPW slots. All of these should be considered in optimization the design and fabrication.

6.5 *Chapter summary*

This chapter focused on the development of a high-Q cavity for millimeter-wave applications, using surface micromachining technologies. A high-Q cavity resonator can find many application in filter design.

CHAPTER VII

MICROMACHINED ALL-POLE BAND-PASS CAVITY FILTERS

This chapter presents our research efforts on integrating high-performance millimeter-wave filters on top of a substrate by extending the surface micromachining technologies we have discussed in previous chapters. This chapter focuses on the development of all-pole bandpass filters while the next chapter introduces our research advance in transmission zero filters development.

With the aid of the polymer-core conductor surface micromachining technology, one can eventually eliminate the dielectric loss to elevate cavity-based filters into air. The electrical fields of the cavity are thus entirely in air. A coplanar waveguide input and output interface is designed for easy integration with other planar electronics. Several 60 GHz (V-band) air-cavity filters with superior performances are developed and characterized to demonstrate advantages of the proposed technology. The filters exhibit excellent performances. Design curves and parametric analysis are included to summarize key factors in optimizations.

7.1 Background

High-performance millimeter-wave filters play very important roles including filtering, duplexing and multiplexing in emerging communication systems [64]. In the millimeter-wave regime, substrate loss has become a dominant factor that limits filters' performances [35]. Waveguide filters have been used for millimeter-wave applications for years because of their excellent insertion loss, power handling capability and frequency selectivity [12]-[4]. In the millimeter wave regime, sizes of waveguide filters become smaller and silicon wafers can be etched, metalized, stacked and bonded together to implement millimeter waveguide filters [26][67][50]. Great fabrication accuracy can be achieved, which is critical for millimeter wave and THz applications. However, most of these filters use standard waveguide input/output interfaces that can limit their applications. Stereo-lithography uses laser to make various complicated three-dimensional (3-D) structures [22]. However, it is hard to

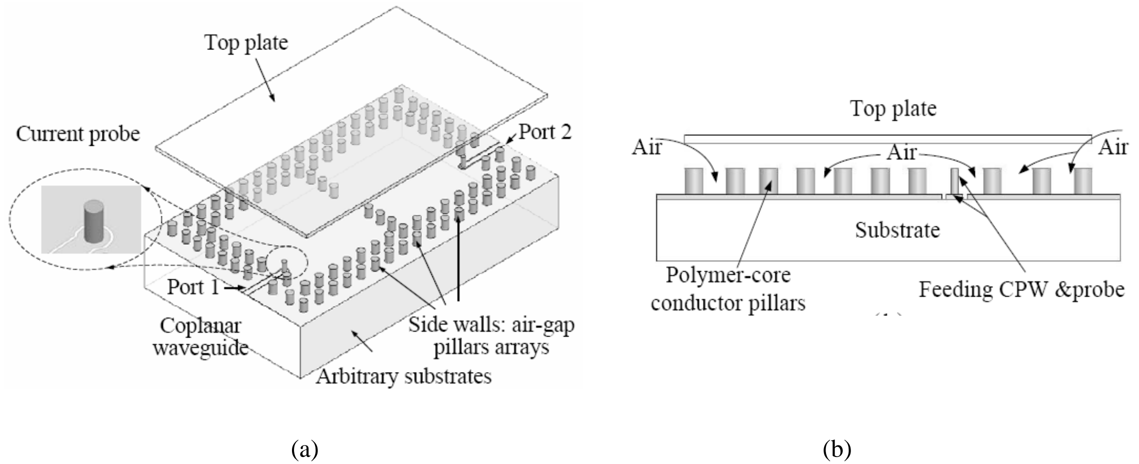
directly integrate those structures with planar components. In [44], a silicon micromachined filter with an integrated transition from a coplanar waveguide to a rectangular waveguide was reported. Great performance was demonstrated except for the requirement of using a bulk-micro-machine-able substrate. As an alternative method, the surface micromachining technology based on polymer-core conductor approach is substrate-independent and can be implemented on any substrate theoretically.

Another idea is a substrate integrated-waveguide (SIW) (or called EBG/MBG cavity, laminated waveguide and post-wall waveguide in some literatures)[71][19][11][14][29]. It is compatible with planar component integration. This concept has been implemented using various substrates such as PCB boards [29] and LTCC [78]. Great performances were reported from these designs. One limit is that the technology requires a low-loss substrate and use of via-hole technologies. A substrate integrated image waveguide/resonator is associated with the similar issue [77]. [69] reported a surface micro-machined approach to implement substrate integrated waveguide. It uses a photo-definable dielectric to form the waveguide on top of substrate. It still requires a low-loss dielectric material.

In our investigation, a waveguide cavity filter is moved onto the top of substrate. The entire cavity/waveguide filter is *on top of* the substrate. The requirement for a low-loss substrate is no longer necessary since air fills the cavity/waveguide. This chapter will focus on design, fabrication and characterization of 60 GHz (V-band) filters with superior measurement results using this new integration method, including a 2-pole filter with CPW-waveguide transition sections and a 2-pole filter with direct CPW-probe feeding.

7.2 Proposed polymer-core conductor surface micromachining technology for filter implementation

Figure 7.1 shows the filter structure. Figure 7.1 (b) shows its side view. Unlike a substrate integrated waveguide (SIW) where rows of vias are located inside the substrate, metalized pillars rows here are moved onto top of the substrate, with air gaps between them. These pillars make the side walls of the elevated cavity/waveguide. When the diameter of the pillars and the pitch between pillars satisfies the rule suggested in [15],which is also described in Chapter 6, the leakage from the air gaps between pillars can be neglected. The top plate is



(a) (b)

Figure 7.1: (a) Proposed cavity-resonator filter structure using polymer-core conductor surface micromachining technology (top plate elevated for clarity). (b)side view of the proposed filter structure.

a separate metalized piece stacked on top of pillars and the bottom plate is the metallization on the top of substrate. The underneath substrate only plays as a carrying medium. In Figure 7.1 (a), the top plate is raised high deliberately to reveal the side wall details.

Cores of pillar arrays are formed through patterning a thick layer of photo-definable polymer SU-8, and then plating their outer surface up to several microns. Compared with traditional via-hole plating using in a SIW, the proposed method is more economical. Although it is possible to directly pattern solid walls, pillar fences are used instead due to the fabrication feasibility concern, which has also been discussed in Chapter 6.

The proposed configuration offers several advantages for filter implementation:

1) *Reduced loss*: the dielectric loss is eliminated because the entire electromagnetic field is constrained in a air-filled waveguide/cavity; the metalized ground blocks the dielectric loss from the underneath substrate.

Now, we will demonstrate loss reduction of the proposed technology quantitatively. When leakage loss from the gap between pillars can be minimized, the conductor loss will dominate the overall attenuation because the dielectric loss is eliminated in this technology. According to [15] and [76], the conductor loss of vias is almost the same as the one of a solid wall surface and the latter can easily be calculated from equations in [12]. In addition, a

surface roughness of 0.2 μm is the average value we measured in our prototypes metalized by the gold electroplating technology. This roughness increases the surface resistance of the waveguide and thus needs to be taken into account.

To get a quick estimation of insertion losses for the proposed filter and waveguide structures, FEM-based numerical simulations (Using Ansoft HFSS 10.1) are performed to compare attenuation per unit length for the following waveguide configurations and unloaded quality factors for different cavity configurations: (a) a solid-wall gold waveguide without surface roughness, (b) a solid-wall gold waveguide with 0.2 μm surface roughness and a total surface metal thickness of 3 μm (c) a pillar-array sidewalls surface micromachined gold waveguide with 0.2 μm surface roughness and a total surface metal thickness of 3 μm. Unloaded quality factors are extracted for the following cavity configurations: (d) a 60 GHz solid-wall gold cavity resonator without surface roughness, (e) a 60 GHz solid-wall gold cavity resonator with 0.2 μm surface roughness and and a total surface metal thickness of 3 μm, and finally (f) a 60 GHz pillar-array sidewalls surface micromachined gold cavity resonator with 0.2 μm surface roughness and a total surface metal thickness of 3 μm. The surface roughness assignment is achieved through a built-in boundary condition feature of HFSS 10.1. The simulation results, as well as the calculated conductor and dielectric losses using equations in [12], are listed in Table 7.1.

It can be seen from Table 7.1 that replacing solid-walls with pillar-array sidewalls with air gaps only slightly increases the conductor loss from 0.117 dB/cm to 0.134 dB/cm. It also can be observed that an additional 0.154 dB/cm attenuation from the dielectric loss will be added onto the conductor loss if a material with the loss tangent of 0.002 is used instead of air at 60 GHz. This value is comparable with the conductor loss associated with the one of (c). In other words, eliminating the dielectric loss can significantly reduce the overall loss. It is also found that the unloaded Q of a pillar-array-based cavity resonator is quite close to one with solid walls.

2) *Improved manufacturing accuracy and flexibility*: because photolithography is used in fabrication, the accuracy of the pillars' diameter can be well controlled on the level of micrometer and continuously tuned. The proposed technology can also introduce more design

Table 7.1: Comparisons of waveguide/cavity insertion losses for different conditions

index	attenuation (dB/cm)	index	unloaded Q
a	0.074	d	795
b	0.117	e	679
c	0.134	f	645
α_c [3]	0.0876		
α_d [3]	0.154		

(TE_{10} mode for waveguide and TE_{101} mode for cavity)

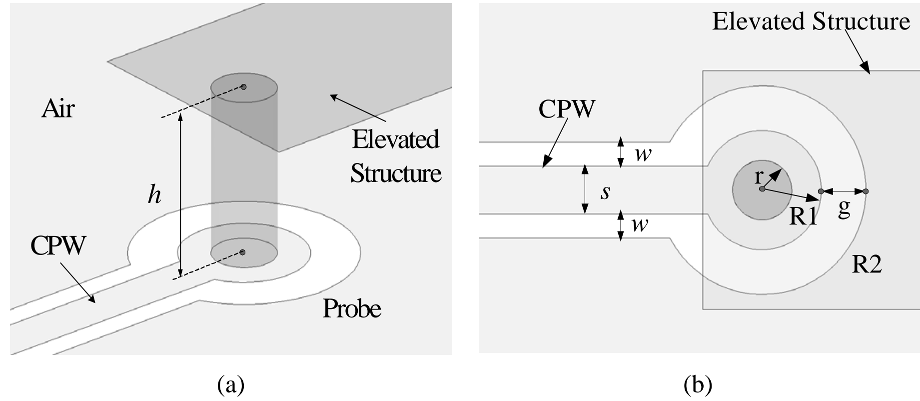


Figure 7.2: (a) 3-D view (b) top view of a vertical probe connected with a CPW line.

flexibilities that help create new designs/topologies that might be hard from a traditional mechanically-machined waveguide: the diameters for different pillars can be designed to be different with each other; the height of the pillars can also be continuously controlled from several microns up to 1~2 mm; SU-8 2150 can reach as high as 600 μm for the single spin coating and repeatable and high yield pillar array with aspect ratio of 25 or higher can be achieved [2]. Without the requirements for standard via dimensions and standard board thicknesses, this method extends the design space.

3) *Substrate independent*: Last but not the least, it is a substrate independent approach; one optimized design can be easily used on other substrates.

Taking into account all of these advantages, the polymer core conductor micromachining method can be an excellent candidate for millimeter-wave filter implementation.

7.2.1 Feeding scheme

For a substrate integrated cavity filter, feeding using a microstrip-line is the most popular way. It is hard to implement similar feeding for the proposed structure when "via"-arrays are placed onto the substrate surface. A slot opening on the intermittent metal plate for multilayer configuration [40] is also not feasible for the proposed single layer elevating structure.

A CPW line can be used as feed; the CPW signal line can be inserted into the cavity to excite it. This has been used to weakly excite the air cavity in Chapter 6. Here, however, it is hard to get the critical coupling level for filter applications. This is because the dielectric constant of the substrate is higher than the air; the energy along the feeding line will be mainly constrained in the substrate.

A CPW-connected current probe is used instead. To feed a substrate integrated cavity, it can be just half way or completely reach the bottom plate [13][40]. Here, the current probe has to touch the top plate to simplify the fabrication. The detail of feeding is shown in Figure 7.2.

7.2.2 Design flow

Several 60 GHz filters are designed, fabricated and characterized in this chapter to demonstrate the claimed advantages. All designs follow the same procedure described below.

1) Specifications are first given, including center frequency, fractional bandwidth, desired matching level and filter-type (Chebyshev, max flat or elliptical type).

2) A group of the low pass prototype parameters g_0, g_1,..., g_n is given from the desired filter response; the required external and internal coupling coefficient can be calculated using these parameters [49].

3) Decide the type of the coupling structure for external and internal coupling and look up the design curve to find the optimal physical dimension. Solid walls are used for the time being to expedite simulations.

4) Solid walls are transformed into pillar arrays and full wave simulations are performed to make the final adjustments using Equation 7.1 (from [11]):

$$W_{eff} = W - D^2/0.95b \quad (7.1)$$

where W_{eff} is the equivalent width of the waveguide and W is measured distance between the two inner rows of pillars (center to center). D is the diameter of the pillar and b is the pitch between two adjacent pillars. D and b were chosen to minimize the EM-wave leakage while meeting the fabrication constrains [15].

7.2.3 Fabrication flow

Figure 7.3 details fabrication steps: a thin Ti layer was sputtered to improve SU-8's adhesion to the glass. A layer of several hundred microns thick negative-tone photo-definable epoxy SU-8 2035 was dispensed and patterned to define the cores of the pillar fences. Ti/Cu/Ti was then sputtered as the seed layer to cover the pillars, as well as the substrate in a conformal manner. Negative-tone photo-resist NR9-8000 was coated and patterned in a non-contact way to cover the CPW slot region, preventing the metal coverage on the slot in the following electroplating step. Electroplating of copper and gold covers the sidewall of the pillars and the exposed feeding structures. A piece of silicon wafer was metalized to be used as a top plate of the cavity, by flipping the silicon wafer and bonding together using silver paste. The electrical properties of silver paste we used can be found in [33].

7.3 Development of an elevated waveguide iris filter with a CPW-waveguide transition

The first filter design is an elevated waveguide filter with inductive irises. A Chebyshev-type 2-pole filter with a 0.1 dB pass-band ripple is designed. It has a 2.65% fractional bandwidth centered at 60 GHz.

Shown in Figure 7.4, it consists of two cavity resonators in the middle and one CPW-to-waveguide transition at each end. The top plate is not shown for clarity in Figure 7.4. The CPW-to-waveguide transition is used to transform the CPW quasi-TEM mode to the rectangular waveguide TE_{10} mode [47][62]. The mode transition is achieved with the current probe [13].

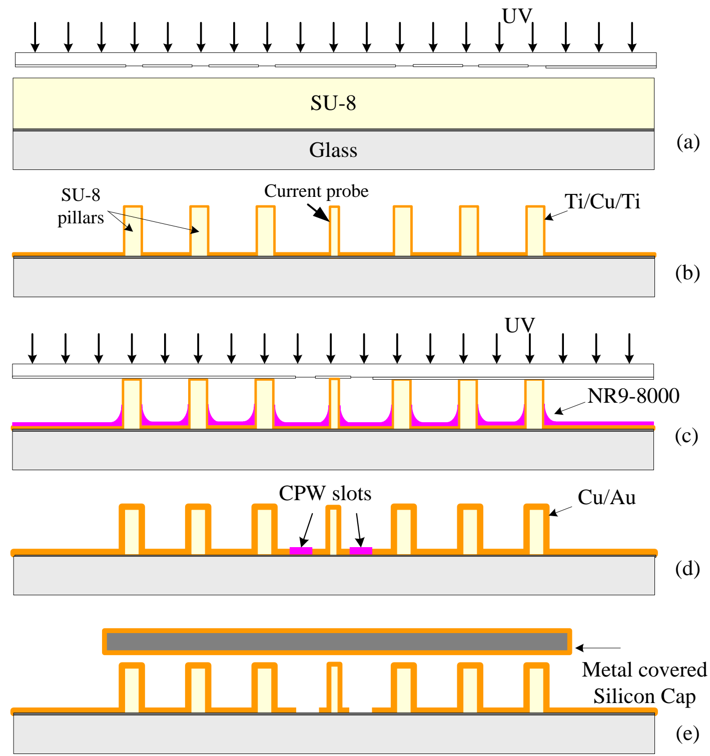


Figure 7.3: Fabrication flow of the proposed air-lifted cavity resonator filter using polymer-core pillar arrays.

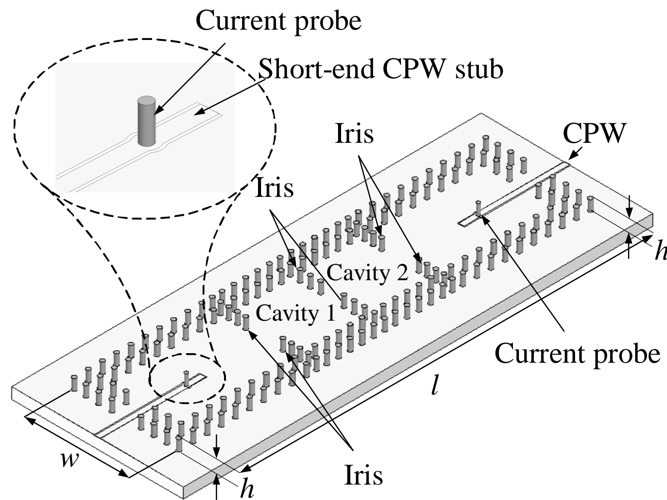


Figure 7.4: Schematic of an air-lifted two-pole cavity filter integrated with a coplanar-waveguide to waveguide transition.

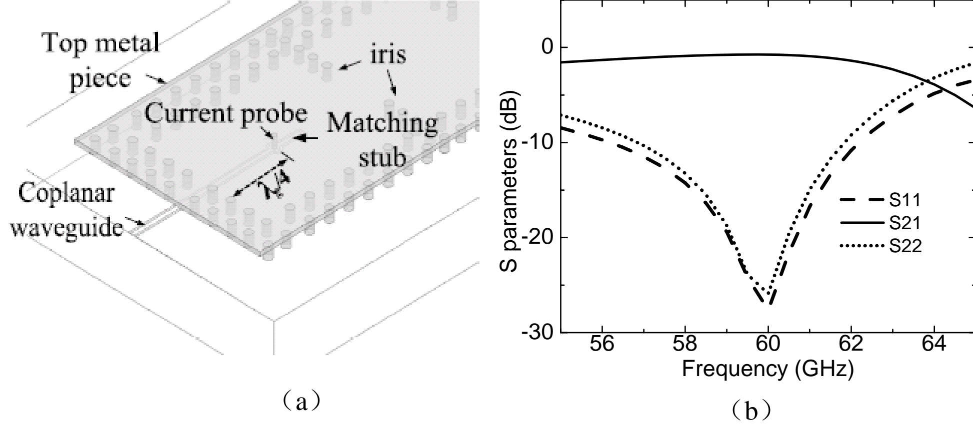


Figure 7.5: (a) Schematic of a CPW-waveguide transition (b)full-wave simulation results for the transition.

Table 7.2: Optimized filter dimensions (Units: mm).

Dimensions	Value	Dimensions	Value
l	19.16	i_in	1.0
w	8.32	d_ex	1.0
l_c	3.16	xl	2.7
d_in	1.3	t	0.2

Figure 7.5 (a) shows the CPW-to-waveguide transition used in this paper, with full wave simulated performances plotted in Figure 7.5 (b). The transition shows good impedance matching for both CPW port (S_{11}) and rectangular waveguide port (S_{22}) in the vicinity of 60 GHz. A 0.74 dB insertion loss is found for the transition itself using the full-wave simulator Ansoft HFSS.

A two-pole iris-based waveguide filter is designed using the classical synthesis procedure. By looking up appropriate external and internal dimensions from design curves in Figure 7.6, the required external coupling level and internal coupling level can be achieved.

After the waveguide filter is designed, it is connected with the CPW-waveguide transition at each end. The whole structure is re-optimized by FEM-based full-wave simulations and final dimensions for this solid wall CPW-connected 2-pole Chebyshev filter are listed in Table 7.2, with legends marked in Fig. 7.7. Finally, solid walls are replaced by two rows of pillar arrays using Equation 7.1.

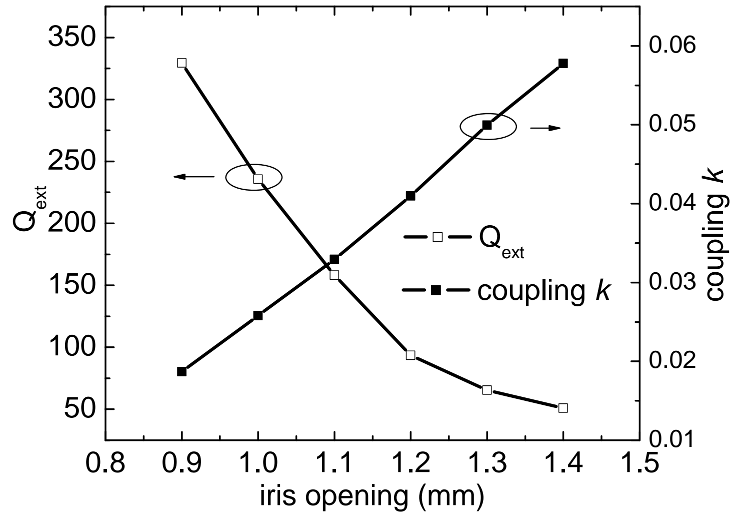


Figure 7.6: External loading quality factors vs. external iris opening; internal coupling coefficients vs. internal iris opening.

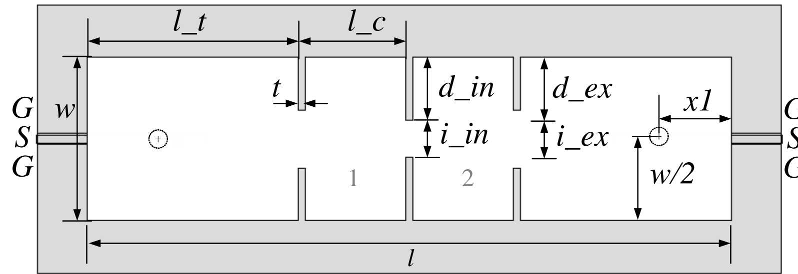


Figure 7.7: Dimension illustration of two-pole cavity resonator filter with a CPW-waveguide transition.

Table 7.3: Comparison of simulated and measured filter responses

	f_{res}(GHz)	Insertion Loss(dB)	3dB BW(GHz)
Simulated	60.20	2.4 dB	1.6 (2.65%)
Measured	60.25	2.9 dB	1.6 (2.65%)

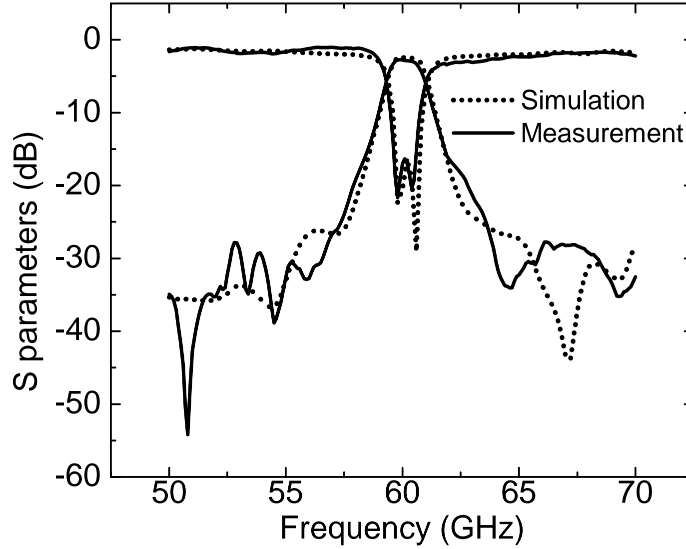


Figure 7.8: Comparisons of simulated and measured responses for the filter in Fig. 7.4

The fabricated sample on the quartz glass substrate is measured by an Agilent 8510XF vector network analyzer station connected with GSG probes of a 250 μm pitch. The system is calibrated with NIST Multical TRL scheme between 50 GHz and 70 GHz [48].The reference plane is set to the outer surface of the sidewall. The measurement results are plotted together with the simulation results in Figure 7.8.

Great agreement between the simulation and the measurement is observed, shown in Table 7.3. The central frequency moved from 60.20 GHz in simulations to 60.25 GHz in measurements. The fractional bandwidths are same in simulation and measurement. A 2.9 dB insertion loss and a return loss greater than 15 dB are achieved for the fabricated prototype. The insertion loss is slightly higher than the simulation result, which is 2.4 dB. From Figure 7.5 (b), one CPW-to-waveguide transition introduces 0.74 dB loss and two transitions used in the filter will introduce 1.48 dB loss. Simulation results using HFSS indicate a 0.32 dB loss for if PEC is used for this transition. This shows a 0.42 dB loss is from the metal loss of the transition and 0.32 dB for the radiation leakage into the substrate with a long CPW line used in this transition.

Only less than 1.5 dB comes from waveguide filter itself. If the transition loss can be minimized, better performance should be observed.A 2-pole filter without a CPW-waveguide

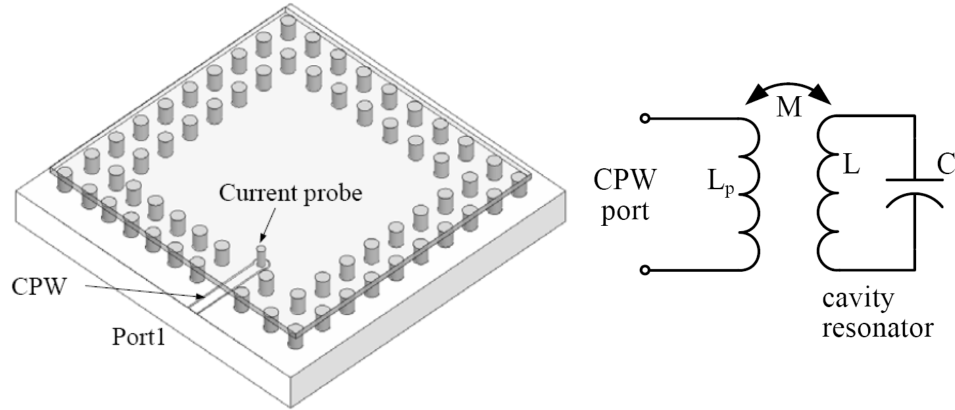


Figure 7.9: Schematic and equivalent circuit of a single air-lifted cavity directly fed by a CPW-connected current probe.

transition will be presented in the next section to further improve the filter performance.

7.4 An elevated cavity filter with current probes directly fed into resonating cavities

As found in the previous section, including a CPW-to-waveguide transition simplifies the filter design into two independent steps: optimizing the transition itself and designing the waveguide filter. Many mature waveguide filter designs can directly be transformed to elevated pillar-array based filters using the same transition. However, for a low order filter, the transition consumes more circuit area than the waveguide filter itself. It also increases the whole insertion loss.

In this section, the CPW-waveguide transition is removed. Instead of exciting a cavity filter from the external waveguide using an iris, a CPW-connected probe is directly fed into the resonating cavity. Shown in Figure 7.9, the current probe excites the cavity using magnetic coupling; its equivalent circuit model is given in Figure 7.9. Figure 7.10 shows the schematic drawing of the CPW probe directly-fed 2-pole filter.

The external coupling level is controlled by the position of the current probes inside the cavity. The external coupling decreases when the probe moves away from the center of the cavity, but the resonating frequency also decreases at the same time. So the size of the cavity has to be adjusted to compensate for this frequency shift. Another issue is that the minimum distance between the probe and the sidewall is restricted by the fabrication limit;

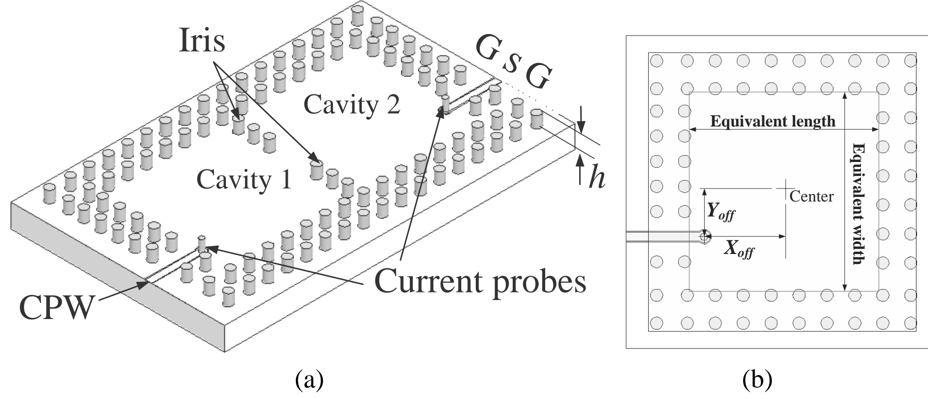


Figure 7.10: (a) Schematic of CPW probe directly fed 2-pole filter.(b) 2-D view of possible moving directions of the feeding current probe.

Table 7.4: Optimized filter dimensions (Units: mm).

Dimensions	Value	Dimensions	Value
l	8.32	i	1.0
l_c	3.4	X_{off}	1.5
w	3.5	Y_{off}	0.8
t	0.2		
d	1.3		

moving the probe only along the center line may not get the a required low coupling level. In our work, we find that moving the probe off the center line can overcome this limitation and greatly increase the tuning range of the external coupling level. This is because the field distribution is the product of two sinusoid functions in both X and Y directions (offsets from the cavity center are determined by X_{off} and Y_{off}) (The definitions for X_{off} and Y_{off} are indicated in Figure 7.10 (b)). Moving probes only within one direction will limit the tuning range.

Figure 7.11 (a) and (b) show how X_{off} and Y_{off} affect the external quality factors. In Figure 7.11 (a), Y_{off} is fixed as zero. For (b), X_{off} is fixed as 1.4 mm. From these two curves, we can see that designing a very narrow band filter is made possible by moving current probes to the corner of the cavity.

A Chebyshev type filter with 0.1 dB pass band ripple is designed to cover a 2.0 GHz 3-dB bandwidth centered at 60 GHz using this direct feeding approach. By looking up the

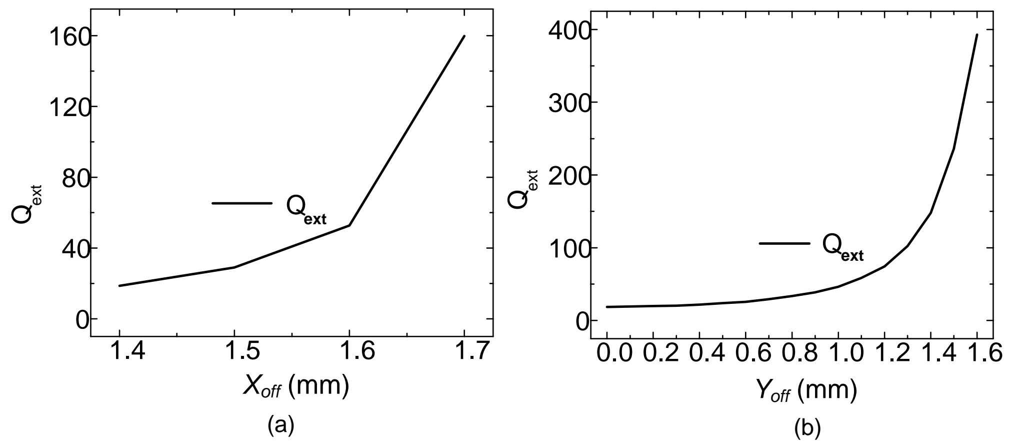


Figure 7.11: (a) External quality factor vs. X_{off}. (b) External quality factor vs. Y_{off}.

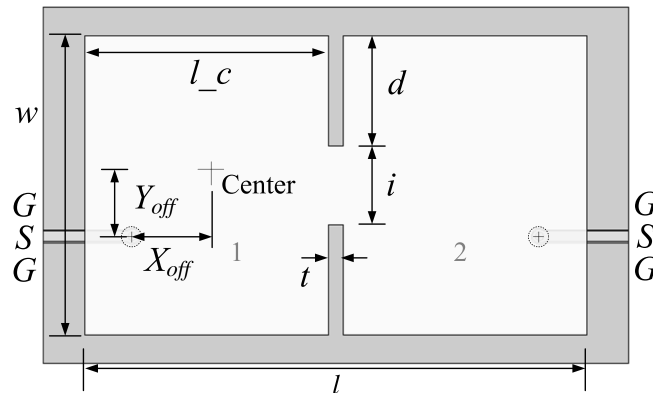


Figure 7.12: Dimension illustration of the filter in Fig. 7.10 (a).

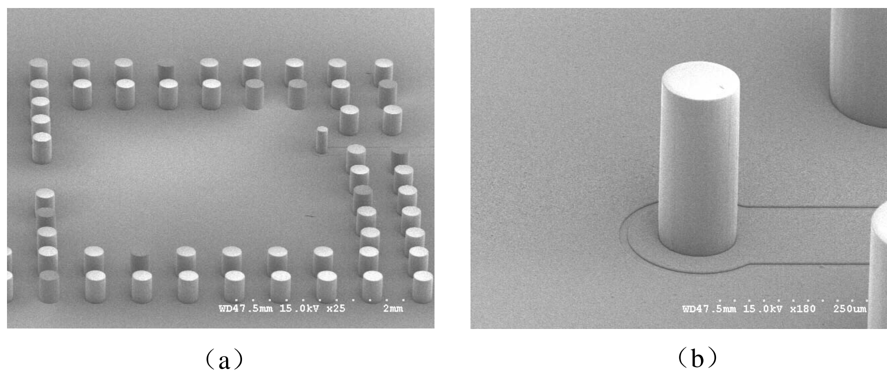


Figure 7.13: SEM pictures for a fabricated prototype (a) one pillar fence cavity with a feeding probe connected with a CPW line (b) A vertical current probe connected with a CPW line.

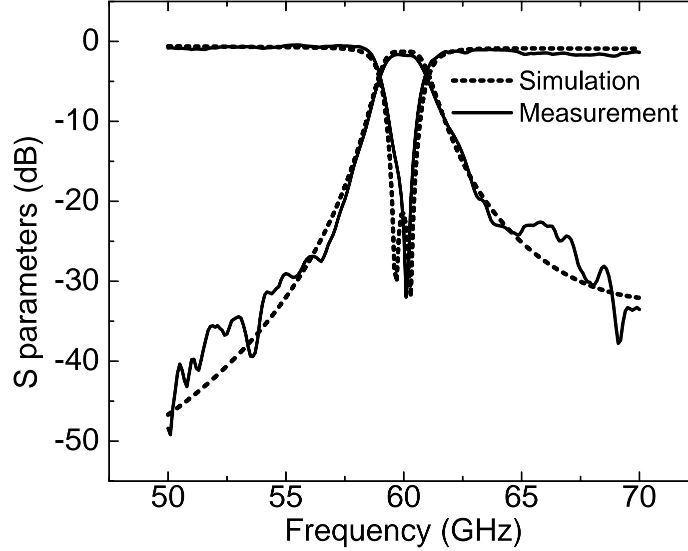


Figure 7.14: Comparisons of simulated and measured responses for the filter in Figure 7.10(a).

appropriate external and internal dimensions from the design curves in Figure 7.11 (a)(b) and Figure 7.6, the required external coupling level and internal coupling level can be found. The whole structure is optimized by full-wave simulation and the final dimensions for this compact solid wall 2-pole Chebyshev filter are listed in Table 7.4, with legends marked in Figure 7.12. Solid walls are replaced by two rows of pillar arrays using Equation 7.1.

A prototype is fabricated using the similar procedure as the one in the previous section. SEM pictures are shown in Figure 7.13 for the fabricated pillar side walls and patterned feeding structures. A similar measurement setup and calibration method with the one used in the last section are used here. Measured results show a good agreement with the simulated ones (Figure 7.14). A 1.45 dB insertion loss is found from measurement while the center frequency keeps the same. The excellent performances result from elimination of the dielectric loss in this proposed technology.

In summary, compared with the CPW-waveguide-cavity feeding technique in the previous section, the directly feeding approach can further reduce the insertion loss. This novel offset feeding increases the tuning range of the external coupling level and make it possible to design the very narrow band filter.

7.5 Discussion

Unlike the monopole and the elevated patch discussed in previous chapters, the micro-machined filters consist of rows of pillars. Ideally, these pillars should have exactly same heights. This is for good contact between pillar rows and the top cover. It is equivalent to say that SU-8 coating should be uniform across the wafer because SU-8 coating thickness defines pillar height.

In our experiments, we have found several non-ideal factors, and here we discuss their impact on filter performance.

7.5.1 Dealing with air bubbles

The first one is air bubbles inside SU-8 during coating. Bubbles exist for any photoresist but they put more challenge to SU-8. This is because SU-8 is very dense and viscous. When air gets trapped in SU-8, it is not easy to get it out.

Air bubbles in SU-8 not just introduce defects for a pillar-based structure, more severely, they change coating thickness of SU-8 in the vicinity of bubbles. After SU-8 is pre-baked at 95 °C for a long time and all solvent gets evaporated, SU-8 becomes harder and trapped air bubbles emerge on top of SU-8 thick-film. Because of their existence, the nearby film is pulled up and form a small bump. After these bubbles are pierced broken, a crater profile forms. Consequently, the region close to the crater cannot be used. Pillars can still be patterned in this region, but their heights are different with other pillars.

If a relatively large bubble forms during SU-8 curing, the uneven surface will extend far away from the center of the crater region. Even though the pillars close to this region can be removed, the electrical performance of a structure can be severely degraded because of possible leakage. This may even cause system disfunction.

Here are several solutions for this issue:

Use new SU-8: It is very important to avoid using a SU-8 epoxy bottle that is close to its expiration date. Air bubbles accumulate throughout its life time. Newly made SU-8 has less bubbles.

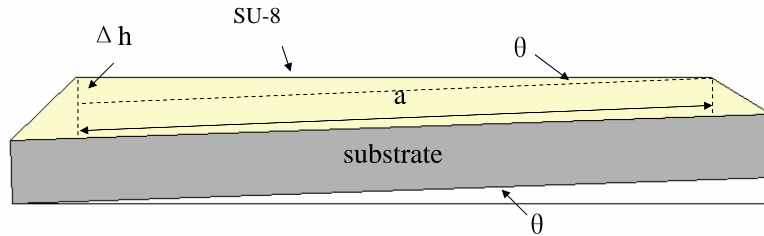


Figure 7.15: Illustration of uneven film coverage for a tilted wafer.

Use a syringe instead of a pipette to dispense SU-8: In fabrication, pulling SU-8 out of a bottle into a syringe, then slowly squeezing air out of the syringe, and then carefully dispensing SU-8 on wafer can introduce less air bubbles than using a pipette.

Heat to 50 °C and break air bubbles: Around 40-50 °C, SU-8 has better mobility. If the temperature is too high, solvent will evaporate quickly and SU-8 will lose its fluidity. Trapped air bubbles stay in the SU-8 film and it is hard to get rid of them. It is best to use a tool with a sharp tip to break air bubbles when SU-8 has a good flowing mobility, or it is also good to use a pipette to move air bubbles to the edge of the sample.

After combining these techniques and with a very careful handling, a good SU-8 film can be achieved. The resulted film will have a very smooth surface.

7.5.2 Impact of a tilted substrate

Because SU-8 film thickness is on the order of several hundred microns for the filters discussed in this chapter, a small tilting angle from the horizontal plane will introduce a significant difference of film thickness at different ends of a wafer. An evenly SU-8 coating is realized with the aid of SU-8's self planarity property. When SU-8 is heated to 40-50 °C and becomes more like liquid, its upper surface is always lined as water-level even if the wafer is tilted. This happens because a hot plate to bake SU-8 is hard to be perfectly levelled.

As illustrated in Figure 7.15, when the wafer is tilted, the upper surface of a SU-8 film is completely levelled with the horizontal plane, while the bottom of the film is not. This

Table 7.5: Pillar height difference versus different tilting angles.

	a (mm)	θ (degree)	ΔH (μm)
	8.3	1	145
	8.3	0.25	36
	8.3	0.1	14
	3.5	0.25	16
	3.5	0.1	6

introduces different film thickness across the wafer. Since this variation is continuous, it is not a big problem for good contact with a top cover. However, when a filter dimension is large, this might introduce a significant height difference for pillars at two ends of a filter. The impact on the electrical performance of such a filter need to be studied.

Using Equation 7.2, the height difference ΔH along a distance of a for a wafer tilted by a degree of θ can be calculated. Computed results for different angles are listed in Table 7.5.

$$\Delta H = a \tan(\theta) \tag{7.2}$$

For large-scale manufacturing, this system error can be excluded by using highly precise tools to level the hotplate for SU-8 baking. It is thus not an issue for manufacturing.

However, for prototype building in a multiple-user shared cleanroom, this factor has to be taken into account. As can be seen from Table 7.5, a tilting angle of 1 ° can introduce 145 μm thickness difference at a distance of 8.3 mm. Since pillars' height of the filters presented in this chapter is only 300 μm, this thickness variation is apparently unacceptable. To minimize thickness variation, several spirit levels are used to level the hotplate for baking SU-8.

From our experiments, for the first filter that has a length of 19.2 mm, the height of SU-8 pillars is measured between 265 μm to 330 μm, which corresponds to a tilting angle less than 0.25 °. for the second filter that has a length of 8.3 mm, the height is measured between 280 μm to 315 μm. They are not consistent to each other. This is because they were fabricated at different time and we can not maintain same conditions for our fabrication

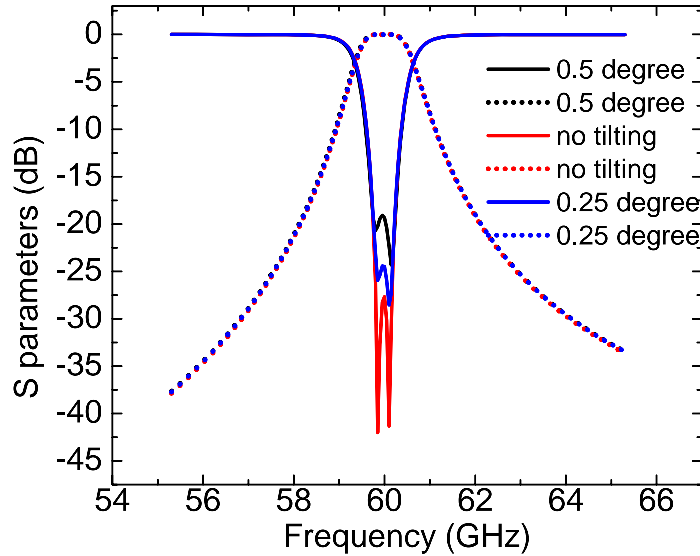


Figure 7.16: Simulated filter responses versus substrate tilting angle.

because of the nature of prototype building. However, the tilt angles of the hotplate after calibrated with spirit levels at different time are close to each other. This means, this angle (approximately 0.25 °)is within the precision limits of this simple levelling tool.

Full-wave simulations are performed to find out the impact of this thickness variation across a wafer. To expedite simulations, a solid-wall version is simulated. Otherwise, changing heights for each pillar is not just tedious, but more importantly, will cause objects intersection issues. The result gotten from the solid-wall design should be the same as the pillars design since pillars are used just for representation of a solidwall.

Figure 7.16 show simulation results for the filter with direct-feeding probes. As can be seen, the center frequency and fractional bandwidth remains unchanged. It only shows a slight mismatch compared with the ideal case. However, they are all still below -15 dB and one can conclude that substrate tilting is not a big problem for this type of filter.

7.6 Chapter summary

This chapter focused on the development of low-loss all-pole band-pass filters using polymer-core conductor micromachining technology. Superior measured results demonstrate that the polymer-core conductor surface micromachining technology can be used for high-performance millimeter-wave filters.

CHAPTER VIII

MICROMACHINED TRANSMISSION-ZERO FILTERS

8.1 Background

Introducing transmission zeros at finite frequencies is a popular way to get a sharp roll-off characteristic and improve filter selectivity. A general approach is to create two transmission paths from the source to the load. The phase shift difference between the two paths is designed to be 180 ° at two certain frequencies below and above the pass band. At these two frequencies, signals from the two paths are destructively added together, thus creating two transmission zeros.

8.2 A 4-pole transmission-zero filter using both electrical and magnetic coupling

In this section, a four-pole cavity resonator filter with a pair of transmission zeros is developed. Figure 8.1 shows the coupling scheme of a 4-pole transmission-zero filter. Four resonators are cascaded between the source and the load. As can be seen, two transmission paths are created in this design. Path 1 is *source-1-2-3-4-load* and Path 2 is *source-1-4-load*. The mutual coupling coefficients between two adjacent resonating nodes are denoted as m_{12}, m_{23} and m_{34}, respectively. The cross-coupling coefficient between cavity 1 and 4 is m_{14}. Figure 8.2 shows how the coupling schemes shown in Figure 8.1 can be implemented by the polymer-core conductor surface micromachining technology. The top plate of the 4-pole transmission-zero filter is not shown for clarity. Four pillar array cavities are integrated on top of the substrate. The external coupling uses the similar scheme that has been used for the one in the previous section for compactness and insertion loss reduction. An iris is used between adjacent cavities to provide inductive coupling because of its simplicity. The challenge is to realize capacitive coupling. The capacitive coupling for cavity-based resonators can be realized using a septa [65] or a slot opening into the broad wall shared by two stacked cavities [25][43]. The former requires building a waveguide ridge, which is hard

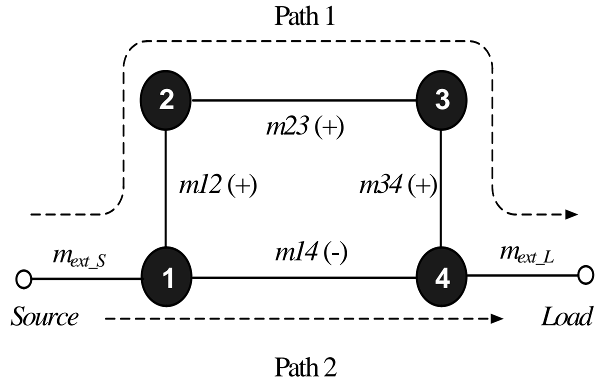


Figure 8.1: Node representation of a four-pole transmission-zero filter.

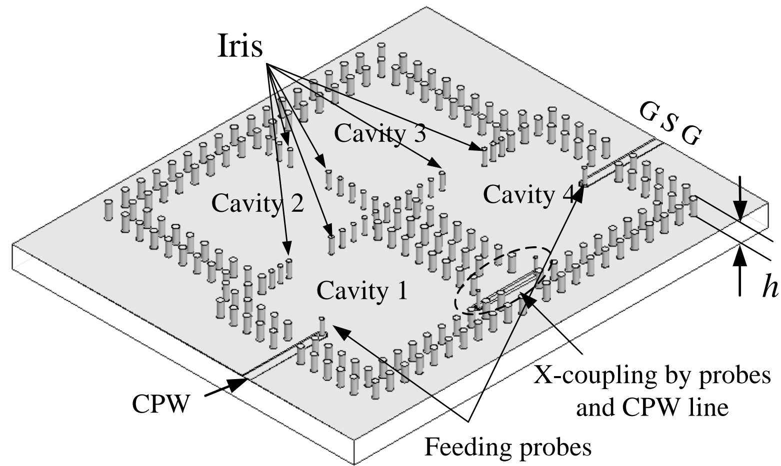


Figure 8.2: Proposed four-pole transmission-zero filter using polymer-core conductor surface micromachining technology (top plate not shown for clarity).

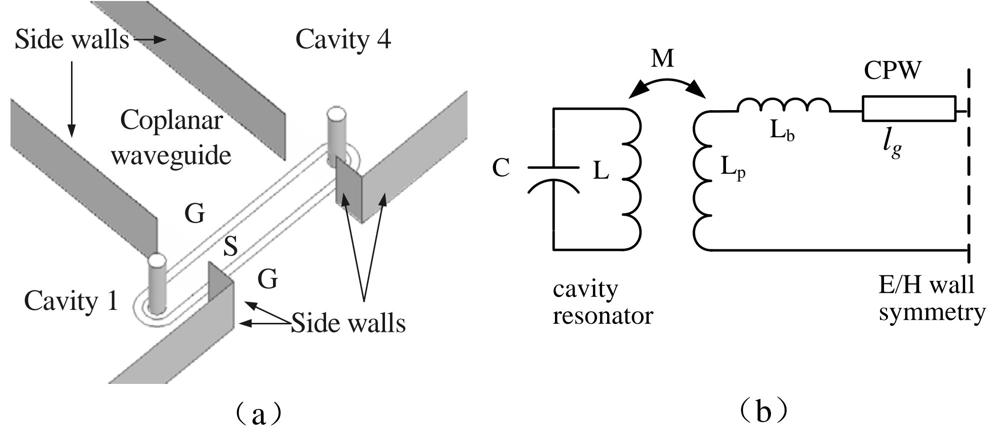


Figure 8.3: (a) Detailed cross-coupling scheme between cavity 1 and 4 (top plate not shown and side wall replaced by solid wall for clarity).(b) Equivalent circuit model for the half of the coupling structure.

to implement for this single layer surface micromachining technology; the latter needs multilayer processing capability. Another way is to use over-mode or dual-mode operation [52] [23][75], which requires oversized cavities. [52] also introduces asymmetry into the design. This increases the overall size and the optimization complexity. Therefore, a new capacitive coupling structure must be developed specially in our research.

8.2.1 A novel electrical coupling design for cross-coupling

Besides the loss reduction, the other big advantage provided by the integration scheme discussed in this dissertation is easy connection with planar components and this feature is used here to get a novel capacitive coupling structure. By combining 3-D structures and planar transmission lines, one can create new coupling schemes that are not implementable using either fabrication method only.

Figure 8.3(a) shows the detailed cross-coupling scheme. To better understand the operating mechanism, the first-order equivalent circuit model for the capacitive structure is plotted in Figure 8.3 (b). Since the structure is symmetrical, only half of it is shown and modelled below. In Figure 8.3(a), the pillar array side walls are replaced by solid sheets for clarity and the top plate is not shown. Two current probes, similar to the probes used for an input/output coupling, couple energy out of cavities to the CPW line connecting between them. Since the whole structure between 1 and 4 is symmetry, the easiest way to analyze

whether the coupling is electrical (capacitive coupling) or magnetic (inductive coupling) is to compare the resonant frequencies by inserting electrical walls and magnetic walls at the symmetry plane respectively. If f_e is less than f_m, the coupling is electrical; otherwise, it will be magnetic [39].

Numerical simulations are performed and it is found that electrical (capacitive or negative) coupling can be created for certain CPW lengths between cavity 1 and 4.

In Figure 8.3 (b), Cavity 1(or 4) is represented by a shunt LC circuit. The vertical current probe with a self inductance l_p couples from cavity 1(or 4) to the CPW line. The mutual coupling level M between the cavity and the probe is controlled by the probe position inside cavity 1. The short CPW section inside the cavity is represented by a small inductance L_b. The CPW length between the cavity wall and the symmetry plane is l_g. The line characteristic impedance is Z_{cpw}.

The value of l_g can be changed in the design and its impact on circuit performance will be given later. Here, to understand the general operating mechanism and for simplicity of the analysis, we choose l_g as one eighth of the guided wavelength at center frequency. For this length, the input impedance looking into the CPW line will have the same magnitude but a opposite sign when the right-end of the line is short-circuited and open-circuited with the ground respectively. The will greatly simplify the expressions for resonating frequencies. The loaded resonating frequency for the cavity can be written as:

$$f_e = \frac{1}{\sqrt{C\{(C-M) + \frac{2M*(L_p - M + L_b + Z_{cpw}/\omega)}{2M+(L_p - M + L_b + Z_{cpw}/\omega)}\}}} \tag{8.1}$$

Similarly, when a magnetic wall is inserted at the symmetry plane, the loaded resonating frequency for the cavity is:

$$f_m = \frac{1}{\sqrt{C\{(C-M) + \frac{2M*(L_p - M + L_b - Z_{cpw}/\omega)}{2M+(L_p - M + L_b - Z_{cpw}/\omega)}\}}} \tag{8.2}$$

If we keep $(L_p - M + L_b - Z_{cpw}/\omega) > 0$, since

$(L_p - M + L_b + Z_{cpw}/\omega) > (L_p - M + L_b - Z_{cpw}/\omega)$,

we can see $f_e < f_m$ and this indicates a capacitive coupling is achieved.

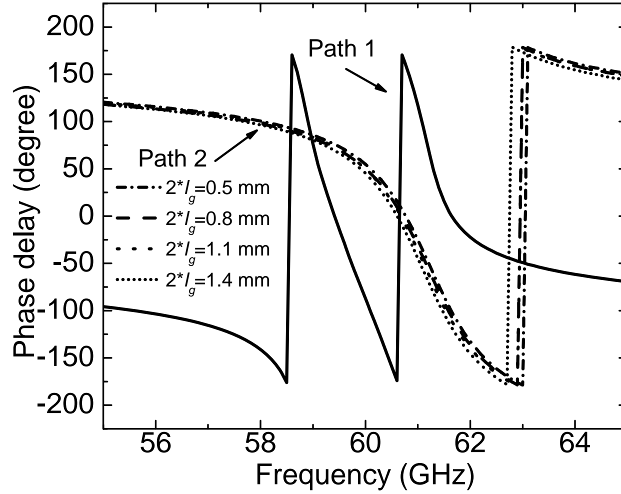


Figure 8.4: (Phase response from path 1(inductive-coupling path) and path 2 (cross-coupling path).

Another way to prove the existence of transmission-zeros is to study phase shift responses from path 1 and path 2 separately. If phase shifts with opposite signs are observed for two different paths, transmission cancellation is made possible. Phase shift from path 1 is simulated by blocking transmission between cavity 1 and 4. The response is plotted in Figure 8.4 (a). Phase shift of path 2 is studied by blocking transmission through cavity 2 and 3, plotted in Figure8.4 (b). The lengths of the CPW line are swept to demonstrate that cancellation is only effective within a certain range. As can be seen from Figure 8.4, phase shifts from two different paths are 180 degree apart from each other at certain frequencies below and above the resonance. So far, we have proven this cross-coupling scheme is capacitive. The magnitude of this capacitive coupling coefficient can be calculated using the following equation [39]:

$$m_{14} = \frac{f_m^2 - f_e^2}{f_m^2 + f_e^2} \tag{8.3}$$

Full-wave simulations have found that m_{14} is affected by the CPW length (2*l_g) and the offset from the center line (*y2* in Figure 8.7). The results are plotted in Figure8.5. It should be noted that m_{14} has a negative sign and only the magnitudes are shown in the figure. Parametric simulation results show that the variation is small regarding to 2*l_g and

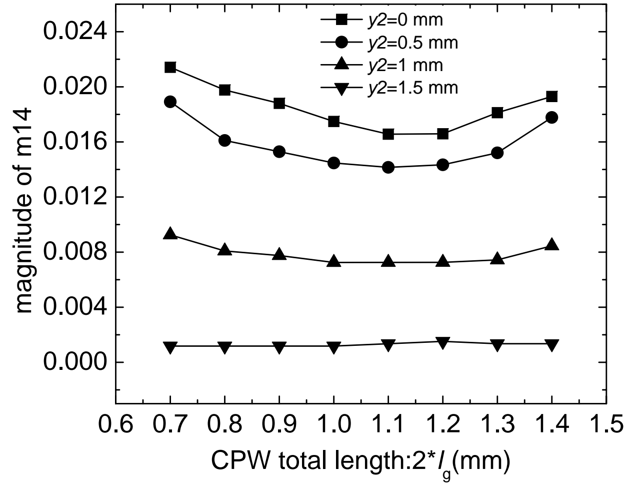


Figure 8.5: Impact of the CPW length and position on the magnitude of m_{14}.

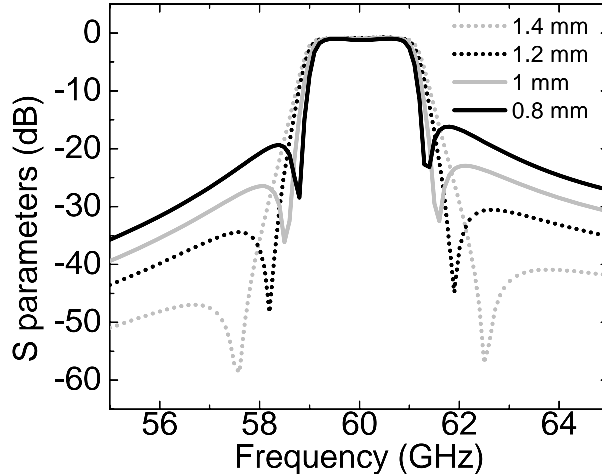


Figure 8.6: Tuning of transmission-zero positions by varying CPW positions ($y2$).

big for the offset *y2*. These curves can be used to tune the positions of transmission zeros. Transmission responses with different zero positions by tuning the positions of the CPW line are shown in Figure 8.6.

8.2.2 Transmission-zero filter design

Using the capacitive coupling described above, a 4-pole transmission-zero filter is designed. The center frequency is chosen as 60 GHz. The ripple band width is 1100 MHz. In-band return loss is greater than 25 dB.

The required filter response can be synthesized using the algorithm in [30], with the

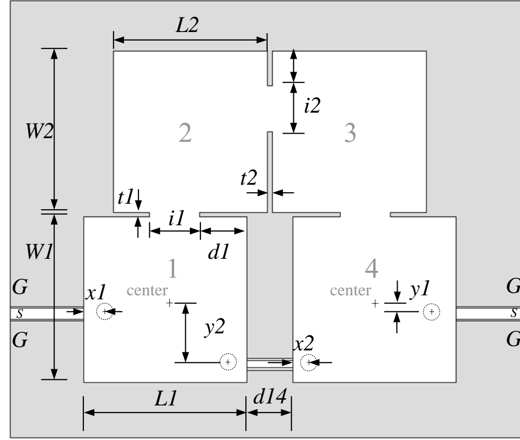


Figure 8.7: Dimensions of the 4-pole transmission-zero filter.

coupling matrix given as:

$$\begin{bmatrix} 0 & 1.132 & 0 & 0 & 0 & 0 \\ 1.132 & 0 & 0.962 & 0 & -0.287 & 0 \\ 0 & 0.962 & 0 & 0.866 & 0 & 0 \\ 0 & 0 & 0.866 & 0 & 0.962 & 0 \\ 0 & -0.287 & 0 & 0.962 & 0 & 1.132 \\ 0 & 0 & 0 & 0 & 1.132 & 0 \end{bmatrix}$$

These coupling coefficients are then normalized with the fractional bandwidth and transformed to iris dimensions using the design curve in Figure 7.6. The normalized negative coefficient is transformed to an appropriate CPW length and offset from the center line by using design curves in Figure 8.5.

Optimized solid-wall 4-pole transmission-zero filter dimensions are listed in Table 8.1, with legends shown in Figure 8.7. The structure is symmetric so there are only two sets of resonator dimensions. The solid walls are replaced by the pillar arrays. Simulation results after transforming are plotted together with responses from the ones synthesized from the specifications in Figure 8.8. In full wave simulations, transmission zeros are found at 58.9 and 61.1 GHz respectively. The return loss is larger than 25 dB within the ripple bandwidth. Four poles are located at 59.55, 59.75, 60.25, 60.55 GHz respectively.

Table 8.1: Optimized dimensions of 4-pole transmission zero filters (units: mm)

Dimensions	Value	Dimensions	Value
$W1$	3.6	$t1$	0.1
$W2$	3.5	$d1$	1.15
$L1$	3.6	$i1$	0.95
$L2$	3.4	$x1$	0.5
$d14$	0.9	$x2$	0.2
$t2$	0.1	$i2$	1
$d2$	0.6	$y1$	0
$i2$	1	$y2$	1.1

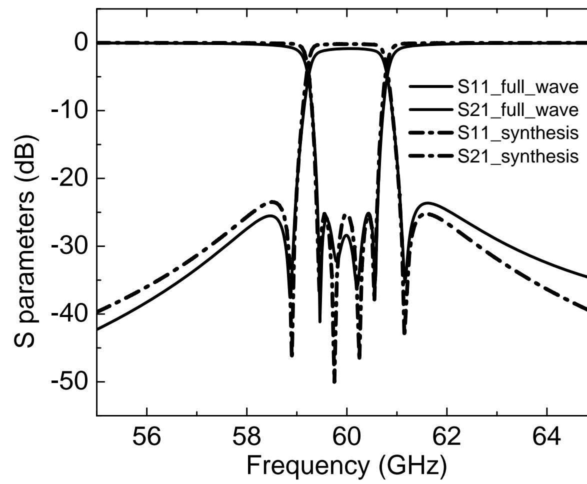


Figure 8.8: Filter response from matrix synthesis and from full-wave simulation.

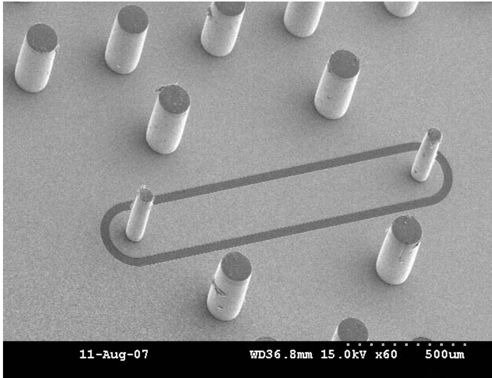


Figure 8.9: A SEM picture of the fabricated cross-coupling structure.

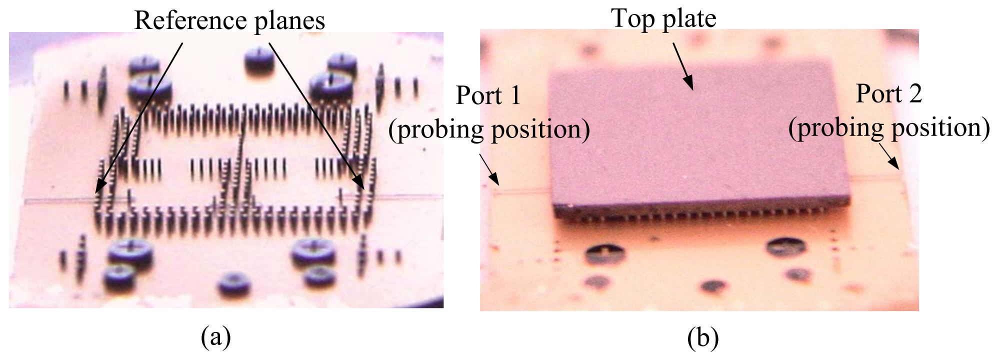


Figure 8.10: (a) The picture of transmission-zero filter before the top plate is attached.(b) The picture of final assembly (alignment posts removed for clarity of sidewalls).

8.2.3 Fabrication and measurement

The designed 4-pole transmission zero filter is fabricated using the similar approach. Figure 8.9 shows the SEM picture of the proposed capacitive coupling structure. Figure 8.10 shows the filter pictures before and after attaching top piece. Probing positions and reference planes are indicated in the figure. A similar measurement setup discussed in previous sections is used to characterize this filter. NIST Multical calibration sets the reference plane to the outer surface of the sidewalls. The measurement result shown in Figure 8.11 agrees well with the post-fab simulated response. Two transmission zeros are found at 58.7 GHz and 61.4 GHz respectively. A 2.45 dB insertion loss is observed for this 4-pole filter. Excellent insertion loss is contributed to elevating the filter into the air and elimination of the dielectric loss.

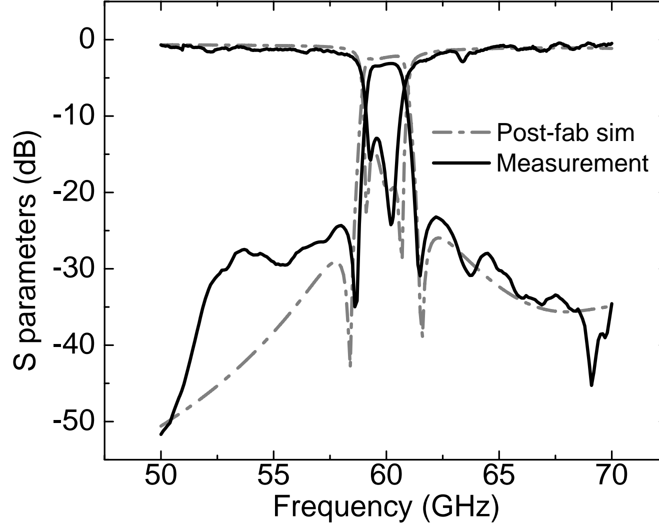


Figure 8.11: Measured response of the 4-pole transmission-zero filter .

8.3 A transmission-zero filter with direct source-loading coupling

This section presents a novel surface micromachined low-loss integrated cavity filter with a pair of transmission zeros using a simple source-load coupling scheme for emerging 60 GHz applications. The inter-cavity inductive coupling is realized through the use of pillar array iris, with the source-load capacitive coupling achieved with integrated coplanar waveguide lines. This combination of couplings creates a pair of transmission zeros to help achieve better selectivity. A measured insertion losses as low as 1.92 dB, along with a pair of transmission zeros, has been observed at 60 GHz.

To enhance the stopband rejection performance, transmission zero synthesis techniques, have been also introduced in the design of the integrated waveguide filters[30][65]. These include introducing cross coupling between non-adjacent cavities, dual-mode operations, non-resonating nodes and source-load coupling. Among them, the source-load coupling scheme can create two transmission zeros by using only two cavities that lead to a more compact design. Its synthesis methods, along with different implementation schemes, have been reported in [3][78].

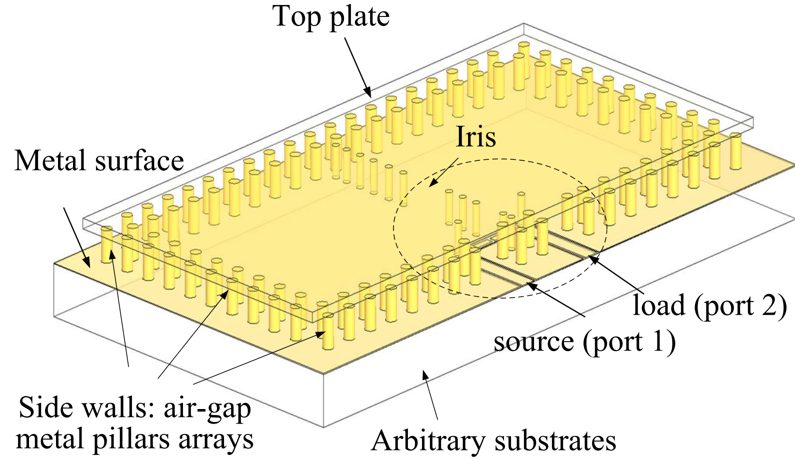


Figure 8.12: Concept drawing of the proposed filter structure (detailed structures in the dashed circle is shown in Figure 8.13).

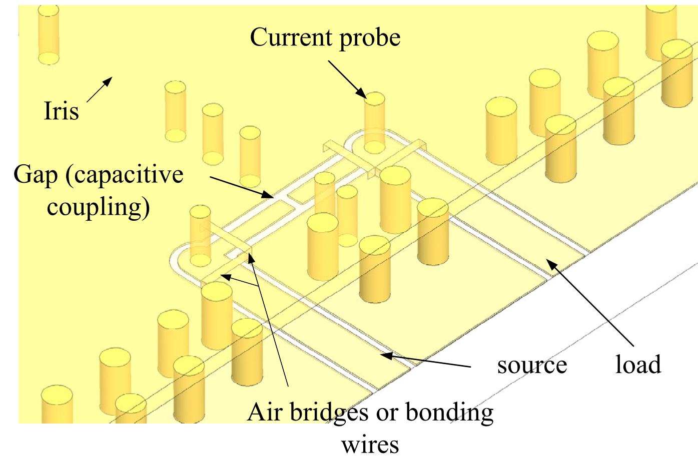


Figure 8.13: Feeding and coupling schemes for the proposed filter.

8.3.1 Design and optimization

Figure 8.12 shows the filter structure. Figure 8.13 shows the detail of source-loading coupling . In Figure 8.12 , the top plate is shown as a transparent frame to reveal the details inside.

The equivalent circuit model of the source-load direct coupling two-pole transmission zero filter is shown in Figure 8.14. The circuit consists of two shunt LC resonators representing two cavities, a mutual coupling inductor L_m representing the inductive coupling between two cavities, a capacitor C_c connecting the source and the load to provide an electrical coupling that has an opposite sign compared with the inductive coupling, and two

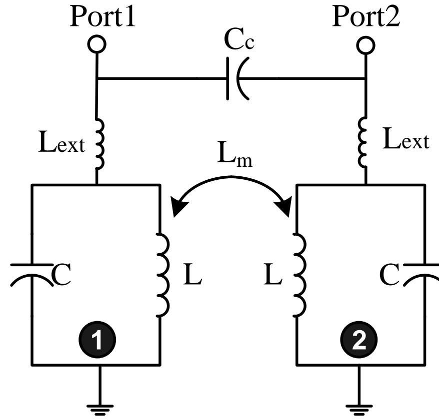


Figure 8.14: Equivalent circuit model for the proposed source-loading coupling 2-pole filter

inductors L_{ext} that represent the external coupling current probes. A pair of transmission zeros out of the passband can be created when there is a 180° phase difference between two paths($Path1$: source → capacitor→load; $Path2$: source→current probe→cavity 1→iris coupling→ cavity 2→current probe→load). Details of the phase delay calculations can be found in [42].

The inductive coupling between the two cavities is implemented by the pillar iris.The capacitive coupling is realized in a planar form instead, using a gap formed by two CPW stubs as shown in Figure 8.13. To form the CPW gap between the source and the load, the spacing between two pillars has to be increased to allow sufficient space for CPW routing. The impact on the inductive coupling between the cavities, from this increased pillar spacing, has been taken into account in the full-wave simulations. The locations of the transmission zeros can be controlled by varying the gap; it essentially changes the coupling capacitance between the source and the load. Simulated filter responses versus the gap are plotted in Figure 8.15. As can be seen, the smaller the gap, the closer the transmission zeros from the passband. A smaller gap means a larger coupling capacitance, leading to a closer-to-passband transmission cancellation from the two different paths.

The external coupling is realized through a current probe connected to a CPW line. The probe contacts the top wall of the cavity and excites it using magnetic coupling. The external coupling level is controlled by the probe position. The relationship between the

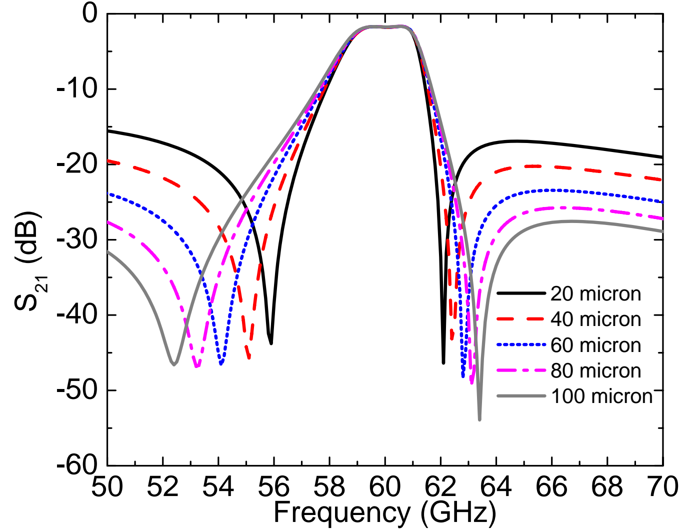


Figure 8.15: S_{21} as the function of the CPW gap in source-load capacitive coupling

external quality factor Q_{ext} and the physical positions of the feeding probe can be found in [55]. The inter-cavity coupling level is controlled by the iris opening and its design curve can be found in any waveguide filter design handbook.

A prototype filter is designed for proof of concept in this research. The design center frequency is set as 60 GHz and the 3-dB fractional bandwidth is chosen as 1 GHz. A solid wall version is designed first to reduce the full-wave simulation time and then transformed into pillar arrays.

The inductive iris is formed by only one row of pillars since it will not introduce leakage to the outside of the cavity. Different diameters are chosen for sidewall pillars and inter-cavity pillars to effectively block EM-wave leakage and reduce the chip real estate.

To facilitate on-wafer probe measurement, CPW lines from the source and the load (as shown in Figure 8.13) are bent and carefully routed to minimize parasitic effects.

Figure 8.16 shows the full wave simulated performances using Ansoft HFSS 10.1 for the proposed filter, with the dimensions shown in Table 8.2. A pass-band insertion loss of 1.7 dB is found in the simulations, taking into account the metal loss (with finite metal roughness) and radiation leakage. Two transmission zeros are located at 58.6 GHz and 60.9 GHz respectively.

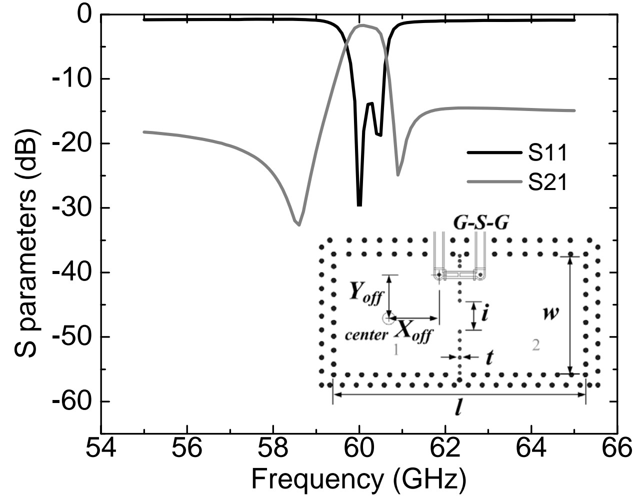


Figure 8.16: Optimized filter response and illustration of physical dimensions

Table 8.2: Optimized filter dimensions. (units: mm)

Dimensions	Value	Dimensions	Value
l	7.3	i	0.8
w	3.5	t	0.1
X_{off}	1.05	gap	0.05
Y_{off}	1.6	$pitch$	0.44
$diameter$	0.14		

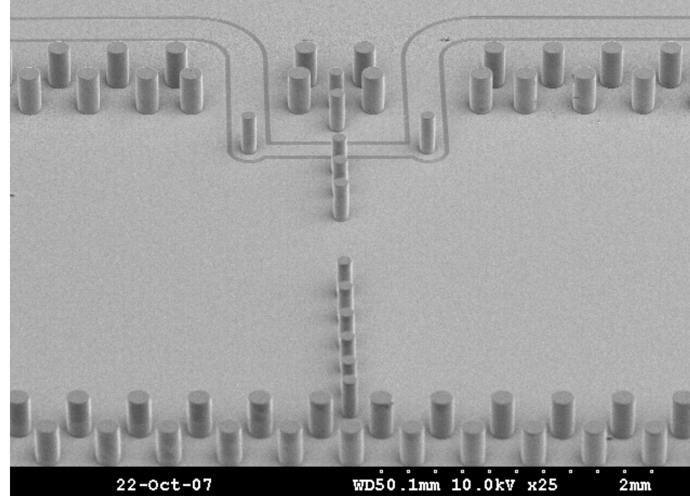


Figure 8.17: SEM pictures of the source-load coupling filter, showing cavities, iris and feeding lines

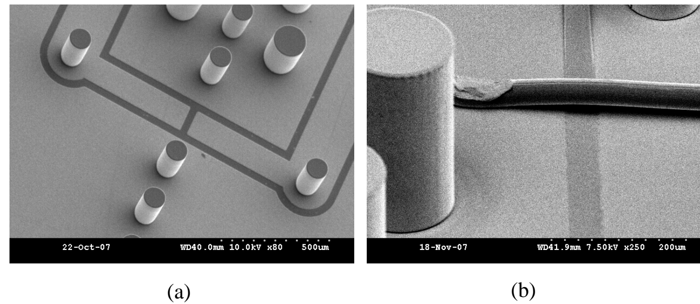


Figure 8.18: SEM pictures of the source-load coupling filter (a) capacitive coupling gap (b)a bonding wire

8.3.2 Fabrication and measurement

The same process step as the one used for other filters is used to fabricate this filter. A piece of silicon wafer was metallized to be used as a top plate of the cavity and bonded with the pillars using silver paste. Figure 8.17 shows cavity/iris part of a fabricated sample before assembly.

Figure8.18 (a) shows the capacitive coupling gap between the source and the load. Pillars with a smaller diameter are used for inductive iris and feeding probes, while larger ones for the sidewall. Al/Si wedge bonding wires are used to connect the CPW grounds preventing parasitic slot-mode radiation. An SEM picture of a bonding wire is shown in Figure8.18 (b).

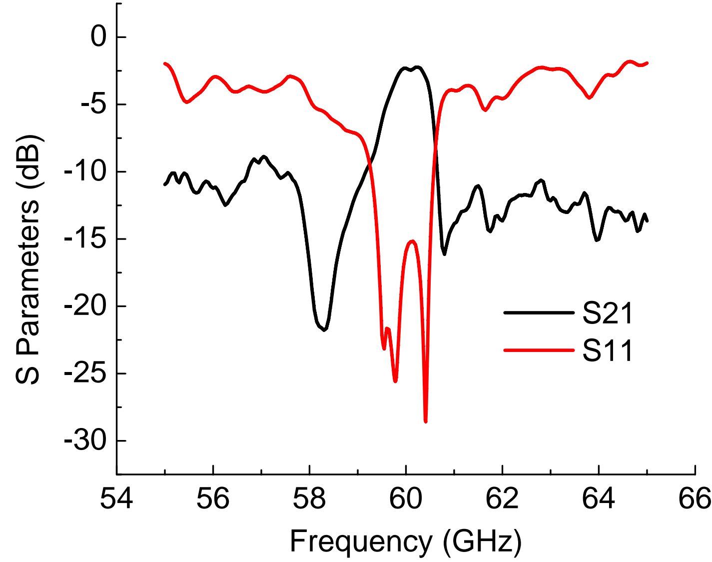


Figure 8.19: Measurement results of the fabricated source-load coupling filter

Table 8.3: Comparison of simulated and measured responses (units: GHz)

	center	3-dB BW	pole 1	pole 2	zero 1	zero 2
sim	60.14	1.0	60	60.5	58.6	60.9
meas	60.04	1.1	59.8	60.4	58.3	60.8

The fabricated sample on a glass substrate is measured by an Agilent 8510XF vector network analyzer station connected with GSG probes of a 250 μm pitch. The reference plane was set to the outer surface of the sidewall. The measurement results are plotted in Figure 8.19.

Good agreement between simulation and measurement is observed, as shown in Table 8.3. A slight frequency shift (less than 0.17 %) to a lower band (from 60.14 GHz to 60.04 GHz) was observed and might be explained by numerical errors in the simulations. Two transmission zeros are observed at 58.3 and 60.8 GHz. A 1.92 dB insertion loss and a return loss greater than 15 dB were achieved for the fabricated prototype.

8.4 Discussions

The polymer-core conductor surface micromachining technology demonstrates excellent agreement between simulation and measurement results since photolithography is used to

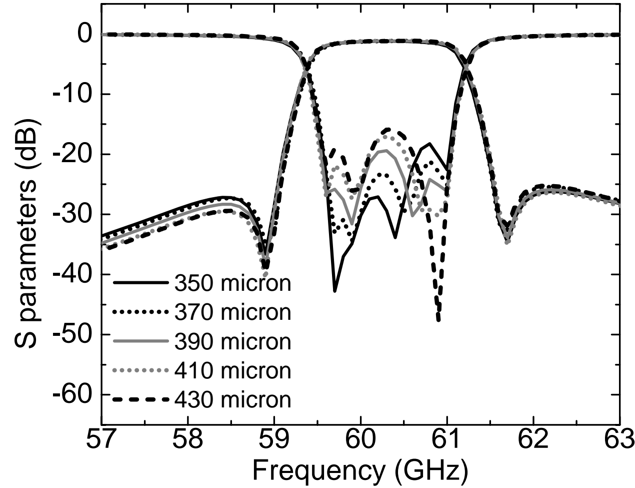


Figure 8.20: Simulated responses for the filter in Figure 8.2 considering pillar height variation.

control pillar positions and dimensions. However, discrepancies are still observed after the prototypes are fabricated. Although disagreement between theoretical predictions and scientific experiments are inevitable, knowledge of sources that contribute to it will help minimize it.

In this technology, besides for numerical errors from EM-simulation tools, two major variations explain for the disagreement. One is the height of the pillar and the other is CPW dimension. The height of the pillar is affected by the amount of the epoxy used, the wafer size, the accurate spinning speed and the exact viscosity of the epoxy. The actual coating thickness can only approach the desired one during our prototype building effort. A further process optimization is required for a massive production.

Taking the four-pole transmission-zero filter as an example, Figure 8.20 shows how the pillar height variation affects the filter response. The zeros' positions keep almost unchanged but poles' locations are shifted or merged together. Another important factor is the variation of CPW dimensions. CPW dimensions variation is possible during etching and electroplating. It consequently changes the characteristic impedance of the line and thus affect filter performance. Figure 8.21 shows how CPW line impedance affects filter response. As can be observed, it directly affects the impedance matching. Both factors contribute to the mismatch between simulations and measurements.

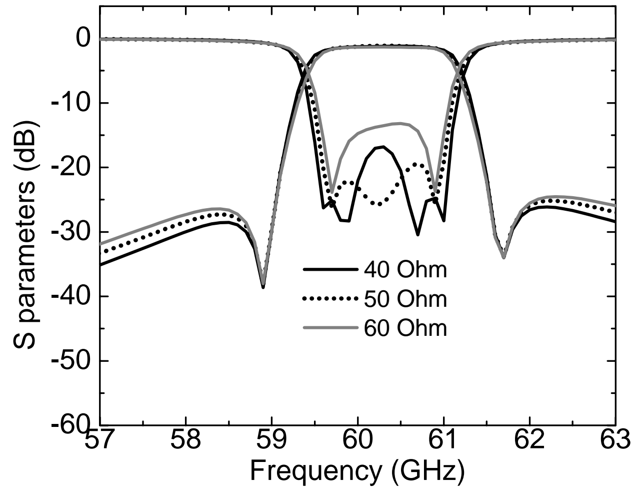


Figure 8.21: Simulated responses for the filter in Figure 8.2 considering CPW line impedance variation.

8.5 Chapter summary

In this chapter, two high-performance transmission-zero filters are implemented using polymer-core conductor surface micromachining technologies. By combining 3-D structures and planar transmission lines, novel coupling structures can be designed to create transmission zeros. Simulation and measurement results show that polymer-core conductor surface micromachining is a powerful technology for the integration of high-performance transmission-zero filters.

CHAPTER IX

INTEGRATION OF MICROMACHINED COMPONENTS INTO A FULLY-DUPLEX TRANSCEIVER FRONT-END

In previous chapters, we have presented the development of various individual transceiver-frontend components, including multiple antennas and filters. Experimental results have demonstrated significant loss reduction compared with traditional approach. Furthermore, a simple planar input/output interface makes it easy to integrate other components.

In this chapter, the thick-film surface micromachining technology is used for whole transceiver front-end integration.

A transceiver is a device that has two sub-devices - a transmitter and a receiver, and contains some modules that are common between the transmitting and receiving functions. Usually, for a specific wireless application that has a designated frequency band, the frequency for the transmitting channel is very close to the one of the receiving channel. To avoid leakage from transmitting to receiving, a good isolation is required for the duplexer. To cover both transmitting and receiving channels, a relatively broadband antenna is also required.

Shown in Figure 9.1 is a common transceiver front-end architecture. We report our experimental results for integrated modules in the blue shadowed box and the green box, respectively, in this chapter.

For 60 GHz applications, there are quite a few great results reported for individual components [6][41]. Many chip-level integration designs using the state-of-art semiconductor technologies have been also reported [63][51]. However, little research is directly dealing with package-level integration. IBM research demonstrated a fully integrated chipset using silicon-based technologies [21]. In addition to the IC development, IBM also developed an antenna integration and packaging scheme [59][59]. Essentially, their transmitter and receiver were integrated using a chip-on-board method. Researchers from Georgia Tech

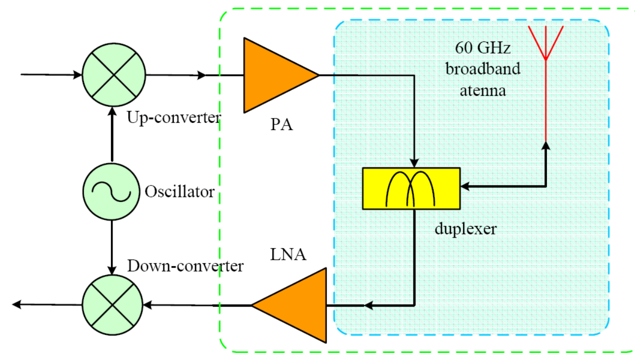


Figure 9.1: Diagram of a common transceiver front-end

have successfully established a 60 GHz test-bed that supports 15 Gbps data transfer speed at a distance of 1 m. It uses FR4-LCP multilayer substrates for antenna integration and packaging [66].

However, these existing approaches all use different platforms for active circuits and passive components. This is resulted from different substrate requirements for antenna and other modules. Furthermore, they only demonstrated a single transmitter or receiver, other than a fully-duplex transceiver.

In our research, a micromachined transceiver front-end capable of duplexing operation was developed and characterized. In our approach, this front-end consists of a micromachined horn antenna used both for transmitting and receiving, a cavity-based duplexer, a low-noise amplifier chip and a power amplifier chip. Compared with other existing integration approaches, this is a substrate-independent solution which is capable of integrating both passive components and active circuits on the same wafer. The best scenario to demonstrate our proposed integration method is to directly integrate all passive components on top of a wafer that has already had active circuitry in it. However, the development of 60 GHz IC chipset is beyond our expertise and scope of this dissertation. Design of 60 GHz chipset is also premature and most stays at the research stage.

Alternatively, we purchased 60 GHz amplifier dies from Hittite and use bonding-wires to inter-connect to micromachined passive parts The objective is to demonstrate feasibility of using this thick-film surface micromachining technology as a platform for millimeter-wave

system integration. The proposed transceiver structure is shown in Figure 9.2.

An air transmission test was performed to verify the transceiver's functionality.

9.1 System planning

For transceiver integration, our objective is to integrate amplifiers, a duplexer and a horn antenna onto a 1 inch by 1.5 inch glass wafer.

Our system development procedure is: first, an appropriate topology for system and suitable forms for individual component is chosen. Reasonable specifications are assumed for individual components. Then each individual component is optimized to meet these specifications. Finally, we come back to interconnect all components together and perform final tuning. If any individual component brings up any issue, we modify our system design and revisit the necessary individual design.

9.1.1 Choosing appropriate topology

To make the on-wafer air transmission test possible, an end-fire radiation pattern is required for the antenna used in the transceiver. In a real product, both broadside and end-fire radiation pattern are acceptable since the millimeter wave signal is down-converted to the baseband and demodulated to the digital processing module. In that scenario, the input signal to the transceiver front-end is directly provided by chips in the same package and no external connectors are required; the transceiver can be oriented to any direction to assure maximum power delivered to the receiver via air. However, in our prototype development, since we must connect the transceiver front-end to the test equipment that can only provide coaxial or on-wafer probing interface, we have to put certain restrains for the selection of the antenna for integration.

In 60 GHz, the size of an antenna is several millimeters. Introducing a bulky connector that is on the same physical scale will greatly interfere the antenna performance and thus not a favorable choice here. An on-wafer test is preferred to minimize this interference.

A broadband and high gain antenna is very important for this transceiver integration. This is because EM wave propagation attenuation is very high at 60 GHz due to O_2 absorption. A high gain antenna has to be used both for transmission and receiving to increase

received power presented to a low-noise receiver. High data-rate wireless transmission is the major attraction of 60 GHz. High data-rate implies that a broadband antenna has to be used to cover the whole interested band. It is not only broadband for impedance matching, but also for constant radiation pattern. A micromachined V-band horn discussed in [54] is an ideal candidate for this purpose. However, it needs modification when it is used in the system integration.

First, the electrical performance of a horn antenna is easily affected by the size of ground and the relative position of the horn when it is integrated on top of the wafer. The out-going wave can get diffraction from the wafer edge and reflection from the finite-size ground. Our design philosophy here is to be aware of and utilize these imperfect boundary conditions, instead of neglecting or avoiding them.

More specifically, during the development of the stand-alone micromachined V-band horn antenna, we found that the parasitic metallization on the substrate and from the testing fixture could actually greatly affect its radiation pattern, as well as return loss measurement results. This is mainly because of the radiation beam diffraction from the metal surface.

Secondly, another practical concern is the physical size. As a stand-alone components, the size of the V-band horn discussed in the previous chapter is acceptable when performance is the major concern. However, there is only a limited real-estate on the substrate that can be reserved for horn integration. Miniaturization is certainly a concern, however, the major concern here is that it is challenging to achieve a large area of uniformity for SU-8 coating in our process. As discussed earlier, a small tilt angle of the wafer will introduce a large pillar height difference at the two ends when the wafer is big. After reserving enough space for other components, we leave the rest of the wafer for horn integration.

A further practical consideration for the horn is the opening and the sidewall can not be too close to the wafer edge. This is because SU-8 coating has a curved surface at the edge due to the surface tension. The height of SU-8 gradually decreases to near-zero on the edge. Pillars close to this region can not make good contact with other layers of the horn.

A strip of 6 mm width is used as a margin between the outermost SU-8 pillar for the

horn sidewall and the wafer edge. Instead of neglecting the impact from this strip, we actually include this part for optimization of the horn performance. Different schemes are considered and compared, including EBG pattern, bare wafer surface and metallization. Finally, continuous metallization is chosen since it can boost maximum directivity and tilt the main radiation beam to the upper space.

Optimization of the horn is given in below sections. The final horn length is chosen to be 14 mm including a back-short section used in the CPW-waveguide transition. Its H-plane cut has a width of 12 mm. This also leaves around 6 mm margin on each side of the sidewall since the wafer width is 25.4 mm.

As for the duplexer, two direct-fed two-pole filters are placed in parallel. To get the good isolation, a T-junction is also incorporated right after the two filters. More design details are given in the following sections. Here, we need to know its total footprint is 12.7 mm by 10 mm.

The amplifiers used in the integration is commercial product. It is based on GaAs technology. To minimize the parasitic effects, bare dies are used instead of packaged chips. The chip area is less than 2 mm by 2mm. However, to integrate with CPW-fed front-end components fabricated using surface micromachining technologies, wire-bonding is required to carry mm-wave signals from pads on the chip die to CPW lines. To minimize mismatch between chip dies and CPW lines on the substrate, a tapering bonding layout is designed for this transition. This consumes another 3-4 mm length of the substrate.

So totally a 12 mm by 30 mm substrate has to be reserved for these above components. Adding a couple of millimeters margin on every side to make sure SU-8 thickness uniformity can be guaranteed, we decide to integrate this whole transceiver front-end on a 1 inch by 1.5 inch substrate.

Another important aspect of system planning is choosing an appropriate height for pillars. The higher the pillars, the higher the quality factor of the cavity. This leads to an even-narrower band design for two filters of the duplexer. It gets easier to put two bands closer to each other without lowering the isolation between two channels. The total bandwidth occupied by two channels is reduced and this will lower the bandwidth

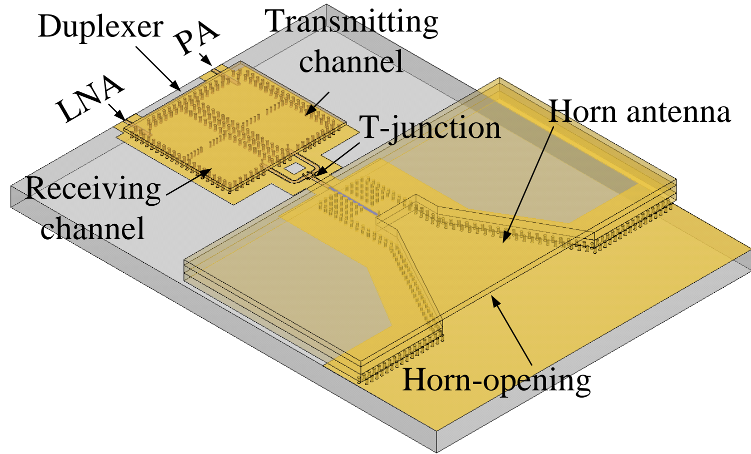


Figure 9.2: Schematic of the transceiver front-end integration.

requirements for amplifiers and antennas to cover both bands.

At the same time, a higher feeding probe for our proposed micromachined horn leads to a higher operating bandwidth.

In general, from the view of circuit performances, a thicker SU-8 coating, equivalently a higher pillar profile is preferred. However, to ensure mechanical robustness and keep a good SU-8 pillar profile, a lower pillar pattern is more fabrication-friendly. With all of the above concern, a 350 micron SU-8 coating is chosen.

9.2 V-band duplexer development

A duplexer is a key component for a transceiver front-end. This is because the transmitting channel and the receiving channel shares one antenna. In other words, the antenna connects the transmitting and the receiving path. Because of this common element, leakage from one channel to the other is become possible. Usually, a power amplifier is the last stage for the transmitting path, its output power can be leaked into receiving path through the common antenna if the antenna can not provide ideal isolation between two channels. Since the output power level is high for the power amplifier, even a small amount of power can saturate the low-noise amplifier that is the first stage on the receiving path. If the low-noise amplifier has a large dynamic range, saturation may not be a problem, but the leakage from the transmitting path is still a large interference presented to the receiving path.

A duplexer is a three-port device that can provide enough isolation between transmitting and receiving paths. Meanwhile, it needs to filter out undesired out-of-band signal for both channels. This requires a high out-of-band rejection. Very straightforwardly, a duplexer can be realized by putting two band-pass filters in parallel. The center frequency of one filter is tuned for transmitting and the other for receiving. Usually, the transmitting and receiving channels fall in the same band and are very close to each other; this makes the duplexer design very challenging since it is hard for one channel to get enough rejection of interference from the other channel.

To get enough out-of-band rejection, filters with very sharp roll-off skirts are required for duplexer design. For a planar-type filter, this can be realized either increasing the order of the filter, leading to a large number of cascaded resonators, or using very complicated advanced filter design techniques such as introducing multiple transmission zeros out of the pass-band. Still, the out-of-band rejection is quite limited since the unloaded quality factor of a planar resonator is not high enough and it is very challenging to get a very narrow band design.

Another important requirement for a duplexer is low insertion loss for both channels. In the receiving path, a low insertion loss means less power is consumed in the receiving filter and thus more power can be delivered into the input of the low noise amplifier. This can improve the overall receiver sensitivity. In the transmitting path, a low insertion loss means less power is required from the output of the power amplifier for the same amount of power delivered into the common antenna. This helps save the overall power consumption of the transceiver. For a planar-type filter, this requirement can only be met by using a substrate with a low loss tangent.

That is why we want to explore the possibility of using integrated waveguide cavity for duplexer design. As we observed earlier in our work, a micromachined cavity has a much higher unloaded quality factor, compared with its planar counterpart. This makes possible to design a narrow-band filter with a very low insertion loss using just a small number of resonators but still providing excellent out-of-band rejection.

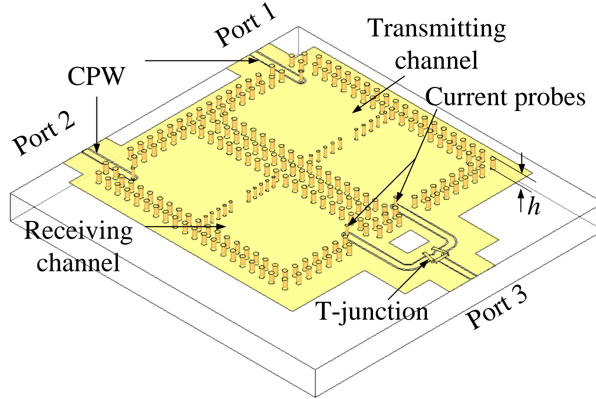


Figure 9.3: Schematic of the micromachined duplexer(top cover not shown for clarity).

In this section, the design techniques and experimental results for a surface micromachined duplexer are documented in details. Both simulation and measurement results demonstrated the advantages brought to duplexer design by the surface micromachining technology.

9.2.1 filter design for each channel

As shown in Figure 9.3, the duplexer we have developed using the surface micromachining technology consists of two two-pole filters and a T-junction that connects the two filters. Port 1 will be the output of the power amplifier and Port 2 be the input of the LNA; while Port 3 is reserved for the common antenna.

The two-pole filter uses the one with the direct probe-feeding we described in the previous chapter. Compared with the one with a CPW-waveguide transition, the direct probe-feeding schemes gives a more compact and low loss design.

The transceiver front-end discussed in this chapter are to be used both in a base-station and for a user terminal. To do the transmission test, for the transceiver front-end in the user terminal, the lower frequency channel is reserved for transmitting and the upper channel for receiving. This is because a user terminal is usually battery-powered and thus more power-stringent than a base-station. Propagation loss increases with the frequency and thus the transmitting channel of a user-terminal prefers lower frequency. After the frequency allocation scheme is set for the transceiver in a user-terminal, the one in a base-station just

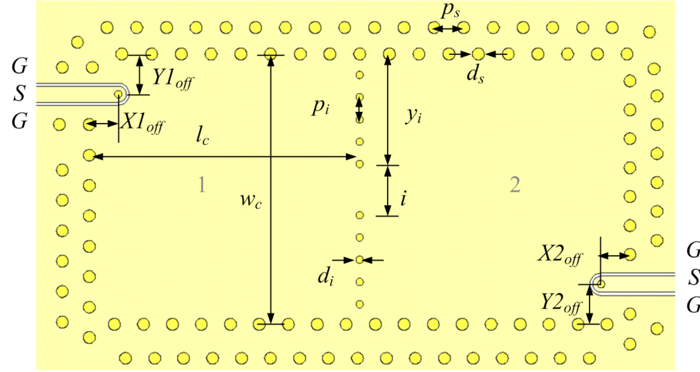


Figure 9.4: Dimension illustration of the micromachined duplexer filters.

Table 9.1: Optimized dimensions of 4-pole transmission zero filters (units:mm)

Design Parameters	Transmitting channel	Receiving channel
cavity length (l_c)	3.64	3.64
cavity width (w_c)	3.64	3.42
iris position (y_i)	1.48	1.35
iris length (i)	0.69	0.74
probe position ($X1_{off}$)	0.54	0.52
probe position ($Y1_{off}$)	0.35	0.39
probe position ($X2_{off}$)	0.59	0.50
probe position ($Y2_{off}$)	0.39	0.39

simply switches the transmitting/receiving frequency.

In this design, the center frequencies of two channels are picked as 59.1 and 61.1 GHz respectively. The 3-dB bandwidth is chosen as 1 GHz for both channels.

Following the same procedure described in the previous chapter, two two-pole filters are designed. First, a solid-wall version is designed to reduce the simulation time. Then, it is converted to pillar array version to facilitate fabrication. FEM-based full wave simulation using Ansoft HFSS is performed to optimize the final dimensions and positions of the pillars.

Table 9.1 lists the optimized parameters for two filters.

Figure 9.4 shows the simulation results for two filters.

Table lists the optimized parameters for two filters. Physical meanings of all parameters are provided in Figure 9.5.

Figure 9.5 shows the simulation results for two filters.

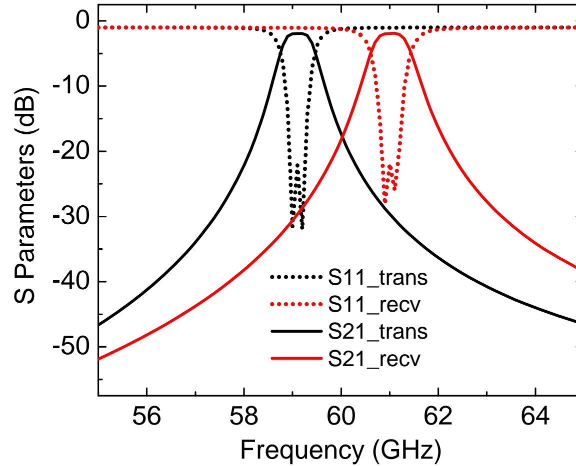


Figure 9.5: Simulation results of duplexer filters

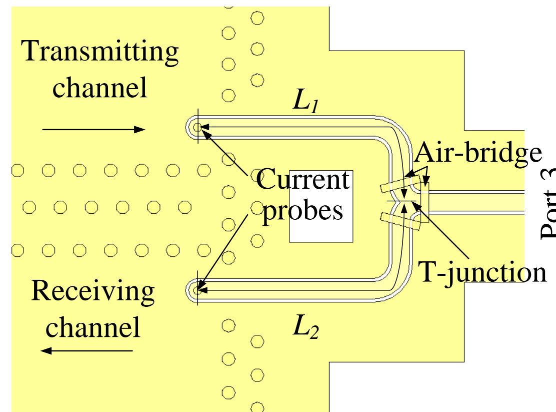


Figure 9.6: Schematic of a T-junction.

As can be seen, a 1.92 dB insertion loss and larger than 20 dB return loss are observed for both filters.

9.2.2 T-junction design and duplexer optimization

To achieve a high-level of channel-to-channel isolation, the design of the CPW line T-junction is critical for proper operation. Figure plots the T-junction we designed in our research. An appropriate length of L1 is chosen to present an open circuit condition looking into the channel 1 at the T-junction at the resonating frequency of the channel 2. Similarly, the length of L2 is adjusted to transform the output impedance of channel 2 into an open circuit. Mathematically, this leads to the following design equation:

Table 9.2: Optimized simulation results for a duplexer

Optimized results	Transmitting channel	Receiving channel
matching	> 15 dB	> 15 dB
insertion loss	3.05 dB	3.14 dB
isolation	> 35 dB	> 35 dB

$$L_1 \approx \frac{n\lambda_{g2}}{2}, L_2 \approx \frac{n\lambda_{g1}}{2}, \tag{9.1}$$

where λ_{g1} and λ_{g2} are effective resonant wavelengths of the channel 1 and channel 2, respectively. This equation only gives the initial design value to choose the length of each arm in T-junction. To considering discontinuity and bending effects of CPW lines, optimization is performed to adjust the line lengths.

There are many possible combinations of the line lengths. To reduce the overall size of the duplexer, the lengths should be minimized while still providing enough space for line routing.

Based on this principle, the line lengths are first chosen by using Agilent-ADS schematic simulations. A data box contains the full-wave simulation result of the duplexer is used in this simulation. After line lengths are determined by this way, a full-wave simulation by Ansoft HFSS is performed to extract the scattering matrix of the T-junction. An ADS schematic simulation is performed at this time to verify the design by using data boxes to represent two filters and T-junction respectively. Finally, a full-wave simulation is performed for final adjustment before the final layout is generated for fabrication. The final optimized values of L_1 and L_2 are 3.34 mm and 3.50 mm, respectively.

Simulation results of an optimized duplexer design are plotted together with measurement results and will be discussed in detail in next subsection. Table 9.2summarizes the simulated duplexer performance.

9.2.3 Fabrication and measurement

A prototype of this duplexer is fabricated using the polymer-core conductor approach. Figure 9.7 shows an SEM picture of the fabricated sample. To prevent slot mode radiation

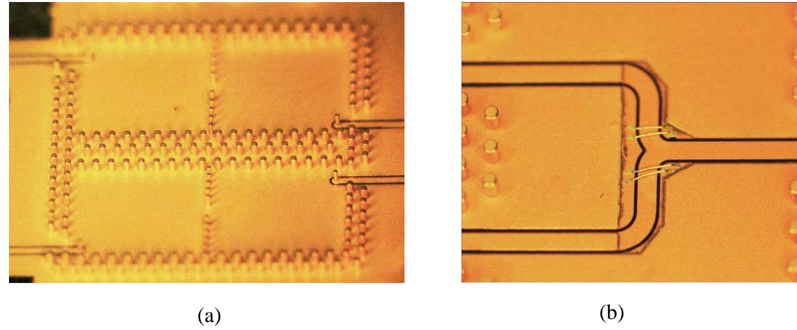


Figure 9.7: Micro-images of the fabricated duplexer.

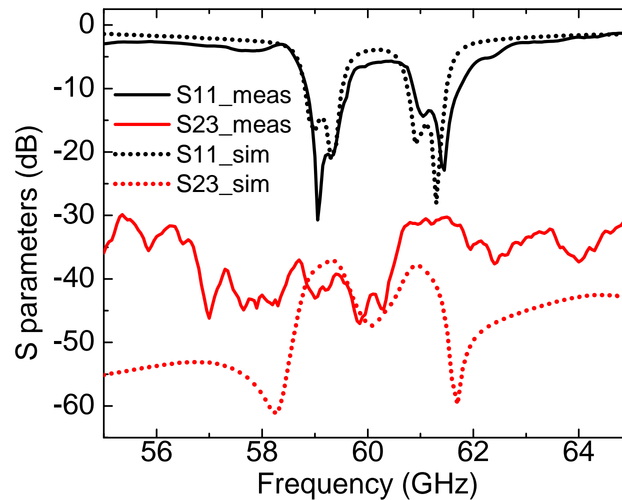


Figure 9.8: Simulated and measured duplexer performance: impedance matching at the power combining port, and isolation between two channels.

from the T-junction, three pieces of ground are connected together by bonding wires. The measured scattering parameters of this duplexer is taken by a 8510 XF network analyzer. Since this is a three port device, the unused port is terminated by a broadband coaxial termination using a positioner. The coplanar probe that is terminated with the coaxial impedance. To facilitate the probe orientation during measurement, three sets of duplexer with different CPW pad orientation are fabricated.

Figures 9.8-9.10 show the measured scattering parameters of the duplexer. Insertion loss for channel 1 and channel 2 is 3.58 dB and 3.60 dB, respectively, slightly larger than simulation prediction. This might be explained by metal surface roughness which is not included in full-wave simulation. Center frequencies of two channels both shift upwards

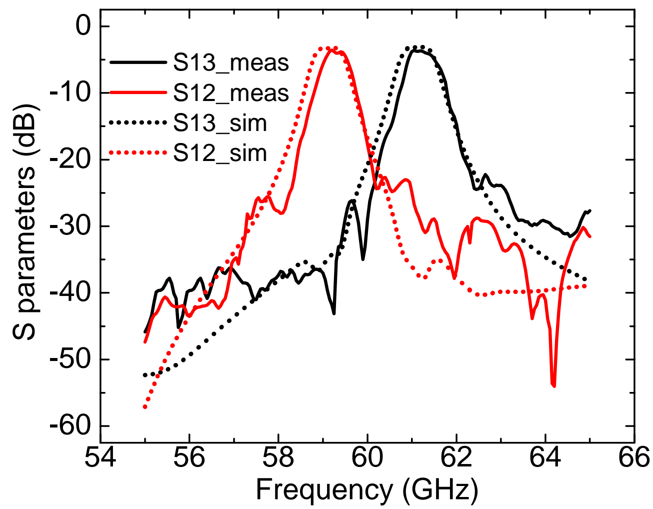


Figure 9.9: Simulated and measured duplexer performance: insertion loss for each channel

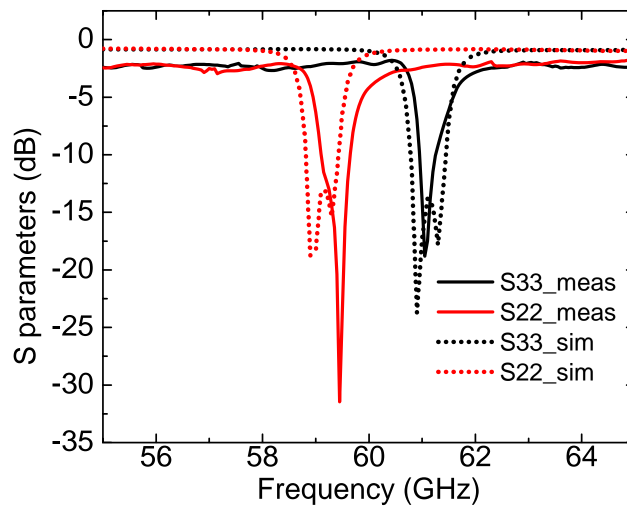


Figure 9.10: Simulated and measured duplexer performance: impedance matching at power dividing ports

approximately 0.5 %. Measured return loss is larger than 15 dB for all three ports. Isolation is larger than 30 dB across the whole band. In general, good agreement between simulation and measurement has been observed; experimental data shows that a cavity filter based duplexer can meet system integration requirements. Discrepancy comes from simulation error of numerical tools and non-ideal fabrication conditions.

9.3 Antenna development for integration

9.3.1 horn optimized for front-end integration

The same horn structure as the one discussed in [54] is re-optimized in this integration. This horn is composed of three parts: a CPW-connected vertical current probe for feeding, a rectangular waveguide with a height of 0.35 mm to help transit the CPW mode to the waveguide mode, and a H-plane linearly flared horn. A linear flare in the E-plane is hard to realize in this technology, so a simple E-plane step from 0.35 mm -high waveguide to 1.4 mm -high horn opening is used instead. The CPW-connected vertical current probe directly contacts the rectangular waveguide on top of the substrate. Four rows of pillars are used to terminate the back-short to ensure there is no direct wave leakage into the backside. Two rows of pillars with staggered positions are used as the waveguide sidewalls, as well as lower part of the horn sidewall. Two 525 μm-thick identical metalized silicon piece to build the horn's upper part are stacked on top of the pillar arrays. One solid metalized silicon piece is used as the horn's top wall.

The optimized horn is 14 mm long and 12 mm wide, with a backshort of 0.9 mm long and 3.2 mm wide. The H-plane flare angle is 58 degree. The E-plane step is located 1.3 mm after the vertical probe. The overall height of this horn is 1.4 mm.

The simulated return loss for the optimized horn antenna is plotted in Figure 9.11 with the projected E-plane and H-plane radiation pattern plotted in the same figure. As can be seen, since the horn flare is only on the H-plane, the H-plane beam width is much narrower than the E-plane one. The maximum gain angle is tilted into the upper space on the E-plane, resulted from wave reflection from the 6 mm metal strip extended from the bottom wall of the horn.

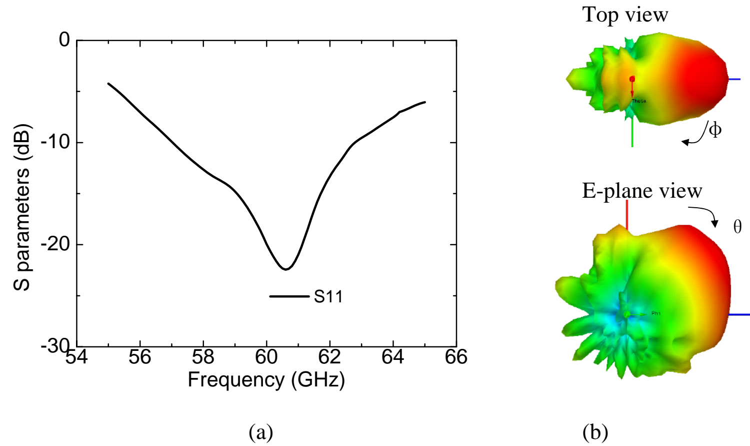


Figure 9.11: Simulated horn performance.

Larger than 10 dB return loss is observed from 57 GHz to 63 GHz. The maximum gain is 11.5 dBi and the front-to-back ratio is 13 dB. The E-plane 3-dB beamwidth is 50 degree and the H-plane one is 30 degree.

A picture of a fabricated horn lower part is shown in Figure 9.12.

More design details are provided in the previous chapter and not repeated here.

9.4 Duplexer/Antenna integration

Integration of the duplexer and the antenna is quite straightforward because their I/O interfaces are both CPWs. To prevent damaging sidewall pillars during wire-bonding on the T-junction zone, there should be a minimum length for the CPW section between T-junction and horn backshort. In our integration, a length of 1.5 mm is chosen.

The simulated and measured scattering parameters of the two-port integrated module are shown in Figure 9.13. The measured isolation is better than 26 dB across the frequency range of interest. The measured return loss is better than -10 dB for both channels, indicating power transmission and receiving are enabled in these two channels. Overall, a good agreement between the simulations and measurements can be observed.

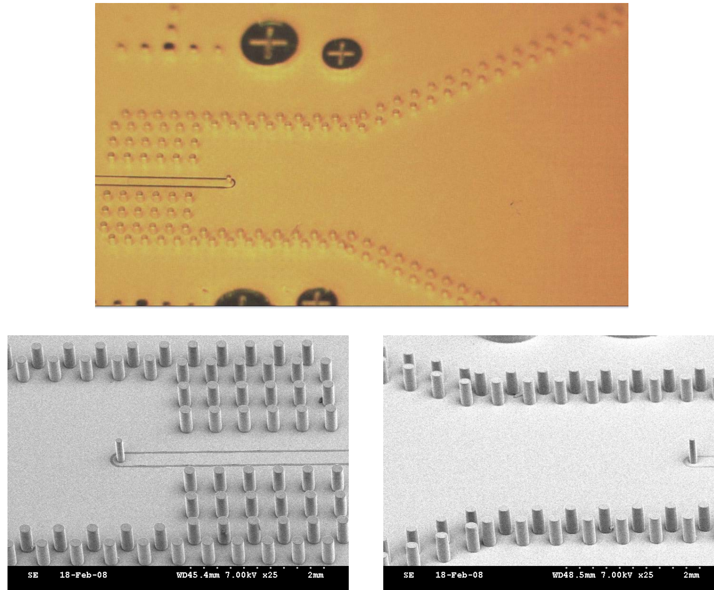


Figure 9.12: Micro-images of fabricated horn.

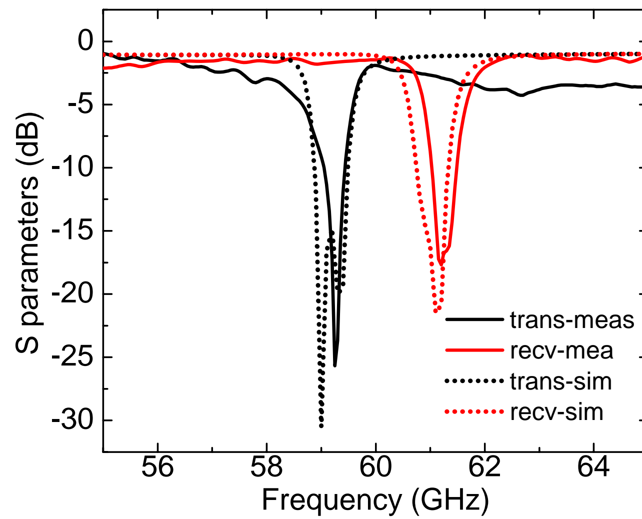


Figure 9.13: Simulated and measured performance of a transceiver front-end passive module.

9.5 *Amplifier integration*

As a substrate-independent solution, the polymer-core conductor surface micromachining technology can provide us a versatile platform for system integration. As we have emphasized in previous sections, various issues in using different substrate requirements for active circuits and passive parts in all existing technologies can be solved by this technology.

Ideally, to demonstrate this advantage, all passive components discussed above should be integrated directly above an active circuitry die. In this scenario, all modules are connected with just regular transmission lines, with active circuits embedded in the substrate and passive components stand on top of substrate. This integration scheme introduces minimal parasitics associated with a bonding wire or solder bump used in other technologies.

However, developing active circuits at this frequency, though available both in academia and industry, is far from mature. It still keeps a hot research area and there are many issues being resolved. It is unrealistic for us to have foundry service provider to modify their standard semiconductor process to test our proposed technology. In our research, instead, we demonstrate the integration of commercially available chips without packaging, using the simplest form of interconnection- wirebonding.

The significance of this work lies in several folds: first, it shows that this integration platform supports integrating active parts using simplest method-wirebonding, as other existing approaches do; secondly, issues and experiences we have met in our research for this type of interconnection method are summarized for future research; thirdly, we want to demonstrate a fully functional transceiver front-end module, integrated with both active parts and passive components.

Two types of millimeter-wave amplifier chips from Hittite Co. are integrated with the micromachined duplexer and horn antenna. A low noise amplifier (LNA), HMC-ALH382, is the connected with receiving channel, while a medium power amplifier (PA), HMC-ABH209, configured for the transmitting channel.

Because packaging amplifiers for such high frequency application still keeps a challenge, these millimeter-wave chips are usually shipped as bare die. This removes package parasitics but posts great challenge for handling, at least in prototyping. The dimension of the LNA

is 1.55 x 0.73 x 0.1 mm and 2.2 x 1.22 x 0.1 mm for the PA. Both of them are made out of GaAs wafer and very fragile. Both amplifiers need dual power supply. Before RF input/output is wire-bonded to CPW lines that feed the duplexer, amplifiers performance was tested on chip using DC probes and RF probes. Figure 9.14 shows the measured LNA S parameters with its micro-image shown in the inset. As can be seen, a total 64-mA drain current gives a forward gain around 21 dB and a total 80-mA drain current raises gain up to 23 dB. For the PA, the measure on-chip four S parameters are shown in Figure 9.15, with a micro-image shown in the inset. Less gain is observed for this chip. It is around 12-13 dB.

The amplifiers are then wire-bonded to power splitting ports. Al/Si bonding wires with 1.5 mils (38 μm) diameter are used to connect RF pads of the amplifiers with CPW lines. In our design, since the CPW signal line width is 220 μm, the discontinuity between a bonding wire and a 220 μm wide CPW line is thought to introduce large reflection. A tapered CPW section is designed to transform signal line width down to 100 μm to minimize power reflection. The length of bonding wire is critical for impedance matching. The shorter the wire, the less reflection is caused by interconnect. In reality, to make reliable interconnect, the bonding angle can not be reduced to zero. Meanwhile, if the starting point of a bonding wire is very close to the end point, a big curve forms and introduces more parasitic inductance. In our research, based on our best bonding facility and expertise, a length of approximately 350 μm is observed for all RF bonding. The thickness of the chip is 100 μm. To further reduce lengths of bonding wires, a 100 μm deep cavity can be made to sit amplifiers. This brings RF pads of a chip and CPW lines onto the same level and leads to a shorter bonding wire. However, the substrate used in our prototyping experiment is glass and it is not easy to form this cavity. Considering all these issues, a wire length of 350 μm is very practical.

In terms of electrical performance, this length introduces significant impedance mismatch. These relatively long and thin wires introduces a significant amount of parasitic inductance to the input port of the LNA, and to the output port of the PA. These amplifiers are thus operated in a sub-optimal condition. Once the amplifier is bonded to the

duplexer and horn, it is hard to evaluate its individual performance degradation caused by long bonding wires. However, its impact on system performance can be observed in the following reported experiment data.

Two useful pieces of experience we have gained in amplifier integration are ESD protection and oscillation prevention. Millimeter-wave chips usually are not integrated with ESD protection circuitry. Extremely strict precautions should be followed to avoid damaging amplifiers. Static charge shock is believed to be the No. 1 cause to damage millimeter-wave chips in our experiments. In terms of oscillation prevention, two decoupling capacitors of 100 pF and 0.1 μF are used both for gate biasing and drain biasing. Strong oscillation has been observed without decoupling capacitors. CPW feeding is used for passive modules and a large area of ground exists on top of substrate. Meanwhile, the backside of an amplifier chip is metalized with Ti/Au and connected with ground pads on the frontside using plated through-vias. The amplifier chip needs a good RF/DC ground. This is achieved by attaching amplifier on CPW grounds with the help of silver epoxy. Directly patterning DC biasing circuits on the top of substrate can be achieved at the same time when CPW lines are patterned. However, because of lack of appropriate tools to dispensing silver epoxy within such a tiny area under the amplifier chip, all these dispensing and mounting work are done manually. Silver epoxy dispensed by this way will mess DC biasing circuits and introduce short-circuit problem. To solve this problem, DC biasing circuits are patterned onto a 4 mil(100 micron)-thick LCP substrate instead. Decoupling capacitors are bonded to a small piece of LCP substrate. Amplifier chips and DC biasing LCP circuits are bonded on top of substrate using silver epoxy. Interconnect between DC pads on an amplifier chip and pads on the LCP circuit is realized again using wire-bonding. Long and curved bonding wire is actually a plus here since it introduces large inductance for RF choking and provides additional isolation between DC and RF path. The possible return path between RF input/output through DC biasing circuit is further blocked to prevent potential oscillation. Figure 9.16 shows a micro-image of a LCP DC bias circuit with an amplifier chip placed close to it.

Figure 9.18 shows pillar arrays and amplifiers integration. Duplexer cover is manually

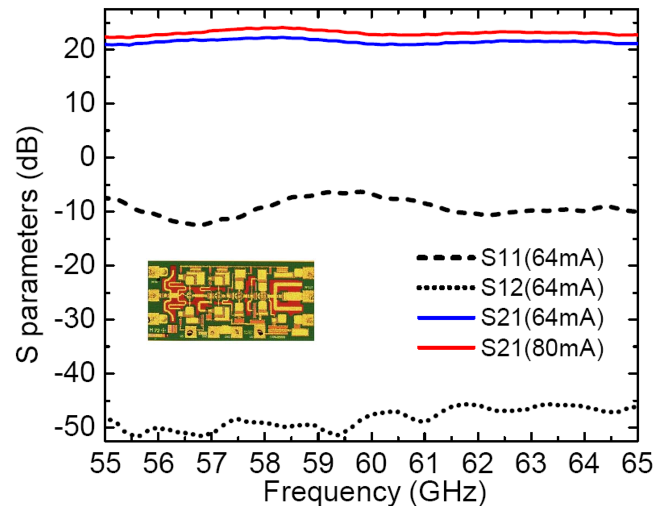


Figure 9.14: Measured LNA performance for different biasing current.

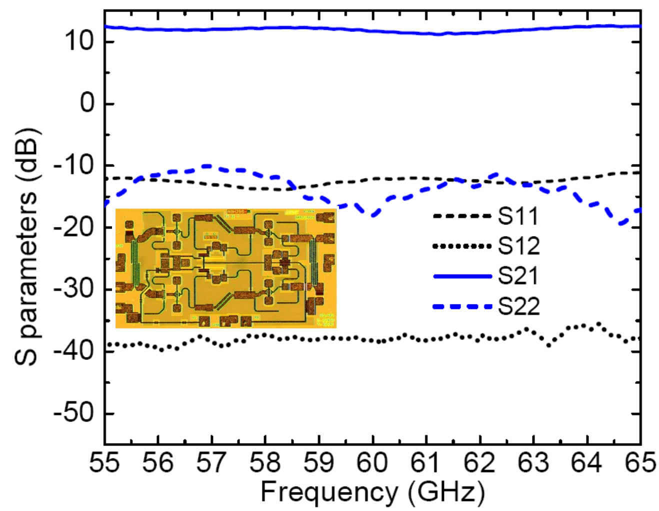


Figure 9.15: Measured PA performance for different biasing current.

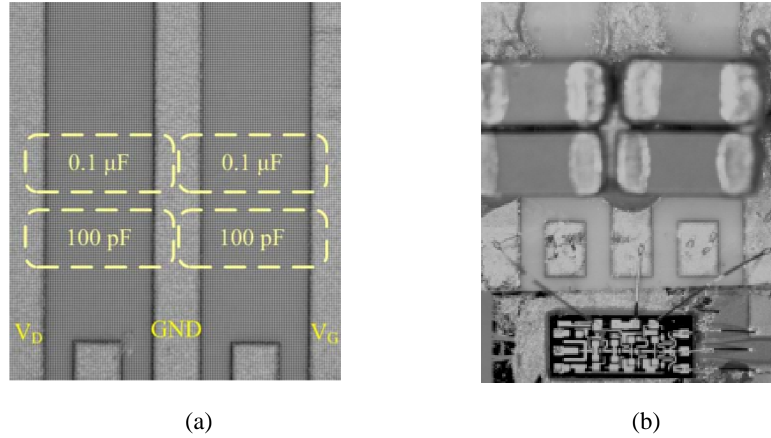


Figure 9.16: Biasing circuits on a 4-mil LCP.

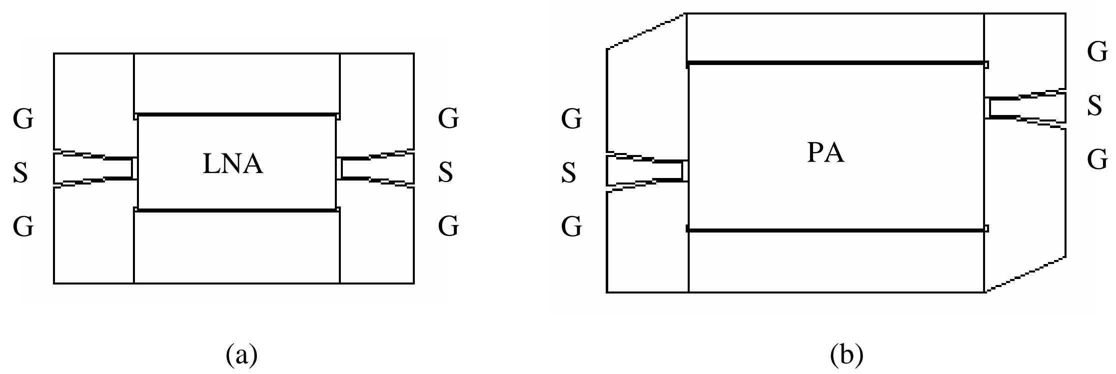


Figure 9.17: Layouts for amplifier integration.

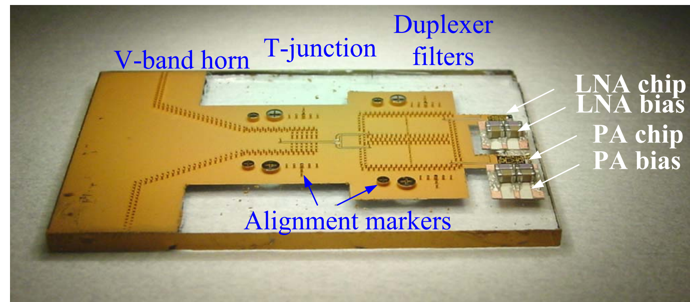


Figure 9.18: Integration of amplifiers, duplexer, and antenna before bulk-micromachined upper half is bonded.

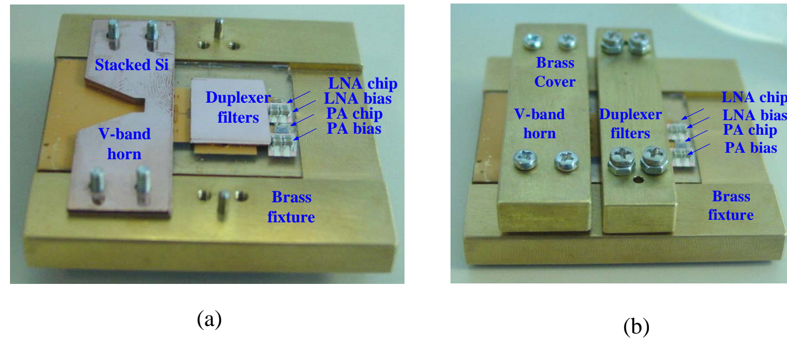


Figure 9.19: (a)Integration picture after duplexer cover is bonded and bulk-micromachined horn upper half is assembled. (b) Final assembled circuit with the aid of a brass fixture

bonded to pillar-array sidewalls using high-conductivity nano-particle silver epoxy provided by [33]. No alignment is needed for this step. To prevent performance degrading, silver epoxy is only applied to top ends of pillars by carefully flipping the circuit and dipping all pillar ends into a layer of shallow silver epoxy. It is very important to avoid directly applying silver epoxy on the metalized silicon cover.

Now, bulk-micromachined silicon pieces for the horn upper half are bonded with the aid of a brass fixture. The brass fixture is used to align and hold together bulk-micromachined layers and pillar arrays since alignment between layers is critical for performance; manually bonding with silver epoxy is not a good choice here. Figure 9.19 (a) shows the integrated module after duplexer cover is bonded and dry-etched silicon pieces are assembled; Figure 9.19 (b) shows the final integrated module after two brass covers are fastened to press all layers tightly.

Scattering parameters are measured after the whole module is assembled. Since integrated amplifier is broadband matched, S parameters reading can not give any evidence of wireless transmission. An air transmission testing is then performed to evaluate the transceiver.

9.5.1 wireless transmission testing

Wireless transmission tests are performed before amplifiers are integrated and after, respectively.

For a test without amplifier, an integrated module with duplexer and antenna is connected to Port 1 of a 8510 XF network analyzer, while a standalone CPW-fed micromachined horn antenna reported in [54] is connected to Port 2. S21/S12 is plotted to test wireless transmission between two modules. TRL calibration is performed and the unused port is terminated with 50 Ohm load using a probe positioner. Both the transmission channel and the receiving channel are tested and results are plotted in Figure 9.20 and Figure 9.21 respectively. As can be seen, wireless transmission peaks are found at 59.2 GHz and 61.25 GHz respectively.

After the amplifiers are integrated, wireless transmission test is performed again. Connection between the modules and the network analyzer is same except for the unused port is not terminated with a 50 Ohm load. This is because an amplifier needs three DC probes for biasing. There is no space to put additional positioners because of bulky millimeter-wave mixer modules equipped with 8510 XF test system. From amplifier test, we found that the amplifier input/output is matched to 50 Ohm even with DC pads all connected in floating mode. Both transmit channel and receive channel are tested. Results are plotted in Figure 9.20 and Figure 9.21 respectively, with comparison of results without amplifier.

Transmission peaks are observed at almost the same frequencies. The channel 1 peak with the amplifier is 10 dB higher than the one without a PA, while channel 2 peak with the amplifier is 18 dB higher than the one without a LNA. It is also found that S21 with an amplifier is not simply the sum of the S21 without an amplifier and the amplifier gain, although curve shapes are similar. This is attributed to two factors. First,the impedance

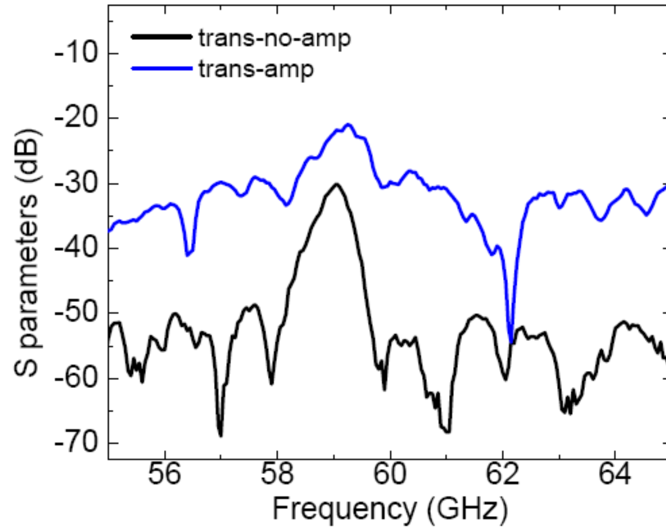


Figure 9.20: Measured wireless test results for transmission channel.

matching between an amplifier and the duplexer is not constant; more power is transmitted to the antenna at certain frequencies. Secondly, compared with in-band strong radiation, out-of-band weak radiation is more likely to be mixed with measurement system noise, especially in a multi-path propagation environment consisting of two bulky millimeter-wave modules, several DC probes, the metal stage, and metal probe positioners/heads.

9.5.2 Radiation pattern and gain measurement

After wireless transmission test in GEDC, Atlanta, Georgia, the integrated transceiver module was sent to NASA Glenn Research Center for pattern and gain measurement. The objective of this measurement is to get radiation pattern of this transceiver module, as well as gain measurement to compute efficiency of this technology. Because of amplifier failure during testing, channel 2 LNA is replaced with a PA that has a lower gain.

The antenna is characterized on a specialized far field antenna range comprised of an RF GSG probe head supported on a wood/foam shelf, a Styrofoam shelf to support the antenna under test, a rotary stage that rotates a WR-15, 25 dBi gain horn in an arc around the antenna under test, and an Agilent 67 GHz PNA. DC probes for biasing the amplifier are supported by the same shelf that supports the RF probe head. The radius of the arc traversed by the gain horn, which is the distance between the gain horn and the antenna

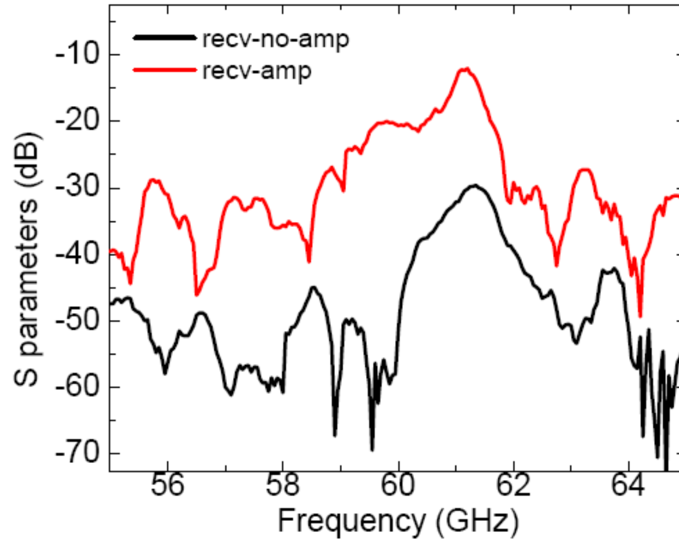


Figure 9.21: Measured wireless test results for receiving channel.

under test, is 57 cm. The system is calibrated with a second, identical WR-15, 25 dBi gain horn. The measured results are not corrected for the difference in insertion loss between the 1.85 mm to WR-15 adapter required for the calibration and the probe at 60 GHz. Cascade estimates the insertion loss of the probe at 60 GHz to be 2 dB, and the insertion loss of the adapter is estimated to be 1.2 dB. Also, the M/A Com data sheets estimate the gain of the horn antenna to be 0.2 dBi lower at 60 GHz. Thus, overall, there could be +0.6 dB correction to the measured gain, but because these insertion loss and gain corrections were not verified, the data was not corrected. Instead, it is stated that the error in the measured data is estimated to be 0.6 dB. Ripples on the measured radiation patterns are due to required auxiliary equipment, such as microscope stand and microscope, metal probe fixture, metal stand to support the wood/foam shelf, and metal sheet required to hold the DC probe heads; absorber was used to minimize the effects of the metal structures but it could not eliminate them. Figure 9.22 shows the pattern measurement setup.

Figure 9.23 shows measured E-plane co-polarization and cross-polarization gain. The maximum total gain is read as 14.5 dBi approximately at θ=55$^{(\circ})$.

Table 9.3 calculates the expected gain from this measurement. The amplifier's gain is estimated as 10 dB based on wireless transmission testing data shown in Figure 9.20. Gain boosting of 10 dB is observed for this type of amplifier. It includes loss and mismatch from

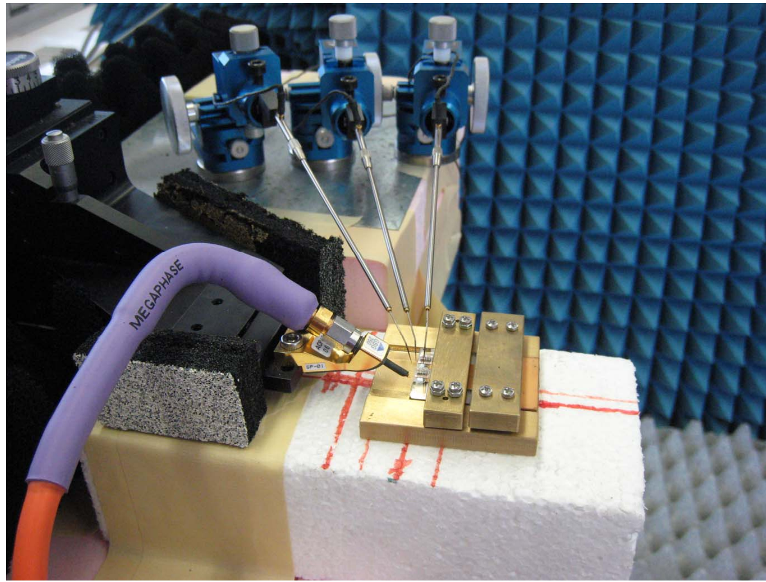


Figure 9.22: A picture of on-wafer pattern measurement system setup in NASA.

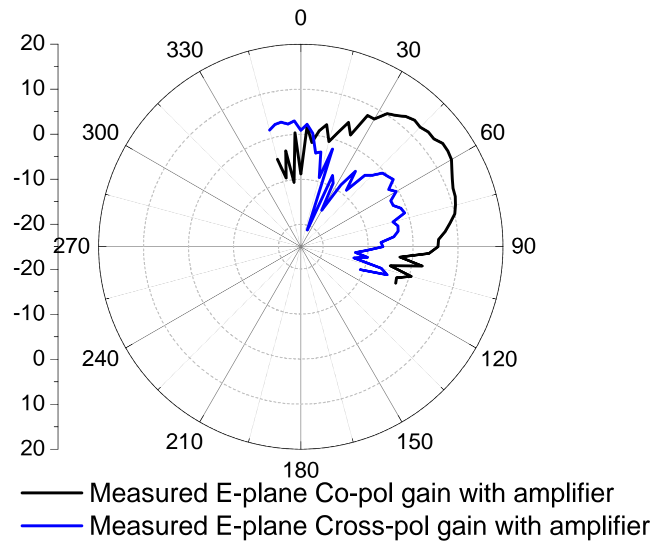


Figure 9.23: Measured E-plane copolarization and crosspolarization gain patterns.

Table 9.3: Theoretical gain calculation breakdown

	amplifier	duplexer	line loss	horn antenna	overall
gain	10 dB	-3.6 dB	-1.1 dB	11.5 dB	16.8 dB

long RF bonding wires and adhesion epoxy, thus is lower than its on-chip measured gain. Various line loss is estimated as 1.1 dB based on our characterization data of CPW lines on this glass substrate. Since this integrate horn antenna is not characterized separately, its theoretical gain is used in calculating overall gain of the integrated module. The calculated gain is 16.8 dB. Considering another additional +0.6 dB correction stated previously and measured antenna gain could be lower than its theoretical value, good agreement is achieved between calculation and measurement.

So far, we have fully characterized this micromachined integrated transceiver front-end module. An overall gain of 14.4 +0.6 dB is measured and could be higher when a reliable high gain LNA is connected.

9.6 Chapter summary

In this chapter, a novel approach to integrate high performance millimeter-wave transceiver front-end using polymer-core conductor surface micromachining technology is presented for the first time. By elevating a cavity-filter-based duplexer and a horn antenna on top of the substrate and using air as the filler, the dielectric loss can be eliminated. A full-duplex transceiver front-end integrated with amplifiers are designed, fabricated, and comprehensively characterized to demonstrate advantages brought by this surface micromachining technology. The proposed method offers an easy integration of both planar components and 3-D integrated modules on top of the substrate. It is a low loss and substrate-independent solution for millimeter-wave transceiver integration.

CHAPTER X

CONTRIBUTIONS AND PUBLICATION TO DATE

This work has explored systematically design, fabrication and characterization of polymer-core-conductor surface micromachining approach for millimeter-wave integration, from individual devices to subsystems. There have been many contributions both to the academic and industry communities, mostly in helping better understand advantages and challenges brought by this technology. Perhaps the most substantial of these contributions are the following:

- The first W-band CPW-fed vertical monopole antenna
- The first Ka-band CPW-fed elevated patch antenna
- The first 15-45 GHz CPW-fed elevated coupler
- The first pillar-array-based millimeter-wave micromachined cavity
- The first CPW-fed surface micromachined V-band horn antenna
- Two high-performance micromachined millimeter-wave all-pole filters using polymer-core-conductor surface micromachining technology
- Two novel transmission-zero micromachined millimeter-wave filters
- The first micromachined full-duplex V-band transceiver front-end

In addition, one testbed for millimeter-wave on-wafer radiation pattern measurement system has been built for further investigation of more millimeter-wave antenna designs.

This work and other related research in my PhD has led to the following publications:

Book Chapter

- B. Pan, J. Papapolymerou and M. M Tentzeris, "MEMS-Integrated and Micromachined Antenna Elements, Arrays and Feeding Networks", book chapter in Modern

Antenna Handbook, edited by Prof. Constantine A. Balanis, John& Wiley Sons Inc., 2008

Journal Publications

- B. Pan, Y. Li, G. E. Ponchak, J. Papapolymerou and M. M Tentzeris, "A 60 GHz CPW-Fed Micromachined Horn Antenna", submitted to IEEE Antennas and Wireless Propagation Letters, April 2008.

- B. Pan, Y. Li, G. E. Ponchak, M. M Tentzeris and J. Papapolymerou, "A Substrate-Independent V-band Transceiver Front-end using Surface Micromachining Polymer-core Conductor Approach", submitted to IEEE Transaction on Microwave Theory and Technology, April 2008.

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- R.-L. Li, B. Pan, J. Laskar and M.M.Tentzeris, "A Very-Low-Profile Broadband Planar Antenna for DCS-1800 and IMT-2000 Applications", Microwave and Optical Technology Letters, pp1679-1681, Vol.49, No.7, July 2007
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Conference Publications

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60 GHz Cavity Filter with Source-Load Coupling using Surface Micromachining Technology", accepted for presentation by IEEE MTT-s 2008

- Y. Li, H.-G. Doo, B. Pan, M. M. Tentzeris, J. Zhang, and J. Papapolymerou, "Characterization of a novel ferromagnetic thin film with an increased thickness", accepted by presentation by IEEE MTT-s 2008

- Y. Zhao, S-H. Kim, X. Wu, Y. Li, B. Pan, M. M. Tentzeris, J. Papapolymerou and M. G. Allen, "A Micromachined Airflow Sensor based on RF Evanescent-mode Cavity Resonator", accepted by presentation by IEEE MTT-s 2008

- Y. Li, B. Pan, M. M. Tentzeris and J. Papapolymerou, "A Fully Micromachined W-Band Coplanar Waveguide to Rectangular Waveguide Transition", Proc. of 2007 IEEE-IMS Symposium, pp.1031-1034, Honolulu, Hi, June 2007

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