DESIGN OF A COMPLEMENTARY SILICON-GERMANIUM VARIABLE GAIN AMPLIFIER

A Thesis

by

Nand Kishore Jha

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DESIGN OF A COMPLEMENTARY SILICON-GERMANIUM VARIABLE GAIN AMPLIFIER

Approved by:
Professor John D Cresslor, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Kevin T. Kornegay
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Joy Laskar
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 7th July 2007

To Papaji, Mammi, Neha, and Bhaiya

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

This thesis presents an overview of the simulation, design, and measurement of state-of-the-art Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) variable gain amplifier (VGA). The VGA design trade-off space is presented and methods for achieving an optimized design are discussed.

In Chapter 1, we review the importance of VGAs and the benefit of SiGe HBT technology in high frequency amplifier design. Chapter 2 introduces VGA design and basic theory. A graphical VGA design approach is presented to aid in understanding of the high frequency VGA design process. Chapter 3 presents a VGA design optimization method for linear VGA design. Simulation result using design technique is highlighted and shown to have good performance.

We demonstrate in this thesis that SiGe HBT VGA has the capability to meet the demanding needs for the next generation wireless systems. The aim for the analysis presented herein is to provide designers with the fundamentals of designing SiGe HBT VGA through relevant design examples and simulated results.

Chapter 1

Introduction

1.1 Motivation

A key building block in a wireless communication system is the radio-frequency (RF) front-end. The push for increasingly speed, low-cost technologies and compactness requires novelty in front-end circuit design. The basic structure of a heterodyne receiver is shown in Figure 1.1. Almost in all of wireless communication, a low-noise amplifier (LNA), mixer, variable gain amplifier (VGA), voltage-controlled oscillator (VCO), and filter are needed.

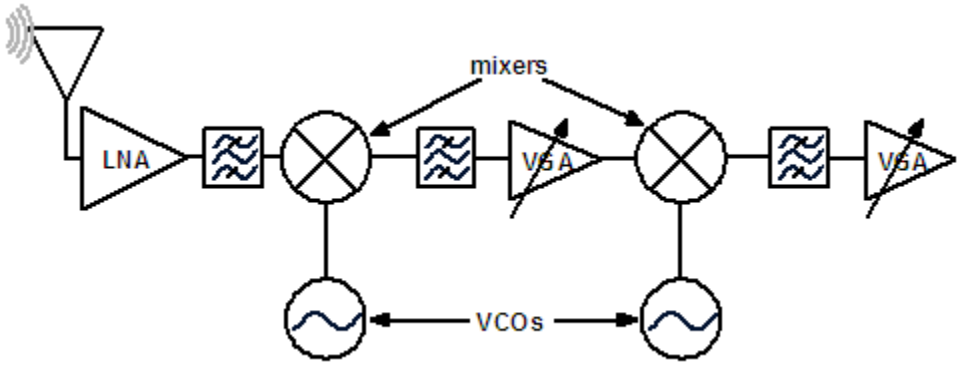

Figure 1.1. RF frontend for heterodyne receiver architecture.

Due to the rapid growing trend of the RF communication systems in the recent years, the need for high selectivity and good control of the output signal level is an important design criterion in any communication systems. Fading, defined as slow variations in the amplitude of the received signals, requires continual adjustments in the receiver's gain in order to maintain a relatively constant output signal. Such a situation led to the design of circuits whose primary ideal function

was to maintain a constant signal level at the output, regardless of the input signal's variations. Originally, these circuits were described as automatic volume control circuits, a few years later they were generalized under the name of Automatic Gain Control (AGC) circuits. With the huge development of communication systems during the last decade, the need of the selectivity and good control of the output signal level became a fundamental issue in the design of any communication system. Nowadays, AGC circuits can be found in any system where signal's amplitude variations in the output signal could lead to a loss of information or to an unacceptable performance of the system. The main objective of this chapter is to provide an insight of the theory of the AGC circuits and its major component.

A variable gain amplifier (VGA) has a wide range of applications in wireless systems. In communication systems, it plays an indispensable role in receivers by controlling the incoming signal's power level and normalizing the average amplitude of the signal to a reference value. This helps in increasing data range without giving extra burden of linearity to the front-end circuits. Third-order input intercept point (IIP3) is an important parameter in designing a receiver chain. It limits the maximum signal at the input of antenna. Thus, to increase the range of input signal, it has to be maximized. Also, to use VGA effectively, one has to increase its gain range as well. In addition to maximizing IIP3 of VGA and increasing gain range, other specifications also impacting VGA design choices include: noise figure (NF), power consumption, and bandwidth. These specifications are rarely simultaneously optimized, therefore, understanding the design trade-off space is necessary for a successful VGA design. In addition to these trade-offs, improvements in device technology performance enable new applications for Si-based systems which offer low-cost solutions with similar performance to more expensive technology.

This thesis explores the VGA design trade-off space using Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs). The remainder of this chapter will focus on the SiGe HBT transistor and highlight its performance benefits. Subsequent chapters will focus on linearity theory and VGA design and optimization. A number of VGA designs are analyzed, and an understanding of device linearity performance as it relates to VGA design is explored.

The proposed VGA uses a SiGe fully differential architecture. It includes complementary differential pairs with source degeneration as its input transconductor to convert the input voltage into current. A programmable current mirror acts as a current gain stage to further amplify the current and fixed load resistors to provide the linear current-to-voltage conversion at the output of the VGA.

1.2 Variable Gain Amplifier Configuration

The primary function of automatic gain control (AGC) is to maintain a constant signal level at the output, regardless of the signal variations at the receiver input. The major component of the AGC is a variable gain amplifier (VGA) whose gain can be dynamically varied. Thus, a VGA is an indispensable function block of all radio communication systems. A good VGA design with large dynamic range is a major factor to ease the design of AGC systems. In recognition of the importance of the AGC systems and VGA design, this report introduces readers to the background of VGA as well as its basic configuration.

1.3 Silicon-Germanium Heterojunction Bipolar Technology

SiGe HBTs combines the speed and performance of many III-V technologies with Si-processing compatibility yielding a high-performance device that is readily commercially available. Since the first SiGe HBT demonstration over 20 years ago, SiGe HBT technology has shown an almost exponential growth both in terms of performance and number of commercial facilities as shown in Figure 1.2, [5]. SiGe technology uses band-gap engineering in the base of a Silicon Bipolar Junction Transistor (BJT) to enhance device characteristics. By epitaxial growing compositionally graded SiGe alloy as the transistor base, device parameters are decoupled allowing exponential "tuning" based on the Ge content.

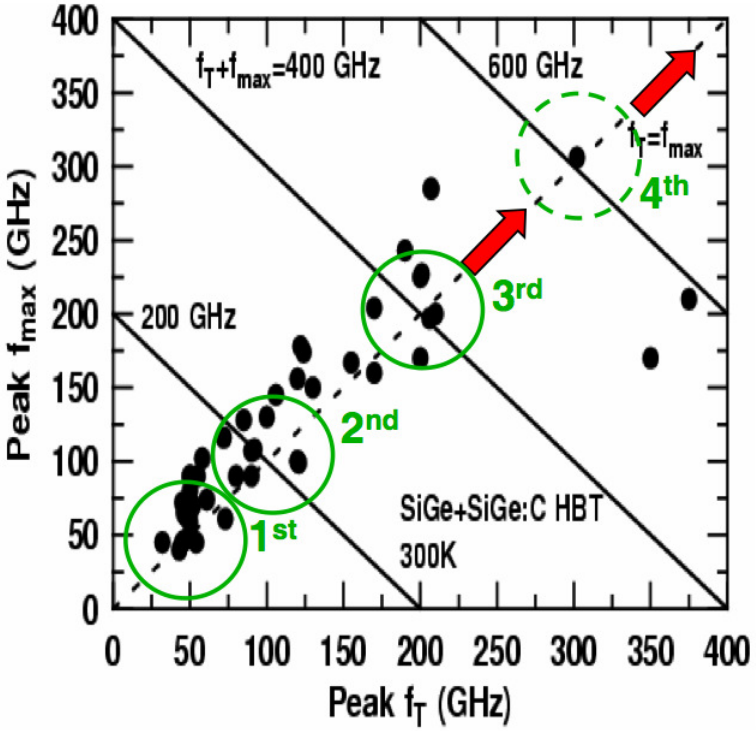

Figure 1.2. SiGe HBT technology performance growth as measured by f_T and fmax [7].

The mechanism for this tuning capability is driven by the bandgap difference between Si (1.12eV at 300K) and Ge (0.66eV at 300K). This difference allows the bandgap of the SiGe alloy to be optimized to improve transistor performance. The effect of the graded Ge in the base directly impacts key performance metrics such as current gain (β), base transit time (τ_b), cutoff frequency (f_T), and maximum oscillation frequency (f_{max}) which couple strongly to high-frequency amplifier performance [7].

A comparison of these parameters between a standard Si BJT and SiGe HBT yields an understanding of how Ge content can influence device performance. Assuming a linearly graded Ge profile (Figure 1.3), the collector current density enhancement directly relates to the β enhancement between a SiGe HBT and a Si BJT [7]:

$$\frac{J_{C,SiGe}}{J_{C,Si}} \simeq \frac{\beta_{SiGe}}{\beta_{Si}} \simeq \frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/kT e^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}} \quad \textbf{(1.1)}$$

Where ˜ denotes the positioned averaged quantities across the base, γ is the "effective density-of-states" ratio and η is the minority electron diffusivity ratio between SiGe and Si. The Ge profile enters the relationship through $\Delta E_{g,Ge}(grade)$ which is defined as $E_{g,Ge}(W_b) - E_{g,Ge}(0)$. This equation shows that as $\Delta E_{g,Ge}(grade)$ is increased, the total current gain will also increase. In addition, this enhancement is temperature activated through the $\frac{1}{kT}$ term. This relative enhancement in β has an impact on high frequency amplifier performance in terms of gain and noise figure. Further analysis shows that two crucial metrics of device performance, f_T and f_{max} are largely enhanced through the minimization of τ_b through the addition of Ge in the base. Assuming a strong Ge grading scenario, equation 2 which is true for the current generation of HBT technologies, τ_b is improved by $\Delta E_{g,Ge}(grade)$:

$$\tau_{b,SiGe} \simeq \frac{W_b^2}{2D_{nb}} \cdot \frac{kT}{\Delta E_{g,Ge}(grade)} \quad \textbf{(1.2)}$$

Where W_b is the base width and D_{nb} is the minority electron diffusivity. By increasing $\Delta E_{g,Ge}(grade)$, τ_b is reduced. Also, τ_e (emitter charge storage delay) is proportional to 1/β therefore resulting in a reduction of the total transit time. This can be further explored by examining f_T:

$$f_T = \frac{1}{2\pi}\left[\frac{1}{g_m}(C_{te} + C_{tc}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc}\right]^{-1} \quad \textbf{(1.3)}$$

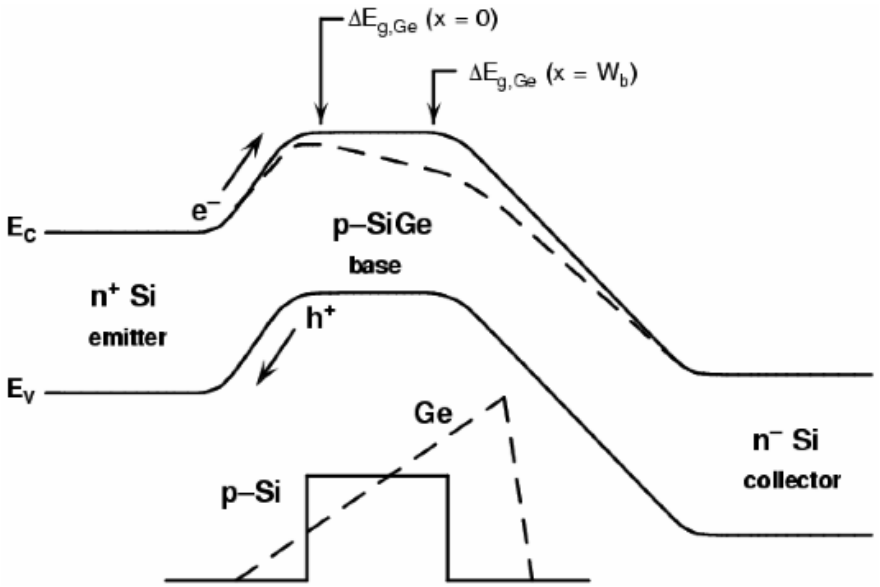

Figure 1.3. Energy band diagram for SiGe HBT (dashed) compared to Si BJT (solid) biased in the forward active region [7]

where gm is the device transconductance $\frac{\partial I_c}{\partial V_{BE}}$, C_{te} + C_{tc} are the depletion capacitances W_{CB} is the junction width of the collector-base(CB) space charge region, v_{sat} is saturation

velocity, and r_c is the small-signal collector resistance. Since f_T is inversely proportional to τ_b and τ_e, their reduction will increase f_T. Also, f_{max} will improve since it is a function of f_T :

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}} \quad \textbf{(1.4)}$$

Where C_{bc} is the collector base capacitance, and r_b is the intrinsic base resistance. By adjusting the Ge grading, higher base doping can be used while still maintaining a high β, yielding a lower base resistance and improved noise performance. These performance parameters point to the ability to increase amplifier characteristics such as gain and noise figure, which can greatly benefit VGA and system design. One of the key advantages of SiGe HBT technology is its compatibility with traditional Si CMOS processing. The Ge layer is grown using an ultra-high vacuum/chemical vapor deposition (UHV/CVD) processing step, which reduces the necessary thermal cycle and has fine control of the Ge profile. This process modification is typically included as a "plug-in module" in traditional Si CMOS fabrication facilities allowing for a high-yielding low-cost BiCMOS technology. A micrograph of a cross-section of a third-generation SiGe HBT is shown in Figure 1.4. SiGe HBTs compatibility with Si CMOS processing is a key advantage over competing III-V technologies which are typically characterized by low to moderate-yielding, non-Si CMOS compatible processing. In addition, the performance improvements at a given technology node allow SiGe HBTs to provide cost vs performance advantage even over Si-CMOS. Figure 6 compares RFCMOS versus SiGe HBT relative trusted foundry pricing at a similar technology performance as measured by f_T. Some relevant performance specifications for a third generation SiGe technology are highlighted in Table 1.1.

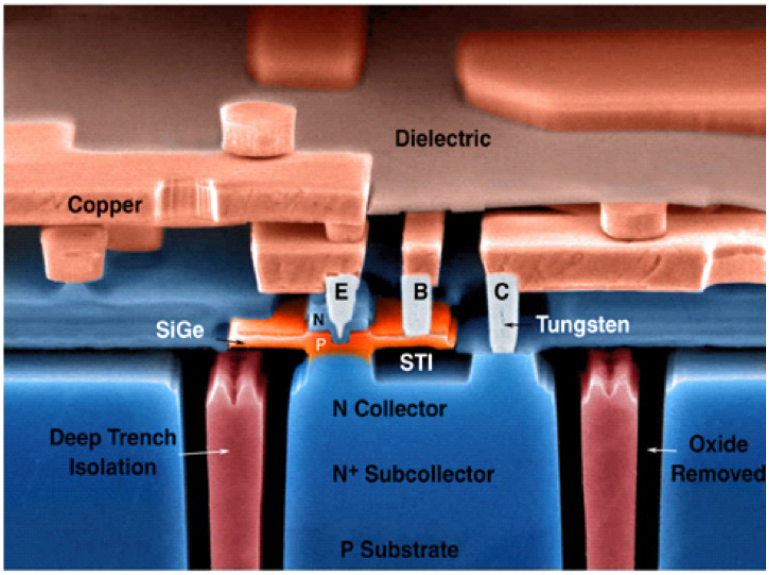

Figure 1.4. Structure of third-generation SiGe HBT (courtesy of IBM) [7].

Table 1.1: Typical npn SiGe HBT device performance parameters across generation [7].

Parameter	1st generation	2nd generation	3rd generation
W_E	0.50 μm	0.18 μm	0.13 μm
β	110	270	400
BV_{CBO}	10.5 V	6.4 V	5.9 V
BV_{CEO}	3.3 V	2.0 V	1.7 V
f_T	50 GHz	120 GHz	200 GHz

1.4 Broadband Noise Fundamentals of SiGe HBT

Equation 1.1-1.4 directly relate the Ge profile to improvements in β, f_T, and τ_b. The ability to simultaneously optimize these factors allows for superior noise performance of SiGe HBTs. To

further understand the noise characteristics of a HBT, linear noisy two-port theory can be used to analyze the noise sources of an HBT. The primary sources of broadband noise in an HBT are base thermal noise ($4kTr_b$), base shot noise ($2qI_B$), and collector shot noise ($2qI_C$).

The noise parameters, R_n, $Y_{s,opt} = G_{s,opt} + jB_{s,opt}$, and F_{min} are typically used to characterize the noise performance of a transistor. These parameters are defined in terms of v_n^2 (equivalent noise voltage), i_n^2 (equivalent noise current), and γ (cross correlation factor) by [16]:

$$\boldsymbol{R_n = \frac{v_n^2}{4kT_0\Delta f}} \quad \textbf{(1.5)}$$

$$\boldsymbol{Y_{s,opt} = \left(\sqrt{1-\gamma_i^2} - j\gamma_i\right)^{-1} \frac{i_n}{v_n}} \quad \textbf{(1.6)}$$

$$\boldsymbol{F_{min} = 1 + \frac{v_n i_n}{2kT_0\Delta f}\left(\gamma_r + \sqrt{1-\gamma_i^2}\right)} \quad \textbf{(1.7)}$$

In addition, these parameters can be related to the noise sources and fundamental device parameters by performing a two port analysis. As shown in [7], v_n^2, i_n^2, and γ for an HBT can be expressed in terms of Y parameters:

$$\boldsymbol{v_n^2 = 4kTr_b + \frac{2qI_c}{|Y_{21}|^2}} \quad \textbf{(1.8)}$$

$$\boldsymbol{i_n^2 = 2q\frac{I_c}{\beta} + 2q\frac{I_c}{\left|\frac{Y_{21}}{Y_{11}}\right|^2}} \quad \textbf{(1.9)}$$

$$\boldsymbol{\gamma = \frac{2qI_cY_{11}}{|Y_{21}|^2}} \quad \textbf{(1.10)}$$

Expressing the HBT as two port device yields the following Y- parameters

$$\boldsymbol{y_{11} = \frac{g_m}{\beta} + j\omega C_i} \quad \textbf{(1.11)}$$

$$\boldsymbol{y_{12} = -j\omega C_{bc}} \quad \textbf{(1.12)}$$

$$y_{21} \approx g_m \quad (1.13)$$

$$y_{22} = j\omega C_{bc} \quad (1.14)$$

where $C_i = C_{be} + C_{bc}$. Combining equation 1.5-1.10, 1.11-1.14 yield the following results for the noise parameters of a SiGe HBT in terms of device parameters:

$$R_n = r_b + \frac{1}{2g_m} \quad (1.15)$$

$$G_{s,opt} = \sqrt{\frac{g_m}{2R_n\beta} + \frac{(\omega C_i)^2}{2g_m R_n}\left(1 - \frac{1}{2g_m R_n}\right)} \quad (1.16)$$

$$B_{s,opt} = \frac{\omega C_i}{2g_m R_n} \quad (1.17)$$

$$F_{min} = 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m R_n}{\beta} + \frac{2R_n(\omega C_i)^2}{g_m}\left(1 - \frac{1}{2g_m R_n}\right)} \quad (1.18)$$

Equation 1.18 shows that the noise factor improves through enhancements to β, C_{be}, C_{bc}, and r_b which are all improved through addition of Ge into the base. For a typical third generation SiGe HBT, this level of performance allows for very low-noise, high-gain, and high frequency VGAs with low power consumption.

1.5 Complementary SiGe HBTs

Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technology is well-known to provide compelling advantages for high-frequency integrated circuit applications. A large number of SiGe ICs with impressive performance have being aggressively deployed by various companies. With the increasing demands of analog applications, such as drivers amplifiers, data converters, video amplifiers, cable modems, etc., complementary (npn + pnp) has emerged as an

important enabling technologies in the analog domain. For instance a high speed pnp transistor in the signal path allows the design of push-pull drivers and active loads for high-speed analog circuits. In addition, high-speed pnp ‘s can enhance circuit performance as drivers in the output stages by reducing the total supply current, thereby improving the power delay performance. Extensive work has been published on high high-frequency, low-breakdown voltage SiGe HBT technologies, using npn only transistors, and these are widely used today. Pnp SiGe HBT’s, however, are known to be very challenging in their design and optimization [7], and the successful integration of SiGe pnp’s and npn’s on chip to form a complementary SiGe HBT technology, has proven to be extremely challenging. Even through conventional complementary silicon bipolar technology have been in use for some time, only very recently have complementary SiGe HBT BiCMOS technology has made inroads in analog circuit design. Recent development in the SiGe HBT filed include the first report of a complementary (npn + pnp) SiGe HBT (C-SiGe) technology in 2003, rapidely followed by a C-SiGe technology with f_T for both npn and pnp SiGe HBTs above 100GHz [23].

Table 1.2: Typical npn and pnp SiGe HBT device performance parameters in BiCOM3X Technology.

Parameter	npn	Pnp
W_E	0.4 μm	0.4 μm
β	200	400
BV_{CEO}	5	-5.25
BV_{CBO}	11	-11
f_T	25GHz	28GHz
f_{max}	40GHz	35GHz

The novel complementary SiGe HBT BiCMOS technology (Figure 1.5) was developed and fabricated by Texas Instruments, and involve dual depositions of SiGe epitaxy (boron doped for the npn and arsenic doped for pnp), shallow and deep trench isolation, polysilicon emitter contacts with thin, interfacial oxide layers [15] . Both npn and pnp SiGe HBTs, as well as the Si CMOS devices, were integrated on SOI material for improved isolation. For the standard C-SiGe process, the npn and pnp transistor have a peak f_T of about 25GHz, a BV_{CEO} of 6.0 V/5.5 V and Early voltage of 150 V/100 V, respectively [16].

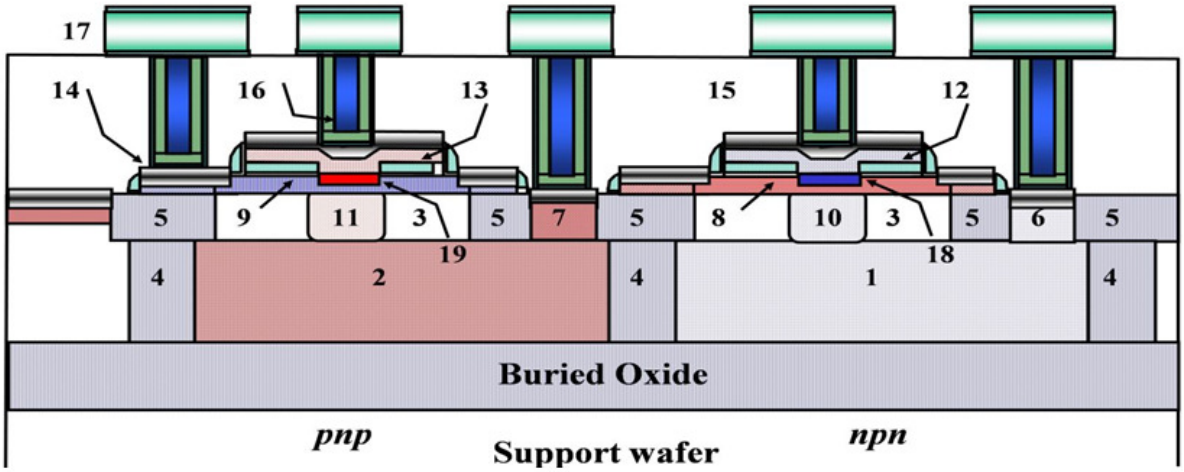

Figure 1.5. C-SiGe Technology BICOM3X [7].

The historical bias in favor of npn Si BJT, compare to larger minority electron mobility in the p-type base of an npn Si BJT, compare to the lower minority hole mobility in the n-type base of pnp Si BJT. In addition, the valence band offset in SiGe strained layer is generally more conductive compare to npn SiGe HBT designs, because it translates into induced conduction band offset and band grading that greatly enhance minority electron structured Si BJT. For a pnp SiGe HBT, valence band offset directly results into valence band barrier, even at low injection which strongly degrades minority hole transport and thus, limits the frequency response. Careful

optimization to minimize these hole barriers in pnp SiGe HBT is required, and has in fact, yielded in impressive device performance compared to Si pnp BJTs.

1.6 Measurement Results

The dc characterization at ambient temperature was performed on TI's complementary devices. Temperature was kept ambient. Test structures are shown in Figure 1.6.

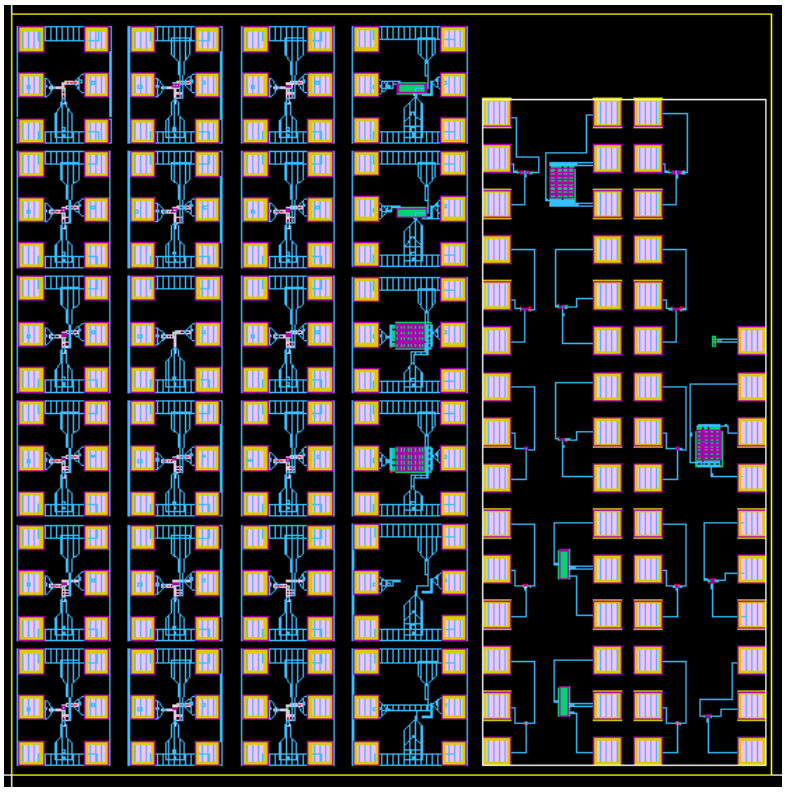

Figure 1.6. Dc and ac test structure of BICOM3X.

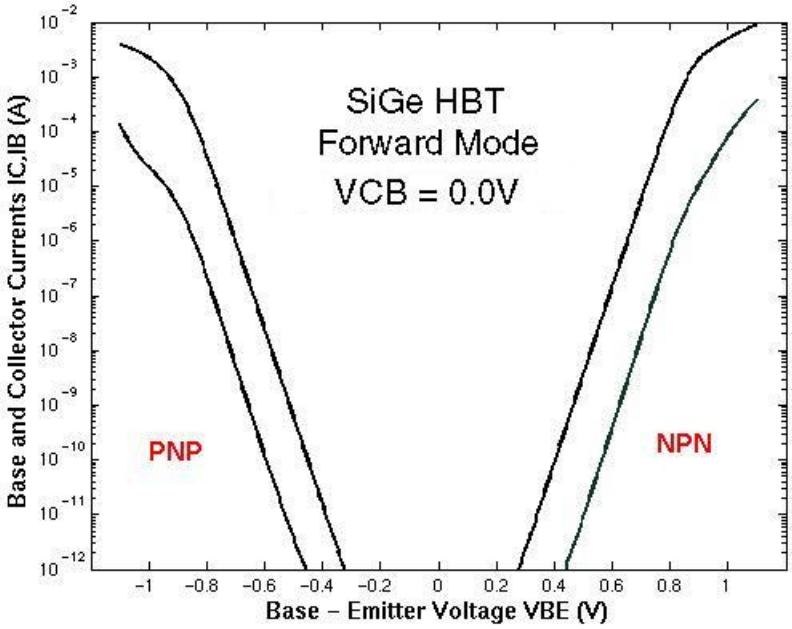

Figure 1.7. Forward gummel characteristics of SiGe complementary devices ($A_E = 0.4X3.2X1\ \mu m^2$).

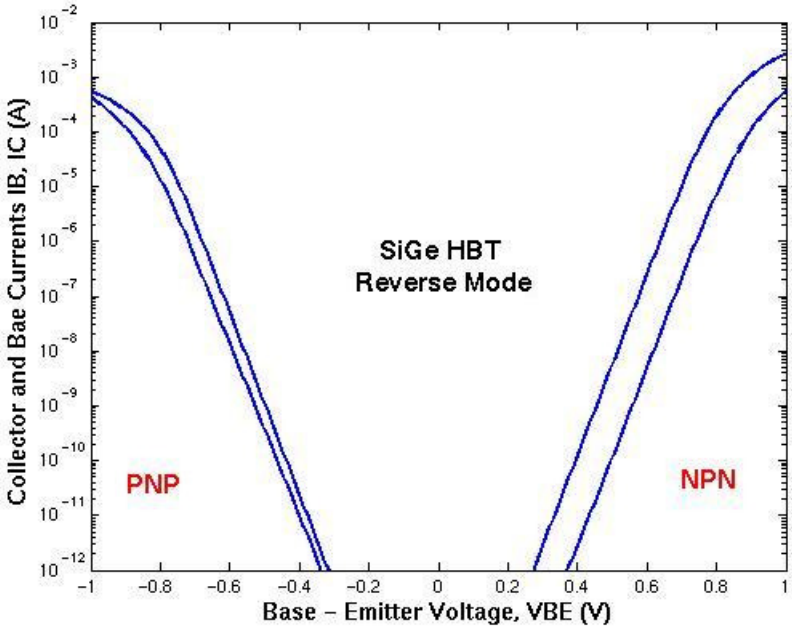

Figure 1.8. Inverse gummel characteristics of SiGe complememntary devices ($A_E = 0.4X3.2X1\ \mu m^2$).

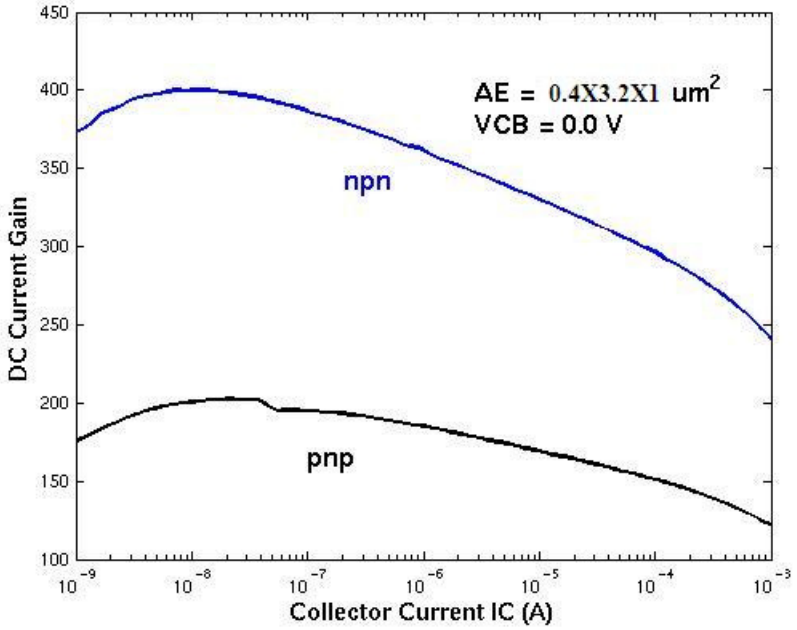

Figure 1.9. DC current gain (β) of npn and pnp in BiCOM3X.

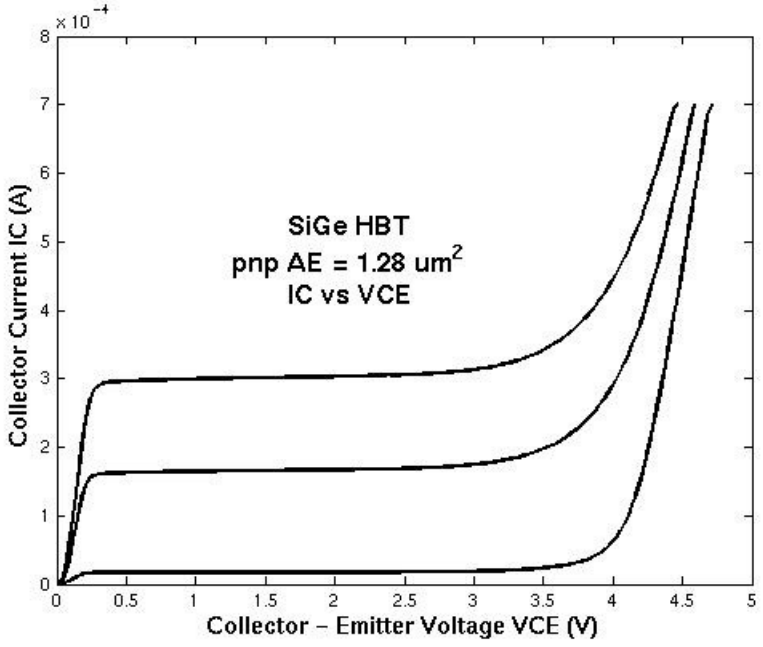

Figure 1.10. Ic vs Vce characteristics of pnp SiGe HBT.

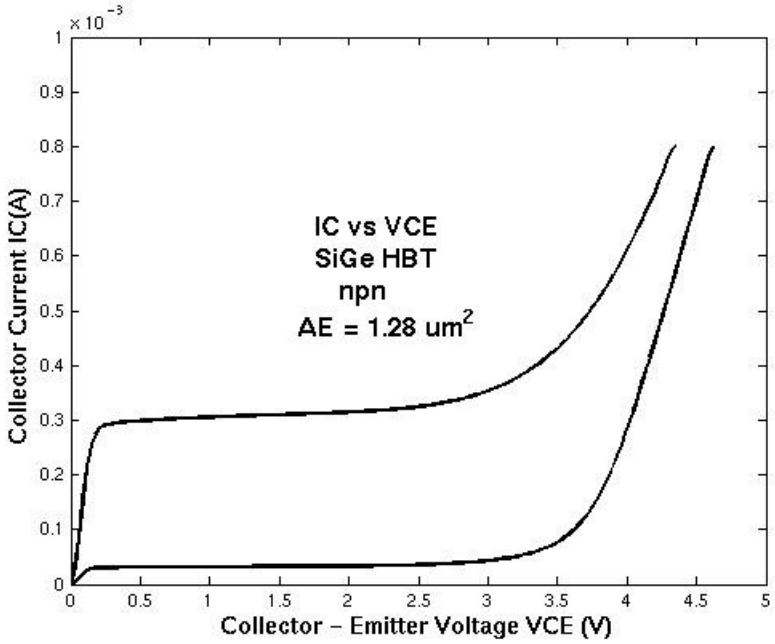

Figure 1.11. Ic vs Vce characteristics of npn SiGe HBT.

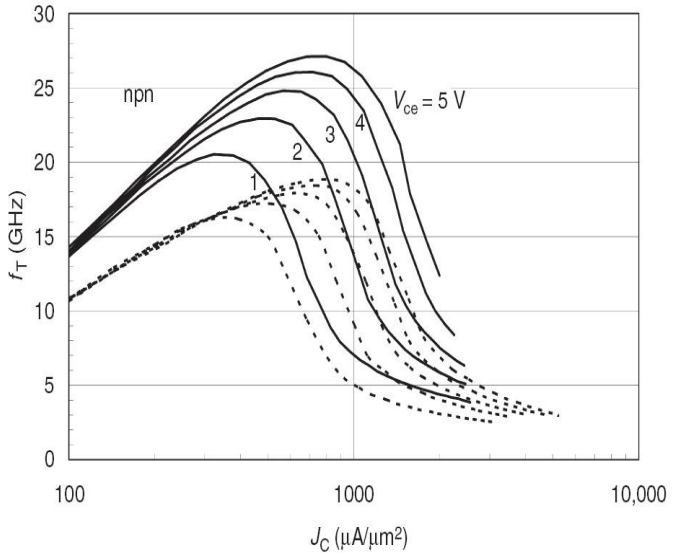

Figure 1.12. Cut off frequency of npn BICOM3X transistor [6].

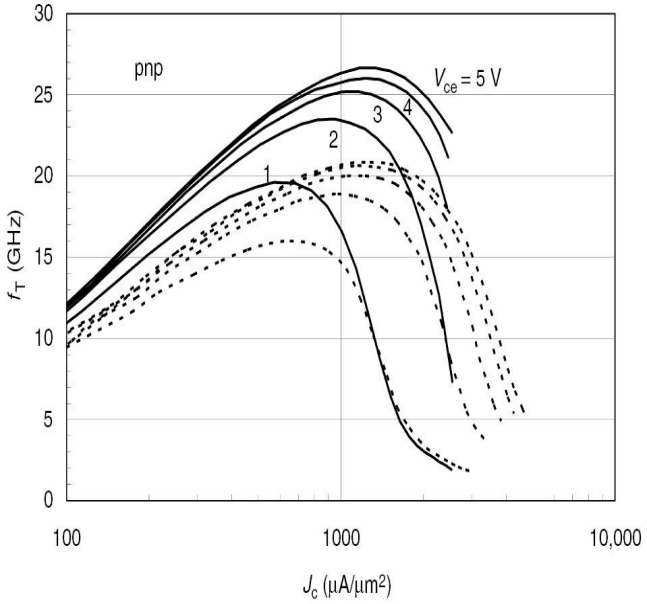

Figure 1.13. Cut off frequency of pnp BICOM3X transistor [6].

TI's Bicom3x is an ideal example of improved pnp. As shown In Figure 1.13, Cut off frequency of pnp transistor is around 28GHz which is similar to the npn transistor.Both npn and pnp have cut off frequency around 25GHz, which shows a very good match between npn and pnp transistor. This is one of the primary requirements of push-pull circuit design. Turn on voltages is slightly asymmetric of npn and pnp devices. There is good amount of difference in inverse characteristics of complementary devices. As shown in Figure 1.10 and Figure 1.11 breakdown voltage are not same for both type of devices. Breakdown voltage of pnp is slightly higher then npn, which auger well for power amplifier (PA) design.

In spite of the historical bias in favor of npn SiGe HBTs, complementary (npn + pnp) SiGe HBT technologies has recently emerged as a viable mixed-signal technology. It is very important to analog market and it enables a wide variety of best-of-breed precision analog

blocks. It can be used in many new circuit applications such as push-pull driver, current sources, and low noise circuits.

1.7 Summary

In Chapter 1, we discussed the importance of VGAs in receiver design and the benefits of SiGe HBT BICMOS technology for wireless applications. Through bandgap engineering by introducing Ge into the base of a transistor, the performance of a standard Si BJT can be greatly improved allowing new high frequency, low-cost, and high performance Si-compatible processing technology [7]. The relationship between device performance and Ge content were highlighted, showing how relevant parameters such as gain, noise figure, and linearity are enhanced. An improved pnp Si HBTs was discussed and its potential use in high performance analog, and wireless markets was shown. Typical third generation performance metrics were shown, focusing on those parameters important as VGA design.

The remainder of this work will focus on actual VGA designs and highlight the performance achievable through the use of C-SiGe HBT BICOM3X technology. Chapter 2 provides a tutorial for designing a high-linear VGA and an example VGA design. Chapter 3 explores the methods for optimization of VGA design for a power constrained application. Chapter 4 explores VGA design in C-SiGe using push-pull complementary design. Chapter 5 concludes by summarizing the results of this work and discussing future research paths.

Chapter 2

VGA Design In C-SiGe HBT BICMOS Technology

2.1 Introduction

As shown in the previous chapter, SiGe HBT technology has remarkable broadband gain, noise, and linearity performance, making these devices well suited for high-frequency amplifier design. This chapter will start with general outline of VGA design focusing on improvement of linearity. The design of an amplifier requires a detailed analysis of the trade-offs involved in meeting the specifications. For instance, the higher the gain of the amplifier, the lower its bandwidth and the higher its non-linearity. Hence, selection of a particular topology is based upon the feasibility of the design meeting most of the specifications, as well as upon a careful consideration of the compromises that need to be made for certain parameters.

2.2 Theory of the Automatic Gain Control System

Ample attempts have been made to describe thoroughly and vividly AGC system in terms of control system theory, from pseudo linear approximations to multivariable systems [1]. The most simple and primary idea of an AGC system is illustrated in Figure 2.1

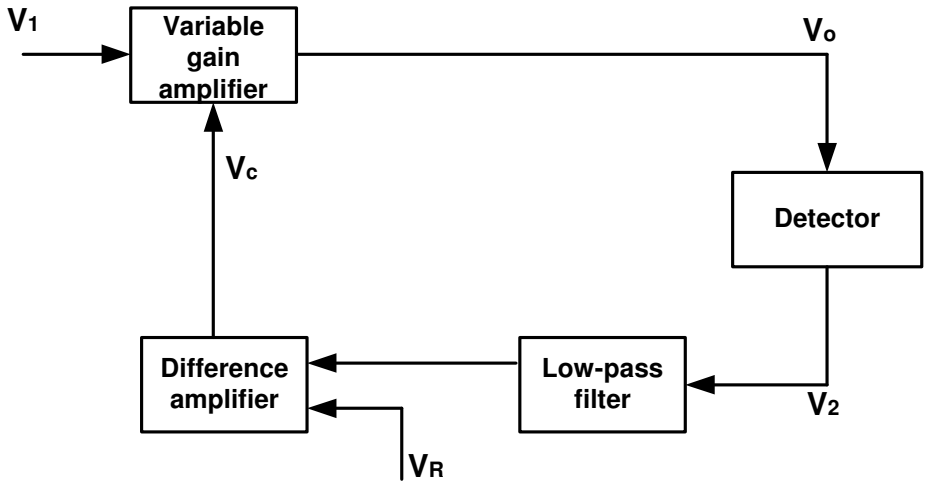

Figure 2.1. AGC Block Diagram.

The input signal is amplified by a variable gain amplifier (VGA), whose gain is controlled by an external signal Vc. The output from the VGA can further amplified by a second stage, if needed to generate an adequate level of Vo. Some of the output signal's parameters, such as amplitude, carrier frequency, index of modulation or frequency, are sensed by the detector. Any undesired component is filtered out and the remaining signal is compared with a reference signal. The result of the comparison is used to generate the control voltage (Vc) and adjust the gain of the VGA. For low input signals the AGC is disabled and the output is a linear function of the input. When the output reaches a threshold value, the AGC becomes operative and maintains a constant output level until it reaches a second threshold value. At this point, the AGC becomes inoperative again. This is usually done in order to prevent stability problems at high level of gain [8].

Unpredictable incoming signal amplitudes from any possible directions necessitate an AGC system in almost every transceiver design of wireless systems. The need for VGA is undoubtedly essential in these systems for normalizing the signal amplitude for further digital

signal processing in the receiver. This makes a VGA an indispensable function block for all radio communications systems. The dynamic range and bandwidth of the VGA range from 20dB to -50dB and frequency from 100MHz to 1GHz depending on particular applications [22]. There are various component and circuit configurations that can be used as a Variable gain amplifier (VGA). The primary factors that must be taken into consideration while selecting a suitable circuit are: desired control range of the VGA, available control voltage, frequency response, linearity, noise, and system configuration.

2.3 Design Consideration of Variable Gain Amplifier

In wireless communication application, the received and transmitted signals have a wide amplitude range depending on the instantaneous signal path and other obstructions. Hence, the transmitter and receiver should have capability to handle this. Thus, one of the important parameters of a variable gain amplifier is its dynamic range. Moreover a basic requirement of the VGA is that gain should exhibit linear-in-dB variation with respect to the control voltage and maintain good linearity over the complete range. Thus special attention is paid to the design of a variable gain amplifier with linear-in-dB gain control. Chapter 3 provides the description of operation of the designed VGA and the blocks involved.

Prior to discussing the advancement of variable gain amplifier (VGA) by studying several typical circuit topologies, it will be beneficial to discuss the basic design requirements of a VGA. This helps to understand the limitation and design challenges often faced by IC designers.

2.3.1 Linear-in-dB gain variation

Traditionally, variations in the gain of a VGA can be obtained by varying the transconductance of a transistor operating in active region. An important feature of VGAs is that the gain should increase exponentially with the controlling voltage/current signals. This transforms into a linear increase in gain or a decibel(dB) scale as in Figure 2.2 below.

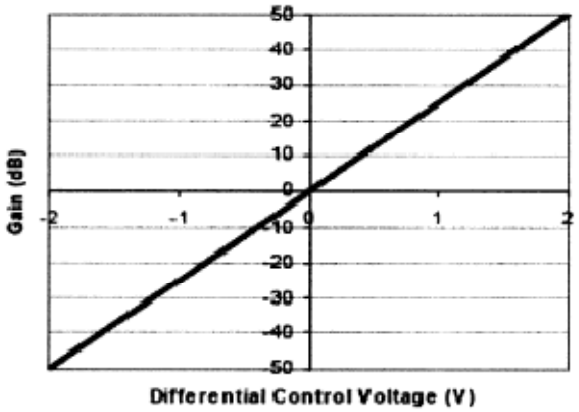

Figure 2.2. Gain Vs. differential control voltage on a semi-logarithmic plot.

The functional dependence of VGA gain on control voltage should be such that the loop gain of the AGC remains constant across the entire operating range of the controlling signal. This property leads to a uniform loop transient response and a guaranteed loop settling time regardless of input signal level. This, in turn, allows a wide dynamic range for the amplifier, as well as makes the settling time of the AGC constant, which is desired in any wireless receiver designs. The inherent exponential property with input voltage of SiGe presents a viable solution.

2.3.2 Dynamic Range

The dynamic range of the gain control is another important parameter of a VGA. Dynamic range is defined as the maximum range of input signal amplitude that the circuit can handle for given limits on noise for small signals and distortion for high signal. In simple words the range of signal power that a system can handle. The main reason for a large dynamic range in gain is the need for low noise figure and low 3^{rd}-order (IM3) distortion. Finally a large input dynamic range of VGA is also required so that incoming signal received will not be distorted due to clipping or attenuation [11].

2.3.3 Higher Bandwidth product

Motivated by the tremendous growth in RF electronics, a good design of VGAs should posses a high and constant gain over a wide region of operating frequencies. Higher gain can be easily obtained by cascading several stages, but this also means and increases in noise level per stage and eventually causes harmonic distortion of the complete circuit. Thus, an extra output stage is often added to existing VGAs to obtain better high frequency response, while still maintaining high and precise trans-resistance. Another viable solution to date is the development of BICMOS process which combines the high-integration feature of CMOS technology and is also capable of possessing high bandwidth product with an exponential relationship.

2.3.4 Low Noise

Noise processes generate incoherent signals, and collectively, do so over a frequency range. In any electrical circuit, signals are subject to degradation and corruption due to the negative effects of physical interaction between travelling electrons. A measure of input noise corruption relative to output noise corruption is called the noise factor (F), if measured in decibels it is known as the noise figure (NF). The VGA is usually used at high frequencies where any noise results in spectral impurity of the frequency band. Hence, a VGA should be designed with minimal noise. In order to reduce the noise contribution from the following stages, the maximum gain of the VGA is maintained larger than unity and is typically around 8dB at maximum gain.

2.3.5 Low Distortion and Intermodulation

While many analog and RF circuits are approximated with a linear model to obtain their response to small signals, nonlinearities often lead to harmful phenomena. If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. The resulting higher order frequency terms, called harmonics, cause distortion in the output. While harmonic distortion is often used to describe the nonlinearities of analog circuits [11], certain cases require other measures of nonlinear behavior, such as intermodulation distortion. A commonly used measure of linearity is the third order intercept point (IP3). This measure describes the real-world scenario of having two input signals spaced relatively close together on the input frequency spectrum, one being the desired signal in the channel of interest and the other being the undesired interfering signal from the adjacent

channel. Most critical are third-order intermodulation (IM3) products that occur at $(2\omega_1 - w_2)$ and$(2\omega_2 - w_1)$. If the difference between ω_1 and ω_2 is small, the components at $(2\omega_1 - w_2)$ and $(2\omega_2 - w_1)$ will appear very close to the original signals. These unwanted signals may cause errors in the detection of the wanted signals. Since a VGA is used to provide a linear control in gain in RF receivers, it should have a high linearity and low distortion [10].

2.4 Concept in Variable Gain Amplifier Design

This section discusses the development of VGAs in the past in terms of design criteria and performance. A differential pair is the main core of any VGA configuration. Hence, the base-driven and emitter-driven pair is analyzed before studying advanced configurations. The inherent exponential property of collector current with the input voltage of bipolar junction transistor makes them and obvious choice to attain a linear-in-dB gain variation.

2.4.1 Exponential property of single HBT

In a HBT the ac-collector current, ic, depends on the base-emitter voltage, V_{BE}, by an exponential relationship of form

$$\boldsymbol{I_C + i_c = I_S . \exp\left(\frac{V_{BE}+v_{be}}{V_T}\right)} \qquad \textbf{(2.1)}$$

In which

I_C is the dc collector current

I_S is the collector saturation current,

$V_{BE}$is the dc base-emitter voltage, and

$V_T = \frac{K.T}{q}$ is the thermal voltage.

For small v_{be} the exponential can be expanded in v_{be} and after rearrangement equation 2.1 becomes

$$\boldsymbol{i_c = g_m . v_{be} . \left[1 + \frac{1}{2}\left(\frac{v_{be}}{V_T}\right) + \frac{1}{6}\left(\frac{v_{be}}{V_T}\right)^2 + \cdots\right]} \quad \textbf{(2.2)}$$

The first-order coefficient g_m is given by

$$\boldsymbol{g_m = \frac{I_C}{V_T}} \quad \textbf{(2.3)}$$

Where $g_m$is the small signal transconductance of the transistor. Consequently, gain can be varied by changing I_C. The higher order terms in equation 2.2 are due to exponential nonlinearity and give rise to signal distortion, commonly measured in terms of harmonic distortion (HD), and intermodulation (IM). Under low distortion the power series in equation 2.2 converges rapidly so that only the second and third order terms need to consider. The distortion is then given by following equation.

$$\boldsymbol{IM_3 = \frac{1}{8}\left(\frac{v_{bep}}{V_T}\right)^2} \quad \textbf{(2.4)}$$

Here v_{bep} is peak value of v_{be}. Series base and emitter resistances in the transistor linearize the exponential relation between $I_C - V_{BE}$ and thus reduce the didtortion. This corresponds however with a reduction in the available gain range

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2.4.2 Cascode amplifier

Similar gain can be obtained by using cascode stage at a significant lower power consumption level [18]. Another advantage of cascode stage is the reduction in miller capacitance, which results into increasing bandwidth.

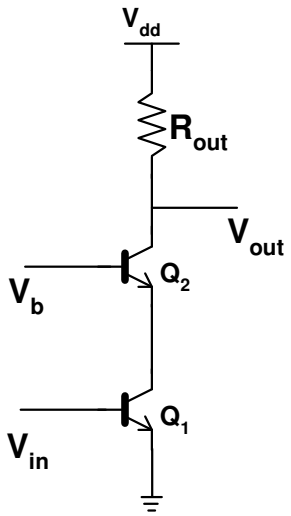

Figure 2.3. Cascode single ended amplifier design.

When this topology is implemented in a VGA, we have few choices for varying gain. Bias voltage at v_{in} can be a choice, but it causes high amount of non linearity into the circuits, which further results into lower IIP3. Output load may be the other choice, but output matching degrades when load resistance varies. To compensate matching, an extra buffer stage can be added, but this will increase power consumption of the circuit. The third viable option is by varying g_m of the base transistor. This technique gives wider gain range, but has a limitation in terms of linearity. As we reduce transcondutace of cascode transistor, circuit moves into more non-linear region as the bottom transistor moves toward saturation. To overcome this problem, we propose a new technique.

This normally results in a better frequency response of the cascode structure as compared to a simple common-source amplifier. A disadvantage of the cascode structure is its limited output voltage swing, as a result of which it is not used frequently in low voltage applications.

2.4.3 Base Driven Differential VGA

The input signal v_i is applied between the bases of a differential pair, and the control signal is applied at the coupled emitters as shown in Figure 2.4. The large values of even-order distortion in the single transistor can be balanced out by applying the input signal v_i between the bases of a matched pair. Varying the common-emitter current I_E changes the gain.

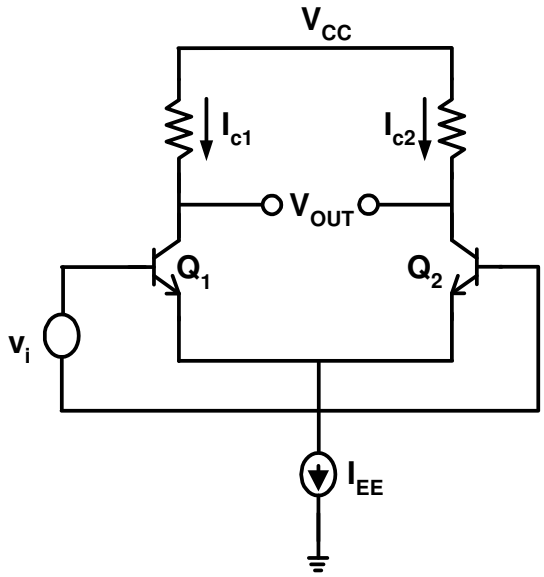

Figure 2.4. Base driven variable gain pair.

If $\beta \gg 1$, signal output current $i_{c2}$is given by

$$\boldsymbol{i_{c2} = I_E.\left[\frac{1}{1+exp\left(\frac{v_i}{V_T}\right)} - \frac{1}{2}\right]} \qquad \textbf{(2.5)}$$

Under low-distortion conditions equation 2.5 can be expanded in v_i and becomes

$$\boldsymbol{i_{c2} = -\frac{1}{4} g_m v_i \left[1 - \frac{1}{12}\left(\frac{v_i}{V_T}\right)^2\right]} \quad \textbf{(2.6)}$$

In which, $g_m = \frac{I_C}{V_T}$. The second order term is zero. The third order terms yields

$$\boldsymbol{IM_3 = \frac{1}{16}\left(\frac{v_{ip}}{V_T}\right)^2} \quad \textbf{(2.7)}$$

Where $\left(\frac{v_i}{V_T}\right)^2$ is the peak voltage of v_i [11].

In practice, small mismatches between transistors cause some second-order distortion. However, since collector currents i_{c1} and i_{c2} have an opposite phase, a differential output can be taken which significantly improves the rejection of even-order distortion. As for single transistor, the presence of base and emitter resistance linear the transfer characteristic so that the available gain variation is exchanged for distortion reduction. The base-driven pair is thus able to suppress even order distortion but decreases the odd order distortion by a factor of only 1.4 compared to a single transistor. A significant improvement in distortion performance can be obtained by applying the signal input as a current via the current source of the differential pair [18].

2.4.4 Emitter-driven variable Gain Pair

Interchanging the position of input signal and gain control signal in the base-driven pair, results in the emitter driven pair are shown in Figure 2.5.

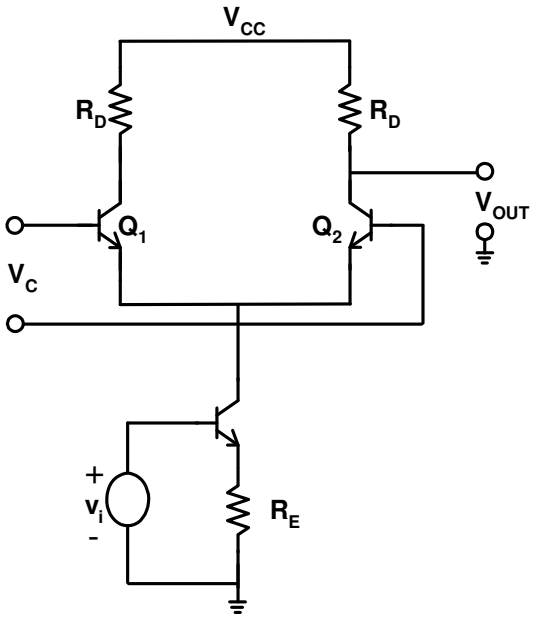

Figure 2.5. Emitter driven variable gain pair.

Input current $(I_E + i)$, in which i represents the AC signal level, feeds both transistors in parallel. DC control voltage, V_B, determines the fraction of the input current that flows in the second transistor and develops output voltage V_{OUT}. At low voltage frequencies, the signal output current i_{c2} is readily found from above equation and is given by

$$\boldsymbol{i_{c2} = \frac{I_E + i}{1 + exp\left(\frac{V_B}{V_T}\right)}} \qquad \textbf{(2.8)}$$

Since equation is linear in input current, no distortions occurs so that the emitter-driven pair is far superior to the base-driven pair. However the input signal must be available as a current. The required voltage-current conversion implies a tradeoff between circuit gain and distortion. Thus the distortion actually present in i_{c2} is never zero but can be made very low at the expense of circuit gain [11].

Whereas the presence of base and emitter resistance improves the distortion performance of base-driven pair, it has a deteriorating effect for the emitter-driven pair. Inclusion of base resistance r_{B1} and r_{B2}in the transistors of Figure 2.5 gives the circuit equation

$$\boldsymbol{I_{c1}\left(1+\frac{1}{\beta_1}\right)+I_{c2}\left(1+\frac{1}{\beta_2}\right)=I_E+i} \qquad \textbf{(2.9)}$$

Which shows that the collector currents are linear in I, but when the drop across the base resistances is also taken into account the output current ratio becomes,

$$\boldsymbol{\frac{I_{c1}}{I_{c2}}=exp\left[\frac{V_B}{V_T}-\frac{1}{V_T}\left(\frac{r_{B1}.I_{c1}}{\beta_1}-\frac{r_{B2}.I_{c2}}{\beta_2}\right)\right]} \qquad \textbf{(2.10)}$$

In which I_{c1} and I_{c2} represent total collector currents. The equation 2.10 is nonlinear if the voltage drops across the base resistances are different [11]. Maximum current gain (0-dB attenuation) is achieved for high negative value of V_B. Almost all of current flows in the transistor Q2, which thus, acts as a current-driven common base stage. As a result, there is no distortions when β is assumed indepent of current. This is also seen from equation 2.9, I_{c1} is then negligible in equation 2.9 and I_{c2} is linear in current. When both transistors carry the same current the exponential in equation 2.10 equals unity. Voltage V_B is zero. Current I_{c1} and I_{c2} are equal and again linear in current. Thus, there is no distortion at an attenuation of 6 dB. For attenuation nearly all the current flows in transistor Q1. Voltage V_B is both positive and large compared with respect to V_T. The ac voltage drop across the base resistance of the current-carrying transistor causes distortion in the attenuated output current. The intermodulation in this case is given by [11].

$$\boldsymbol{IM_3 = \frac{3}{8}\left(r_1 . i_p\right)^2 \frac{1+\frac{r_1}{3}}{1+r_1}} \quad \textbf{(2.11)}$$

Where $r_1 = \frac{r_{B1}.I_E}{(1+\beta_1).V_T}$

All the basic variable gain amplifiers consist of a quadruple of transistors formed from emitter-coupled pairs. Thus, it is worthwhile to examine the noise sources of emitter driven pair. For the emitter driven pair of Figure 2.5, six noise sources have to be considered; thermal noise and shot noise in each transistor, and also the thermal noise associated with resistances R_E, R_B and R_C. At full gain, the pair behaves as a cascode amplifier with gain $\frac{R_L}{R_g}$. The total noise output is low and is mainly due to transistor Q3 and the resistance R_g. However, at half gain, the current in transistors Q1 and Q2 are equal, and the noise due to the base resistances of Q1 and Q2 causes a large output noise peak with a value given by

$$\boldsymbol{V_{CM} = \sqrt{kT.(r_{B1} + r_{B2}).\Delta f}.\frac{I_E.R_L}{V_T}V_{rms}} \quad \textbf{(2.12)}$$

where V_T is the thermal voltage and Δf represents the noise power bandwidth. For increasing attenuation, the current in transistor Q2 decreases such that the contribution of the base resistance noise at the output decreases proportionally. If the pair current is very low, the base resistance noise peak given by equation 2.12 may become lower than the shot noise of Q2 (which decreases only as $\sqrt{I_E}$), or lower than the noise output R_L and R_b, which does not depend on I_E. This is only true for lower value of I_E at which wide band performance is hard to obtain. As a consequence, higher current ar usually chosen, and the maximum noise peak is thus entirely

due to the base resistance in the pair. It is given by above equation and occurs at half the maximum gain [12].

The excellent properties of an emitter-driven pair are realized in the advanced VGA topologies such as the ACG amplifier, the multiplier, the Gilbert's variable gain quadruple, and variable-g_m cell. The use of a balanced quad arrangement results in cancellation of the second-order distortion of the emitter-driven differential pair discussed previously.

2.5 Automatic Gain Control Amplifier

An AGC amplifier, also called the signal-summing VGA is advantageous in terms of low-noise and low distortion characteristics. The circuit employs a base-driven pair with emitter degeneration as a differential current source as shown in Figure 2.6.

The signal-summing VGA can also operate at high frequency, because the gain control stages common base transistors. However, there remains unusable gain-control range of about 20 dB around the maximum gain in linear-in-dB VGAs of this type. This is because the current gain (A_I) dependence on the gain-control signal is given by the following expression.

$$\boldsymbol{A_I = \frac{+I_{out}}{+I_{in}} = \frac{g_{m1}}{g_{m1}+g_{m2}} = \frac{1}{1+exp\left(\frac{V_B}{V_T}\right)}} \qquad \textbf{(2.13)}$$

Where g_{m1} and g_{m2} are the transconductances of Q1 and Q2, respectively. The current gain is approximately an exponential function only for $exp\left(\frac{V_B}{V_T}\right) \gg 1$. This condition requires the VGA to operate with a 20-dB headroom from the maximum gain. This damages the noise performance and reduces the operational gain range [13].

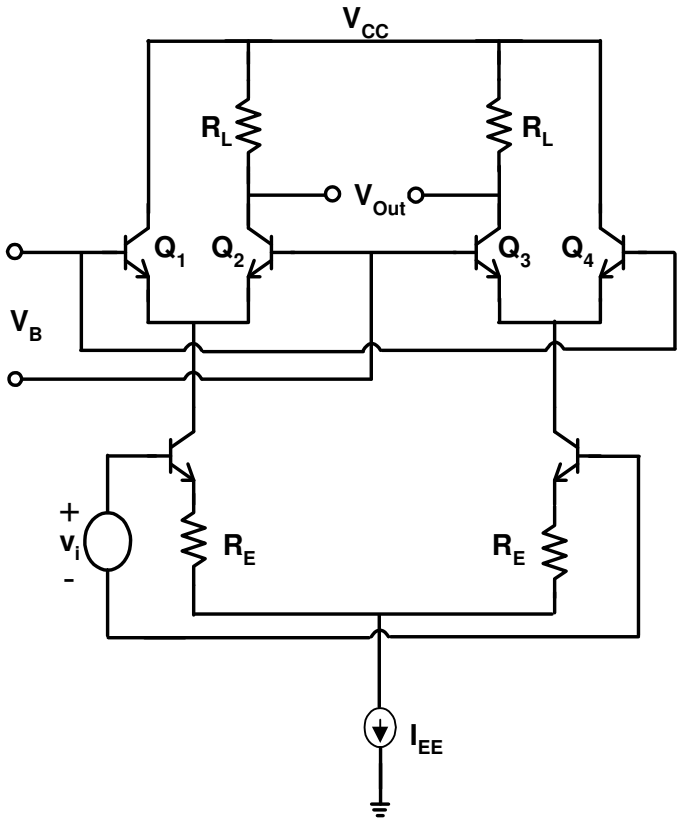

Figure 2.6. Simplified circuit of signal summing (AGC) amplifier.

As the AGC quad shown in Figure 2.6, is formed by balancing two emitter-driven pairs, even-order distortion is absent for perfectly matched transistors. Odd-order components however, add up. For high dynamic range, the AGC amplifier exhibits the lowest distortion and is thus, the best choice. The presence of emitter resistance R_E, or an arbitrary increase in it, decreases the distortion, and also the maximum current gain. Consequently, a tradeoff has to be made between the gain and distortion while choosing emitter resistance R_E [11].

The noise output power of the AGC quad is simply twice that of the emitter-driven pair. At maximum gain, the amplitude of the input signal reaches its lowest value. Whereas at the half maximum gain, where the amplitude of the input signal is twice its lowest value, the value of the

output signal-to-noise ratio S_O/N_O is minimum. For higher input signals, the attenuation increases, and so does S_O/N_O until it levels out because of the noise from R_L. Thus, for a specific minimum requirement in S_O/N_O over the whole dynamic range, only the amount of noise at the half maximum gain has to be examined. Under all other gain conditions, S_O/N_O is higher and automatically satisfies the requirement.

For AGC amplifier at high frequencies, the noise contributions from R_L, Q1, and I_{C4} remain approximately constant, but the noise output voltage due to a r_B decrease with a slope of 20 dB/decade above the -3 dB frequency. In first order analysis, noise generation at high frequencies is thus less important than at low frequencies, and therefore, need not be considered further [12].

2.6 Summary

In this chapter, we have discussed various design techniques of a VGA design. The advantage of these techniques is the ability to achieve linear-in-dB gain-control voltage relationship. These simple designs can provide wide gain range. However, above circuit designs have reflected lower IIP3 and hence, lesser dynamic range of overall system. Another drawback of above design technique is that at lower input power linearity decreases.

In the following chapter, we will focus on a very high linear VGA design. We will incorporate the idea of linearity enhancement using resistive degeneration in our design. We will show how resistive degeneration helps in enhancing linearity. We will also discuss how

complementary design can provide high linearity at lower power consumption using higher order harmonic cancellation technique.

Chapter 3

Design of Variable Gain Amplifier

3.1 Introduction

For communication application at radio frequencies, it is often advantageous to be able to vary the power level to minimize interference problems and maximize battery life of portable products. Thus the variable gain amplifier (VGA) in mobile transmitter plays a crucial role in optimizing system performance. Since multiple users can operate in closely spaced frequency channels, the transmitter gain has to be regulated so that equal power is received at the base station from each user. To vary the transmitter gain, linear-in-dB variable gain amplifier (VGA) is required in the transmit path. There are two options in realizing highly linear wide-gain- range VGA. One is digitally controlled VGA which is comprised of a series of switchable gain stages to adjust the gain discreetly. The other is an analog linear-in-dB VGA which uses a variable transconductance or a variable resistance controlled by an analog gain-control signal. Analog control is preferred because it provides a continuous gain control and needs only one gain control signal line [22].

. In the preceding chapter, VGA design techniques were examined. In this chapter those techniques will be applied in order to design a VGA with analog gain-control signal. The gain control is linear-in-dB. It is a challenge to design an integrated circuit amplifier that operates at RF frequencies and simultaneously has high gain, good input and output matching, low noise

figure, high IIP3, sufficient stability and isolation in a particular package. The design of VGA is based on the following specifications:

Table 3.1. VGA specification.

Parameter	Specification
Gain Range	-7dB to 14dB
Bandwidth	400MHz to 1GHz
Noise Figure	6dB @ Maximum Gain
IIP3	15dbm

These strict IIP3 requirement demands a system with a very good linearity. In the next section, the design of high IIP3 VGA is presented.

3.2 Gain Stage

The critical issues to be considered when designing an amplifier for radio frequency applications are: input and output matching, bandwidth, stability, noise and linearity. Single stage SiGe HBT amplifiers at high frequencies are analyzed below to make a proper choice for the VGA.

- A common–emitter amplifier provides a high gain, high output impedance and moderately high input impedance and low noise. The -3dB frequency of this configuration decreases as the source and load resistances increase. It has relatively low linearity.

- A Common-base amplifier has low input impedance, high output impedance, approximately unity current gain and wide bandwidth. The effect of large load resistances on the frequency response of the common-base stage is much less than that in the common-emiiter stage. It exhibits higher linearity and greater reverse isolation compared to common-emitter stage but has relatively high noise figure.
- A Common-collector amplifier or Emitter-follower provides low gain, large bandwidth, high input impedance and low output impedance. However, the frequency dependence of the terminal impedance may limit the useful bandwidth. It provides good linearity but higher noise figures compared to common-emitter stage.

The above analysis helps in designing an RF VGA utilizing the merits of different configurations as follows: A common emitter stage preceded by an emitter follower improves the IIP3 compared to cascaded common emitter stages. Placing a diode across the base-emitter junction of the emitter follower improves the stability and noise figure, and allows a better IIP3. This also defines the input impedance more predictably than a simple common emitter stage preceded by an emitter follower. The cascode transistor at the output of common-emitter stage increases the reverse isolation.

3.3 Differential VGA Design and Simulation

Keeping the above specifications in mind, a fully differential SiGe VGA has been designed as shown in Figure 3.1.

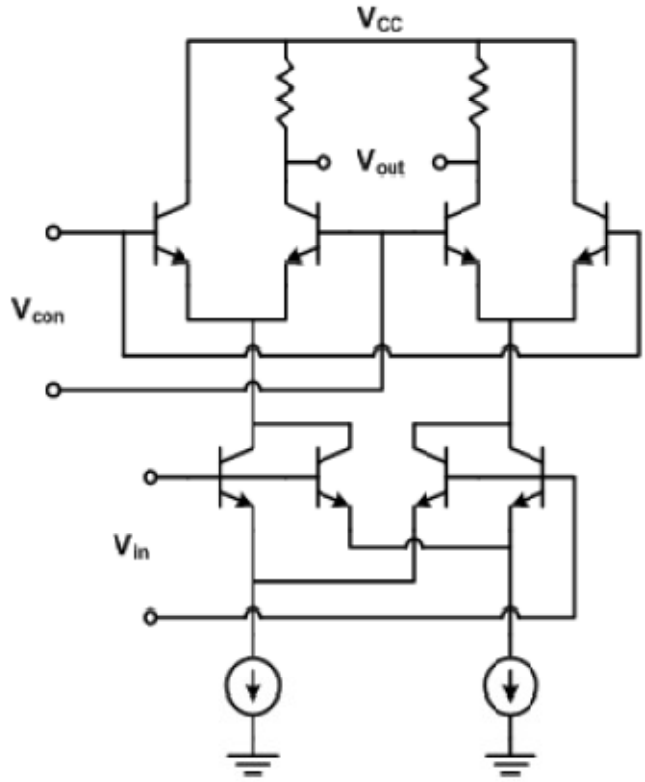

Figure 3.1. Fully differential VGA.

3.4 Frequency analysis

The RF input to the gain stage can be considered to be applied at the base of the bottom transistor. Thus, the RF amplifier circuit given in figure 3.1 can be simplified as shown in figure3.2 which results in a cascode amplifier. The cascode connection is a multiple-device configuration that is useful for high-frequency applications. It consists of a common-emitter stage driving a common-base stage. The transconductance, input and output resistances of this configuration are derived below.

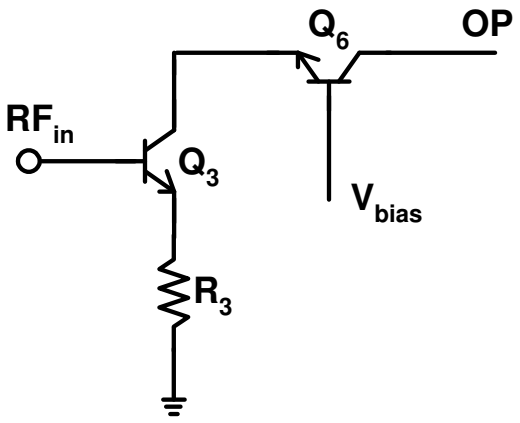

Figure 3.2. Simplified schematic of the RF amplifier-cascode amplifier.

Transconductance

Since the current gain from the emitter to the collector of Q6 is nearly unity, the transcondance of the circuit from input to output is the transconductance of only the common-emitter stage with emitter degeneration.

$$\boldsymbol{G_m \cong \frac{g_{m3}}{1+g_{m3}R_3}} \quad \textbf{(3.1)}$$

Where $g_{m3}$is the transconductance of Q3.

Assuming that the output resistance of the cascade circuit is larger than R_L, the voltage gain of the circuit can thus be written as

$$\boldsymbol{\frac{v_o}{v_i} \cong -G_m R_L} \quad \textbf{(3.2)}$$

Input Resistance

At low frequencies, the input resistance is essentially the input resistance of the common-emitter stage.

$$\boldsymbol{R_{in} = r_{\pi 3} + (1 + \beta_0) R_3} \quad \textbf{(3.3)}$$

Output Resistance

The output resistance can be calculated by shorting the input to the ground and applying a test signal at the output. Then the circuit becomes identical to a common-emitter stage with emitter degeneration. Therefore, the output resistance is

$$\boldsymbol{R_O = r_{O5} \cdot \left(1 + \frac{g_{m3} \cdot r_{O6}}{1 + \frac{g_{m3} \cdot r_{O6}}{\beta_O}} \right)} \quad \textbf{(3.4)}$$

Where β_O is small-signal current gain. If $g_{m3} . r_{O3} \gg \beta_O$ and $\beta_O \gg 1$

$$\boldsymbol{R_O \cong \beta_O . r_{O6}} \quad \textbf{(3.5)}$$

The cascade amplifier is useful at high frequencies because the load for transistor Q3 is the low input impedance of the common-base stage. This makes the Miller effect multiplication factor much smaller. Since the common base has a wide bandwidth, the cascade circuit overall has good high frequency performance. Other useful characteristics include the small amount of reverse transmission and high output resistance.

3.5 Gain Control Stage

The goal for the gain control circuit is to have the same change in control voltage results in proportional change in decibel gain at any signal level. This implies that a linear-in-dB gain control characteristics is required. A linear change in the voltage between the bases of a differential pair of transistors changes their current ratio exponentially. As described by Coffing

[22], this behavior is used to design the gain control circuit with linear-in-dB gain variation.

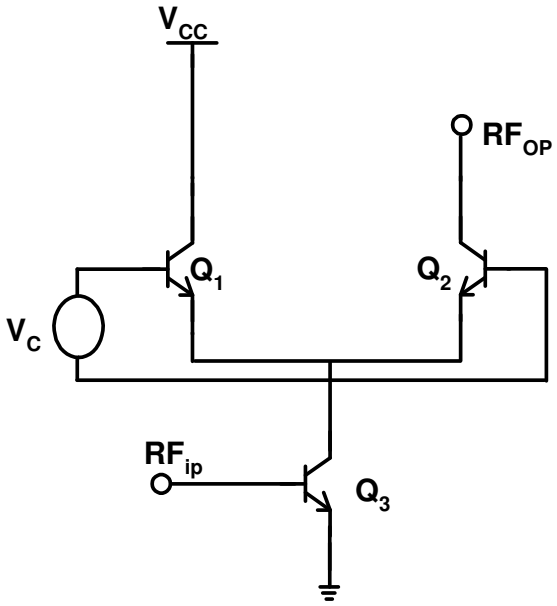

Figure 3.3. Conventional gain control circuit.

A conventional method of implementing the gain-control circuit is shown in Figure 3.3. This is the same as the emitter–driven pair explained in previous chapter. The signal current through Q3 is switched between the differential pair Q1-Q2. The signal is thus split between the two transistors with the collector current from Q2 being used as the output, while the collector current from Q1 is shunted to the supply. A voltage V_C between the bases of the transistors determines the output current and thus the gain or attenuation of the circuit. The gain-control characteristic can be found by solving the ratio of I_{C2}/I_{C3}. The current I_{C2} is the current at the output, and I_{C3} is the bias current at the input. Their ratio describes the gain-control function. As explained below, the ratio of currents in two transistors is an exponential function of their base-emitter voltage differential. The collector current of a transistor can be expressed in terms of its

base-emitter voltage by the following equation.

$$\boldsymbol{I_C = I_2 . exp\left(\frac{V_{BE}}{V_T}\right)} \quad \textbf{(3.6)}$$

Where I_2 is the saturation current and V_T is the thermal voltage. Then the ratio of the two differential pair currents can be written as

$$\boldsymbol{\frac{I_{C2}}{I_{C1}} = \frac{exp\left(\frac{V_{BE2}}{V_T}\right)}{exp\left(\frac{V_{BE1}}{V_T}\right)} = \exp\left(\frac{V_{BE2}-V_{BE1}}{V_T}\right) = \exp\left(\frac{V_C}{V_T}\right)} \quad \textbf{(3.7)}$$

The input bias current I_{C3} is the sum of the two differential pair currents.

$$\boldsymbol{I_{C3} = I_{C2} + I_{C1}} \quad \textbf{(3.8)}$$

Solving for the gain control characteristic gives

$$\boldsymbol{\frac{I_{C2}}{I_{C3}} = \frac{I_{C2}}{I_{C2}+I_{C1}} = \frac{1}{1+\frac{I_{C1}}{I_{C2}}} = \frac{1}{1+exp\left(\frac{-V_C}{V_T}\right)}} \quad \textbf{(3.9)}$$

Whereas, ideally the desirable gain-control characteristic should be linear-in-dB over the entire gain-control range, which corresponds to

$$\boldsymbol{\frac{I_{C2}}{I_{C3}} = exp\left(\frac{V_C}{V_T}\right)} \quad \textbf{(3.10)}$$

The exponential characteristics of the current ratio of two transistors can be used to create a true linear-in-dB characteristic for the current ratio between one transistor and the tail current as shown in Figure 3.3. Thus a truly linear-in-dB gain control is achieved. It is advantageous to use low power signals to control high power outputs.

3.6 Linearity enhancement using resistive degeneration

Even with higher power consumption, linearity performance as demanded by the specification could not be obtained. To overcome this issue, a degeneration resistor was added at the bottom of transistor, where RF input is applied. The principle behind linearization is to reduce the dependence of the gain of the circuit upon the input level [18]. This usually translates into making the gain relatively independent of the transistor bias currents. The simplest linearization method is emitter degeneration with a linear resistor as shown in Figure 3.4. For a common emitter stage and discussed in the previous chapter, degeneration reduces signal swing applied between the base and emitter of transistor, thereby making input and output characteristic more linear [18]. From another point of view G_m can be written as

$$\boldsymbol{G_m = \frac{g_m}{1+g_m R_E}} \qquad \textbf{(3.11)}$$

which for large $g_m R_E$ approaches $1/R_E$, an input independent value. Note that the amount of linearization depends on $g_m R_E$ rather then R_E. With a relatively constant G_m the voltage gain $G_m R_L$ is also relatively independent of input.

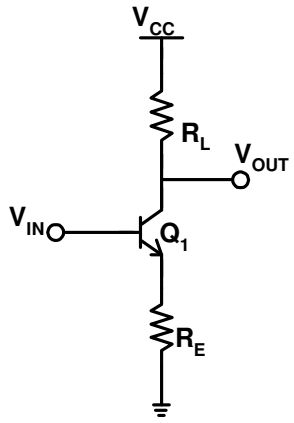

Figure 3.4. Single ended common emitter amplifier with degeneration resistor.

Resistive degeneration presents trade-offs between linearity, noise, power dissipation, and gain. A differential pair can be degenerated as shown in Figure 3.5. Current I_{EE} flows through the degeneration resistors, thereby consuming voltage headroom of $I_{EE}R_E/2$, an important issue if a high level of degeneration is required

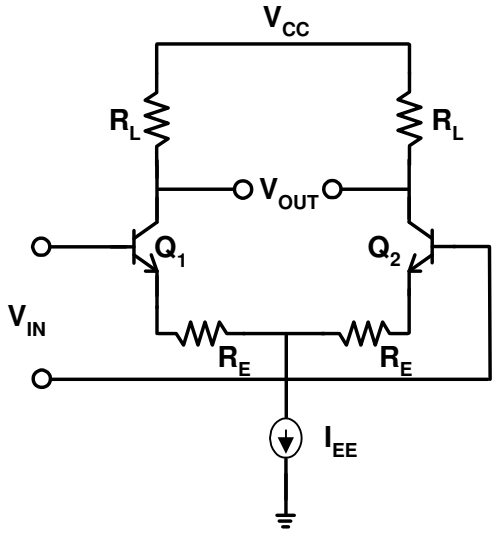

Figure 3.5. Degeneration apllied to differential amplifier:schematic 1.

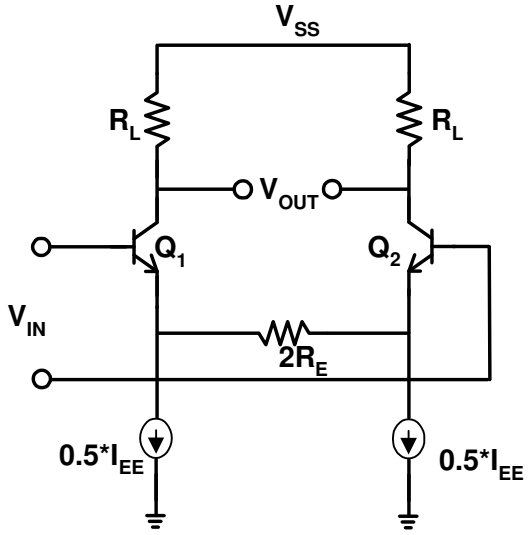

Figure 3.6. Degeneration apllied to differential amplifier:schematic 2.

The circuit of Figure 3.6, on the other hand does not involve this issue but it suffers from

slightly higher noise because the two tail current sources produce differential error [18]. The differential error occurs because it does not see equal impedance from both sides because in one side it see emitter where as on the other side it gets $2R_E$. Figure 3.6 includes differential pairs as its input trans-conductor to convert the input voltage into current. A programmable current mirror acts as a current gain stage to further amplify the current and fixed load resistors provide the linear current-to-voltage conversion at the output of the VGA. This differential structure helps in reducing the 2nd harmonic distortion. Bias current in the input transistor remains same, even if trans-conductance of the cascode transistor varies. Thus the transistor behaves in linearly, even if the gain of the VGA is decreased. Thus, IIP3 of -3dbm can be achieved using this topology. However to increase linearity further a novelty is required. High IIP3 has been achieved by adding degeneration resistance at the input trans-conductance stage. This has a tradeoff of gain and linearity. Degeneration resistance reduces the maximum gain, and hence reduces the gain range. However this tradeoff can be exploited carefully in VGA design.

3.7 Amplifier Layout

The layout is shown in Figure 3.7. The layout of VGA was kept as compact as possible to minimize parasitics. The metal interconnects in the signal path were kept short to minimize RC delays. On-chip decoupling capacitors were added to prevent spurious power supply oscillations from coupling into the circuit. The pad-limited chip area is 1 mm^2.

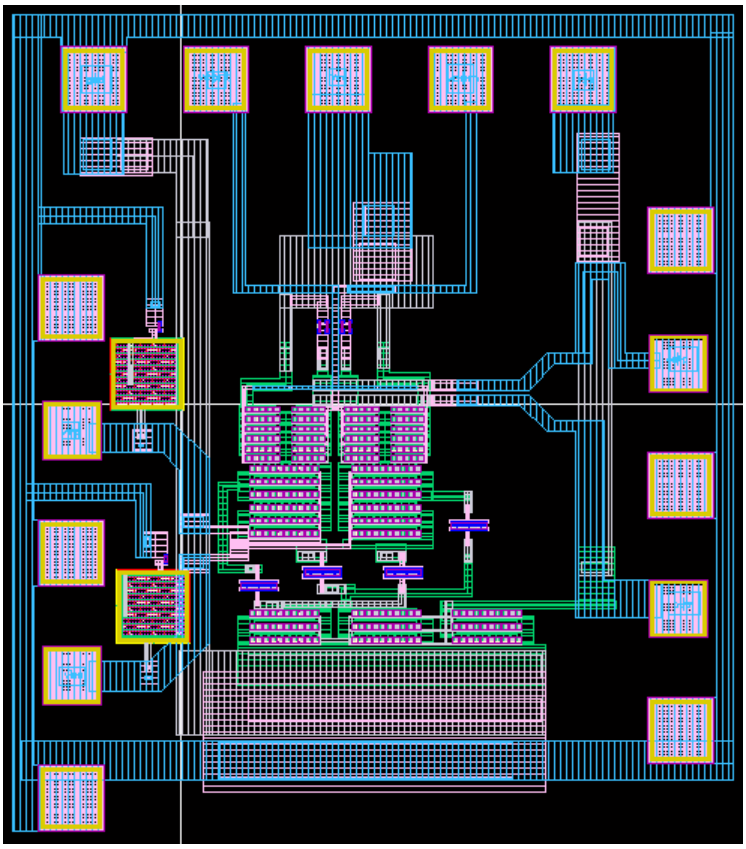

Figure 3.7. Layout of degenerated VGA.

3.8 Simulation Result

Core of the variable gain amplifier, shown in Figure 3.8, was designed using TI's BICOM3X process. Simulation has been done using SpectreRF simulator available in cadence.

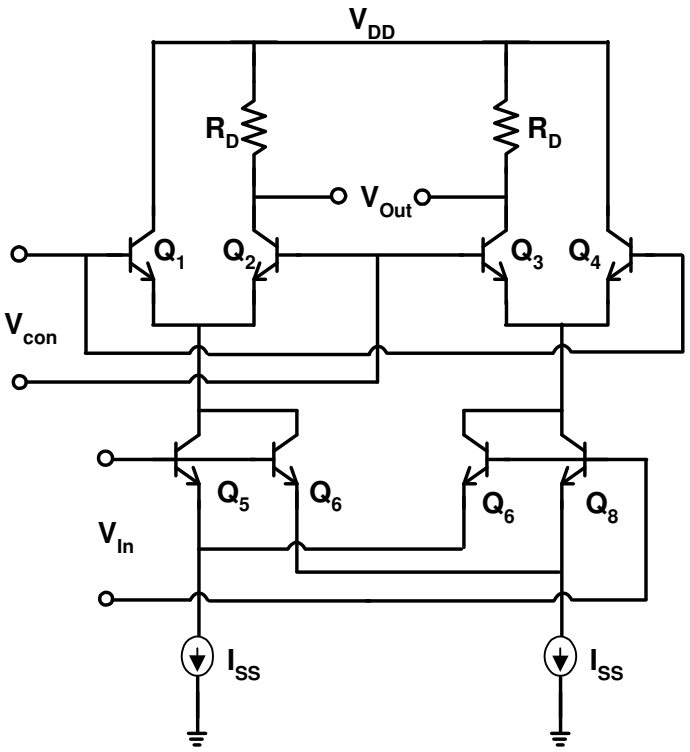

Figure 3.8. Core of variable gain amplifier.

The designed VGA (Figure 3.8) has been simulated with 50 ohm load and source resistance. As shown in Figure 3.9, gain is flat upon few GHz. Our bandwidth requirement was 400MHz to 1GHz, which has been achieved quite comfortably. Linear-in-dB gain control was achieved as shown in Figure 3.10. This has been possible due to exponential I-V relationship of SiGe HBT. It gives a wide range of gain from -65dB to 20dB. It consists of a differential input amplifier feeding a double differential current divider. Variable gain is achieved by adjusting the control voltage (Vcon), thereby varying the signal current fed to the resistive load. The amplifier achieves 70dB of linear-in-dB gain range up to a maximum of 20dB gain (Figure 3.10) and operates across a bandwidth of 3GHz (Figure 3.9) as required by the specifications.

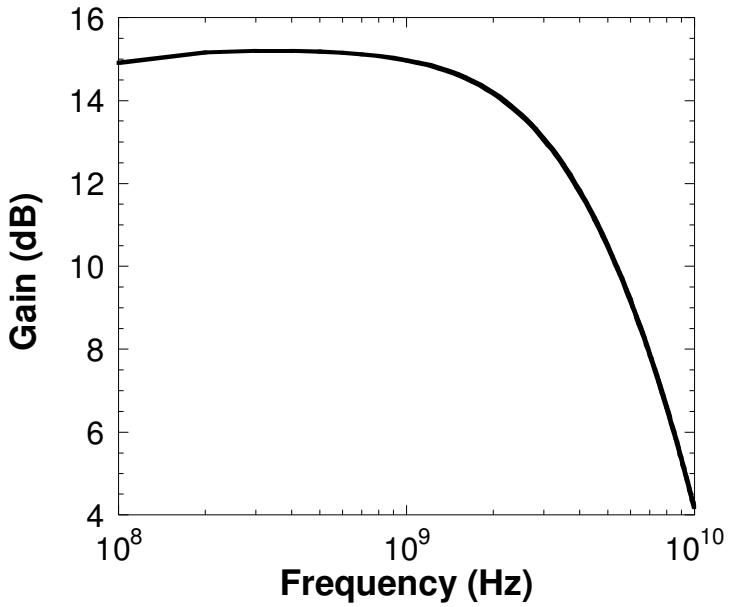

Figure 3.9. Frequency response of VGA.

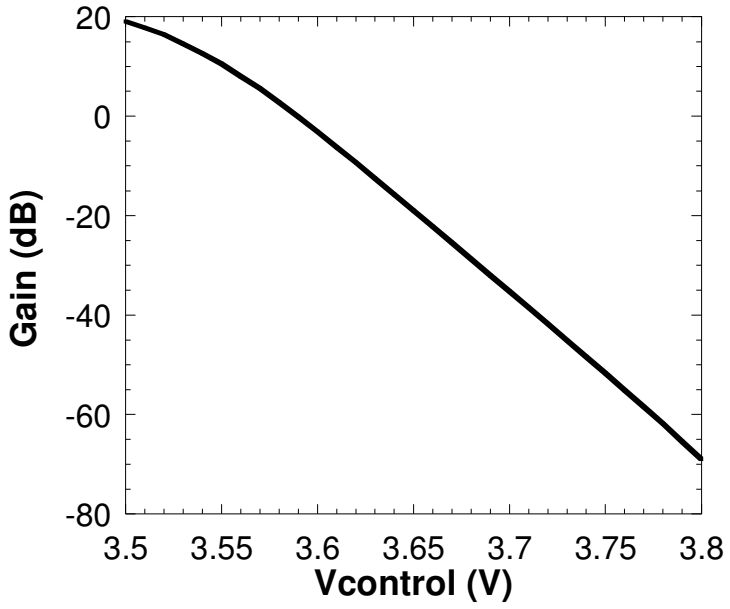

Figure 3.10. Linear-in-dB gain to control voltage.

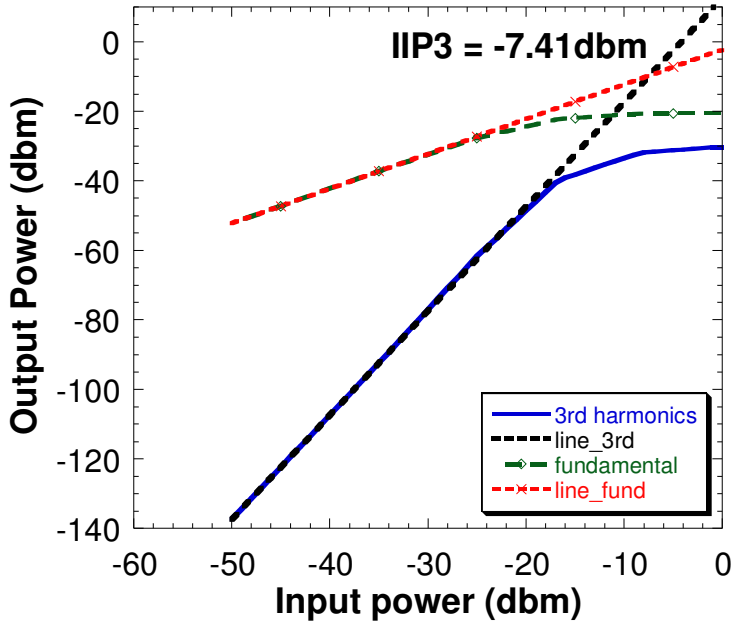

Figure 3.11. IIP3 of variable gain amplifier.

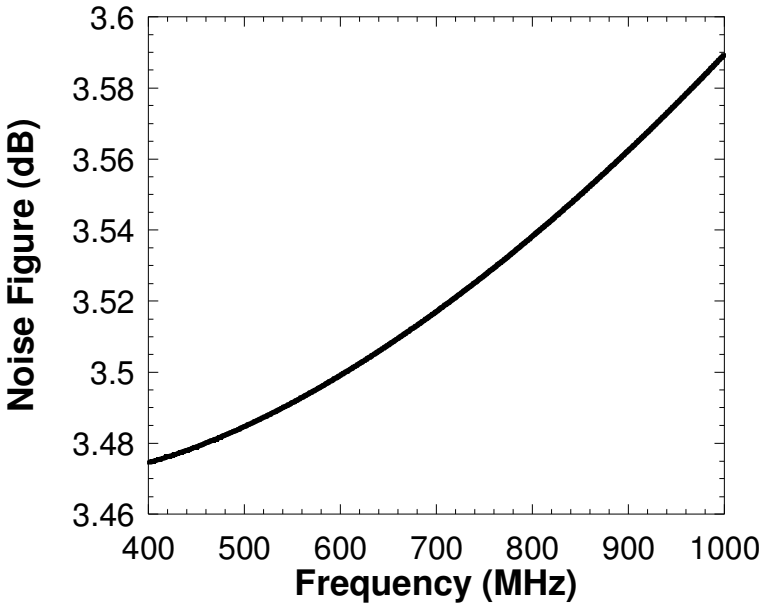

Figure 3.12. Noise figure of variable gain amplifier.

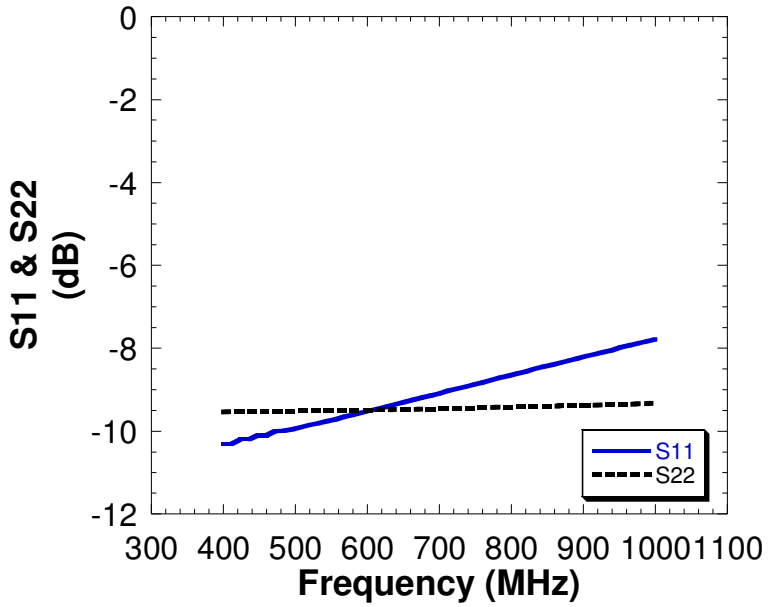

Figure 3.13. Input and output matching of variable gain amplifier.

A noise figure of 4dB, which remains within the requirements of the receiver chain, has been achieved(Figure 3.12) at maximum gain. Emitter lengths of 1.70μm were used for the input pairs, while the devices in the current divider were sized with a ratio of roughly 4 to 1 to improve gain linearity. With this architecture, IIP3 achieved was -7dbm, which is less then the required IIP3. To improve IIP3 we have introduced degeneration as shown in Figure 3.14. It has been discussed in detail in previous chapter how degeneration improves linearity. As value of the degeneration resistance increases IIP3 increases and gain decreases. Hence we have exploited gain vs linearity trade off. It has been summarized in Table 3.2. As degeneration resistance R_E increases gain decreases and linearity increases. Thus a linearity of 15dbm can be achieved using high degeneration resistance of 8ohm.

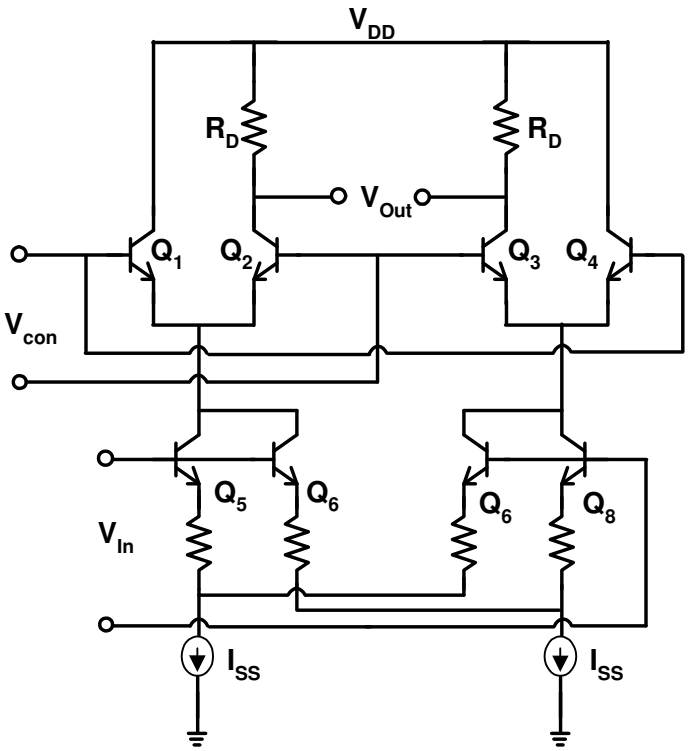

Figure 3.14. core of variable gain amplifier with degeneration.

Table 3.2. IIP3 and gain vs degeneration resistance.

	Maximum Gain (dB)	IIP3 (dbm)
Without resistive degeneration	20	-7.41
Resistive degeneration (4 ohm)	15	4.88
Resistive degeneration (8ohm)	10	15.04

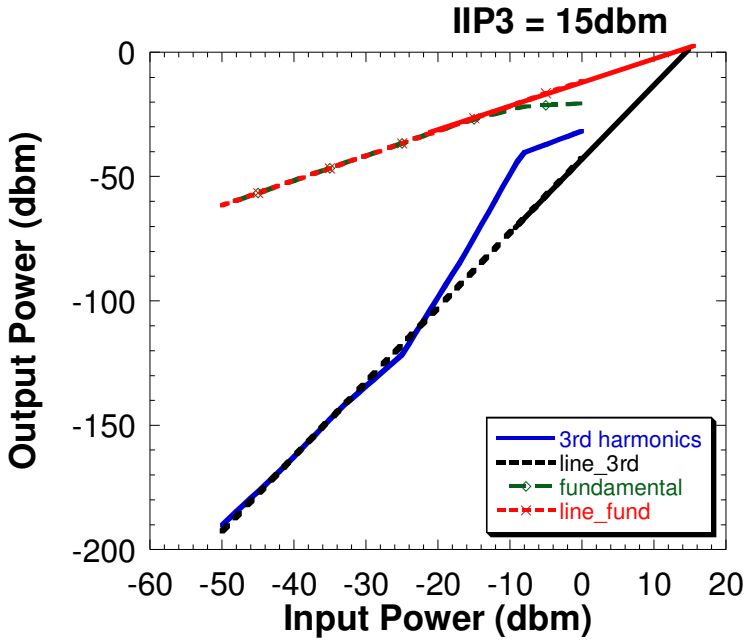

Figure 3.15. IIP3 of variable gain amplifier using degeneration resistance of 8ohm.

3.9 Summary

In this chapter, analysis and design of a linear SiGe HBT VGA have been presented. This VGA demonstrate very high IIP3. The designed VGA is well suited for wide range of applications such as wireless communication in GSM and mobile technology. A designer has many options of choosing gain and linearity for their VGA design, depending on system requirements. This VGA also highlights the potential of using SiGe HBT technology for highly linear amplifier design.

Chapter 4

Complementary VGA

4.1 Introduction

Integrated complementary npn/pnp transistors add new dimensions to the application base of heterojunction bipolar transistor (HBT) technology. Power consumptions can be reduced and circuit performance and efficiency can be improved using complementary HBTs. One such example is the use of active loads, which can replace load resistors of differential pair stages in operational amplifiers. This would reduce voltage supply required, and increase the voltage gain of differential stage [16].

Another application of complementary HBTs is for high efficiency push-pull amplifiers. This can be realized without the need for complex transformer circuits to implement 180^0 baluns. The push-pull amplifier is a basic building block of many bipolar applications, including output stages in operational amplifiers, oscillators, and power amplifiers which need to efficiently drive low impedance load [20].

As in low frequency circuits, the availability of high performance pnp HBT's will make the high-efficiency complementary microwave amplifier implementation feasible. In contrast to conventional push-pull amplifiers using an identical device type for each type of amplifier, a complementary amplifier does not need an external 180 degree phase shifters (or baluns) for high efficiency class AB push-pull amplifier, since the required phase reversal can automatically be achieved by using complementary pnp/npn HBT pair [20]. The development of high-

performance, complementary push-pull amplifier at microwave frequencies has been hampered by the lack of matched high-performance pnp HBTs. In BICOM3X process they are well matched in terms of cutoff frequency and phase delay. The push-pull operation also helps to cancel 2nd order harmonics at the output [20].

4.2 Circuit Design

The circuit diagram shown in Figure 4.1 is core of the complementary variable gain amplifier. It has two signal path, one is coming from npn common emitter amplifier, and the other is from pnp common emitter amplifier.

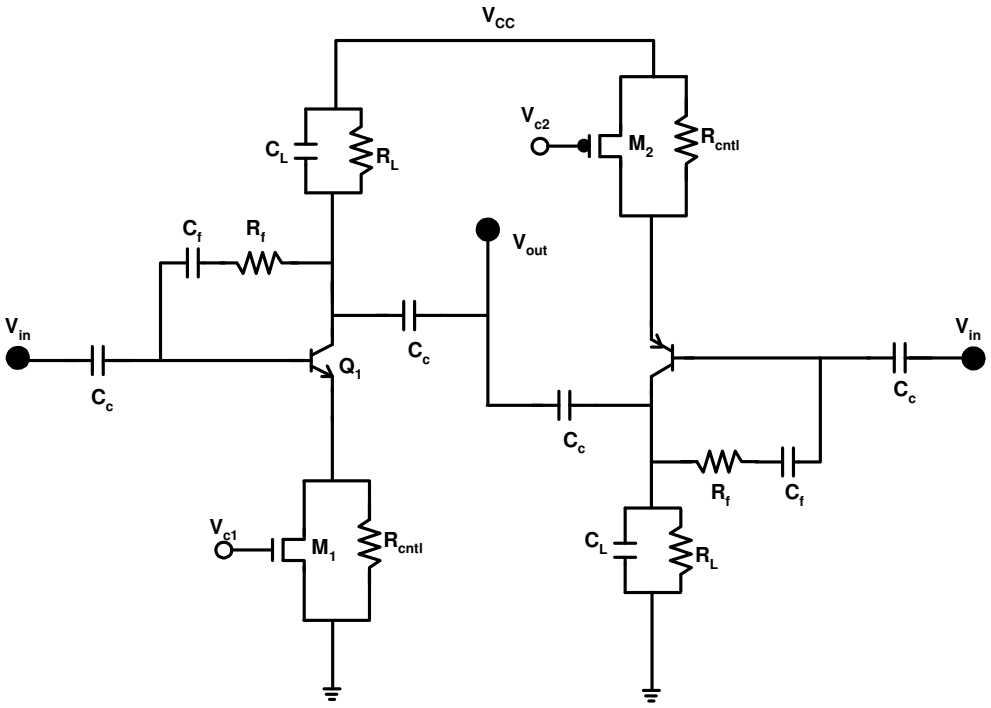

Figure 4.1. Schematic of complementary VGA.

Both paths has been designed in such a way that they keep phase shift to a minimum. It helps in increasing output power and reducing cross over distortion. It needs two separate control voltage in order to vary gain. These control voltage need to be very specific in order to get the benefit of higher order harmonics cancellation. Higher order harmonics are cancelled when both signals path have same gain from both paths. If the gain does not match i.e. control voltage is not accurately managed then the benefit of push-pull operation is not fully realized. In this design variable gain has been achieved by varying mos resistance [17]. Nmos transistor was kept in linear region.

4.2.1 MOS as Linear Resistor

In this design variable gain has been achieved by varying mos resistance [17]. Nmos transistor (Figure 4.2) was kept in linear region of operation. Since mos is operating in linear region, drain current I_D can be given by

$$\boldsymbol{I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]} \quad \textbf{(4.1)}$$

Where $V_{GS} - V_{TH}$ is the "overdrive voltage" and W/L the "aspect reation". If $V_{DS} \leq V_{GS} - V_{TH}$, then device operates in "linear region"[18].

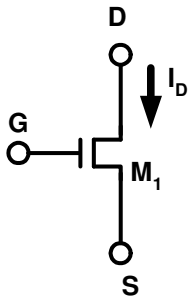

Figure 4.2. Mos transistor.

Above equation is the basic of mos behavior in deep triode region [18]. If $V_{DS} \leq 2(V_{GS} - V_{TH})$,

$$\boldsymbol{I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}} \quad \textbf{(4.2)}$$

Clearly drain current is linear function of V_{DS}. The linear relationship implies that the path from the source to drain can be represented by a linear resistor equal to

$$\boldsymbol{R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}} \quad \textbf{(4.3)}$$

A MOSFET can therefore operate as a resistor whose value is controlled by the overdrive voltage [18].

4.2.2 Linear Gain-Control Relationship

As shown in Figure 4.1, using equation 3.12 and 4.3, G_m can be given as

$$\boldsymbol{G_m = \frac{g_m}{1 + g_m R_E}} \quad \textbf{(4.4)}$$

When $g_m R_E \gg 1$, then

$$\boldsymbol{G_m = \frac{1}{R_E}} \quad \textbf{(4.5)}$$

Here R_E is resistance of mos from source to drain as given by equation 4.3. Using value of R_E

$$\boldsymbol{G_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \quad \textbf{(4.6)}$$

Here V_{GS} is control voltage, and when $V_C = V_{GS} \gg V_{TH}$,

$$\boldsymbol{G_m = \mu_n C_{ox} \frac{W}{L} V_C} \quad \textbf{(4.7)}$$

Thus voltage gain can be expressed as

$$v_{gain} = G_m R_L \quad \textbf{(4.8)}$$

$$v_{gain} = \mu_n C_{ox} \frac{W}{L} R_L \, V_C \quad \textbf{(4.9)}$$

Thus voltage gain v_{gain} is linear function of control voltage v_c.

4.2.3 Harmonic Cancellation

As shown in Figure 4.1, there are two paths of output from input. One path contains gain from npn and other from pnp. If both gain values are close, then their 2nd harmonics at output are out of phase and they cancel each other. Gain from npn is controlled by v_{c1} and pnp gain is controlled by v_{c2}. For harmonic cancellation v_{c1} and v_{c2} are need to be of very specific value.

4.2.4 Amplifier Layout

The layout is shown in Figure 4.3. The layout of VGA was kept as compact as possible to minimize parasitic. The metal interconnects in the signal path were kept short to minimize RC delays. The layout of complementary signal paths were kept symmetrical to obtain matching delays in these signal paths. On-chip decoupling capacitors were added to prevent spurious power supply oscillations from coupling into the circuit. The pad-limited chip area is 0.9 mm^2.

4.3 Simulation Result:

One of the features that separate this VGA is that it offers linear absolute gain rather the linear-in-dB gain. It offers a gain range from -7 dB to 12 dB. Also the absolute gain has linear

characteristics as shown in Figure 4.4. Another aspect of this design is that its linearity increases as gain decreases. Clearly, VGA will work in low gain mode when it receives higher input power. The VGA delivers high linearity in low gain mode, as required by high input power level.

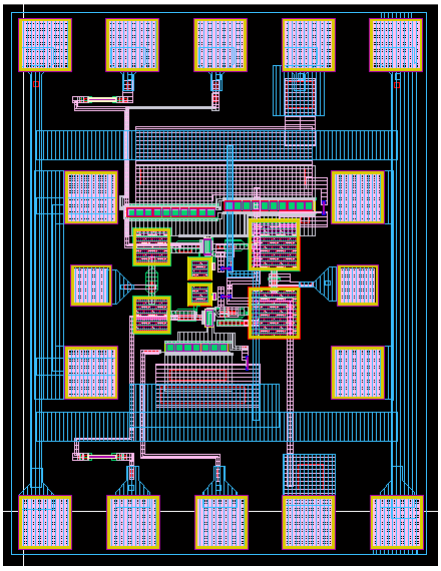

Figure 4.3: Layout of complementary VGA.

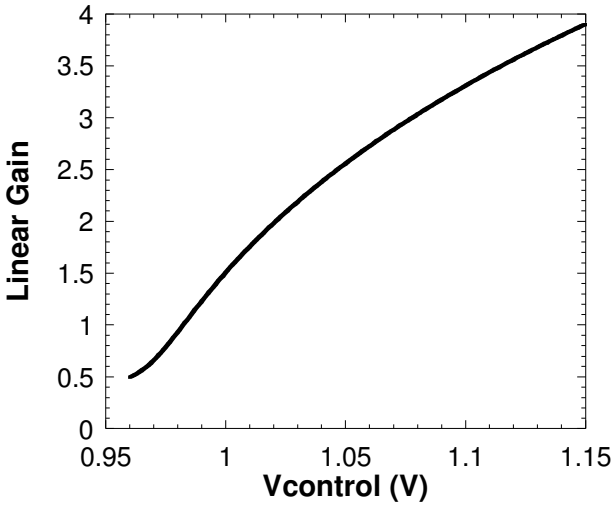

Figure 4.4: Gain vs Control voltage.

Output spectrum has been plotted in Figure 4.5. If control voltage is precisely controlled to cancel third harmonics, it results into very high IIP3 at lower power consumption. One important note is that if control voltage is not precisely controlled then it does not improve the IP3 performance of VGA design. Certainly in such scenario one do not get advantage of harmonics cancellation in IP3. Another aspect of this design for linearity is that its IP3 increases as gain of circuit decreases. This can be understood from the fact that as resistance increases gain decreases, and hence linearity increases. Noise performance of this circuit is also excellent (Figure 4.6). At maximum gain noise figure is less then 3.5dB. Such a good noise figure was achieved because of C-SiGe HBT devices, which has excellent noise performance [16].

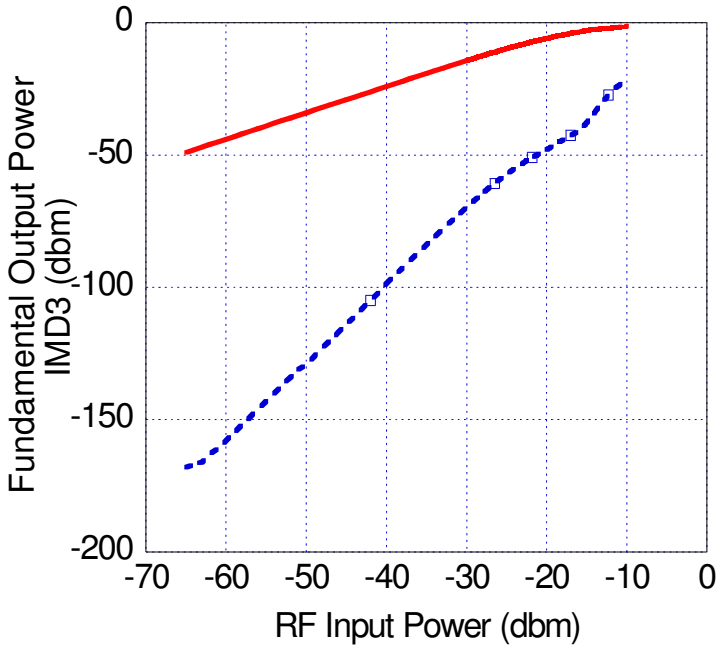

Figure 4.5. Power spectrum of C-SiGe VGA.

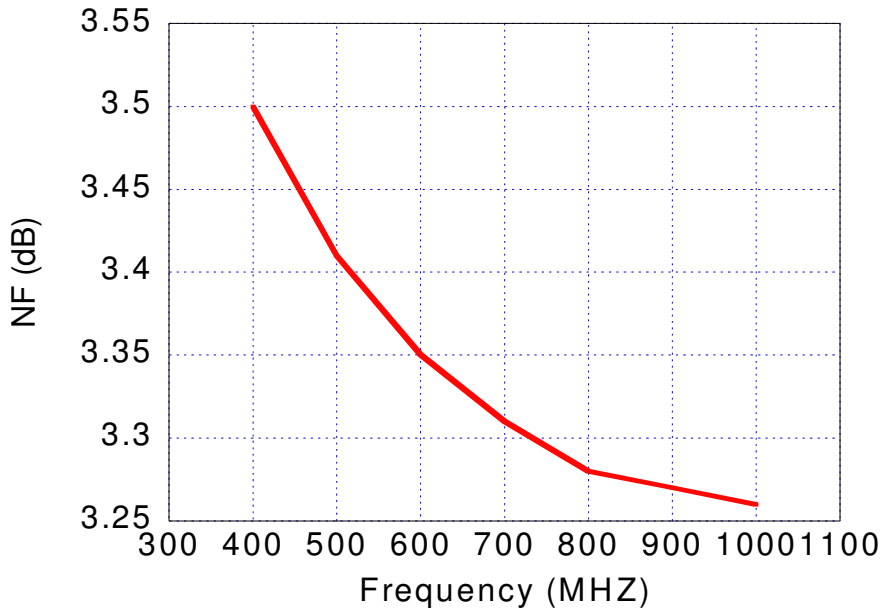

Figure 4.6. Noise figure of C-SiGe VGA.

4.4 Summary

In this chapter, analysis and design of a linear complementary SiGe HBT VGA have been presented. This VGA demonstrates very good linearity at lower power consumption. Higher order harmonic cancellation technique was for the novel VGA design. The designed VGA is well suited for wide range of applications such as wireless communication in GSM and mobile technology. This VGA also highlights the potential of using SiGe HBT in wireless communication circuits.

Chapter 5

Summary

5.1 Conclusions

As we have demonstrated in this thesis, SiGe HBT VGAs have the capability to meet the demanding needs for future generation wireless system. Combining the performance improvements of the SiGe HBT with high IIP3 VGA design and optimization schemes yields a very good performance, capable of achieving 15dbm IIP3. Throughout this thesis, we have presented a thorough analysis of VGA design and optimization, providing both simulated and measured results and a framework for understanding the design trade-offs and optimization schemes required for these designs.

In chapter 1, we reviewed the importance of VGA in wireless communication system and their impact on receiver performance. The benefits of SiGe HBT technology were introduced and linearity related characteristics were highlighted. We analyzed gain and linearity in SiGe HBT.

Chapter 2 concentrated on VGA design and introduced basic design of amplifier. Various techniques of achieving variable gain have been explored. Linearity related parameters were highlighted. We end this chapter with an example of a fully differential VGA using SiGe HBT technology.

In Chapter 3, we used a modification of the previous technique to present a design for high IIP3 VGA's. The design process, simulation, and layout for this SiGe HBT VGA were presented and shown to have good performance. However such a high IIP3 was difficult to

achieve with the traditional design due to nonlinearity contribution from device. Simulation results have been presented and shown to satisfy all the given specifications.

In Chapter 4, we presented a complementary VGA. We applied the idea of push-pull operation in VGA design. The design process, simulation and layout for this SiGe HBT VGA were presented and shown to have good performance. It offers us high IIP3 at lower power consumption. However it does not have linear-in-dB gain control.

In Conclusion, we present a thorough analysis of various aspects of SiGe HBT VGA design. The aim of the analysis presented herein was to provide designers with the fundamentals of designing SiGe HBT VGAs. Both relevant design and simulated results were presented. Through these designs and examples, we highlight the potential of using SiGe HBT technology to develop the next generation of wireless and communication systems.

5.2 Future Work

This thesis provides a general overview of VGA design, and provides some concrete example of linear VGA design and their simulated results. There are many opportunities to extend this research to new areas and further understand both SiGe HBT linearity performance and VGA design. Some of these new opportunities include: Current reuse push-pull VGA design, better gain control relationship, and low power VGA design.

Linearity can be further be increased by understanding, and cancelling higher harmonics term using complementary devices in differential mode. Currently dynamic range enhancement is a very active research area in wireless communication. A Linear VGA design has been

explored in SiGe HBT BICOM3X technologies. However, additional research could provide more insight into device and circuit optimization, dynamic range improvements, decreased power consumption, and increased bandwidth.

Immediate step of this work would be to measure the fabricated. Linearity measurement of differential amplifier is going to be the big challenge for future work. Also for complementary VGA, control voltage need to be very precise for complementary VGA design. SiGe HBT VGA could provide high linearity with low noise figure, and at lower power consumption.

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