AUTOMATED DESIGN OF MICROWAVE DISCRETE TUNING DIFFERENTIAL CAPACITANCE CIRCUITS IN Si-INTEGRATED TECHNOLOGIES

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ABSTRACT: *A genetic algorithm used to design radio-frequency binary-weighted differential switched capacitor arrays (RFDSCAs) is presented in this article. The algorithm provides a set of circuits all having the same maximum performance. This article also describes the design, implementation, and measurements results of a 0.25* **1***m BiCMOS 3-bit RFDSCA. The experimental results show that the circuit presents the expected performance up to 40 GHz. The similarity between the evolutionary solutions, circuit simulations, and measured results indicates that the genetic synthesis method is a very useful tool for designing optimum performance RFDSCAs.*

Key words: *automated circuit synthesis; genetic algorithms; RF integrated circuits; RF switched capacitor arrays; RF tuned circuits*

1. INTRODUCTION

The radio-frequency switched capacitor arrays (RFSCAs) have a great potential for use in reconfigurable or adaptive radio-frequency (RF) circuits for actual and future wireless transceivers, because they allow a large capacitance tuning range with small tuning steps, when maintaining its quality factor at acceptable values. Moreover, these circuits have no power consumption, which is an important aspect when the transceivers are powered by a battery. At present, RFSCAs can be found in multistandard low-phase-noise ultra-wide-band voltage controlled oscillators [1], in fast-settling time frequency synthesizers [2], in process dispersion compensation techniques [3] and in adaptive imped- ance matching circuits [4].

Optimization and search tools, such as, the genetic algorithms (GAs) [5], have been progressively used to automate the design of RF integrated circuits [6–8]. An algorithm to design optimum performance radio-frequency and microwave binary-
weighted differential switched capacitor arrays (RFDSCAs) is presented in this article. This new approach, based on e-concept [9] and maximin sorting scheme [10], provides a set of solutions well distributed along an optimal front. Each GA solution that
corresponds to a distinct implementation of the desired RFDSCA meets the initial design specifications and has the same maximum performance as the others. This method has better performance than the one already reported in the scientific

literature [11], because it reduces substantially the solutions dispersion along the optimum front. The reported method, based on sharing scheme [12], presents a poor solutions distribution and, consequently, an undefined front.

To provide a better insight into the design of RFDSCAs with optimum performance, a case study is presented. Bearing this idea in mind, all the design steps, including the specifications, circuit synthesis, SpectreRF simulations, implementation, and measurements, are performed. The design used a 0.25 **l**m BiCMOS technology. The measurement results demonstrate that the implemented 3-bit RFDSCA has a high minimum quality factor and presents the expected performance up to 40 GHz. The similarity between the evolutionary solutions, circuit simulations, and measured results clearly shows that the proposed RFDSCA synthesis procedure constitutes a very powerful design tool.

This article is divided in four sections. Section 2 presents the behavior model of the RFDSCAs, the developed GA, which is used to synthesize several RFDSCA circuits, and the design steps that must be followed to implement successfully an optimum performance RFDSCA. Section 3 presents a case study, namely, the design, simulation, implementation, and measurements results of a microwave RFDSCA. Finally, Section 4 draws some conclusions.

2. RFDSCA DESIGN PROCEDURE

This section describes in detail the automated synthesis procedure adopted for designing optimum performance RFDSCAs. In this sense, it begins by presenting the closed-form mathematical expressions that characterize the RFDSCA behavior. After that, the developed GA, which is the core of the automated design procedure, is described. Finally, the section ends with the enumeration of the required steps that should be followed to design successfully an optimum performance RFDSCA.

2.1. The RFDSCA Behavior Model

The simplified circuit of a RFDSCA is illustrated in Figure 1. This schematic has a similar topology to the one reported in [11]. The changes introduced in the single-ended RFSCAs model were done to account for the use of a differential topology. Figure 1 shows that the RFDSCA circuit can be divided in *N* different cells. The first cell, which is the reference cell, comprises two reference capacitors with value *C* and a reference switch. The other cells of the RFDSCA are constituted by two cell capacitors and a cell switch. The capacitance value of the

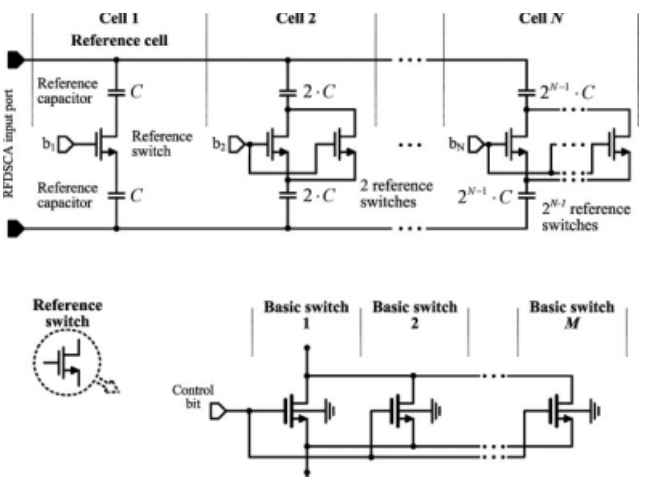

Figure 1 Generic RFDSCA schematic

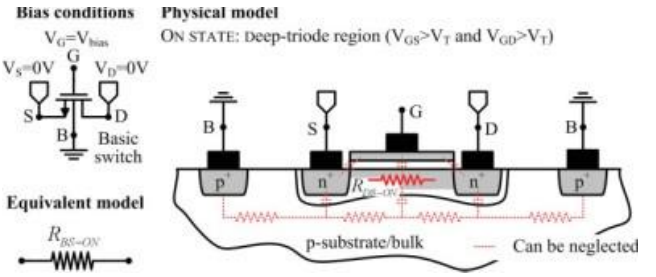

Figure 2 Basic switch model: ON state. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

cell capacitors is equal to $2^{k-1}\cdot C$ and the number of reference switches of each cell is given by 2^{k-1} (*k* is the number of the cell, $1 < k :; N$). Figure 1 also shows that the reference switch is formed by placing in parallel *M* basic switches (BS).

The BS, implemented with MOS transistors, has two dominant sources of loss: the channel resistance when the transistors operate in the deep triode region, $R_{\text{BS-ON}}$ (BS-ON) (Fig. 2), and the substrate resistance when the transistors are in cut-off region, R_{sub} (BS-OFF) (Fig. 3). Both resistances limit the maximum achievable quality factor of the RFDSCA (Q_{RFDSCA}). Furthermore, in the cut-off region, it is important to consider the substrate-drain junction capacitance, C_{subD}, the substrate-source junction capacitance, C_{subS}, the gate-drain capacitance, C_{GD}, and the gate-source capacitance, C_{GS}, because these elements have a major impact upon the RFDSCA minimum capacitance and the maximum attainable Q_{RFDSCA}. Taking into account the aforesaid considerations and the NMOS physical model represented in Figures 2 and 3 [13], the simplified BS model for the ON and OFF states can be represented by the equivalent circuits of Figures 2 and 3 [14] [15], respectively. Note that the BS-ON resistance, $R_{\text{BS-ON}}$, the BS-OFF resistance, $R_{\text{BS-OFF}}$, and the BS-OFF capacitance, $C_{\text{BS-OFF}}$, are highly dependent on the fabrication process, layout, and bias conditions.

The RFDSCA can be modeled as a nonideal controlled capacitor. The RFDSCA input admittance can be described by the following:

$$\bar{Y}_{\text{RFDSCA}}(D,f) = \frac{1}{R_{\text{RFDSCA}}(D,f)} + j\cdot 2\cdot\pi\cdot f\cdot C_{\text{RFDSCA}}(D,f), \tag{1}$$

where C_{RFDSCA} and R_{RFDSCA} represent the RFDSCA equivalent parallel capacitance and resistance, respectively. In this equation, *D* is the control word and *f* represents the operating frequency. The control word $D = b_N\cdot 2^{N-1} + \ldots + b_2\cdot 2^1 + b_1\cdot 2^0$ is the decimal representation of the binary word $[b_N \ldots b_2\ b_1]$

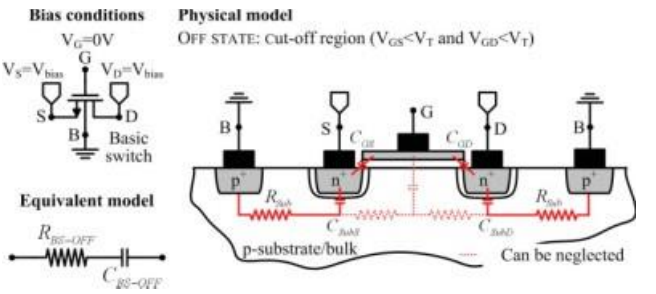

Figure 3 Basic switch model: OFF state. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

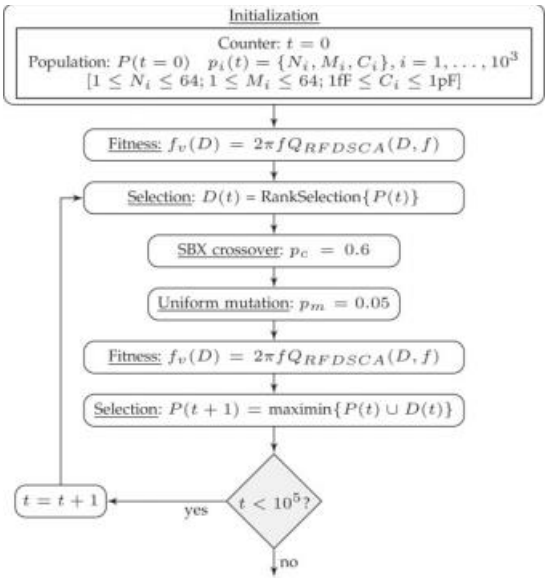

Figure 4 Flowchart of the genetic algorithm

(control bits). This relation is fundamental in the following analysis, because the closed-form mathematical expressions use D as an independent variable. Moreover, $D_{MAX} = 2^M - 1$ corresponds to the maximum value of D.

It can be demonstrated, considering the RFDSCA topology and the BS equivalent circuit, that the equivalent capacitance and quality factor of the RFDSCA are expressed by (2) and (3), respectively.

$$C_{RFDSCA}(D,f) = \frac{D \cdot \frac{C}{2} + D_{MAX} \cdot M \cdot C_{BS-OFF}}{1 + \frac{2M \cdot C_{BS-OFF}}{C}} + 0 \cdot f \quad (2)$$

$$Q_{RFDSCA}(D,f) = \frac{\left(1+\frac{2M \cdot C_{BS-OFF}}{C}\right) \cdot \left(1+\frac{D}{D_{MAX}} \frac{C}{2M \cdot C_{BS-OFF}}\right)}{2 \cdot \pi \cdot f \cdot R_{BS-OFF} \cdot C_{BS-OFF}} \quad (3)$$
$$1 + \frac{D}{D_{MAX}} \cdot \left[\left(\frac{C}{2M \cdot C_{BS-OFF}} + 1\right)^2 \cdot \frac{R_{BS-ON}}{R_{BS-OFF}} - 1\right]$$

R_{BS-ON}

The RFDSCA model is based on six design parameters and two independent variables (D and f). The design parameters that can be optimized to obtain a RFDSCA with optimum performance are N, M, and C, because $R_{BS\text{-}ON}$, $R_{BS\text{-}OFF}$, and $C_{BS\text{-}OFF}$ are defined by the integration technology and bias conditions. Thus, any RFDSCA circuit can be fully defined by the variables N, M, and C. Besides that, Eqs. (2) and (3) are crucial to the RFDSCA design algorithm because they are used during the automated synthesis procedure to verify the initial specifications and to evaluate the performance of each solution, as it will be explained in the next two subsections.

2.2. Optimization Algorithm

The automatic design synthesis procedure uses a GA to generate several RFDSCA circuits that meet the design specifications, all with identical maximum performance (given by the quality factor). Each GA solution, that corresponds to a specific RFDSCA circuit, is defined by the N, M, and C. The developed GA, which is described by the flowchart of Figure 4, uses the e-concept and the maximin sorting scheme to guarantee that the generated solutions are spread along an optimal front in the parameter space. The e-dominance allows keeping a solution front in the search space over evolution and the maximin technique promotes the diversity along each generation.

The flowchart of Figure 4, apart from the maximin selection step, represents a standard GA. It begins by randomly initializing the population $P(t)$, where variable t identifies the generation, videlicet, the GA cycle number. Each individual of the population (potential solution/circuit) is represented by $p_i(t) = \{N_i, M_i, C_i\}$ where N_i, M_i, and C_i are the number of cells, number of BSs, and the value of the reference capacitances for the individual i, respectively. The algorithm uses a population of 1000 individuals (the maximum value of i is 1000). The floating point values of N_i, M_i, and C_i are randomly initialized (at $t = 0$) in an appropriate range ($N_i = 1 \ldots 64$, $M_i = 1 \ldots 64$, and $C_i = 1$ fF … 1 pF). The search is then carried out within this population over 10^5 generations (the maximum value of t is 10^5). After the initialization, a fitness value (f_v) for each population element is evaluated in order to determine the solution performance. The evaluation of f_v leads to a positive value equal to $2 \cdot p \cdot f \cdot Q_{RFDSCA}$ if the solution verifies all the design specifications, otherwise it takes a negative value according to the distance to the feasible space. Then, the selection operator, based on the linear ranking scheme, is used to identify the most capable parents to generate proficient offspring (set $D(t)$). To create individuals with new genetic material, the operators simulated binary crossover and mutation are used. When mutation occurs, the operator replaces the value of each individual chromosome according to a uniform distribution function. The uniform function varies in the range $[-U_i, U_i]$ where $U_i = \{0.2, 0.2, 0.4 \times 10^{-15}\}$ for N_i, M_i, and C_i, respectively. The crossover and mutation probabilities are $p_c = 0.6$ and $p_m = 0.05$, respectively. In the following step, the fitness of each element of the population is again calculated and the maximin technique is applied to disperse the solutions over a continuous front. The cycle is repeated until the predefined maximum number of iterations is reached ($t = 10^5$).

2.3. Design Steps

The simplified flowchart of the RFDSCA design procedure is depicted in Figure 5. The first design step comprises two actions. One action is the specification of the desired performance characteristics of the RFDSCA, which are defined by the maximum capacitance, C_{MAX}, minimum capacitance, C_{MIN}, and the tuning capacitance step, DC. These three values impose the

bounds for the RFDSCA capacitance. The other action consists in the definition of the technology design variables $R_{\text{BS-ON}}$,

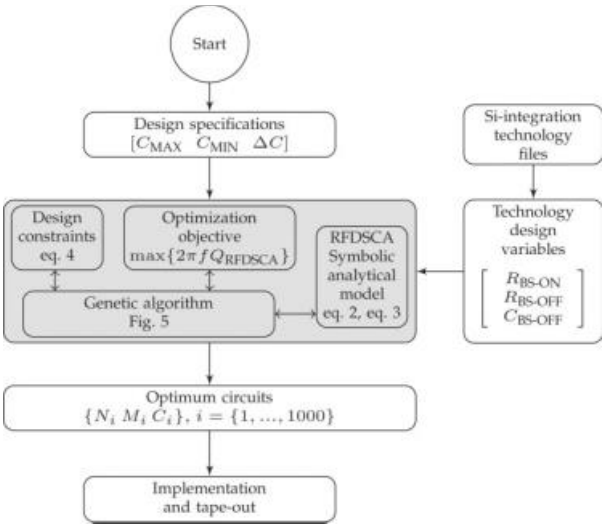

Figure 5 Flowchart of the RFDSCA design algorithm

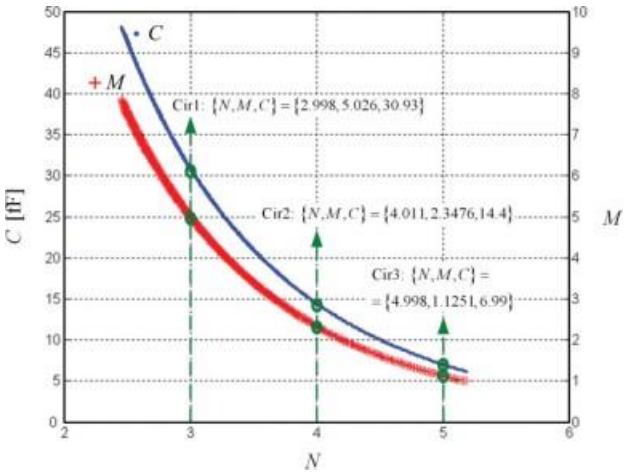

Figure 6 Automated synthesis results: *M* and *C* versus *N*. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

$R_{BS\text{-}OFF}$, and $C_{BS\text{-}OFF}$, which can be determined from the Si-integration technology process parameters and models.

The second design step is the execution of the proposed GA. For that, it is necessary to define the design restrictions and the fitness function appropriated for this type of circuits. The design restrictions that are related to the initial RFDSCA specifications are defined by the three inequalities given in (4):

$$\begin{cases} C_{RFDSCA-MAX} \geq C_{MAX} \\ C_{RFDSCA-MIN} \leq C_{MIN} \\ \Delta C_{RFDSCA} \leq \Delta C \end{cases} \quad (4)$$

In (4) $C_{RFDSCA\text{-}MAX}$, $C_{RFDSCA\text{-}MIN}$, and DC_{RFDSCA} represent the maximum RFDSCA capacitance, the minimum RFDSCA capacitance, and the RFDSCA tuning capacitance step, respectively. These three values are determined by the GA from expression (2). To achieve high performance RFDSCAs, it is necessary to determine the number of cells and the components values and sizes that maximize the RFDSCA quality factor. Noting that Q_{RFDSCA} decreases monotonically with f (see (3)), the objective function for this kind of RF circuits can be made independent of it. Therefore, the chosen optimization objective function is given by expression (5):

$$f_v(D) = 2 \cdot \pi \cdot f \cdot Q_{RFDSCA}(D,f) \quad (5)$$

The outcome of the GA is a set of several RFDSCA circuits, each one defined by specific values of *N*, *M*, and *C*, all having identical performance. The next step in the RFDSCA design procedure consists in choosing the circuit that is best suited to be implemented in a particular Si-integration technology. This action is done by the designer. As a general design rule, the circuit that should be implemented is the one that has the lower number of cells, because this allows minimizing the number of control variables and, in certain cases, the parasitic elements associated to the interconnections. The design procedure ends with the circuit tape-out.

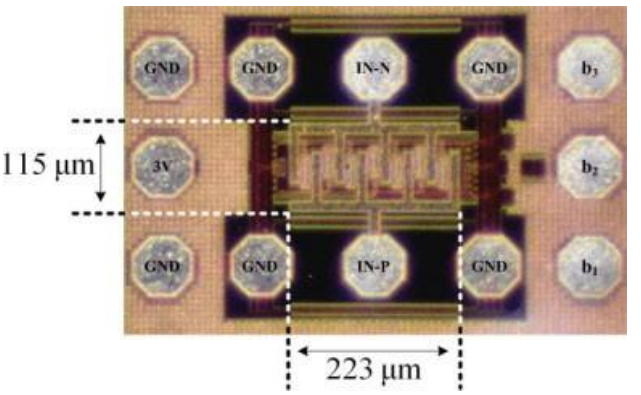

Figure 7 Die photomicrograph. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

3. A RFDSCA DESIGN CASE STUDY

This section presents the design and measurement results of an optimum performance RFDSCA, intended for applications that operate at frequencies up to 40 GHz. The design is accomplished using the home made automated synthesis procedure previously described.

3.1. Specifications, Design, and Simulation

The objective is to implement a microwave discrete tuning differential capacitance circuit in a 0.25 **1**m BiCMOS technology. The RFDSCA should present at least a minimum capacitance of C_{MIN} ¼ 72 fF, a maximum capacitance of C_{MAX} ¼ 108 fF, and a maximum tuning step of D*C* ¼ 8 fF, as indicated in (4). Besides that, the quality factor of the RFDSCA should be as high as possible.

The differential BS is made up of a single NMOS transistor, with length of 0.25 **1**m and width of 720 nm, which corresponds to the minimum dimensions provided by the BiCMOS integration technology. Considering the SPICE models of the transistors and the technological process parameters, the elements of the BS model are those given in (6):

TABLE 1 RFDSCA Performance Results

					Design Constraints		
Circuit	Type of Results	*N*	*M*	*C* (fF)	$C_{RFDSCA\text{-}MAX}$ (fF) (−108 fF)	$C_{RFDSCA\text{-}MIN}$ (fF) (::;72 fF)	DC_{RFDSCA} (fF) (::;8 fF)
Cir1	Genetic algorithm	2.998	5.026	30.93	108	71.95	5.185
	SpectreRF (schematic)	3	5	30.9	108	71.70	5.185
Cir2	Genetic algorithm	4.0011	2.3476	14.40	108	71.90	2.408
	SpectreRF (schematic)	4	2	14.40	108	67.92	2.670
Cir3	Genetic algorithm	4.998	1.1251	6.99	108	71.65	1.179
	SpectreRF (schematic)	5	1	6.97	108	68.74	1.265

$$\begin{cases} R_{BS-ON} = 73.6\Omega\,(@V_{GS} = 3V) \\ R_{BS-OFF} = 18.9\Omega\,(@V_{GS} = 0V) \\ C_{BS-OFF} = 6.1fF\,(@V_{GS} = 0V) \end{cases} \quad (6)$$

These values are almost constant in the frequency range from 1 to 40 GHz.

The values of the six design variables specified in (4) and (6) are the only ones that must be known before running the RFDSCAs synthesis method. The solutions found by the automated synthesis procedure are represented in the two curves of Figure 6, where the red one presents M versus N (curve marked with the þ symbol) and the blue corresponds to C versus N (curve marked with the (symbol). Moreover, all the circuits generated by the algorithm reveal an high performance because the minimum Q_{RFDSCA} at 15 GHz, calculated by the GA, is rv47. To find an optimum performance RFDSCA circuit, it is only necessary to select the appropriate value of N, because M and C are immediately defined by this value. Figure 6 also shows that the algorithm finds a well-defined front with good diversity. Moreover, the results obtained show that the algorithm convergence ability is very good because all the solutions are in the nondominated front.

To verify the solutions provided by the RFDSCAs synthesis procedure, three different circuits were chosen and simulated in SpectreRF. These are identified as Cir1, Cir2, and Cir3 in Figure 6 and in Table 1. The results of Table 1 show that the values of $C_{RFDSCA\text{-}MAX}$, $C_{RFDSCA\text{-}MIN}$, and DC_{RFDSCA} obtained through the SpectreRF schematic simulations of the three circuits are similar to those achieved with the GA. Moreover, the simulated circuits meet all the design constraints.

3.2. Implementation and Experimental Results

To verify, in practice, the performance of the design procedure, one RFDSCA was implemented and tested. The circuit Cir1 of Table 1 was chosen to be implemented and tested, because it is the one that requires the lower number of cells.

To improve the similarity between the calculated, simulated, and experimental results some valuable techniques can be used during the RFDSCA layout design. Parasitic elements are an important issue, because the RFDSCA performance is extremely sensitive to them. Thus, the interconnection lines should be as short as possible in order to reduce their parasitic resistance, capacitance, and inductance. The cross line also must be avoided, to reduce the parasitic capacitance. Furthermore, too thin or too wide lines are not recommended, because they will produce large parasitic resistance or capacitance, respectively. The interconnecting resistance is further reduced by using the topmost metal layer, due to low resistivity, or by stacking the top two metal layers. All the above considerations were taken into account when laying out the RFDSCA.

TABLE 2 Cir1 Performance Results

	Design Constraints		
Cir1 Results	$C_{RFDSCA\text{-}MAX}$ (fF)	$C_{RFDSCA\text{-}MIN}$ (fF)	DC_{RFDSCA} (fF)
SpectreRF (schematic)	108	71.70	5.185
SpectreRF (post-layout)	147	111	5.14
Measured (after de-embedding)	148@15 GHz	116@15 GHz	4.57@15 GHz

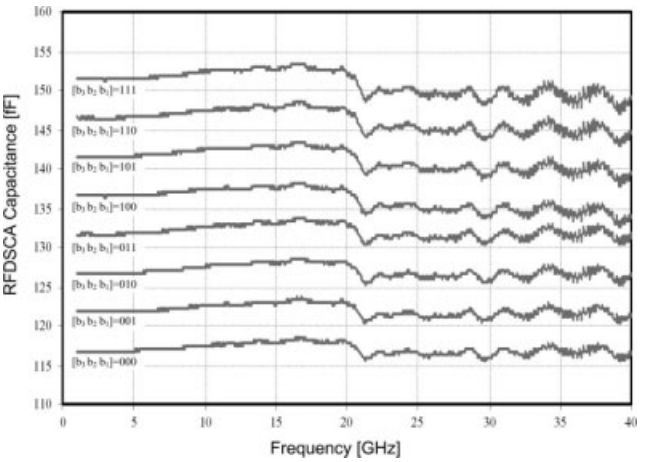

Figure 8 Measured RFDSCA capacitance versus frequency for all the tuning words

Figure 7 depicts the photomicrograph of the implemented RFDSCA. The differential input is identified by the IN-P and IN-N pads and the control bits by the b_1, b_2, and b_3 pads. The circuit size, excluding the pads, is 0.0256 mm^2. The RFDSCA was measured on-wafer using a Cascade Summit 9000 probe station, two 40 GHz Cascade Infinity ground-signal-ground probes and a 67 GHz Agilent PNA network analyzer (E8361A).

The SpectreRF schematic and post-layout simulations and the experimental results of Cir1 are shown in Table 2. The measured results presented in this table are obtained after de-embedding the effects of the auxiliary measure structures, in other words, after removing the parasitic resistances, capacitances, and inductances associated to the interconnections between the probes and the RFDSCA circuit. The differences between the schematic and the pos-layout simulations results are fundamentally due to the parasitics associated to the RFDSCA metal interconnections, because the major differences occur only in the extreme values of the capacitive tuning range. The simulation results of Table 2 show that these differences come from a constant parasitic capacitance of 39 fF, which is also independent of the tuning word. The RFDSCA measured results presented in Table 2 show that the implemented version of Cir1 has a performance very similar to the one obtained by the pos-layout simulations. Besides that, the RFDSCA capacitance for each tuning word is almost constant in the frequency range of 1–40 GHz, as illustrated in Figure 8.

4. CONCLUSIONS

This article presents a RFDSCA automated synthesis procedure. This algorithm determines several RFDSCA circuits, all with the same maximum performance, from the top-level system specifications. The genetic synthesis tool optimizes a fitness function proportional to the RFDSCA quality factor and uses the e-concept and maximin sorting scheme to achieve a set of solutions well distributed along a nondominated front. To verify the results of the algorithm, three RFDSCAs were simulated in SpectreRF and one of them was implemented and tested. The design used a 0.25 1m BiCMOS process. All the synthesized, simulated, and measured results were very close.

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