

Title: High Performance Multi-Standard Architecture for DCT Computation in H.264/AVC High Profile and HEVC Codecs

Author(s): Dias, Tiago ^[1,2,3]; Roma, Nuno ^[1,2]; Sousa, Leonel ^[1,2]

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Abstract: A new high performance architecture for the computation of all the DCT operations adopted in the H.264/AVC and HEVC standards is proposed in this paper. Contrasting to other dedicated transform cores, the presented multi-standard transform architecture is supported on a completely configurable, scalable and unified structure, that is able to compute not only the forward and the inverse 8×8 and 4×4 integer DCTs and the 4×4 and 2×2 Hadamard transforms defined in the H.264/AVC standard, but also the 4×4, 8×8, 16×16 and 32×32 integer transforms adopted in HEVC. Experimental results obtained using a Xilinx Virtex-7 FPGA demonstrated the superior performance and hardware efficiency levels provided by the proposed structure, which outperforms its more prominent related designs by at least 1.8 times. When integrated in a multi-core embedded system, this architecture allows the computation, in real-time, of all the transforms mentioned above for resolutions as high as the 8k Ultra High Definition Television (UHDTV) (7680×4320 @ 30fps).

Author KeyWords: Video coding; AVC / HEVC; Integer DCT; Multistandard architecture; Systolic array; FPGA

Reprint Address: Dias, Tiago (reprint author) - INESC-ID Lisbon, Rua Alves Redol, 1000-029 Lisbon, Portugal

Addresses:

[1] INESC-ID, P 1000029 Lisbon, Portugal

[2] IST-TU, P 1000029 Lisbon, Portugal

[3] ISEL, P-1959007 Lisbon, Portugal

E-mail Addresses: tiago.dias@inesc-id.pt

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