Title: Runtime Elision of Transactional Barriers for Captured Memory

Author(s): Carvalho, Fernando Miguel ^[1,2]; Cachopo, Joao

Source: ACM Sigplan Notices Volume: 48 Issue: 8 Pages: 303-304 DOI: 10.1145/2517327.2442556 Published: Aug 2013

Document Type: Article

Language: English

Abstract: In this paper, we propose a new technique that can identify transaction-local memory (i.e. captured memory), in managed environments, while having a low runtime overhead. We implemented our proposal in a well known STM framework (Deuce) and we tested it in STMBench7 with two different STMs: TL2 and LSA. In both STMs the performance improved significantly (4 times and 2.6 times, respectively). Moreover, running the STAMP benchmarks with our approach shows improvements of 7 times in the best case for the Vacation application.

Author Keywords: Neutrino Physics; Discrete and Finite Symmetries Performance; Transactions; Software Transactional Memory; Runtime Optimizations

Reprint Address: Carvalho, FM (reprint author) - Lisbon Polytech Inst ISEL, ADEETC, Lisbon, Portugal Addresses:

[1] Lisbon Polytech Inst ISEL, ADEETC, Lisbon, Portugal

[2] Univ Tecn Lisboa, INESC, ID Lisboa, Lisbon, Portugal

E-mail Addresses: mcarvalho@cc.isel.pt; joao.cachopo@ist.utl.pt

Funding:

Funding Agency	Grant Number
FCT via INESC-ID through the PIDDAC Program	
FCT via RuLAM project	PTDC/EIA-EIA/108240/2008

Publisher: Association Computing Machinery

Publisher Address: 2 Penn Plaza, STE 701, New York, NY 10121-0701 USA ISSN: 0362-1340

Citation: CARVALHO, Fernando Miguel; CACHOPO, Joao - Runtime Elision of Transactional Barriers for Captured Memory. <u>ACM Sigplan Notices</u>. ISSN 0362-1340. Vol. 48, nr. 8 (2013), p. 303-304