Front-End and Readout Electronics for Silicon Trackers at the ILC

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A highly integrated readout scheme for Silicon trackers making use of Deep Sub-Micron CMOS electronics is presented. In this context,a 16-channel readout chip for Silicon strips detector has been designed in 180nm CMOS technology, each channel comprising a low noise amplifier, a pulse shaper, a sample and hold and a comparator. First results are presented.

1. INTRODUCTION

A Front-end readout system for tracking Silicon detectors has to manage millions of channels. Consequently, the amount of material and power per channel has to be carefully optimized keeping noise and readout speed within the constraints of the experiment. It is therefore essential to look for the most available integrated technologies that allow to minimize the amount of material added to the detector, as well as the connexion capacitances in order to cope with a manageable amount of dissipated power. Actually, a Silicon strips envelope around the central tracker in the case of the LDC design would cover a few hundreds square meters for a few millions channels to be read. This would also be true in the case of the SiD that in the present baseline design covers of the order of 100 square meters and a total of 6 millions channels. Therefore, the multiplexing of tasks such as analog to digital conversion and data sparsification are mandatory.

The timing of the ILC machine will allow to cycle the power, since the front-end has to be active for 1 ms and accept at that stage all events every 300 ns, followed by a stand-by period of 100 to 200 ms. Calibration of the electronics will be also performed at the front-end level.

The full context of this work is described in the document available from the Website: [1]

2. FRONT-END PROCESSING

The foreseen front-end processing is sketched in Figure 1. Silicon strips detectors of a capacitance between 10 and 100pF with a maximum foreseen presently of 75 pF (60cm ladder). The Front-end signal processing chips amplify, filter, sample and digitize the input charge. Only charges collected on three adjacent strips, whose sum exceeds a given threshold, are stored and digitized. Shaping times between 30ns and 10μs are foreseen, since it is intended to get the hit coordinate along the strip by timing between the two ends of the detector. This timing is presently under investigations.

Digital processing for charge, time, cluster, and fast track algorithms is under study while designing the front-end electronics. (See Data Acquisition and Global Network session: "Silicon Data Acquisition and Front-end Electronics" from the same authors). The detector's occupancy dictating the analog buffers depth is of the order of a few per cent, mostly in the forward regions.

[1] http://www.linearcollider.ca/lcws05/h/Savoy.pdf

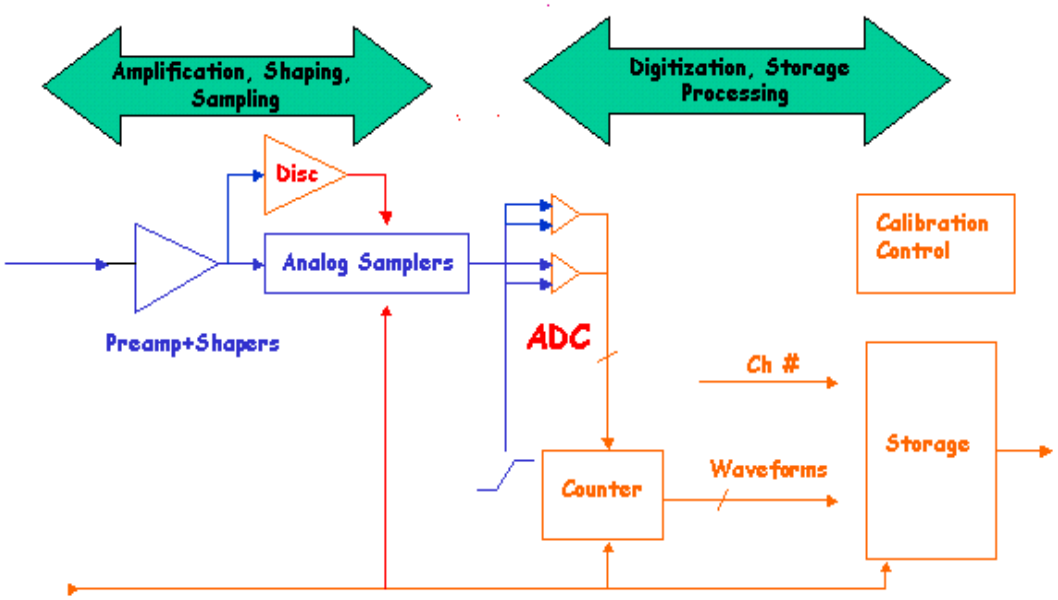

Figure 1: Front-End Processing

More precisely, a low noise charge integrator stores the input signal in a 400fF capacitor, giving an intrinsic gain of the order of 10mV/MIP at this level, assuming 24,000 electrons are deposited in a 300μm thickness Silicon detector. The voltage step from the preamplifier is pulse-shaped by a CR-RC stage with a peaking time tunable between 2 and 10μs.

Two analog samplers, one fast, one slow, with 10ns and 100ns scale clockings respectively, generate samples of the analog shaper output stored in two circular analog buffers of depth 16 running continuously. In order to store charge signals in the detector above a given threshold, an analog sum of three neighbouring channels is compared to a voltage level, taken at the output of the slow shapers, for each channel. A trigger decision at this level freezes the analog buffers, and selects an available set of two buffers for the next pulse to come. The total number of buffers for a given channel depends on the Silicon strips occupancy which is foreseen to be of the order of a few per cents. Therefore, a depth of 16 should cope with even worse detector output rate conditions.

This process runs for the total duration of an ILC train, of the order of one millisecond. At the end of the train, digitization takes place. In order to minimize the power, a single ramp ADC is foreseen, allowing to digitize in parallel as many channels as possible. The cost in power per channel is due to one comparator stage only.

2.1. Test chip

A test chip has been designed in a 180nm CMOS technology by United Microelectronics Corporation (Taiwan) available at multiproject cost through Europractice. It includes 16-channels comprising a low-noise preamplifier, a pulse shaper, a sample and hold, a voltage buffer and a comparator. A single test channel allows to check all blocks reachable through six I/O pads. All stages have bias controls allowing to optimize each DC operating point.

2.2. Low-noise analog section

The low-noise preamplifier (Figure 2) is a folded cascode stage with a PMOS input transistor biased under 40μA, in moderate-weak inversion. The corresponding transconductance is 0.69mA/V. The simulated open loop gain is 70dB, the noise from this stage being 85 + 16.5e-/pF.

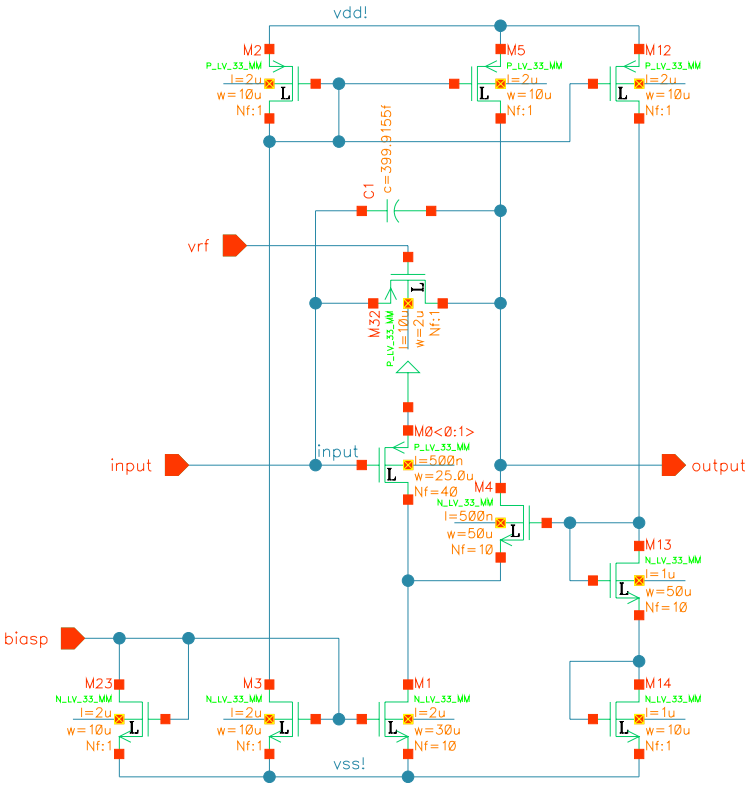

Figure 2: Preamplifier schematics

The drain is tied to ground at half the supply voltage,setting the DC point around -0.5V. The 400fF feedback capacitor is reset (or discharged with a given time constant) using a NMOS transistor controlled through an external voltage. The voltage gain of this stage is simulated to be 8mV/MIP. The pulse shaper is an active CR-RC network using the same folded cascode structure as above, buffered with a source follower in order to drive the 600fF sample and hold capacitor. Two analog controls allow to tune the peaking time between one and five microseconds

2.3. Sampling and comparator

The sample and hold is switched with a single NMOS transistor sized to trade off between rise-time, possible leaks, and the injected charge resulting in a voltage offset. A voltage buffer drives the next stage, a comparator, which is a cascoded differential pair followed by inverters driving the output pads. A trade-off between power and accuracy has been set at 30μW per channel, regarding the foreseen 10-bit ADC precision.

3. TEST CHIP RESULTS

The layout and chip are shown Figure 3.

3.1. Gain and Linearity

The measured gain of 8mV/MIP is in agreement with the simulations.

Dynamic range 70 MIPS for the amplifier and 50 MIPS for the shaper, instead of 100 MIPS and 60 MIPS as simulated. In addition, the deviation from linearity from the preamplifier is 1.5% instead of 0.5% simulated, and 5% for the shaper, for low amplitudes values. These points are presently investigated.

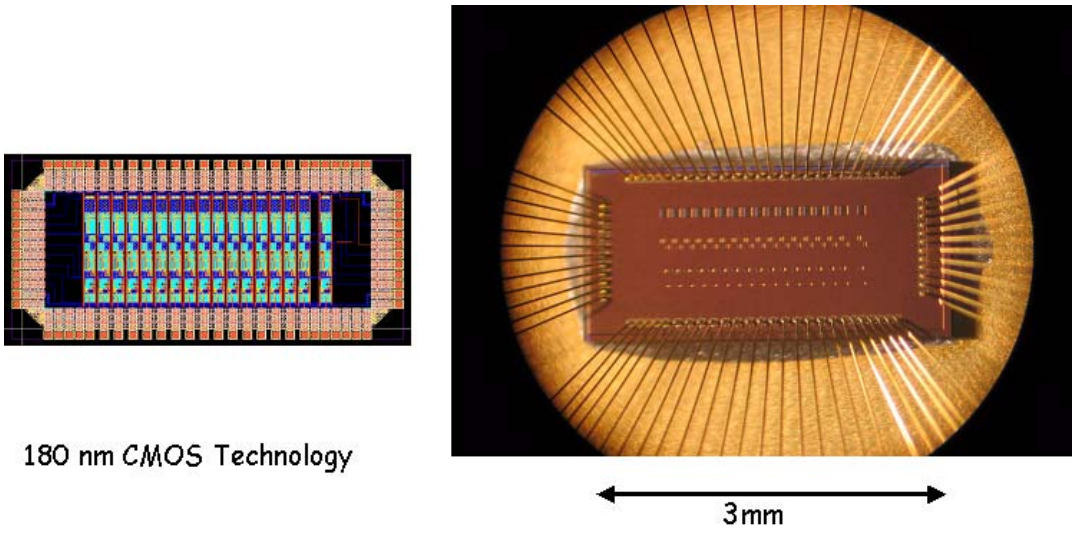

Figure 3: 180 nm CMOS Chip layout and picture

3.2. Noise

At 60μW input stage power, 50pF detector capacitance, 3μs shaping time, the various contributions to the detector and front-end electronics noise are summarized in Table 1.

Table I: Foreseen noise contributions at 50pF detector capacitance and 3μs shaping time

Noise source	**Value**	**Noise**
Input FET	g_m = 0.69mA/V	910e-
Detector leak	10nA	588e-
Bias resistor	10MΩ	423e-
Total		1163e-

The electronics noise comes mainly from the low-noise preamplifier input FET. The measured noise slope is 205 + 16.5e-/pF. The discrepancy between the simulated noise floor at zero capacitance and the experimental result is under investigations, at the present time, the noise spectral density has not been measured. According to the noise models from the manufacturer, no 1/f noise should show-up, even at 10μs shaping time. If this were the case, Silicon-Germanium technology could be an effective alternative both for low frequency noise reduction and speed performance having in view the timing measurements.

The 60μW power dissipated in the preamplifier is due to the input transistor biasing, in order to obtain a sufficient gain. It dictates the noise performance of the stage. In case of lower noise requirements, particularly for long strips, an increase of power could be envisaged, leading for instance to slopes below 10e-/pF.

3.3. Power

In order to take advantage of the ILC machine timing, all electronic stages running during the collisions only could be switched off for the readout stage. Therefore, a factor 100-200 can be saved at this level.

This process has been simulated to be effective with the present front-end electronics provided the integration capacitor is reset before power-off and after power-on.

4. CONCLUSION AND FUTURE WORK

These encouraging preliminary results regarding the integration of a front-end electronics for Silicon detectors in Deep Sub-Micron CMOS technology need to be confirmed by thorough tests of the set of samples delivered. Furthermore, tests with an actual Silicon of bare chips detector will be done with MIP signals on a test bench and compared with other front-end chips off the shelf.

A 128-channels version that include fast and slow shapers, the sparsifier stage, analog samplers and a full ADC, digital section including possibly digital filtering and lossless data compression, power switching, is under design and will benefit from the lessons learnt after this prototyping work.

Acknowledgments

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