COPPER TO COPPER BONDING BY NANO INTERFACES FOR FINE PITCH INTERCONNECTIONS AND THERMAL APPLICATIONS

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COPPER TO COPPER BONDING BY NANO INTERFACES FOR FINE PITCH INTERCONNECTIONS AND THERMAL APPLICATIONS

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Ever growing demands for portability and functionality have always governed the electronic technology innovations. IC downscaling with Moore's law at IC level and system miniaturization with System-On-Package (SOP) paradigm at system level, have resulted and will continue to result in ultraminiaturized systems with unprecedented functionality at reduced cost. However, system miniaturization poses several electrical and thermal challenges that demand innovative solutions including advanced materials, bonding and assembly techniques. Heterogeneous material and device integration for thermal structures and IC assembly are limited by the bonding technology and the electrical and thermal impedance of the bonding interfaces. Solder - based bonding technology that is prevalent today is a major limitation to future systems.

The trend towards miniaturized systems is expected to drive downscaling of IC I/O pad pitches from 40μm to 1- 5μm in future. Solder technology imposes several pitch, processability and cost restrictions at such fine pitches. Furthermore, according to International Technology Roadmap for Semiconductors (ITRS-2006), the supply current in high performance microprocessors is expected to increase to 220 A by 2012. At such supply current, the current density will exceed the maximum allowable current density of solders. The intrinsic delay and electromigration in solders are other daunting issues that become critical at nanometer sized technology nodes. In addition, formation of intermetallics is also a bottleneck that poses significant mechanical issues. Similarly, thermal power dissipation is growing to unprecedented

high with a projected power of 198 W by 2008 (ITRS 2006). Present thermal interfaces are not adequate for such high heat dissipation.

Recently, copper based thin film bonding has become a promising approach to address the abovementioned challenges. However, copper-copper direct bonding without using solders has not been studied thoroughly. Typically, bonding is carried out at 400^{o}C for 30 min followed by annealing for 30 min. High thermal budget in such process makes it less attractive for integrated systems because of the associated process incompatibilities. Hence, there is a need to develop a novel low temperature copper to copper bonding process. In the present study, nanomaterials - based copper-to-copper bonding is explored and developed as an alternative to solder-based bonding. To demonstrate fine pitch bonding, the patterning of these nanoparticles is crucial. Therefore, two novel self-patterning techniques based on: 1.) Selective wetting and 2.) Selective nanoparticle deposition, are developed to address this challenge. Nanoparticle active layer facilitates diffusion and, thus, a reliable bond can be achieved using less thermal budget. Quantitative characterization of the bonding revealed good metallurgical bonding with very high bond strength. This has been confirmed by several morphological and structural characterizations. A 30-micron pitch IC assembly test vehicle is used to demonstrate fine pitch patternability and bonding. In conclusion, novel nanoparticle synthesis and patterning techniques were developed and demonstrated for low-impedance and low-cost electrical and thermal interfaces.

1. INTRODUCTION

This chapter deals with the electrical and thermal challenges in highly miniaturized and multifunctional System-On-Package (SOP) based systems. The electrical, thermophysical, and mechanical limitations of present interconnection and thermal structure technologies are discussed in order to define the need for innovative solutions. Finally, the present research objectives and thesis outline are presented.

Ever-growing demands for portability and functionality have always governed electronic technology innovations. Gordon E. Moore foresaw the market demand and set forth the empirical Moore's law [1], or the so-called first law of electronics, which predicts the increment in the number of transistors on a chip as a function of time. This coupled with shrinking die size contributed to several electrical and thermal challenges.

In the past, driven by Moore's law, the integration efforts were focused predominantly on silicon using CMOS technology. The System-on-Chip (SoC) approach of integrating functionalities on a single chip is beset with several fundamental and practical barriers like high cost, several photolithography steps, low yield and licensing and Intellectual Property (IP) issues. Currently, System-in-Package (SIP) approach of vertical stacking of bare and packaged ICs is pursued by several packaging companies for integration of functions at module and subsystem levels. SIP extends silicon integration in 3D but is still limited by CMOS capabilities.

To overcome the limitations of SoC approach, the System-On-Package (SOP) approach was proposed by Prof. Rao Tummala at the Packaging Research Center in 1994 [2]. The SOP enables highly miniaturized heterogeneous integration of RF/digital/opto/sensing functions by system-centric IC-package codesign and functional optimization with 3D integration of thin film components between the ICs and package. The focus of SOP is thus on miniaturization of system components, including not only actives, but also passives, power sources, I/Os, thermal structures, and system I/Os. With this fundamentally new paradigm, the SOP methodology overcomes the barriers of SoC leading to cheaper and faster-to-market convergent Microsystems. SOP is expected to enable the electronic devices to achieve unprecedented functionality and miniaturization at reduced cost.

1.1 Thermal Challenges in SOP Based Systems

The chip power consumption has been increasing despite reductions in the power supply voltage and an increase in the efficiency of devices. According to the International Technology Roadmap for Semiconductors (ITRS-2006), high-performance microprocessors may dissipate 198 W by 2008 as seen in Figure 1.1 [3]. This situation can be worse in radiofrequency (RF) and power electronic components. The resulting thermal management challenges can be appreciated by comparing heat fluxes in various electronic components with those in some well-known heat generating systems (see Figure 1.2) [4].

The thermal implications of SOP are enormous. Since SOP has two major components—device components and system components, it is convenient to understand the thermal

implications in these two parts of SOP technology separately. The thermal aspects of devices in the SOP concept remain the same whether the system is based on SOP or SOB (system-on-board). However, the system miniaturization of SOP has a huge impact because of the exponential decrease in the available volumetric system space. An illustration of such an impact is shown in Figure 1.3 [5].

The cooling requirements of SOP systems are dictated by performance and reliability needs. Operating temperatures outside a range can cause deteriorated performance of active semiconductors—the leakage current may increase in DRAM, clock frequency may reduce, and wavelength drift and power drop may occur in optoelectronic modules. The mismatch in the coefficient of thermal expansion (CTE) between ICs and organic substrates (2.8 ppm/^{o}C for Si, ~6 ppm/^{o}C for GaAs, ~25 ppm/^{o}C for eutectic $Sn_{63}Pb_{37}$ solder, and 14 to 20 ppm/^{o}C for organic epoxy fiberglass FR4) generates thermal stress at the solder joints. Repeated thermal cycling due to switching thus can lead to thermal fatigue and ultimate failure. Both operational reliability and functional performance are thermally influenced. An approach often taken by designers of multifunctional microsystems is to limit the maximum "junction temperature," an average measure of the chip temperature during operation. This limit is usually different for commercial and military equipment, as each sees different ranges of ambient temperatures in operation. For handheld and portable devices, the market sometimes demands an even more stringent limit to ensure a greater degree of customer satisfaction. The International Technology Roadmap for Semiconductors (ITRS) provides a projected value of allowable junction and operating temperatures in various microsystems [3]. This is illustrated in Figure 1.4 [3]. As evident from the figure, the junction temperature for single chip-packaged devices can't be allowed to rise above 125°C in low-cost, handheld, and memory devices; above 175°C in devices working in

harsh environment; and above 100°C in high-performance and cost-effective devices. SOP modules and systems, thus, may fail due to a variety of causes unless they are designed with the right set of materials and appropriate thermal management solutions.

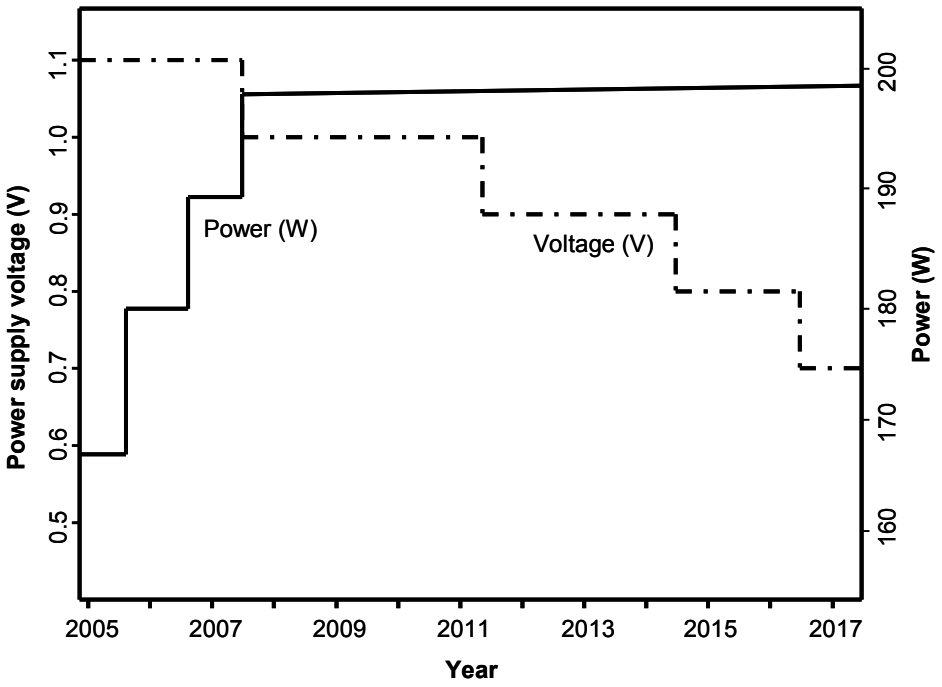

Figure 1.1 Power supply voltage and maximum power consumption in high-performance processors [3, 5]

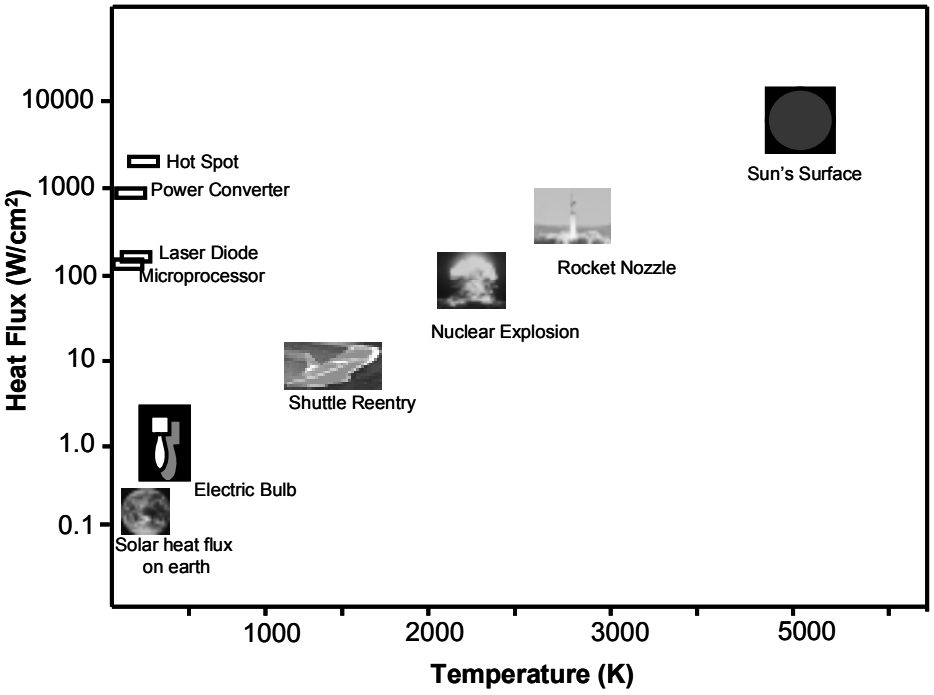

Figure 1.2 Comparison of heat fluxes in various phenomena and systems [4, 5]

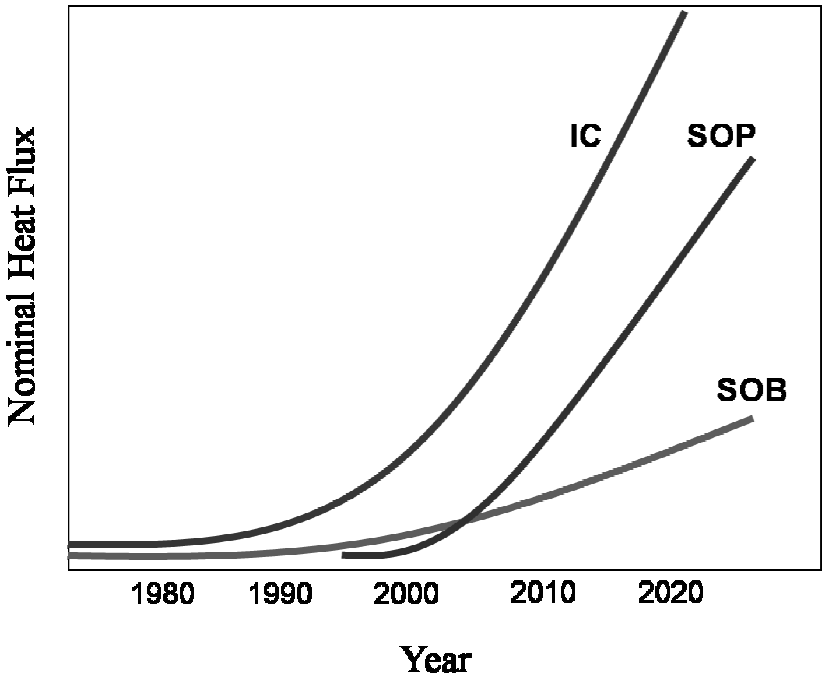

Figure 1.3 Impact of SOP on thermal challenges [5]

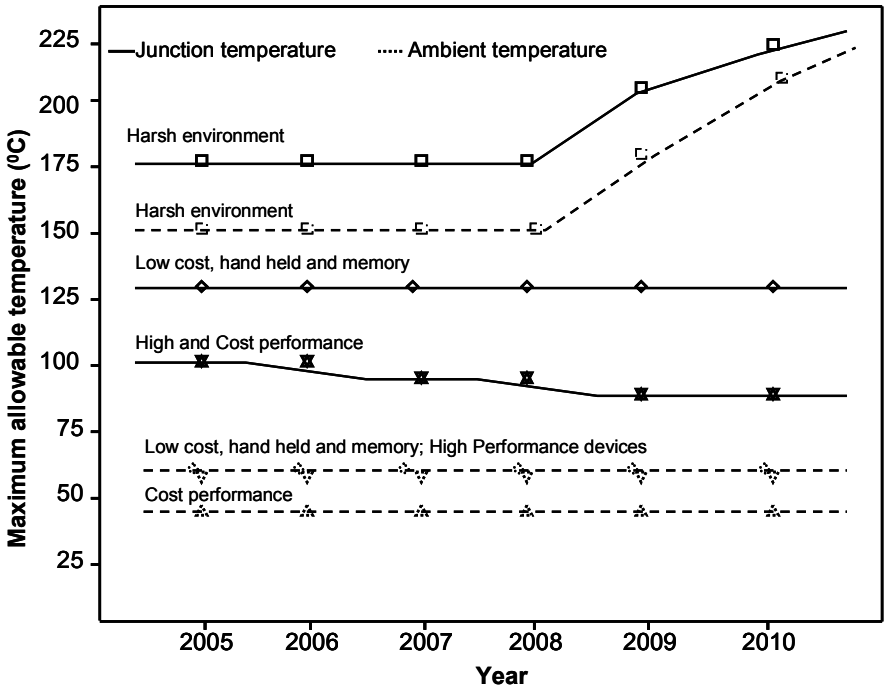

Figure 1.4 Maximum allowable junction and ambient temperature as a function of time [3, 5]

1.1.1 Thermal structures and interface challenges

The heat transfer path from the source, such as an IC, to the eventual heat sink consists of various interfaces. Microscale surface roughness at these interfaces results in regions of contacts and air gaps, and thus effective heat conduction may severely reduce due to increased interfacial resistance. Howeverm this resistance can be decreased using compliant and gap filling interface materials, known as thermal interface materials (TIM). TIM can be fabricated to minimize voids by providing a conformal and planar surface, thereby reducing the interfacial thermal resistance. Thermal resistance of TIM is governed by both the bulk, as well as the contact resistance [6, 7], as given by

$$R_{TIM} = \frac{BLT}{A \times K_{TIM}} + R_{C1} + R_{C2} \qquad 1.1$$

where BLT is the bond line thickness, A is the contact area, K_{TIM} is the bulk thermal conductivity of TIM, and R_{C1} and R_{C2} are the contact resistances. From Equation 1.1 it is apparent that the TIM should be as thin as possible, while still filling all the voids between the two higher conducting parts. BLT, however, can't be reduced below a limiting thickness due to reliability concerns. An increase in thermal conductivity and reduction of contact resistance are other ways to reduce the effective thermal resistance. Contact resistance is dependent on the surface roughness, contact pressure, and compressive modulus [7]. Various limiting factors can affect the selection of TIM including thermal conductivity, thermal resistance, operating temperature range, electrical conductivity, phase change temperature, pressure, viscosity, outgassing, surface finish, mechanical stability, reliability, and cost [7].

The present thermal interface solutions are not adequate for the next generation SOP based systems. They have high BLT, low thermal conductivity, low diffusivity and very high thermal impedance as shown in Figure 1.5 [5].

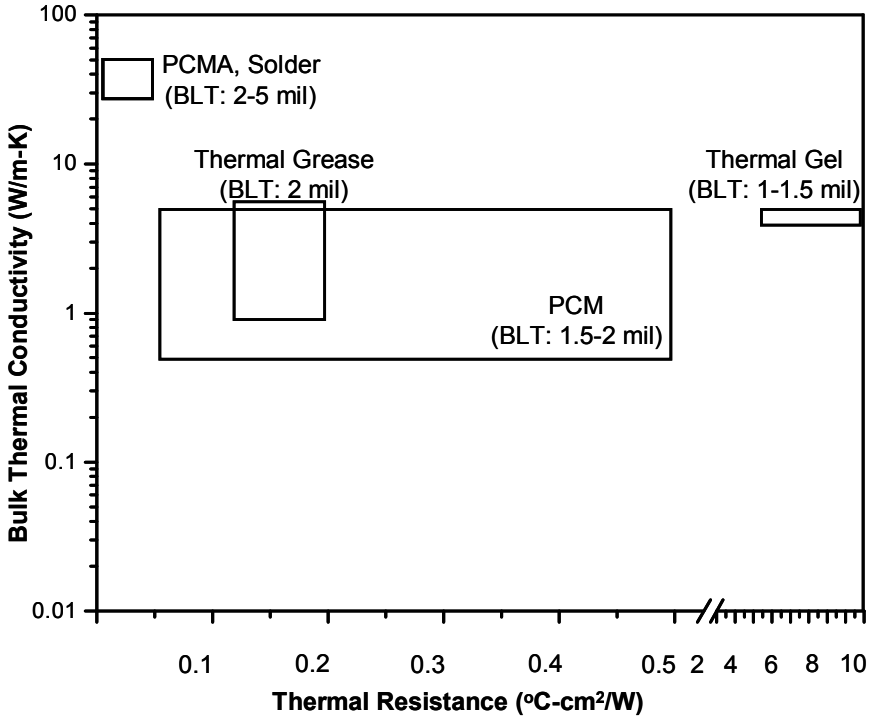

Figure 1.5 Trends in thermal interface materials [5]

Similar limitations are seen in thermal structures. Therefore, there is a need to develop new materials based interfaces that can alleviate thermal challenges by providing improved thermomechanical properties. One of the most attractive materials is copper that presents excellent thermal, electrical and mechanical properties suitable for abovementioned applications.

1.2 Fine Pitch Interconnection Trends and Challenges

Miniaturization at system and component level is plagued with myriads of electrical challenges in addition to the aforementioned thermal challenges. Integration of over a billion transistors on high end microprocessors witnesses interconnection scaling challenges that include issues related to degradation of resistivity, material integration, planarity control, high aspect ratio via and wire coverage, and reliability problems due to electrical, thermal and mechanical stresses in a multilevel wire stack [3].

According to the International Technology Roadmap for Semiconductors (ITRS 2006), the transition in electronic industry will cause nanochips with less than 32 nm nodes, in excess of 10000 I/Os and pitch down to 20 μm [3, 8]. A chronological trend in transition in electronic technology is shown in Figure 1.6. With such downscaling of the feature size signal integrity, interconnection delay, parasitics, mechanical stability of the interconnections and electromigration become utmost important.

Table 1.1 compares intrinsic interconnection delay with transistor switching delay at different technology nodes [9]. As the nodes become smaller, evidently interconnection delay becomes more prominent. At 35 nm node, the intrinsic delay surprisingly becomes two order magnitudes higher than the transistor delay. SIP technology has shown potential to address abovementioned issues by enabling vertical integration of devices and allowing significant reduction in interconnect length and thus high packing density [10, 11]. Heterogeneous device integration (e.g., logic, memory, analog, sensors, microfluidics, and power sources) at wafer-scale will push the interconnection pitch to 2-10 microns and terabit bandwidth.

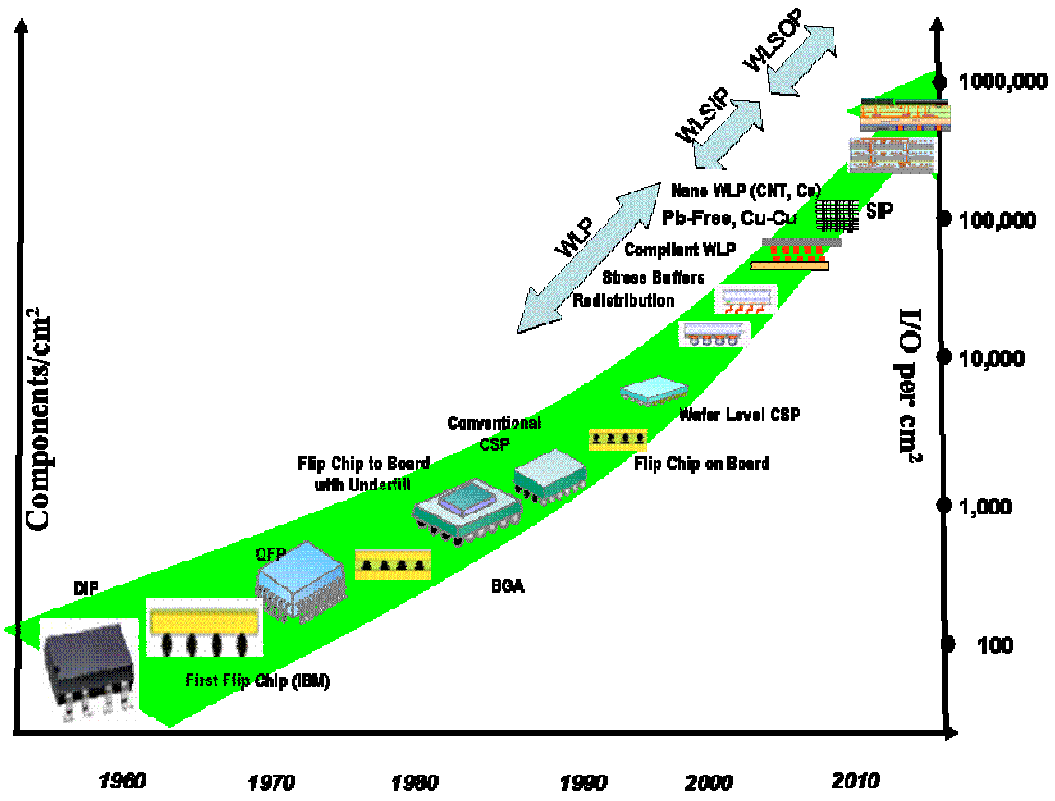

Figure 1.6 Chronological advancement in IC packaging [8]

Table 1.1 Transistor and interconnect delay at different technology nodes [9]

Technology Node	MOSFET Switching delay (ps)	Intrinsic delay of minimum scaled 1mm interconnect (ps)	Intrinsic delay of reverse scaled 1mm interconnect (ps)
1.0 µm (Al, SiO_2)	20	5	5
0.1 µm (Al, SiO_2)	5	30	5
35 nm (Cu, low K)	2.5	250	5

1.2.1 Limitations of current chip-to-package interconnection technologies

Current solder-based interconnection technologies are becoming inadequate to address the emerging needs for pitch, electrical and reliability performance. Fine pitch solder plating inevitably leads to processing issues associated with controlled plating chemistry and solder bridging. Solders require a complex stack of UBM, barriers and surface finish making them less attractive for size miniaturization. Formation of intermetallics is another big concern in solder based technologies. In addition, underfill is required to compensate for the thermomechanical stress in solder based interconnections, which raises significant concern in fine pitch technologies where dispensing of underfill becomes a daunting challenge. According to ITRS-2006, the supply current in high performance microprocessors is expected to increase to 220 A by 2012 [3]. At such supply current, the current density will exceed the maximum allowable current density of solders [12]. Moreover, solder performance at gigahertz frequency is modest and electro-migration becomes a critical issue.

Polymer based adhesives, including nano anisotropic conductive film (ACF), and nonconductive film (NCF) are some of the recent alternatives. However, materials reliability at fine pitch and issues with copper interfaces are still a major concern and have not yet been addressed. Moreover, these alternatives have modest electrical and mechanical properties, making them less attractive for nanometer node technologies.

All-Copper interconnections is identified as one of the key enabling technology to address many of the abovementioned challenges. Thin film die to wafer and wafer-to-wafer bonding with copper-based interconnections have several benefits in terms of low cost, process compatibility

with semiconductor infrastructure, and the shortest interconnection with the best electrical performance. Copper is electrically and thermally more conductive, and thus will be able to reduce the interconnect delay to a significant extant. In addition, copper interconnections will provide an efficient thermal path. Copper to copper bonding will also avoid formation of intermetallics and thus is mechanically more reliable. Electro-migration problem can also be reduced to a significant extent. Furthermore, the copper interconnection can be designed to achieve high mechanical compliance and thus the underfill can be eliminated. This will further enhance the electrical reliability by lowering the permittivity and loss and also will be instrumental in lowering cost [12]. Such direct wafer bonding using copper-copper bonding is also attractive for Microelectromechanical systems (MEMS) for device applications [13] such as sensors and actuators [14] and SOI [15].

Copper to copper bonding has been investigated by several research groups that include Reif et al [16, 17] and Chen et al [13, 18-27] using thermocompression bonding; Tadepalli et al [11] using ultrahigh vacuum technology; Kohl et al [12] using electroless copper bonding technology. However, the bonding is accomplished in ultrahigh vacuum and cleanroom environments with careful copper oxide cleaning procedures at around 400^{o}C, with pressures exceeding 30 N/cm^{2}, which may not be compatible with thinned dies. The bonding is carried out by exposing the device at high bonding and annealing temperature for about an hour that limits the throughput. The process windows are relatively narrow with several temperature compatibility issues. Lowering the thermal budget is a critical issue especially in SOP systems as they integrate several thermally sensitive elements including sensors, optoelectronic devices and polymer thin films [10, 11]. Therefore, there is a need to develop a novel process that can address the issue of lowering the thermal budget in the copper to copper bonding process.

1.3 Objective of The Current Research

The present research attempts to address two fundamental issues associated with system miniaturization--- the thermal and interconnection issues

1) Copper to copper thin metallurgical bonding using high thermal conductivity metallic nanoparticles: This is done to achieve low thermal impedance interface. Nanoparticle approach helps reduce the thermal budget during thermocompression bonding. In addition, it helps decreasing the bond line thickness and thus reduces the thermal path and hence the overall thermal resistance.

2). High electrically conductive metallic nanoparticles based copper to copper thin film bonding: This is done to achieve fine pitch interconnections with low electrical impedance, low electromigration, high current carrying capability and good mechanical reliability.

3) Novel patterning technique for patterning of nanoparticles: Patterning of nanoparticle is done to assist the fine pitch copper-to-copper bonding. The patterning techniques studied in this work are based on selective wetting of copper solution and selective deposition of gold nanoparticles.

1.4 Proposed Approaches

Metallic nanoparticles of copper, silver and gold are explored and evaluated for the nanostructured bonding layers between the copper surfaces. High surface energy of the nanoparticle lowers the melting temperature of the material [28]. Notably, kinetics of interdiffusion of copper is dependent on the homologous temperature. Therefore, diffusion rate is enhanced by lowering the melting temperature. In addition, high surface energy and high grain boundary to volume ratio endows the particles with elaborate mobility making the diffusion kinetic even faster.

However, nanoparticle approach has several issues including particle aggregation, particle oxidation during processing and particle coarsening (Oswald ripening). In-situ nanoparticles formation and bonding can overcome many of these disadvantages. In addition, patterning of these nanoparticles is crucial for fine pitch interconnection. In the present research, therefore novel methods to accomplish fine pitch patterning of copper (and gold) nanoparticles are also discussed.

Previous studies mostly deal with qualitative analysis of bond reliability such as dicing and razor test. In the present study, emphasis has been give to quantify the bond strength using die shear test. This gives a unique opportunity to study the bond characteristics in more comprehensive manner. In order to demonstrate the feasibility of this technology, the nanoparticle self-patterning was demonstrated on a 30 micron pitch silicon carrier substrate, followed by bonding with 30 micron pitch thin film copper pads.

In summary, a novel approach has been studied to achieve maskless patterning of metal nanoparticles that has been used to carry out copper to copper bonding at low temperature and reduced bonding time. The bond strength has been quantified to get better understanding of the bonding mechanisms.

1.5 Thesis Outline

This thesis deals with copper-to-copper thin film bonding based on metallic nanoparticles. Novel approaches for nanoparticle patterning, based on selective wetting or selective catalytic deposition approach are also studied. Various metallic nanoparticles including solgel derived copper, solution reduced silver and catalytically deposited gold, are studied for the purpose of fine pitch interconnection and thermal structure applications in 3D SOP systems.

Chapter 2 deals with the chronological advancement in copper-to-copper direct bonding technology. In addition, a brief review of alternate bonding technologies is presented. The process parameters affecting the bonding characteristics are reviewed. Lastly, various mechanisms affecting diffusion controlled copper to copper direct bonding are discussed.

Chapter 3 covers the experimental approach of the present work. This includes synthesis of different nanoparticles using sol-gel technique followed by gas reduction, and wet-chemical synthesis. Experimental details of nanoparticle patterning approach are also presented. Lastly, the details of thermocompression bonding and methods of structural, mechanical and morphological characterization are presented in the chapter.

Chapter 4 describes the nanomaterial synthesis results, thermocompression copper to copper bonding, bonding characterization and fine pitch process demonstration.

Chapter 5 presents the key conclusions from this research work. Chapter 6 recommends some future works that can be done to further consolidate the results, and to provide greater understanding and industrial viability of nanoparticle based copper-to-copper bonding.

2. LITERATURE REVIEW

High speed and multi functionality in digital and mixed signal devices demand short and reliable interconnections, fine pitch, higher I/O density and 3D packaging [29]. Thinner modules with embedded actives are beginning to drive the need for less than 20 micron pitch interconnections [29]. Multicore microprocessors to achieve high signal speed and data rates at low power constitute another application that is being witnessed by present generation computer and communications technology [30]. These multi-core architectures are pushing the I/O density to more than 10,000/cm^2 and pitch to less than 50 microns [30, 31]. Downscaling solder plating inevitable leads to barriers from solder plating process control and solder bridging at fine pitch. Solder reliability requires a complex stack of UBM, barriers and surface finish making them less attractive for size miniaturization and low cost. Dominating role of intermetallics at fine pitch and the associated thermomechanical failures is another big concern with solder based technologies. In addition, underfill is required to compensate for the thermomechanical stress in solder based interconnections, which raises significant concern in fine pitch technologies where dispensing of underfill becomes a daunting challenge. According to International Technology Roadmap for Semiconductors (ITRS-2006), the supply current in high performance microprocessors is expected to increase to 220 A by 2012 [3]. At such supply current, the current density will exceed the maximum allowable current density of solders [12]. In addition, traditional solder based interconnection technology has high resistivity, mechanically reliability issues due to formation of intermetallics at the bond interface and high electromigration at high frequency. Microelectromechanical systems (MEMS) based sensors and actuators are other

applications that would require alternate interconnection approach beyond solder [14]. Therefore, there is a need for an innovative bonding and assembly approach that can address the aforementioned issues.

Various research groups have reported alternate technologies to address these issues. Yeoh et al [32] have studied on copper pillar technology coupled with solder technology to achieve electrically and mechanically more reliable bonding. It has been reported to be beneficial for low k interlayer dielectrics integration into back end interconnect architecture. Such approach can partially or fully reduce the low k dielectric failure. Moreover, copper die bumps as used in the process has added advantages that includes lowering of critical dimension floor, simple underbump metallization scheme that can improve electromigration resistance and higher I/O density than seen in earlier technologies. In addition, they are very compatible to high volume manufacturing as observed in Intel's 65 nm technology, which employs eutectic lead-tin solders to mate copper die bumps [32]. Similar approach has been reported by Wang et al [33]. The novel characteristic of their study is the use of non-reflowable pillar like copper base and reflowable eutectic lead tin (Sn63Pb37) solder cap processed using electroplating for 200 micron pitch for silicon on insulator substrate. They reported no shear strength deterioration after 1000 hr thermal cycling. In addition, it has been claimed that the maximum shear stress for 200 micron pitch lies below the shear strength of copper, and thus a notably reliable interconnect can be expected. Such composite technology based on Copper bumping reportedly enables easier processing, minimizes the thermomechanical concerns, distribute the current density uniformly over the interconnection, and lowers the bump temperature to mitigate several reliability issues. Nevertheless, solders based bonding approach involves several interconnection processing steps, barrier layers to prevent diffusion and still impose bottlenecks associated with intermetallics and

electromigration. Traditional solder interconnections may not be adequate to meet the fine pitch process constraints, thermo-mechanical and electrical reliability requirements in the emerging packaging applications [3, 34].

Another emerging technology is gold stud bumping [35-48]. Gold bumping can be grouped into two categories - thermocompression gold to gold bonding without any adhesive layer and thermocompression bonding using adhesive layer such as Anisotropic Conductive Fillers (ACF) and Nonconductive Filler (NCF). Details of gold stud bumping technology can be found out in the research paper of Miessner et al [38]. Gold stud bumping, typically, involves bonding of gold wire to the substrate, which is induced by thermal and ultrasonic energy coupled with pressure, followed by shearing off the wire from the formed ball to leave a stud bump [35]. Direct gold to gold bonding using thermocompression technique can be useful to lower the bonding temperature and achieve high bond reliability. However, planarity and the bump shape are important issues that are deterrent to the effectiveness of such process. Majeed et al has studied the reliability issues in gold bump technology for flip chip applications [35]. Some of the reliability concerns can be addressed using conductive film adhesives. Oh et al has reported a thermoplastic conducting polymer bumping approach that uses thick film photoresist to achieve high planarity bumps [49]. Such process can decrease the bonding temperature and eliminate the need of adhesive. A notably low contact resistance and high degree of planarity have been reported. However, this technology involves added process steps and low pitch resolution. Similar approach by Johanson et al uses an epoxy perform and aligns it on the die which is then aligned to the substrate and bonded by simultaneous application of pressure and temperature [50]. This approach needs very high degree of alignment resolution. Gold stud bumping and bonding using Anisotropic Conductive Film (ACF), Isotropic Conductive Film (ICF) and

Nonconductive Film (NCF) have been understood to be more attractive [35, 51]. This polymeric adhesive can eliminate some of the problems associated with the earlier bonding approaches. Low temperature bonding, simple processing steps, fine pitch capability and high reliability make these attractive candidates for next generation packaging applications [35, 52]. However, these polymeric adhesives have modest electrical performance than the metal interconnects such as copper. Therefore, there is a need to develop an all copper based interconnect approach that can enhance the electrical performance and enable high signal speed.

Recently, there has been several reported works that discuss approaches to carry out copper to copper direct bonding. Table 2.1 lists important works in chronological order. Copper to copper direct bonding using thermo-compression method is most attractive in this regards. The bonding is carried out by thermally induced diffusion. Several research group including Veer, Kolster et al. [53], Ward and Carroll [54], and Iijima, Wakabayashi et al. [55] have studied the diffusion characteristics of copper in copper silicon systems that includes the inter diffusion coefficient and vacancy assisted self diffusion coefficient. Though the reported values of temperatures are higher than the bonding temperature of interest, the above mentioned works give the basic understanding of the diffusional process that is crucial for thermo-compression bonding. The pioneering work on actual demonstration of copper to copper direct bonding has been done by Fan et al [17] and Chen et al [13, 18-27]. Fan et al demonstrated copper to copper face to face bonding at 450 C for 30 min. followed by 30 min nitrogen annealing at same temperature range. The thickness of evaporated copper, which was used in the process, was 300 nm. They reported good quality bonding with their processes. However, in absence of quantitative bond strength measurement bonding at different process parameters could not be comprehensively compared. In addition, it was found that the presence of diffusion layer (Ta) did

not affect the bonding at the bonding temperature of interest. From this finding it can be safely concluded that the bonding doesn't involve copper –silicon diffusion that is only interlayer copper self diffusion across the bonding interface is only important. This is an important understanding because the diffusional work done in copper silicon systems reveals very fast diffusion kinetics of copper in silicon [53-55]. Since copper is a deep-level trap for carriers, a diffusion barrier is indispensable [17].

Further work by Chen et al developed methods to carry out bonding at 400 C at 4000 mbar pressure. Also, studies on microstructural evolution at the interface and other bonding locations during the bonding process suggest several phenomena including copper self diffusion, recrystallization and grain growth acting together to form a strong metallurgical bond some time free of any identifiable interfacial region. However, the bonding interfaces may take several forms including indistinguishable interface, zigzag interface and distinct interface.

Table 2.1 Chronological listing of important literatures on copper-to-copper bonding by various research groups

Research Group	Experimental Variables	Salient features	Reference
Iijima, Wakabayashi et al.	• Copper-silicon (up to 8%) system • Temperatures ranging from 900-1150 K	• Inter-diffusion of copper in copper in copper rich silicon system • Intrinsic diffusion of copper	[55]
Fan, Rahman et al.	• Silicon wafers with evaporated copper (150-300 nm) • Bonding temperature – 450 C for 30 min • Bonding pressure- 4000 mbar • Annealing temperature – 450 to 600C for 30 min • Qualitative Razor test for bond assessment	• Successful bonding with appreciable strength • Ta diffusion barrier has no effect on bonding • Post bonding annealing improves the bonding quality. • No effect, however, is noticed as a result of change in annealing temperature due to lack of quantitative assessment of bonding	[17]
Chen, Fan et al.	• Silicon wafer with 300 nm evaporated copper • Bonding temperature – 400 C for 30 min • Bonding pressure – 4000 mbar	• Good morphological understanding • Homogeneously distributed oxides and defects • Basic understanding of	[21, 25]

	• Annealing – 400 C for 30 min	underlying mechanisms	
Chen, Fan et al.	• Process parameters same as [17]	• Roughness is found to be very critical • Indication of recrystalization and grain growth • Various possible mechanisms are proposed	[13]
Chen, Fan et al.	• Bonding -300-400 C for 30 min • Nitrogen annealing at 300-400 C for 30 min	• Effect of bonding temperature and time is established • Good bonding at high bonding temperature coupled with less annealing time as well as at low bonding temperature and more annealing time suggesting diffusion to be very critical for bonding • Bonding temperature can be thus reduced to 350 C at the expense of overall bonding time (1.5 hr)	[24]

Chen, Fan et al.	• Face to face bonding at 400 C for 30 min • Nitrogen annealing at 400 C for 30-60 min	• Demonstration of copper to copper bonding technology for 3D integration • Contact resistance is appreciably low especially for longer annealing time suggesting that the contact resistance is directly related to the post-bonding annealing	[23]
Chen, Chang et al.	• 4 layers stacking of silicon wafers	• Demonstration of multi-stacking using copper to copper bonding • High residual stress to cause bowing in large wafers • A homogenous bonding with nonidentifiable interface	[27]
Chen, Tan et al.	• Face to face bonding with various surface roughness • Bonding parameter same as [24]	• Better understanding of the effect of surface roughness on the bond strength and quality	[18]
Chen, Fan et al.	• Bonding parameter similar to [24]	• Review of various bonding parameters that affect the bonding quality and electrical performance	[22]

Chen, Chang et al.	• Bonding parameter similar to [24]	• Thermal annealing is effective at high bonding temperature only • Investigation of bond quality using various qualitative as well as quantitative methods (Die shear and wire pull test	[26]
Ate, Osborn et al.	• Silicon wafer with high aspect ratio electroplated copper • Bonding at room temperature followed by annealing at 250 C • Mechanical shear force measurement for bond characterization	• Room temperature bonding using electroless copper deposition • Electroless copper makes up for nonplanarity and misalignment • Bond strength as high as 148 MPa	[12]
Tadepalli and Thompson	• Silicon all copper to copper bonding • Ultrahigh vacuum (2 X 10^{-10} torr) • Bond strength analysis using AFM surface energy analysis at high vacuum (10^{-10} torr)	• Room temperature bonding in ultrahigh vacuum environment • In presence of oxide layer needed bonding temperature is 300 C or above • Good bonding	[11]

2.1 Process Parameters for Thermo-Compression Bonding

Copper to copper direct bonding using thermocompression is a diffusion driven process and thus the quality of the bond depends on several diffusion thermodynamic and kinetic phenomena. Therefore, several critical process parameters that can affect the bonding behavior include bonding temperature, pressure and time, annealing temperature and time, bonding environment, cleanliness, intimate contact and roughness of the matting surfaces. The effect of various bonding parameters on the bond characteristics is reviewed by Chen, Fan et al. [22]. A short overview of that is as following.

2.1.1 Bonding Temperature:

For diffusion-driven process, temperature becomes very important parameter. Temperature provides copper atoms with required kinetic energy to diffuse across the interface. In addition, the grain growth is higher at high temperature. Therefore, the bond quality can be enhanced by adopting high bonding temperature. Nevertheless, material considerations require low thermal budget to prevent degradation. Typically, bonding is done at 400^{o}C for 30 minute followed by annealing for 30 min. This has been reported to provide a reliable bonding with a distinguishable bond interface. However, bonding at 300^{o} C for 30 min and longer annealing time can also help achieving reliable bonding; however a longer total bonding time can make the bonding interface indistinguishable.

2.1.2 Post bonding annealing

Post bonding annealing has been found to be very important in enhancing the quality of the bonding by providing more opportunity for diffusion processes. The annealing temperature is usually kept same as the bonding temperature. As discussed earlier, longer post bonding annealing can render indistinguishable bond interfaces.

2.1.3 Bonding and annealing duration

Since diffusion is a kinetic phenomenon, the bonding and annealing durations therefore are important key parameters. Bonding time becomes even more crucial for low temperature bonding. 30 min bonding and 30-60 min post bonding annealing has been reported to be optimal for reliable bonding at 300-400 bonding temperature.

2.1.4 Bonding pressure

Inter diffusion is enhanced by making the matting surfaces as close as possible. Therefore, sufficient pressure is needed to achieve a reliable bonding. Typical, bonding pressure applied by various researchers is around 4000 mbar.

2.1.5 Bonding Environment

Bonding environment should be chosen with care to facilitate a good quality bond. As copper is very reactive, presence of oxygen can form oxide layer on copper surface and thus can deteriorate the bonding quality. Thus, a vacuum or inert environment is better suited for copper-copper direct bonding. Vacuum has an added advantage in that it can ensure a clean atmosphere by effectively ensuring less number of particles present in the bonding atmosphere. Typical,

bonding is done in a vacuum atmosphere (10^{-3} torr). Oxygen is removed by nitrogen purging prior to bonding.

2.1.6 Surface conditions

For good bonding, it is imperative to have a clean bonding surface free of deleterious particulates, which can appear as barriers to the bonding process. Surface roughness is also very important. A good bonding requires surface roughness as low as possible. The recommended surface roughness is around 5 nm. Surface roughness increases when the copper oxide layer is removed from the copper surface using HCL as cleaning reagent. Hence, prevention of copper oxide formation is necessary. Bonding is better if the bonding follows immediately after copper evaporation or electrodeposition. Some research groups have carried out bonding without removal of copper oxide. A good bonding can still be achieved using higher temperature and bonding duration, thus making this less attractive.

2.1.7 Bond quality assessment

Bond quality analysis using bond strength measurement helps understand the underlying bonding mechanism including the chemical reactions that takes place during bonding and annealing [56]. Vallin, Jonsson et al. have done a thorough review on various methods for bond quality assessment [56]. A brief description of some of the available methods is presented in this section. There are several qualitative and quantitative methods for bond quality assessment. However, the attractiveness of a method is quantized in terms of cost and time involved in a measurement. In addition, nondestructive testing is more attractive in such a way that the bond strength can be measured without breaking the bond interface.

Qualitative approaches give fair idea regarding the bond quality. However, they are not suited for good comparison of the bonding strengths. A small change in the bonding strength is not detected through qualitative approach. There are several qualitative approaches including dicing and razor test. The bond quality assessment using these methods are based on the percentage of successful dicing or cutting..

Quantitative bond strength assessment approaches, however, provides quantified measurements to compare and contrast between the bonding of interest. There are several techniques for quantification of the bond strength including Double Cantilever Beam (DCB) test, Tensile test, Chevron test and Die Shear test. In DCB method the bonded interface is sheared apart using thin blade and bond strength is measured in terms of the length of the crack. This is a difficult process especially for brittle materials, such as Silicon, since insertion of blade might break Silicon. In addition, it is most suited for week bonds as it is very difficult to insert blade inside strong bonds. Tensile test is also not very suitable for brittle silicon as the test involves pulling test samples by a tensile test machine. Chevron test is similar to tensile test. This is done using test structures with chevron shaped notch. This test is particularly useful for brittle materials. Die shear test involves shearing of the bond using shear force parallel to the bonding interface. The shear force per unit contact area that is required to break bonding gives the shear strength.

2.2 Bonding Mechanisms

Chan, Fan et al have proposed several mechanisms of copper to copper direct bonding [13]. Their work reveals that the bonding is a strong function of the surface roughness, and bonding is associated with recrystallization and grain growth during bonding and annealing processes. Copper to copper bonding occurs due to interdiffusion of copper between two contact surfaces due to temperature and pressure. Three possible mechanisms based on contact between two matting surfaces include peak to peak contact between two surfaces having comparable roughness, peak to valley contact of two surfaces with comparable roughness, and contact between two surfaces with different scale roughness [13]. The abovementioned mechanisms have been reported to explain various kinds of interfaces including indistinguishable interface, distinguishable interface and zigzag interface.

Despite of the several developments, copper to copper direct bonding is still in the embryonic stage. The bonding needs high temperature that might not be attractive to next generation SOP based technologies, which integrate several temperature sensitive elements. The situation is excruciated by the longer bonding and annealing time duration to which the system has to be exposed. In most of the cases, the total bonding time is approximately 1 hour. Moreover, to avoid thermal stress induced cracking special care is taken to cool the bonded system, which sometime requires prolonged cooling duration as high as 2 hours. Moreover, emerging trend in semiconductor industries to add low k polymeric materials to reduce RC delay also demands alternate bonding approaches to reduce the thermal budget. Very few alternate technologies have been reported to avoid the high thermal budget induced challenges. Tadepalli and Thompson discussed a low temperature pressure bonding method to join copper films [11].

However, this method requires ultrahigh vacuum of the order of 10^{-10} torr. Similar approach was reported by Kim et al., which was based on surface activated bonding approach [57]. They claimed void or defect free bonding with a bonding strength of 6.47 MPa. However, this method requires extremely clean and planarized surface, activated using Argon ions bombardment in ultrahigh vacuum. Another method was reported by Ate, Osbom et al., which was based on electroless copper deposition [12]. High aspect ratio copper pillars are first fabricated using thick polymer layer on both substrate and die side, and then bonding is carried out using electroless copper deposition. Electroless copper is claimed to compensate for the misalignment and coplanarity issues. However, this method is too process intensive. Therefore, still there is a need to devise novel technologies that can some of the aforementioned concern.

To overcome the abovementioned disadvantages, metallic nanoparticle based thin film copper bonding has been investigated. Next chapter discusses the details of the experimental procedures.

3. EXPERIMENTS

This chapter deals with the experimental details used in the synthesis of nanostructured metallic particles that include Copper, Silver and Gold. The shape of the nanomaterials significantly depends on the process variables such as choice of precursors, concentration, stirring conditions and reaction temperature. However, an optimal synthesis scheme is chosen to ensure spherical nanostructural metallic particles, as suited for thin film bonding purpose. Various techniques used for copper to copper bonding with different interface layers are also described in later subsections. Lastly, different characterization schemes including structural, morphological and bond strength characterization, as utilized in the study, are presented.

3.1 Nanostructured Spherical Copper Particles

An increase in the surface area to volume ratio increases the surface energy of the copper nanoparticles, hence nanoparticles are very prone to oxidation and grain coarsening even at room temperature. This is more predominant with base metals such as copper. To avoid these, an in-situ synthesis and bonding approach using gel-derived nanocopper is pursued. A low cost, low temperature sol-gel technique was employed to prepare copper ethoxide gel by dissolving copper precursor in a carrier solvent. The so synthesized copper ethoxide gel upon subsequent reduction in a reducing atmosphere produces nanostructured copper thin films for in-situ bonding.

A generic process flow of copper nanoparticles synthesis using such scheme has been shown in the Figure 3.1. A 0.05 Molar Copper (II) ethoxide $Cu(OC_2H_5)_2$ (Alfa Aesar) was dissolved in 50 ml of 2-methoxyethanol (2-MOE) as the carrier solvent in a flask and refluxed at 125ºC for 4 hours in nitrogen atmosphere. The solution was then cooled to room temperature under same environment. The anhydrous copper precursor solution so formed was again refluxed at 125ºC for 1 hour. The resulting precursor solution was then spin coated at 2000 RPM for 30 seconds on silicon wafer coated with titanium/copper thin layer to form a thin and uniform organometallic film. The thickness and uniformity of the film are function of the spinning variables such as speed and time of spinning. Therefore, optimization of process variables is needed to ensure uniform thin layer of copper gel. The film thickness affects the reduction ease and hence, a thin film (approximately 1-5 micron thick) was deposited to facilitate reduction. The spin coated wafers were then reduced in forming gas (5-10% H_2 and N_2) atmosphere at 200-400^{o}C in a tube furnace and Rapid Thermal Processing (RTP) chamber. The RTP chamber is an enclosed chamber, which due to high temperature ramping rate is useful to decrease the reduction time. As compared to RTP chamber, reduction in tube furnace calls for extra precautionary measures to prevent gas leakage and unwarranted oxidizing atmosphere due to bad sealing of the tube. Therefore, reduction in the tube furnace warrants purging for several times with forming gas before increasing the furnace temperature.

3.1.1 Maskless patterning of copper nanoparticles precursor

Metal based bumping is easily done with electroless or electrochemical plating. However, nanoparticle and nanopaste patterning technologies at fine pitch of less than 100 microns are not widely developed. Selective patterning of copper precursor gels on bond pads was investigated to

avoid complex photopatterning and inkjet printing processes. Such maskless patterning process reduces number of process steps associated in patterning of bonding layer. A suitable polymer surfaces is selected to enable selective wetting on the metal pads.

Solution carrier chosen for the copper precursor induces selective wetting on preferred surfaces and does not wet unwanted surface, and thus ensure maskless patterning of the copper gel. The wetting behavior of the copper precursor was qualitatively studied by spin coating of the solution over various surfaces including copper, gold, silicon dioxide and polyimide. Process variables of spin coating were optimized to get an optimal wetting on copper surface and insignificant or no wetting on polymer and silicon dioxide surface. The spin coating resulted in formation of thin film on the copper pads, and some loosely bonded droplets of copper precursor on polymer and silicon dioxide surface, which was then, removed using acetone or isopropanol solvent.

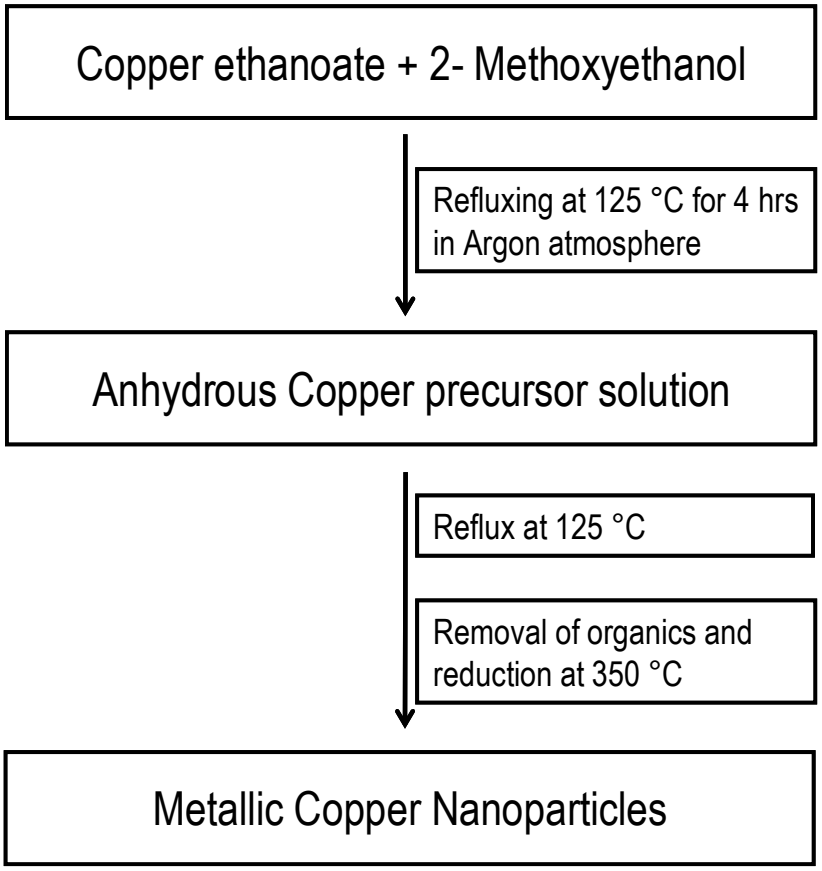

Figure 3.1 Synthesis scheme of sol gel derived copper nanoparticles

3.2 Solution Reduction Derived Nanostructured Silver

The nanogranular silver used in the process was synthesized using solution reduction technique. The process detail has been shown in Figure 3.2. A 0.04 molar Silver Nitrate (Sigma Aldrich) was dissolved in 50 ml of 2-methoxyethanol (2-MOE) that acts as an organic solvent. The solution was thoroughly mixed using magnetic stirrer for 30 min. Polyvinyl Pyrrolidone (PVP, Sigma Aldrich) was then added to solution and thoroughly mixed by stirring for several minutes. The molar ratio of PVP to Silver Nitrate is an important parameter that dictates the silver particle size and distribution after reduction by a reducing agent. Therefore, an optimum

amount of PVP was chosen to control the silver size in the range below 200 nm. Furthermore, addition of PVP in the Silver Nitrate solution results in formation of Ag-PVP complex due to PVP lone pair electron donated to Ag s-orbital. This complex is easier to be reduced by a mild reducing agent at low temperature. Sodium Tetrahydridoborate ($NaBH_4$, Sigma Aldrich), a reducing agent, was then added to the solution and stirred for several hours. The resulting solution was kept for 6-7 hours, and then filtered to get fine granular silver particles. The silver particles thus formed were then dissolved in low molecular weight organic solvent.

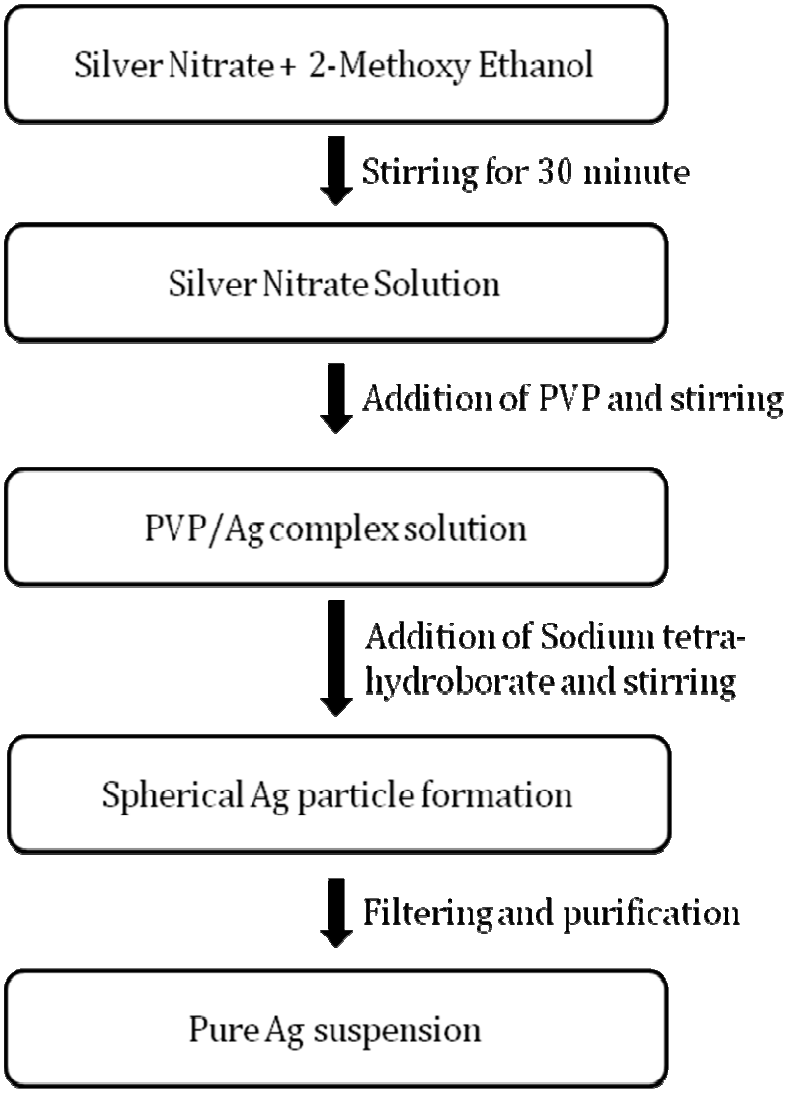

Figure 3.2 Process flow of solution reduction synthesis of nanostructured Silver

3.3 Wet chemical synthesis of nanostructured Gold

The Gold particles were prepared at room temperature using wet chemical process by catalytic reduction of Gold (III) Chloride. A generic process flow of gold particle synthesis has been shown in the Figure 3.3. The aqueous solutions of analytical grade Gold (III) Chloride ($HAuCl_4$, 99.999%, Sigma Aldrich) was added to dilute nonionic surfactant t-

Octylphenoxypolyethoxyethanol solution (Triton X-100 solution, Sigma Aldrich), followed by addition of Hydroxylamine (NH_2OH, 99.999%, Sigma Aldrich) under sonication for rapid mixing. The resulting reaction mixture was purified by washing several times with de-ionized water (ddH_2O). The particles were stored in ddH2O until use.

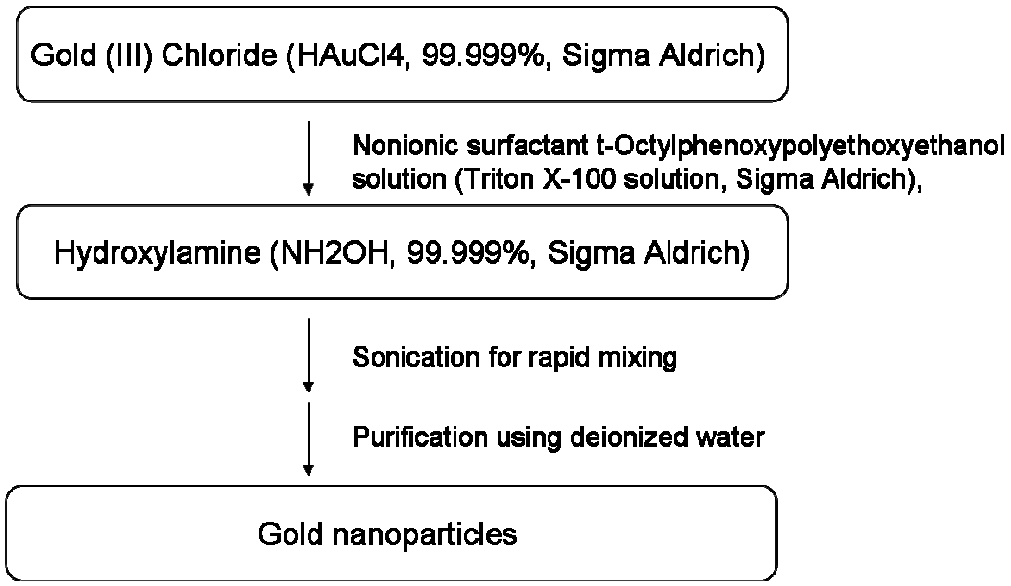

Figure 3.3 A generic process flow of gold nanoparticle synthesis

3.3.1 Patterning of Gold nanoparticles

Preferential patterning of gold nanoparticles on copper and gold pads was done by taking advantage of catalytic effect of copper on the reduction reaction on the desired locations. The die with copper interconnection patterns was immersed into a beaker containing the aqueous solution of gold (III) chloride, the nonionic surfactant Triton X-100 solution and hydroxylamine. The gold particles are instantly preferential nucleated on the copper surfaces. The reaction was stopped by immersing and rinsing the die with ddH_2O.

3.4 Test Vehicle Fabrication

A simple die-substrate assembly was fabricated to demonstrate copper-to-copper bonding. The die, consisting of peripheral array of interconnects at a pitch of 30 and 200 μm was fabricated onto a 4'' silicon wafer using etch back process. The fabrication was assisted by two glass masks, containing a thick (800 Å) chromium layer that acted as an absorber pattern metal. These transparent glass masks (to UV light) were placed in direct contact with the photo resist coated wafer surface in subsequent process steps and exposed to UV light. The first glass mask defined the copper pad and the second defined the daisy chain structures on the die. A generic process flow of die fabrication method is illustrated in Figure 3.4. The process consisted dc sputtering deposition of Ti/Cu/Ti/Cu layer on a silicon wafer with a thin layer of silicon dioxide deposited by plasma enhanced chemical vapor deposition. Titanium layer works as the adhesion layer as well as etch protection layer. Shipley 1827 photoresist was spin coated on the wafer at 3000 rpm spinning rate and a ramping rate of 500 for 30 seconds. This was then exposed and patterned. Top copper and titanium layer was then etched out to make copper pad on the wafer. After striping the first photoresist layer, a thick Shipley 1827 photoresist was spin coated on the wafer at 1000 rpm spinning rate and 500 ramping rate for 30 seconds. This photoresist was patterned using daisy chain mask and similar procedure was repeated.

Similarly the substrate was fabricated on silicon wafer using etch back process. Ti/Cu was sputtered on Si/SiO_2 using DC sputterer. Copper interconnection were made on the substrate using substrate mask. A similar process flow as die fabrication was adopted to fabricate substrate.

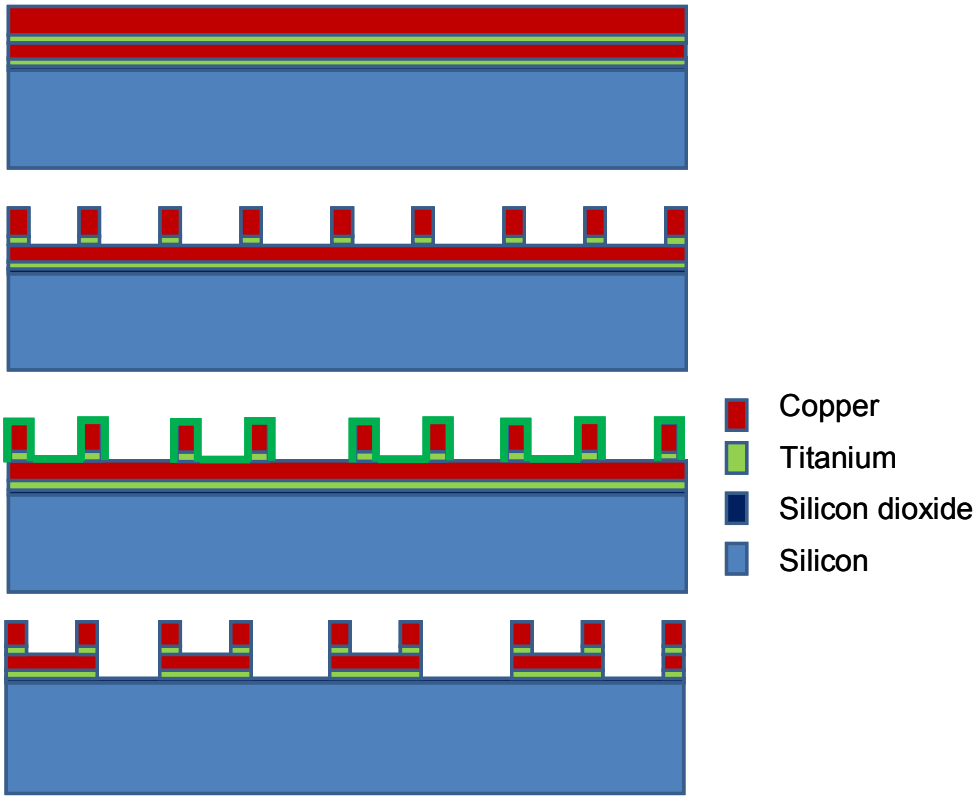

Figure 3.4 Generic process flow of etch process for die fabrication

3.5 Copper to Copper Bonding

Copper to copper bonding process involved synthesis and subsequent or simultaneous patterning of nanoparticles followed by thermocompression bonding. Thermocompression bonding was done in various environments at different process parameters to optimize the bonding process.

3.5.1 Copper bonding using copper precursor solution

Copper precursor solution was preferentially coated on the substrate copper pads using spin coating at 2000 rpm and 500 ramping rate for 40 seconds. The die and the substrate was

then aligned, and pressed using a normal compressive force. The assembly was then heated at a temperature of 350^{o}C under an applied pressure of 500 kPa under a reducing dry forming gas (5-10% N_2/H_2) environment. The copper bump stand-off height allowed reducing atmosphere under the whole die area. For simplicity, sometime substrate with copper interconnections was replaced by copper blanket (sputter deposited wafer). A novel rapid thermal processing (RTP) tool with infrared lamps was utilized to lower the process time to less than 10 minutes. In this way, a high throughput can be accomplished compared to traditional Cu-Cu bonding that takes 1 hour.

3.5.2 Copper to copper bonding using silver nanoparticles

The solution containing silver suspension was first spin coated on a silicon wafer coated with copper thin layer using 3000 RPM for 30 min. High spinning speed ensured a thin and uniform layer of silver solution over the copper surface. This spin-coated wafer was then placed onto a silicon substrate with copper finishing. The bonding was done using simultaneous application of temperature and pressure. The bonding was performed under various atmospheric conditions –

a. FINETECH Flip Chip Bonder (FINEPLACER) was used to bond copper to copper in ambient atmospheric conditions. After placement of the chip on the substrate, the chip and substrate are heated to a specified temperature. The chip-contact heating module and heating plate ensure controlled temperature on die and the substrate heating. The chip contact module heats the die by direct contact thermal transfer. The heating plate is attached with an internal gas cooling system that helps to achieve very high ramping rate. Simultaneous force is applied using bonding force module. The bonding force is applied

by lever-shaft force transmission using a separate force arm. The FINEPLACER can apply as high as 20 N bonding force and has a resolution of 0.1 N. For thin film bonding using silver nanoparticles a thermal load of 370 degrees for 5 minutes on the substrate side and same temperature for 10 minutes on the die side were applied. The normal compression force was maintained at 20 N.

b. A nitrogen gas furnace was utilized to perform bonding under an inert atmosphere. The bonding temperature and pressure were same as above. The bonding time varied from 5-30 minutes.

3.5.3 Copper bonding using gold nanoparticles

Die and substrate were prepared as discussed in earlier section and gold nanoparticles were preferentially deposited on substrate copper pads using catalytic gold deposition as described in section 3.3.1. The substrate and the die were then aligned in FINEPLACER flip chip bonder. A detailed description of the procedure has been given in section 3.5.2. The bonding temperature was 370^{o}C and the compressive bonding pressure of 500 MPa was used for 5 min.

3.6 Bonding Characterization

3.6.1 X-ray diffraction analysis

X-ray diffraction study of the nanostructured copper was done using PANalytical X'pert PRO Alpha. The diffraction profile was measured using Cu-Kα (1.54 A) radiation. A divergence slit of ½ degree and an Xcelerator detector was used. To minimize the diffraction from the

substrate an offset of $1^{o}\omega$ was used. Measurements were taken from 20-100^{o} at a scan rate of 0.002 counts per second.

3.6.2 Field emission scanning electron microscope

The morphological study of the copper nanoparticles and the bonding interface was done using Thermally Assisted Field Emission Scanning Electron Microscope (FESEM LEO 1530). This has a capability of 3 nm resolution at low voltage (1kV).

3.6.3 Destructive die shear test

The bond strength was measured using DAGE 4000 (Dage Precision Industries) die shear testing tool. Compressed air (4 bar minimum) is utilized to operate the shear cartridge, which can apply a shear load of as high as 100 Kg. A frictionless load cartridge system and air bearing technology ensures maximum accuracy and thus is useful to measure very small load with high precision.

4. RESULTS AND DISCUSSIONS

This chapter describes the key process results from this research and discusses the key findings. This includes results involved in the synthesis of sol-gel derived nanostructured Copper by gas phase reduction, nanostructured silver by solution reduction technique, and wet-chemical synthesis of nanostructured gold, and subsequent processing techniques. Structural and morphological characterizations are done using X-ray diffraction and thermally assisted field emission scanning electron microscope (FESEM). The results associated with thin film copper to copper bonding using aforementioned nanostructured metallic interfaces and subsequent bond strength characterization are also presented in this chapter.

4.1 Sol-gel Derived Nanostructured Copper

As described in the previous chapter, the nanostructured copper was synthesized by gas phase reduction of sol-gel derived copper precursor solution in forming gas atmosphere. The Cu K_α X-ray diffraction profile, as shown in Figure 4.1 shows the copper diffraction peaks for the nanocopper reduced in RTP for 5 min and 20 minutes time at 350^{o}C. Notably a reduction for 5 min can result in partial reduction of copper precursor to copper particle. However, an increase in the reduction time up to 20 min completely can drive complete reduction of copper precursor. Ankur et al. has shown that such solution sol-gel derived copper precursor can be reduced at a

temperature less than 300^0C [58]. However, the time for reduction is higher (approximately 40 min) for low reducing temperature.

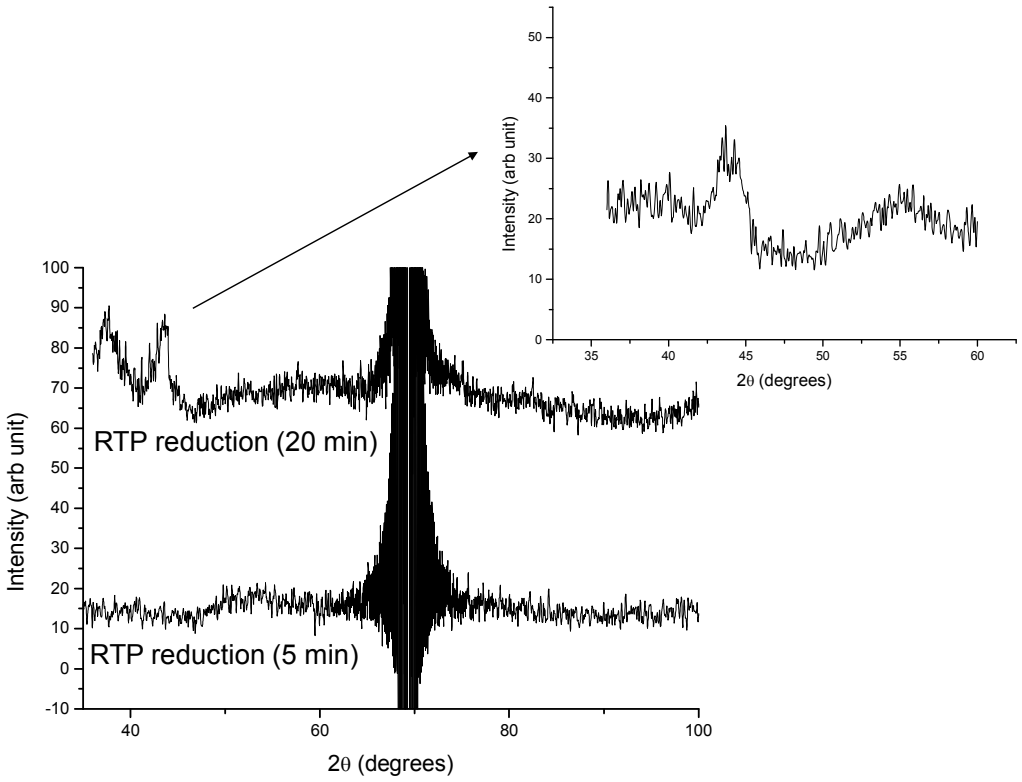

Figure 4.1 X-ray diffraction profile of sol-gel derived copper after reduction in rapid thermal processing tool in forming gas environment

The FESEM micrograph of the copper formed after reduction in RTP for 20 minutes at 350^oC is shown in the Figure 4.2. As evident, the copper particles formed are smaller than 50 nm in size and are densely populated. The final particle size after gas reduction depends largely on the purity and homogeneity of the precursor solution. In addition, the sol-gel parameters affect the final particle size. Therefore, optimization of the affecting parameters is necessary to achieve an ultrafine and well disperse copper particles. The purity can be ensured by using pure starting precursor materials, homogeneity is ensured by elongated stirring, fine starting precursor

particles, optimal refluxing and stability time. Moreover, reduction in RTP under forming gas atmosphere renders finer particle after reduction, than observed with reduction in conventional forming gas furnaces. RTP because of very high ramping rates checks the grain growth and thus very fine grains are achieved.

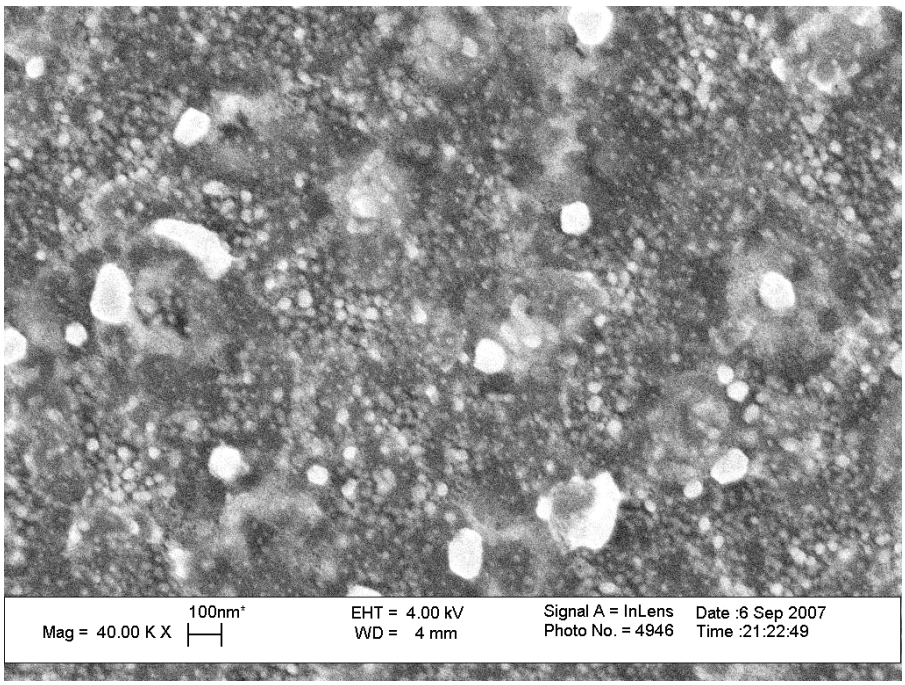

Figure 4.2 FESEM micrograph of sol-gel derived copper nanoparticles

Patterning of nanoparticles on the copper interconnection pads is crucial to be able to make use of them for bonding. Like other patterning technologies such as metal based bumping, electroless plating and contact lithography followed by etching, patterning of nanoparticle suspension or nanopaste at fine pitch is not well developed. Therefore, a novel method was developed for patterning of copper nanoparticles. Instead of patterning final nanogranular copper, the sol-gel derived copper ethoxide precursor was patterned as it was observed to be easier to pattern than the former. Due to the preferential wetting of the precursor on copper pads

as opposed to interlayer polymeric dielectric or solicon dioxide, this can be easily spin coated preferentially on the copper interconnection pads while leaving the other area as it is. Thus, a maskless patterning can be done, which eliminates several process steps. However, a good patterning requires optimization of several process variables that affect the quality of the pattern. The important process variables include the spinning rate, ramping rate, time of spinning and precursor viscosity. Optimal selection of process parameter resulted in a good quality copper precursor film on copper surface but practically insignificant loosely bound droplets of copper precursor on silicon oxide and/or polyimide. Figure 4.3 shows an optical micrograph of copper precursor solution on a substrate, after spin coating. As evident, the copper precursor makes thin film on the copper pad, whereas that don't attach to the polymeric surface used for passivations. However, some droplets are present on the polymer surface that can be removed by immersing the die into ethanol or acetone solution. The copper particles formed on the polymer surface due to the reduction of left over copper precursor solution are scarcely dispersed on the polymeric surface as can be observed in the Figure 4.4. In addition, it was observed that these particles were loosely bound to the surface and thus a simple washing in organic solvent like before followed by drying was able to remove these unwanted copper particles from the unwanted region.

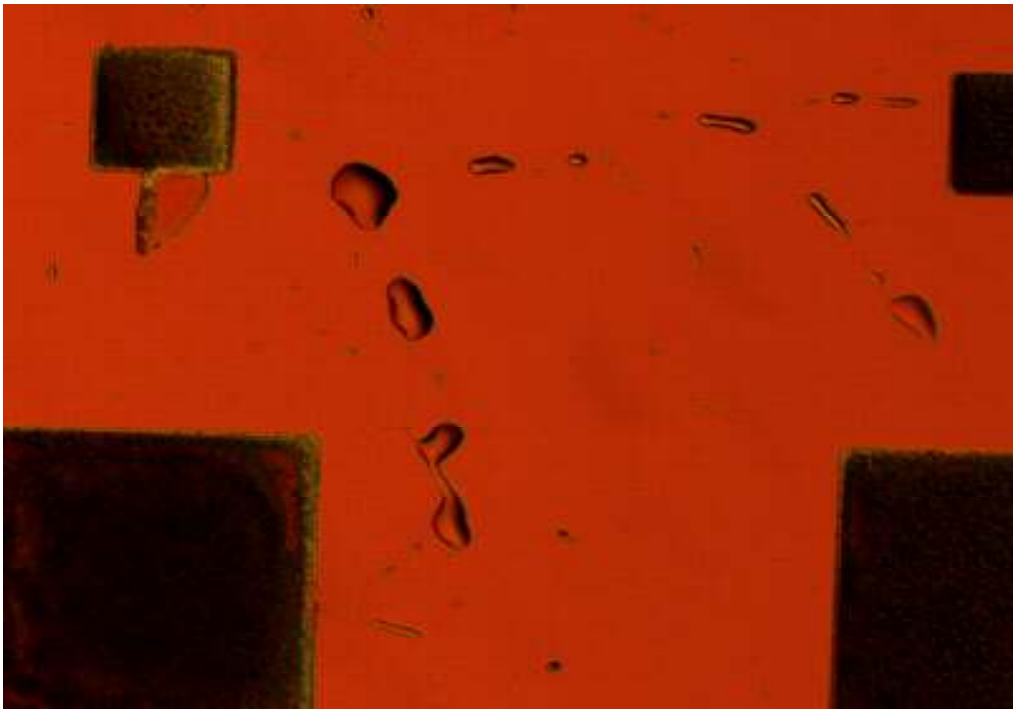

Figure 4.3 Optical micrograph of selective wetting of copper gel on copper

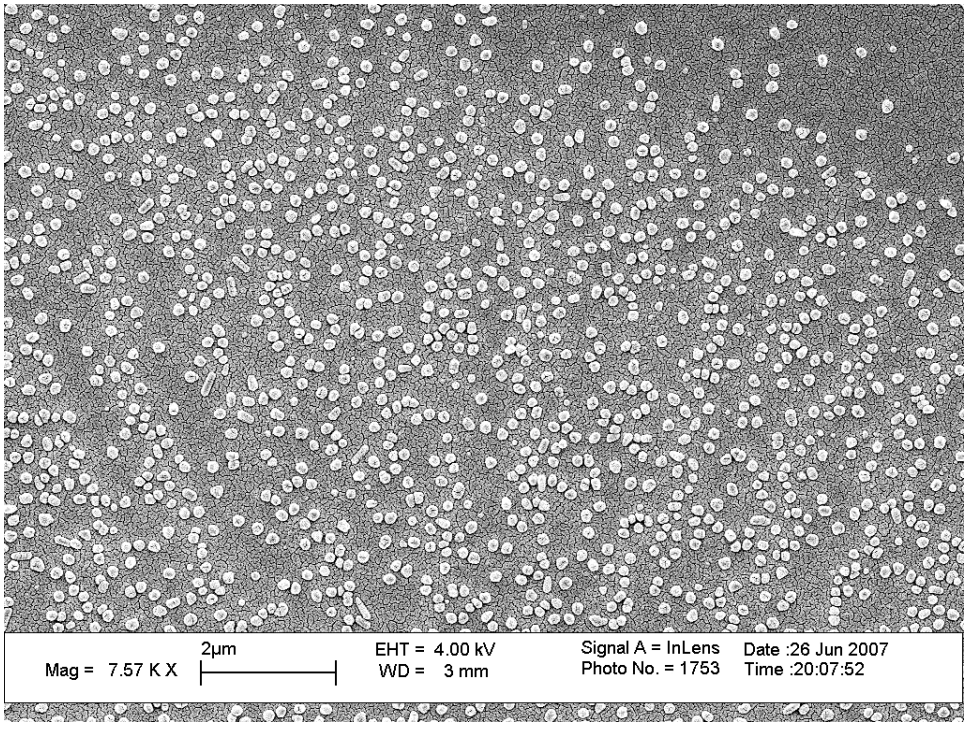

Figure 4.4 FESEM micrograph of sol-gel derived naostructured copper loosely held on polymer surface

Figure 4.5 shows the FESEM micrograph of a copper pad coated with copper precursor thin film using selective patterning technique. As shown, the copper precursor forms a uniform and dense film all over the copper surface and thus is very suited for bonding purpose. However, it should be noted that the bonding quality depends on the in-situ reduction of the film in presence of forming gas. Hence, the film thickness plays a crucial role in determining the bonding characteristics. It is also worth noting that SEM images shows no sign of copper precursor in the surrounding area of the copper pad and thus, prevents any possibility of unwanted electrical contact after bonding.

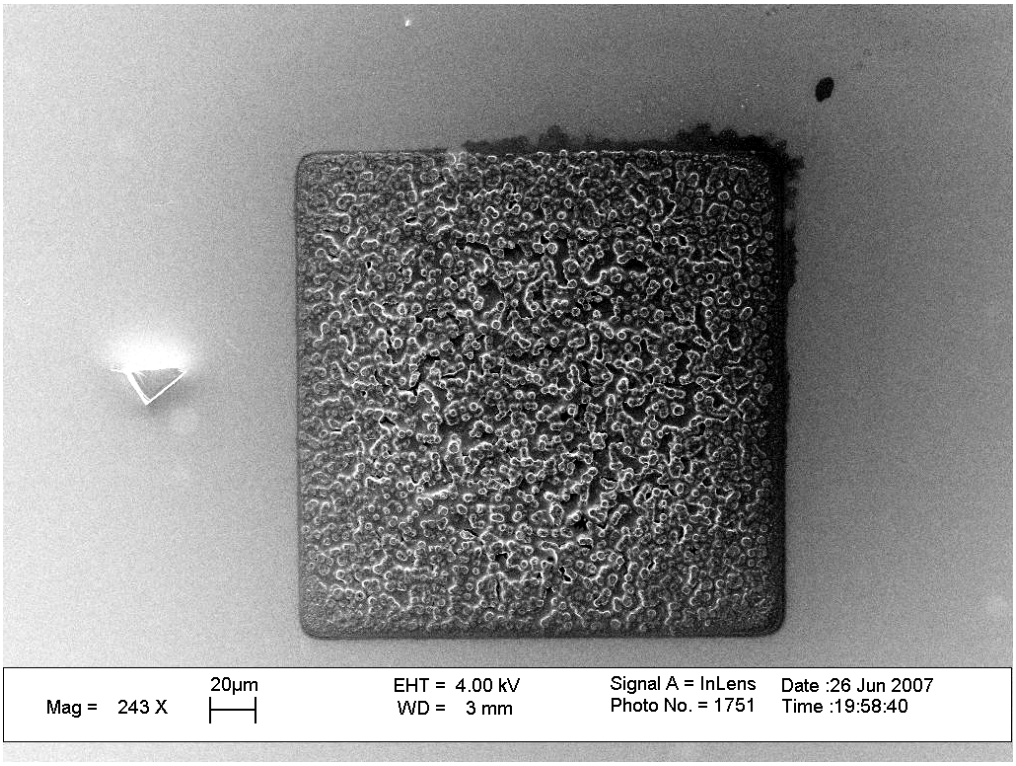

Figure 4.5 FESEM micrograph of selectively wetted copper gel on copper pad

Nanogranular copper facilitates copper-to-copper direct bonding process. To demonstrate bonding a die preferentially coated with copper precursor solution was aligned on a substrate and

pressed using normal compressive force. The detail of the bonding parameters have been given in the previous chapter. Nanoparticle processing is a challenging task, as these are very susceptible to grain coarsening (Ostwald repening) and oxide formation. Both of these can affect the bonding behavior and quality. Therefore, an in situ reduction and bonding was performed in closed reducing atmosphere in a RTP chamber. Reducing atmosphere obviates chances of oxidation and simultaneous occurrence of bonding and nucleation of nanoparticles forestall the Oswald ripening. The assembly was heated at 370^{o}C for 20 minutes and a compressive load of 1-1.5 MPa was applied simultaneously. The quantitative estimation of bonding strength was done using destructive die shear tool. Standard test procedure for destructive shear test of ball bonds (ASTM F 1269) was followed for the purpose. The copper to copper bond strengths for various process conditions is listed in the Table 4.1. As seen, presence of oxygen is detrimental for bonding. Nanocopper in ambient environment at elevated temperature, immediately is oxidized. The presence of oxide coating makes the diffusion process very difficult. Grain coarsening due to elevated temperature also negatively affect the bonding behavior. As the grain starts growing, the surface roughness becomes a big issue. Large grains between the matting surface increases the interdiffusion distance. Grain coarsening and resulting surface roughness coupled with oxidation of copper plays a detrimental role and therefore, practically no bonding is observed even for a prolonged bonding and annealing duration and notably high bonding pressure. However, if the environment is protected bonding can be observed at very low thermal budget. From the table it can be seen that sol-gel derived copper interface provides metallurgical bonding strength in the range of 9-11 MPa, if bonded in presence of forming gas. In situ reduction and simultaneous bonding makes these particle less susceptible to grain coarsening and oxidation. Also, it can be seen that a small change in the bonding force doesn't affect the bonding strength

significantly. The bonding time in both the cases is 6 minute. The morphological examination of fracture surface using FESEM (Figure 4.6) reveals that the fracture occurs at the copper-copper interface. The fractured surface shows big sheared copper particles. As evident, a shear type fracture (ductile) causes shearing of the bonding. Also the FESEM micrograph shows that the fracture involved overall pad area. This further suggests a good metallurgical bonding between copper to copper with sol-gel derived copper interface.

From the above discussion, it is evident that the nanogranular copper is beneficial in decreasing the thickness of bonding interface and minimizing the thermal budget associated with copper to copper bonding without any active nanogranular particulates. In addition to the electrical and thermal superiority, nanogranular copper particles are reported to have enhanced fatigue life and ultimate tensile strength [59]. Thus, a thin bonding interlayer of copper nanoparticles can provide good mechanical stability and hence, a robust bonding.

Table 4.1 Bond strengths of copper to copper bonding using copper nanoparticle interlayer

Bonding Layer	Bonding Tool	Bonding Temp (C)	Bonding Pressure (MPa)	Environment	Time	Shear Strength (MPa)
Solgel nanocopper film reduced in RTP with 10% FG	Fine placer thermocomp. Bonding	350	600	Open hot stage sprayed with 2% FG	10-30 min bonding 0-30 min annealing	No bonding
In-situ reduced solgel nanocopper	Rapid Thermal Annealing	370	1	5 l/min 10% H2, FG	20 min	10.5

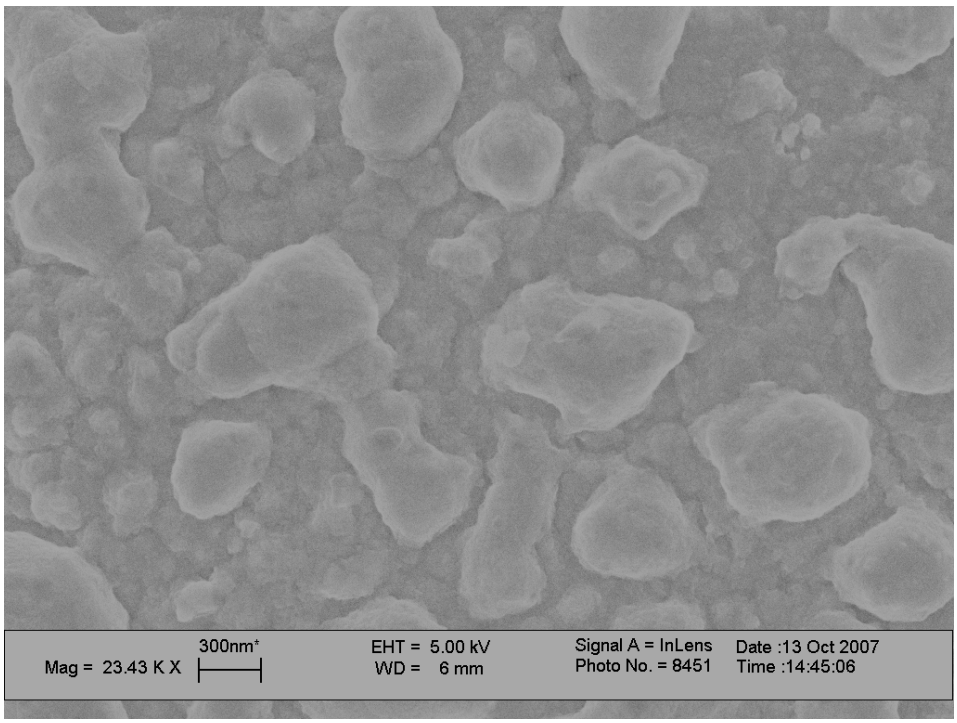

Figure 4.6 FESEM micrograph of copper nanoparticles on die pads after sheering

4.2 Silver Nanoparticles Using Solution Reduction

Silver nanoparticles are very attractive for their good mechanical, thermal and electrical properties. Good mechanical properties are useful to attain good mechanical reliability of the bond. High thermal diffusivity and conductivity of silver is very promising for thermal interface materials applications. They are also very attractive for thermal structure application in 3-D silicon SOP architecture. In addition, good electrical conductivity of silver makes it an attractive candidate for electrical interconnections. Copper to copper direct bonding using silver nanoparticle, hence, is valuable. The nanoparticles were synthesized using solution reduction technique. Synthesis involved reduction of $AgNO_3$ with $NaBH_4$, reducing agent. The particle size and shape were controlled using PVP, as dispersing agent. PVP forms Ag-PVP complex by sharing a lone pair electron with Ag^+ ion. This complex can easily be reduced by a reducing agent to form Ag particles. The large size of PVP causes a steric effect that forestalls grain growth and thus fine silver particles are synthesized. The final particle size and distribution depends largely on the relative amount of the PVP dispersant with respect to the $AgNO_3$. Therefore, an optimum amount of the molar ratio was used, that ensured nanometric size of silver particles (below 200 nm) and small size distribution. The formation of silver particles was confirmed using X-ray diffraction profile measured with Cu-K_α radiation (Figure 4.7). The Debye-Scherrer formula was used for a rough estimation of the mean particle dimension of the silver nanoparticles. Annealed silver particles were used as reference to eliminate the instrumental broadening. It should be noted that the Debye-Scherrer's formula is based on assumption of translational symmetry in the involved crystal structure and nanoparticles do not necessarily have translational symmetry [60]. Possibility of peak overlap can further make the method even less useful in estimating the nanometer size. However, this gives a rough estimation

of the mean size involved. The mean size so calculated was 40-50 nm. A more close estimation was done using FESEM. A FESEM micrograph of the silver nanoparticles, as synthesized, is shown in Figure 4.8. As evident, the average particle dimension is less than 150 nm. In addition, it can be noted that the particles are of uniform size and spherical in shape. Spherical particles ensure high density of the silver film and thus good quality as bonding interface. Also, the surface roughness remains minimal with spherical particles. The sintering behavior of the silver particles was studied using FESEM at two different sintering temperatures, namely 60 and 250^0C. As can be seen from Figure 4.9, the silver particles are very prone to sintering and particles starts coagulating even at a temperature as low as 60^0C. The particles starts coarsening in accordance with the Ostwald ripening and bigger particles grow at the expense of smaller particles. Initial sintering stage is characterized by the initial neck formation. The spherical particles get elongated in a specific direction to reduce overall surface energy. At 250^0C (Figure 4.10) the silver particles become dense with some visible indication of air pockets. Moreover, grains coarsen significantly and form closed metallurgical bonding with each other. The particle dimension at this temperature ranges from 50-100 nm. This suggests that a good metallurgical bonding can be achieved at very low bonding temperature. Thus, this can be elemental in reducing the thermal budget in copper to copper bonding process.

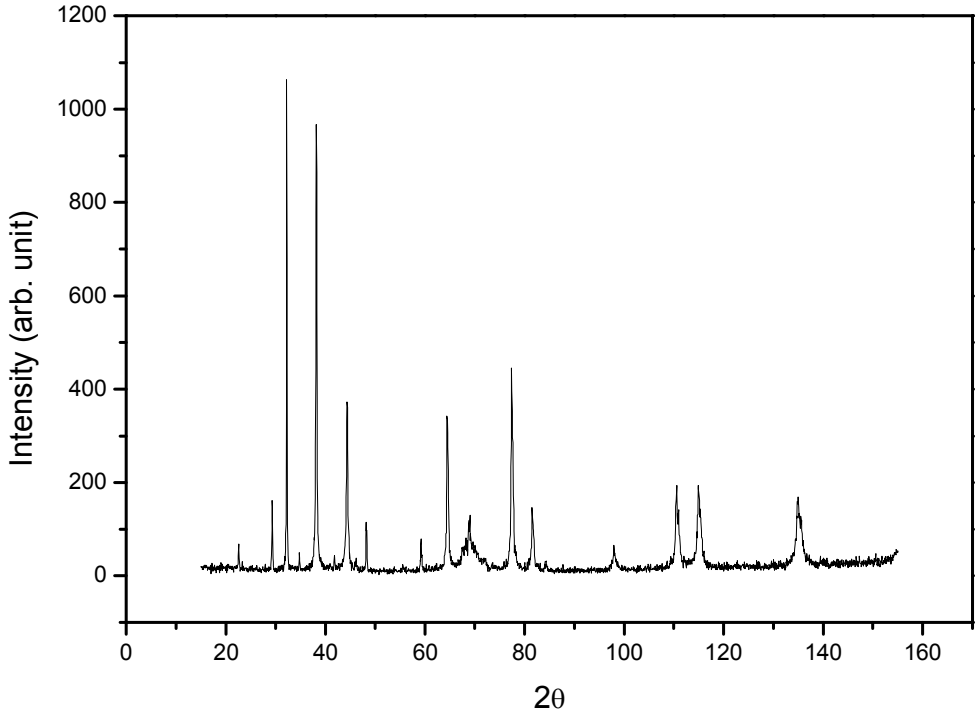

Figure 4.7 X-ray diffraction profiles of silver nanoparticles

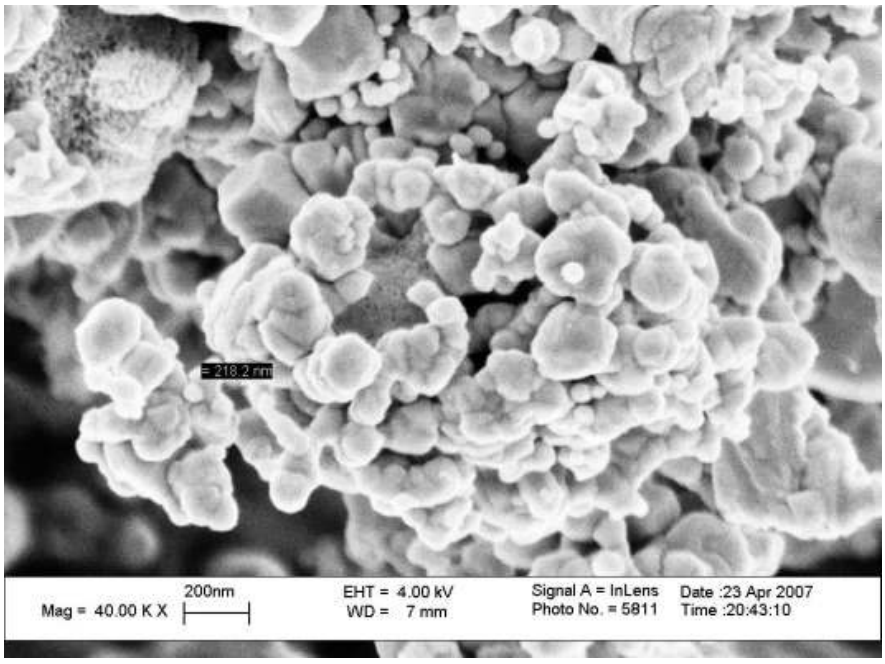

Figure 4.8 FESEM micrograph of silver nanoparticles as synthesized

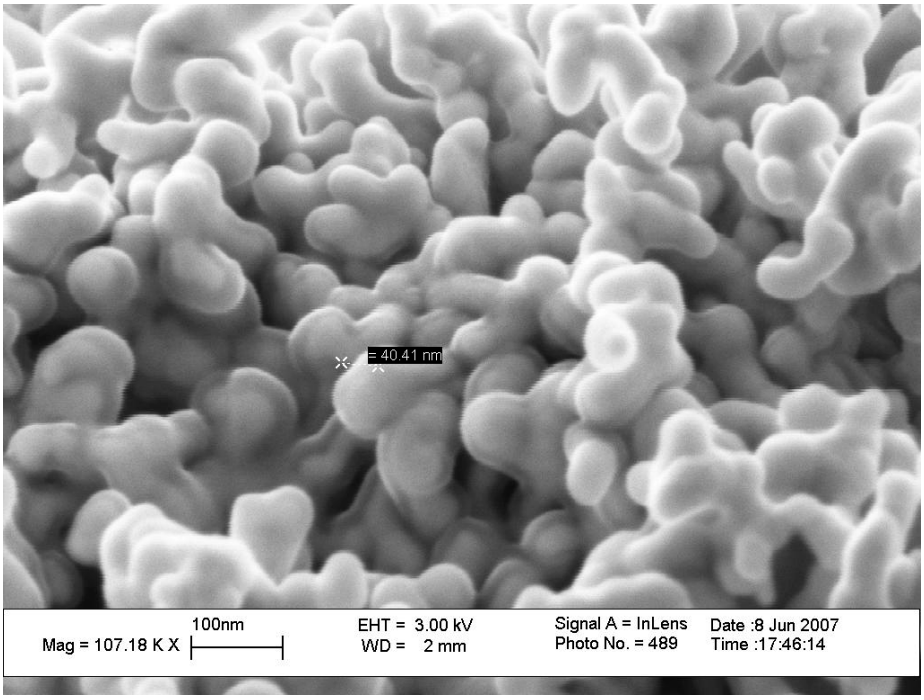

Figure 4.9 Field emission scanning electron micrograph of the silver nanoparticles sintered at 60 C

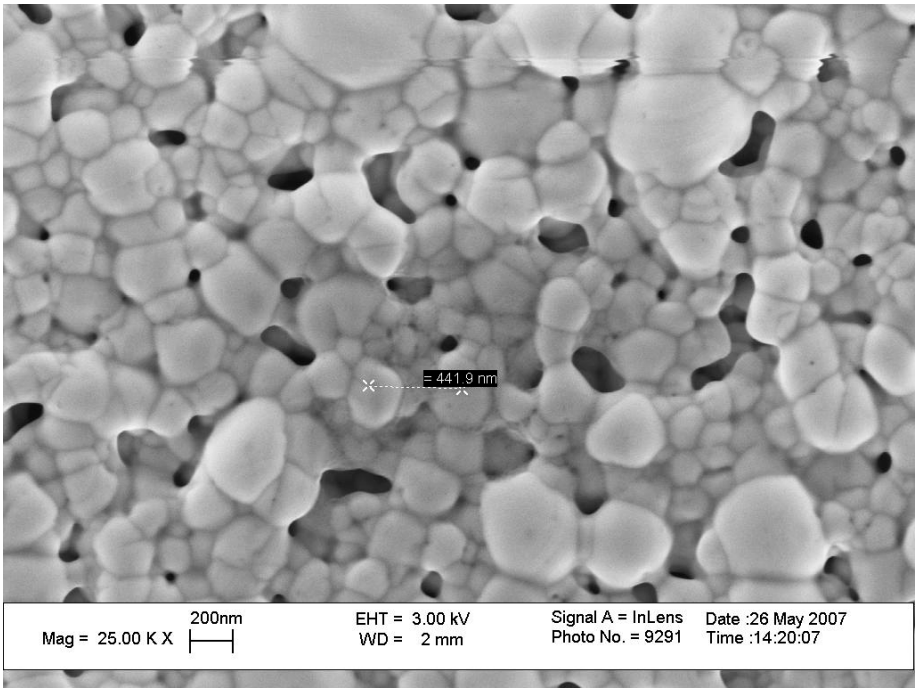

Figure 4.10 FESEM micrograph of the silver nanoparticles sintered at 250 C

The bonding using silver nanoparticle thin interface was performed using simultaneous heating and application of bonding force, the so called thermo-compression technique. Bonding at different environmental conditions was done including open atmosphere, nitrogen gas and forming gas atmosphere. A detailed description can be found in chapter 3, section 3.5.2. Figure 4.11 and Figure 4.12 show the bonding interfaces resulted due to bonding in open atmosphere and inert environment respectively. As evident, the nanoparticles allow achieving a bonding as thin as 2 micron. In addition, it can be noted that an inert atmosphere reduces the amount of voids present in the bonding interface. The presence of void decreases the strength of the bond. These are also deleterious to the electric and thermal properties of the interface. The bond strength was measured using destructive shear test, which is listed in the table …Interfacial shear strength as high as 1-2 MPa was noticed. It should be noted that the bonding strength depends on both the bonding temperature and force. Due to instrumental limitations, the bonding force applied was from 50-100 kPa in N_2 atmosphere and up to 5 MPa in open atmosphere. Low bonding pressure applied for bonding in N_2 atmosphere is not adequate to achieve very strong bond. However, it is expected to attain high bond strength by increasing the bond force applied during bonding. Similarly, bonding in open atmosphere has many limitations. Due to nanogranular particles, silver is very prone to oxidation and grain coarsening. Such unwanted phenomena reduce the bond strength. Since, the bonding involves diffusion of silver particles to from a homogenous solid solution a good bonding requires good contact between the mating surfaces to promote diffusion. However, evaporation and escape of organic solvent in the spin coated silver, used as bonding layer, at elevated temperature results in poor physical contact between the two mating surfaces. Thus, the resulting bond becomes weaker than that achieved in case of copper interface. Bonding under vacuum, however, facilitated better escape of

evaporated solvents and thus was able to furnish bond strength as high as 10 MPa. Thus, it is apparent from the results that the process parameters including bonding temperature, pressure and bonding environment can be optimally selected to achieve a good quality bond with very thin and mechanically reliable interface.

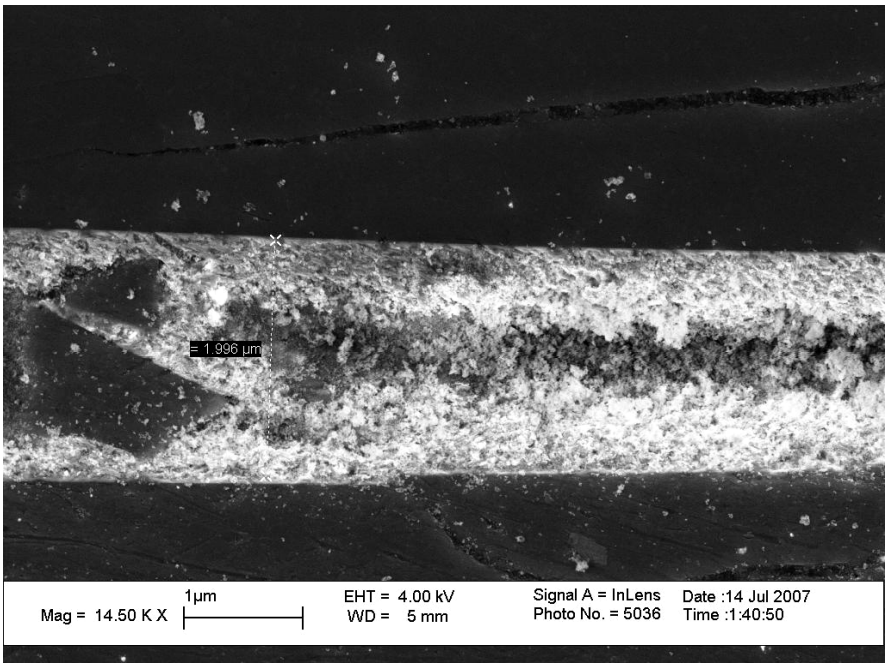

Figure 4.11 FESEM micrograph of the silver interface in N_2 atmosphere

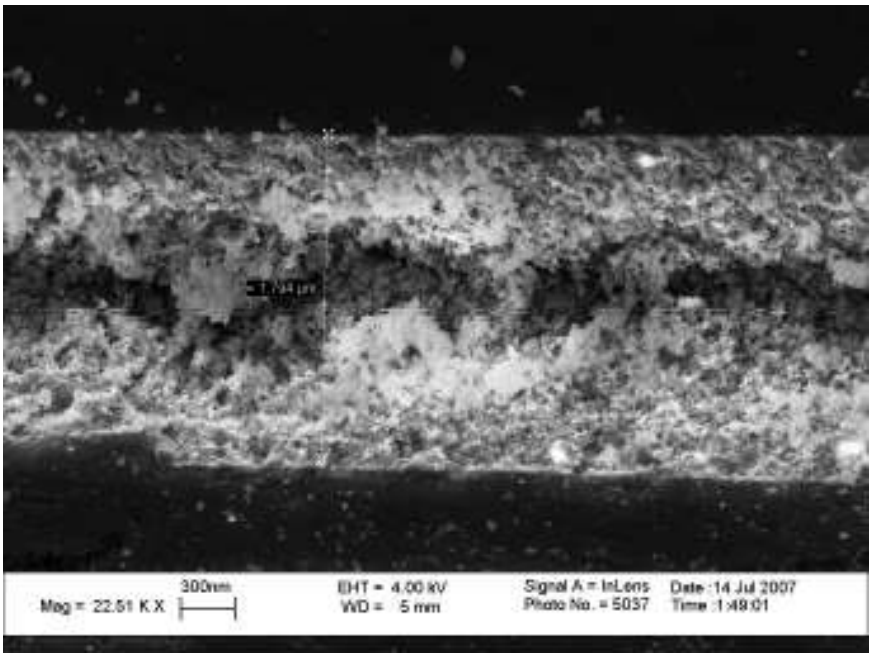

Figure 4.12 FESEM micrograph of the silver interface bonded in open atmosphere

Table 4.2 Shear strength of copper-to-copper bond using silver nanoparticle interface

Bonding Tool	Bonding Temp (C)	Bonding Pressure (MPa)	Environment	Time	Shear Strength (MPa)
Fineplacer Thermo Compress bonding	350	5	Open hot stage sprayed with 2% FG	30 min bonding 30 min annealing	No bonding
Rapid Thermal Annealing	370	1	5 l/min 10% H2, FG	6 min	1
Nitrogen furnace	370	1	Nitrogen	10 min	1.2

4.3 Thin Interface Bonding Using Gold Nanoparticles

Gold nanoparticles being less reactive than copper and silver nanoparticles are less prone to oxidation and grain coarsening at elevated temperature. Hence, Gold was selected to demonstrate bonding in open atmosphere. Gold nanoparticles were synthesized by wet chemical reduction of Gold (III) ion by hydroxylamine. The reduction was carried out in an aqueous solution. FESEM was used to study the morphological characteristics of Gold nanoparticles. As can be seen from Figure 4.13 the Gold particles have a tendency to aggregate. Several particles agglomerate and make big particle to reduce surface energy. However, application of surface capping agent prevented such agglomeration and thus, fine granular gold particles were produced. The FESEM micrograph of gold nanoparticles with capping agent has been shown in the Figure 4.14. The average particle dimension in presence of capping molecule is less than 200 nm. The capping

agent does not affect the bonding behavior to a significant extent as it forms few atomic layers on the particles, which can be evaporated by heating at a very low temperature.

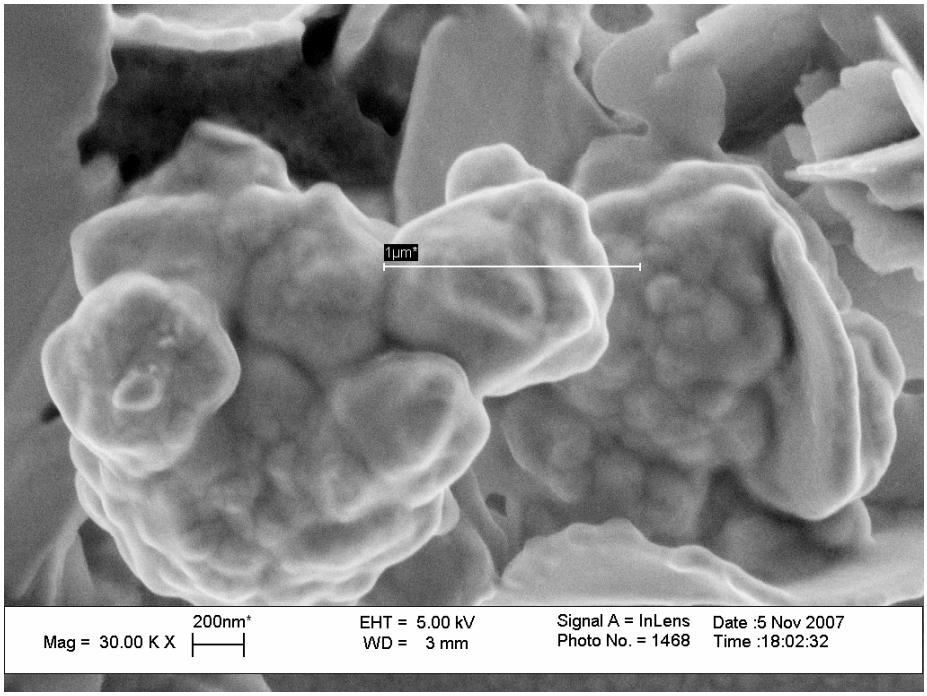

Figure 4.13 FESEM micrograph of gold nanoparticles

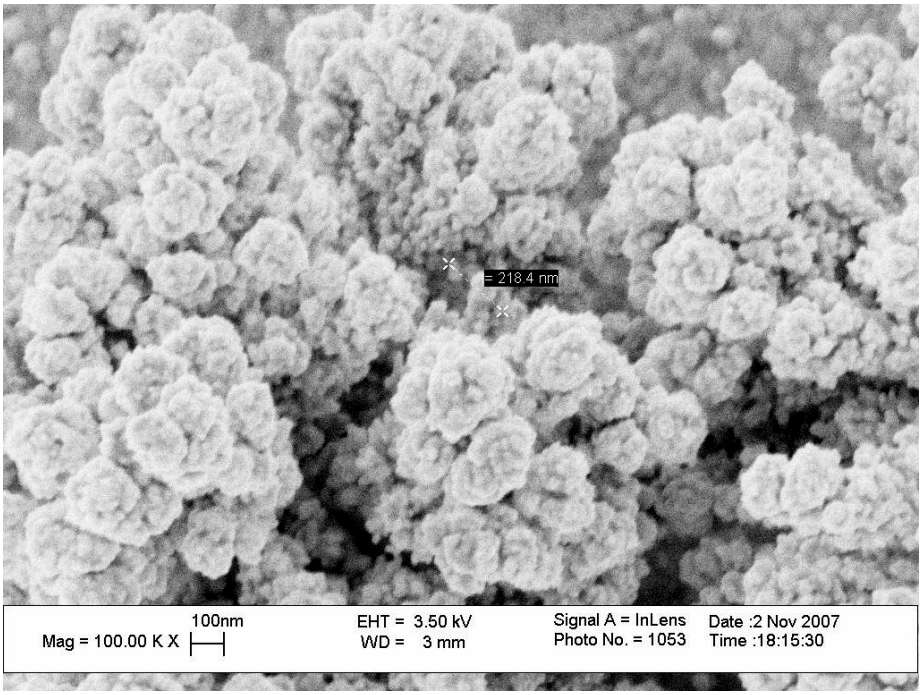

Figure 4.14 FESEM micrograph of encapsulated gold nanoparticles

4.3.1 Patterning of gold nanoparticles

Patterning of gold nanoparticles is necessary to be able to get technological advantages of the excellent thermal and electrical properties of gold. The gold nanoparticles suspension did not attach preferentially to copper pads or gold pads on mere spin coating, as was seen in case of copper precursor solution. Therefore, various alternatives were investigated.

Catalytic nucleation of gold nanoparticles on copper or gold pads was found to be most useful. This process included synthesis of gold particles on metal pads, which was catalyzed by copper or gold. Due to this gold was deposited on copper or gold only. However, no deposition was observed on polymer or SiO_2 surface. This is equivalent to selective electroless deposition but with nanoparticulate structure that is more reactive compared to typical thin films.

Figure 4.15 show gold patterning on copper surface using such catalytic deposition technique. As can be seen from the figure, gold deposits only on copper surface, while the polymer (and/or SiO_2) surface remains uncovered. Further, the optical micrograph reveals that the gold nucleates uniformly on all over copper surface resulting in uniform dense gold layer. A similar patterning on gold surface is shown in Figure 4.16. As evident, the gold particles can be nucleated preferentially on gold surface. Hence, a uniform and dense layer of gold thin film results on the gold interconnection while no deposition of gold particles is observed on the polymer surface used for passivation. Such catalytic deposition method provides a unique opportunity to control the thickness of the deposited layer. When the desired thickness is achieved, the deposition is stopped by removing the substrate from the chemical bath. As can be seen from the figure, this method is equally effective in carrying out patterning at very fine pitch

of 30 micron. This is thus very useful for fine pitch interconnection technology and thus attractive for SOP driven micro- miniaturization.

The morphological characteristics and size distribution of the gold nanoparticles as deposited on copper surface and gold surface were investigated using FESEM. Figure 4.17 shows such FESEM micrograph for copper surface catalytic deposition. Evidently, the gold nanoparticles are of uniform size. The quality of film deposited on copper surface seems to be better as compared to that on gold surface, as observed in the Figure 4.18 gold nucleation on gold surface does not cover total surface area and hence the resulting film is not as dense as seen on copper surface.

Bonding using gold nanoparticles was carried out in open atmosphere. As the gold particles are less reactive than silver and copper particle, it is relatively easy to get good bonding even in ambient atmosphere. Thermocompression bonding was used by applying simultaneous application of thermal and bonding force. The bonding temperature and pressure were maintained at 350^0C and 500 MPa. The bond strength was measured using die shear testing. Table 4.3 lists the bond strength of copper to copper bond with gold nanoparticles as interlayer. As evident, a bonding strength as high as 100-150 MPa was achieved. This bonding strength is higher than that achieved with copper or silver interface. This is due to that fact that gold is less reactive and thus does not form oxides at the bonding temperature. The bonding interface may be more denser and pore-free because grain coarsening is less in gold as compared to copper and silver nanoparticles. This was confirmed by heating the gold film, as grown on copper and gold surface by catalytic deposition, at 350^0 in ambient atmosphere. Figure 4.19 and Figure 4.20 show the FESEM micrograph of gold nanoparticles as grown on copper and gold surface, respectively.

Evidently,, the bonding temperature causes insignificant increase in the grain size. Therefore, it is safe to conclude that copper and silver can also be made to get better bonding in open atmosphere if the oxidation and grain coarsening can be prevented by some technique.

The bond interface was also studied using FESEM. The fracture surface on the die side and the substrate side, after destructive die shear testing, has been shown in the Figure 4.21 and Figure 4.22 respectively. As evident, bonding involves whole area of the copper bumps. The gold nanoparticles are observed to be very densely sintered. It can be seen that there is no continuous gold particle network in the surrounding area of the bump. The die side fracture bolsters the argument that there is very less increase in the grain size as a result of heating during bonding.

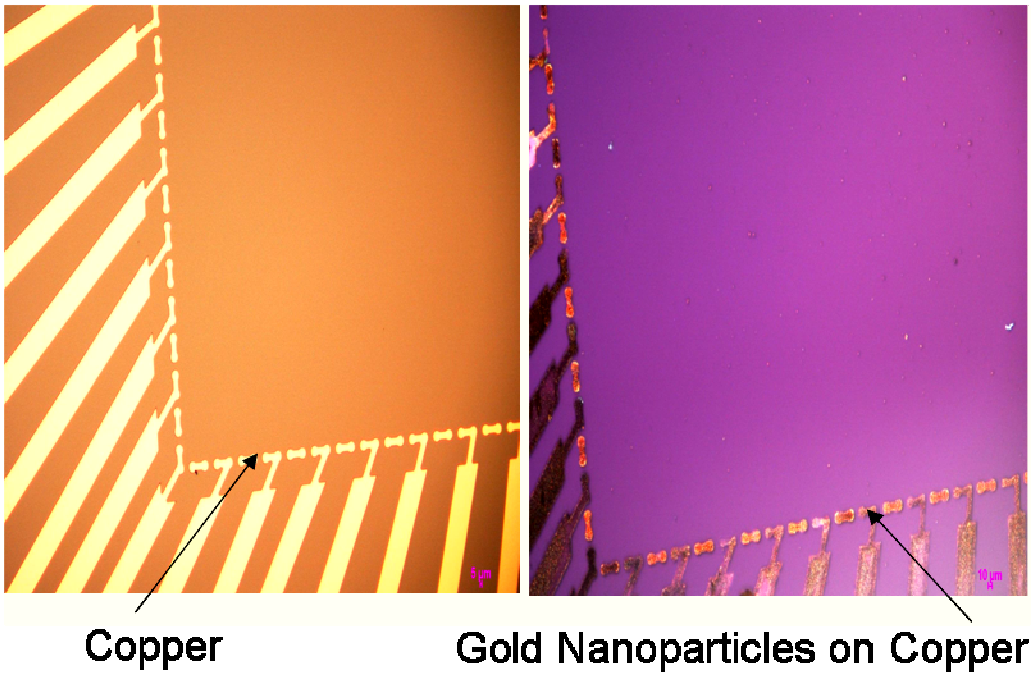

Figure 4.15 Optical micrograph showing selective wetting of gold nanoparticles on copper pad

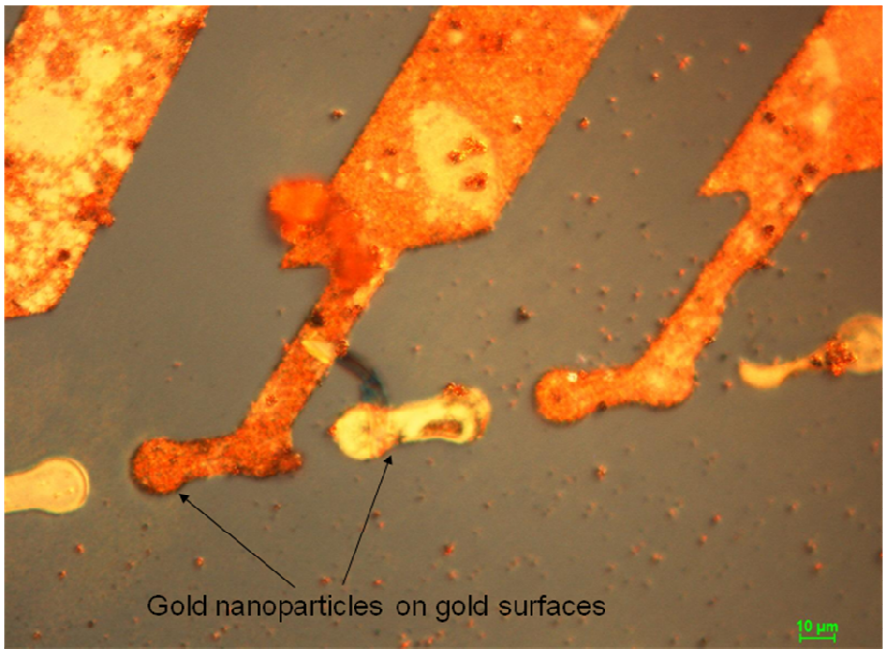

Figure 4.16 Optical micrograph showing selective wetting of gold nanoparticles on gold pad

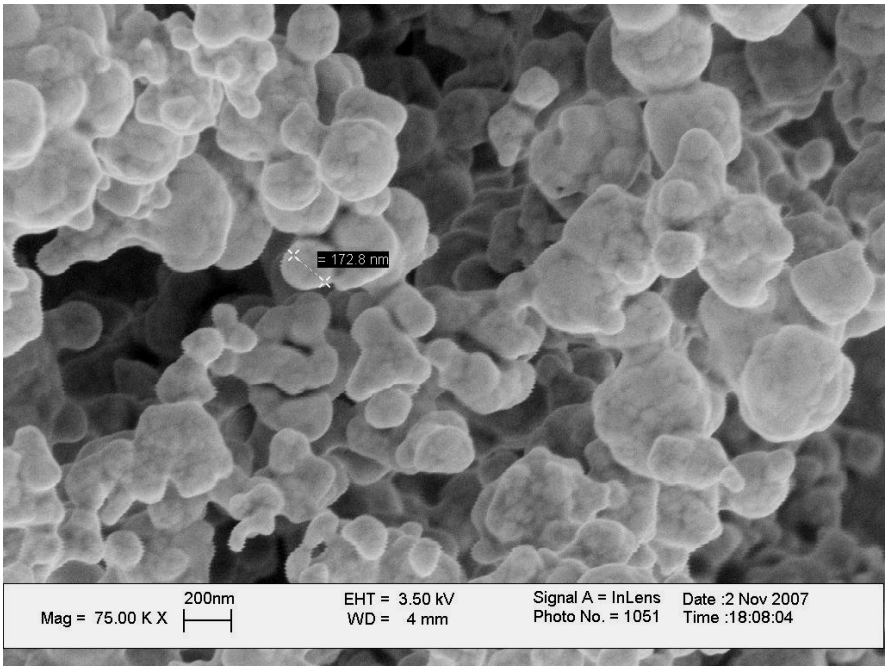

Figure 4.17 FESEM micrograph of selectively deposition gold nanoparticles on copper surface

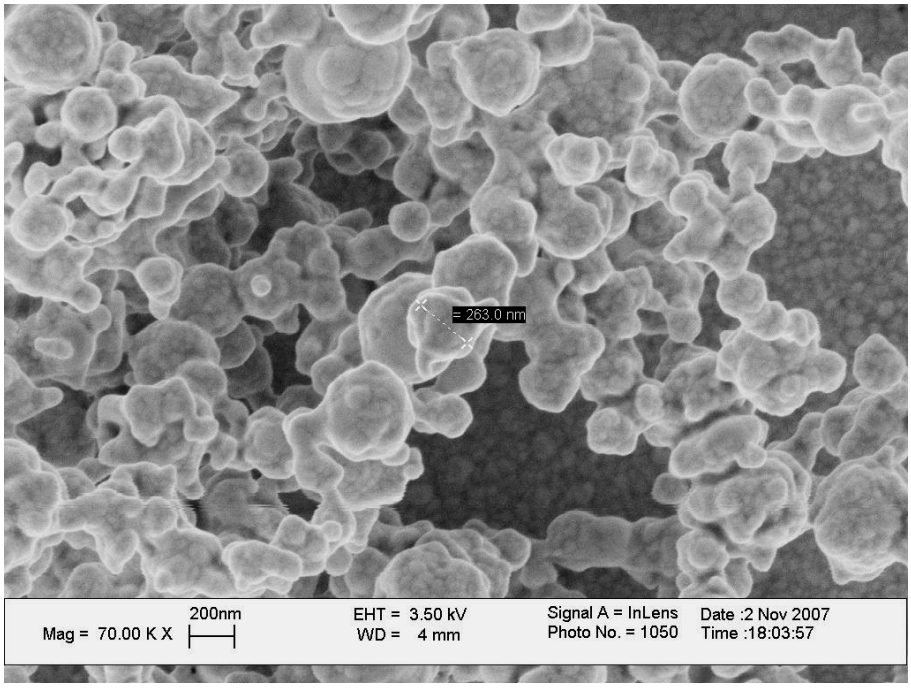

Figure 4.18 FESEM micrograph of selectively deposited gold nanoparticles on gold substrate

Table 4.3 Copper to copper bond strength with gold nanoparticles interlayer

Bonding layer	**Bonding tool**	**Bonding Temp (C)**	**Bonding Pressure (Mpa)**	**Environment**	**Time (min.)**	**Shear strength (Mpa)**
Gold Nanoparticle on gold surface	Fine Placer Thermocomp. Bonding	350	600	Open environment	5	10
Gold Nanoparticle on copper surface (with caping agent)	Fine Placer Thermocomp. Bonding	350	600	Open environment	5	10.2
Gold Nanoparticle on copper surface (catalytic deposition)	Fine Placer Thermocomp. Bonding	370	500	Open environment	6	100-150

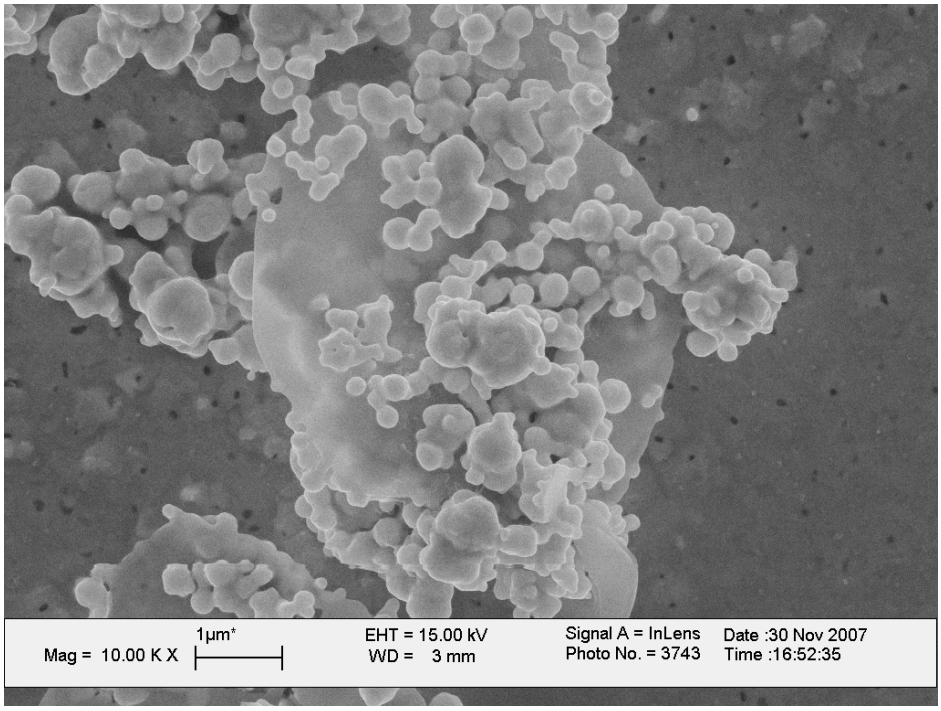

Figure 4.19 FESEM micrograph of Gold nanoparticles on copper surface after sintering at 350 C

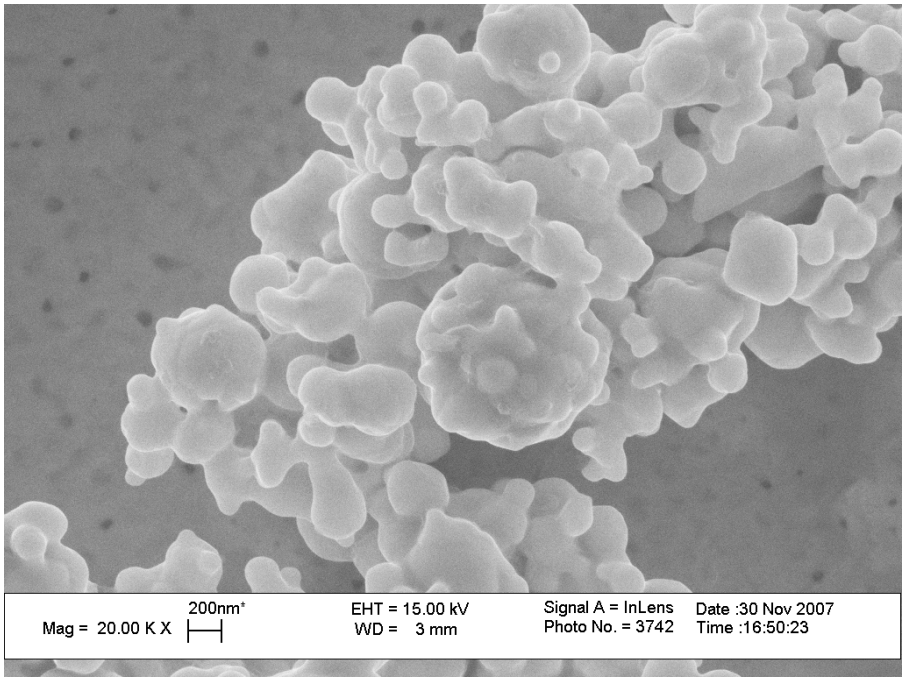

Figure 4.20 FESEM micrograph of Gold nanoparticles on gold surface after sintering at 350 C

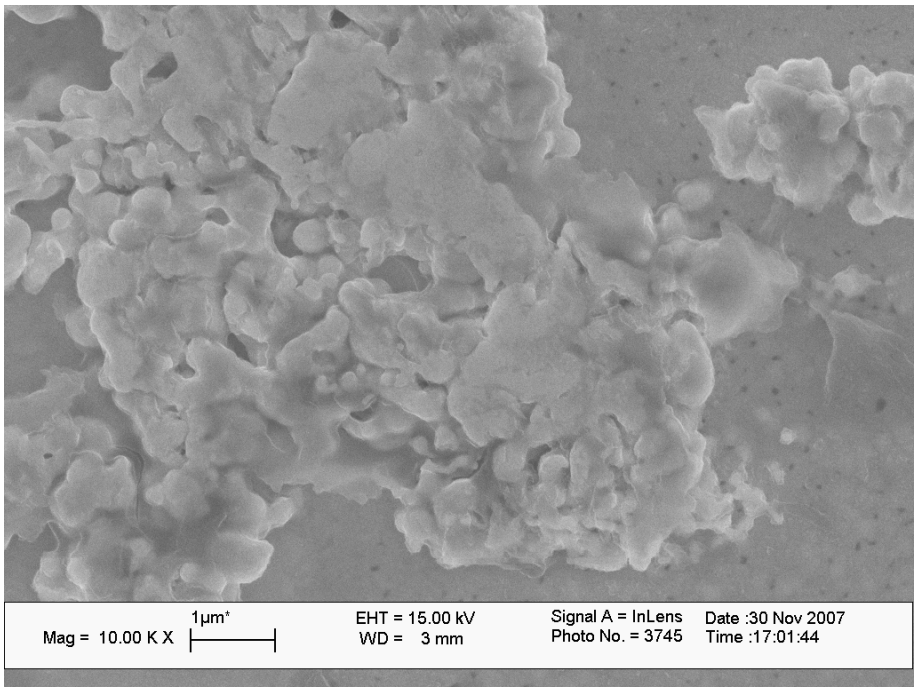

Figure 4.21 FESEM micrograph of the bond interface on the substrate side

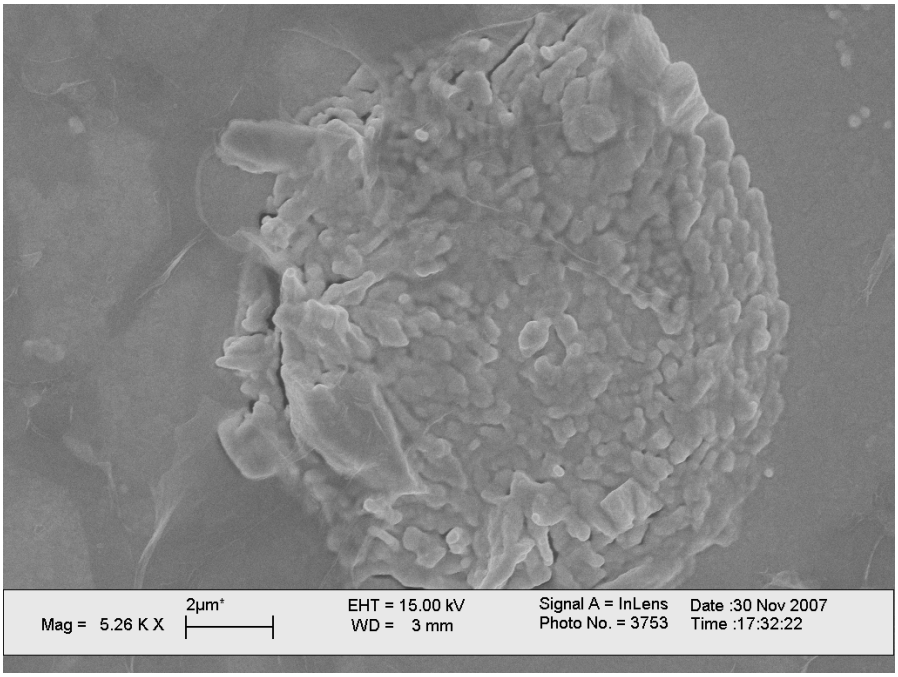

Figure 4.22 FESEM micrograph of the bond interface on the die side

5. CONCLUSIONS

Unceasing demands for better performance, higher functionality, portability and low cost has driven the Moore's law and System-On-Package technology. These technological advancements are plagued with several electrical and thermal challenges. Heterogeneous material and device integration for thermal structures and IC assembly is currently limited by reliable, low cost and high performance bonding technology. Industry is currently depending on low melting point indium and tin-based solders for thin film bonding of thermal structures and electrical interconnections. Solder based interconnections may no longer be adequate to meet the requirements of fine pitch technologies and 3D silicon architecture needs. On the other hand, thermal management of embedded devices, as often seen in SOP based systems, has become a significant issue. Therefore, there is a need to develop alternate technologies that can address the abovementioned issues. Novel thermal interfaces are needed to alleviate the daunting thermal challenges.

All copper based thermal structures and interconnections have been identified as a potential solution to address the limitations of solder interfaces. However, high melting temperature makes copper to copper bonding highly thermal intensive making it incompatible for 3D silicon or organic packaging. Recently, several works have been done to carry out bonding at 400^0C. However, the bonding duration and annealing time are still higher.

In the present work, novel nanoparticle based bonding approaches were explored and developed to reduce the thermal budget for thin film Cu-Cu bonding. In house synthesis of

various kind of metallic nanoparticles were done including gas phase reduction of sol-gel derived copper gel for copper nanoparticle, solution reduction for silver nanoparticle and wet chemical reduction for gold nanoparticle synthesis. Patterning technique for nanoparticles was also developed that enabled selective attachment of nanoparticles on the desired locations. Maskless patterning for copper based on selective wetting and for gold based on catalytic deposition was demonstrated at 30 micron and 200 micron pitch.

Bonding was performed in various atmospheric conditions. The thermocompression process variables were optimized. Presence of oxygen was found to detrimental for nanocopper and nanosilver based bonding interfaces. Due to oxidation and grain growth, no bonding was observed in ambient atmosphere for these material systems. However, an in situ reduction and bonding approach resulted in good bonding with copper nanoparticle interface. Silver interface yielded better bond due to less reactivity than copper. Bonding in various environmental conditions showed that good bonding was largely contingent on vacuum conditions during bonding. Gold interface due to its least reactivity among the three resulted in the best bonds. The bond strength in ambient atmosphere was measured to be as high as 100-150 MPa. The bond interface study revealed ductile fracture mode. The nanoparticles on the fracture surface were found to be sheared in the direction of shearing force. This process is then extended to a 30 micron pitch process test vehicle to demonstrate fine pitch patterning and bonding. These nanoparticle derived thin film bonding techniques can provide best electrical and thermal performance, with low cost and simple processing.

6. FUTURE RECOMMENDATIONS

This work evaluated the possibility of nanoparticle based copper to copper bonding to reduce the thermal budget. There is a need for several other studies to have a better understanding of the nanoparticle-induced bonding. Some of the recommendations for future work are as follows.

6.1 Void Characterization

Interfacial voids are detrimental for thermal and electrical applications. Voids increase the thermal impedance and thus, are less attractive for thermal transport. In addition, they increase the contact electrical resistance. Moreover, they are deleterious to the mechanical property and makes he bond less reliable. Therefore, C mode scanning acoustic microscopy (C-SAM) study of the bond interface might help understanding the bond quality even in greater detail. However, C-SAM resolution may limit the analysis. A combination of electron microscopy and C-SAM may be more effective.

6.2 Electrical characterization

A complete electrical characterization with load and temperature is required to demonstrate the reliability of this bonding technology.

6.3 Thermal characterization

Thermal characterization with measurement of thermal diffusivity, interfacial thermal resistance and effective thermal conductivity is an important next step. FEM based thermomechanical analysis might also provide good insight to design and develop the bonding process more effectively. Role of grain boundaries, interfaces and porosity in the reliability and thermal performance has to be accurately characterized.

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