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High Ge content p-channel SiGe MOSFETs on Virtual Substrate

by

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Declarations

This thesis is the result of research carried out by the author in the Department of Physics, The University of Warwick, UK between February 2001 and February 2004 and is submitted as partial fulfilment of the requirements for the award of the degree of Doctor of Philosophy in Physics. The work described here is all my own, except where acknowledged as otherwise in the text. The main results of the performed work during this research has been published in scientific journals and presented at the international scientific conferences.

Publications in journals during this research

1. S. Durov, O.A. Mironov, M. Myronov, T.E. Whall, E.H.C. Parker, T. Hackbarth, G. Höck, H.-J. Herzog, U. König, H. von Känel, "*DC and low-frequency noise analysis for buried SiGe channel metamorphic p-MOSFETs with high Ge content*", (Journal of Telecommunications and Information Technology, Warsaw, Poland, in-press, 8 pages), (Proceedings of 6^{th} Symposium Diagnostics &Yield: Advanced Silicon Devices Technologies for ULSI Era, Warsaw, Poland, 2003).

2. M. Myronov, O.A. Mironov, S. Durov, T. Hackbarth, G. Höck, H.-J. Herzog, U. König, T.E. Whall and E.H.C. Parker, "*Reduced 1/f noise in p-$Si_{0.3}Ge_{0.7}$ metamorphic hetero-MOSFETs*", Applied Physics Letters, 2004, v. 84, i. 4, pp. 610-612

3. M. Myronov, S. Durov, O.A. Mironov, E.H.C. Parker, T.E. Whall, T. Hackbarth, G. Höck, H.-J. Herzog, U. König, "*Low-frequency noise suppression and DC characteristics enhancement in sub-μm metamorphic p-MOSFETs with strained $Si_{0.3}Ge_{0.7}$ channel grown by MBE*", Applied Surface Science, **XXX** (2003) XXX-XXX, (ISTDM-2003 Proceedings, Nagoya, Japan, 2003, in-press, 5 pages)

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1. O.A. Mironov, M. Myronov, S. Durov, D.R. Leadley, T. Hackbarth, G. Höck, H.-J. Herzog, U. König, H. von Känel, E.H.C. Parker and T.E. Whall, "*p-$Si_{0.3}Ge_{0.7}$ and p-$Si_{0.2}Ge_{0.8}$ MOSFETs of enhanced performance*", Proceedings of ESSDERC-2003, Estoril, Portugal, 2003 (submitted, 4 pages).

2. M. Myronov, S. Durov, O.A. Mironov, D.R. Leadley, T. Hackbarth, G. Hock, H.-J. Herzog, U. Konig, E.H.C. Parker and T.E. Whall, "*Reduced 1/f noise at 293K in 0.55mm p-$Si_{0.3}Ge_{0.7}$ hetero-MOSFETs*", Proceedings of ESSDERC-2003, Estoril, Portugal, 2003 (submitted, 4 pages).

3. M. Myronov, S. Durov, O.A. Mironov, E.H.C. Parker, T.E. Whall, T. Hackbarth, G. Höck, H.-J. Herzog, U. König, H. von Känel, "*Low-frequency noise analysis for buried SiGe channel metamorphic p-MOSFETs with high Ge content*", Proceedings of 17^{th} International Conference on Noise and Fluctuations (ICNF-17), Prague, Czech Republic, 2003, published by CNRL s.r.o., Brno, Czech Republic, 2003, pp. 343-346.

4. S. Durov, O.A. Mironov, *"Optimised preamplifier for LF-noise MOSFET characterization"*, NATO ARW "Advanced Experimental Methods for Noise Research in Nanoscale Electronic Devices", Brno, Czech Republic, 2003, proceedings (submitted 7 pages).

5. S. Durov, O.A. Mironov, M. Myronov, T.E. Whall, V.T. Igumenov, V.M. Konstantinov and V.V. Paramonov, *"Hooge mobility fluctuations in n-InSb magnetoresistors as a reference for access resistance LF-noise measurements of SiGe metamorphic HMOS FETS"*, NATO ARW "Advanced Experimental Methods for Noise Research in Nanoscale Electronic Devices", Brno, Czech Republic, 2003, proceedings (submitted 8 pages).

Abstract

This thesis demonstrates the advantages and disadvantages of investigated p-type SiGe MOSFETs with high Ge content $Si_{1-x}Ge_x$ p-channel grown on $Si_{1-y}Ge_y$ virtual substrate (VS) ($x = 0.7-0.9$, $y = 0.3-0.5$) in comparison with conventional Si devices. The ways to overcome current difficulties in conventional Si technology and mixed SiGe-Si technology are shown.

Current-voltage (I-V) and capacitance-voltage (C-V) DC characteristics for p-channel $Si/Si_{1-x}Ge_x/Si_{1-y}Ge_y$ hetero-MOSFETs with high Ge content ($x = 0.7-0.9$, $y = 0.3-0.5$) are reported. Enhancement in the maximum drain current for the p-SiGe devices in comparison with p-Si control is 2.5-3.0 times. DC characteristic simulations of SiGe p-channel MOSFETs were used to improve the accuracy of MOSFET and heterostructure parameters extraction. Calibrated during the simulation theoretical models were used for future design. The effective mobility, the source-drain access resistance, the doping profile, the layers thickness, oxide/semiconductor interface charge and other important characteristics were extracted.

The effective mobility values, extracted for p-$Si_{0.3}Ge_{0.7}$ MOSFETs, exceed the hole mobility in a conventional Si p-MOS device by a factor of 3.5 and reach the mobility of conventional Si n-MOS transistors. The peak value of μ_{eff} = 760 $cm^2V^{-1}s^{-1}$ at field 0.08 $MVcm^{-1}$ was obtained for p-$Si/Si_{0.2}Ge_{0.8}$/ $Si_{0.5}Ge_{0.5}$ MOSFETs.

Efficiency of special *n*-type doped layer, also known as "punch-through" stopper, introduced into heterostructure is shown. Perfect I-V and also low frequency noise characteristics of investigated MOSFET show that the p-type $Si/Si_{1-x}Ge_x/Si_{1-y}Ge_y$ ($x = 0.7-0.9$, $x-y = 0.3-0.4$) heterostructures with "punch-through" stopper could be very impressive opportunity to conventional Si for modern semiconductor industry.

For the first time, quantitative explanation of the low frequency noise reduction in metamorphic, high Ge content, SiGe p-MOSFETs compared to Si p-MOSFETs have been proposed. Quantitative analysis demonstrates the importance of both carrier number fluctuations and correlated mobility fluctuations (CMF) components to the $1/f$ noise of surface channel Si p-MOSFET, but the absence of CMF for buried channel p-$Si_{0.3}Ge_{0.7}$ and p- $Si_{0.2}Ge_{0.8}$ MOSFETs. The low frequency noise was measured to be three times smaller for a 0.55 μm effective gate length p-$Si_{0.3}Ge_{0.7}$ MOSFET than the Si control, at linear regime (V_{DS} = -50 mV) and high gate overdrive voltage (V_{gt}= -1.5 V). This result is very important, because we have reduction in LF noise at high gate overdrive voltages, which are typical for analogue and power electronics application.

Both DC and low frequency noise characteristics show that access source and drain resistance for metamorphic p-SiGe MOSFETs ($R_S + R_D \approx$1.5-2.0k$\Omega \times \mu$m) roughly 2 times lower then for conventional p-Si MOSFETs.

Chapter 1

Introduction

The main requirements of modern electronic industry for transistors and other active elements are high speed, small size, low power consumption, low supply voltage, short full fabrication time, and low cost [1, 2]. Other important requirements are high linearity and small inter-modulation coefficient for amplifiers, fast switching time for digital application and power devices, and low internal noise for amplifiers, oscillators and power devices. Silicon have got widest prevalence as main material for transistors fabrication due to lowest cost among other semiconductors and simple fabrication technology. For the past three decades, the silicon IC industry has sustained astonishing growth and development. The size of the Metal-Oxide-Semiconductor (MOS) transistor has been continually reduced by a factor of two every two years, which has resulted in chips which are significantly faster, contain more transistors, and consume less power per transistor in every generation. The silicon-based transistor and its continued scaling have brought information technology to its current mature status. Transistor scaling, in turn, has been made possible by the improved lithographic capability to print shorter gate lengths and the ability to grow nearly perfect insulators with ever decreasing thicknesses.

However, conventional scaling based on the reduction of feature sizes obviously cannot continue forever. Short channel effects, and the punch-through effect in small devices, impose a limitation on the minimum size. Significantly increased electrical noise and power dissipation degrade device electrical characteristics whith size decreased. Minimum available size, as well as low carrier mobility, are the major factors that limit device speed. The latter is especially important in Si p-type MOSFETs, since the maximum hole mobility

($\mu_p = 450$ cm^{2}V^{-1}s^{-1}) in Si is more than three times less than the maximum electron mobility ($\mu_e = 1500$ cm^{2}V^{-1}s^{-1}) [3, 4, 5].

The punch-through effect can be reduced with help of increased vertical electric field in MOSFETs. It can be realized by decreasing the oxide thickness or increasing the oxide permittivity and using a heavily doped area under the channel, also known as a punch-through stopper. However, the reduction in oxide thickness is limited by the direct tunneling distance (about 1.5-2nm) [6]. Doping of the punch-through stopper layer is limited to an impurity concentration of $\sim 10^{19}$cm^{-3} by technology. Effective oxide thickness could be decreased, if alternative high-κ dielectrics are used [7, 8, 9]. However addition of high-k dielectrics usually decreases the carrier mobility due to the oxide-semiconductor interface quality degradation [150, 11]. Vertical electric field also introduces additional electric noise to MOSFET due to scattering on dielectric-to-semiconductor interface.

Special device designs such as "silicon on insulator" (SOI) or "silicon on nothing" also can help to reduce short channel effects. SOI is already used in silicon technology [12], however it leaves the problems of speed limitation and increased electrical noise unsolved.

Heterostructures with other semiconducting materials can be used in order to increase the sheet density and carrier mobility in the device operating regime. However, this method is limited in the choice of materials compatible with silicon technology [2, 5].

Such materials as InAs ($\mu_e = 33000$ cm^{2}V^{-1}s^{-1}), GaAs ($\mu_e = 8500$ cm^{2}V^{-1}s^{-1}), InSb ($\mu_e = 77000$ cm^{2}V^{-1}s^{-1}), PbTe ($\mu_e = 6000$ cm^{2}V^{-1}s^{-1}), Ge ($\mu_e = 3900$ cm^{2}V^{-1}s^{-1}) have electron mobilities greater than in Si. Hole mobility of some of them, namely InSb ($\mu_p = 1250$ cm^{2}V^{-1}s^{-1}), PbTe ($\mu_p = 4000$ cm^{2}V^{-1}s^{-1}), Ge ($\mu_p = 1900$ cm^{2}V^{-1}s^{-1}), GaSb ($\mu_p = 850$ cm^{2}V^{-1}s^{-1}) are also greater than in Si [13]. However, only Ge and SiGe alloys are compatible with Si technology without full modification of the fabrication process. This is the major driving force behind the SiGe electronics.

The first step to improve the MOSFET characteristics is to use a thin SiGe layer in the MOSFET structure. Devices obtained this way are called pseudomorphic MOSFETs. Due to the mismatch in Si and Ge lattice constants, a SiGe layer grown on a Si substrate without dislocations is extremely strained. On the one hand, strain increases the hole mobility in the alloy, however on the other, the SiGe layer thickness and the maximum Ge content in

the alloy are limited by this strain [5]. The maximum Ge content in an alloy pseudomorphically grown on a Si substrate, and suitable for device fabrication, is 40-50%, and the corresponding valence band offset is 300-370 meV. The maximum mobility for these materials is $\mu_p = (1.5-2) \times \mu_p(Si)$ $\mathrm{cm^2V^{-1}s^{-1}}$ [14]. Unfortunately, the oxide-semiconductor interface quality decreases abruptly with increasing Ge content in the SiGe material, and there is a need to use a Si cap layer between the oxide and SiGe alloy layer to maintain high quality the channel. Another problem is the high diffusion coefficient of Ge atoms at high temperatures, thus the fabrication process of these devices requires a lower thermal budget than in the pure Si technology. The best reported effective hole mobility obtained for pseudomorphic p-MOSFETs is 300-500 $\mathrm{cm^2V^{-1}s^{-1}}$ [15].

The next step to improve MOSFET characteristics and to obtain high hole and electron mobility in SiGe hetero-MOSFET's (HMOSFET) is to use an alloy with a high Ge content grown on a relaxed SiGe virtual substrate (VS) with a relatively low Ge content. It allows the carrier mobility in the channel to increase, whilst keeping the same valence band offset and difference in Ge concentration in the channel and virtual substrate. The main advantage of devices fabricated using this method are the high effective hole mobility, low channel resistance and low thermal noise. The main problem is a very low thermal budget for devices with high Ge concentration due to fast diffusion of Ge and other impurities in the SiGe alloy. Another specific problem is current leakage through the virtual substrate due to a large number of defects in this relaxed SiGe buffer. Other shortcomings are the same as present in normal Si MOSFET's and SiGe pseudomorphic MOSFET's.

This thesis deals with experimental studies of metamorphic SiGe p-HMOSFETS properties using electrical characterization. Aspects of the device size minimisation and solution numerous problems, which occur when smaller devices are fabricated, are thoroughly described. Particular attention is paid to low frequency noise in MOSFETs as one of the main performance-limiting factor for small size devices.

Chapter 2 presents general theory related to device characterisation, device parameters extraction and general theory of electrical noise generation in MOSFETs. Special attention is paid to application and modification of general theory for SiGe technology. Previous and current investigations in described areas also will be discussed.

Chapter 3 describes investigated samples and experimental techniques, wich used in cur-

rent research. Own developed preamplifier for low frequency noise measurements in wide range of device conductance are presented.

Chapter 4 focused on description and analysis of experimental results. Advantages and disadvantages of investigated devices in comparison with Si p-MOSFETs fabricated with help of conventional CMOS technology are shown. Possible problems during continued CMOS scaling will be discussed.

Chapter 5 proposes the next generation of SiGe p-MOS device design, based on results obtained in **chapter 4**. Possible solutions of current problems are proposed. Really available today or perspective nearly productions ready technologies are discussed in order to apply to proposed device fabrication.

Finally, in **chapter 6**, I draw conclusions and make suggestions for future work.

Chapter 2

Theoretical background and literature review

2.1 Electronic structure and physical properties of strained Si, SiGe heterostructures

2.1.1 Lattice constant and strain

There is a 4.2% difference in the lattice constants of Si (a_{Si} = 5.431Å) and Ge (a_{Ge} = 5.657Å) [5, 3]. The lattice constant of relaxed $Si_{1-x}Ge_x$ alloy lie between the lattice constants of Si and Ge and its value well described by expression $a_{SiGe}(x) = (1-x) \times a_{Si} + x \times a_{Ge}$. Therefore when a layer of $Si_{1-x}Ge_x$ is grown on top of Si, it has a bulk relaxed lattice constant which is larger than Si. If layers are grown below the critical thickness (Fig. 2.1), then they become strained with the lattice symmetry changing from cubic to tetragonal and its lattice constant is a_{Si}.

Above the critical thickness, it costs too much energy to strain additional layers of material into coherence with the substrate. Instead defects appear, this case misfit dislocations, which act to relieve the strain in the epitaxial film. The epitaxial layer relaxes with defect density depend on difference in the lattice constants. The high defect density significantly reduces the hole and electron mobility and also increases parasitic conductivity along misfit dislocations. Thick ($\sim$ 1 μm) layer of $Si_{1-y}Ge_y$, grown on Si substrate with varied step by step or linearly Ge content y from zero to maximum value, has reduced density of

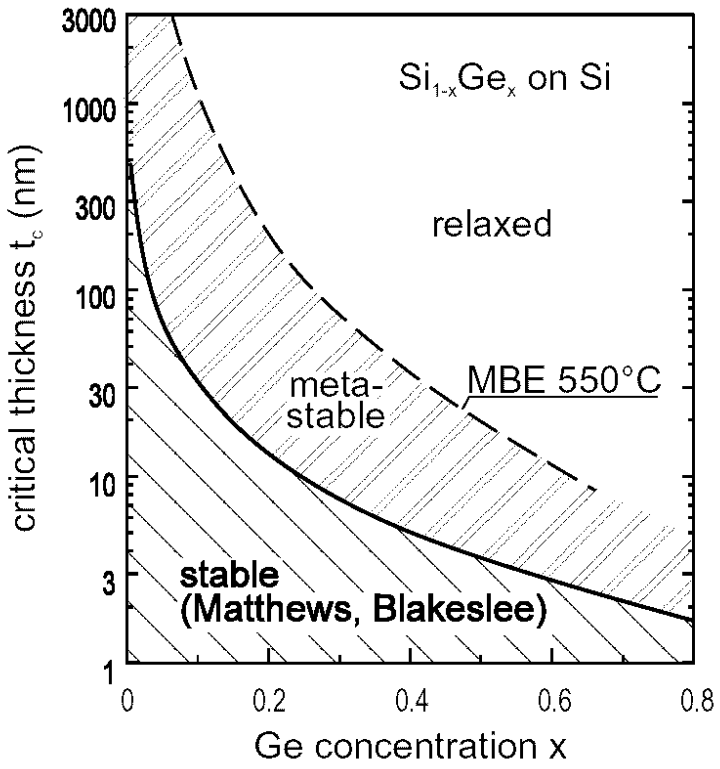

Figure 2.1: Critical thickness against composition for $Si_{1-x}Ge_x$ on Si. The lowest curve gives the theoretical limit in thermal equilibrium, whereas the experimental curve is for a metastable layer grown at 550 C by MBE.

dislocations lattice constant on top of them close to bulk $Si_{1-y}Ge_y$ lattice constant. Such layer is named Virtual Substrate (VS). The $Si_{1-y}Ge_y$ layer with fixed y value grown on top of VS can be relaxed with very low defect density.

The strain of strained layer dependence on lattice constant mismatch can be written as [16, 17]:

$$\varepsilon_{\parallel} = \frac{a_1}{a_2} - 1 \tag{2.1}$$

$$\varepsilon_{\perp} = -D\left(\frac{a_1}{a_2} - 1\right) \tag{2.2}$$

Here, the biaxial strain $\varepsilon_{\parallel}$ parallel to the plain of the interface and the unaxial strain $\varepsilon_{\perp}$ perpendicular to it. a_1 is the lattice constant of the VS ($a_1 = a_{SiGe}(y)$) for metamorphic or substrate ($a_1 = a_{Si}$) for pseudomorphic, a_2 is the equilibrium lattice constant of strained layer ($a_2 = a_{SiGe}(x)$). Constant D is dependent on the elastic constants c_{ij} of the layer material and on the interface orientation:

$$D^{100} = 2\frac{c_{12}}{c_{11}} \tag{2.3}$$

$$D^{111} = 2\frac{c_{11}+2c_{12}-2c_{44}}{c_{11}+2c_{12}+4c_{44}} \tag{2.4}$$

Here c_{11} is $(1.564-1.6564)\times10^{11}$ Nm^{-2},and c_{12} is $(0.6037-0.6394)\times10^{11}$ Nm^{-2} and c_{44} is $(0.7955-0.7951)\times10^{11}$ Nm^{-2} for Si [3, 18]. Si wafers with (001) orientation are mostly used for CMOS technology. So, $D = D_{Si}^{100}$ = 0.7720 can be used in most cases.

2.1.2 Band gap and band offsets

Indirect bandgap at 300 K (4.2 K) of bulk Si is 1.11 (1.17) eV, bandgap of bulk Ge is 0.66 (0.74) eV. The indirect bandgap of bulk $Si_{1-x}Ge_x$ alloys decreases monotonically from 1.11 (1.17) to 0.66 (0.74) eV as the Ge content increases from x=0 to x=1. The band gap of $Si_{1-x}Ge_x$ alloys as function of Ge content is shown in Fig. 2.2 [5]. Bandgap of $Si_{1-x}Ge_x$ decreased faster from x = 0.85, which show a crossover from the Si-like (conduction band minima at Δ point) to the Ge-like bandstructure (conduction band minima at the L point). The Si, Ge and SiGe alloys also have temperature and doping-induced light variations in the band gap. The Si/$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ heterostructures have additional variations in the bandgap due to mechanical stress and strain in silicon and silicon-germanium regions. Moreover, additional band offsets in the valence and conduction bands are introduced in Si/$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ heterostructures due to these variations.

Under Boltzmann statistics, the changes in the conduction and valence band edges are as follows:

$$E_C = -k_bT \cdot \ln\left(\sum_{i=1}^{3}\frac{1}{3}\exp\left(-\frac{\Delta E_{C_i}}{k_bT}\right)\right) \tag{2.5}$$

$$E_V = -k_bT \cdot \ln\left(\frac{x_0}{1+x_0}\exp\left(-\frac{\Delta E_{V_l}}{k_bT}\right)+\frac{1}{1+x_0}\exp\left(-\frac{\Delta E_{V_h}}{k_bT}\right)\right) \tag{2.6}$$

where ΔE_{C_i} is the shift of the band edge of the i^{th} ellipsoidal conduction minima,

ΔE_{V_l} and ΔE_{V_h} are the shifts of the band edges for the light and heavy hole maximum respectively, that make up the valence band, and x_0 is given by $x_0 = \left(\frac{m^*_{lh}}{m^*_{hh}}\right)^{3/2}$.

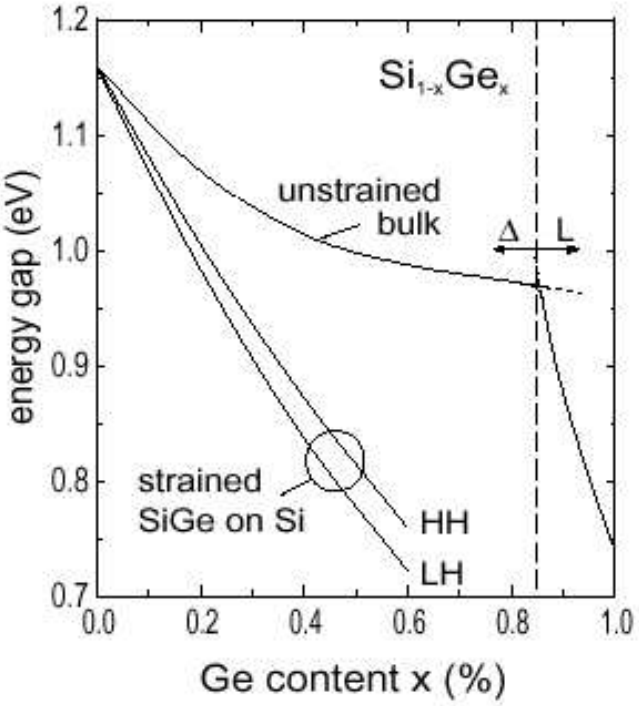

Figure 2.2: Band gap variation of $Si_{1-x}Ge_x$ alloys against Ge content x.

The band edge shifts can be computed using the deformation potential theory by Bir and Pikus [19]:

$$\Delta E_{C_i} = (\delta_1 (\varepsilon_{11} + \varepsilon_{22} + \varepsilon_{33}) + \delta_2 \varepsilon_{ii}) \tag{2.7}$$

$$\Delta E_{V_{(l,h)}} = \begin{pmatrix} \delta_3 (\varepsilon_{11} + \varepsilon_{22} + \varepsilon_{33}) \\ \pm \sqrt{\begin{array}{l} \frac{1}{2}\delta_4^2 \left((\varepsilon_{11} - \varepsilon_{22})^2 + (\varepsilon_{22} - \varepsilon_{33})^2 + (\varepsilon_{33} - \varepsilon_{11})^2 \right) \\ + \delta_5^2 \left(\varepsilon_{12}^2 + \varepsilon_{23}^2 + \varepsilon_{31}^2 \right) \end{array}} \end{pmatrix} \tag{2.8}$$

where ε is the strain tensor in the crystallographic coordinate system. The deformation potential constants are $\delta_1 = 8.6eV$, $\delta_2 = -9.5eV$, $\delta_3 = -2.1eV$, $\delta_4 = -0.5eV$, and $\delta_5 = -4.0eV$ for Si.

The spatial variation of E_C and E_V results in an adjustment to the potential energy terms that are used in Schrodinger equation for calculations of electron and hole concentration and to the electric field terms that are used in the transport equations. Independent variations of E_C and E_V are handled using a formalism similar to that used for graded heterostructures. Using this formalism, effective electric fields for electrons and holes can be written as:

$$\vec{E}_n = \frac{1}{q}\vec{\nabla}E_C \tag{2.9}$$

$$\vec{E}_p = \frac{1}{q}\vec{\nabla}E_V \tag{2.10}$$

We have to remember that hole effective masses vary due to mechanical strain:

$$\frac{\hbar^2}{2m_{ij}^{*l}} = \frac{\hbar^2}{2m_{ij}^{*}} \pm \delta_4^2 \left((\varepsilon_{11} - \varepsilon_{22})^2 + (\varepsilon_{22} - \varepsilon_{33})^2 + (\varepsilon_{33} - \varepsilon_{11})^2 \right) \tag{2.11}$$

The strain ε can be found directly from the difference of lattice parameters or from the stress tensor at the interface. The stress tensor σ is converted to strain using the compliance tensor S: $\varepsilon = S\sigma$. In silicon, S has three unique, non-zero, components which are taken as $S_{11} = c_{11}^{-1}$ = 7.684×10^{-13} cm^2/dyne, S_{12} = -c_{12}^{-1} = -2.139×10^{-13} cm^2/dyne, $S_{44} = c_{44}^{-1}$ = 1.257×10^{-12} cm^2/dyne [3].

The Si/$Si_{1-x}Ge_x$/$Si_{1-y}Ge_y$ p-MOSFETs and p-MODFETs have a fully relaxed, or partially strained, $Si_{1-y}Ge_y$ buffer, a compressively strained $Si_{1-x}Ge_x$ channel, and a tensile strained Si cap on the surface of semiconductor structure. Band gaps and band offsets of strained SiGe with various Ge content grown on relaxed Si or SiGe layers have been calculated by Riegl and Vogl [20] and further corrected for better agreement with experimental data by Schaffler [5]. The results are shown in Fig. 2.3.

2.1.3 Effective masses and mobility

A direct consequence of the band structure is the effective transport mass both of electrons and holes. The areas of constant energy in the conduction band minima consist of six (Δ) and eight (L) ellipsoids for Si and Ge, respectively. So, the electrons in both materials are completely described by two mass parameters: the longitudinal mass m_l along the symmetry axis of the ellipsoid, which is (100) directions in Si and (111) directions in Ge, and the transversal mass m_t within the plane normal to the symmetry axis. In both materials the longitudinal mass is significantly larger than the transversal mass (Table 2.1). Published papers on electron masses measurements in bulk Si and Ge showed that the conduction band minima behave to good approximation parabolic, i.e. the mass parameters

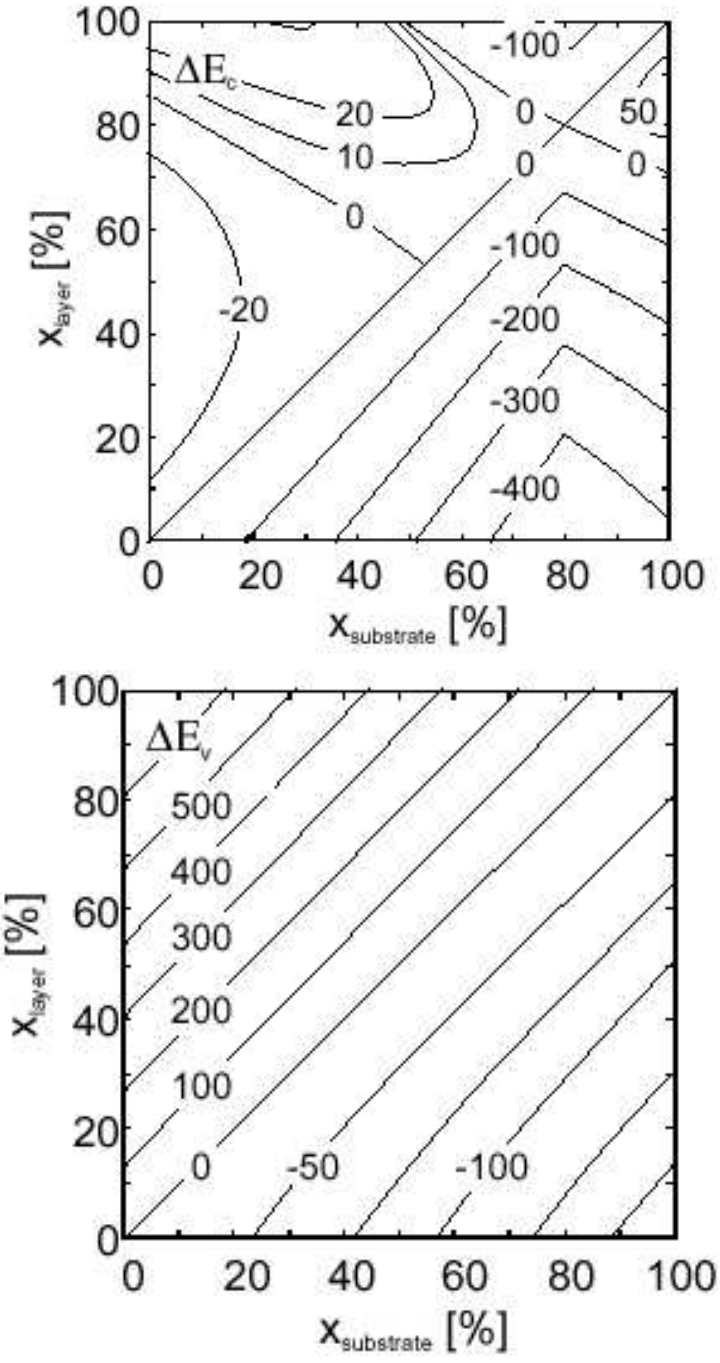

Figure 2.3: Contour plots for the minimum conduction and valence band offsets of $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ interfaces.

are only weakly affected by band-filling effects via temperature or doping [21]. Theoretical investigations suggest that the Δ (Si-like) and L (Ge-like) mass parameters remain almost unaffected over the entire range of compositions, and that they are also rather insensitive to strain [20].

Table 2.1: Experimental band parameters of unstrained, undoped bulk Si and Ge at room temperature [3].

		Si	Ge
Electron mass (m_0)	m_t	0.19	0.08
	m_l	0.91	1.59
Valence band parameters	A	-4.26	-13.27
	B	-0.63	-8.63
	$\|C\|$	4.93	12.4
Band-edges masses of hole (m_0)	m_{hh}	0.53	0.28
	m_{lh}	0.15	0.04
	m_{so}	0.23	0.09

The situation at the valence band edge is even more complex, because the Γ-point valence band maximum is made up of three strongly interacting bands. In unstrained Si and Ge the heavy-hole (HH) and light-hole (LH) bands are degenerate at the Γ point, whereas the spin-orbit-split hole (SO) band is separated by Δ_{Si} = 44 meV in Si and Δ_{Ge} = 290 meV in Ge [22]. The HH and LH bands are warped, i.e. the effective masses depend on the crystal direction. In a first approximation the band dispersion is frequently described by the three band parameters A, B, and C according to

$$E_{HH,LH} = E_v - \frac{\hbar^2 k^2}{2m_0} \times \left(A \pm \sqrt{B^2 + \frac{C^2}{k^4}\left(k_x^2 k_y^2 + k_y^2 k_z^2 + k_z^2 k_x^2\right)} \right) \tag{2.12}$$

$$E_{SO} = E_v - \Delta - \frac{\hbar^2}{2m_0} A k^2 \tag{2.13}$$

where E_v is the Γ-point energy, m_0 is the free electron mass, Δ is the spin–orbit splitting, and $\hbar$ is Planck's constant devided on 2π. The **+** and **-** signs describe the LH and HH bands, which split for $k \neq 0$. The parabolic approximation in (2.12) is only valid next to the Γ-point. The close proximity of the bands leads also to a significant non-parabolicity, especially of the HH band, even for minor changes of the hole energy. As a result, the effective hole masses depend sensitively on external electric fields as well as on doping concentration and temperature. Hence the experimental values of the three hole masses for

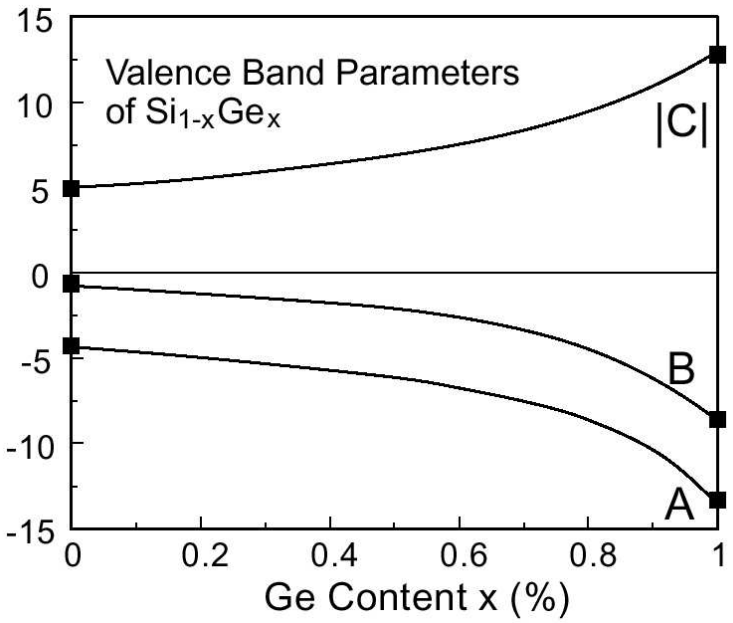

Figure 2.4: Valence band parameters A, B, and C as a function of the Ge content x. The curves are based on the non-linear interpolation scheme for the L, M, N representation proposed by Lawaetz [24] and are converted into the frequently used A, B, C parameter set.

Si and Ge given in table 4.1 apply only to small hole densities and are averaged values over all crystal directions.

Experimental and theoretical work concerning the valence bands in $Si_{1-x}Ge_x$ alloys has been performed by several groups. It was found that a linear interpolation of the SO splitting between the values of Si and Ge agrees reasonably well with experimental results conducted on $Si_{1-x}Ge_x$ bulk alloys [23]. On the other hand, the variation of the band parameters with x, and thus of the effective hole masses, is the subject of much more controversial discussions. Most of the calculations or interpolation schemes employing the band parameters A, B, and C, or other sets of band parameters derived from the different matrix representations of the valence band, failed to reproduce all experimental data available. At least qualitative agreement of the x dependence has been achieved by the non-linear interpolation scheme proposed by Lawaetz [24]. A conversion of his original L, M, N representation into the band parameters A, B, and $|C|$ [22] used in (2.12) and (2.13) is plotted in Fig. 2.4 as a function of the Ge content x. Application of strain lifts the degeneracy of the HH and LH bands at the Γ-point [19] and as a result, change effective masses (see also equation (2.11)). In the important case of a pseudomorphic $Si_{1-x}Ge_x$ layer on an Si substrate, or, more generally, on an unstrained $Si_{1-y}Ge_y$ substrate with $x > y$, the HH band is shifted upward. In addition, the effective in-plane mass of the HH hole band becomes

lighter and warping is reduced [25]. High enough strain can even lead to a mass inversion, i.e. the topmost 'HH' band can have a lower mass than the lower-lying 'LH' band. This class of layer sequences correspond to biaxial compressive strain in the (100) plane concomitant with uniaxial tensile strain perpendicular to this plane. The strain components are reversed, if a pseudomorphic $Si_{1-x}Ge_x$ layer is grown on cubic $Si_{1-y}Ge_y$ substrate with $x < y$. Accordingly, the LH is shifted up while simultaneously its effective mass becomes heavy-hole-like.

The most important transport parameter of a semiconducting material is the carrier mobility μ, which describes the linear relation between the average carrier velocity υ and an external electrical field E in the low-field limit (and in the absence of external magnetic fields).

$$\upsilon = \mu \cdot E \tag{2.14}$$

μ is directly proportional to the transport scattering time τ and indirectly proportional to the effective mass of the respective carrier:

$$\mu = \frac{q}{m^*}\tau \tag{2.15}$$

where q is the carrier charge ($q = e^-$ for electrons and $q = -e^-$ for holes, here e^- is electron charge). Within the limits of the wave-vector-independent relaxation time approximation $1/\tau$ is defined by Mathiessen's rule:

$$\frac{1}{\tau} = \sum_i \frac{1}{\tau_i} \tag{2.16}$$

with τ_i being reciprocal scattering times associated with the various scattering mechanisms. Thus the mobility is limited by the mechanism with the smallest scattering time. As HH and LH effective masses of bulk and especially strained $Si_{1-x}Ge_x$ decreased with Ge content x, the hole mobility in plain also increased. The main scattering mechanisms in the elemental (non-polar) semiconductors are scattering at acoustic and optical phonons ('lattice scattering'), and scattering at ionized and neutral impurities. In $Si_{1-x}Ge_x$ crystals random alloy scattering contributes as a fourth independent mechanism, which can reduce mobility in $Si_{1-x}Ge_x$. Strain will affect all scattering mechanisms, because the strain-induced changes

in the valence and conduction band structure affect the relative importance of intra- and inter-valley scattering events [26]. Ample experimental and theoretical data exist for bulk Si, and, to some extent, for bulk Ge. The most available models work best for unstrained n-type bulk material at temperatures above 100 K and for rather small doping concentrations below some 10^{17} cm^{-3} [5]. Under these conditions intra- and inter-valley lattice scattering is dominating. However, some authors show importance of alloy scattering [27, 137] With the freezing out of phonons at cryogenic temperatures ionized impurity scattering becomes the limiting mechanism whereas the influence of neutral impurity scattering remains moderate.

2.2 Electrical characteristics of Si and SiGe MOSFETs

The MOSFET current-voltage (I-V) characteristics can be qualitatively described by several operating regions [29] related to applied gate and drain voltages. If a small drain voltage is applied, carriers will flow from the source to the drain through the conducting channel. Thus, the channel acts as a resistor, and the drain current I_D is proportional to the drain-source voltage. This is the *linear region* (*ohmic region*). When the drain voltage increases, eventually it reaches V_{DS_sat}, at which the thickness of the inversion layer near the drain reduced to zero (this is called the pinch-off point). Beyond the pinch-off point, the drain current remains the same because $V_{DS} > V_{DS\_sat}$, carriers velocity reaches saturation velocity υ_{sat} in this material. This is the *saturation region*. Further drain voltage increasing lead to MOSFET breakdown due to impact ionisation process in drain depletion area.

If positive for p-MOSFET or negative for n-MOSFET voltage is applied to the gate, minor carriers accumulated and major carriers depleted in the channel area. So, the drain current in this regime, which is correspond to *depletion* state in channel is very small and its origin mainly is uncontrollable by gate voltage *leakage currents*. MOSFET is closed, it is in "off" state, and drain current is named as *off-current* I_{OFF} in this regime.

As gate voltage increased (moved to negative values for p-MOSFETs and positive values for n-MOSFETs), the MOSFET start to be open and the drain current increases very fast. This is the *subthreshold region*, which corresponds to *weak inversion* in channel. After some voltage V_{Th}, which is named threshold voltage, drain current increases with gate

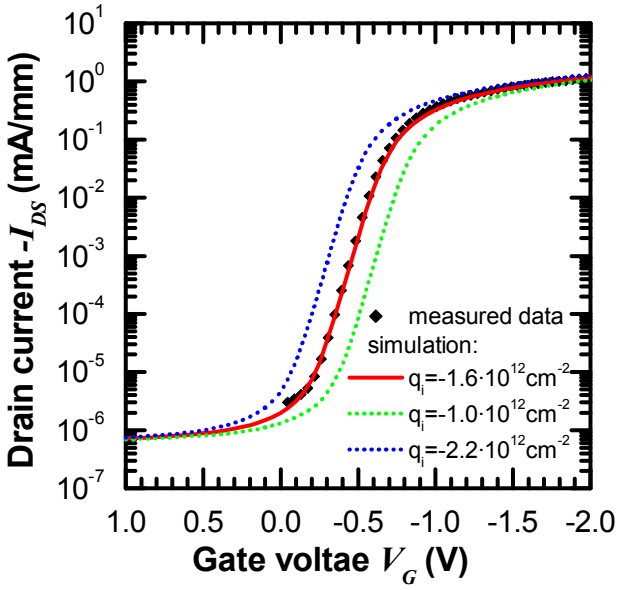

Figure 2.5: MOSFET threshold voltage dependence on the fixed charge density at the Si/SiO_2 interface at low V_{DS}. Simulations of I-V characteristics carried out for p-SiGe hetero MOSFET c2321(a) investigated in this thesis (sections 2.3, 3.1).

voltage slowly and its dependence on gate voltage is close to linear. This region corresponds to *strong inversion* in channel. Difference between gate voltage and threshold voltage $V_G - V_{Th}$, also known as *overdrive gate voltage*, is more useful for description of input I-V characteristics and will be used very often during the analysis. At maximum overdrive gate voltages, drain current increases much slower or even can decrease with gate voltage increases. This is *unlinear region*. The drain current in the subthreshold region at low drain voltage can be modelled by an exponential expression of the form:

$$I_D = I_0 \cdot \exp\left(\frac{\beta\,(V_G - V_{Th})}{\kappa}\right), \tag{2.17}$$

where $\beta = \frac{e}{k_b T}$ is the inverse of the thermal voltage, V_G is the intrinsic gate-to-source voltage, and κ is a quality factor, which is more often used in form $S = \frac{\kappa}{\beta} = \kappa\frac{k_b T}{e}$ known as the *subthreshold slope*.

The threshold voltage V_{Th} depends on the fixed charge at the Si/SiO_2 interface, the work-function of the gate material, the impurity concentration in the doped layers and the gate dielectric capacitance (thickness and dielectric permittivity of the oxide). The threshold

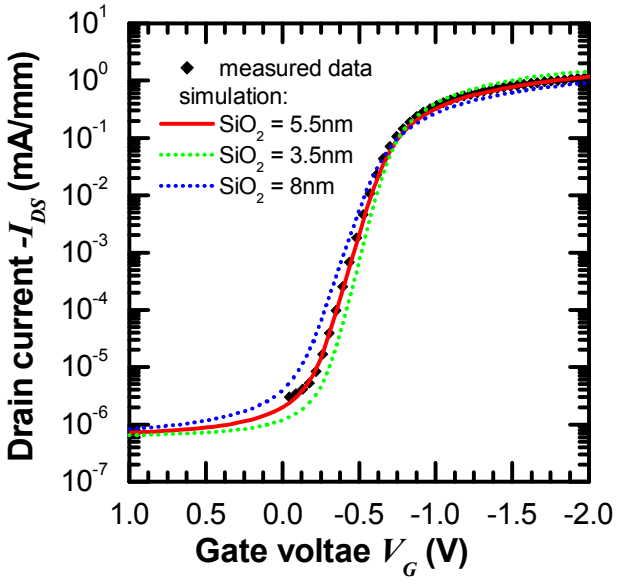

Figure 2.6: MOSFET subthreshold slope dependence on the oxide thickness at low V_{DS}. Simulations of I-V characteristics carried out for p-SiGe hetero MOSFET investigated in this thesis (sections 2.3, 3.1).

voltage sensitivity to fixed charge at the Si/SiO_2 interface is shown in Fig. 2.5.

The oxide capacitance, and the depletion layer capacitance depend on the thickness and permittivity of the oxide, Si cap and SiGe channel. The vertical electric field in the structure depends on the oxide capacitance, and the depletion layer capacitance for a given V_G. So, the subthreshold slope is mainly related to the thickness and permittivity of the oxide, Si cap and SiGe channel. The drain-to-source leakage current depends on the valence band offset between the strained Si cap and the strained SiGe channel, and to a lesser degree it depends on charge trapped at the Si/SiO_2 interface (Fermi level pinning position). The optimal slope is obtained by taking the oxide thickness as a main parameter and the Si cap thickness as a second parameter, see Fig. 2.6.

The drain current I_D in the linear region at intermediate values of V_G can be expressed as

$$I_D \approx \mu_n n V_{DS} \approx \mu_n \frac{W}{L_{eff}} C_{ox} (V_G - V_{Th}) V_{DS}, \tag{2.18}$$

where μ is the average mobility, n is the average sheet density (which depends on V_G) L_{eff} is the effective gate length, W is the gate width, and C_{ox} is the oxide capacitance. To a first

approximation, the linear dependence $n(V_G)$ and a constant value for μ can be used. The effective mobility dependence on gate voltage or sheet density together with electric field is very complicate. However, it can be approximated at low drain-source voltages with help of a simple empirical dependence on vertical electric field $E_\perp$, which is included carrier scattering on charge trapped at semiconductor to insulator interface and well described drain current for most cases (Fig. 2.7).

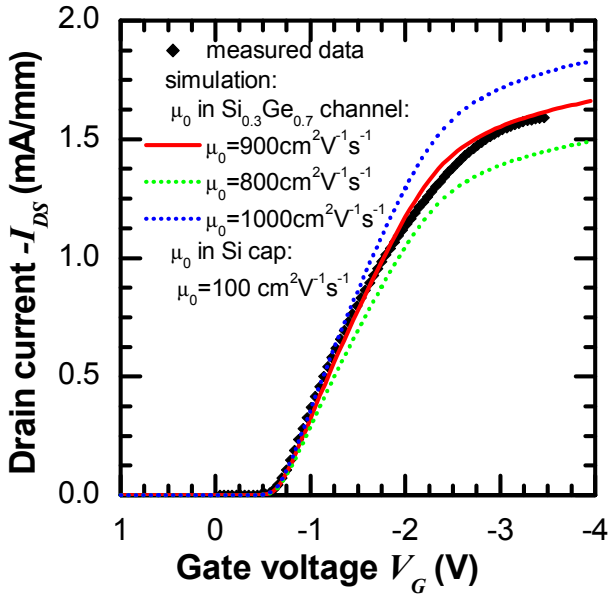

Figure 2.7: The drain current I_D slope at low $(V_G - V_{Th})$ and low V_{DS} is fitted by adjustment of zero field mobility and critical vertical electric field. Simulations of I-V characteristics carried out for p-SiGe hetero MOSFET investigated in this thesis (sections 2.3, 3.1).

$$\mu_{0,p} = \mu_0 \cdot \frac{1}{\sqrt{1 + \frac{E_\perp}{E_{\perp,0}}}} \tag{2.19}$$

where μ_0 is the zero field mobility and $E_{\perp,0}$ is a constant, that depends on material parameters.

The dependence I_D versus V_G at high V_G can be described by taking into account the appearance of parallel conduction in Si cap (Fig. 2.8), source and drain access resistance and by considering different mechanisms of carrier scattering, such as roughness, interface scattering and carrier-carrier scattering.

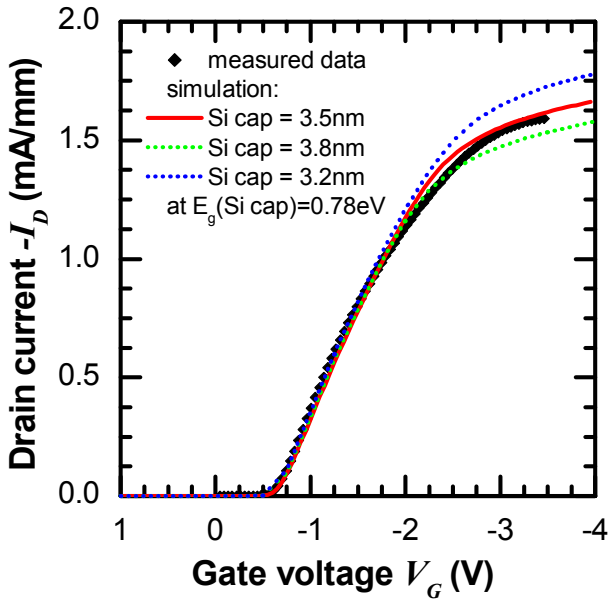

Figure 2.8: Gate voltage dependence of the drain current I_D at high $(V_G - V_{Th})$ and low V_{DS} is fitted by adjustment of Si cap thickness. Simulations of I-V characteristics carried out for p-SiGe hetero MOSFET investigated in this thesis (sections 2.3, 3.1).

2.2.1 Channel length and MOSFET performance

2.2.2 Threshold voltage

Threshold voltage for long channel MOSFETs depend on many factors discussed above in section 2.2. It can be adjusted during the fabrication process using doping variation of poly-Si gate or substrate doping. It can also be adjusted after fabrication process using substrate bias.

For short channel devices, the threshold voltage in linear region usually becomes less negative as channel length decreases for p-MOSFETs. Such behaviour named as threshold voltage roll-off phenomena. Roll-off can be explained by the charge-shaping model [30] as illustrated in Fig. 2.9. This figure shows the cross section of an conventional p-channel MOSFET with short gate length. The channel depletion region overlaps the source and drain depletion regions, charges induced by the field created by the gate bias can be approximated by those within the trapezoidal region. The threshold voltage shift ΔV_{Th} is due to the reduction of charges in depletion layer from the rectangular region $L \times W_m$ to the trapezoidal region $(L + L')W_m/2$. ΔV_{Th} can be approximated [29] as:

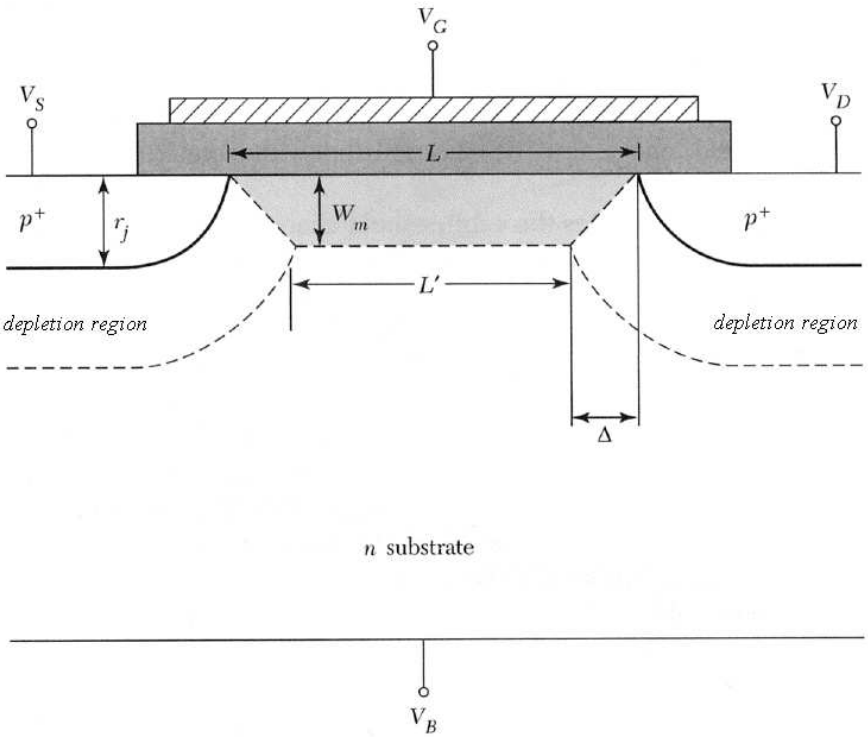

Figure 2.9: Schematic of the charge sharing model [30]. The cross section of an conventional p-channel MOSFET with short gate length is shown.

$$\Delta V_{Th} = -\frac{qN_D W_m r_j}{C_{OX} L}\left(\sqrt{1+\frac{2W_m}{r_j}}-1\right) \tag{2.20}$$

where N_D is substrate doping concentration, W_m is the depletion width, r_j is the junction depth, L is the channel length, C_{OX} is the gate per unit oxide capacitance.

Several different methods to obtain V_{Th} are known in the literature. There are commonly used linear extrapolation of I_{DS} vs V_G dependence at low overdrive voltages [31], constant current method [32, 31], extrapolation g_m vs V_G [32], second-derivative method [33] and Y function method [34]. All methods based on theoretical approximation of drain current near the threshold (see expresiion (2.17)) and would give us the same result in ideal case. However, experimentally measured current dependencies are lightly differ in comparison with theoretical. So, different techniques give us different threshold voltages for the same device. Each method have advantages and disadvantages The second-derivative method, which define threshold voltage as V_G at which the 2^{nd} derivative of the drain current versus the gate voltage reaches its maximum was used in this thesis as most reproducible.

2.2.3 Mobility

The carrier mobility is very important transport parameter of a semiconducting material. It is very often used to describe material quality and devices fabricated from this material However, it is the only one of many factors, which has an influence on device performance.

There are several mobility definitions in use [31]. The fundamental mobility is the *microscopic mobility*. It is describes the mobility of the individual carriers in their respective band. However, no direct experimental methods to measure microscopic mobility are available. The *conductive mobility* is derived from the conductivity or the resistivity of a semiconductor material. The *Hall mobility* is determined from the Hall effect and differs from the conductivity mobility by a factor dependent on the scattering mechanisms. The *drift mobility* is the mobility measured when carriers drift in an electric field. The drift mobility is more useful than others for transport description of devices with bulk channel. The geometry and technology of fabrication have a big influence on the drain current in MOSFETs due to surface scattering (Coulomb scattering from oxide charges and interface states and surface roughness scattering), different mobilities of semiconductor layers in heterostructure, contact resistance and other factors. So, the very useful quantity to compare different devices is the *effective mobility*, determined from the device current-voltage and capacitance-voltage characteristics.

The methods of effective mobility extraction based on the fact that the MOSFET drain current I_D is due to drift and diffusion carriers in the channel. The drain current in this approximation can be written as

$$I_D(V_G) = q\frac{W \cdot \mu_{eff}(V_G) \cdot p_s(V_G) \cdot V_{DS}}{L} - W \cdot \mu_{eff}(V_G) \cdot kT \cdot \frac{dp_s}{x} \qquad (2.21)$$

where L and W is the MOSFET channel length and width respectively, q is the carrier charge (e^- for electrons and $-e^-$ for holes) p_s is the mobile channel carriers density, and μ_{eff} is the effective mobility ($\mathrm{cm^2V^{-1}s^{-1}}$). For low V_{DS}, one can assume the channel charge to be fairly uniform from source to drain, allowing the diffusive second term in (2.21) to be dropped. Solving for μ_{eff} then gives

$$\mu_{eff}(V_G) = \frac{L \cdot I_D(V_G)}{q \cdot W \cdot p_s(V_G) \cdot V_{DS}} = \frac{g_d(V_G) \cdot L}{q \cdot W \cdot p_s(V_G)} \tag{2.22}$$

The methods of μ_{eff} extraction have difference only in approximations used to determine channel carriers density p_s. Simplest approximation, which is used for channels from homogenous material as bulk Si MOSFETs with not very high vertical electric field on SiO_2/Si interface, can be presented as

$$p_s(V_G) = \frac{1}{q} C_{ox}(V_G - V_{Th}) \tag{2.23}$$

This approximation gives very significant drop of mobility near $V_G = V_{Th}$ and also incorrect results for heterostructure based MOSFETs.

The approximation giving better results is based on a direct calculate of p_s from C-V measurements according to

$$p_s(V_G) = \frac{1}{q} \int_{-\infty}^{V_G} C_{GS}(V_G)\, dV_G \tag{2.24}$$

where C_{GS} is the gate-to-channel capacitance per unit area (F / cm^2). Method of measurements of C_{GS} will be described in chapter 3, section 3.3. Even if (2.24) together with (2.22) used for μ_{eff} extraction, there are still some sources of error, because the I-V and C-V characteristics measured at slightly different conditions. The drain current measured at $V_{DS} \neq 0$, capacitance at $V_{DS} = 0$. Diffusion component in (2.21) also can not be neglected every case. The assumption that the drain current depends only on channel characteristics is also can be wrong for short channel devices, were source and drain resistance can not be neglected. Leakage currents also can introduce error if we interested in mobility only in the channel region (Fig. 2.10).

The μ_{eff} dependence on vertical electric field near the surface E_{eff} is very important MOSFET characteristic, because this dependence can be quantitatively compared with the same dependencies for similar MOSFETs with other level of doping in heterostructure or for MOSFETs based on other heterostructures or bulk materials. Ionised impurity and surface scattering, which is very often gives the main contribution to μ_{eff}, are depend on substrate doping density and the gate voltage. The dependence of μ_{eff} on E_{eff} at $V_G > V_{Th}$, where

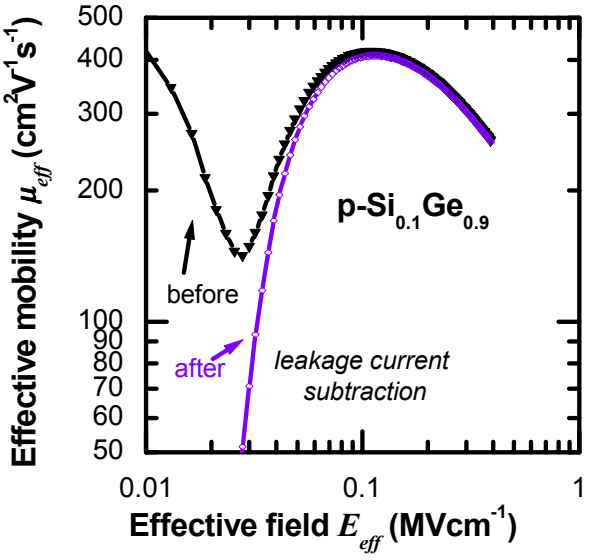

Figure 2.10: Leakage current influence on effective mobility extracted with the help of conventional techniques. Black line shows effective mobility extracted without any corrections. Violet line shows effective mobility extracted after subtraction drain-to-substrate leakage current from the total drain current.

surface scattering is prevail, is very often expressed as some "universal" law for investigated material:

$$\mu_{eff}\left(E_{eff}\right) = \frac{\mu_0}{1+\left(\alpha E_{eff}\right)^{\gamma}} \tag{2.25}$$

A large body of experimental data for Si MOSFETs at room temperature agrees closely with empirical expressions [31]:

$$\mu_{eff,n} = \frac{638}{1+\left(E_{eff}/7\times 10^5\right)^{1.69}} \tag{2.26}$$

for electrons, and

$$\mu_{eff,p} = \frac{240}{1+\left(E_{eff}/2.7\times 10^5\right)^{1.0}} \tag{2.27}$$

for holes.

The electric field E_{eff} is not actually field in area, where the carriers flow. It is again some effective quantity, which is useful for device comparison. This point is especially

important for understanding of MOSFETs based on heterostructures with buried channel. The effective field E_{eff} for homogenous bulk p-MOSFETs is usually defined as [31]:

$$E_{eff}(V_G) = \frac{q}{\varepsilon_0}\left(\frac{N_{depl}(V_G)}{\varepsilon_{Si}} + \eta\frac{p_s(V_G)}{\varepsilon_{Si}}\right) \tag{2.28}$$

where N_{depl} and p_s are the carrier sheet densities (cm^{-2}) in the space-charge region and in the inversion layer respectively. The parameter η is usually taken as the η = 1/3 for hole mobility and η = 1/2 for electron mobility.

Expression (2.28) is unuseful in the case of heterostructure based MOSFETs, because depletion and inversion charge can be allocated in areas with different dielectric constants. So for SiGe buried channel p-MOSFET on virtual substrate expression (2.28) should be modified as:

$$E'_{eff}(V_G) = \frac{q}{\varepsilon_0}\left(\begin{array}{l}\frac{n_{s\_cap}(0)-n_{s\_cap}(V_G)}{\varepsilon_{Si}} + \frac{n_{s\_channel}(0)-n_{s\_channel}(V_G)}{\varepsilon_{Si_{1-x}Ge_x}} \\ +\frac{n_{s\_VS}(0)-n_{s\_VS}(V_G)}{\varepsilon_{Si_{1-y}Ge_y}} \\ +\frac{1}{3}\left(\frac{p_{s\_cap}(V_G)}{\varepsilon_{Si}} + \frac{p_{s\_channel}(V_G)}{\varepsilon_{Si_{1-x}Ge_x}} + \frac{p_{s\_VS}(V_G)}{\varepsilon_{Si_{1-y}Ge_y}}\right)\end{array}\right) \tag{2.29}$$

where n_{s_cap} is minor carrier (electrons) sheet density in the Si cap layer, $n_{s\_channel}$ in the $Si_{1-x}Ge_x$ channel, and n_{s_VS} in the $Si_{1-y}Ge_y$ VS, p_{s_cap}, $p_{s\_channel}$ and p_{s_VS} is major carrier (holes) sheet density in the Si cap, $Si_{1-x}Ge_x$ channel and $Si_{1-y}Ge_y$ VS respectively, and ε_{Si},$\varepsilon_{Si_{1-x}Ge_x}$ and $\varepsilon_{Si_{1-y}Ge_y}$ are dielectric constants of Si, $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ respectively. Sheet densities of minor and major carriers could be obtained from fitting of measured C_{GS} and C_{BS} capacitance by theoretical simulation of C-V characteristics. However, this approximation required full knowledge about heterostructure used in fabricated MOSFET, which can be differ from original design, and it also can be unuseful due to this limitations.

Other often-used expression for the E_{eff}, which is simple approximation of (2.28), can be presented as:

$$E_{eff}(V_G) = \frac{q}{\varepsilon_0}\left(\frac{N_{depl}(V_G)}{\varepsilon_{Si}} + \frac{1}{3}\frac{p_s(V_G)}{\varepsilon_{SiGe}}\right) \tag{2.30}$$

It based on assumption that almost all depletion charge concentrated only in Si cap, and almost all accumulation charge concentrated in $Si_{1-x}Ge_x$ channel. One can see that (2.30)

electric field on SiO_2/Si interface and electric field in $Si_{1-x}Ge_x$ channel is differ from electric field in conventional Si MOSFETs, and can be used only as "effective" quantity. However, it is more useful than (2.29) for comparison investigated SiGe MOSFETs with other SiGe and Si MOSFETs.

So the best available method to extract effective mobility is the combination of $I_D(V_G)$ characteristic measurements for long channel MOSFET at low V_{DS} voltage with split C-V measurements ($C_{GS}(V_G)$) for the same device.

2.2.4 Subthreshold swing and Drain Induced Barrier Lowering (DIBL)

The drain current in the subthreshold region is dominated by diffusion instead of drift and is derived as the same as the collector current in a bipolar transistor with homogenous base doping. The p-MOSFET can be considered as a p-n-p (source-substrate-drain) bipolar transistor in this region [29]. Hole concentration for long channel p-MOSFET varied from source to drain mostly linear and drain current can be approximated as:

$$I_D = -qW\int_0^{h_B} D_p \frac{\partial p\,(x,y)}{\partial x}dy \approx -qA\int_0^{h_B} D_p \frac{p\,(x=0,y)-p\,(x=L,y)}{L}dy \qquad (2.31)$$

where W is the channel width, x is the distance along the channel ($x = 0$ is source placement and $x = L$ is the drain placement), y is the depth under gate oxide, h_B is the maximum depth of the current flow, D_p is the diffusion coefficient for holes (D_p is can be depth dependent for complicate heterostructure), $p(x)$ is the hole density along the channel, L is the channel length. The hole density can be written as:

$$p\,(x=0,y) = p_i \exp\left(q\frac{\Psi_{SB}\,(y)}{k_B T}\right) \qquad (2.32)$$

$$p\,(x=0,y) = p_i \exp\left(q\frac{\Psi_{SB}\,(y)-V_{DS}}{k_B T}\right) \qquad (2.33)$$

where p_i is the intrinsic hole concentration, $\Psi_{SB}(y)$ is the depth dependant potential, y varied from surface to substrate. In the simplest case of the conventional Si homogeneously doped p-MOSFET, potential can be approximated as $\Psi_{SB}(y) = \Psi_S - \Psi_B$ (h_B - y). The surface potential Ψ_S is approximately equal to (V_G - V_{Th}). Drain current can be written as:

$$I_D = \frac{qWD_p p_i}{L} \exp\left(\frac{q\left(V_G - V_{Th}\right)}{k_B T}\right) \exp\left(-\frac{q\Psi_B}{k_B T}\right) \left(1 - \exp\left(-\frac{qV_{DS}}{k_B T}\right)\right) \tag{2.34}$$

So, for this case at low V_{DS} and $\Psi_B = 0$ drain current can be easy approximated by (2.17) with quality factor n = 1:

$$I_D = \frac{qWD_p p_i}{L} \exp\left(\frac{q}{k_B T}\left(V_G - V_{Th}\right)\right) \tag{2.35}$$

Subthreshold swing of such device $S = \left(\partial\left(\log I_D\right)/\partial V_G\right)^{-1} = k_B T/q$ has lowest value. However, even for conventional Si MOSFETs subthreshold swing is higher due to more complicate $\Psi_{SB}(y)$ dependence on y and also $\Psi_S \neq (V_G$ - $V_{Th})$ due to presence movable charge in the gate dielectric. The S typical value is 70-100mV/decade for Si p-MOSFETs at room temperature ($T = 293$ K).

For SiGe p-MOSFETs the $\Psi_{SB}(y)$ dependence is much more complicate and the D_p is different for each heterostructure layer. So, estimated S should be higher than for conventional Si p-MOSFETs.

There are several methods to extract subthreshold swing from measured I-V characteristics. All methods based on definition (2.36), which would give us the same result in ideal case:

$$S = \left(\partial\left(\log I_D\right)/\partial V_G\right)^{-1} \tag{2.36}$$

However, slope extracted from measured data is typically depend on method used due to not ideal $I_D(V_G)$ dependence in reality. Lowest S value could obtain with help of method close to Ghibaudo Y function method [34] for threshold voltage extraction. Here subthreshold slop defined as a minimum of function $\ln(10 \cdot I_D/g_m)$, and it correspond to maximum slope of tangent to $\log I_D(V_G)$ curve. Most widely used method is straight line pass through $\log I_D(V_G = V_{Th})$ point and most points in subthreshold region of $\log I_D(V_G)$ curve. Last one was used in this thesis.

Dependence of I_D in subthreshold region on drain voltage can be characterised with help of important parameter named as DIBL (Drain Induced Barrier Lowering). DIBL is defined as threshold voltage difference, when drain voltage is for 1.0 V increased. DIBL for long channel devices can be estimated from (2.34) and it is close to zero:

$$\Delta V_{Th} \approx -\frac{k_B T}{q} \ln\left(1 - \exp\left(-\frac{q}{k_B T}\Delta V_{DS}\right)\right) \approx -0.026 \ln\left(1 - \exp\left(-38\right)\right) \text{V} \qquad (2.37)$$

For short channel devices hole concentration $p(x,y)$ depend on distance along channel x and depth y more complicate than for long channel devices. Expression (2.31) can be used only with modification, where channel length is not fixed, but depth and drain voltage dependent $L(y,V_{DS})$ as described in subsection 2.2.2. For a device operated in the saturation region, the depletion layer width of the drain junction is significantly wider than that of the source junction. So, expression (2.20) for short channel devices is drain voltage dependent and it should be observed DIBL phenomena for short-channel MOSFETs.

2.2.5 Contact Resistance

Most methods used for extraction of access contact resistance R_{SD} and channel effective length L_{eff} based on simplest R vs L method [35].

From expression (2.18) for low values of V_{DS}, we can obtain:

$$R_{total} = \frac{V_{DS}}{I_D} = \frac{L - \Delta L}{W \mu_{eff} q N_s} + R_{SD} \qquad (2.38)$$

Here the drawn geometrical length L changes to the effective length is $L_{eff} = L - \Delta L$.

Provided that the first term on the right hand side of (2.38) is an approximately linear function of $V_G - V_{Th}$, the second term R_{SD} will be a constant, which is independent of $V_G - V_{Th}$ and gate length and dependent only on device fabrication technology.

Therefore, plotting R_{total} against the measured L, with V_G as a parameter, should give a series of straight lines, with crossover point, where $L = \Delta L$ and $R_{total} = R_{SD}$. Often it is difficult to define a point where all the lines meet and this is normally an indication that values of R_{SD} and ΔL change with $V_G - V_{Th}$. This can also be due to slight differences in the properties of different devices or a failure of the assumptions leading to (2.38).

To remove the problem of multiple straight lines not meeting a single point, Hu *et al* [36] propose to use just two lines. This method does not assume ΔL and R_{SD} are constant with V_G and can discover their functional dependencies. If the two lines are almost parallel, which is typical for low $V_G - V_{Th}$, then a small error will make a big difference to the point

of intersection. This error worsens at higher values of $V_G - V_{Th}$ since the angle between the two lines is smaller, however, values extracted at high $V_G - V_{Th}$ can be differ from values extracted at low $V_G - V_{Th}$ due to previous assumption. So, this method significantly reduces the precision of extracted variables.

Terada and Muta [37] propose other presentation for expression (2.38):

$$R_{total}\left(\frac{1}{W\mu_{eff}qN_s}\right) = L\frac{1}{W\mu_{eff}qN_s} + \left(R_{SD} - \Delta L\frac{1}{W\mu_{eff}qN_s}\right) \tag{2.39}$$

The $A^\star = 1/W\mu_{eff}qN_s$ and $B^\star = \left(R_{SD} - \Delta L/W\mu_{eff}qN_s\right)$ extracted from interception of R_{total} and L for different $V_G - V_{Th}$ can be plotted one versus other and dependence obtained can be fitted to extract average R_{SD} and ΔL. This procedure of ΔL and R_{SD} extraction is also known as double regression method. Unfortunately, the accuracy of method is dependent on accuracy $A^\star$ and $B^\star$ extraction. So, this method also have not significant advantages in comparison with R vs L method.

Suciu and Johnston [38] propose dE method, which is very similar to double regression method with some modifications. They use analytical expression for μ_{eff} and extract also values of zero field mobility μ_0 and subthreshold swing together with R_{SD} and ΔL values.

Taur *et al* [39] propose "shift and ratio" method which is also based on (2.38). As the mobility can be any function of overdrive gate voltage, the equation (2.38) can be rewritten as

$$R_{total} = \frac{V_{DS}}{I_D} = Lf\left(V_G - V_{Th}\right) + R_{sd} \tag{2.40}$$

If the resistance R_{SD} is a weak function of gate voltage and its derivative can be neglected, then we obtain after differentiation (2.40) with respect to V_G:

$$S = \frac{dR_{total}}{dV_G} = L\frac{df\left(V_G - V_{Th}\right)}{dV_G} \tag{2.41}$$

Large device and several small devices are used for ΔL extraction. S is plotted versus V_G for the large device and one small device. To solve for L and V_{Th}, one curve is shifted horizontally by a varying amount δ and the ratio $r_{21} = S_1(V_G)/S_2(V_G - \delta)$ between the two devices is calculated. When δ is close to threshold voltage difference between the two

devices, r_{21} is nearly constant. So, for constant gate overdrive, where the mobility identical or nearly identical, the r_{21} can be written as

$$r_{21} = \frac{S_1(V_G)}{S_2(V_G - \delta)} = \frac{L_1 - \Delta L}{L_2 - \Delta L} \approx \frac{L_1}{L_2 - \Delta L} \tag{2.42}$$

where L_1 and L_2 are the channel lengths of the large and small device, respectively. The line, plotted through obtained L_1/r_{1i} values versus L_i, intercept L axis at ΔL. Hence, this method is less sensitive to devices threshold voltage variation, however S variable have large error due to differentiation.

The capacitance-voltage technique can be also used to determine $L_{eff} = L - \Delta L$ by source and drain contacts to gate overlap capacitance extraction. However, for small-area MOSFETs the capacitance is very small, making measurements not easy even though today's capacitance meters allow measurements in the sub-pF regime. The measurement problems can be partially alleviated by connecting many devices in parallel, however any reliability problems neglect this advantage.

So, we conclude that all described methods of ΔL and R_{SD} extraction produce the similar results with enough accuracy in ideal case, however all produce errors when ΔL or R_{SD} are dependent on gate voltage V_G. All methods are unuseful when ΔL or R_{SD} are varied from device to device due to fabrication technology limits for short channel MOSFETs.

2.2.6 Short Channel Effects

There are several effects, which are become apparent with channel length reduced. Several of these are associated with the source and drain implanted regions and become more important as a larger proportion of the channel is close to the contacts. Drain voltages used in MOS devices do not scale in proportion to the channel length so electric fields along channel will increase as devices shrink.

Increasing the drain bias will increase the depletion width of the p-n junction between the drain contact and the oppositely doped region containing the inverted channel. In saturation, the majority of the applied bias will drop across this depletion region. The increased depletion width means an effectively shorter channel, increasing drain current. Like many short channel effects, this causes an increase of current with V_{DS}, even after the saturation

point. Also in common with other short channel effects, an increase in the channel doping reduces the dependence of depletion width on V_{DS}. The increased doping introduces additional problems, not least is that the increased scattering from ionised impurity atoms lowers the mobility.

Considering the band diagram in the off state, with high applied V_{DS}, the drain bias depletion region lowers the potential barrier at the source. This lowers the threshold voltage and hence increases the current for a particular gate voltage. This behaviour more thoroughly described in subsection 2.2.4.

The extreme example of DIBL is punch through. In this case the depletion regions of the source and drain touch each other and there is no barrier to current flow. The gate still has some control over current since it can reduce the resistance to current flow by forming an inversion layer. By applying a specific potential to the gate, the barrier may reappear and stop current flow. However, the implanted contacts can be quite deep within the semiconductor (tens or hundreds of nanometres) where the gate has little effect. The device therefore may not turn off, no matter at what potential the gate is.

When the electric field at the drain end of the channel is high enough, carriers may gain enough energy to excite electron-hole pairs by impact ionisation. Minority carriers will join the original carriers, increasing the current. Majority carriers travel to the substrate. This current induces a potential difference across the channel-substrate junction, which can charge the semiconductor bulk and affect the threshold voltage. This results in an extra increase in I_D. This effect is most common in devices with high resistance substrates, for example those using silicon on insulator (SOI) techniques or those operated at low temperature where the substrate becomes more resistive.

2.2.7 Leakage currents

There are several sources of leakage currents in p-SiGe MOSFETs. Gate leakage current significantly depends on gate dielectric quality, which could be worsen due to reduced thermal budget of fabrication process. Gate leakage current has influence on device characteristics in subthreshold region such as subthreshold swing of threshold voltage and off current. Also, it limits maximum applied gate voltage due to gate dielectric degradation. A

source of drain-to-source leakage current can be found in hole conductunce through substrate due to not enough n-type background or negatively biased substrate (it can be also dynamically biased substrate due to internal charge redistribution for the float body contact or body contact separated from surface by field oxide or thick VS). Hole and electron conductance of VS is additional source of leakage current for metamorpfic MOSFETs due to deffects in VS. Impact ionisation and other generation-recombination processes in drain depletion area are also source of drain to source and drain to substrate leakage. All leakage currents are mostly uncontrolable and it makes device DC characteristics worse.

2.3 Current-voltage characteristics simulations of SiGe p-MOSFET and extraction of MOSFET parameters

Commercial software for drift-diffusion (DD) (see section subsec:IVsimDD-DC) simulations from ***Avant!*** [40] or ***Silvaco*** [49] can be used to simulate the current-voltage characteristics. The procedure is split into several steps:

The first step is a simulation of the $I_D(V_G)$ p-MOSFET characteristics at low drain-source voltages V_{DS} for a long channel device.

Fitting of the subthreshold characteristics starts with fitting the subthreshold slope by changing the oxide thickness and the oxide permittivity (see Fig. 2.6). The next step is fitting the threshold voltage, by defining the trapped charge density at the oxide-cap interface (see Fig. 2.5). The off-current can depend on the leakage through dislocations in the substrate, device surface purity, etc. Therefore its fitting is usually not included in simulation. A further step is the correction of the band profile and low field carrier mobilities to adjust for the current (sheet density) at low V_G above the threshold (see Fig. 2.7). The best fitting can be obtained by changing the SiGe channel bandgap (correction of the Ge content in the channel) and the electron affinity in the strained silicon layer (correction of the purity and strain of the Si cap). After that we need to adjust the current at high V_G by correcting the thickness of the Si cap (see Fig. 2.8). The last step to fit $I_D(V_G)$ is to adjust the whole curve by correcting the low field mobility parameters.

The second step is a simulation of $I_D(V_G)$ p-MOSFET characteristics at low and high drain-source voltages V_{DS} for devices with different lengths. The short channel effect model is

calibrated at this step. After fitting $I_D(V_G)$ characteristic at low V_{DS} for a long channel device, $I_D(V_G)$ characteristics for all devices with different length are fitted. Best fitting can be obtained by changing the shape of the contacts and the contact doping concentrations. This fitting is carried out for several iterations. During each iteration, fitting at the long channel device $I_D(V_G)$ characteristics must be readjusted.

The final, third step is simulation of the output $I_D(V_{DS})$ p-MOSFET characteristics at different gate voltages V_G for devices with different lengths. High field effects are simulated and the efficiency of the employed MOSFET model is rechecked in this step.

The MOSFETs output characteristics are simulated to describe the saturation behavior of MOSFETs at high source-drain voltages. The drain current versus drain-source voltage dependencies are fitted in the Caughey-Thomas high field mobility approximation (2.43) by varying the saturation velocity v_p^{sat} parameter (Fig. 2.11).

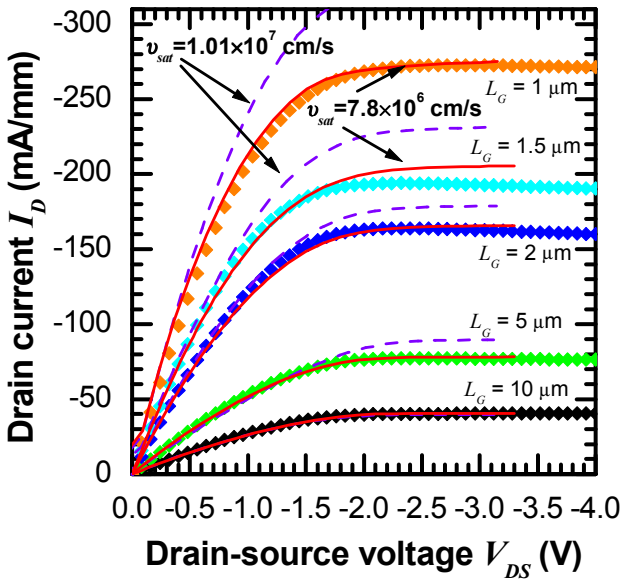

Figure 2.11: Measured (dots) and simulated (solid lines) output current-voltage characteristics of $Si_{0.3}Ge_{0.7}/Si_{0.7}Ge_{0.3}$ p-MOSFETs with gate length 1-10 μm. Saturation velocity for holes υ_p^{sat} was used as fitting parameter. It was found decreased saturation velocity $\upsilon_p^{sat} = 7.8 \times 10^6$ cm/s for $Si_{0.3}Ge_{0.7}$ in comparison with $\upsilon_p^{sat} = 1.01 \times 10^7$ cm/s for Si. Simulations of I-V characteristics carried out for p-SiGe hetero MOSFET investigated in this thesis (sections 2.3, 3.1).

$$\mu_p = \mu_{0,p} \cdot \left(1 + \frac{\mu_{0,p} \cdot E_{\|,p}}{v_p^{sat}}\right) \tag{2.43}$$

where $\mu_{0,p}$ is a low field mobility defined in (2.19), $E_{\|,p}$ is the electric field along the channel, and v_p^{sat} is the saturation velocity.

No variation of saturation velocity with device gate length was observed down to the minimum of available for measurements gate length 1 μm. Such a possible dependence, known also as a velocity overshoot effect, is expected to appear in devices with a gate length of $\sim$0.1-0.2 μm at room temperature or in devices with gate length of 1 μm at low temperatures.

The calibrated p-MOSFET model obtained as a result of this fitting can be used to design and simulate the new heterostructures with optimized parameters. Also it can be used to compare parameters extracted from simulation of measured I-V and C-V characteristics with parameters obtained with help of other experimental techniques.

2.3.1 Schrodinger-Poisson modeling

The software normally used for calculating the sheet density in semiconductor structures such as MODFET or MOSFET, only solves the Poisson equation and uses Boltzmann statistics to obtain the density of charge from the band profile. As a result the solution is not self-consistent and it starts to deviate from experimental data as the size of a structure decreases. If one solve the Poisson and the Schrodinger equations together, then one obtain a self consistent solution. This requires more time and computational resources, however the self consistent solution is very important for sheet density calculation and $C(V)$ dependence in Si/SiGe heterostructures with few nanometer layer's thickness.

Governing equations to solve the problem are the Schrodinger equation :

$$-\frac{\hbar^2}{2}\frac{d}{dx}\left(\frac{1}{m^*(x)}\frac{d}{dx}\right)\psi(x)+V(x)\psi(x)=E\psi(x) \tag{2.44}$$

and the Poisson equation:

$$\frac{d}{dx}\left(\varepsilon_s(x)\frac{d}{dx}\right)\phi(x)=\frac{-q\left[N_d(x)-N_a(x)-n_e(x)+n_p(x)\right]}{\varepsilon_0} \tag{2.45}$$

The first step is to calculate the Fermi level and the conduction band offset for each layer of structure. The Fermi level is approximated as

$$E_F = E_{Fi} + k_b T \cdot arcsh\left(\frac{N_d^+ - N_a^+}{2 \cdot n_i}\right), \tag{2.46}$$

where $E_{Fi}(T)$ is the intrinsic Fermi level:

$$E_{Fi}(T) = E_c - \frac{1}{2}E_g + k_b T \ln\left(\frac{N_\upsilon}{N_c}\right), \tag{2.47}$$

$n_i(T)$ is the default intrinsic concentration

$$n_i(T) = \frac{1}{4}\left(\frac{2k_b T}{\pi\hbar^2}\right)^{3/2}(m_c m_\upsilon)^{3/4} e^{-\frac{E_g}{2k_b T}}, \tag{2.48}$$

N_d^+, N_a^+ are the ionised donor and acceptor concentration.

Donors and acceptors can be considered to be fully ionised and thus $N_d^+ = N_d$, $N_a^+ = N_a$ at room temperature for N_d, $N_a > N_{mott}$, where N_{mott} $\sim 10^{18}$-10^{19}cm^{-3} is the Mott critical concentration (i.e. impurity concentration on which corresponds the Mott transitions [41]). As it was shown recently in literature, N_{mott} lightly decreased with increasing Ge content in $Si_{(1-x)}Ge_x$ alloy [42]. For all other cases N_d^+, N_a^+ can approximated as:

$$N_d^+ = N_d \cdot \left(1 - \frac{1}{\frac{N_c}{2N_d} \cdot \exp\left(\frac{E_F - E_d}{k_b T}\right) + 1}\right) \tag{2.49}$$

$$N_a^+ = N_a \cdot \left(1 - \frac{1}{\frac{N_\upsilon}{4N_a} \cdot \exp\left(\frac{E_a - E_F}{k_b T}\right) + 1}\right) \tag{2.50}$$

Electron and hole concentration in each layer can be calculated treating each layer separately:

$$\begin{aligned} n_c &= \tfrac{1}{2}\sqrt{\left(N_d^+ - N_a^+\right)^2 + 4n_i^2} + \tfrac{1}{2}\left(N_d^+ - N_a^+\right) \\ n_\upsilon &= \tfrac{1}{2}\sqrt{\left(N_d^+ - N_a^+\right)^2 + 4n_i^2} - \tfrac{1}{2}\left(N_d^+ - N_a^+\right) \end{aligned} \tag{2.51}$$

Equilibrium condition for the whole structure requires $E_F^i = E_F^j$.

The Fermi level inside the substrate and far from the edges of the structure has a value close to the Fermi level calculated inside the substrate treating this layer separately. The Fermi level on the semiconductor-dielectric interface is fixed at a value that depends on interfacial

charge. The Fermi level of a metal is constant throughout and defined by its workfunction. The potential energies for electrons $V_e(x)$ and holes $V_h(x)$ are defined as :

$$V_e(x) = -q\phi(x) + (E_c - E_F), \text{ where } E_c = -\chi + q \cdot \varphi(x),$$

$$V_h(x) = +q\phi(x) + (E_F - E_\upsilon), \text{ where } E_v = -\chi - E_g + q \cdot \varphi(x) \tag{2.52}$$

χ is electron affinity, $\varphi(x)$ is electrostatic potential, generated by the redistributed charge, ΔE_c is the pseudo-potential energy due to the band offset at the heterointerface.

The next step is to solve the Schrodinger equation (2.44) in order to obtain $\Psi_k^{(0)}(x)$ and E_k. It is solved separately for electrons, light holes and heavy holes. Solution of equation (2.44) allows one to calculate the charge density that is required for the Poisson equation in order to obtain the electrical potential $\varphi(x)$.

Concentrations of electrons n_e and holes n_p can be calculated directly from:

$$n_e^{(i)}(x) = \frac{1}{L}\sum_{k=1}^{m} \Psi_k^*(x)\Psi_k(x)\frac{m_e^*(x)}{\pi\hbar^2}\int_{E_k}^{\infty}\frac{1}{1+\exp\left(\frac{E-E_F}{k_bT}\right)}dE, \tag{2.53}$$

$$n_p^{(i)}(x) = \frac{1}{L}\sum_{k=1}^{m} \Psi_k^*(x)\Psi_k(x)\frac{m_p^*(x)}{\pi\hbar^2}\int_{E_k}^{\infty}\frac{1}{1+\exp\left(-\frac{E-E_F}{k_bT}\right)}dE, \tag{2.54}$$

where the Fermi integral was the following form

$$\int_{E_k}^{\infty}\frac{1}{1+\exp\left(\frac{E-E_F}{k_bT}\right)}dE = \ln\left(1+\exp\left(\frac{E_k-E_F}{k_bT}\right)\right) - \left(\frac{E_k-E_F}{k_bT}\right) \tag{2.55}$$

$$\int_{E_k}^{\infty}\frac{1}{1+\exp\left(\frac{E-E_F}{k_bT}\right)}dE = \begin{cases} \ln\left(1+\exp\left(\frac{E_k-E_F}{k_bT}\right)\right) - \left(\frac{E_k-E_F}{k_bT}\right), E_k < E_F \\ \ln\left(1+\exp\left(-\frac{E_k-E_F}{k_bT}\right)\right), E_k > E_F \end{cases} \tag{2.56}$$

Then the Poisson equation is solved directly by substituting equations (2.53) and (2.54) into (2.45).

Another way to calculate the concentration n_e and n_p and to solve the Poisson equation is to use the "iterations method". We can easily calculate the variation of concentration from (2.52) and (2.54):

$$\delta n^{(i)}(x)/\delta\varphi(x) = \sum_{k=1}^{m} \Psi_k^* \Psi_k \frac{qm^*}{\pi\hbar^2 \left(1 + e^{\frac{(E_k - E_F)}{k_b T}}\right)}, \tag{2.57}$$

$$n^{(i+1)}(x) = n^{(i)}(x) + \delta n^{(i+1)}(x)$$

That is why Newton's method [45] can be used to solve (2.45) iterating follow equation:

$$\frac{d}{dx}\left(\varepsilon_s(x)\frac{d\left(\delta\phi^{(i+1)}(x)\right)}{dx}\right) + \frac{q}{\varepsilon_0}\sum_{k=1}^{m}\Psi_k^*\Psi_k\frac{\partial n_k}{\partial E_k}\langle\Psi_k|\, q\delta\phi^{(i+1)}\,|\Psi_k\rangle = -e^{(i)}(x) \tag{2.58}$$

where $e^{(i)}(x) = \frac{d}{dx}\left(\varepsilon_s(x)\frac{d\left(\phi^{(i)}(x)\right)}{dx}\right) + \frac{q}{\varepsilon_0}\left(N_d^+ - N_a^+ - n^{(i)}(x) + p^{(i)}(x)\right)$.

The result solving of (2.58) is a variation of electrostatic potential $\delta\phi^{(i+1)}(x)$, such that $\phi^{(i+1)}(x) = \phi^{(i)}(x) + \delta\phi^{(i+1)}(x)$ can be used in calculating the potential energy in 2.52).

The next step is to repeat the iteration procedure of equation (2.44) solving with the corrected potential energy $V(x)$ together with equation (2.44) to obtain the next value of concentration $n^{(i+1)}(x)$ and $\phi^{(i+1)}(x)$ until variations of potential and concentration are less than some necessary precision $\delta\phi^{(i+1)}(x) < \phi_{err}$, $\delta n^{(i+1)}(x) < n_{err}$

Self consistent solution of the Schrodinger and Poisson equations gives a vertical charge profile $n(x)$ and an electric potential $\varphi(x)$ for each predefined gate voltage. The sheet charge density is calculated from the following:

$$Q(V_G) = q\int_{substrate}^{surface}\left[N_d(x) - N_a(x) - n_e(x) + n_p(x)\right]dx \tag{2.59}$$

The capacitance can be obtained as a derivative of this charge with respect to gate voltage $C(V_G) = \frac{\partial Q}{\partial V_G}$.

This capacitance-voltage (C-V) characteristic is related to the low frequency or quasi-static gate-body C-V characteristics, if all the carriers present in the structure are included in the calculation. Such Poisson-Schrodinger calculations are especially useful for extraction of structural information for devices with very thin oxide, Si cap and SiGe channel layers. This approach can provide accurate results when other methods are unavailable.

Another important application of Poisson-Schrodinger simulation is to calculation the probability of different tunnelling processes in semiconductor heterostructure. It can be used to estimate the leakage current through the oxide layer and to explain low frequency noise due to trapping-detrapping processes. Also the probability of direct tunnelling through the drain barrier can be calculated, and short channel effects can be explained.

Number of commercial and noncommercial 1-D Schrodinger-Poisson solvers is available at the moment. Most known noncommercial solvers are G. Snider solver [123, 44, 45], *SHRED* [46], *SimWindows* [47]. Commercial solvers are included now into *Taurus Device* from Avant! [48] and *Atlas* from Silvaco [49] with some limitations. All of them have very useful and mostly completed material databases and comparable numerical schemes. Unfortunately, most solvers have disadvantages, such as limitations in mesh generation, unstability of numerical algorithms, limited number of calculated wavefunctions and limitations of material parameters modification. So, it should be thoroughly adapted to simulations. Author of this thesis partially realize own version of 1-D Schrodinger-Poisson code, which was used together with G. Snider code [123] during the C-V characteristics simulation.

2.3.2 Main aspects of drift diffusion modelling

The MOSFET current-voltage (I-V) characteristics can be simulated in terms of several transport models. One of them, the drift diffusion transport model is described here. The electrostatic potential is related to the charge density according to the Poisson equation:

$$\vec{\nabla}\left(\varepsilon_s\left(\vec{x}\right)\vec{\nabla}\right)\phi\left(\vec{x}\right)=\frac{-q\left[N_d\left(\vec{x}\right)-N_a\left(\vec{x}\right)-n\left(\vec{x}\right)+p\left(\vec{x}\right)\right]}{\varepsilon_0} \tag{2.60}$$

Continuity equations for electrons and holes have the following form:

$$\begin{aligned}\frac{\partial n}{\partial t}&=\frac{1}{q}\vec{\nabla}\cdot\vec{J}_n-U_n\\ \frac{\partial p}{\partial t}&=\frac{-1}{q}\vec{\nabla}\cdot\vec{J}_p-U_p\end{aligned} \tag{2.61}$$

Here $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities, $U_n=qD_n\vec{\nabla}n$ and $U_p=-qD_p\vec{\nabla}p$ are the electron and hole net recombination rates. D_n and D_p are the diffusion coefficients for electrons and holes. In terms of classical (Boltzmann) transport theory:

$$\begin{aligned} \vec{J_n} &= -q\mu_n n\vec{\nabla}\phi_n \\ \vec{J_p} &= -q\mu_p p\vec{\nabla}\phi_p \end{aligned} \tag{2.62}$$

where μ_n, μ_p are the mobility of carriers, and φ_n, φ_p are the electrostatic potentials. Equation (2.61) can be rewritten as :

$$\begin{aligned} \vec{J_n} &= -q\mu_n n\vec{E}_n + qD_n\vec{\nabla}n \\ \vec{J_p} &= -q\mu_p p\vec{E}_p - qD_p\vec{\nabla}p \end{aligned} , \tag{2.63}$$

where $\vec{E}_n$ and $\vec{E}_p$ is electric field for electron and holes ($\vec{E}_n = \vec{E}_p = \vec{E} = -\vec{\nabla}\phi$), n and p is electron and hole concentration, which can be written as:

$$n = n_i \exp\left(\frac{q\,(V-\phi_n)}{k_b T}\right) p = n_i \exp\left(\frac{q\,(V-\phi_p)}{k_b T}\right) \tag{2.64}$$

Equations (2.60), (2.62) and (2.63) together make up a self-consistent system of equations to model the charge density distribution and currents as a function of applied voltage V. Since, the perturbation of electron distribution function from their equilibrium states is weak one can use the relaxation time approximation of the Boltzmann equation, adding the following electric field dependencies of mobility $\mu\left(\vec{E}\right)$ and diffusion coefficient $D\left(\vec{E}\right)$:

$$\mu = \mu\left(\vec{E}\right) = \frac{q\tau}{m^*} D = D\left(\vec{E}\right) = \frac{\mu k_b T}{q} \tag{2.65}$$

where τ is the total scattering time and is given by Mathiessen's rule (2.16)

So, we can simulate the I-V characteristics of our devices by calibrating the $\mu\left(\vec{E}\right)$ dependence and defining the structure of the investigated devices. As well, we can try to solve the inverse problem and describe the scattering mechanisms in our heterostructure by fitting the measured I-V characteristics.

Numbers of commercial and noncommercial solvers, which use drift diffusion approximation to simulate device characteristics, are available at the moment. Most known commercial solvers are *Medici* or *Taurus Device* from Avant! [40, 48] and *Atlas* from Silvaco [49]. All of them have very useful and mostly completed material databases and comparable numerical schemes. Uncommercial solvers such as P-spice [50] or NextNano3 [51] are also available. However, it should be thoroughly adapted for simulations of metamorphic

p-$Si_{1-x}Ge_x$ MOSFETs with high Ge content due to relatively new material used for its fabrication.

2.4 Electrical noise

Electrical noise is mostly defined, as any unwanted electromagnetic energy that degrades the quality of signals and data in electrical devices and circuits. Noise occurs in both digital and analog systems.

Current or voltage noise can be defined as any fluctuation of current or voltage respectively from its average value, which is associated with pure signal. So noise can be represented as a function of time $\delta I(t) = I(t) - I_0(t)$ for current noise and $\delta V(t) = V(t) - V_0(t)$ for voltage noise, where $I_0(t)$ and $V_0(t)$ is current and voltage values expected without noise and $I(t)$ and $V(t)$ real measured values with noise. The averaged value of noise fluctuations on time is equal zero and $\langle I(t)\rangle = I_0(t)$, $\langle V(t)\rangle = V_0(t)$. The average value of fluctuations power on time are not equal to zero: $\left\langle \delta I^2(t)\right\rangle = \left\langle (I(t) - I_0(t))^2\right\rangle = \left\langle I^2(t)\right\rangle$ - $\langle I(t)\rangle^2$

2.4.1 Noise Power Spectral Density (NPSD)

If we like to investigate spectral dependence of electrical noise, the autocorrelation function $c(s)$ is more useful to describe of how quickly the fluctuation varies with time:

$$c(s) = \langle \delta I(t)\, \delta I(t+s)\rangle \tag{2.66}$$

The power spectral density (PSD) of variable $X(t)$ defined by the Wiener-Khintchine theorem:

$$S_X(f) = 4\int_0^\infty \langle X(t) X(t+s)\rangle \cos\left(2\pi f^{-1} s\right) ds \tag{2.67}$$

So, the noise PSD can be obtained from autocorrelation function with the help of Fourier transform:

$$S_I(f) = 4\int_0^\infty c(s)\cos\left(2\pi f^{-1} s\right) ds = 4F[c(s)] \tag{2.68}$$

2.4.2 Thermal Noise (also known as Johnson noise)

Thermal noise is the result of the thermal movement of the charge carriers. This movement causes a statistically fluctuating signal in a conductor, with the result a noise voltage on the outside connections and fluctuation of current through conductor. According to Nyquist the formula for this noise is:

$$S_V(f) = 4k_B T R \tag{2.69}$$

$$S_I(f) = \frac{4k_B T}{R} \tag{2.70}$$

where k_B is Boltzman constant, T is temperature (K), and R is conductor's resistance value (Ω).

PSD of thermal noise is independent on frequency. That is why this type of noise also called "white noise".

2.4.3 Shot Noise

The noise caused by random fluctuations in the motion of charge carriers in a conductor originates in quantisation of charge non-continuous current is named "*shot noise*" [52]. Very often in electronic devices or circuits we got charge carriers which will cross a some voltage threshold (for example pn-junction) independent of each other. The charge carriers pass the threshold with temporal fluctuations (mathematically speaking: a Poisson process). The PSD of current noise due to this process described as:

$$S_I(f) = 2qI \tag{2.71}$$

where q is the carrier charge, I is the mean current through device.

The expression (2.71) is only valid when the charge carriers move completely independent of each other. This is however not always the case. For unsaturated thermal diode the current is limited by the charge in the diode. This causes a feedback mechanism. The number of electrons that reaches the anode is correlated with the charge in the diode on

that moment and because of that with the momentarily emission. So, this current fluctuations across the threshold will be limited. This mechanism is described by a factor Γ^2 (space charge smoothing factor). For tubes under working conditions factor Γ^2 has a value between 0.15 and 0.5. The formula for this case is:

$$S_I(f) = 2qI\Gamma^2 \tag{2.72}$$

2.4.4 1/f Noise (also known as flicker or excess noise)

In a lot of electrical parts the noise has a component which is frequency dependent. This noise contribution is caused by statistical fluctuations in the conduction mechanism. In a composite resistor for instance the contact resistance between the individual particles is not constant. In semiconductors besides mass-effects (fluctuations in the number of electrons and holes in the conducting band) also generation and recombination effects have their contribution. This noise is known under the names: Current noise, 1/f noise, flicker noise and excess noise. The power spectrum of this noise is usually inverse proportional to frequency.

2.4.5 Phase noise

In signal sources such as crystal oscillator, rapid, short-term, random fluctuations in the phase of a wave, caused by time-domain instabilities, are named "*phase noise*" [52]. As performance of such systems as communications and radar advance, the spectral purity of the crystal oscillators, which they employ, is increasingly critical.

Phase noise, in decibels relative to carrier power (dBc) on a 1-Hz bandwidth, is given by $10\log((S_\Phi(f)/2))$ where $S_\Phi(f)$ is the spectral density of phase fluctuations. A plot of responses at various offsets from the desired signal is usually comprised of three distinct slopes corresponding to three primary noise generating mechanisms in the oscillator, as shown in Fig 2.12 [53]. Noise relatively close to the carrier (Region A) is called "*flicker FM noise*"; its magnitude is determined primarily by the quality of the crystal. Its PSD is is close to $1/f^3$ or $1/f^5$. Noise in region A could be generated due to filtering of $1/f$ noise from internal oscillator sources. High frequency crystals result in high close-in noise

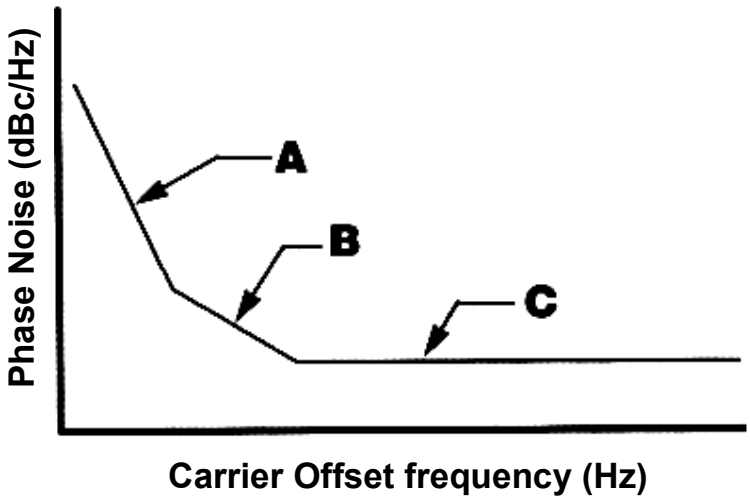

Figure 2.12: The residual phase noise versus carrier offset frequency.

because of their wide bandwidths. Noise in Region B of Fig 2.12, called $1/f$ noise, is caused by semiconductor activity. Region C of Fig 2.12 is called white noise or broadband noise.

So, low frequency $1/f$ noise in oscillator components such as individual MOSFETs, semiconductor diodes or resistors has very important influence on phase noise of final device.

2.4.6 $1/f$ Noise in MOSFETs

The noise behaviour of CMOS devices is dominated primarily by two noise sources: thermal noise and flicker $(1/f)$ noise. Other sources that are sometimes present in the noise spectrum are shot noise, generation/recombination noise, and "popcorn" noise. Of these sources, thermal noise and shot noise are physically fundamental to the operation of the device and are always present. Depend on level of each noise component at operated device region some noise sources can be neglected. The quality of the manufactured MOSFET determines the level of $1/f$ noise (the average number of defects in the bulk silicon, in the gate oxide, and in the various interfaces), generation/recombination (GR) noise (order of trap's placement inhomogeneity in material, isolated deep energy levels in bandgap) and random telegraph signal (RTS) noise (individual traps in small area devices). It is probable that flicker noise appears through both quality-dependent and fundamental noise processes.

So, the $1/f$ noise is very important itself as a factor limiting device performance at high frequencies (subsection 2.4.5) and as a useful parameter for device characterisation. That is

why, it is very important to determine main sources of $1/f$ noise in investigated MOSFETs. There are several possible sources of $1/f$ noise in MOSFET device. It could be the carrier number fluctuations (CNF) in device channel due to modulation of carrier number by any random processes in gate area, the correlated mobility fluctuations (CMF) in channel area due to modulation of carrier mobility in channel during the same processes. Also it could be the CNF or the Hooge mobility fluctuations (HMF) in channel area due to processes in channel area. The contact areas also can introduce noise in MOSFET drain current due to the contact access source and drain resistance fluctuations (SDRF), which can be associated with CNF or HMF in source and drain area. Also, it could be any other sources as leakage current fluctuations or external noise, which modulate drain current. Each of this sources can be more or less important depend on conditions of device operated. The main sources can be different even for one device at different gate, drain and body voltages, at different temperatures and so on. So, the components of $1/f$ noise should be thoroughly investigated in order to determine of $1/f$ noise origin at each operation region.

2.4.7 Carrier number fluctuations (CNF)

In the classical carrier number fluctuation scheme, the fluctuations in the drain current stem from the fluctuations of the inversion charge nearby the Si/SiO_2 interface, arising from the variations of the interfacial oxide charge after dynamic trapping-detrapping of free carriers into slow oxide traps. This interface charge fluctuations δQ_{it} can be equivalently equated to a flat band voltage variation:

$$\delta V_{fb} = -\delta Q_{it} / (WLC_{OX}) \tag{2.73}$$

The drain current fluctuations due to carrier number fluctuations then read [120, 55]:

$$\delta I_D = -g_m \delta V_{fb} = g_m \delta Q_{it} / (WLC_{OX}) \tag{2.74}$$

where g_m is transconductance.

Other possible course of flat band voltage variations is oxide leakage current fluctuations. The oxide resistance can fluctuate and voltage fluctuations on this resistor can be also amplified by MOSFET.

Capacitance fluctuations due to mechanical vibrations of material could be also equated to a flat band voltage variation, as it will be shown in subsection 2.4.7.4.

2.4.7.1 McWhorter Model

McWhorter number fluctuation (δn) theory states that flicker noise is generated by fluctuations in the number of carriers due to charge trapping in surface states. McWhorter obtained the necessary $1/f$ spectrum by assuming that the time constant τ of the surface states varied with a $1/\tau$ distribution [56]. Christensson *et al* [57, 58] were the first to apply McWhorter theory to MOSFETs, using the assumption that the necessary time constants are caused by the tunneling of carriers from the channel into traps located inside the oxide.

A number of other applications of the McWhorter theory to MOSFETs have been done. Das and Moore [59] reviewed and compared these theories and found that the basic assumptions behind any explanation affects the interpretation of experimental results. They said, "theoretical calculations of the MOSFET drain noise current have been performed by many investigators, which have led to different results, mainly due to the difference in the method of attack and nature of assumptions."

Reimbold [60] developed McWhorter model further, taking into account all the capacitive components of the small-signal equivalent circuit, so as to account for all transistor operating regimes. This development was done to fit Reimbold's measurements in weak inversion. Ghibaudo [61] and other authors [62, 131] showed a shortcut through Reimbold's work and came up with the same result, where the spectral density of the drain current is

$$S_{V_{fb}} = \frac{q^2 k_B T N_{st}}{W L C_{ox}^2 f^\gamma} = \frac{q^2 k_B T \lambda N_t}{W L C_{ox}^2 f^\gamma} \tag{2.75}$$

where f is the frequency, γ is the characteristic exponent close to unity, $k_B T$ is the thermal energy, N_{st} is a density of traps near the semiconductor/oxide interface, λ is the tunnel attenuation distance into oxide ($\tau(x) = \tau_o \exp(x/\lambda)$), and N_t is the volumetric trap density in the oxide.

Parameter λ is typically taken to equal 0.1 nm for electrons and 0.1-0.08 nm for holes for Si/SiO_2 interface. It can be approximated as:

$$\lambda = \sqrt{\frac{2\hbar^2}{m^* \Phi_B}} \tag{2.76}$$

where m^* is the carrier effective mass in the oxide and Φ_B is the tunnelling barrier for carrier.

Expressions (2.75) and (2.76) are correct for Si MOSFETs with Si/SiO_2 interface and electric field in oxide less than 3 MV/cm [131]. These expressions for SiGe p-MOSFETs should be correct in the case when carriers tunneling to oxide from Si cap and carriers sheet density in Si cap much higher than oxide trap density involved in LF noise generation. If carrier tunneling to traps in oxide or Si cap from SiGe channel or field in oxide is much higher than 3 MV/cm, then we should solve full tunnelling problem:

$$S_{V_{fb}} = \frac{q^2}{WLC_{ox}^2} \int_0^{dox} \int_{E_V}^{E_C} \frac{N_t(x,E)\,\tau(x)}{1+\omega^2\tau^2(x)} f_T(E)\,(1-f_T(E))\,f_c(E)\,dxdE \tag{2.77}$$

where f_T is the probability that trap is filled, and f_c is the probability of presence of carrier available for tunnelling near the interface. Parameter λ can also be not a constant, and becomes a function of x for very high fields.

2.4.7.2 Thermal Activation Model

Thermal activation model as well as McWhorter theory describe the number fluctuations in active area (channel) due to interface trap charge fluctuations and following flat band voltage fluctuations. However, interface charge fluctuates due to thermally activated process of traps occupancy at energy levels below the Fermi level. $1/f$ noise spectrum can be obtained by assuming the traps density distribution is uniformly by energy and traps are placed directly at interface against uniform distribution by distance from interface inside gate dielectric in McWhorter model.

For a thermally activated trapping process [64], the trapping probability decreases exponentially with the cross-section activation energy E_a, such that the flat band voltage spectral density reads [65]:

$$S_{V_{fb}} = \frac{q^2 k_B^2 T^2 N_{it}}{WLC_{ox}^2 f^\gamma \Delta E_a} \tag{2.78}$$

where the ΔE_a is the activation energy dispersion amplitude and N_{it} is the oxide surface state density.

2.4.7.3 Flat band voltage fluctuations due to gate leakage current

The mobile charge in oxide provides gate leakage current, which can introduce additional noise to MOSFET drain current. Vandamme *et al* discussed the influence of base and emitter series resistance on collector noise in BJT [121]. Similar analysis can be carried out for MOSFETs to investigate influence of gate leakage current on drain current noise. Equivalent scheme of MOSFET under test with noise source due to gate leakage is shown on Fig. 2.13. Drain current noise for such case can be written as:

$$\frac{S_{I_D}}{I_D^2} = \left(\frac{S_{0I_D}}{I_D^2}\right) + \left(\frac{g_m^2}{I_D^2}\right) S_{V_{fb}^{leak}} \tag{2.79}$$

where $S_{V_{fb}^{leak}}$ is the PSD of flat band voltage fluctuations due to gate leakage, g_m is MOSFET transconductance , and S_{0I_D} is drain current noise from any other sources.

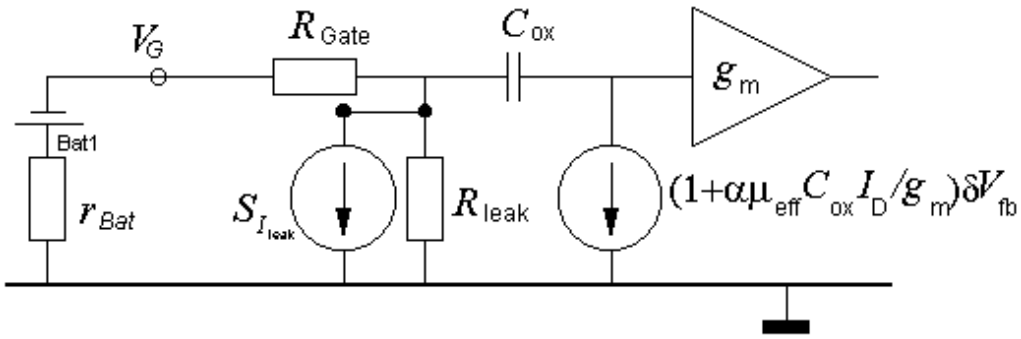

Figure 2.13: Equivalent scheme of MOSFET under test with noise source $S_{I_{leak}}$ due to gate leakage current.

The $S_{V_{fb}^{leak}}$ can be rewritten as:

$$S_{V_{fb}^{leak}} = S_{I_{leak}} \left(\frac{1}{R_{leak}} + \frac{1}{R_{Gate} + r_{bat}}\right)^{-2} \tag{2.80}$$

where R_{Gate} is the gate access resistance, R_{leack} is the gate leakage resistance, r_{bat} is the gate bias source internal resistance, $S_{I_{leak}}$ is the PSD of leakage current I_{leak} fluctuations (the I_{leak} is equal to the gate current I_G).

Pavelka *et al* shown that $1/f$ noise in capacitors are proportional to square of leakage current through capacitor [67]. This is in very good agreement with Hooge mobility fluctuations model, which will be described in section 2.4.9. The source of leakage current fluctuations is the leakage resistance value fluctuations in term of this model:

$$S_{R_{leak}} = \alpha_{H\_oxide} \frac{R_{leak}^2}{f N_{oxide}} \sim \frac{R_{leak}^3}{f}, \tag{2.81}$$

$$\frac{S_{I_{leak}}}{I_{leak}^2} = \frac{S_{R_{leak}}}{R_{leak}^2} = \beta \frac{R_{leak}}{f}, \tag{2.82}$$

So, PSD of leakage current fluctuations depend on R_{Gate} and R_{leack} :

$$S_{I_{leak}} = \frac{S_{R_{leak}}}{R_{leak}^2} I_{leak}^2 = \frac{S_{R_{leak}}}{R_{leak}^2} \left(\frac{V_G}{R_{Gate} + R_{leak}} \right)^2 = \beta \frac{V_G^2}{f} \frac{R_{leak}}{(R_{Gate} + R_{leak})^2}, \tag{2.83}$$

Finally, the $S_{V_{fb}^{leak}}$ can be written as a function of the R_{Gate}, R_{leack}, and r_{bat} :

$$S_{V_{fb}^{leak}} = S_{I_{leak}} \left(\frac{1}{R_{leak}} + \frac{1}{R_{Gate} + r_{bat}} \right)^{-2} = \beta \frac{V_G^2}{f} \frac{R_{leak}^3 (R_{Gate} + r_{bat})^2}{(R_{leak} + R_{Gate} + r_{bat})^2 (R_{Gate} + R_{leak})^2} \tag{2.84}$$

If $r_{bat} \ll R_{Gate}$ and R_{leak} than expression can be rewritten as

$$S_{V_{fb}^{leak}} = S_{I_{leak}} \left(\frac{1}{R_{leak}} + \frac{1}{R_{Gate}} \right)^{-2} = \beta \frac{V_G^2}{f} \frac{R_{leak}^3 R_{Gate}^2}{(R_{leak} + R_{Gate})^4} \tag{2.85}$$

If $R_{Gate} \ll R_{leak}$, then

$$S_{V_{fb}^{leak}} = S_{I_{leak}} \frac{1}{R_{leak}^{-2}} = \beta \frac{V_G^2}{f} \frac{R_{Gate}^2}{R_{leak}} \tag{2.86}$$

If device is very leaky and $R_{Gate} \approx R_{leak}$ then

$$S_{V_{fb}^{leak}} \approx S_{I_{leak}} \frac{4}{R_{leak}^{-2}} \approx \frac{\beta}{16} \frac{V_G^2}{f} R_{leak} \tag{2.87}$$

So, the gate leakage current can generate additional $1/f$ noise in MOSFETs, which is significantly depend on gate and oxide resistance and mechanism of this leakage. In case of very leaky device (2.87) the $1/f$ noise component introduced by leakage can decreased with

gate leakage increased due to gate leakage resistance decreased. So, devices with high gate leakage can be even less noisy in drain current then devices with low gate leakage.

No direct publications on influence of gate current leakage on drain current noise are available at the moment for SiGe MOSFETs and also for MOSFET devices at all. Some data are available on manufacturers application notes in order to chose right OPA or MOSFET for final application [122].

2.4.7.4 Oxide capacitance fluctuations

The capacitance of gate dielectric layer $C_{ox} = \varepsilon_{ox}/d_{ox}$ can fluctuate itself due to mechanical vibrations. These capacitance fluctuations δC_{ox} can be equated also to a flat band voltage variation:

$$\delta V_{fb} = -\delta C_{OX}\left(Q\left(V_G\right) + Q_{it}\right)/\left(WLC_{OX}^2\right) \approx -\delta C_{OX}\left(V_G - V_{fb}\right)/C_{OX} \tag{2.88}$$

The mechanical noise (fluctuations of oxide thickness δd_{ox}) could be cause of such capacitance fluctuations.

$$\delta C_{OX} = -\delta d_{OX}\varepsilon_{OX}/d_{OX}^2 = \left(\delta d_{OX}/d_{OX}\right)C_{OX} \tag{2.89}$$

$$\delta V_{fb} = \delta d_{OX}\left(Q\left(V_G\right) + Q_{it}\right)/\left(WL\varepsilon_{OX}\right) \tag{2.90}$$

The mechanical noise can also follow from fluctuations of sample temperature δT :

$$\delta d_{OX} = \delta T\,\alpha_{OX} d_{OX} \tag{2.91}$$

where α_{ox} coefficient of temperature expansion for gate dielectric ($\alpha_{ox} \approx 9.6 \times 10^{-6}\mathrm{K}^{-1}$ for SiO_2 [3]). So, the sample temperature fluctuations can be source of capacitance and flat band voltage fluctuations:

$$\delta C_{OX} = \delta T\,\alpha_{OX}\varepsilon_{OX}/d_{OX} = -\delta T\,\alpha_{OX} C_{OX} \tag{2.92}$$

$$\delta V_{fb} = \delta T \alpha_{OX} \left(Q\left(V_G\right) + Q_{it} \right) \big/ \left(WLC_{OX} \right) \tag{2.93}$$

Finally, PSD of flat band voltage fluctuations $S_{V_{fb}^{cap}}$ due to capacitance variation can be written as:

$$S_{V_{fb}^{cap}} = S_T \alpha_{OX}^2 \left(Q\left(V_G\right) + Q_{it} \right)^2 \left(WLC_{OX} \right)^{-2} \tag{2.94}$$

where the S_T is the PSD of sample temperature fluctuations (K^2/Hz).

There are no publications on influence of capacitance fluctuations on drain current noise of MOSFETs. However, estimation for p-MOSFET with carrier sheet density $\sim 1 \times 10^{12}$ cm^{-2}, oxide capacitance $\sim$300-400 nFcm^{-2}, and gate area WL = 1×50 μm^2 give us $S_{V_{fb}^{cap}} \approx S_T \times 2.5 \cdot 10^{-11}$ V^{2}K^{-2}. This value is comparable with published results for extracted $S_{V_{fb}}$ or directly recalculated equivalent input gate voltage noise S_{V_G} [131, 69, 70] at $S_T \approx 1 K^2/Hz$.

2.4.8 Correlated mobility fluctuations (CMF)

Interface charge fluctuations δQ_{it} due to tunneling or thermal activation processes can be equivalently equated to a flat band voltage variation (equation 2.74) as it shown in [126], which is equal interface potential variation averaged on gate area. So, interface charge fluctuations are following carrier number fluctuations due to flat band voltage variation. However, such charge fluctuations are inhomogeneous on area without time averaging. Hence, carriers mobility will be fluctuate as well due to variation of interface charge distribution. Importance of these correlated carrier mobility fluctuations (CMF) was shown by Surya [72] and many other authors.

Mechanism of CMF is Coulomb scattering. Mobility change $\delta \mu_{eff}$ due to the modulation of the scattering rate induced by the interface charge fluctuations can be written as:

$$\frac{\delta \mu_{eff}}{\mu_{eff}} = \alpha \mu_{eff} \delta Q_{it} \tag{2.95}$$

where α is the Coulomb scattering coefficient, μ_{eff} is the effective mobility. Equation (2.95) taking to account screening of carriers by part of carriers, which is closer to the

interface than others. Coulomb scattering coefficient is equal to $\alpha \approx 10^4$ VsC^{-1} for electrons and to $\alpha \approx 10^5$ VsC^{-1} for holes in the case of simple semiconductor/oxide interface, which corresponds to conventional MOS structure with surface channel. In complicate heterostructures like buried channel SiGe MOSFETs equation (2.95) already has not describe scattering process correctly. However, it can be used with assumption that α is depending on distance between main carriers and interface.

The PSD of drain current S_{I_D} included CMF together with CNF components can be written from (2.74) and (2.95) as:

$$\frac{S_{I_D}}{I_D^2} = \left(1 + \alpha\mu_{eff} C_{OX} I_D / g_m\right) \left(g_m / I_D\right)^2 S_{V_{fb}} \tag{2.96}$$

2.4.9 Hooge mobility fluctuations (HMF)

In his paper "1/f noise is no surface effect", F. N. Hooge [73] proposed that 1/f noise is essentially a bulk phenomenon. Working with metal films [74], he championed an empirical relation for 1/f noise in terms of resistance fluctuations, where the spectral density of the resistance is

$$\frac{S_R}{R^2} = \alpha_H \frac{1}{fN} \approx \alpha_H \mu \frac{R}{f \cdot L} \tag{2.97}$$

where N is the total number of free carriers in the bulk, and α_H is known as "Hooge's constant" an empirical parameter with value about 2×10^{-3}. This equation fit his data for metal films very well. Based on these results [75], he said "Investigations of noise... proved that the fluctuations in the conductivity are due to fluctuations in mobility and not in the number of charge carriers." Hooge summarised experimental support for his mobility fluctuation ($\Delta\mu$) theory in [76] and some theoretical support (a development of a phonon scattering theory) was provided by Jindal and van der Ziel [77].

2.4.9.1 Source-Drain resistance fluctuations

The source-drain resistance fluctuations (SDRF) have its origin in Hooge mobility fluctuations and can be very important in strong inversion [126, 78, 79]. The PSD of SDRF described by expression:

$$S_{R_{SD}} = \alpha_{H\_SD}\frac{R_{SD}^2}{fN_{SD}} = \alpha_{H\_SD}\mu_{SD}\frac{|e|R_{SD}^3}{L_{SD}^2 f} \sim \frac{R_{SD}^3}{f} \tag{2.98}$$

where α_{H_SD} is Hooge parameter for source and drain material (heavily doped semiconductor), N_{SD} is total number of carriers in source and drain area, μ_{SD} is mobility of source and drain material, R_{SD} is total source and drain access resistance and L_{SD} is effective length of contacts area. So, the drain current noise due to the SDRF is dependent only on current through contact areas and source and drain resistance can be easy extracted from measured data.

Hooge and other authors [76] shown that Hooge parameter is very lightly varied from one material to another and lightly depend on such material quality properties as concentration of defects. Jevtic *et al* [134] and late Makoviychuk *et al* [81] propose to use Hooge parameter multiplied on carriers mobility as more useful parameter to characterise quality of material. So, if we suggest that product of Hooge parameter and mobility of carriers in contact area $\alpha_{H\_SD} \times \mu_{SD}$ is very similar for source and drain areas of MOSFETs fabricated by similar technologies and shape of contact areas is the same or very similar, then source and drain access resistance can be extracted from noise data for each investigated device. This suggestion is very important for individual device characterisation.

2.4.9.2 Off-current noise

The off-current flow through very high resistive areas in heterostructure and is uncontrollable by gate voltage. So, off-current fluctuations can have frequency independent shot noise component and also $1/f$ noise component. Source of $1/f$ noise component is not clearly understandable. Its origin can be Hooge mobility fluctuations or trapping-detrapping processes in areas where current flow. However, off-current $1/f$ noise dependence on current is well described by Hooge empirical relation (2.97).

2.4.9.3 Noise of various leakage currents

The various leakage currents in MOSFET can be source of extra noise in drain and gate current. First of all, the leakage currents introduce shot or thermal noise depend on leakage conductivity. Also, the leakage currents are source of $1/f$ noise, which can be described

by Hooge relation [76] for material, where leakage current flows. Gate leakage current influence on gate current noise and drain current noise is analysed thoroughly in subsection 2.4.7.3. Source to drain and substrate to drain leakage currents are gate uncontrollable. So, they can introduce $1/f$ noise component, which is gate dielectric and channel material quality independent, to drain current noise. If leakage current $1/f$ noise is small relatively to channel current noise, then the drain current noise can be significantly reduced as leakage current increased. This fact can explain, for example, well known drain current noise reduction for dynamical threshold MOSFETs [82, 83, 84], where substrate biased the same voltage as a gate.

2.4.9.4 Hooge mobility fluctuations in MOSFET channel

Channel semiconductor can also introduce noise in drain current due to mobility fluctuations. The PSD of this noise can be described with the help of Hooge relation (2.97).

However, total carriers concentration and mobility in MOSFET in comparison with bulk material depends on distance from oxide/semiconductor interface and gate voltage. So, mobility in expression (2.97) should be changed to MOSFET effective mobility:

$$\frac{S_{I_D^{HMF}}}{I_D^2} = \alpha_H \frac{1}{Nf} \approx \alpha_H \mu_{eff} \frac{V_D}{I_D L f} \tag{2.99}$$

2.4.9.5 Hooge mobility fluctuations and material quality

Hooge and Vandamme [75] derived the following relation between Hooge parameter α_H used in relation (2.97) and mobility μ:

$$\alpha_H = \alpha_H^{'} \left(\frac{\mu}{\mu_{lattice}} \right)^2 \tag{2.100}$$

where μ is the mobility, μ_L is the mobility that would be found if only lattice scattering was present, and $\alpha_H^{'} \approx 2 \times 10^{-3}$.

The Hooge parameter $\alpha_H = \alpha_H^{'}$ found if there is only lattice scattering. The value of the factor depends on the quantity of free carrier concentration in the sample material and its value obeys the relation $10^{-8} \leq \alpha_H \geq 10^{-3}$ [85]

Damaging the crystal lattice increases Hooge parameter α_H. If we consider all values reported, we found values α_H in very wide range 10^{-8}-10^{2} [81]. The values, which is higher then maximum predictable value 2×10^{-3} are can not be explained by equation (2.100). For example α_H value 2×10^{-2} was measured [86] for strongly inhomogeneous materials like heavily doped poly-Si or poly-SiGe. Chen at al [86] shown that relation (2.100) is unsuitable for description of strongly inhomogeneous materials. Relation (2.100) should be changed to relation:

$$\alpha_H = \gamma^2 \alpha_H^{'} \left(\frac{\mu}{\mu_{lattice}} \right)^2 \tag{2.101}$$

where γ^2 is the depends on the dopant concentration and, thus, depends on mobility. It is clear that in polycrystalline materials the lattice scattering model does not predict that Hooge parameter α_H is proportional to the square of the Hall mobility.

One can conclude from wide range of α_H variation that α_H obviously strongly depend on technological conditions of material growth, technique, which is used to make contacts to material, etc. So, we can use parameter α_H or more suitable parameter $\alpha_H \times \mu$, as it was shown by Makoviychuk *et al* [81], for rapid control of semiconductor material quality.

2.4.10 Random Telegraph Signal (RTS) noise

Random-telegraph-signal (RTS) noise, sometimes called "burst noise" or "popcorn noise", is a discrete modulation of the channel current caused by the capture and emission of a channel carrier. The histogram of the drain current amplitudes is no longer Gaussian for RTS noise. It has two maximums with distance ΔI_D between them. This distance ΔI_D is the average drain current RTS amplitude. The average values of the high and low level time constants represent for an acceptor like trap, the capture time τ_c and the emission time τ_e respectively. The PSD of RTS noise is very similar to generation-recombination noise:

$$S_{I_D^{GR}} = 4A\Delta I_D^2 \frac{\tau}{1+\omega^2\tau^2} \tag{2.102}$$

where $\tau = (1/\tau_c + 1/\tau_e)^{-1}$ is an effective time constant, $A = \tau / (\tau_c + \tau_e) = f_t(1-f_t)$ is the space mark ratio, $\omega = 2\pi f_t$ is the angular frequency and f_t is the trap occupancy factor,

$f_t = 1/(1+\exp((E_t - E_f)/k_BT))$ with E_t being the trap energy and E_f the Fermi level position.

2.4.11 Generation – Recombination (GR) Noise

In addition to the flicker noise caused by equally distributed traps in the oxide, trapping centres distributed inhomogeneously by distance or by energy levels in the oxide or in the bulk of the device can cause generation-recombination (GR) noise. The trapping of carriers causes fluctuations in the number of carriers, and thus fluctuation in the resistance. The spectral density of the resistance fluctuation is [87]

$$S_{I_D^{GR}} = 4\frac{\sigma^2}{N^2} I_D^2 \frac{\tau}{1+\omega^2\tau^2} \tag{2.103}$$

where τ is the trap relaxation time, $\omega = 2\pi f$, N is total number of carriers, and the variance σ^2 is given by:

$$\frac{1}{\sigma^2} = \frac{1}{N} + \frac{1}{N_O} + \frac{1}{N_E} \tag{2.104}$$

where N_O is the number of occupied traps and N_E is the number of empty traps. If there is more than one kind of trap, the equations are significantly more complicated. Note that GR noise creates a Lorentzian noise spectrum.

The sources and PSD of GR noise is very similar to sources and PSD of RTS noise. However, when RTS noise describe the trapping-detrapping process on individual traps, GR noise caused by number trapping-detrapping processes averaged on device area. RTS noise can be observed only on small area devices or at low temperatures, when only one or several trapping-detrapping centres could be activated. GR noise points to inhomogenous trap distribution or selected trap energy levels and can be observed on big area devices as well as on small area devices.

Temperature dependence of trap realxation time τ is a powerful tool to characterize traps near Si/SiO_2 interface [88].

2.4.11.1 Nonuniformity traps distribution

Some authors use measured $1/f$ noise on gate bias dependence for MOSFETs to extract trap distribution without any additional analisys [128, 129, 130]. These techniques based directly on McWhorter model (see section 2.4.7.1) for $1/f^{\gamma}$ noise. However, McWhorter model use assumption that traps uniformly distributed in oxide and trap energy levels uniformly distributed by energy to obtain $1/f$ noise. Non uniform distribution of traps by distance or trap energy levels by energy should be manifested as a GR "bumps" on noise spectra, or at least significantly change noise exponent γ. So, if no GR "bumps" on noise spectra and γ close to unity at all gate biases, then the trap concentration could only slightly depends on distance from Si/SiO_2 interface into oxide or interface trap density could only slightly depends on barrier height.

Number of authors [62, 92, 93, 94] show that the shape of the low frequency noise spectrum is strongly dependent on the trap distribution in the oxide. Actually, traps are distributed over space x into the oxide as well as in energy E over the band gap. A complete characterization of traps in (x,E) window is extremely difficult. It is widely accepted that trap states are classified by two distinct groups. The first is 'fast states' with capture cross-sections of about 10^{-16} cm^2, and the second is 'slow states' characterized by capture cross sections much less than 10^{-16} cm^2 [95]. The slow states play a fundamental role in $1/f$ low frequency noise and are due to defect states extended into the oxide layer. Technique, which can be used to extract distribution of traps and traps energy levels from shape of LF noise, are well described in [92].

2.4.11.2 GR and direct tunneling in drain depletion area

High electric field in drain depletion area lead to impact ionisation in this area. Generated electron and hole pairs partially recombinate in drain depletion area. This process becomes apparent as GR noise. Additional current due to generated charge can also short another sources of drain current noise and also it can be additional source of noise. High instability of impact ionisation process at critical V_{DS}, when impact ionisation just start, can be seen in drain current noise as "noise overshoot" due to unstable value of drain current at this bias conditions [96].

2.4.12 Noise in SiGe MOSFETs

Initial low frequency noise (LFN) measurements for $Si_{0.2}Ge_{0.8}$ p-type pseudomorphic hetero-MOSFETs have been reported by Chang *et al* in 1991 [97]. They have associate $1/f$ and GR noise with traps in the Si cap. However, noise spectra was measured just at several gate bias points of intermediate MOSFET operation range and any quantitative model was not presented to explain results. Measured noise for SiGe MOSFET also have not compared with noise for p-Si MOSFETs. The effective trap density extracted from the noise spectra is about three order of magnitude higher than that was found in silicon surface channel MOSFETs.

Lambert *et al* [98] repeated LFN measurements on similar structures p-$Si_{0.2}Ge_{0.8}$ and carried out more thorough analysis with help of Christensson model [99]. Their results show very strong influence of traps in oxide on drain current noise as well as for conventional Si MOSFETs. Influence of traps in Si cap on noise was not also excluded. Referred PSD presented in [98] was higher in comparison with conventional Si MOSFETs at weak inversion.

Okhonin *et al* [100] shown reduced LFN for pseudomorphic p-$Si_{0.75}Ge_{0.25}$ MOSFETs in strong inversion. This behavior has been explained by separation of holes in p-SiGe channel and traps in SiO_2 due to Si cap presence.

Mathew *et al* [101, 102] have published the same results for p-$Si_{0.85}Ge_{0.15}$ and p-$Si_{0.80}Ge_{0.20}$ MOSFETs on sapphire substrates. However, they proposed another reason for observed reduced $1/f$ noise in SiGe FETs: at the same gate overdrive the separation between the quasi-Fermi level of holes and the valence band edge at the Si/SiO_2 interface is higher for SiGe device. It is then believed that the density of "border traps" close to Fermi level and responsible for noise is lower for SiGe FET. This model can be used only with limitation discussed in section 2.4.11.1.

Later, Prest *et al* [130] have considered $1/f$ noise for p-$Si_{0.64}Ge_{0.36}$ MOSFETs in terms of Mathew model. They obtained reduced reffered noise in both weak inversion and strong inversion regions.

Chroboczeck and Ghibaudo [127, 104] reported $1/f$ noise for pseudomorphic p-$Si_{1-x}Ge_x$ MOSFETs with Ge fraction $x = 0.0 - 0.29$. Carrier number fluctuation (CNF) (subsec-

tion 2.4.7) together with correlated mobility fluctuation CMF (subsection 2.4.8) model have been proposed to describe $1/f$ noise in p-type SiGe MOSFETs. Reduced $1/f$ noise in SiGe MOSFETs have been associated with reduced CMF component ($\alpha_{SiGe\_channel} \approx R \times \alpha_{Si\_cap}$, where R = 0.1-02) in noise for SiGe MOSFETs due to increased distance from fluctuating charge distribution in oxide to channel and also due to charge fluctuations screening [127]. They also proposed to take into account Hooge mobility fluctuations in Si cap layer and SiGe channel layer.

Tsuchiya *et al* [105] present LFN results for pseudomorphically grown p-$Si_{1-x}Ge_x$ MOSFETs with Ge fraction x = 0.2, 0.5 and 0.7, however, SiGe channel for p-$Si_{0.5}Ge_{0.5}$ and p-$Si_{0.3}Ge_{0.7}$ MOSFETs can be unstrained (see section 2.1.1 and [5]). Results show reduction of $1/f$ noise for p-$Si_{1-x}Ge_x$ in comparison with p-Si in strong inversion and the same or a little bit increased referred noise for p-$Si_{1-x}Ge_x$ at gate biases, which are close to threshold voltage.

Li and Liao [106, 107] have obtained LFN results for p-$Si_{1-x}Ge_x$ MOSFETs with Ge fraction x = 0.15, 0.3 and 0.5 similar to Chroboczek and Gibaudo results in strong inversion. However, referred noise for some p-$Si_{1-x}Ge_x$ MOSFETs was increased at maximum gate overdrive voltages, which can not easily explained in terms only CNF + CMF model with constant trap density in SiO_2. Li and Liao proposed to use Mathew model [101] due to this reason. Results presented in [107] also show lightly decreased referred noise of p-$Si_{1-x}Ge_x$ MOSFET in subthreshold region in comparison with p-Si MOSFET, which is agreed with Prest *et al* [130] and in contradictionary with Lambert *et al* and Tsuchiya *et al* [98, 105]. So, noise in weak inversion can be well explained only by simple CNF model with oxide trap density strongly dependent on Si/SiO_2 interface quality. Li *et al* [108] also investigate effect of substrate biasing on p-$Si_{1-x}Ge_x$ MOSFETs $1/f$ noise. Referred noise was reduced in subthreshold region and unchanged in strong inversion when substrate potential was lowered.

Lukyanchikova *et al* [109] present comparison of LF-noise pseudomorphic p-SiGe MOSFETs with buried and surface channel, which were fabricated with the help of Si cap anodic oxidation. Referred noise of buried channel MOSFETs was obtained lower than referred noise of surface channel MOSFETs, hovewer, SiO_2/Si and $SiO_2/SiGe$ interfaces could have different quality due to partial SiGe oxidation. Authors also present $1/f$ Hooge mobility

fluctuations for buried p-SiGe channel MOSFETs, however results shown not in whole device operation range and could be associated also with access source-drain resistance as well.

Song *et al* [110] also reported reduced by a factor of 10 noise for p-$Si_{0.8}Ge_{0.2}$ MOSFETs in comparison with p-Si MOSFETs as well as other authors.

Chapter 3

Experiment details and measurement techniques

3.1 Description of samples

Samples of metamorphic p-MOSFETs from 6 different wafers, c2321(a), c2321(b), c2154, k5660, k5888 and k5889 have been fabricated in DaimlerChrysler Research and Technology Center [112]. The wafers have different Ge compositions of SiGe channel and cross section design. Two different technologies were used for fabrication of c2321, c2154 and for fabrication of k5660, k5888, k5889 MOSFET devices.

Graded $Si_{0.7}Ge_{0.3}$ relaxed buffer for c2321(a), c2321(b) and $Si_{0.6}Ge_{0.4}$ relaxed buffer for c2154 were grown by molecular beam epitaxy (MBE) on a high resistivity n-type (100) Si substrate. Wafers c2154 and c2321(a) also contained a 500nm *in situ* 5×10^{17}cm^{-3} Sb doped punch through stopper layer. The compressively strained $Si_{0.3}Ge_{0.7}$ channel (7 nm for c2321 and 9 nm for c2154) was grown on a relaxed $Si_{0.7}Ge_{0.3}$ (c2321) or $Si_{0.6}Ge_{0.4}$ (c2154) buffer and capped by a thin Si layer (7 nm) [111].

The k5660, k5888, k5889 heterostructures were grown on a n^+-Si(100) substrate by low-energy plasma-enhanced chemical vapour deposition (LEPECVD) technique [113]. A specific advantage of this epitaxy technique is the high bandwidth of growth rates for the deposition of SiGe heterostructures ranging from 0.08 to 5 nm/s. Cross sections of the grown wafers before the fabrication process are shown in Fig. 3.1.

Fig. 3.2 shows the structure of a p-type SiGe MOSFETs fabricated from grown wafers.

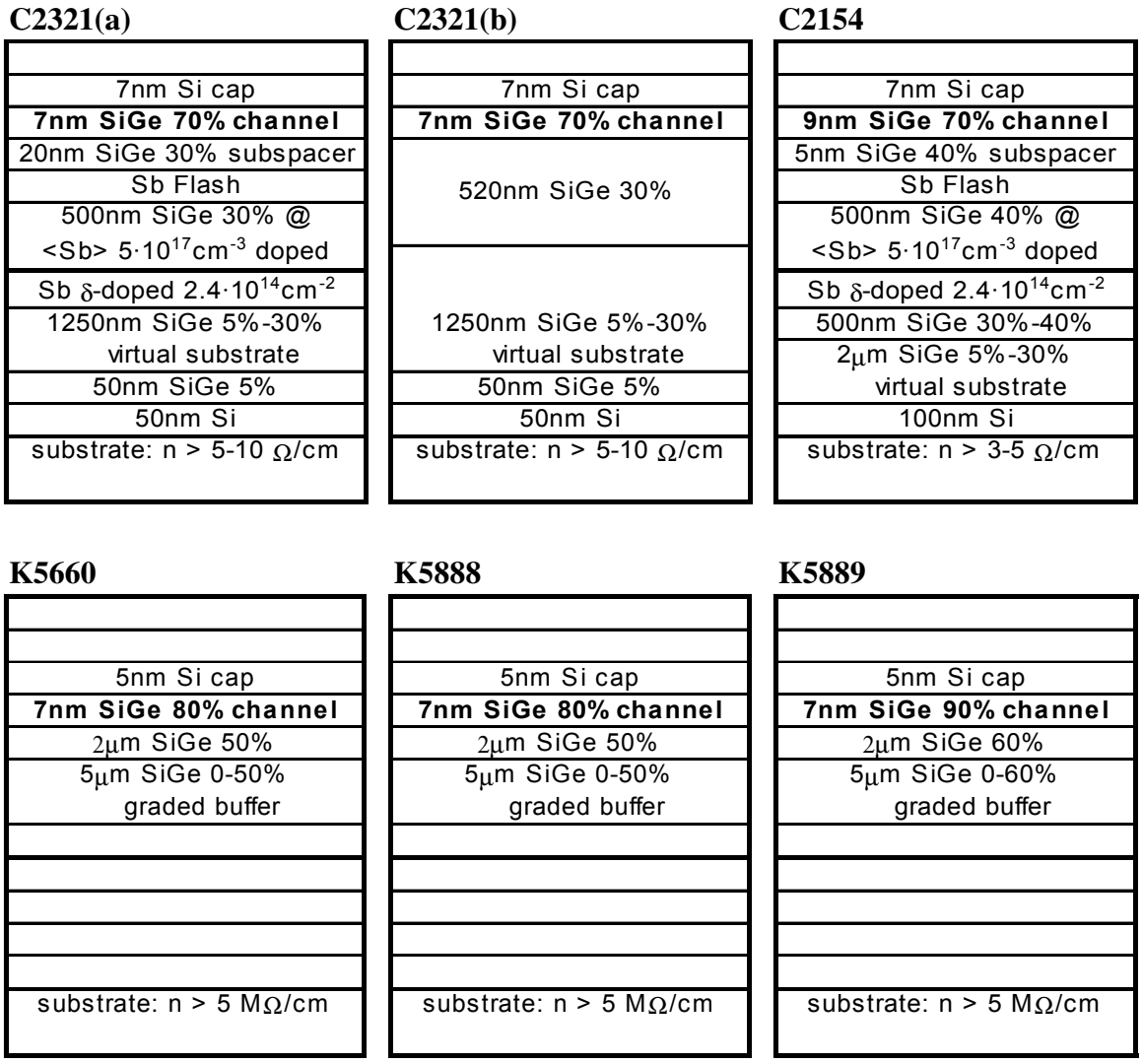

Figure 3.1: Cross sections of the wafers used for MOSFETs fabrication. Wafers with punch through stopper (c2321(a), c2154) and without punch through stopper (c2321(b), k5660, k5888, k5889) are presented.

The 3.5 nm thick Remote PECVD (RPCVD) deposited gate oxide [125] was used for samples c2321(a), c2321(b) and c2154. Ohmic contacts were fabricated by a BF_2^+ implant at 50 keV. Finally, the overlapping Al gate and the contact Au/Pt/Ti metallization were deposited [111].

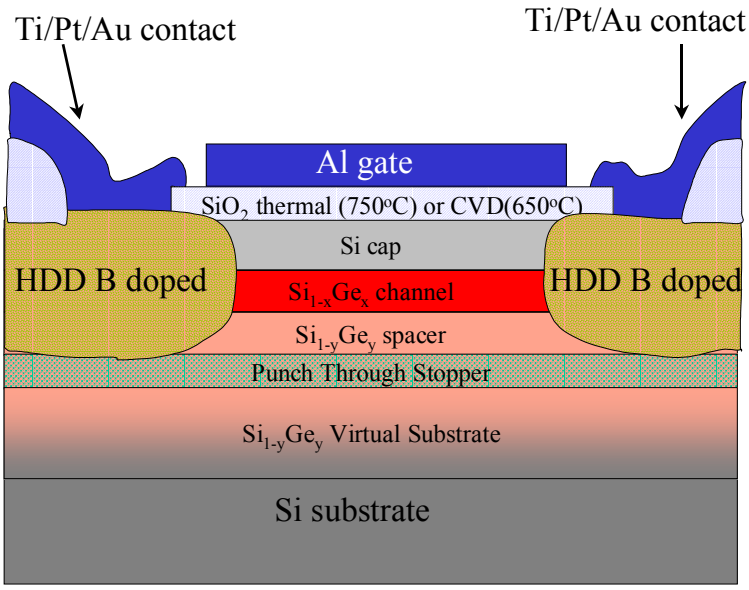

Figure 3.2: The typical structure of a p-type metamorphic SiGe MOSFET.

The processing of MOS devices fabricated from wafers k5660, k5888 and k5889 started with a 200nm PECVD SiO_2 deposition as a field oxide. In the active transistor areas the field oxide was removed by wet chemical etching. After a cleaning step the gate oxide was fabricated by deposition of 10 nm PECVD oxide at 370 , followed by a NH_3 plasma treatment for 2 min and a 650 anneal in a N_2O atmosphere for 1 min. This process was found to yield low interface trap densities in the range of $(1\text{-}3)\times10^{11}\text{cm}^{-2}\text{eV}^{-1}$. Ohmic contacts were fabricated by implantation of BF_2^+ and futher activation at 650 in N_2 for 30 s. Finally, the Al gates and the contact metallization were evaporated [112].

Two Si controls were used to compare investigated samples with conventional Si technology devices. First, p-Si(p^-) control were fabricated in DaimlerChrysler in the same fabrication process as k5888 and k5889 samples. It was used to investigate SiGe influence on device performance and reliability independently on used technology. p-Si(n^+) MOSFET devices (Sotton, wafer 6) [115] were fabricated on SS-MBE grown 100 nm Si epilayers on n-type (1×10^{17} cm^{-3}) Si(001) wafers using a self-aligned gate process, with 9 nm SiO_2 dry thermally grown at 800 for 120 min and 300 nm p-type (5×10^{19} cm^{-3})

poly-Si gate. This technology close to standard industrial CMOS process and p-Si(n^+) MOSFETs performance close to ideal. That is why these p-Si(n^+) devices were used to overall comparison of investigated SiGe MOSFETs on VS with conventional Si CMOS technology.

All devices were fabricated using the same mask, and MOSFETs were available with different gate length of 50, 10, 5, 2, 1.5 and 1 μm and the same gate width W=50 μm (Fig. 3.4). The parameters of the device structure extracted from the characterisation are shown in table 4.1. Cross sections of the p-Si samples and p-$Si_{0.67}Ge_{0.33}$ pseudomorphic samples used for comparison are shown in Fig. 3.3. Devices fabricated in Sotton and used in this work have gate width 40 μm and gate length 10 and 1 μm.

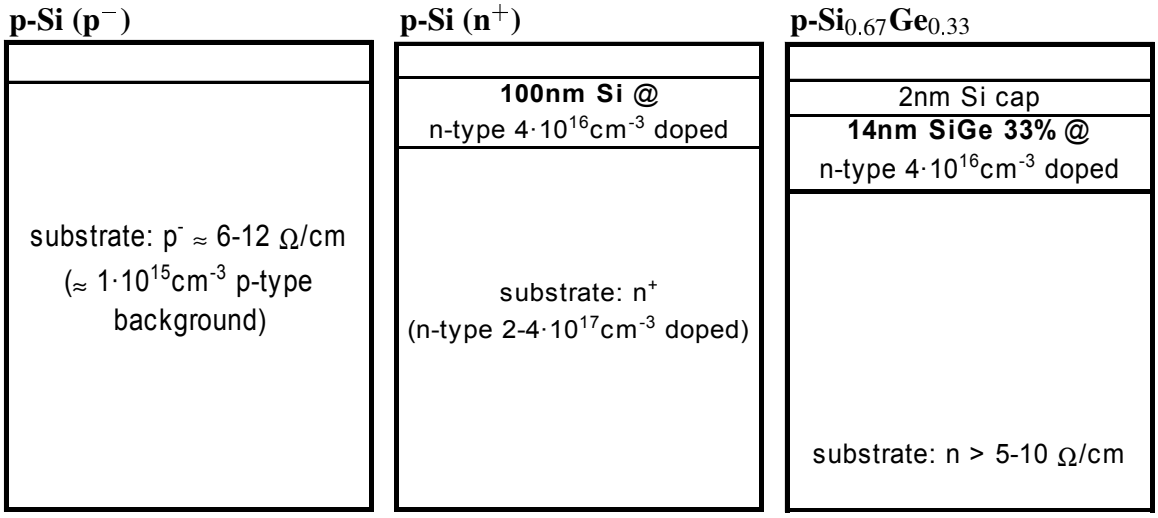

Figure 3.3: Cross sections of the control samples. Daimler p-Si MOSFET with lightly p-type doped substrate (p-Si (p^-)), conventional p-Si MOSFET with heavy doped n-type substrate (p-Si (n^+) - Sotton p-Si, w6) and pseudomorphic p-SiGe MOSFET (p-$Si_{0.67}Ge_{0.33}$ - Sotton, w1) are shown.

3.2 Current-voltage *I-V* measurements technique

Room temperature characterisation of MOSFETs included on-wafer and in-package DC characteristics measurements, as well as noise measurements. On-wafer FET characterisation employs a four-terminal technique. Chips or whole wafers were placed on top of an aluminium Faraday cage connected to the substrate line. The gate contact, the source, the drain contacts and the back metallised (substrate) contact were connected to the measurement equipment by 3 titanium needle probes with fine position controls. Measurements

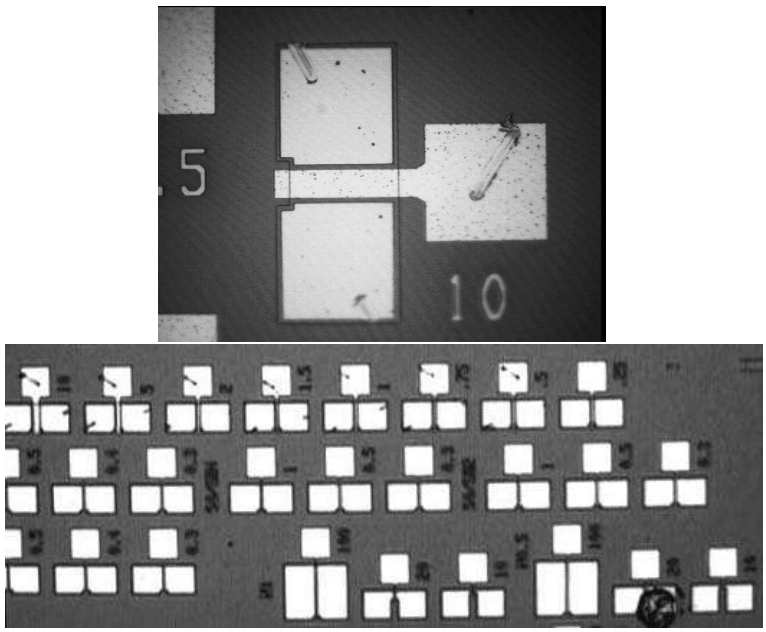

Figure 3.4: Photo of DaimlerChrysler MOSFET's set with gate length 1-10 μm.

were carried out in an electrically and optically shielded box (Karl Suss probing station).

After the on-wafer characterisation the wafers were cut into pieces by a diamond saw. The pieces were placed in standard 14-16 pin ceramic packages and the devices were bonded to package contact pads by gold wire using a ball bounder. Packages with bonded samples were placed in a HP16058A test fixture for DC measurements or in a preamplifier box in an electrically shielded room for noise measurements.

I-V characteristics of investigated p-MOSFETs were measured using the Agilent HP4156C precision parameter analyser (Fig. 3.5).

3.3 Capacitance-voltage *C-V* measurements

The experimental setup mentioned in the previous section was also used to perform quasi-static and high frequency capacitance-voltage measurements. Results of the on-wafer capacitance-voltage (*C-V*) measurements were more reproducible than the measurements performed on devices in packages due to a lower capacitance of connection wires. *C-V* measurements were carried out using the Keithley based *C-V* kit (K590 + K595). High frequency *C-V* characteristics were measured by the K590 *C-V*-meter. Quasi-static *C-V* characteristics were measured on capacitance dots using both the Keithley K595 and the Agilent HP4156C precision parameter analyser (Fig 3.6). Quasi-static split-*C-V* charac-

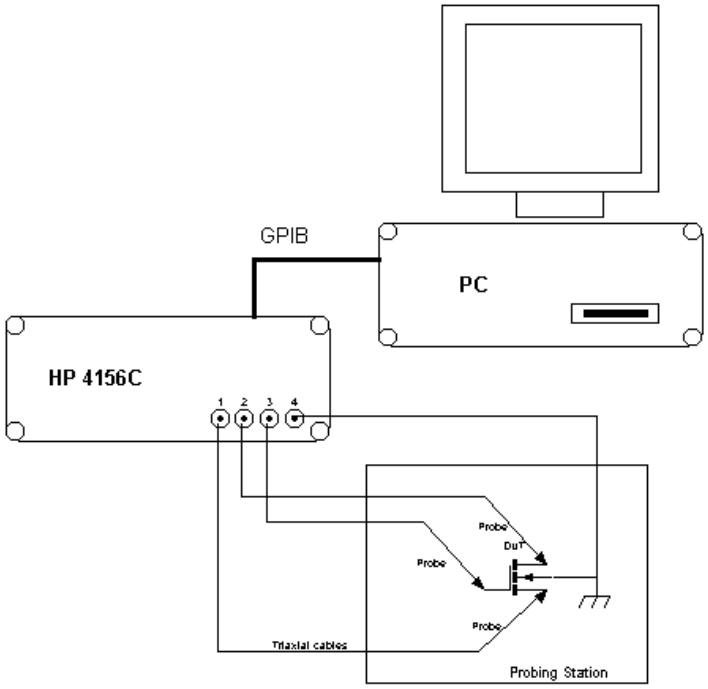

Figure 3.5: The equipment setup for current-voltage measurements.

teristics on $50\times50\mu$m, $10\times50\mu$m and $5\times50\mu$m devices were measured by the HP4156C analyser.

3.4 Low temperature measurements

Low temperature measurements were carried out at liquid nitrogen temperature T=77K. The chip package with the sample was mounted in a chip socket at the end of a probe for the cryostat. This probe with a sample was moved slowly into the dewar with liquid nitrogen. Since the chip pins connect permanently to the contact pads, they need protection from electrostatic discharges. This applies both during handling and when connecting and disconnecting the FETs for measurement.

To help protect the FETs, an interface box connects the cryostat probe outputs to the measurement system. This includes a circuit (shown in Fig. 3.7) for every chip package pin to protect against excessive voltages. Two back-to-back Si diodes with a high back resistance will insulate if the voltage across them is less than their rated value. The value chosen (100 V) is much higher than the maximum voltage used in the measurements, however it protects our devices from electrostatic discharges perfectly. Gate leakage, substrate leakage and de-

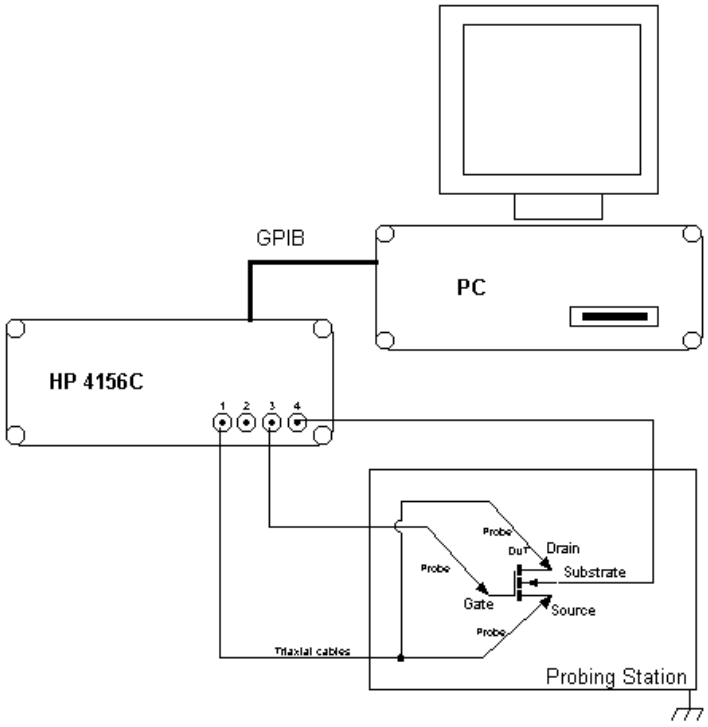

Figure 3.6: The equipment setup for capacitance-voltage measurements.

vice "off current" was measured at low temperatures without this protection circuit in order to increase the accuracy of low current measurements. Connection cables with minimal allowable length were used to reduce parasitic capacitance and excessive electrical noise.

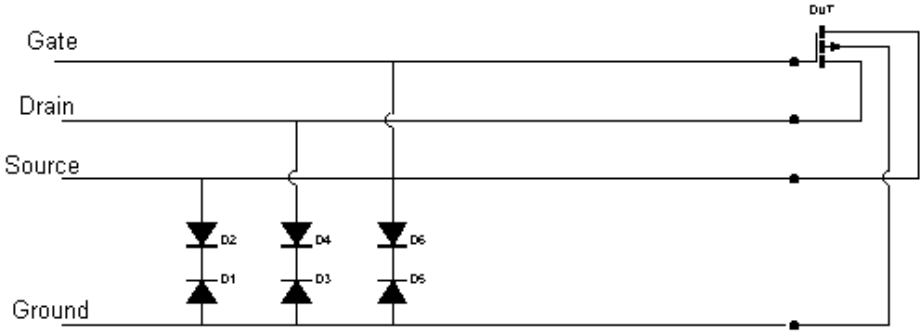

Figure 3.7: Device protection circuit for low temperature measurements.

3.5 Low frequency (LF) noise measurements

The low frequency noise was measured using an HP 35670A dynamic signal analyzer and custom-made preamplifier containing OPA637 (Texas Instruments) and LT1028 (Linear

Technology) operational amplifiers in the first stage. All measurements were done on MOSFETs with a geometrical gate length of 1.0 μm (an effective gate length was extracted as 0.55 μm) - 10 μm in an electrically shielded room at 293 K. The SiGe MOSFETs show enhancement in drain-current and transconductance at the same gate overdrive voltages in comparison with p-Si devices. LF noise has been measured in the linear regime of the output *I-V* characteristics (V_{DS}= -50 mV), from the sub-threshold through weak to strong inversion ($V_G - V_{TH}$ from 0.5 to –3 V) of the input *I-V*, in a wide range of drain-source conductance $g_d = I_D/V_{DS}$. Collected data were processed and analysed on computer. Measured power spectra were filtered by own written computer software to remove peaks connected to excess (50Hz and overtones) electrical noise. Next, analysis on type of LF noise was performed at each frequency range of spectra. 1/f noise values at 1 Hz were used for further analysis and fitting.

3.6 Preamplifier design for LF noise measurements

Conventional MOSFET characterisation techniques, such as the combination of *I-V* (current-voltage) and *C-V* (capacitance-voltage) measurements, are very problematic as device sizes decrease down to the deep sub-μm (DS-μm) scale. "Average per square" characteristic parameters obtained from large-scale devices cannot be suitable for DS-μm MOSFET analysis due to statistical uncertainty of fabrication technology together with the importance of mesoscopic quantum effects. Low frequency noise measurements could be a powerful diagnostic technique for DS-μm MOSFET characterization in a wide range of device operation regimes [126]. Unfortunately, the commercially available current preamplifiers such as ITHACO-1211 [117], SR-570 [118], EG&G-181 [119] have been optimised only for limited ranges of device input impedance and their conventional "all-in-one" desktop design also introduces extra problems when long cables are used to connect to the sample test fixture. To overcome all the above problems the optimised preamplifier modules as the first stages for gate leakage and drain current noise measurements of MOSFETs with input impedance 50Ω-10^8Ω in the frequency range of 1.0 Hz-10^5 Hz.

Background equivalent noise of amplifier is defined by equivalent noise of the first stage. Electrical noise of first stage was described earlier by Hung *et al* [120] and more thoroughly

analysed by Vandamme *et al* [121] for the particular case of common-emitter amplifier with BJT input. However, the individual current source introduces additional noise in system, and the first stage here was also used as a current source for device under test (DUT). The equivalent scheme for the first stage of such a preamplifier is shown on Fig. 3.8

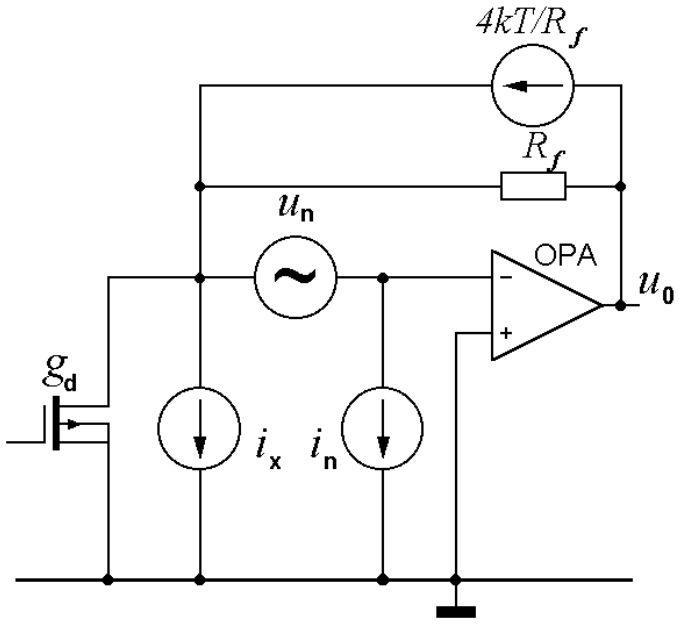

Figure 3.8: The first stage of current preamplifier equivalent scheme. Sources of current i_x, i_n, $4k_BT/R_f$ and voltage u_n noise are shown.

According to Fig. 3.8, output voltage fluctuations of the first stage could be presented as:

$$u_0^2 = R_f^2 \left(i_x^2 + i_n^2 + \frac{4k_BT}{R_f} + u_n^2 \left(\frac{1}{R_f} + g_d \right)^2 \right) \tag{3.1}$$

where i_n – equivalent input current noise of OPA, v_n – equivalent input voltage noise of OPA, i_x – drain current noise of DUT, R_f – feedback resistance value, g_d – DUT conductance ($g_d = 1/R_{tot}$ in linear regime). At low frequencies (below 10^5Hz), a feedback resistor can introduce extra $1/f$ noise, which depends on quality of resistor material.

Drain current MOSFET noise could be measured if background noise from the preamplifier is less than noise from our device:

$$i_x^2 \geq i_n^2 + \frac{4k_BT}{R_f} + u_n^2 \left(\frac{1}{R_f} + g_d \right)^2 \tag{3.2}$$

The condition for reduced drain current noise can be rewritten as:

$$\frac{i_x^2}{I_D^2} = \frac{i_x^2 R_{tot}^2}{V_{DS}^2} \geq \left(i_n^2 + \frac{4k_B T}{R_f}\right)\frac{R_{tot}^2}{V_{DS}^2} + \frac{u_n^2}{V_{DS}^2}\left(\frac{R_{tot}}{R_f}+1\right)^2 \tag{3.3}$$

We can get optimal resistance and device impedance for each OPA or optimal OPA for defined device impedance, if we could compare preamplifier noise with DUT thermal noise $i_x^2/I_D^2 = 4k_B T R_{tot}/V_{DS}^2$ and minimise the functional (3.4) by R_{tot} and R_f variation:

$$F(R_{tot}, R_f) = \left(\left(i_n^2 + \frac{4k_B T}{R_f}\right)\frac{R_{tot}^2}{V_{DS}^2} + \frac{u_n^2}{V_{DS}^2}\left(\frac{R_{tot}}{R_f}+1\right)^2\right) \Bigg/ \frac{4k_B T R_{tot}}{V_{DS}^2} \tag{3.4}$$

$$\frac{\partial F(R_{tot}, R_f)}{\partial R_{tot}} = 0 \tag{3.5}$$

$$R_{tot} = \frac{R_f u_n}{\sqrt{i_n^2 R_f^2 + 4k_B T R_f - u_n^2}} \tag{3.6}$$

If an OPA is used as a current source for a DUT, current through the DUT is limited by supply voltage V_{batt} of OPA and feedback resistance value R_f :

$$I_{max} \approx \frac{V_{batt}}{R_f} \geq \frac{V_{DS}}{R_{tot}} \Rightarrow R_{tot} \geq R_f \frac{V_{DS}}{V_{batt}} \tag{3.7}$$

Table 3.1: Parameters of operational amplifiers (OPAs) used for preamplifier modules

OPA	Input noise at f = 1 Hz		Input noise at f = 10 kHz	
	i_n (fA$\times$Hz$^{-1/2}$)	u_n (nV$\times$Hz$^{-1/2}$)	i_n (fA$\times$Hz$^{-1/2}$)	u_n (nV$\times$Hz$^{-1/2}$)
LT1028	9000	1.6	1000	0.85
OPA637	2.5	50	2.0	3.7
AD549	0.7	200	0.15	35

OPA	feedback resistance R_f (Ω)	DUT resistance (Ω)	Gain-Bandwidth product (MHz)
LT1028	1×10^4	(0.05-5) $\times10^3$	75
OPA637	1×10^5	(0.05-5) $\times10^5$	80
AD549	1×10^7	(0.05-9) $\times10^7$	1

So, the choice of feedback resistance and selection OPA restricted on the DUT impedance range [122]. Optimal feedback resistor for selected OPA can be chosen from condition $R_f i_n \approx u_n$. Choice of R_f is also depend on stability of designed module and maximum

input current, which limits the minimum allowed DUT resistance for measurements at fixed drain-source voltage V_{DS}.

Thorough analysis of currently available commercial OPAs was carried out. Average values and frequency dependence at frequency range 10^0-10^5 Hz of equivalent input current i_n and voltage v_n noise were determined from datasheets and measurements of available samples. The AD549, OPA637 and LT1028A OPAs were chosen to use in the first stage modules at three impedance ranges to obtain the lowest noise at each range. Feedback resistance R_f and i_n , v_n values for used OPA are presented in table 3.1. Functional $F(R_{tot},R_f\ )$ for selected OPAs are shown on Fig. 3.9. Thermal noise of the DUT could be measured, if $F(R_{tot},R_f) \leq 1$, while $1/f$ noise could be measured at low frequency (1-10Hz) even if $F(R_{tot},R_f) > 1$.

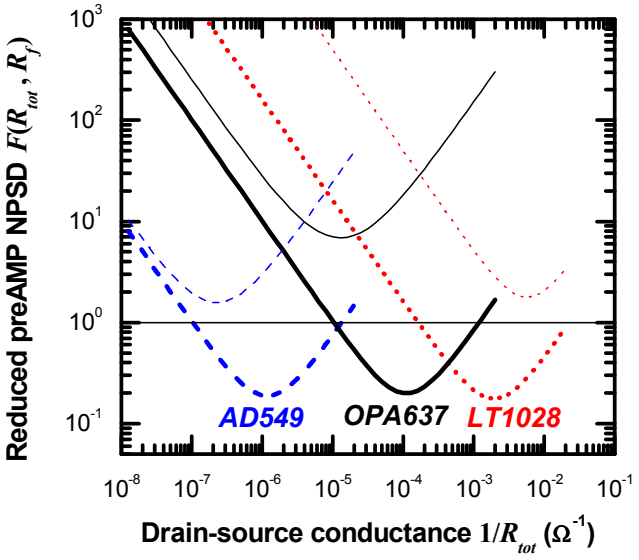

Figure 3.9: Preamplifier modules background noise normalised on thermal noise of DUT for OPAs AD549 with R_f = 10 MΩ, OPA637 with R_f = 100 kΩ and LT1028 with R_f = 10 kΩ at f = 10 kHz (thick lines) and f = 1 Hz (thin lines).

The feedback resistor was chosen of wired or metal film type to keep preamplifier stability and bandwidth and to reduce $1/f$ noise introduced by it. Each preamplifier module was placed in a separate small shielded metal box with coaxial connectors. A digital oscilloscope (Tektronix 24678) and dynamic spectral analyser (HP35670A) were used to adjust and calibrate the preamplifier. A modular design was chosen to increase reliability of the amplifier and reduce the influence of connection cables on measurement results.

The schematic amplifier circuit diagram is shown on Fig. 3.10 Preamplifier modules ***A***, ***B*** and ***C*** can be used for drain current noise measurements (connectors 1,2,3). Module ***C*** with AD549 OPA is also suitable for gate leakage current noise measurements (connectors 1,2,4).

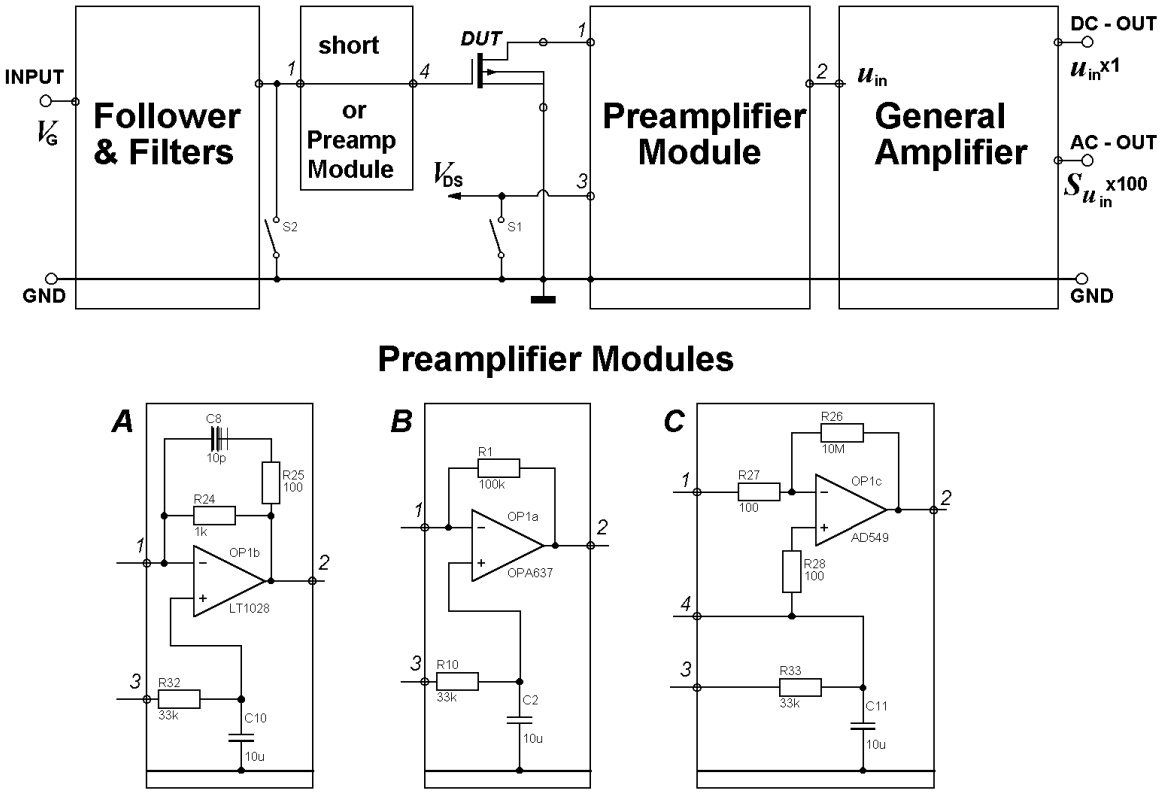

Figure 3.10: Schematic circuit diagram of the current preamplifier with modular design and interchangeable first stages *A*, *B* and *C* for LF-noise measurements.

Three preamplifier modules, a follower with two-pass LF noise filter, a general amplifier module with gain of $G = 100$, Pb-acid batteries and a test fixture or cryostat with DUT were used for the measurements. The preamplifier modules' background noise mixed together with MOSFET's noise measured at $f = 1$ Hz and $f = 100$ kHz versus DUT conductance are shown on Fig. 3.11.

Normalised drain current power spectral density (NPSD) for MOSFETs at $f = 100$ kHz agree with preamplifier noise together with thermal noise NPSD predicted and measured on set of metal film resistors at low and high DUT conductance. Increased values of NPSD for MOSFETs at $f = 100$ kHz at intermediate DUT conductance range correspond to $1/f$ noise. NPSD for MOSFETs at $f = 1$ Hz are almost several orders of magnitude higher than preamplifier background noise at chosen conductance ranges.

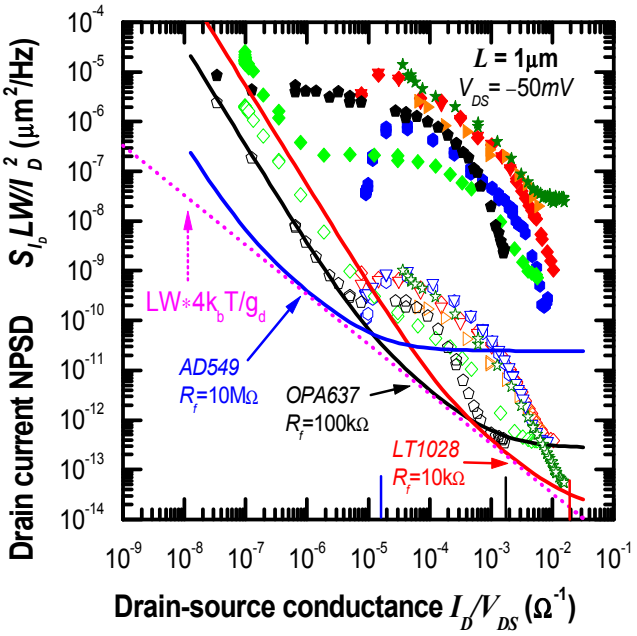

Figure 3.11: Normalised drain current noise of measured MOSFETs (filled symbols at f = 1 Hz and unfilled symbols at f = 100 kHz) and background noise of built preamplifier modules at f = 10 kHz (solid lines). Thermal noise of devices is also shown for comparison (dotted line).

Chapter 4

Results and Analysis

Current-voltage DC characteristics, capacitance-voltage characteristics and low frequency noise were measured on investigated samples at different temperatures and different biased condition.

4.1 Current-voltage characteristics of SiGe p-MOSFETs

Input I-V characteristics in the ohmic region are shown in Fig. 4.1 for the 1 μm written gate length (L = 1 μm, W = 50 μm) MOSFETs. This figure demonstrates that higher drain currents can be achieved in SiGe devices in comparison with conventional Si devices. The input I-V characteristics in the region of saturation are shown in Fig. 4.2 for the same MOSFETs. Some of p-SiGe devices (c2321(b), k5660, k5888, k5889) and the Daimler Chrysler Si control p-Si (p^-) devices do not contain either a "punch-through" stopper (PTS) or a buried oxide to prevent short channel effects. However, these devices still work at high source-drain voltages. The drain current in the off state (I_{OFF}) is at least 10 times less than the maximum drain current in the open state (I_{ON}) at maximum drain-source voltage. The c2154 p-MOSFETs with PTS have a very good subthreshold slope S = 85 mV/decade and low I_{OFF} , which is 7 order of magnitude less than I_{ON}. Subthreshold slope is ideal for such a structure and is close to the ideal subthreshold slope of 61 mV/decade for conventional p-Si MOSFETs.

Typical output I-V characteristics at different gate voltages are shown in figure 4.3 for the 1.0 μm written gate length MOSFETs. The drain current in the SiGe MOSFETs exceeds

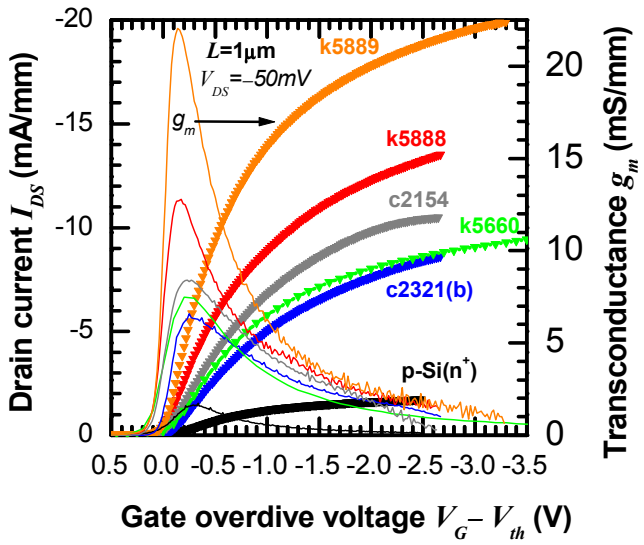

Figure 4.1: Drain current and transconductance versus gate voltage dependence for Daimler Chrysler p-SiGe MOSFETs and conventional p-Si (n^+) MOSFET in ohmic region at $V_{DS} = -50$ mV.

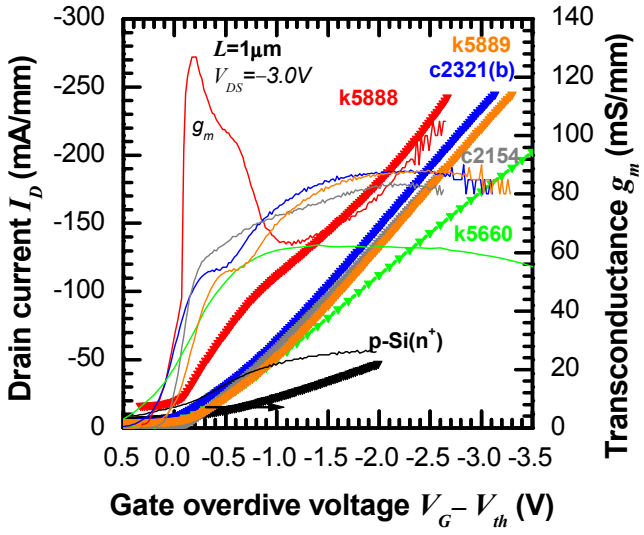

Figure 4.2: Drain current and transconductance versus gate voltage dependence for Daimler Chrysler p-SiGe MOSFETs and conventional p-Si (n^+) MOSFET in saturation region at $V_{DS} = -2.5$ V.

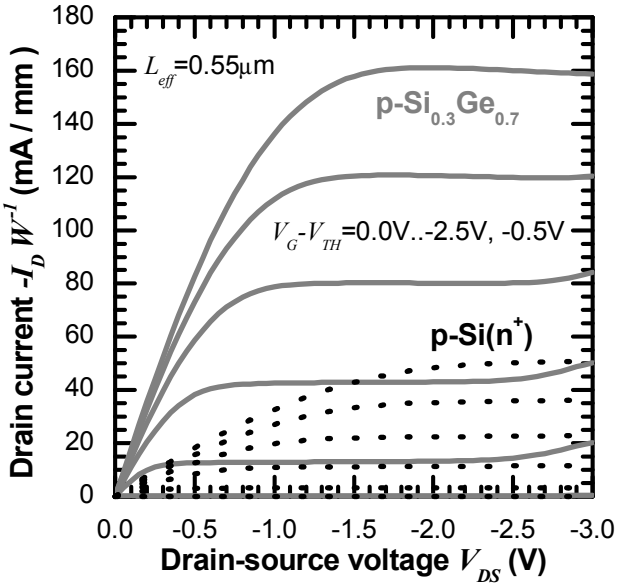

Figure 4.3: Output I-V characteristics for p-Si (n^+) (Sotton, w6) and p$-Si_{0.3}Ge_{0.7}$ (c2154) MOSFET with $L = 1\mu$m at the same $V_G - V_{TH}$.

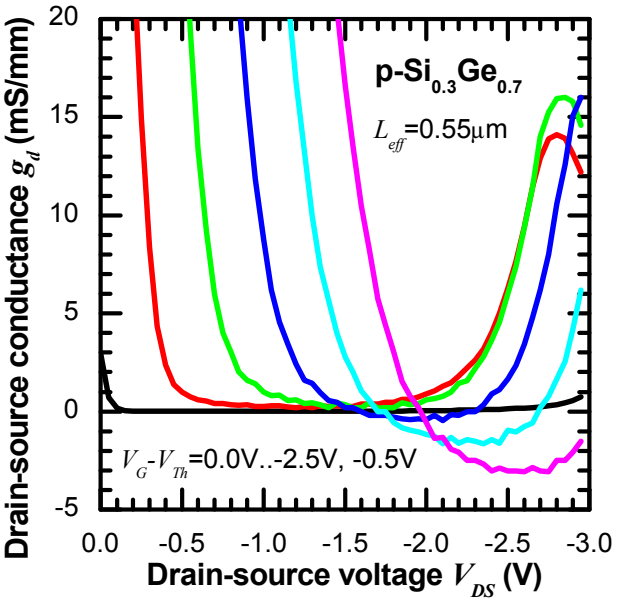

Figure 4.4: Drain-source conductance g_d for p$-Si_{0.3}Ge_{0.7}$ (c2154) MOSFET with $L = 1$ μm. Negative g_d values at high V_{DS} can be assoiated with overheating effect.

the drain current in a conventional Si p-MOS device by a factor of 3.5. The drain current slowly changes with drain-source voltage in the saturation region increasing on devices with gate length 50-1.5μm and sometime falling on 1.0 μm gate length devices. This is indication of increasing channel resistance at high drain currents due to a self heating effect (see negative g_d in Fig. 4.4). In the output I-V characteristics for the 1.0 μm gate length c2154 MOSFET devices the drain current sharply grows at a drain-source voltage $V_{DS} \approx -2.5$ V. This points to impact ionisation or tunnelling in the depleted area near the drain contact.

Measured I-V characteristics were used to create and calibrate numerical models for MOSFET characteristics simulation (see chapter 2, section 2.3) and all parameters extracted (such as effective mobility, source-drain resistance, oxide trap density) with help of conventional techniques, also were rechecked during the simulation.

4.1.1 Threshold voltage and gate electrode material

As it shown in chapter 2 (section 2.2.2), the threshold voltage strongly depend on gate material, heterostructure design, gate dielectric quality and SiO_2/Si interface fixed charge. The threshold voltage of all investigated Daimler Chrysler p-MOSFETs has the negative values due to metal Al gate used. The threshold voltage of p-Si (n^+) (Sotton, w6) and pseudomorphic p-$Si_{0.67}Ge_{0.33}$ (Sotton, w1) MOSFETs used for comparison have a positive values or values close to zero. The average threshold voltage values, extracted for all samples, are presented in table 4.1. Fig. 4.5 shows the threshold voltage V_{Th} for all samples as a function of gate length.

The figure shows that the V_{Th} for p-SiGe devices with Al gate is higher than for p-Si devices with Al gate due to the offset in the valence band between Si and SiGe. However, the V_{Th} for p-SiGe devices with Al gate is lower than for p-Si devices with poly-Si gate. The MOSFETs with the same gate, the similar Si/SiO_2 interface quality and with n-type PTS have a lower (more negative) threshold voltage (c2154 and c2321(a) in comparison with c2321(b)). This is normal since the Fermi level lay close to the conduction band in the heavy doped n-type region. This pulls the valence band down and requires a more negative gate bias to pull the valence band up at the surface. The threshold voltage for k5888 and k5889 devices more close to zero than for other samples without any special gate design.

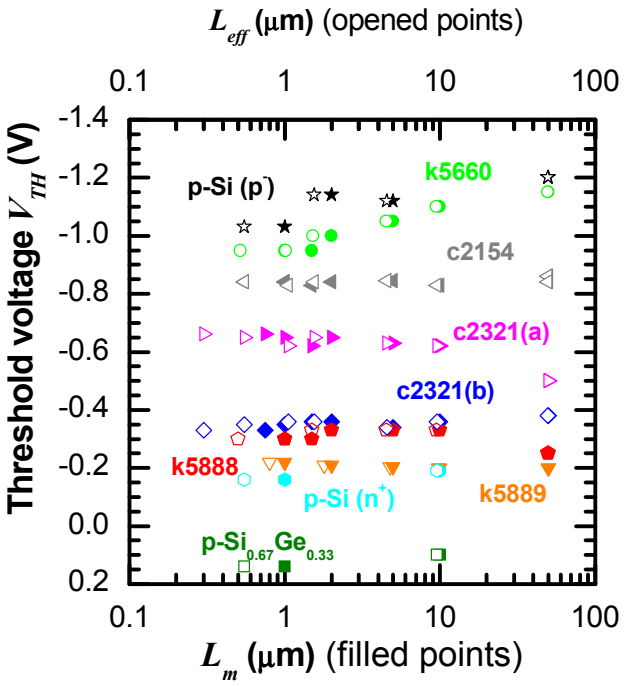

Figure 4.5: Threshold voltage versus geometrical gate length for p-SiGe metamorphic MOSFETs with Al gate, p-SiGe pseudomorphic MOSFET with p-type doped poly-Si gate and p-Si MOSFETs with Al and p-type doped poly-Si gates.

Table 4.1: P-MOSFETs parameters extracted from I-V and C-V measurements.

p-MOSFET	Oxide thickness (nm)	Cap thickness (nm)	ΔL_{eff} (μm)	R_{cont} (k$\Omega\cdot\mu$m)	Subthreshold Slope (mV/decade)	Interface fixed charge density ($eV^{-1}cm^{-2}$) *(from MEDICI fitting)*
C2154	7.1	5.1	0.45	2.10	95	
C2321(b)	6.2	6.22	0.45	2.15	127	1.6×10^{12}
K5660	6.2	3.4	0.48	4.25	200	2×10^{11}
K5888	9.1	3.3	0.50	2.30	170	
K5889	4.8	5.8	0.45	1.35	150	
p-Si (p^-), Daimler)	10.1	-	0.45	-	150	
p-Si (n^+), Sotton)	9.4	-	-	-	61	

p-MOSFET	Interface fixed charge density ($eV^{-1}cm^{-2}$) *(from CV)*	Interface fixed charge density ($eV^{-1}cm^{-2}$) *(from noise)*	V_{Th} (V)	$g_{m(sat)}$ (mS/mm)	I_{ON}/I_{OFF} V_{DS}=-50mV	I_{ON}/I_{OFF} V_{DS}=-3V
C2154	$3\text{-}7\times10^{11}$	6×10^{9}	-0.84	95	10^6	10^4
C2321	$3\text{-}7\times10^{11}$	6×10^{9}	-0.61	88	2×10^4	52
K5660	$1\text{-}3\times10^{11}$	-	-1.1	200	2.5×10^3	26
K5888	$0.3\text{-}2\times10^{12}$	8×10^{9}	-0.25	130	2.5×10^3	15
K5889	$0.3\text{-}4\times10^{12}$	1×10^{10}	-0.26	135	2.5×10^3	16
Si (Daimler)	$0.3\text{-}4\times10^{12}$	2×10^{10}	-1.02	39	1.0×10^3	11
Si (Sotton)	$<2\times10^{11}$	5×10^{8}	-0.2	40	10^6	10^4

This is especially important due to impossibility V_{Th} adjustment by gate doping as for poly-Si gates. The difference between k5888, k5889 and k5660 devices, which have a similar design, is due to the extra interface charges and traps in wafers k5888 and k5889 (see section 4.2.3). The threshold voltage roll-off at low channel lengths is very small (Fig 4.4) for all Daimler Chrysler wafers and tendentious to V_{Th} increasing (moving to positive values) with gate length decreasing from 50 μm to 1.0 μm (L_{eff} = 0.55 μm) was not observed for investigated samples. For $V_{DS} = -2.5$ V (not shown), the threshold roll-off is much more severe for MOSFETs with low doped substrates without PTS (of the order of a volt) due to large DIBL for short channel devices but is almost unchanged (15 mV/V for c2154 and 7.5 mV/V p-Si (n^+) (Sotton, w6)) for the high n-type doped substrates case or devices with PTS.

4.1.2 Punch through stopper influence on short channel effects

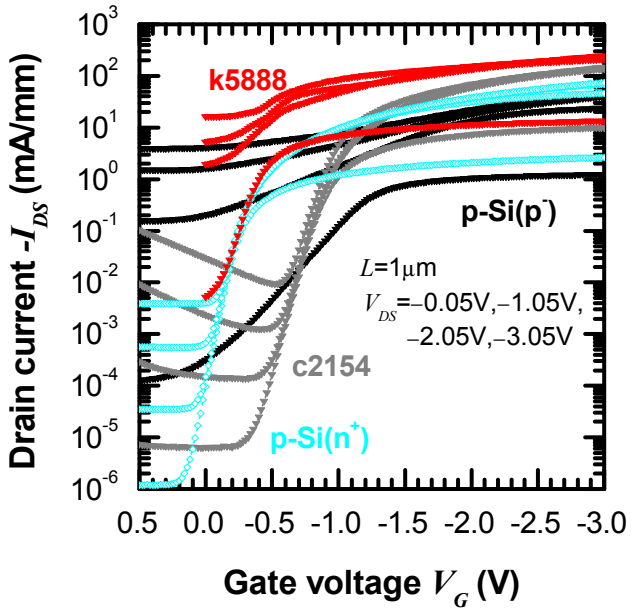

Figure 4.6: Drain current versus gate voltage dependence at different drain-source voltages for samples p-$Si_{0.3}Ge_{0.7}$ (c2154), p-$Si_{0.2}Ge_{0.8}$ (k5888) and p-Si MOSFETs with gate length L= 1.0 μm. Logarithmic scale of drain current axis used for indication subthreshold swing and DIBL effect illustration. p-Si (n^+) MOSFET (Si Sotton) with n-type doped substrate and p-SiGe MOSFET with punch through stopper (c2154) have the lower DIBL and better subthreshold swing than devices without punch through stopper.

Characteristics of devices with a “punch-through stopper” (PTS) (samples c2154) are very

similar to characteristics of an n-type doped Si p-MOSFET in subthreshold region and off state. Fig. 4.6 demonstrates the presence and efficiency of a PTS that considerable improves the characteristics of sub-μm gate length MOSFETs. Introduction of a punch through stopper into the c2154 heterostructure allows one to get excellent $I_{ON}/I_{OFF} \approx 10^7$ at $V_{DS} = -50$ mV and $I_{ON}/I_{OFF} \approx 10^4$ at $V_{DS} = -3$ V.

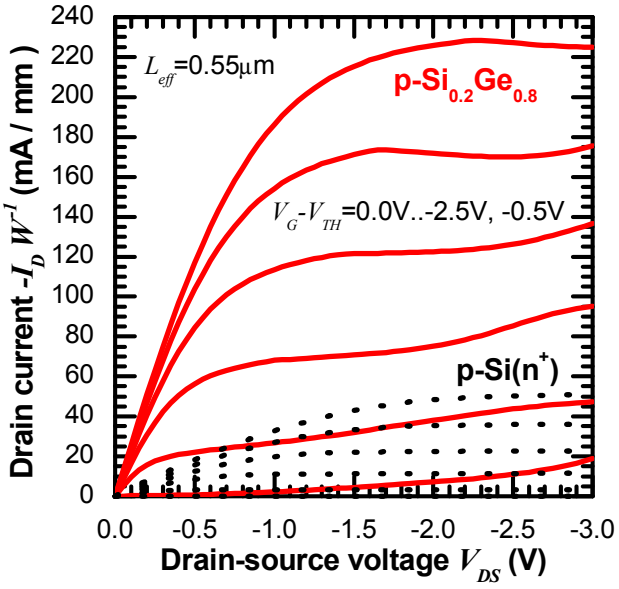

Figure 4.7: Output I-V characteristics for p-Si (Sotton, w6) and p$-$Si$_{0.2}$Ge$_{0.8}$ (k5888) MOSFET with $L_{eff} = 0.55\mu$m at the same $V_G - V_{TH}$.

Maximum current of devices with a PTS (samples c2154) is less then maximum current of devices without a PTS (samples k5888) with similar mobility characteristics in linear and saturation region (Fig. 4.3 and 4.7). It can be explained in this way: increased effective field due to PTS for c2154 decreases effective mobility in p-Si$_{1-x}$Ge$_x$ channel and reduce drain current. Devices without PTS operate at lower effective fields than devices with PTS. As a result. It operate at higher mobility at the same sheet density, even if the maximum mobility is lower than maximum mobility for device with PTS.

4.1.3 Contact resistance extracted from I-V characteristics

Contact resistance has been extracted from the total resistance R_{total} of devices with different gate lengths and at different gate voltages in the ohmic region using the standard R vs L technique described in [35], [31] and 2.2.5. This technique has discussed in subsection 2.2.5 and provides results with sufficient accuracy in our case. The contact resistance extraction procedure for sample k5888 is shown in Fig. 4.8.

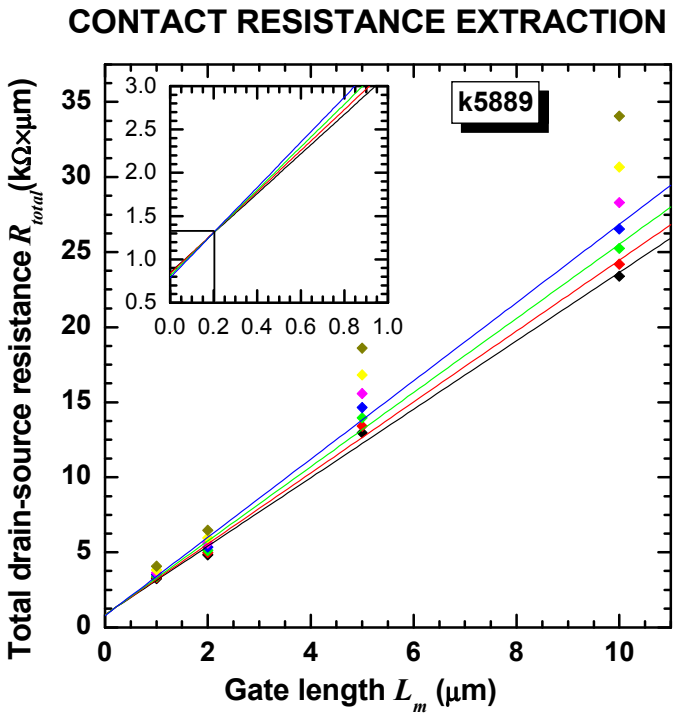

Figure 4.8: Source-drain series resistance and effective gate length extraction for sample (k5889) with the help of "R vs L" method [35]. p-MOSFETs with gate length $L = 1, 2, 5, 10$ μm were used for extraction. Colour points correspond to device resistance in ohmic region at gate voltages -1.5/-3.0V with step -0.25V. Total source-drain resistance extracted for k5889 is $R_S + R_D = 1.35 \pm 0.1$ k$\Omega \times \mu$m and effective length reduction is $\Delta L = 0.2 \pm 0.05$ μm.

Contacts for all the DaimlerChrysler devices, except the Si control, were fabricated by the same technology, and the series source-drain resistance of all devices has approximately the same value $R_S + R_D \approx 1.5 - 2.0$ $k\Omega \times \mu$m. Extracted values are presented in table 4.1.

4.2 Capacitance-voltage characteristics of SiGe p-MOSFETs

Typical split C-V curves measured on 50×50μm devices are shown in Fig. 4.9. Lines are the high frequency data measured by the K595 C-V meter and points are the quasi static C-V measured using the HP4156C parameter analyser. Capacitance in the depletion region closes to a plateau. This indicates the absence of gate depletion as a result of using an Al metal gate. High frequency capacitance and quasi static capacitance have a small difference in weak inversion due to the presence of mobile traps in the oxide. Structural parameters presented in table 4.1 have been extracted from the C-V fits performed using the one-dimensional Poisson-Schrödinger simulator (see subsection 2.3.1) by Greg Snider [123]. The simulation is extremely useful as it includes quantum-mechanical effects in calculating the vertical charge distribution. To improve the accuracy of C-V fitting, Poisson-Schrödinger simulation was used in connection with doping profile extraction from the measured C-V curves.

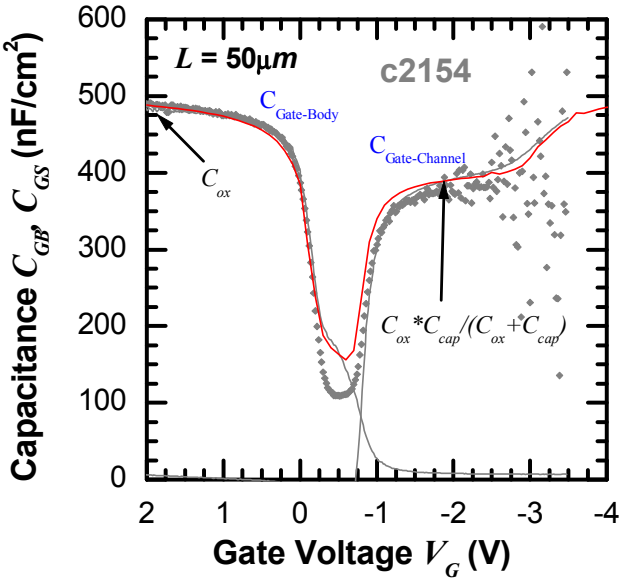

Figure 4.9: Gate to body and gate to channel split capacitance-voltage (C-V) characteristics measured at high frequency for c2154 50×50 μm p-MOSFET. Gray lines are high frequency split C-V characteristics, gray points are quasi static gate to body C-V characteristic, and red line is Poisson-Schrodinger simulation of C-V characteristic.

4.2.1 Device doping profiles from C-V measurements

The doping profiles were extracted using the depletion mode approximation for the investigated devices. The C-V technique relies on the fact that the width of the reverse biased space-charge region of a semiconductor junction depends on the applied voltage. Measured capacitance can be written through the charge variation in the gate electrode:

$$C = \frac{dQ_{gate}}{dV} \tag{4.1}$$

where Q_{gate} is the gate charge. However $C = \frac{C_{ox} \cdot C_{semic}}{C_{ox}+C_{semic}}$, where C_{semic} is the semiconductor capacitance, C_{ox} is the oxide capacitance and $C_{semic} = \frac{C \cdot C_{ox}}{C_{ox}-C}$. At the same time $C = -\frac{dQ_{semic}}{dV}$, where dQ_{semic} is the charge variation in the semiconductor.

In the *depletion approximation*, we suppose that all the charge at a depth less than the depletion depth W_{depl} is depleted at an applied voltage and the charge density at a depth more than W_{depl} is equal to the real carrier density. This approximation leads to errors at large carrier densities, small W_{depl}, and the results obtained are larger than values obtained by other methods. Hence, the method can be used for extraction of doping profiles near the semiconductor-oxide interface and for a rough estimation of the charge density profile in the accumulation region.

In this approximation the charge variation in the whole semiconductor can be written:

$$dQ_{semic} = -qSN_D\left(W_{depl}\right)dW_{depl} \tag{4.2}$$

$$C = -\frac{dQ_{semic}}{dV} = qSN_D(W_{depl})\frac{dW_{depl}}{dV} \tag{4.3}$$

at the same time, $C_{semic} = \varepsilon_{semic}\varepsilon_0 S/W_{depl}$ and depletion concentration is

$$N_D(W_{depl}) = -\frac{C^3}{q\varepsilon_{semic}\varepsilon_0 S^2 dC/dV} \tag{4.4}$$

or:

$$N_D(W_{depl}) = \frac{2}{q\varepsilon_{semic}\varepsilon_0 S^2 d\left(1/C^2\right)/dV} \tag{4.5}$$

were the depletion depth $W_{depl} = \frac{\varepsilon_{semic}\varepsilon_0 S}{C_{semic}}$

$$W_{depl} = \varepsilon_{semic}\varepsilon_0 S\left(\frac{1}{C} - \frac{1}{C_{ox}}\right) \tag{4.6}$$

and finally we have:

$$N_D(W_{depl}) = -\frac{C^3}{q\varepsilon_{semic}\varepsilon_0 S^2 dC/dV}$$

$$W_{depl} = \varepsilon_{semic}\varepsilon_0 S\left(\frac{1}{C} - \frac{1}{C_{ox}}\right)$$

In SiGe HMOS ε_{semic} could depend on W_{depl}(different for different layers, $11.9 \leq \varepsilon_{semic} \leq 16$).

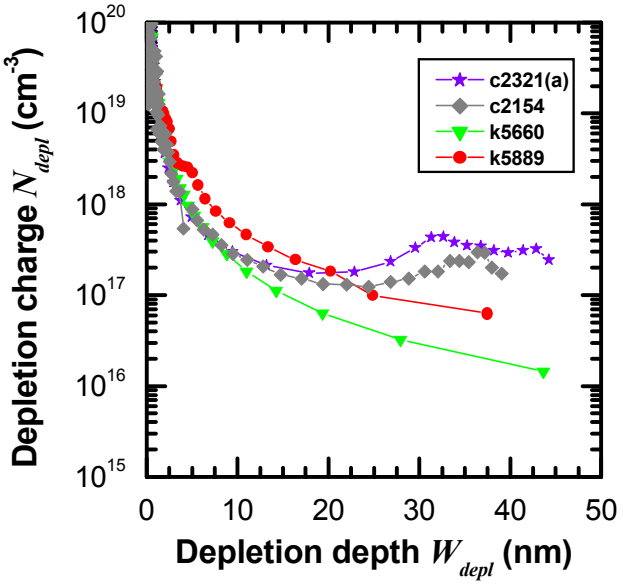

Figure 4.10: Depletion charge profile of metamorphic p-SiGe MOSFETs. Four different p-MOSFET's, c2321(a), c2154, k5660, k5889 were analysed. We can see distinct plateau on c2321(a) depletion charge curve started at 30 nm depth. Depletion charge value is 3×10^{17} cm^{-3} on this plateau. It corresponded to n-type doped SiGe buffer layer that lied 20 nm deeper channel. After 15 nm (45 nm full depth) plateau is broken abruptly, that point to limitation of depletion approximation. Depletion regime is changed to inversion regime (holes accumulation) at this depth. And we do not see any peculiarity on depletion charge curves of k5660, and k5889 p-MOSFET's. It indicate that this samples undoped under channel or doped with donor concentration less then 1×10^{16} cm^{-3}.

The depletion approximation can be used when the majority carrier density is approximately equal to the dopant density. Reasonable deviations of one from the other are limited

by the Debye length given by

$$L_D = \sqrt{\frac{k_b T \varepsilon_{semic} \varepsilon_0}{q^2 (p+n)}} \tag{4.7}$$

The doping profile obtained from the depletion approximation cannot be resolved accurately to less than about two or three Debye lengths [28].

Another limitation of this method to extract the dopant density is a finite maximum depletion depth at which the depletion regime changes to accumulation. The maximum depletion depth corresponds to a minimum capacitance in the gate-body low frequency C-V.

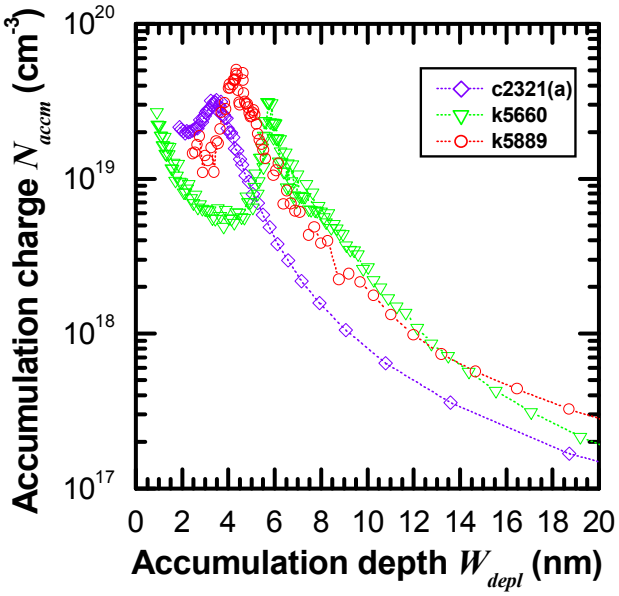

Figure 4.11: Accumulation charge profile of Daimler Chrysler p-SiGe MOSFETs. Peaks are correspond to charge in p-SiGe channels for MOSFET's. Peak depth is 3.5 nm for c2321(a) MOSFET, 5.5-6 nm for k5660 MOSFET, 4.5 nm for k5889 MOSFET.

Extracted depletion charge for samples c2321(a), c2154, k5660 and k5889 is shown in Fig. 4.10. Doping level 3×10^{17} cm^{-3}, which is lie 20 nm under SiGe channel, in c2154 samples correspond to punch through stopper doped area. Doping level 3×10^{17} cm^{-3} agreed well with level 5×10^{17} cm^{-3}, which was defined in structure design. The same calculations carried out for the accumulation region Fig. 4.11 provide information about the distribution of major mobile charge. Peaks in Fig. 4.11 correspond to carriers in the channel. Peak positions (3.5 nm for c2321, 4.5 nm for k5889 and 5.5 nm for k5660) are

well agreed with data obtained from Schrödinger-Poisson fitting of C-V characteristics and drift diffusion simulation of input I-V characteristics.

4.2.2 Effective Mobility of SiGe devices

The mobility of holes is perhaps the most important parameter for device characterisation, at least in long channel devices. The high (100 kHz) and low frequency C-V and split C-V techniques measure the sheet density of holes as detailed above. The mobility follows from a measurement of the current at a low source-drain bias. Sheet density and effective mobility were calculated using expressions (2.24) and (2.22)

The effective field is the vertical electric field averaged with respect to the volume density of holes. A standard approximation of effective field for holes in SiGe MOSFETs (2.30) was used.

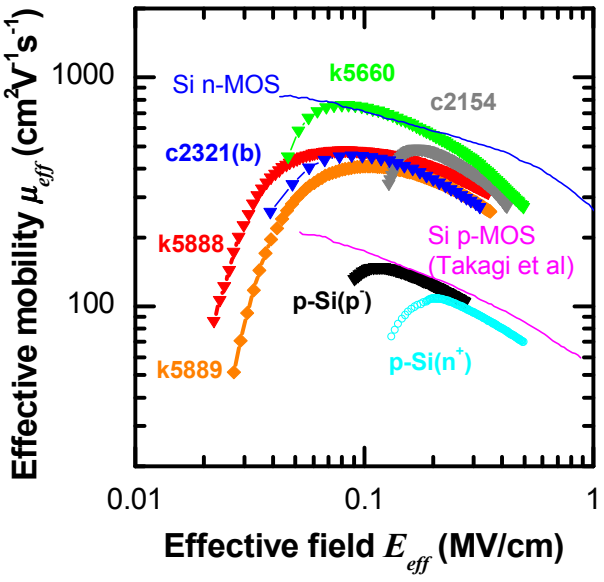

Figure 4.12: Effective mobility versus effective field for Daimler Chrysler SiGe and Si p-MOSFETs.

Fig. 4.12 shows that, reassuringly, the silicon mobility is close to the universal function of electric field (Takagi *et al* [4]). SiGe devices with high Ge content in the channel have a much larger effective mobility than the effective mobility in the Si control. The effective mobility falls faster than the universal curve at high effective electric fields. This can be explained by taking into account the influence of the contact resistance, which is not in-

cluded in the approximation, or the appearance of a parallel surface channel in the Si cap with lower mobility.

4.2.3 Interface traps dencities extracted from C-V measurements

The interface trap density for SiGe p-MOSFETs were only estimated by order of magnitude due to small gate area of investigated samples (Fig. 4.13). High frequency (f = 100kHz) and quasi-static split C-V characteristics were used to obtain interface trap density profile. Interface trap density is 3×10^{11}-4×10^{12}cm^{-2}eV^{-1} for k5888, k5889 samples, 3×10^{11}-7×10^{11}cm^{-2}eV^{-1} for c2321, c2154 samples and (1-3)$\times10^{11}$cm^{-2}eV^{-1} for k5660 [112]. Interface trap density for p-Si (Sotton, w6) is less then 2×10^{11}cm^{-2}eV^{-1} [124]. The yield low interface trap density for k5660 is due to very low impurity background in CVD chamber and also thorough optimisation of LT LEPECVD SiO_2 growth process. Reduced interface trap density for c2123 and c2154 samples in comparison with k5888 and k5889 samples is due to higher temperature of RPCVD oxide fabrication [125] and lower Ge content in SiGe channel. Low interface trap density for p-Si (Sotton, w6) is due to high quality SiO_2 obtained with the help of conventional high temperature oxidation process.

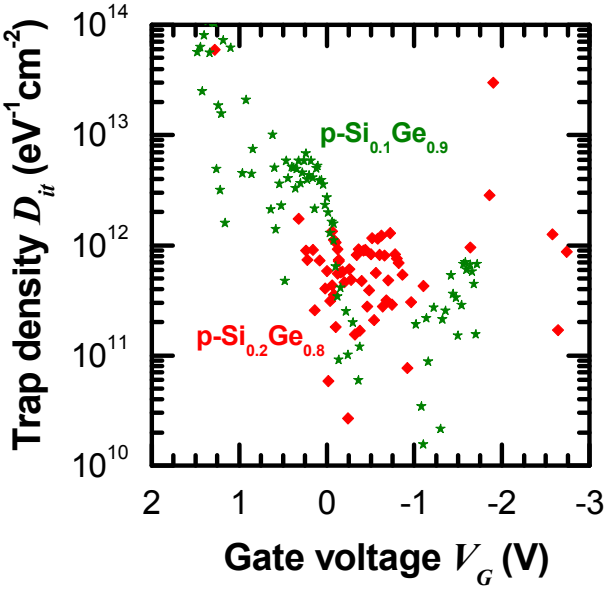

Figure 4.13: Interface trap density versus overdrive gate voltage for p-$Si_{0.2}Ge_{0.8}$ (k5888) and p-$Si_{0.1}Ge_{0.9}$ (k5889) MOSFETs. Estimated D_{it} values are $3\times10^{11} - 1\times10^{12}$ cm^{-2} for k5888 sample and $3\times10^{11} - 4\times10^{12}$ cm^{-2} for k5888 sample

4.3 Low frequency noise of SiGe p-MOSFETs

Most LF-noise measurements have done on MOSFETs with a geometrical gate length of 1.0 μm (an effective gate length was extracted as 0.55 μm, see table 4.1) in an electrically shielded room at 293 K. LF-noise on MOSFETs with other gate lengths 2, 5, and 10 μm also was measured. LF noise has been measured in the linear regime of the output I-V characteristics (V_{DS} = -50 mV), from the sub-threshold to strong inversion ($V_G - V_{TH}$ from 0.5 to –3 V) of the input I-V, in a wide range of drain-source conductance $g_d = I_D/V_{DS}$.

A typical normalized power spectral density (NPSD) $S_I / I^2$of drain current fluctuations versus frequency in the range 1-10^5 Hz is presented in Figs. 4.14 and 4.15. Flicker, $1/f$ component, at low frequencies and thermal noise at high frequency range, dominates the spectra. In Fig. 4.14 the $1/f$ noise for the p-$Si_{0.3}Ge_{0.7}$ MOSFET is clearly seen to be over three times lower than for Si.

4.3.1 $1/f$, GR, RTS and thermal noise of drain current for $1\times50\mu$m SiGe p-MOSFETs

We have not observed a generation-recombination (GR) noise component at any gate overdrive voltage on most devices at RT. This is usually manifested as bumps in the spectra as for c2321(b) MOSFETs. GR noise could appear in the spectra due to Sb diffusion into the $Si_{0.3}Ge_{0.7}$ channel from the Sb-doped "punch-through" stopper or the existence of deep levels or traps in the heterostructure. Thus we can confirm the absence of these defects and contaminations after the full MOSFET fabrication process for most investigated samples.

RTS noise also was not observed for our devices at T=300K, due to big area under gate (50 μm^2 for smallest device).

Thermal noise of MOSFETs were measured together with preamplifier background noise and mostly very well agreed with predicted results for preamplifier. Increased values of NPSD for MOSFETs at f = 100 kHz at intermediate DUT conductance range (10^{-3}-$10^{-5}\Omega^{-1}$) correspond to $1/f$ noise. So, thermal noise of investigated MOSFETs can not be measured at this range due to limited bandwidth of spectra-analyser. Thermal noise of p-SiGe MOSFETs less than thermal noise of p-Si MOSFETs at the same gate overdrive bias due to lower total resistance of SiGe devices.

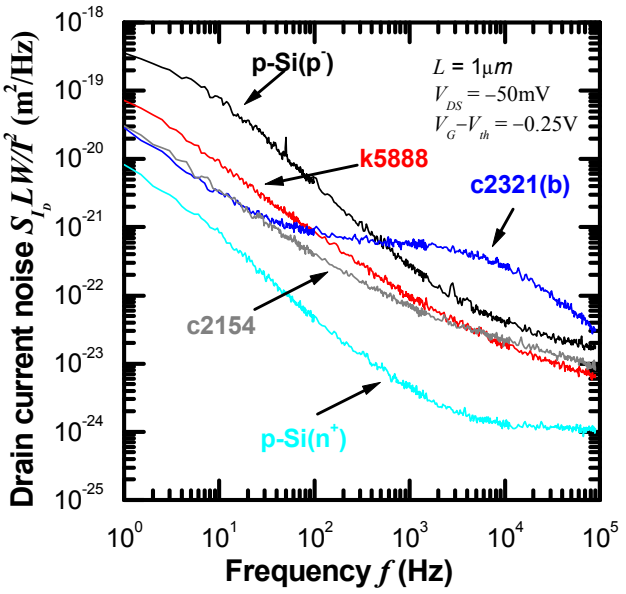

Figure 4.14: Normalized power spectral density of drain current fluctuations as a function of frequency at 293 K for p-$Si_{0.3}Ge_{0.7}$(c2154, c2321), p-$Si_{0.2}Ge_{0.8}$ (k5888) and p-Si MOSFETs with L_{eff}= 0.55 μm. V_{DS} = –50 mV and $V_G - V_{TH}$ = –0.25 V.

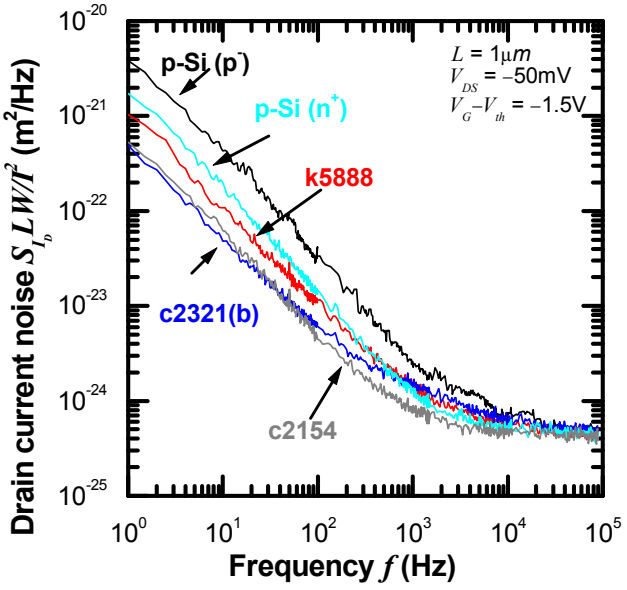

Figure 4.15: Normalized power spectral density of drain current fluctuations as a function of frequency at 293 K for p-$Si_{0.3}Ge_{0.7}$(c2154, c2321), p-$Si_{0.2}Ge_{0.8}$ (k5888) and p-Si MOSFETs with L_{eff}= 0.55 μm. V_{DS} = –50 mV and $V_G - V_{TH}$ = –1.5 V.

The $1/f$ noise observed at frequencies below corner frequency 5×10^2-10^7 Hz depend on gate bias and size of device. The $1/f$ noise PSD values at f = 1 Hz were extracted for further analysis.

4.3.2 Dependence $1/f$ noise on source-drain conductance, components of $1/f$ noise

A typical NPSD $S_I/I^2$of drain current fluctuations in $1/f$ region versus source-drain conductance for c2154 MOSFET with gate length L = 1.0 μm is shown on Fig. 4.16. The NPSD S_I/I^2 in the $1/f$ region can be generally described in terms of carrier number fluctuations (CNF), correlated mobility fluctuations (CMF), source-drain series resistance fluctuations (SDRF) and Hooge mobility fluctuations in the "channel region (HMF):

$$S_{I_D}/I_D^2 = \left(1+\alpha\mu_{eff}CI_D/g_m\right)^2\left(\frac{g_m}{I_D}\right)^2 S_{V_{fb}} + \left(\frac{I_D}{V_{DS}}\right)^2 S_{R_{SD}} + \frac{q\alpha_H\mu_{eff}V_{DS}}{L^2 I_D f} \qquad (4.8)$$

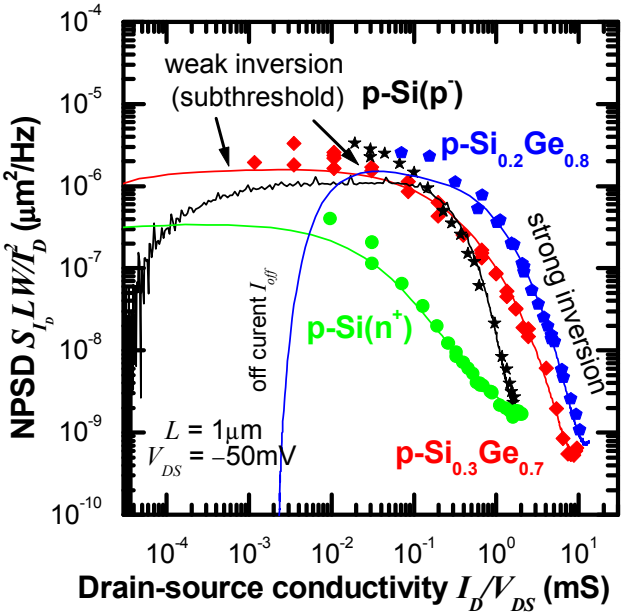

Figure 4.16: A typical NPSD S_{I_D}/I_D^2 of drain current fluctuations in $1/f$ region versus source-drain conductance for p-$Si_{0.3}Ge_{0.7}$ (c2154), p-$Si_{0.2}Ge_{0.8}$ (k5888) and p-Si(p^-) (Daimler), p-Si(n^+)(Sotton, w6) MOSFETs MOSFET with gate length L = 1.0 μm.

So, we have four variable parameters $S_{V_{fb}}$, α, $S_{R_{SD}}$ and α_H to fit experimental results. The SDRF and HMF components could be important only at high overdrive gate voltages

or in device off state, when carrier concentration in device is not depend or depend very slowly on gate voltage (see Fig. 4.17 and Fig. 4.18). The CMF component also has not described MOSFET $1/f$ noise in weak inversion as it shown below (Fig. 4.19). So, only CNF can describe MOSFET $1/f$ noise in subthreshold region. Experimental data in this region can be fitted by $S_{V_{fb}}$ parameter variation. Fitting in this area is insensitive to other $1/f$ noise components as it sown below. However, accuracy of fitting is very sensitive to any errors in measured current due to gate voltage offsets during measurements (see Fig. 4.20). The best way to obtain good accuracy is simultaneous measurements of drain current and drain current noise and gate voltage offset correction for further analysis. This measurement technique used in current approach and described in sections 3.5 and 3.6. So, fitting procedures shown on Figs. 4.17 - 4.20 should be repeated after gate voltage offset have been corrected. Note, the same gate voltage offset was used during the analysis of results for different samples.

In order to improve fitting accuracy and reduce error of extracted noise components I propose to use two additional representations (Fig. 4.20 and (Fig. 4.25)) of measured NPSD together with all known conventional (Fig. 4.21).

CNF component fitting in subthreshold region and region just above threshold is start point to fit $1/f$ noise on drain-conductance dependence (Fig. 4.21). The HMF and the CMF can not describe abrupt increasing (Fig. 4.22) of drain current noise NPSD at high gate overdrive voltages, because the MOSFET effective mobility μ_{eff} decreased with V_G increasing. So the next step is the SDRF noise component fitting at highest gate overdrive voltages (MOSFET "open" state) by $S_{R_{SD}}$ parameter variation (Fig. 4.23).

It was found that this two steps are enough for fitting of $1/f$ noise data measured on *SiGe* metamorphic p-MOSFETs with high *Ge* content (samples k5888, k5889, c2154 and c2321). The $1/f$ noise data measured on Si MOSFETs and pseudomorphic p-$Si_{0.67}Ge_{0.33}$ MOSFET have not fitted only by CNF and SDRF components and fitting procedure required more steps. It was found that $1/f$ noise on these MOSFETs well described with enough accuracy by CNF, CMF and SDRF components. HMF on source-drain conductance dependence closes to $(S_{I_D})_{HMF} \sim R_{SD}$ when $(S_{I_D})_{SDRF} \sim R_{SD}^3$ and $(S_{I_D})_{CMF}$ vary R_{SD}^2 at high currents. HMF component of noise can not describe $1/f$ noise of investigated devices at high overdrive gate voltage as well as CMF and SDRF components.

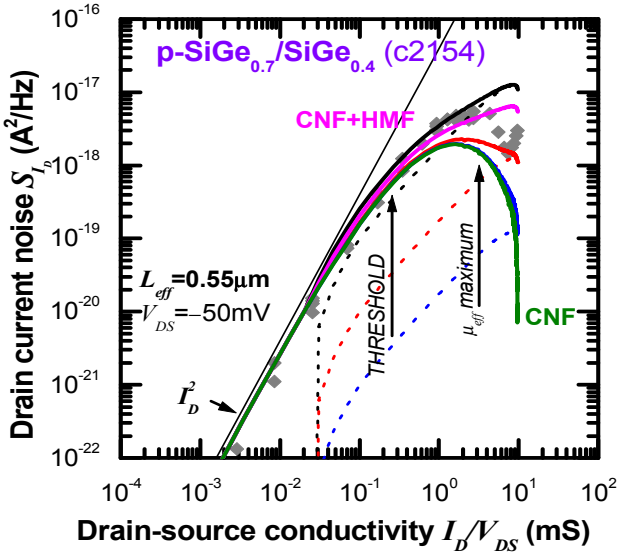

Figure 4.17: Fitting procedure of NPSD S_{I_D} to extract HMF noise component. The Drain current $1/f$ noise NPSD on source-drain conductance dependence for c2154 MOSFET with gate length $L = 1.0\ \mu$m at $f = 1$ Hz (symbols), fitted by CNF and HMF components (lines). Dotted lines are HMF component with Hooge parameter $\alpha_H = 10^{-6}, 10^{-5}, 10^{-4}$. Solid lines is CNF+HMF components with $\alpha_H = 0, 10^{-6}, 10^{-5}, 5\times10^{-5}, 10^{-4}$.

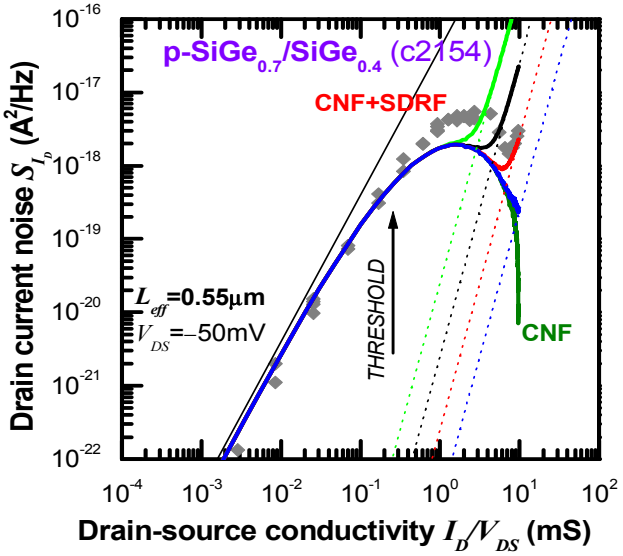

Figure 4.18: Fitting procedure of NPSD S_{I_D} to extract SDRF noise component. The Drain current $1/f$ noise NPSD on source-drain conductance dependence for c2154 MOSFET with gate length $L = 1.0\ \mu$m at $f = 1$ Hz (symbols), fitted by CNF and SDRF components (lines). Dotted lines are SDRF component with parameter $S_{R_{SD}} = 10^{-8}, 10^{-7}, 10^{-6}, 10^{-5}\Omega^2/\text{Hz}$. Solid lines is CNF+SDRF components with $S_{R_{SD}} = 0, 10^{-8}, 10^{-7}, 10^{-6}, 10^{-5}\Omega^2/\text{Hz}$.

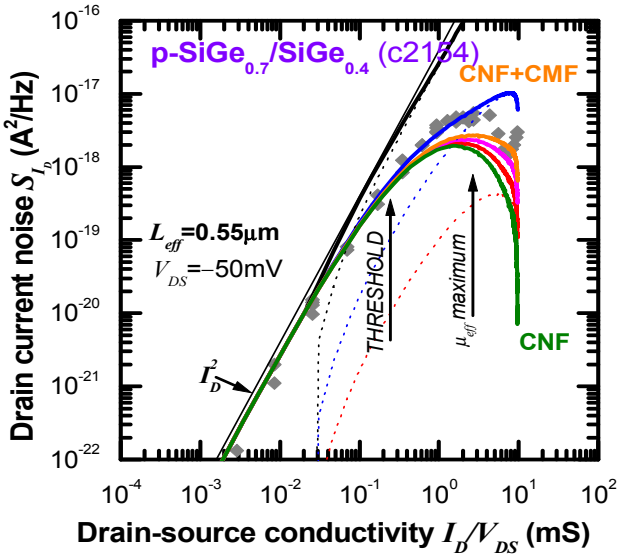

Figure 4.19: Fitting procedure of NPSD S_{I_D} to extract CMF noise component. The Drain current $1/f$ noise NPSD on source-drain conductance dependence for c2154 MOSFET with gate length L = 1.0 μm at f = 1 Hz (symbols), fitted by CNF and CMF components (lines). Dotted lines are CMF component with Coulomb scattering parameter $\alpha = 10^3, 10^4, 10^5$ Vs/C. Solid lines is CNF+CMF components with $\alpha = 0, 10^3, 2\times10^3, 10^4, 10^5$ Vs/C.

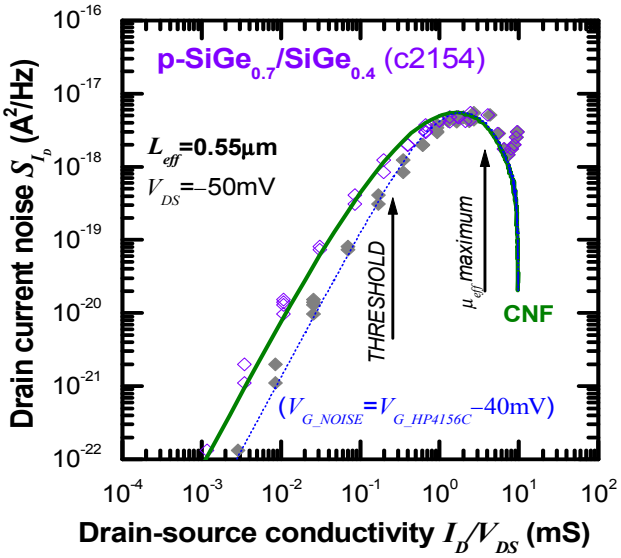

Figure 4.20: Fitting procedure with gate voltage offset correction of NPSD S_{I_D} to extract CNF noise component. The Drain current $1/f$ noise NPSD on source-drain conductance dependence for c2154 MOSFET with gate length L = 1.0 μm at f = 1 Hz (symbols), fitted by CNF (lines) with gate voltage offset correction. Filled symbols are measured data before correction, open symbols are measured data after corrections.

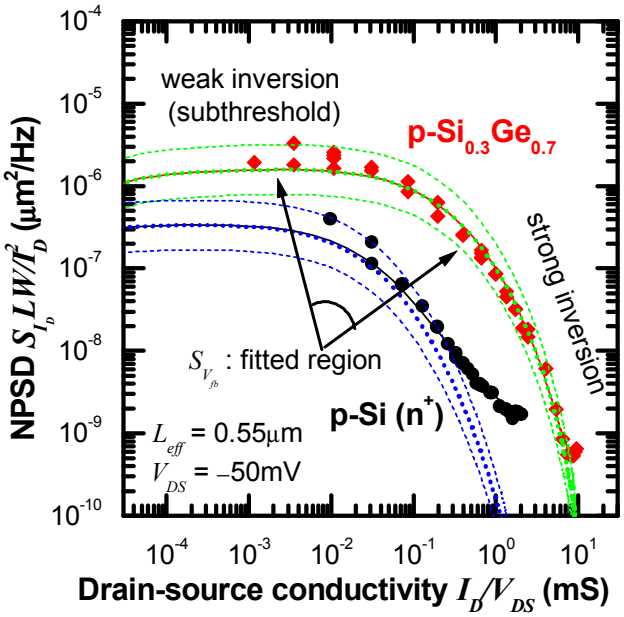

Figure 4.21: The Drain current $1/f$ noise NPSD on source-drain conductance dependence fitting in subthreshold and V_G just above threshold for *p-Si*$_{0.3}$*Ge*$_{0.7}$ (c2154) and *p-Si* (Sotton, w6) MOSFETs with gate length $L = 1.0\ \mu$m at $f = 1$ Hz. The CNF component with optimal $S_{V_{fb}}$ parameter and $2 \times S_{V_{fb}}$, $0.5 \times S_{V_{fb}}$ parameters are shown (dotted lines).

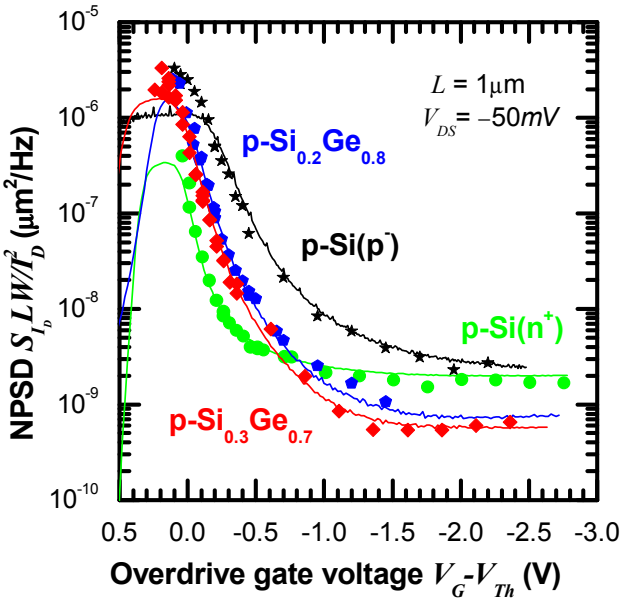

Figure 4.22: A typical NPSD S_{I_D}/I_D^2 of drain current fluctuations in $1/f$ region versus overdrive gate voltage for p-Si$_{0.3}$Ge$_{0.7}$ (c2154), p-Si$_{0.2}$Ge$_{0.8}$ (k5888) and p-Si(p$^-$) (Daimler), p-Si(n$^+$)(Sotton, w6) MOSFETs MOSFET with gate length $L = 1.0\ \mu$m.

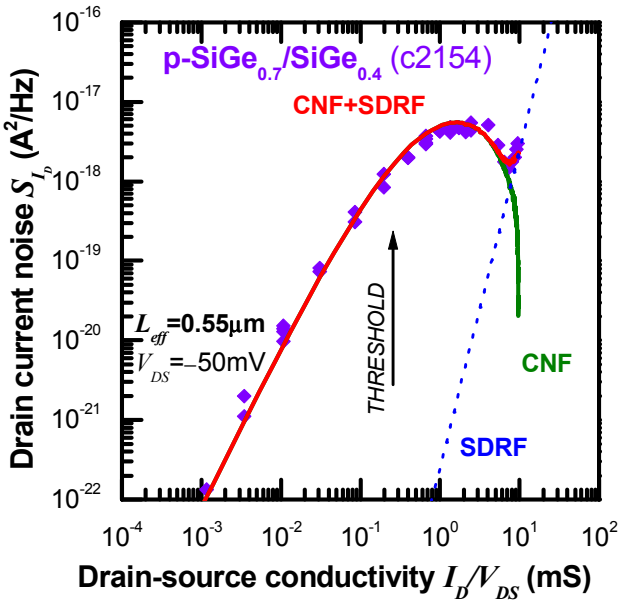

Figure 4.23: The Drain current $1/f$ noise NPSD on source-drain conductance dependence for c2154 MOSFET with gate length $L = 1.0$ μm at $f = 1$ Hz, fitted by CNF and SDRF components after gate voltage offset correction.

The spectral density of the source-drain series resistance we defined by:

$$S_{R_{SD}} = \alpha_{H\_SD} \frac{R_{SD}^2}{f N_{SD}} \sim \frac{R_{SD}^3}{f} \tag{4.9}$$

where α_{H_SD} is the Hooge parameter for $1/f$ noise in the series resistance, N_{SD} is the total number of free carriers in source and drain area and R_{SD} is the source-drain series resistance.

CMF can be important in weak inversion at low and high gate overdrive voltage of MOSFET operation. Typically, SDRF can appear only at the highest gate voltages for the shortest channel lengths, when the channel resistance becomes comparable to the source-drain series resistance.

Fig. 4.24 shows how measured and calculated PSD vary with device conductance for the p-Si MOSFET. This curve was very well fitted by CNF, CMF and SDRF using equation (4.8). The Coulomb scattering coefficient $\alpha = 8\times10^4$ Vs/C extracted from the fitting of experimental data for p-Si MOSFET is close to the predicted value of 10^5 Vs/C for holes [126]. It is comparable to Coulomb scattering coefficient $\alpha^{PM_{Si\_cap}}$ for the Si-cap of pseudomor-

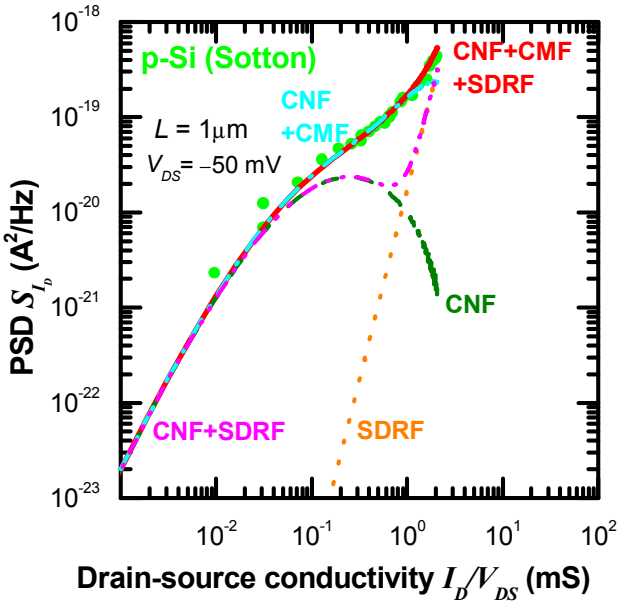

Figure 4.24: The Drain current $1/f$ noise NPSD on source-drain conductance dependence for p-Si (Sotton, w6) MOSFET with gate length L = 1.0 μm at f = 1 Hz, fitted by CNF, CMF and SDRF components.

phic p-SiGe devices and much bigger than for SiGe channels of the same pseudomorphic p-SiGe MOSFETs $\alpha^{PM_{SiGe}} =\sim 0.1 \times \alpha^{PM_{Si\_cap}}$ (see chapter 2, subsection 2.4.12, [127] and Table 4.2). The Coulomb scattering coefficient $\alpha = 5\times10^3$ Vs/C extracted from the fitting of experimental data for pseudomorphic p-$Si_{0.67}Ge_{0.33}$ MOSFET is agree with results obtained in [127].

Fig. 4.23 and Fig. 4.25 shows the variation of PSD with device conductance for the p-$Si_{0.3}Ge_{0.7}$ and p-$Si_{0.2}Ge_{0.8}$ MOSFETs respectively. The $1/f$ noise characteristics of both are completely explained by CNF and SDRF, which reduces Eq. (4.8) for the NPSD to:

$$S_{I_D}/I_D^2 = \left(\frac{g_m}{I_D}\right)^2 S_{V_{fb}} + \left(\frac{I_D}{V_{DS}}\right)^2 S_{R_{SD}} \tag{4.10}$$

For our metamorphic p-SiGe MOSFETs a CMF component was not observed ($\alpha \ll 5 \times 10^2$ Vs/C) (Fig. 4.23 and Fig. 4.19) due to the presence of thin Si cap layer ($4-5$ nm) between the SiGe channel and the Si-SiO_2 interface. The SDRF component dominated in strong inversion for all the measured devices, and its value is 10-100 times lower in metamorphic p-SiGe MOSFETs than in p-Si due to their lower source-drain access resistance.

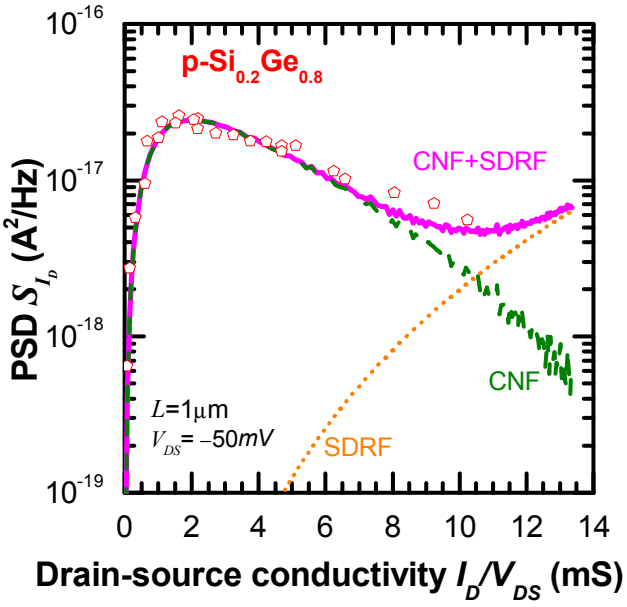

Figure 4.25: The Drain current $1/f$ noise NPSD versus source-drain conductance for k5888 MOSFET with gate length L = 1.0 μm at f = 1 Hz.

4.3.3 Influence of Si cap layer on $1/f$ noise for high Ge content SiGe p-MOSFETs on Virtual Substrate (VS)

There are several ways for influence of Si cap layer on $1/f$ noise of p-SiGe MOSFETs. The first way is reduction of carriers tunneling probability from SiGe channel to traps in oxide. This effect is not physical due to relatively big thickness of Si cap in comparison with tunneling atenuation distance and only light reduction of $1/f$ noise in p-SiGe MOSFETs. Second, the carriers could tunnel from SiGe channel on traps in Si cap for p-SiGe MOSFETs and from Si body to traps in SiO_2 for p-Si MOSFETs. Third, the separation between the quasi-Fermi level of holes and the valence band edge at the Si/SiO_2 interface is higher for SiGe device at the same gate overdrive, and traps density in oxide could increase rapidly neare the valence band edge in SiO_2. And forth, the Coulomb scattering rate of carriers in the SiGe channel on fluctuating centres in oxide is reduced due to separation of carriers from Si/SiO_2 interface.

Si cap thicknesses used in our devices relatively wide for tunneling process, even tunneling barrier is reduced from $\sim$4 eV for Si/SiO_2 interface to $\sim$ 300meV for SiGe/Si interface. So, we should observed apparent $1/f$ noise reduction for all p-SiGe MOSFETs especially in

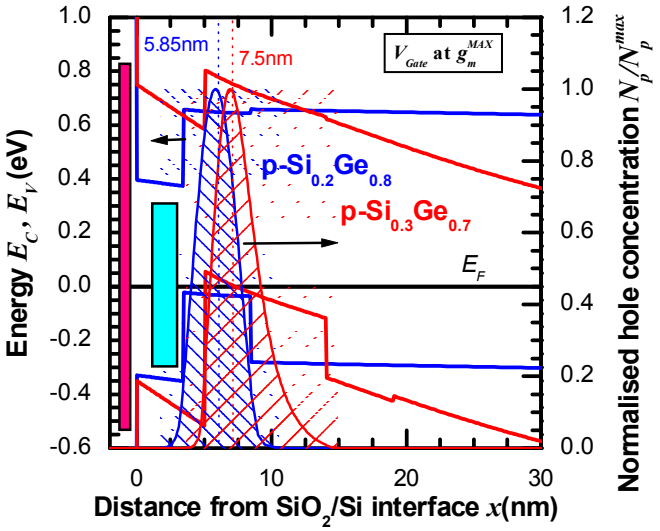

Figure 4.26: Calculated band diagram and hloe concentration for p-$Si_{0.3}Ge_{0.7}$ (c2154) and p-$Si_{0.2}Ge_{0.8}$ (k5888) MOSFETs at gate overdrive bias, which is correspond to maximum transconductance.

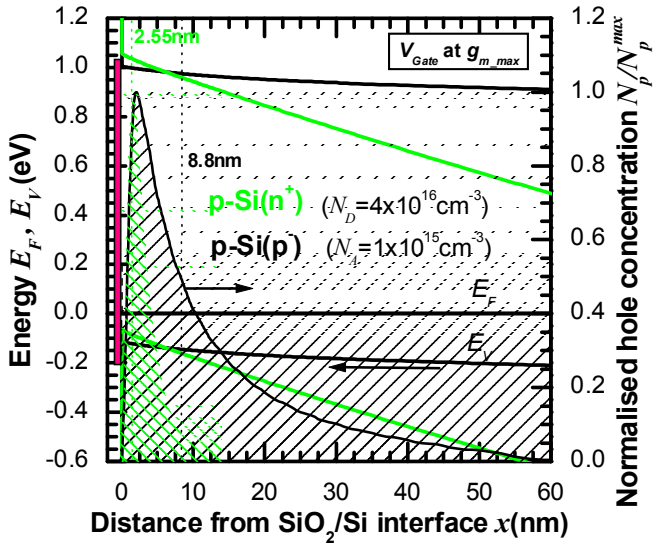

Figure 4.27: Calculated band diagram and hole concentration for p-Si(p^-) (Daimler Si) and p-Si(n^+) (Sotton Si, w6) (c2154) and p-$Si_{0.2}Ge_{0.8}$ (k5888) MOSFETs at gate overdrive bias, which is correspond to maximum transconductance.

subthreshold region, where only CNF mechanism present and third and forth mechanisms of flatband voltage fluctuations are unimportant. However, this prediction is in contradiction with our measured results. Tunneling on traps in Si cap together with first mechanism should reduce $1/f$ noise proportionally at all biasing regions. So, first two mechanisms can not explain noise NPSD reduction for metamorphic p-SiGe MOSFETs in comparison with NPSD for p-Si controls at high gate overdrive and the same or increased level for p-SiGe devices in subthreshol. Third mechanism required variation of traps density with distance from Si/SiO_2 interface, which should be clearly seen on measured results as GR bumps or significantly increased of noise exponent. Model, which describe Coulomb scattering rate reduction, has not disadvantages discribed above and fitting, which is carried out for samples (subsection 4.3.2), point to its sutability. Coulomb scattering coefficient should depend on distance from main carriers to Si/SiO_2 interface and also on presence of additional screening carriers between the interface and main carriers. The CMF are important component in $1/f$ noise when device already operate in strong inversion, however, channel resistance still much higher than source and drain access resistance. So, influence of CMF component on noise at gate overdrive bias, which is correspond to maximum transconductance, is proposed for comparison of devices with different design.

Fig. 4.26 shows calculated band diagram and hole concentration for the p-$Si_{0.3}Ge_{0.7}$ and p-$Si_{0.2}Ge_{0.8}$ MOSFETs at gate overdrive bias, which is corresponds to maximum transconductance. Fig. 4.27 shows calculated band diagram and hole concentration for the p-Si(p^-) and p-Si(n^+) MOSFETs. It is clearly seen that Coulomb scattering coefficient decreased, when distance from main carriers in the channel to fluctuating traps increased. Hence, increased Si cap thickness will reduce CMF noise component. The same time, if Si cap thickness will be increased very much, cap will be filled by carriers in device operating regime and CMF component of noise will be significantly increased in drain current component, which is flow in the Si cap. Increased Si cap thickness also increase short channel effects and decrease device performance due to decreased gate to channel capacitance.

Metamorphic p-SiGe heterostructures with high Ge content are more preferred to design low noise MOSFET devices than pseudomorphic heterostructures due to large difference between carriers mobility in Si cap and SiGe channel and also large valence band offset between Si cap and SiGe channel. Si cap of metamorphic MOSFETs start to fill by carriers

later than Si cap of pseudomorphic MOSFETs and drain current component in Si cap is less important for metamorphic MOSFETs.

4.3.4 Influence of "punch-through" stopper doping on 1/f noise for conventional Si and SiGe on VS p-MOSFETs

In order to reduce channel length we should prevent significantly increased influence of short channel effects. Widely used way to reduce short channel effects is to uise heavy doped n^+ substrate or specially introduced n^+ doped "punch through" stopper layer for p-type MOSFETs (see subsection 4.2.1).

Introduction of PTS or heavy doped substrate increase vertical electric field in heterostructure and place carriers more close to Si/SiO_2 interface (Fig. 4.27 and 4.26). Parameters extracted from 1/f noise (subsection 4.3.2 and table 4.2) show no direct dependence of CNF and SDRF component on presence of PTS or heave doped substrate. Coulomb scattering coefficient, which is used for CMF noise component, for heavy doped p-Si(n^+) MOSFETs dramatically increased in comparison with lightly p-type doped p-Si(p^-) MOSFET and close to its theoretical limit [126].

Table 4.2: Noise components extracted for p-MOSFETs from LF noise fit.

Sample	S_{Vfb}	α_C	S_{Rsd}	λN_t^{MIN}	λN_t^{MAX}
	V^2Hz^{-1}	VsC^{-1}	Ω^2Hz^{-1}	$eV^{-1}cm^{-2}$	$eV^{-1}cm^{-2}$
C2154	4.00E-11	0	1.20E-07	5.00E+09	1.00E+10
K5888	8.00E-11	0	8.00E-08	8.00E+09	1.20E+10
C2321	4.00E-11	0	8.00E-08	2.00E+09	5.00E+09
p-Si (p^-)	3.00E-10	5.00E+03	1.3E-05	1.20E+10	3.30E+10
p-Si (n^+)	5.00E-12	8.00E+04	7.00E-06	4.00E+08	6.00E+08
p-$Si_{0.67}Ge_{0.33}$	3.20E-12	5.00E+03	2.30E-07	2.00E+08	4.50E+08

Opposite to the case of conventional p-Si MOSFETs, introduction of PTS for p-SiGe MOSFETs with high Ge contain on VS has not increase Coulomb scattering coefficient so apparently and CMF component for investigated p-SiGe Daimler Chrysler MOSFETs has not observed ($\alpha_{SiGe} \ll 5 \times 10^2$ VsC^{-1}, which is lower than experimental error) in device operational bias range. Very reduced CMF noise component ($\alpha_{SiGe} \approx 3 \times 10^3$ VsC^{-1}) was extracted for pseudomorphic p-$Si_{0.67}Ge_{0.33}$ MOSFET, which can be associated with thin Si cap or presence of carriers in Si cap. These results agreed withresults published by

Ghibaudo [127].

4.3.5 Extraction of interface trap density from measured 1/f noise

The origin of flat band voltage fluctuations will be discussed in section 4.4.4. Most published up to date papers conclude that it is due to carriers trapping-detrapping processes on traps placed at semiconductor/insulator interface. This model described in section 2.4.7.1. The flat band voltage PSD depends on density of traps near the Si/SiO_2 and/or Si/SiGe interface (subsection 2.4.7.1). Absence of CMF component of 1/f noise in our metamorphic p-SiGe MOSFETs (section 4.3.2) pointed on absence of traps at Si/SiGe interface or its unimportance for flat band voltage fluctuations.

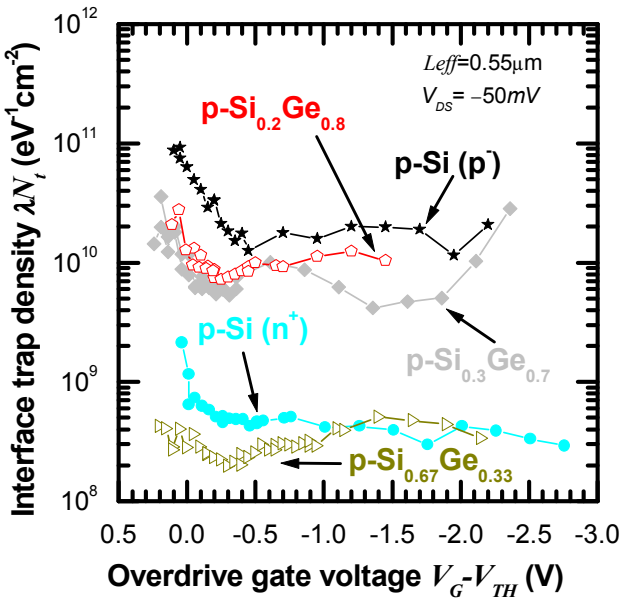

Figure 4.28: Interface trap density extracted from LF noise measurements versus overdrive gate voltage for p-$Si_{0.2}Ge_{0.8}$ (k5888), p-$Si_{0.3}Ge_{0.7}$ (c2154), p-Si (n^+) (Sotton, w6), p-Si (p^-) (Daimler) and p-$Si_{0.67}Ge_{0.33}$ (Sotton, w1) MOSFETs.

So, we can extract density of traps near the Si/SiO_2 interface N_{st} from given $S_{V_{fb}}$using measured oxide capacitance C_{ox} with help of equation (2.75):

$$N_{st} = \frac{WLC_{ox}^2 f^{\gamma}}{q^2 k_B T} S_{V_{fb}} \tag{4.11}$$

Very often authors [128, 129, 130] use equivalent input gate voltage noise S_{V_G} against

$S_{V_{fb}}$ to extract N_{st}. This is corresponding to $1/f$ noise with just one CNF component. However, if we do not take into account CMF and SDRF components, the N_{st} increases several orders of magnitude with overdrive gate voltage increasing. This is in contradiction with experimentally measured $1/f$ spectra at LF (see sections 2.4.7.1, 2.4.11.1, 4.3.1).

The traps density near the Si/SiO_2 interface N_{st} extracted from $S_{V_{fb}}$ obtained after fitting procedure (described in section 4.3.2) for different samples are shown in Fig 4.28. It is clearly seen that trap density varies very lightly with overdrive gate voltage.

Absolute values of N_{st} is two orders of magnitude lower than interface charge values extracted from C-V measured (see section 4.2.3). This behaviour is also was observed by other authors [131, 132, 133]. So, we can conclude that traps involved to noise generation due to flat band voltage fluctuations and traps, which are increase quasi-static gate-to-body capacitance of device, are different or expressions (2.75) and (4.11) should be corrected.

4.3.6 Extraction of contact resistance from LF noise measurements

The SDRF component dominated in strong inversion for all the measured devices, and its value is 10-100 times lower in metamorphic p-SiGe MOSFETs than in p-Si due to their lower source-drain access resistance. Contact resistance estimated from SDRF component decreased with Ge content increasing (Table 4.3).

Table 4.3: Source-drain resistance R_{SD} extracted from I-V and R_{SD} estimated from LF-noise results.

Sample	S_{Rsd}	R_{SD}/R_{SD_C2154}	R_{SD} (LF-noise)	R_{SD} (R vs L)
	$\Omega^2 \cdot Hz^{-1}$		$\Omega \cdot \mu m$	$\Omega \cdot \mu m$
C2154	1.2×10^{-7}	1.00	2025†	2025
K5888	8.0×10^{-8}	0.87	1769	2300
p-Si (n^+)	7.0×10^{-6}	3.88	7854	4680
p-$Si_{0.67}Ge_{0.33}$	2.3×10^{-7}	1.24	2515	4400

† - resistance 2025 $\Omega\mu$m of sample C2154 (p-$Si_{0.3}Ge_{0.7}$) measured on DC (R vs L method) [35] was used as a reference to estimate resistance from LF-noise measurements. R_{SD} (R vs L) was obtained as a point of cross-section of lines drawn through points $R(V_G)$ for devices with different gate length L at several fixed gate voltages V_G (R vs L method) [35]. R_{SD} values for samples p-Si (n^+) and p-$Si_{0.67}Ge_{0.33}$ [115] are also shown for comparison.

R_{SD} (noise) was calculated using equation (2.98) with suggestion that shape of contact areas

(L_{SD} – effective length of contacts area) the same or very similar, and Hooge parameter multiplied to mobility of carriers in contact area $\alpha_{H\_SD} \times \mu_{SD}$ are similar. This product also known as "noise reduced mobility" can be used as quality indicator of material in contact area [134]. R_{SD} obtained from I-V (section 4.1.3) for sample c2154 (see table 4.1) was used as a reference for R_{SD} extraction from noise for all other devices (table 4.3).

In order to check our conclusions, we can estimate Hooge parameter from measured SDRF component. The normalised noise PSD generated in access resistance of p-$Si_{0.7}Ge_{0.3}$ (c2154) MOSFET is $S_{I_D}/I_D^2 R = 8\times10^{-14}\ \Omega^{-1}\mathrm{Hz}^{-1/2}$. If we estimate the Hooge parameter using contact extentions length $L_{SD} \approx 5\ \mu$m and $\mu_{SD} \approx$ 10-100 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, then we obtain the reasonable value $\alpha_H \approx 10^{-2}$-10^{-3} for contact areas.

R_{SD} extraction procedure from LF-noise requires just one device to measure and one reference device. Results estimated from LF-noise are applied to individual measured device opposite to set of devices in conventional R_{SD} vs L method.

4.4 Temperature dependence of I-V and LF noise characteristics

The low temperature measurements have been carried out in liquid nitrogen (T= 77K).

4.4.1 I-V characteristics of p-SiGe MOSFETs on VS at T=77K

The input I-V characteristics for the p-$Si_{0.3}Ge_{0.7}$ MOSFET at T= 77K in comparison with characteristics at room temperature T= 293K are shown in Fig. 4.29. The threshold voltage V_{TH} is lightly increased with temperature decreasing to 77K. The maximum transconductance g_m and maximum drain current I_D at 77K in linear regime was increased 2.8 and 1.6 times respectively in comparison with it's value at 293K. The maximum transconductance g_m and maximum drain current I_D at 77K in saturation was increased 1.4 and 1.3 times respectively in comparison with it's value at 293K.

The increasing of maximum g_m and I_D can be explained by increased carriers mobility in heterostructure at low temperature. The same time, maximum I_D increased less than maximum g_m due to contact resistance influence on I-V characteristics. The series resistance is subject to two opposing factors: (i) increase of mobility (via reduced phonon scatter-

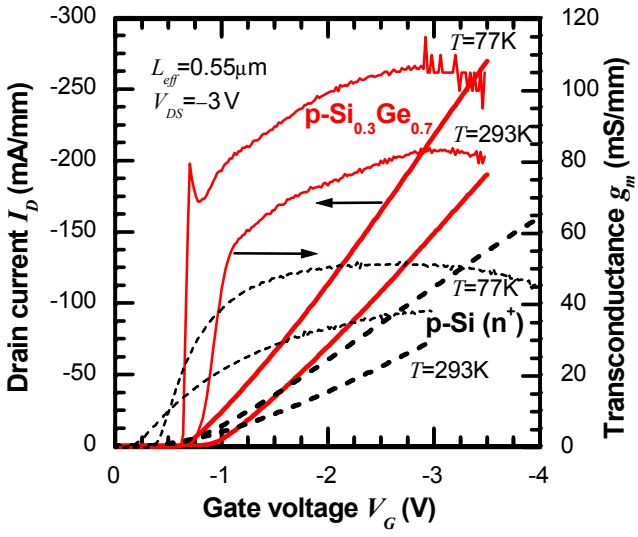

Figure 4.29: Drain current I_D (thick lines) and transconductance g_m (thin lines) versus gate voltage for p-$Si_{0.3}Ge_{0.7}$ (c2154, solid lines) and p-Si (Sotton, w6, dashed lines) MOSFETs with gate length 1 μm at room (T= 293K) and nitrogen (T= 77K) temperatures.

ing) which lowers the resistivity of the drift region and (ii) impurity freeze-out in depletion regions and extension of the depletion depth which tends to increase R_{SD}. Source-drain access resistance for c2154 MOSFETs was estimated as $R_{SD} \approx 2.9\ \mathrm{k\Omega} \times \mu\mathrm{m}$ at $T = 77$ K.

4.4.2 "Punch-through" stopper and "kink" effect on output I-V characteristics at $T = 77$ K

The self-heating effect, which is responsible for the mobility degradation, threshold voltage lowering and negative differential conductance, was observed in all high Ge content metamorphic Si-Ge MOSFETs with gate length below 2 μm at high V_{DS} at $T = 77$ K. "Kink" effect (Fig. 4.30) was clearly observed at low temperature (77K) for devices with punch-through stopper (p-$Si_{0.3}Ge_{0.7}$). It is due to majority carriers, generated by impact ionisation, which collect in the body and increase the body potential (lower threshold voltage). This behaviour of our devices is similar to partially depleted silicon-on-insulator (SOI) MOSFETs [136]. For devices without punch-through stopper (p-$Si_{0.2}Ge_{0.8}$) "kink" effect was not observed. Moreover, typically these MOSFETs were "killed" just after impact ionisation process was started. It can be explained due to minority carriers generated during the impact ionisation, which are not removed from drain depletion area and in-

creased the device breakdown probability in the case of "punch through" stopper absence. So, "punch through" stopper can improve device reliability not only due to vertical electric field increasing and off current decreasing, but also due to increasing reliable maximum supplied drain-source voltage.

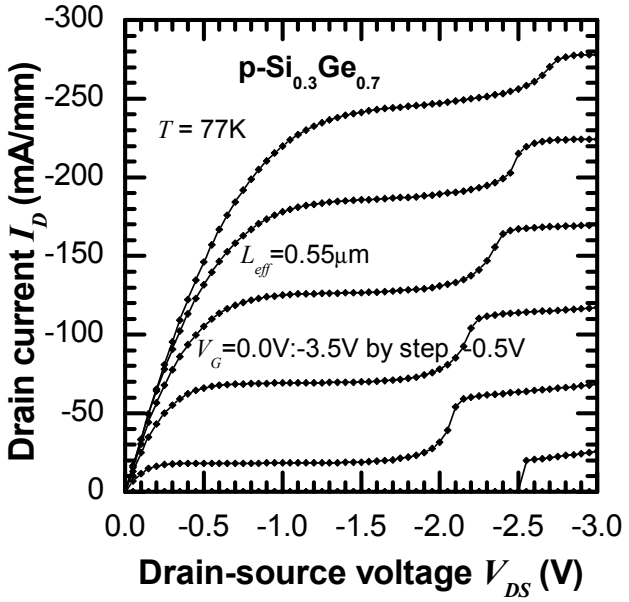

Figure 4.30: Kink effect on output I-V characteristics of p-$Si_{0.3}Ge_{0.7}$ (c2154) at $T = 77$ K.

4.4.3 Low frequency noise of p-SiGe MOSFETs on VS at T=77K

Drain current LF noise PSD versus source-drain conductance for the p-$Si_{0.3}Ge_{0.7}$ (c2154) MOSFET at T= 77K in comparison with LF noise PSD at room temperature T= 293K are shown in Fig. 4.31. It is clearly seen that PSD of CNF component increased with temperature decreased, which can be partially explained by drain current increased at nitrogen temperature. PSD of SDRF component also increased with temperature decreased. Access resistance estimated from LF noise at $T = 77$ K with the help of method described in subsection 4.3.6 is several orders of magnitude (≈ 140 times) higher than access resistance at $T = 293$ K, which is in contradiction with results obtained in subsection 4.4. It can be explained by the fact that SDRF component at low temperatures generated mainly in source and drain depletion areas, where impurities easy freeze out and diffusion length decreased. Depletion areas still uncontrolled by gate bias due to high parallel electric fields here. At

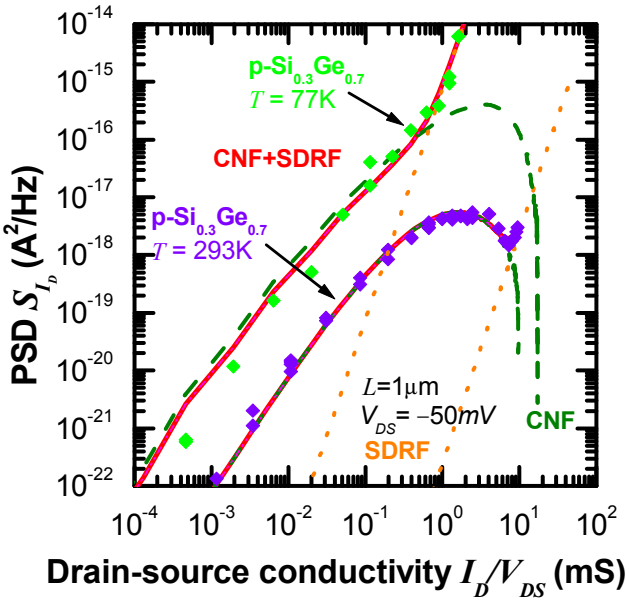

Figure 4.31: Drain current LF noise PSD versus source-drain conductance for the p-$Si_{0.3}Ge_{0.7}$ (c2154) MOSFET with gate length L=1μm at $T = 77$ K in comparison with LF noise PSD of the same MOSFET at room temperature $T = 293$ K.

room temperature, influence of depletion areas on SDRF component of noise is less than influence of doped contact areas, which allow to use approximation described in subsection 4.3.6.

Slow trap density extracted for the p-$Si_{0.3}Ge_{0.7}$ (c2154) MOSFET at $T = 77$ K (see Fig. 4.32) with help of McWhorter model (subsection 2.4.7.1) is higher than slow trap density extracted for the same MOSFET at $T = 293$ K and comparable with interface trap density extracted form C-V (subsection 4.2.3). So increased PSD of CNF component at $T = 77$ K can not be explained only with the help of increased MOSFET drain current at $T = 77$ K.

This behaviour could be explained by gate dielectric mobile carriers influence on flat band voltage fluctuations. Mobile carrier concentration decreased exponentially with temperature decreased. As well as mobile carrier concentration, gate leakage current also decreased with temperature decreased. So, model described in subsection 2.4.7.3 can be useful in description CNF noise component.

Another possible reason of decreased flat band voltage fluctuations $S_{V_{fb}}$ at room temperature in comparison with $S_{V_{fb}}$ at low temperatures is screening of tunnelled charge by mobile

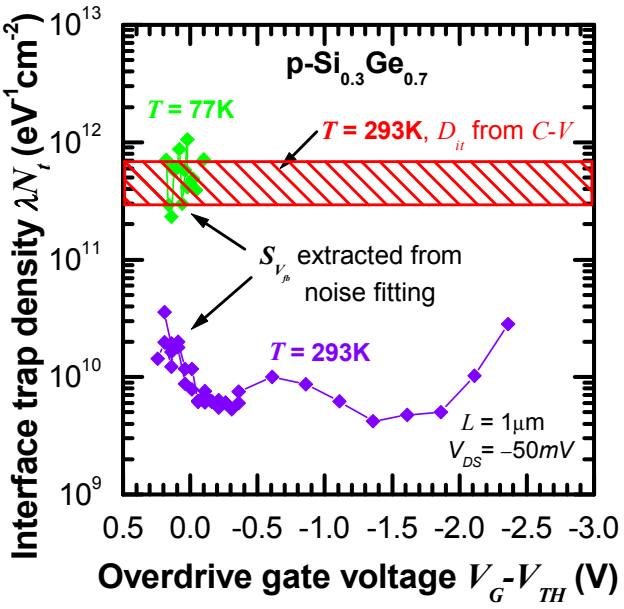

Figure 4.32: Slow trap density extracted for the p-$Si_{0.3}Ge_{0.7}$ (c2154) MOSFET at T= 77 K and T= 293 K with help of Mc'Whorter model. Oxide trapped charge density D_{it} extracted from high frequency and quasystatic C-V at T= 293 K is also shown for comparison (red area).

charge in gate dielectric due to polarization effect.

4.4.4 Origin of flat-band voltage fluctuations: trapping-detrapping, thermal activation processes and mobile charge

Several models were proposed to describe of carrier number fluctuations origin in section 2.4.7. Interface trap densities extracted from LF noise (section 4.3.5) with help of McWhorter model described in subsection 2.4.7.1 have values less than extracted from C-V (section 4.2.3). The McWhorter model, thermal activation model (subsection 2.4.7.2), and capacitance fluctuation model (subsection model 2.4.7.4) can not explain temperature dependance of PSD in subthreshold MOSFET operation region (section 4.4.3). It can be explained with the help of model described in section 2.4.7.3 or with help of McWhorter model modification to take into account mobile charge influence.

So, the question about origin of CNF noise component in subthreshold regime of MOSFET operation is still open. In my opinion all three mechanisms, charge trapping-detrapping on traps in gate dielectric, thermal activation processes and mobile charge influence on noise

are important. Clear separation of each mechanism and its influence on flat band voltage fluctuations require further investigation.

Chapter 5

MOSFET design and further work

Knowledge described in chapter 2 and data obtained for investigated devices in chapter 3 can be used to design next generation of p-MOSFET devices. The 50-100nm gate length p-MOSFET design presented in this chapter should solve at least part of problems pointed and discussed in previous chapters. Schematical structure of designed device, which will be described below, shown on Fig. 5.1.

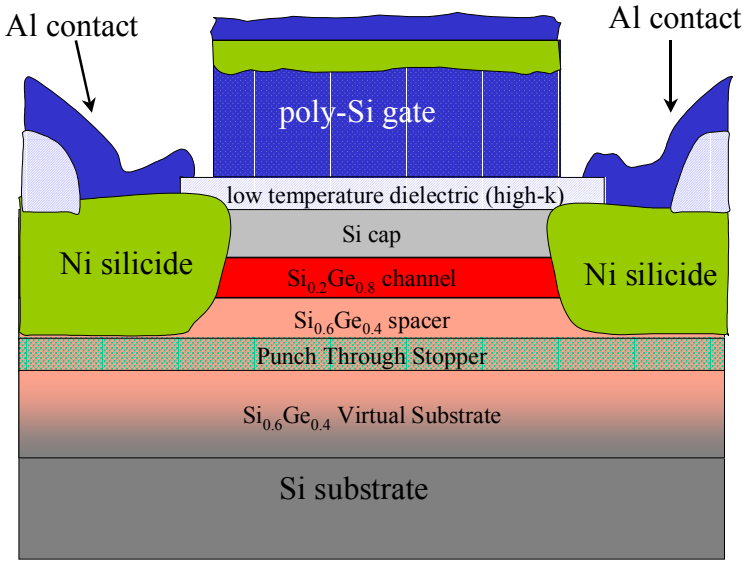

Figure 5.1: The schematical structure of a designed p-type metamorphic SiGe MOSFET.

5.1 Heterostructure

It was found that high Ge content strained channel grown on virtual substrate show very good performance in carriers mobility and output drain current. Myronov *et al* [137, 138]

noted that the best enhancement in hole mobility should be observed for strained p-$Si_{0.2}Ge_{0.8}$ layer on relaxed p-$Si_{0.7}Ge_{0.3}$ buffer with thickness of channel not more than 10-15 nm. I propose to use p-$Si_{0.6}Ge_{0.4}$ VS to reduce strain between strained p-$Si_{0.2}Ge_{0.8}$ channel and Si cap (see critical thickness in chapter 2, section 2.1.1). These conclusions also agreed well with our results for k5888, k5889 and c2154 MOSFETs. PTS, which is used for c2154 MOSFETs, can be well used to reduce short channel effects as it shown in chapter 5. However, increased Ge content in relaxed VS also increases Sb and P diffusion [139, 140, 141] in this layer during fabrication and their segregation [142, 143] during MBE growth. Simulation of Sb diffusion carried out for designed heterostructure show that better to use PTS layer with highest Sb content separeted from channel by thick p-$Si_{0.6}Ge_{0.4}$ spacer layer. So, we propose to use grown by PECVD 3-5μm p-$Si_{0.6}Ge_{0.4}$ VS, overgrown on top of relaxed p-$Si_{0.6}Ge_{0.4}$ buffer layer with 10^{18}-10^{19}cm^{-3} Sb doped 50 nm PTS, 30 nm relaxed p-$Si_{0.6}Ge_{0.4}$ spacer, 10nm strained p-$Si_{0.2}Ge_{0.8}$ channel layer and 5-8 nm Si cap layer. All structure should be grown at low thermal budget (maximum temperature less than 750K). All fabrication steps should also use low thermal budget and RTA, when it is possible, to prevent Ge out-diffusion from p-$Si_{0.2}Ge_{0.8}$ channel to Si cap and Sb diffusion to p-$Si_{0.2}Ge_{0.8}$ channel [137, 144].

5.2 Gate dielectric

The conventional high temperature oxidation of Si cap is unsuitable for heterostructure described in 5.1. Remote plasma CVD oxide [145] and LE-PECVD oxide [112] used for investigated devices also shown not perfect quality. Hence, we should try to use alternative gate dielectrics. Dielectric should be chosen taking into account low thermal budget required (5.1) and compromising dielectric volumetric and dielectric-to-Si cap interface quality. The dielectric capacitance should be 0.9-2 μFcm^{-2} and the equivalent SiO_2 thickness should be in range 2-4nm.

Thorough analysis of available fabrication technologies was done for SiO_2 [7, 146, 147, 148, 155, 156] and also high-k dielectrics [149, 150, 151, 9, 152, 154]. It can be concluded that most high-k dielectrics available at the moment provide very poore dielectric/Si interface quality . Most technologies available for SiO_2 fabrication required high thermal

budget or also provide poore SiO_2 quality. The atom layer deposited Al_2O_3 [153, 154] or SiO_2 obtained by low thermal budget pyrogenic ("wet") Si oxidation in hydrogen and oxygen atmosphere [155, 156] can be used for presented design as a compromising variants. Unfortunately, these technologies add additional cost to device fabrication process. Another available technologies are the low temperature Si oxidation as the enhancement of conventional oxidation process [157] or N_2O annealed LE-PECVD grown SiO_2 [112]. Specially designed composite SiO_2-high-k dielectric also can be used to improve MOSFET LF-noise due to reduction CMF noise component [158].

5.3 Gate material

The Al metal gate, which was used for investigated devices show very good performance at high frequencies due to low gate access resistance and absence of gate depletion. However, Al metal gate is not self aligned, and it is unsuitable for device fabrication with gate length less than 1 μm due to limited resolution of optical lithography. So, heavily *in-situ* n-type doped self-aligned poly Si gate was proposed for p-MOSFETs designed. Typically used p-type HDD doping of poly Si gate for p-MOSFET strongly decrease the threshold voltage and devices operate in open state at zero gate bias usually. B or BF_2 widely used as acceptor impurity also dramatically decrease SiO_2 quality and heterostructure under oxide [159, 160]. The main reason, which avoids from n-type poly Si gate application for p-MOSFET devices, is gate depletion during the HDD implantation of p-type impurities in device contact areas. This problem can be solved, if silicide contacts will be used in designed device (section 5.4). I propose also start of *in-situ* Sb doping of poly Si gate with short delay after start of poly Si gate growth to prevent fast Sb diffision to gate dielectric.

5.4 Contacts

Conventional contacts for p-MOSFET, which is obtained with the help of HDD p-type doping, is absolutely unsuitable for described design due to required high temperature annealing [161]. It is also required to use p-type doped poly Si gate, which disadvantages described in sec:gate-Design.

Alternative way to make ohmic contacts to heterostructure is using metal silicides [162] with workfunction, which is close to valence band of channel material.

TiSi and CoSi [163] are unsuitable for our heterostructure due to high sacilidisation temperatures and high Si consumption, which is incompatible with shallow contact fabrication process.

NiSi [164, 165] and PtSi [166, 167, 168] can be used for contact fabrication. PtSi has better workfunction allign to SiGe channel valence band, however, PtSi fabrication process has a higher thermal budget, Pt initialise gate dielectric degradation [169] and also extremely high cost.

NiSi contacts fabrication process reliability can be increased with the help of small amount of Pt added to Ni target for evaporator [170, 171, 172]. Sacilidisation process should also improved with help of low energy BF_2 implantation [173] to preamorphisation of contact areas. This implantation step without post annealing improves sacilidisation process due to increased Ni diffusion in damaged crystal SiGe structure.

Introduction of NiSi contacts should decrease resistivity of contact material from 1-2 $m\Omega\times cm$ [22] to $20-40\ \mu\Omega\times cm$ [165]. So access source and drain resistance of designed MOSFET expected to be at least 10 times less then access resistance of investigated devices.

Chapter 6

Conclusions

A detailed characterisation of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) containing high Ge content buried strained $Si_{1-x}Ge_x$ channels, grown on relaxed $Si_{1-y}Ge_y$ virtual substrates (VS) has been carried out.

The solid source molecular beam epitaxy (SS-MBE) was used to obtain two heterostructures c2154 ($x = 0.7/y = 0.4$), c2321(a) ($x = 0.7/y = 0.3$) with 5×10^{17} cm^{-3} Sb *in situ* doped "punch-through" stopper (PTS) layer and one heterostructure c2321(b) ($x = 0.7/y = 0.3$) without PTS layer [111]. This technique maintained the structural integrity of the strained layers and easy incorporated *in situ* doping.

The other three heterostructures k5660 ($x = 0.8/y = 0.5$), k5888 ($x = 0.8/y = 0.5$) and k5889 ($x = 0.9/y = 0.6$) were grown using low energy plasma enhanced chemical vapour deposition (LEPECVD) with high bandwidth of growth rates (0.08 to 5 nm/s) to obtain high quality structures during the short growth time [113], [112].

The fabrication of MOSFET devices was compatible with a 1.0 μm CMOS process for radio frequency (RF) application, but with a reduced thermal budget. Two types of gate oxide was used. Remote PECVD (RPCVD) deposited oxide [125] was used for samples c2154, c2321(a), c2321(b) and PECVD oxide [112] was deposited for samples k5660, k5888, k5889. Metal Al gates were used for all devices to reduce parasitic gate depletion effect and improve MOSFETs performance for RF application.

Electrical characterisation of MOSFETs at $T = 293$ K and $T = 77$ K was completed with the help of current-voltage (I-V), capacitance-voltage (C-V) and low frequency (LF) noise

measurement techniques. The study focuses on MOSFETs LF noise of as the most important factor, which is limit performance of sub-micron gate length devices. All results obtained were compared with characteristics of conventional bulk p-Si MOSFETs and pseudomorphic p-$Si_{0.67}Ge_{0.33}$ MOSFETs [124].

MOSFETs fabricated from both SS-MBE and LEPE-CVD grown heterostructures show very significant hole effective mobility improvement over bulk Si, with peak values of $\mu_{eff} = 760$ cm^{2}V^{-1}s^{-1} at field 0.08 MVcm^{-1} for k5660 sample among devices without PTS and $\mu_{eff} = 500$ cm^{2}V^{-1}s^{-1} at field 0.17 MVcm^{-1} for c2154 devices with PTS.

The current drive enhancement factors of five and two over p-Si MOSFET controls are found for c2154 MOSFET with geometrical gate lengths $L = 10\mu$m and $L = 1\mu$m respectively. The highest drive current among MOSFETs with gate length $L = 1\mu$m (effective gate length $L_{eff} = 0.55\mu$m) is found for k5888 MOSFET, with a current drive enhancement ratio of more than three over the p-Si MOSFET. It shows importance of effective mobility improvement for p-SiGe devices and source-drain access resistance influence for short channel devices. Source and drain access resistance ($R_{SD} \approx 1.5 - 2$ k$\Omega \times \mu$ m) decrease maximum drain current and transconductance at high overdrive gate voltages for 1-0.5 μm gate length MOSFETs. Negative influence of R_{SD} is less for metamorphic p-SiGe devices due to presence high Ge content layers in contact areas in comparison with p-Si devices, where $R_{SD} \approx 4$ k$\Omega \times \mu$ m. So, results demonstrate clearly the potential of using strained c2154 and k5888 heterostructures for the p-MOSFETs in CMOS.

Of the all devices studied the c2154 batch shows much the best performance for a sub-micron $L_{eff} = 0.55\mu$m MOSFETs ($I_{ON}/I_{OFF} = 10^6$ at $V_{DS} = -50$ mV and $I_{ON}/I_{OFF} = 10^4$ at $V_{DS} = -3$ V), mainly due to the incorporation of an Sb-doped PTS. These I_{ON}/I_{OFF} ratios are the same as for Si control with high doped substrate. Devices without PTS has worse short channel properties, however it still work at high drain-source voltages ($I_{ON}/I_{OFF} = (1.0 - 2.5) \times 10^3$ at $V_{DS} = -50$ mV and $I_{ON}/I_{OFF} = 11 - 52$ at $V_{DS} = -3$ V).

The self-heating effect on I-V at high I_D and V_{DS} for metamorphic p-SiGe MOSFETs was observed due to high heat resistance of VS. However, it influence on device performance is insignificant. Impact ionisation processes in drain depletion area of metamorphic p-SiGe MOSFETs were observed at $V_{DS} > 2.5 - 4.0$ V at 293 K. Also, "Kink" effect was clearly observed at low temperature (77 K) for devices with PTS (c2154). It is due to

majority carriers, generated by impact ionisation, which collect in the PTS and increase the body potential (lower threshold voltage). Devices without PTS were "killed" due to oxide breakdown just after impact ionisation was started. So, presence of PTS increases reliable maximum supplied drain-source voltage for MOSFET.

C-V measurements were used to determine the room temperature effective mobility of MOSFETs, depletion and accumulation charge profiles, and interface trap charge densities for investigated MOSFETs. Depletion charge results confirm heterostructure doped profiles used during SS-MBE growth. Active donor's density 3×10^{17} cm^{-3} was found for PTS areas. Background impurity level was estimated as low as $5 \times 10^{15} - 1 \times 10^{16}$ cm^{-3}. Relatively high interface trap densities in the range $3 \times 10^{11} - 4 \times 10^{12}$ cm^{-2}eV^{-1} were extracted for metamorphic p-SiGe MOSFETs, except sample k5660 ($1 \times 10^{11} - 3 \times 10^{11}$ cm^{-2}eV^{-1}), which was fabricated at conditions of less background impurities. It was found, that gate dielectric quality and insulator to semiconductor interface quality of p-SiGe MOSFETs with high Ge content is less favorable than gate insulator quality of conventional p-Si MOSFETs with thermal oxides due to used low thermal budget. The p-SiGe MOSFETs and p-Si MOSFET fabricated using the same thermal budget (k5888, k5889 and p-Si (p^-)) have similar insulator quality.

A significant reduction in low frequency noise normalized power spectral density (NPSD), achieved in metamorphic p-Si/$Si_{1-x}Ge_x$/ $Si_{1-y}Ge_y$ MOSFETs compared to bulk p-Si. This advantage is realised for sub-micron devices relevant to current Si-CMOS technology. In the linear region of MOSFET operation the reduction in $1/f$ noise is greater than a factor of three. PSD in the p-Si MOSFET was well described with the help of carrier number fluctuations (CNF), carrier mobility fluctuations (CMF), and source-drain resistance fluctuations (SDRF) components of 1/f noise. Detail PSD analysis for the buried channel metamorphic p-SiGe MOSFETs showed the absence of CMF LF noise component due to the existence of the Si cap layer, which further separates the holes in the buried $Si_{1-x}Ge_x$ channel from traps near the Si/SiO_2 interface. The obtained results can be also applied to MOSFETs based on any other heterostructures with similar interface properties.

The drain current noise of metamorphic p-SiGe MOSFETs, with shortest gate lengths in strong inversion, is associated with access resistance fluctuations, which are described by an empirical Hooge relation [74] and increased with resistance increasing. This allows extract-

ing access source-drain resistance R_{SD} of investigated MOSFET from LF noise measured at room temperature. R_{SD} extraction procedure from LF-noise requires just one device to measure and one reference device in contrast to the series of devices used for methods based on I-V measurements.

Analysis shown, that LF noise performance of p-SiGe MOSFETs in subthreshold region of MOSFET operation could be also significantly improved, if technology of gate dielectric fabrication for p-SiGe metamorphic MOSFETs will be improved.

Influence of "punch-through" stopper on device reliability was analysed. It reduces short channel effects in sub-micron developed MOSFETs and provides perfect performance of devices especially in the subthreshold region as it is most important for switching devices of CMOS logic. Also $1/f$ noise is not significantly increased in buried channel p-SiGe devises with PTS as in conventional p-Si MOSFETs with heavy doped substrate due to 4-5 nm Si cap used. On the other hand, PTS only lightly decrease maximum current of device. One could reduce this effect through contact shape and doping profile optimisation. Better results could be obtained by using p-SiGe buried channel heterostructures within SOI technology (analogue of fully depleted SOI MOSFETs [136]).

Improved fitting procedure and new useful presentations of measured LF noise PSD (log(PSD) versus drain conductance I_D/V_{DS} and log(PSD) versus $\log(I_D/V_{DS})$) were proposed during LF noise analysis. Preamplifier for LF noise measurements in wide range of MOSFET impedance was developed.

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