ANALYSIS AND DESIGN OF LOW-NOISE AMPLIFIERS IN SILICON-GERMANIUM HETROJUNCTION BIPOLAR TECHNOLOGY FOR RADAR AND COMMUNICATION SYSTEMS

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ANALYSIS AND DESIGN OF LOW-NOISE AMPLIFIERS IN SILICON-GERMANIUM HETROJUNCTION BIPOLAR TECHNOLOGY FOR RADAR AND COMMUNICATION SYSTEMS

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In memory of a great mentor, teacher, and friend:

Dr. Robert E. "Woody" Wood.

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SUMMARY

This thesis presents an overview of the simulation, design, and measurement of state-of-the-art Silicon-Germanium Hetro-Junction Bipolar Transistor (SiGe HBT) low-noise amplifiers (LNAs). The LNA design trade-off space is presented and methods for achieving an optimized design are discussed.

In Chapter 1, we review the importance of LNAs and the benefits of SiGe HBT technology in high frequency amplifier design. Chapter 2 introduces LNA design and basic noise theory. A graphical LNA design approach is presented to aid in understanding of the high-frequency LNA design process. Chapter 3 presents an LNA design optimization method for power constrained applications. Measured results using this design technique are highlighted and shown to have record performance. Lastly, in Chapter 4, we highlight cryogenic noise performance and present measured results from cryogenic operation of SiGe HBT LNAs.

We demonstrate in this thesis that SiGe HBT LNAs have the capability to meet the demanding needs for next generation wireless systems. The aim of the analysis presented herein is to provide designers with the fundamentals of designing SiGe HBT LNAs through relevant design examples and measured results.

CHAPTER I

INTRODUCTION

1.1 Motivation

A key building block in any wireless radar or communication system is the radio-frequency (RF) front-end. These challenging circuits prove to be a limiting factor in restricting bandwidth, range, and sensitivity of RF radar and communication systems. The push for increasingly higher data rates, low-cost technology, and compact designs drives much of the demand in wireless and its supporting technologies that comprise the front-end.

The basic block topology for a heterodyne receiver is shown in Figure 1. These basic components: low-noise amplifier (LNA), mixer, variable gain amplifier (VGA), voltage-controlled oscillator (VCO), and filter are needed for almost all wireless systems.

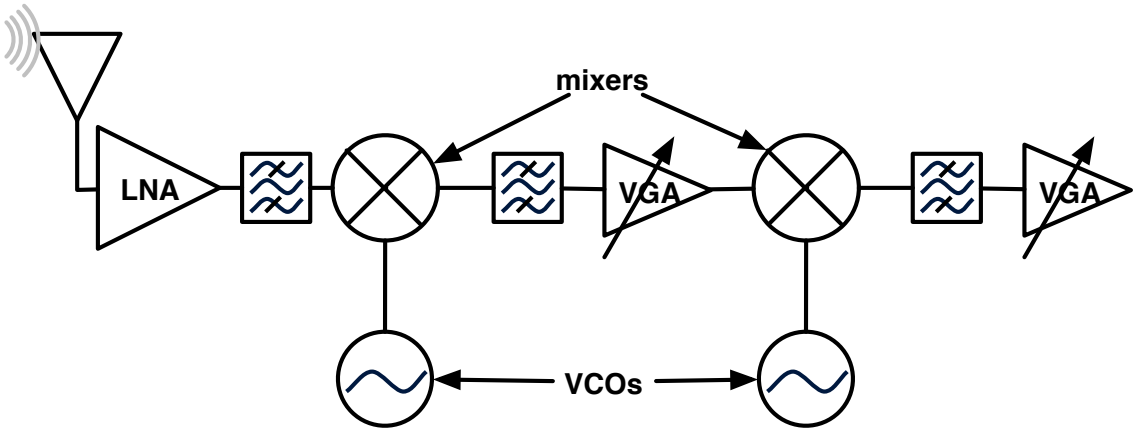

Figure 1: RF front end for heterodyne receiver architecture.

A crucial component of these architectures is the LNA. The purpose of the LNA is to amplify the very low signal received at the antenna with adding only a minimum amount of noise. The LNA has a direct impact on the receiver signal-to-noise ratio

(SNR) and thus can restrict the maximum data rate, receiver sensitivity, and other receiver specifications. For example, SNR limits the complexity of the modulation scheme used in the data transmission, thus the overall data rate. For radar receivers, the SNR limits the minimum detectable signal and therefore limits the size and distance of the detected object. The importance of the LNA and its impact on SNR can be observed by analyzing Friis equation [11]:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{1}$$

where F_i is the noise factor of the i^{th} component in the receiver chain, and G_i is the gain of the i^{th} component. Given a large gain in the first stage, it can be shown that the noise figure of this stage dominants the total noise figure. Therefore, by minimizing the noise figure and maximizing the gain of the LNA, the total receiver noise figure can be minimized [22]. To explore how this relationship relates to receiver performance, we can observe that noise factor is defined as:

$$F = \frac{SNR_{out}}{SNR_{in}} \tag{2}$$

Therefore, a noiseless amplifier will have a noise factor of one. This metric can be better understood as the ratio between the actual SNR at the output of the amplifier to the SNR of a noiseless amplifier. Noise factor can be related to the more commonly used noise figure (NF) by $NF = 10\log(F)$ which is expressed in dB. By re-arranging Equation (2), the following relationship is obtained:

$$SNR_{out} = SNR_{in} - NF_{tot} \tag{3}$$

which shows that minimizing the total noise figure will yield the highest output SNR. Designing very high-performance LNAs is an active research area and is of crucial importance for next-generation wireless technologies. In addition to maximizing gain and minimizing noise figure, other specifications also impacting LNA design

choices include: power consumption, linearity, and bandwidth. These specifications are rarely simultaneously optimized therefore understanding the design trade-off space is necessary for a successful LNA design. In addition to these trade-offs, improvements in device technology performance enable new applications for Si-based systems which offer low-cost solutions with similar performance to more expensive technology.

This thesis explores the LNA design trade-off space using Silicon-Germanium Hetro-Junction Bipolar Transistors (SiGe HBTs). The remainder of this chapter will focus on the SiGe HBT transistor and highlight its performance benefits. Subsequent chapters will focus on noise theory and LNA design and optimization. A number of LNA designs are analyzed, and an understanding of device level noise performance as it relates to LNA design is explored.

1.2 Silicon-Germanium Hetro-Junction Bipolar Transistor Technology

SiGe HBTs combines the speed and performance of many III-V technologies with Si-processing compatibility yielding a high-performance device that is readily commercially available. Since the first SiGe HBT demonstration over 20 years ago, SiGe HBT technology has shown an almost exponential growth both in terms of performance and number of commercial facilities as shown in Figure 2 and 3, [7] , [8] .

SiGe technology uses band-gap engineering in the base of a Silicon Bipolar Junction Transistor (BJT) to enhance device characteristics. By epitaxially growing compositionally graded SiGe alloy as the transistor base, device parameters are decoupled allowing exponential "tuning" based on the Ge content. The mechanism for this tuning capability is driven by the bandgap difference between Si (1.12 eV at 300K) and Ge (0.66 eV at 300K). This difference allows the bandgap of the SiGe alloy to be optimized to improve transistor performance . The effect of the graded Ge in the base directly impacts key performance metrics such as current gain (β), base transit time (τ_b), cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) which couple

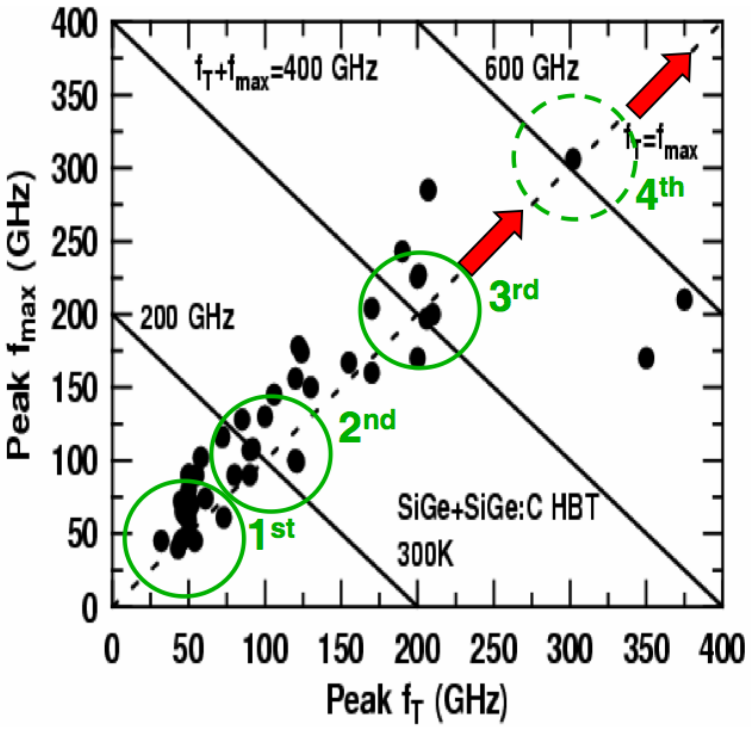

Figure 2: SiGe HBT technology performance growth as measured by f_t and f_{max} [7].

strongly to high-frequency amplifier performance.

A comparison of these parameters between a standard Si BJT and SiGe HBT yields an understanding of how Ge content can influence device performance. Assuming a linearly graded Ge profile (Figure 4), the collector current density enhancement directly relates to the β enhancement between a SiGe HBT and a Si BJT [7]:

$$\frac{J_{C,SiGe}}{J_{C,Si}} \simeq \frac{\beta_{SiGe}}{\beta_{Si}} \simeq \frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/kTe^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}} \tag{4}$$

where $\tilde{}$ denotes the positioned averaged quantities across the base, γ is the "effective density-of-states" ratio and η is the minority electron diffusivity ratio between SiGe and Si. The Ge profile enters the relationship through $\Delta E_{g,Ge}(grade)$ which is defined as $E_{g,Ge}(Wb) - E_{g,Ge}(0)$. This equation shows that as $\Delta E_{g,Ge}(grade)$ is increased, the total current gain will also increase. In addition, this enhancement is temperature activated through the $1/kT$ term. This relative enhancement in β has

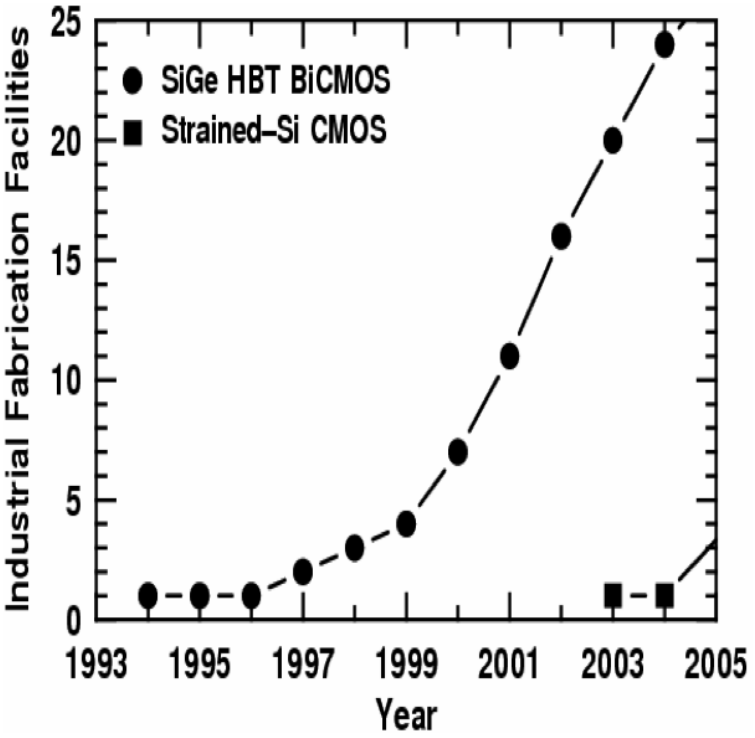

Figure 3: SiGe HBT technology commercial fabrication facilities [7].

an impact on high frequency amplifier performance in terms of gain and noise figure.

Further analysis shows that two crucial metrics of device performance, f_T and f_{max}, are largely enhanced through the minimization of τ_b through the addition of Ge in the base. Assuming a strong Ge grading scenario, which is true for the current generation of HBT technologies, τ_b is improved by $\Delta E_{g,Ge}(grade)$:

$$\tau_{b,SiGe} \simeq \frac{W_b^2}{2\tilde{D_{nb}}} \frac{kT}{\Delta E_{g,Ge}(grade)} \tag{5}$$

where W_b is the base width and D_{nb} is the minority electron diffusivity. By increasing $\Delta E_{g,Ge}(grade)$, τ_b is reduced. Also, τ_e (emitter charge storage delay) is proportional to $1/\beta$ therefore resulting in a reduction of the total transit time. This can be further explored by examining f_T:

$$f_T = \frac{1}{2\pi} \left[\frac{1}{g_m}(C_{te} + C_{tc}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc} \right]^{-1} \tag{6}$$

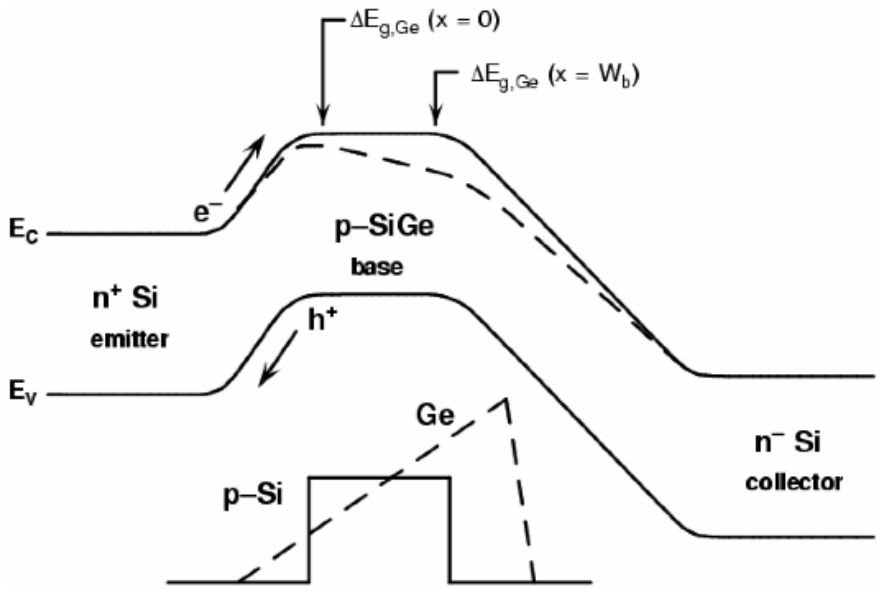

Figure 4: Energy band diagram for SiGe HBT (dashed) compared to Si BJT (solid) biased in the forward active region [7]

where g_m is the device transconductance ($\delta I_c/\delta V_{BE}$), $C_{te} + C_{tc}$ are the depletion capacitances, W_{CB} is the junction width of the collector-base (CB) space charge region, v_{sat} is saturation velocity, and r_c is the small-signal collector resistance. Since f_T is inversely proportional to τ_b and τ_e, their reduction will increase f_T. Also, f_{max} will improve since it is a function of f_T:

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}} \tag{7}$$

where C_{bc} is the collector base capacitance, and r_b is the intrinsic base resistance. By adjusting the Ge grading, higher base doping can be used while still maintaining a high β, yielding a lower base resistance and improved noise performance. These performance parameters point to the ability to increase such amplifier characteristics such as gain and noise figure, which can greatly benefit LNA and system design.

One of the key advantages of SiGe HBT technology is its compatibility with

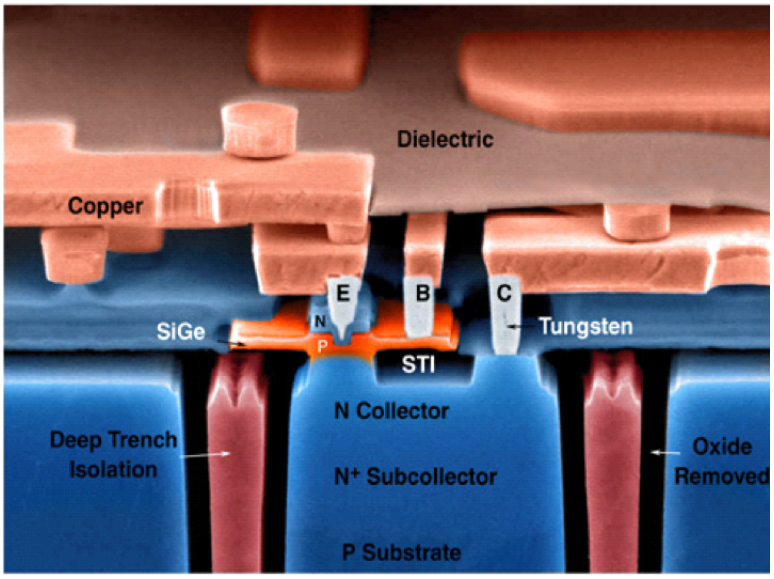

Figure 5: Structure of third-generation SiGe HBT (courtesy of IBM).

traditional Si CMOS processing. The Ge layer is grown using a ultra-high vacuum/chemical vapor deposition (UHV/CVD) processing step, which reduces the necessary thermal cycle and has fine control of the Ge profile. This process modification is typically included as a "plug-in module" in traditional Si CMOS fabrication facilities allowing for a high-yielding low-cost BiCMOS technology [8]. A micrograph of a cross-section of a third-generation SiGe HBT is shown in Figure 5. SiGe HBTs compatibility with Si CMOS processing is a key advantage over competing III-V technologies which are typically characterized by low to moderate-yielding, non-Si CMOS compatible processing. In addition, the performance improvements at a given technology node allow SiGe HBTs to provide cost vs performance advantage even over Si-CMOS. Figure 6 compares RFCMOS versus SiGe HBT relative trusted foundry pricing at a similar technology performance as measured by f_T. Some relevant performance specifications for a third generation SiGe technology are highlighted in Table 1.

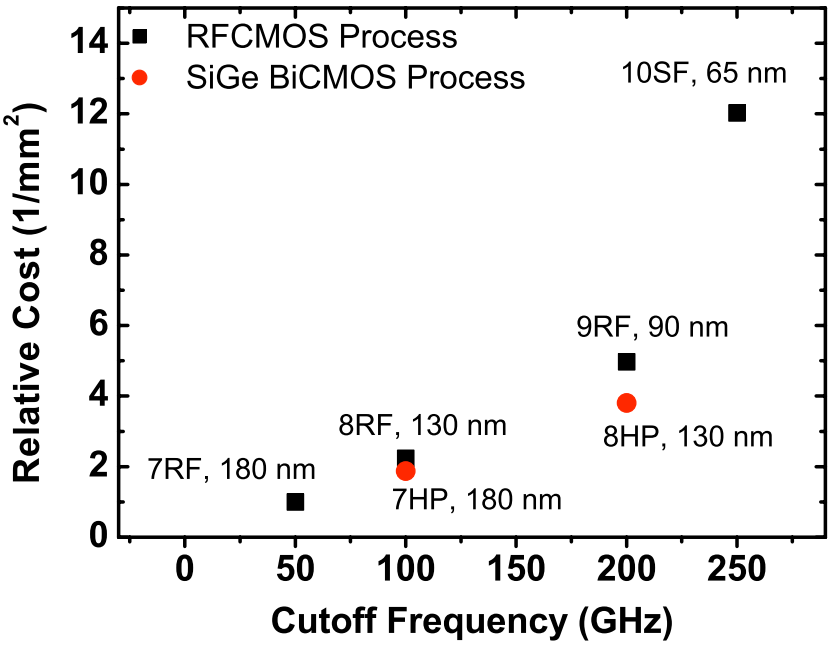

Figure 6: Comparison of normalized trusted foundry pricing as a function of f_T for Si CMOS and SiGe HBTs at various technology nodes.

Table 1: Typical SiGe HBT third generation device performance parameters

W_E	0.12 μm
β	400
f_T	200 GHz
f_{max}	250 GHz

1.3 Broadband Noise Fundamentals of SiGe HBTs

Equations (4) - (7) directly relate the Ge profile to improvements in β, f_T, and τ_b. The ability to simultaneously optimize these factors allows for superior noise performance of SiGe HBTs. To further understand the noise characteristics of a HBT, linear noisy two-port theory can be used to analyze the noise sources of an HBT (Figure 7). The primary sources of broadband noise in an HBT are base thermal noise ($4kTr_b$), base shot noise ($2qI_B$), and collector shot noise ($2qI_C$).

The noise parameters, R_n, $Y_{s,opt} = G_{s,opt} + jB_{s,opt}$, and F_{min} are typically used

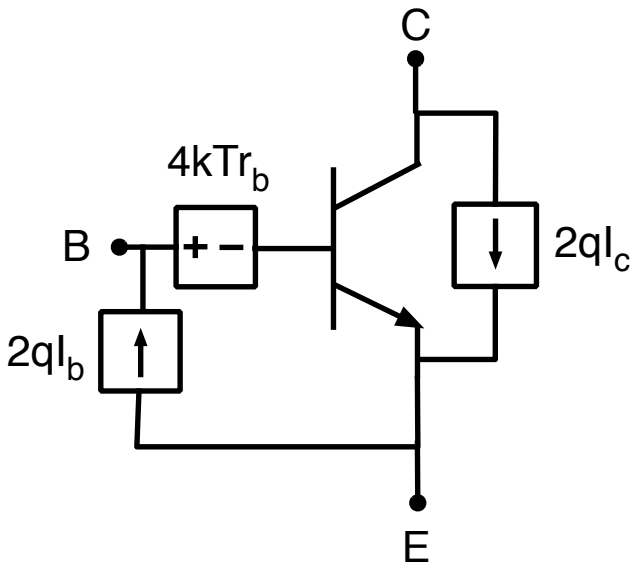

Figure 7: Noise model of a SiGe HBT highlighting relevant noise sources.

to characterize the noise performance of a transistor. These parameters are defined in terms of v_n^2 (equivalent noise voltage), i_n^2 (equivalent noise current), and γ (cross-correlation factor) by [16]:

$$R_n = \frac{v_n^2}{4kT_o\Delta f}, \tag{8}$$

$$Y_{s,opt} = \left(\sqrt{1-\gamma_i^2} - j\gamma_i\right)^{-1} \frac{i_n}{v_n}, \tag{9}$$

$$F_{min} = 1 + \frac{v_n i_n}{2kT_o\Delta f}\left(\gamma_r + \sqrt{1-\gamma_i^2}\right). \tag{10}$$

In addition, these parameters can be related to the noise sources and fundamental device parameters by performing a two port analysis on Figure 7. As shown in [7], v_n^2, i_n^2, and γ for an HBT can be expressed in terms of Y parameters:

$$v_n^2 = 4kTr_b + \frac{2qI_c}{|Y_{21}|^2}, \tag{11}$$

$$i_n^2 = 2q\frac{I_c}{\beta} + 2q\frac{I_c}{|\frac{Y_{21}}{Y_{11}}|^2}, \tag{12}$$

$$\gamma = \frac{2qI_cY_{11}}{|Y_{21}|^2}. \tag{13}$$

Expressing the HBT as a two-port device yields the following Y-paramaters [7]:

$$y_{11} = \frac{g_m}{\beta} + j\omega C_i, \tag{14}$$

$$y_{12} = -j\omega C_{bc}, \tag{15}$$

$$y_{21} \approx gm, \tag{16}$$

$$y_{22} = j\omega C_{bc}. \tag{17}$$

where $C_i = C_{be} + C_{bc}$. Combining equations(8) - (10), (11) - (13), and (14) - (17) yield the following results for the noise parameters of a SiGe HBT in terms of device parameters:

$$R_n = r_b + \frac{1}{2g_m}, \tag{18}$$

$$G_{s,opt} = \sqrt{\frac{g_m}{2R_n\beta} + \frac{(\omega C_i)^2}{2g_m R_n}\left(1 - \frac{1}{2g_m R_n}\right)}, \tag{19}$$

$$B_{s,opt} = \frac{\omega C_i}{2g_m R_n}, \tag{20}$$

$$F_{min} = 1 + \frac{1}{\beta} + \sqrt{\frac{2g_m R_n}{\beta} + \frac{2R_n(\omega C_i)^2}{g_m}\left(1 - \frac{1}{2g_m R_n}\right)}. \tag{21}$$

Equation (21) shows that the noise factor improves through enhancements to β, C_{be}, C_{bc}, and r_b which are all improved through addition of Ge into the base.

For a typical third generation SiGe HBT, Figure 8 plots f_T and NF_{min} against collector current density. For nominal bias values of 5-10 x below peak f_T, the achievable NF at 10 GHz is below 1 dB. This level of performance allows for very low-noise, high-gain, and high frequency LNAs with low power consumption.

1.4 Summary

In Chapter 1, we discuss the importance of LNAs in receiver design and the benefits of SiGe HBT BiCMOS technology for wireless applications. Through bandgap engineering by introducing Ge into the base of a transistor, the performance of a standard

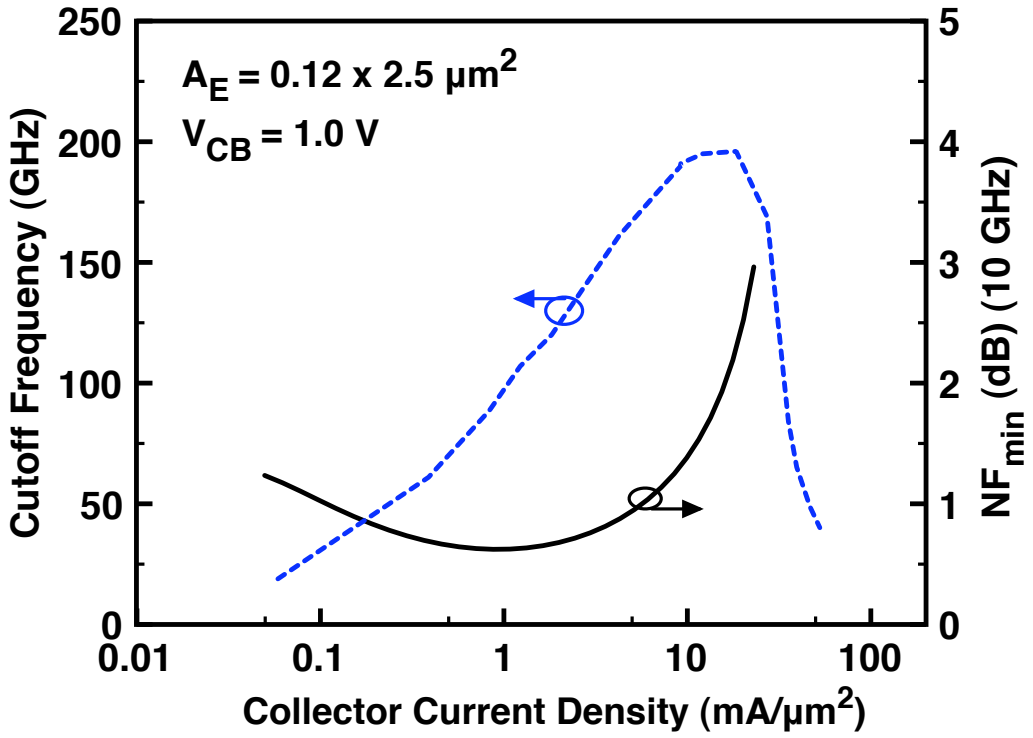

Figure 8: f_T and NF_{min} at 10 GHz versus J_c for a 0.12 x 2.5 μm^2 third generation SiGe HBT.

Si BJT can be greatly improved allowing new high freqeuncy, low-cost applications in a Si-compatible processing technology. The relationship between device performance and Ge content were highlighted, showing how relevant parameters such as gain and noise figure are enhanced. Typical third generation performance metrics were shown, focusing on those parameters important to LNA design.

The remainder of this work will focus on actual LNA designs and highlight the record performance achievable through the use of SiGe HBT BiCMOS technology. Chapter 2 provides a tutorial for designing a high-frequency LNA and an example LNA design. Chapter 3 explores the methods for optimization of LNA design for a power constrained application. Chapter 4 will investigate cryogenic performance of SiGe HBT LNAs. Chapter 5 concludes by summarizing the results of this work and discussing future research paths.

CHAPTER II

LNA DESIGNS IN SIGE HBT BICMOS TECHNOLOGY

2.1 Introduction

As shown in the previous chapter, SiGe HBT technology has remarkable broadband noise performance, making these devices well suited for high-frequency amplifier design. First, this chapter will provide a general outline of high-frequency LNA design focusing on the theory of amplifier noise matching. We will introduce a common LNA design technique using an inductively degenerated cascoded architecture (Figure 9). The LNA designs presented here will use a third generation SiGe HBT in a 130 nm BiCMOS platform . The addition of the common base second stage allows for reduction of miller capacitance of the first stage, improves stability, and enhances isolation between the input and output, with only a minimal increase in noise figure as compared to a single stage, common emitter configuration.

2.2 Basic Concepts in High-Frequency LNA Design

The basic approach to high-frequency LNA design involves noise and gain impedance matching. The lowest achievable noise figure for a transistor (NF_{min}) is only attainable if the source impedance is Z_{opt}. This impedance, however, may not coincide with the optimum small-signal power or gain matching condition, thus, there is an inherent trade-off between noise figure, gain, and input matching. As shown in equation (22), the noise factor has a squared dependance on any noise mismatch, therefore in order to achieve low noise figures, the source impedance must be near the optimum noise matching impedance.

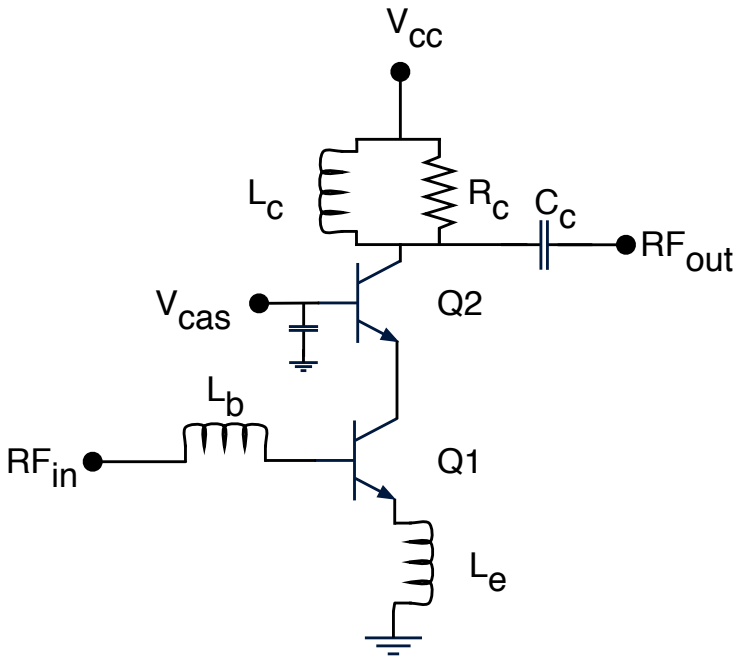

Figure 9: Simplified schematic of an inductively degenerated cascode LNA.

$$F = F_{min} + \frac{G_n}{R_s}|Z_s - Z_{opt}|^2 \tag{22}$$

where G_n is the noise conductance and R_s is the real part of the source impedance. For this given source impedance Z_s and conjugately matched output impedance, a figure of merit, the available gain, can be defined in Equation (23).

$$G_A = \left|\frac{Y_{21}}{Y_{11} + Y_S}\right|^2 \frac{G_S}{G_{out}} \tag{23}$$

where Y_S is the source admittance, G_S is real part of the source admittance, and G_{out} is defined as:

$$G_{out} = real\left(Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11} + Y_S}\right). \tag{24}$$

The available gain is typically called the associated gain when $Y_S = Y_{s,opt}$. The associated gain represents the amount of gain when the input is noise matched and the output is conjugately matched.

These two parameters, noise figure and associated gain, are typically graphically displayed on a Smith chart as circles, aiding in the design of LNAs. For a given bias and emitter area, noise and gain circles can be plotted as shown in Figure 10.

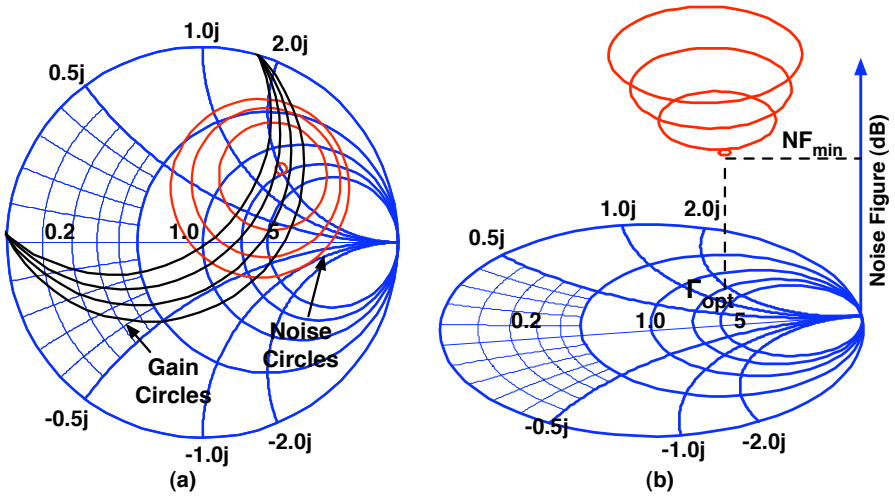

Figure 10: (a) Gain and noise figure circles for third generation 0.12 x 30 μm^2 SiGe HBT for $I_C = 5.5$ mA at 10 GHz. (b) 3-D diagram showing elevated noise circles on the Smith chart.

From Figure 10 (a) the red contours represents the noise circles while the black contours plot the available gain. This graphical design tool helps visualize the optimum source matching impedance and helps the designer understand the gain and noise figure tradeoff. Figure 10 (b) rotates these noise contours in 3-D to highlight the minimum noise figure point and how that corresponds to Γ_{opt}. As shown in 10 (b), the slope of the noise contour is very sensitive to source impedance, thus a small change in source impedance can greatly change the total noise figure.

One metric that is typically not included until later in the design process is linearity, typically measured by the third order intercept point (TOI) or IP3. In modern wireless systems, amplifier linearity is very important as it sets the maximum dynamic range of the signal. A tool presented in [17] specifically characterizes an inductively degenerated cascode LNA structure along NF, Gain, and IP3 as a function of emitter

length and bias. Simulation results for a standard cascode LNA at X-band using a third generation SiGe HBT are shown in Figure 11. This tool performs a simultaneous noise and power match across bias and geometry to calculate noise figure and gain contours, and uses a volterra series analysis to determine IIP_3 contours.

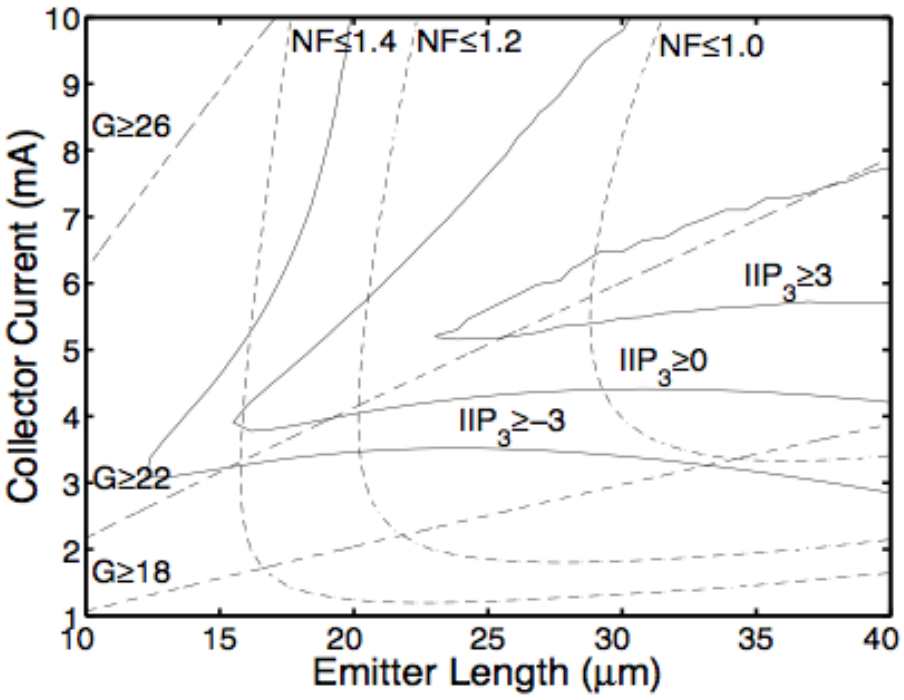

Figure 11: Simulation of NF, Gain, and IP3 vs collector current and emitter length for a cascode LNA using the design tool presented in [17].

In this section, we analyzed a basic approach to LNA design, introducing the tradeoffs between gain and noise matching. The basic relationships between gain and noise figure as a function of source impedance were explored, and a graphical understanding of these concepts were presented. In the following section, we introduce a more systematic design approach to produce an optimized cascode SiGe HBT LNA design.

2.3 Inductively Degenerated Cascode X-band LNA design

A very common practice for high-frequency LNA design involves using device size scaling and inductive degeneration to perform a simultaneous noise and power match. This procedure has been discussed [18], [19], and [22]. In this section we present a graphical procedure which aids in understanding the design procedure and tradeoffs.

Step 1: Selection of collector current density (J_c).

The first step in this design procedure is to select the collector current density (J_c) which satisfies gain and noise figure requirements for the intended application. This selection can be accomplished by fixing an emitter area and sweeping collector current. Figure 12 plots NF_{min} at 10 GHz versus J_c for an emitter area of 0.12 x 2.5 μm^2. For this example, $J_c = 3.4$ mA/μm^2 was selected yielding a current gain (H_{21}) of above 20 dB and NF_{min} below 1 dB. Lower noise minimum noise performance could be achieved, however, the resulting gain would also be reduced.

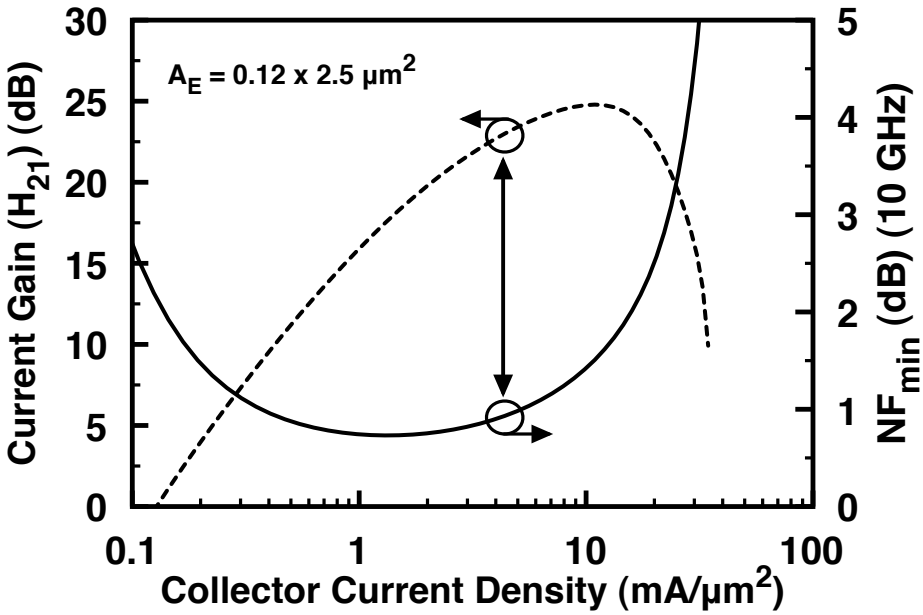

Figure 12: NF_{min} and H_{21} as a function of J_c for a fixed emitter area of 0.12 $\times$ 2.5 μm^2 to determine optimum bias conditions.

Step 2: Selection of emitter length.

Once the specific collector current density is determined in step 1, the device geometry can be scaled in order to move the real part of the noise matching impedance to 50 Ω. To accomplish this, fix the collector current density and sweep emitter length to determine Γ_{opt}. $R_{s,opt}$ is given by Eq. 25:

$$R_{s,opt} = 50\Omega \cdot Re\left(\frac{1+\Gamma_{opt}}{1-\Gamma_{opt}}\right) \tag{25}$$

Figure 13 plots $R_{s,opt}$ as a function of emitter length for $J_c = 3.4$ mA/μm^2. Figure 14 plots Γ_{opt} as a function of emitter length on a Smith chart. This diagram aids in visualizing how the optimum noise matching impedance changes as the emitter length is scaled. For this example, the emitter length was chosen to be 40 μm, yielding a total collector current of 16.1 mA. For the cascode architecture used for this design, equal sized Q_1 and Q_2 were selected each employing the "high-performance" HBT device option. However, the designer may choose to alter this procedure and select an unequal sized cascoded device, this has the benefit of a greater degree of design flexibility but adds complexity to the design process. A larger area cascoded device could potentially help improve linearity and gain without a large degradation to overall noise figure.

This design technique enables noise matching to the system impedance without the need for a lossy matching network. $R_{s,opt}$, Equation (26), and NF_{min}, Equation (27), are given in [7], where L_E and W_E are the emitter length and width, respectively, $r_b \cdot L_E/W_E$ is the scaled base resistance, and f is the operating frequency. As seen from Equation (26), $R_{s,opt}$ is inversely proportional to L_E, and therefore scaling L_E allows the selection of an optimum source resistance. In addition, NF_{min} is independent of emitter length since the scaling does not alter the f_T at a fixed J_c.

$$R_{s,opt} = \frac{f_T}{f}\frac{1}{L_E}\sqrt{\frac{2}{J_C}\frac{r_b L_E}{W_E}\frac{kT}{q}} \tag{26}$$

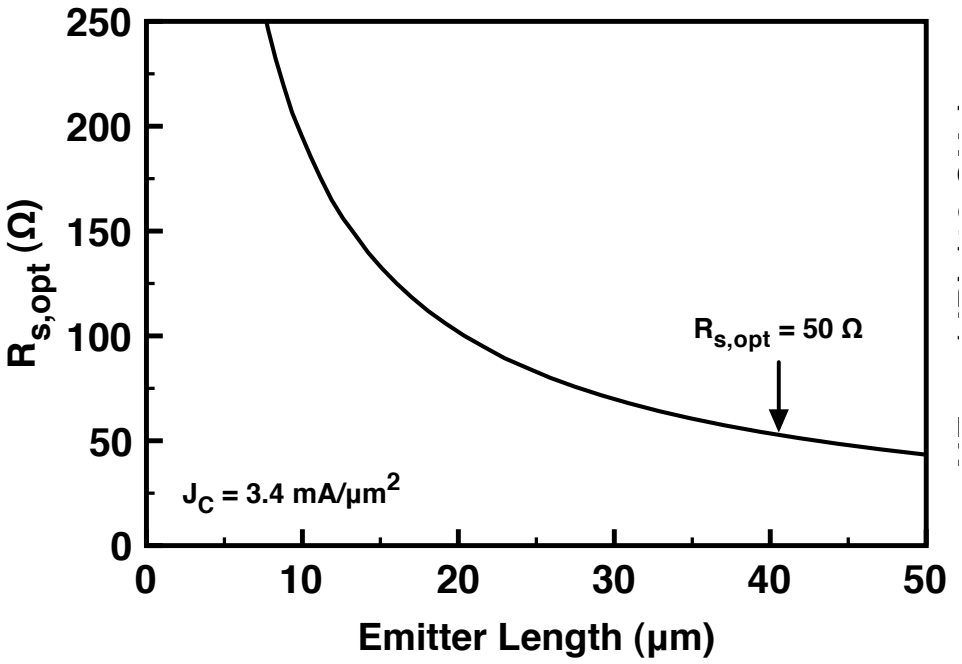

Figure 13: $R_{s,opt}$ as a function of emitter length for a fixed $J_c = 3.4$ mA/μm^2.

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2} \tag{27}$$

Therefore, NF_{min} and $R_{s,opt}$ are effectively decoupled and can be selected independently.

Step 3: Selection of degeneration inductance L_e and base inductance L_b

From steps 1 and 2, the device size and bias conditions are selected to achieve a specific noise figure and enable noise matching to 50 Ω. The next step is to match the input impedance to 50 Ω which is accomplished by the addition of a degenerating emitter inductor with only a moderate noise degradation. The value for this inductor L_e is given by:

$$L_e = \frac{50}{2\pi f_t} \tag{28}$$

where f_t is the cutoff frequency of the device at its operating point. For this example, f_t was simulated in Figure 15 to be approximately 100 GHz, and L_e is

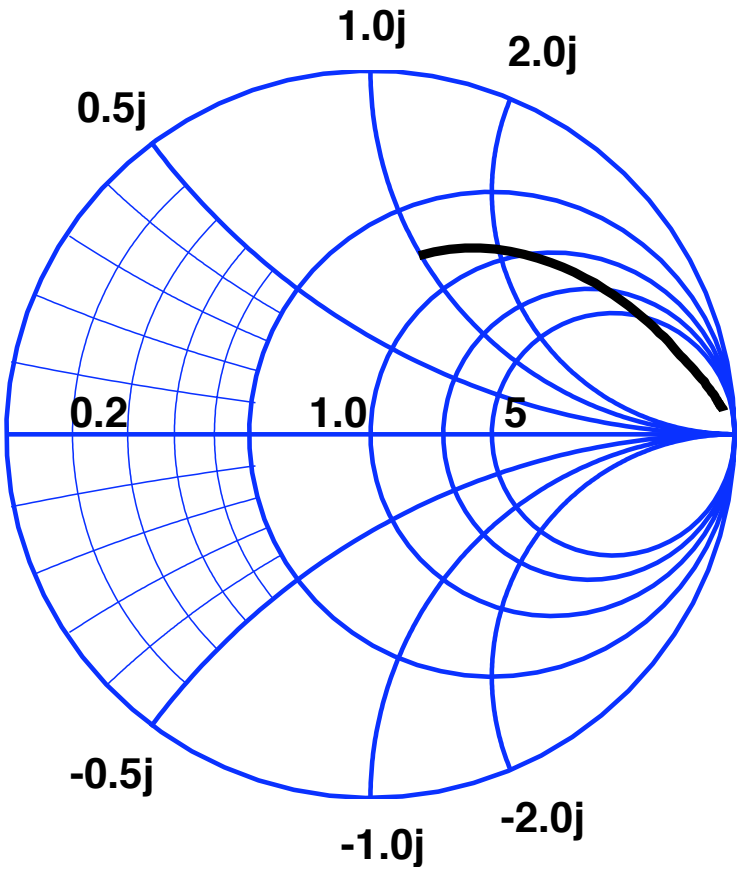

Figure 14: Γ_{opt} as a function of emitter length displayed on Smith chart showing the optimal noise matching impedance.

calculated to be 80 pH. Figure 16 plots the input match as a function of emitter inductance on a Smith chart. This graphs shows a value of closer to 100 pH would provide a more optimum match, this difference is due to unaccounted device parasitics that are captured within simulation but not within the design equations.

Once the emitter inductance has been selected, the remaining portion of the input matching network, L_b serves to resonant out the C_{BE} capacitance and conjugately match the reactive portion of the noise impedance. Equation 29 can be used to determine the value of this inductance. L_b was determined to be 900 pH, which completes the input noise and power matching network. Figure 18 plots NF_{min}, NF, S_{11}, and H_{21} against frequency, showing that this example LNA is well noise and input matched. The remaining portion of this design requires an output matching

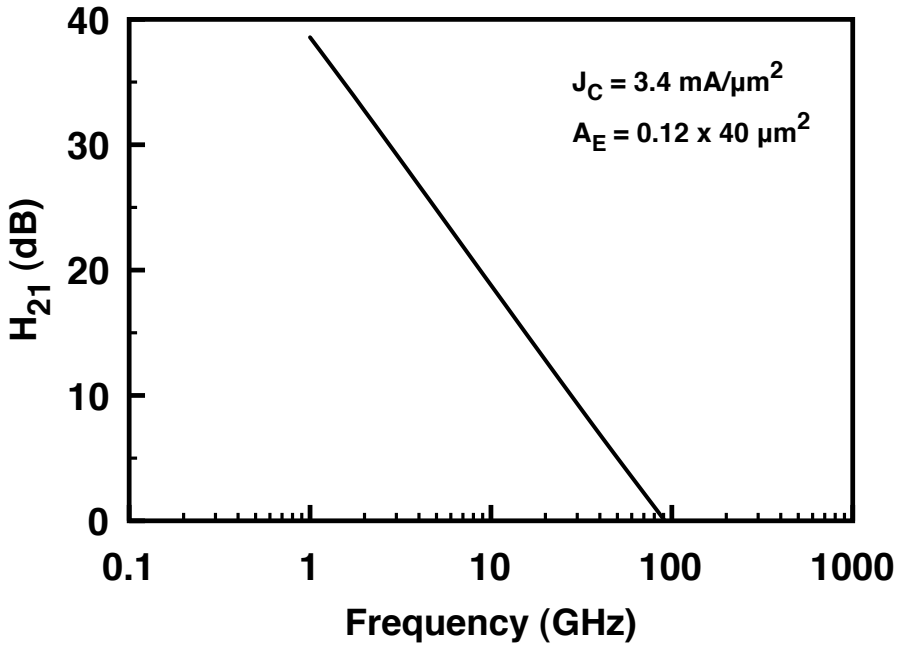

Figure 15: H_{21} as function of frequency at $I_c = 16.3$ mA which is used to extract f_t at the device operating point.

network meeting the requirements for gain and bandwidth.

$$L_b = \frac{1}{\omega^2 C_{BE}} - L_e \tag{29}$$

2.4 Summary

Some advantages of this technique are the ability to achieve simultaneous noise and power match and maintain low noise figure. As seen in Figure 18, the input and noise match are both well centered at the design frequency (10 GHz). S_{11} was simulated to be less than 40 dB at 10 GHz, and the NF curves closely matches NF_{min} at the frequency of interest. This simple matching network allows for a very efficient design yielding optimal performance.

However, there are number of drawbacks for this design procedure. The noise and power match are accomplished through dissipating more *dc* power, thus this design is not suited for power constrained applications. Typically, this type of matching

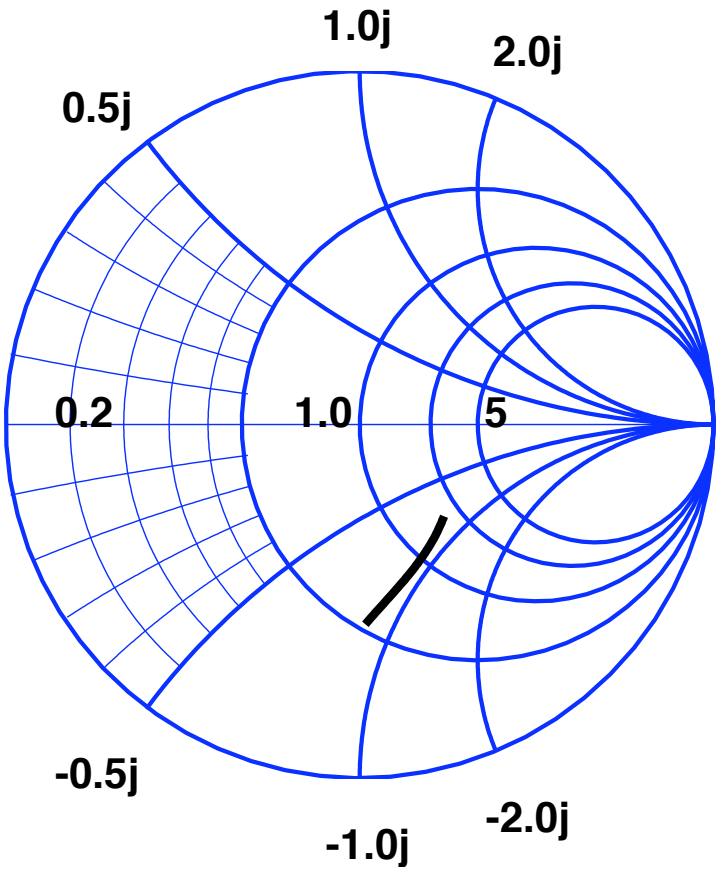

Figure 16: Input reflection coefficient (S_{11}) as a function of emitter degeneration inductance (L_e) plotted on a Smith chart

network is very narrow band, therefore not suitable for some next generation wireless applications. In addition, this design does not include linearity specifications in the design procedure, however, the tool shown in Figure 11 could be used in conjunction with this design technique to help design for linearity.

In the following chapter, we will focus on a power constrained LNA design using the cascoded LNA architecture. The design procedure, simulation results, and layout will be presented, and measured results from the low-power X-band cascoded LNA will be shown.

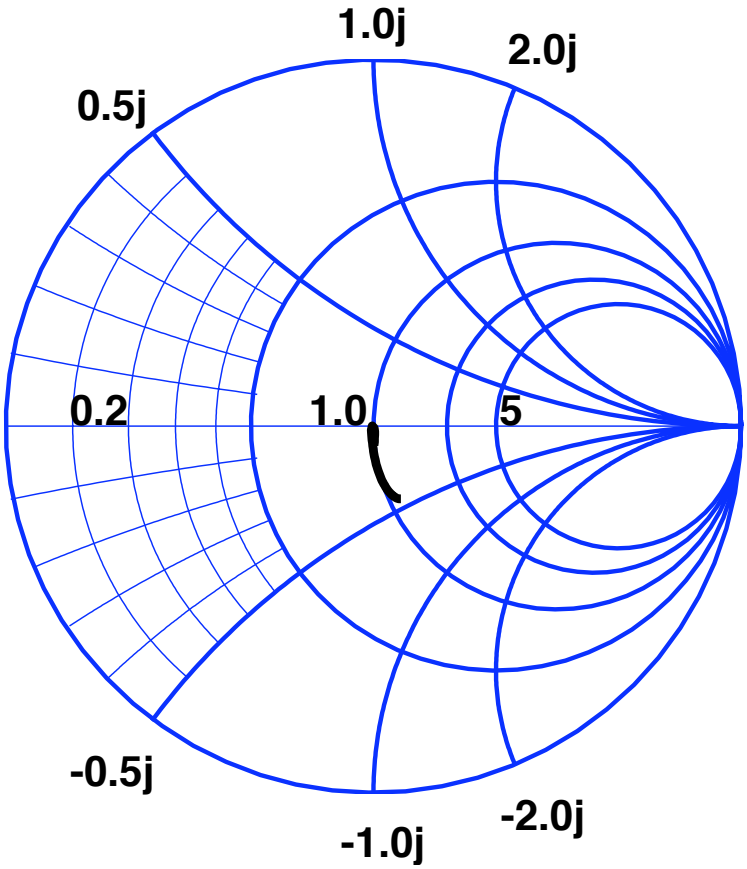

Figure 17: Input reflection coefficient (S_{11}) as a function of base inductance (L_b) plotted on a Smith chart.

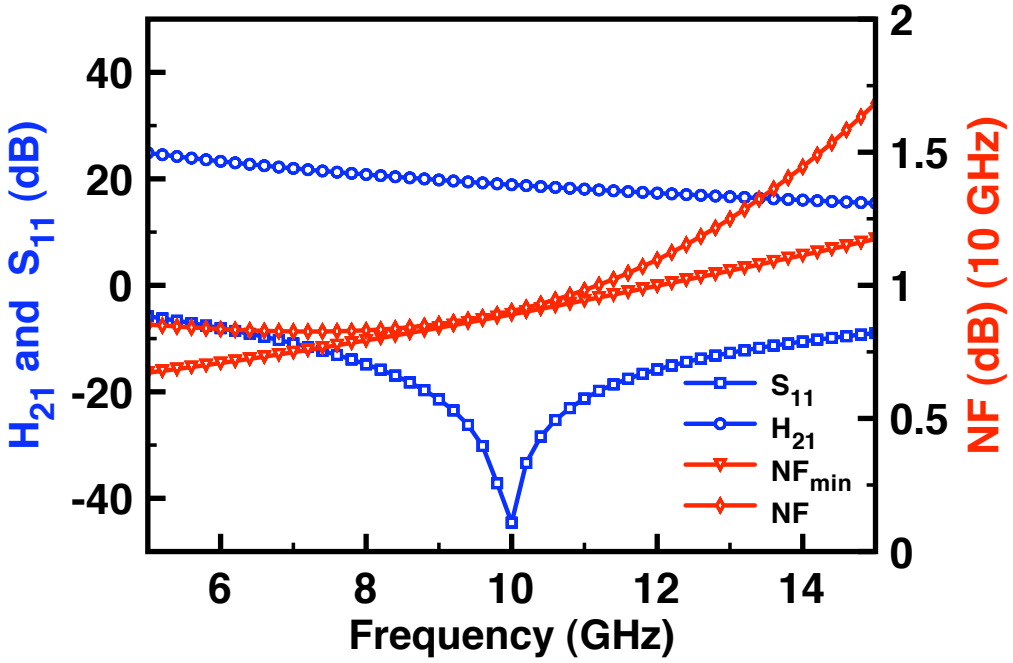

Figure 18: Input matching network results from example X-band LNA design.

CHAPTER III

POWER-CONSTRAINED LNA DESIGN AND OPTIMIZATION

3.1 Introduction

In the preceding chapter, we examined an LNA design technique using a cascoded amplifier structure with emitter degeneration enabling simultaneous noise and power match. In this chapter we apply that similar design to a power constrained application.

The low power LNA was specifically designed to target space-based and high altitude radar applications. Some of the LNA requirements for these radars are highlighted in Table 2.

Table 2: Low power LNA requirements.

Frequency	8-12 GHz
Noise Figure	$<$ 2dB
dc power	$<$ 2 mW

These platform's strict power requirements demands a receiver system with ultra low-power consumption. In many receiver systems, LNAs can account for a large portion of dc power due to their near continuous operation. Low-power LNAs dissipating under 2 mW have been demonstrated in III-V technology [12], however, substantial benefits would be gained by a low-power LNA in a Si-compatible technology [14]. In [25] we present the first SiGe HBT sub-2 mW X-band LNA achieving less than 2 dB of NF. In the next section, we highlight the design of this low-power LNA and present measured results.

3.2 Low-power cascoded X-band LNA design and simulation

In chapter 2, we examined the basic procedures for designing an inductively degenerated cascode LNA at X-band. This LNA was designed to meet certain gain and noise figure specifications which was accomplished by increasing *dc* power consumption, allowing simultaneous noise and power matching. Certain LNA design applications are power constrained, and require a fixed I_c, therefore, the design procedure outlined in the previous chapter will not suffice. In [25] we present a modified procedure to the traditional inductively degenerated cascoded design that is suited for low-power applications.

In this modified procedure, I_c is directly determined from the required power dissipation and supply voltage. This I_c must remain fixed as the desired $R_{s,opt}$ is selected requiring J_c to scale as L_E is scaled. Therefore, L_E and J_c cannot be determined independently as in the previous procedure. These two resulting parameters,NF_{min} and $R_{s,opt}$, must be solved simultaneously, appropriately scaling J_c and L_E within the limits of the specified I_c.

Figure 19 provides a simple graphical tool where simulated results for NF_{min} and $R_{s,opt}$ are plotted against L_E for a fixed $I_c = 1.33$ mA. Given this fixed current, achieving $J_{c,opt}$ requires L_E to be 7.8 μm yielding an $NF_{min} = 0.73$ dB. However, the resulting $R_{s,opt} = 250\ \Omega$ making noise matching difficult. An $R_{s,opt}$ of close to 50 Ω is desirable in order to achieve a simultaneous power and noise match. By trading-off 0.3 dB NF, $R_{s,opt}$ is reduced to 75 Ω, yielding a more acceptable matching condition. By graphically solving for both NF_{min} and $R_{s,opt}$ simultaneously, the appropriate noise and gain trade-off can be accomplished.

The emitter area for this LNA was determined from Figure 19 to be 0.12 μm $\times$ 24 μm. Due to process constraints, two 0.12 μm $\times$ 12 μm parallel devices were used. The input matching network was designed using the same technique as in Chapter

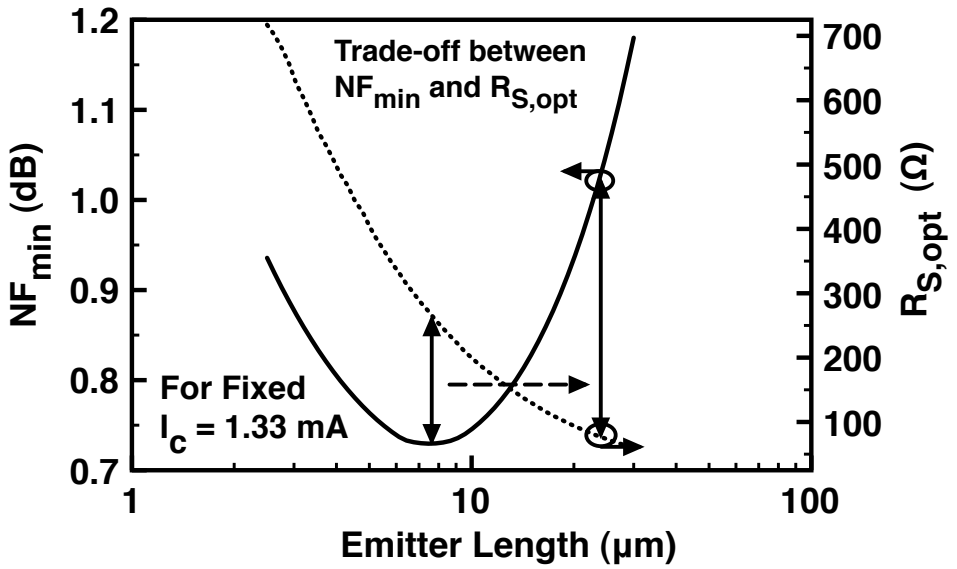

Figure 19: Simulated NF_{min} and $R_{S,opt}$ as a function of emitter length for a fixed $I_c = 1.33$mA.

2. Table 3 lists the values used for the input and output match networks. The output matching was realized through a shunt-RL, series-C passive network, where the shunt-resistance assisted in output matching and stability with only a moderate gain degradation.

Table 3: Design parameters for cascoded low-power X-band LNA.

A_e	0.12 μm $\times$ 24 μm
L_e	335 pH
L_b	906 pH
L_c	1 nH
C_c	135 fF
R_c	435 Ω

The design and simulation was performed using Cadence and Agilent's Advanced Design System (ADS) tools in a commercially-available 130 nm SiGe HBT BiCMOS technology (f_T/f_{max} of 200/280 GHz respectively), and a full suite of passive components [20]. Figure 20 depicts the fabricated low-power LNA with total area of 667 μm $\times$ 653 μm including bondpads. The final simulation results for the design are shown

in Figure 21. In the next section, we examine the noise measurement methodology used to characterize this LNA and then present the measured results.

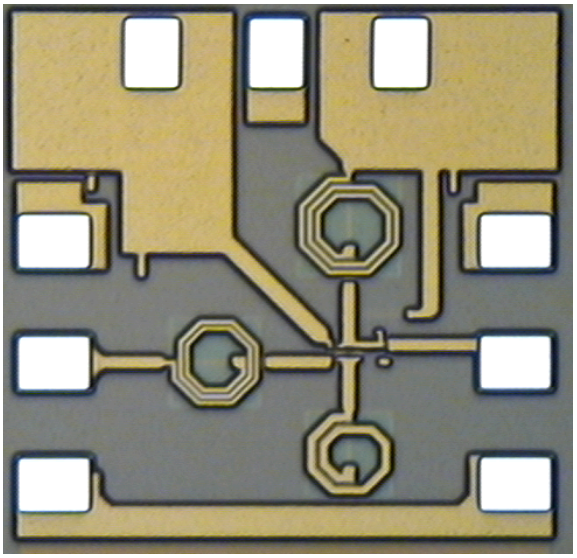

Figure 20: Photograph of fabricated LNA.

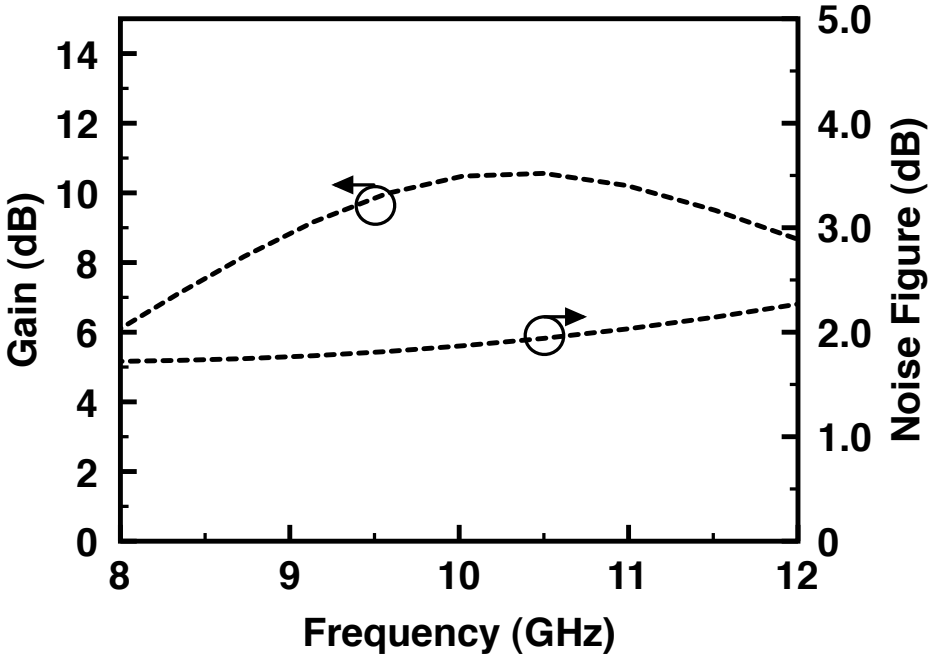

Figure 21: Simulated NF and S_{21} over frequency for the low-power X-band LNA.

3.3 Noise Measurement Theory

In this section, we present basic noise measurement theory as it pertains to high-frequency amplifier design. In order to ensure accurate noise measurements, an understanding of noise measurement techniques is necessary. It is also important to understand the uncertainties and sources of error to provide a level of confidence and accuracy in the measurement. There are a number of noise measurement techniques including the cold noise source and the Y-factor (also referred to as the hot/cold method), the most common technique being the Y-Factor method [2]. We will begin this discussion by defining some common terms used in noise figure analysis, then continue by explaining how the Y-factor measurement is conducted, and conclude with an understanding of the sources of measurement uncertainty.

As shown in Figure 22, the Y-factor noise measurement requires a noise source and a noise figure analyzer (NFA). The purpose of the noise source is to provide a calibrated input noise power, typically referred to as an Excess Noise Ratio (ENR). The ENR is quoted in dB and varies over frequency for a given noise source:

$$ENR_{dB} = 10 \log \frac{T_s^{ON} - T_s^{OFF}}{T_o} \tag{30}$$

where T_s^{ON} and T_s^{OFF} are the noise temperatures of the noise source in its off and on state respectively, and T_o is the reference temperature of 290K. T_s^{OFF} is typically calibrated to this reference temperature, 290K, however, in some situations, this may not be the case. For a given noise source, the ENR values will be specified over frequency and are specific to that noise source. These values are directly entered into the NFA and used for calibration and measurement.

The Y-factor, shown in Equation (31), is the ratio of two noise power levels or noise temperatures. This ratio depends on the ENR of the noise source, therefore, any uncertainties of the ENR will directly impact the noise measurement accuracy.

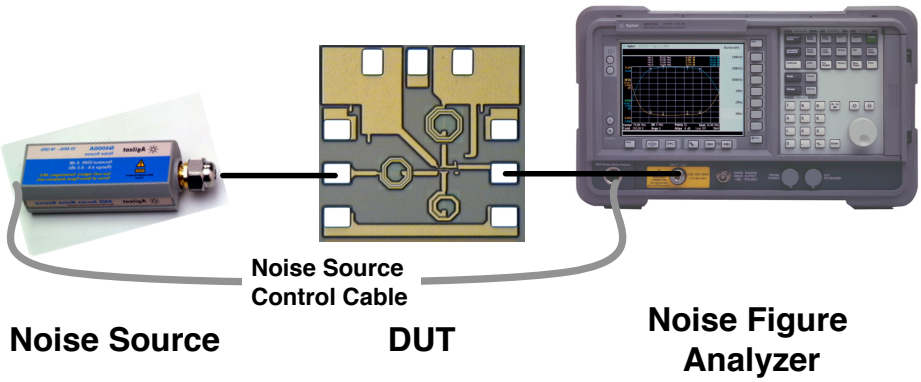

Figure 22: Noise measurement setup using the Y-factor method.

$$Y = \frac{N_2}{N_1} = \frac{T^{ON}}{T^{OFF}} \tag{31}$$

where N_2, N_1 is the noise power recorded when the noise source is on, off respectively. In order to calibrate the output losses, the noise source is connected directly to the output cable of the DUT. Since the ENR table is known, the NFA is able to determine the appropriate correction factors and calibrate any losses. If the noise of the instrument and output cables is T_2, the the Y-factor can be computed as:

$$Y = \frac{T_s^{ON} + T_2}{T_s^{OFF} + T_2} \tag{32}$$

solving for T_2 yields:

$$T_2 = \frac{T_s^{ON} - Y_2 T_s^{OFF}}{Y_2 - 1} \tag{33}$$

If there are extra losses that are either before or after the DUT that cannot be directly calibrated, they should be measured independently, and entered into the NFA manually.

Once this measurement has been completed, the NFA normalizes its noise figure and gain calibration by applying the appropriate correction factor for T_2 and the DUT can be connected as shown in Figure 22. A similar measurement is made

with the DUT in place, and the noise of both the DUT and the output cables and instrumentation is measured as T_{12}:

$$T_{12} = \frac{T_s^{ON} - Y_{12} T_s^{OFF}}{Y_{12} - 1} \tag{34}$$

where Y_{12} is the ratio of the noise powers of both the DUT and measurement equipment as measured between the ON and OFF states. Since T_2 is known, the noise of the DUT can be calculated:

$$T_{DUT} = T_{12} - \frac{T_2}{G_{DUT}} \tag{35}$$

where G_{DUT} is the gain of the DUT computed by taking the ratio of the noise power differences. Figure 23 is an illustration of how the Y-factor method can also be understood graphically [3]. In this graph, the output power from the DUT is plotted against the source temperature and since the DUT has a linear noise response, the slope of this line is kG_aB where k is Boltzmann's constant, G_a is the gain of the DUT and B is the measurement noise bandwidth.

By measuring two points on the line (T_s^{ON}, N_2) and (T_s^{OFF}, N_1), the slope and the y-intercept, N_a, can be determined through simple algebra. Solving for N_a, which is the added noise power by the DUT, yields:

$$N_a = N_1 - \left(\frac{N_2 - N_1}{T_s^{ON} - T_s^{OFF}} \right) T_s^{OFF} \tag{36}$$

Combining this relationship with the Equations (30) and (31) and taking $T_s^{OFF} = T_o$, the added noise power of the DUT in terms of the source ENR and the Y-factor is:

$$N_a = kT_oBG \left(\frac{ENR}{Y - 1} - 1 \right) \tag{37}$$

The Y-factor method is a straight-forward and accurate approach to measuring

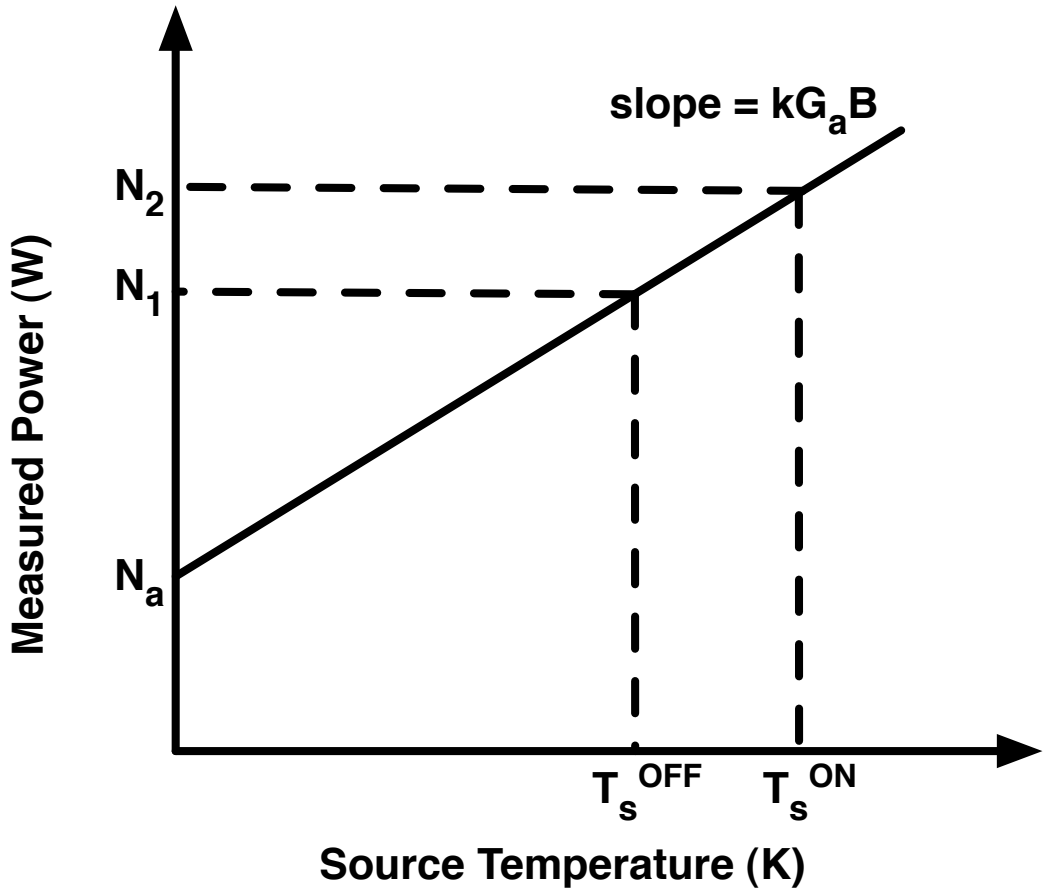

Figure 23: Noise power output versus source temperature for determining DUT noise power.

amplifier noise performance. However, care should be taken when the DUT noise figure is much higher than the ENR of the noise source, since the Y-factor will be close to 1. To ensure accuracy, the noise figure of the DUT should not be more than 10 dB above the ENR [3].

Additional errors can be introduced in noise measurements that will both limit the precision and accuracy of the measurement. Interfering signals can effect the minimum noise that is detectable since these signals provide spurious signals into the measurement receiver. To mitigate these influences, proper electronic shielding should be used when taking sensitive noise measurements. In addition, selection of the appropriate noise source can help reduce measurement errors and possibly non-linearities

of the measurement equipment. Also, if the DUT has low gain, the correction factor to remove the influence from the instrument will be large and any calibration errors will be more severe. The use of an external amplifier at the output of the DUT can mitigate these effects and improve accuracy. Also, any mismatches between the noise source, DUT, and NFA will increase the uncertainty of the measurement [2].

This technique can be combined with a conventional impedance tuner system to obtain noise parameter characteristics of devices and circuits. This is accomplished by tuning to various impedance states across the Smith chart and performing a noise measurement. By measuring at least four different impedance states, the noise parameters, R_n, $Y_{s,opt} = G_{s,opt} + jB_{s,opt}$, and F_{min}, can be determined. The following section reports measured data for the low-power X-band LNA using this Y-factor noise measurement method.

3.4 Low-Power LNA Measured Results

The LNA characterization was performed in an RF shielded room using an Agilent 8510C VNA and an ATN NP5B/Agilent 8970B system to measure scattering-parameters (SP) and broadband noise characteristics, respectively. The LNA was measured on-wafer, with calibration to remove the cable and probe losses. Two-tone linearity characterization was performed using two 8360 series swept signal generators and a 8563EC spectrum analyzer. Keithley 2400 source meter units were used to bias the LNA to $V_{cc} = 1.5$ V and $I_c = 1.33$ mA, yielding a total power dissipation of 2 mW.

Two primary low-power LNA characteristics are shown in Figure 24. The gain (S_{21}) is 10 dB at 10 GHz while the NF varies from 2.6 dB to 1.7 dB, yielding a mean NF of less than 2 dB. The -3 dB bandwidth is greater than 4 GHz, spanning 8.25 to 13 GHz. The return loss characteristics (Figure 26) indicate a good match with both S_{11} and $S_{22} < -10$ dB at 10 GHz. The isolation is better than 45 dB over the entire band (Figure 25). In addition, the input third-order intercept point (IIP_3) is 0 dBm,

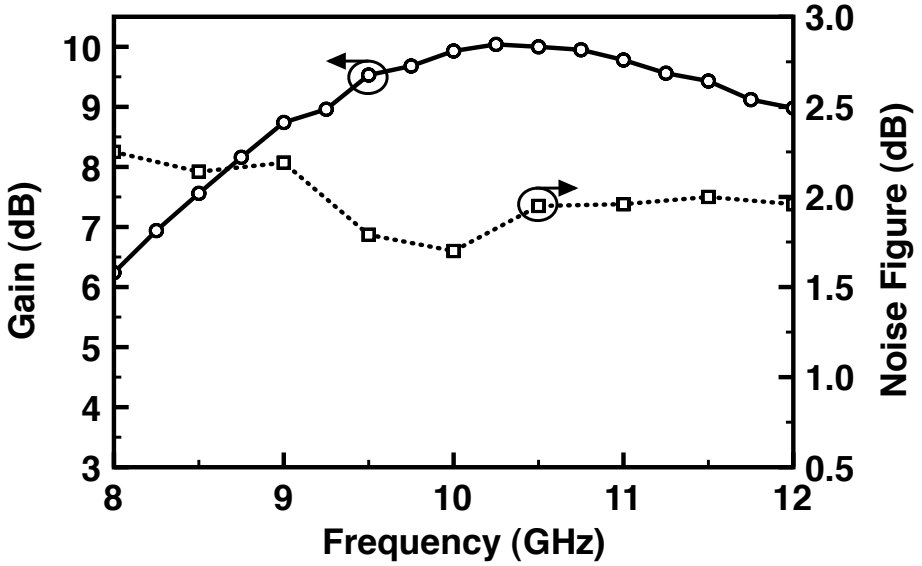

Figure 24: Measured gain and noise figure.

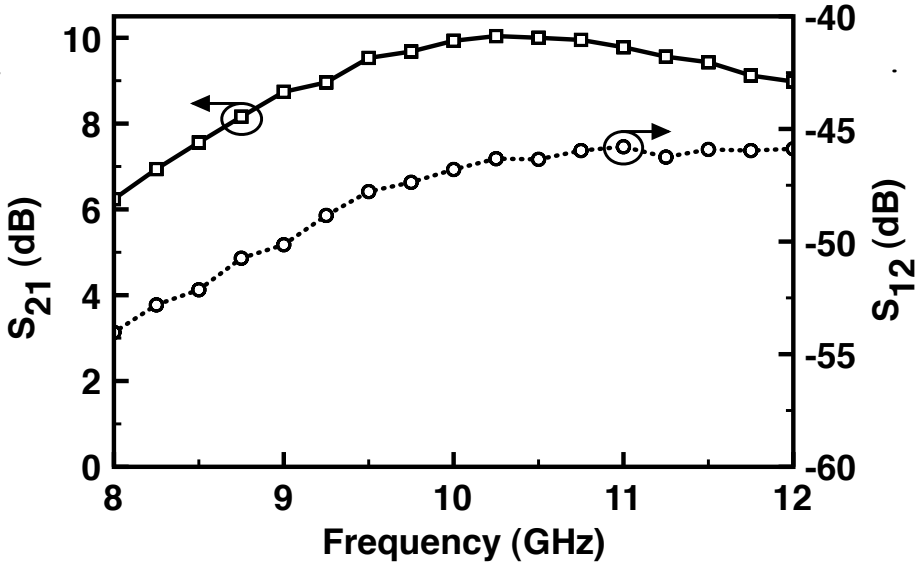

Figure 25: Measured gain (S_{21}) and isolation (S_{12}) .

using a fundamental of 10.00 GHz and a third order intermodulation term of 10.02 GHz (Figure 27).

In order to verify the matching conditions, impedance tuners were used to determine the noise parameters of the amplifier. Figure 28 plots the measured Γ_{opt} versus

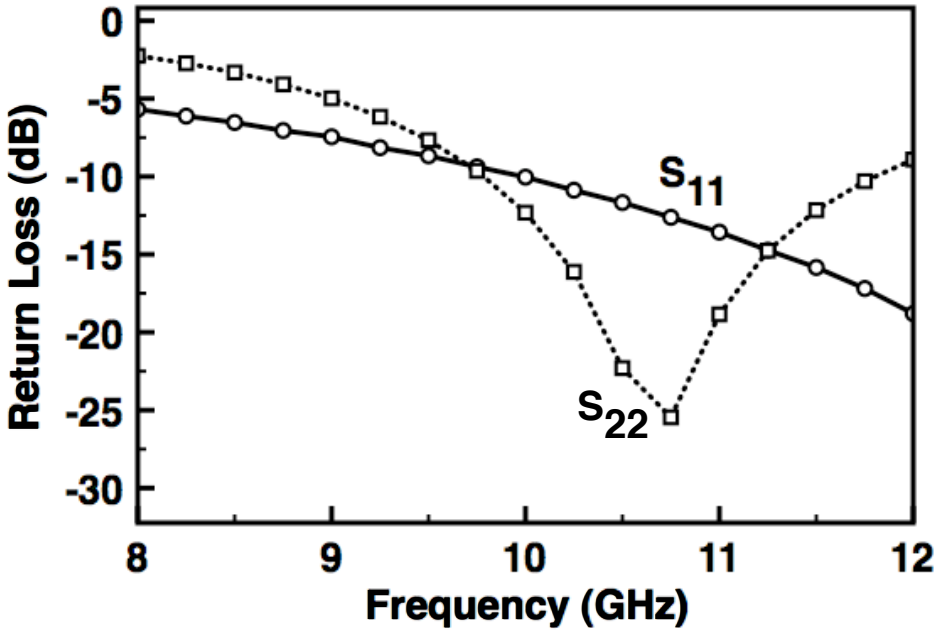

Figure 26: Measured S_{11} and S_{22} (return loss).

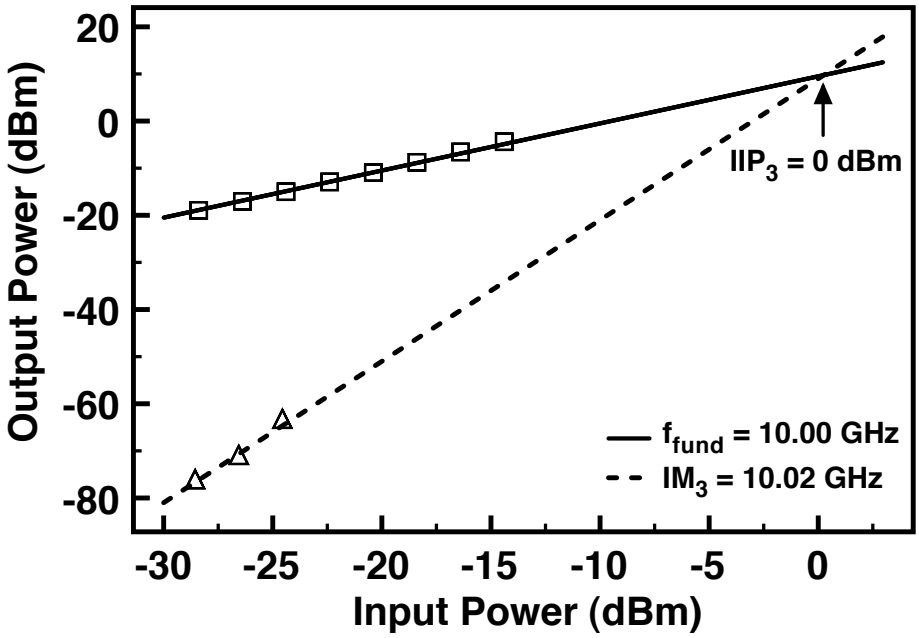

Figure 27: Measured input 3rd-order intercept point.

frequency on a Smith chart. There is only a slight mismatch toward higher frequencies, however, this graph does verify that Γ_{opt} is a slightly higher impedance than 50 Ω as was selected in the design procedure. In addition Figure 29 highlights the small

difference between NF and NF_{min}, showing that the LNA is well noise matched.

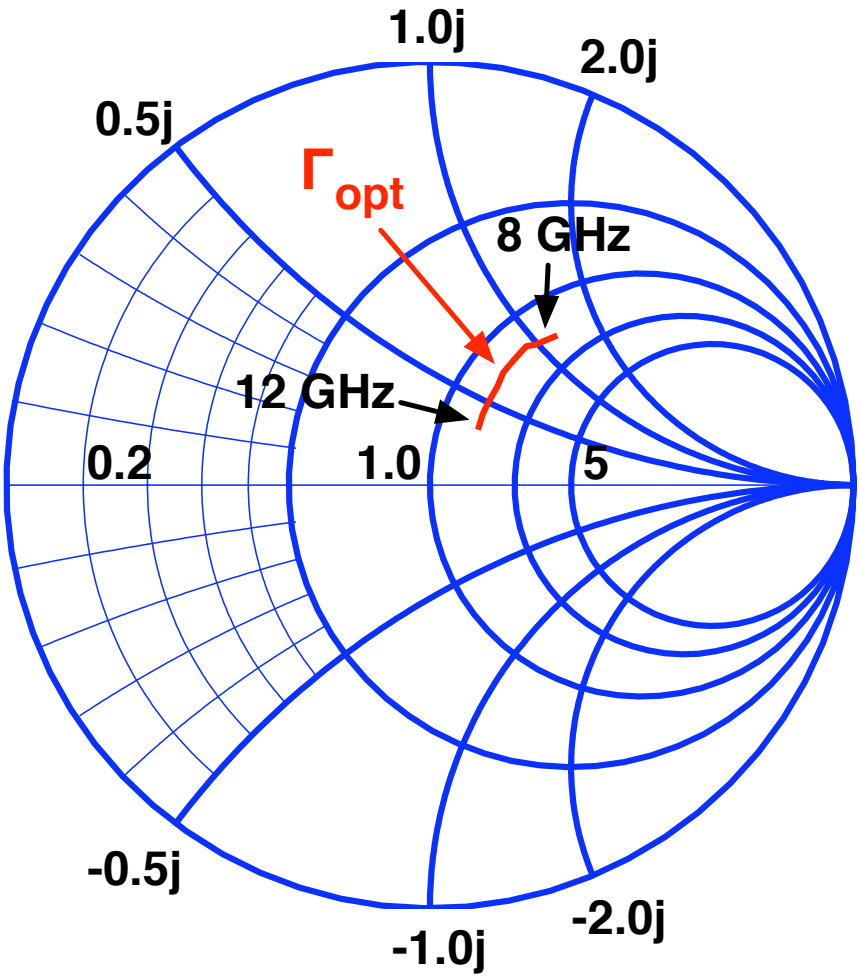

Figure 28: Measured Γ_{opt} versus frequency on a Smith chart.

3.5 Summary

In this chapter, we presented the analysis and design of a power constrained SiGe HBT LNA. The relevant measurement results for this low power LNA design are listed in Table 4. To our knowledge, this LNA demonstrates the lowest noise figure at X-band at this power level for any Si-based LNA to date. The designed LNA is well-suited for applications such as high-altitude and space-based radar systems which require ultra-low power consumption. This LNA highlights the potential of using SiGe HBT technology for low-power applications.

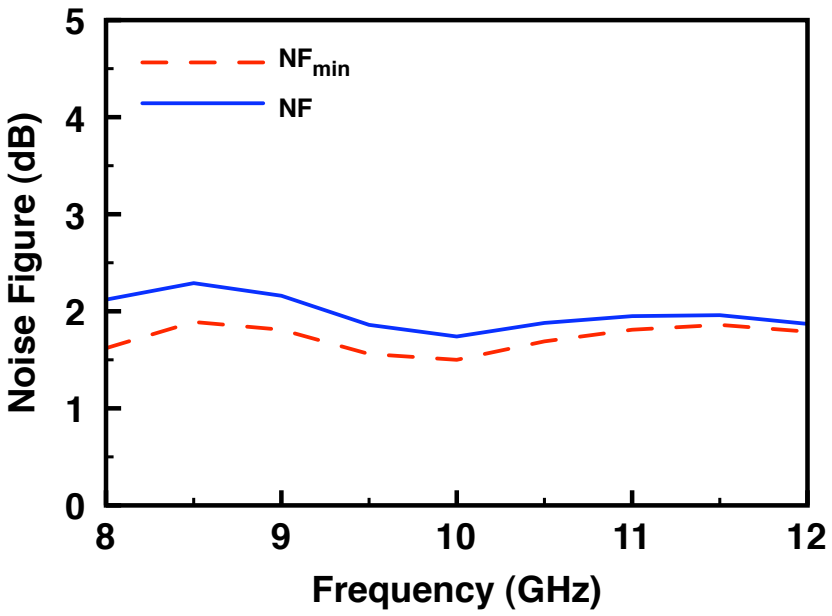

Figure 29: Measured NF_{min} and NF versus frequency indicating good noise match.

Table 4: Summary of low power SiGe HBT X-band LNA characteristics

Frequency	8.5 - 13 GHz
Gain	10 dB at 10 GHz
mean NF	1.98 dB
NF_{min} - NF_{max}	1.7 - 2.6 dB
P_{diss}	2 mW
S_{11}	-10 dB at 10 GHz
S_{22}	-12.3 dB at 10 GHz
S_{12}	$<$ -45 dB
IIP_3	0 dBm

In the following chapter, we will explore cryogenic SiGe HBT LNA applications and present measured results of two LNAs from cryogenic noise testing.

CHAPTER IV

CRYOGENIC PERFORMANCE OF SIGE HBT LNAS

4.1 Introduction

In the previous chapters, we examined high-frequency LNAs for use in radar and communication systems. Another important application for LNAs is in radio astronomy receivers. These receivers require a very high level of sensitivity due to the extremely low signal levels of cosmic radiation. The amplifiers are typically cryogenically cooled to help improve noise performance. Currently, most of these cryogenic amplifiers use InP HEMT or other III-V technology [5], [21], and [27]. The potential for SiGe HBTs in cryogenic environments has been shown in [4], [13], and [28]. These articles allude to the possible performance improvements using SiGe HBTs in cryogenic high-frequency circuits such as LNAs.

We will begin this discussion by examining some of the low-temperature performance improvements of SiGe HBTs. Next, we will introduce the cryogenic noise measurement technique and review the challenges of measuring very low noise figure devices. Lastly, we will highlight the results of two SiGe HBT LNAs operating at 15K physical temperature.

4.2 SiGe HBT Cryogenic Performance

As mentioned in section 1.2, the performance enhancements of SiGe HBTs are thermally activated, therefore, as these devices are operated in cryogenic environments, their performance greatly increases. Reviewing Equation (4) show that two terms: $\Delta E_{g,Ge}(grade)/kT$ and $\Delta E_{g,Ge}(0)/kT$ are aligned such that a decrease in temperature increases the current gain (β), which improves the *dc* and *ac* performance of

the device. Figure 30 depicts the Gummel characteristics of a third-generation SiGe HBT at both 300K and 85K [4]. Figure 31 highlights the improvement in *dc* performance as the peak β increases from 500 at 300K to almost 4000 at 85K. Lastly, improvements in SiGe HBT *ac* performance can be evidenced in Figure 32, which plots f_t as function of collector current at 300K and 85K. This plots shows a greater than 50 GHz improvement in peak f_t which is expected as the drift field is increased in the base [8]. Thus, the bandgap engineering pursued to improve room temperature performance, also aims to improve low temperature performance of SiGe HBTs. These performance improvements will also enhance device noise parameters as these relations heavily rely on β and f_t, therefore, we can expect improvements in amplifier noise performance as these devices are cooled.

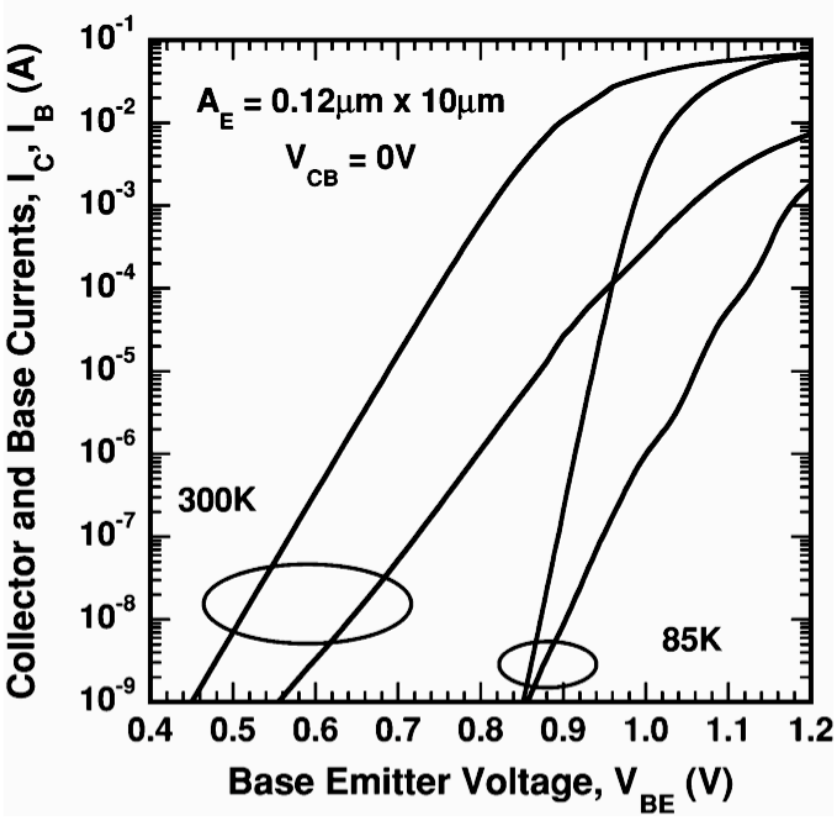

Figure 30: Forward Gummel characteristics for third-generation 0.12 × x 10.0 μm^2 SiGe HBT at 300K and 85K [4].

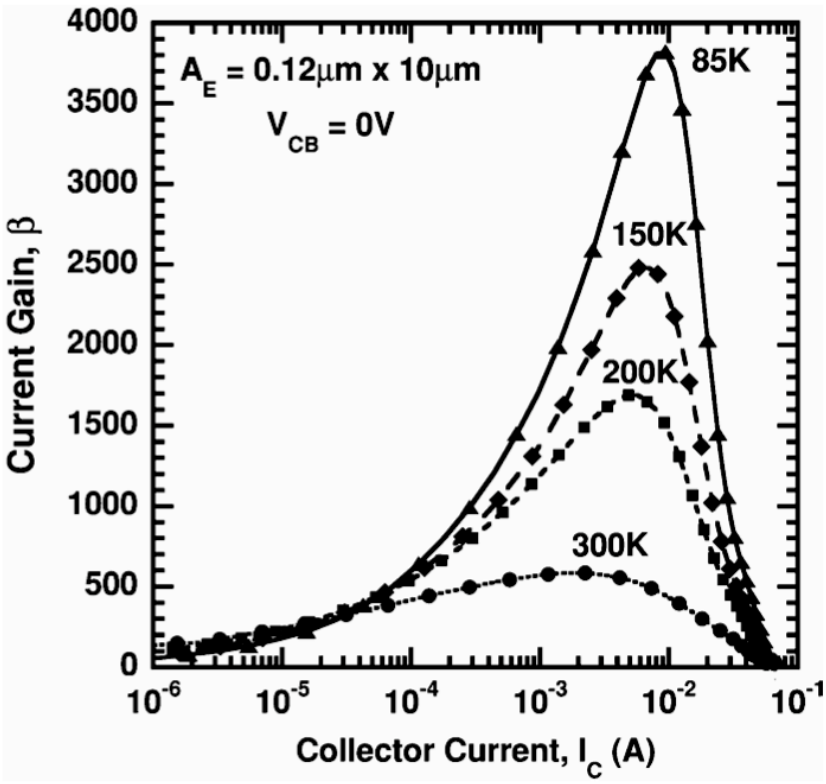

Figure 31: *dc* current gain, β, as a function of collector current for third-generation 0.12 $\times$ x 10.0 μm^2 SiGe HBT at 300K and 85K [4].

4.3 Cryogenic Noise Measurement Technique

A serious challenge in designing cryogenic LNAs is the ability to accurately measure extremely low noise figures. These cryogenic measurements discussed herein were performed using the cold attenuator method and were conducted at the CalTech RF and Microwave Group Facility in Pasadena California [26].

For very low noise applications such as radio astronomy receivers, effective noise temperature, T$_e$, is a more common metric used to define amplifier noise performance. T$_e$ is the equivalent temperature of a resistor ($v_t^2 = 4kTBR\Delta f$) that would produce the same added noise at the output of a noiseless DUT. It is typically defined as:

$$T_e = \frac{N_a}{kGB} \tag{38}$$

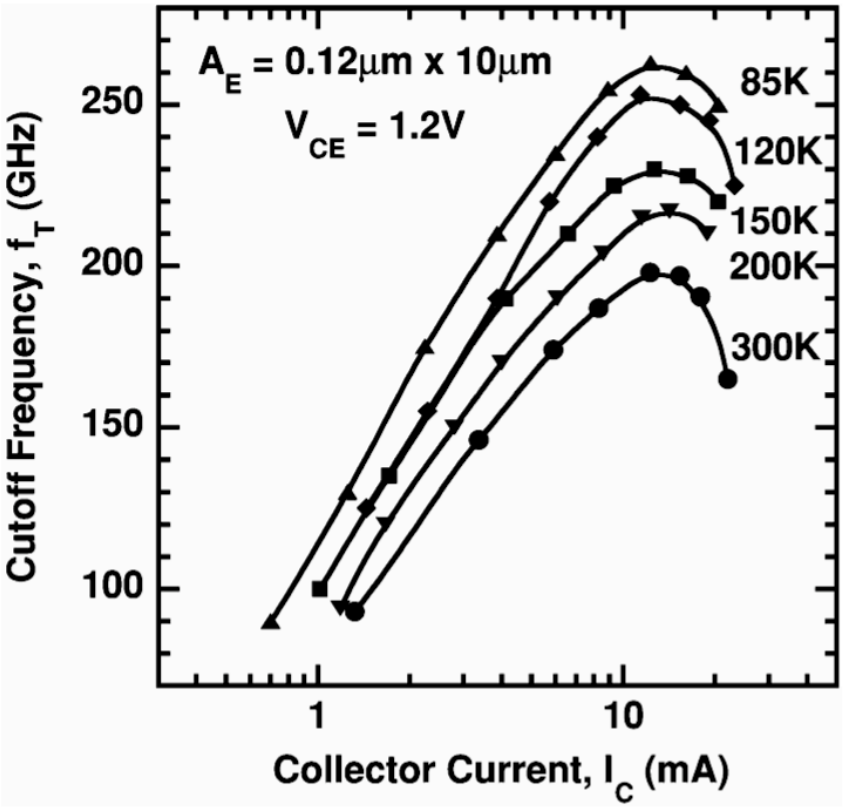

Figure 32: Cutoff frequency (f_t) as a function of collector current for a third-generation 0.12 × x 10.0 μm^2 SiGe HBT [4].

where N_a is the added noise, G is the gain of the DUT, and B is the signal bandwidth. Noise temperature can be related to noise factor by the following relation:

$$T_e = T_o(F - 1) \tag{39}$$

where T_o is the reference temperature of 290K. Noise temperature is used in these applications since the input noise level from looking into space is much less than 290K, therefore, the relationship between noise figure and SNR degradation cannot be directly calculated. This effect is due to the fact that noise figure is defined for a source impedance temperature of 290K and SNR degradation is function of the source temperature [3]. Therefore the relationship, $SNR_{out} = SNR_{in} + NF$ is not valid if temperature of the source impedances are different. For these reasons, the

noise performance given for the amplifiers in the remainder of this section will be in terms of T_e.

For a room temperature noise measurement, the off state for the diode noise source is approximately 300K. The ENR of the noise sources have a finite error ($\pm$ 1 %), which yields a variation of noise temperature of approximately 10K [1]. This uncertainty limits the minimum resolution to between 0.1 - 0.2 dB. In addition to this source of error, there is typically an impedance difference between the off and on states of the noise source which also increases the measurement uncertainty. These uncertainties prevent the characterization of very low noise temperatures, and therefore the standard noise measurement method will not yield reliable results in a cryogenic environment.

The cold attenuator method overcomes these uncertainties by inserting a temperature calibrated 20 dB pad at the input of amplifier. This attenuator lowers the effective temperature as presented to the DUT of the noise source and reduces the measurement uncertainty by a factor of 100. When the noise source is in the off state, the noise presented to the amplifier is the physical temperature of the cryogenic pad, 15K, plus a contribution from the diode noise source which is attenuated by 20 dB yielding a total noise temperature of 18K. When the noise source is on, noise temperature at the output of the noise source is approximately 9000 K which is reduced by the attenuator to 90K, including the attenuator noise, the total noise temperature is 105K. Therefore, the off and on noise temperatures presented to the amplifiers is reduced to 18K and 105K respectively, in addition, any errors due to the uncertainties of the noise source are also reduced, thus enabling accurate measurement of cryogenic amplifiers with noise temperatures below 50K [9].

In order to de-embed the noise figure of the amplifier, the temperature of the attenuator and any cables must be known very accurately. A calibrated temperature

sensor is affixed to the attenuator and a system verification was performed to determine the correction factor to enter into the Agilent N8975A Noise Figure Analyzer (NFA). The analyzer has the ability to de-embed losses at a different temperature both before and after the DUT and calculates the corrected noise temperature using the standard Y-factor noise measurement method discussed earlier. The measurement setup is shown in Figure 33, with the expanded view highlighting the internal dewar connections and the cold attenuator with the temperature sensor.

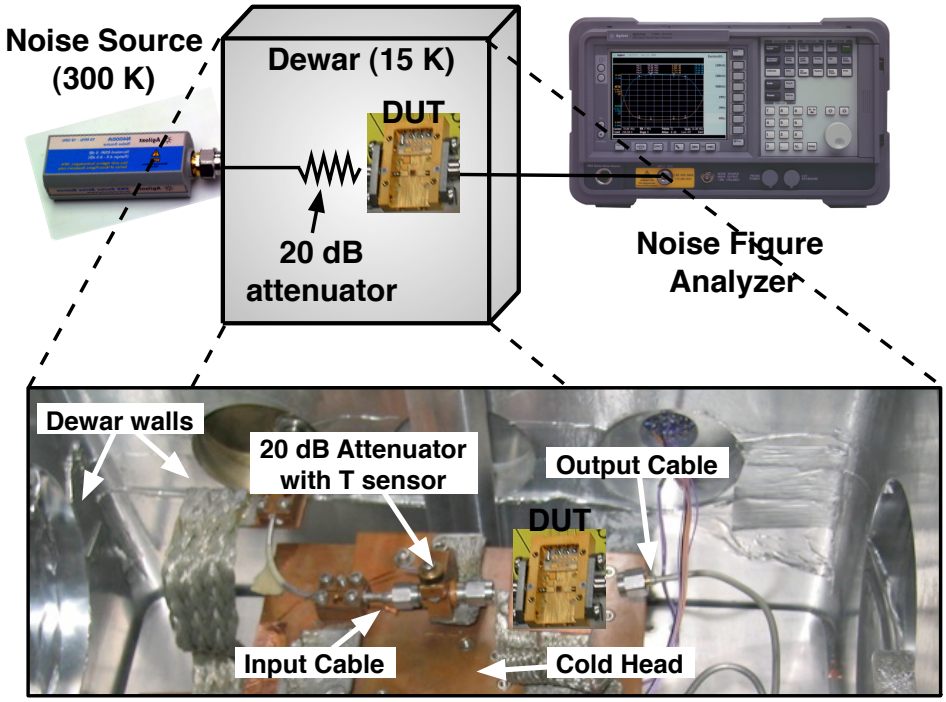

Figure 33: Schematic of cryogenic measurement setup with expanded view of inside dewar.

The measurement facility discussed here has been extensively used to measure noise figures of a variety of cryogenic amplifiers. The system has been verified against a National Institute of Standards and Technology (NIST) characterized cryogenic amplifier [9]. The remaining section discusses the results from measuring SiGe HBTs X-band LNAs in this cryogenic noise measurement setup.

4.4 Results from Cryogenic Measurement of SiGe HBT LNAs

The inductively-degenerated cascode LNA (referred to as LNA - A) [15] and the modified low-power variant (referred to as LNA - B) [25] were measured using the cryogenic noise measurement system discussed in the previous section. Neither LNA was specifically designed for low temperature operation, however, the bias currents were adjusted appropriately to achieve the lowest noise temperature performance. Figure 34 shows an example of LNA - A mounted in the package for cryogenic testing.

Both LNAs were cooled to 15K and noise and gain performance were measured. Figure 35 and 36 shows the cryogenic performance of LNA-A / LNA-B respectively. The room temperature performance of LNA - A in fixture varies only slightly from the corresponding on-wafer measurements. These room temperature measurement shows a gain of above 17 dB across band and a noise performance of above 170K (2 dB noise figure) while dissipating 15 mW of *dc* power. As shown in Figure 35, LNA-A's cyrogenic noise performance is improved dramatically with T_e below 21K (0.3 dB noise figure) and dissipating only 2.25 mW of *dc* power. The approximate 1-2 dB reduction in gain is due to the change in collector current (approximately 5 mA) which was selected to minimize noise.

Similar performance improvements can be shown for LNA-B operating at a physical temperature of 15K. Figure 36 shows over a 150K reduction in T_e and an almost 5 dB increase in gain across the band. Since LNA - B was optimized for lower current, the operating points between the room and low temperature measurement were similar with only 0.2 mA change in collector current therefore there is a gain enhancement in contrast to the gain degradation from the LNA - A measurement.

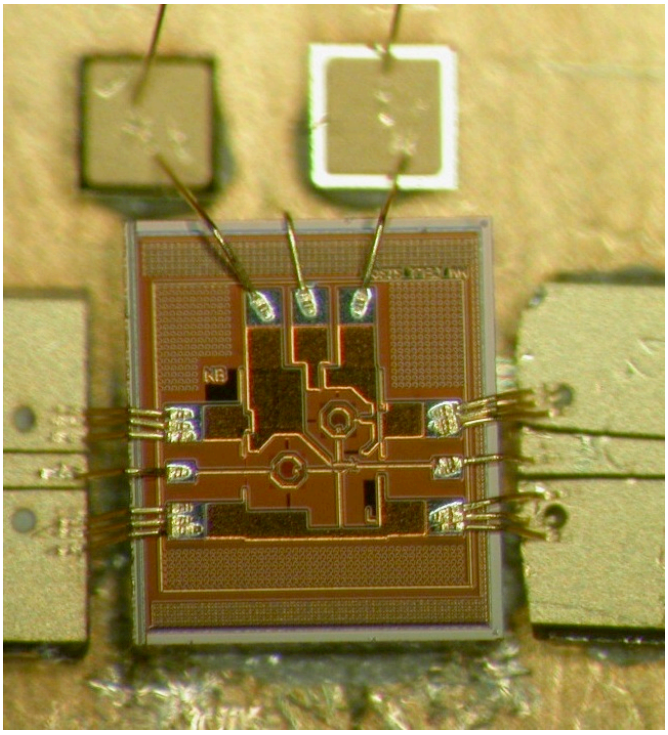

Figure 34: Photograph of X-band LNA in package for cryogenic testing.

4.5 Summary

These two examples demonstrate the dramatic performance improvements that can be achieved through cryogenically cooling these amplifiers. The effective noise temperature was reduced in both cases by approximately 150K. These amplifiers represent the lowest measured noise figure of any Si-based LNA operating at X-band in a cryogenic environment. However, neither LNA was designed specifically for low-temperature operation therefore cryogenic optimization will most likely yield increased performance. These designs do demonstrate the potential for SiGe HBT LNAs in cyrogenic applications.

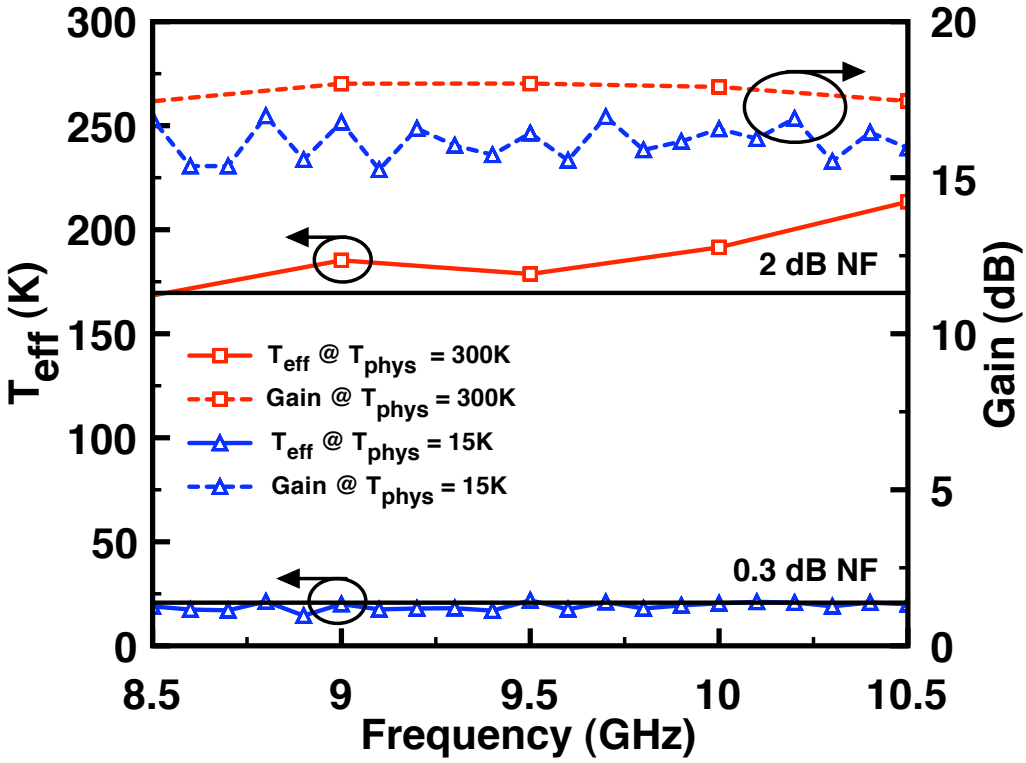

Figure 35: Effective noise temperature (K) and gain (dB) of the X-band LNA - A at 300K and 15K.

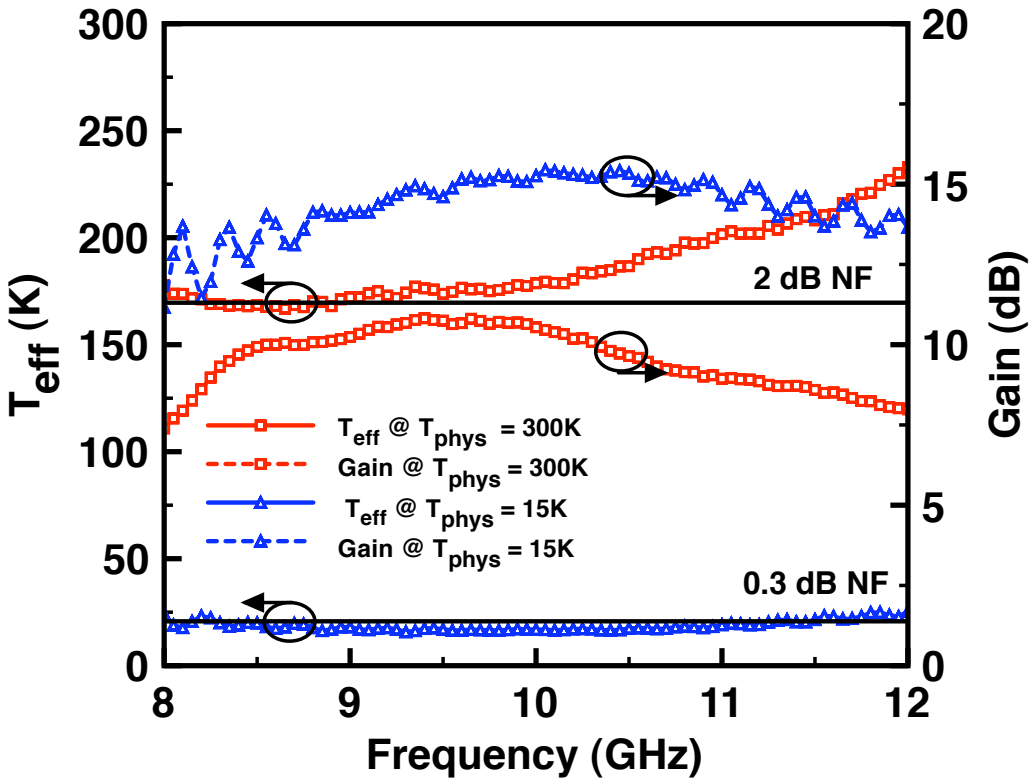

Figure 36: Effective noise temperature (K) and gain (dB) of the X-band LNA - B at 300K and 15K.

CHAPTER V

CONCLUSION

5.1 Conclusions

As we have demonstrated in this thesis, SiGe HBT LNAs have the capability to meet the demanding needs for future generation wireless systems. Combining the performance improvements of the SiGe HBT with high-frequency LNA design and optimization schemes yields record performance, capable of achieving less than 2 dB noise figure at X-band. Throughout this thesis, we have presented a thorough analysis of LNA design and optimization, providing both simulated and measured results and a framework for understanding the design trade-offs and optimization schemes required for these designs.

In Chapter 1, we reviewed the importance of LNAs in an RF front-end and their impact on receiver performance. The benefits of SiGe HBT technology were introduced and their high-frequency performance enabling characteristics were highlighted. We analyzed the noise sources in a SiGe HBT and expressed the traditional noise parameters in terms of device characteristics.

Chapter 2 concentrated on LNA design and introduced basic noise theory. Noise and gain circles were introduced and a discussion of broadband noise theory resulted in the importance of noise matching to achieve a minimum noise figure. We end this chapter with an example of a inductively degenerate cascode LNA design using SiGe HBT technology. A graphical design approach was presented to aid in understanding the design process.

In Chapter 3, we use a modification of the previous technique to present a design for a power constrained X-band LNA. The design process, simulation, and measured

results for this SiGe HBT LNA are presented and shown to have record performance. Also, we presented a brief introduction to noise measurement theory as it pertains to high-frequency LNA design. The X-band LNA was measured to have less than 2 dB of noise figure while dissipating less than 2 mW of *dc* power. This example highlights the low-power performance capabilities of SiGe HBT technology and its use in high frequency circuit design.

Lastly, in Chapter 4, we presented the results of a cryogenic SiGe HBT LNA. We began by discussing the cryogenic performance of SiGe HBTs and how these improvements can aid in low temperature LNA design. Next, we introduced the cryogenic noise measurement technique and the challenges in measuring extremely low noise figure devices. We conclude this chapter with the presentation of two LNAs measured at 15 K physical temperature and shown to have less than 21 K of effective noise temperature at X-band representing the lowest recorded noise figure of any Si-based X-band LNA.

In conclusion, we present a thorough analysis of various aspects of SiGe HBT LNA design. The aim of the analysis presented herein was to provide designers with the fundamentals of designing SiGe HBT LNAs. Both relevant design examples and measured results were presented including the results of a power constrained X-band LNA. In addition, cryogenic performance of SiGe HBT amplifiers was also presented. Through these designs and examples, we highlight the potential of using SiGe HBT technology to develop the next generation of wireless and communication systems.

5.2 Future Research

This thesis provides a general overview of high-frequency LNA design,and provides some concrete examples of X-band LNA design and the relevant results. There are many opportunities to extend this research to new areas and further understand both SiGe HBT noise performance and LNA design and optimization. Some of these new

opportunities include: high linearity LNAs, higher frequency LNAs, limits on LNA power handling/survivability, and cryogenic-optimizied LNA design.

High linearity LNAs can prove to be very useful in high dynamic range applications. By increasing receiver linearity and maintaining good overall noise figure, the range of signal levels that can be detected will be improved. Techniques such as frequency trapping and other IM_3 cancellation techniques enhance the third order intercepts by suppressing these unwanted tones [10].

Currently, the 60 GHz spectrum is a very active research area with many opportunities for creating ultrafast high-data rate wireless links [24]. High-frequency LNAs have been explored in SiGe HBT BiCMOS technologies, however, additional research could provide more insight into device and circuit optimization, dynamic range improvements, decreased power consumption, and increased bandwidth.

Also, a topic of growing concern due to device scaling and voltage limitations is survivability. As an increased number of wireless systems coexist, there is an increased probability for a very high power signal to damage the receiver. Since LNAs are the first device in the receive chain, they must be tolerant of these high power signals. There has been some research on device level damage mechanisms of SiGe HBTs [6]. Also, some research has been conducted on the survivability of GaN LNAs [23], however a study of the survivability of SiGe HBT LNAs would prove to be insightful.

Lastly, as mentioned in Chapter 4, the LNAs that were measured at low temperature were not specifically designed for cryogenic operation. Through developing an accurate and scalable low-temperature model, cryogenic SiGe HBT LNA could provide exceptionally low noise figures and possibly replace the more expensive InP and other III-V devices for radio astronomy applications. Also, designing these cryogenic LNAs for very wide bandwidths can also prove to be of much research value.

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