Low-Power ASIC Design for Multiple Integrated Sensors Applications

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Abstract

The aim of this work is to develop sensor integrated low-power chip for biomedical and other applications. Complementary metal-oxide-semiconductor (CMOS) technology in integrated circuit (IC) design has been applied to develop application specific integrated circuits (ASIC). An ASIC design that includes analog and digital sub-systems for various applications forming a system on chip (SoC) is presented. The analog sub-system drives multiple sensors, while the digital sub-system manages power, sensors, and signal output. A frequency of the pulse signals generated by the analog sub-system depends on the input voltage, which in-turn varies with sensor parameters. The frequency change of 750 MHz to 1 GHz was observed for input voltage variations of 1.2 to 2.2 V, with sensitivity of 10 mV. A separate temperature sensor included in the analog sub-system demonstrated frequency change of 830 to 440 MHz for temperature variations of -50°C to 100°C with resolution of 1°C. The output signal in digital sub-system is generated by counting the input pulses for each clock which has ‘on-state’ of only 3/16 seconds. This results in a significant reduction in the power consumption. This poster presents and discusses the system design and simulation results.

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