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Afshin Izadian

Maher Rizkalla

Lingxi Li

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Approved by Major Professor(s): Afshin Izadian

Maher Rizkalla

Approved by: Brain King 04/21/2014

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SOLAR MICRO INVERTER

A Thesis

Submitted to the Faculty

of

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by

Shweta Hegde

In Partial Fulfillment of the

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ABSTRACT

Hegde, Shweta. M.S.E.C.E., Purdue University, May 2014. Solar Micro Inverter. Major Professors: Afshin Izadian and Maher Rizkalla.

The existing topologies of solar micro inverter use a number of stages before the DC input voltage can be converted to AC output voltage. These stages may contain one or more power converters. It may also contain a diode rectifier, transformer and filter. The number of active and passive components is very high.

In this thesis, the design of a new solar micro inverter is proposed. This new micro inverter consists of a new single switch inverter which is obtained by modifying the already existing single ended primary inductor (SEPIC) DC-DC converter. This new inverter is capable of generating pure sinusoidal waveform from DC input voltage. The design and operation of the new inverter are studied in detail. This new inverter works with a controller to produce any kind of output waveform. The inverter is found to have four different modes of operation. The new inverter is modeled using state space averaging. The system is a fourth order system which is non-linear due to the inherent switching involved in the circuit. The system is linearized around an operating point to study the system as a linear system. The control to output transfer function of the inverter is found to be non-minimum phase. The transfer functions are studied using root locus. From the control perspective, the presence of right half zero makes the design of the controller structure complicated.

The PV cell is modeled using the cell equations in MATLAB. A maximum power point tracking (MPPT) technique is implemented to make sure the output power of the PV cell is always maximum which allows full utilization of the power from the PV cell. The perturb and observe (P&O) algorithm is the simplest and is used here.

The use of this new inverter eliminates the various stages involved in the conventional solar micro inverter. Simulation and experimental results carried out on the setup validate the proposed structure of inverter.

CHAPTER 1. INTRODUCTION

1.1 Need for Renewable Energy

The rapid depletion of fossil fuel resources has created an urgent need for use of alternate and renewable energy sources to meet the coming scary future of rapid consumption and population growth [1]. Today's world is excessively worried about fossil fuel exhaustion and environmental impacts, hence renewable energy sources such as wind energy, solar power, thermal gradients, biomass energy, etc. have become the hub of the present generation for energy extraction. Green energy sources flourish in our surroundings. Among the diverse ambient energy sources available, solar energy has become the most popular one since it is clean, inexhaustible and free [2]. The use of the photovoltaic (PV) array as an electrical energy source is providing to be a critical solution to the long awaited answer to the growing energy demand [1].

Since the shortage of traditional fossil fuel is getting increasingly acute and thermal power generation is unfriendly to the environment, alternative and renewable energy is gaining more and more importance. Compared to other inexhaustible and clean source such as wind energy, solar energy can be easily developed with a wider range in the world. Recently, the photovoltaic (PV) power conversion development comes into people's view due to a remarkable advancement [3].

Even though the availability of solar energy depends on the climatic conditions, it has higher power density compared to supplementary renewable energy sources which makes it more popular. Numerous methods exist for extracting solar energy. Many conventional methods include a dc-dc converter followed by an inverter for ac voltage applications [2].

Photovoltaic (PV) generation is gaining increased importance as a renewable source due to its advantages like absence of fuel cost, little maintenance, no noise and no wear due to absence of moving parts etc. In particular, energy conversion from solar cell array (SCA) received considerable attention in the last two decades [4]. The continuing decrease of the cost of the PV's, the advancement of power electronic and semiconductor technology and favorable incentives in a number of industrial countries in general had a profound impact on the commercial acceptance of grid connected PV systems in the recent years. A core technology associated with these systems remains the inverter, which has evolved to quite mature technology offering a number of advantages to customers that were not possible many years ago. The technology has changed from line commutated inverters to switch mode ones mainly due to the availability of high frequency fully-controlled switching devices [5].

1.2 DC-AC Converters

Switch-mode dc- ac inverters have been used in various types of applications, such as uninterruptible power supplies, communication ring generators, aerospace power systems, and variable-speed ac machine drives [6]. Traditionally, a bridge configuration is employed for the switch-mode dc-to-ac inverters. By using a pulse width modulation (PWM) switching technique, the input dc voltage is transformed into a high-frequency pulse waveform at the output of the bridge. Through a filter, this high-frequency pulsed voltage is smoothed into a sinusoidal waveform [6]. However, switch-mode dc-ac inverters which employ dc-dc converter topology have eliminated the use of a filter at the output [7].

Conventional voltage-fed inverters (VSI) are subject to the inherent drawbacks that they can either step down or step up voltage. In addition the upper and lower devices of each phase leg cannot be gated on or off simultaneously in the conventional voltage-fed inverter, either by purpose or EMI noises [8]. As the number of levels of output required increases, the number of active and passive elements required in VSI increases which increases the cost and volume. A possible solution to improve power density while

keeping the cost low is to reduce the active and passive components. This led to interest among researchers to develop inverter topologies having reduced count of switches [9] - [15].

In recent years, the increase in medium and high voltage and power applications has led to development of voltage source inverters. The developments of flexible ac transmission system devices, medium voltage drives, and different types of distributed generations, have provided great opportunities for the implementations of medium and high power inverters. In these applications, the frequency of the pulse-width modulation (PWM) is often limited by switching losses and electromagnetic interferences caused by high dv/dt [16]. Since multilevel inverters have a large number of power devices, any device failure may cause the abnormal operation of the electrical drives, and require shutdown of the inverter and the whole system to avoid further serious damage. However, in some critical industrial processes with high standstill cost and safety-aspect concern, high reliability and survivability of the drive system is very important [17].

The DC-DC converters that can operate in both buck and boost modes are buck-boost, Cuk, and SEPIC converters. However, the buck-boost and Cuk converters, in their basic form, produce the output voltage, whose polarity is reversed from the input voltage [18]. On the other hands, the SEPIC (Single-Ended Primary Inductor Converter) converter is capable of operating in both step-up and step- down modes and does not suffer from the polarity reversal problem.

Multilevel inverters have been preferred in high voltage and high power applications. The reason is the large number of advantages it has over two level inverters. They have the advantage of producing high-voltage, high-power capability with improved voltage quality. It also reduces the power ratings of the required power devices. As the number of voltage level increases, the output voltage waveform adds more steps and the output waveform has lower total harmonic distortion (THD) [13]. For a pure sinusoidal waveform as output, the numbers of levels required are infinite. In addition, the output filtering capacitors in the dc-to-dc converters can be a dc-type capacitor, e.g., an electrolytic capacitor which is smaller and less expensive than the ac-type capacitor for

the same capacity required in the bridge configuration. However, the inverters using bridge configuration must use an ac-type capacitor as a filter. More important is that, with a dc-dc converter topology, the advanced control techniques, such as current mode control, digital data sampling control, and sliding-mode control, etc., developed from the investigations of dc-dc converters can be directly applied to the dc-ac switch mode inverter. Therefore, a good dynamic performance can be achieved [6].

Compared to the bridge-type inverter, the inverter using a dc-dc converter configuration has several advantages. Only one switch operates at high frequency and, as a result, switching losses will be significantly lower [15]. In inverters, the total power losses can be divided into the following: switching losses, snubber losses, conduction losses and off-state losses. Generally, switching losses depend on switching frequency of power semiconductor devices and instantaneous value of device voltage and current during switching interval. Increasing the switching frequency reduces the need of filtering equipment but leads to high switching losses and decrease in efficiency. In low switching frequency applications, the proportion of switching losses is very less and can be neglected because total switching time is much less than the switching cycle. Switching losses become dominant part of the total power loss in high switching frequency applications [9]. In a multilevel inverter, large number of levels requires large number of switching devices which leads to large switching losses. Reducing the switching losses is an important issue to increase the power capability of standard inverters. Since a significant part of the losses is directly proportional to the switching frequency of the semiconductor devices, this should be reduced in order to increase the maximum rated load current. Unfortunately this will increase the current harmonics due to the lower effective PWM frequency and consequently the maximum fundamental current is reduced [19]. However, the major advantage of multilevel inverter is that their switching frequency can be lower than the conventional two level inverter for the same THD of the output voltage, which means lower switching losses [13]. The switching losses can also be reduced if the number of switches used in the inverter is reduced.

1.3 About this thesis

In this thesis, a new topology for the solar micro inverter is introduced. The conventional bridge inverter is replaced by a new single switch inverter which is a modified version of the DC-DC SEPIC converter. The design and operation of the new inverter is studied. The inverter is modeled using state space averaging technique and small signal modeling. The control to output transfer function of the inverter is studied using root locus maps. The effect of varying component values on the operation of the inverter is studied in detail. On the basis of this study, a controller is designed for the inverter which enhances the capability of the inverter to produce a sinusoidal output waveform. A sizing procedure is developed for the new inverter. The advantage that this inverter possesses over conventional bridge inverters and multilevel inverters is that the efficiency is improved while the switch count is reduced. Also, the total harmonic distortion is reduced to a great extent.

This inverter, along with a PV array will complete the new model of solar micro inverter. A maximum power point tracking (MPPT) method needs to be implemented to ensure that the maximum power is always harnessed. The perturb and observe (P&O) algorithm is used as it is the simplest algorithm. While the algorithm ensures that the panel operates at the voltage associated with maximum power, the inverter is capable of boosting and inverting the voltage to be compatible with the grid. Simulation and experimental results validate the operation of the proposed inverter.

CHAPTER 2. SOLAR MICRO INVERTER

2.1 Introduction

With the draining of fossil fuel and increasingly serious pollution caused by traditional power generation methods across the world, renewable and pollution-free energy has gained much attention in economic and political fields. Majority of renewable energy sources include photovoltaic (PV) and wind power generation systems. Wide application of renewable energy is now impeded by cost and extensive researches shall be conducted in order to improve the cost effectiveness. PV converter systems, also known as solar inverters, have gained popularity in recent years as a convenient renewable energy with bright prospects [20].

A solar micro inverter is a device that is capable of converting the dc voltage obtained from the solar PV array into grid-compatible ac voltage. Typically, the micro inverter is attached to every single PV panel. As the name suggests, these inverters are designed for lower power ranges, usually 190-220 W. However, as the capacity of solar panels increases, the size of micro-inverters should increase as well.

Micro inverters connected to a single PV panel are becoming the trend for the future of grid-connected PV systems due to the following reasons [21]:

1) Improved energy harvest
2) Improved system efficiency
3) Lower installation costs
4) Plug-N-play operation
5) Enhanced flexibility and modularity

2.2 Evolution of Solar Inverters

1. Centralized Inverters: The PV modules are divided into series connections (called a string), where each string is capable of generating a sufficiently high to avoid further amplification. These series connections panels are then connected in parallel, through string diodes, in order to reach high power levels. This centralized inverter includes some severe limitations, such as high-voltage dc cables between the PV modules and the inverter, power losses due to a centralized MPPT, mismatch losses between the PV modules, losses in the string diodes, and a nonflexible design where the benefits of mass production cannot be reached. The grid-connected stage was usually line-commutated by means of thyristors, involving many current harmonics and poor power quality [22].

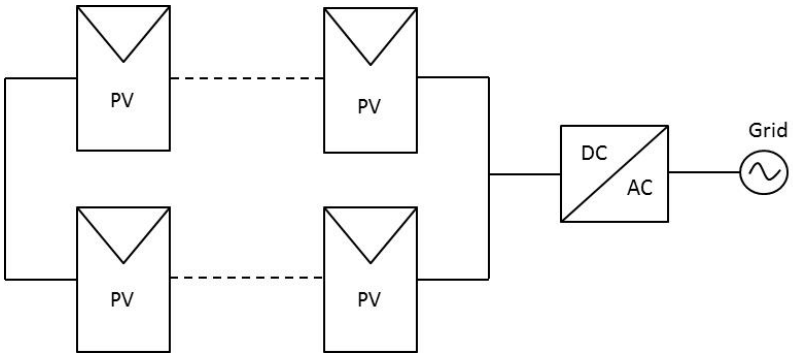


Figure 2.1 Centralized inverter

Advantages of Centralized Inverters [23]:

i. Low capital price per watt
ii. High efficiency
iii. Comparative ease of installation – a single unit in some scenarios

Disadvantages of Centralized Inverters [23]:

i. Size and Noise
ii. A single potential point of entire system failure

2. String Inverters: The string inverter is a reduced version of the centralized inverter. In this type of inverter, a single string of the PV modules is connected to each inverter [22]. The input voltage may or may not be sufficiently high to avoid voltage amplification depending on the number of PV panels [3]. The choice of employing fewer number of PV modules in series also exists, if a dc–dc converter or line-frequency transformer is used to provide voltage amplification. There are no losses associated with string diodes and separate MPPTs can be applied to each string. This increases the overall efficiency compared to the centralized inverter, and reduces the price. The device can now be used like a "plug and play" device, which can be used by person without any knowledge of electrical installations. On the other hand, the necessary high voltage-amplification may reduce the overall efficiency and increase the price per watt, because of more complex circuit topologies. On the other hand, the ac module is intended to be mass produced, which leads to low manufacturing cost and low retail prices [22]. Powers of such inverters are relatively low, which can result in the low internal temperature and prolong inverter operating life [3].

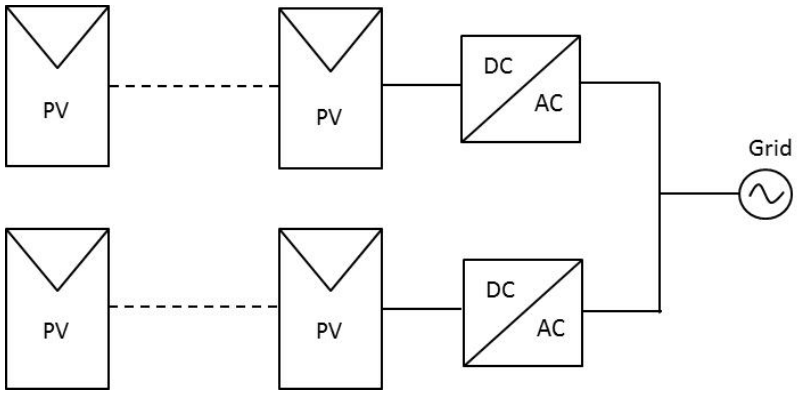


Figure 2.2 String inverter

Advantages of String Inverters [23]:

i. Allows for high design flexibility
ii. High Efficiency
iii. Robustness

iv. 3-phase variations available
v. Low cost
vi. Well supported
vii. Remote system monitoring capabilities

Disadvantages of String Inverters [23]:

i. No panel level MPPT
ii. No panel level monitoring
iii. High voltage levels present a potential safety hazard.

3. Multi String Inverters: The multi-string inverter is the further development of the string inverter, where several strings are connected to their own dc–dc converter and then a common dc–ac inverter is used to interface the common dc-link to the AC grid. The advantage that this configuration offers over the centralized inverters is that every string can be controlled individually. The size of the system can be increased easily as a new string with a dc-dc converter can be plugged into the existing system [22]. Therefore, it can achieve a higher system efficiency and more flexible design scheme [3].

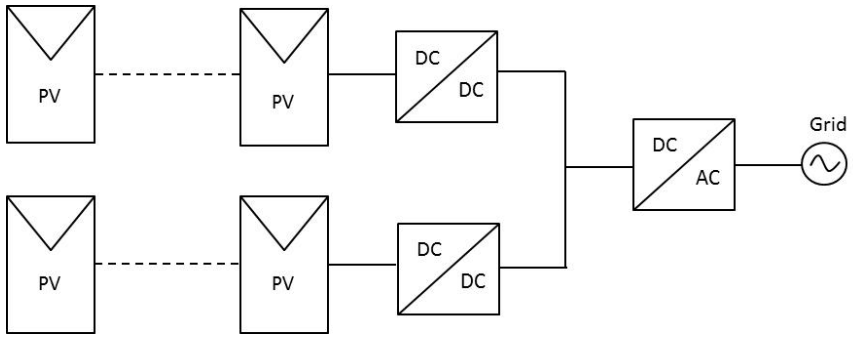


Figure 2.3 Multi string inverter

4. Micro Inverters: A PV module composed of a PV panel with an individual DC-AC inverter is called solar micro-inverter. In micro inverters, one inverter is connected to each solar panel. These inverters are connected to the back of

every solar panel [24]. This structure integrates the PV module and the inverter into a device. Each micro-inverter needs to harvest the optimum power by performing maximum power point tracking for its connected panel. Since there is only a PV module, it has several merits such as no mismatch of losses and easy realization of optimal adjustment between different units. With this modular structure, the system is easier to enlarge. Besides, even persons without relevant knowledge can use the device since it can be produced as a plug-and-play unit [3].

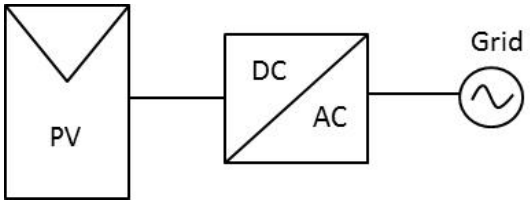


Figure 2.4 Micro inverter

Advantages of Micro Inverter [23]:

i. Panel level MPPT
ii. Increase system availability – a single manufacturing panel will not have such an impact on entire array
iii. Panel level monitoring
iv. Lower dc voltage, increasing safety. No need for ~600V dc cabling requiring conduits
v. Allows for increased design flexibility, modules can be oriented in different directions
vi. Increased yield from sites that suffer from overshadowing as one shadowed module doesn't drag down a whole string
vii. No need to calculate string lengths – simple to design systems
viii. Ability to use different makes/models of modules in one system, particularly when repairing or updating older systems

Disadvantages of Micro inverter [23]:

i. Higher costs in terms of dollars per watt, currently up to double the cost compared to string inverters
ii. Increased complexity in installation.
iii. Given their positioning in an installation, some micro inverters may have issues in extreme heat.
iv. Increased maintenance costs due to there being multiple units in an n array.

However, all the advantages that micro inverters have come with additional design challenges. The two main challenges associated with micro inverters are achieving the high efficiency and keeping low cost-per-watt of generation. These challenges become much more significant due to several system constraints: high-voltage transformation ratio from low-voltage DC panel voltage to grid compatible AC-voltage, safety isolation requirements, extreme temperature variations and uncontrolled environmental conditions due to its mounting to the solar panels, lower profile and expectation of very high reliability (comparable with the solar panel itself). Due to these design challenges there is always a quest for newer and better topologies/techniques in solar inverter manufacturers [24].

2.3 Types of Micro Inverters

Traditionally two approaches for energy conversion are being used in the solar inverters. The first approach is to use a single-stage topology. In this approach, the solar panel DC-voltage is converted to AC-voltage in a single step or there is only a high frequency switching stage [24]. A DC-AC inverter forms the high frequency stage and a transformer is used at the inverter output terminals. The second approach is called as two-stage or multiple-stage approach. In this type the solar panel, voltage is converted to AC voltage in multiple stages of power conversion. First, the low voltage from the panel is converted into a high-voltage DC and then the high-voltage DC is converted to a grid-

compatible AC-voltage [24]. In this scheme, the PV system requires to have two power electronic converters which have power rating almost equal to the PV array power capability. Further, this scheme needs the synchronized control circuitry both for dc-dc converter and inverter. The only advantage of this scheme is that it reduces the transformer [4]. Since the single-stage architecture has a single high frequency switching converter, the number of power electronic converters requirement, in this scheme, is less and the problems arising due to them are also less [4]. It also leads to lower overall losses in the system. This leads to the conclusion that this is a better approach for achieving high efficiency [24].

Based on the electrical isolation between the input and output terminals, inverters can be classified as isolated inverters or non-isolated inverters. While electrical isolation is usually achieved using transformers, either line-frequency transformers as in Figure 2.5 or high-frequency transformers as in Figure 2.6 can be employed. Depending on the input dc voltage range in comparison to the output ac voltage, inverters can be buck inverters, boost inverters, or buck-boost inverters [25].

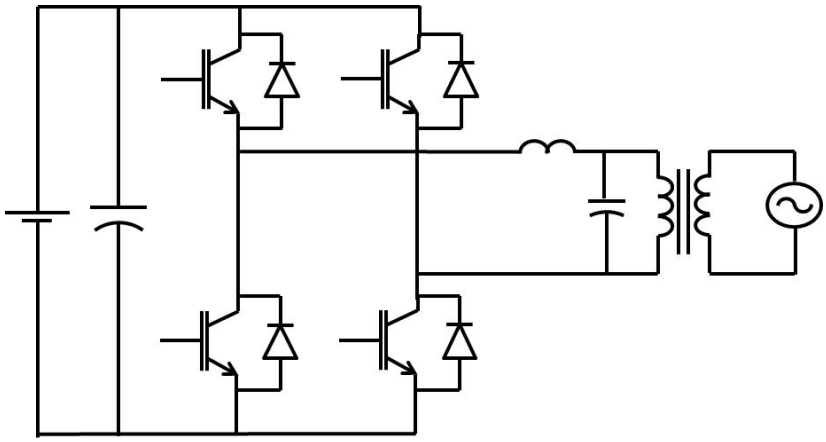


Figure 2.5 Traditional buck inverter and line-frequency transformer

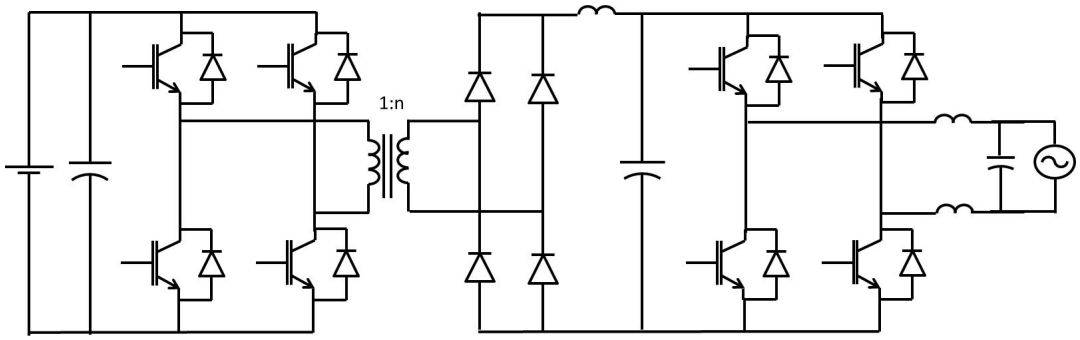


Figure 2.6 Multiple-stage inverter with high frequency transformer

The inverters shown in Figures 2.5 and 2.6 function as buck inverters, but the entire topologies together represent either a boost or a buck-boost inverter owing to the PWM operations implemented and step up the voltage in low frequency or high frequency.

Based on the number of power switches [25], single-phase inverters can be classified as

1) Four-switch topologies
2) Six-switch topologies

In a multiple-stage power inverter, e.g., a two-stage inverter, boost and isolation (if necessary) are carried out in the first stage while the inversion is conducted in the second stage [25]. The controls for each stage can be implemented separately or a single synchronous control system can be designed to control all stages simultaneously. A number of multiple stage topologies have been found which would use the buck-boost nature of an inverter. For the buck or boost operation, either a dc–dc converter or dc–ac–dc converter can be used in the first stage. For the choice of dc-link, the system can be configured with a dc-link followed by a PWM inverter or a pseudo-dc-link followed by a line-frequency operated inverter [25].

Multiple-stage inverters can be classified as:

1) DC-DC-AC topologies: In this topology, the power conversion process can be easily divided into two different stages – dc-dc and dc-ac conversions. In this case,

the dc-dc converter may be controlled to track the maximum power point of the PV module and the dc-ac converter may be controlled to produce ac power of unity power factor [26].

Many conventional methods include a dc-dc converter followed by an inverter for ac voltage applications [2]. In this topology, the dc voltage from the solar panel is stepped up to a higher level by a dc-dc converter and then the inversion is achieved by using a dc-ac converter stage. The first method is to the use transformerless inverters which have the advantage of reduced size and cost and high efficiency. In these inverters, the necessary boosting of voltage may not be obtained for the universal grid voltage range (85-265V ac). Also, in the absence of transformers, there are serious issues related to the grounding of the solar cell side of the inverter. The second method uses an isolated scheme which consists of one or more dc voltage boosting stages and an inverter with proper isolation using a line frequency or high frequency transformer. The problems of insufficient voltage boosting and grounding of solar cell can be eliminated by using this topology. Also the problem of leakage current caused by the earth parasitic capacitance is avoided using isolation transformer [2].

A two stage boost inverter can be formed by cascading a DC-DC boost converter before the buck inverter as shown in Figure 2.7. In this topology, the output of the first stage is raised dc voltage with tolerable ripple. A high frequency PWM buck inverter is used in the second stage to generate the required ac waveforms. In this topology, synchronization between the two stages is not required. The control of output power is usually implemented in the second stage. Also, controls can be implemented on the first stage so as to make the dc link voltage a rectified sine wave. Then the second stage would only need to convert the waveform into ac voltage of line frequency. This method would improve the efficiency by reducing the overall switching losses and saving the large intermediate dc-link capacitor [25].

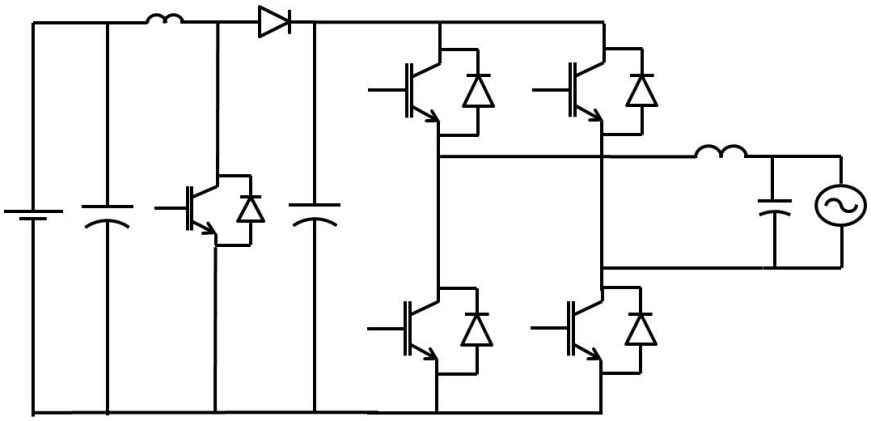


Figure 2.7 Two stage boost inverter

According to the dc link configurations, the micro inverter topologies can be classified into three different arrangements:

a) With dc-link: The dc-dc conversion may be achieved by using half bridge converter, full bridge converter, push-pull converter, buck boost converter, fly back converter, cuk converter, zeta converter, D2 converter or two inductor boost converter. The dc-ac conversion is obtained by using a full bridge inverter.

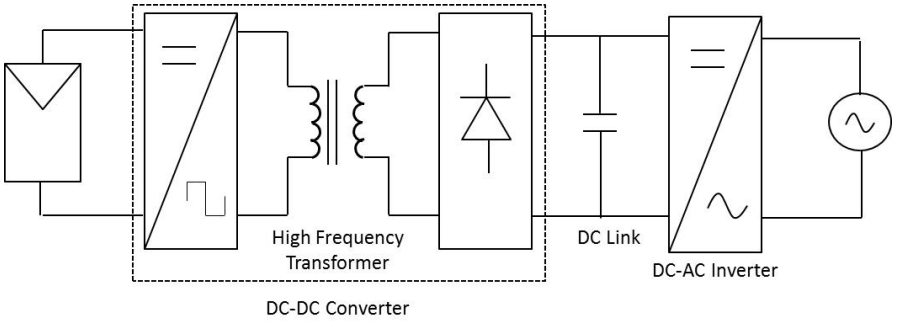


Figure 2.8 Micro-inverter with dc-link

In this topology, the power conversion process can be simply divided into two separate stages: dc-dc and dc-ac. Usually, the dc-dc converter is controlled in a way to track the maximum power point of the solar PV array. The dc-ac converter may be controlled to obtain desired ac power.

However, two major drawbacks do exist in this arrangement [26].

- The dc–ac converter generally requires PWM control in order to meet the harmonic requirements by the grid but this control technique is comparatively complex to implement. The control circuitry can be greatly simplified by the modern microcontroller technology but complications do exist in the gate driver design in order to produce fast turn-on and turn-off transients under high frequencies.
- If only the hard-switching topologies are used, the switching loss tends to be high as the semiconductors in both conversion stages switch at high frequencies. Power loss in the gate driving circuit can also be significant with the conventional totem-pole arrangement and this will further deteriorate the converter overall efficiency. To minimize the drawback of this arrangement, soft switching technique can be utilized in both conversion stages. However, the tradeoff could be higher components count therefore a higher cost and a lower reliability.

In this arrangement, it is favorable to place the power balancing capacitor at the dc link. Since the dc link voltage is of the same level as the grid, the energy stored by the capacitor per unit volume is high and this allows a better and condensed overall design.

b) Pseudo dc-link: In this topology, a rectified sinusoidal voltage is generated on the dc link by a modulated dc-dc converter or the cascade of a modulated dc-dc converter and a non-modulated dc-dc converter. A grid-commutated dc–ac converter with the square-wave control unfolds the link voltage to the sinusoidal form in phase with the grid [26].

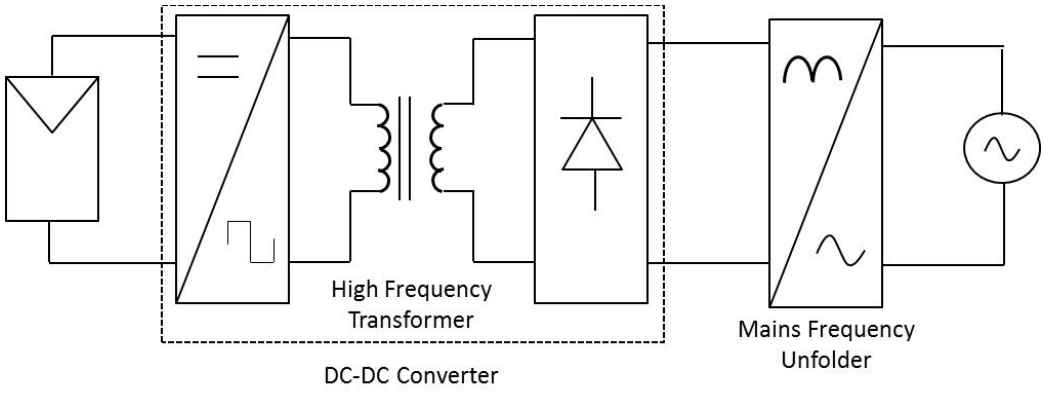


Figure 2.9 Micro-inverter with pseudo dc-link

Amongst all the existing topologies based on the dc-links, the micro inverter with a pseudo dc link has received the greatest interest and a large number of the reviewed topologies employ this arrangement [26]. Except the ease of design of controller for this micro inverter, the advantage that this topology offers is that the dc-ac inversion occurs at line frequency. Simple square-wave control can be employed and high switching losses can be avoided even with the hard-switched design. However, more challenging control techniques may be required in the dc–dc conversion stage due to the need for modulation [26]. In this topology, if a non-isolated dc-dc converter is employed, high frequency transformer can be removed to offer space and cost saving.

Further size and cost reduction of the micro inverters can be achieved by using the single-stage converter topology. These topologies normally consist of two relatively independent converters with possible shared passive components and each converter produces a half cycle sinusoidal waveform 180 out of phase [26]. It has increased efficiency due to the smaller component count and lower power loss. This topology does suffer from the following drawbacks.

- The transformerless inverters have limited ac peak voltages that are less than dc bus voltages.
- The dual grounding becomes a difficult issue in the transformerless inverters.

- The working range of dc voltage in the single-stage inverters is more limited than the range of dc voltage in multi-stage inverters.

In this arrangement, the most favorable place for the power balancing capacitor is at the converter input as it needs to provide a wide range of voltage for control. This would eliminate any large capacitors present in the system. Compared with the capacitive energy storage at the dc link, this solution has an obvious disadvantage of lower energy storage per unit volume [26].

c) Without dc-link: Fig 2.10 shows the micro inverter implementation without a dc link, where the dc voltage is transformed to a high frequency ac voltage and amplified to a higher level compatible with the ac grid. A frequency changer follows and directly translates the ac voltage or current of the high frequency to that of the grid frequency in the absence of any kind of the dc link [26].

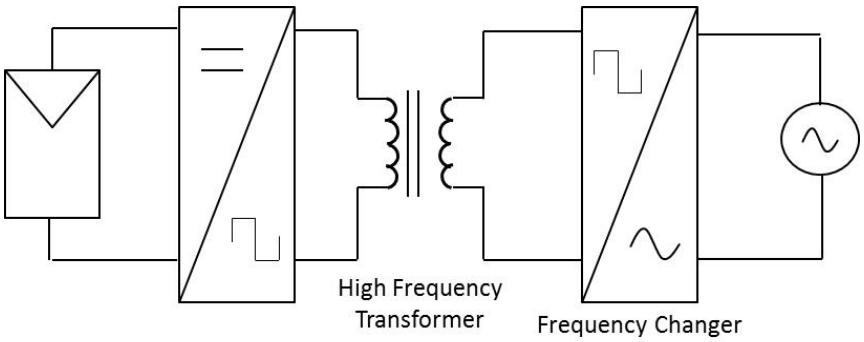


Figure 2.10 Micro-inverter without dc-link

The major advantage of the frequency-changer-based micro inverter is the reduction of the total power conversion stages to two. With the current technology, the construction of the bidirectional switches remains a challenge and this greatly hinders the development of the micro inverter topologies with frequency changers. However, this arrangement does open the possibility of lower component count and higher overall efficiency along with the technology advancement [26].

However, the system now required more sophisticated and higher bandwidth controls as there is no intermediate energy storage stage. Also, the dc-dc and dc-ac stages of power conversion can no longer be identified separately. In this configuration, the power balancing capacitor needs to be connected at the input terminals of the converter as no dc-link is available. As the capacitor experiences an ac voltage, the capacitor can be easily implemented by a small non-polarized capacitor and the volume and the lifetime issues of the large electrolytic capacitors can be avoided. The obvious advantage is that the lifetime of the inverter can be significantly extended [26].

2) DC-AC-DC-AC topologies: Some topologies of inverters may require a high boosting ratio for the voltage. These inverters may consist of a high frequency dc-ac-dc converter to obtain a controlled dc voltage from a variable dc voltage and a high frequency or line frequency inverter to generate the required ac output waveforms. A number of topologies have been studied and they can be classified into two categories depending on the intermediate dc-link.

    a) Dc-link between two stages: A conventional topology consisting of an intermediate dc-link is shown in Figure 2.6. The first inverter is responsible for the boosting and control of the dc-link voltage. It also has a high frequency step-up transformer, a rectifier and a dc filter. However, both the inverter stages are operated at high switching frequency, thus leading to higher losses and cost.

    b) Pseudo dc-link between two stages: Figure 2.11 represents a multi stage boost inverter which has a PWM dc pulse train implemented in the “pseudo dc-link”. The pulse train consists of multiple pluses whose widths distribute in a sinusoidal or semi-sinusoidal way repeating in half of an ac output period. The advantage that this topology has over the former is that there are no dc filter components required. The last stage implements an inverter switching at line frequency to convert the train of dc pulses to required ac output waveform. A low pass filter may be needed at the output to ensure that the total harmonic distortion (THD) is within acceptable limits.

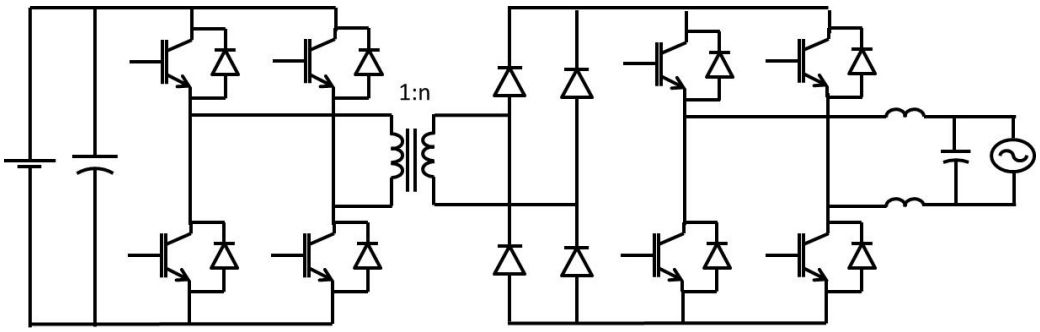


Figure 2.11 Multiple-stage boost inverter with pseudo dc-link

3) DC-AC-AC topologies: For stand-alone or autonomous systems, a bidirectional power flow is required in inverter control. In this case, provisions must be provided for the power to flow from the output side to the input side [25]. For these applications, a bidirectional ac-ac converter is used in the second stage without an intermediate dc-link. This is done to eliminate the bulky intermediate dc-link filter components as seen in most of the multi stage boost inverters. The change in voltage level and isolation is provided by using a high frequency transformer.

Review of multiple-stage topologies shows that it is desirable to use a high frequency transformer in the first stage so as to increase the boosting ratio and provide the required electrical isolation and a line-frequency inverter in the last stage to reduce total switching losses. However, a multiple-stage inverter has two or more stages of power conversion to achieve a wide input voltage range and a large power capacity as compared to a single-stage inverter at the cost of additional power components and losses [25].

In order to achieve good system performance, at least four issues must be considered in the micro inverter design [26].

1. Power Density: The power density is a sole indicator of the compactness of a micro inverter. One of the highest power densities achieved to date in the prototype design is $0.6 W/cm^3$ for a 110-W inverter. The goal for the next generation micro inverters aims at around $1 W/cm^3$.

2. Efficiency: A high efficiency is a must in obtaining a compact micro inverter design. However, compared with large converters, micro inverters have smaller power ratings and tend to have lower efficiencies. The highest reported micro inverter efficiency seen, for an isolated design, is 94% achieved by NKF OK4-100 at 40% of the maximum input power. A "future" target of 95% was set in 1998 to further decrease the temperature stress and increase the lifetime of the systems. It is not known if this has been achieved amongst the commercial micro inverters with isolated designs and less than 500-W power rating although larger PV inverters have achieved efficiencies higher than 98%.

3. Reliability: Because micro inverters are mounted on the PV module, it is important that the lifetime of the micro inverter is comparable to that of the PV module, which lasts more than 20 years.

4. Balance of System Cost: Balance of system (BOS) is defined as the parts of the PV system other than the PV array cost and will become increasingly important as the PV module costs drop. The major component of BOS cost in the micro inverter systems is the cost of the inverters due to the absence of the storage batteries.

Recently, most of research works on micro inverters still focus on low cost, high efficiency, and new topologies. Typically, the micro inverter is attached to a single PV panel, which requires that the micro inverter should have a lifespan matching the PV panel's one, namely 25 years. Therefore, achieving high reliability and long life span of the micro inverters is very crucial and should be one of the top priorities [21].

2.4 New Micro inverter using single switch inverter

All existing models of micro inverters use either single stage or multiple stages of power converters. They also use more components like a high frequency transformer, filters, diode rectifier and a bridge inverter. A new single switch inverter is developed which is capable of generating a pure sinusoidal waveform from a fixed DC input voltage. The single switch inverter is a modified version of the existing SEPIC DC-DC converter.

The use of the SEPIC based inverter as the solar inverter will eliminate the high frequency switching converter, high frequency transformer, filter and diode rectifier. This would reduce the size and cost of the micro-inverters.

CHAPTER 3. SOLAR PV MODULE

3.1 Introduction

While exhaustion of fossil fuels and green house effects have become a huge concern around the world, one of the most critical issues towards finding a solution for these problems is finding an alternate energy as a long-term solution. Green energy offers the promise of clean and abundant energy which can be harnessed from self-renewing sources such as solar energy, geothermal energy and wind energy [27]. Photovoltaic systems naturally harness the energy from the sun. Solar cells are capable of directly converting the incident solar irradiation into electricity. Photovoltaic (PV) power management concepts are essential to extract the maximum power from solar energy. PV energy systems are being extensively studied because of its benefits of environmental friendly and renewable characteristics [27].

Currently PV cells are one of the world's fastest growing technologies to generate electrical power. This technique is being used in more than 100 countries [28]. The system has to be designed to be reliable and efficient. The system mainly consists of PV modules, inverter and switching point for utility. Different types of PV cells will yield different energy output; meanwhile the controlling technique of inverter is very important. Inverter design should consider the size and capacity of the plant. On the other hand, choosing the right controlling technique is needed in order to achieve an efficient renewable energy system [28].

PV cell is very similar to that of a classical diode with a p-n junction. When the junction absorbs light, the incident energy is absorbed by the photons. The absorbed energy is transferred to the electron-proton system of the material, thus creating charge carriers that are separated at the junction. The charge carriers may be electron–ion pairs

in a liquid electrolyte or electron–hole pairs in a solid semiconducting material. The charge carriers in the junction region create a potential gradient, get accelerated under the electric field, and circulate as current through an external circuit. The square of the current multiplied by the resistance of the circuit is the power converted into electricity. The remaining power of the photon elevates the temperature of the cell and dissipates into the surroundings [29].

The solar cell described in the preceding subsection is the basic building block of the PV power system. Typically, it is a few square inches in size and produces about 1 W of power. To obtain high power, numerous such cells are connected in series and parallel circuits on a panel (module) area of several square feet. The solar array or panel is defined as a group of several modules electrically connected in a series–parallel combination to generate the required current and voltage [29].

Solar cells generate current in a large range independent from the load; thus, these cells are modeled as current sources [30]. They are designed with built-in -asymmetries to capture the photo-excited and released electrons and send them through an external circuit to build electric currents. The current generated from the cell is directly dependent on the illumination area and the probability that one photon can release one electron in the device. Under conditions where the illumination is zero, the solar cells behave like a diode. Therefore, their current in dark condition is a function of the cell's voltage. In illumination, however, based on the light intensity, the cell generates a current that affects the diode characteristics at the terminal. In open circuit, the voltage is created based on the recombination of carriers in solar cell. The open circuit voltage is defined as the voltage at which the short circuit current and the forward bias diffusion currents become equal with opposite polarities. Open circuit voltage has also been defined as the separation of Fermi energies at the equilibrium of electron-hole generation [30].

3.2 Modeling of PV cell

Generally, a photovoltaic cell models consists of a current source with a diode connected in anti-parallel. The output in parallel with them through a series resistor. In its

basic form, the current generated from the photocurrent source is directly conducted to the terminals. The diode connected across is used to model the I-V curve normally generated from the cells. The series resistance at the terminal of the cell is used to model the voltage drop. The parallel resistance is used to model the current leakage in the device proportional to the terminal voltage [30]. The Figure 3.1 shows the equivalent circuit of the solar cell with parallel and series resistors.

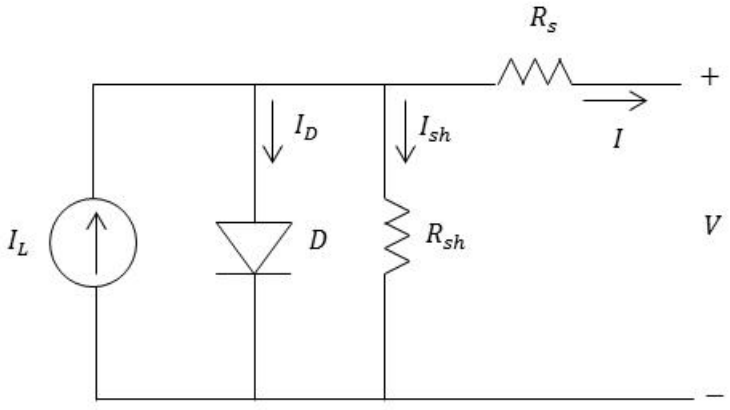


Figure 3.1 Equivalent circuit of solar cell

The I-V characteristics of solar cell with series and parallel resistors can be represented by

$$I = I_L - I_o \left\{ exp\left[\frac{e}{mkT}(V + IR_s)\right] - 1 \right\} - \frac{V+IR_s}{R_{sh}} \quad (3.1)$$

Where,

$I -$ PV array output current

$V -$ PV array output voltage

$I_o -$ Reverse saturation current of diode

$T -$ Cell temperature (K)

$e -$ Charge of an electron

$k -$ Boltzmann's constant

$m -$ Ideality factor

The photocurrent of the solar PV cell is defined by Equation (3.2)

$$I_L = [I_{SC} + k_i(T - 298)]\frac{G}{1000} \quad (3.2)$$

Where,

I_L – Photo current of PV cell

I_{SC} – Short circuit current of cell

k_i – Short circuit current temperature co-efficient

G – Solar radiation

The relation between the saturation current of the diode and temperature is given by Equation (3.3)

$$I_o(T) = I_o \left(\frac{T}{T_{nom}}\right)^3 \exp\left[\left(\frac{T}{T_{nom}} - 1\right)\frac{E_g}{NV_t}\right] \quad (3.3)$$

Where,

I_o – Reverse saturation current of diode

T_{nom} – Nominal temperature (K)

E_g – Band gap energy of the semiconductor

V_t – Thermal Voltage

The solar cell is modeled in Simulink. The P-V and I-V graphs are plotted for standard conditions i.e. radiance $G = 1000\, W/m^3$ and temperature $T = 25℃$ as shown in Figures 3.2 and 3.3.

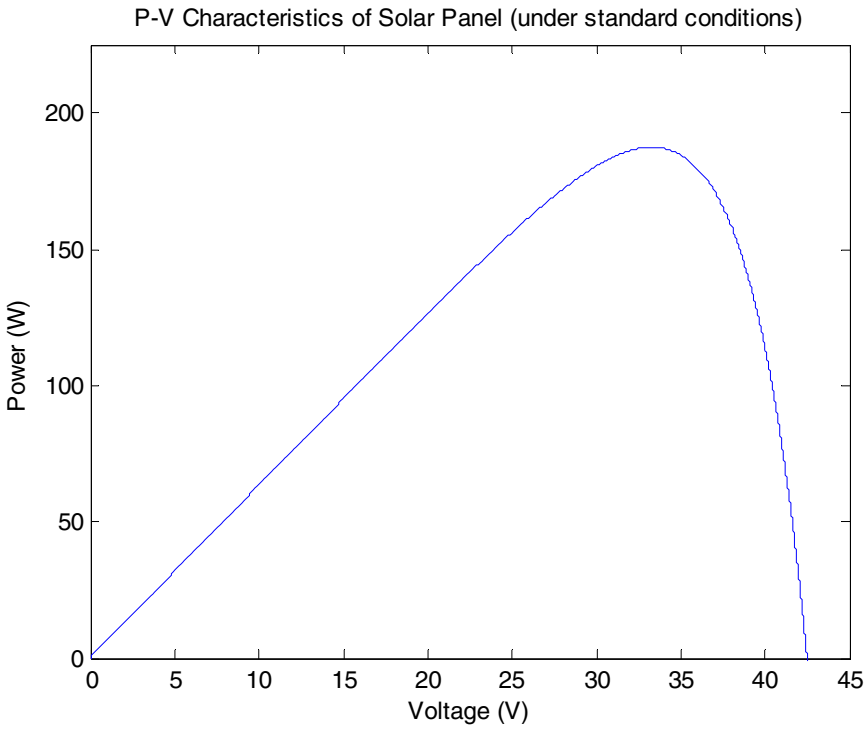


Figure 3.2 P-V characteristics of solar panel under standard conditions

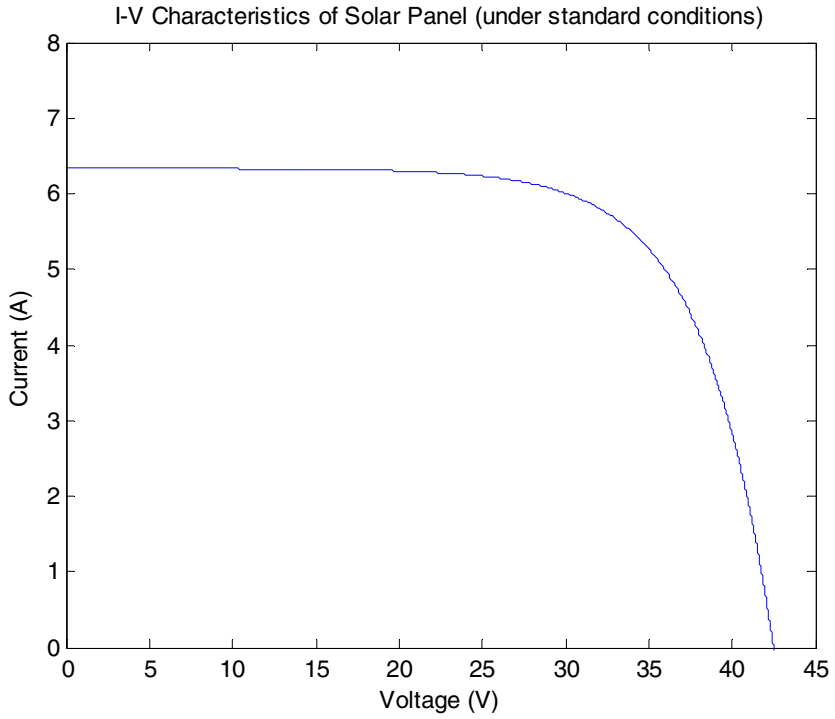


Figure 3.3 I-V characteristics of solar panel under standard conditions

From Equation 3.2, it can be seen that the photocurrent of the PV cell is dependent on the temperature and radiation. The P-V and I-V plots are studied for varying radiation and temperatures.

From Equation 3.3, the reverse saturation current of the diode varies as the cube of the temperature. Figures 3.4 and 3.5 show the P-V and I-V plots for variation in temperature while the radiation is constant. The temperature is varied from 0℃ to 70℃ while the radiation is assumed to be $1000\,W/m^3$.

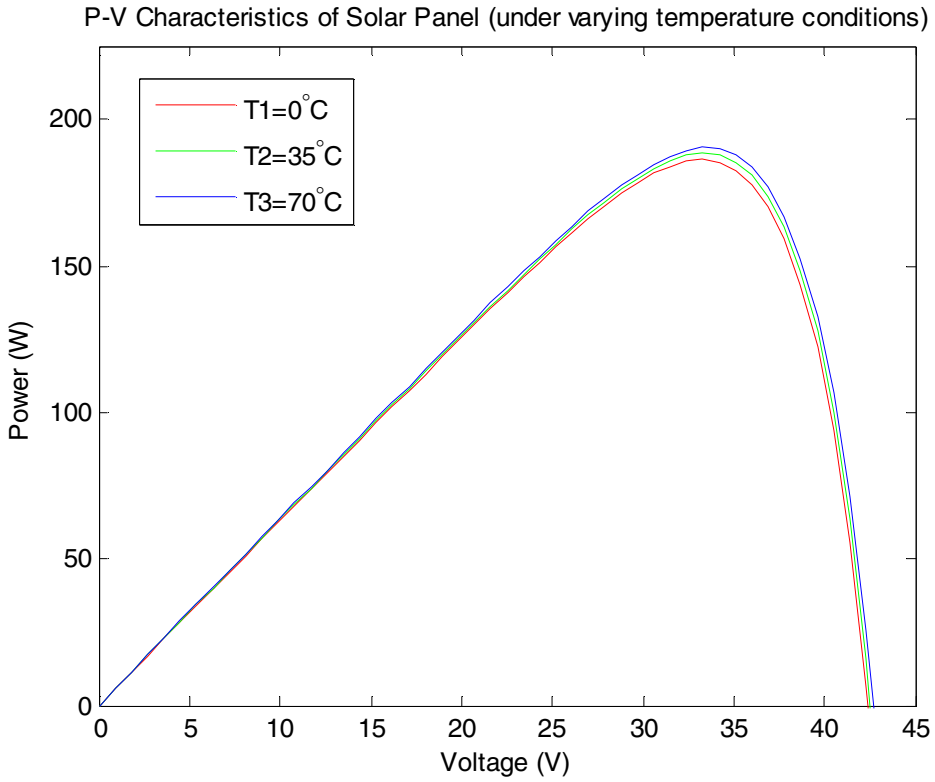


Figure 3.4 P-V characteristics of solar panel under varying temperature conditions

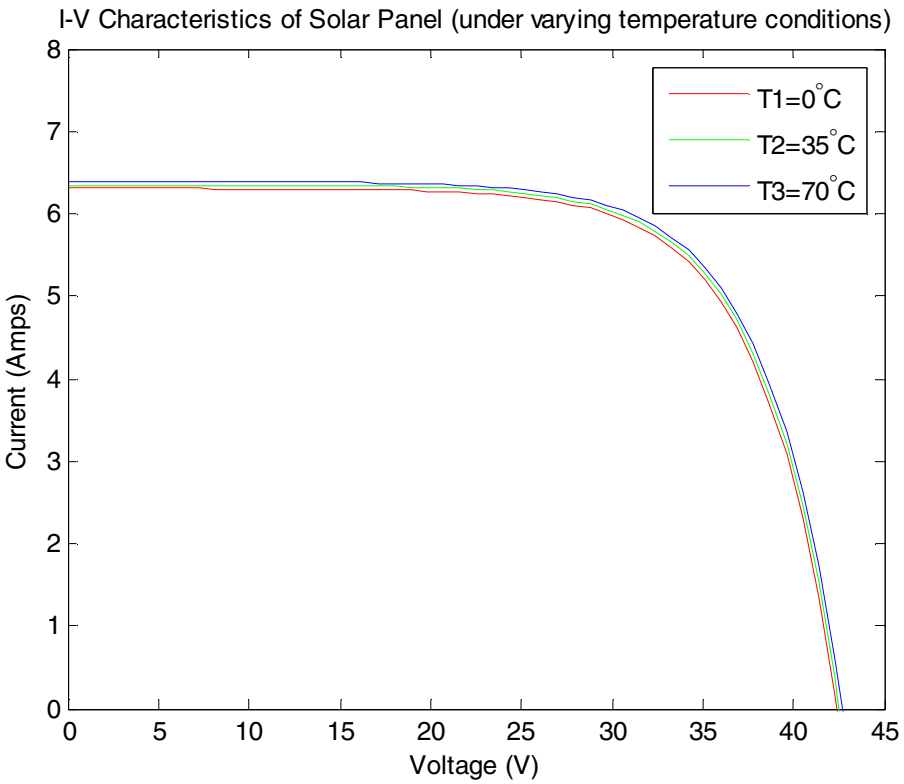


Figure 3.5 I-V characteristics of solar panel under varying temperature conditions

In general, when the temperature of the cell increases, for a given radiation, the open circuit voltage, V_{oc} drops slightly while the short circuit current, I_{sc} increases. This is validated by figures 3.4 and 3.5.

From Equation 3.2, the photocurrent is dependent directly on the solar radiation. Figures 3.6 and 3.7 show the P-V and I-V plots for variation in radiation while the temperature is constant. The radiation is varied from $600\,W/m^3$ to $1000\,W/m^3$ while the temperature is assumed to be $25℃$.

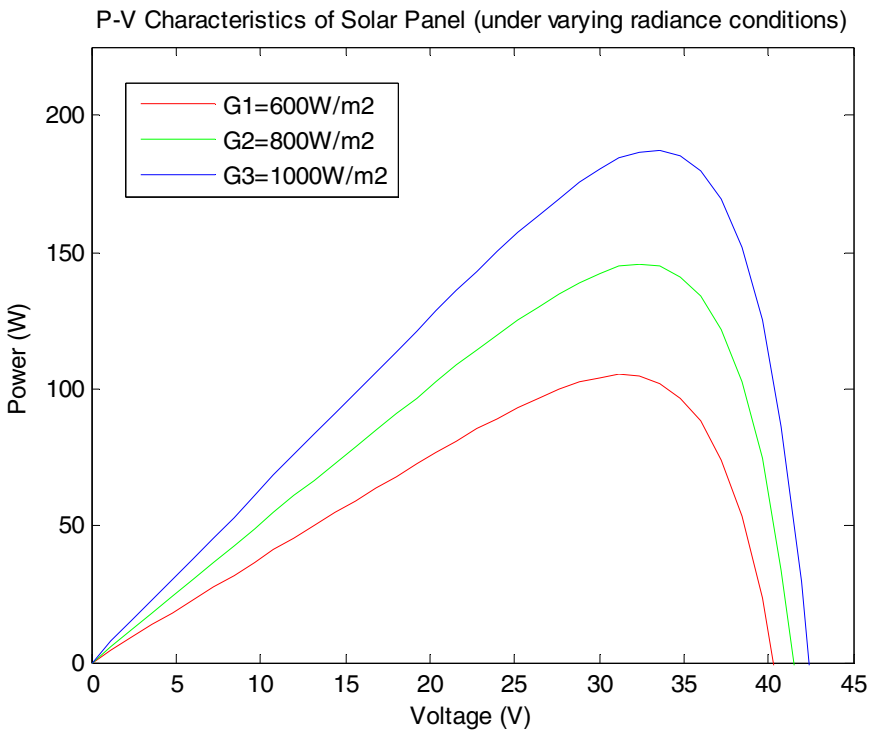


Figure 3.6 P-V characteristics of solar panel under varying radiance conditions

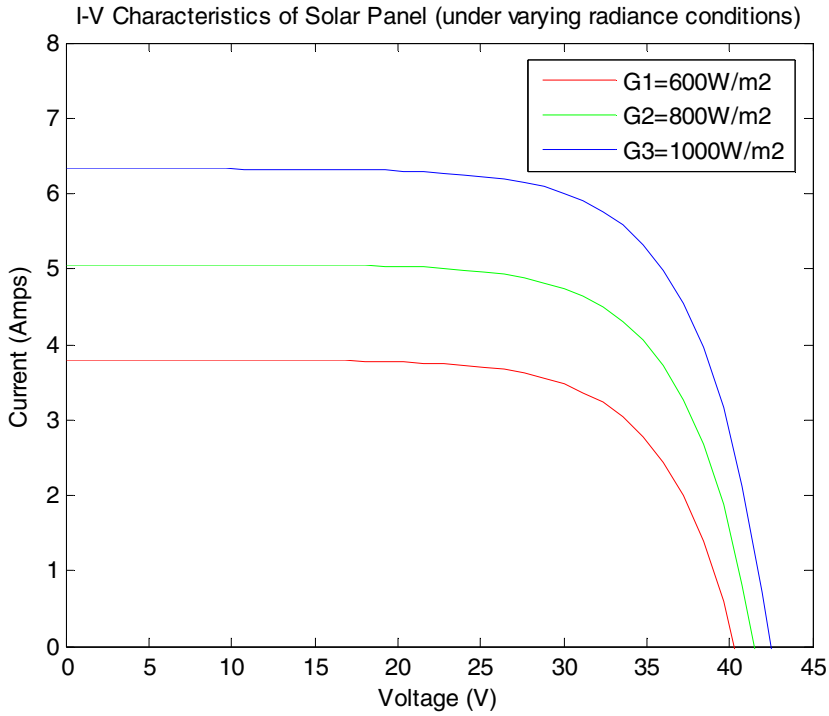


Figure 3.7 I-V characteristics of solar panel under varying radiance conditions

It can be seen that when the radiation increases, the open circuit voltage, V_{oc} and the short circuit current, I_{sc} increases. The change in P-V and I-V curves is more prominent for change in radiation.

3.3 Methods of MPPT

The PV generation systems have two major problems: the conversion efficiency of electric power generation is very low (9-17%), especially under low radiation conditions and the amount of electric power generated by solar arrays changes continuously with weather conditions [31].

Moreover, the solar cell I-V characteristic is nonlinear and varies with radiation and temperature. In general, there is a unique point on the I-V or P-V curve, called the Maximum Power Point (MPP), at which the entire PV system (array, converter, etc…) operates with maximum efficiency and produces its maximum output power. The location of the MPP is not known, but can be located, either through calculation models or by search algorithms. Therefore Maximum Power Point Tracking (MPPT) techniques are needed to maintain the PV array's operating point at its MPP [31].

A typical solar panel converts only 30 to 40 percent of the incident solar irradiation into electrical energy. Maximum power point tracking technique is used to improve the efficiency of the solar panel [32]. According to Maximum Power Transfer theorem, the power output of a circuit is maximum when the thevenin impedance of the circuit (source impedance) matches with the load impedance. Hence, the problem of tracking the maximum power point reduces to an impedance matching problem.

There are a number of methods used for MPPT. Depending on the time taken to track the MPP and the complexity of the algorithm, any one of the algorithms can be selected. Some of the techniques used to track the maximum power point are:

1. Fractional Open circuit voltage: This method is based on the fact that the voltage at MPP, V_{MPP} and the open circuit voltage, V_{OC} of the PV array are almost

linearly dependent on each other, under varying conditions of radiance and temperature. The relation between the two voltages is given by Equation (2.4).

$$V_{MPP} = k_1 V_{OC} \tag{2.4}$$

Where k_1 is a constant of proportionality. Since k is dependent on the characterstics of the PV array being used, it is usually computed by empirically determining V_{MPP} and V_{OC} for the specific PV array at different radiance and temperature levels. The factor k is found to be between 0.371 and 0.78 [32]. If the value of k_1 is determined, the V_{MPP} can be calculated from periodical measurement of V_{OC}. This can be done by switching the power converter off momentarily. However this leads to temporary loss of power.

2. Fractional Short circuit current: This method is based on the fact that under varying atmospheric conditions, I_{MPP} is approximately linear to the short circuit current, I_{SC} of the PV array.

$$I_{MPP} = k_2 I_{SC} \tag{2.5}$$

Where k_2 is a constant of proportionality. Similar to the fractional open circuit voltage method, the constant k_2 can be determined from the PV array that is being used. The value of constant k_2 is found to lie between 0.78 and 0.92 [32]. The measurement of I_{SC} needs an additional switch in the circuit which would short the PV array periodically. A current sensor is used to measure the current.

3. Incremental Conductance: This method uses both the output voltage and current of the PV array. From the P-V plot of a PV array, it can be observed that at the MPP, the slope of the curve is zero.

$$\left(\frac{dP}{dV}\right)_{MPP} = \frac{d}{dV}(VI) \tag{2.6}$$

$$0 = I + V\frac{dI}{dV_{MPP}} \tag{2.7}$$

$$\frac{dI}{dV_{MPP}} = -\frac{I}{V} \tag{2.8}$$

The right hand side of Equation 2.8 is the instantaneous conductance while the left hand side is the incremental conductance. When the optimum operating point in the P-V plane is to the right of the MPP, we have $\frac{dI}{dV_{MPP}} + \frac{I}{V} < 0$, where as when optimum operating point is to the left of the MPP, we have $\frac{dI}{dV_{MPP}} + \frac{I}{V} > 0$. Therefore, the sign of the term $\frac{dI}{dV_{MPP}} + \frac{I}{V}$ indicates the correct direction of perturbation leading to the MPP [31]. Once the MPP is reached, the perturbations are stopped till any change in *I* is observed to maintain the operation of the PV array at that point.

4. Perturb and Observe (P&O): It is one of the simplest methods. In this method, the power of the PV array is measured and compared with the values at the previous instant. Depending on the sign of change in power, either the voltage or current of the PV array is increased or decreased. If the change in power is positive, the voltage/current is increased while if the change in power is negative, the voltage/current is reduced. Eventually, the algorithm reaches the MPP.

5. Fuzzy logic: Microcontrollers have made using fuzzy logic control popular for MPPT over last decade. Fuzzy logic controllers have the advantages of working with imprecise inputs, not needing an accurate mathematical model, and handling nonlinearity [32].

6. Neural networks: This is another technique that has been developed to implement MPPT using microcontrollers. Neural networks commonly have three layers: input, hidden, and output layers. The number of nodes in each layer varies and is user-dependent. In this technique, the PV array parameters like V_{OC}, I_{SC} , atmospheric data like the amount of radiance, temperature or a combination of these parameters can be the input variables. The output signal could be one or more signals like the duty cycle which is used to drive the power converter so that the PV array operates at or close to the MPP [32].

3.4 Perturb & Observe (P&O)

The P&O method or hill climbing method operates by periodically perturbing i.e. incrementing or decrementing the array terminal voltage or current and comparing the PV output power with that of the previous perturbation cycle [31]. If a change in the operating voltage leads to increase in the power (i.e. $\frac{dP}{dV} > 0$), then the control algorithm moves the operating point of the PV array in the same direction, or else the operating point is moved in the opposite direction.

Figure 3.8 shows the plot of the output power of the array versus the array voltage at a given radiation. Consider two operating points A and B. As seen in the figure below, A is on the left side of MPP. The MPP can be reached by positive perturbation of voltage i.e. increasing the array voltage. While B is on the right side of MPP, any increase in the array voltage will reduce the power. Thus, the MPP can be reached by negative perturbation i.e. decreasing the array voltage.

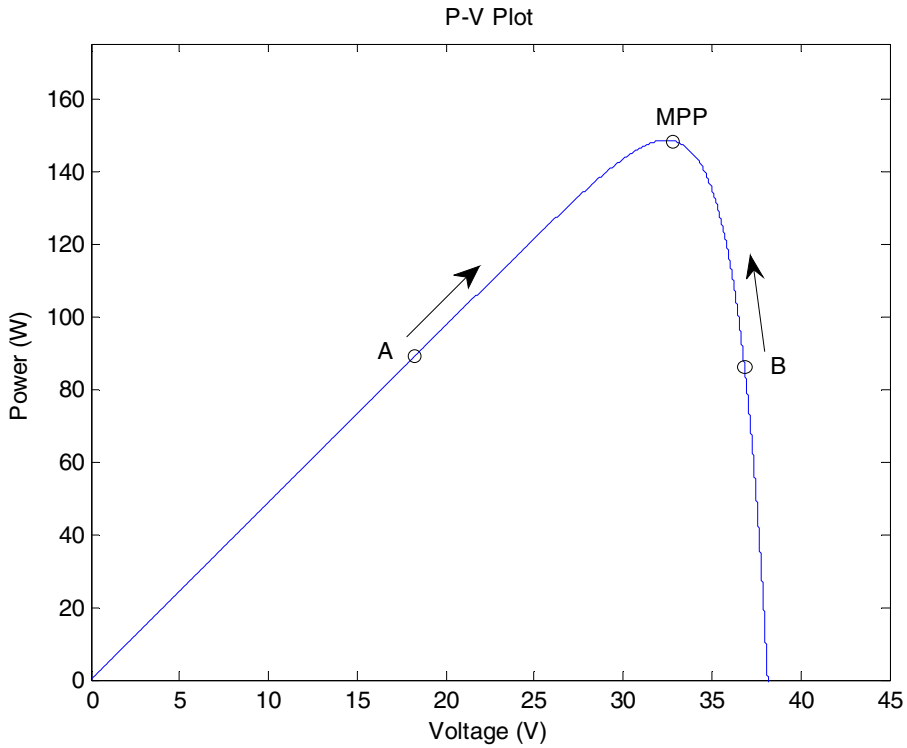


Figure 3.8 P-V characteristic of solar cell

The flowchart of the P&O algorithm is shown in Figure 3.9

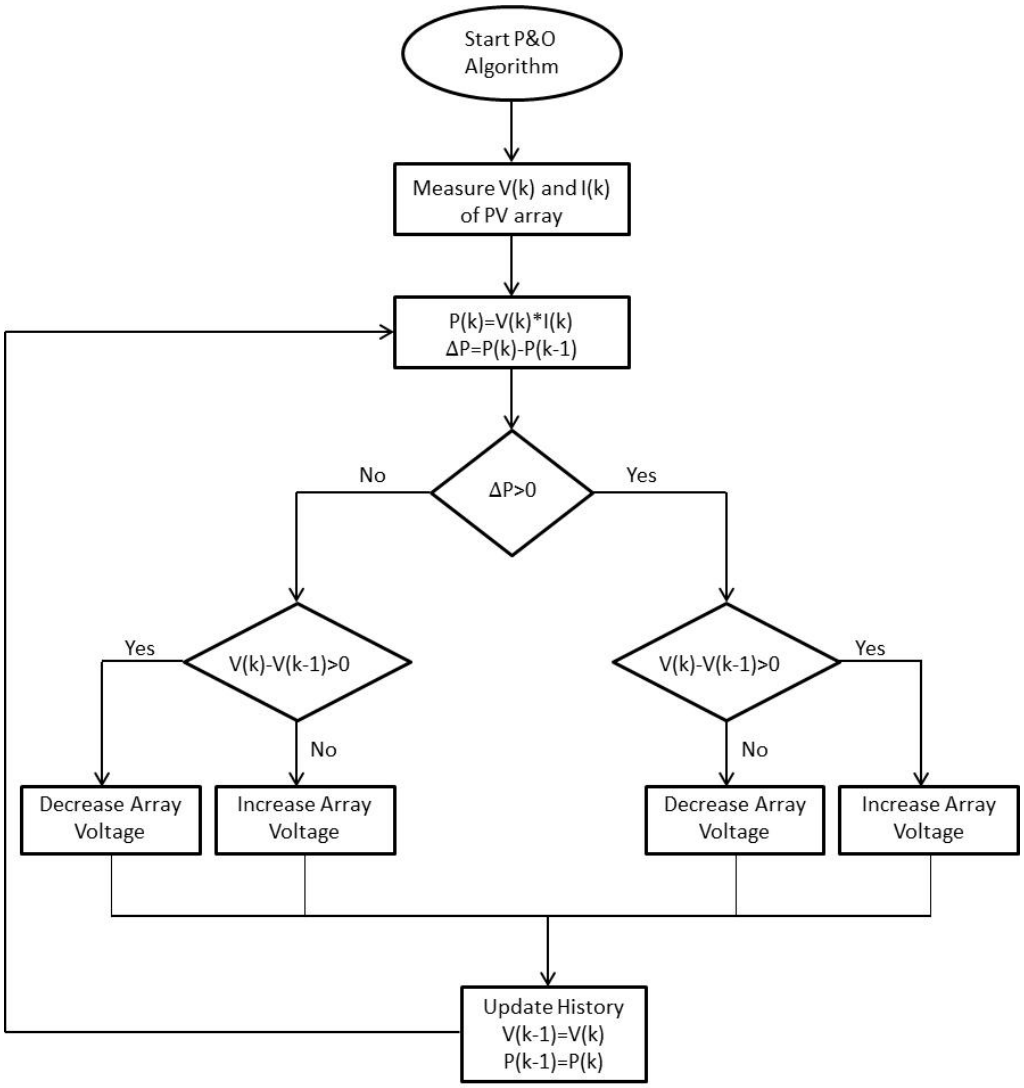


Figure 3.9 Flowchart for Perturb & Observe algorithm

This algorithm has some advantages. In this method, only one sensor is used i.e. the voltage sensor to sense the PV array voltage and so the cost of implementation is less. The complexity of this algorithm is less but when MP is reached, it doesn't stop at the MPP and swings around that point creating perturbations in both the directions [32]. In this case, the step-size of array voltage plays a crucial role. If the step size is large, then the MPP might not be reached, while if the step size is too small, it would take longer time to track the MPP. When the algorithm has reached close to the MPP, an appropriate

error limit or a wait function can be used [32]. Thus, a trade off needs to be made between the time taken to reach MPP and the accuracy with which the MPP needs to be identified. Also, under conditions for varying radiation, the MPP also moves to the right side of the curve. The algorithm would consider this as a change due to the perturbation and would reverse the direction of perturbation in the next iteration. Thus, moving away from the MPP of the array.

CHAPTER 4. SINGLE SWITCH INVERTER

4.1 Design and Operation

The single switch inverter is derived by modifying the SEPIC converter to function as an inverter. Typically, the SEPIC converter consists of an active power switch, a diode, two inductors and two capacitors. Thus, it is a fourth order system. In the modified SEPIC converter, the diode is replaced by a set of polarity reversing switch component. This component consists of two reverse connected transistors to be synchronized to the polarity of the desired waveform. This circuit is capable of producing a pure sinusoidal waveform, when a DC input is given to the circuit.

A schematic diagram of the new inverter has been shown in Figure 4.1. It consists of a switch Q which is operated at high frequency and switches T_1 and T_2 which are operated to generate positive and negative peaks of output voltage. When the switch Q is on, the inductor L_1 is charged from the input source and inductor L_2 takes energy from the capacitor C_1. The output capacitor C_2 provides the load current. When the switch Q is on, both inductors are disconnected from the load. When the switch Q is turned off, the inductor L_1 charges the capacitor C_1 and also provides current to the load. The inductor L_2 is also connected to the load during this time.

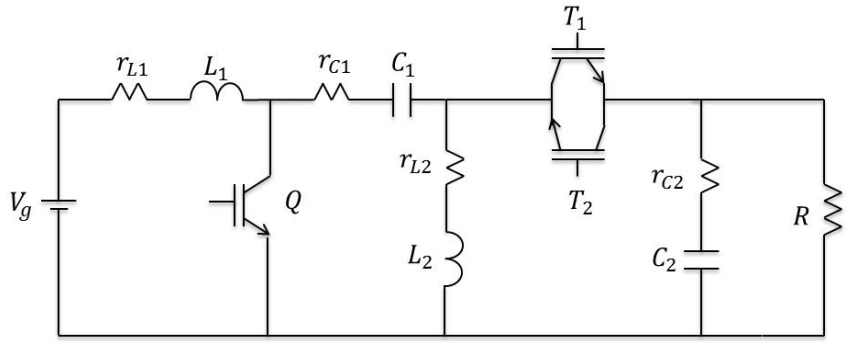


Figure 4.1 Schematic Diagram of SEPIC based Inverter

Modes of operation are generated when the status of switches change. When the switch Q is on, the input voltage is applied across L_1 and causes a linear increase of current to charge the inductor. The charged capacitor C_2 discharges through the inductor L_2. In this mode of operation, the transistor T_1 does not conduct. Even though the gate receives the turn-on command, the transistor collector is not forward biased to conduct current. When the switch Q is off, the input voltage charges the capacitor C_1 while maintaining the current through the inductor L_1. The sum of currents through the inductors L_1 and L_2 form the output current that flows through the load to produce positive voltage in the output.

In negative peak voltage, the same procedure occurs, but to reverse the load current direction, synchronizing switch T_2 is turned on. This will introduce a transition mode to the system operation. When the switch Q is on, the input voltage is applied across L_1 and causes a linear increase of current to charge the inductor. The charged capacitor C_2 discharges through the inductor L_2. In this mode of operation, the transistor T_2 does not conduct. Even though the gate receives the turn-on command, the transistor collector is not forward biased to conduct current. When the switch Q is off, the input voltage charges the capacitor C_1 while maintaining the current through the inductor L_1. The difference of currents through the inductors L_1 and L_2 form the output current that flows through the load to produce negative voltage in the output.

In Continuous Conduction Mode (CCM), the input and output voltages of the converter are related as follows:

$$\frac{Vout}{Vin} = \pm\frac{D}{1-D} \ , \tag{4.1}$$

where $0 < D < 1$ is the converter's ideal duty cycle. The positive and negative signs are used for the positive peak and negative peak voltages respectively. In each half cycle, for values of D less than 0.5, the converter ideally operates in buck mode, and for values of D larger than 0.5 the converter ideally operates in boost mode.

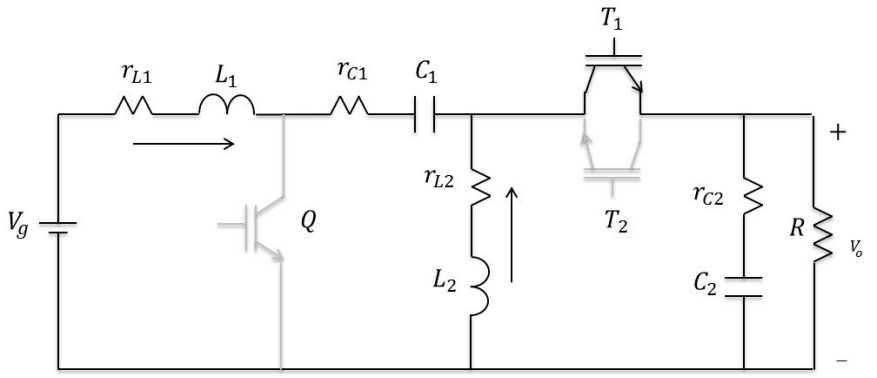
4.2 Modeling of Inverter

4.2.1 State Space Averaging

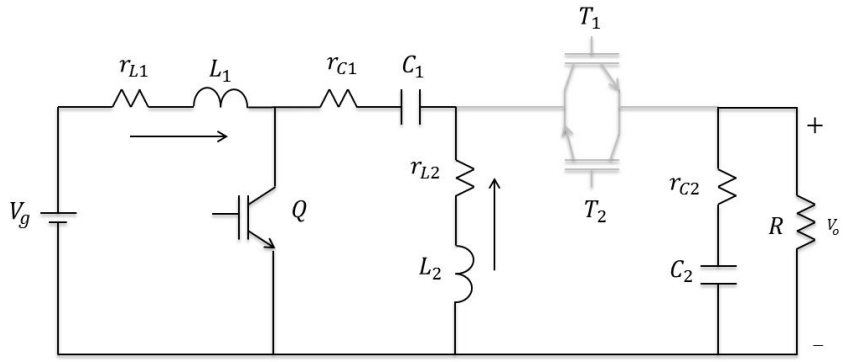
State space averaging is a dynamic modeling technique used for mathematical representation of converters. State space averaging technique is used for better understanding of different modes of operation. In this technique, the state space representation of each mode of operation is obtained, and the overall system is represented as an averaged system over a cycle. Since this inverter has a positive and a negative mode of operation, the model will be provided in these conditions.

When the inverter operates in mode I and mode II, positive cycle of output voltage is obtained. When it operates in mode III and mode IV, negative cycle of output voltage is generated. Therefore, two sets of equations can be written for this circuit, which includes the internal resistances of the inductors and capacitors as r_{L1}, r_{L2}, r_{C1} and r_{C2}.

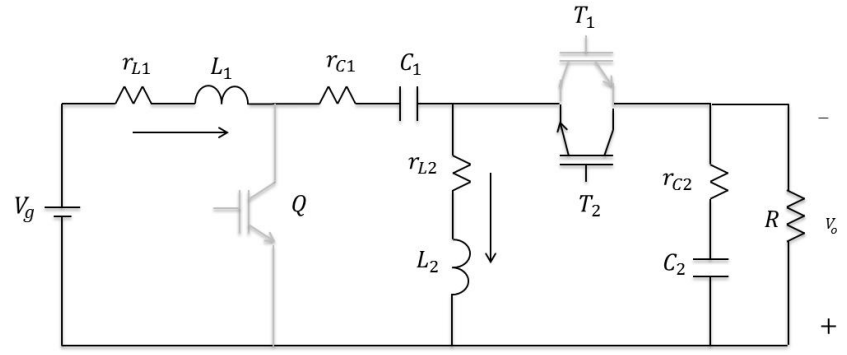
The four modes of operation of the inverter circuit are shown in Figure 4.2.



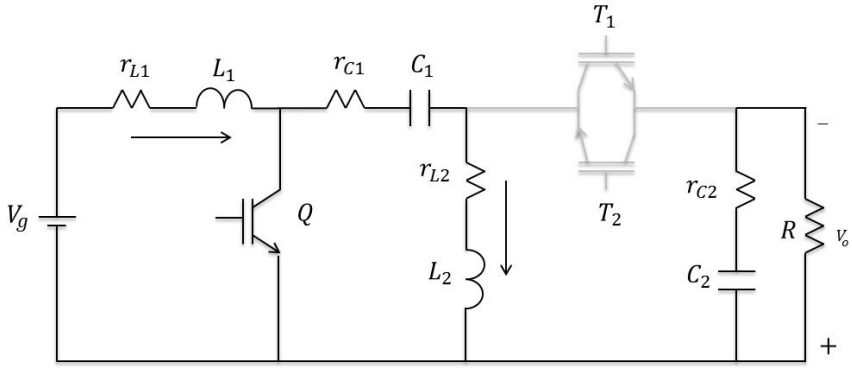
A) Mode I: Positive Peak, Q and T_1 are synchronized, Q: Off, T_1: On



B) Mode II: Positive Peak, Q and T_1 are synchronized, Q: On, T_1: Off



C) Mode III: Negative Peak, Q and T_2 are synchronized, Q: Off, T_2: On



D) Mode IV: Negative Peak, Q and T_2 are synchronized, Q: On , T_2: Off

Figure 4.2. Modes of operation and transition from positive to negative peak voltage.

Figure 4.2.A shows the rise in current through the inductor L_1 and charging of capacitor C_1 by the input voltage source. The current through the inductors flow to the output resistance R. Figure 4.2.B shows the rise in current through the inductor L_1 and

discharge of capacitor C_1 through inductor L_2 and discharge of capacitor C_2 through the load resistance and positive output voltage generation. Figure 4.2.C shows the transition from positive peak to negative peak by switching the synchronizing transistor T_2 on. The current direction will change and the negative peak will be generated by circuit D. This mode of operation charges the inductor L_2 with reverse current and provides a path to build up negative cycle of output voltage.

A. Positive Peak Voltage Generation

I. Mode I

In this mode, the switch Q is off and T_1 is on for duty cycle $1 - d^+$. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o. The equations describing mode I are as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = -\frac{\left(r_{L1}+r_{C1}+\frac{R*r_{C2}}{R+r_{C2}}\right)}{L_1} i_{L1} - \frac{\frac{R*r_{C2}}{R+r_{C2}}}{L_1} i_{L2} - \frac{1}{L_1} v_{C1} + \frac{\frac{R}{R+r_{C2}}}{L_1} v_{C2} + \frac{Vi}{L_1} \\ \frac{di_{L2}}{dt} = \frac{-\frac{R*r_{C2}}{(R+r_{C2})}}{L_2} i_{L1} - \frac{r_{L2}+\frac{R*r_{C2}}{R+r_{C2}}}{L_2} i_{L2} - \frac{\frac{R}{R+r_{C2}}}{L_2} v_{C2} \\ \frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} \\ \frac{dv_{C2}}{dt} = \frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L1} + \frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L2} - \frac{\frac{1}{(R+r_{C2})}}{C_2} v_{C2} \\ V_o = \frac{R*r_{C2}}{R+r_{C2}} i_{L1} + \frac{R*r_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} v_{C2} \end{cases} \quad (4.2)$$

II. Mode II

In this mode, the switch Q is on and T_1 is off for duty cycle d^+. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o. The equations describing mode II are as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{V_i}{L_1} - \frac{r_{L1}}{L_1} i_{L1} \\ \frac{di_{L2}}{dt} = -\frac{(r_{L2}+r_{C1})}{L_2} i_{L1} + \frac{1}{L_2} v_{C1} \\ \frac{dv_{c1}}{dt} = -\frac{1}{C_1} i_{L2} \\ \frac{dv_{c2}}{dt} = -\frac{1}{C_2(R+r_{C2})} v_{c2} \\ V_o = \frac{R}{R+r_{C2}} v_{C2} \end{cases} \tag{4.3}$$

Considering x= [i_{L1}, i_{L2}, v_{C1}, v_{C2}], the averaged state space model of positive peak voltage can be obtained as:

$$\begin{cases} \dot{x} = A^+_{avg} x + B^+_{avg} u \\ V_o = C^+_{avg} x \end{cases} \tag{4.4}$$

The positive peak averaged model parameters can be obtained as:

$$A^+_{avg} = \begin{bmatrix} \frac{-r_{L1}(R+r_{C2}) + (D-1)(r_{C1}(R+r_{C2}) + Rr_{C2})}{L_1(R+r_{C2})} & \frac{(D-1)Rr_{C2}}{L_1(R+r_{C2})} & \frac{D-1}{L_1} & \frac{(D-1)R}{L_1(R+r_{C2})} \\ \frac{(D-1)Rr_{C2}}{L_2(R+r_{C2})} & \frac{(D-1)Rr_{C2} - (R+r_{C2})(Dr_{C1}+r_{L2})}{L_2(R+r_{C2})} & \frac{D}{L_2} & \frac{(D-1)R}{L_2(R+r_{C2})} \\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ \frac{(1-D)R}{C_2(R+r_{C2})} & \frac{(1-D)R}{C_2(R+r_{C2})} & 0 & -\frac{1}{C_2(R+r_{C2})} \end{bmatrix}$$

$$B^+_{avg} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

$$C^+_{avg} = \begin{bmatrix} \frac{(1-D)Rr_{C2}}{C_2(R+r_{C2})} & \frac{(1-D)Rr_{C2}}{C_2(R+r_{C2})} & 0 & \frac{R}{R+r_{C2}} \end{bmatrix}$$

B. Negative Peak Voltage Generation

III. Mode III

In this mode, the switch Q is off and T_2 is on for duty cycle $1 - d^-$. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o. The equations describing mode III are as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = -\frac{\left(r_{L1}+r_{C1}+\frac{R*r_{C2}}{R+r_{C2}}\right)}{L_1} i_{L1} + \frac{\frac{R*r_{C2}}{R+r_{C2}}}{L_1} i_{L2} - \frac{1}{L_1} v_{C1} + \frac{\frac{R}{R+r_{C2}}}{L_1} v_{C2} + \frac{Vi}{L_1} \\ \frac{di_{L2}}{dt} = \frac{\frac{R*r_{C2}}{(R+r_{C2})}}{L_2} i_{L1} - \frac{r_{L2}+\frac{R*r_{C2}}{R+r_{C2}}}{L_2} i_{L2} - \frac{\frac{R}{R+r_{C2}}}{L_2} v_{C2} \\ \frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} \\ \frac{dv_{C2}}{dt} = -\frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L1} + \frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L2} - \frac{1}{C_2(R+r_{C2})} v_{C2} \\ V_o = -\frac{R*r_{C2}}{R+r_{C2}} i_{L1} + \frac{R*r_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} v_{C2} \end{cases} \quad (4.5)$$

IV. Mode IV

In this mode, the switch Q is on and T_2 is off for duty cycle d^-. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o. The equations describing mode IV are as follows:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{V_i}{L_1} - \frac{r_{L1}}{L_1} i_{L1} \\ \frac{di_{L2}}{dt} = -\frac{(r_{L2}+r_{C1})}{L_2} i_{L2} - \frac{1}{L_2} v_{C1} \\ \frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L2} \\ \frac{dv_{C2}}{dt} = -\frac{1}{C_2(R+r_{C2})} v_{C2} \\ V_o = \frac{R}{R+r_{C2}} v_{C2} \end{cases} \quad (4.6)$$

Considering x= [i_{L1}, i_{L2}, v_{C1}, v_{C2}], the averaged state space model of negative peak voltage can be obtained as:

$$\begin{cases} \dot{x} = A_{avg}^{-} x + B_{avg}^{-} u \\ V_o = C_{avg}^{-} x \end{cases} \quad (4.7)$$

The negative peak averaged model parameters can be obtained as:

$$A_{avg}^{-} = \begin{bmatrix} \frac{-r_{L1}(R+r_{C2})+(D-1)(r_{C1}(R+r_{C2})+Rr_{C2})}{L_1(R+r_{C2})} & \frac{(1-D)Rr_{C2}}{L_1(R+r_{C2})} & \frac{D-1}{L_1} & \frac{(1-D)R}{L_1(R+r_{C2})} \\ \frac{(1-D)Rr_{C2}}{L_2(R+r_{C2})} & \frac{(D-1)Rr_{C2}-(R+r_{C2})(Dr_{C1}+r_{L2})}{L_2(R+r_{C2})} & -\frac{D}{L_2} & \frac{(D-1)R}{L_2(R+r_{C2})} \\ \frac{1-D}{C_1} & \frac{D}{C_1} & 0 & 0 \\ \frac{(D-1)R}{C_2(R+r_{C2})} & \frac{(1-D)R}{C_2(R+r_{C2})} & 0 & -\frac{1}{C_2(R+r_{C2})} \end{bmatrix}$$

$$B_{avg}^{-} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

$$C_{avg}^{-} = \begin{bmatrix} \frac{(D-1)Rr_{C2}}{(R+r_{C2})} & \frac{(1-D)Rr_{C2}}{(R+r_{C2})} & 0 & \frac{R}{R+r_{C2}} \end{bmatrix}$$

The inverter can also be modeled as a complete system where the different modes are averaged over one complete cycle. In this case, the load current is modelled as a current source in the modeling of the inverter as shown in Figure 4.3.

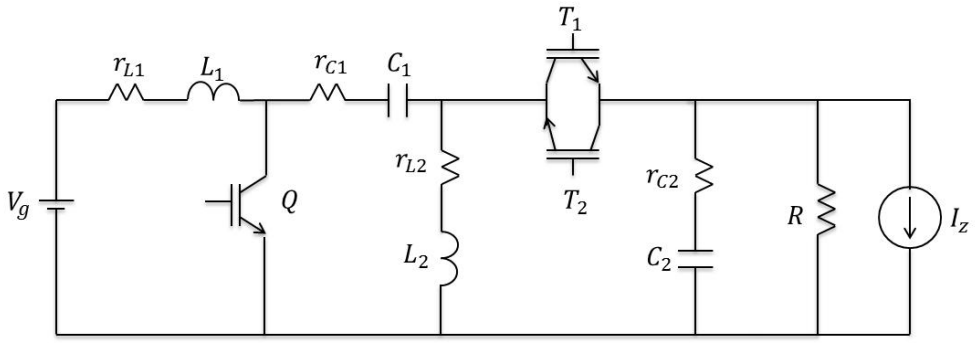
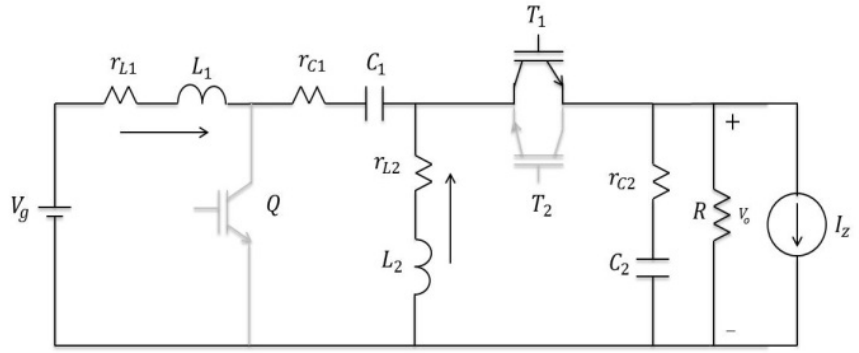
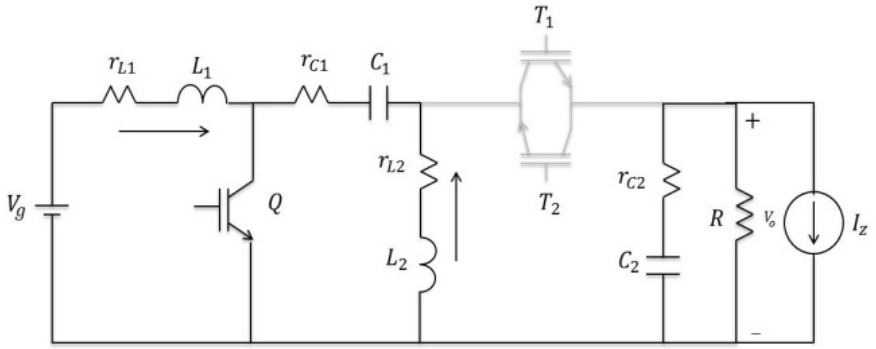


Figure 4.3 Schematic diagram of SEPIC based inverter with load current modeled as source

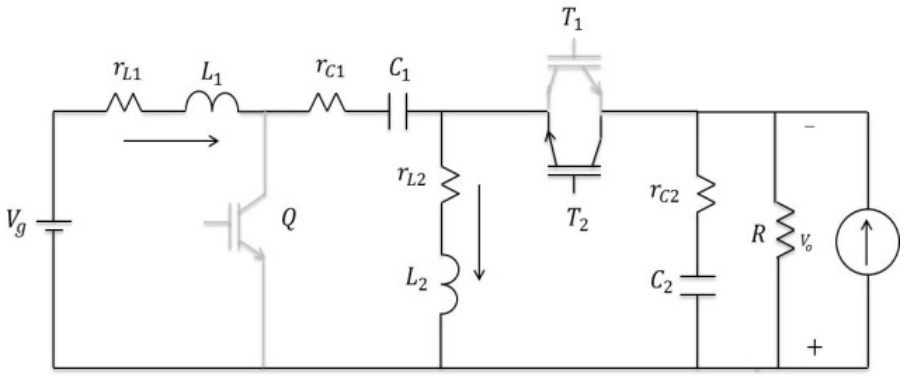
The four different modes of operation that are identified are depicted by the following figures.



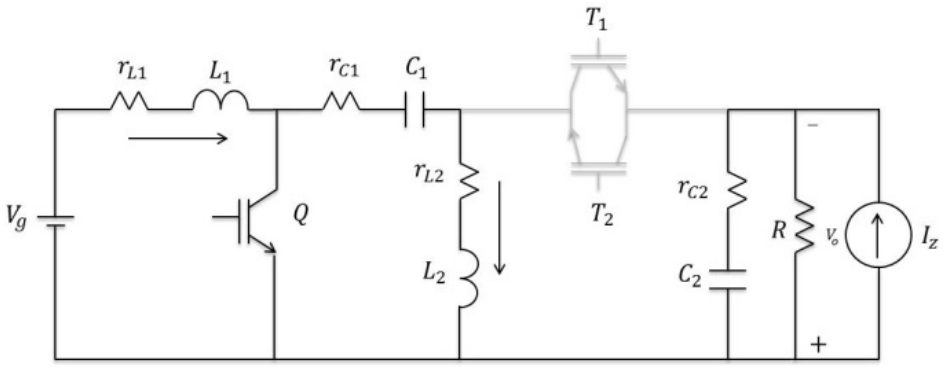
A) Mode I: Positive Peak, Q and T_1 are synchronized, Q: Off, T_1: On



B) Mode II: Positive Peak, Q and T_1 are synchronized, Q: On, T_1: Off



C) Mode III: Negative Peak, Q and T_2 are synchronized, Q: Off, T_2: On



D) Mode IV: Negative Peak, Q and T_2 are synchronized, Q: On , T_2: Off

Figure 4.4. Modes of operation and transition from positive to negative peak voltage.

I. Mode I

In this mode, the switch Q is off and T_1 is on for duty cycle $1 - d^+$. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o.

$$\begin{cases} \frac{di_{L1}}{dt} = -\frac{\left(r_{L1}+r_{C1}+\frac{Rr_{C2}}{R+r_{C2}}\right)}{L_1} i_{L1} - \frac{Rr_{C2}}{L_1(R+r_{C2})} i_{L2} - \frac{1}{L_1} v_{C1} - \frac{R}{L_1(R+r_{C2})} v_{C2} + \frac{1}{L_1} V_g + \frac{Rr_{C2}}{L_1(R+r_{C2})} I_z \\ \frac{di_{L2}}{dt} = -\frac{Rr_{C2}}{L_2(R+r_{C2})} i_{L1} - \frac{\left(r_{L2}+\frac{Rr_{C2}}{R+r_{C2}}\right)}{L_2} i_{L2} - \frac{R}{L_2(R+r_{C2})} v_{C2} + \frac{Rr_{C2}}{L_2(R+r_{C2})} I_z \\ \frac{dv_{C1}}{dt} = \frac{i_{L1}}{C_1} \\ \frac{dv_{C2}}{dt} = \frac{R}{C_2(R+r_{C2})} i_{L1} + \frac{R}{C_2(R+r_{C2})} i_{L2} - \frac{1}{C_2(R+r_{C2})} v_{C2} - \frac{R}{C_2(R+r_{C2})} I_z \\ V_o = \frac{Rr_{C2}}{R+r_{C2}} i_{L1} + \frac{Rr_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} v_{C2} - \frac{Rr_{C2}}{R+r_{C2}} I_z \end{cases} \quad (4.8)$$

II. Mode II

In this mode, the switch Q is on and T_1 is off for duty cycle d^+. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o.

$$\begin{cases} \dfrac{di_{L1}}{dt} = -\dfrac{r_{L1}}{L_1} i_{L1} + \dfrac{1}{L_1} V_g \\ \dfrac{di_{L2}}{dt} = -\dfrac{(r_{L2}+r_{C1})}{L_2} i_{L2} + \dfrac{1}{L_2} v_{C1} \\ \dfrac{dv_{C1}}{dt} = -\dfrac{i_{L2}}{C_1} \\ \dfrac{dv_{C2}}{dt} = -\dfrac{1}{C_2(R+r_{C2})} v_{C2} - \dfrac{R}{C_2(R+r_{C2})} I_z \\ V_o = \dfrac{R}{R+r_{C2}} v_{C2} - \dfrac{Rr_{C2}}{R+r_{C2}} I_z \end{cases} \tag{4.9}$$

III. Mode III

In this mode, the switch Q is off and T_2 is on for duty cycle $1 - d^-$. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o.

$$\begin{cases} \dfrac{di_{L1}}{dt} = -\dfrac{\left(r_{L1}+r_{C1}+\frac{Rr_{C2}}{R+r_{C2}}\right)}{L_1} i_{L1} + \dfrac{Rr_{C2}}{L_1(R+r_{C2})} i_{L2} - \dfrac{1}{L_1} v_{C1} + \dfrac{R}{L_1(R+r_{C2})} v_{C2} + \dfrac{1}{L_1} V_g - \dfrac{Rr_{C2}}{L_1(R+r_{C2})} I_z \\ \dfrac{di_{L2}}{dt} = \dfrac{Rr_{C2}}{L_2(R+r_{C2})} i_{L1} - \dfrac{\left(r_{L2}+\frac{Rr_{C2}}{R+r_{C2}}\right)}{L_2} i_{L2} - \dfrac{R}{L_2(R+r_{C2})} v_{C2} + \dfrac{Rr_{C2}}{L_2(R+r_{C2})} I_z \\ \dfrac{dv_{C1}}{dt} = \dfrac{i_{L1}}{C_1} \\ \dfrac{dv_{C2}}{dt} = -\dfrac{R}{C_2(R+r_{C2})} i_{L1} + \dfrac{R}{C_2(R+r_{C2})} i_{L2} - \dfrac{1}{C_2(R+r_{C2})} v_{C2} - \dfrac{R}{C_2(R+r_{C2})} I_z \\ V_o = -\dfrac{Rr_{C2}}{R+r_{C2}} i_{L1} + \dfrac{Rr_{C2}}{R+r_{C2}} i_{L2} + \dfrac{R}{R+r_{C2}} v_{C2} - \dfrac{Rr_{C2}}{R+r_{C2}} I_z \end{cases} \tag{4.10}$$

IV. Mode IV

In this mode, the switch Q is on and T_2 is off for duty cycle d^-. Each set of state space system consists of four equations representing the states i_{L1}, i_{L2}, v_{C1}, v_{C2} and one equation to represent the output voltage, V_o.

$$\begin{cases} \dfrac{di_{L1}}{dt} = -\dfrac{r_{L1}}{L_1} i_{L1} + \dfrac{1}{L_1} V_g \\ \dfrac{di_{L2}}{dt} = -\dfrac{(r_{L2}+r_{C1})}{L_2} i_{L2} - \dfrac{1}{L_2} v_{C1} \\ \dfrac{dv_{C1}}{dt} = \dfrac{i_{L2}}{C_1} \\ \dfrac{dv_{C2}}{dt} = -\dfrac{1}{C_2(R+r_{C2})} v_{C2} - \dfrac{R}{C_2(R+r_{C2})} I_z \\ V_o = \dfrac{R}{R+r_{C2}} v_{C2} - \dfrac{Rr_{C2}}{R+r_{C2}} I_z \end{cases} \tag{4.11}$$

The system is averaged over the full cycle. The averaged state space model of the inverter can be obtained as:

$$\begin{cases} \dot{x} = A_{avg}x + B_{avg}u \\ V_o = C_{avg}x + E_{avg}u \end{cases} \tag{4.12}$$

The state space matrices are averaged as:

$$A_{avg} = d_pA_1 + (1-d_p)A_2 + d_nA_3 + (1-d_n)A_4$$
$$B_{avg} = d_pB_1 + (1-d_p)B_2 + d_nB_3 + (1-d_n)B_4$$
$$C_{avg} = d_pC_1 + (1-d_p)C_2 + d_nC_3 + (1-d_n)C_4$$
$$E_{avg} = d_pE_1 + (1-d_p)E_2 + d_nE_3 + (1-d_n)E_4$$

Where subscripts 1-4 represent the four modes of operation.

The averaged state space matrices are given as:

$$\mathrm{A_{avg}} = \begin{bmatrix} \mathrm{A_{11}} & \frac{\mathrm{Rr_{C2}}(k_n(1-d_n)-k_p(1-d_p))}{\mathrm{L_1(R+r_{C2})}} & -\frac{(k_p(1-d_p)+k_n(1-d_n))}{\mathrm{L_1}} & \frac{\mathrm{R}(k_n(1-d_n)-k_p(1-d_p))}{\mathrm{L_1(R+r_{C2})}} \\ \frac{\mathrm{Rr_{C2}}(k_n(1-d_n)-k_p(1-d_p))}{\mathrm{L_2(R+r_{C2})}} & \mathrm{A_{22}} & \frac{k_pd_p-k_nd_n}{\mathrm{L_2}} & -\frac{\mathrm{R}(k_p(1-d_p)+k_n(1-d_n))}{\mathrm{L_2(R+r_{C2})}} \\ \frac{(k_p(1-d_p)+k_n(1-d_n))}{\mathrm{C_1}} & \frac{k_nd_n-k_pd_p}{\mathrm{C_1}} & 0 & 0 \\ \frac{\mathrm{R}(k_p(1-d_p)-k_n(1-d_n))}{\mathrm{C_2(R+r_{C2})}} & \frac{\mathrm{R}(k_p(1-d_p)+k_n(1-d_n))}{\mathrm{C_2(R+r_{C2})}} & 0 & \frac{-(k_p+k_n)}{\mathrm{C_2(R+r_{C2})}} \end{bmatrix}$$

$$\mathrm{B_{avg}} = \begin{bmatrix} \frac{(k_p+k_n)}{\mathrm{L_1}} & \frac{\mathrm{Rr_{C2}}(k_p(1-d_p)-k_n(1-d_n))}{\mathrm{L_1(R+r_{C2})}} \\ 0 & \frac{\mathrm{Rr_{C2}}(k_p(1-d_p)+k_n(1-d_n))}{\mathrm{L_1(R+r_{C2})}} \\ 0 & 0 \\ 0 & \frac{-\mathrm{R}(k_p+k_n)}{\mathrm{C_2(R+r_{C2})}} \end{bmatrix}$$

$$\mathrm{C_{avg}} = \begin{bmatrix} \frac{\mathrm{Rr_{C2}}(k_p(1-d_p)-k_n(1-d_n))}{\mathrm{R+r_{C2}}} & \frac{\mathrm{Rr_{C2}}(k_p(1-d_p)+k_n(1-d_n))}{\mathrm{R+r_{C2}}} & 0 & \frac{\mathrm{R}(k_p+k_n)}{\mathrm{R+r_{C2}}} \end{bmatrix}$$

$$\mathrm{E_{avg}} = \begin{bmatrix} 0 & -\frac{2\mathrm{Rr_{C2}}(k_p+k_n)}{\mathrm{R+r_{C2}}} \end{bmatrix}$$

4.2.2 Small Signal Modeling

Small signal analysis is a mathematical method for studying the dynamic response of the system when perturbed by a small disturbance. It is a technique of analyzing the behavior of a non-linear system with linear equations. The system is linearized around the DC operating point. The assumption made here is that the perturbation in the signal is small and is insufficient to cause any change in the operating point of the system. The small signal model can be derived by assuming each signal to be sum of a constant DC value and small AC perturbation. The DC quantities present in the model are considered to be constant and cancel of on either side of the voltage equations for inductors and current equations for capacitors, thus can be eliminated. In addition, the second order non-linear terms are eliminated as they are assumed to be negligible when compared to the first order AC terms.

The SEPIC inverter shown in Figure 4.1 is a fourth order nonlinear system. The nonlinearity is originated from their inherent switching behavior, which makes the stability analysis, designing and evaluating controllers difficult [33]. The most common, systematic and successful approach to these tasks is linearization. Stability of the linearized model or small signal model indicates the system is stable when operating under nominal operating conditions for small perturbations [34]. System is linearized in a region around the operating point where the system response is assumed to be linear [35].

The state-space averaging (SSA) technique is applied to find small-signal linear dynamic model of the converter and its various transfer functions. As opposed to the PWM-switch model and averaged switch model, the SSA is a matrix-based approach in that all modeling steps in the SSA are performed systematically via matrices. Hence, mathematical software such as MATLAB can readily be used to aid the modeling process [36].

Consider a switching circuit containing one switch such that the circuit switches between two different states in one switching period. There are two circuit states when the switch is operated. One state is when the switch is closed for duration of dT where d

is the duty cycle and T is the switching time period. The other state is when the switch is open for duration of (1-d)T.

Consider the state space model of the circuit with index 1 when switch is closed as:

$$\begin{cases} \dot{x}(t) = A_1 x(t) + B_1 u(t) \\ y = C_1 x(t) + E_1 u(t) \end{cases} \quad (4.13.a)$$

and with index 2 when the switch is open as:

$$\begin{cases} \dot{x}(t) = A_2 x(t) + B_2 u(t) \\ y = C_2 x(t) + E_2 u(t) \end{cases} \quad (4.13.b)$$

The operation of the circuit averaged over one switching cycle can be obtained as:

$$\begin{cases} \dot{x}(t) = A_{avg}\langle x(t)\rangle + B_{avg}\langle u(t)\rangle \\ y = C_{avg}\langle x(t)\rangle + E_{avg}\langle u(t)\rangle \end{cases} \quad (4.14)$$

where in:

$$A_{avg} = dA_1 + (1-d)A_2$$

$$B_{avg} = dB_1 + (1-d)B_2$$

$$C_{avg} = dC_1 + (1-d)C_2$$

$$E_{avg} = dE_1 + (1-d)E_2$$

The terms in the brackets ⟨ ⟩ are the average values. The Equation (4.14) is a nonlinear continuous time equation and it can be linearized by small signal perturbation. Each signal is replaced by a sum of two terms a fixed DC quantity and a small ac variation. The assumption made is that the perturbation is very small compared to the DC values. This perturbation yields the steady state and linear small signal state space equations as:

$$\begin{cases} \dot{X} = AX + BU = 0 \\ Y = CX + EU \end{cases} \quad (4.15)$$

and

$$\begin{cases} \hat{\dot{x}} = A\hat{x}(t) + B\hat{u}(t) + B_d\hat{d}(t) \\ \hat{y} = C\hat{x}(t) + E\hat{u}(t) + E_d\hat{d}(t) \end{cases} \quad (4.16)$$

where

$$A = DA_1 + (1-D)A_2$$

$$B = DB_1 + (1-D)B_2$$
$$C = DC_1 + (1-D)C_2$$
$$E = DE_1 + (1-D)E_2$$
$$B_d = (A_1 - A_2)X + (B_1 - B_2)U$$
$$E_d = (C_1 - C_2)X + (E_1 - E_2)U.$$

The steady state solution of the inverter can be found by solving Equation (4.15) as:

$$\begin{cases} X = -A^{-1}BU \\ Y = (-CA^{-1}B + E)U \end{cases} \tag{4.17}$$

The small signal transfer function of the inverter can be obtained by applying Laplace transform to Equation (4.16). In matrix form, we have

$$\begin{cases} \hat{x}(s) = [(sI - A)^{-1}B \quad (sI - A)^{-1}B_d] \begin{bmatrix} \hat{u}(s) \\ \hat{d}(s) \end{bmatrix} \\ \hat{y}(s) = [C(sI - A)^{-1}B + E \quad C(sI - A)^{-1}B_d + E_d] \begin{bmatrix} \hat{u}(s) \\ \hat{d}(s) \end{bmatrix} \end{cases} \tag{4.18}$$

The SEPIC inverter operates in four different modes. The voltage equations around loops and current equations at nodes, which govern every mode of operation, can be written using kirchoff's laws (KVL and KCL) respectively.

The system is considered to have two inputs namely: input voltage V_g and duty cycle d. The output of the system is the voltage across the load, V_0. To derive the small signal model, each signal is assumed to be the sum of a fixed DC value and a small time varying perturbation. The input voltage becomes $V_g + \hat{v}_g(t)$ and the duty cycle becomes $D + \hat{d}(t)$. The output voltage becomes $V_0 + \hat{v}_0(t)$ and the states become $X + \hat{x}(t)$ where V_g, D, V_0 and X are the steady state operating point variables and the variables expressed with ^ are the small signal perturbations.

When the system is modeled separately for positive and negative half cycles, the small signal equations and models are presented below.

A. Positive Half Cycle

The averaged state space representation of the system when operating to produce positive half cycle of output is:

$$\begin{cases} \dot{x} = A_{avg}^{+} x + B_{avg}^{+} u + B_{d}^{+} d \\ V_o = C_{avg}^{+} x + E_{d}^{+} d \end{cases} \tag{4.19}$$

The positive peak averaged model parameters can be obtained as:

$$A_{avg}^{+} = \begin{bmatrix} \frac{-r_{L1}(R+r_{C2}) + (D-1)(r_{C1}(R+r_{C2}) + Rr_{C2})}{L_1(R+r_{C2})} & \frac{(D-1)Rr_{C2}}{L_1(R+r_{C2})} & \frac{D-1}{L_1} & \frac{(D-1)R}{L_1(R+r_{C2})} \\ \frac{(D-1)Rr_{C2}}{L_2(R+r_{C2})} & \frac{(D-1)Rr_{C2} - (R+r_{C2})(Dr_{C1}+r_{L2})}{L_2(R+r_{C2})} & \frac{D}{L_2} & \frac{(D-1)R}{L_2(R+r_{C2})} \\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ \frac{(1-D)R}{C_2(R+r_{C2})} & \frac{(1-D)R}{C_2(R+r_{C2})} & 0 & -\frac{1}{C_2(R+r_{C2})} \end{bmatrix}$$

$$B_{avg}^{+} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

$$C_{avg}^{+} = \begin{bmatrix} \frac{(1-D)Rr_{C2}}{C_2(R+r_{C2})} & \frac{(1-D)Rr_{C2}}{C_2(R+r_{C2})} & 0 & \frac{R}{R+r_{C2}} \end{bmatrix}$$

$$B_{d}^{+} = [B_{d11}^{+} \;\; B_{d21}^{+} \;\; B_{d31}^{+} \;\; B_{d41}^{+}]^T$$

$$E_{d}^{+} = [E_{d11}^{+}]$$

Upon application of Laplace transform, Equation (4.19) is transformed as shown in Equation (4.20).

$$\begin{cases} sL_1\hat{\imath}_{L1}(s) = \hat{v}_g(s) - \hat{\imath}_{L1}(s)r_{L1} - D'\big(\hat{\imath}_{L1}(s)r_{C1} - \hat{v}_{C1}(s) - \hat{v}_0(s)\big) + \hat{d}(s)(I_{L1}r_{C1} + V_{C1} + V_0) \\ sC_1\hat{v}_{C1}(s) = D'\hat{\imath}_{L1}(s) + D\hat{\imath}_{L2}(s) + \hat{d}(s)(I_{L2} - I_{L1}) \\ sL_2\hat{\imath}_{L2}(s) = D(\hat{v}_{C1}(s) - \hat{\imath}_{L2}(s)r_{C1}) + D'\hat{v}_0(s) + \hat{d}(s)(V_{C1} - I_{L2}r_{C1} - V_0) - \hat{\imath}_{L2}(s)r_{L2} \\ sC_2\hat{v}_{C2}(s) = D'(\hat{\imath}_{L1}(s) + \hat{\imath}_{L2}(s)) - \hat{d}(s)(I_{L1} + I_{L2}) - \frac{\hat{v}_0(s)}{R} \\ \hat{v}_0(s) = \frac{Rr_{C2}}{R+r_{C2}}\big(D'\hat{\imath}_{L1}(s) + D'\hat{\imath}_{L2}(s) - \hat{d}(s)I_{L1} - \hat{d}(s)I_{L2}\big) + \frac{R}{R+r_{C2}}\hat{v}_{C2}(s) \end{cases} \tag{4.20}$$

The small signal model for the system operating to produce positive cycle of output can be obtained from Equation (4.20) and is shown in Figure 4.5.

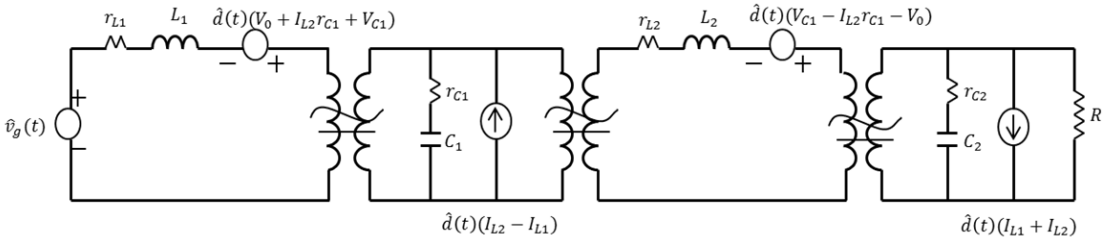


Figure 4.5 Schematic diagram of Small Signal Model of the SEPIC Inverter when operating to produce positive half cycle of output

B. Negative Half Cycle

The averaged state space representation of the system when operating to produce negative half cycle of output is:

$$\begin{cases} \dot{x} = A_{avg}^{-}x + B_{avg}^{-}u + B_d^{-}d \\ V_o = C_{avg}^{-}x + E_d^{-}d \end{cases} \tag{4.21}$$

The negative peak averaged model parameters can be obtained as:

$$A_{avg}^{+} = \begin{bmatrix} \frac{-r_{L1}(R+r_{C2}) + (D-1)(r_{C1}(R+r_{C2}) + Rr_{C2})}{L_1(R+r_{C2})} & \frac{(1-D)Rr_{C2}}{L_1(R+r_{C2})} & \frac{D-1}{L_1} & \frac{(1-D)R}{L_1(R+r_{C2})} \\ \frac{(1-D)Rr_{C2}}{L_2(R+r_{C2})} & \frac{(D-1)Rr_{C2} - (R+r_{C2})(Dr_{C1}+r_{L2})}{L_2(R+r_{C2})} & -\frac{D}{L_2} & \frac{(D-1)R}{L_2(R+r_{C2})} \\ \frac{1-D}{C_1} & \frac{D}{C_1} & 0 & 0 \\ \frac{(D-1)R}{C_2(R+r_{C2})} & \frac{(1-D)R}{C_2(R+r_{C2})} & 0 & -\frac{1}{C_2(R+r_{C2})} \end{bmatrix}$$

$$B_{avg}^{-} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T$$

$$C_{avg}^{-} = \begin{bmatrix} \frac{(D-1)Rr_{C2}}{C_2(R+r_{C2})} & \frac{(1-D)Rr_{C2}}{C_2(R+r_{C2})} & 0 & \frac{R}{R+r_{C2}} \end{bmatrix}$$

$$B_d^{-} = [B_{d11}^{-} \; B_{d21}^{-} \; B_{d31}^{-} \; B_{d41}^{-}]^T$$

$$E_d^{-} = [E_{d11}^{-}]$$

Upon application of Laplace transform, Equation (4.21) is transformed as shown in Equation (4.22).

$$\begin{cases} sL_1\hat{\imath}_{L1}(s) = \hat{v}_g(s) - \hat{\imath}_{L1}(s)r_{L1} - D'\big(\hat{\imath}_{L1}(s)r_{C1} - \hat{v}_{C1}(s) + \hat{v}_0(s)\big) + \hat{d}(s)(I_{L1}r_{C1} + V_{C1} - V_0) \\ sC_1\hat{v}_{C1}(s) = D'\hat{\imath}_{L1}(s) - D\hat{\imath}_{L2}(s) - \hat{d}(s)(I_{L1} + I_{L2}) \\ sL_2\hat{\imath}_{L2}(s) = -D(\hat{v}_{C1}(s) - \hat{\imath}_{L2}(s)r_{C1}) - D'\hat{v}_0(s) + \hat{d}(s)(V_0 - I_{L2}r_{C1} - V_{C1}) - \hat{\imath}_{L2}(s)r_{L2} \\ sC_2\hat{v}_{C2}(s) = D'(\hat{\imath}_{L2}(s) - \hat{\imath}_{L1}(s)) + \hat{d}(s)(I_{L1} - I_{L2}) - \frac{\hat{v}_0(s)}{R} \\ \hat{v}_0(s) = \frac{Rr_{C2}}{R+r_{C2}}\big(-D'\hat{\imath}_{L1}(s) + D'\hat{\imath}_{L2}(s) + \hat{d}(s)I_{L1} - \hat{d}(s)I_{L2}\big) + \frac{R}{R+r_{C2}}\hat{v}_{C2}(s) \end{cases} \quad (4.22)$$

The small signal model for the system operating to produce negative cycle of output can be obtained from Equation (4.22) and is shown in Figure 4.6.

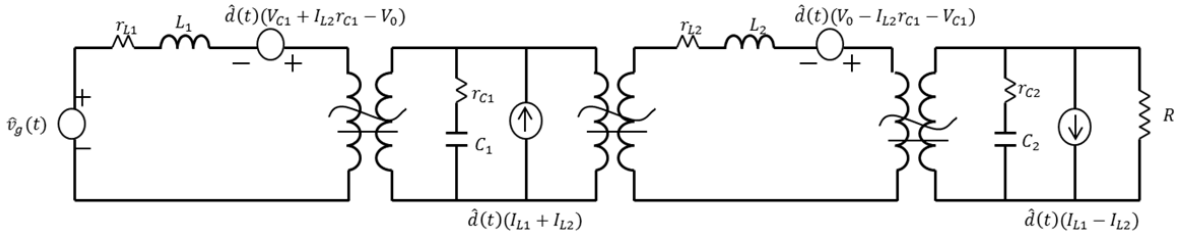


Figure 4.6 Schematic diagram of Small Signal Model of the SEPIC Inverter when operating to produce negative half cycle of output

C. Steady State Equations

In Mode I, the switch Q is off and T_1 is on for duty cycle 1-D. In Mode II, the switch is on and T_1 is off for period of D. The averaged state space model of the system for positive cycle of output voltage is given as:

1) Positive Half-Cycle: Given the averaged matrices in Equation (4.19), the steady state equations of this inverter are obtained from Equation (4.15) as:

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} = \begin{bmatrix} \frac{D}{D'\left(\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}\right)} \\ \frac{1}{\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}} \\ \frac{r_{L2}+Dr_{C1}+\frac{Rr_{C2}}{R+r_{C2}}+\frac{D'R^2}{R+r_{C2}}}{D\left(\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}\right)} \\ \frac{R}{\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}} \end{bmatrix} [V_g]$$

$$V_0 = \left[\frac{\frac{Rr_{C2}}{R+r_{C2}}+\frac{D'R^2}{R+r_{C2}}}{D'\left(\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}\right)}\right][V_g] \quad (4.23)$$

2) Negative Half-Cycle: Given the averaged matrices in Equation (4.21), the steady state equations of this inverter are obtained from Equation (4.15) as:

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} = \begin{bmatrix} \frac{D}{D'\left(\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}\right)} \\ \frac{-1}{\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}} \\ \frac{r_{L2}+Dr_{C1}+\frac{Rr_{C2}}{R+r_{C2}}+\frac{D'R^2}{R+r_{C2}}}{D\left(\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}\right)} \\ \frac{-R}{\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}} \end{bmatrix} [V_g]$$

$$V_0 = \left[\frac{-\frac{Rr_{C2}}{R+r_{C2}}-\frac{D'R^2}{R+r_{C2}}}{D'\left(\frac{D}{D'}r_{L1}+r_{C1}+\frac{Rr_{C2}}{D(R+r_{C2})}+\frac{D'R^2}{D(R+r_{C2})}+\frac{D'}{D}r_{L2}\right)}\right][V_g] \quad (4.24)$$

When the inverter is modeled as one system in all four modes of operation, the system is considered to have four inputs namely: input voltage V_g, load current I_z, duty cycles d_p and d_n describing the duty related to positive and negative half cycles respectively. The output of the system is the voltage across the load, V_0.

The averaged state space representation of the system when operating to produce a complete cycle of output is:

$$\begin{cases} \dot{x} = A_{avg}x + B_{avg}u + B_{dp}d^+ + B_{dn}d^- \\ V_o = C_{avg}x + E_{avg}u + E_{dp}d^+ + E_{dn}d^- \end{cases} \quad (4.25)$$

Where

$$A_{avg} = \begin{bmatrix} A_{11} & \frac{Rr_{C2}(d^+ - d^-)}{L_1(R+r_{C2})} & \frac{d^+ + d^- - 2}{L_1} & \frac{R(d^+ - d^-)}{L_1(R+r_{C2})} \\ \frac{Rr_{C2}(d^+ - d^-)}{L_2(R+r_{C2})} & A_{22} & \frac{d^+ - d^-}{L_2} & \frac{R(d^+ + d^- - 2)}{L_2(R+r_{C2})} \\ \frac{2 - d^+ - d^-}{C_1} & \frac{-(d^+ + d^-)}{C_1} & 0 & 0 \\ \frac{R(d^- - d^+)}{C_2(R+r_{C2})} & \frac{R(2 - d^+ - d^-)}{C_2(R+r_{C2})} & 0 & \frac{-(d^+ + d^-)}{C_2(R+r_{C2})} \end{bmatrix}$$

$$B_{avg} = \begin{bmatrix} \frac{2}{L_1} & -\frac{Rr_{C2}(d^+ - d^-)}{L_1(R+r_{C2})} \\ 0 & \frac{Rr_{C2}(2 - d^+ - d^-)}{L_1(R+r_{C2})} \\ 0 & 0 \\ 0 & \frac{-2R}{C_2(R+r_{C2})} \end{bmatrix}$$

$$C_{avg} = \begin{bmatrix} \frac{Rr_{C2}(d^- - d^+)}{R+r_{C2}} & \frac{Rr_{C2}(2 - d^+ - d^-)}{R+r_{C2}} & 0 & \frac{2R}{R+r_{C2}} \end{bmatrix}$$

$$E_{avg} = \begin{bmatrix} 0 & -\frac{2Rr_{C2}}{R+r_{C2}} \end{bmatrix}$$

$$B_{dp} = [B_{dp11} \quad B_{dp21} \quad B_{dp31} \quad B_{dp41}]^T$$

$$B_{dn} = [B_{dn11} \quad B_{dn21} \quad B_{dn31} \quad B_{dn41}]^T$$

$$E_{dp} = [E_{dp11}]$$

$$E_{dn} = [E_{dn11}]$$

Upon application of Laplace transform, Equation (4.25) is transformed as shown in Equation (4.26).

$$\begin{cases} sL_1\hat{\imath}_{L1}(s) = (k_p + k_n)(\hat{v}_g(s) - \hat{\imath}_{L1}(s)r_{L1}) - (k_pD_p' + k_nD_n')(\hat{\imath}_{L1}(s)r_{C1} + \hat{v}_{C1}(s)) - (k_pD_p' - k_nD_n')\hat{v}_0(s) + (k_p\hat{d}_p + k_n\hat{d}_n)(I_{L1}r_{C1} + V_{C1}) + (k_p\hat{d}_p + k_n\hat{d}_n)V_o \\ sC_1\hat{v}_{C1}(s) = (k_pD_p' + k_nD_n')\hat{\imath}_{L1}(s) - (k_pD_p - k_nD_n)\hat{\imath}_{L2}(s) - (k_p\hat{d}_p + k_n\hat{d}_n)I_{L1} - (k_p\hat{d}_p - k_n\hat{d}_n)I_{L2} \\ sL_2\hat{\imath}_{L2}(s) = (k_pD_p - k_nD_n)\hat{v}_{C1}(s) - (k_p + k_n)\hat{\imath}_{L2}(s)r_{L2} - (k_pD_p + k_nD_n)\hat{\imath}_{L2}(s)r_{C1} - (k_pD_p' + k_nD_n')\hat{v}_0(s) + (k_p\hat{d}_p + k_n\hat{d}_n)V_o + (k_p\hat{d}_p - k_n\hat{d}_n)V_{C1} \\ sC_2\hat{v}_{C2}(s) = (k_pD_p' - k_nD_n')\hat{\imath}_{L1}(s) + (k_pD_p' + k_nD_n')\hat{\imath}_{L2}(s) - (k_p\hat{d}_p - k_n\hat{d}_n)I_{L1} - (k_p\hat{d}_p + k_n\hat{d}_n)I_{L2} - (k_p + k_n)(\frac{\hat{v}_0(s)}{R} - \hat{\imath}_z(s)) \\ \hat{v}_0(s) = (k_p + k_n)\left(\hat{v}_{C2}(s)\frac{R}{R+r_{C2}} - \hat{\imath}_z(s)\frac{Rr_{C2}}{R+r_{C2}}\right) + (k_pD_p' - k_nD_n')\hat{\imath}_{L1}(s)\frac{Rr_{C2}}{R+r_{C2}} + (k_pD_p' + k_nD_n')\hat{\imath}_{L2}(s)\frac{Rr_{C2}}{R+r_{C2}} - (k_p\hat{d}_p - k_n\hat{d}_n)I_{L1}\frac{Rr_{C2}}{R+r_{C2}} - (k_p\hat{d}_p + k_n\hat{d}_n)I_{L2}\frac{Rr_{C2}}{R+r_{C2}} \end{cases} \quad (4.26)$$

The small signal model for the system operating to produce a complete cycle of output can be obtained from Equation (4.26).

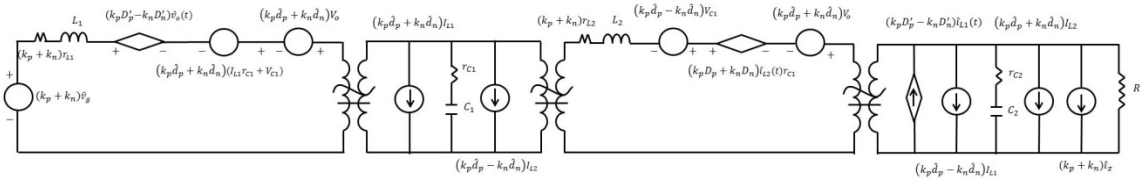


Figure 4.7 Schematic diagram of Small Signal Model of the SEPIC Inverter when operating to produce complete cycle of output

Given the averaged matrices in (4.25), the steady state equations of this inverter are obtained from Equation (4.15) as:

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} = \begin{bmatrix} S_{11} \\ S_{21} \\ S_{31} \\ S_{41} \end{bmatrix} [V_g] \qquad (4.27)$$

$$V_0 = [S_0][V_g]$$

4.3 Transfer Functions of Inverter

State space averaging techniques have been employed to derive the transfer functions and small signal model of the inverter after mathematical analysis.

The AC output voltage $\hat{v}_0(t)$ can be expressed as the superposition of the terms arising from the two inputs.

$$\hat{v}_0(s) = G_d^{v_0}(s)\hat{d}(s) + G_{v_g}^{v_0}(s)\hat{v}_g(s) \qquad (4.28)$$

The first term in (4.27) represents the control to output transfer function while the second term represents the line to output transfer function. The transfer functions $G_d^{v_0}(s)$ and $G_{v_g}^{v_0}(s)$ can be defined as:

$$G_d^{v_0}(s) = \left.\frac{\hat{v}_0(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0} \quad and \quad G_{v_g}^{v_0}(s) = \left.\frac{\hat{v}_0(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0}$$

From (4.18), the various transfer functions can be determined as follows:

The control to output and line voltage to output transfer functions can be determined using the equations shown in (4.29).

$$\begin{cases} G_d^{v_0}(s) = C(sI - A)^{-1}B_d + E_d \\ G_{v_g}^{v_0}(s) = C(sI - A)^{-1}B + E \end{cases} \tag{4.29}$$

The transfer functions for the control to inductor currents, control to capacitor voltages can be derived from Equation (4.18) as follows:

$$\begin{cases} G_d^{i_{L1}}(s) = [(sI - A)^{-1}B_d]_{11} \\ G_d^{i_{L2}}(s) = [(sI - A)^{-1}B_d]_{21} \\ G_d^{v_{c1}}(s) = [(sI - A)^{-1}B_d]_{31} \\ G_d^{v_{c2}}(s) = [(sI - A)^{-1}B_d]_{41} \end{cases} \tag{4.30}$$

The transfer functions of line voltage to inductor currents and capacitor voltages are determined from Equation (4.18) as:

$$\begin{cases} G_{v_g}^{i_{L1}}(s) = [(sI - A)^{-1}B]_{11} \\ G_{v_g}^{i_{L2}}(s) = [(sI - A)^{-1}B]_{21} \\ G_{v_g}^{v_{c1}}(s) = [(sI - A)^{-1}B]_{31} \\ G_{v_g}^{v_{c2}}(s) = [(sI - A)^{-1}B]_{41} \end{cases} \tag{4.31}$$

The control to output transfer function is studied to determine if the system has any right half plane zeros. The presence of right half zeros implies system is non-minimum phase. Control of such systems is complicated compared to minimal phase systems. The values of the circuit components may be varied to check if the zeros can be moved from the right half plane to the left half plane.

Various transfer functions of the inverter are derived in Equations (4.29) - (4.31). The transfer functions of the control to inductor currents and capacitor voltages are given in

Equation (4.30). The transfer function for the line voltage to inductor currents and capacitor voltages are given in Equation (4.31). However, only the control to output transfer function is analyzed.

4.4 Analysis of transfer functions of Inverter

1. *Positive Half Cycle:* The structure of the control to output transfer function is:

$$G_d^{v_0}(s) = \frac{N_{p4}s^4+N_{p3}s^3+N_{p2}s^2+N_{p1}s+N_{p0}}{D_{p4}s^4+D_{p3}s^3+D_{p2}s^2+D_{p1}s+D_{p0}} \quad (4.32)$$

The system when operating to produce positive half cycle of output voltage has four zeros of which one is in the right half plane making the system non-minimal phase. All four poles of the system lie in the left half plane. It is important to study the movement of poles and zeros of the system in its entire operating range to keep satisfactory performance and stability [35]. The location of the poles and zeros are plotted and studied when one parameter is varied at a time. The values of the inductors L_1, L_2; capacitors C_1, C_2 and duty cycle D are varied separately while keeping all other parameters constant. The plots are analyzed to check the region in the operating range which would give satisfactory response.

For the sizing parameters of the system, the system has three zeros in left half plane (LHP) and one zero in right half plane (RHP). All poles of the system are in the LHP. The inductance L_1 value is varied from 1 μH to 100 μH. From Figure 4.8, it can be seen that one of the four zeros of the system does not move for any change in value of L_1. As we increase the value of L_1 more than 11 μH, the complex pair of zeros move from the LHP to the RHP and moves along the imaginary axis towards the origin. The zero which was already in the RHP moves towards the origin on the real axis but does not go into the LHP. From Figure 4.9, it can be seen that as we increase the value of L_1, one pair of complex poles move slightly towards the RHP but remain in the LHP at all times while the other pair of complex poles moves further into the LHP.

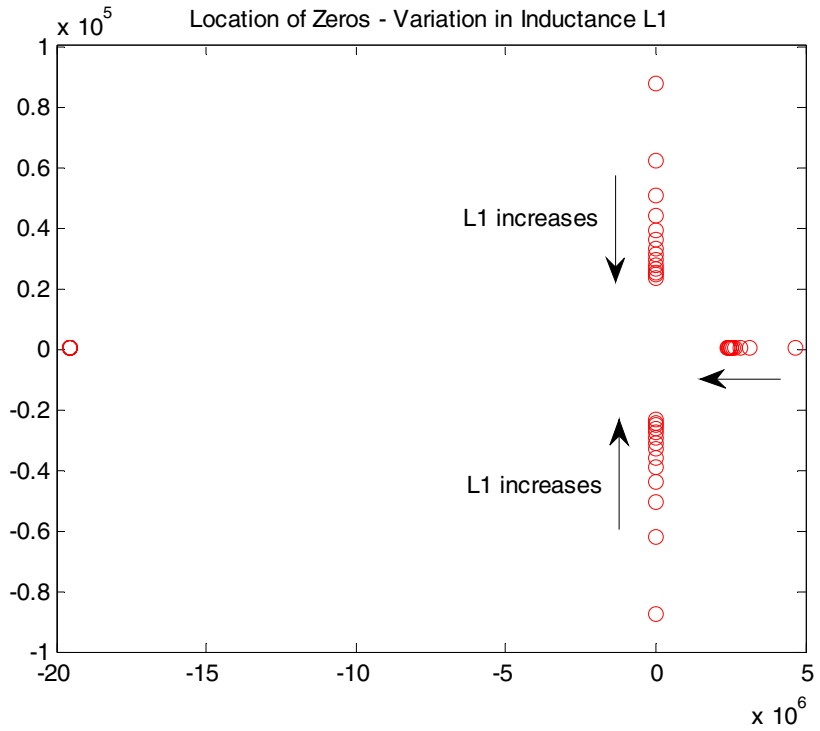


Figure 4.8 Locations of zeros for variation in inductance L_1 - Positive half cycle

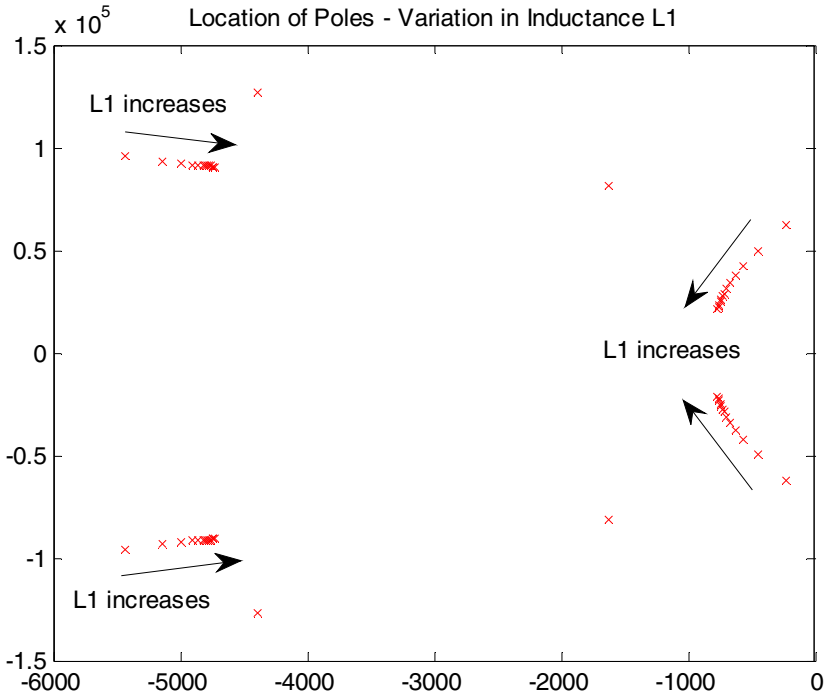


Figure 4.9 Locations of poles for variation in inductance L_1 - Positive half cycle

For the sizing parameters of the system, the system has three zeros in the LHP and one zero in the RHP. The inductance value is varied from 1 μH to 100 μH. From Figure 4.10 it can be seen that one of the zeros in the LHP does not move for any change in value of L_2. As we increase the value of L_2, the complex pair of zeros moves along the imaginary axis towards the origin. The zero which was already in the RHP moves towards the origin on the real axis but does not go into the LHP. From Figure 4.11, it can be seen that all poles of the system are in the LHP. As we increase the value of L_2,one pair of complex poles move slightly towards the RHP but remain in the LHP at all times while the other pair of complex poles moves further into the LHP.

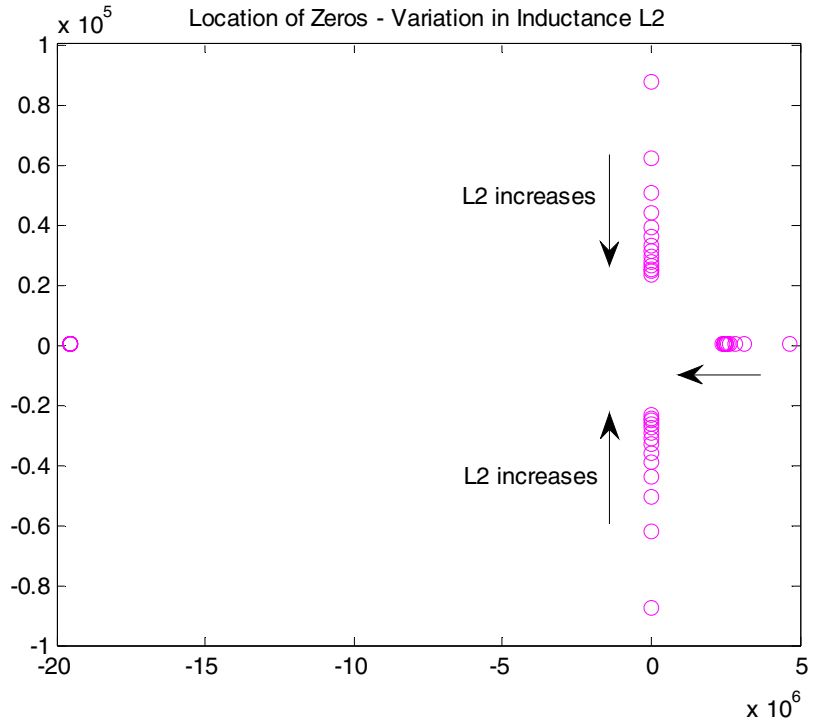


Figure 4.10 Locations of zeros for variation in inductance L_2 - Positive half cycle

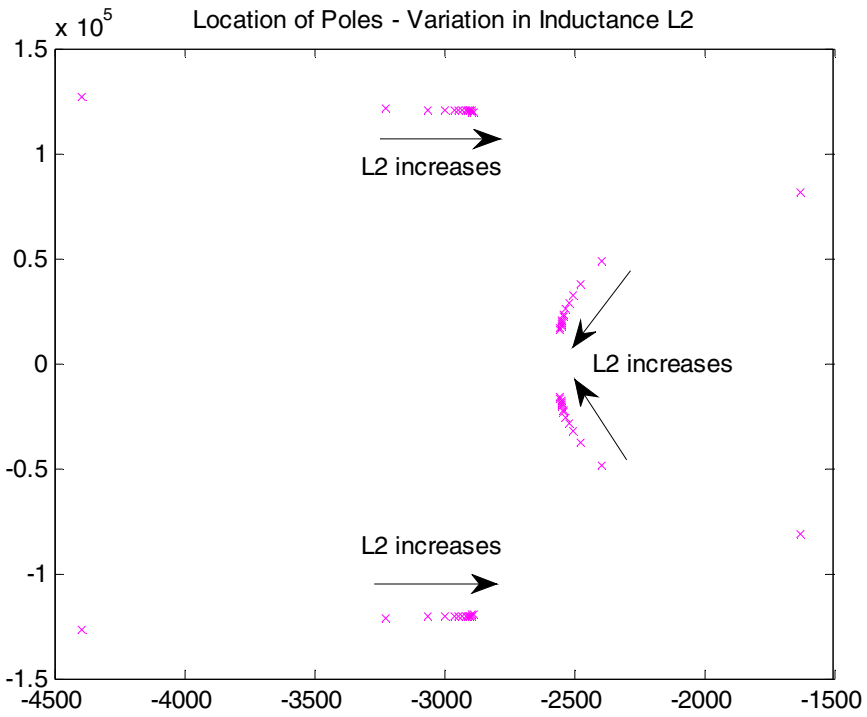


Figure 4.11 Locations of poles for variation in inductance L_2 - Positive half cycle

From Figures 4.12, the system has three zeros in the LHP and one zero in the RHP. As the value of C_1 is increased, the complex pair of zeros moves along the imaginary axis towards the origin. The other zero in the LHP and the zero in the RHP never move for any change in the value of C_1. From Figure 4.13, all poles of the system remain in the LHP at all times. As the value of C_1 is increased, one complex pair of poles moves further into the LHP while the other pair of poles moves towards the RHP. But the poles never cross over into the RHP.

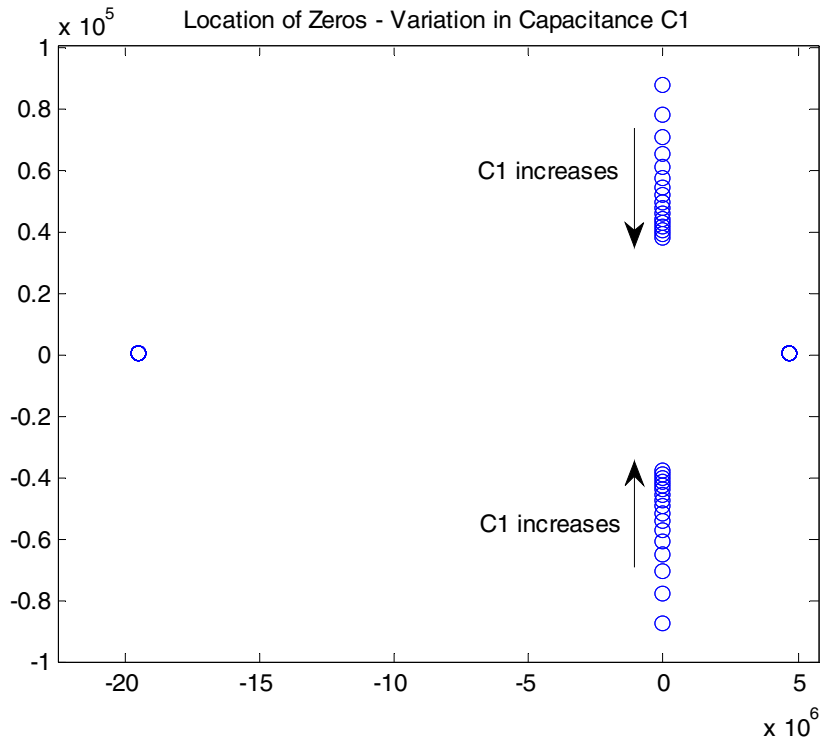


Figure 4.12 Locations of zeros for variation in capacitance C_1 - Positive half cycle

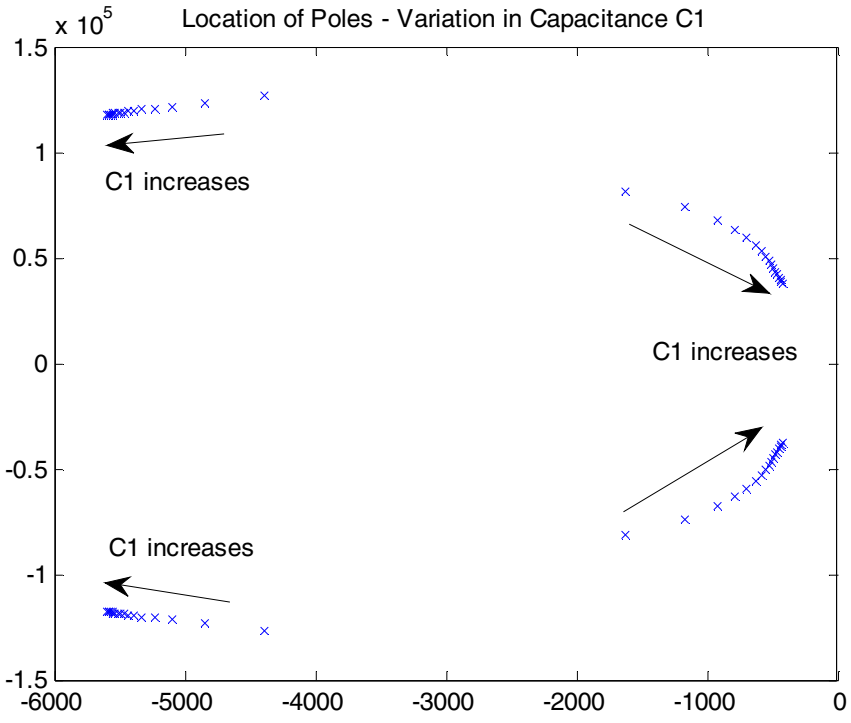


Figure 4.13 Locations of poles for variation in capacitance C_1 - Positive half cycle

The capacitance C_2 is varied from 15 µF to 1000 µF. From Figure 4.14, it can be seen that the system has three zeros in the LHP and one zero in the RHP. The zero in the RHP does not move for any change in value of C_2. One of the zeros in the LHP moves along the axis towards the origin but always remains in the LHP. The complex pair of zero does not move for any change in value of C_2. From Figure 4.15, as the value of C_2 is increased, the two pairs of complex poles moves slowly towards the origin but remains in the LHP.

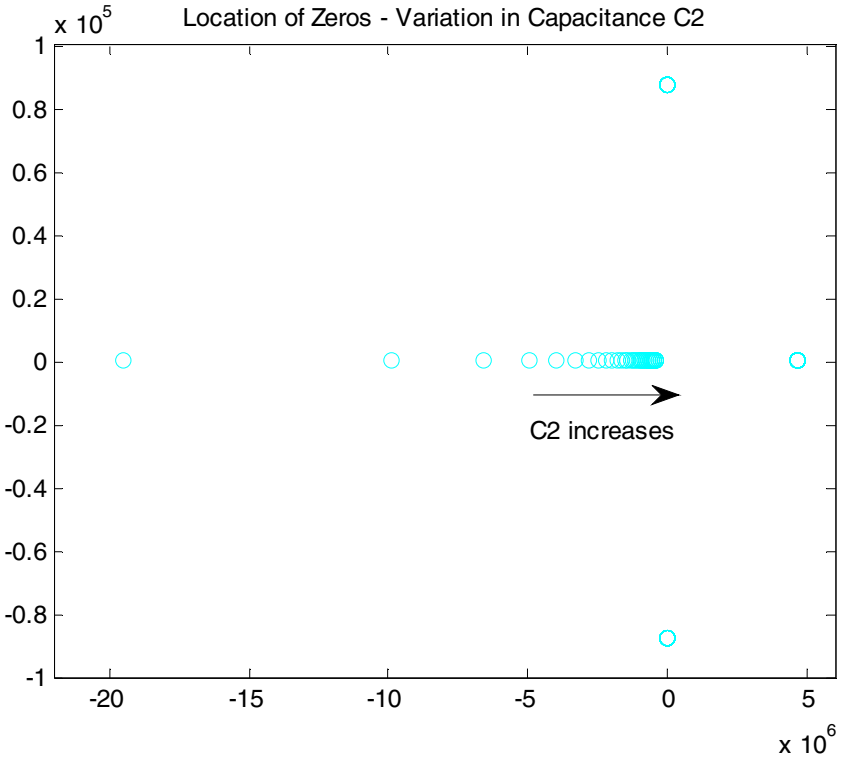


Figure 4.14 Locations of zeros for variation in capacitance C_2 - Positive half cycle

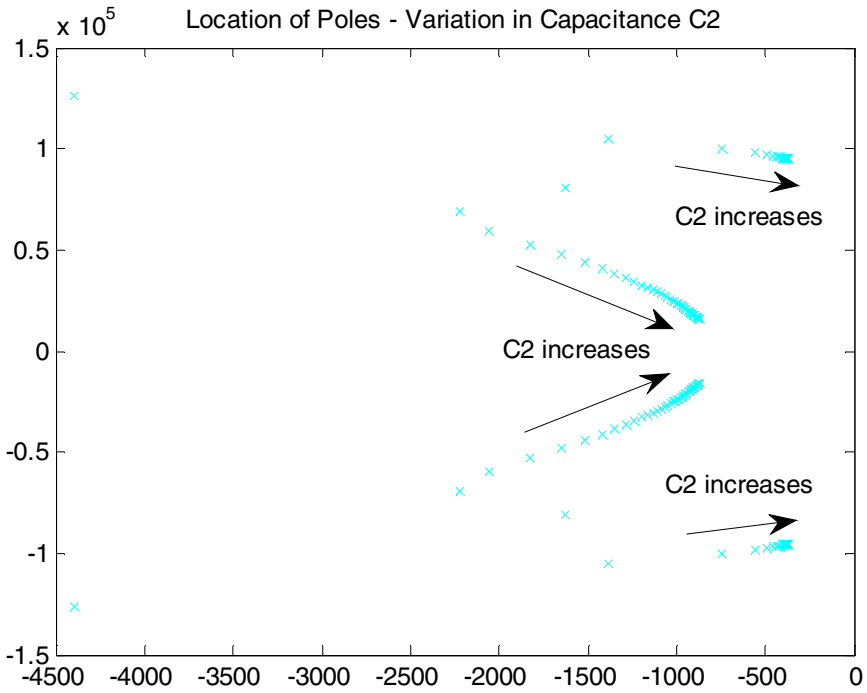


Figure 4.15 Locations of poles for variation in capacitance C_2 - Positive half cycle

Figures 4.16 and 4.17 show the movement of the zeros and poles of the system when the duty cycle is varied, respectively. The duty cycle is varied from 0.1 to 0.9. For buck operation, 3 zeros are in the LHP and one in the RHP. When the operation shifts to boost, two zeros move from the LHP to the RHP. However, one zero remains in the LHP and doesn't move for any change in value of duty cycle. The zero which was earlier in the RHP moves towards the origin but doesn't go into the LHP. All the poles remain in the LHP for both buck and boost operation.

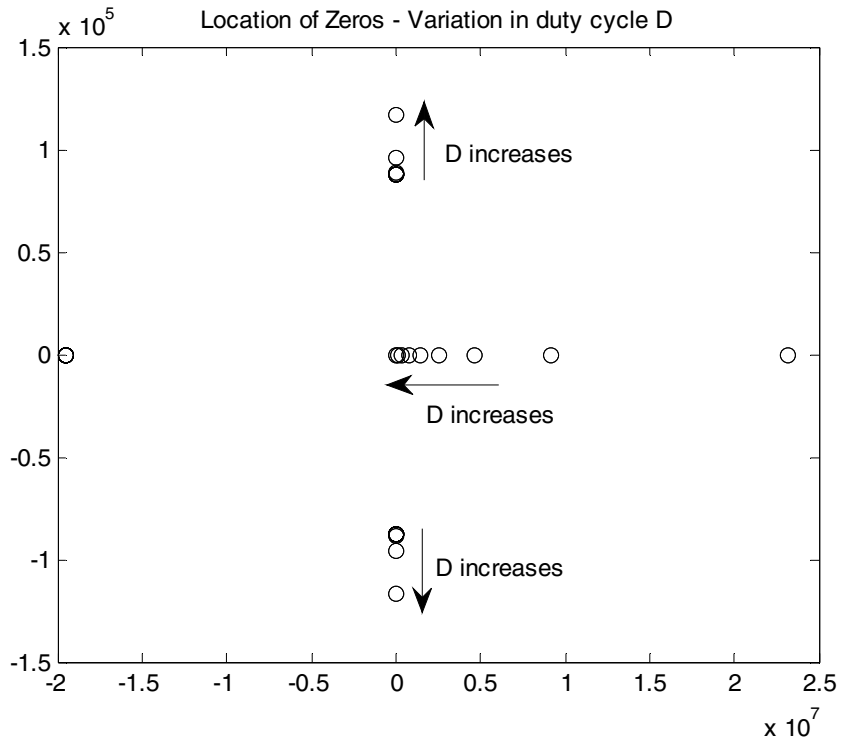


Figure 4.16 Locations of zeros for variation in duty cycle D - Positive half cycle

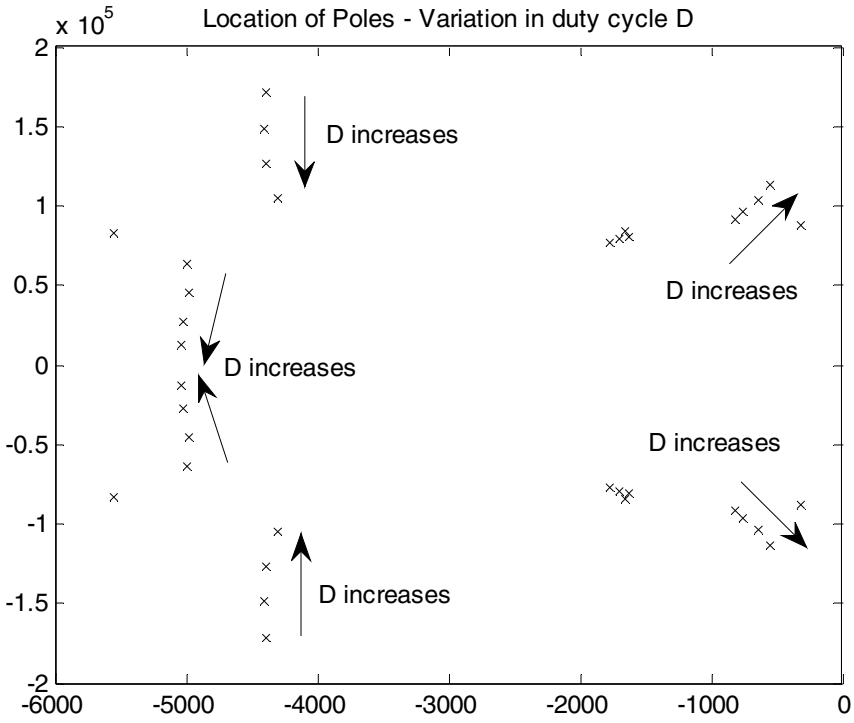


Figure 4.17 Locations of poles for variation in duty cycle D - Positive half cycle

2. *Negative Half Cycle:* The structure of control to output transfer function is:

$$G_d^{v_0}(s) = \frac{N_{n4}s^4+N_{n3}s^3+N_{n2}s^2+N_{n1}s+N_{n0}}{D_{n4}s^4+D_{n3}s^3+D_{n2}s^2+D_{n1}s+D_{n0}} \quad (4.33)$$

When the system is operating to produce negative cycle of output voltage, it has four poles all of which are in the LHP ensuring stable operations. The system has four zeros. The root-locus has been plotted to study the movement of poles and zeros to determine a region of stable operation and satisfactory response. One parameter is varied at a time to check the movement of poles and zeros while other parameters are fixed. The values of the inductors L_1, L_2; capacitors C_1, C_2 and duty cycle D are varied separately while keeping all other parameters constant.

For the sizing parameters of the system, the system has three zeros in the LHP and one zero in the RHP when the system is operating to produce negative half cycle. The inductance value is varied from 1 μH to 100 μH. From Figure 4.18, it can be seen that one complex pair of zeros moves along the imaginary axis towards the origin while the other zero in the LHP moves further into the LHP. As the value of L_1 is increased above 11 μH, the complex pair of zeros moves into the RHP. The zero in the RHP moves towards the LHP but never crosses over. From Figure 4.19, it can be seen that all poles of the system are in the LHP. One pair of complex poles moves towards the RHP but never moves into the RHP while the other pair of complex poles moves further into the LHP only.

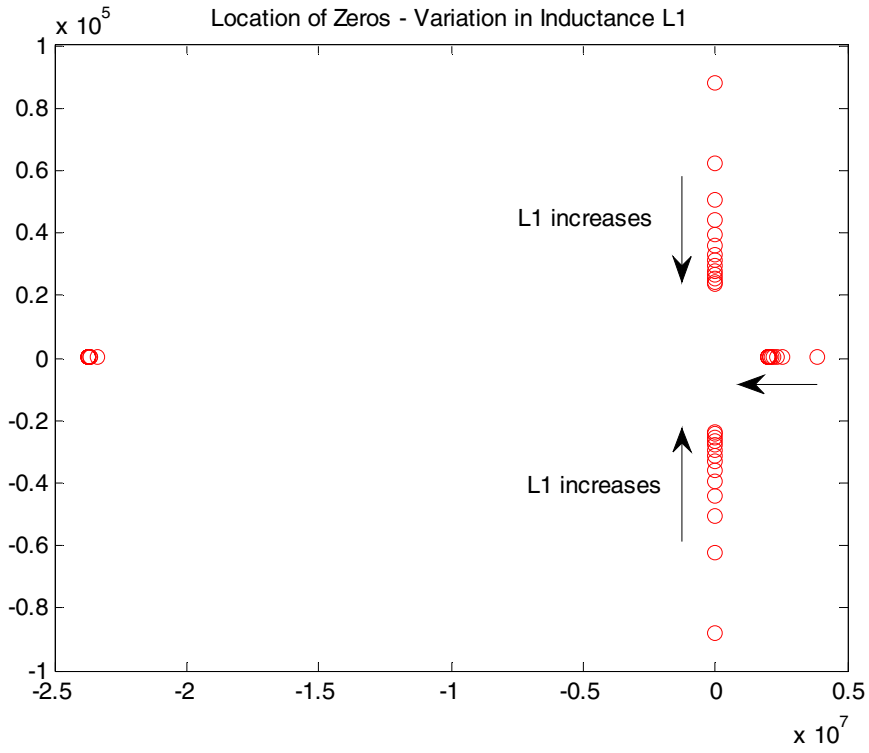


Figure 4.18 Locations of zeros for variation in inductance L_1 - Negative half cycle

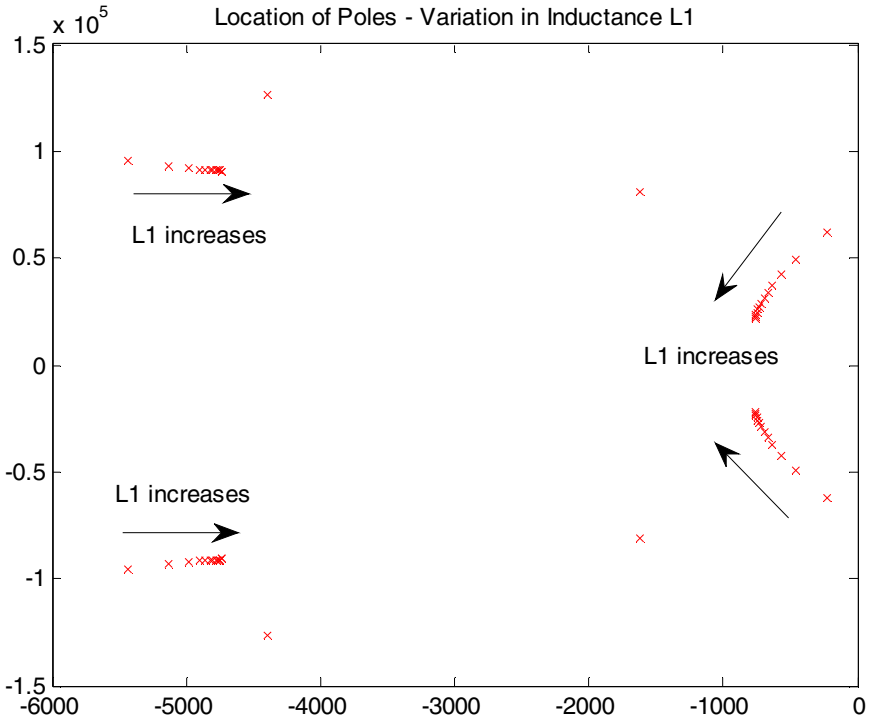


Figure 4.19 Locations of poles for variation in inductance L_1 - Negative half cycle

The value of L_2 is varied from 1 μH to 100 μH. The system has four zeros of which three are in the LHP and one in the RHP. The system has non-minimal phase behavior. From Figure 4.20, as the value of L_2 is increased, the complex pair of poles in the LHP moves along the imaginary axis towards the origin. The zero in the LHP moves towards the RHP while the zero in the RHP moves towards the LHP but neither of them cross over the imaginary axis. From Figure 4.21, it can be seen that all the poles are in the LHP. One complex pair of poles moves towards RHP while the other complex pair moves further into the LHP. The poles remain in the LHP for all values of L_2.

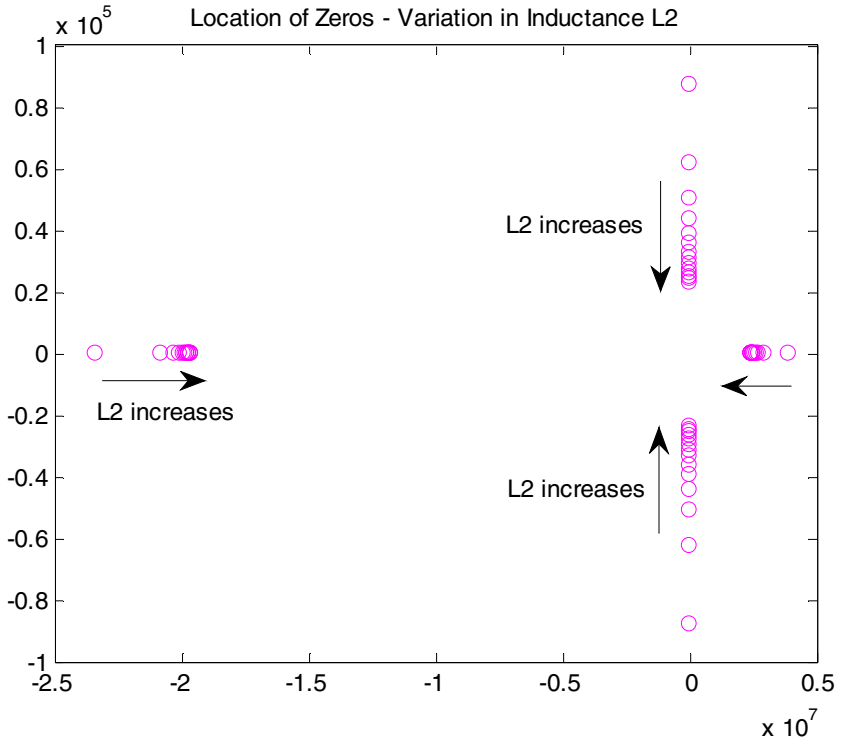


Figure 4.20 Locations of zeros for variation in inductance L_2 - Negative half cycle

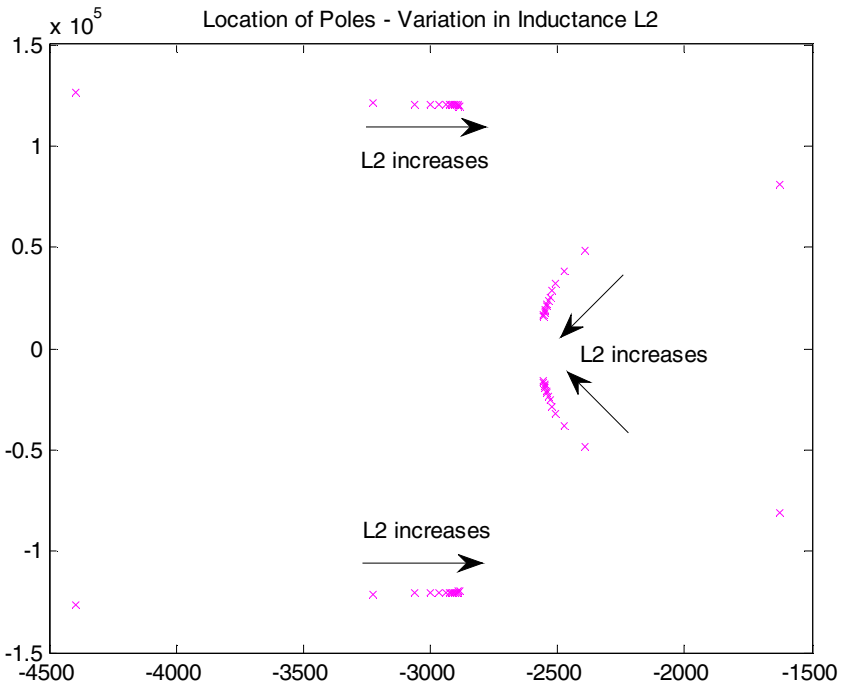


Figure 4.21 Locations of poles for variation in inductance L_2 - Negative half cycle

The capacitance C_1 is varied from 12 µF to 100 µF. From Figure 4.22, it can be seen that the system has four zeros of which three are in the LHP while one is in the RHP. The complex pair of zeros in the LHP moves along the imaginary axis towards the origin. The other zeros do not move for any change in value of C_1. From Figure 4.23, the system has four poles, all of which are in the LHP. One complex pair of poles moves deeper into the LHP while the other pair moves towards the RHP but never crosses over.

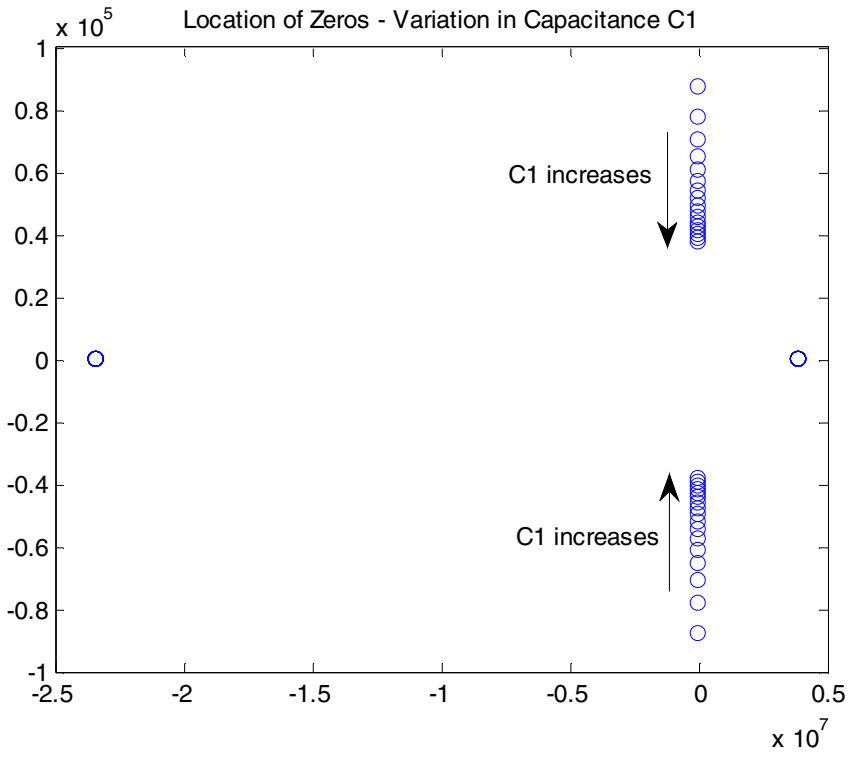


Figure 4.22 Locations of zeros for variation in capacitance C_1 - Negative half cycle

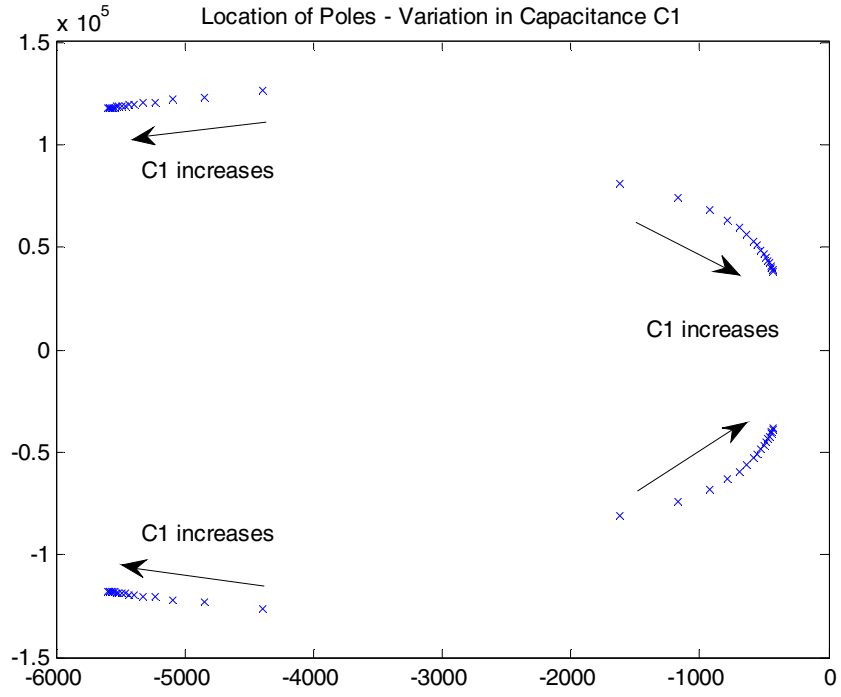


Figure 4.23 Locations of poles for variation in capacitance C_1 - Negative half cycle

The capacitance C_2 is varied from 15 µF to 1000 µF. The system has three zeros in the LHP and one zero in the RHP. From Figure 4.24, it can be seen that as the value of C_2 is increased, the zero in the LHP moves towards the RHP while the zero in the RHP moves towards the LHP. The complex pair of zeros moves from the LHP into the RHP as the value of C_2 increases beyond 170 µF. From Figure 4.25, it can be seen that the system has two complex pairs of poles which are in the LHP. The poles never move into the RHP. Both the pairs of poles move towards the RHP for an increase in value of C_2.

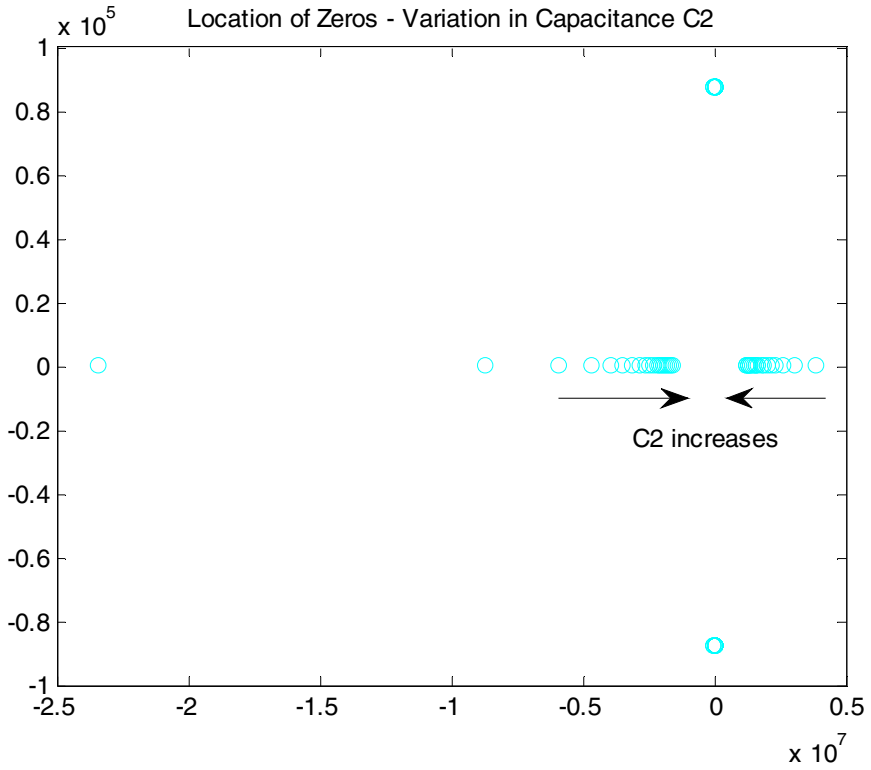


Figure 4.24 Locations of zeros for variation in capacitance C_2 - Negative half cycle

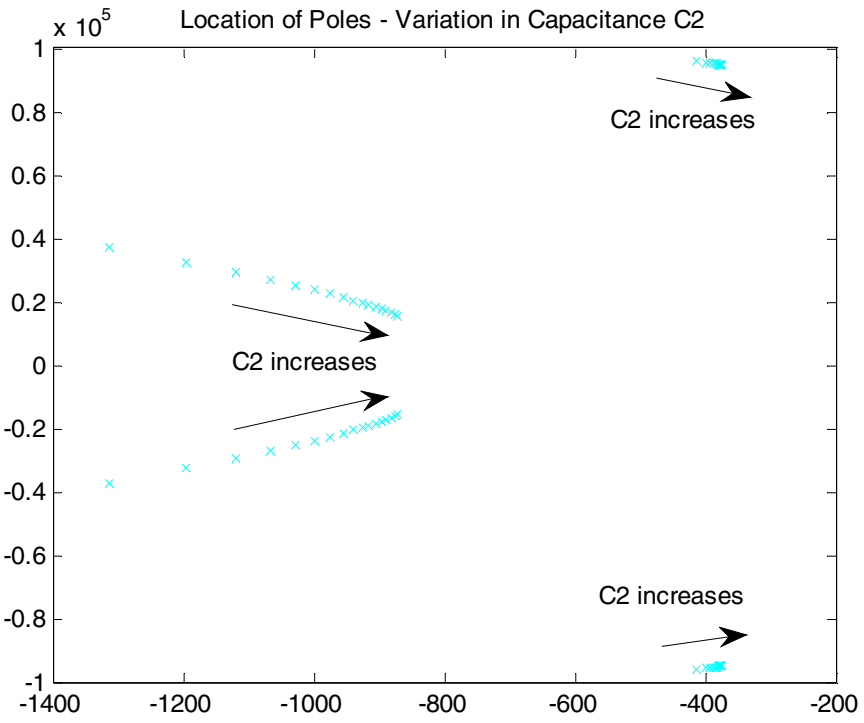


Figure 4.25 Locations of poles for variation in capacitance C_2 - Negative half cycle

Figures 4.26 and 4.27 show the movement of the zeros and poles of the system when the duty cycle is varied, respectively. The duty cycle is varied from 0.1 to 0.9 to study the system in buck and boost operating modes. In the buck mode, the system has minimal phase behavior i.e. all zeros in the LHP for a duty cycle up to 0.2 while two zeros move into the RHP for duty between 0.2 and 0.5. All the poles remain in the LHP but move towards the RHP. In the boost mode, the all zeros of the system are in the LHP for duty cycle between 0.5 and 0.6. One of the zeros moves into the RHP for duty cycle greater than 0.6. All poles remain in the LHP but one pair moves deeper into the LHP while the other pair moves towards the RHP.

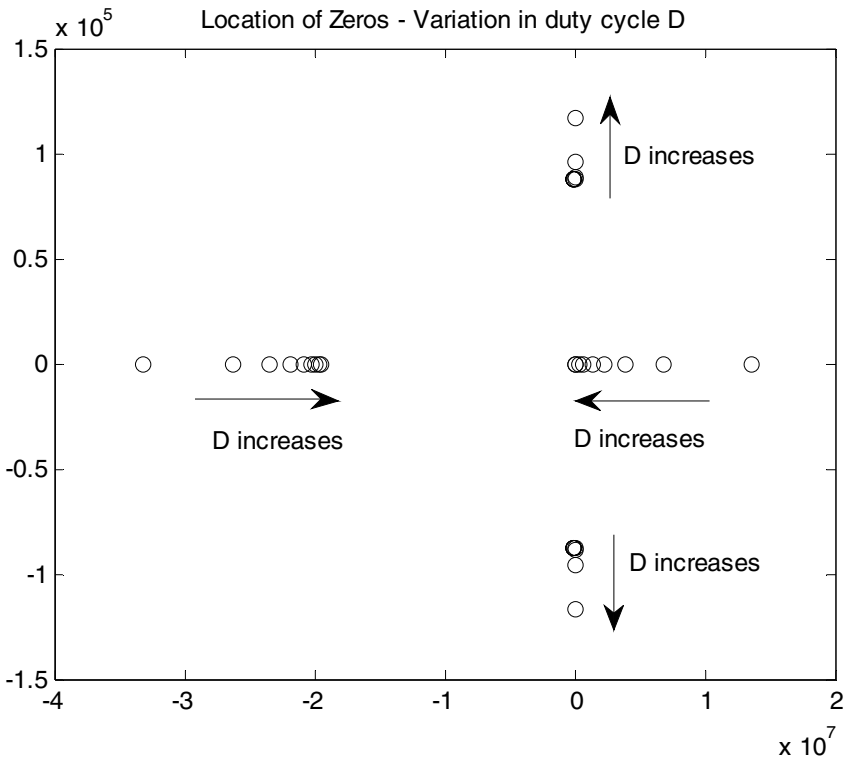


Figure 4.26 Locations of zeros for variation in duty cycle D - Negative half cycle

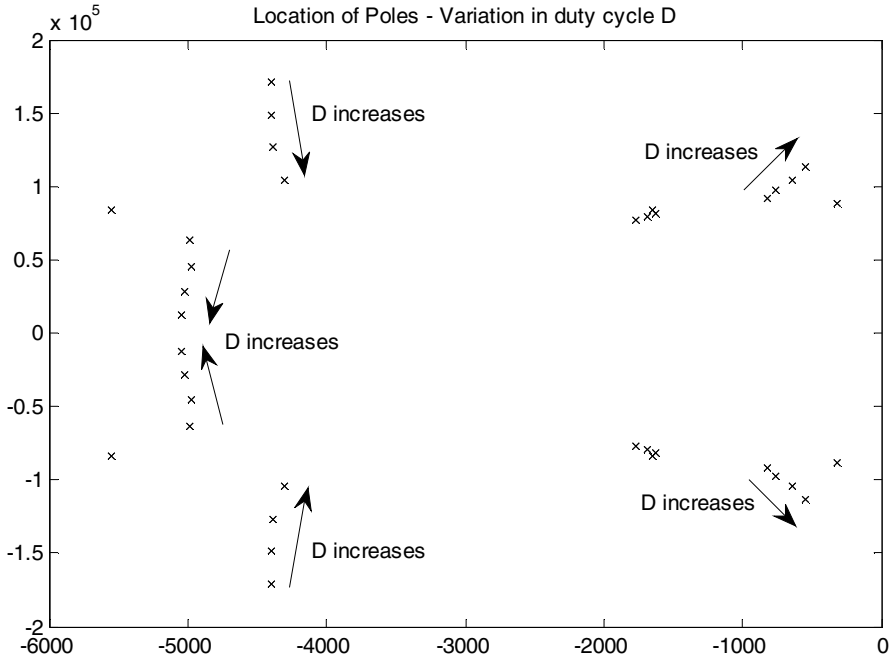


Figure 4.27 Locations of poles for variation in duty cycle D - Negative half cycle

When the system is modeled as a complete system where the different modes are averaged over one complete cycle, the control to output transfer functions for the positive and negative half cycles have similar structure. These transfer functions are analyzed to validate the root locus maps obtained in the previous modeling.

A. Positive Half-Cycle: The structure of the control to output transfer function is:

$$G_d^{v_0}(s) = \frac{N_{p4}s^4+N_{p3}s^3+N_{p2}s^2+N_{p1}s+N_{p0}}{D_{p4}s^4+D_{p3}s^3+D_{p2}s^2+D_{p1}s+D_{p0}} \tag{4.34}$$

The system when operating to produce positive half cycle of output voltage has four zeros of which three are in the left half plane and one in the right half plane. All four poles of the system lie in the left half plane. There is a need to study the movement of poles and zeros of the system to find regions of stable and satisfactory operation of the inverter [35]. The location of the poles and zeros are plotted and studied when one parameter is varied at a time. The values of the inductors L_1, L_2; capacitors C_1, C_2 and duty cycle D are varied separately while keeping all other parameters constant.

The value of L_1 is varied from 1 μH to 100 μH. From Figure 4.28, the system is found to have four zeros of which three are in the LHP and one is in the RHP. One of the LHP zeros does not move for any change in value of L_1. The complex pair of zero moves along the imaginary axis towards the origin and for a value of L_1 greater than 11 μH, this pair of zeros moves into the RHP. The RHP zero moves towards the LHP along the real axis but never crosses over. From Figure 4.29, all poles of the system are in the LHP. One pair of complex poles moves further into the LHP while the other pair moves towards the RHP but never crosses over.

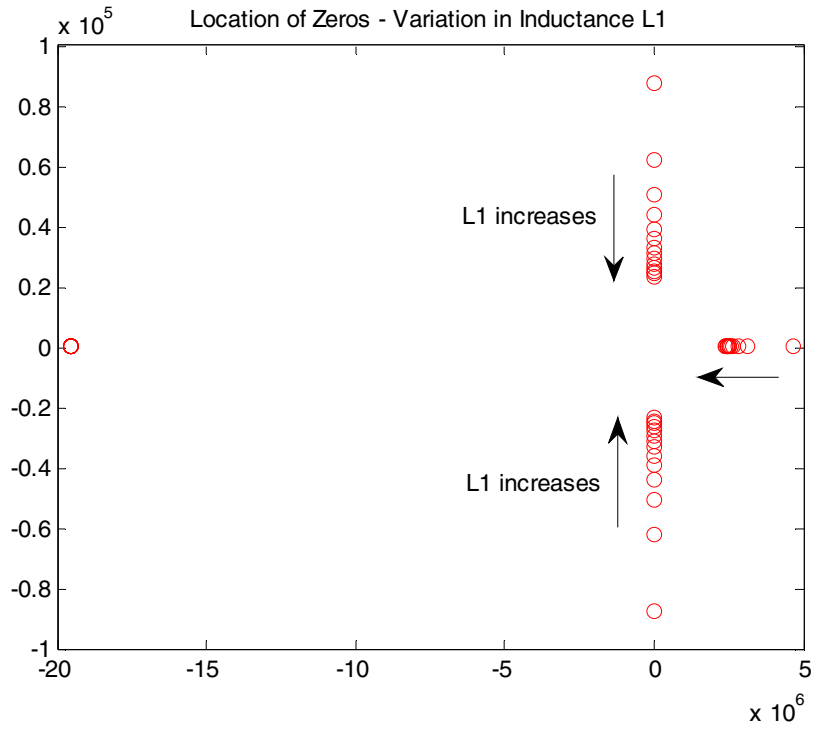


Figure 4.28 Validation of movement of zeros for variation in inductance L_1 - Positive half cycle

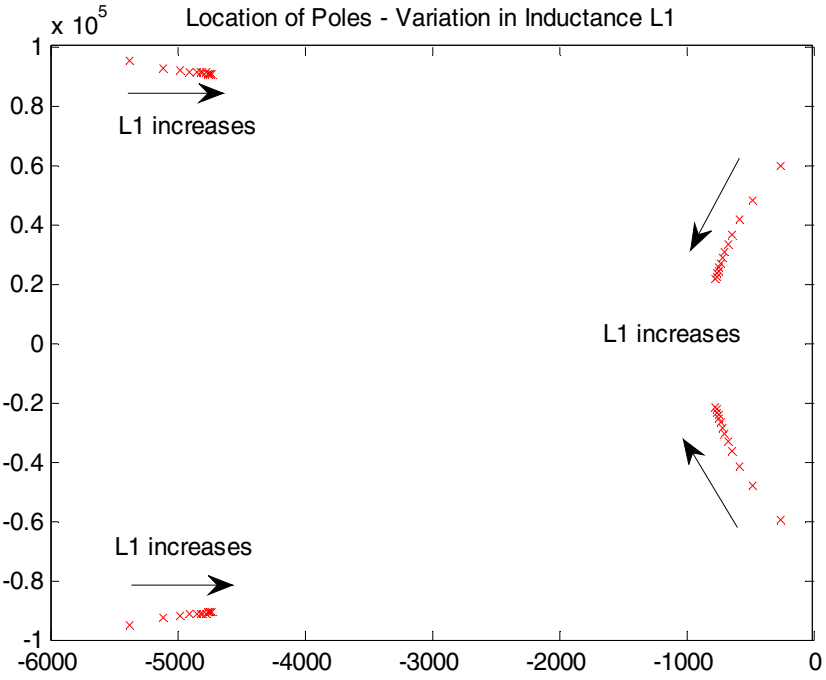


Figure 4.29 Validation of movement of poles for variation in inductance L_1 - Positive half cycle

The value of L_2 is varied from 1 µH to 100 µH. From Figure 4.30, the system has four zeros of which three are in the LHP and one in the RHP. One LHP zero does not move for any change in L_2. The complex pair of LHP zeros moves along the imaginary axis towards the origin. The zero in the RHP moves along the real axis towards the origin but remains in the RHP. From Figure 4.31, the system has four poles all of which always remain in the LHP. One pair of the poles move towards the RHP and the other pair of poles move into the LHP towards the real axis.

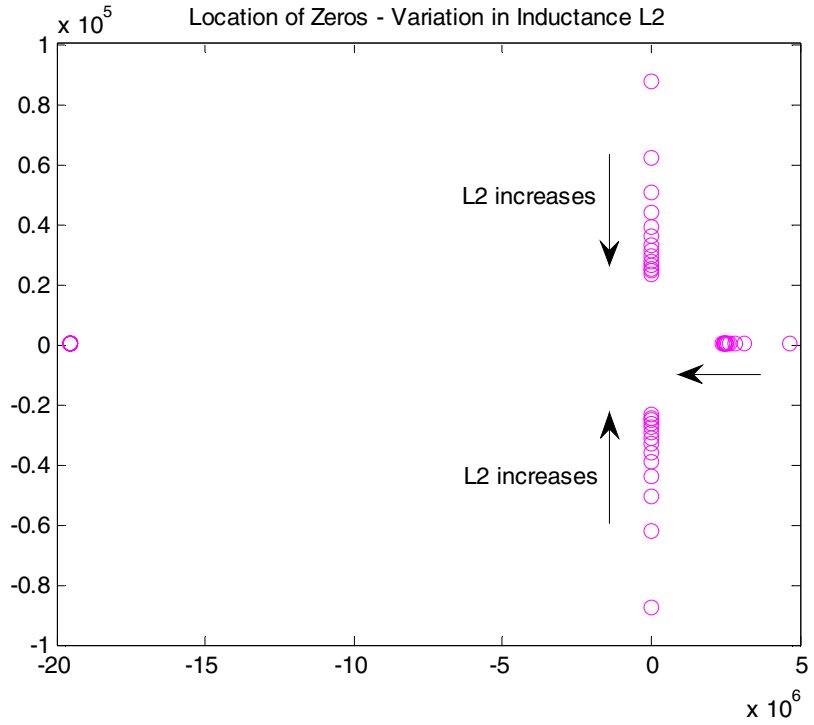


Figure 4.30 Validation of movement of zeros for variation in inductance L_2 - Positive half cycle

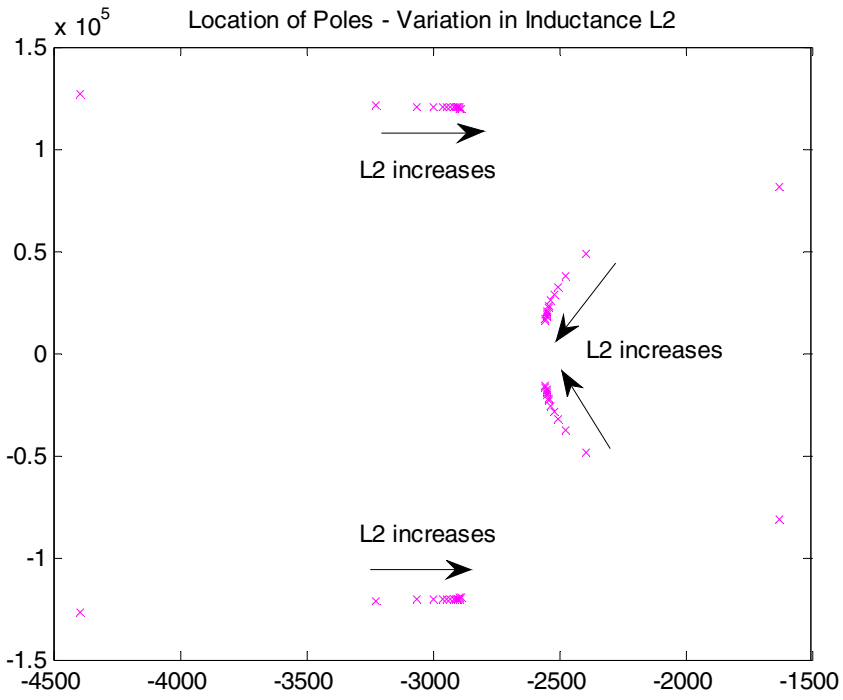


Figure 4.31 Validation of movement of poles for variation in inductance L_2 - Positive half cycle

The capacitance C_1 is varied from 12 µF to 100 µF. From Figure 4.32, it can be seen that the system has four zeros, three of which remain in the LHP and one in the RHP. As the value of C_1 is increased, the complex pair of zeros move along the imaginary axis towards the origin. The other zeros do not move for any change in value of C_1. From Figure 4.33, the poles of the system remain in the LHP. One pair of the complex poles moves further into the LHP while the other pair moves towards the RHP but never crosses over.

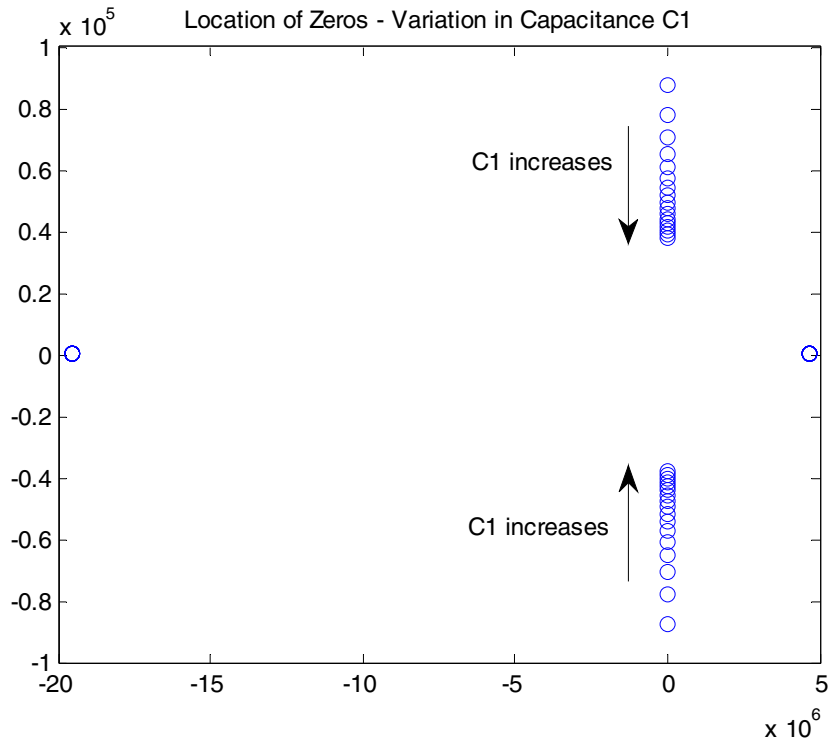


Figure 4.32 Validation of movement of zeros for variation in capacitance C_1 - Positive half cycle

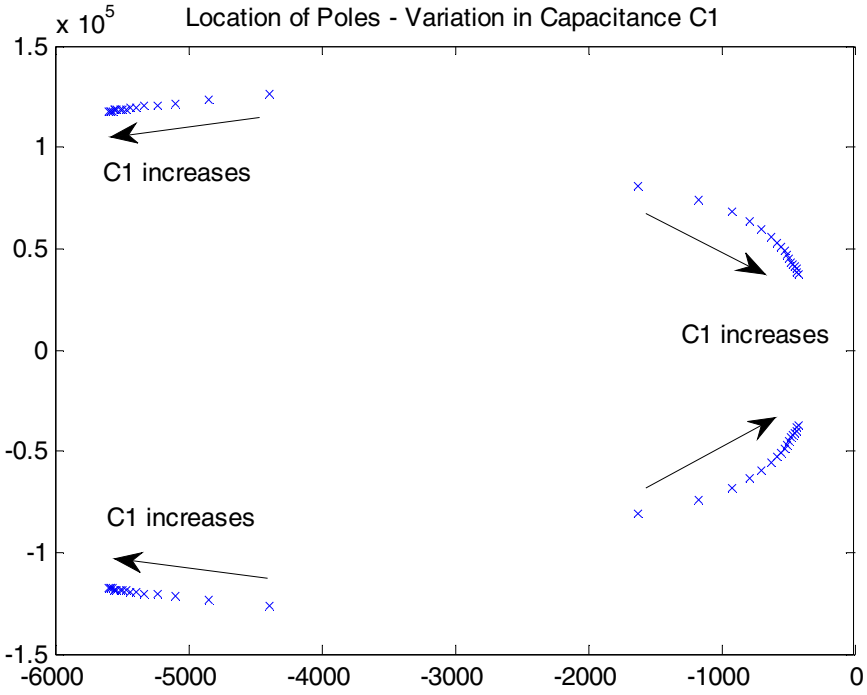


Figure 4.33 Validation of movement of poles for variation in capacitance C_1 . Positive half cycle

The value of C_2 is varied from 15 µF to 1000 µF. From Figure 4.34, the four zeros of the system of which three remain in the LHP and one zero is in the RHP at all times. The zero in the LHP move slowly towards the RHP along the real axis. The other three zeros do not move for any change in value of C_2. From Figure 4.35, the poles remain in the LHP always. One complex pair of poles moves towards the RHP till a point and then move along the imaginary axis towards the origin. The other pair of poles also moves towards the RHP.

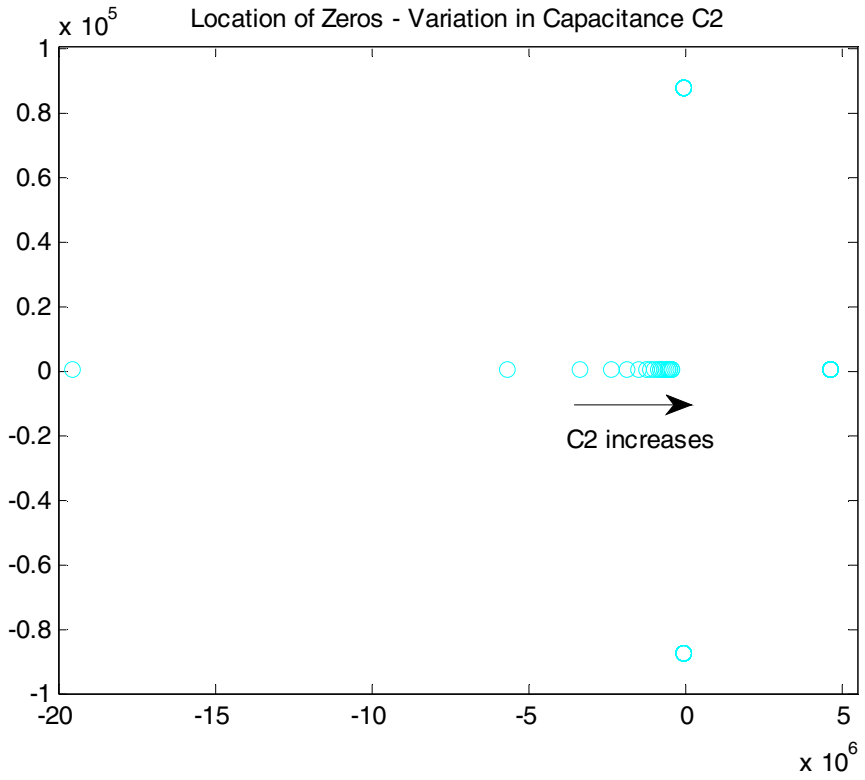


Figure 4.34 Validation of movement of zeros for variation in capacitance C_2 . Positive half cycle

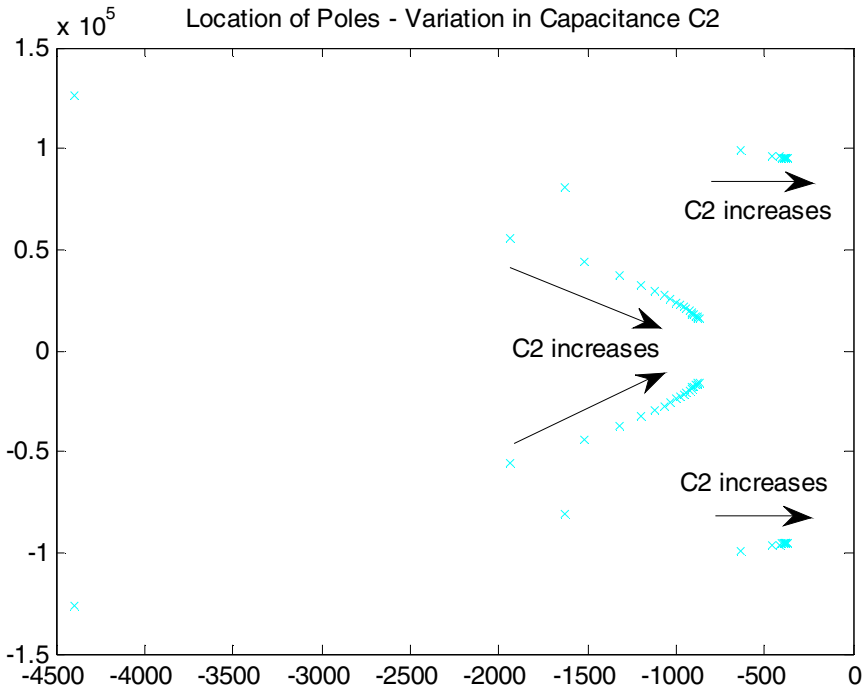


Figure 4.35 Validation of movement of poles for variation in capacitance C_2 . Positive half cycle

Figures 4.36 and 4.37 show the movement of zeros and poles of the system respectively. The duty cycle is varied from 0.1 to 0.9 to cover buck and boost modes of operation. In the buck mode, the system has four zeros, three of which are in the LHP and one in the RHP. The system has non-minimal phase behavior in buck mode. In the boost mode, the complex pair of zeros in the LHP moves into the RHP. The system now has three zeros in the RHP and one zero in the LHP. The zero in the RHP moves along the real axis towards the origin but never moves into the LHP. The zero in the LHP does not move for any change in the duty cycle. All the poles remain in the LHP ensuring stable operation for all values of duty cycle. As the duty cycle is increased, the poles move further into the LHP.

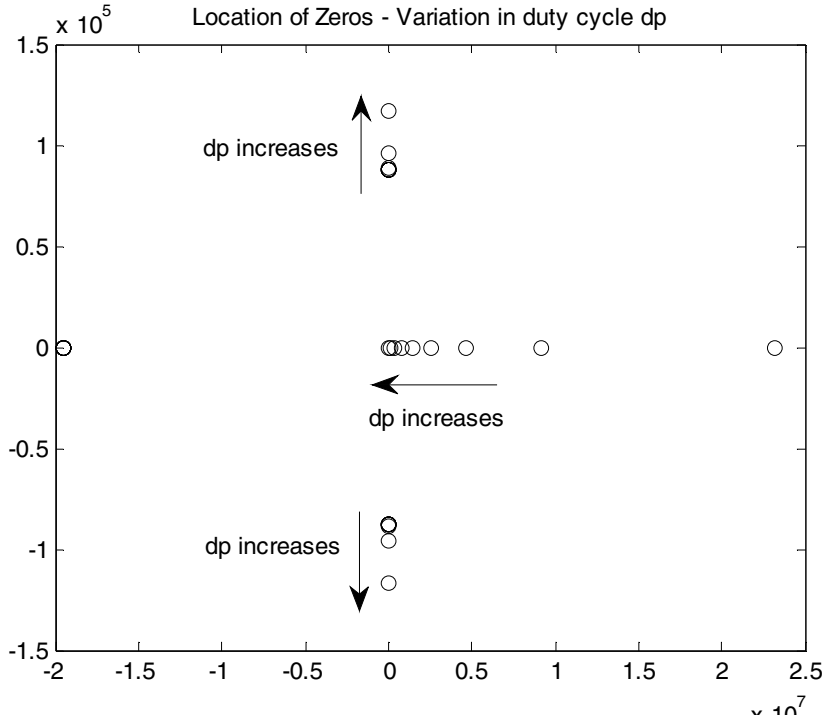


Figure 4.36 Validation of movement of zeros for variation in duty cycle dp - Positive half cycle

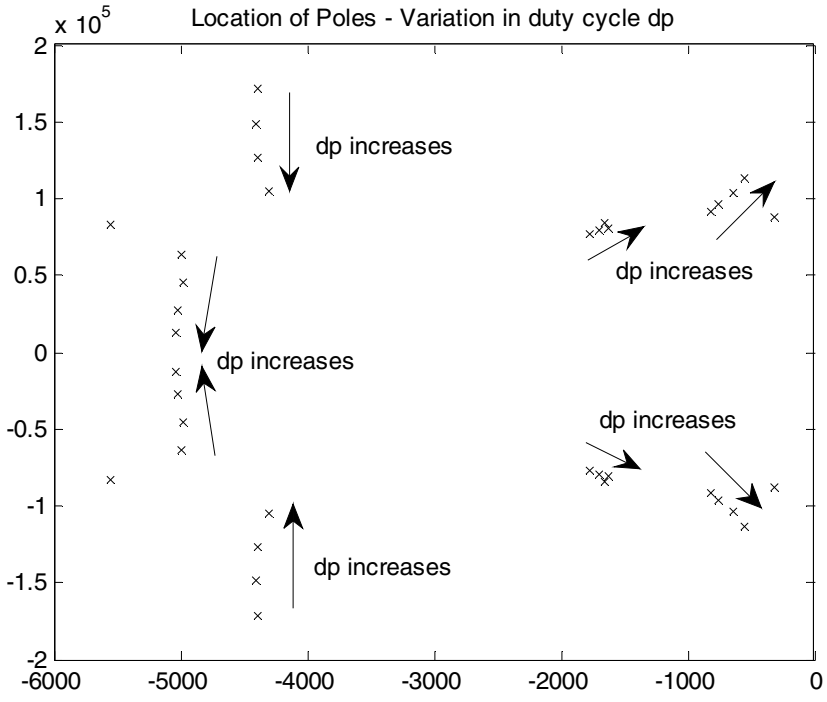


Figure 4.37 Validation of movement of poles for variation in duty cycle dp - Positive half cycle

B. Negative Half-Cycle: The structure of the control to output transfer function is:

$$G_d^{v_0}(s) = \frac{N_{n4}s^4+N_{n3}s^3+N_{n2}s^2+N_{n1}s+N_{n0}}{D_{n4}s^4+D_{n3}s^3+D_{n2}s^2+D_{n1}s+D_{n0}} \quad (4.35)$$

The system when operating to produce negative half cycle of output voltage has four zeros of which three are in the left half plane and one in the right half plane. All four poles of the system lie in the left half plane. There is a need to study the movement of poles and zeros of the system to find regions of stable and satisfactory operation of the inverter [35]. The location of the poles and zeros are plotted and studied when one parameter is varied at a time. The values of the inductors L_1, L_2; capacitors C_1, C_2 and duty cycle D are varied separately while keeping all other parameters constant.

The value of L_1 is varied from 1 μH to 100 μH. From Figure 4.38, the system has four zeros of which three are in the LHP and one in the RHP. As the value of L_1 is increased, the complex pair of zeros moves along the imaginary axis towards the origin. As the value of L_1 is increased above 11 μH, the complex pair of zeros moves into the RHP. The other zero in the RHP moves towards the origin along the real axis but never moves into the LHP. The zero in the LHP does not move for any change in value of L_1. From Figure 4.39, the poles of the system are in the LHP. As the value of L_1 is increased, one complex pair of poles moves towards the RHP while the other complex pair of poles moves deeper into the LHP. All the poles of the system remain in the LHP at all times.

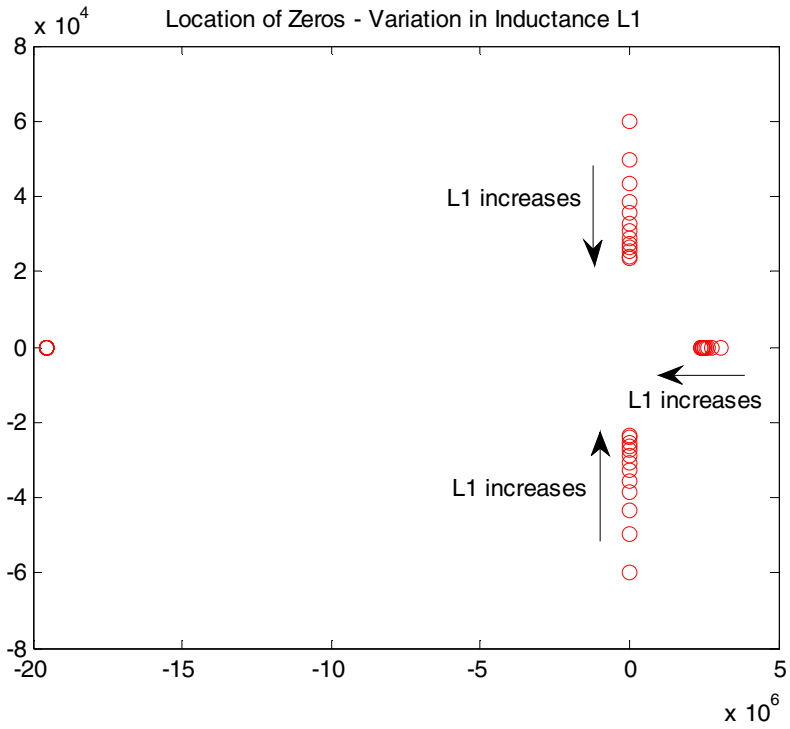


Figure 4.38 Validation of movement of zeros for variation in inductance L_1 - Negative half cycle

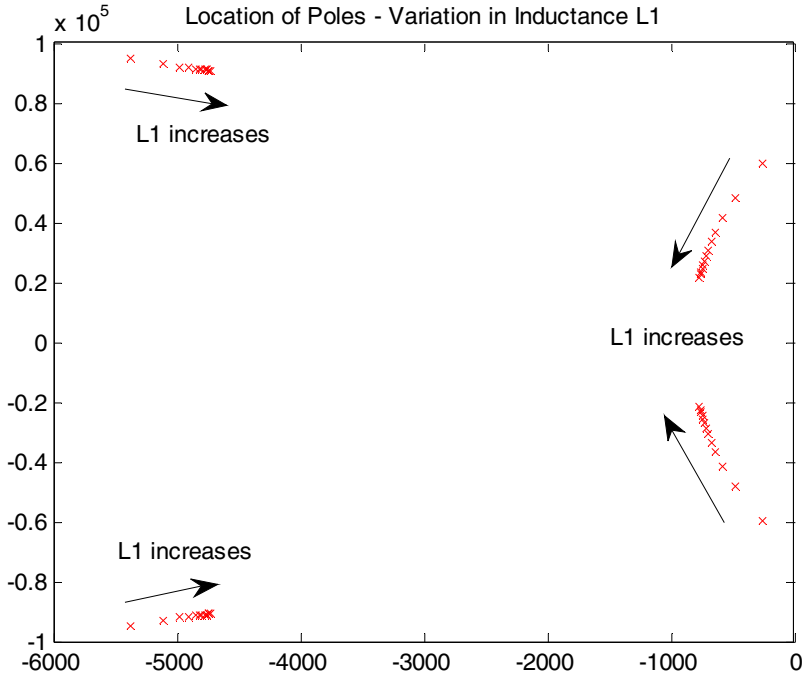


Figure 4.39 Validation of movement of poles for variation in inductance L_1 - Negative half cycle

The value of inductance L_2 is varied from 1 µH to 100 µH. From Figure 4.40, the system has four zeros of which three are in the LHP and one in the RHP. The zero in the RHP moves towards the origin along the real axis but never crosses over into the LHP. The complex pair of zero moves along the imaginary axis towards the origin while the other zero in the LHP does not move for any increase in L_2. From Figure 4.41, all poles are always in the LHP. All the poles move towards the RHP for any increase in value of L_2 but never cross over.

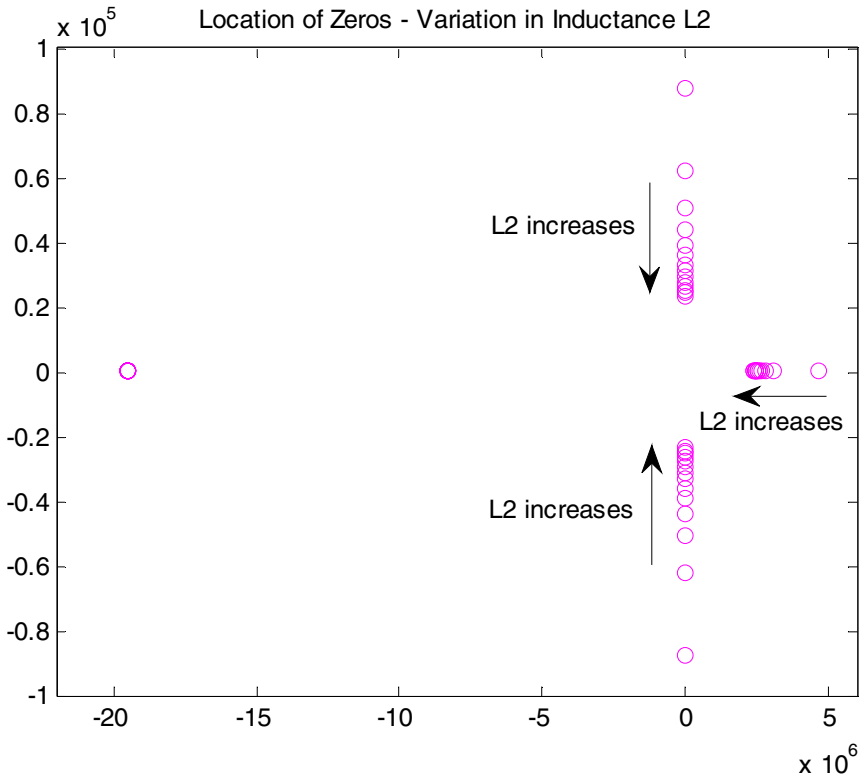


Figure 4.40 Validation of movement of zeros for variation in inductance L_2 - Negative half cycle

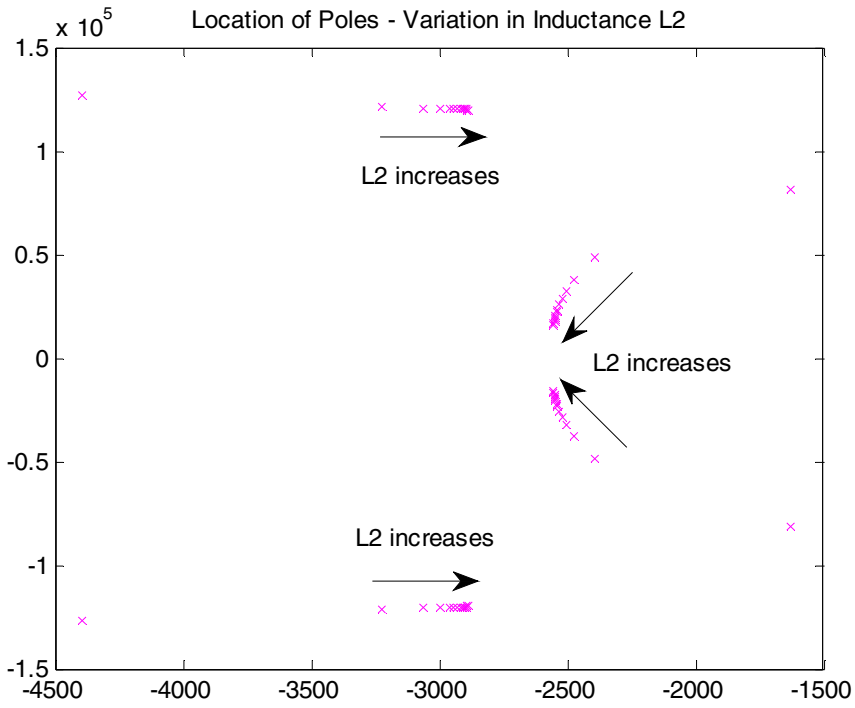


Figure 4.41 Validation of movement of poles for variation in inductance L_2 - Negative half cycle

The value of C_1 is varied from 12 μF to 100 μF. From Figure 4.42, the system has four zeros of which three are in the LHP and one in the RHP. As the value of C_1 is increased, the complex pair of zeros move along the imaginary axis towards the origin while the other zeros does not move. From Figure 4.43, all poles remain in the LHP always. One pair of complex poles moves further into the LHP while the other pair of poles move slightly towards the RHP. All poles remain in the LHP at all times.

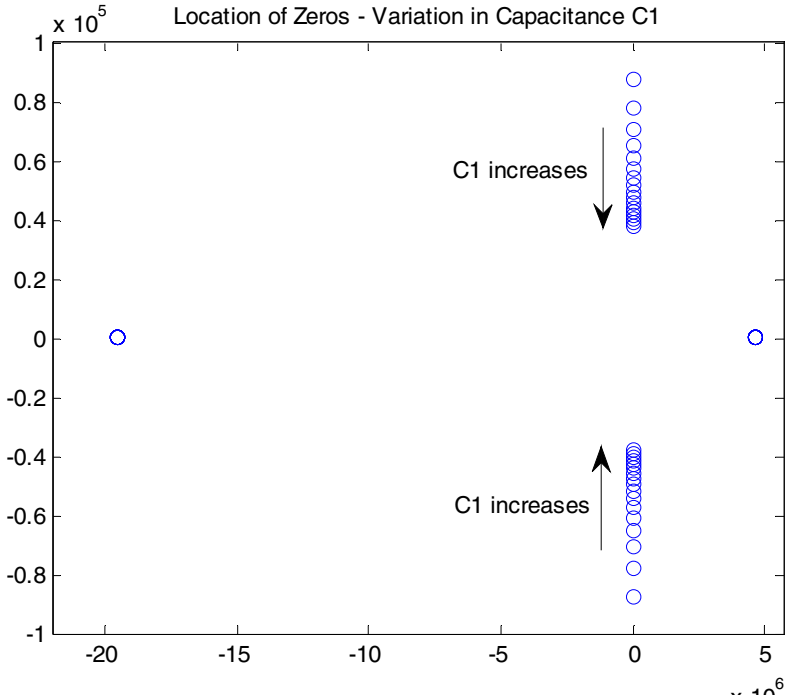


Figure 4.42 Validation of movement of zeros for variation in capacitance C_1 - Negative half cycle

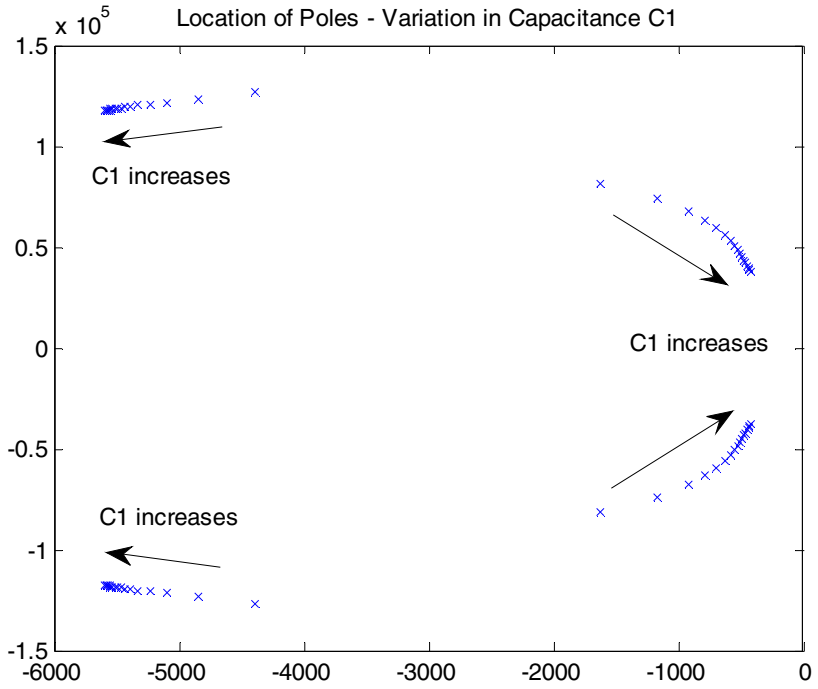


Figure 4.43 Validation of movement of poles for variation in capacitance C_1 - Negative half cycle

The value of C_2 is varied from 15 µF to 1000 µF. From Figure 4.44, the system has four zeros of which three are in the LHP and one in the RHP. The complex pair of zeros does not move for any change in value of C_2. The other zero in the LHP moves towards the RHP but never crosses into the RHP. From Figure 4.45, all the poles remain in the LHP. All poles move in the LHP towards the RHP but never cross into the RHP.

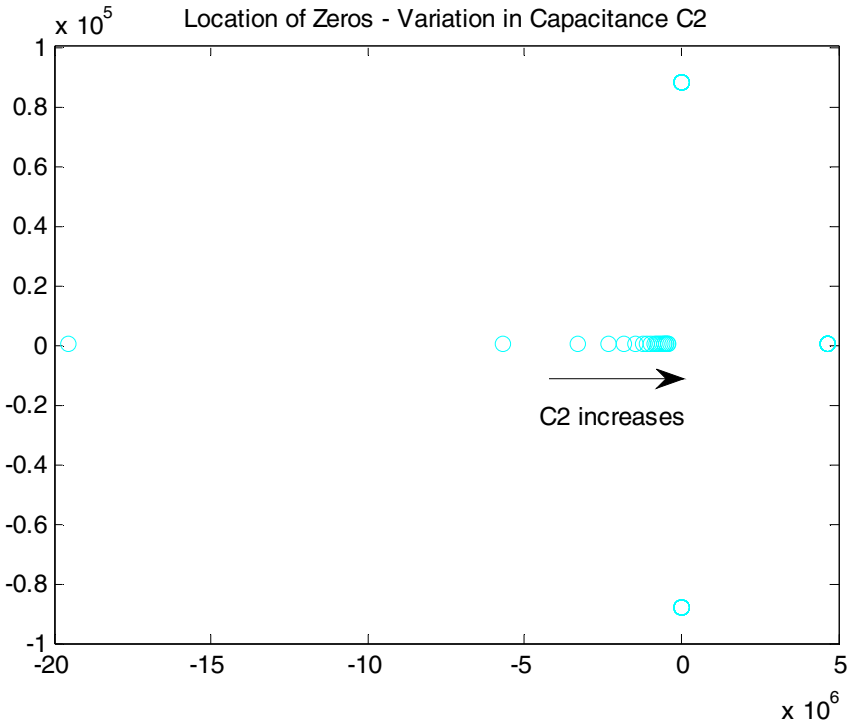


Figure 4.44 Validation of movement of zeros for variation in capacitance C_2 - Negative half cycle

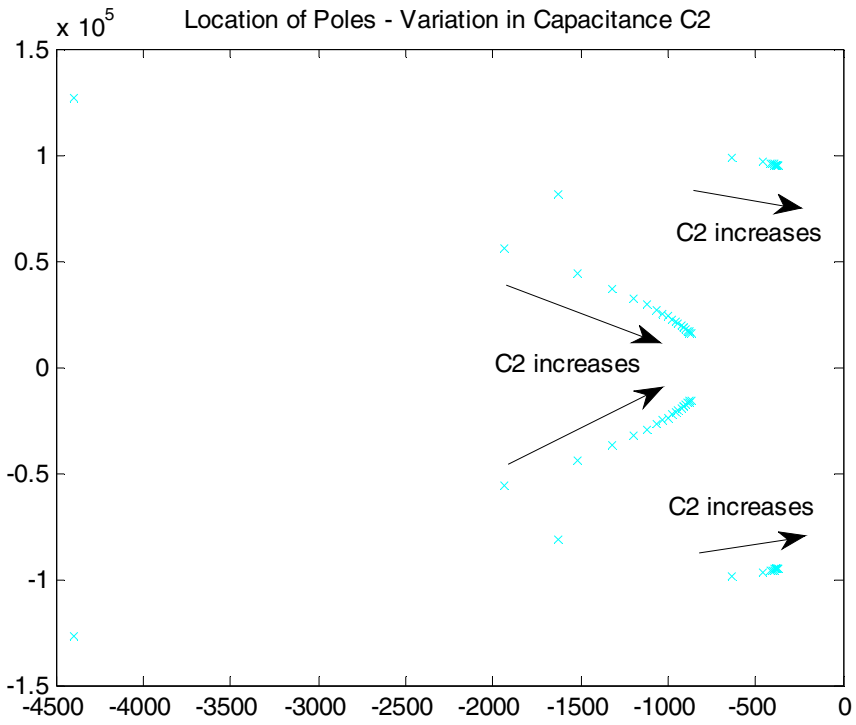


Figure 4.45 Validation of movement of poles for variation in capacitance C_2 - Negative half cycle

Figures 4.46 and 4.47 show the movement of zeros and poles of the system respectively. Duty is varied from 0.1 to 0.9 to cover buck and boost modes of operation. In buck mode i.e. for duty less than 0.5, the system has three zeros in the LHP and one zero in the RHP. As the duty is increased, the zero in the RHP moves along the real axis towards the LHP but never crosses over. When the duty is greater than 0.5, the complex pair of zero moves from the LHP to the RHP. As we increase the duty further, the complex pair of zero moves further into the RHP. The two complex pair of poles remains in the LHP at all times. When the duty is increased, one pair of poles moves deeper into the LHP while the other pair of poles moves towards the RHP.

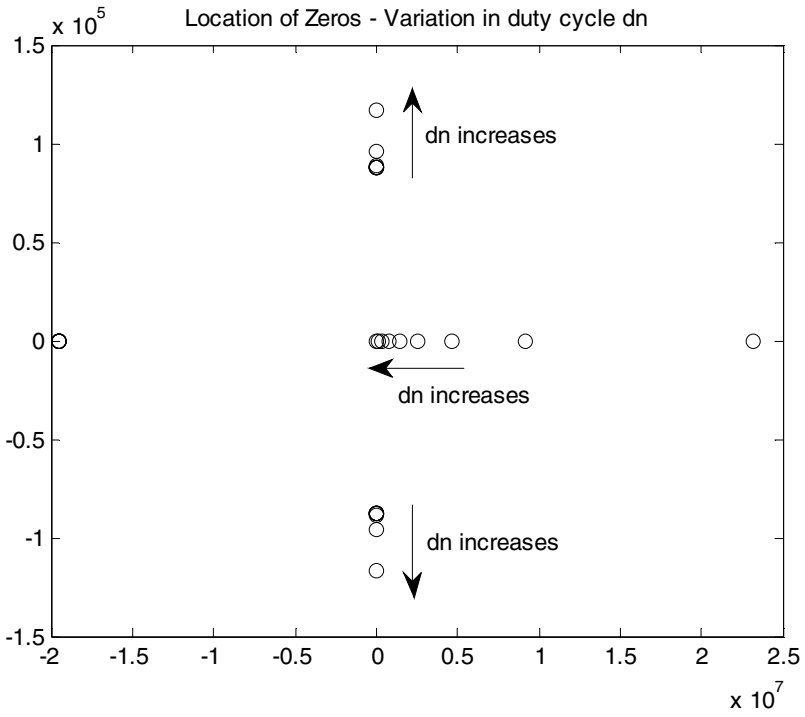


Figure 4.46 Validation of movement of zeros for variation in duty cycle dn - Negative half cycle

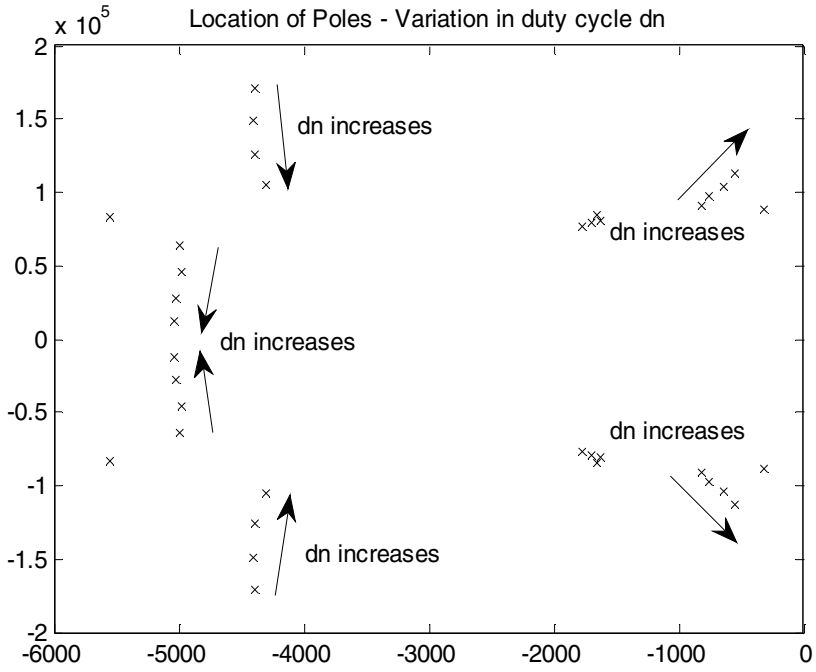


Figure 4.47 Validation of movement of poles for variation in duty cycle dn - Negative half cycle

4.5 Sizing Procedure

The sizing of the inductors and capacitors in the inverter is of great importance. For the purpose of designing the sizing procedure, the operation of the inverter in buck mode for positive and negative cycles is combined and the operation in boost mode for positive and negative cycles is combined. This results in two sets of values for the inductors and capacitors.

The design procedure is derived for a system to generate 110 V rms voltage and 10 A rms current in the output. This design would work for an output power of 110 – 1.1 KW for a power factor ranging from 0.1 to 1. The input voltage is assumed to be 34 V DC. The variation in input voltage is assumed to be from 24 – 44 V.

A. Buck Mode

In this mode, the output voltage is less than the input voltage i.e. the output voltage is assumed to be 20 V rms. When the inverter is operating in buck mode, the switching frequency of the transistor Q is assumed to be 10 KHz.

Equation (4.1) describes the relation between the output voltage and input voltage.

When the input voltage is 24 V i.e. $V_{gmin} = 24\ V$, the duty cycle is calculated as:

$$\frac{V_o}{V_{gmin}} = \frac{D_{max}}{1-D_{max}} = \frac{20\sqrt{2}}{24}$$

Solving the above equation, gives the value of $Dmax$ as 0.54.

When the input voltage is 44 V i.e. $V_{gmin} = 44\ V$, the duty cycle is calculated as:

$$\frac{V_o}{V_{gmax}} = \frac{D_{min}}{1-D_{min}} = \frac{20\sqrt{2}}{44}$$

Solving the above equation, gives the value of $Dmin$ as 0.39.

The allowed ripple in the inductor current can be assumed to be 30% of the input current, I_g. The input current can be found using the following relation:

$$I_g = \frac{D}{1-D} I_o. \tag{4.36}$$

For $Dmax = 0.54$, the input current is calculated as:

$$I_{gmax} = \frac{Dmax}{1-Dmax} I_o = \frac{0.54}{1-0.54} 10\sqrt{2} = 16.60\ A$$

For $Dmin = 0.39$, the input current is calculated as:

$$I_{gmax} = \frac{Dmin}{1-Dmin} I_o = \frac{0.39}{1-0.39} 10\sqrt{2} = 9.04\ A$$

When the switch Q is on, the inductor L_1 is charged by the input voltage source and L_2 is charged by the capacitor C_1. The inductors are charging in this mode. When the switch Q is off, the inductors L_1 and L_2 release the energy stored to the load.

The charging of inductors can be represented as an equation to determine the size of the inductors. Also, assuming that the inductors L_1 and L_2 are closely coupled, the ripple current is divided between them and thus the required inductance value is halved.

$$L_1 = L_2 \geq \frac{1}{2} \frac{D_{max} V_{gmin}}{\Delta I_L f_{sw}} \tag{4.37}$$

$$L_1 = L_2 \geq \frac{1}{2} \frac{0.54*24}{0.3*16.60*10000} = 130\ \mu H$$

The series coupling capacitor is charged by the input current when the switch Q is off. The equation describing the charging of the capacitor can be used to determine the critical capacitance required. The ripple voltage is assumed to be 5% of the input voltage.

$$C_1 \geq \frac{I_{gmax}(1-D_{max})}{\Delta V f_{sw}} \tag{4.38}$$

$$C_1 \geq \frac{16.06(1-0.54)}{0.05*44*10000} = 335.8\ \mu F$$

The output capacitor discharges to the load when the switch Q is on. This equation describing the discharge of the capacitor to the load can be used to determine the value of output capacitance required by the inverter. The ripple allowed is assumed to be 2 V.

$$C_2 \geq \frac{I_o D_{max}}{\Delta V f_{sw}} \tag{4.39}$$

$$C_2 \geq \frac{10\sqrt{2}*0.54}{2*10000} = 381.83\ \mu F$$

B. Boost Mode

In this mode, the output voltage is greater than the input voltage i.e. the output voltage is assumed to be 110 V rms. When the inverter is operating in boost mode, the switching frequency of the transistor Q is assumed to be 250 KHz.

From Equation (4.1), when the input voltage is 24 V i.e. $V_{gmin} = 24\ V$, the duty cycle is calculated as:

$$\frac{V_o}{V_{gmin}} = \frac{D_{max}}{1-D_{max}} = \frac{110\sqrt{2}}{24}$$

Solving the above equation, gives the value of $Dmax$ as 0.86.

When the input voltage is 44 V i.e. $V_{gmin} = 44\ V$, the duty cycle is calculated as:

$$\frac{V_o}{V_{gmax}} = \frac{D_{min}}{1-D_{min}} = \frac{110\sqrt{2}}{44}$$

Solving the above equation, gives the value of $Dmin$ as 0.78.

The allowed ripple in the inductor current can be assumed to be 30% of the input current, I_g. The input current can be calculated from Equation (4.36).

For $Dmax = 0.86$, the input current is calculated as:

$$I_{gmax} = \frac{Dmax}{1-Dmax} I_o = \frac{0.86}{1-0.86} 10\sqrt{2} = 91.63\ A$$

For $Dmin = 0.78$, the input current is calculated as:

$$I_{gmax} = \frac{Dmin}{1-Dmin} I_o = \frac{0.78}{1-0.78} 10\sqrt{2} = 49.98\ A$$

When the switch Q is on, the inductor L_1 is charged by the input voltage source and L_2 is charged by the capacitor C_1. The inductors are charging in this mode. When the switch Q is off, the inductors L_1 and L_2 release the energy stored to the load.

The charging of inductors can be represented as an equation to determine the size of the inductors. Also, assuming that the inductors L_1 and L_2 are closely coupled, the ripple current is divided between them and thus the required inductance value is halved. Similar to Equation (4.37),

$$L_1 = L_2 \geq \frac{1}{2} \frac{D_{max} V_{gmin}}{\Delta I_L f_{sw}}$$

$$L_1 = L_2 \geq \frac{1}{2} \frac{0.86*24}{0.3*91.63*250000} = 1.5\ \mu H$$

The series coupling capacitor is charged by the input current when the switch Q is off. The equation describing the charging of the capacitor can be used to determine the critical capacitance required. The ripple voltage is assumed to be 5% of the input voltage. Similar to Equation (4.38),

$$C_1 \geq \frac{I_{gmax}(1-D_{max})}{\Delta V f_{sw}}$$

$$C_1 \geq \frac{91.63(1-0.86)}{0.05*44*250000} = 22.27\ \mu F$$

The output capacitor discharges to the load when the switch Q is on. This equation describing the discharge of the capacitor to the load can be used to determine the value of output capacitance required by the inverter. The ripple allowed is assumed to be 2 V. Similar to Equation (4.39),

$$C_2 \geq \frac{I_o D_{max}}{\Delta V f_{sw}}$$

$$C_2 \geq \frac{10\sqrt{2}*0.86}{2*250000} = 17.35\ \mu F$$

The values of L and C obtained in this procedure are the critical values which should be used to maintain continuous conduction operation of the inverter. The value of L and C can be selected from either mode. If the values are selected from the buck mode, then the operating frequency for the boost mode is re-scaled using the equation of L_1 as the current through the inductor is more sensitive to changes in frequency than the voltage across the capacitors. Similarly, if the values are chosen from the boost mode, the operating frequency for the buck mode is re-scaled using the value of L_1.

4.6 Control of Single Switch Inverter

The new single switch inverter is introduced to generate a pure sinusoidal output voltage [37]. The system behaves like a non-minimum phase system in all operating ranges. When addressed from a control perspective, the right half plane zeros or the non-minimum phase zeros in the transfer function complicate the control design scheme [38], [39]. The response of such a system is characterized by undershoots and overshoots [40].

These systems can be controlled if they could be converted to minimum phase systems. Parallel feed-forward compensators can be used to convert any plant into a minimum phase system. Parallel compensators have been successfully implemented in [40]-[45] and are proven to be a more efficient way of controlling non-minimum phase systems compared to pole-zero cancellation techniques [46], [47]. For non-minimum phase systems, pole-zero cancellation can lead to having unstable structure of feedback controller. However, this method uses a compensator T(s) which is not a part of the plant but is derived to make the plant a minimum phase system.

The Dual Feed forward Predictive Control structure can be used to solve the tracking problem of a non-minimum phase system. In general the DFPC may provide perfect tracking for Biproper and strictly proper systems, Minimum and non-minimum phase systems [48].

In this case, the feed-forward controller is used to provide either the feed-forward prediction. The feed-forward controllers are based on the plant model [48]. The feedback controller is responsible for tracking reference signals. For perfect tracking, the reference

signal is divided into two signals namely a reference signal that can be inverted by the ballistic response and a prediction of the path that the plant output will follow based on the ballistic response. The feedback controller is designed to result in perfect tracking performance. A simple PI controller can be used for regulations. However, for reference tracking a gain adaptation is utilized to constantly tune the gains of the controller [49]-[52].

This method of feed-forward control is used to force the non-minimum phase system to behave like a minimum phase system. In this method, the plant is split into two parts to generate two signals. One signal is to make the plant track $r_{ff}(t)$ with a feed-forward control signal $u_{ff}(t)$ that drives the plant to track the reference signal. The signals produced by the feed-forward transfer functions are assumed to contain bounded energy and have no influence on the closed loop stability [48]. For perfect tracking, the error should reach zero which can be accomplished using various types of controller including a simple gain [40]. However, in the new inverter circuit, an adaptive PI controller is required to adjust the gains continuously. The block diagram, for the structure of a dual feed-forward predictive control (DFPC) is shown in Figure 4.48.

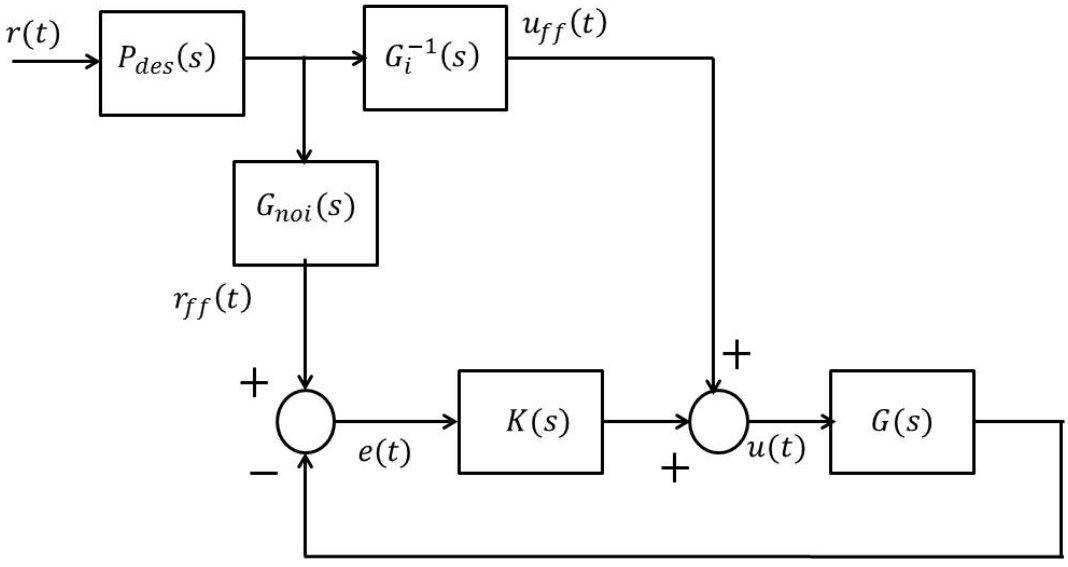


Figure 4.48 Block diagram of Dual Feed-forward Predictive Control

The stable and causal blocks $G_{noi}(s)$ and $G_i^{-1}(s)$ are the non–invertible and invertible parts of the plant. The non-invertible part refers to the non-minimum phase and unstable part of the plant where as the invertible part refers to the minimum phase and stable part of the plant. $P_{des}(s)$ is the design parameter that determines the reference signal and the feed-forward control signal. The conditions to be satisfied by the design parameter are:

1. The steady state gain from $r(t)$ to $r_{ff}(t)$ must be unity gain i.e. $P_{des}(0)G_{noi}(0) = 1.$
2. The feed-forward transfer functions: $FF1 = P_{des}(s)G_{noi}(s)\& \; FF2 = P_{des}(s)G_i^{-1}(s)$ must be proper (i.e. number of zeros are less than or equal to number of poles).

The first condition is required so that the steady state reference equals the actual reference: $r_{ff}(t) = r(t)$. The second condition is required to make the feed-forward controller realizable from the hardware point of view. The conclusion drawn from the second condition is that $P_{des}(s)$is stable and the relative degree of $P_{des}(s)$ is greater than or equal to the relative degree of $G_i(s)$.

Also, the controller $K(s)$ should be designed to guarantee internal stability. The nominal tracking requirements are satisfied by the feed-forward paths and the feedback controller focuses on correcting model inaccuracies and disturbance rejection.

In particular, $\mathrm{P_{des}(s)G_{noi}(s)}$ determines the class of signal that has to be perfectly tracked and $\mathrm{P_{des}(s)G_i^{-1}(s)}$ determines the associated feed-forward control signal to achieve perfect tracking. Consider the plant to have a transfer function as follows:

$$G(s) = \frac{K_{DC}N_{mp}(s)N_{nmp}(s)}{D_s(s)D_u(s)}$$

where K_{DC} is the DC gain of the system, $\mathrm{N_{mp}(s)}$ is the minimum phase polynomial of the numerator while$\mathrm{N_{nmp}(s)}$ is the non-minimum phase polynomial of the numerator of the transfer function. $\mathrm{D_s(s)}$ is the stable denominator polynomial and $\mathrm{D_u(s)}$ is the unstable denominator polynomial.

The transfer function is decomposed into two parts: $G_i(s)$ and $G_{noi}(s)$. $G_i(s)$contains the minimum phase numerator polynomial and the denominator polynomial and $G_{noi}(s)$ contains the non-minimum phase numerator polynomial.

$$G_i(s) = \frac{K_{DC}N_{mp}(s)}{D_s(s)D_u(s)} \quad \text{and} \quad G_{noi}(s) = N_{nmp}(s)$$

It is to be noted that the transfer functions $G_i(s)$ and $G_{noi}(s)$ are not proper and cannot be realized as individual systems. This leads to the selection of the design parameter $P_{des}(s)$ such that the feed-forward transfer functions FF1 and FF2 are proper and realizable.

The control effort is a sum of the feed-forward control signal obtained at the output of the block ${G_i}^{-1}(s)$ and the feedback control signal obtained at the output of $K(s)$.

The feedback controller needs to be designed to provide zero tracking error. In some cases, a simple gain or simple PI controller can be very effective [40]. However, PI controllers give best results when the goal of control is regulation. Also, using a simple PI controller needs tuning of the gains offline. In our case, the signal to be tracked is continuously varying (sine wave) and thus an adaptive PI controller structure was considered suitable. Also, the gains of adaptive controller are tuned automatically online [42]. Any change in the control objectives or change in the plant parameters can be compensated by using online tuning of the gains of the controller [53].

The self-tuning PI controller is viewed as a non-linear controller as the gains K_p and K_i are varying continuously. It is not necessary for the gains to converge to a constant value as the gains may keep varying as the reference signal needed to track varies.

The equations for the proportional gain K_p and integral gain K_i are obtained from [53] as:

$$\begin{cases} \dot{K_p} = -\gamma e y_1 \\ \dot{K_i} = -\gamma e y_2 \end{cases} \tag{4.40}$$

where $\gamma > 0$ is the adaption gain, e is the error between the plant output and the reference input, y_1 is the output of the proportional block and y_2 is the output of the integral block of the controller.

A. Buck Operation

When the inverter operates in buck mode to produce positive cycle of output voltage, the control to output transfer function has non-minimum phase behavior. The system has four zeros of which three are in LHP and one zero in RHP.

For buck operation with duty cycle as 30%, and the following parameters: $L_1 = 1\mu H$, $L_2 = 25\mu H$, $C_1 = 1\mu F$, $C_2 = 75mF$ and $R = 5$, the control to output transfer function is determined as follows:

$$G_d^v(s) = \frac{(-s + 84.98)(s^3 + 0.0853s^2 + 3.8475s + 0.2050)}{s^4 + 0.0398s^3 + 49.3610s^2 + 0.1283s + 0.0026}$$

The transfer function is decomposed as follows:

$$G_{mp}(s) = \frac{s^3+0.0853s^2+3.8475s+0.2050}{s^4+0.0398s^3+49.3610s^2+0.1283s+0.0026}$$

$$G_{nmp}(s) = (-s + 84.98)$$

The minimum phase part is the stably and causally invertible G_i and the non-minimum phase part is considered to be causally non-invertible G_{noi}.

$$G_i^{-1}(s) = \frac{s^4 + 0.0398s^3 + 49.3610s^2 + 0.1283s + 0.0026}{s^3 + 0.0853s^2 + 3.8475s + 0.2050}$$

$$G_{noi}(s) = (-s + 84.98)$$

Following the design requirements for the choice of $P_{des}(s)$ the relative degree of $P_{des}(s)$ is chosen to be equal to 1 and has the structure as $P_{des}(s) = \frac{k}{\alpha s+1}$, where α is varied to determine a suitable response in terms of the settling time and undershoot associated with the non-minimum phase zero.

In addition, where $G_{noi}(0) = 84.98$ yields $P_{des}(0) = k = 84.98^{-1}$

Thus, $P_{des}(s) = \frac{84.98^{-1}}{\alpha s+1}$

The presence of right half plane (RHP) zero means that the step response will have an undershoot that is related to the value of α. The value of α is determined such that the undershoot is reduced and the response is fast. It is a trade-off between the undershoot and the response time. For smaller values of α, the response is fast but the undershoot is larger and for larger values of α, the undershoot is less but the response is slower [47]. The step response of this system is shown in Figure 4.49 for various values of α. The response for $\alpha = 5$ is chosen to give the best result.

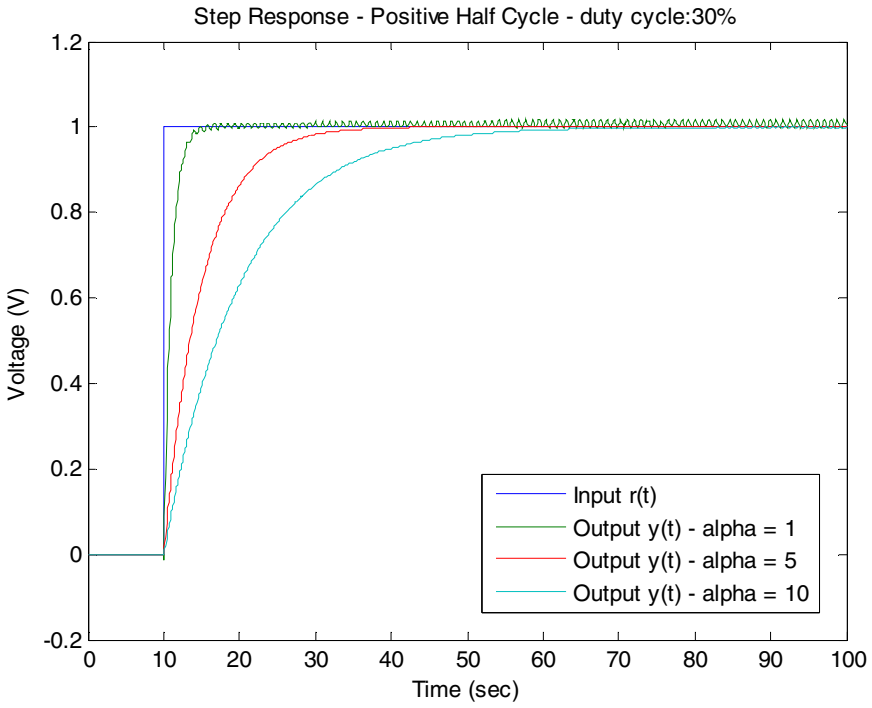


Figure 4.49 Step Response of system for positive half cycle for duty cycle of 30%

When the inverter operates in buck mode to produce negative cycle of output voltage, the control to output transfer function has minimum phase behavior. The system has three zeros in the RHP and one zero in the LHP which is associated to the value of C_2.

For operation with duty cycle as 30%, the control to output transfer function is determined as follows:

$$G_d^v(s) = \frac{(s+1.373)(-s^3+79.73s^2-104.433s+12.6479)}{s^4+0.0398s^3+49.3610s^2+0.1283s+0.0026}$$

The transfer function is decomposed as follows:

$$G_{mp}(s) = \frac{s+1.373}{s^4+0.0398s^3+49.3610s^2+0.1283s+0.0026}$$

$$G_{nmp}(s) = (-s^3+79.73s^2-104.433s+12.6479)$$

The minimum phase part is the stably and causally invertible G_i and the non-minimum phase part is considered to be causally non-invertibleG_{noi}.

$${G_i}^{-1}(s) = \frac{s^4+0.0398s^3+49.3610s^2+0.1283s+0.0026}{s+1.373}$$

$$G_{nmp}(s) = (-s^3+79.73s^2-104.433s+12.6479).$$

The relative degree of $P_{des}(s)$ is required to be greater than or equal to the relative degree of $G_i(s)$. Since the relative degree of $G_i(s)$ is three, the relative degree of $P_{des}(s)$ is assumed to be three.

$$P_{des}(s) = \frac{k}{(\alpha s+1)^3}$$

In addition, $G_{noi}(0) = 12.6479$ and thus $P_{des}(0) = k = 12.6479^{-1}$, Therefore,

$$P_{des}(s) = \frac{12.6479^{-1}}{(\alpha s+1)^3}$$

The value of α is determined from the step response of the system operating to produce negative peak as shown in Figure 4.50. The value of α is selected such that the

overshoot and settling time are not very large. From Figure 4.50, it is seen that the undershoot is largest for $\alpha = 1$ and the settling time is highest for $\alpha = 10$. When $\alpha = 5$, the undershoot and settling time are best suited.

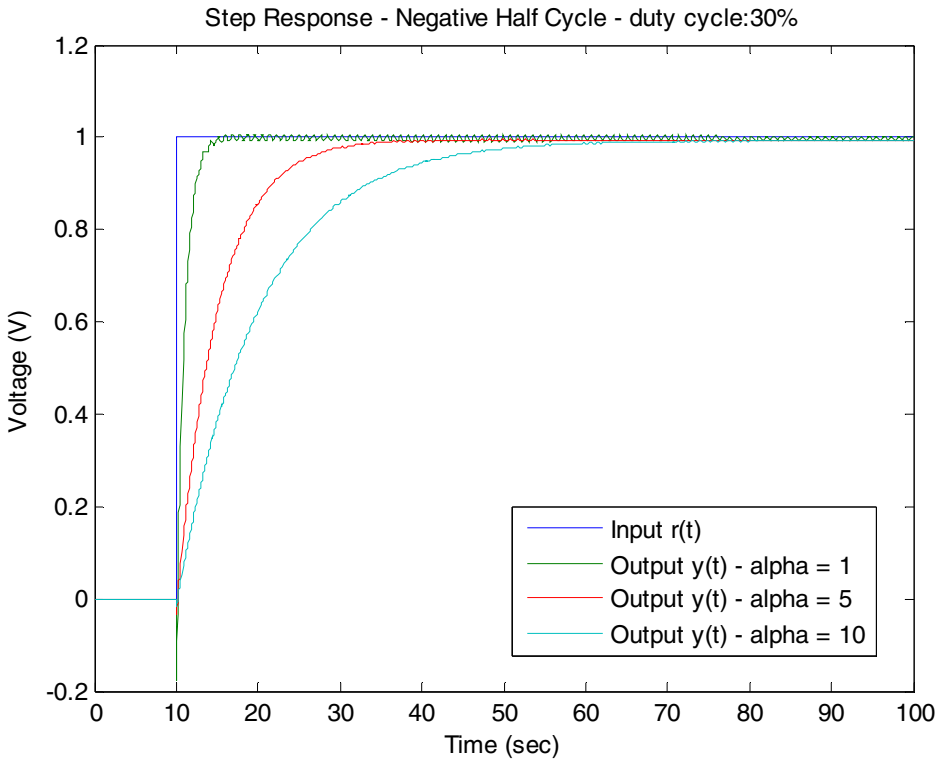


Figure 4.50 Step Response of system for negative half cycle for duty cycle of 30%

The system when operating to produce a complete cycle for duty cycle of 30% was simulated using the DFPC control and adaptive PI. Figure 4.51 shows the tracking of the plant output. The plant output follows the reference signal exactly at every instant of time. The output of the plant was made to track the reference signal exactly.

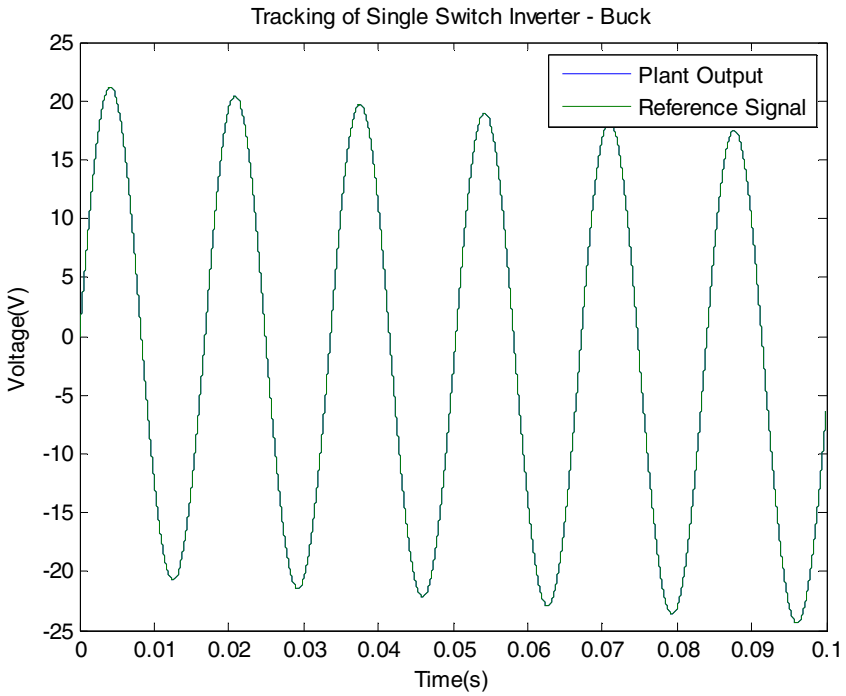


Figure 4.51 Perfect tracking for inverter operation with duty of 30%

B. Boost Operation

When the inverter operates in boost mode to produce positive cycle of output voltage, the control to output transfer function has non-minimum phase behavior.

For boost operation with duty cycle as 70% and the following parameters:$L_1 = 1\mu H$, $L_2 = 25\mu H$, $C_1 = 1\mu F$, $C_2 = 75mF$ and $R = 5$, the control to output transfer function is determined as follows:

$$G_d^v(s) = \frac{(-s + 6.8207)(s^3 + 0.1969s^2 + 3.7752s + 0.2008)}{s^4 + 0.0236s^3 + 10.96s^2 + 0.0701s + 0.0005}$$

The transfer function is decomposed as follows:

$$G_{mp}(s) = \frac{s^3+0.1969s^2+3.7752s+0.2008}{s^4+0.0236s^3+10.96s^2+0.0701s+0.0005}$$

$$G_{\ nmp}(s) = (-s + 6.8207)$$

The minimum phase part is the stable and causally invertible part G_i and the non-minimum phase part is considered to be causally non-invertible part G_{noi}.

$$G_i{}^{-1}(s) = \frac{s^4 + 0.0236s^3 + 10.96s^2 + 0.0701s + 0.0005}{s^3 + 0.1969s^2 + 3.7752s + 0.2008}$$

$$G_{noi}(s) = (-s + 6.8207)$$

The design parameter $P_{des}(s)$ is found to have the structure as

$$P_{des}(s) = \frac{k}{\alpha s + 1}$$

In addition, $G_{noi}(0) = 6.2520$ and thus $P_{des}(0) = k = 6.8207^{-1}$

Therefore,

$$P_{des}(s) = \frac{6.8207^{-1}}{\alpha s + 1}$$

The value of α is determined from the step response of the system. The trade-off leads to selection of $\alpha = 5$. The step response of the system is shown in Figure 4.52.

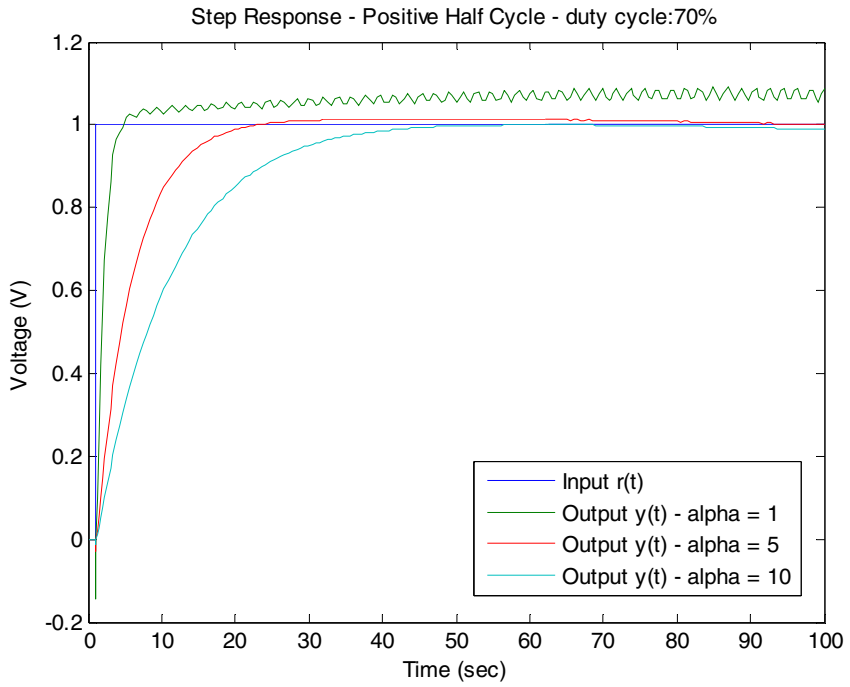


Figure 4.52 Step Response of system for positive half cycle for duty cycle of 70%

From Figure 4.52, it can be seen that for value α=1, the undershoot is large while the time taken for the response to settle is very small. For $\alpha = 10$, the undershoot is small but the response time is very large. The best response can be obtained for $\alpha = 5$.

When the inverter operates in boost mode to produce negative cycle of output voltage, the control to output transfer function has non-minimum phase behavior.

For operation with duty cycle as 70%, the control to output transfer function is determined as follows:

$$G_d^v(s) = \frac{(-s + 6.2520)(s^3 + 0.1433s^2 + 1.6553s + 0.2191)}{s^4 + 0.0236s^3 + 10.96s^2 + 0.0701s + 0.0005}$$

The transfer function is decomposed as follows:

$$G_{mp}(s) = \frac{s^3+0.1433s^2+1.6553s+0.2191}{s^4+0.0236s^3+10.96s^2+0.0701s+0.0005}$$

$$G_{\ nmp}(s) = (-s + 6.2520)$$

The minimum phase part is the stably and causally invertible G_i and the non-minimum phase part is considered to be causally non-invertible G_{noi}.

$$G_i^{-1}(s) = \frac{s^4+0.0236s^3+10.96s^2+0.0701s+0.0005}{s^3+0.1433s^2+1.6553s+0.2191},$$

$$G_{noi}(s) = (-s + 6.2520).$$

The structure of $P_{des}(s)$ is selected to be as follows:

$$P_{des}(s) = \frac{k}{\alpha s + 1}$$

Considering, $G_{noi}(0) = 0.0009$ and thus $P_{des}(0) = k = 6.2520^{-1}$

Therefore,

$$P_{des}(s) = \frac{6.2520^{-1}}{\alpha s + 1}$$

The value of α is determined from the step response of the system as shown in Figure 4.53. The value of α which gives the best trade-off is selected. When $\alpha = 1$, there is some steady state error in the step response. Thus, it is not desirable to consider this value of α. For α being 5 and 10, the undershoot is reduced, however the settling time for $\alpha = 5$ is more desirable than for $\alpha = 10$.

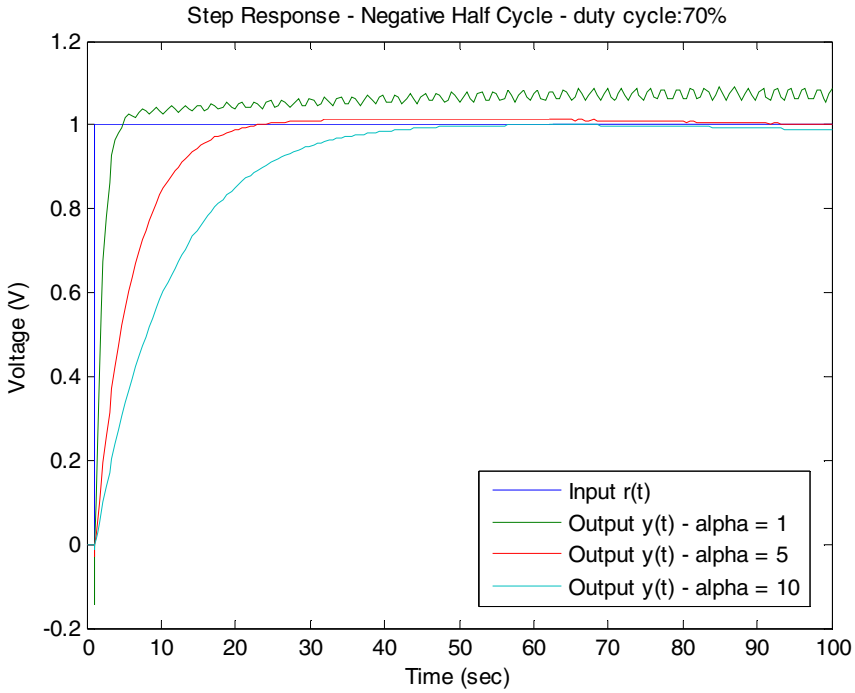


Figure 4.53 Step Response of system for negative half cycle for duty cycle of 70%

The simulation result for perfect tracking of this system when operating to boost the input voltage with duty cycle of 70% is shown in Figure 4.54.

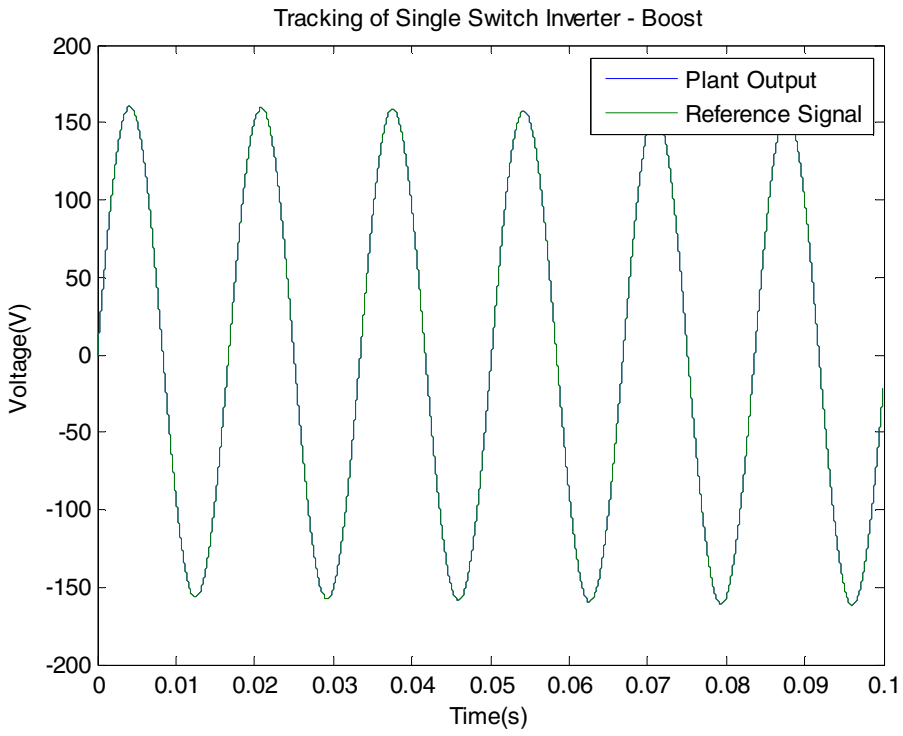


Figure 4.54 Perfect tracking for inverter operation with duty of 70%

A single structure of feedback controller was designed for the inverter operating to produce positive and negative half cycles. An adaptive PI controller was selected and designed using MATLAB/SIMULINK. The gains of the controller were taken from Equation (4.40).

CHAPTER 5. DISCUSSIONS

5.1 Simulation Results

The solar panel is designed with the following parameters: V_{oc} 42 V, $I_{sc} = 6.3\ A, V_m = 34\ V, I_m = 5.5\ A$. The P-V and I-V characteristics of the solar panel are shown in Figures 3.2 and 3.3.

The perturb and observe method for MPPT is used and Figure 5.1 shows the results the maximum power tracking of the solar panel.

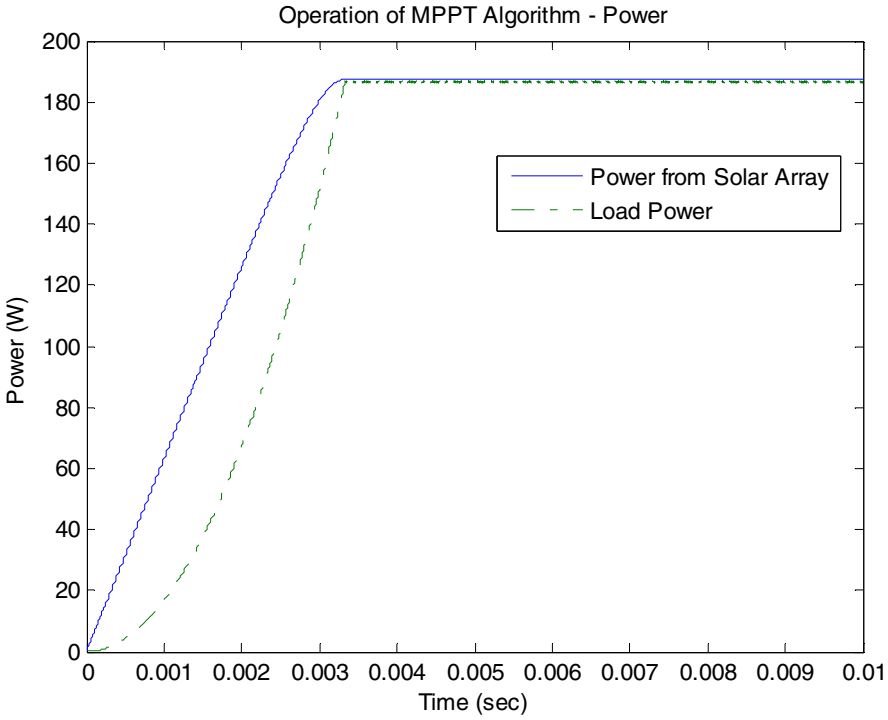


Figure 5.1 Constant power (maximum) generation by the MPPT algorithm

In this case, the MPPT algorithm is used to generate a reference voltage level instead of duty cycle. Figure 5.2 shows the constant voltage reference which is tracked by the MPPT algorithm. The SEPIC inverter uses this voltage as input voltage.

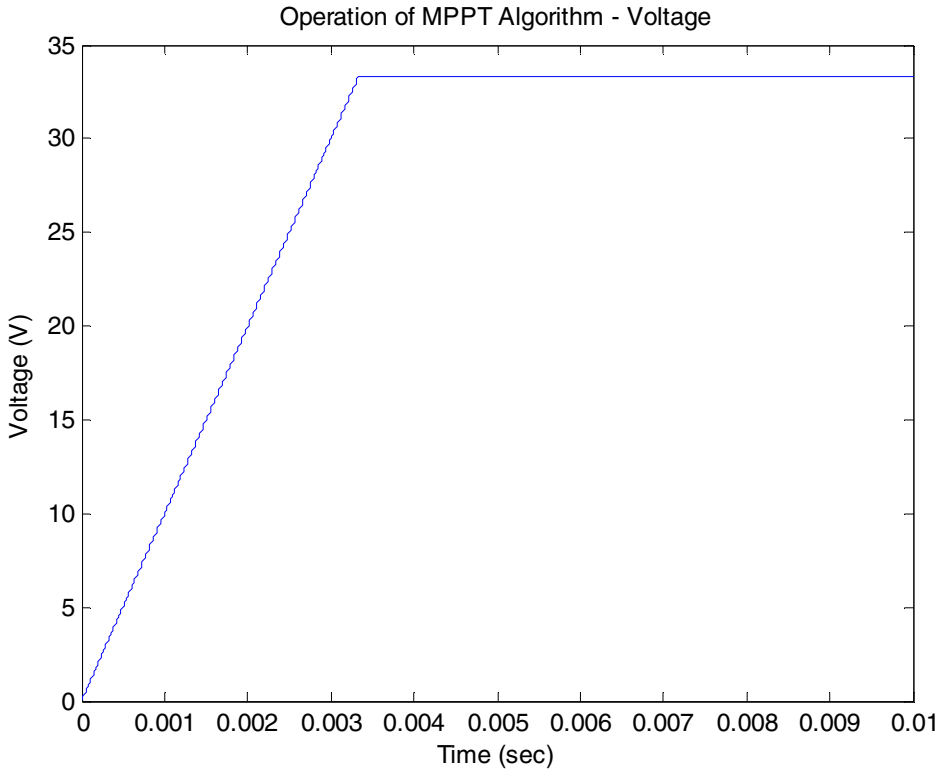


Figure 5.2 Constant voltage generation by the MPPT algorithm

Figure 5.3 presents the simulation results to validate the operation of the new SEPIC based inverter. The SimPowerSystems toolbox of MATLAB is used to simulate the inverter. For the simulation of the SEPIC based inverter, the following parameters are used: $L_1 = 0.6$ µH, $L_2 = 5$ µH, $C_1 = 1$ µF, $C_2 = 650$ µF. The load is of inductive nature with $R = 3$ ohm and $L = 10$ mH.

In mode I, the current through the inductor L_1 and voltage across capacitors $C_1$and C_2 rise with positive amplitude. In this mode, the current through the inductor L_2 becomes negative. In mode II, the voltages and currents reach a point of stable operation. The transition from positive peak to negative peak occurs in mode III. In mode IV, the current

through the inductor L_2 becomes positive as the output voltage becomes negative. In this mode, the current through the inductor L_1 and voltage across capacitor C_1 are positive.

The value of inductor L_1 is chosen so as to have continuous conduction i.e. the current through the inductor L_1 never falls to zero. The current through the inductor L_2 is negative for positive cycle of output voltage and is positive for negative cycle of output voltage. The voltage across the capacitor C_1 remains positive. The voltage across the capacitor C_2 is the output of the SEPIC inverter.

A switching between modes I and II generates stable operation of positive peak voltage and modes of III and IV generate a negative peak voltage. Figure 5.3 shows the sinusoidal voltage generated by the SEPIC based inverter.

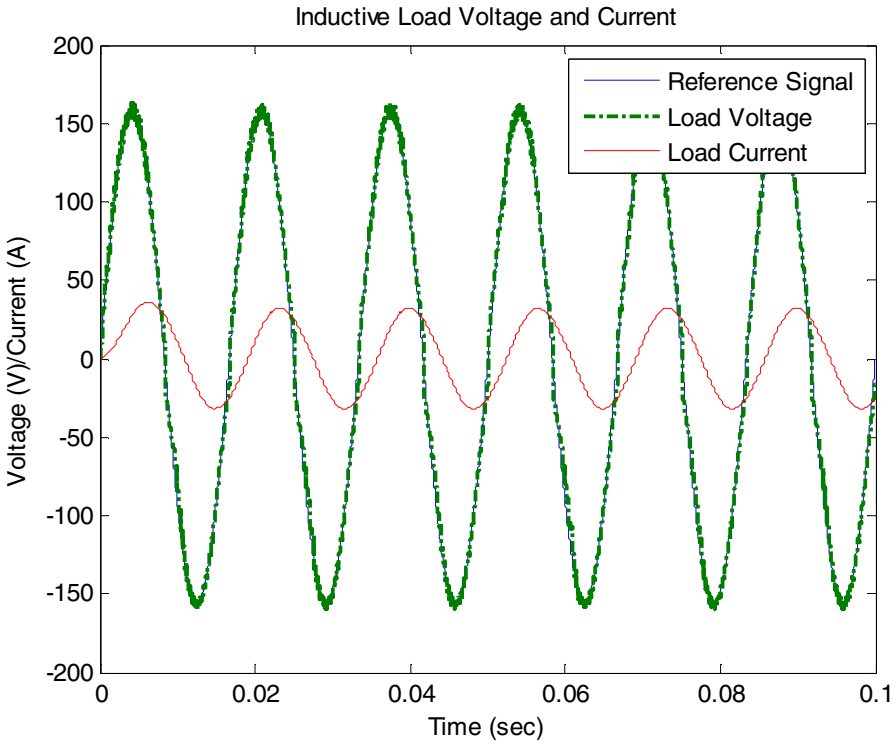


Figure 5.3 Load voltage and current of SEPIC based inverter

For the micro-inverter, the PV solar module is connected to the SEPIC based inverter. The MPPT algorithm is applied to the PV solar panel model. The output of the solar panel is connected to the input of the inverter. A capacitor is connected at the input

terminals of the inverter to maintain steady voltage. While the MPPT algorithm ensures that the output voltage corresponds to the MPP, the inverter converts the dc voltage of the solar panel into ac voltage. The output of the micro-inverter is shown in Figure 5.4. The maximum power from the PV panel is 187 W and the output power of the SEPIC based inverter is 180 W.

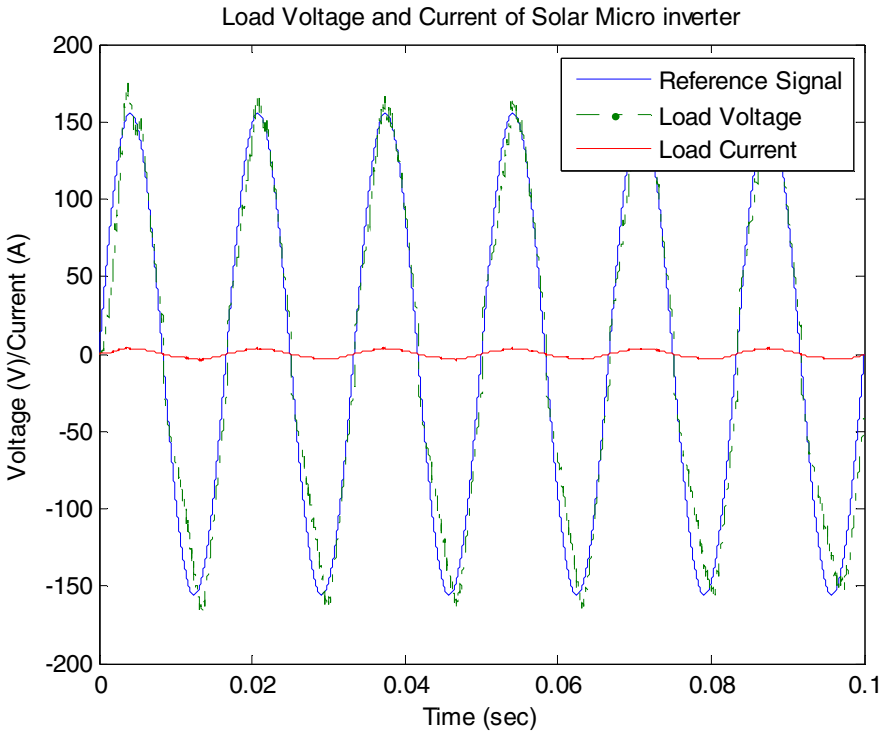


Figure 5.4 Load voltage and current of the Solar Micro-inverter

5.2 Experimental Results

Experiments were carried out on the SEPIC inverter. It is observed from simulations that the inverter operation is sensitive to the choice of inductors. The effect of the different values of inductors is studied. The inductance L_1 and L_2 are varied one at a time and the effect of these changes are noted on the output voltage, output current and input current drawn by the inverter.

Firstly, the inductance L_1 is varied while the other components have fixed values. While inductance L_1 is varied from 2.5 µH to 1 mH, the other components used are:

$L_2 = 3\,mH$, $C_1 = 3\,\mu F$ and $C_2 = 70\mu F$. The dc source used is a 12V battery. The switching frequency of the main transistor, Q; input voltage and current and output voltage are tabulated in Table 5.1.

Table 5.1 Effect of Variation of L_1

Inductance, L_1 (μH)	Frequency (KHz)	Input Voltage (V)	Input Current (A)	RMS Output Voltage (V)
2.5	50	12	4.32	30
11.2	45	12	3.62	37
100	40	12	1.95	39
285	30	12	1.4	40
1000	20	12	1.25	44

Selecting lower values of inductance L_1 needs increase in the switching frequency of the transistor, Q. The transistor used in the setup, limits the working frequency of the inverter. For lower values of L_1 like 2.5 μH, the working range of frequency is 60-70 KHz, which is not in the working range of the transistor, Q. This leads to higher current being drawn by the inductor L_1 from the battery.

From Table 5.1, it can be seen that for lower values of L_1 the output voltage is reduced while the input current is increased. The reason is the mismatch in the inductance L_1 and the switching frequency. Also, lower switching frequency is better operating condition as the switching losses are lower and the heat generated by the transistor, Q is less which means less effort is required for cooling. Figure 5.5 and 5.6 show the output voltage of the inverter without controller plotted against a reference sine wave signal. The output voltage of the inverter can be made to follow the reference signal if active control is implemented. Also, the positive and negative cycles are not symmetric because the inverter output is limited in boost mode. From Figures 5.5 and 5.6, the ripple in the negative peak increases for lower values of L_1. Also, as the value of L_1 is increased, the negative peak is reduced.

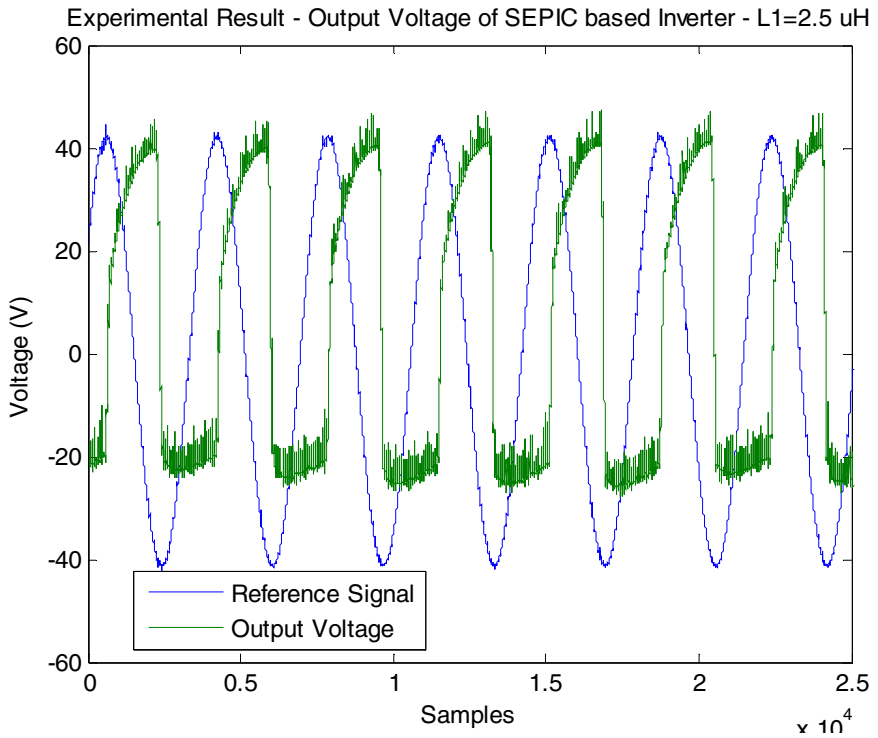


Figure 5.5 Experimental Result of Output Voltage of SEPIC Inverter when L_1=2.5 µH

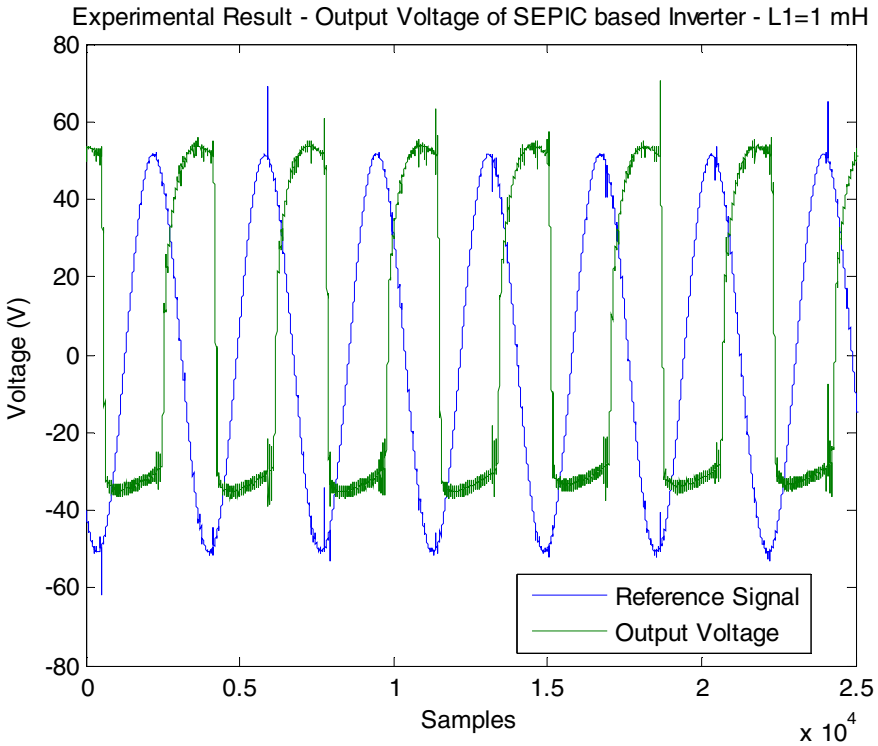


Figure 5.6 Experimental Result of Output Voltage of SEPIC Inverter when L_1=1 mH

The inductance L_1 is varied while the other components have fixed values. While inductance L_2 is varied from 100 µH to 7 mH, the other components used are: $L_1 = 100$ µH, $C_1 = 3$ µF and $C_2 = 70$µF. The switching frequency of the main transistor, Q; input voltage and current and output voltage are tabulated in Table 5.2.

Table 5.2 Effect of Variation of L_2

Inductance, L_2 (µH)	Frequency (KHz)	Input Voltage (V)	Input Current (A)	RMS Output Voltage (V)
100	40	12	1.79	30
285	40	12	1.44	35
1000	40	12	1.45	38
4000	40	12	1.62	32
7000	40	12	1.64	30

From simulations, it was observed that the inductance L_2 should be equal or greater than the inductance L_1. The range was chosen from 100 µH to 7 mH. In this case, changing the switching frequency of the transistor, Q with the change in inductance L_2 did not improve the output of the inverter. If frequency was reduced to 20 KHz when L_2 is 4 mH, the negative peak was distorted, while if the frequency was increased to 50 KHz when L_2 is 100 µH, it did not reflect any change in the input current or output voltage. So, the switching frequency was maintained consistent at 40 KHz which gives best results.

From Table 5.2, it is seen that the input current and the output voltage increase as the inductance L_2 is increased from 100 µH till 1 mH. As we go for higher inductance values for L_2, the input current increases slightly while the output voltage drops. From Figures 5.7 and 5.8, the positive peak is slightly higher when L_2 is 1 mH. From Figure 5.9, as the value of inductance L_2 is increased to very large values, the negative peak is reduced by 10V. The value of L_2 is best in the range of 1-3 mH from the results for variations in L_1 and L_2. It can be seen from Figures 5.6 and 5.8, that the matching of inductor sizes and frequency is very important to reduce the ripple in the output. The difference is size of L_2 in Figures 5.6 and 5.8 is 2 mH, but the ripple is significantly reduced when L_2 is 3 mH.

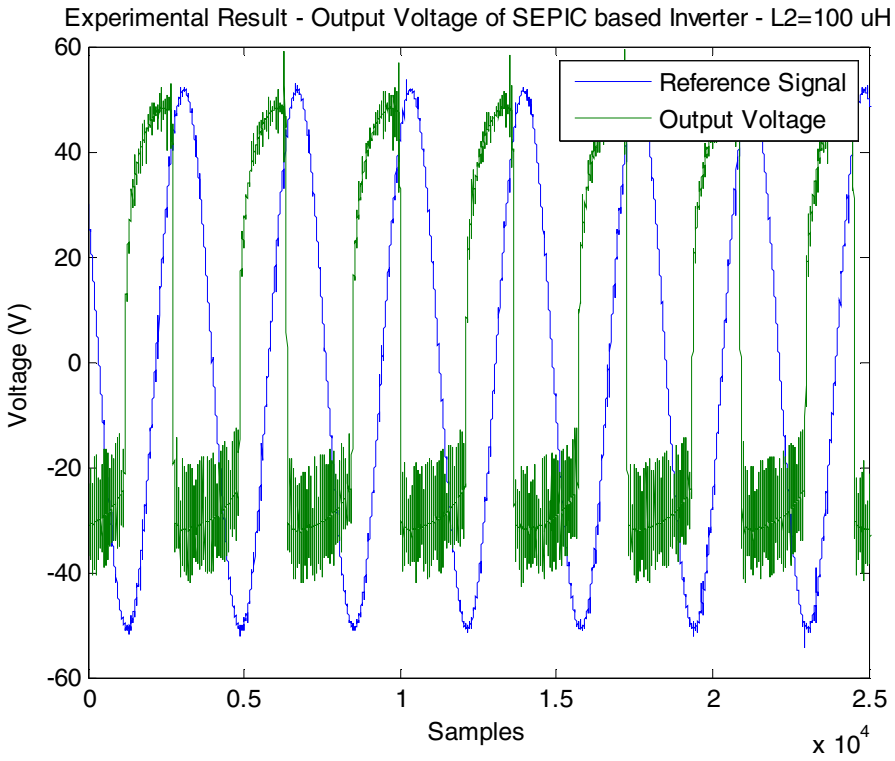


Figure 5.7 Experimental Result of Output Voltage of SEPIC Inverter when L_2=100 µH

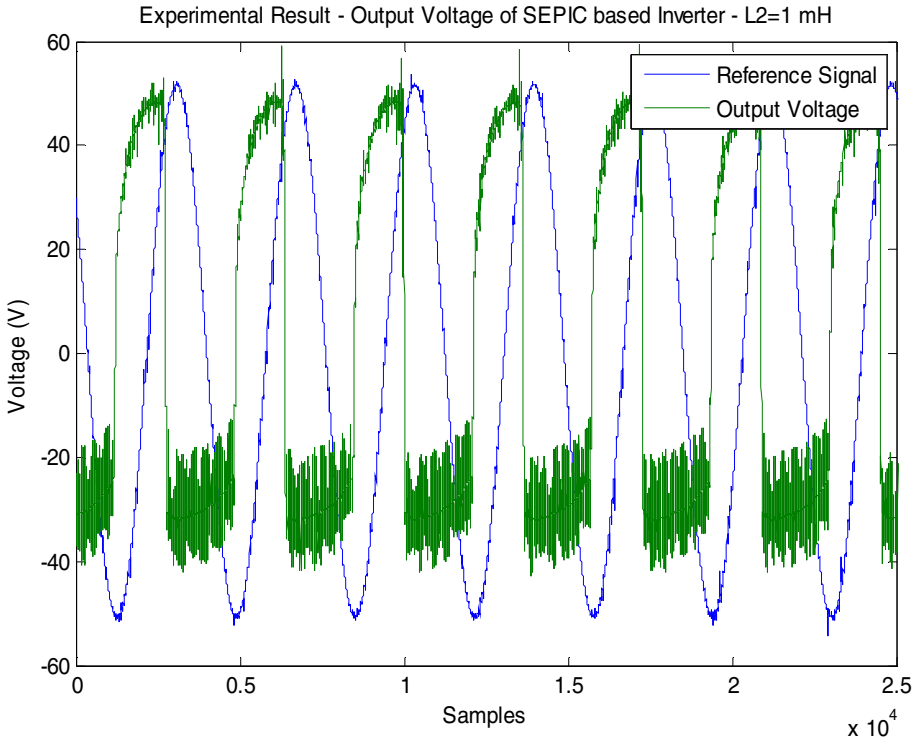


Figure 5.8 Experimental Result of Output Voltage of SEPIC Inverter when L_2=1 mH

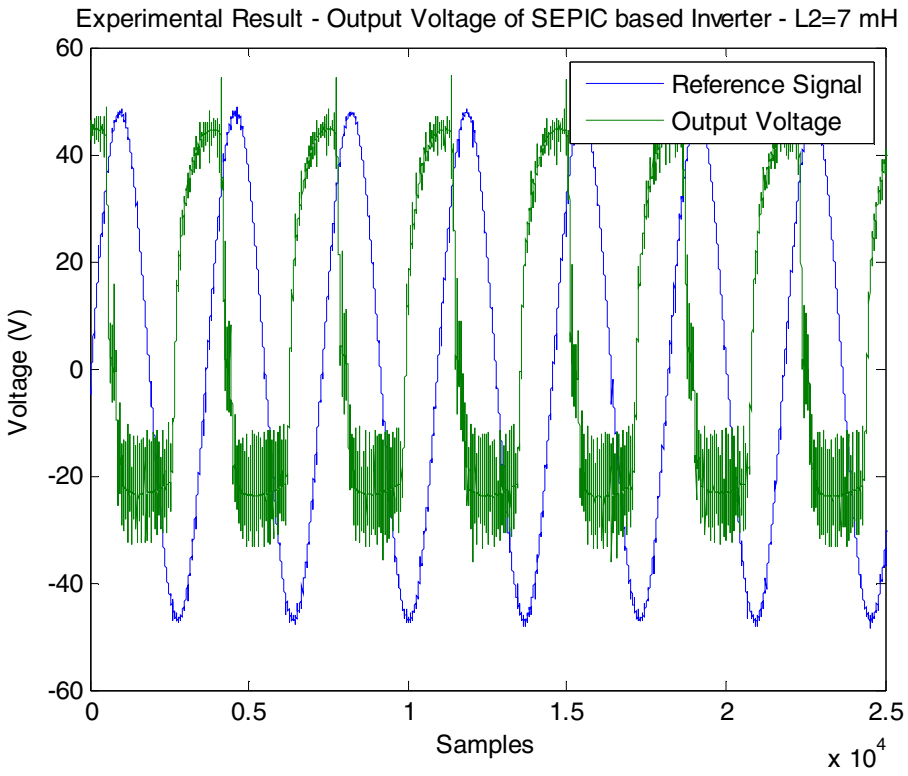


Figure 5.9 Experimental Result of Output Voltage of SEPIC Inverter when L_2=7 mH

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APPENDIX

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$$S_{11} = -\frac{1}{\alpha}\left(k_p + k_n\right)\left[\frac{k_p d_p - k_n d_n}{k_p(1-d_p)+k_n(1-d_n)}\right]$$

$$S_{21} = -\frac{1}{\alpha}\left(k_p + k_n\right) \mathrm{R}$$

$$S_{31} = \frac{\beta}{\alpha}\frac{(k_p+k_n)}{R+r_{C2}}$$

$$S_{41} = -\frac{1}{\alpha}\left[k_p(1-d_p) + k_n(1-d_n) + \frac{(k_p d_p - k_n d_n)\left(k_p(1-d_p)-k_n(1-d_n)\right)}{k_p(1-d_p)+k_n(1-d_n)}\right]R$$

Where,

$$\alpha = \left[\frac{-(k_p+k_n)(k_p d_p - k_n d_n)}{k_p(1-d_p)+k_n(1-d_n)}(Rr_{L1} + r_{L1}r_{C2}) - \left(k_p d_p - k_n d_n\right)(Rr_{C1} + r_{C1}r_{C2} + Rr_{C2}) + \right.$$

$$2Rr_{C2}\left(k_n(1-d_n) - k_p(1-d_p)\right) + \frac{(k_p+k_n)\left(k_p(1-d_p)+k_n(1-d_n)\right)}{k_p d_p - k_n d_n}(Rr_{L2} + r_{L2}r_{C2}) -$$

$$\frac{\left(k_p(1-d_p)+k_n(1-d_n)\right)^3}{(k_p+k_n)(k_p d_p - k_n d_n)}R^2 - \frac{2((k_p(1-d_p))^2-(k_n(1-d_n))^2)}{(k_p+k_n)}R^2 -$$

$$\left.\frac{(k_p d_p - k_n d_n)\left(k_p(1-d_p)-k_n(1-d_n)\right)^2}{(k_p+k_n)\left(k_p(1-d_p)+k_n(1-d_n)\right)}R^2\right]$$

$$\beta = \left[\left(\frac{k_n(1-d_n)-k_p(1-d_p)}{k_p(1-d_p)+k_n(1-d_n)} - \frac{k_p(1-d_p)+k_n(1-d_n)}{k_p d_p - k_n d_n}\right)Rr_{C2} - \frac{k_p+k_n}{k_p d_p - k_n d_n}(Rr_{L2} + r_{L2}r_{C2}) -\right.$$

$$\left.\frac{k_p d_p + k_n d_n}{k_p d_p - k_n d_n}(Rr_{C1} + r_{C1}r_{C2}) - \left(\frac{\left(k_p(1-d_p)+k_n(1-d_n)\right)^2}{(k_p+k_n)(k_p d_p - k_n d_n)} + \frac{k_p(1-d_p)-k_n(1-d_n)}{k_p+k_n}\right)R^2\right]$$