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Advanced Graphene Microelectronic Devices

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ADVANCED GRAPHENE MICROELECTRONIC DEVICES

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2016

To: Interim Dean Ranu Jung
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This dissertation, written by Chowdhury G. Al-Amin, and entitled Advanced Graphene Microelectronic Devices, having been approved in respect to style and intellectual content, is referred to you for judgment.

We have read this dissertation and recommended that it be approved.

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Date of Defense: March 31, 2016

The dissertation of Chowdhury G. Al-Amin is approved.

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and Dean of the University Graduate School

Florida International University, 2016

DEDICATION

I dedicate this thesis to my family. Without their patience, understanding, support and most of all love, the completion of this work would not have been possible.

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ABSTRACT OF THE DISSERTATION

ADVANCED GRAPHENE MICROELECTRONIC DEVICES

by

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The outstanding electrical and material properties of Graphene have made it a promising material for several fields of analog applications, though its zero bandgap precludes its application in digital and logic devices. With its remarkably high electron mobility at room temperature, Graphene also has strong potential for terahertz (THz) plasmonic devices. However there still are challenges to be solved to realize Graphene's full potential for practical applications.

In this dissertation, we investigate solutions for some of these challenges. First, to reduce the access resistances which significantly reduces the radio frequency (RF) performance of Graphene field effect transistors (GFETs), a novel device structure consisting of two additional contacts at the access region has been successfully modeled, designed, microfabicated/integrated, and characterized. The additional contacts of the proposed device are capacitively coupled to the device channel and independently biased, that induce more carriers and effectively reduce access resistance.

In addition to that, in this dissertation, bandgap has been experimentally introduced to semi-metallic Graphene, by decorating with randomly distributed gold nano-particles and zinc oxide (ZnO) nano-seeds, where their interaction breaks its sublattice symmetry and opens up bandgap. The engineered bandgap was extracted from its temperature dependent conductivity characteristics and compared with reported theoretical estimation. The proposed method of device engineering combined with material bandgap engineering, on a single device, introduces a gateway towards high speed Graphene logic devices.

Finally, THz plasmon generation and propagation in Graphene grating gate field effect transistors and Graphene plasmonic ring resonators have been investigated analytically and numerically to explore their potential use for compact, solid state tunable THz detectors.

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CHAPTER I

INTRODUCTION

1.1 Graphene Material Overview

Graphene, a novel electro-optic material consisting of one or a few atomic layers of carbon sheets is considered to be the first truly 2D crystal ever observed in nature and is very promising for high performance micro/nanoelectronics [1]. Carbon, the elementary constituent of Graphene, is the 6th element of periodic table consisting of 6 protons, 6 to 8 neutrons, and 6 electrons. The electronic configuration of carbon is $1s^2 2s^2 2p^2$; 2 electrons in 1s atomic orbital (full), 2 electrons in 2s atomic orbital (full), 1 electron in $2p_x$ atomic orbital (not full), 1 electron in $2p_y$ atomic orbital (not full) and 0 electron in $2p_z$ atomic orbital (empty) [2]. In Graphene, the orbitals 2s, $2p_x$ and $2p_y$ make a sp2 hybridization while the remaining p_z is perpendicular to the x-y plane as shown in Figure 1, and thus it forms a honeycomb lattice.

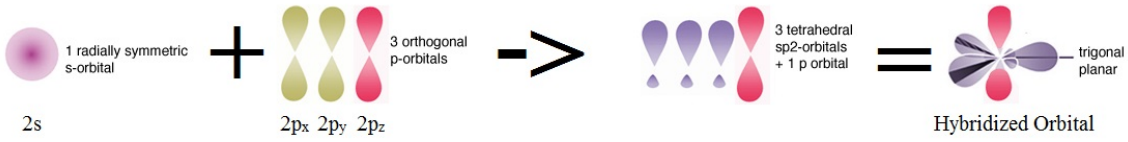

Figure 1: SP2 hybridization in Graphene

Fullerine, carbon nanotube, Graphene, and graphite are respectively 0D, 1D, 2D and 3D allotropes of carbon as shown in Figure 2 [3]. Fullerines are molecules consisting of wrapped Graphene by the introduction of pentagons on the hexagonal lattice, carbon nanotubes can be viewed as rolled-up cylinders of Graphene, while graphite can be viewed as a stack of Graphene layers sticking together due to van der Waals interaction. As we

already know, three out of four valence electrons of carbon in Graphene form covalent bond with the neighbor atoms and their wave function can be expressed as follows [4]:

$$\frac{1}{\sqrt{3}}\left(\psi_e(2s)+\sqrt{2}\psi_e(\tau_i 2p)\right),(i=1,2,3) \quad (1)$$

Here, $\psi_e(2s)$ is the 2s wave function and $\psi_e(\tau_i 2p)$ are the 2p wave function. The forth electron is in the $2p_z$ state. As three of the valence electrons form the coplanar bonds, they do not participate in electric conduction and thus has one conduction electron in $2p_z$ state.

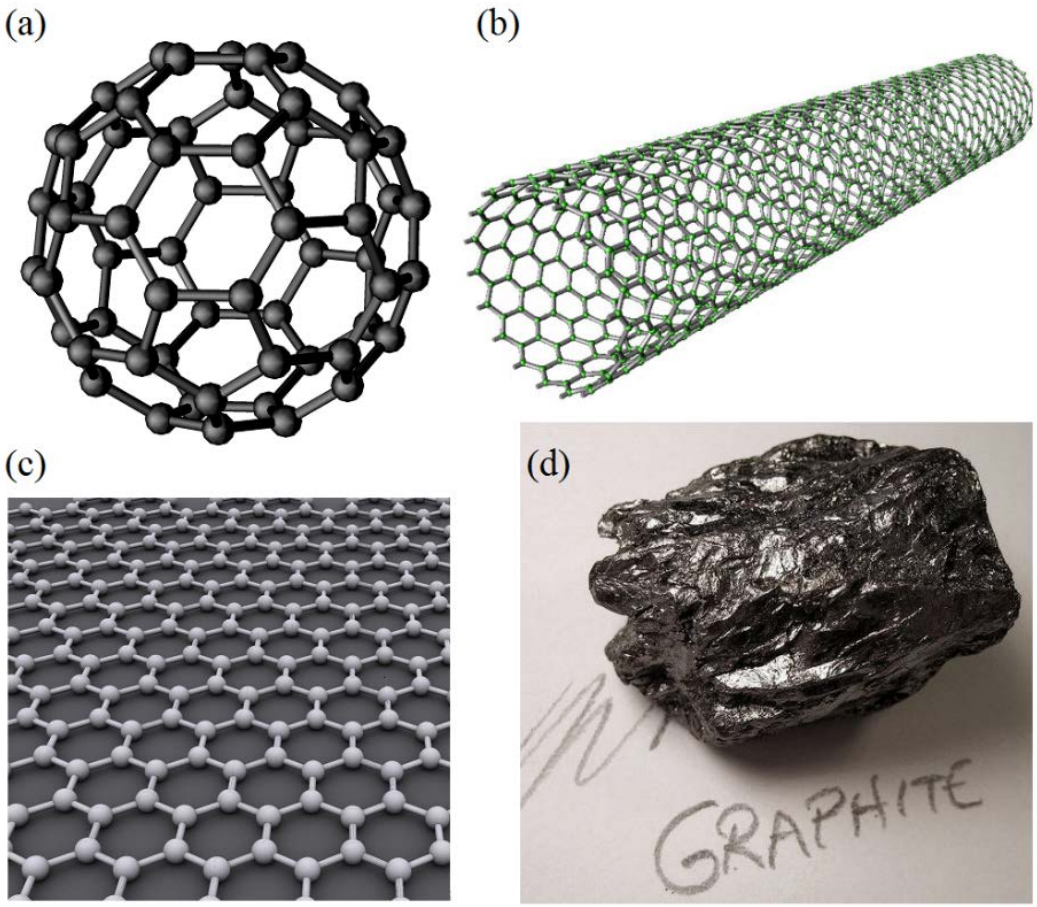

Figure 2: (a) Fullerine, (b) Carbon Nanotube, (c) Graphene, and (d) Graphite [3]

The unit cell of the hexagonal layer, *PQRS* as shown in Figure 3 contains two carbon atoms A and B. The distance *AB* is the lattice constant *a*=1.42 Aº. The fundamental lattice displacements of Graphene are a1=AA´ and a2=AA´´ and theirs magnitude is a1=a2= $\sqrt{3}\times$ 1.42 Aº=2.46 Aº. The reciprocal lattice vectors are 8π/3a and are in the directions of *AB* and *AS*, respectively.

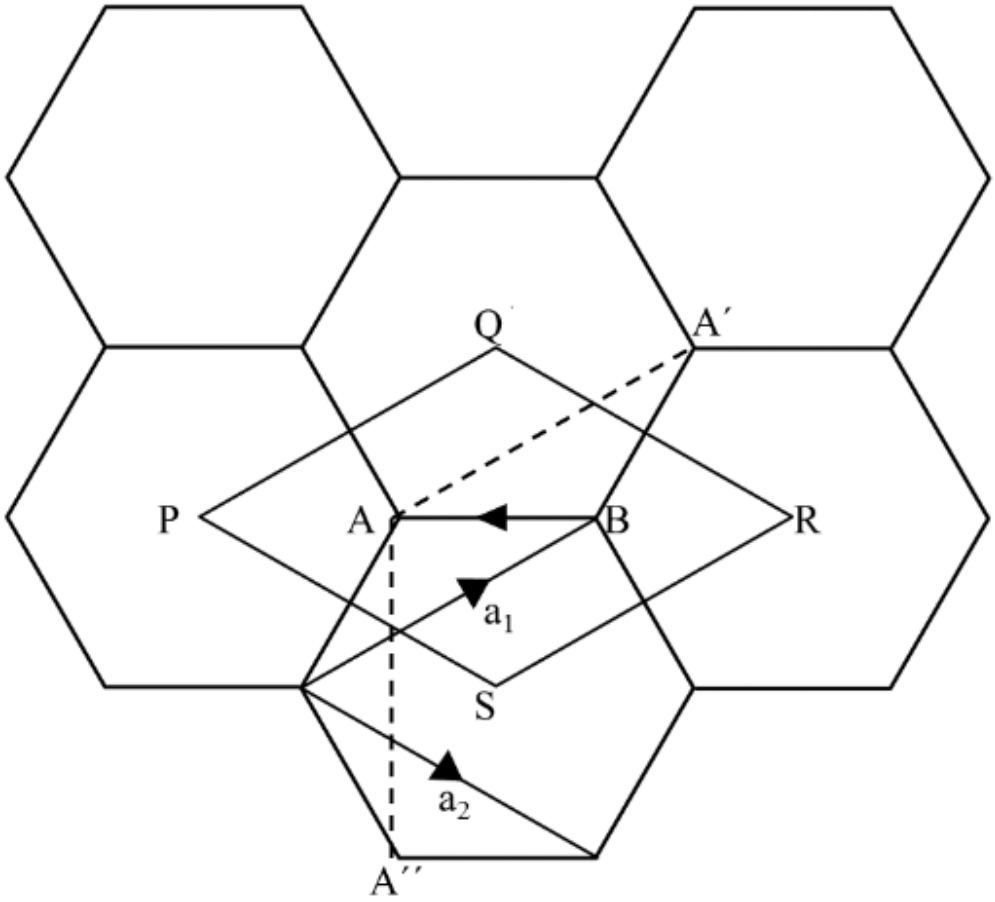

Figure 3: Honeycomb lattice structure of Graphene, made out of two interpenetrating triangular lattice.

Graphene has an unusual band structure with a zero bandgap. The energy momentum relation of a conventional semiconductor material can be expressed as [5]:

$$E^2 = m^2c^4 + p^2c^2 \tag{2}$$

where E= total energy, m= rest mass, c= velocity of light, p= momentum.

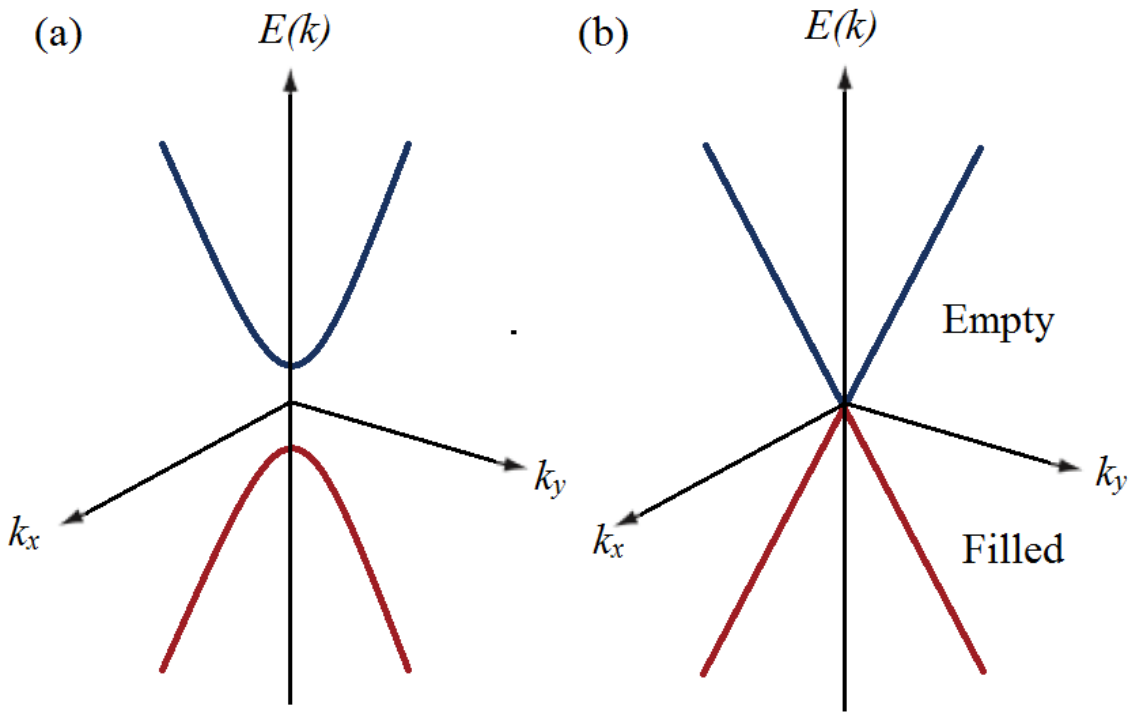

Figure 4: Energy-Momentum relation of (a) conventional semiconductor (b) Graphene

This equation represents a parabolic relationship which is true for ordinary semiconductors as shown in Figure 4 (a). For Graphene, this relationship is linear as in Figure 4 (b) and it can be expressed by the above equation if and only if we consider m=0. When an object moves with velocity (v), it has kinetic energy. Electrons in ordinary systems obey Newton's equation where energy increases quadratically in relation to velocity ($E \sim v^2$). But in Graphene, electrons' energy increases linearly with velocity ($E \sim v$). That is the reason electrons in Graphene behave as if they are relativistic, massless particles that obey Diract's equation and have high fermi velocity, 1/300 times the velocity of light [6].

Single layer Graphene and few layer Graphene can be synthesized by several methods and can be broadly classified into exfoliation, chemical vapor deposition (CVD), arc discharge, and reduction of Graphene oxide [7]. Exfoliation can be divided into two sub-categories: mechanical exfoliation and chemical exfoliation. Stacking of Graphene sheets in graphite is due to the overlap of partially filled p_z orbital which is perpendicular to the plane. Exfoliation of Graphene from graphite is the reverse process of stacking where work is done against the weak van der Waals force between Graphene layers with large lattice spacing. It has been possible to peel off one or a few sheets of Graphene using scotch tape and deposition on SiO_2/Si substrate. Mechanical exfoliation produces highest quality Graphene though it's limited due to low productivity. In case of chemical exfoliation, the first step is to increase the interlayer spacing by intercalating Graphene to prepare Graphene intercalated compounds (GICs) which are then exfoliated into Graphene in the second step by heating or sonication [7]. The most promising and inexpensive process for deposition of reasonably high quality Graphene is CVD on transition metal substrate. A RF plasma-enhanced CVD system is widely used to synthesize Graphene on various transition metal substrates by decomposing hydrocarbons such as methane, ethylene, acetylene, and benzene. The layer number of Graphene depends on the hydrocarbon and reaction parameters. Synthesis of Graphene by arc evaporation of graphite in presence of H_2 has also been possible and reported. In this process, two or three layers of Graphene with flake size of 100-200 nm can be prepared. Chemical reduction of graphite oxide is another established procedure in which large quantity of Graphene can be prepared. Graphite oxide when ultrasonicated in water forms a homogeneous colloidal dispersion of predominantly sheet Graphene oxide (SGO) in water. Reduced Graphene oxide (RGO)

with properties similar to that of Graphene is prepared through chemical, thermal, or electrochemical reduction pathways [7].

1.2 Prospect of Graphene as an Electronic Material

Graphene is considered to be a very promising novel material for high performance nanoelectronics, due to its high carrier mobility, concentration, and stability [8, 9]. It is a prime candidate for many electrical and optical applications due to its extremely high thermal conductivity, long phonon mean free path, and as a 2D material, it could also enable extreme device scaling [10, 11]. With its large band structure velocity (1×10^8 cm/s), large saturation velocity (4×10^7 cm/s), and low 1/f noise characteristics [12, 13, 14, and 15], Graphene is particularly attractive for high frequency electronics. Significant progress has been made on Graphene analog devices capable of good high frequency performance in the region of radio frequency (RF) and Terahertz (THz) frequency.

Numerous groups have reported Graphene based analog devices with amplification and phase detection capability [16, 17] as well as plasmonic THz detection capability [18]. Moreover, because of strong ambipolar effect and lack of bandgap [9], Graphene is believed to be more suitable for analog applications than for digital electronics. The physical thinness of Graphene shows prospect of two dimensional high-speed electronics. In addition to its outstanding electrical and thermal properties, its high optical transparency (97.7%) and mechanical elasticity open windows for high-speed transparent and flexible electronics.

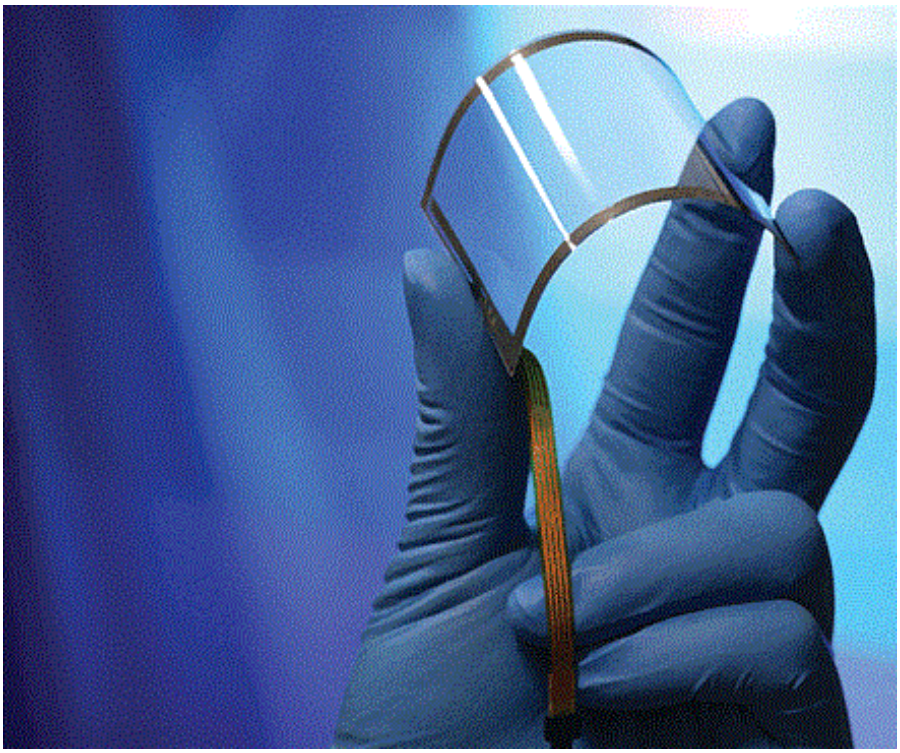

Figure 5: Graphene based transparent and flexible electronics [19]

Numerous groups have reported many fascinating and outstanding high frequency characteristics of Graphene field effect transistors. For example, Lin et al. reported a GFET with a gate length of 144 nm and a current gain cut-off frequency, f_T of 350 GHz [1].

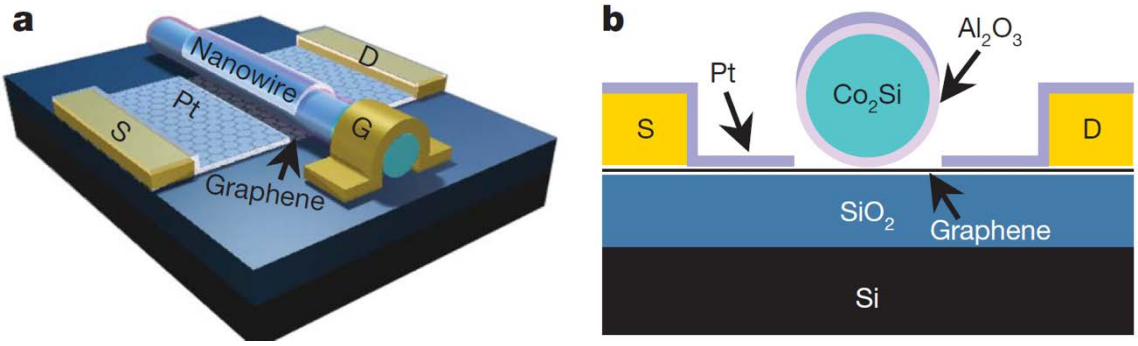

Figure 6: Graphene nanowire gate GFET

Duan et al. reported a nanowire gate GFET as shown in Figure 6 of 144 nm long gate with a f_T of 300 GHz [20]. Similarly, Avouris et al. and Farmer et al. reported GFET with gate length of 40 nm and 240 nm with a f_T of 100 GHz and 155 GHz, respectively [8, 21].

In addition to Graphene based RF FETs, numerous groups have also worked and reported on Graphene based plasmonic THz detectors that operates in room temperature. For example, Knap et al. reported GFETs based on single layer and bilayer Graphene as shown in Figure 7, with acceptable responsivity and photoresponse in room temperature [89].

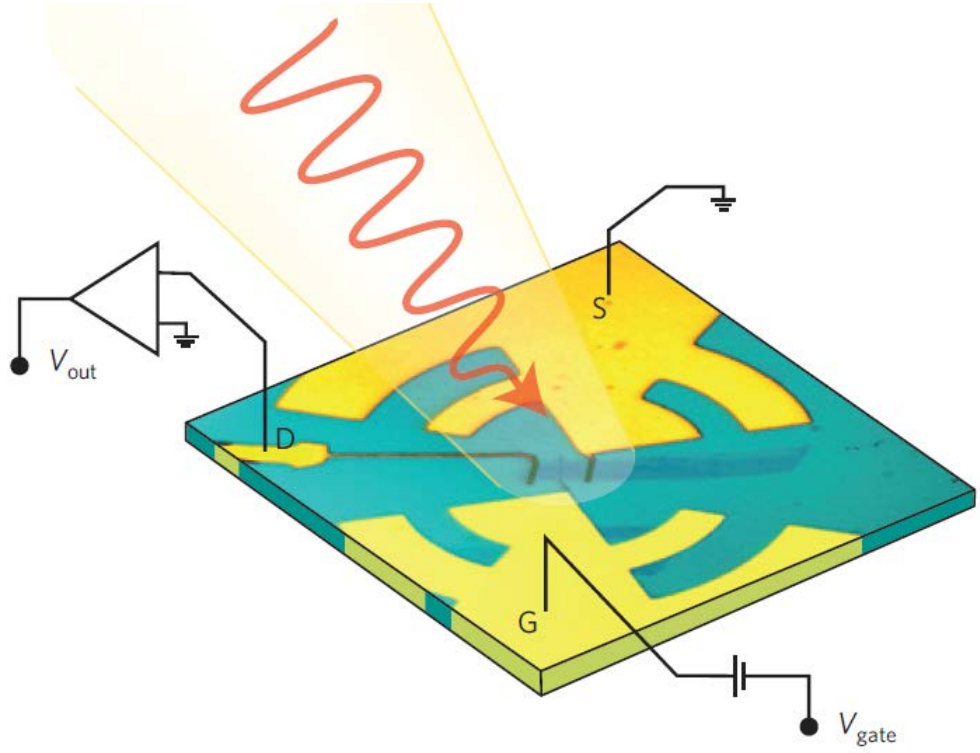

Figure 7: Schematic of THz plamsonic detectors based on Graphene

1.3 Effect of Zero Bandgap Graphene as Channel Material

The electronic bandgap of a solid material is the energy gap between the bottom of the conduction band and the top of the valence band. Electrons from the valence band can jump the gap to the conduction band to participate in electric conduction by means of thermal or optical excitation [22]. The band structure of different types of materials including Graphene is shown in Figure 8.

The insulators have a large bandgap that the electrons in valence band cannot gain enough energy to jump up to conduction band, as a result, insulators are bad conductors. On the other hand, metals valence and conduction bands overlap and the electrons in valence band can go to conduction band without any excitation, that's why metals are good conductors.

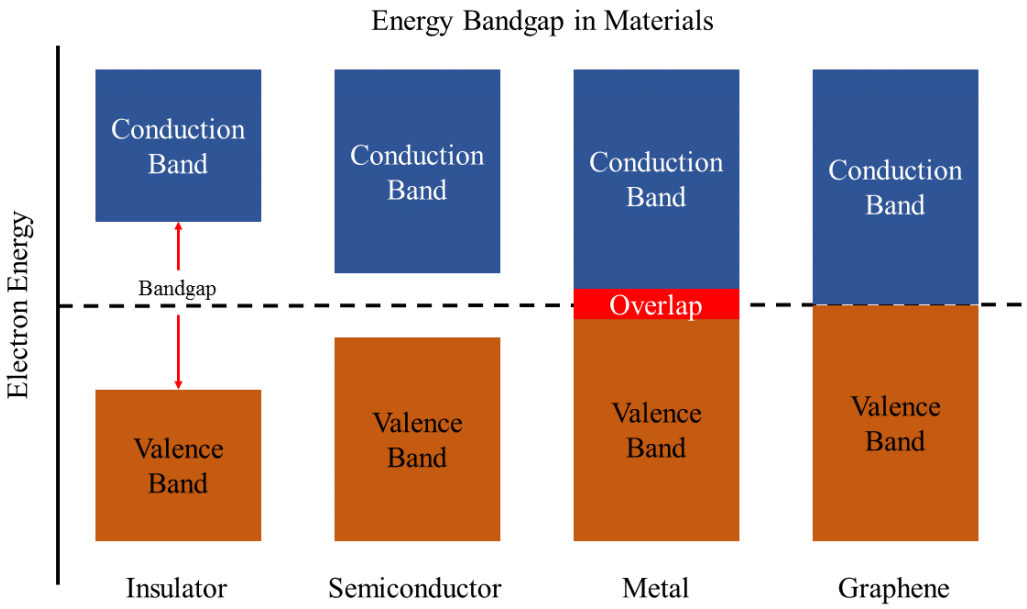

Figure 8: Band structure of insulators, semiconductors, metals and Graphene

The existence of a small bandgap allows semiconductor devices to partially conduct as the word “semiconductor” implies. It is the bandgap that gives semiconductors the ability to switch currents on and off as, in order to achieve a desired electrical function. Unlike metals, the band structure of Graphene exhibits two bands intersecting at the k and $k´$ points in the Brillouin zone—Dirac point, and at this point, valence and conduction band are degenerate, which results in Graphene to be a zero bandgap semi-metal material. As it has a zero bandgap, Graphene transistors can never be turned off, which precludes it use in digital and logic application, as well as in pseudospintronics, and infrared nanophotonics [23].

CHAPTER II

GRAPHENE FET WITH IMPROVED CONTACT RESISTANCE

2.1 Introduction:

The advantages of Graphene as a channel material of FETs include but not limited to its perfect 2D confinement of carriers, high residual carrier concentration, high carrier mobility, mechanical flexibility, and extremely high thermal conductivity. The access resistance of GFETs adversely affect the current gain cut-off frequency, f_T by reducing the transconductance and drain current and specially becomes very crucial in downscaled GFETs with shorter gate length. It is therefore desired to minimize GFET access resistance. In conventional silicon based RF transistors, the resistance of access regions is reduced by doping through ion implantation [24]. However, In GFETs, the access regions consist of just a monolayer ungated Graphene with a high sheet resistance, compared to that of heavily doped Si MOSFETs. As a result, the access resistance of GFETs is comparable to the resistance of gated Graphene channel and the 2D structure of Graphene negates the use of ion implantation to dope [25]. The typical value of access resistance of a Silicon MOSFET is at the order of ~150 Ω-μm [26]. On the other hand, the typical access resistance value of a Graphene FET is ~350 Ω-μm and 80% of the total device resistance [27]. To utilize the complete advantage of Graphene as a channel material, the set of limitations on the high-frequency performance of GFETs arisen from the access resistances must be eliminated.

It is well known that the source/drain resistances comprising of contact resistance and access resistance impose important set of limitations on the high frequency performance of sub-micrometer FETs by reducing the external transconductance leading to a lower drain current and their minification ensures improved RF performance. These resistances delay

the transition of carriers through the device and in terms of delay time, reduction of transit delay time caused by channel resistance and parasitic delay time caused by source/drain resistance ensure high cut-off frequency that can be achieved through shorter gate length and smaller access regions, respectively. Here are some attempts of transit time reduction to improve RF performance: 550 nm and 240 nm long top gated GFET with epitaxially formed Graphene on the Si face of a semi-insulating high purity SiC wafer and 10 nm HFO_2 as gate dielectric demonstrated cutoff frequency of 53 GHz and 100 GHz respectively [8]. GFET with epitaxial Graphene on Si-face of 4H-SiC having gate lengths between 2 μm to 0.5 μm demonstrated current gain cut-off frequency f_T of 4.1 GHz for 2.0 μm long gate GFET whereas the 0.5 μm long gate GFET showed an exceptional high power gain cut-off frequency of 16 GHz [28]. GFETs having CVD Graphene transferred from copper to diamond-like carbon (DLC) as substrate with 500nm, 140nm and 40nm long gates demonstrated cut-off frequencies of 26GHz, 70GHz and 155GHz respectively [21].

Self-aligned process is used to reduce access region length that can effectively reduce parasitic delay time and increase f_T. Self-aligned fabrication of T-gate CVD Graphene FET with gate length of 110nm and 170nm with shorter ungated Graphene sections of about 20-40nm were reported showing f_T of 15 GHz and 23 GHz respectively [29]. GFETs with self-aligned nanowire gate having gate length of 210 nm, 182 nm and 144 nm demonstrated f_T of 125 GHz, 168 GHz and 300 GHz respectively [20]. However self-aligned process makes fabrication more complex with smaller tolerances.

Reduction of access resistance for enhanced RF performance in III-N high electron mobility transistors (HEMT) [30] and in Graphene FETs (GFET) have been reported [31,

32]. Here, rather than reducing the access resistance by minimizing ungated region length or doping, we propose, extensively analyze, fabricate/integrate, and characterize a novel device structure with controllable access resistance having a total of 5 contacts including source, drain, gate, and 2 field controlling electrodes (FCEs). The FCEs are capacitively coupled to the access regions of the device. The proposed device shows a higher cut-off frequency due to minimization of parasitic resistance. In addition to that, the capacitive coupling technique of the additional contacts ensures mitigation from additional power consumption.

2.2 Theory

2.2.1 Current Gain and Current Gain Cut-off Frequency

An important metric for RF transistor's performance measurement is its current gain cutoff frequency, f_T. Current gain is the ratio of current at the output terminal to that in the input terminal [33]. In common emitter configuration, the input terminal of a FET is the gate and the output terminal is drain.

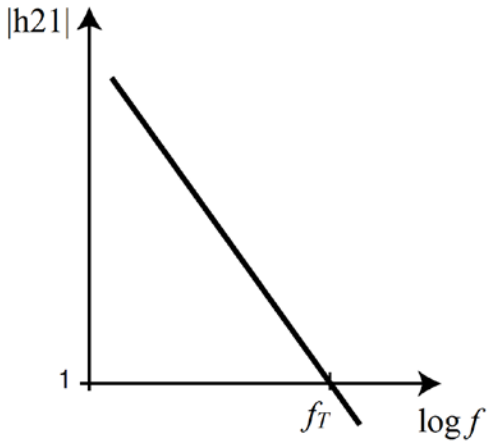

Figure 9: Relation between current gain, |h21| and frequency

As it is a FET, the input current in DC is zero. As a result, the current gain for DC is theoretically infinite, h21 = i_{out}/i_{in} = $i_{out}/0$ = infinite. The reactance of gate to channel capacitance is inversely dependent on frequency and with increasing frequency, the reactance decreases. As a result, the input AC current also increases with frequency which results in a decrement of current gain. The frequency at which, current gain drops to unity is called current gain cut-off frequency. A typical relation of current gain, |h21| and frequency is shown in Figure 9.

2.2.2 Small Signal Circuit Analysis of Regular Graphene FET

The schematic of a conventional 3-terminal GFET on SiO_2 with the small-signal equivalent circuit laid on top is shown in Figure 10.

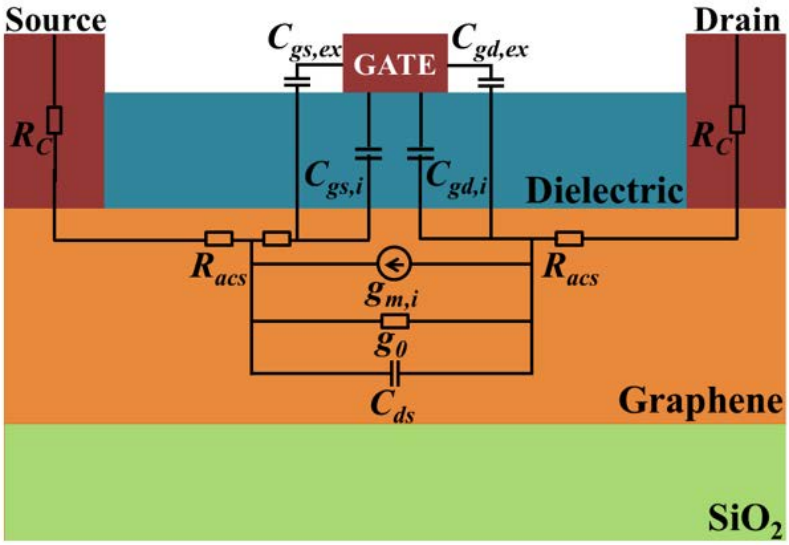

Figure 10: Schematic of a conventional 3-terminal GFET on SiO_2 with the small-signal equivalent circuit laid on top.

The gate to channel capacitance is actually a distributed capacitance and is usually simplified as two capacitors: gate to source capacitance, C_{gs} and gate to drain capacitance,

C_{gd}, such that

$$C_g = C_{gs} + C_{gd} \tag{3}$$

The gate to source capacitance and gate to drain capacitance are composed of both internal and external parts which can be expressed as

$$\begin{aligned} C_{gd} &= C_{gd,i} + C_{gd,ex} \\ C_{gs} &= C_{gs,i} + C_{gs,ex} \end{aligned} \tag{4}$$

Where $C_{gd,i}$ and $C_{gd,ex}$ are the intrinsic and extrinsic part of gate to drain capacitance, whereas, $C_{gs,i}$ and $C_{gs,ex}$ are the intrinsic and extrinsic part of gate to source capacitance. The intrinsic capacitances, $C_{gd,i}$ and $C_{gs,i}$ are parallel plate capacitances which are dependent on gate length. On the other hand, the extrinsic capacitances $C_{gd,ex}$ and $C_{gs,ex}$ are in fact fringe capacitances and independent on gate length [34].

The small-signal gate-source and gate-drain capacitance can be calculated as:

$$C_{gs} = \frac{\delta Q_{CH}}{\delta V_{GS}} \text{ , } V_{DS} \text{ is constant} \tag{5}$$

$$C_{gd} = \frac{\delta Q_{CH}}{\delta V_{DS}} \text{, } V_{GS} \text{ is constant} \tag{6}$$

Here, Q_{CH} is the total charge in Graphene channel, V_{GS} is gate to source voltage and V_{GD} is the gate to drain voltage. The total channel charge Q_{CH} can be expressed as:

$$Q_{CH} \approx \frac{WC_{OX}}{E_{AV}} V_{DS} \left(V_{eff} - \frac{V_{DS}}{2} \right) \tag{7}$$

Here, W is the device width, C_{OX} is the gate oxide capacitance, E_{AV} is the average electric field, and V_{eff} is effective gate-source overdrive voltage. If we replace $E_{AV} \approx \frac{V_{DS}}{L}$ in the above equation, the simplified expression for Q_{CH} turns out to be:

$$Q_{CH} = C_{OX} WL (V_{eff} - \frac{V_{DS}}{2}) \tag{8}$$

Now, the small signal gate to drain and gate to source capacitance can be calculated as:

$$\begin{aligned} C_{gs} &= C_{ox} WL \\ C_{gd} &= \frac{C_{ox} WL}{2} \end{aligned} \tag{9}$$

If $g_{m,i}$ is the intrinsic transconductance, the extrinsic delay of the device τ_{ext} can be expressed as [35]

$$\tau_{ext} = \frac{C_{gs,ex} + C_{gd,ex}}{g_{m,i}} \tag{10}$$

The intrinsic capacitances $C_{gd,i}$ and $C_{gs,i}$ are dependent on gate length and directly scale with that. The intrinsic delay time τ_{int} can be expressed as

$$\tau_{int} = \frac{C_{gs,i} + C_{gd,i}}{g_{m,i}} \tag{11}$$

The parasitic time delay due to parasitic resistances and capacitances can be expressed as [34]

$$\tau_{par} = C_{gd}(R_S + R_D).[1 + (1 + C_{gs} / C_{gd}) g_0 / g_m] \quad (12)$$

where $g_0 = 1/R_{SD}$ is the output conductance and R_S and R_D are the source and drain resistance representing the ohmic contact resistance, R_C and source/drain access resistance, R_{acs} in series:

$$R_D = R_S = R_C + (L_{acs} / \mu q n_0 W) \quad (13)$$

here L_{acs} is the access region length (L_{gs} and L_{gd}), μ is the carrier mobility, q is electronic charge, n_0 is the residual carrier density in Graphene and W is the device width. The current gain cut-off frequency f_T is inversely proportional to the total delay time in the device and can be expressed as

$$1/2\pi f_T = \tau_{\text{int}} + \tau_{ext} + \tau_{par} \quad (14)$$

Thus according to [35], through summing up all the delay times and rearranging, the f_T of the device can be related to the small signal circuit parameters as follows:

$$f_T = \frac{g_m / (2\pi)}{[C_{gs} + C_{gd}].[1 + (R_S + R_D) / R_{SD}] + C_{gd}.g_m.(R_S + R_D)} \quad (15)$$

where R_{SD} is the channel resistance that can be expressed as follows [29]:

$$R_{SD} = L_G / \mu q (n_0^2 + n_g^2)^{1/2} W \quad (16)$$

where n_g is the carrier density due to gate modulation. One needs to minimize the delay times to increase the current gain cut-off frequency, f_T as well as maximum oscillation frequency, f_{MAX}, which is proportional to f_T. From Figure 11, it is visible that for short channel devices, the effect of parasitic time delay, τ_{par} becomes more prominent compared to that of long channel devices. So, for short channel devices with good high frequency performance, its minimization becomes indispensable [36].

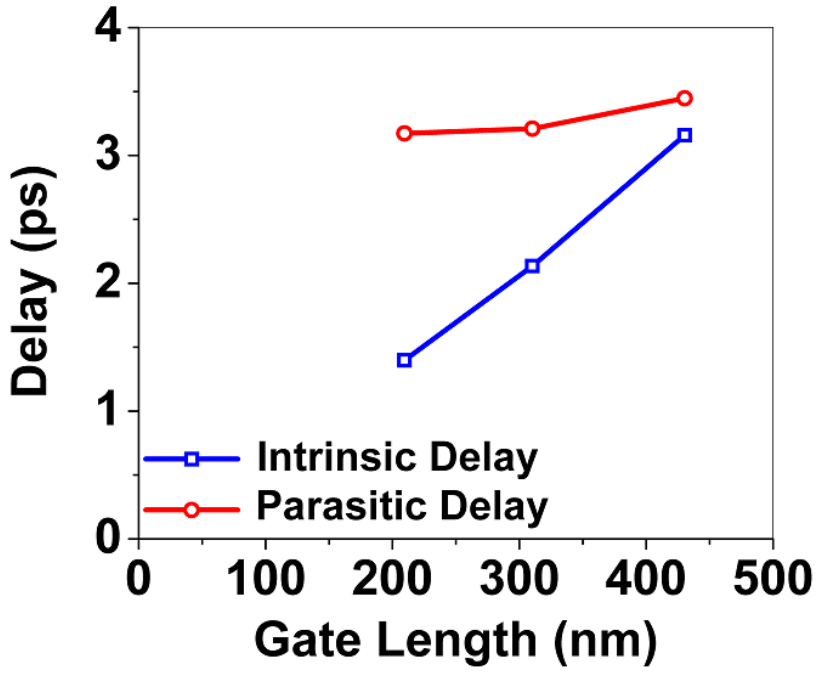

Figure. 11: Intrinsic and parasitic time delays vs. gate length of $In_{0.7}Ga_{0.3}As$-channel HEMTs reproduced from [36].

2.2.3 Small Signal Circuit Analysis of Top FCE GFET

To reduce the GFET access resistance, here we propose a novel device structure consisting of two capacitively coupled FCEs, placed on top of the device, at the ungated access regions as shown in Figure 12 (b). As the transistor action of the device takes place at the

gate terminal, the additional DC bias at the FCEs will help supporting the total device current in either of the transportation regimes (electron/hole) by selective population of particular type of carriers at the access regions.

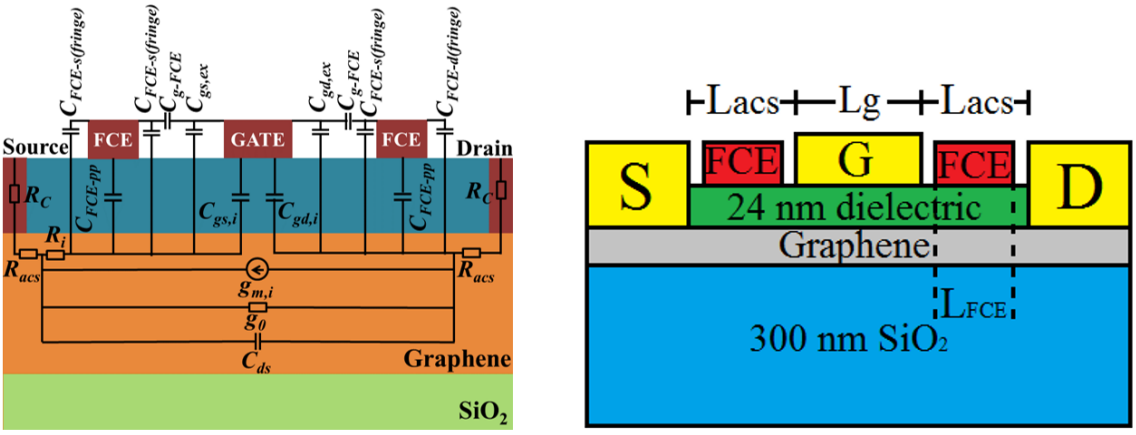

Figure 12: (a) Small signal equivalent circuit overlaid on top of top FCE GFET (b) Schematic of the proposed top FCE GFET (not in scale).

The proposed FCEs independently biased with a DC voltage reduce the source/drain access resistance, as well as, introduce some additional parasitic capacitance. A small signal equivalent circuit overlaid on top of the proposed GFET with two FCEs placed on top of the access regions is shown in Figure 12 (a). The FCEs make a parallel plate capacitance, $C_{FCE\text{-}pp}$ and two fringe capacitances, $C_{FCE(fringe)}$ with the Graphene channel. As all three of the capacitances are parallel to each other, the total FCE capacitance, C_{FCE} can be expressed as:

$$\begin{aligned} C_{FCE} &= C_{FCE(pp)} + 2C_{FCE(fringe)} \\ &= \varepsilon_0 \varepsilon_r \frac{WL_{FCE}}{t_{ox}} + 2C_{FCE(fringe)} \end{aligned} \tag{17}$$

Here, ε_0 is the permittivity of free space, ε_r is the relative permittivity of air, W is the device width, L_{FCE} is the FCE length, and t_{ox} is the gate oxide thickness. The gate terminal makes two parallel plate capacitance with FCE on each side and can be expressed as:

$$C_{g-FCE} = \varepsilon_0 \varepsilon_r \frac{Wt}{L_{g-FCE}} \tag{18}$$

The total gate to source capacitance, $C_{gs(total)}$ and $C_{gd(total)}$ after adding FCEs turn out to be

$$\begin{aligned} C_{gs(total)} &= C_{gs} + \frac{C_{FCE} \times C_{g-FCE}}{C_{FCE} + C_{g-FCE}} \\ C_{gd(total)} &= C_{gd} + \frac{C_{FCE} \times C_{g-FCE}}{C_{FCE} + C_{g-FCE}} \end{aligned} \tag{19}$$

If an FCE of length L_{FCE} is placed at the access region of length L_{acs}, then the new expression for R_S and R_D becomes

$$R_D = R_S = R_C + \frac{(L_{acs} - L_{FCE})}{W \mu e n_0} + \frac{L_{FCE}}{W \mu e \left(n_0^2 + n_{FCE}^2\right)^{1/2}} \tag{20}$$

The induced carriers n_{FCE} caused by FCE modulation effectively reduces the resistance of the ungated access regions and thus results in a decrement of τ_{par} and increment of f_T.

2.2.4 Small Signal Circuit Analysis of Bottom FCE GFET

In this part of this report, we study the theory of the proposed device consisting of two independently biased capacitively coupled contacts placed at the access regions on bottom

of the GFET as shown in Figure 13. As like as the top FCE GFET, the FCEs on the bottom of the device are independently biased and capacitively coupled to the channel.

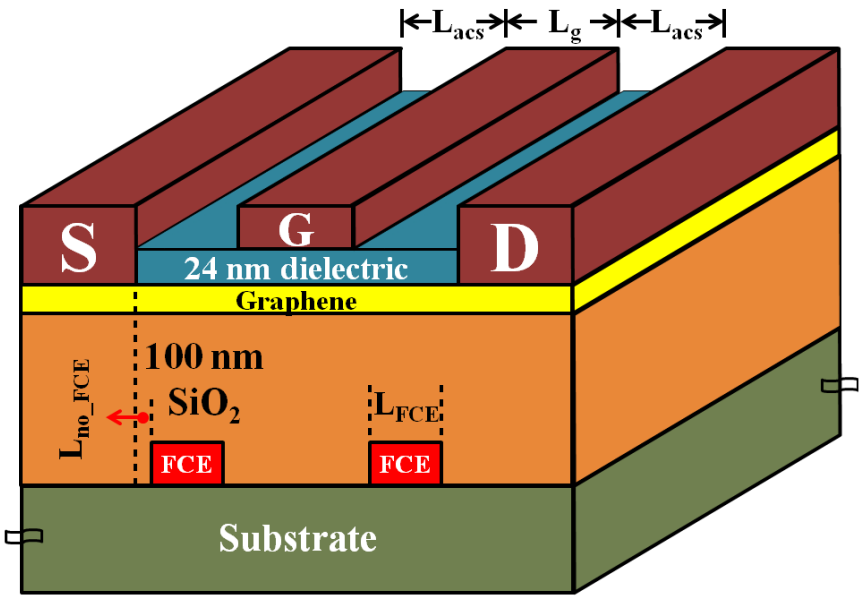

Figure 13: Schematic of the proposed GFET with 2 bottom FCEs at the ungated region

The independently biased FCEs induce additional carriers at the access region according to eqn. 16 As proposed, an FCE of length L_{FCE} placed at the access region of length Lacs making two no-FCE regions on both sides each having a length of L_{no_FCE} changes the expression of R_S and R_D as follows-

$$R_S = R_D = 2R_C + \frac{4L_{no\_FCE}}{\mu e n_0 . W} + \frac{2L_{FCE}}{\mu e (n_0^2 + n_{FCE}^2)^{1/2} W} \tag{21}$$

The resistance of the ungated access regions decreases by the induced carriers n_{FCE} due to FCE modulation which results in a decrement of τ_{par} and increment of f_T. In this device, the key advantage is the ease of fabrication with high tolerance, because the FCEs are to

be patterned on a different layer other than the gate layer. In addition to that, the larger distance between FCEs and gate will result in lower parasitic capacitances.

2.2.5 Small Signal Circuit Analysis of Hybrid Contact GFET

In this part, we have proposed, studied, and extensively analyze a GFET with hybrid contacts capable to reduce the access resistance and contact resistance of the device, simultaneously.

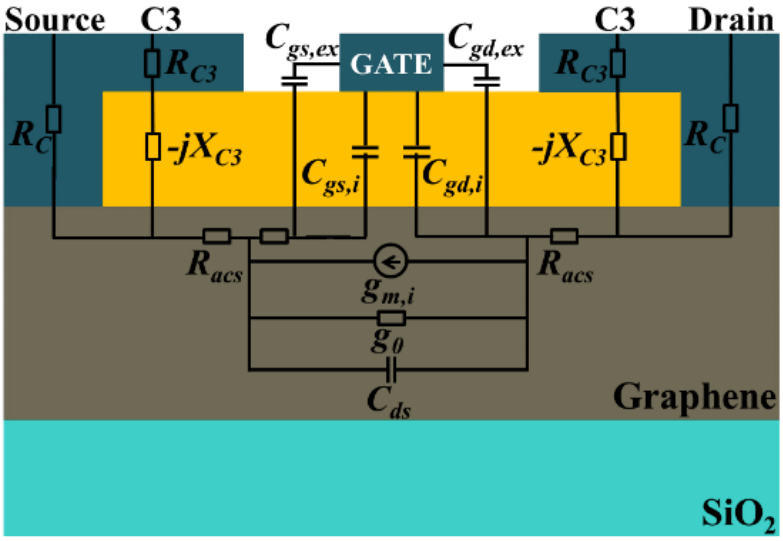

Figure 14: Small signal equivalent circuit overlaid on top of the proposed hybrid contact Graphene FET

The hybrid contact consists of a ohmic contact having capacitive extension towards the Gate. The capacitively coupled part of the contact reduces the contact resistance and provides a low resistance path for the high frequency signal. In addition, the extension towards Gate reduces the access region length and the associated resistance—the access resistance. Small signal equivalent circuit of the proposed hybrid contact GFET overlaid on the device schematic is shown in Figure 14.

If two capacitively coupled contacts (C3s) are placed on the access regions and connected to the ohmic Source/Drain as shown in Figure 2, the C3 will make a path for high frequency RF signal parallel to the ohmic contact. The C3 impedance $Z_{C3}=R_{C3}-jX_{C3}$ consists of real and imaginary parts and the total contact impedance comes to be $Z_C = R_C||Z_{C3} = R_C||(R_{C3}-jX_{C3})$. After rearrangement and simplification, Z_C can be expressed as:

$$Z_C = \frac{R_C^2 R_{C3} + R_{C3}^2 R_C + X_{C3}^2 R_C}{(R_C + R_{C3})^2 + X_{C3}^2} - j\frac{X_{C3} R_C^2}{(R_C + R_{C3})^2 + X_{C3}^2} = R_C' - jX_C' \tag{22}$$

Assuming the length of C3 is L_{C3}, the access region length of the hybrid contact GFET comes to be $L_A' = L_A - L_{C3}$ and the new expression for Source/Drain impedance and total channel impedance become as follows:

$$\begin{aligned} Z_D = Z_S &= Z_C + R_A' = R_C' - jX_C' + (L_A' / \mu q n_0 W) \\ Z_{SD} &= 2Z_D + R_{CH} = R_{SD} - jX_{SD} \end{aligned} \tag{23}$$

From the equation above, we can see that the total channel resistance has real part as well as an imaginary part. A simple matching network can be designed for matching and eliminating the imaginary part of the input impedance. An impedance matching network is an additional circuit that consists of a reactive element of such a value that can effectively nullify the opposite signed reactive element of the device and thus eliminate the effective reactance of the whole system. It can be achieved with only 2 reactive elements that transform both the real and imaginary part. A common 2 reactive element configuration is referred to as L-section matching network as shown in Figure 3(a).

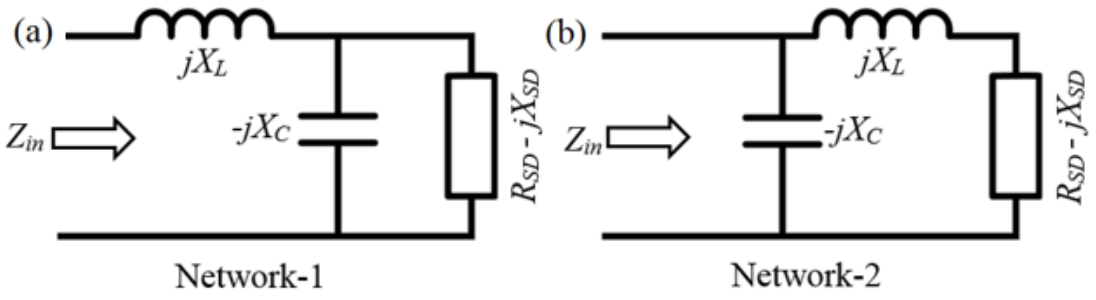

Figure 15. (a) Matching Network-1 (b) Matching Network-2.

Considering network-1, we can quantify the input impedance as:

$$Z_{in} = jX_L + \frac{R_{SD} + jX_{SD}}{1 + jX_C R_{SD} - X_C X_{SD}} \tag{24}$$

To match it with a resistance R, we consider $Z_{in}=R$ and after equating the real and imaginary parts, we get:

$$X_L = \frac{1}{X_{CAP}} + \frac{X_{SD}R}{R_{SD}} - \frac{R}{X_{CAP}R_{SD}}$$
$$X_{CAP} = \frac{X_{SD} \pm \sqrt{\frac{R_{SD}}{R}}\sqrt{R_{SD}^2 + X_{SD}^2 - RR_{SD}}}{R_{SD}^2 + X_{SD}^2} \tag{25}$$

By solving these equations, we can determine the capacitor and inductor values required to nullify imaginary part of contact impedance. These two relations are derived for network-1 and are valid if $R_{SD}>R$. On the other hand, if $R_{SD}<R$, network-2 as shown in Figure 3(b) needs to be used and after following the same procedure, we can estimate X_L and X_{CAP} as follows:

$$X_L = \pm\sqrt{R_{SOURCE-DRAIN}(R - R_{SOURCE-DRAIN})} - X_L$$
$$X_{CAP} = \pm\frac{\sqrt{(R - R_{SOURCE-DRAIN})} / R_{SOURCE-DRAIN}}{R} \quad (26)$$

For devices working on a wide frequency range, a very common technique in RF/mobile communication named “frequency transformation technique” needs to be used, as reported in [37].

Once the matching network has been used, only the real part of contact resistance R’$_c$ remains and the new expression of source/drain resistance comes out to be:

$$R_D = R_S = R'_C + (L'_A / \mu q n_0 W) \quad (27)$$

One can easily get the relation between f_T and Z_C by plugging this new R_S and R_D into the f_T equation in (5).

The C3 can be considered as a RC transmission line and its impedance can be analytically calculated [38]. If a C3 is placed on top of Gate dielectric, the contact metal and Graphene channel with in-between dielectric material form a RC transmission line. The propagation constant γ and characteristics impedance Z_0 of this transmission line can be estimated by the following equations:

$$\gamma = \sqrt{i2\pi R_{sh} C}, Z_0 = \frac{1}{W}\sqrt{\frac{R_{sh}}{i2\pi fC}} \quad (28)$$

where, R_{sh} is sheet resistance of Graphene channel, C is the metal to Graphene capacitance per unit area, W is the width and f is the frequency. The C3 impedance can be estimated equal to the input impedance of this open ended transmission line as follows:

$$Z_{in} = Z_0 \coth\left(\gamma L_{C3}\right) \tag{29}$$

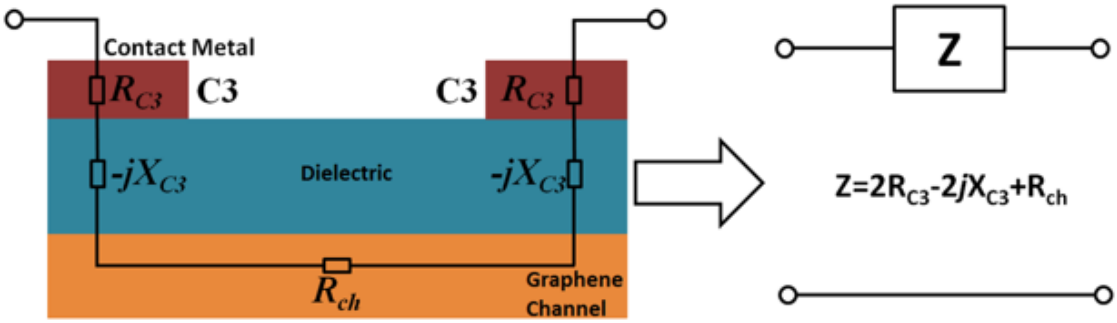

Figure 16. Schematic of a RF TLM structure on Graphene with small-signal equivalent circuit overlaid on top and the equivalent 2-port network

In simulation, the impedance of C3s can be calculated by using RF Transmission Line Method (TLM) structures with multiple C3s with various in-between distances. Two C3s and the Graphene channel in-between is a Two-Port network as shown in Figure 4 and its impedance can be estimated by extracting the 2 port S-Parameters and converting them to B-Parameter [39]. The real and imaginary parts of B-parameter are actually the real and imaginary parts of total impedance of the two port network—two C3 impedance in addition to in-between Graphene channel resistance.

2.3 Simulation of GFET with FCEs

2.3.1 Simulation of Top FCE GFET

Here we simulate and analytically estimate the performance of the top FCE GFET and compare with the conventional ones. The baseline conventional GFET in this study was chosen similar to the one reported in [10]. We name it as GFET-A. It consists of 3.0 μm long gate and 1.5 μm long access region having SiO_2 as substrate and Al_2O_3 with SiO_2 as gate dielectric as shown in Figure 17 (a). Using the reported characteristics, residual carrier (hole) concentration at the Graphene channel is extracted as 7.02 $\times 10^{12}$ cm^{-2} at $V_{GS}=0$ which results in an access resistance of R_{acs}=25.2 Ω for the device width of 100 μm. We simulated the DC and RF characteristics of the baseline GFET using physics based numerical device simulation tool with parameters modified for Graphene. This type of simulation approximates the operation and transportation of carriers through the structure by applying a set of differential equations including Poisson's Equation, Carrier Continuity Equations and Drift-Diffusion Equation, derived from Maxwell's laws, onto a 2D grid, consisting of a number of grid points called nodes. This way the electrical performance of a device can be modeled in DC, AC or transient modes of operation [40]. The results presented in Figure 17 (b) are in good agreement with the measured characteristics in [10] which validate our simulation method where the contribution of both the electrons and holes to the drain current is considered. For the baseline GEFT, f_T and f_{MAX} are extracted as 1.0 GHz and 1.2 GHz, respectively. Operating regime (electron or hole) of the device can be chosen by biasing the gate on either side of Dirac point to make one type of carriers dominant. The total device current on either regime is still supported by the low density

residual carriers at the ungated access regions causing high source/ drain resistance which adversely affect the RF performance. The simulation decks have been documented in APPENDIX A and APPENDIX B.

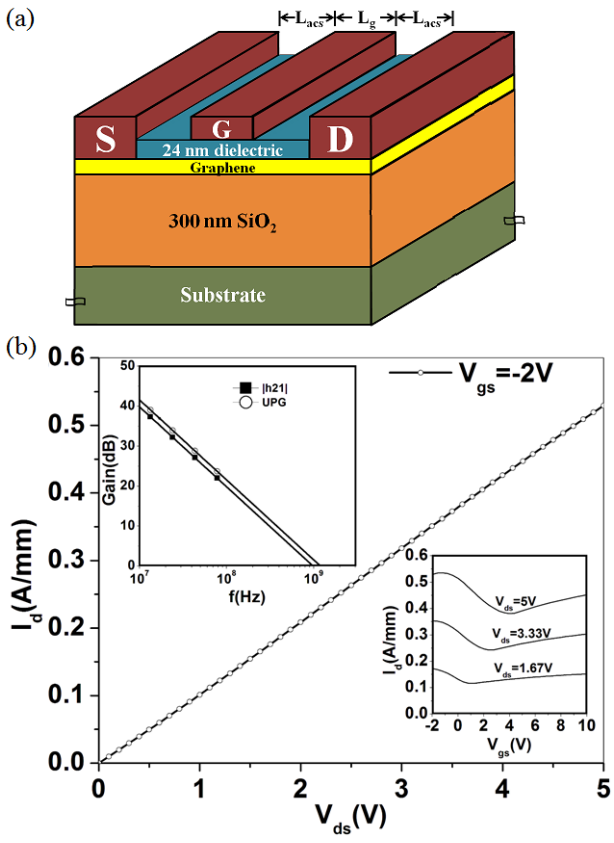

Figure 17: (a) Schematic of the baseline GFET-A, (b) DC and RF characteristics (Current Gain, $|h_{21}|$ and Unilateral Power Gain, UPG) of the baseline GFET-A from simulation.

In the proposed device, two capacitively coupled FCEs are placed at the ungated access regions as already shown in Figure 12 (b). As the transistor action of the device takes place at the gate terminal, the additional DC bias at the FCEs will help supporting the total device current in either of the transportation regimes by selective population of particular type of carriers at the access regions.

We consider two devices for our analysis: (i) GFET-A; the long channel device with L_g=3.0 μm, L_{acs} =1.5 μm, μ_h=530 cm^2/V.s and μ_e=336 cm^2/V.s and (ii) GFET-B; the short channel device with L_g=0.5 μm, L_{acs}=1.5 μm, μ_e=4900 cm^2/V.s and μ_h=3100 cm^2/V.s. Analytical calculations using the equations above show that for GFETs with a typical residual carrier (hole) concentration of 4.8×10^{12} cm^{-2}, the GFET-A, the long channel low mobility device with two 1.3 μm long FCEs each biased at -3 V can lower the R_{acs} of an initial value of 36.8 Ω down to 20 Ω.

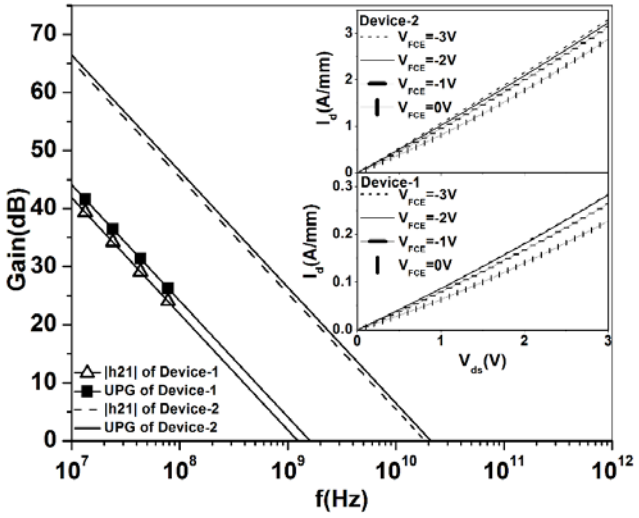

Figure 18: RF characteristics of both GFET-A and GFET-B with V_{FCE}=-3V and V_{gs}=-2V. Inset shows the I_d-V_d characteristics of GFET-A & B with V_{FCE} in hole transportation regime at V_{gs}=-2V considering concentration dependence of the hole mobility.

The minimization of R_{acs} makes the f_T of Device-1 to be 1.47 GHz whereas the f_T of this device with V_{FCE}=0 is 1.1 GHz calculated for hole transportation regime. Similar minimization of access resistance due to biased FCE makes the f_T of GFET-B; the short channel high mobility device to be 22.1 GHz which has a value of 16.9 GHz at V_{FCE}=0 also for hole regime operation.

The numerical device simulation tool was used to simulate the proposed novel GFET with residual carrier (hole) concentration of 4.8×10^{12} cm^{-2} same as that used for baseline device simulation and analytical calculations. The RF characteristics at V_{gs}=-2V (hole regime) and V_{FCE} = -3V along with the I_d-V_{ds} characteristics with FCE bias of both GFET-A and GFET-B are shown in Figure 18. The I_d-V_{ds} characteristic is depicting the decrement of R_S and R_D due to the decrement of R_{acs} by FCE bias.

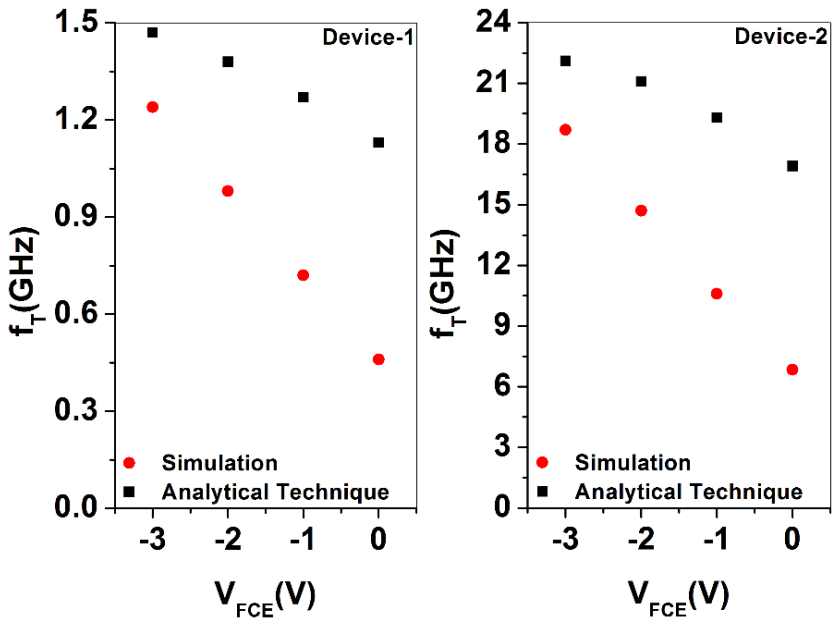

Figure 19: Improvement of f_T with V_{FCE} for both GFET-A and GFET-B in hole regime.

The improvement of RF characteristics with FCE bias estimated using both analytical and numerical techniques for hole regime is shown in Figure 19. It was reported that carrier mobility did not show significant dependence on carrier concentration in the range of concentration we worked [41]. Therefore, the hole mobility for the GFET-A value was kept constant at 530 cm^2/V.s throughout the entire range of FCE in both analytical and numerical analyses.

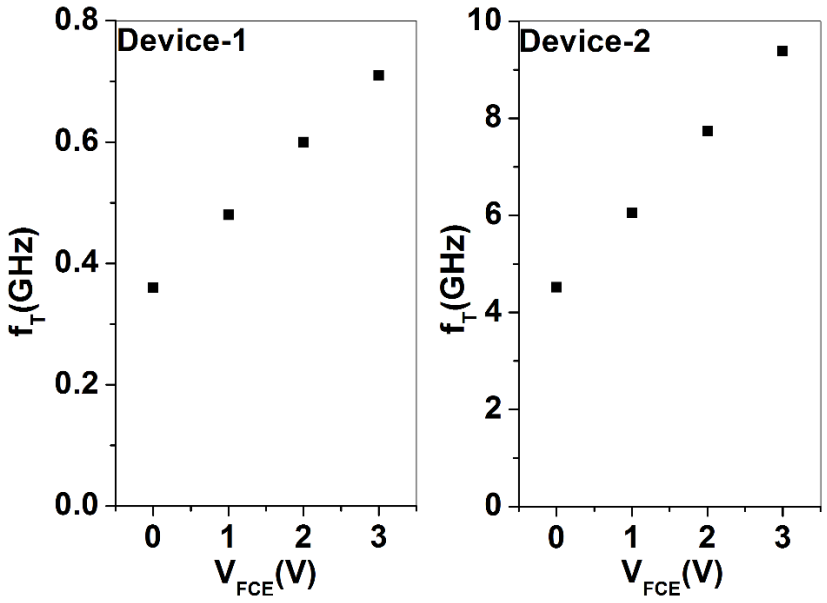

Figure 20: Improvement of f_T with V_{FCE} for both GFET-A and GFET-B in electron regime at V_{gs}=6.0 V (numerical simulation results).

On the other hand, Graphene hole mobility was considered to be significantly dependent on carrier concentration for the GFET-B, and its values at V_{FCE}=0, -1, -2, and -3V were estimated using the data in [42] for all analyses. The analytical technique resulted higher cutoff frequency compared to that obtained from numerical simulations because of the limitations to take the additional parasitic capacitances introduced due to the FCE contacts into account.

One can expect similar improvement of f_T while the GFET is in electron transport regime. Such improvement is estimated using the simulation tool considering similar concentration dependent mobility of electrons for GFET-B and shown in Figure 20.

2.3.2 Simulation of Bottom FCE GFET

To improve the RF performance we added FCEs at the 1.5 μm long ungated regions on bottom of GFET-A as already shown in Figure 13. As we cannot make the gate dielectric so thick that the gate loses good control over the channel, we have a limitation on the gate voltage too not to surpass the gate dielectric breakdown electric field. As the dielectric between FCEs and channel is much thicker compared to the gate dielectric, the FCE voltage was much higher than the gate voltage. To determine the optimum FCE length and position providing maximum f_T for GFET-A, we placed FCEs of different lengths at the center of the access regions leaving two equal no_FCE regions both sides and simulated the RF performance at V_{FCE}= -9V which represents an electric field moderately lower than the breakdown electric field of SiO_2 [43]. It was reported that carrier mobility did not show significant dependence on carrier concentration in the range of concentration we consider here [44]. Therefore, the hole and electron mobility was kept constant at 530 cm^2/V.s and 336 cm^2/V.s respectively for V_{FCE}= -9V as well as for rest of the analyses performed on GFET-A throughout the entire range of FCE bias. The dependence of f_T over L_{FCE} shown in Figure 21 (a) reveals that two 1.4 µm long FCEs at the access regions leaving 50 nm no_FCE regions on each side is the optimum condition in this case. Keeping the Source/Drain to FCE distance ($L_{s/d\text{-}FCE}$) unchanged to 50 nm, we gradually decreased the Gate to FCE distance down to zero (FCE edge aligned to Gate edge) and plotted f_T against them as shown in Figure 21 (b). The decrement of $L_{g\text{-}FCE}$ showed deterioration of f_T rather than improvement here. At $L_{g\text{-}FCE}$= 50 nm, we later decreased the $L_{s/d\text{-}FCE}$ from 50 nm down

to zero gradually. This time, the decrement of $L_{s/d\text{-}FCE}$ increased the f_T as shown in Figure 21 (c).

From Figure 21, the optimum L_{FCE}, $L_{s/d\text{-}FCE}$ and $L_{g\text{-}FCE}$ were found 1.45 µm, 0 µm and 50 nm respectively. Using the FCEs with optimum length and position, for hole regime operation of GFET-A (V_{gs} = -2.0 V), the DC simulations showed that the drain current increased with increasing negative FCE bias (V_{FCE}) shown in Figure 22, which reveals reduction of access resistance.

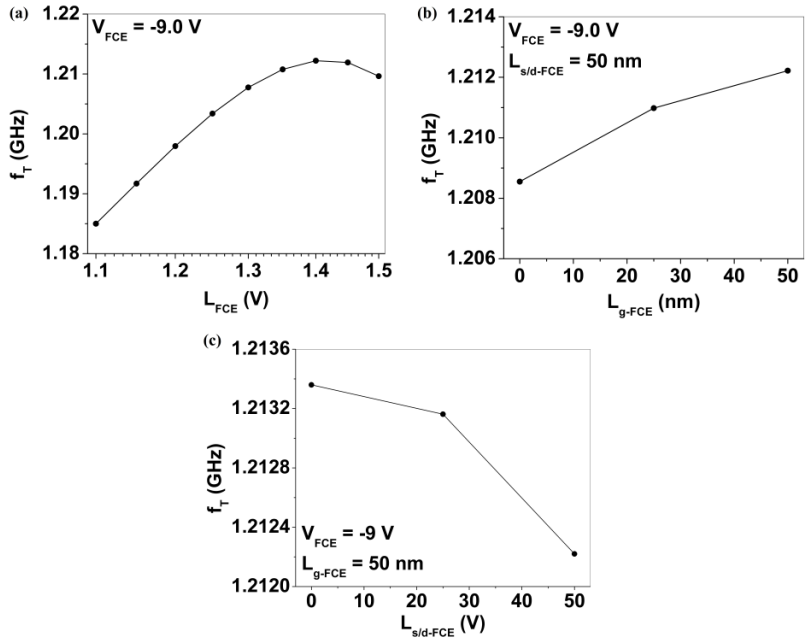

Figure 21: At V_{FCE}= - 9 V (a) f_T plotted against different L_{FCE}. (b) At $L_{s/d\text{-}FCE}$ =50 nm, f_T plotted against $L_{g\text{-}FCE}$. (c) At $L_{g\text{-}FCE}$ = 50 nm, f_T plotted against $L_{s/d\text{-}FCE}$.

Analytical calculations based on the equations presented above were used to quantify the reduction and was found that for L_{gs}/ L_{gd}=1.5 μm with FCEs of optimum size and position, the access resistance R_{acc}=36.8 Ω of the baseline device went down to 23.0 Ω at V_{FCE} = -9 V.

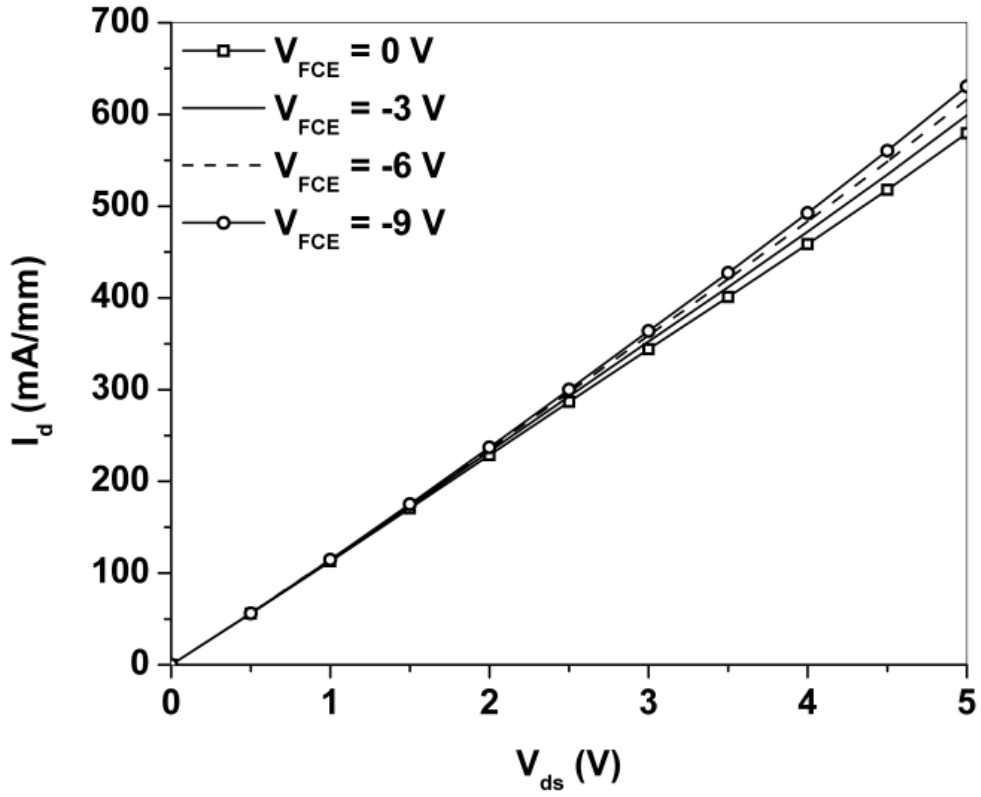

Figure 22: Increment of drain current with FCE bias at V_{ds} = 5.0 V and V_{gs} = -2.0 V.

We used analytical and numerical investigation to estimate the RF improvement in both electron and hole regime of operation. Fig. 5 (a) shows the simulated current gain, $|h_{21}|$ - frequency relationship of the device for the DC biasing conditions of $V_{gs} = -2$ V, $V_{ds} = 5$ V which represents hole regime operation of GFET-A and for different FCE biases. The current gain cutoff frequency, f_T was extracted from the data in Figure 23 (a) and compared to the ones analytically calculated in Figure 23 (b). As the simulation tool estimates the transportation of carriers through the structure by applying differential equations onto the nodes of a 2D grid, it was capable of including the additional capacitances arisen due to the presence of the additional contacts (FCEs) by itself. To include them in the analytical calculation part, we modified the capacitance values of C_{gs}

and C_{gd} in the RF equations derived for conventional 3-terminal FETs by calculating the FCE capacitances using geometric and material parameters. Considering the device width to be 100 µm, each of C_{gs} and C_{gd} valued 3.90×10^{-13} F calculated for conventional 3 terminal GFET and after inclusion of additional capacitances due to FCEs, it became 4.40×10^{-13} F.

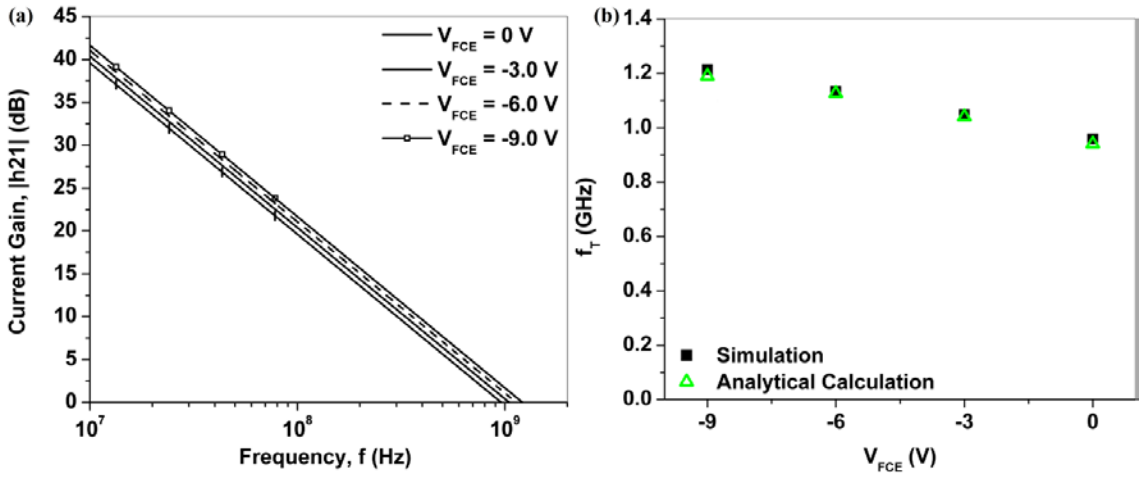

Figure 23: (a) Current gain $|h_{21}|$ - frequency relationship of the GFET-A with FCEs at varying V_{FCE} values in hole regime of operation. (b) f_T vs. V_{FCE} where f_T is calculated using analytical technique and also extracted from (a).

For electron regime of the same device, DC biasing of V_{ds} = 5 V and V_{gs} = 6 V was considered for similar analytical and numerical estimation of the cut off frequency, f_T . The f_T of baseline GFET-A in this condition was extracted to be 0.57 GHz. Figure 24 (a) shows the |h21|-frequency relationship of GFET-A with FCEs at different V_{FCE} and the extracted f_T values along with those from analytical technique are plotted against V_{FCE} in Figure 24 (b).

We also explored the effect of biased FCEs on RF improvement in short channel high mobility GFETs. The baseline GFET chosen for this analysis is similar to the one reported

in [34]. The device has CVD-grown Graphene channel with carrier mobility of μ = 2234 cm^2/ V.s on sapphire substrate with L_g = 210 nm, L_{sd} = 1.5 μm and named as GFET-B. Considering the device geometry to be symmetrical, access region length is $L_{gs} = L_{gd}$ = 645 nm.

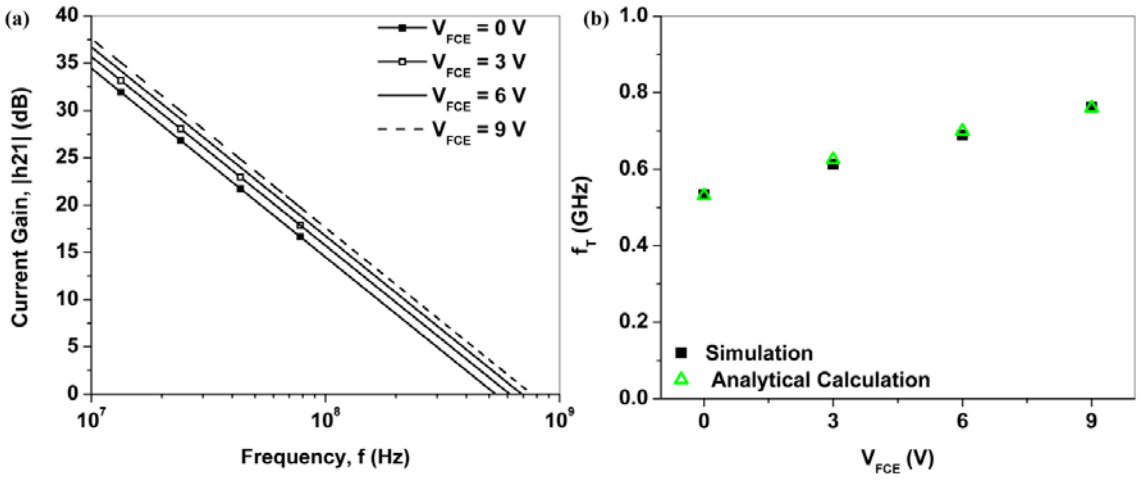

Figure 24: (a) Current Gain |h21| - Frequency relationship of GFET-A with FCEs at different V_{FCE} values in electron regime of operation. (b) f_T vs. V_{FCE} where f_T is calculated using analytical technique and also extracted from (a).

The simulated RF performance of the baseline device presented in Figure 25 is in good agreement with the reported one after de-embedding. f_T and f_{MAX} were extracted as 22.1 GHz and 23.3 GHz, respectively. To improve the RF performance, FCEs are added on bottom of two 645 nm long ungated regions and biased up to ±9.0 V as before not to exceed the breakdown voltage of Al_2O_3 reported in [45]. Graphene hole and electron mobility was considered to be significantly dependent on carrier concentration and their values at different V_{FCE} were estimated using the data in [42] for all analyses.

To determine the optimum FCE length and position for GFET-B, we placed FCEs of different lengths as before and simulated the RF performance. The dependence of f_T over

L_{FCE}, $L_{g\text{-}FCE}$ and $L_{s/d\text{-}FCE}$ shown in Figure 26 reveals that the optimum values of L_{FCE}, $L_{s/d\text{-}FCE}$ and $L_{g\text{-}FCE}$ are 495 nm, 0 nm and 150 nm respectively.

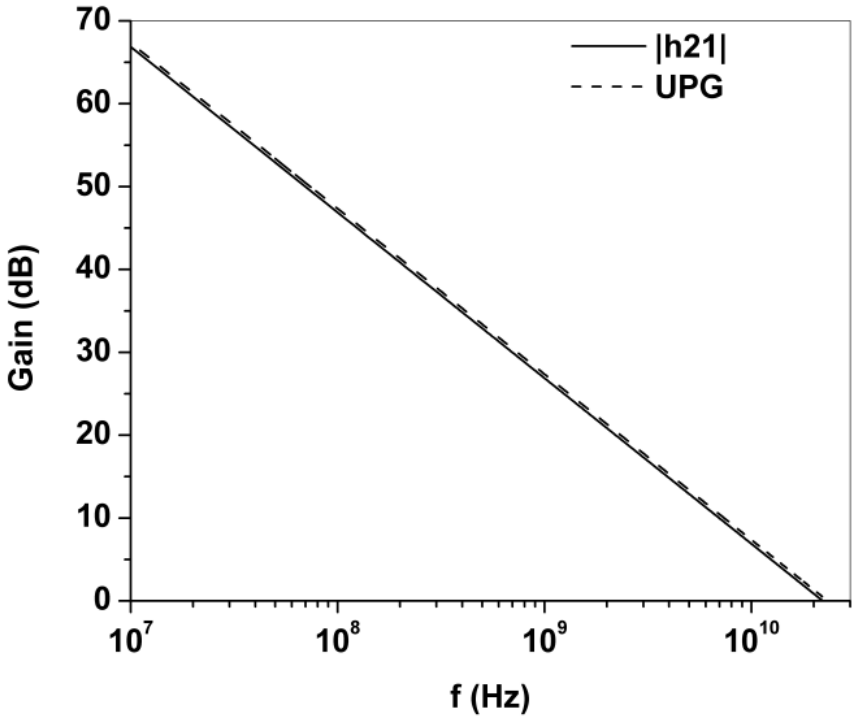

Figure 25: Current Gain and Unilateral Power Gain vs. frequency of the short channel high mobility baseline GFET.

Using the optimum FCE length and position, we estimated the RF improvement in both electron and hole regime of operation using both simulations and analytical technique. Analytical calculation showed that the access resistance of 645 nm long access region with an initial value of 3.66 Ω went down to 2.31 Ω for V_{FCE} = -9 V. In frequency domain AC simulations, a biasing condition of V_{ds}= -1.6 V, V_{gs}= -0.6 V was assumed for hole regime and V_{ds} = -1.6 V, V_{gs} = 1 V was assumed for electron regime.

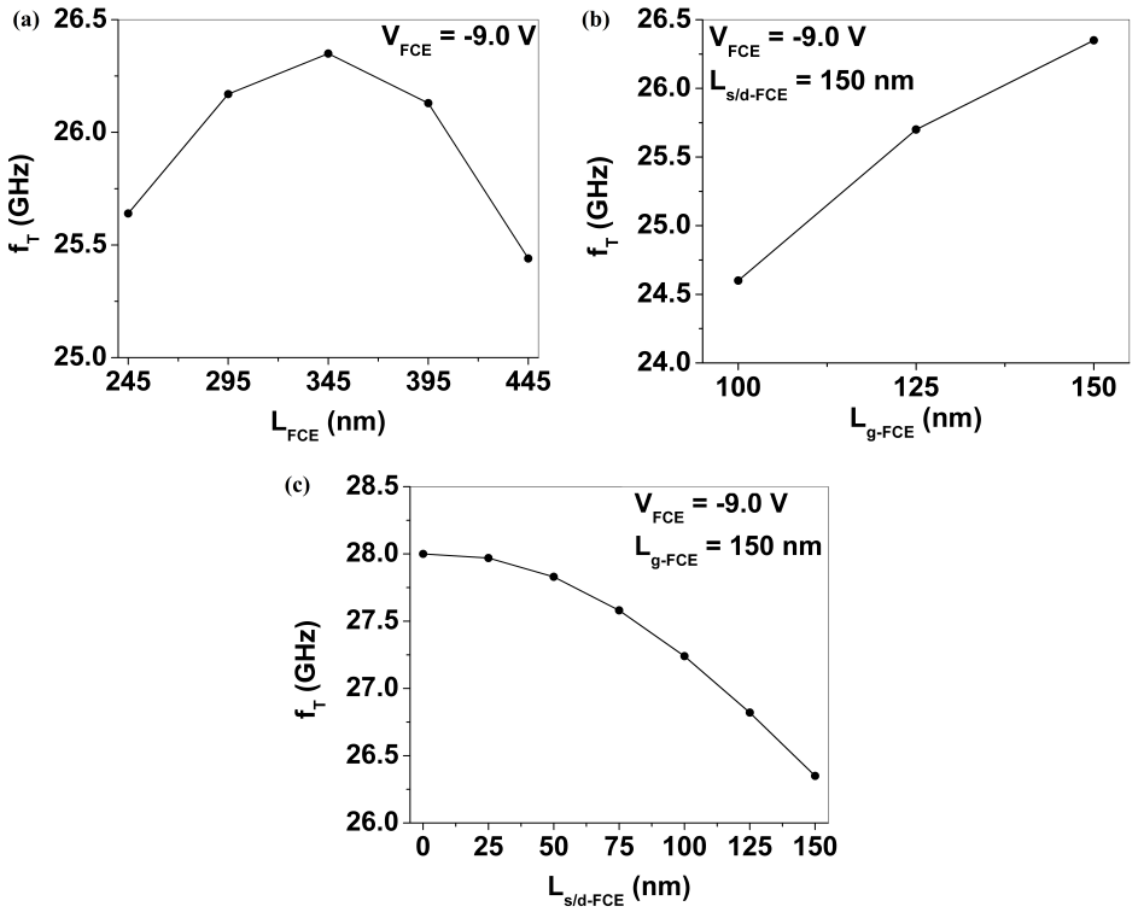

Figure 26: At V_{FCE}= - 9 V (a) f_T plotted against different L_{FCE}. (b) At $L_{s/d-FCE}$ =150 nm, f_T plotted against L_{g-FCE}. (c) At L_{g-FCE} = 150 nm, f_T plotted against $L_{s/d-FCE}$.

The extracted f_T values from the frequency response for hole regime along with those from analytical calculation using modified RF equation for 5-terminal GFET are plotted against V_{FCE} in Figure 27 (a) whereas that for electron regime in Figure 27 (b).

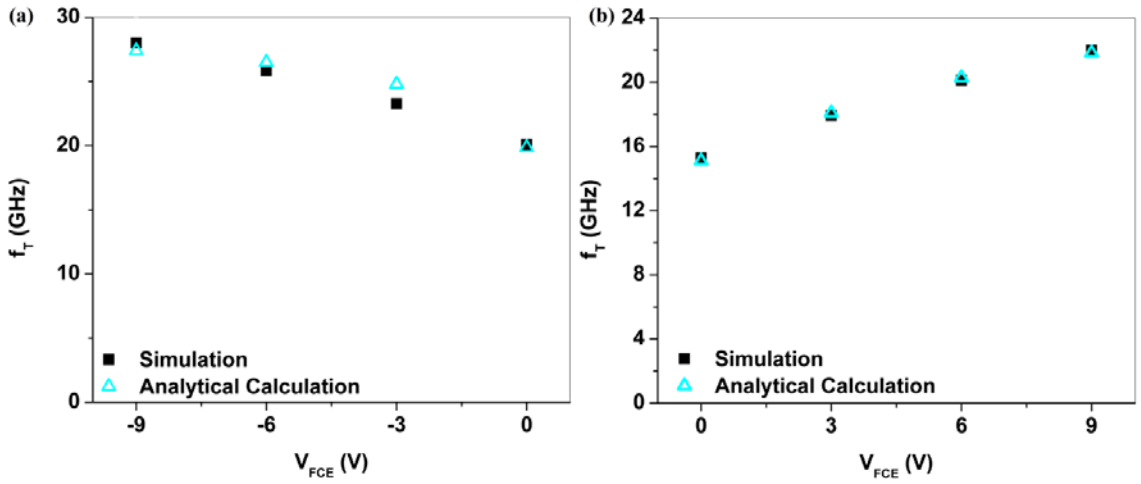

Figure 27: Extracted f_T from frequency response and from analytical calculations plotted against V_{FCE} for (a) hole regime operation and (b) electron regime operation.

2.3.3 Simulation of Hybrid Contact GFET

We aim to add two C3s on this device and short them to the ohmic contacts to extensively analyze its effect on the device's high frequency performance. As a starting point of capacitive impedance simulation, we first simulated a simple capacitor-like structure. It consists of 30nm SiO_2 between two metal contacts and each metal contact has a contact resistance of 0.7 ohm-mm, shown in Figure 28 (a).

The real and imaginary parts of this capacitive impedance are estimated using simulation as well as analytical technique. In Figure 28 (b), the real and imaginary part of capacitive impedance estimated from simulation and analytical calculations are plotted with respect to frequency. We can see that the results using both of the methods are in a very good agreement, which validates our simulation technique of estimating capacitive impedance. For further verification, we successfully regenerated the experimental data for III-N RF TLM structures reported in [38]. To estimate the impedance of the capacitance formed

between a C3 and Graphene channel with Gate dielectric in-between, we simulated a RF TLM structure on Graphene having two C3s with various in-between distances.

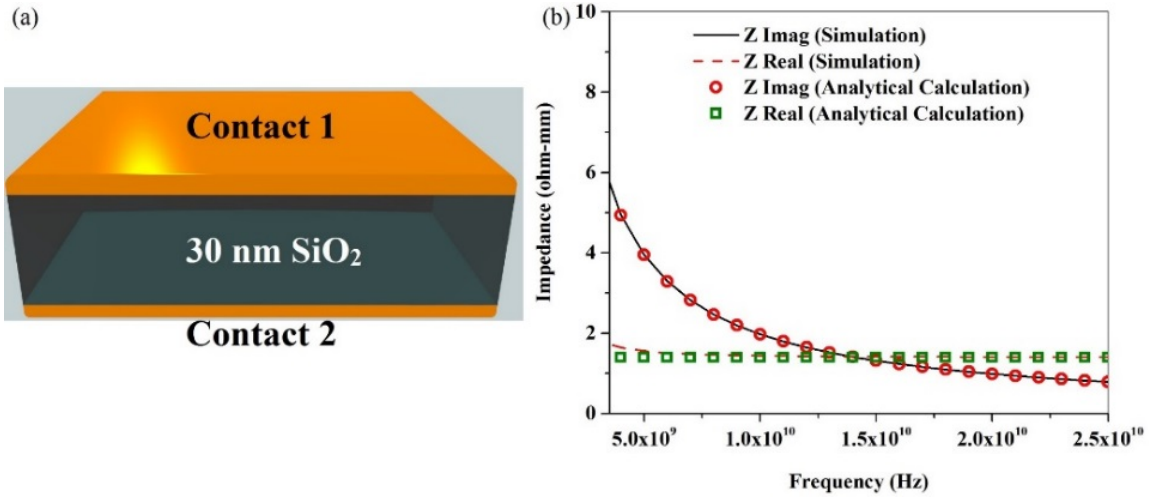

Figure 28: (a) Schematic of the capacitor like structure (b) The real and imaginary part of impedance estimated from simulation and analytical calculation.

The C3s were placed on exactly the same structure, as in baseline GFET-1, consisting of 9 nm SiO_2 and 15 nm Al_2O_3 serving as Gate dielectric deposited on CVD Graphene with carrier mobility same as that of baseline GFET-1, shown in Figure 17 (a). The impedance between contact 1 & 2, 2 & 3, and 3 & 4 were calculated at a specific single frequency, plotted with respect to distance, and extrapolated up to zero distance to extract the real and imaginary part of a single C3 impedance at that frequency. This procedure was repeated over the frequency range of 5 GHz to 25 GHz with a step size of 1 GHz. The real and imaginary part of C3 impedance plotted with respect to frequency is shown in Figure 29 (b).

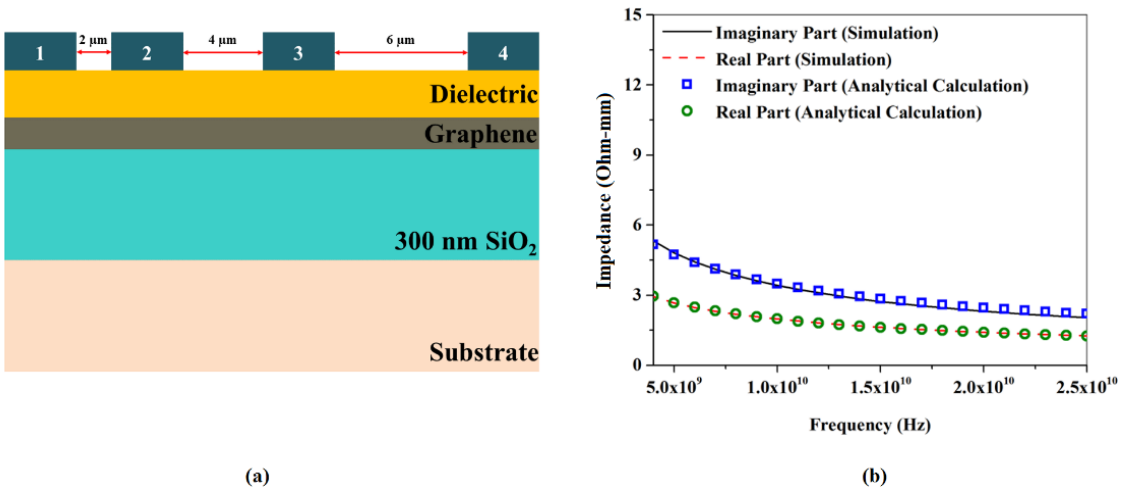

Figure 29: (a) Schematic of RF TLM structure on Graphene. (b) The real and imaginary part of C3 impedance estimated from both simulation and analytical calculations plotted with respect to frequency.

Finally, we simulated the proposed GFET which has two C3s shorted to the ohmic Source/Drain contacts of the already simulated baseline GFET-1, shown in Figure 30. The length of capacitively coupled extension was 0.8 µm in this simulation. The Current Gain, |h21| of the baseline GFET-1 and the proposed modified version with C3s are plotted with respect to frequency in Figure 31 (a). According to definition, the frequency at which current gain becomes 0 dB is the current gain cut-off frequency, f_T. We can see from Figure 31 (a) that for a C3 length of 0.8 µm, the f_T of this proposed GFET reached a value of 0.78 GHz whereas that for the baseline GFET-1 was 0.74 GHz. In each and every numerical calculation, the gate to source/drain parasitic capacitances have been considered. In addition to that, in analytical calculations, the parasitic capacitances have been estimated using geometric and material parameters. The value of these parasitic capacitances ranged from 3.90×10^{-13} F to 4.40×10^{-13} F.

The drain to source voltage as well as the drain side C3 to source voltage, V_{ds} was 5.0 V during frequency domain AC simulation. As the drain bias as well as the drain side C3 bias is positive, we considered the GFET electron regime operation so that the drain side C3 bias accumulate more major carriers (electrons) underneath. A Gate bias of V_{gs}=2V was used to operate the GFET in electron regime.

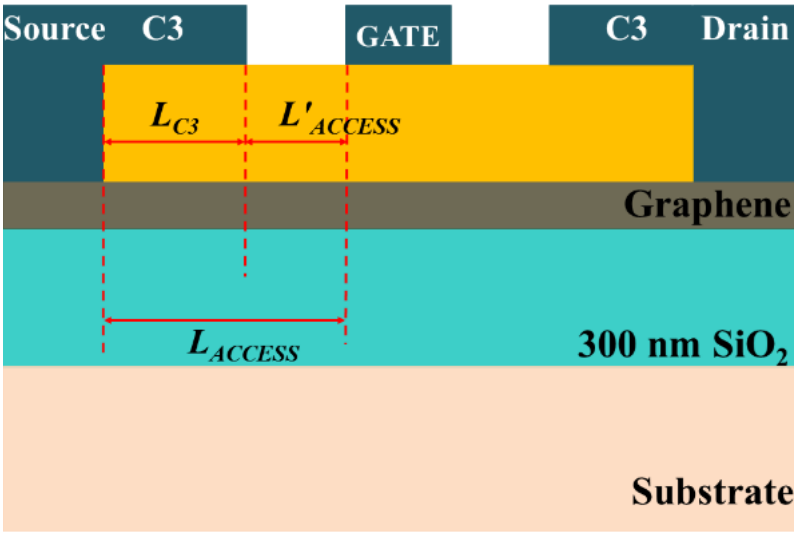

Figure 30: Schematic of the proposed GFET (not in scale).

We later gradually increased the length of C3s. The approaching C3 towards Gate reduced access region length as well as access resistance. Also the increment of capacitive coupling area due to C3 length increment decreased capacitive impedance. As a result of access resistance decrement as well as the decrement of capacitive impedance, the f_T of the proposed GFET further increased. The effect of increased C3 length over f_T for this device is shown in Figure 31 (b) estimated from both simulation and analytical calculation. We can find from Figure 31 (b) that the f_T of this proposed device reached a value of 0.89 GHz for a C3 length of 1.4 μm whereas it was just 0.78 GHz for C3 length of 0.8 μm before.

Further increment of C3 length was studied and due to introduction of high parasitic capacitance, that resulted in f_T deterioration.

As the C3 impedance is dependent on frequency and from our results in Figure 29 (b), it was found that the real part of C3 impedance is reduced at higher frequencies; we intended to quantify the effect of C3 on RF performance of a shorter channel higher mobility GFETs. To do so, as before, a short channel high mobility GFET reported in [34] was chosen as our short channel high mobility baseline and named it as GFET-2.

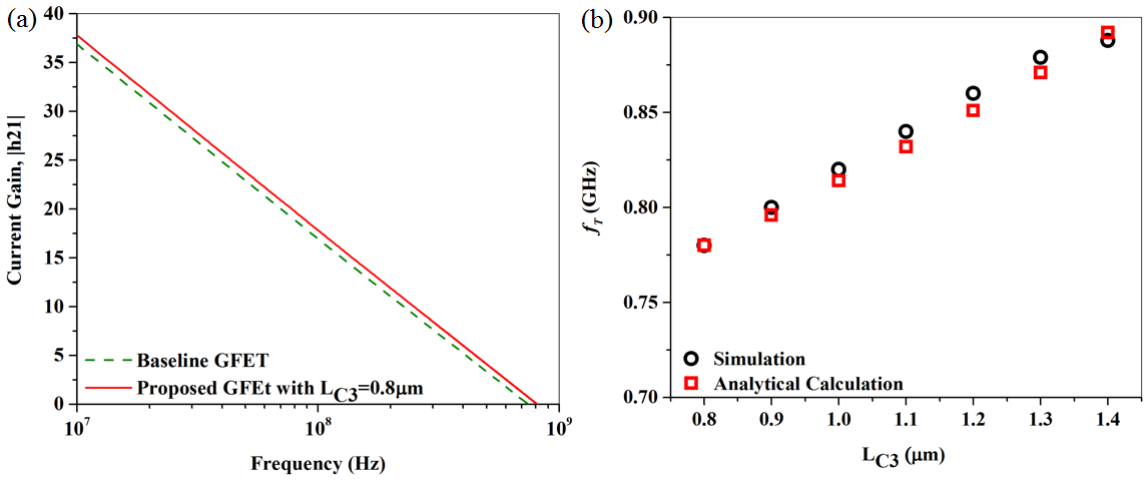

Figure 31: (a) Current Gain, |h21| of the baseline GFET-1 along with that of the proposed hybrid contact GFET in electron regime (V_{gs}=+2.0 V and V_{ds}=+5.0 V) plotted with respect to frequency (b) The current gain cut-off frequency (f_T) of the proposed GFET extracted from |h21|vs *f* characteristics, plotted with respect to L_{C3}.

The device has CVD-grown Graphene channel with carrier mobility of μ = 2234 cm^2/ V.s on sapphire substrate with gate length of 210 nm, Source to Drain distance of 1.5 μm. We considered the device geometry to be symmetrical and estimated the access region length to be 645 nm on each side of the Gate. We simulated the DC and RF characteristics of the baseline GFET-2 as before and they were in a very good agreement with the reported data [34]. For this simulation as well as for the following simulations and analytical

calculations, the device width was considered to be 100 μm as before. Later we simulated our proposed short channel high mobility GFET with hybrid contact by making a capacitive extension of 245 nm of both Source and Drain towards Gate.

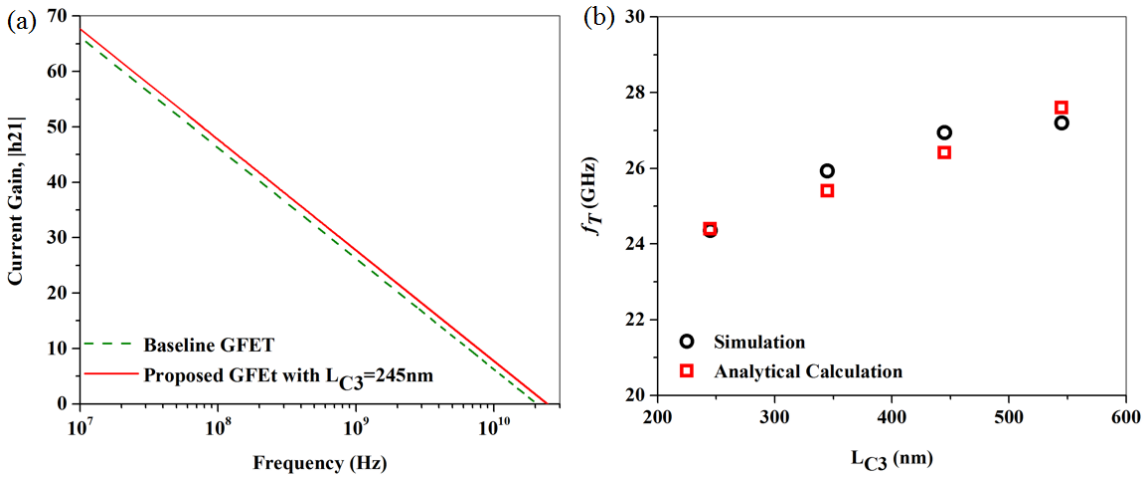

Figure 32: (a) Current Gain, |h21| of the baseline GFET-2 along with that of the proposed hybrid contact GFET in electron regime (V_{gs}=+0.6 V and V_{ds}=+1.6 V) plotted with respect to frequency (b) The current gain cut-off frequency (f_T) of the proposed GFET extracted from |h21|vs *f* characteristics, plotted with respect to L_{C3}.

The RF characteristics of the baseline GFET-2 in electron regime along with that of the proposed GFET having a C3 length of 245 nm are shown in Figure 32 (a). From Figure 32 (a), we see that the f_T of the baseline reported GFET and proposed GFET with 245nm capacitive extension are 20.05 GHz and 24.4 GHz respectively. Later the C3 length was gradually increase up to 550 nm as shown in Figure 32 (b). Due to the increment of C3 length, the f_T gradually increased and eventually reached a value of 25.9 GHz. As before, further increment of C3 length was studied and L_{C3}=550 nm was found to be the optimum extension.

In addition to the C3 extension over the access region, we also simulated a GFET with the source to drain distance same as that of the baseline, but with a longer gate. The new length

of gate was equal to old gate length plus $2L_{C3}$, $L_{g\text{-}new}=L_{g\text{-}old}+2L_{C3}$. From our simulation, we found that this device does not show any improvement of f_T, rather the f_T deteriorates compared to the baseline GFET. The reason behind this deterioration is the increment of transit delay. Though the C3 is capacitively coupled to the channel as like as the gate contact, the switching of the device takes place in gate, not in C3s. The increment of the gate length increased the transit delay, whereas the equal C3 extension length reduced the parasitic delay.

2.4 Fabrication/Integration of GFET:

2.4.1 Theory of Microfabrication:

The proposed GFET with two additional contacts was fabricated jointly in a class 100 clean room of The Advanced Materials Engineering Research Institute (AMERI) at Florida International University and Nanoscale Research Facility (NRF) at University of Florida. The microfabrication involved processes including e-beam lithography, photolithography, e-beam evaporation, atomic layer deposition, and reactive ion etching. In conventional GFET fabrication process, the first step is transfer of Graphene on a suitable substrate, followed by patterning device mesa and source/drain contacts. The pattering of Graphene mesa as well as the patterning of source/drain contacts involve lithography, requiring the Graphene to be exposed to resists and developer several times. It is well known that Graphene is very much prone to contamination from resists and solvents [46], and the more it is exposed to contamination, the more the key feature of Graphene— mobility, degrades. Rather than following the conventional sequence of GFET fabrication steps starting with Graphene transfer and mesa etch, and ending with gate patterning, here we started the

process by firstly pattering gate-FCE on the substrate, then oxide deposition and patterning, followed by source/drain patterning, and finally Graphene transfer followed by mesa etch. As a result, starting from the Graphene transfer ending with mesa etch, Graphene was never exposed to resists and developers, and prevented from the consequential contamination.

2.4.1.1 Lithography

Lithography is the process of transferring geometric pattern on the surface of a substrate wafer. The geometric pattern is transferred on a layer of resist which is coated on top of the wafer or a chip. When the coated resist is exposed to ultraviolet light (photolithography) or electron beam (e-beam lithography), it changes it physical properties in such a way that the exposed (positive resist) or unexposed (negative resist) part of the resist dissolves in the developed during the development process. The exposure of resist can be done in 2 ways: selectively obstructing light by using a mask, or direct writing where the writing head exposes the resist according to the design file. The lithography process includes the following steps:

2.4.1.2 Substrate Preparation

The basic intension behind surface preparation is to improve the adhesion of resist on the wafer/chip surface. The first step of surface preparation—surface cleaning, is done to remove organic and inorganic contaminants. Widely used solvents for surface cleaning are Acetone, Isopropyl Alcohol, and Methanol. After cleaning with solvents, it is washed with deionized water and baked at more than 100 °C for a few minutes to dehydrate. If the

surface is hydrophilic, adhesion promoters such as hexamethyl disilizane (HMDS) is used to improve adhesion.

2.4.1.3 Resist Spin Coat

Resist is a material which is sensitive to radiation, UV for photolithography and e-beam for e-beam lithography. For photolithography, the resist that is used is sensitive to ultra violet light and is called photoresist. On the other hand, e-beam resist is sensitive to electron beam and used in electron beam lithography. In general, it contains inactive resin, solvent, and photoactive compound. When a resist polymer and electromagnetic radiation interact, two different types of chemical reactions can take place: (1) cross-linking (2) chain scission. The second one is also referred as fragmentation. In case of negative resists, cross-linking takes place, whereas, chain scission takes place with positive resist. In cross-linking, after interaction with incoming radiation, the atoms in adjacent chains of the get displaced and the carbon atoms bond directly, resulting in a material not dissolvable in developer. On the other hand, radiation disrupts the polymer chains of positive resists, breaking them up to smaller pieces, and makes a material, very fast dissolvable to developer. The spin coater tool consists of a spinner chuck which holds wafer by vacuum and its spin speed (RPM), ramp, and spinning time can be set by user.

2.4.1.4 Baking:

After coating the substrate with resist, the coated resist film contains remaining solvent concentration, and is baked on hot plate before exposure. The baking reduces the quantity of remaining solvent content to avoid mask contamination and sticking to the mask, prevent

popping or foaming of the resist by N_2 created during exposure, improve resist adhesion to the substrate, minimize dark erosion during development, prevent dissolving one resist layer by a following multiple coating, and prevent bubbling during subsequent thermal processes (coating, dry etching). Baking can be divided in to two types: soft baking and hard baking. Immediately after resist coating, soft baking is done. On the other hand, had baking is the last step of lithography, done after exposure and development, in order to harden the photoresist and improve adhesion to the wafer surface.

2.4.1.5 E-beam Direct Writing:

Once the substrate is coated with e-beam resist, direct e-beam writing is performed. Patterning techniques other that UV lithography including electron beam lithography and x-ray lithography are developed due to two driving forces. They are: higher resolution (smaller feature size) and cost. The maximum achievable resolution of a UV lithography system is limited with the wavelength of the beam. Conventional photolithography systems, which rely on UV light, can therefore achieve a minimum “diffraction-limited” feature size of several hundreds of nanometers and can be improved using advanced resolution enhancement techniques (RET). However, RET for photolithography increases cost and cycle time of masks along with increment of complexity for technology nodes. An electron’s velocity and kinetic energy are related by the following equation:

$$E_{kin} = \frac{1}{2} m v^2 \tag{30}$$

And the de Broglie wavelength for electrons with kinetic energy E_{kin} can be expressed as:

$$\lambda = \frac{h}{\sqrt{2mE_{kin}}} = \frac{1.23}{\sqrt{E_{kin}}}[nm] \quad (31)$$

It states that an electron accelerated to an energy of 10 keV would have a wavelength, λ=0.12 Å. This clearly shows that e-beam lithography has a huge advantage over current optical lithography systems, which are limited by their wavelength.

Modern sophisticated electron beam lithography (EBL) systems have the same fundamental parts in common including electron sources, electron lenses, beam deflector, aperture, beam blanker, stigmator, and stage. EBL patterning is performed in a high vacuum chamber. The sample is mounted on a wafer holder consisting of a set of test standards for calibration, focusing, and position. Calibration subroutines can be performed before the actual writing or during the writing. The stage is moved by piezoelectric motors and the position is controlled by laser interferometry system. The use of laser interferometry system ensures to achieve nanometer-scale precision. To isolate mechanical vibration from the system, the stage is also placed on a vibration isolation system. In some of the systems, there is an additional charge coupled device camera inside the chamber to assess the control of sample positioning.

2.4.1.6 Photo Mask Writing

Photo mask consists of a glass, one side covered with chrome, and the chrome is covered with a photo resist. The pattern information, to be transferred on a wafer or chip, is created in a drawing package and generally stored in a database. The design file is then reformatted and transferred to a direct writing tool, which is generally named as Mask Maker.

According to the drawing file, the mask maker exposes selective part of the photoresist on mask. The imaged pattern on the mask is then developed to form a template over the opaque chrome and put in chrome etchant to etch away chrome where the resist is clear. Once the chrome is etched away, the remaining photoresist is removed, cleaned and stored for later use, in a mask aligner tool.

2.4.1.7 Mask Alignment and exposure:

In a multi-layer device fabrication/integration process, the first layer does not require any alignment, but the subsequent layers require to be aligned to the preceding layer. To aid the alignment process, each layer is accompanied by some features which help to align the mask for the next layer. These features are called alignment marks and these marks are transferred on the wafer in such a way they can be easily seen through a microscope of the mask aligner tool on the surface of the wafer and the photomask. The alignment marks are generally etched into the wafer after a previous photolithography step and it is required of the lithography to know what marks on the wafer are supposed to line up with what marks on the mask - which can get complicated after several masking steps. The mask alignment procedure starts with loading of the mask and the wafer in the aligner tool. The wafer vacuum stage on which the wafer is placed can be moved in x-dierection, y-direction, and can be rotated (θ). Using these knobs, the wafer is aligned to the fixed mask using a microscope. Once the alignment is done, the wafer is brought to contact with mask. Following the mask alignment and contact, the UV source power is measured, exposure time is calculated and the wafer is exposed.

2.4.1.8 Development

Once exposed, the wafer is removed from the stage and put into a solution named developer. The developer is a chemical that removes the exposed (unexposed) part of the positive (negative) photoresist coated on top of the wafer. The concentration of the developer and development duration need to be estimated during process development. After development, the wafer is rinsed with DI water and dried with N2 for subsequent steps.

2.4.1.9 Descum:

This procedure is used to remove residual photoresist from the arears where photoresist is removed by developer. The thickness of such residual photoresist film is generally less than 1000 Å, but its interference can very detrimental in the subsequent processing, especially if the pattern geometry is very small. A low power short time reactive ion etching is generally used to remove these residues.

2.4.1.10 Reactive Ion Etching:

The reactive ion etching (RIE) uses chemically reactive plasma generated at the presence of RF power under a low pressure (10-100 mTorr) to consume the material on wafer, in addition to ionic bombardment. In the RIE system, the wafer is placed on a chuck which is grounded, and another electrode on top of the grounded chuck is connected to RF source. Generally the frequency of the RF source is 13.56 MHz. As the electrons are lighter compared to ions, they move faster, collide very frequently and as a result, is removed of the plasma. The positively charged plasma forms a DC electric field. In addition to

chemical reaction between the plasma and target material, the positive ions can be accelerated by applied electric field and can physically bombard the target as well. This process of physical bombardment can also assist the etching process. In contrast to wet etching, RIE can move the etchant in the direction of applied electric field and produce anisotropic profile.

2.4.1.11 E-beam Evaporation

The electron beam evaporation system is used to produce uniform high-purity thin films. It is used to evaporate refractory and dielectric materials, as well as the more common conductive and semiconductor materials. Electron beam heating is an efficient way to achieve high temperatures for uniform thin film, optical coating and vacuum metallurgic processes. The e-Gun is a self-accelerated electron beam device, held at a high negative potential, which is produced by the hot tungsten filament. The beam of electrons leaves the filament and then magnetically focused. The evaporant material is put in a crucible and the crucible is placed in a pocket where it is grounded and water cooled. The beam strikes the evaporant material with a set spot size and intensity. Using an electro-magnetic system, the electron beam can be swept over the evaporant material. The material deposition rate can be changed by tuning input power, charge size, charge shape, and the characteristics of the material to be evaporated. Material with low evaporation temperature and high thermal conductivity can be evaporated with highest evaporation rates. In this process, the evaporant are not contaminated because the focused electron beam strikes only the evaporant source material in the crucible. The e-Gun source generally operates in a high vacuum chamber and the magnitude of chamber pressure, which normally increases during

evaporation, depends on the pumping capacity of the system and the cleanliness of the evaporant material.

2.4.1.12 Lift-off:

Lift-off is a method of patterning deposited thin films which are difficult to pattern by dry etching. The pattern is transferred on the substrate using standard photolithographic process followed by descum. The thin film is blanket deposited on top of the whole substrate which covers the photoresist as well as the areas where photoresist has been removed to open windows. As a result, at the windows, the film is deposited on the substrate, whereas, in rest of the areas, it is deposited on photoresist. During lift-off, the thin film covered substrate is put in a solvent that removes the photoresist as well as the thin film deposited on top of photoresist, leaving behind the film deposited directly on substrate.

2.4.1.13 Graphene Transfer

CVD Graphene grown on Copper sheet is coated with PMMA and put floating on a suitable copper etchant without any disturbance while copper surface touching the solution. Once the copper is completely etched, it is washed with DI water multiple times without flipping, and eventually transferred on suitable substrate. After being transferred, the sample is put in a desiccant to remove water molecules and then put in a suitable solvent to remove the PMMA.

2.4.2 Fabrication of GFET: Process Details

A 300 nm SiO_2 on top of N-type Silicon was chosen as substrate of the device. The substrate was cleaned with acetone/IPA/methanol, rinsed with DI water, and dried with N_2 flow. The sample was then baked at 100 ºC for 3 minutes to remove solvent remnants. The fabrication process consists of a total of 6 different layers, and the layout design of these layers was done using Layout Editor.

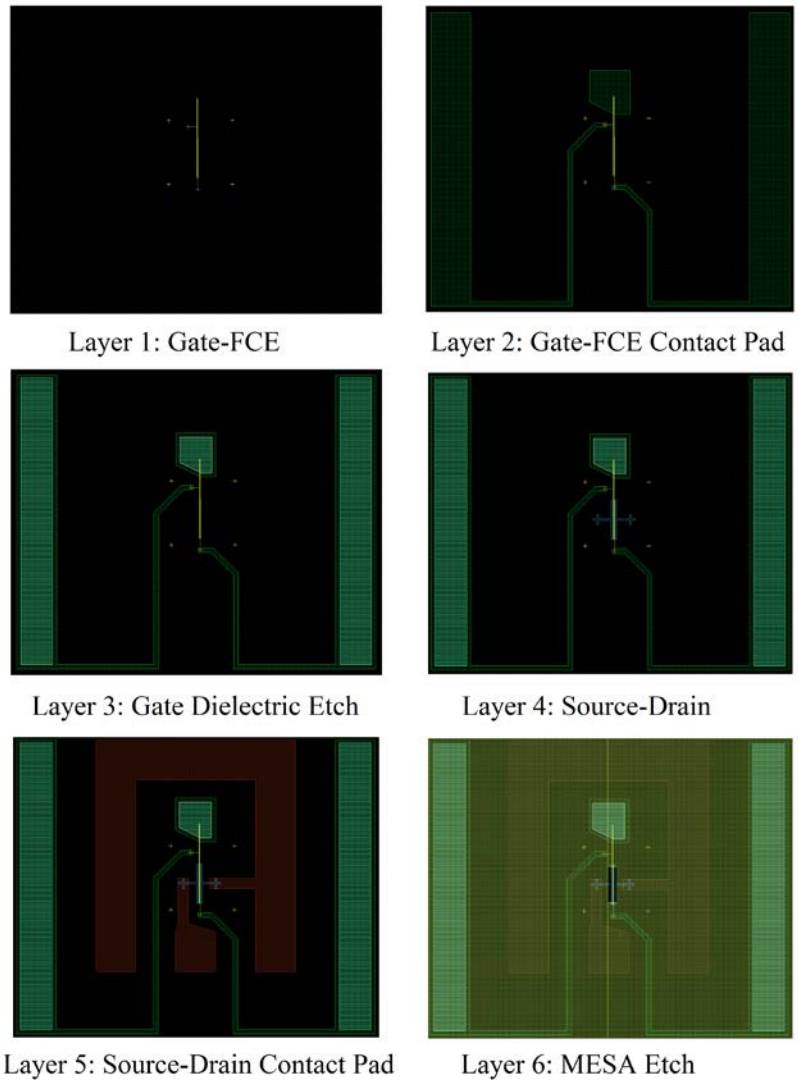

Figure 33: Layout design of 6 different layers.

The layout design of the 6 different layers is shown in Figure 33. 200 nm of 950 PMMA A4 was spin coated (200nm thick, static pour, at 500 RPM for 5s, then 4000 RPM for 45s) and oven baked at 185 ºC for 30 minutes. The Gate-FCE layer with alignment marks were patterned using e-beam lithography. For e-beam writing, 15kV beam voltage was used at a dose of 18 0uC/Cm^2, with a step size of 25 nm, column aperture of 30 um, and a write field of 200 um. It was developed in a solution of MIBK: IPA=1: 3 for 30 seconds at 4 ºC using a chiller plate. 10-nm Ti/40-nm Au was evaporated using e-beam evaporator at a chamber pressure of 2×10^{-7} mTorr and lifted-off in acetone, in a standard sonic bath, by sonicating for 1 minute. Figure 34 shows the optical image of gate-FCE along with the alignment marks after lift-off.

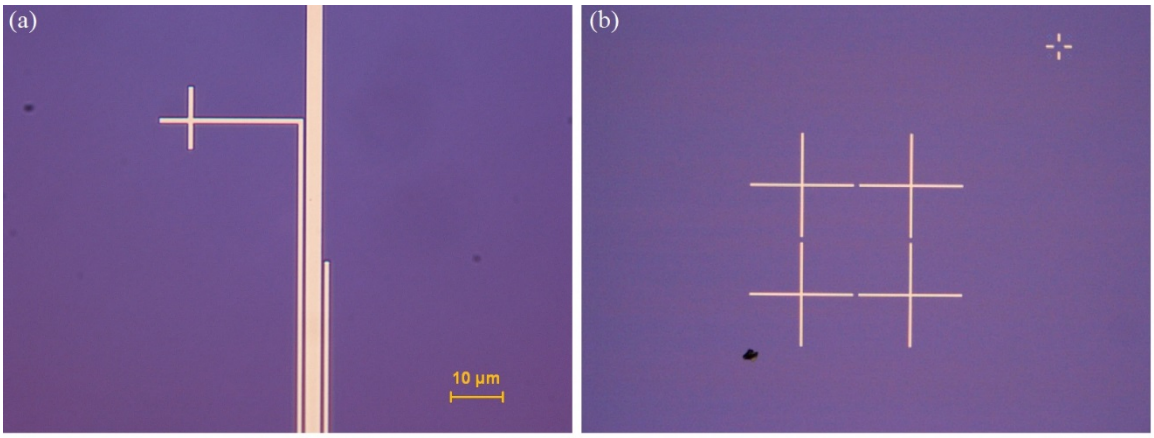

Figure 34: Optical microscope image of (a) Gate-FCE layer after metallization and lift-off (b) Alignment marks for mask alignment after metallization and lift-off.

The next layer was the pads. The substrate with Gate-FCE layer patterned and metalized is then coated with 600 nm LOR 3B (Step 1: 500 RPM/100 Ramp, 5 s; Step 2: 1000 RPM/500 Ramp, 60 s) on top of 600 nm S1805 photoresist (Step 1: 1500 RPM/300 Ramp, 5 s; Step 2: 3000 RPM/500 Ramp). The LOR 3B lift off resist and S1805 photoresist were cured on

a hotplate at 180 ºC (10 minutes) and 115 ºC (3 minutes), respectively. Photo mask for the Gate-FCE pad layer was written using mask maker and aligned on the patterned substrate using a mask aligner. After exposing with UV, it was developed in developer MF-26A for 15 minutes, rinsed with DI, dried with N_2, and a descum was done by oxygen plasma etching for 15 seconds. 10-nm Ti/500-nm Ni was evaporated for pad layer metallization and lifted-off in Remover-PG without sonication. The optical microscope image of the sample after lift-off is shown in Figure 35 (a).

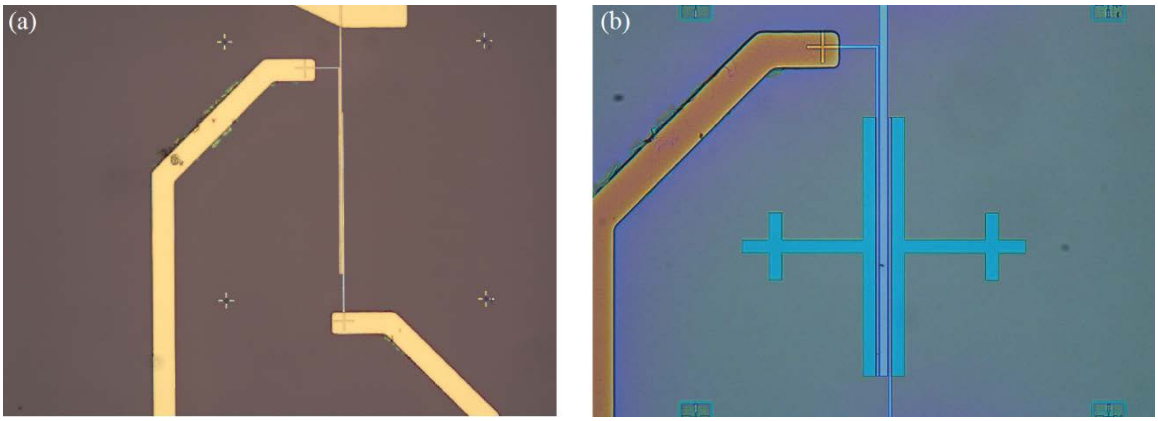

Figure 35: Optical microscope image of (a) Gate-FCE pad layer after metallization and lift-off, (b) Source/drain layer after metallization and lift-off.

Following the Gate-FCE layer and pad layer formation, 20 nm HfO_2 was deposited by ALD, as gate dielectric. Then it went through the same photolithographic process with mask to open windows for the pads. The 20 nm dielectric above the pads was etched by reactive ion etching (Chlorine + Argon) through the windows. For the Source-Drain patterning, the same e-beam lithographic process was used and 10-nmTi/50-nm Au was evaporated, followed by the same lift-off process in sonic bath. The image of the chip after source/drain metallization and lift-off is shown in Figure 35 (b). Source-Drain pad layer

was patterned by the photolithographic process used for Gate-FCE pad layer, followed by a 10-nm Ti/500-nm Au evaporation, and lift-off.

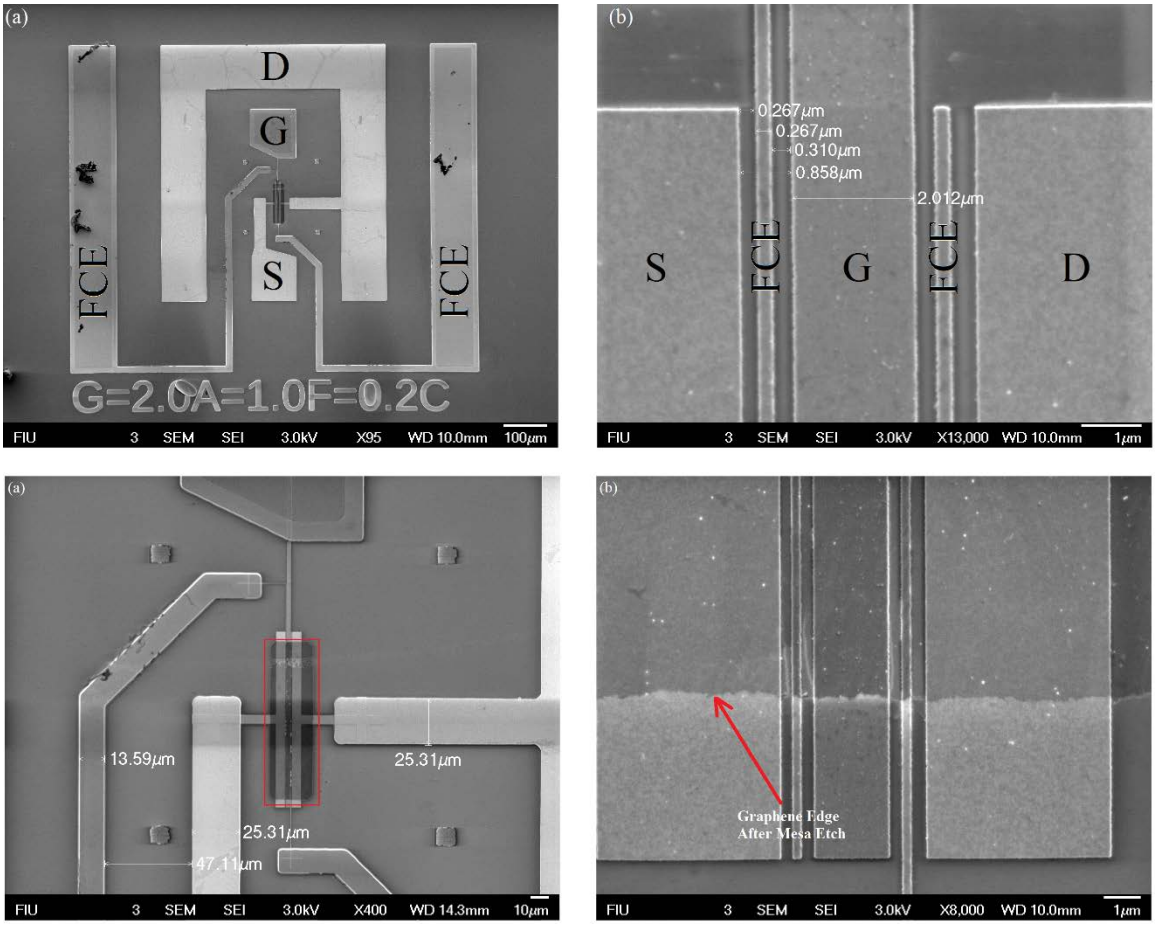

Figure 36: (a) SEM image of the GFET with source, drain, gate, and FCEs marked. The letters S, D, and G stand for source, drain, and gate respectively. (b) High magnification image of the device with embedded scale showing FCE length, gate length, and access region length, (c) The Graphene channel after mesa etch, marked with red rectangle, (d) a closer view of the Graphene channel edge.

Single layer CVD Graphene grown on Copper sheet was coated with PMMA using a regular spin coater and was put floating on $FeCl_3$ solution for 8 hours without any disturbance while copper surface touching the solution. Once the copper was completely etched, it was washed with DI water multiple times without flipping, and eventually was transferred on the patterned substrate. After transfer, the sample was put in a desiccant for

8 hours. Graphene covered with PMMA was then coated with S1805 photoresist and went through the same photolithographic process with mesa mask, to open windows for mesa etch, through which oxygen plasma etching was used to etch PMMA and Graphene. Figure 36 shown the SEM image of the GFET after fabrication at low and high magnification at different regions. After mesa etch, the sample was put in acetone at 50 ºC for 15 minutes to remove PMMA over the Graphene channel. The simplified process flow is shown in Figure 37.

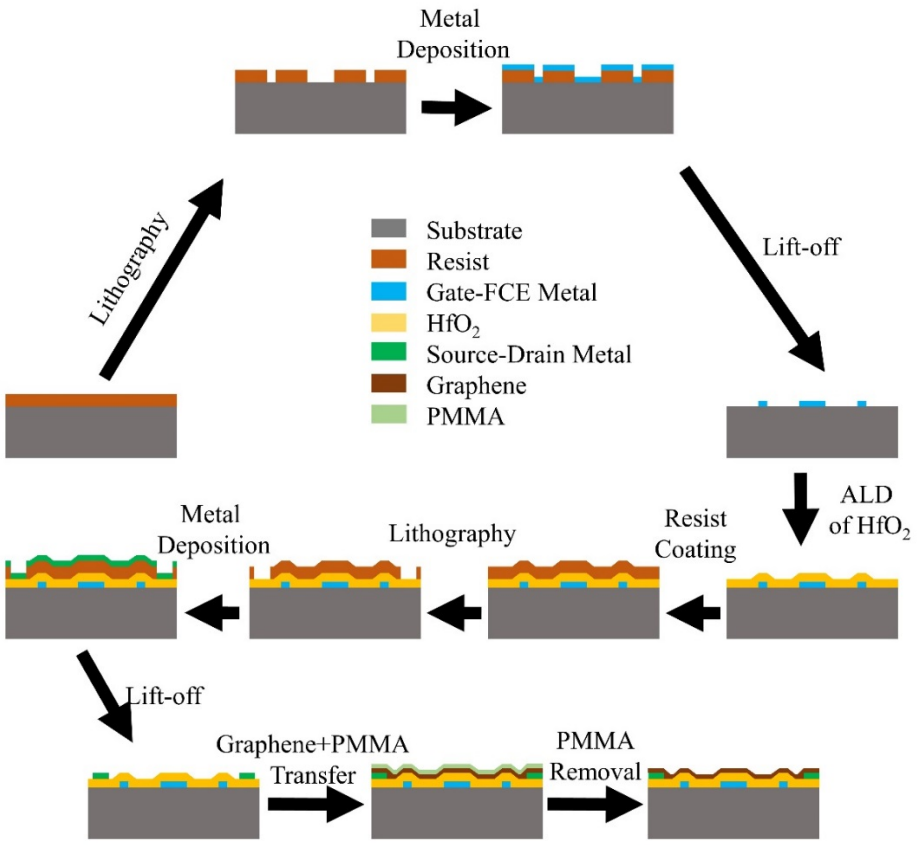

Figure 37: Simplified process flow of GFET fabrication/integration

2.5 Characterization of GFET

The Graphene channel was characterized by Raman spectroscopy. Figure 38 shows the Raman spectrum of the Graphene taken using a 532 nm laser with a spot size of 1 μm^2. The 2D/G ratio (0.93) of the Raman spectrum confirms the presence of single layer Graphene.

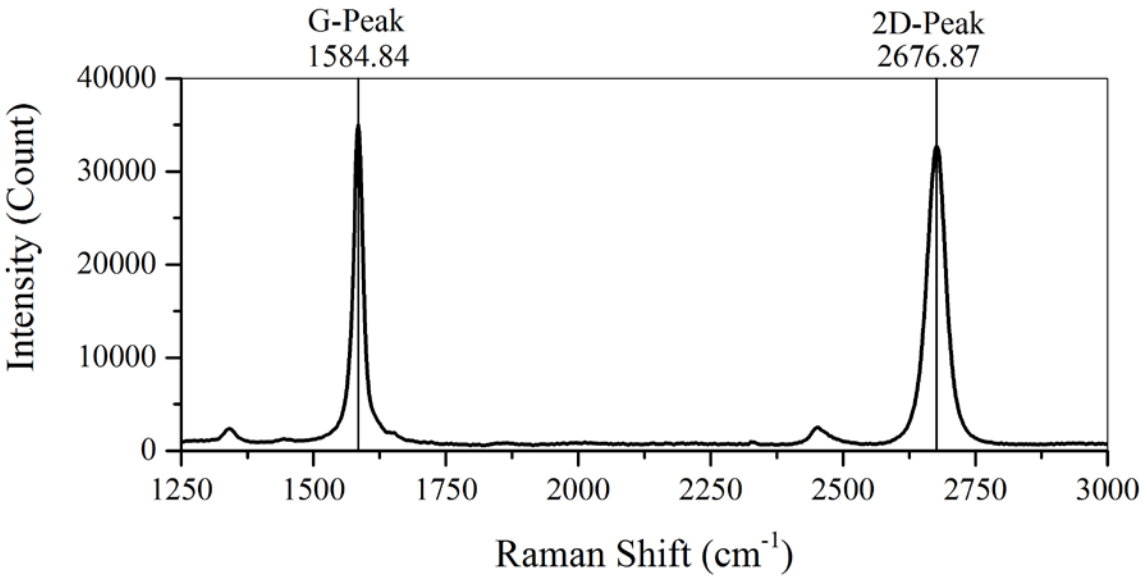

Figure 38: Raman spectrum of single layer Graphene forming FET channel

The DC characteristics of the fabricated device was measured using a HP 4156 A semiconductor parameter analyzer integrated with a probe station. Figure 39 (a) shows the drain voltage vs. drain current characteristics with different FCE biases starting from 0 V to -6.0 V, applied on both of the FCEs, with a step size of 2.0 V. In Figure 39 (b), the gate voltage vs drain current characteristics is plotted for different FCE biases, as well. From the transfer characteristics, it is evident that the Dirac point was not reached up to +8.0 volts. It implies that the Graphene had unintentional p-type doping during growth/transfer.

From the I_d-V_d characteristics, as well as the I_d-V_g characteristics, it is evident that the additional DC bias applied at both of the FCEs result in decrement of access resistance, which eventually increases Drain current.

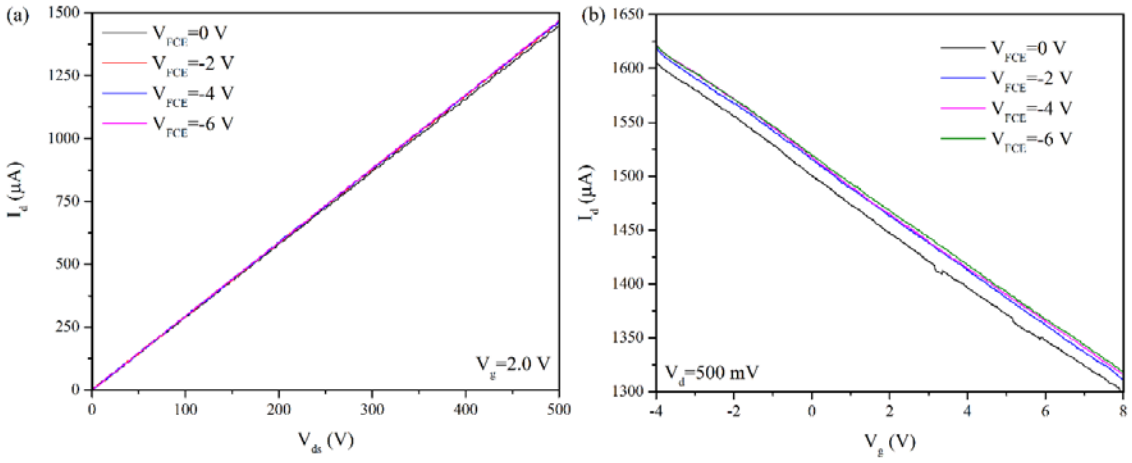

Figure 39: (a) The Id-Vd characteristics of GFET at different V_{FCE} (b) The Id-Vg characteristics of GFET at different V_{FCE}.

The gate leakage current of the device is plotted in logarithmic scale and shown in Figure 40. The leakage current was at the order of a pA.

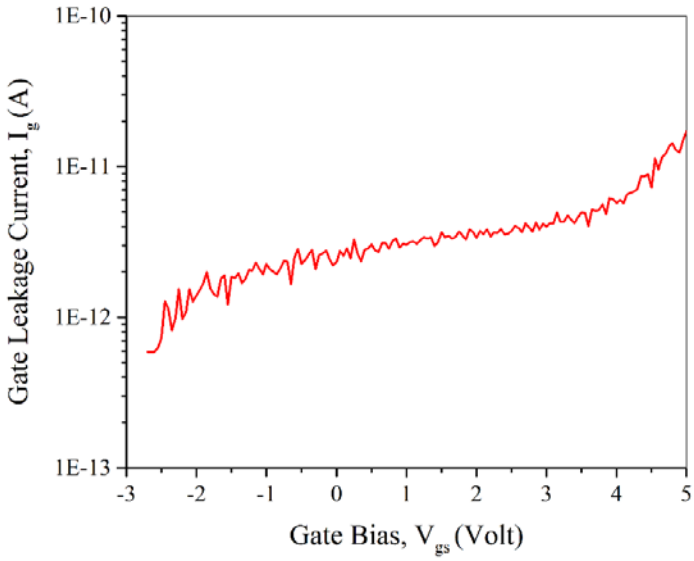

Figure 40: Gate leakage current

In addition to gate leakage current, the FCE leakage current was measured as well. The FCE leakage current was at the order of pA as well, as shown in Figure 41. Low gate leakage current as well as low FCE leakage current is important for good RF performance.

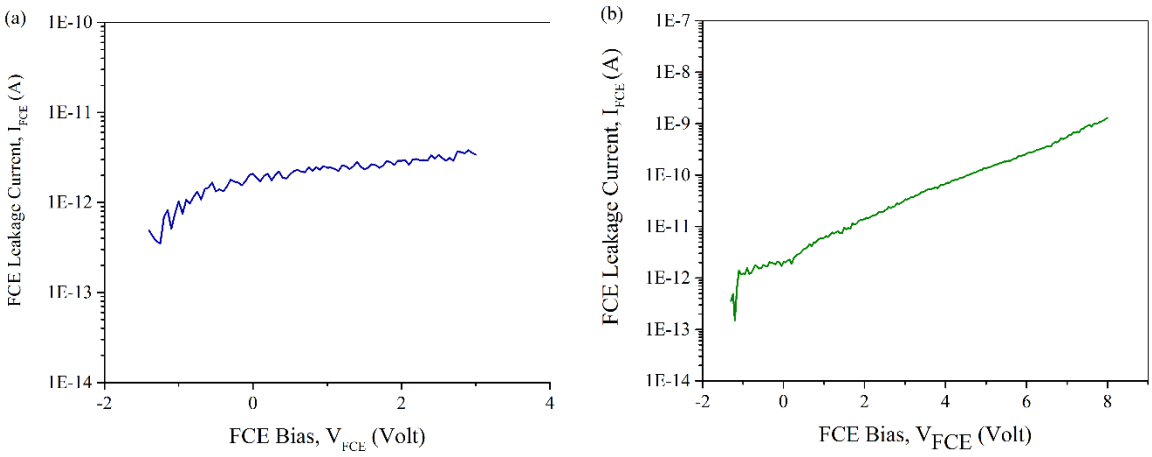

Figure 41: Leakage current of (a) FCE-1 and (b) FCE-2

The RF characteristics of the GFET was measured using a vector network analyzer HP 8510 C integrated with a probe station from J micro Technology with two coplanar waveguide probes (50A-GSG-200-DP) from GGB Industries. The schematic of the setup is shown in Figure 42.

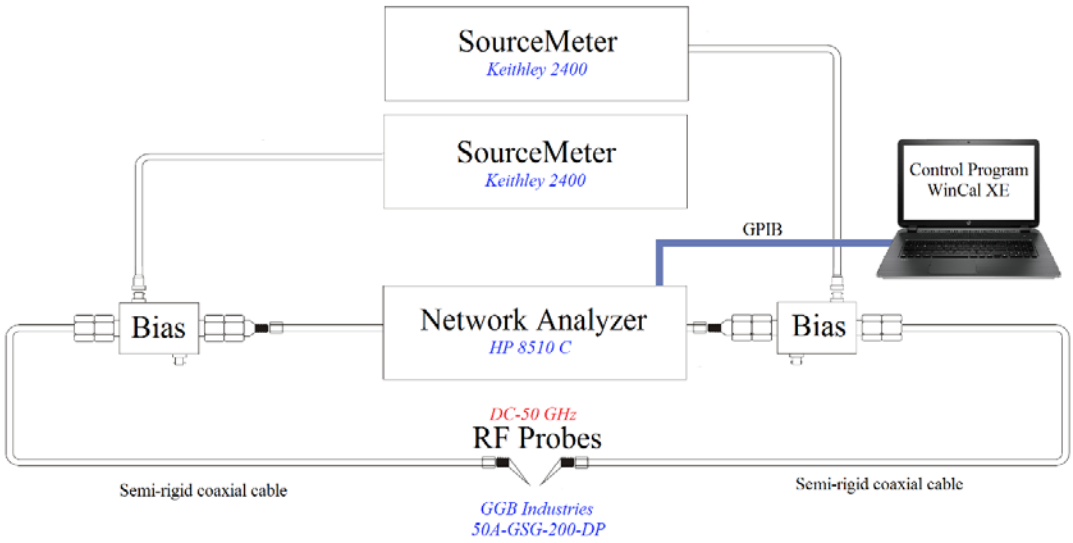

Figure 42: Schematic of the S-parameter measurement setup

Two 24" long low loss phase stable semi-rigid coaxial cable with one 2.4mm Female connector and one 2.4mm Male connector were used to connect the probes. DC bias was applied using two bias tees PE1610 from Pasternack and two Keithley 2400 SourceMeters. Standard Short-Open-Load-Thru (SOLT) calibration was performed using a clabration substrate CS-5 from GGB Industries, before measuring the 2-port S-Parameters. The network analyzer was controlled by a comprehensive and intuitive on-wafer RF measurement calibration software named WinCal XE from Cascade Microtech [47], to achieve accurate and repeatable S-parameter measurement. The WinCalXE features include exclusive 1-, 2-, 3-, and 4-port calibration algorithms, immediate and live data measurement and viewing, LRRM, LRM+, SOLT-LRRM hybrid and NIST-style multi-line TRL calibrations, as well as an Error Set Management capability for data comparison and augmentation. A picture of the setup is shown in Figure 43.

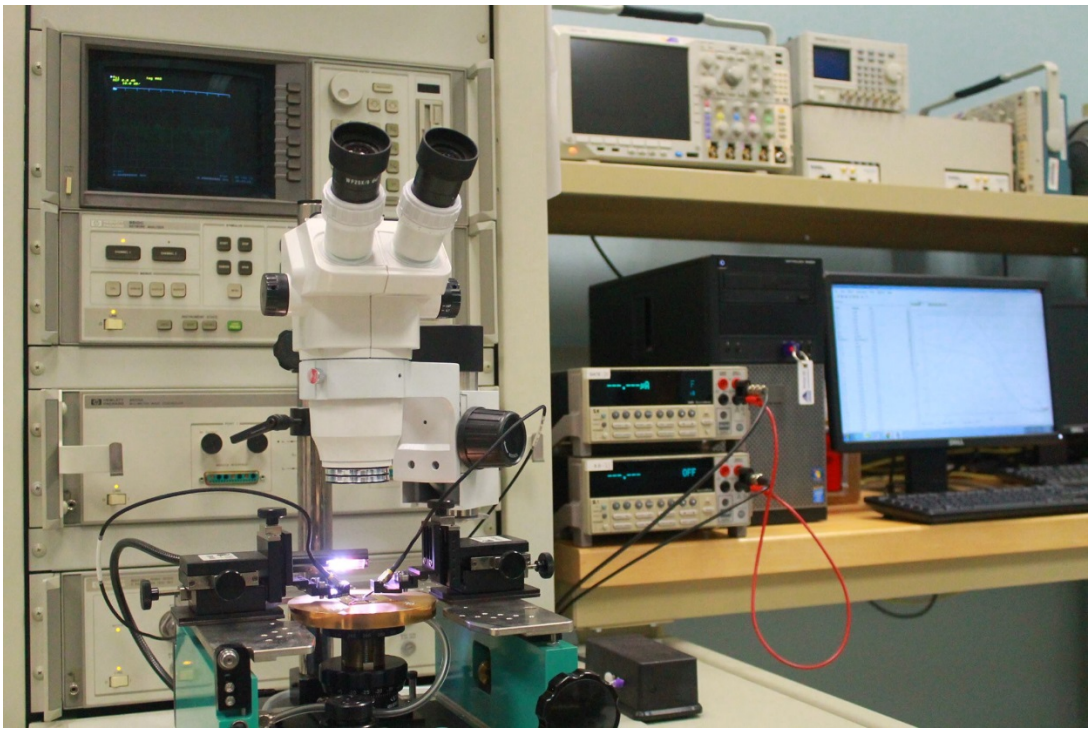

Figure 43: A picture of RF measurement Setup

The two port S-parameter of the device was measure, corrected by the calibration file, and converted to h21 parameter using the following equation [48]:

$$h_{21} = \frac{-2S_{21}(R_{01}R_{02})^{1/2}}{(1-S_{11})(Z_{02}^{*}+S_{22}Z_{02})+S_{12}S_{21}Z_{02}} \tag{32}$$

Where Z_{01} is source impedance and Z_{02} is load impedance. The complete procedure of on- wafer S-parameter measurement has been documented step by step in APPENDIX C.

The current gain, |h21| is plotted with respect to frequency in Figure 44 for two different devices: conventional 3 terminal GFET and the same geometry GFET with proposed additional contacts (FCEs). The DC biasing condition at source, drain and gate were same for both of the devices whereas the proposed device had both of its FCEs biased at -3.0 V. From Figure 44, it is evident that -3.0 V applied at both of the FCEs increases the current gain cut-off frequency from 1.10 GHz to 1.22 GHz.

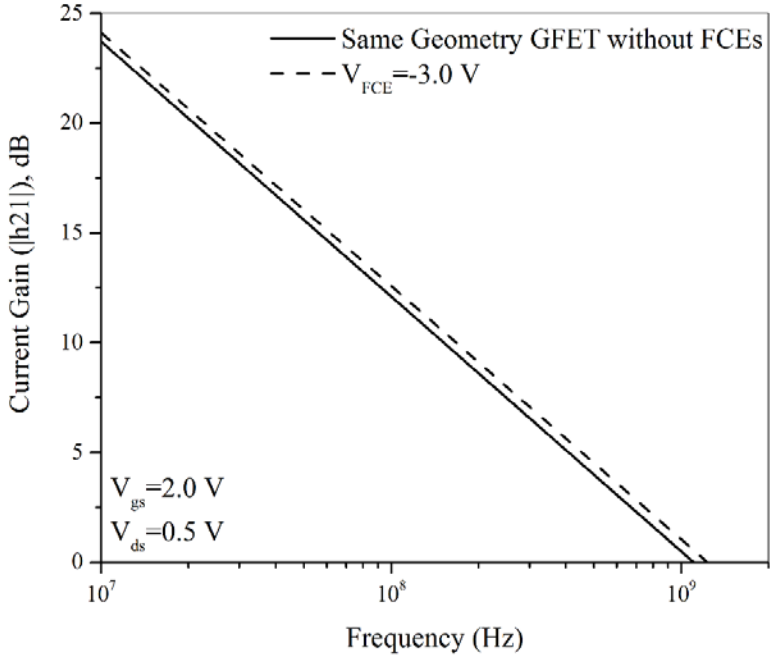

Figure 44: Current gain of a conventional 3 terminal GFET along with that of a same geometry proposed GFET plotted with respect to frequency for comparison.

2.6 Conclusion

We proposed, extensively analyzed, fabricated, and characterized a Graphene FET with two capacitively coupled field-controlling electrodes at the access regions of the device. It is observed that the biased FCEs could control sheet carrier concentration at the ungated regions, and thus resulted in a reduction of the access resistance and improvement of the RF performance of GFETs. The increment of current gain cut-off frequency, f_T was 10.9% compared to that of same geometry GFET without FCEs. The proposed GFET with improved RF characteristics can be used for high frequency applications.

CHAPTER III

BANDGAP ENGINEERING OF GRAPHENE

3.1 Introduction

Atomically thin Graphene has attracted attention of researchers as a promising novel material for electronic/optoelectronic applications due to its outstanding electrical, optical and thermal properties that include but not limited to its high carrier mobility, residual carrier concentration, saturation velocity, thermal conductivity and mechanical strength [49, 50, 8, and 51]. Due to the degeneracy of Graphene valence and conduction band at the Dirac point, it shows a semimetalic characteristics—zero bandgap nature, which precludes its application in digital and logic circuits. In order to make Graphene a technology applicable to real systems and devices, a non-zero bandgap is indispensable. A bandgap can be introduced in Graphene either by breaking the translational symmetry or by breaking the sublattice symmetry [52, 53]. From density functional theory studies, it is evident that a bandgap in Graphene can be achieved in several ways, which include but not limited to: adsorption of hydrogen molecule [54], doping with silicon [55] and group IV element [56], adsorption of water molecule [57], and aromatic molecules [58]. In experiment, it has been demonstrated that a bandgap starting from 2.5 meV up to 450 meV can be introduced in Graphene by decoration with Si-rich two dimensional islands [59], fabrication of Graphene nanomesh via nanoimprint lithography [60], formation of nanoperforated Graphene via block copolymer (BCP) lithography [61], adsorption of patterned hydrogen [62] and adsorption of water molecules [63], as mentioned in Table 1. However, these methods either result in a negligible bandgap value, or demand sophisticated/complex lithographic processes and controlled environment.

Table 1: Bandgap opening method and value

Method	Bandgap (meV)	Ref.
Decoration with Si-rich two dimensional islands	3.2	[59]
Fabrication of Graphene nanomesh via nanoimprint lithography	~ 135	[56]
Formation of nanoperforated Graphene	100	[61]
Adsorption of patterned hydrogen	450	[62]
Adsorption of water molecules	206	[63]

3.2 Theory of Bandgap Opening

The band structure of Graphene exhibits two bands intersecting at the *k* and *k´* points in the Brillouin zone—Dirac point. At this point, valence and conduction bands are degenerate, which results in Graphene to be a zero bandgap material. To introduce bandgap in Graphene, this degeneracy of valence and conduction bands at the Dirac point needs to be lifted off and it can be done by breaking the equivalence between the Graphene sublattices—the sublattice symmetry. In the Graphene decorated with randomly distributed nanoparticles, the interaction (van der Waals) between nano-seeds/particles and Graphene breaks the sublattice symmetry resulting in opening a bandgap. The bandgap of a semiconductor as well as engineered Graphene can be extracted from the slope of Arrhenius plot [63, 64, 65, and 66].

3.3 Method

The rate constant of a chemical reaction (k) depends on absolute temperature (T), pre-exponential factor (A), universal gas constant (R), and activation energy (A) by the following exponential equation, well known as Arrhenius equation [67], as follows:

$$k = Ae^{\frac{-E_a}{RT}} \tag{33}$$

In a similar fashion, the conductivity of a semiconductor is dependent on its absolute temperature (T) and activation energy for conduction (bandgap, E_g) by the following equation:

$$\sigma = \sigma_0 e^{-E_g/2kT} \tag{34}$$

The factor of 2 in the exponent is because, the excitation of an electron across bandgap produces two mobile carriers: an intrinsic electron and an intrinsic hole. The last equation can be written in the form of a linear equation and bandgap can be calculated from its slope:

$$\ln\sigma = \ln\sigma_0 - \frac{E_g}{2k}\frac{1}{T}, \tag{35}$$

3.4 Fabrication of Decorated Single Layer Graphene

3.4.1 Graphene Decorated with ZnO Nano-Seed

For the ZnO nanoseeds decorated Graphene, the nanoseeds were grown on top of single layer Graphene using Zinc acetate dihydrate ($Zn(CH_3COO)_2 \cdot 2H_2O$) (ZAD) as reported in [68]. We modified this approach and utilize the effects of sonication to produce solution phase seeding in a solution exposed to the ambient. A 0.005M concentration of ZAD in isopropyl alcohol (IPA) solution was prepared at room temperature by stirring with a magnetic stir bar at 350 rpm for 5 minutes. Single layer CVD Graphene grown on Copper sheet was coated with PMMA using a regular spin coater and was put floating on $FeCl_3$ solution for 8 hours without any disturbance while copper surface touching the solution.

Once the copper was completely etched, it was washed with DI water multiple times without flipping, and eventually was transferred on SiO_2. After being transferred, the sample was put in a desiccant for 8 hours, and then was put in acetone at 50 ºC for 15 minutes to remove the PMMA. Shadow Mask for Source/Drain patterning was written using a laser engraver. 10 nm Ti and 100 nm Au were e-beam evaporated to pattern the Source/Drain contacts at a chamber pressure of 2×10^{-7} mTorr. The contact length and width were 5 mm and 1 cm respectively and the distance between contacts were 5 mm. The samples were cleaned with methanol, acetone and isopropanol before immersing into the ZAD-IPA solution. The solution with the immersed substrate then was irradiated using a commercially available high intensity ultrasound setup (750W ultrasonic processor, Sonics and Systems). The sample was prepared with a single sonication cycles of 15 minutes duration and the amplitude of the 20 kHz ultrasonic probe was 75% of the maximum amplitude (~30 $W.cm^{-2}$). The global temperature of the aqueous solutions did not exceed ~70ºC.

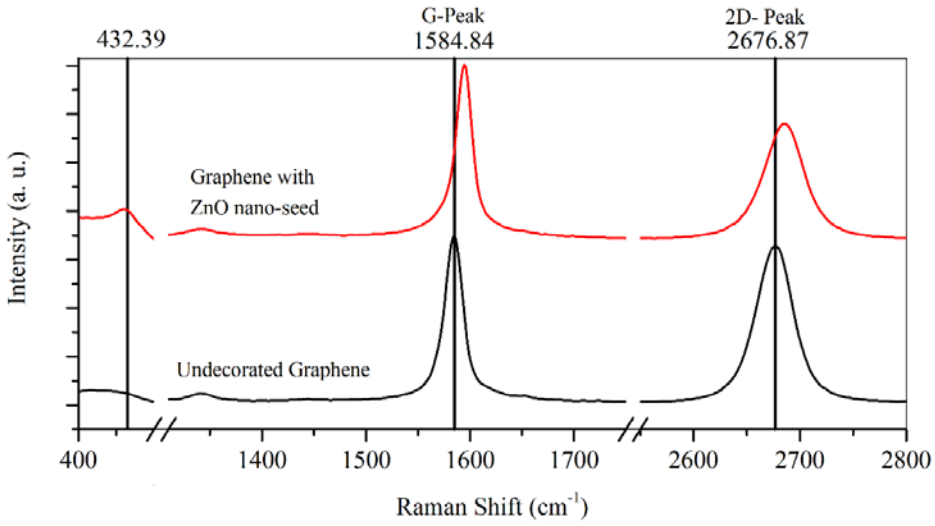

Figure 45: Raman spectra of pristine and ZnO nano-seed decorated single layer Graphene

The undecorated Graphene as well as Graphene decorated with ZnO nano-seeds were characterized by Raman spectroscopy. Figure 45 shows the Raman spectrum of the pristine Graphene and Graphene decorated with ZnO nano-seeds. The 2D/G ratio (0.93) of the pristine Graphene (bottom panel of Fig. 1) confirms the presence of single layer Graphene. In addition, a peak at 432.39 cm^{-1} of the decorated Graphene (top panel of Fig. 1) confirms the presence ZnO [69]. From the Raman spectra of decorated Graphene, a shift of G and 2D peaks is visible, with respect to those of the undecorated one. This shift is due to elongation or contraction of C-C bond because of van der Waals interaction between Graphene and nanoparticles [70].

The SEM image of the ZnO nano-seed decorated Graphene shown in Figure 46 confirms the average size of the nano-seeds to be ~ 10 nm with the average separation distance of 10 nm.

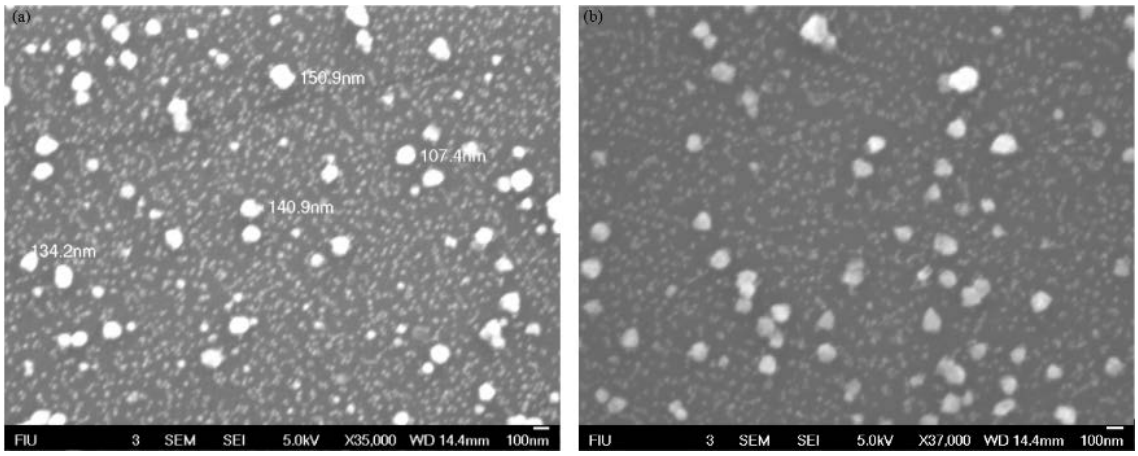

Figure 46: SEM image of ZnO nano-seed decorated single layer Graphene at two different magnifications

The AFM image of the decorated Graphene shown in Figure 47 confirms the RMS and average roughness to be 15.85 nm and 12.34 nm, respectively. This large roughness is due

to the presence of ZnO nano-seeds, as well as, due to the surface roughness of Graphene itself.

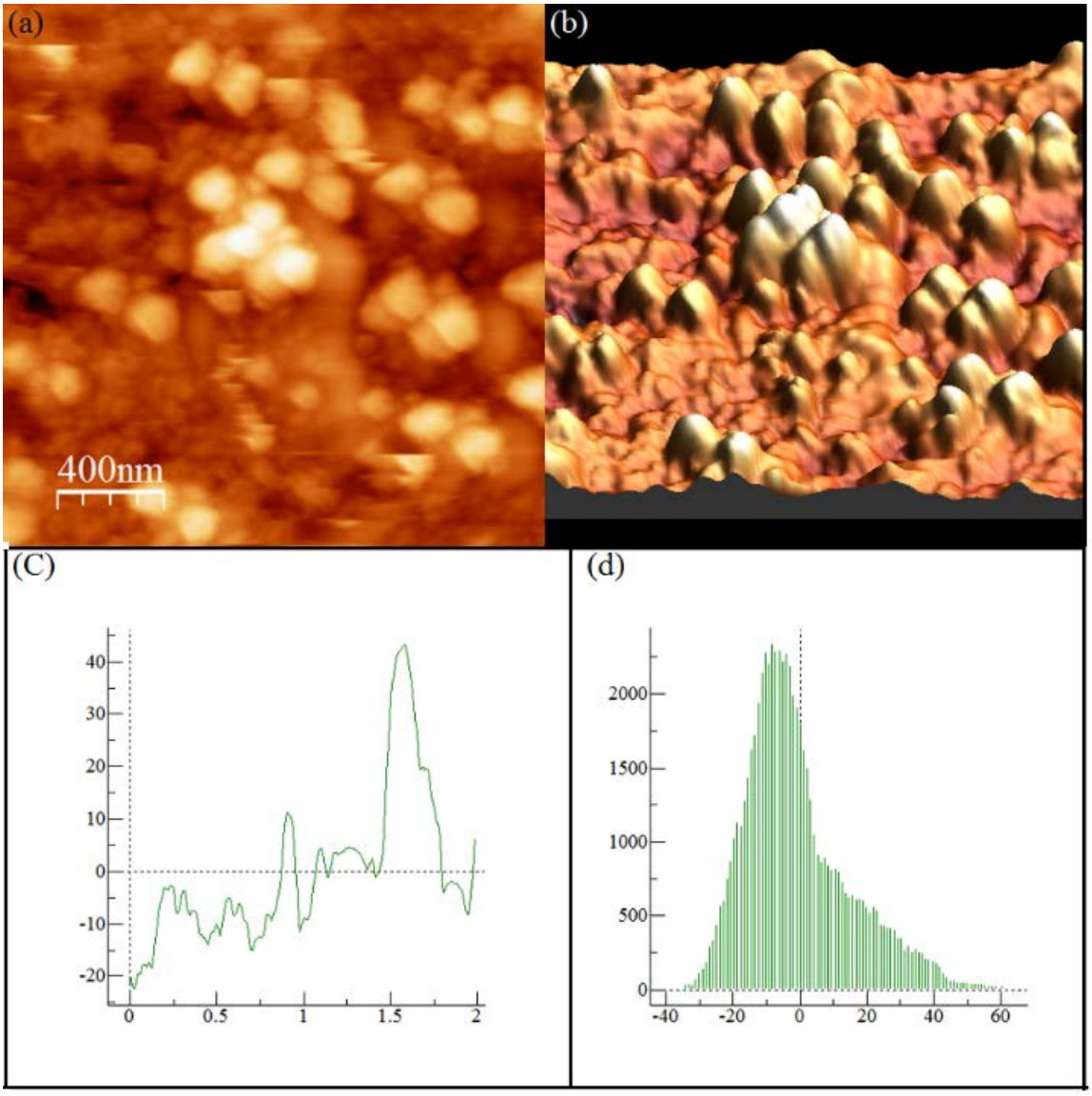

Figure 47: AFM image of ZnO nano-seed decorated single layer Graphene. (a) 2D image. (b) 3D image. (c) The profile along a straight line. (d) Roughness analysis: RMS Roughness= 15.85 nm and Average Roughness= 12.34 nm.

3.4.2 Graphene Decorated with Gold Nanoparticles

For gold nanoparticles decorated Graphene, the nanoparticles were grown first on top of the SiO_2/Si substrate and then CVD Graphene was transferred on top of the gold nanoparticles.

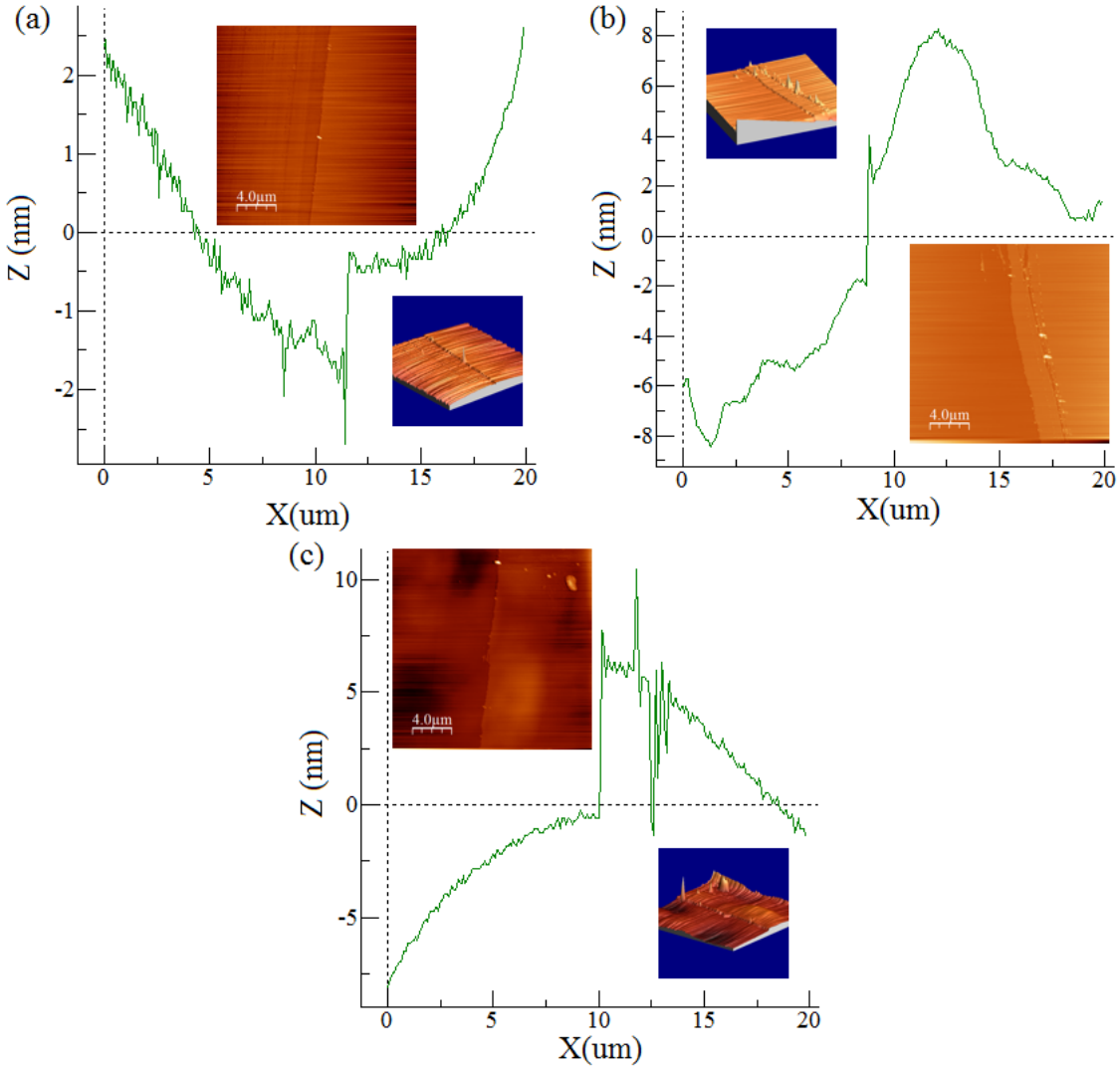

Figure 48: The profile of the step at the edge of sputtered gold thin film on (a) Sample-A, (b) Sample-B, and (c) Sample-C, measured by Atomic Force Microscopy (AFM) with 2D and 3D views (inset).

Three SiO_2/Si chips with 300 nm SiO_2, named as Sample-A, Sample-B, and Sample-C, were first solvent cleaned. Gold thin film was grown on SiO_2 by sputtering. The gold film

thickness on Sample-A, Sample-B, and Sample-C were measured at the edge by using atomic force microscopy (AFM). Figure 48 (a), (b), and (c) show the profile of the step of Sample-A, B, and C, with the 2D and 3D views inset. The film thickness estimated from the AFM image for Sample-A, B, and C were 1 nm, 4 nm, and 7 nm, respectively.

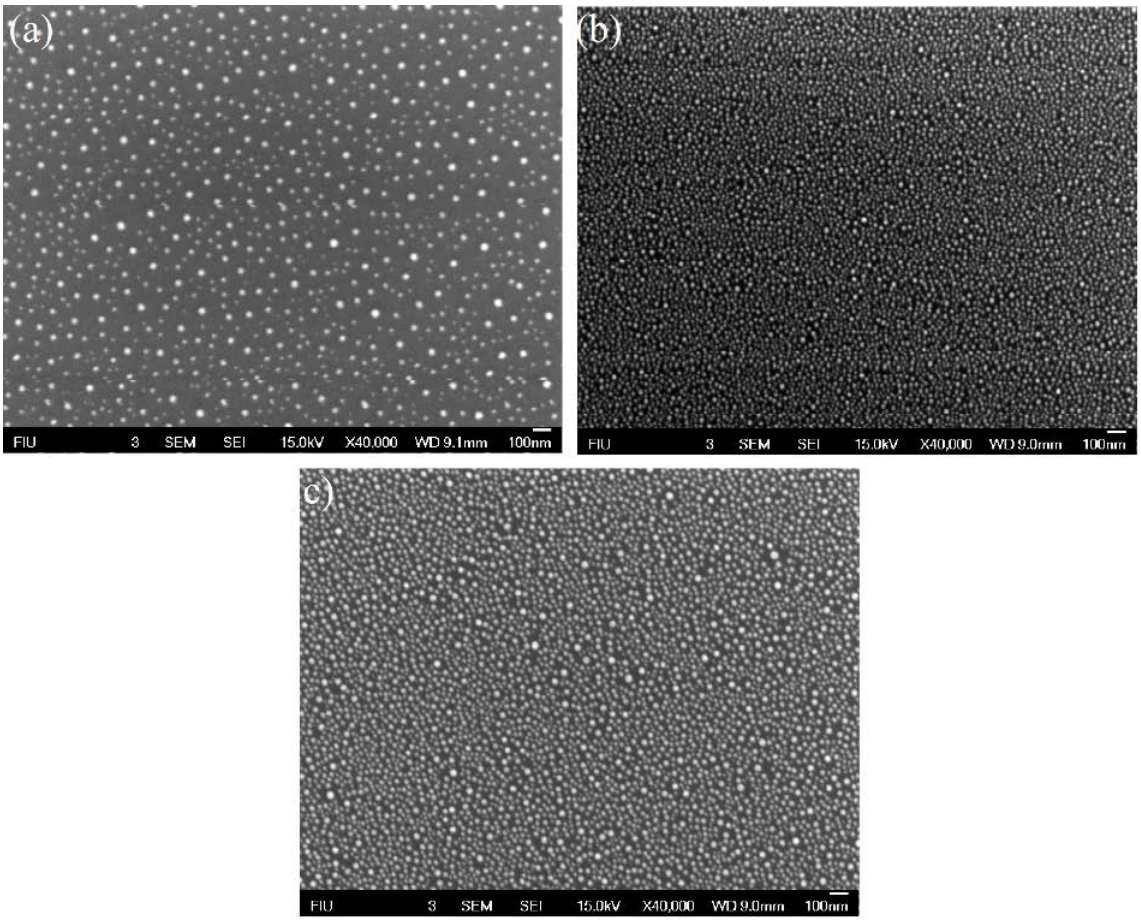

Figure 49: SEM image of gold nanoparticles grown on SiO_2 of (a) Sample-A, (b) Sample-B, and (c) Sample-C.

The samples were then annealed in N_2 environment at 800 ºC for 30 minutes with a ramp of 5 ºC/s. At this high temperature and ramp, the gold thin film dewetted and formed gold nanoparticles, as expected [71, 72]. The presence of nanoparticles was confirmed through SEM imaging, as shown in Figure 49. From the AFM and SEM image shown in Figure 48

and Figure 49, it is evident that: Sample-A with the thinnest gold film sputtered (1 nm) resulted in the least dense nanoparticles growth with largest diameter, Sample-B with 4 nm sputtered gold has denser nanoparticles with smaller diameter, compared to Sample-A, and Sample-C with the thickest gold film (7 nm) has intermediate nanoparticle density and diameter.

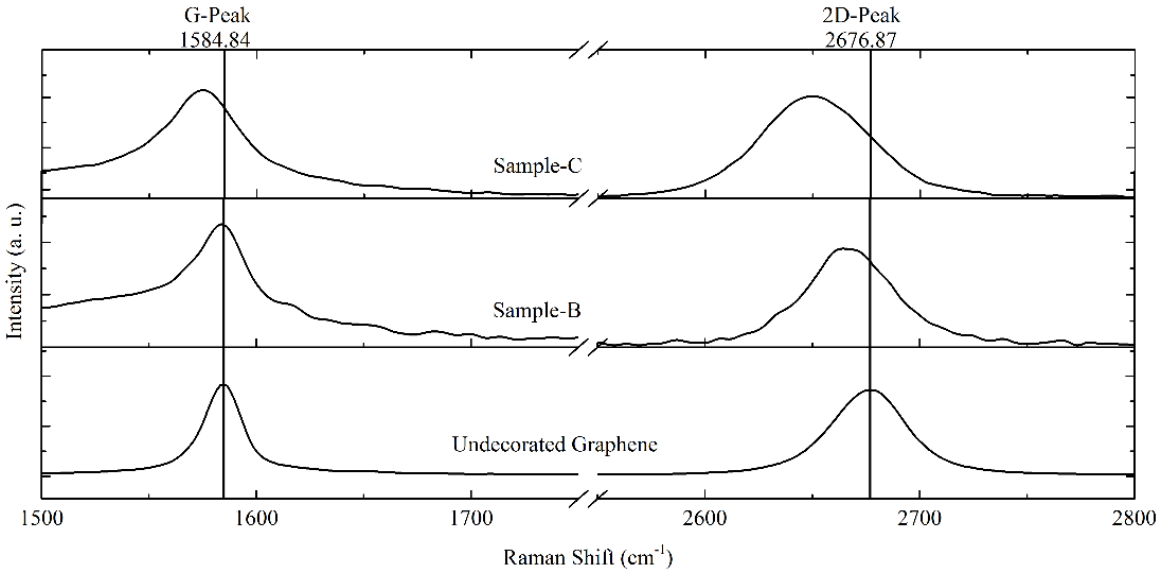

Figure 50: Raman spectrum of undecorated Graphene and decorated Graphene: Samples-B, C

Using the standard Graphene transfer method mentioned above, single layer Graphene was transferred on top of the gold nanoparticles decorated substrate, and eventually, PMMA was removed with acetone. From Raman spectroscopy as shown in Figure 50, it is evident that the 2D and G peaks of Graphene decorated with gold nanoparticles shifted compared to those of the undecorated one, as expected [73, 74]. As before, shadow masks were used to pattern contact pads with length, width, and in-between separation of 2 mm, 2mm, and 7 mm, respectively, consisting of 10 nm Ti and 300 nm Gold.

3.5 Bandgap Measurement of Decorated Graphene

Bandgap of nanoparticles decorated Graphene was estimated measuring temperature dependent conductivity using the Eqn. 34. A commercially available vacuum probe station integrated with a precision thermal chuck and temperature control system, turbo pump and semiconductor parameter analyzer, as shown in Figure 51, was used to measure the temperature dependent I-V characteristics.

Figure 51: A picture of the temperature dependent conductivity measurement setup

At first, the current-voltage characteristics of the sample was measured inside a constant pressure (25 mBar) chamber at different temperatures starting from 0 ^{o}C to 110 ^{o}C with a step size of 5 ^{o}C, and at each temperature step, the sample was left for 5 minutes before the measurement was taken.

For the Graphene sample decorated with ZnO nano-seeds, a DC voltage was ramped starting from -500 mv to +500 mv with a step size of 10 mV as shown in Figure 52 (a), and both the hold time and delay time at each bias point were set at 20 ms. From the current-voltage characteristics of this sample, its resistivity and conductivity were extracted for each temperature value and the resistance was found to decrease linearly with temperature. Eventually, from the Arrhenius plot shown in Figure 52 (b), slope was extracted and the bandgap was calculated to be 7.36 meV. We further investigated this bandgap opening process by decorating single layer Graphene with ZnO nano-seeds, whose lateral size (~300 nm) was much bigger compared to Graphene lattice constant (~ 2.46 Å) [75], and it did not show semiconductor properties.

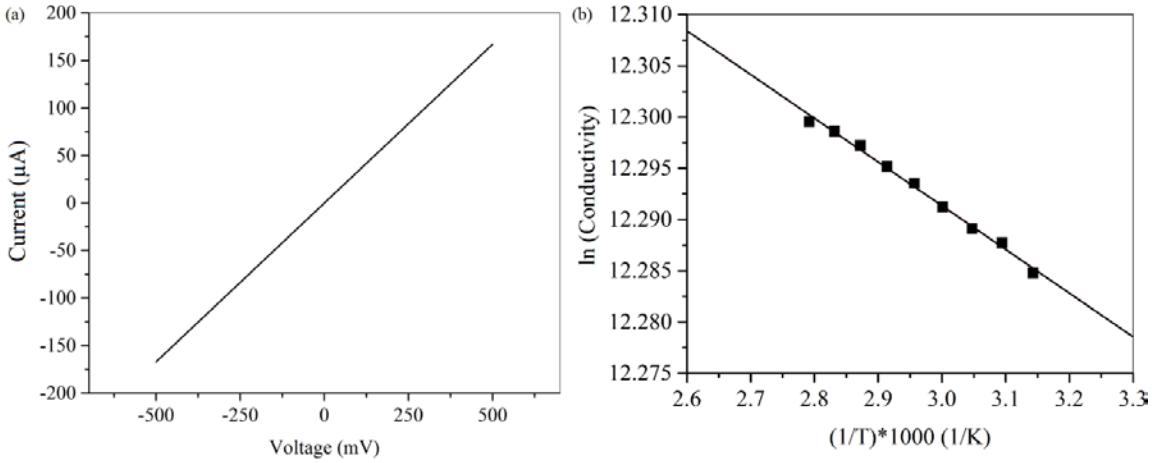

Figure 52: (a) The current-voltage characteristics of the ZnO nano-seed decorated Graphene at various temperatures, (b) The temperature dependent conductivity property.

For the Graphene samples decorated with gold nanoparticles, the same experimental setup and procedure was followed to measure the introduced bandgap. The logarithm of film conductivity versus inverse of temperature of Sample-B, and C are shown in Figure 53, with the respective current-voltage characteristics and temperature-resistance

characteristics at 50 ºC, inset. The extracted bandgap from the slope of conductivity curve of Sample-A (not shown in Figure 53), B, and C were 40.27 meV, 83.98 meV, and 59.91 meV, respectively, as expected from the density functional calculations reported in [76].

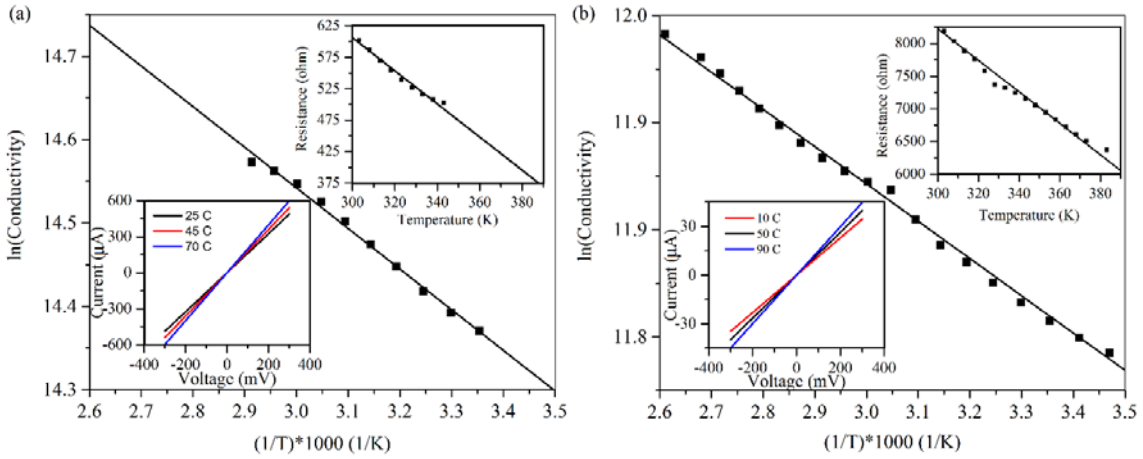

Figure 53: The temperature dependent conductivity curve of (a) Sample-B and (b) Sample-C, with corresponding current-voltage characteristics at different temperatures and temperature-resistance characteristics, inset.

3.6 Conclusion

In conclusion, we have experimentally demonstrated the opening of a bandgap of single layer CVD Graphene by decorating it with randomly distributed nanoparticles. The first approach of decoration with randomly distributed ZnO nano-seeds opened an insignificant bandgap. On the other hand, the resulting bandgap due to decoration with gold nanoparticles was much more prominent compared to the ZnO nano-seed samples and showed a dependence on nanoparticle density and size. The proposed method of bandgap opening can be further investigated varying nanoparticle size, height, and density. Graphene with a moderate bandgap achieved by fine tuning of this decoration process can be used for digital and logic devices.

CHAPTER IV

GRAPHENE THz DETECTOR

4.1 Graphene Grating Gate THz Detector

4.1.1 Introduction

Terahertz technologies utilize electromagnetic (EM) radiation in the frequency range between 300 GHz and 10 THz and their potential applications in biology, chemistry, medicine, astronomy and security are wide ranging. The abundance of potential THz applications fueled intense research in the last decade leading impressive advancements in emission and detection of THz radiation. Plasma wave propagation in two-dimensions (2D) has contributed to advancements in detection and control in THz spectral region [77]. Large propagation velocity of plasma waves compared to electron drift velocities allows plasmonic device to exceed electron drift limited cut off frequencies. Plasmonic THz detection has been demonstrated using Silicon [78, 79, 80], III–V compounds [81, 82, 83, and 84], and III-N [85, 86, and 87] based semiconductor devices. III-N devices have been particularly of interest due to their high sheet carrier concentration. The coupling efficiency of single gate plasmonic devices to THz radiation is weak due to small active region of these devices. To mitigate this problem, grating gate couplers on a large active region and linearly integrated Field Effect Transistor (FET) arrays with high integration density are proposed [88]. Device geometry has not been the only limitation for the response of THz plasmonic devices. Most of the previously observed THz plasmonic detectors have demonstrated very weak response at room temperature due to high electron scattering rates [89, 90, and 90]. Graphene with remarkably high electron mobility at room temperature, with reported values in excess of 15,000 cm2/Vs [92] has strong potential for THz plasmonic devices. Recently, the high mobility properties of Graphene at room temperature

was exploited to demonstrate Graphene plasmonic THz metamaterials [93]. However, the reported structures were based on Graphene nanoribbons which were fabricated by plasma etching presented low quality factors. The low quality factor could be ascribed to the high carrier scattering rate and limited mobility due to the plasma damages induced during the etching process [94]. Recently large area Graphene samples with good electrical characteristics have been grown [95]. Intense research in the field is expected to make mass production of large area high quality Graphene widely available in near future for various applications [96]. True capabilities of Graphene grating gate structures need to be explored to design and fabricate Graphene plasmonic THz devices. In this letter, we report on theoretical and numerical analysis of THz plasmonic behavior in large area Graphene FET structures with grating gate couplers.

4.1.2 Theory

A short channel with high sheet carrier concentration acts as a resonant cavity for the plasma waves with the fundamental frequency of ω_0 and its harmonics. An incoming electromagnetic radiation excites plasma waves in such a channel. When $\omega_0\tau >> 1$ (τ is the momentum relaxation time) the resonant condition is satisfied. Sheet electron density in a Graphene layer can be estimated by

$$N_s = \frac{\varepsilon}{ed}(V_g - V_d) \tag{36}$$

Where ε is the permittivity, d is the dielectric thickness, e is the unit charge, V_g is the gate voltage and V_d is the voltage corresponding to Dirac point at which the Graphene sheet has

charge neutrality. The electron energy dispersion in undoped Graphene is linear $E = \hbar V_F.k$ with k being the electron momentum and V_F being the 2D Fermi velocity, which is a constant for Graphene (V_F = 10^6 m/s). The linear electron energy spectrum implies zero effective electron mass in Graphene. The electron "inertia" in massless Graphene is described by a fictitious "relativistic" effective mass $m_F = E_F / V_F^2$, where E_F is the Fermi energy. The relation between the Fermi energy and sheet carrier density can be given as

$$E_F = \hbar V_F \sqrt{2\pi N_S} \tag{37}$$

Using Eqs. (1) and (2), one can obtain

$$m_F = \frac{\hbar}{V_F}\sqrt{\frac{2\pi\varepsilon}{ed}}V_0 \tag{38}$$

where $V_0 = V_g - V_d$. For a typical value of V_0= 1, Eq. (3) yields m_F= 0.03 m_0 where m_0 is the free electron mass. It should be noted that m_F decreases to zero with the gate voltage V_g approaches to the Dirac voltage. Electron relaxation rate in Graphene with electron mobility, μ can be estimated as $1/\tau = e/\mu m_F$. Therefore, $\omega_0\tau >> 1$ is satisfied for frequencies above 2 THz even for low mobility Graphene with μ = 1600 cm^2/Vs. Coupling of EM radiation into 2D electron gas (2DEG) in high sheet carrier concentration channels via grating gate couplers was first investigated by Zhent et al. [97] and later applied to III–IV [81, 82] and III-N systems [86]. Plasmon dispersion in a gated Graphene can be formally written in the same form as in a conventional semiconductor structure with substituting the effective electron mass by the "relativistic" effective mass m_F

$$\omega = k\sqrt{\frac{eV_0}{m_F}} \tag{39}$$

where q is the plasmon wavevector, which is determined by the grating gate period L, $k = 2\pi n/L$ (n = 1, 2, 3….). Substituting Eqs. (3) into (4) results in [98]

$$\omega = k\sqrt[4]{N_S \frac{{V_F}^2 e^4 d^2}{2\pi\hbar^2\varepsilon^2}} \tag{40}$$

which gives the plasmon resonant modes in Graphene.

Room temperature operation is a crucial aspect for the practicality of the THz devices for many practical applications like medical imaging, security and sensing. Plasma resonances in a grating gate device can be best excited when the radiative damping, γ_{rad} is equal to the dissipative damping, γ_{dis} caused by the carrier scattering [87]. In this case the maximum absorbance is given by 0.5 ($1-\sqrt{R_0}$) where R_0 is the reflectivity when there is no resonant surface layer. Dissipative damping γ_{dis} of a plasmon mode increases with temperature. Therefore, matching condition of $\gamma_{dis}= \gamma_{rad}$ requires strong radiative broadening at room temperatures. Since the radiative broadening is directly proportional to the conductivity of the channel, Graphene layers are especially promising for room temperature resonant absorption of THz radiation. Radiative dampening is also directly proportional to the strength of coupling between the plasmon modes and the incident THz radiation. Strong electric near field induced in narrow slits between the grating gate fingers greatly enhances the coupling and hence the radiative dampening. Slit width w in the investigated devices

was chosen to be about 10% of the gate finger width to achieve the maximum resonant absorbance.

Resonant absorption of THz radiation by the plasmons induces an oscillating current and creates nonuniform impedance distribution in the active layer which leads to an electrical response depending on incident power, polarization and frequency. In the photovoltaic (PV) detection scheme when asymmetric boundary conditions (i.e., short circuit boundary condition at the source side of the channel and open circuit boundary condition at the drain side of the channel) are applied, nonlinear properties of the transistor structure rectifies the oscillating current induced by the incoming radiation and results in a photoresponse in the form of DC voltage between source and drain [77, 78, and 79]. An improved signal can be obtained when a constant current is applied between the ohmic terminals at the both ends of the channel and drain voltage is monitored which is referred as the photoconductive (PC) detection mode [81, 82]. Analysis of the electrical response at different modalities is beyond the scope of this study.

4.1.3 Simulation and Results

The structures investigated in this study consist of Graphene layers on sapphire substrates as shown in Figure 54. Titanium grating gates are placed on 17 nm thick SiO2 layer deposited on Graphene. Different gate period, *L*, and gate finger length, *w*, combinations were studied.

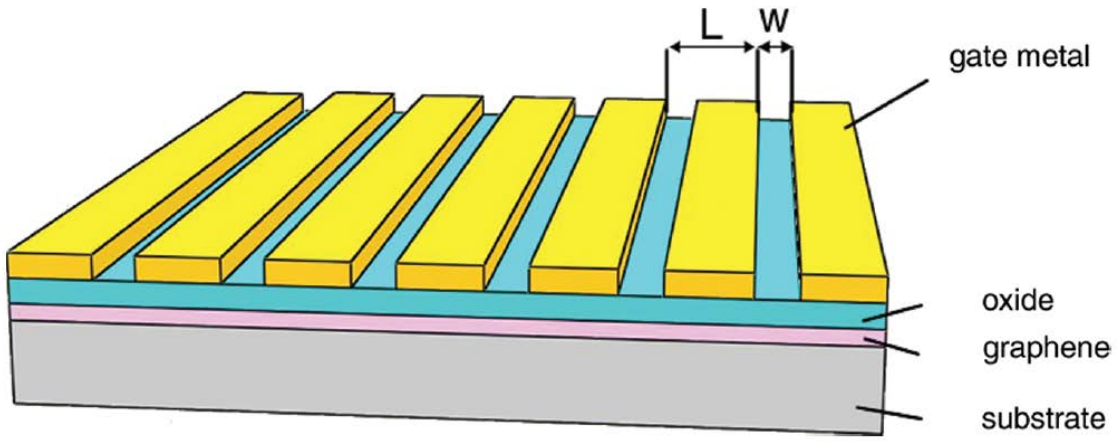

Figure 54: Cross section of the studied structures (not to scale).

A commercial simulation package of finite-difference time-domain (FDTD) method with a 3D Maxwell equation solver and a custom code for data analysis were used to calculate absorption and transmission spectra of the structures. FDTD tool allowed both time domain and frequency domain information. A broadband pulse was sent from the source and EM field propagation through the structure was calculated until there was no electromagnetic field left in the entire devices. Frequency domain information at the spatial points of interest were obtained through Fourier transform of the time domain information. Frequency dependence of power flow and modal profiles were obtained in the frequency range of 1–8 THz. The simulations were carried out using periodic boundary conditions for the grating gate arrays. Furthermore, real experimental data for dispersion relations and different loss mechanisms for materials were used in the simulation. The mesh size was sufficiently small to match experimental data for structures with small features. We validated our simulation method by comparing the numerical results with the experimental

results reported in the literature for GaN-based grating gate devices [86] and Graphene nanoribbon metamaterial structures [93].

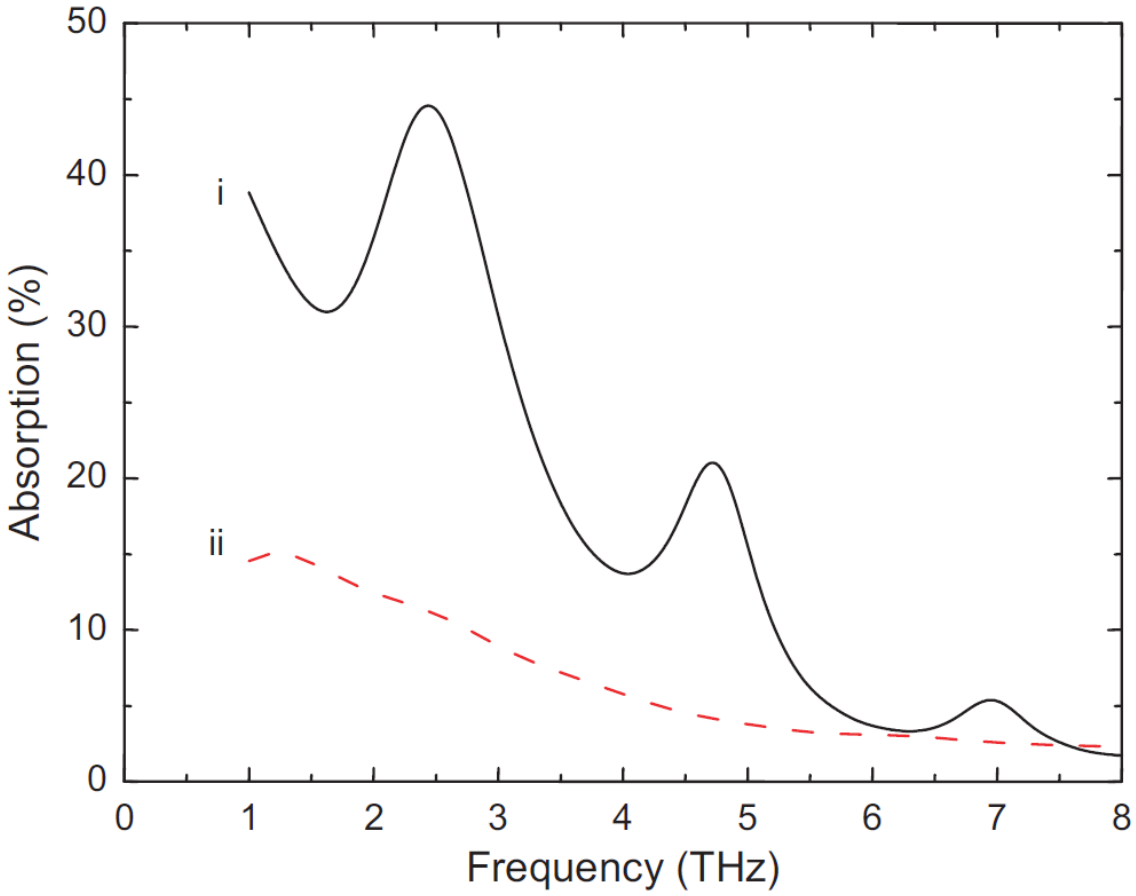

Figure 55: Room temperature absorption spectra of AlGaN/GaN and Graphene grating gate FET structures with L = 1.5 µm, w = 0.15 µm, N_S= 7.5×10^{12} cm^{-2}. (i) Graphene (ii) $Al_{0.2}Ga_{0.8}N$/GaN. Curve (ii) is in well agreement with the experimental data reported in Ref. [86].

In Figure 55, we compare the room temperature absorption spectra of Graphene and GaN grating gate devices with the same geometrical parameters. Following the experimental details reported in Ref. [86], $Al_{0.2}Ga_{0.8}N$/GaN High Electron Mobility Transistor (HEMT) epilayer structure on sapphire was used for GaN devices with room temperature electron mobility of µ= 1200 cm^2/V · s and sheet carrier density of N_S =7.5×10^{12} cm^{-2}. For the Graphene devices, mobility of µ = 3000 cm^2/V.s was used while the sheet carrier

concentration was kept the same with the one for GaN devices. The Graphene devices present well pronounced resonant absorption peaks corresponding to the fundamental mode and first two harmonics in the 1–8 THz range. The resonant frequencies are in agreement with the calculated values using the eqn. 40. Electric field distributions for the first two resonant modes of the plasmons are shown in Figure 56. Resonant absorption for GaN-based devices on the other hand is not observable due to higher scattering rates at room temperature.

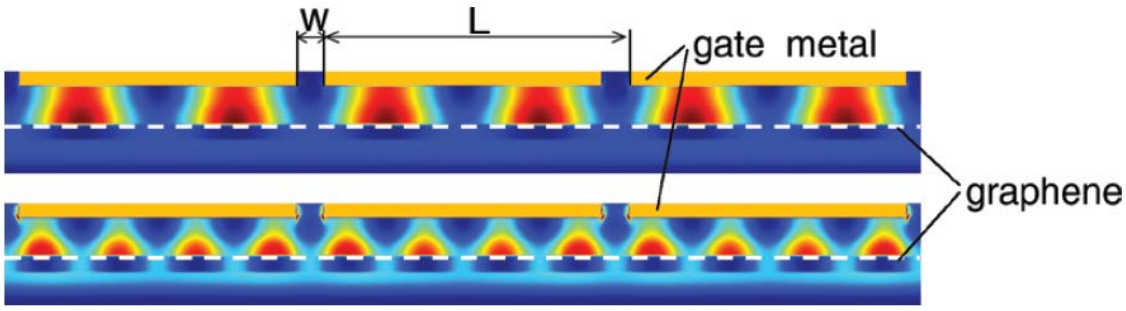

Figure 56: Electric field distribution for the first mode (top) and second mode (bottom) of plasmon resonances in Graphene grating gate devices. Light colored boxes representing gate metals and dashed lines representing Graphene layers are added for the clarity

The absorption characteristics for GaN devices is in good agreement with theoretical and experimental ones reported in Ref. [86] which validates our simulation method. The modulation depth in the absorption spectrum of the periodic gated FET structures is also controlled by the carrier scattering rate in the channel. The lower scattering rate in Graphene compared to GaN HEMT devices allows clear absorption peaks with large modulation depth. Effect of the scattering rate in Graphene is presented in Figure 57.

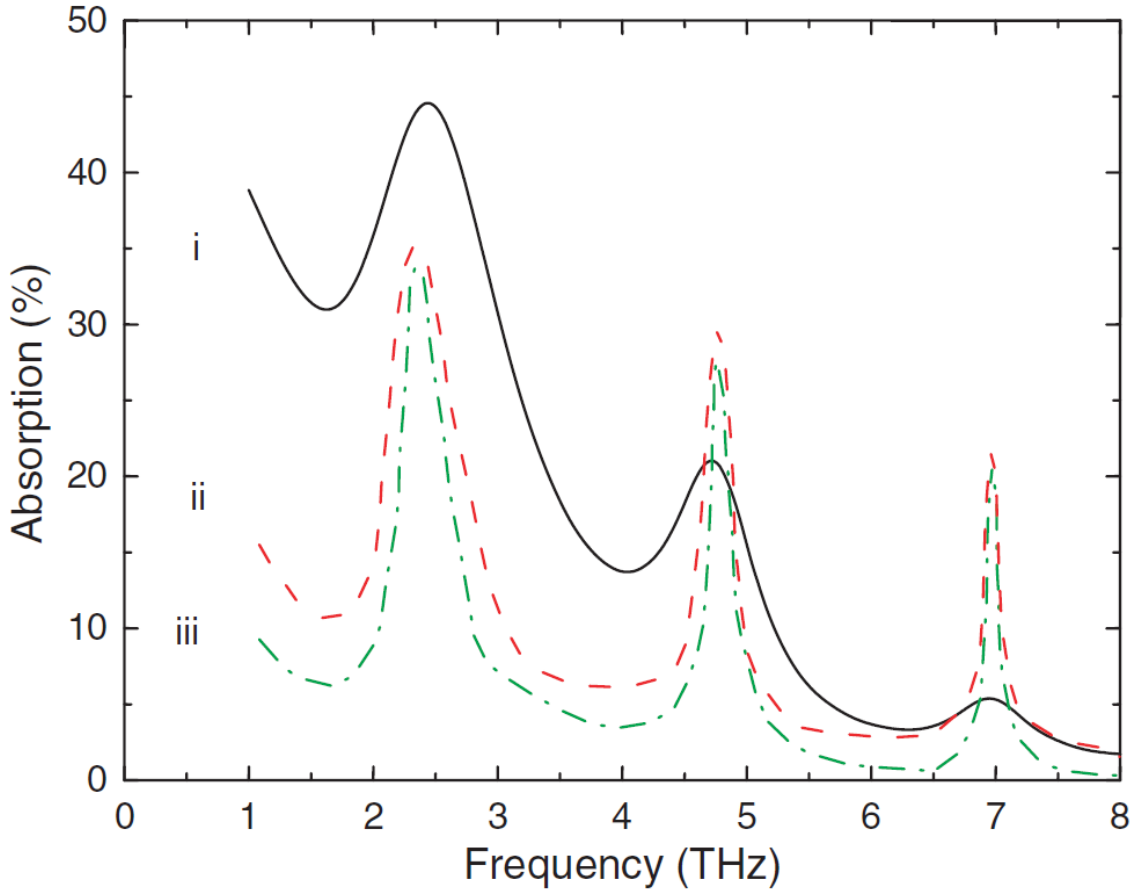

Figure 57: Absorption spectra of Graphene with different mobilities. L = 1.5 µm, w = 0.15 µm, N_S= 7.5×10^{12} cm^{-2}. (i) µ = 3000 $cm^2/V \cdot s$ (ii) µ = 15000 $cm^2/V \cdot s$ (iii) µ = 40000 $cm^2/V \cdot s$.

For lower mobilities (curve *i*), contribution of Drude absorption which monotonically decreases with frequency is visible at the background. As the mobility increases, modulation depth increases especially at higher frequency modes. This is in agreement with the fact that Drude absorption also decreases with increasing mobility [99]. An important advantage of the grating gate devices is tunability of the resonant absorption frequencies though controlling the charge concentration by the applied gate voltage.

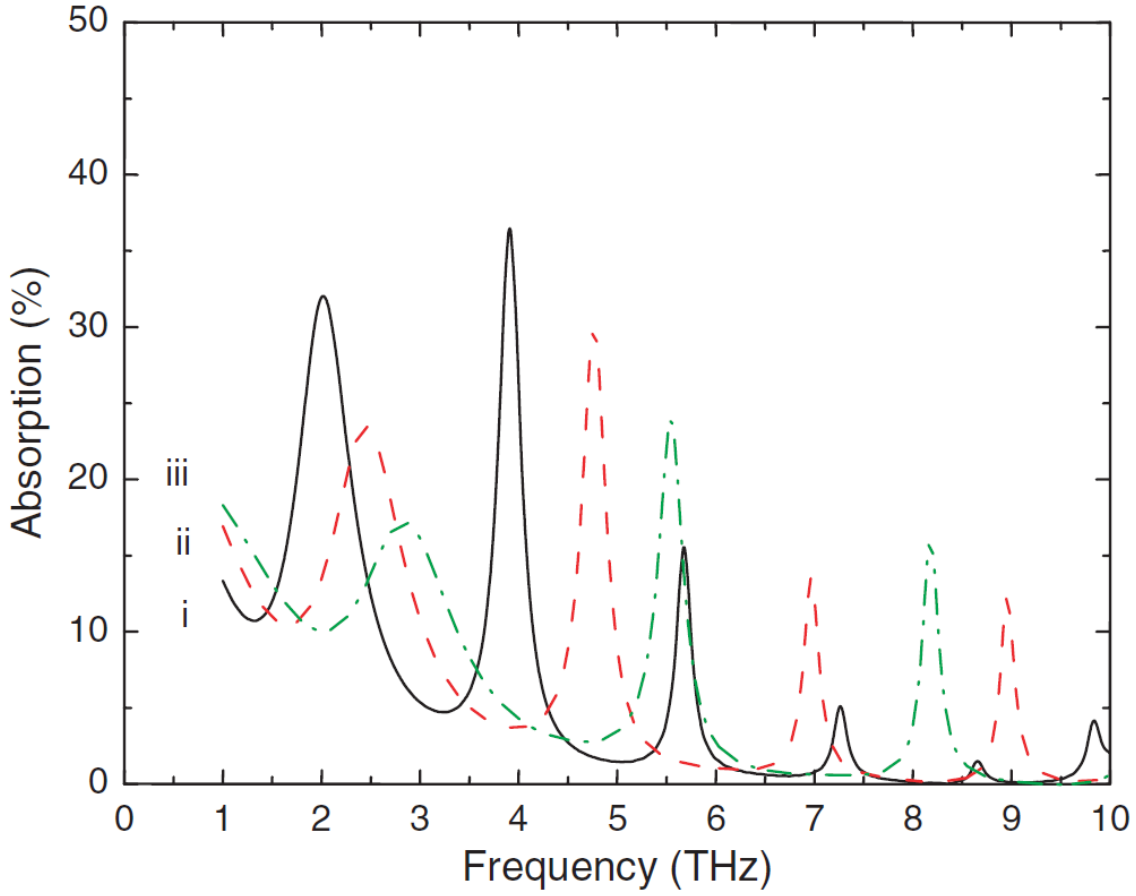

Figure 58: Absorption spectra of Graphene grating gate FET structure with different carrier concentrations. L = 1.5 µm, w = 0.15 µm, µ =15000 $cm^2/V \cdot s$ (i) $N_s = 3.6 \times 10^{12}$ cm^{-2} (ii) $N_s = 8.3 \times 10^{12}$ cm^{-2} (iii) $N_s = 1.5 \times 10^{13}$ cm^{-2}.

Figure 58 clearly shows the shift of the resonant frequencies by the charge carrier concentration as expected from the eqn. 40. It should be noted that the plasmon frequency in Graphene exhibits different dependence on the gate voltage ($\sim N^{1/4}$) as compared with gated plasmons in conventional semiconductor structures ($\sim N^{1/2}$). The data in Figure 58 also shows that, it is possible to reduce spectral separation of modes (increase the spectral density) by slightly decreasing the carrier concentration and to observe higher order modes in a selected spectral range.

4.2 Graphene THz plasmonic Ring Resonators

4.2.1 Introduction

Plasma oscillations in various types of field effect transistors (FETs) [77, 100] are used for THz detection [100, 101, 81, 102, 103, and 104], mixing [105, 106, and 107] and generation [108, 109]. Plasmonic THz detectors have the advantage of continuous tunability over the conventional detectors such as bolometers and pyroelectric detectors [110]. However, detection of THz radiation by such devices is greatly size dependent [87] and therefore, their response to THz sources is diminished with decreasing size. On the other hand, responsivity of FET based detectors is also limited by the size of their active region which is typically much smaller than the wavelength of THz radiation [87]. The grating gate devices need to have periodically spaced gate that are generally consists of tens and hundreds of gates [86]. These resonant plasmon devices are typically hundreds of microns in sizes [86].

Here, we propose novel Graphene plasmonic ring resonators with the capability to guide THz radiation into deep sub-wavelength size with relatively higher quality factors with sustaining the periodic structure. The size of the proposed devices can be a few microns which is much smaller than the THz disc resonators consisting of dielectric [111] and dielectric-metal plasmonic [112] that are in centimeter and hundreds of micrometer size range reported in the literature. Moreover, the resonant modes of the guided plasmons can be tuned by the applied voltage on the metallic gratings. The proposed devices can find applications in THz filtering with the advantage of tunability. The proposed devices also

prove that the THz plasmonic excitation can be achieved with split rings and THz plasmons can be guided in plasmonic waveguides with waveguide width of as low as λ/1200.

4.2.2 Simulation and Results

Graphene has high electron mobility characteristics at room temperature which makes it a very attractive material for THz plasmonic applications. We investigated the response of the Graphene based split rings to the incident THz radiation.

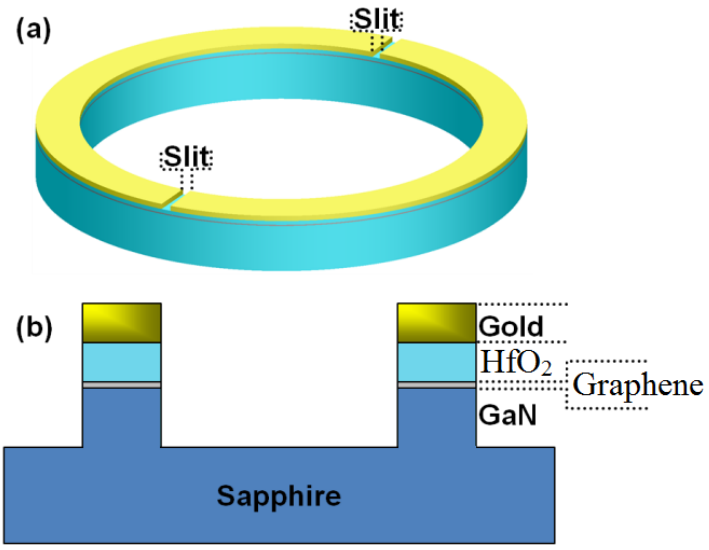

Figure 59: (a) Split ring resonator placed on top of Graphene. (b) The cross section of the resonator device.

In our Graphene ring design, a Graphene layer is placed on a THz transparent substrate and covered by a thin layer of dielectric layer. On top of the thin dielectric layer, a split ring structure is described as shown in Figure 59. Electron collision frequency and electron concentration used in our simulations are extracted from the data in reference [113]. Our simulation model is validated successfully by replicating the experimental data of THz

transmission through Graphene micro ribbons. The mobility used in simulations is 12500cm^2/(V.s) (epitaxial growth Graphene on SiC [114]).

The response of the Graphene devices are in a wider THz spectrum compared to the AlGaN/GaN based devices due to its high mobility and electron concentration which arises from the dispersion relation of the gated plasmons [77], as shown in Figure 60. The increase in electron concentration will cause the higher energy shift of the modes like applying a positive voltage over the split ring as discussed before in previous sections. According to the dispersion of the plasmons in Graphene, the resonant frequency has fourth root dependence on the electron concentration which causes smaller shift of the resonant modes to the applied gate voltage compared to the AlGaN/GaN devices.

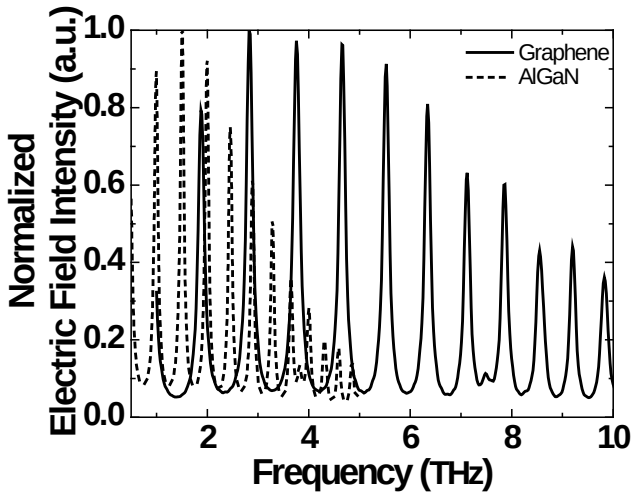

Figure 60. (a) Calculated electric field intensity of the fundamental mode in between the circular grating and 2DEG, (b) second mode, (c) summation of modes from 1 to 5.

4.3 Conclusion

We investigated the plasmonic absorption characteristics of Graphene grating gate FET structures at THz frequencies. FDTD simulations and analytic calculations showed that the

investigated devices could present well pronounced resonant absorption peaks up to 6th harmonic even at room temperature in 1–8 THz. The large modulation depth of higher order modes hints that it is possible to observe even higher modes beyond 10 THz which was the spectral limit in this study. Moreover, the resonant frequencies can be tuned by modulating the channel carrier concentration by gate bias. The results are important to design Graphene based plasmonic THz devices operating at ambient temperature for wide range of applications. In addition to that, we have investigated split ring resonator for Graphene based high electron mobility devices. The responses of the devices are in a wide spectral range of THz frequencies. The resonant modes can be controlled with an applied voltage over the gates. The radius and the width of the ring can be used to passively to tune the resonant frequency. Increasing the radius of the ring causes higher order modes to be observed. Graphene active layer devices show resonance response to the incident radiation in a wider spectral range because of the dispersion relation and higher mobility at room temperature. The proposed device can be used for applications of compact tunable THz filters and THz detectors.

CHAPTER V

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this thesis, two different problem areas were addressed regarding the successful application of Graphene as a field effect transistor channel material. First the adverse effect of access resistance on high frequency performance of Graphene FET. To decrease the access resistance, as well as, to increase the current gain cut-off frequency of GFET, three different novel geometry GFETs were proposed consisting of two additional contacts named field controlling electrodes (FCE), capacitively coupled to the device access region. They are: the top FCE GFET, bottom FCE GFET, and hybrid contact GFET. The proposed devices were extensively analyzed; their DC and small signal RF performance we estimated from TCAD simulation as well as from analytical calculation. The successful simulation of proposed device performance was followed by fabrication and experimental characterization of DC and RF performance. The fabricated proposed device showed a prominently improved DC and RF performance over those of same geometry conventional GFET without FCEs.

The other problem area addressed in this thesis is the zero bandgap of Graphene. In spite of its outstanding electrical and optical characteristics over conventional semiconductor materials, Graphene's zero bandgap property precludes its application in high speed digital and logic devices, which require a high on/off current ration. To experimentally introduce a bandgap in Graphene, it was decorated with two different types of nanoparticles: gold nanoparticles and ZnO nano-seed, and the bandgap was measured from its temperature dependent conductivity characteristics.

In addition to that, a Graphene plasmonic THz detectors were analytically and numerically investigated to estimate its performance as a room temperature THz detector which showed a well pronounced resonant absorption peaks even at room temperature over a wide frequency range.

5.2 Future Work

Based on the results presented in this thesis, one can find several further research topics worth further investigation.

5.2.1 Fabrication of the proposed GFET with shorter gate length, different gate dielectric and metal.

The current gain and cut-off frequency of a FET is inversely dependent on the gate length. Using sophisticated lithographic technique, the gate length can be further shortened and the effect of FCEs on the short channel device can be investigated. In addition to that, the thickness of gate dielectric (HfO_2) can be varied, as well as, different gate dielectric other than HfO_2 can be investigated. Besides, gate and FCE metals other than Ti/Ni can also be investigated.

5.2.2 Decoration of Graphene with gold nano-particles different size, shape, and density

In this thesis, to decorate Graphene with nanoparticles, gold thin film of three different thicknesses were sputtered and annealed. One can further investigate the growth of nano-particles from gold thin films of other thicknesses and its effect on opened bandgap. In

addition to that the effect of metal nanoparticles other than gold, including copper and aluminum, can also be investigated.

5.2.3 Fabrication of the proposed GFET with bandgap engineered Graphene as channel

The bandgap engineered Graphene can be used as the channel material of the proposed GFET with FCEs, and its DC performance including on/off current ration along with high speed switching performance can be further investigated. Successful investigation of this device could lead towards high speed Graphene logic devices.

5.2.4 Fabrication and characterization of Graphene grating gate THz detector

Graphene THz detectors with grating gate can be fabricated and characterized to further investigate its viability as a room temperature THz detector.

REFERENCES

1. Y. Wu, K.A. Jenkins, A. Valdes-Garcia, D.B. Farmer, Y. Zhu, A.A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia and P. Avouris, "State-of-the-art Graphene high-frequency electronics," Nano Letters, vol. 12, no. 6, pp. 3062-3067 2012.

2. M. Pindzola, J. Colgan, F. Robicheaux and D. Griffin, "Time-dependent close-coupling calculations for the electron-impact ionization of carbon and neon," Physical Review A, vol. 62, no. 4, pp. 042705 2000

3. Y. Wang, Z. Li, J. Wang, J. Li and Y. Lin, "Graphene and Graphene oxide: Biofunctionalization and applications in biotechnology," Trends Biotechnol., vol. 29, no. 5, pp. 205-212 2011

4. P.K. Misra, Physics of condensed matter, Elsevier, 2012.

5. P.J. Freitas, "Connections between special relativity, charge conservation, and quantum mechanics," arXiv preprint quant-ph/9710051 1997

6. F. Xia, T. Mueller, Y. Lin, A. Valdes-Garcia and P. Avouris, "Ultrafast Graphene photodetector," Nature nanotechnology, vol. 4, no. 12, pp. 839-843 2009

7. C. Rao, U. Maitra and H. Matte, "Synthesis, characterization, and selected properties of Graphene," Graphene: Synthesis, Properties, and Phenomena, pp. 1-47 2012

8. Y.M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.Y. Chiu, A. Grill and P. Avouris, "100-GHz transistors from wafer-scale epitaxial Graphene," Science, vol. 327, no. 5966, pp. 662, Feb 5 2010.

9. H. Xu, Z. Zhang, H. Xu, Z. Wang, S. Wang and L. Peng, "Top-gated Graphene field-effect transistors with high normalized transconductance and designable dirac point voltage," ACS nano, vol. 5, no. 6, pp. 5031-5037 2011

10. O.M. Nayfeh, "Radio-frequency transistors using chemical-vapor-deposited monolayer Graphene: Performance, doping, and transport effects," Electron Devices, IEEE Transactions on, vol. 58, no. 9, pp. 2847-2853 2011.

11. A.A. Balandin, "Thermal properties of Graphene and nanostructured carbon materials," Nature materials, vol. 10, no. 8, pp. 569-581 2011

12. S.O. Koswatta, A. Valdes-Garcia, M.B. Steiner, Y. Lin and P. Avouris, "Ultimate RF performance potential of carbon electronics," Microwave Theory and Techniques, IEEE Transactions on, vol. 59, no. 10, pp. 2739-2750 2011.

13. A.A. Balandin, "Low-frequency 1/f noise in Graphene devices," Nature nanotechnology, vol. 8, no. 8, pp. 549-555 2013.

14. G. Liu, W. Stillman, S. Rumyantsev, Q. Shao, M. Shur and A. Balandin, "Low-frequency electronic noise in the double-gate single-layer Graphene transistors," Appl.Phys.Lett., vol. 95, no. 3, pp. 033103 2009.

15. G. Liu, S. Rumyantsev, M.S. Shur and A.A. Balandin, "Origin of 1/f noise in Graphene multilayers: Surface vs. volume," Appl.Phys.Lett., vol. 102, no. 9, pp. 093111 2013.

16. X. Yang, G. Liu, A.A. Balandin and K. Mohanram, "Triple-mode single-transistor Graphene amplifier and its applications," ACS nano, vol. 4, no. 10, pp. 5532-5538 2010.

17. X. Yang, G. Liu, M. Rostami, A.A. Balandin and K. Mohanram, "Graphene ambipolar multiplier phase detector," Electron Device Letters, IEEE, vol. 32, no. 10, pp. 1328-1330 2011

18. M. Karabiyik, C. Al-Amin and N. Pala, "Graphene-based periodic gate field effect transistor structures for terahertz applications," Nanoscience and Nanotechnology Letters, vol. 5, no. 7, pp. 754-757 2013

19. M. Peplow, "Graphene: The quest for supercarbon," Nature, vol. 503, no. 7476, pp. 327-329, Nov 21 2013

20. L. Liao, Y. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K.L. Wang, Y. Huang and X. Duan, "High-speed Graphene transistors with a self-aligned nanowire gate," Nature, vol. 467, no. 7313, pp. 305-308 2010

21. Y. Wu, Y. Lin, A.A. Bol, K.A. Jenkins, F. Xia, D.B. Farmer, Y. Zhu and P. Avouris, "High-frequency, scaled Graphene transistors on diamond-like carbon," Nature, vol. 472, no. 7341, pp. 74-78 2011

22. M. Kaltschmitt, W. Streicher and A. Wiese, Renewable energy: technology, economics and environment, Springer Science & Business Media, 2007.

23. F. Xia, D.B. Farmer, Y. Lin and P. Avouris, "Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature," Nano letters, vol. 10, no. 2, pp. 715-718 2010

24. D.B. Farmer, Y. Lin and P. Avouris, "Graphene field-effect transistors with self-aligned gates," Appl.Phys.Lett., vol. 97, no. 1, pp. 013103 2010

25. Y. Lin, H. Chiu, K.A. Jenkins, D.B. Farmer, P. Avouris and A. Valdes-Garcia, "Dual-gate Graphene FETs with fT of 50 GHz," Electron Device Letters, IEEE, vol. 31, no. 1, pp. 68-70 2010

26. U. Singisetti, In0.53Ga0.47As MOSFETs with 5 nm channel and self-aligned source/drain by MBE regrowth, University of California, Santa Barbara, 2009.

27. S.K. Hong, S.C. Jeon, W.S. Hwang and B.J. Cho, "Resistance analysis and device design guideline for graphene RF transistors," *2D Materials*, vol. 2, no. 3, pp. 034011 2015.

28. K. Tahy, D. Shilling, T. Zimmermann, H. Xing, P. Fay, R. Feenstra and D. Jena, "Gigahertz operation of epitaxial Graphene transistors," in 2009 Device Research Conference, 2009

29. Badmaev, Y. Che, Z. Li, C. Wang and C. Zhou, "Self-aligned fabrication of Graphene RF transistors with T-shaped gate," ACS nano, vol. 6, no. 4, pp. 3371-3376 2012.

30. G. Simin, M.S. Shur and R. Gaska, "5-terminal THz GaN based transistor with field-and space-charge control electrodes," Int.J.High Speed Electron.Syst., vol. 19, no. 01, pp. 7-14 2009

31. Y. Lin, D.B. Farmer, K.A. Jenkins, Y. Wu, J.L. Tedesco, R.L. Myers-Ward, C.R. Eddy, D.K. Gaskill, C. Dimitrakopoulos and P. Avouris, "Enhanced performance in epitaxial Graphene FETs with optimized channel morphology," Electron Device Letters, IEEE, vol. 32, no. 10, pp. 1343-1345 2011.

32. H.C. Movva, M.E. Ramón, C.M. Corbet, S. Sonde, S.F. Chowdhury, G. Carpenter, E. Tutuc and S.K. Banerjee, "Self-aligned Graphene field-effect transistors with polyethyleneimine doped source/drain access regions," Appl.Phys.Lett., vol. 101, no. 18, pp. 183113 2012.

33. R. Sobot, Wireless Communication Electronics: Introduction to RF Circuits and Design Techniques, Springer Science & Business Media, 2012

34. H. Wang, A. Hsu, D.S. Lee, K.K. Kim, J. Kong and T. Palacios, "Delay analysis of Graphene field-effect transistors," arXiv preprint arXiv:1112.4831 2011

35. P.J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum fT of millimeter-wave MODFETs," Electron Device Letters, IEEE, vol. 10, no. 7, pp. 291-293 1989

36. S. Fukuda, T. Suemitsu, T. Otsuji, D. Kim and J.A. del Alamo, "Analysis of gate delay scaling in In0.7Ga0.3As-channel high electron mobility transistors," Japanese Journal of Applied Physics, vol. 48, no. 4S, pp. 04C086 2009

37. S. Dutta Roy, "Triple frequency impedance matching by frequency transformation," IETE Journal of Education, vol. 55, no. 1, pp. 47-51 2014.

38. G. Simin, Z. Yang, A. Koudymov, V. Adivarahan and M.A. Khan, "III-nitride transistors with capacitively coupled contacts," Appl.Phys.Lett., vol. 89, no. 3, pp. # 033510 2006.

39. D.M. Pozar, Microwave engineering, John Wiley & Sons, 2009

40. D.S. Atlas, "Atlas user's manual," Silvaco International Software, Santa Clara, CA, USA 2005

41. Y. Tan, Y. Zhang, K. Bolotin, Y. Zhao, S. Adam, E. Hwang, S.D. Sarma, H. Stormer and P. Kim, "Measurement of scattering rate and minimum conductivity in Graphene," Phys.Rev.Lett., vol. 99, no. 24, pp. 246803 2007

42. X. Du, I. Skachko, A. Barker and E.Y. Andrei, "Approaching ballistic transport in suspended Graphene," Nature nanotechnology, vol. 3, no. 8, pp. 491-495 2008

43. M. Green, T. Sorsch, G. Timp, D. Muller, B. Weir, P. Silverman, S. Moccio and Y. Kim, "Understanding the limits of ultrathin SiO_2 and Si-O-N gate dielectrics for sub-50 nm CMOS," Microelectronic Engineering, vol. 48, no. 1, pp. 25-30 1999

44. W. Zhu, V. Perebeinos, M. Freitag and P. Avouris, "Carrier scattering, mobilities, and electrostatic potential in monolayer, bilayer, and trilayer Graphene," Physical Review B, vol. 80, no. 23, pp. 235402 2009

45. M. Groner, J. Elam, F. Fabreguette and S.M. George, "Electrical characterization of thin al2O3 films grown by atomic layer deposition on silicon and various metal substrates," Thin Solid Films, vol. 413, no. 1, pp. 186-197 2002.

46. V. Iberi, I. Vlassiouk, X. Zhang, B. Matola, A. Linn, D.C. Joy and A.J. Rondinone, "Maskless lithography and in situ visualization of conductivity of Graphene using helium ion microscopy," Scientific reports, vol. 5 2015

47. X. WinCal, "Cascade microtech inc., beaverton, OR," Available Fall 2006

48. D.A. Frickey, "Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances," IEEE Transactions on Microwave Theory Techniques, vol. 42, pp. 205-211 1994

49. C. Mattevi, G. Eda, S. Agnoli, S. Miller, K.A. Mkhoyan, O. Celik, D. Mastrogiovanni, G. Granozzi, E. Garfunkel and M. Chhowalla, "Evolution of electrical, chemical, and structural properties of transparent and conducting chemically derived Graphene thin films," Advanced Functional Materials, vol. 19, no. 16, pp. 2577-2583 2009.

50. Z. Guo, D. Zhang and X. Gong, "Thermal conductivity of Graphene nanoribbons," Appl.Phys.Lett., vol. 95, no. 16, pp. 163103 2009.

51. C. Lee, X. Wei, J.W. Kysar and J. Hone, "Measurement of the elastic properties and intrinsic strength of monolayer Graphene," Science, vol. 321, no. 5887, pp. 385-388, Jul 18 2008.

52. S. Kwon, C.V. Ciobanu, V. Petrova, V.B. Shenoy, J. Bareno, V. Gambin, I. Petrov and S. Kodambaka, "Growth of semiconducting Graphene on palladium," Nano letters, vol. 9, no. 12, pp. 3985-3990 2009.

53. S. Zhou, G. Gweon, A. Fedorov, P. First, W. De Heer, D. Lee, F. Guinea, A.C. Neto and A. Lanzara, "Substrate-induced bandgap opening in epitaxial Graphene," Nature materials, vol. 6, no. 10, pp. 770-775 2007.

54. M. Mirzadeh and M. Farjam, "First-principles study of bandgap effects in Graphene due to hydrogen adsorption," Journal of Physics: Condensed Matter, vol. 24, no. 23, pp. 235304 2012.

55. M.S. Azadeh, A. Kokabi, M. Hosseini and M. Fardmanesh, "Tunable bandgap opening in the proposed structure of silicon-doped Graphene," Micro & Nano Letters, IET, vol. 6, no. 8, pp. 582-585 2011.

56. D. Kaplan, V. Swaminathan, G. Recine, R. Balu and S. Karna, "Bandgap tuning of mono-and bilayer Graphene doped with group IV elements," J.Appl.Phys., vol. 113, no. 18, pp. 183701 2013.

57. W. Tao, G. Qing, A. Zhi-Min, L. Yan, W. Wen-Bo, S. Kuang and Y. Bin, "The tunable bandgap of AB-stacked bilayer Graphene on SiO2 with H2O molecule adsorption," Chinese Physics Letters, vol. 28, no. 11, pp. 117302 2011.

58. C. Chang, X. Fan, L. Li and J. Kuo, "Band gap tuning of Graphene by adsorption of aromatic molecules," The Journal of Physical Chemistry C, vol. 116, no. 25, pp. 13788-13794 2012.

59. D.H. Lee, J. Yi, J.M. Lee, S.J. Lee, Y. Doh, H.Y. Jeong, Z. Lee, U. Paik, J.A. Rogers and W.I. Park, "Engineering electronic properties of Graphene by coupling with si-rich, two-dimensional islands," ACS nano, vol. 7, no. 1, pp. 301-307 2012.

60. X. Liang, Y. Jung, S. Wu, A. Ismach, D.L. Olynick, S. Cabrini and J. Bokor, "Formation of bandgap and subbands in Graphene nanomeshes with sub-10 nm ribbon width fabricated via nanoimprint lithography," Nano letters, vol. 10, no. 7, pp. 2454-2460 2010.

61. M. Kim, N.S. Safron, E. Han, M.S. Arnold and P. Gopalan, "Fabrication and characterization of large-area, semiconducting nanoperforated Graphene materials," Nano letters, vol. 10, no. 4, pp. 1125-1131 2010.

62. R. Balog, B. Jørgensen, L. Nilsson, M. Andersen, E. Rienks, M. Bianchi, M. Fanetti, E. Lægsgaard, A. Baraldi and S. Lizzit, "Bandgap opening in Graphene induced by patterned hydrogen adsorption," Nature materials, vol. 9, no. 4, pp. 315-319 2010.

63. F. Yavari, C. Kritzinger, C. Gaire, L. Song, H. Gulapalli, T. Borca-Tasciuc, P.M. Ajayan and N. Koratkar, "Tunable bandgap in Graphene by the controlled adsorption of water molecules," Small, vol. 6, no. 22, pp. 2535-2538 2010.

64. L. Solymar, D. Walsh and R.R. Syms, Electrical properties of materials, OUP Oxford, 2014.

65. J.D. Livingston, Electronic properties of engineering materials, Wiley New York, NY, 1999.

66. M.G. Campbell, D.C. Powers, J. Raynaud, M.J. Graham, P. Xie, E. Lee and T. Ritter, "Synthesis and structure of solution-stable one-dimensional palladium wires," Nature chemistry, vol. 3, no. 12, pp. 949-953 2011.

67. M.I. Barja, J. Proupin and L. Núnez, "Microcalorimetric study of the effect of temperature on microbial activity in soils," Thermochimica acta, vol. 303, no. 2, pp. 155-159 1997.

68. P.K. Vabbina, P. Nayyar, A.P. Nayak, A.M. Katzenmeyer, V. Logeeswaran, N. Pala, M.S. Islam and A. Talin, "Synthesis of crystalline ZnO nanostructures on arbitrary substrates at ambient conditions," in SPIE NanoScience Engineering, 2011, pp. 81060H-81060H-9.

69. R. Cuscó, E. Alarcón-Lladó, J. Ibáñez, L. Artús, J. Jiménez, B. Wang and M.J. Callahan, "Temperature dependence of raman scattering in ZnO," Physical Review B, vol. 75, no. 16, pp. 165202 2007.

70. Z.H. Ni, T. Yu, Y.H. Lu, Y.Y. Wang, Y.P. Feng and Z.X. Shen, "Uniaxial strain on graphene: Raman spectroscopy study and band-gap opening," ACS nano, vol. 2, no. 11, pp. 2301-2305 2008.

71. F. Ruffino and M. Grimaldi, "Self-organized patterned arrays of au and ag nanoparticles by thickness-dependent dewetting of template-confined films," J.Mater.Sci., vol. 49, no. 16, pp. 5714-5729 2014.

72. D. Wang and P. Schaaf, "Two-dimensional nanoparticle arrays formed by dewetting of thin gold films deposited on pre-patterned substrates," J.Mater.Sci.: Mater.Electron., vol. 22, no. 8, pp. 1067-1070 2011.

73. T. Yu, Z. Ni, C. Du, Y. You, Y. Wang and Z. Shen, "Raman mapping investigation of Graphene on transparent flexible substrate: The strain effect," The Journal of Physical Chemistry C, vol. 112, no. 33, pp. 12602-12605 2008.

74. Z.H. Ni, T. Yu, Y.H. Lu, Y.Y. Wang, Y.P. Feng and Z.X. Shen, "Uniaxial strain on Graphene: Raman spectroscopy study and band-gap opening," ACS nano, vol. 2, no. 11, pp. 2301-2305 2008.

75. H. Min, B. Sahu, S.K. Banerjee and A. MacDonald, "Ab initio theory of gate induced gaps in Graphene bilayers," Physical Review B, vol. 75, no. 15, pp. 155115 2007.

76. S.S. Carara, R.J. Batista and H. Chacham, "Modifications in Graphene electron states due to a deposited lattice of au nanoparticles: Density functional calculations," Physical Review B, vol. 80, no. 11, pp. 115435 2009.

77. M. Dyakonov and M. Shur, "Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid," Electron Devices, IEEE Transactions on, vol. 43, no. 3, pp. 380-387 1996.

78. N. Pala, F. Teppe, D. Veksler, Y. Deng, M. Shur and R. Gaska, "Nonresonant detection of terahertz radiation by silicon-on-insulator MOSFETs," Electron.Lett., vol. 41, no. 7, pp. 447-449 2005.

79. W. Stillman, F. Guarin, V.Y. Kachorovskii, N. Pala, S. Rumyantsev, M. Shur and D. Veksler, "Nanometer scale complementary silicon MOSFETs as detectors of terahertz and sub-terahertz radiation," in Sensors, 2007 IEEE, 2007, pp. 934-937.

80. F. Schuster, H. Videlier, M. Sakowicz, F. Teppe, D. Coquillat, B. Dupont, A. Siligaris, L. Dussopt, B. Giffard and W. Knap, "Imaging above 1 THz limit with Si-MOSFET detectors," in 35th International Conference on Infrared, Millimeter and Terahertz Waves, 2010, pp. 1.

81. X. Peralta, S. Allen, M. Wanke, N. Harff, J. Simmons, M. Lilly, J. Reno, P. Burke and J. Eisenstein, "Terahertz photoconductivity and plasmon modes in double-quantum-well field-effect transistors," Appl.Phys.Lett., vol. 81, no. 9, pp. 1627-1629 2002.

82. E.A. Shaner, M.C. Wanke, A. Grine, S. Lyo, J. Reno and S. Allen, "Enhanced responsivity in membrane isolated split-grating-gate plasmonic terahertz detectors," Appl.Phys.Lett., vol. 90, no. 18, pp. 181127 2007.

83. D. Veksler, A. Muravjov, W. Stillman, N. Pala and M. Shur, "Detection and homodyne mixing of terahertz gas laser radiation by submicron GaAs/AlGaAs FETs," in Sensors, 2007 IEEE, 2007, pp. 443-445.

84. S. Nadar, H. Videlier, D. Coquillat, F. Teppe, M. Sakowicz, N. Dyakonova, W. Knap, D. Seliuta, I. Kašalynas and G. Valušis, "Room temperature imaging at 1.63 and 2.54 THz with field effect transistor detectors," J.Appl.Phys., vol. 108, no. 5, pp. 054508 2010.

85. A.E. Fatimy, S.B. Tombet, F. Teppe, W. Knap, D. Veksler, S. Rumyantsev, M. Shur, N. Pala, R. Gaska and Q. Fareed, "Terahertz detection by GaN/AlGaN transistors," Electron.Lett., vol. 42, no. 23, pp. 1342-1343 2006.

86. Muravjov, D. Veksler, V. Popov, O. Polischuk, N. Pala, X. Hu, R. Gaska, H. Saxena, R. Peale and M. Shur, "Temperature dependence of plasmonic terahertz absorption in grating-gate gallium-nitride transistor structures," Appl.Phys.Lett., vol. 96, no. 4, pp. 042105 2010.

87. V. Popov, N. Pala and M. Shur, "Room temperature terahertz plasmonic detection by antenna arrays of field-effect transistors," Nanoscience and Nanotechnology Letters, vol. 4, no. 10, pp. 1015-1022 2012.

88. V. Popov, M. Shur, G. Tsymbalov and D. Fateev, "Higher-order plasmon resonances in GaN-based field-effect transistor arrays," Int.J.High Speed Electron.Syst., vol. 17, no. 03, pp. 557-566 2007.

89. L. Vicarelli, M. Vitiello, D. Coquillat, A. Lombardo, A. Ferrari, W. Knap, M. Polini, V. Pellegrini and A. Tredicucci, "Graphene field-effect transistors as room-temperature terahertz detectors," Nature materials, vol. 11, no. 10, pp. 865-871 2012.

90. Di Gaspare, R. Casini, V. Foglietti, V. Giliberti, E. Giovine and M. Ortolani, "Terahertz current oscillations in a gated two-dimensional electron gas with antenna integrated at the channel ends," Appl.Phys.Lett., vol. 100, no. 20, pp. 203504 2012.

91. S. Preu, S. Kim, R. Verma, P. Burke, M. Sherwin and A. Gossard, "An improved model for non-resonant terahertz detection in field-effect transistors," J.Appl.Phys., vol. 111, no. 2, pp. 024502 2012.

92. A.K. Geim and K.S. Novoselov, "The rise of Graphene," Nature materials, vol. 6, no. 3, pp. 183-191 2007.

93. L. Ju, B. Geng, J. Horng, C. Girit, M. Martin, Z. Hao, H.A. Bechtel, X. Liang, A. Zettl and Y.R. Shen, "Graphene plasmonics for tunable terahertz metamaterials," Nature nanotechnology, vol. 6, no. 10, pp. 630-634 2011.

94. T. Gokus, R. Nair, A. Bonetti, M. Bohmler, A. Lombardo, K. Novoselov, A. Geim, A. Ferrari and A. Hartschuh, "Making Graphene luminescent by oxygen plasma treatment," ACS nano, vol. 3, no. 12, pp. 3963-3968 2009.

95. V.P. Verma, S. Das, I. Lahiri and W. Choi, "Large-area Graphene on polymer film for flexible and transparent anode in field emission device," Appl.Phys.Lett., vol. 96, no. 20, pp. 203108 2010.

96. W. Choi, I. Lahiri, R. Seelaboyina and Y.S. Kang, "Synthesis of Graphene and its applications: A review," Critical Reviews in Solid State and Materials Sciences, vol. 35, no. 1, pp. 52-71 2010.

97. L. Zheng, W. Schaich and A. MacDonald, "Theory of two-dimensional grating couplers," Physical Review B, vol. 41, no. 12, pp. 8493 1990.

98. V. V. Popov, Personal Communication.

99. A.A. Dubinov, V.Y. Aleshkin, M. Ryzhii, T. Otsuji and V. Ryzhii, "Terahertz laser with optically pumped Graphene layers and Fabri–Perot resonator," Applied physics express, vol. 2, no. 9, pp. 092301 2009.

100. M.S. Shur and J. Lü, "Terahertz sources and detectors using two-dimensional electronic fluid in high electron-mobility transistors," Microwave Theory and Techniques, IEEE Transactions on, vol. 48, no. 4, pp. 750-756 2000.

101. W. Knap, Y. Deng, S. Rumyantsev, J. Lü, M. Shur, C. Saylor and L. Brunel, "Resonant detection of subterahertz radiation by plasma waves in a submicron field-effect transistor," Appl.Phys.Lett., vol. 80, no. 18, pp. 3433-3435 2002.

102. Satou, I. Khmyrova, V. Ryzhii and M. Shur, "Plasma and transit-time mechanisms of the terahertz radiation detection in high-electron-mobility transistors," Semiconductor science and technology, vol. 18, no. 6, pp. 460 2003.

103. F. Teppe, W. Knap, D. Veksler, M. Shur, A. Dmitriev, V.Y. Kachorovskii and S. Rumyantsev, "Room-temperature plasma waves resonant detection of sub-terahertz radiation by nanometer field-effect transistor," Appl.Phys.Lett., vol. 87, no. 5, pp. 52107-52107 2005.

104. E. Shaner, M. Lee, M. Wanke, A. Grine, J. Reno and S. Allen, "Single-quantum-well grating-gated terahertz plasmon detectors," Appl.Phys.Lett., vol. 87, no. 19, pp. 193507 2005.

105. D. Veksler, F. Teppe, A. Dmitriev, V.Y. Kachorovskii, W. Knap and M. Shur, "Detection of terahertz radiation in gated two-dimensional structures governed by dc current," Physical Review B, vol. 73, no. 12, pp. 125328 2006.

106. V. Ryzhii, I. Khmyrova, A. Satou, P. Vaccaro, T. Aida and M. Shur, "Plasma mechanism of terahertz photomixing in high-electron mobility transistor under interband photoexcitation," J.Appl.Phys., vol. 92, no. 10, pp. 5756-5760 2002.

107. Satou, V. Ryzhii, I. Khmyrova, M. Ryzhii and M. Shur, "Characteristics of a terahertz photomixer based on a high-electron mobility transistor structure with optical input through the ungated regions," J.Appl.Phys., vol. 95, no. 4, pp. 2084-2089 2004.

108. M. Lee, M. Wanke and J. Reno, "Millimeter wave mixing using plasmon and bolometric response in a double-quantum-well field-effect transistor," Appl.Phys.Lett., vol. 86, no. 3, pp. 3501 2005.

109. W. Knap, J. Lusakowski, T. Parenty, S. Bollaert, A. Cappy, V. Popov and M. Shur, "Terahertz emission by plasma waves in 60 nm gate high electron mobility transistors," Appl.Phys.Lett., vol. 84, no. 13, pp. 2331-2333 2004.

110. N. Dyakonova, F. Teppe, J. Łusakowski, W. Knap, M. Levinshtein, A. Dmitriev, M. Shur, S. Bollaert and A. Cappy, "Magnetic field effect on the terahertz emission from nanometer InGaAs/AlInAs high electron mobility transistors," J.Appl.Phys., vol. 97, no. 11, pp. 114313 2005.

111. S. Preu, H. Schwefel, S. Malzer, G. Döhler, L. Wang, M. Hanson, J. Zimmerman and A. Gossard, "Coupled whispering gallery mode resonators in the terahertz frequency range," Optics express, vol. 16, no. 10, pp. 7336-7343 2008.

112. B. Wang and G.P. Wang, "Plasmonic waveguide ring resonator at terahertz frequencies," Appl.Phys.Lett., vol. 89, no. 13, pp. 133106 2006.

113. L. Ju, B. Geng, J. Horng, C. Girit, M. Martin, Z. Hao, H.A. Bechtel, X. Liang, A. Zettl and Y.R. Shen, "Graphene plasmonics for tunable terahertz metamaterials," Nature nanotechnology, vol. 6, no. 10, pp. 630-634 2011.

114. W.A. De Heer, C. Berger, X. Wu, P.N. First, E.H. Conrad, X. Li, T. Li, M. Sprinkle, J. Hass and M.L. Sadowski, "Epitaxial Graphene," Solid State Commun., vol. 143, no. 1, pp. 92-100 2007.

APPENDIX A

SILVACO ATLAS DECK INPUT FILE FOR THE BASELINE GFET

```
##############################################################
# Normal Gate GFET
#
##############################################################
go atlas
Title Baseline GFET characteristics
#
# SILVACO International 1996
#
####################################
# SECTION 1: Mesh input
####################################
mesh nx=61 ny=49
#
x.m n=1 l=0.0 r=1.0
#x.m n=15 l=1.5 r=1.0
#x.m n=29 l=3.5 r=1.0
x.m n=61 l=6 r=1.0
#
y.m n=1 l=-0.2 r=1.0
y.m n=9 l=0 r=1.0
y.m n=10 l=0.012 r=1.0
y.m n=13 l=0.027 r=1.0
y.m n=16 l=0.036 r=1.0
y.m n=20 l=0.0365 r=1.0
y.m n=26 l=0.048 r=1.0
#y.m n=31 l=0.046 r=1.0
y.m n=49 l=0.25 r=1.0
#
####################################
# SECTION 2: Structure Specification
####################################
region num=1 material=Air y.min=-0.2 y.max=0.012
region num=2 material=al2o3 y.min=0.012 y.max=0.027
region num=3 material=SiO2 y.min=0.027 y.max=0.036
region num=4 user.material=graphene y.min=0.036 y.max=0.0365
region num=8 material=sio2 y.min=0.0365 y.max=0.25
#
# electrodes specification
#
elec  name=source x.min=0.0 x.max=0.0 \
y.min=0.02733 y.max=0.09
```

```
elec  name=drain x.min=6 x.max=6 \
y.min=0.02733 y.max=0.09
elec  name=gate x.min=1.5 x.max=4.5 \
y.min=0 y.max=.012

#elec  name=s x.min=0.1 x.max=1.4 \
#y.min=0 y.max=.012
#elec  name=d x.min=4.6 x.max=5.9 \
#y.min=0 y.max=.012



contact num=1 name=source resistance=130
contact num=2 name=drain resistance=130
contact num=3 name=gate work=4.8
contact num=4 name=s work=4.8
contact num=5 name=d work=4.8

interface intregion="3/4" charge=+7e12
#interface intregion="3/4" charge=-4.8e12
#

#####################################
# SECTION 3: Material Models
#####################################
#
# material parameters
#
material material=Graphene user.group=semiconductor \
user.default=silicon affinity=7.5 eg300=0 permitt=9.5 \
mun=336 mup=530 nc300=0  nv300=0

# mobility velocity model
#
#model print srh fldmob
#mobility material=Graphene fldmob.n fldmob.p \
# betan=2.6 betap=2.6 vsatn=2.7e7 vsatp=2.7e7 \
#evsatmod=0 hvsatmod=0

method newton trap itlim=35 maxtrap=6 \
vsatmod.inc=0.1 carriers=2

output con.band val.band j.total
#
solve initial
```

```
solve vgate=0
save outf=IV_band_0d.str
#####################################
# SECTION 5: Ids-Vds calculation
#####################################
#log off
#
##method newton trap itlim=35 maxtrap=6 \
##vsatmod.inc=0.1 carriers=1 elec
#
##solve init
##save outf=dev.str
##tonyplot dev.str
#
# Apply a set of biases at the gate and save solutions
#
##solve vgate=-2 outf=idvd(-2).out

#
# Calculate IV characteristic at Vg=-6
#
##load inf=idvd(-2).out
##log outf=idvd(-2).log
##solve outf=idvd(-2).out master
##solve v4=0 vstep=-.5 name=s vfinal=-3
##solve v5=0 vstep=-.5 name=d vfinal=-3
##solve vdrain=0.0 vstep=0.1 name=drain vfinal=5
#
##tonyplot -nosplash idvd(-2).log -set idvd.set

##quit

#
#####################################
# SECTION 5: Ids-Vgs calculation
#####################################

method trap newton itlim=35 maxtrap=6 \
vsatmod.inc=0.1 carriers=1 elec

output con.band val.band j.total
#
solve initial
save outf=IV_band_0d.str
solve vdrain=0 vstep=1 name=drain vfinal=5
```

```
log outf=IV_gm_d0.log master
#solve v4=0 vstep=-.5 name=s vfinal=-1
#solve v5=0 vstep=-.5 name=d vfinal=-1
solve vgate=-2 vstep=.4 name=gate vfinal=10

#
tonyplot -nosplash IV_gm_d0.log

tonyplot -nosplash IV_band_0d.str

quit
#####################################
# SECTION 5: Ids-Vgs calculation
#####################################
method newton trap itlim=35 maxtrap=6 \
vsatmod.inc=0.1 carriers=2
#
solve init

solve vgate=-2
save outf=bias.str
#tonyplot bias.str
#solve v4=0 vstep=-.5 name=s vfinal=-3.0
#solve v5=0 vstep=-.5 name=d vfinal=-3.0
solve vdrain=0 vstep=.5 name=drain vfinal=5

save outf=structure.str

log outf=acac.log master gains s.params \
inport=gate outport=drain width=100
#

# AC calculation
#
solve ac freq=10 fstep=1.8 mult.f nfstep=50

#tonyplot -nosplash -add IV_gm_d.log IV_band_0d.str
tonyplot -nosplash acac.log -set ac.set

quit
```

APPENDIX B

SILVACO ATLAS DECK INPUT FILE FOR THE 5-TERMINAL GFET

```
##############################################################
# Normal Gate GFET
##############################################################
go atlas
Title 5-terminal GFET characteristics
#
# SILVACO International 1996
#
####################################
# SECTION 1: Mesh input
####################################
mesh nx=61 ny=49
#
x.m n=1 l=0.0 r=1.0
#x.m n=15 l=1.5 r=1.0
#x.m n=29 l=3.5 r=1.0
x.m n=61 l=6 r=1.0
#
y.m n=1 l=-0.2 r=1.0
y.m n=9 l=0 r=1.0
y.m n=10 l=0.012 r=1.0
y.m n=13 l=0.027 r=1.0
y.m n=16 l=0.036 r=1.0
y.m n=20 l=0.0365 r=1.0
y.m n=26 l=0.048 r=1.0
#y.m n=31 l=0.046 r=1.0
y.m n=49 l=0.25 r=1.0
#
####################################
# SECTION 2: Structure Specification
####################################
region num=1 material=Air y.min=-0.2 y.max=0.012
region num=2 material=al2o3 y.min=0.012 y.max=0.027
region num=3 material=SiO2 y.min=0.027 y.max=0.036
region num=4 user.material=graphene y.min=0.036 y.max=0.0365
region num=8 material=sio2 y.min=0.0365 y.max=0.25
#
# electrodes specification
#
elec  name=source x.min=0.0 x.max=0.0 \
y.min=0.02733 y.max=0.09
```

```
elec  name=drain x.min=3.5 x.max=3.5 \
y.min=0.02733 y.max=0.09
elec  name=gate x.min=1.5 x.max=2 \
y.min=0 y.max=.012

elec  name=s x.min=0.1 x.max=1.4 \
y.min=0 y.max=.012
elec  name=d x.min=2.1 x.max=3.4 \
y.min=0 y.max=.012



contact num=1 name=source resistance=130
contact num=2 name=drain resistance=130
contact num=3 name=gate work=4.8
contact num=4 name=s work=4.8
contact num=5 name=d work=4.8

interface intregion="3/4" charge=+6.3e12
#interface intregion="3/4" charge=-4.8e12
#

####################################
# SECTION 3: Material Models
####################################
#
# material parameters
#
material material=Graphene user.group=semiconductor \
user.default=silicon affinity=7.5 eg300=0 permitt=9.5 \
mun=1603 mup=2530 nc300=0  nv300=0

# mobility velocity model
#
#model print srh fldmob
#mobility material=Graphene fldmob.n fldmob.p \
# betan=2.6 betap=2.6 vsatn=2.7e7 vsatp=2.7e7 \
#evsatmod=0 hvsatmod=0

method newton trap itlim=35 maxtrap=6 \
vsatmod.inc=0.1 carriers=2

output con.band val.band j.total
#
solve initial
```

```
solve vgate=0
save outf=IV_band_0d.str
####################################
# SECTION 5: Ids-Vds calculation
####################################
#log off
#
method newton trap itlim=35 maxtrap=6 \
vsatmod.inc=0.1 carriers=1 elec
#
solve init
save outf=dev.str
tonyplot dev.str
#
# Apply a set of biases at the gate and save solutions
#
solve vgate=-2 outf=idvd(-2).out

#
# Calculate IV characteristic at Vg=-6
#
load inf=idvd(-2).out
log outf=idvd(-2).log
solve outf=idvd(-2).out master
solve v4=0 vstep=-.5 name=s vfinal=-3
solve v5=0 vstep=-.5 name=d vfinal=-3
solve vdrain=0.0 vstep=0.1 name=drain vfinal=5
#
tonyplot -nosplash idvd(-2).log -set idvd.set

quit

#
####################################
# SECTION 5: Ids-Vgs calculation
####################################

method trap newton itlim=35 maxtrap=6 \
vsatmod.inc=0.1 carriers=1 hole

output con.band val.band j.total
#
solve initial
save outf=IV_band_0d.str
solve vdrain=0 vstep=1.11 name=drain vfinal=5
```

```
log outf=IV_gm_d0.log master
#solve v4=0 vstep=-.5 name=s vfinal=-1
#solve v5=0 vstep=-.5 name=d vfinal=-1
solve vgate=-2 vstep=.4 name=gate vfinal=10

#
tonyplot -nosplash IV_gm_d0.log

tonyplot -nosplash IV_band_0d.str


#####################################
# SECTION 5: Ids-Vgs calculation
#####################################
method newton trap itlim=35 maxtrap=6 \
vsatmod.inc=0.1 carriers=2
#
solve init

solve vgate=-2
save outf=bias.str
#tonyplot bias.str
#solve v4=0 vstep=-.5 name=s vfinal=-3.0
#solve v5=0 vstep=-.5 name=d vfinal=-3.0
solve vdrain=0 vstep=.5 name=drain vfinal=5

save outf=structure.str

log outf=acac.log master gains s.params \
inport=gate outport=drain width=100
#

# AC calculation
#
solve ac freq=10 fstep=1.8 mult.f nfstep=50

#tonyplot -nosplash -add IV_gm_d.log IV_band_0d.str
tonyplot -nosplash acac.log -set ac.set

quit
```

APPENDIX C

ON-WAFER S-PARAMETER MEASUREMENT DIRECTIONS

Step-1: Turn on the HP 8510 C VNA, wait until it finishes booting

Step-2: Connect one end of the GPIB cable to the HPIB port on back panel of the VNA, the other end to a computer's USB port

Step-3: Download and install NI MAX from National Instrument website

Step-3: Check the GPIB address of the tool using the front panel and look for this tool in NI MAX. Listing of this tool in NI MAX indicates that a connection has been stablished.

Step-4: Download and install WinCal XE from Cascade Microtech website

Step-5: After installation, run and select HP 8510 C from the dropdown menu under VNA tab, "VNA Found" message indicates that a secure connection has been stablished

Step-6: Place the CS-5 calibration substrate on the probe station, and identify the Short, Open, Load, and Thru structures on the substrate using microscope with help of the calibration substrate manual

Step-7: Setup the frequency range, number of points, and power from the VNA tab of the software

Step-8: Click calibration tab and select 2-port SOLT

Step-9: Place both of the GSG probes on Short structure of the CS-5 substrate, and click measure next to the Short tab on the software. It will perform measurements and save all by itself. Repeat this process for Open, Load, and Thru. After all the measurements associated with calibration, save this calibration file with appropriate name.

Step-9: Replace CS-5 with the DUT, apply additional bias to the bias-T if required, click 2-port S-parameters in the measurement tab, and click run.

Step-10: Once measurements are finished, load your calibration file from Correction tab, the raw data will be corrected.

Step-11: Plot and analyze.

VITA

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2010-2016	Doctoral Candidate, Electrical Engineering Florida International University Miami, Florida

PUBLICATIONS AND PRESENTATION

Al-Amin, C., Karabiyik, M., Vabbina, P., and Pala, N. , "*Fabrication of Graphene Field-Effect Transistor with Field Controlling Electrodes to Improve fT*," Electronics Letter (Submitted) (2016)

Al-Amin, C., Vabbina, P., Sinha, R. and Pala, N. , "*Bandgap Engineering of Single Layer Graphene by Randomly Distributed Nanoparticles*," Journal of Material Science (Submitted) (2016)

Al-Amin, C., Karabiyik, M., Vabbina, P., Sinha, R. and Pala, N. , "*Graphene FETs with Low-Resistance Hybrid Contacts for Improved High Frequency Performance*," Nanomaterials (Submitted) (2016)

Al-Amin, C., Karabiyik, M., Vabbina, P., Sinha, R. and Pala, N. , "*Field controlled RF Graphene FETs with improved high frequency performance*," Solid-State Electronics 95, 36-41 (2014)

Al-Amin, C., Vabbina, P. K., Karabiyik, M., Sinha, R., Pala, N. and Choi, W. , "*Improving High-Frequency Characteristics of Graphene FETs by Field-Controlling Electrodes*," IEEE Electron Device Letter (2013)

Al-Amin, C., Vabbina, P., Karabiyik, M., and Pala, N., "*Bandgap engineering of Graphene decorated with randomly distributed ZnO nano-seed*", SPIE DSS, 2016 (Accepted)

Al-Amin, C., Sinha, R., Pala, N. and Choi, W., "*Lowering contact resistance of Graphene FETs with capacitive extension of ohmic contacts for enhanced RF performance*", SPIE DSS, 2015

Al-Amin, C., Sinha, R., Pala, N. and Choi, W., "*Novel Graphene FETs with field-controlling electrodes to improve RF performance*", SPIE DSS, 2014