AN ACCURATE, TRIMLESS, HIGH PSRR, LOW-VOLTAGE, CMOS BANDGAP REFERENCE IC

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AN ACCURATE, TRIMLESS, HIGH PSRR, LOW-VOLTAGE, CMOS BANDGAP REFERENCE IC

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To my Mother, my clearest vision of God

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LIST OF SYMBOLS AND ABBREVIATIONS

I_{LOAD}	Load Current
V_{REF}	Reference Voltage
V_{BE}	Base-Emitter Voltage
V_T	Thermal Voltage
CTAT	Complementary-to-Absolute-Temperature
DEM	Dynamic-Element Matching
EEPROM	Electrically Erasable Programmable Read-Only Memory
IC	Integrated Circuit
LDO	Low Dropout
LDR	Load Regulation
LNR	Line Regulation
PSRR	Power-Supply Ripple Rejection
PTAT	Proportional-to-Absolute-Temperature
SoC	System-on-Chip
TC	Temperature Coefficient
UGF	Unity-Gain Frequency

SUMMARY

Bandgap reference circuits are used in a host of analog, digital, and mixed-signal systems to establish an accurate voltage standard for the entire IC. The accuracy of the bandgap reference voltage under steady-state (dc) and transient (ac) conditions is critical to obtain high system performance. In this work, the impact of process, power-supply, load, and temperature variations and package stresses on the dc and ac accuracy of bandgap reference circuits has been analyzed. Based on this analysis, the a bandgap reference that

1. has high dc accuracy despite process and temperature variations and package stresses, without resorting to expensive trimming or noisy switching schemes,
2. has high dc and ac accuracy despite power-supply variations, without using large off-chip capacitors that increase bill-of-material costs,
3. has high dc and ac accuracy despite load variations, without resorting to error-inducing buffers,
4. is capable of producing a sub-bandgap reference voltage with a low power-supply, to enable it to operate in modern, battery-operated portable applications,
5. utilizes a standard CMOS process, to lower manufacturing costs, and
6. is integrated, to consume less board space

has been proposed. The functionality of critical components of the system has been verified through prototypes after which the performance of the complete system has been evaluated by integrating all the individual components on an IC.

The proposed 0.6μm-CMOS bandgap reference can withstand 5mA of load variations while generating a reference voltage of 890mV that is accurate with respect to temperature to the first order. It exhibits a trimless, dc 3-σ accuracy performance of 0.84% over a temperature range of -40°C to 125°C and has a worst case ac power-supply

ripple rejection (PSRR) performance of –30dB up to 50MHz using 60pF of on-chip capacitance. All the proposed techniques lead to the development of a CMOS bandgap reference that meets the low-cost, high-accuracy demands of state-of-the-art System-on-Chip environments.

CHAPTER 1

INTRODUCTION

As systems advance towards increasing levels of integration, almost all integrated circuits require an accurate on-chip bandgap reference for optimal system performance. This chapter describes the operating principles of bandgap references along with classical implementations. The primary specifications of bandgap references are then defined and discussed, followed by a discussion on the increasingly popular System-on-Chip (SoC) approach and its impact on the design of state-of-the-art bandgap references. Finally, the objectives of the research are outlined.

1.1 The Basic Bandgap Reference

An accurate voltage or current reference is an important component of most integrated circuits. As its name suggests, a reference establishes a stable point (either a voltage or current) that the rest of the circuits in the system can utilize for generating reliable and predictable results. Whether used with a regulator to build a power-supply [1], in an operational amplifier to set up a bias point [2], or in an analog-to-digital converter (ADC) to establish a standard to compare voltages against [3], the accuracy of the reference directly impacts and often dictates the overall performance of a system.

The bandgap reference circuit has been the most elegant way to fashion an integrated circuit (IC) voltage reference [4]-[6]. The circuit operates on the principle of adding a voltage that decreases linearly with temperature to one that increases linearly with temperature to produce a reference voltage that is stable with respect to temperature to the first order. Barring a small curvature, the base-emitter voltage of a bipolar transistor in the active region decreases linearly with temperature, i.e., it has a complementary-to-absolute-temperature (CTAT) dependence. The voltage that increases

linearly with temperature, i.e., the proportional-to-absolute-temperature (PTAT) voltage, is produced through the difference in the base-emitter voltages of two bipolar transistors operating under different current densities (a manifestation of the well-known Gilbert principle [7]). A bandgap reference circuit adds these CTAT and PTAT voltages to produce a temperature-independent voltage V_{REF}, as shown in Fig. 1.1. Conventionally, since the CTAT component is generated from a diode or base-emitter voltage, the value of the reference voltage is close to the bandgap voltage of silicon (≈1.2V). The reason for this is that the diode voltage has various temperature dependent terms and its zero-order or temperature-independent component is the bandgap voltage.

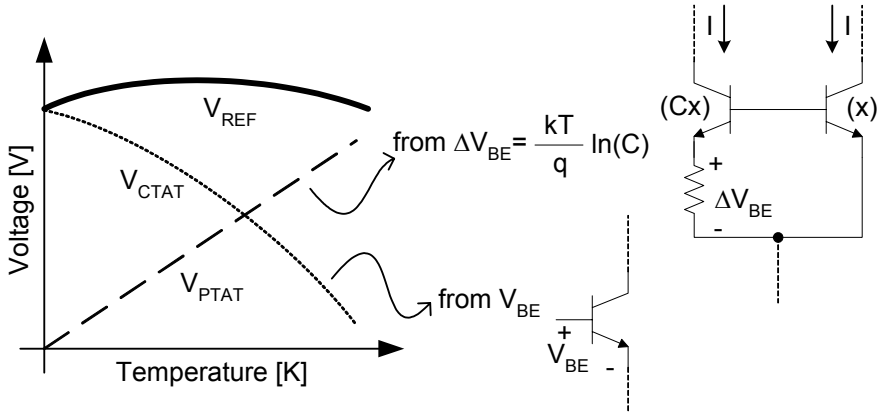


Fig. 1.1. Temperature behavior of a typical bandgap reference circuit.

The Brokaw cell [5] shown in Fig. 1.2 forms the building block of most state-of-the-art bandgap references [6]-[15]. The current-mirror forces the same current to both bipolar transistors Q_1 and Q_2, which have unequal areas and hence different base-emitter voltages. The difference of the base-emitter voltages of transistors Q_1 and Q_2, when applied to resistor R, produces a PTAT current I_{PTAT} and, consequently, a PTAT voltage V_{PTAT} across resistor R_{PTAT}:

$$V_{BE} = V_T \ln\left(\frac{I_C}{J_S \cdot \text{Area}}\right) \tag{1.1}$$

and

$$I_{PTAT} \equiv I_{C2} = I_{C1} = \frac{V_T}{R}\ln\left(C \cdot \frac{I_{C1}}{I_{C2}}\right) = \frac{V_T}{R}\ln(C). \tag{1.2}$$

This voltage, having a positive temperature coefficient, is then added to the base-emitter voltage of Q_1, which has a negative temperature coefficient to generate the temperature stable reference voltage V_{REF} [6], which is given by

$$V_{REF} = V_{CTAT} + V_{PTAT} = V_{BE1} + 2I_{PTAT}R_{PTAT} \tag{1.3}$$

or

$$V_{REF} = V_{BE1} + 2V_T \ln(C)\frac{R_{PTAT}}{R}. \tag{1.4}$$

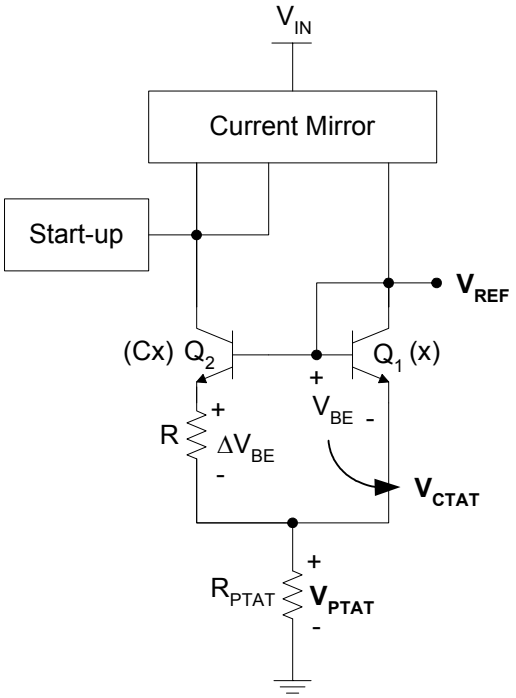


Fig. 1.2. Basic building block of bandgap reference circuits.

Note that one possible solution of Eqn. (1.2) occurs when both I_{C1} and I_{C2} are zero, in other words, the bandgap reference is in a zero-current or "off" state. The circuit can be pulled out of this state if a perturbation of sufficient energy is applied – which is why all bandgap reference circuits require a start-up block that supply this energy and thereby prevent the reference from settling into this undesired yet stable state. In the circuit of Fig. 1.2, the start-up block draws current from the low-impedance node when

the circuit is in the undesired "off" state. This current is then mirrored and forced into the collector of Q_1 and the circuit eventually settles into the desired stable state when the branch currents are defined by the non-zero solution of Eqn. (1.2) [6].

1.2 Primary Specifications

The principal role of a bandgap reference circuit is to generate an accurate and reliable reference voltage and most of its key specifications quantify the deviation of this voltage from its ideal value in the presence of various sources of error. These error sources exhibit a diverse behavior – they may be random or systematic in nature, affect the reference under dc or transient conditions, and have a short- or long-term influence on the accuracy of the output voltage. The impact of various error sources on the dc and ac accuracy of bandgap references shall be analyzed in detail in the subsequent chapters.

The initial accuracy of a reference quantifies the effect of random process variations, mismatch, and package stresses on the dc accuracy of the reference voltage. While the systematic component of these error sources can be accounted for through careful calibration, the random component affects each sample uniquely and initial accuracy can therefore only be specified after statistical analysis of a large sample size. It is defined as the ratio of the 3-σ variation ($3\cdot\sigma_{VREF}$) of a reference, over a large number of samples, to the mean value (μ_{VREF}), and is given by

$$\text{Initial Accuracy} = \pm\frac{3\cdot\sigma_{VREF}}{\mu_{VREF}}. \tag{1.5}$$

During the design phase, the designer uses simulations on the initial accuracy of the untrimmed reference to determine the number of trim bits required to achieve a given accuracy specification. During the testing phase, the initial accuracy of the reference is measured after trim over several devices that have been obtained, ideally, from multiple wafers and multiple lots. Since trimming is carried out at room temperature for purposes of convenience, the initial accuracy is typically specified at room temperature (27°C).

The temperature coefficient (TC) of a reference voltage quantifies the effect of temperature variations on its dc accuracy and is given by

$$TC = \frac{V_{REF-max} - V_{REF-min}}{\left(\frac{V_{REF-max} + V_{REF-min}}{2}\right)} \cdot \frac{1}{T_{high} - T_{low}}, \tag{1.6}$$

where T_{high} and T_{low} are the upper and lower extremes of the measured temperature range and $V_{REF\text{-}max}$ and $V_{REF\text{-}min}$ are the maximum and minimum values of the reference voltage in this range. In other words, the TC of a reference is given by the deviation of the output voltage from its mean value in the tested temperature range. A reference in which the first-order temperature coefficient of V_{BE} has been compensated has an ideal TC of 15-20ppm/°C due to the remaining non-linearity in V_{BE} (corresponding to roughly 3-4mV deviation on a 1.2V reference over -40°C to 125°C). Random process variations, mismatch, and package stresses alter the TC performance of a reference from its theoretical systematic value by introducing inaccuracies in the CTAT and PTAT components of the reference voltage that affect each sample uniquely. Practically, therefore, TC is specified by the box method, whereby it is calculated by using the absolute maximum and minimum reference voltage among all measured samples across the entire temperature range in Eqn. (1.6).

The dc and ac immunity of the bandgap reference to variations in the line or power-supply voltage is specified by its line regulation (LNR) or power-supply ripple-rejection (PSRR) performance, respectively. The former is the ratio of the dc change in the reference voltage (ΔV_{REF}) per unit dc change in the line (ΔV_{IN}), while the latter is the frequency-dependent ratio of the small-signal ac ripple in the reference voltage (δV_{REF}) generated by a corresponding ripple in the power-supply (δV_{IN}). These performance parameters are given by

$$LNR = \left.\frac{\Delta V_{REF}}{\Delta V_{IN}}\right|_{DC} \tag{1.7}$$

and

$$\text{PSRR} = \left.\frac{\delta V_{REF}}{\delta V_{IN}}\right|_{f}. \tag{1.8}$$

The ability of a reference to maintain its accuracy despite changes in loading conditions is crucial in many IC applications. Under dc conditions, the load regulation (LDR) of a reference measures the dc change in the reference voltage (ΔV_{REF}) per unit dc change in the load current (ΔI_{OUT}). The output impedance of the reference (Z_{out}), on the other hand, is a frequency dependent ac specification that quantifies the small-signal change in the reference (δV_{REF}) for a small-signal change in the load current (δI_{OUT}). LDR and Z_{out} are given by

$$\text{LDR} = \left.\frac{\Delta V_{REF}}{\Delta I_{OUT}}\right|_{DC} \tag{1.9}$$

and

$$Z_{out} = \left.\frac{\delta V_{REF}}{\delta I_{OUT}}\right|_{f}. \tag{1.10}$$

For portable applications, the specifications of power consumption and dropout voltage are also very important. Since portable applications are mostly powered from a battery-pack, low power consumption is critical to extend battery life. The dropout voltage is defined as the minimum difference in the output (V_{REF}) and input (V_{IN}) a reference can withstand while maintaining an accurate output. A low dropout voltage is crucial to the reference's ability to operate reliably even as the battery discharges to a low voltage. Other important specifications of a bandgap reference include thermal hysteresis (the change in V_{REF} after operating the reference at 27°C, cycling it through the entire temperature range, and returning to 27°C), long-term drift (change in the output voltage after months or years – it is specified by measuring the change in the reference voltage after 1,000 to 2,000 hours of continuous operation), and output noise.

1.3 Impact of the System-on-Chip (SoC) Paradigm

The 21st century has witnessed an explosion in the market demand for portable applications like cellular phones, personal digital assistants, pagers, and laptops [16]-[19]. Since these electronics are primarily battery-operated, power is always at a premium and circuits like dc-dc converters, linear regulators, and bandgap references, that form an integral component of their power management architecture, are critical to system performance. The primary market requirements for these portable systems are high functional integration (e.g. audio, video, imaging, and web), small size, and most importantly, low cost [17]-[19].

The System-on-Chip (SoC) paradigm satisfies these criteria by fabricating digital, RF, and analog circuits on the same substrate to deliver solutions that are multi-functional (due to the diversity of the circuits that have been integrated) and yet compact (since they use a minimal number of off-chip components) [17]-[19]. Both these characteristics of SoCs increase the speed of product-design cycles, lower manufacturing times, and conserve board area, thereby lowering costs overall. While the SoC paradigm offers solutions to the most important market demands on portable applications, in doing so, it poses a number of design challenges for power management circuits, in general, and a bandgap reference circuit, in particular.

Since SoC solutions for high volume portable applications are always cost conscious, they demand references that have a high degree of precision while incurring minimal manufacturing costs. The dc accuracy of bandgap references is particularly sensitive to process variations and package- and process-induced mismatches whose adverse effects on accuracy varies across devices, wafers, lots, and technology nodes, impacting each device uniquely. As a result, trimming (i.e., tweaking) the output voltage is necessary to produce predictable, and therefore reliable, reference values [6]. Although the effectiveness of trimming cannot be denied, the increase in manufacturing time and equipment costs (e.g., laser) is often prohibitive for state-of-the-art low-cost solutions

[20]-[23]. At the same time, state-of-the-art applications demand a box method accuracy of 1% (with an initial accuracy of 0.5%), making the task of obtaining high initial accuracy without incurring trimming costs extremely challenging.

Cost-conscious SoCs are also increasingly using standard CMOS processes that require fewer masking steps, and hence incur lower costs, than their BiCMOS counterparts [19]. This trend is forcing designers to build critical analog blocks, including voltage references, in the same cost-effective CMOS technologies that were conventionally used to build only digital systems [13]-[15], [20]-[23]. Given the low breakdown voltages of these high resolution CMOS technologies, SoC solutions must survive low supply voltages and generate low-voltage references with high precision. In other words, the reference designed in these state-of-the-art CMOS processes must incur low dropout voltages.

The call for obtaining various functionalities from the same handheld device has led to the fabrication of dense analog circuits (e.g. references, regulators), digital blocks (e.g. microprocessors, DSPs) and RF electronics (e.g. oscillators, filters) on the same substrate, consistent with the SoC approach. These environments are plagued by noise, generated by the switching of digital circuits, RF blocks, and dc-dc converters, that can have amplitudes of the order of hundreds of millivolts and frequency components in the range of tens of kilohertz to hundreds of megahertz [24]-[27]. This noise, propagated onto the supplies through crosstalk, deteriorates the performance of sensitive analog blocks, like the synthesizer and VCO, and manifests itself as jitter in their respective outputs [1], [24], [25], [28], [29]. In this scenario, a bandgap reference circuit having a high precision despite fluctuations in the power-supply, i.e. high PSRR performance, is crucial to maximizing system performance [30]-[34]. These fluctuations also couple capacitively onto the output of the reference, making it crucial for the reference to exhibit low output impedance to shunt this noise. Finally, an important impact of the increased

functionality incorporated onto an SoC IC is that it warrants a bandgap reference that consumes low power to maximize battery life.

A small size or form factor is critical to increase the portability of a mobile device. Since passive components (resistors, capacitors, and inductors) contribute significantly to required board area, circuits that deliver high performance while using integrated passives are in high demand [16]. For a bandgap reference, this requirement translates to an ability to provide an accurate output voltage across line and load transients without the aid of external coupling capacitors. In other words, the entire bandgap reference circuit must be completely integrated and monolithic. Table 1.1 summarizes the market demands of SoC solutions for portable applications and their impact on the design of state-of-the-art bandgap references.

Table 1.1. Characteristics of SoC solutions and their impact on the design of bandgap references.

Characteristic of SoC Solutions	**Requirements on Bandgap References**
Low cost	Trimless
CMOS	Low dropout, low-voltage output
High functionality	High PSRR
	Low output impedance
	Low power
Small size	Integrated

1.4 Research Objectives

The primary thrust of this research is to enhance the accuracy of bandgap reference circuits. It addresses the inherent tradeoffs in state-of-the-art techniques to improve reference accuracy and endeavors to develop novel design strategies that retain the advantages of these techniques without incurring their drawbacks. The proposed strategies have been developed within the context of cutting-edge SoC integration and its

associated challenges, thereby establishing the relevance of this research not only for current but also future bandgap reference designs.

The bandgap reference proposed shall have a targeted box-method accuracy of 1%, which shall be measured over the extended industrial temperature range of -40°C to 125°C, along with an initial accuracy of 0.5% – a performance that rivals that of state-of-the-art IC references. Historically, this level of precision has been achievable primarily through trimming [6], [10], [15]. However, since the target application for the proposed reference is a low-cost SoC, the design aims to achieve this performance without resorting to conventional trimming techniques, which increase manufacturing times and hence deleteriously impact cost. The accuracy shall be measured over multiple samples to increase the statistical validity of the measured results.

Since most modern SoCs use cost-effective digital CMOS processes to design the entire system, including critical analog blocks that conventionally used high performance BiCMOS and bipolar processes [19], the AMI 0.6µm CMOS process (available through MOSIS) will be the technology of choice for the bandgap reference design. The design will aim to maximize the potential of the standard, existing process flow to gain performance advantages for the system.

A common characteristic of modern CMOS processes is their low breakdown voltage, which is often less than the conventional bandgap reference value of 1.2V, thereby necessitating the development of sub-bandgap reference topologies with low dropout. The AMI 0.6µm process has a breakdown voltage of 5V, which is relatively high compared to current CMOS processes, and the threshold voltages of its MOS devices are accordingly large ($V_{TP\text{-}nom}$ = -0.92V and $V_{TN\text{-}nom}$ = -0.67V). These high values impose serious limitations on the minimum operating supply voltage and dropout of the target reference and measurement results may not be indicative of its low-voltage capability. However, the target reference shall be designed under the stringent voltage constraints imposed by modern, low-voltage CMOS processes and would thereby allow a

designer with access to such processes to implement a similar voltage reference. The design target for the reference voltage shall be 900mV, though the design would have the capability of generating any desired sub-bandgap reference voltage.

SoC environments are afflicted by high frequency switching noise that couples onto supply lines and the reference output through crosstalk and degrades the accuracy of integrated bandgap references. These high frequency line fluctuations can be simply and effectively reduced by using appropriately large filter capacitors that provide transient currents to noisy nodes and thereby improve the transient accuracy of the reference [1], [25]. As systems advance towards increasing integration, however, using large, off-chip filter capacitors at the input and output of a bandgap reference is increasingly prohibitive. To this end, the target reference aims to develop strategies that allow it to achieve high PSRR and low output impedance without resorting to large capacitors that resist integration or take up valuable silicon real estate. While systems having a worst-case PSRR of -40dB have been reported using 1.2nF of on-chip capacitance [29], the target reference aims to achieve a PSRR of -30dB using less than 100pF of capacitance since modern SoCs will find a more modest PSRR performance easier to absorb than the significantly higher area demanded by a 1.2nF capacitance.

1.4.1 Target Specifications

With these principles in mind, the objective of this research is to design and implement a high precision CMOS bandgap reference that shall exhibit high dc and ac immunity to temperature, process variations, changes in supply voltage, package stresses, and ac-coupled noise *without any trimming* or additional exotic process steps. In particular, this project explores a number of alternative strategies to implement a trimless, integrated, all-CMOS, low-voltage, regulated bandgap reference topology that is expected to achieve a dc 3-σ box method accuracy better than 1% over a temperature range of -40°C to 125°C, a worst-case PSRR performance of -30dB over the entire

frequency spectrum, and is capable of sourcing 5mA of load current while generating a first-order temperature compensated reference voltage of 900mV. The concept of the proposed system is presented in Fig. 1.3.

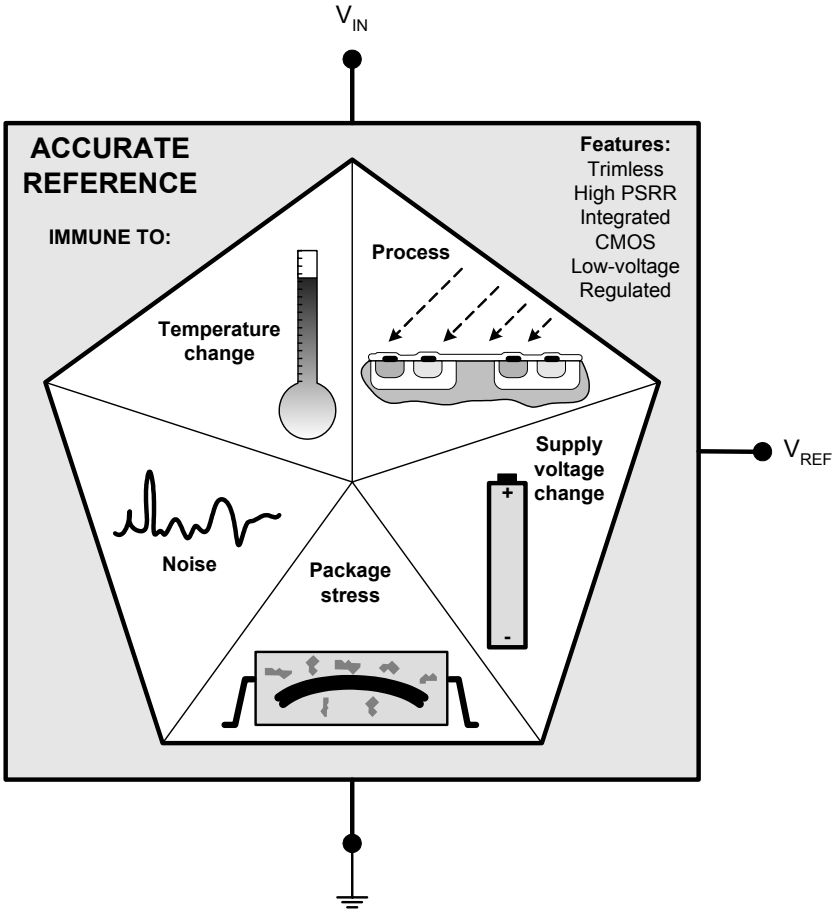


Fig. 1.3. Concept of proposed system.

1.5 Synopsis

System-on-Chip environments impose stringent demands on the accuracy-performance of bandgap references. References for SoC applications must exhibit a high immunity to process variations, mismatch, package stresses and temperature without resorting to costly trimming schemes, must exhibit high PSRR performance and low output impedance without using area-intensive capacitors, and be compatible with modern low-voltage CMOS processes that do not have conventional high performance

devices at their disposal. The design targets for this research are a 900mV first-order temperature-compensated reference voltage with 1% box -accuracy, -30dB worst case PSRR, and 5mA current sourcing capability.

CHAPTER 2

ERROR SOURCES

The study of the sources of error that introduce inaccuracies in references is extremely important in an environment in which the precision of a system's bandgap reference often dictates its overall accuracy performance. Analyzing these various error sources allows a designer to assess their relative impact on the accuracy of the reference voltage and thereby make important decisions regarding all aspects of the design, such as process technology, circuit topology, trim network, layout, and packaging.

A number of factors degrade the accuracy of CMOS bandgap reference circuits, including process variations and mismatch [21]-[23], [35], package stresses [36]-[37], power-supply fluctuations [30]-[34], load variations [10], [38]-[39], and temperature changes [6], [40]. This chapter discusses these various error sources and quantifies their impact on accuracy. Errors due to process variations and mismatch are first analyzed, after which the systematic and random effects of package shift are studied. Next, an intuitive model for predicting the effect of line variations on accuracy is presented. The effects of load variations on the output of a reference are then discussed. Finally, the deviation of the reference voltage due to temperature changes is analyzed.

2.1 Process Variations and Mismatch

Conventionally, process variations and mismatch have been considered to be error sources that a circuit designer has no control over. Their harmful effects have therefore been mitigated primarily through careful layout followed by intensive trimming during the manufacturing process. However, as requirements on initial accuracy rise, raising the level of trimming implies consuming more silicon area and using longer test times to accommodate a higher number of trim bits. Finally, this translates to incurring higher

manufacturing costs. Therefore, even though the importance of judicious layout cannot be overstated nor the effectiveness of trimming denied, quantifying process-induced errors is critical to identifying and studying the dominant culprits and, ultimately, exploring alternate strategies for obtaining high accuracy.

The basic topology of the circuit used for analyzing error sources in bandgap references is shown in Fig. 2.1. This is the building block for most bandgap reference circuits [5], [6], [8], [13]-[14], [20]-[22], [30]-[34], [38]-[39] and expressions for the error in the reference voltage of this circuit can easily be applied to most practical bandgap implementations. Referring to Fig. 2.1, the reference voltage generated by a conventional first-order bandgap reference is given by

$$V_{REF} = V_{CTAT} + V_{PTAT} = V_{BE1} + 2I_{PTAT}R_{PTAT} = V_{BE1} + 2\left(\frac{V_T \ln C}{R}\right)R_{PTAT}, \qquad (2.1)$$

and consequently,

$$\Delta V_{REF} = \Delta V_{BE1} + 2\Delta I_{PTAT}R_{PTAT}, \qquad (2.2)$$

where V_{CTAT} and V_{PTAT} are the complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) components of the reference voltage, respectively, I_{PTAT} is the PTAT current, and C is the ratio of the current densities of Q_1 and Q_2. In Eqn. (2.2) and subsequent expressions, the Δ symbol indicates a change in the variable that follows it. The factor of '2' arises since the current through R_{PTAT} is the sum of the PTAT currents flowing through Q_1 and Q_2 and this value may change from one circuit to another. The magnitude of the error in the reference voltage (ΔV_{REF}) is obtained by comparing the reference voltage of an 'ideal' bandgap reference circuit to that in which the particular error source being studied is artificially introduced. The mathematical analysis of the error sources is presented in Appendix A.

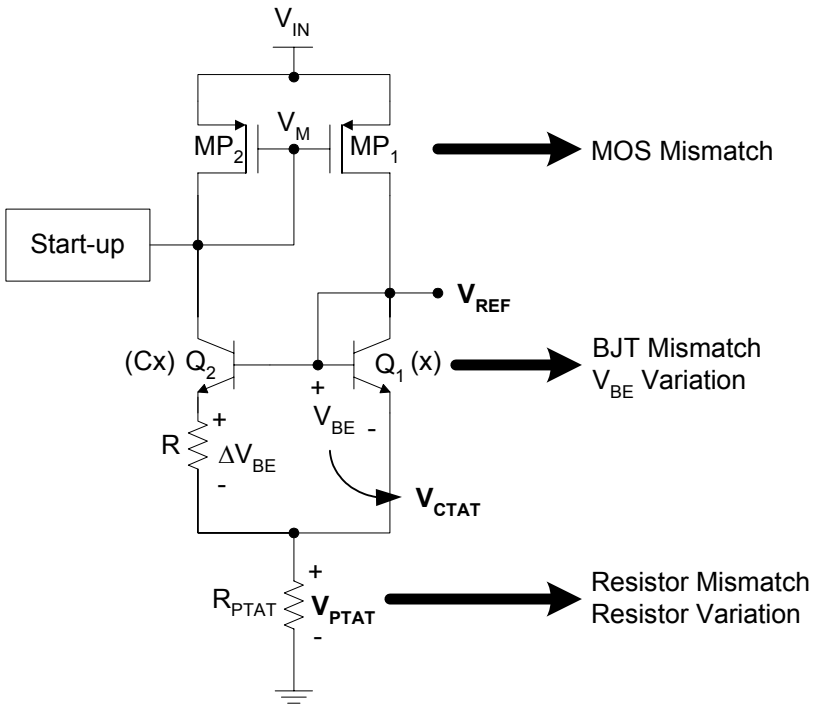


Fig. 2.1. Basic bandgap reference cell and its process-induced error sources.

2.1.1 MOS Mismatch

This error arises from a mismatch in MOS devices MP_1-MP_2 which in turn leads to a deviation in the desired ratio of the mirror currents. The mismatch may occur due to a disparity in the aspect ratio (W/L) or threshold voltage (V_{TH}) of the MOS pair. Using Eqns. (A.1)-(A.10), for a mismatch of δ_M between the mirror currents,

$$\Delta V_{REF} \approx V_T \left(\frac{R_{PTAT}}{R} \right) (2 + \ln C) \delta_M . \tag{2.3}$$

A 3-σ mismatch of 2% is not uncommon and generates an approximate error of 24mV or 2% in a 1.2V reference at room temperature. The magnitude of this error is particularly critical given that state-of-the-art references have a *total* error budget of 1%. Matching performance can be improved by increasing the active area and overdrive voltage (i.e., the difference in gate-source and threshold voltages) of the MOS devices [41] since

$$\delta_M = \frac{\Delta\frac{W}{L}}{\frac{W}{L}} - \frac{\Delta V_{TH}}{\left(\frac{V_{GS} - V_{TH}}{2}\right)} \tag{2.4}$$

and both $\Delta\frac{W}{L}$ and ΔV_{TH} are inversely proportional to the active area of the device [42]-[43].

Obtaining precisely matched MOS devices, however, is extremely challenging in the noisy, low-voltage environments characteristic of SoCs. Improving dc accuracy through increases in transistor area (for better MOS matching) incurs the penalty of higher parasitic capacitance at the mirror nodes (such as V_M in Fig. 2.1). This ultimately leads to a reduction in the reference's bandwidth which lowers its ability to respond to line and load fluctuations in noisy SoC domains and consequently degrades its ac accuracy. Moreover, shrinking supply voltages, characteristic of modern CMOS processes, are imposing stringent constraints on the maximum allowable headroom analog circuits can utilize, thereby making it difficult to generate the large overdrives critical for a high degree of matching performance. Finally, since the threshold voltage of a MOS device has non-linear temperature dependence [41], the offset δ_M also varies non-linearly with temperature, making it difficult to compensate, even through trimming. For these reasons, MOS mismatch is the most critical process-induced error source in bandgap reference circuits.

2.1.2 Resistor Mismatch

Though resistors can be matched to a high degree of accuracy (typically 1% and 0.1% through meticulous layout [43]), resistor mismatch influences the PTAT voltage, which is a strong function of the ratio of resistors R_{PTAT} and R. It can be seen from Eqn. (2.1) that a δ_R mismatch in these resistors leads to an error given by

$$\Delta V_{REF} = V_{PTAT}\,\delta_R\,. \tag{2.6}$$

Mismatch δ_R can be reduced through judicious layout. In particular, the use of dummy devices at the edges of resistor arrays can reduce mismatch due to etching errors while increasing resistor area spatially averages fluctuations in geometry. Techniques like common-centroid layout and interdigitation spatially average geometry and dopant fluctuations over resistor arrays, leading to a high degree of matching [43]. After careful layout, a 0.5% resistor mismatch generates an error of about 3mV or 0.25% for a conventional 1.2V reference.

2.1.3 Resistor Variation

Process variations lead to a large deviation in resistor values (often as large as 20%). This variation changes the V_{BE} component by altering the PTAT current flowing in the circuit. If δ_{RA} is the fractional deviation of the resistors from their nominal value, using Eqns. (A.1)-(A.3) and (A.11)-(A.12), the error in V_{REF} because of resistor variations is given by

$$\Delta V_{REF} = -V_T \delta_{RA} . \tag{2.7}$$

These errors can be reduced by choosing a material for the resistor that does not exhibit significant spread in resistivity over process, voltage, and temperature. Polysilicon resistors, for example, typically exhibit a smaller variation of resistance with voltage and temperature, than n-well resistors. While resistor variations, which occur as a result of deviations in sheet resistance from one die to another, cannot be controlled, they have a minimal impact on the accuracy of the bandgap reference – even a 20% variation generates an error of roughly 5mV, equivalent to a 0.5% error in the reference.

2.1.4 BJT Mismatch

BJT mismatch errors result from a deviation in the desired ratio of the saturation-current density J_S of transistors Q_1 and Q_2 [41]. If δ_Q is the fractional error in the ratio, the error in the reference voltage is given by

$$\Delta V_{REF} \approx \frac{V_{PTAT}}{\ln C}\delta_Q, \tag{2.8}$$

where mismatch δ_Q is given by

$$\delta_Q = \frac{\Delta I_S}{I_S}. \tag{2.9}$$

Since bipolar transistors can be matched to a high degree of accuracy (e.g. 0.1-1%), BJT mismatch has a small effect on the accuracy of the reference voltage. The error due to a mismatch of 1% is only 3mV or roughly 0.25% for a 1.2V reference.

2.1.5 V_{BE} Variation

The spread in the base-emitter voltage of the bipolar transistor used to generate the CTAT component can be a considerable source of error because it directly translates to an error in the reference voltage and is dictated entirely by the process used. For the CMOS references proposed in [20]-[23], in which circuit techniques like dynamic-element matching and auto-zeroing have been used to eliminate the effect of device mismatch, the residual error in V_{REF} of 3-10mV is primarily due to the spread in V_{BE}. This indicates that substrate PNPs available in standard CMOS technologies exhibit a lower V_{BE} variation than their high-β NPN counterparts in BiCMOS processes, which display a variation of 20-30mV. This performance advantage of substrate PNPs has been attributed to their wider base width which spatially averages dopant variations in the base. This leads to a higher degree of uniformity in base-doping and a more stable saturation-current density J_S [23].

2.1.6 Simulation Results

Table 2.1 presents a comparison of the simulated and analytical values of the error in the reference voltage at 25 ºC (the reference voltage at room temperature is 1.235V), from which a close agreement (within 4%) between the simulated and analytical values of the error in the reference voltage (ΔV_{REF}) can be seen. These results used a 2% MOS

mismatch, 1% resistor mismatch, 20% resistor tolerance, and 1% BJT mismatch. As Eqns. (2.6)-(2.8) reveal, the errors due to resistor mismatch, resistor tolerance, and transistor mismatch exhibit linear temperature dependence and Fig. 2.2, which shows a high concurrence between the simulated and analytical error in the reference voltage across the entire temperature range, corroborates this. These PTAT errors can, therefore, be eliminated by trimming resistor R_{PTAT}, which inherently cancels first-order errors because it alters the PTAT voltage to account for their effects.

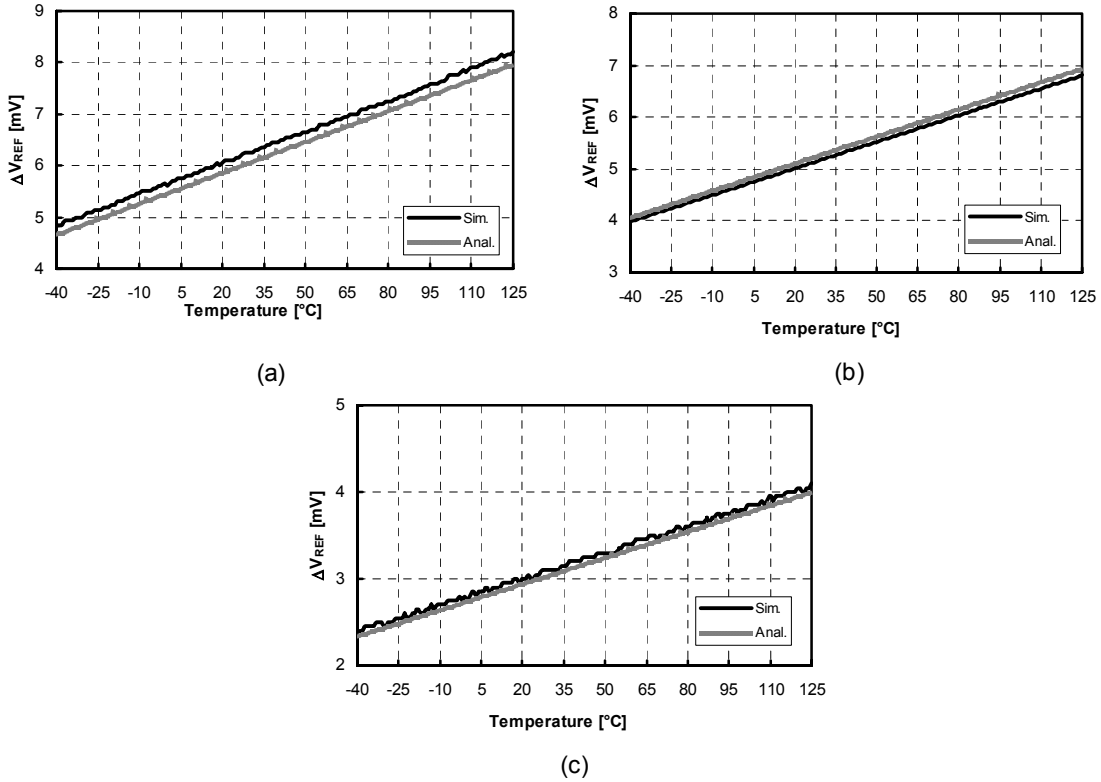


Fig. 2.2. Comparison of simulated and analytical error in the reference voltage for (a) resistor mismatch of 1%,(b) resistor tolerance of 20%, and (c) BJT mismatch of 1%.

Table 2.1. Comparison between simulation and analytical results for process-induced error sources in bandgap references (at room temperature).

Type of Error	Error in Devices	Analytical ΔV_{REF} [mV]	Simulated ΔV_{REF} [mV]	Difference
MOS Mismatch	2%	21.2	20.7	3.9 %
Resistor Mismatch	1%	5.9	5.7	3.3 %
Resistor Tolerance	20%	-5.2	5.1	0.7 %
BJT Mismatch	1%	3.0	2.9	1.6 %

2.1.6 Relative Magnitude

Table 2.2. Principle features of the various process-induced error sources in bandgap references.

Error	Typical Value (3-σ)	Relative Magnitude of Effect	Trimmable	Temperature Dependence
MOS Mismatch	±1 % - 2 %	Very Large	No	Non-linear
Resistor Mismatch	±1 %	Large	Yes	Linear
Resistor Tolerance	±20 %	Small	Yes	Linear
Transistor Mismatch	±1%	Small	Yes	Linear
V_{BE} Spread	±3-6 mV	Large	Yes	Linear

Table 2.2 presents a summary of the various process-induced sources of error in a bandgap reference circuit and their typical 3-σ magnitudes along with qualitative comparison. The 3-σ offset in the reference voltage caused by MOS current-mirror mismatch is the dominant error in a bandgap reference. This is primarily due to the high mismatch characteristic of MOS transistors (as high as 2%), which are often used to implement current-mirrors. Further, the low transconductance of the bandgap cell, that

includes an emitter-degenerated bipolar device, exacerbates the errors caused by mismatch in the collector currents by producing a large offset in the required difference of the base-emitter voltages of the core transistors. In general, MOS devices do not match as well as BJTs (~1%) and resistors (~1%) [41], [43]. Hence, MOS current-mirror mismatch, V_{BE} spread, and resistor mismatch have the largest process-induced impact on the accuracy of a bandgap reference.

2.2 Package Shift

Package shift is the deviation of the reference voltage of a packaged bandgap circuit from its original, unpackaged value. It is an important source of error since it occurs after the unit has been packaged and hence may deteriorate the accuracy of a reference that has been precision-trimmed at the wafer level (before packaging). Conventionally, package shift induced errors have been compensated primarily through post-package trimming procedures, which require an area-intensive EEPROM and associated circuitry.

Package shift is caused by stresses imposed by the package on the die surface. These mechanical stresses create parametric shifts in bipolar transistors [36]-[37], [43], MOS devices [45]-[46], and resistors [45]-[46] by altering carrier distributions and mobilities through piezo-junction and piezo-resistive effects. These shifts ultimately impact the accuracy of the reference and alter its output voltage.

2.2.1 Systematic Package Shift

The root cause of package stresses is the difference in the thermal coefficient of expansion of the die and the plastic compound in which it is encapsulated. Plastic packaging is carried out at an elevated temperature of 175°C and as the silicon and its encapsulating plastic cool, the plastic imposes increasing thermo-mechanical stresses on the die due to a difference in their rates of contraction [37]. Fig. 2.3 [37] presents

measurements on the variation of package shift with temperature over a number of samples.

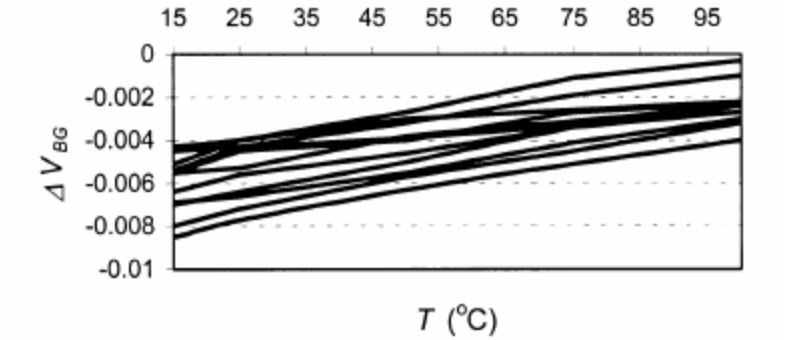


Fig. 2.3. The variation of package with temperature for various samples [37].

Since package shift is decreasing with increasing temperature for each of the samples, a strong systematic component of package shift, the magnitude of which depends on the thermal coefficient of expansion of the package and die, is evident. This systematic component can be accounted for in the design by measuring its temperature coefficient at the cost of increased design time. [36]-[37] have proposed the use of ceramic packages, which have a thermal coefficient of expansion similar to that of silicon, as another means of reducing package shift. [36] has also suggested that substrate PNP devices, commonly available in standard CMOS processes, are less sensitive to stresses than their NPN counterparts, making them a better option to implement package-shift-compensated bandgap references.

2.2.2 Random Package Shift

From Fig. 2.2 it can also be seen that package shift has a random component that varies from sample to sample. [37] proposed that this random variation arises from localized stress fields in the vertical direction imposed by filler particles in the plastic compound. Fillers are added to the plastic packaging compound to reduce its effective thermal coefficient of expansion and hence lower thermo-mechanical stresses on the die surface. These randomly distributed filler particles produce a stress that varies spatially within the die (and also from one die to the next). In particular, these highly localized

stress fields can cause a difference in the electrical characteristics of adjacent devices, leading to significant package-induced mismatch.

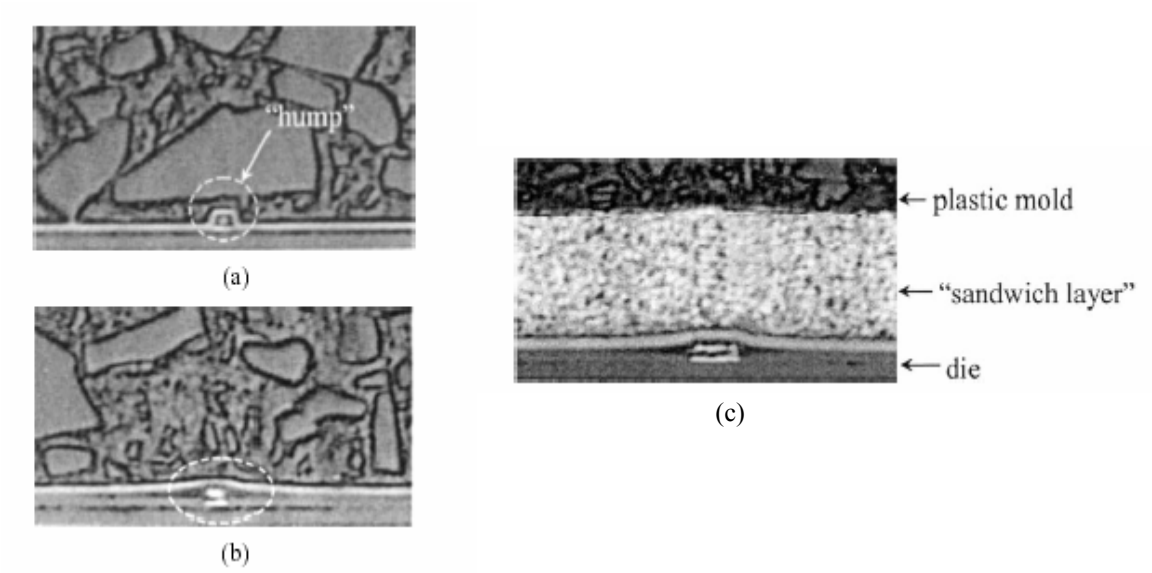


Fig. 2.4. Cross-sectional images of (a) non-planarized, (b) planarized, and (c) mechanically compliant layer dies [37].

The 3-σ magnitude of the inter-die variation shown in Fig. 2.3 is 5-7mV, as reported in [37]. [37] proposed the use of planarization and a mechanically compliant layer between the plastic package and the die as an effective means of alleviating localized stresses imposed by fillers. This mechanically compliant layer inevitably increases packaging costs and may therefore be unviable for cost-conscious SoCs. Fig. 2.4 presents cross-sections of packages, with and without planarization, and with a mechanically compliant layer inserted between the die and package.

2.3 Power-Supply Variations

Conventionally, the effects of power-supply fluctuations on the reference voltage have been suppressed by adding large external bypass capacitors at the input and output of a discrete bandgap reference IC [48]-[51]. As systems undergo higher levels of integration, however, external components increase the bill-of-materials (BoM) and thereby directly impact cost. Simultaneously, higher integration has resulted in the

fabrication of switching digital circuits, which are inherent noise sources, in close proximity to critical analog blocks. The high frequency noise generated by digital circuits can easily couple onto supply lines through crosstalk and subsequently degrade the ac accuracy of a noise-sensitive bandgap reference. Studying the ability of a reference to suppress supply noise across a wide spectrum of frequencies is therefore crucial for a designer to devise economically viable yet effective techniques to improve its Power-Supply Ripple-Rejection or PSRR performance.

A number of analog circuits, including operational amplifiers [2], [41], linear regulators [1], [24], [29], [39], and bandgap references [6], [31], [38], employ shunt feedback to regulate their output voltage. As shown in Fig. 2.5, the output in these circuits is typically sampled by an amplifier that uses the error in the feedback voltage and desired voltage to drive the gate (or base) of a MOS (or bipolar) transistor M_o. M_o sources (or sinks) an appropriate current into (or from) the impedance at the output to maintain a steady voltage in the presence a varying power-supply. The feedback loop is characterized by gain $A_{ol}\beta$ and is comprised of the error amplifier, which exhibits an output resistance $R_{o\text{-}A}$ and corresponding pole $p_{o\text{-}A}$ ($f_{p\text{-}oA} \equiv 1/2\pi R_{o\text{-}A}C_{o\text{-}A}$), and M_o, which has a drain-source resistance r_{ds} and an output pole determined by the output capacitor C_o (which may have a parasitic equivalent series resistance or ESR).

It has been shown that the PSRR of these closed-loop systems is intimately related to the open-loop parameters of their feedback loop [1]-[2], [31], [52]-[55]. While the analytical expressions derived in [2], [31], [52]-[54] provide a designer with good estimates for PSRR performance, they do little to provide him/her with an intuitive understanding of how the open-loop response of these circuits influences their ability to reject noise from the power-supply. An intuitive and insightful model for analyzing PSRR is presented in Fig. 2.6 [55]. While the model is valid for any circuit that employs shunt feedback to regulate its output, it shall be discussed here in the context of a regulated bandgap reference.

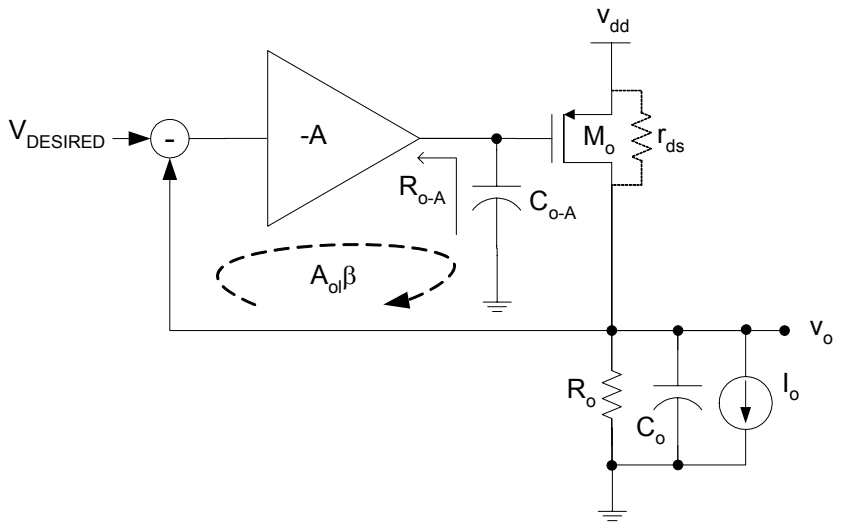


Fig. 2.5. Block diagram of system using shunt feedback to regulate output voltage.

In its simplest form, the PSRR transfer function (a ratio of the output to the supply ripple) can be viewed as the effect of a voltage divider caused by an impedance between the supply and the output and an impedance between the output and ground. Using this approach, the model consists of an impedance ladder comprising of the channel resistance of output device M_o (r_{ds}) and a parallel combination of the open-loop output resistance to ground (z_o) and the shunting effect of the feedback loop ($z_{o\text{-}ref}$). Hence, referring to Fig. 2.5 and Fig. 2.6, we can see that

$$z_o = (z_{Co} + R_{ESR}) \| R_o , \tag{2.10}$$

and,

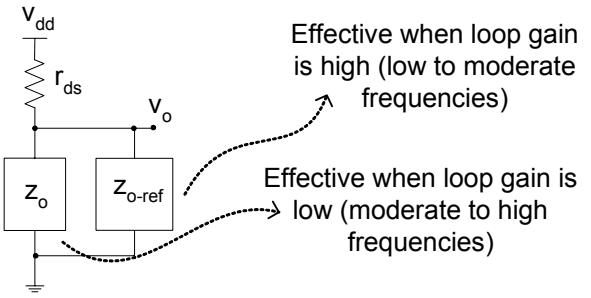
$$z_{o-ref} = \frac{z_o \| r_{ds}}{A_{ol}\beta} . \tag{2.11}$$

The error in the reference voltage due to supply voltage changes, in other words, the PSRR performance of the reference, is hence given by

$$\text{PSRR} = \left.\frac{v_o}{v_{dd}}\right|_f = \left.\frac{\delta V_{REF}}{\delta V_{DD}}\right|_f = \frac{(z_o \| z_{o-ref})}{r_{ds} + (z_o \| z_{o-ref})} . \tag{2.12}$$

Fig. 2.7 depicts the sketch of a typical PSRR curve and how the intuitive model is used to determine the PSRR performance of a regulated reference over a large range of

frequencies, simply by accounting for the frequency dependence of z_o and $z_{o\text{-}ref}$.



$$PSRR = \left.\frac{v_o}{v_{dd}}\right|_f = \left.\frac{\delta V_{REF}}{\delta V_{DD}}\right|_f = \frac{(z_o \,||\, z_{o-ref})}{r_{ds} + (z_o \,||\, z_{o-ref})}$$

$$z_o = (z_{Cout} + R_{ESR}) \,||\, R_o$$

$$z_{o-reg} = \frac{z_o \,||\, r_{ds}}{A_{ol}\beta}$$

Fig. 2.6. Intuitive impedance divider model for PSRR.

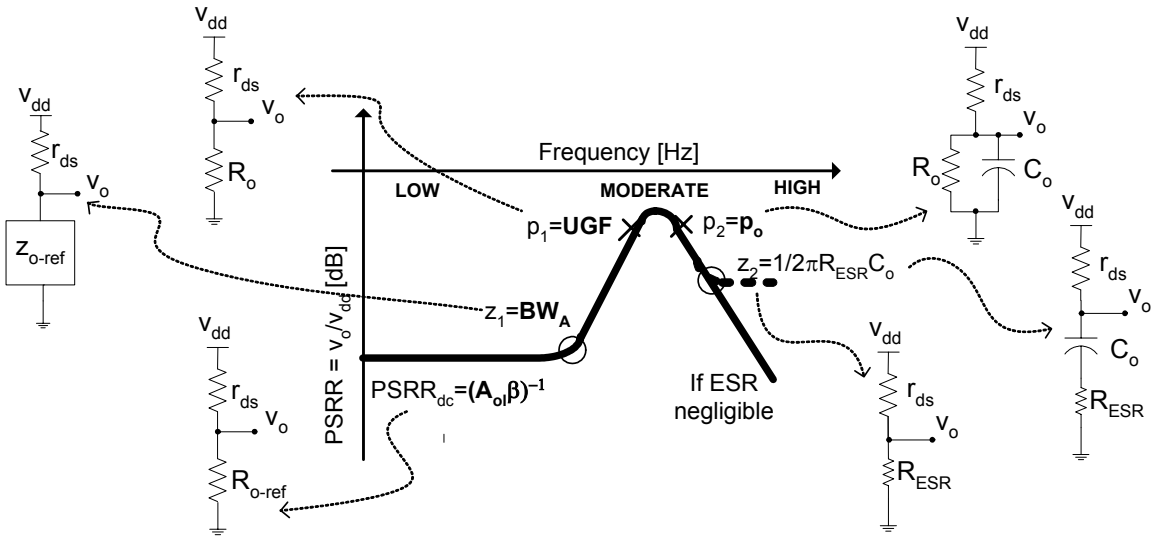


Fig. 2.7. Simple model in action over a wide frequency range.

2.3.1 DC and Low Frequencies

At low frequencies, high loop gain ($A_{ol\text{-}dc}\beta$) allows $z_{o\text{-}ref}$ to shunt z_o, and since r_{ds} is, for the most part, significantly lower than R_o, the following simplification can be derived:

$$\mathrm{PSRR_{dc}} \approx \frac{R_{o-ref}}{r_{ds} + R_{o-ref}} = \frac{\dfrac{r_{ds} \,||\, R_o}{A_{ol-dc}\beta}}{r_{ds} + \dfrac{r_{ds} \,||\, R_o}{A_{ol-dc}\beta}} \approx \frac{\dfrac{r_{ds}}{A_{ol-dc}\beta}}{r_{ds} + \dfrac{r_{ds}}{A_{ol-dc}\beta}} \approx \frac{1}{A_{ol-dc}\beta}. \qquad (2.13)$$

Consequently, the PSRR of the reference is intimately related to the open-loop gain of the system.

2.3.2 Moderate Frequencies

The shunting effect of the feedback loop deteriorates at frequencies beyond the bandwidth of the amplifier, BW_A (or dominant pole $p_{o\text{-}A}$), thereby causing an increase in the regulated output impedance $z_{o\text{-}ref}$. This leads to a rise in the output ripple and, consequently, the dominant PSRR breakpoint in the form of a PSRR zero (z_1). The resultant degradation in PSRR can be obtained by replacing $A_{ol\text{-}dc}$ in Eqn. (2.13) with the bandwidth-limited response of the loop at frequencies where $A_{ol\text{-}dc}$ is greater than one, i.e., between dc and the unity-gain frequency (UGF) of the system. This leads to

$$\mathrm{PSRR}|_{f \le UGF} \approx \frac{z_{o-ref}}{r_{ds} + z_{o-ref}} = \frac{r_{ds}}{(A_{ol}\beta)\, r_{ds} + r_{ds}} = \frac{r_{ds}}{\dfrac{A_{ol-dc}}{1 + \dfrac{s}{p_{o-A}}}\beta\, r_{ds} + r_{ds}}$$

$$= \frac{1 + \dfrac{s}{p_{o-A}}}{(1 + A_{ol-dc}\beta)\left[1 + \dfrac{s}{(1 + A_{ol-dc}\beta)\, p_{o-A}}\right]} \approx \frac{1 + \dfrac{s}{BW_A}}{(A_{ol-dc}\beta)\left(1 + \dfrac{s}{UGF}\right)}. \qquad (2.14)$$

The presence of a PSRR pole (p_1) at the unity-gain frequency, as predicted by Eqn. (2.14), can be easily understood when we note that the deterioration of PSRR due to increasing closed-loop output resistance ceases at the UGF. At this stage, the shunting effect of the feedback loop no longer exists and PSRR performance is determined simply by the frequency-independent resistive divider between the channel resistance r_{ds} of the output device and resistor R_o. The PSRR is now given by

$$\text{PSRR}|_{f=UGF} \approx \frac{z_o}{z_o + r_{ds}} = \frac{R_o}{R_o + r_{ds}} \approx 1. \tag{2.15}$$

At these frequencies, the PSRR of the reference is the weakest since the closed-loop output resistance is not decreased by the feedback loop and output capacitor C_o cannot shunt the output ripple to ground because its impedance is still high.

2.3.3 High Frequencies

When the output capacitor starts shunting R_o to ground, a smaller ripple appears at the output, thereby causing an improvement in PSRR performance (since z_o decreases with increasing frequency) and the second PSRR pole (p_2). Thus,

$$\text{PSRR}|_{f>UGF} \approx \frac{z_o}{z_o + r_{ds}} = \frac{z_{Co}}{z_{Co} + r_{ds}}. \tag{2.16}$$

The effectiveness of the output capacitor is, however, restricted by its ESR. At higher frequencies, since this capacitor is an "ac short", z_o is determined by the ESR, which limits PSRR to

$$\text{PSRR}|_{f>>UGF} \approx \frac{z_o}{z_o + r_{ds}} \approx \frac{R_{ESR}}{R_{ESR} + r_{ds}}, \tag{2.17}$$

thereby leading to an effective PSRR zero at $z_2 = 1/2\pi R_{ESR}C_o$.

2.4 Load Variations

Though regulated references do not typically source load currents in excess of 10mA, they need to exhibit low output impedance to shunt high frequency noise that propagates onto their output via parasitic coupling capacitance – these noise sources can effectively source and sink 100μA to 1mA into the output impedance of a bandgap reference during transient events, as shown in Fig. 2.8. It is crucial, therefore, for the reference to exhibit low output impedance over a wide frequency range to shunt noise currents to ground effectively and thereby minimize errors in the output voltage. The ability of a reference to withstand load variations is thus determined by its output

impedance or

$$z_{o-ref} = \left.\frac{v_o}{i_o}\right|_f = \frac{\delta V_{REF}}{\delta I_{LOAD}} = \frac{R_o \,||\, r_{ds}}{A_{ol}\beta}. \tag{2.18}$$

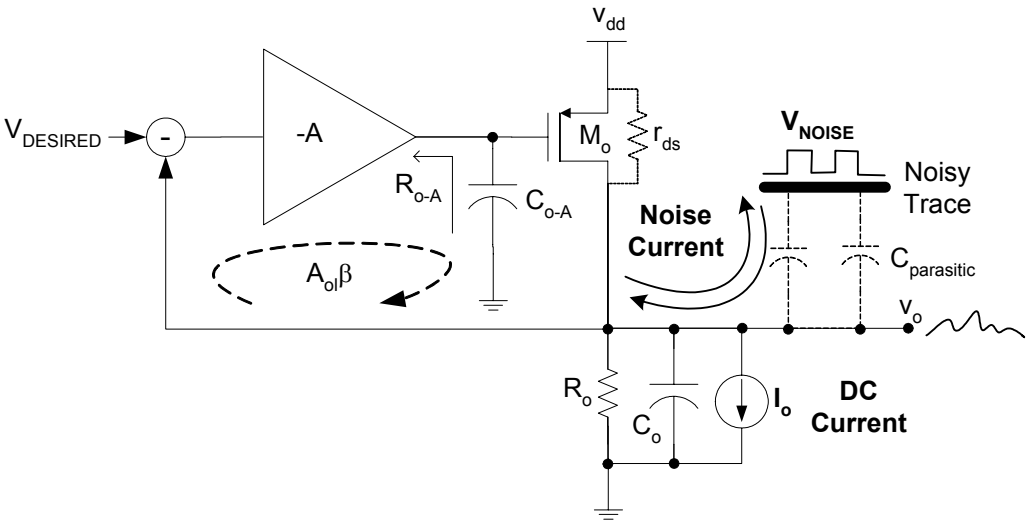


Fig. 2.8. Effect of load variations on a reference.

From Fig. 2.8, the output impedance of a regulated reference at low frequencies is given by

$$R_{o-ref} = \frac{R_o \,||\, r_{ds}}{A_{ol-dc}\beta}. \tag{2.19}$$

The magnitude of this impedance rises dramatically at frequencies beyond the bandwidth of the amplifier (BW_A) when loop gain falls, weakening the ability of the reference to shunt noise. The output impedance of the reference at these frequencies is given by

$$z_{o-ref}\big|_{f\le UGF} = \frac{R_o||r_{ds}}{\dfrac{A_{ol-dc}}{1+\dfrac{s}{p_{o-A}}}\beta} = \frac{R_o||r_{ds}\left(1+\dfrac{s}{p_{o-A}}\right)}{A_{ol-dc}\beta}. \tag{2.20}$$

Since the feedback loop is ineffective at the unity-gain frequency (UGF), the output impedance is the highest at this frequency and is approximately

$$z_{o-ref}\big|_{f=UGF} \approx R_o||r_{ds}. \tag{2.21}$$

Once the output capacitor starts shunting the output noise to ground, the output impedance of the reference is dominated by the output capacitor and

$$z_{o-ref}\Big|_{f\geq UGF} = z_{Co}\,. \tag{2.22}$$

A reference is thus most vulnerable to load variations at frequencies close to its unity-gain frequency, when the loop gain cannot suppress variations at the output via feedback and when the output capacitor cannot shunt these variations to ground since its impedance is still high.

2.5 Temperature Variations

A forward biased base-emitter junction of a bipolar transistor has a temperature dependence given by [6]

$$V_{BE}(T) = \left[V_{go} + (\eta - x)V_{Tr}\right] - \left[\frac{V_{go} - V_{BE}(T_r) + (\eta - x)V_{Tr}}{T_r}\right]T$$
$$- \left\{\frac{(\eta - x)V_{Tr}}{T_r}\left[T\ln\left(\frac{T}{T_r}\right) - T + T_r\right]\right\}, \tag{2.23}$$

where V_{go} is the bandgap voltage of silicon, η is a process dependent constant with an approximately value between 3.6 and 4, x is the order of temperature dependence of the collector current, and V_{Tr} is the thermal voltage at room temperature. The logarithmic term can be expanded to yield higher-order temperature dependence terms. The order of a reference is determined by the highest order of temperature dependence of V_{BE} that is compensated. In other words, a first-order bandgap reference compensates only linear or first-order temperature dependence (using a PTAT voltage), a second-order bandgap reference compensates linear and second-order temperature dependence (using a PTAT and $PTAT^2$) voltage, and so on.

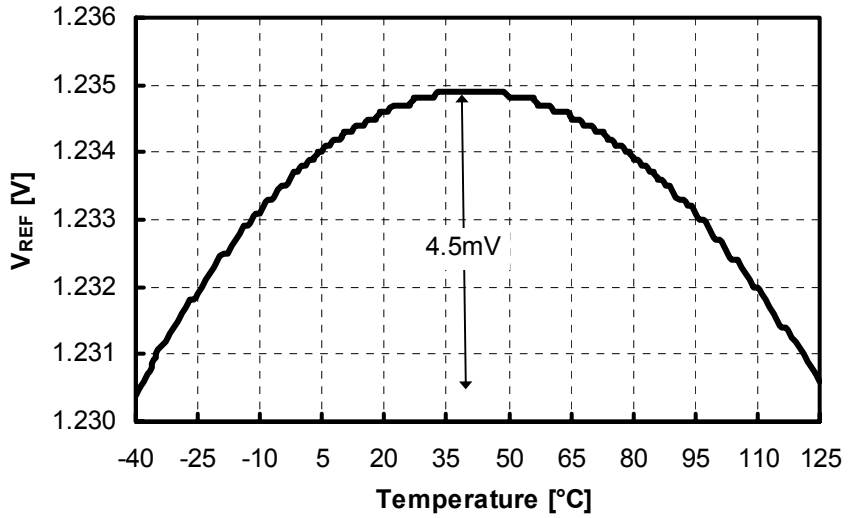


Fig. 2.9. Temperature variation of first-order bandgap reference.

For a first-order reference, the non-linear terms contribute a residual error of roughly 3 to 5mV (on the conventional reference voltage of 1.2V) after the linear CTAT temperature dependence of V_{BE} has been "cancelled out" by the PTAT ΔV_{BE} voltage. This systematic error is considerably smaller than random errors induced by process variations and mismatch, which can cumulatively be as high as 25mV. The use of second- and higher-order references that minimize temperature-induced errors may only be justified, therefore, after the errors due to process variations have been addressed. Fig. 2.9 presents the simulated output voltage of a conventional first-order reference showing the residual errors caused by the non-linear components of V_{BE}.

2.6 Summary of Error Sources

The foregoing analysis has shown that the errors in a bandgap reference may only be static or dc in nature (mismatch, package shift, and temperature) or have an additional transient or ac component (power-supply and load variations). Moreover, these effects may be systematic (power-supply, load, and temperature variations), random (process-induced mismatch), or a combination of both (package shift). Finally, errors due to process and power-supply variations are relatively larger than those because of package

shift, which were empirically observed to be small, and load variations, since bandgap references typically source relatively low currents. These errors were much larger than those due to temperature variations because the systematic curvature in V_{BE} generates an error of only a few millivolts in the bandgap reference. Table 2.3 qualitatively summarizes the diverse nature of these various error sources.

Table 2.3. Summary of various error sources in bandgap references.

Error Source	DC	AC	Random	Systematic	Relative Impact
Process Variations	Yes	No	Yes	No	Very Large
Package Shift	Yes	No	Yes	Yes	Large
Power-Supply Variations	Yes	Yes	No	Yes	Very Large
Load Variations	Yes	Yes	No	Yes	Large
Temperature Variations	Yes	No	No	Yes	Small

2.7 Synopsis

Studying the various sources of error that degrade the accuracy of bandgap references is crucial to understanding their diverse characteristics with the ultimate goal of devising novel strategies to suppress their detrimental effects. MOS mismatch is the most serious process-induced error as precise matching in MOS devices is difficult to achieve under noisy, low-voltage conditions. Moreover, the resultant error in the reference voltage cannot be trimmed because of its non-linear temperature dependence. Package shift is an important source of error as it can only be compensated via post-package trimming, which is expensive and complex. The effects of line variations on the accuracy of the reference are frequency dependent, as are those due to load variations. Both are intimately related to the open-loop parameters of the reference and are most significant at frequencies near the unity-gain frequency of the feedback loop. The effect of temperature variations is relatively small, even in first-order references, and needs to be compensated only after the larger sources of error have been addressed.

CHAPTER 3

TRIMLESS ACCURACY

Random process-induced variations and mismatch can degrade the accuracy of the most well-designed bandgap reference. While trimming offers an effective solution to mitigate these errors, it incurs significant increases in manufacturing costs. In this chapter, the merits and drawbacks of trimming are first presented after which dynamic-element matching (DEM) is discussed. DEM alleviates the effects of process- and package-induced mismatch without increasing manufacturing costs, but simultaneously raises noise levels and degrades system bandwidth. Self-calibration techniques are presented next, after which the Survivor strategy, a self-calibration technique that mitigates the deleterious effects of mismatch without increasing manufacturing costs, introducing noise, or hampering bandwidth, is introduced. The concept of the Survivor strategy is presented, followed by its circuit- and system-level design. Finally, measurement results on a prototype IC are evaluated and analyzed.

3.1 Trimming

Trimming is a post-fabrication circuit adjustment aimed at correcting errors in the reference voltage caused by process- and package-induced variations. Typically, one or more strategically placed resistors are tuned to offset the mismatch of two or more devices. Considering the classical CMOS topology shown in Fig. 3.1, the high gain of operational amplifier OA_1 equalizes the voltages at its input through feedback, thereby generating a PTAT voltage (which is the difference in the emitter-base voltages of Q_1 and Q_2) across resistor R. The resultant PTAT current is mirrored in MP_1-MP_2 and produces a PTAT voltage across R_{PTAT} which, when added to CTAT V_{EB1}, generates a reference voltage V_{REF} given by

$$V_{REF} = V_{CTAT} + V_{PTAT} = V_{EBl} + I_{PTAT} R_{PTAT} = V_{EBl} + V_T \ln C\left(\frac{R_{PTAT}}{R}\right), \qquad (3.1)$$

In this topology, resistor R_{PTAT} is varied to alter the PTAT component of the reference voltage V_{PTAT} and thereby offset any errors induced by process variations or package shifts.

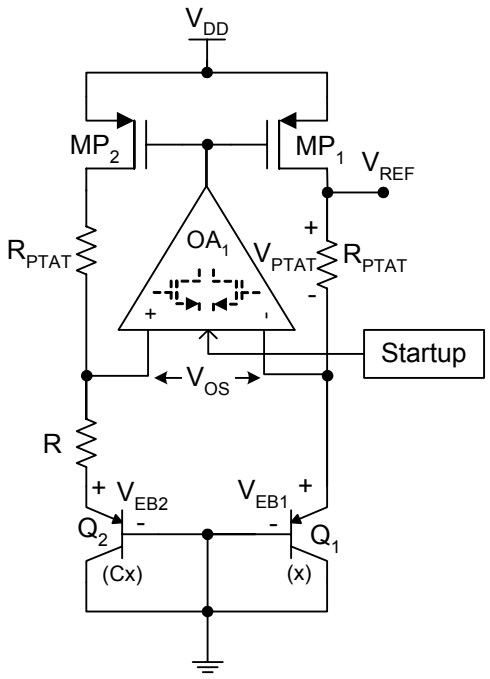


Fig. 3.1. Conventional CMOS bandgap reference.

The resistor R_{PAT} could be varied by: (1) using a digital string of 1s and 0s (a trim code) that control on-chip switches to open- and/or short-circuit a number of binarily-weighted resistors or (2) reshaping and therefore resizing the resistor with a laser [6]. The accuracy of the former is limited by the smallest value by which the reference voltage can be changed; this value, in turn, is determined by the resistance that corresponds to the least significant bit (LSB) of the trim code. Unfortunately, since the untrimmed initial accuracy of the reference that sets the full-scale trim-range resistance is often 3-5%, reducing the LSB resistance to obtain higher resolution typically translates to employing a higher number of trim bits which are always constrained by silicon area and test-time boundaries. Laser trimming [6], on the other hand, is more accurate and area efficient and

therefore often used in high performance data converter applications, but its inherent cost in test time and equipment is oftentimes prohibitive.

The reason why trimming is so attractive is that many process-induced errors, like those due to resistor and BJT mismatch and spread, have an almost linear temperature dependence and consequently trimming at one temperature, for instance, room temperature, is sufficient to cancel the drift of the offset over the entire temperature range [6], [35]. Its cost in manufacturing time, however, can account for 25% of the total cost of a power management IC [56], and this is only to correct first-order errors, i.e., errors that have a linear temperature coefficient. The temperature dependence of higher order errors present in bandgap circuits, such as the mismatch of MOS devices, are not compensated – only their absolute offsets at the trimming temperature (e.g., room temperature) are reduced. In Fig. 3.1, for instance, mismatch in MP_1-MP_2 and the offset of OA_1, which is conventionally designed using MOS devices [6], [8], [13]-[15], [20]-[23], [31], are particularly critical sources of error that cannot be trimmed. Even if trimming is performed at the wafer level for each die, package shift errors require further EEPROM-based post-package trimming, compounding manufacturing costs. Package shift offset effects can be reduced by adding post-fabrication low-stress mechanically compliant layers to the IC before encapsulating it with plastic [1], [37], but again, adding these compounds is costly.

3.2 Switching Solutions

Given that trimming may be unviable for many cost-conscious applications, dynamic-element matching (DEM) offers a circuit designer the capability to mitigate process- and package-shift-induced mismatch errors without increasing manufacturing cost. DEM is similar to the chopping strategy that has been used to improve the input-referred offset of operational amplifiers [23], [57]-[58]. In DEM, devices are matched by periodically interchanging their positions and therefore, on average, duplicating the same

offset in all positions.

An example of DEM as applied to a current-mirror, a critical building block of most bandgap references [5], [6], [8], [13]-[14], [20]-[22], [30]-[34], [38]-[39] is shown in Fig. 3.2. If mirror devices MP_1-MP_2 were perfectly matched, the voltage V_{REF} across the load resistor would simply be $I_{REF}R_{REF}$. However, any mismatch between the two mirror devices generates an offset current and, consequently, an error in the output voltage. DEM overcomes this offset by periodically interchanging the roles of MP_1 and MP_2 through a switching network, i.e., MP_1 is the diode-connected input device for the mirror for one half-cycle and MP_2 performs this role in the other half. Since the output then has equal and opposite errors ($\pm\Delta V_{REF}$) about the desired reference over time, the average is free of mismatch offset effects.

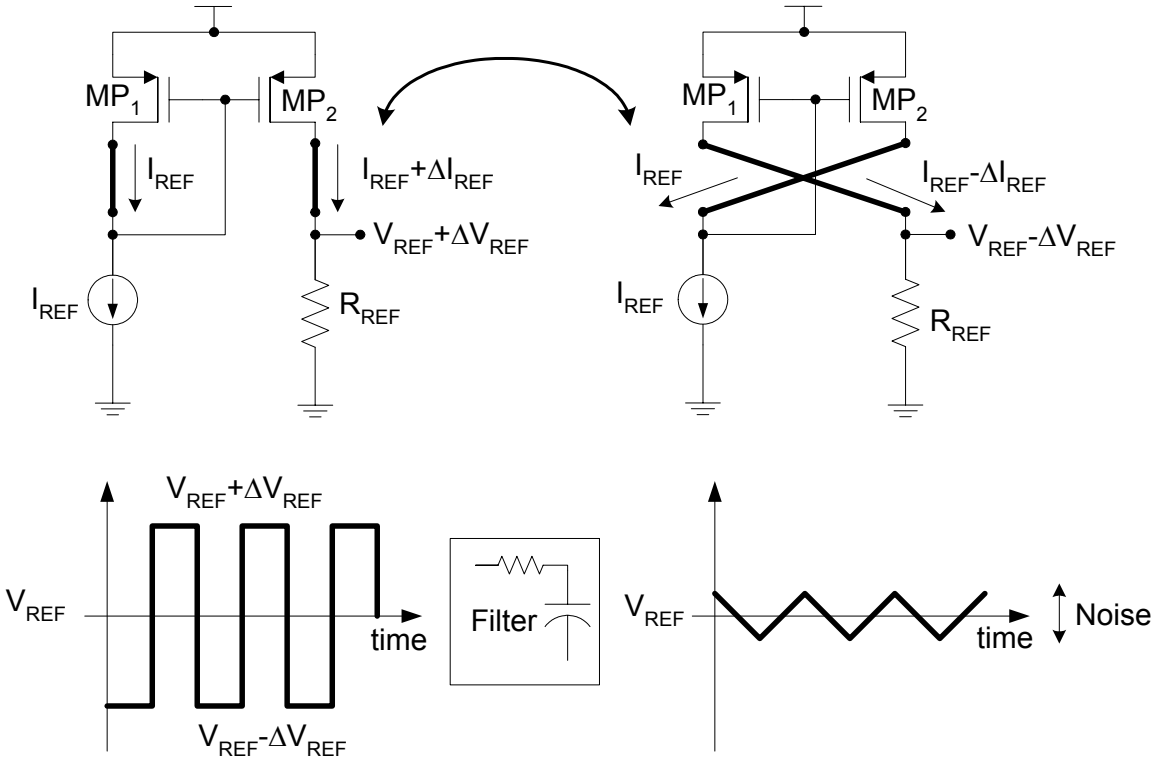


Fig. 3.2. Use of dynamic-element matching (DEM) to reduce mismatch offset errors.

Referring to Fig. 3.2, the real-time output of the mirror is a superposition of the ideal dc reference voltage and the equal and opposite values of the offset voltage. This

peak-to-peak switching variation ($2\Delta V_{REF}$) is suppressed with a low pass filter. Since the switching frequency of DEM is normally low (1-10KHz) to minimize clock feed-through and charge-sharing effects, a low roll-off frequency filter and therefore a large capacitor is required. For a System-on-Chip (SoC) solution, however, establishing a low-frequency filter pole to suppress switching noise is always difficult given the limited on-chip capacitance available. Needless to say, without a large capacitor, the output has a noisy square wave superimposed onto the desired reference, degrading its precision and that of the entire system it supports. Even if a large capacitor *is* placed at the output to damp DEM noise, it degrades system bandwidth and thereby increases the transient response time of the system.

With regards to bandgap references, switching solutions have been primarily used to improve the accuracy of CMOS implementations, such as the one shown in Fig. 3.1. The accuracy of CMOS topologies is hampered by MOS mismatch that generates a large offset having non-linear temperature dependence. In addition to mismatch in the mirror devices MP_1-MP_2, an input-referred offset V_{OS} in the operational amplifier OA_1, which typically has a MOS differential pair input, leads to a large error in the reference voltage since

$$V'_{REF} = V_{EB1} + \left(\frac{\Delta V_{EB} + V_{OS}}{R} \right) R_{PTAT} = V_{EB1} + \frac{R_{PTAT}}{R} V_T \ln(C) + \frac{R_{PTAT}}{R} V_{OS} \quad (3.2)$$

and therefore

$$\Delta V_{REF} = \frac{R_{PTAT}}{R} V_{OS}. \quad (3.3)$$

Since the ratio of resistor R_{PTAT} to R is roughly 10 for a conventional 1.2V reference, even a 1mV input-offset is amplified to an error of roughly 10mV in the output voltage. [20] has reduced the offset of OA_1 using autozeroing, while [22] has used DEM. [21], [23] have extended the use of DEM to devices MP_1-MP_2 and resistors R and R_{PTAT}.

3.3 Self-Calibration Schemes

Instead of relying on costly trimming during the manufacturing phase, a number of systems have used on-chip circuitry for self-calibration during start-up or power-on-reset events. In other words, these systems tweak their components at start-up using internal signals (as opposed to off-chip trim codes) till they achieve desired performance and subsequently resume normal operation. [60] tuned an on-chip inductor for optimal RF matching while [61] tuned a MOS device to achieve an accurate current-mirror. [62] used redundancy to overcome the detrimental effects of process-induced mismatch on the linearity performance of an analog-to-digital converter (ADC) – a bank of comparators was fabricated on-chip from which a subset that generated the maximum linearity performance for the ADC was selected at start-up (the unselected comparators were therefore *redundant*).

A general block diagram for such self-calibrating systems is presented in Fig. 3.3. A switch network activates the critical component that needs to be tuned (an inductor in [60], a MOS device in [61], and a comparator in [62]). The system performance in this configuration is then measured accurately and compared to an ideal or desired value using on-chip circuitry (e.g. instrumentation amplifiers and/or comparators). A digital engine (that may consist of simple logic gates or a complex DSP) then processes the result of this measurement. Based on the error between the system's current performance and the ideal value, the digital engine actuates the appropriate switches in the network to modify the component being tuned (the value of the inductor in the case of [60], the aspect ratio of the MOS device in [61], and the offset of a comparator in [62]), before the next measurement is taken. The ultimate goal of this self-calibration procedure is to tune the critical component such that the error between the system's actual performance and the desired value is minimized.

Needless to say, the most critical block of these self-calibration strategies is the measurement block since its precision determines the ability of the system to converge to

the desired performance. The precision of the measurement block, in turn, depends on the accuracy of the "ideal" reference against which it gauges the performance of the system under test. In almost all self-calibration strategies reported [60]-[62] the accuracy of this reference is either directly or indirectly proportional to the accuracy of a voltage reference. In [60], the voltage reference is used to measure the peak voltage generated by a low-noise amplifier that uses the inductor being tuned while [61] uses it to measure the offset voltage of an amplifier that uses the current-mirror being calibrated. [62] needs a precision voltage reference for implementing a digital-to-analog converter (DAC) whose output signals are used as the input to the ADC being calibrated for maximal linearity.

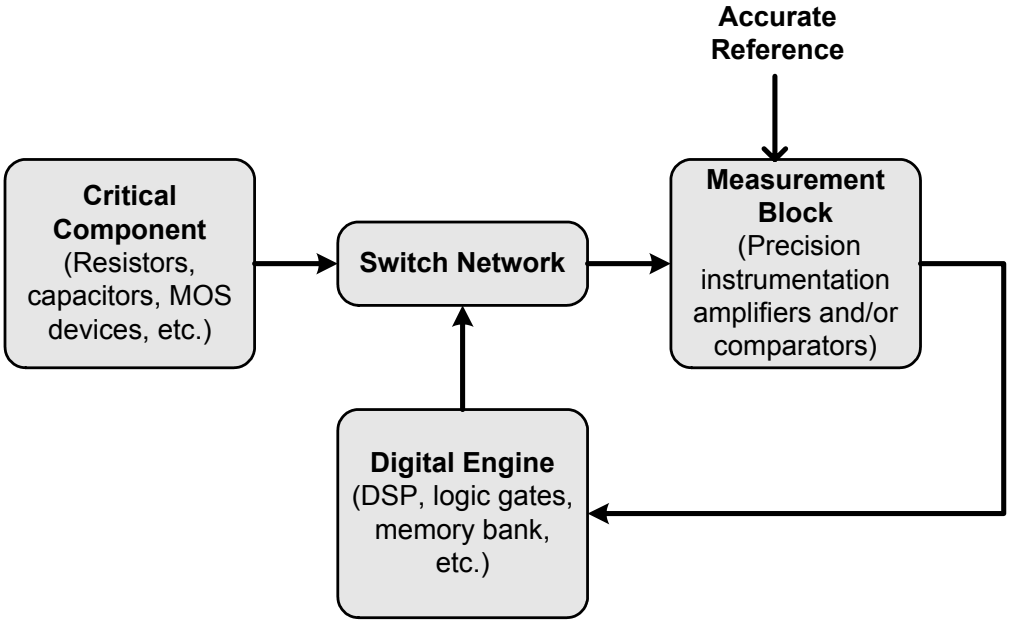


Fig. 3.3. Block diagram of self-calibration strategies.

However, as discussed in Chapter 2, the accuracy of voltage references in general, and bandgap references in particular, is inherently sensitive to variations in process, voltage, temperature, supply, and loading conditions. This makes it difficult to for these self-calibrated systems to converge reliably without the aid of an external, precision-trimmed voltage reference. The Survivor strategy, presented next, uses redundancy to provide a bandgap reference with the ability to self-calibrate, thereby completely exempting these dependent self-calibrating systems from trimming.

3.4 Survivor Strategy

3.4.1 Concept

The heart of the Survivor strategy lies in identifying the best matching pair of devices from a bank of similar transistor pairs during start-up and/or power-on-reset (PoR) events [59]. The best pair is then used to implement a critical pair in a circuit (e.g. a bandgap reference) when the system resumes normal operation. This self-calibration approach is similar in philosophy to [60]-[62], except its implementation does not require an accurate reference, complex DAC, large memory bank, or area-intensive sample/hold capacitors.

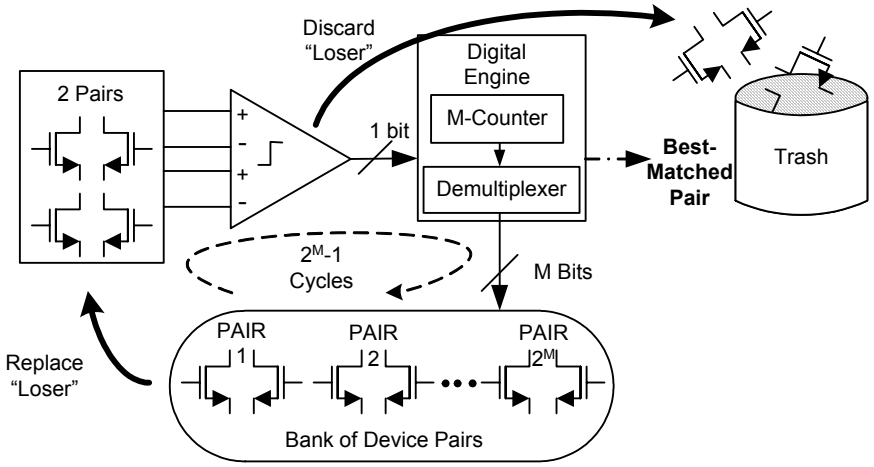


Fig. 3.4. Block diagram of the Survivor strategy.

The block diagram of the Survivor strategy is presented in Fig. 3.4. A bank of pairs, each of which is assigned a unique digital code, is fabricated on-chip. Every time the system starts up or resets, a digital engine connects two pairs from this bank to a high resolution current comparator via a set of switches. The comparator then determines which of the two connected pairs has higher offset (worse mismatch). The digital engine processes the output of the comparator to discard the pair with the higher offset (the *loser*) and connects another pair from the bank in its place. This new pair is then

compared to the *winner* from the previous cycle, and so on. After processing all pairs in the bank, the winner of the last cycle (the *survivor*) is the pair with the least mismatch.

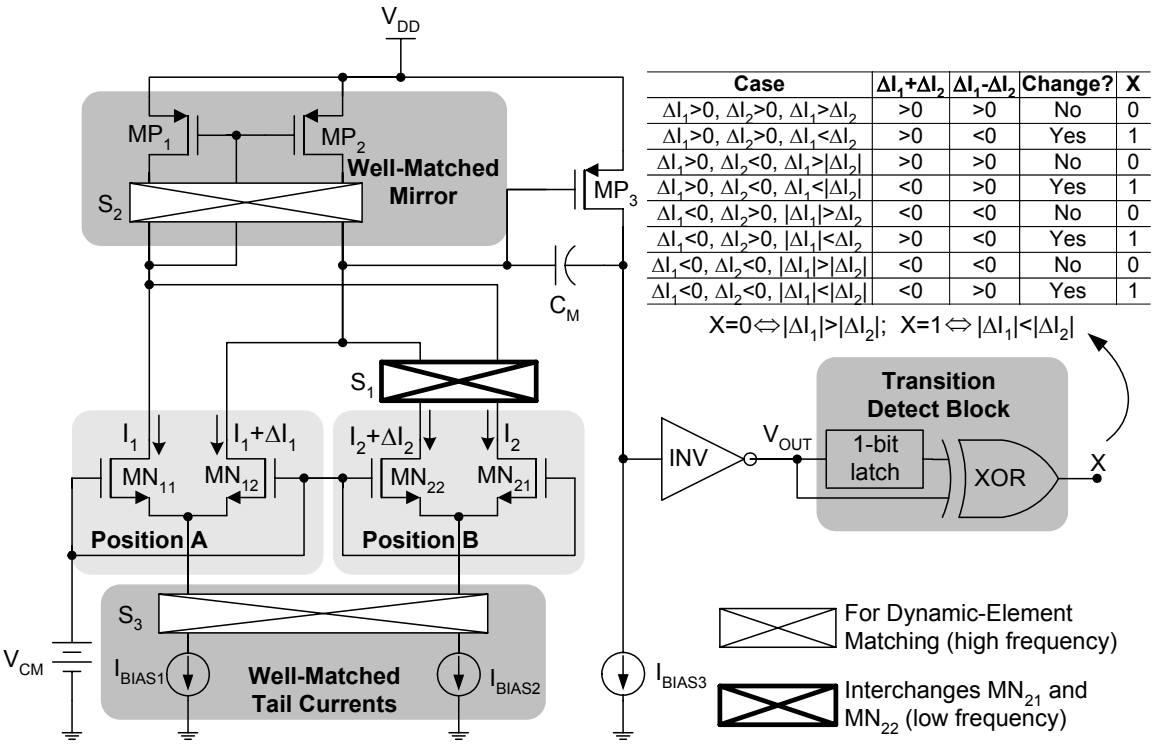
3.4.2 Circuit Design

Comparator

The most important component of the Survivor scheme is the comparator because its resolution determines the matching performance of the winner of every cycle and ultimately the surviving pair. The comparator, shown in Fig. 3.5, is a variation of the differential difference amplifier discussed in [63] and is comprised of accurate current-mirror MP_1-MP_2, well-matched current sources I_{BIAS1}-I_{BIAS2}- I_{BIAS3}, gain stages MP_3 and inverter INV, and a transition-detect block. The two pairs of devices to be tested are first placed in Positions A and B and fed to accurate current-mirror MP_1-MP_2. The offsets of these two pairs (ΔI_1 and ΔI_2) determine the state of inverter INV (i.e., V_{OUT} is low if MN_{12} and MN_{22}, when connected together, conduct more current than their respective counterparts). In the second phase, the connectivity of one of the pairs is reversed, and a resulting state change implies the offset of this reversed pair is dominant ($|\Delta I_2| > |\Delta I_1|$); otherwise, no state change occurs. This state-reversal result is then used to select which pair to discard, and to allow the next pair to take a position, after which point another pair can be processed.

The resolution of this circuit is key and is dependent on the matching performance of the bias currents and devices MP_1-MP_2-MP_3. The overall input-referred offset resulting from a current density mismatch in MP_3, which is dependent on how well MP_3 matches MP_1-MP_2 and I_{BIAS3} matches I_{BIAS1}-I_{BIAS2}, is minimal because it is divided by MP_3's transconductance and the voltage gain of the first stage, which is on the order of 30-40 dB [41]. Offsets in mirror devices MP_1-MP_2 and I_{BIAS1}-I_{BIAS2}, however, are virtually unattenuated when referred to the input, which is why DEM is used for both sets of

devices. DEM nearly eliminates their mismatch effects by exposing the offset to both sides of the mirror (MP_1-MP_2) and both pairs (I_{BIAS1}-I_{BIAS2}) equally. This is achieved by exchanging the connectivity of MP_1-MP_2 and I_{BIAS1}-I_{BIAS2} several times, with every clock cycle, and therefore, over time, *averaging* their overall effects to zero. This averaging (low pass filter) function is performed by capacitor C_M, whose Miller effect enhances its filtering capabilities [58].



Case	$\Delta I_1+\Delta I_2$	$\Delta I_1-\Delta I_2$	Change?	X
$\Delta I_1>0, \Delta I_2>0, \Delta I_1>\Delta I_2$	>0	>0	No	0
$\Delta I_1>0, \Delta I_2>0, \Delta I_1<\Delta I_2$	>0	<0	Yes	1
$\Delta I_1>0, \Delta I_2<0, \Delta I_1>\lvert\Delta I_2\rvert$	>0	>0	No	0
$\Delta I_1>0, \Delta I_2<0, \Delta I_1<\lvert\Delta I_2\rvert$	<0	>0	Yes	1
$\Delta I_1<0, \Delta I_2>0, \lvert\Delta I_1\rvert>\Delta I_2$	<0	<0	No	0
$\Delta I_1<0, \Delta I_2>0, \lvert\Delta I_1\rvert<\Delta I_2$	>0	<0	Yes	1
$\Delta I_1<0, \Delta I_2<0, \lvert\Delta I_1\rvert>\lvert\Delta I_2\rvert$	<0	<0	No	0
$\Delta I_1<0, \Delta I_2<0, \lvert\Delta I_1\rvert<\lvert\Delta I_2\rvert$	<0	>0	Yes	1

$X=0 \Leftrightarrow |\Delta I_1|>|\Delta I_2|$; $X=1 \Leftrightarrow |\Delta I_1|<|\Delta I_2|$

Fig. 3.5. Schematic of comparator and sample switching sequence.

As mentioned earlier, DEM trades off noise performance for system bandwidth. In this case, a large filter capacitance, on one hand, shunts the switching noise generated by DEM, but on the other, increases the comparator's propagation delay, that is, the processing time for each comparison and consequently the system's overall start-up time. As a result, the DEM frequency should be high, but not enough to degrade the matching accuracy of the mirror and the comparator with charge injection and clock feed-through [58]. In simulations, the proposed comparator displayed a worst-case resolution and settling time of 300μV and 200μs with a 25kHz DEM frequency and 20pF filter

capacitor. Since the system is in start-up or reset mode when DEM is engaged, however, the disadvantages associated with DEM (switching noise and low bandwidth) have no effect on system performance, when the best-matched pair (i.e., survivor) is already selected and the comparator is off.

The transition-detect block detects a change of state in the comparator's output by storing the result of the first phase comparison in a 1-bit latch, before the onset of the second phase. The result of the second phase is then compared with that of the first via the XOR gate. If the two states differ, the output of the gate is high, which is the code for a state reversal.

Digital Engine

The block diagram of the Survivor system is presented in Fig. 3.6. For simplicity, the switching network used to implement DEM is omitted and only 4 pairs of devices are used in the bank. Each comparison cycle consists of four phases synchronized by a clock-driven shift register. In the first phase, the output of the comparator is stored in latch D-LTCH1. On the falling edge of this phase, switch network S_1 interchanges the terminals of the pair at Position B, as shown in Fig. 3.5. The new output of the comparator, produced during this second phase, is compared with the contents of the latch via the XOR gate, as described in the comparator section.

In the third phase, the output of the XOR gate is sampled by latch D-LTCH2, which drives demultiplexer DEMUX. DEMUX is fed by an M-bit counter (CTR), whose output corresponds to one among the 2^M pairs in the bank. As a result, when CTR toggles on the falling edge, the new code corresponding to the next sequential pair in the bank is routed through DEMUX to either active-high decoder DEC_A or DEC_B (which control the switch network of Positions A and B) in the fourth phase to replace the code corresponding to the loser, leaving the winner code intact. During start-up, the phase generator is initialized to Phase 4, CTR is set to the code of the second pair, and D-

LTCH2 is set to 1 (to allow the counter to drive one of the decoders), which place the first two pairs in the bank to Positions A and B. Since the counter sequentially and monotonically increments its output up, and its result connects a pair to one of the two positions, there is no chance that a pair will ever be connected to both positions.

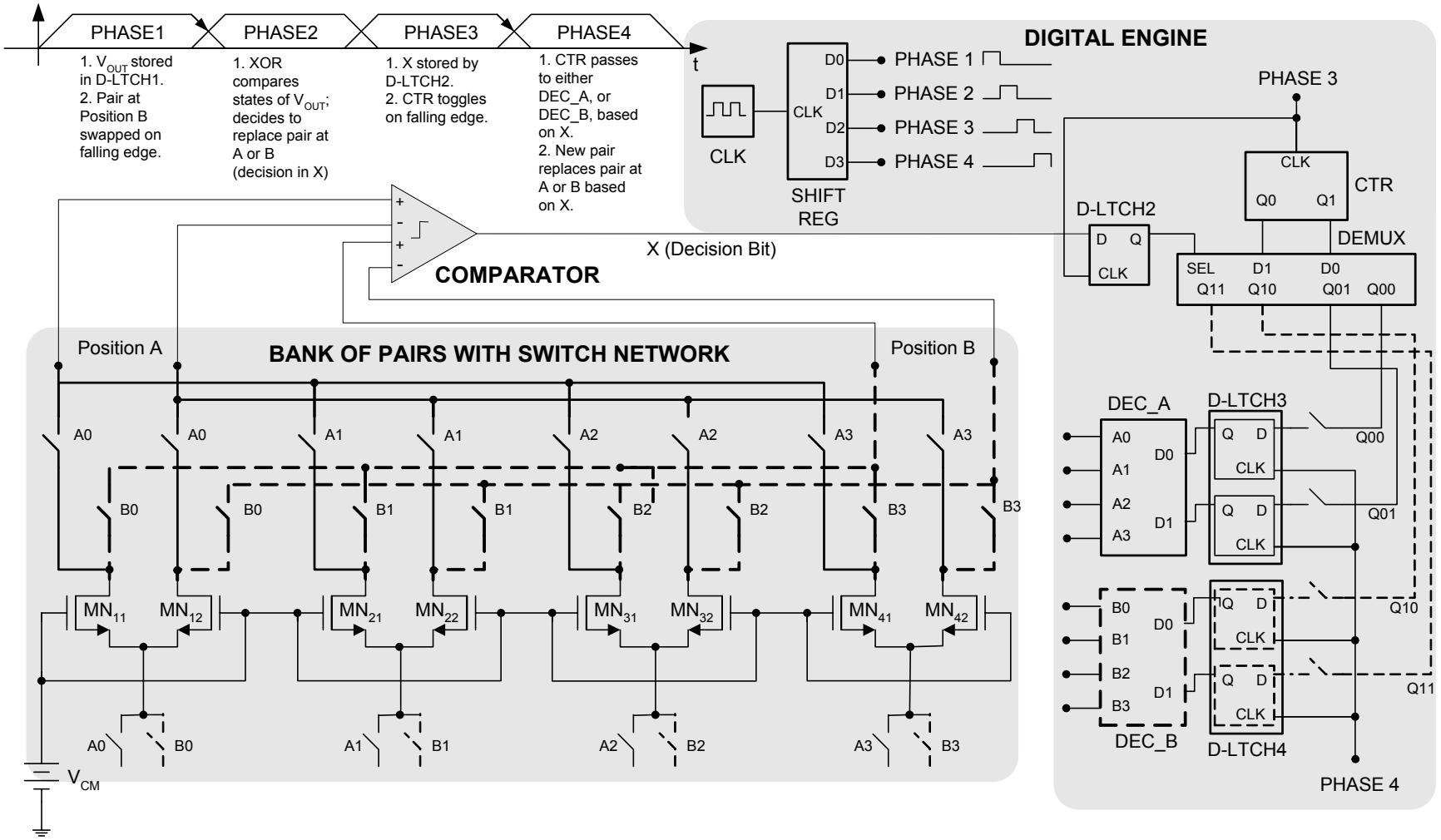


Fig. 3.6. System diagram of the Survivor strategy.

3.4.3 Simulation Results

The system shown in Fig. 3.6 was simulated using BSIM3 models of AMI's 0.6μm CMOS process for transistors and switches and AHDL macromodels for digital blocks, and the bank of devices consisted of eight pairs. An artificial input-referred offset was added to each pair, as shown in Table 3.1. Going down the list on Table 3.1 sequentially, the Survivor strategy should (and the simulation results of Fig. 3.7, which show the binary code corresponding to the winner of each cycle corroborate this) retain the lower offset pair, i.e., Pairs 0, 2, 3, and finally 5, which has the lowest offset.

Table 3.1. Offsets in bank of device pairs.

Pair	Code	Offset [mV]	Pair	Code	Offset [mV]
0	000	3.1	4	100	-2.6
1	001	4.2	5	101	-1.0
2	010	2.3	6	110	1.5
3	011	-1.5	7	111	2.8

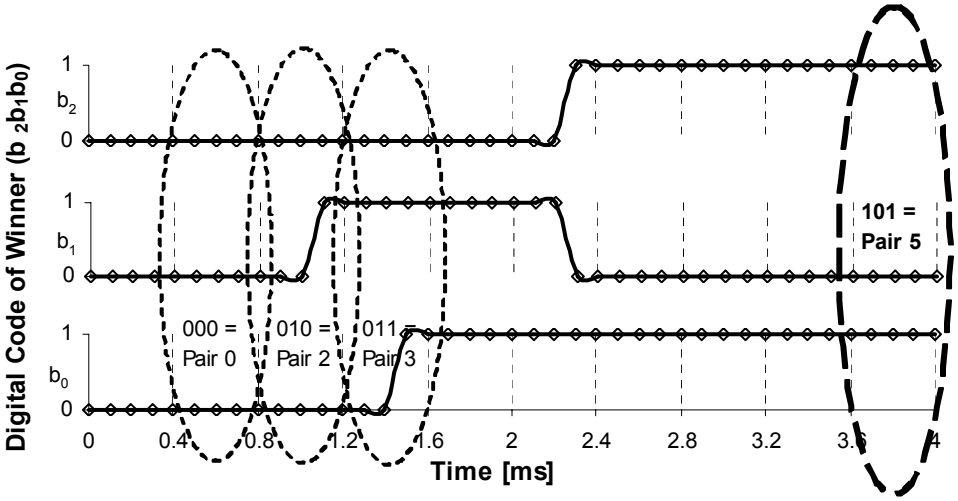


Fig. 3.7. Simulation results showing the digital code of the winner of each cycle with convergence to Pair 101 (Pair 5).

3.4.4 Measurement Results

Mirrors are widely popular analog building blocks that are used in almost all comparators, amplifiers, and bandgap references. Their matching performance improves with increasing device areas but this increase inherently results in a degradation of system bandwidth due to higher parasitic capacitance. As shown in Chapter 2, bandgap references are particularly sensitive to mirror mismatch, especially if the mirrors are constructed using MOS devices. For these reasons, a MOS mirror was used as a vehicle for gauging the potential of the Survivor strategy as an alternative to trimming and DEM.

In particular, the effectiveness of the Survivor strategy in improving the 3-σ matching performance of a MOS mirror constructed of devices having minimum-channel length (0.6μm) and a width-to-length (W/L) ratio of 10 was measured and evaluated through a prototype IC fabricated with AMI's 0.6μm-CMOS process. The die photograph of the IC is shown in Fig. 3.8. The comparator, bank of device pairs, switching network, and decoders were on-chip. The bank of device pairs consisted of 32 NMOS pairs having a W/L ratio of 6μm/0.6μm.

Referring to Fig. 3.6, the functions of the counter CTR, which generates the digital code corresponding to the next pair in the sequence, and demultiplexer DEMUX, which routes this code to decoders DEC_A or DEC_B based on the comparator's output, were carried out manually for ease of testability. Along with these decoders, a third decoder DEC_M was fabricated to connect the survivor pair, once determined, in a current-mirror configuration through another switching network to measure the offset performance of the survivor. Finally, mirrors using devices having the same W/L ratio (10) as the candidate pairs but 3×, 5×, 8×, and 10× the channel length (i.e., dimensions of 18μm/1.8μm, 30μm/3.0μm, 48μm/4.8μm, and 60μm/6.0μm) were also fabricated on the IC to gauge the bandwidth advantage of the surviving small-geometry mirror. The experiments were performed on 30 samples to increase their statistical validity.

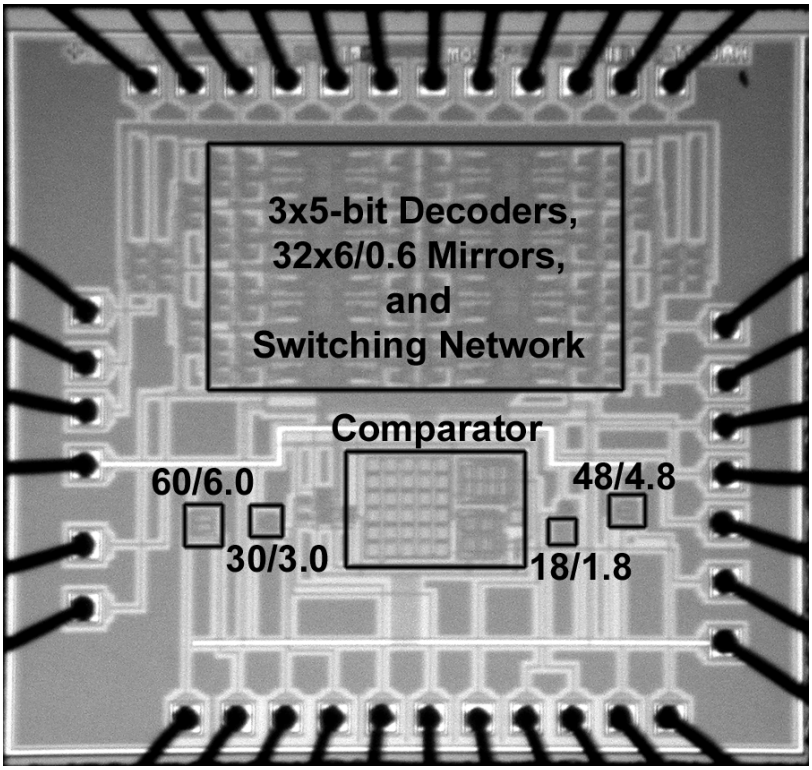


Fig. 3.8. Die photograph of prototype of Survivor strategy.

Test Setup and Procedure

In the test setup shown in Fig. 3.9, the switching frequency of clock CLK1 for DEM was set to 25kHz and CLK2 for swapping the terminals of the pair at Position B to 5kHz. The inputs of DEC_A and DEC_B were set with external Single Pole Double-Throw (SPDT) switches and the output of the comparator was then monitored with an oscilloscope. If the output toggled with CLK2 (if the pair at Position B has higher offset), DEC_B was reprogrammed with the code of the next pair in the sequence. If the output remained unchanged (the pair at Position A has a higher offset), DEC_A was reprogrammed with the code of the next pair. This procedure was repeated until the last digital code was reached (Pair 32: 11111). The winner of this last comparison is the Survivor.

DEC_A and DEC_B were then disabled and the survivor code was programmed into the inputs of DEC_M, which connected this pair in a current-mirror configuration.

The offset of this current-mirror was determined by using a semiconductor parameter analyzer, forcing a known current of 15μA to the input of the current-mirror, and measuring its output current to extract the offset (mismatch) of the pair. The drain-source voltages of the current-mirror pair were equalized to eliminate the effects of channel-length modulation on offset. Finally, DEC_M was disabled and the offsets of the four large geometry mirrors were measured.

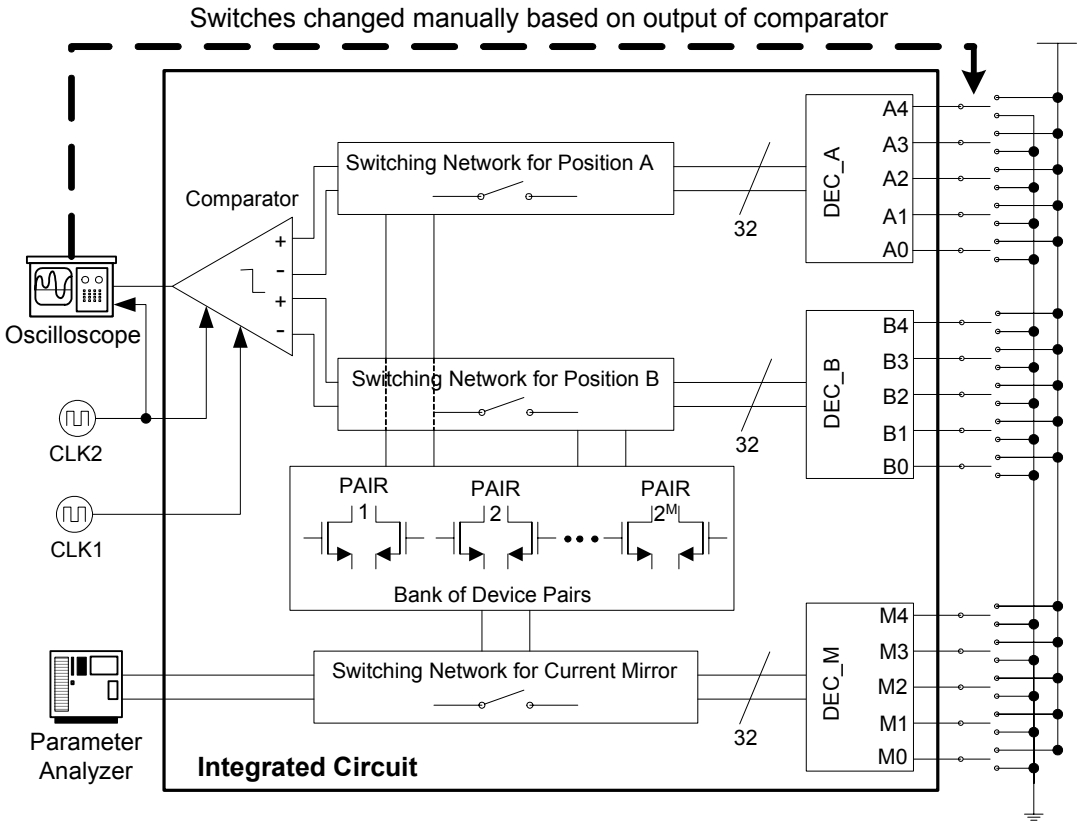


Fig. 3.9. Experimental test setup for prototype.

Experimental Results

To verify if the Survivor strategy was indeed converging on the pair with the best matching performance, the offsets of the pairs in the banks of 5 samples were measured by connecting each of them in a current-mirror configuration. The experimental offset measurements of one such sample are presented in Table 3.2, showing Pair 19 as the best matching pair. Fig. 3.10 shows how the experimental code progression of the Survivor

strategy converges on Pair 19, the survivor. When measured over 30 samples for this technology, the 3-σ offset performance of a minimum channel-length pair was 22.2% whereas the survivor was 1.9% (Fig. 3.11), roughly an order of magnitude improvement.

Table 3. 2. Measured offsets of current-mirror pairs in a sample IC.

Pair	Offset [%]	Pair	Offset [%]	Pair	Offset [%]	Pair	Offset [%]
0	13.2	8	2.6	16	9.7	24	5.1
1	6.7	9	10.3	17	6.8	25	8.3
2	2.9	10	17.6	18	8.1	26	15.9
3	0.8	11	7.1	19	0.2	27	5.5
4	3.8	12	1.9	20	8.1	28	1.8
5	4.1	13	0.5	21	4.0	29	9.9
6	4.7	14	1.5	22	16.0	30	4.3
7	5.8	15	4.3	23	2.0	31	7.3

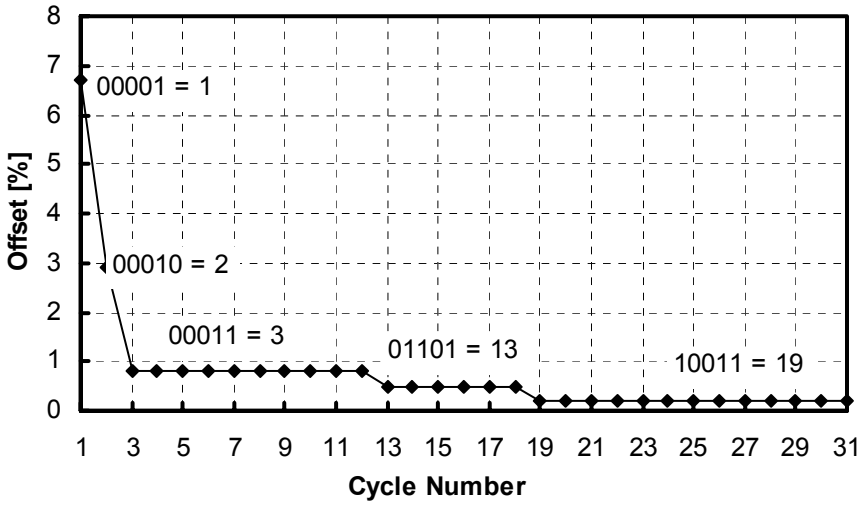


Fig. 3.10. Experimental code and offset progression of the IC with the current-mirror devices depicted in Table 6.2.

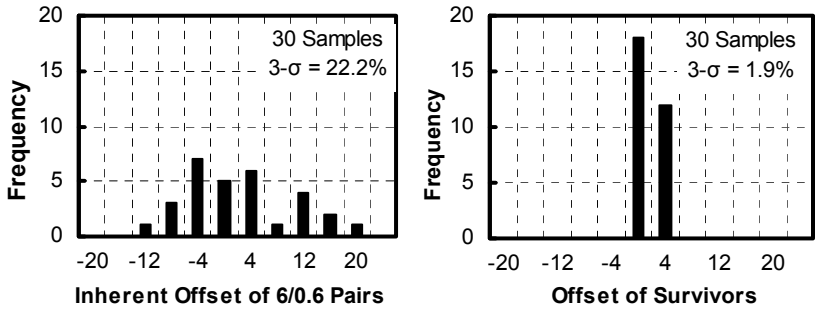


Fig. 3.11. Statistical experimental offset performance of a single (6/0.6) pair and the (6/0.6) survivor out of 32 pairs.

Fig. 3.12 illustrates how the statistical matching performance relates to the number of devices placed in the bank and how a single but larger device compares (3-σ range for a 95% confidence interval is also shown, which can be decreased by increasing the number of samples). The results show that the survivor of 32 (6/0.6) pairs displays the matching performance of a (48/4.8) pair while retaining the speed of a (6/0.6) pair, which amounts to a 64× bandwidth improvement (in the 95% confidence range, the survivor performance at worst and at best is 5× and 10× the device size). Decreasing the geometry of one device from (60/6.0) to (6/0.6) degrades its matching performance from 1.72% to 22.23% (Table 3.3).

From Fig. 3.12, it can also be seen that decreasing the number of pairs in the bank from 32 to 1 degrades the matching performance of the survivor from 1.94% to 22.23%. For example, the survivor of 4 devices outperforms a single device by a factor of nearly 4× while the survivor of 32 outperforms a single device by roughly 11×. The number of pairs required to achieve an offset specification depends on the inherent offset of the individual pairs, as derived in the following section.

The number of pairs in the bank is ultimately limited by die-area limits and start-up time, which increase with the number of device pairs to be compared before the system starts up. The cost of silicon real estate in today's driving CMOS technologies, however, tends to be less than that of trimming test time, especially if post-package

trimming is adopted to mitigate the adverse effects of package shift on matching. In the 0.6µm CMOS prototype built, the bank of 32 pairs, the three 5-bit decoders, and the switching network occupied 0.78mm^2 and the overall scanning time, which is the time required to converge to the surviving pair, would be 24.8ms (31 comparisons at 800µsec per comparison with a 5kHz 4-phase shift-register clock frequency). While this delay has a significant impact on systems and sub-systems that start in less than 15-100ms (e.g., hard disk-drives and various power supplies), it incurs minimal overhead on portable devices like cellular phones and MP3 players, which take seconds to start.

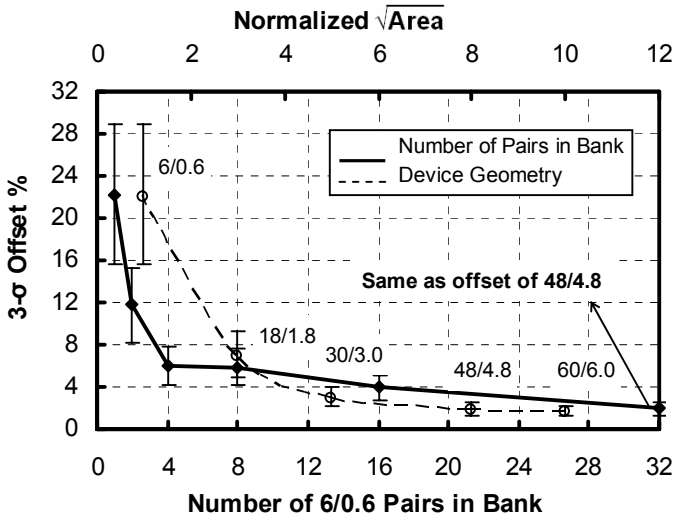


Fig. 3.12. Statistical experimental offset performance of the Survivor scheme and a series of single but larger geometry pairs (95% confidence interval).

Table 3.3. Experimental offset performance of a single device pair with various width-to-length dimensions.

W/L [µm/µm]	6/0.6	18/1.8	30/3.0	48/4.8	60/6.0
Normalized Area	1	9	25	64	100
3-σ Offset [%]	22.23	7.09	3.14	1.91	1.73
3-σ Offset of Survivor [%]	1.94				

3.4.5 Discussion

Number of Pairs Required in Bank

If n, R, and r denote the number of device pairs in the bank of a sample, the 3-σ offset of these n pairs, and the desired 3-σ offset of the survivor pairs of N samples, the probability a pair within a sample has an offset lower than or equal to r is

$$p = \varphi\left(\frac{r}{R}\right) = \frac{1}{2}\,\mathrm{erf}\left(\frac{1}{\sqrt{2}}\frac{r}{R}\right), \tag{3.4}$$

where φ( ) represents the normal distribution function. As a result, the probability that *none* of the n devices within a sample has the required offset is $(1\text{-}p)^n$. If the probability of finding *at least one pair* from each sample within the desired resolution range is P, then

$$P = 1-(1-p)^n \Rightarrow n = \frac{\log(1-P)}{\log(1-p)}. \tag{3.5}$$

Table 3.4. Minimum number of devices required to obtain a given mismatch performance.

r/ R	p	Minimum number of devices required	
		P = 0.9	P = 0.99
0.4	0.3108	7	14
0.2	0.1586	14	27
0.1	0.0793	27	56
0.05	0.0396	56	113

Table 3.4 presents the minimum number of devices required for possible values of r/R, highlighting the values that were chosen for this implementation. For the prototype, P was 0.9 (i.e., the chance of finding at least one pair within the required resolution in each sample was 9 out of 10) and r/R was set to 0.1 (i.e., the desired offset was 10 times lower than the inherent offset of the devices). The probability of finding one pair of

devices with the targeted offset can be set higher when more die area for device pairs and start-up time are allowed.

Effects of Common-Mode Voltage

In the mirror configuration, the bulk and source terminals of the NMOS pairs are at the same potential (V_{SS}) and bulk-effect induced offsets are therefore non-existent. This, however, is not the case, when substrate NMOS pairs are used as differential input pairs, like in Fig. 3.5, where the body of the device is connected to substrate and the source is not. The result is body effect, which not only introduces an additional parasitic transconductance to the device (g_{mb}) but also adds another mismatch component to the threshold voltage by means of a mismatch in the bulk-effect parameter, which unfortunately increases with source-bulk voltages:

$$V_T = V_{T0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right), \tag{3.6}$$

thus

$$\partial V_T|_{body-effect} = \partial\gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right), \tag{3.7}$$

where γ and Φ_F are the bulk effect factor and bulk potential respectively and are given by

$$\gamma = \frac{\sqrt{2q\,\varepsilon_{Si}\,N_A}}{C_{ox}} \tag{3.8}$$

and

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right). \tag{3.9}$$

In Eqn. (3.7), mismatch in bulk potential Φ_F is neglected since its sensitivity to dopant fluctuations is much lower than that of the body factor γ. This can be seen by

$$\left.\frac{\partial\gamma}{\gamma}\right|_{N_A} = \frac{1}{2}\left(\frac{\partial N_A}{N_A}\right) >> \left.\frac{\partial\phi_F}{\phi_F}\right|_{N_A} = \frac{1}{\ln(N_A/n_i)}\left(\frac{\partial N_A}{N_A}\right). \tag{3.10}$$

Fig. 3.13 shows the measured degradation in the 3-σ matching performance of the survivor with increasing source-bulk voltages for common-mode voltages (V_{CM}) above 1.4V. Below 1.4V, V_{CM} pushed the tail current sinks into the linear region, after which

point the gain and resolution of the comparator are affected. In any event, decreasing the source-bulk voltage of a device decreases the mismatch effects of the bulk-effect parameter on offset performance. In other words, for critical devices, it is best to short-circuit the bulk-source terminals, and if the device is a substrate device, it is best to use it as a current-mirror (e.g., PMOS transistors immersed in their own n-wells outperform substrate NMOS devices in a differential input pair configuration, but not necessarily in a current-mirror).

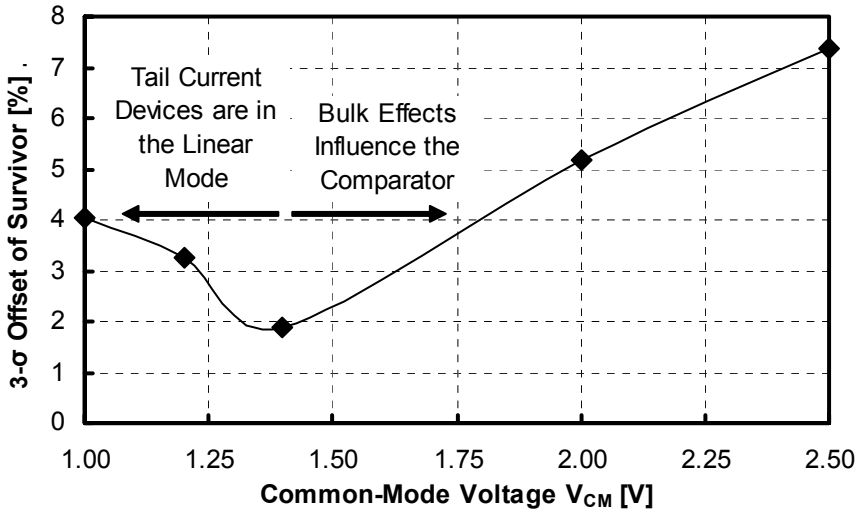


Fig. 3.13. Experimental offset performance of the survivor as a function of input common-mode voltage (i.e., in the presence of bulk effects).

3.4.6 An Improved Comparator

The resolution of the comparator described in Fig. 3.5 suffered from bulk effects that arose because the source and bulk terminals of the candidate NMOS pairs were at different potentials. Fig. 3.14 presents an improved comparator topology in which this disadvantage has been eliminated by tying the source and bulk terminals of the candidate NMOS pairs to ground (PMOS pairs will be tied to the power-supply rail). The improved comparator is comprised of four gain stages, including common-source transistor MN_{31} and inverter INV, and a transition-detect block. Each of the four devices in the two candidate pairs is biased to sink a PTAT current of 8μA which flows into R_{11} and R_{12} to

establish the common-mode signal at the output of the first stage and input of the second – in this case, this common-mode signal is approximately 1.4V below the supply rail (16μA from MN_{11}-MN_{13} and MN_{12}-MN_{14} flows in 90K resistors R_{11} and R_{12}, respectively).

As described in Section 3.4.2, the two pairs of devices to be tested are first placed in positions A and B. The offsets of these two pairs (ΔI_1 and ΔI_2) determine the state of inverter INV (i.e., V_{OUT} is high if MN_{12} and MN_{14}, when connected together, conduct more current than their respective counterparts). In the second phase, the connectivity of the pair at position B is reversed and a resulting state change implies the offset of this reversed pair is dominant ($|\Delta I_2| > |\Delta I_1|$); otherwise, no state change occurs. This state-reversal result is then used (via an XOR function) to select which pair to discard and to allow the next pair to take the position of the discarded pair, after which point another comparison is processed.

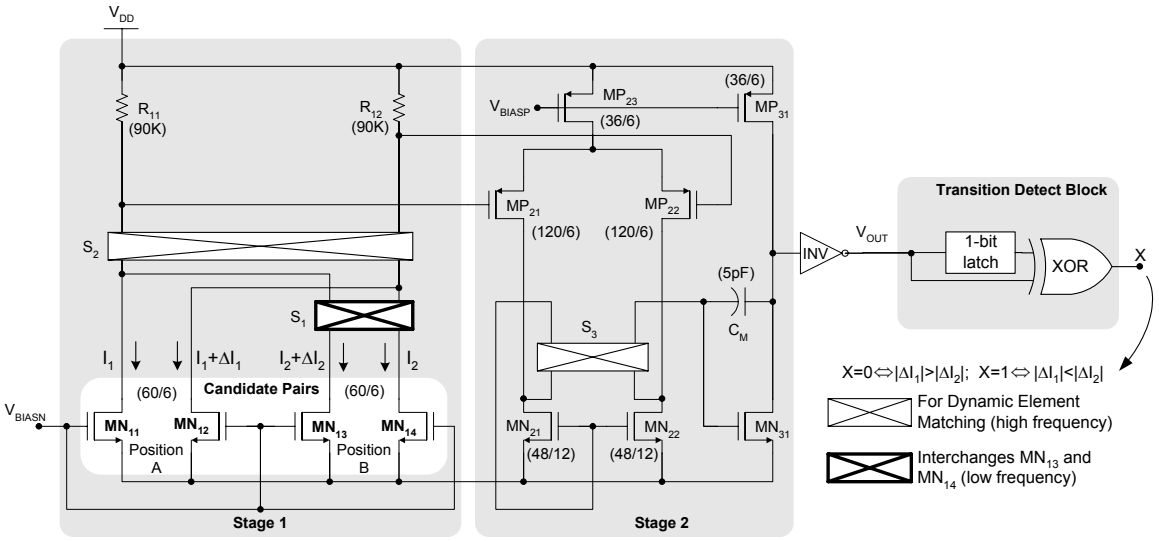


Fig. 3.14. Schematic of an improved comparator whose resolution does not suffer from bulk effects in the candidate pairs.

The accuracy of this circuit is critically dependent on the matching performance of R_{11}-R_{12}, MP_{21}-MP_{22}, and MN_{21}-MN_{22}. The overall input-referred offset resulting from a current density mismatch in MN_{31}, which is dependent on how well MN_{31} matches

MN_{21}-MN_{22} and I_{21} matches I_{31}, is minimal because it is divided by the voltage gain of the first two stages, which is on the order of 50-60dB. Offsets in resistors R_{11}-R_{12} and at the input of the second stage are more critical because they are only divided by the transconductance of the candidate pairs and the gain of the first stage, which is why DEM is used to match these devices – applying DEM by exchanging the connectivity of R_{11}-R_{12}, MP_{21}-MP_{22}, and MN_{21}-MN_{22} several times, with every clock cycle, and therefore, over time, *averaging* their overall effects to zero nearly eliminates all mismatch effects in the comparator. This averaging (low pass filter) function is performed by capacitor C_M, whose Miller effect enhances its filtering capabilities. In simulations, the proposed comparator displayed a worst-case resolution of 90μV with a settling time of 200μs under a 100kHz DEM frequency and 5pF filter capacitor, which is an effective improvement of 3× in resolution from the comparator in Fig. 3.5. Also, since this comparator can achieve this resolution at 4× the DEM frequency, the filter capacitor can be 4 times smaller. This comparator has been used in the next prototype of the Survivor strategy presented in Chapter 6.

3.5 Synopsis

While trimming is a simple strategy to mitigate process-induced errors, it is costly and not as effective against errors like MOS mismatch, which have a non-linear temperature coefficient. By exchanging the effective positions of devices periodically and thereby averaging their mismatch, DEM virtually eliminates MOS mismatch errors without impacting manufacturing cost, but degrades system performance, since it introduces switching noise and lowers bandwidth. Self-calibration techniques offer a viable strategy to effectively perform trimming on-chip, but they inevitably need an accurate voltage reference to maximize their resolution and accuracy. The proposed Survivor strategy is a self-calibration technique that uses DEM strategically (only at start-up or power-on-reset events) to select the best-matched pair from a bank of device pairs,

before using the selected pair to implement critical functions in the system. The IC prototype of the Survivor strategy reliably converged on the best-matching NMOS pair of a bank of 32 pairs, yielding the 3-σ matching performance of (48/4.8) MOSFETs while retaining the bandwidth of (6/0.6) transistors, which amounts to a bandwidth increase of 64×. This improvement is cost-effective because the test-time and noise associated with trimming and DEM schemes are entirely circumvented. The primary trade-off for this is silicon real estate: area used by the bank of devices and relevant control circuits versus the number of fuses or EEPROM electronics used to trim a (6/0.6) device to yield the matching performance of a (48/4.8) transistor. In light of today's increasingly volume-driven, cost-conscious SoC solutions, even if the proposed scheme demands more silicon area, its resulting cost is easier to absorb than test time. In summary, the Survivor strategy is a cost-effective, noise-free method for reducing the random process- and package-induced effects on common, yet critical, analog building blocks like bandgap reference circuits.

CHAPTER 4

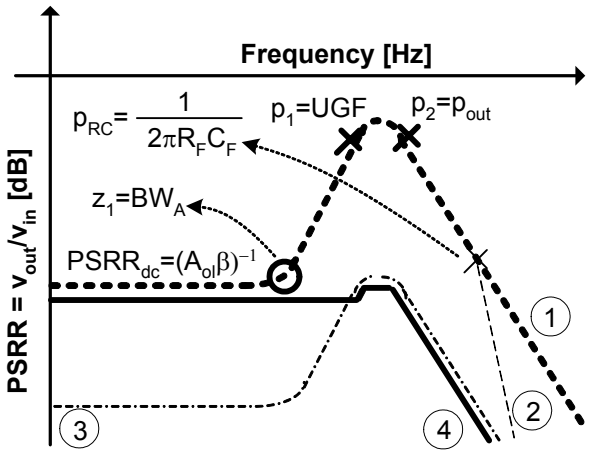
HIGH PSRR

As dense digital circuitry is packed close to sensitive analog blocks for higher integration, SoC solutions are swamped in switching noise generated by digital circuits, RF blocks, and DC-DC converters. To generate a reliable reference voltage in these harsh conditions, bandgap references need to exhibit high dc and ac accuracy despite supply noise that has amplitudes of the order of hundreds of millivolts and frequency components in the range of tens of kiloHertz to hundreds of megaHertz [24]-[27]. Along with high power-supply ripple-rejection (PSRR) performance over a wide frequency range, SoC references need to be capable of operating at the low supply voltages characteristic of modern CMOS processes. These references also need to be stable and reject noise without the aid of bulky external capacitors, using only on-chip capacitors, which are severely constrained in size by silicon real-estate requirements. This chapter discusses state-of-the-art solutions to obtain high PSRR performance, and their respective merits and drawbacks. The discussion leads to the proposed strategy for achieving high PSRR over a large frequency range. The strategy is subsequently described at a system- and circuit-level and experimental results obtained from an IC prototype are then presented and evaluated.

4.1 State-of-the-Art Techniques

In Chapter 2, an intuitive, potential-divider-based model for analyzing the PSRR of bandgap references over a wide range of frequencies was presented. Trace '1' in Fig. 4.1 represents a typical PSRR curve of a conventional reference, as predicted by this model. In particular, PSRR at low frequencies, its dominant zero, and two subsequent poles correspond to the dc open loop gain ($A_{ol}\beta$), the bandwidth of the amplifier (BW_A),

the unity-gain frequency of the system (UGF), and the output pole (p_o), respectively. These curves indicate the worst-case PSRR occurs in the vicinity of the UGF of the system, typically in the range of 1-10MHz [1], [29], [31], [52]-[55]. Intuitively, the loop gain provides high supply-ripple rejection at low frequencies, while the output capacitor shunts any ripple appearing at the output to ground at very high frequencies.



1	- - - -	Conventional reference
2	– – – –	With RC filter at supply
3	-·-·-·-	With NMOS cascode (gate ideal ground)
4	———	With NMOS cascode (large RC filter at gate)

Fig. 4.1. PSRR curve of a bandgap reference.

Numerous techniques have been used to improve the PSRR of bandgap references. The simplest solution is to place an RC filter in line with the power-supply to filter out fluctuations before they reach the reference [1], as shown in Fig. 4.2(a). This adds a pole to the PSRR curve at the filter's corner frequency, as shown by trace '2' in Fig. 4.1. However, since circuits in SoCs often operate under low-voltage conditions, the reduction in available voltage headroom caused by the dc current flowing through this resistor, and the resultant voltage drop, would severely limit its size, pushing the pole to very high frequencies.

A pre-regulator establishes a 'pseudo-supply' for the bandgap reference by forcing a bias current into a small resistance, as shown in Fig. 4.2(b). This technique improves PSRR performance by increasing the resistance between the input supply and

the supply of the reference. While this is a compact and effective technique for achieving high PSRR performance, it has an important drawback: references in SoC solutions need to supply large transient currents to suppress load noise but pre-regulators are limited by their quiescent current in their current sourcing capability. Though this drawback is eliminated by controlling the current source through shunt feedback (as in a linear regulator), the solution proves ineffective to improve PSRR at high frequencies given that the feedback loop of pre-regulator has the same bandwidth limitations as that of the bandgap reference.

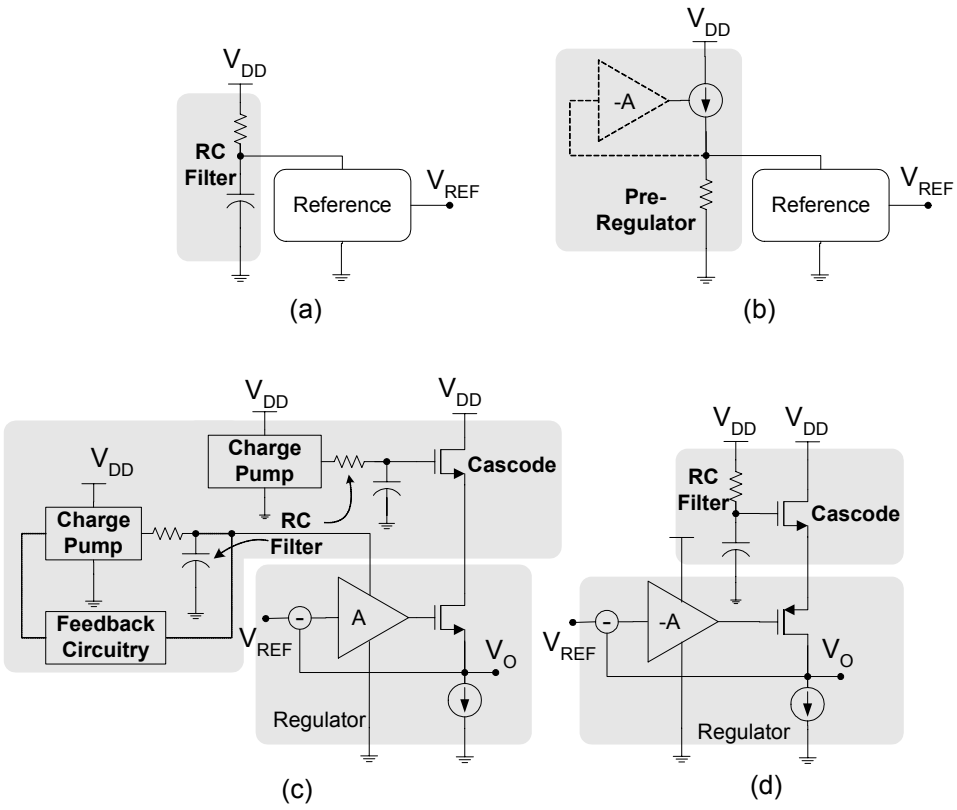


Fig. 4.2. State-of the-art techniques to improve PSRR: (a) use of RC filters, (b) pre-regulation, and (c) and (d) cascoding techniques.

Another technique to suppress the effect of line fluctuations on the accuracy of the reference voltage, and hence improve PSRR performance, is to use NMOS devices to isolate circuits from the power-supply. This strategy has been used effectively with linear regulators [1], [29] and can be applied to references as well. Fig. 4.2(c) presents a

methodology that utilizes a cascode for the NMOS pass device of a linear regulator, thereby isolating it from the noisy power-supply [1]. To maintain low dropout the gate of the cascoding NMOS and the supply of the error amplifier have been boosted using a charge pump. The error amplifier cannot be cascoded as conveniently as the pass device since the gate of its cascode would require a boosted voltage of two gate-source drops above the output, leading to higher complexity in the charge pump design. Hence, it uses an RC filter to suppress fluctuations in the power-supply and the systematic fluctuations of the charge pump. Establishing a low RC filter pole for an SoC solution leads to critical tradeoffs: the capacitance can be increased with a significant increase in silicon real estate consumption or the resistance can be increased thereby limiting the bandwidth of the error amplifier which shall now need to operate at very low current levels to minimize the resistive drop and power dissipation in the filter.

In [29], a PSRR of -40 dB over a wide frequency range is achieved using an NMOS device to cascode the PMOS pass device of a Miller-compensated linear regulator, as shown in Fig. 4.2(d). Due to relatively high voltage headroom (3.3V) the gate of the NMOS cascode is biased through the supply using a simple RC filter. The high voltage headroom also allows the error amplifier, which is powered directly from the supply (versus through a cascode), to use internal cascodes and gain boosting to improve its PSRR performance, leading to higher dropout and power consumption. Moreover, the circuit uses 1.2nF of on-chip decoupling capacitance that occupies an area that is prohibitively large for many VLSI SoC systems.

4.2 Proposed Strategy

4.2.1 Block Diagram

Fig. 4.3 presents the simplified schematic of the proposed system to achieve high PSRR performance and thereby high dc and ac accuracy in the presence of power-supply

fluctuations [64]-[65]. The NMOS cascode, MN_C, shields the entire loading circuit, which may be a voltage reference or a low dropout regulator, from fluctuations in the power-supply through its cascoding effect (effective series resistance), thereby increasing PSRR over a wide range of frequencies, as shown by trace '3' in Fig. 4.1. To relieve voltage headroom requirements and maintain low dropout, the gate of the cascode needs to be biased at a voltage above the supply. This function is performed by the charge pump (CP), which powers a crude voltage reference that establishes a supply-independent bias at the gate of MN_C at a voltage level above the supply.

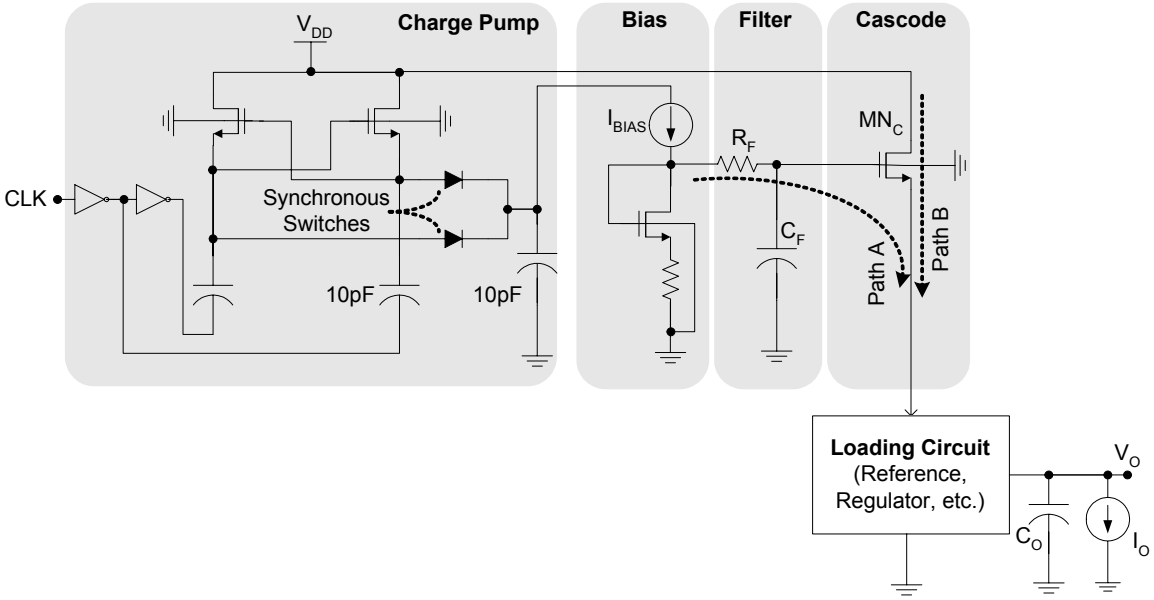


Fig. 4.3. Block diagram of proposed strategy for high PSRR.

Trace '3' in Fig. 4.1 is valid only if the gate of the cascode MN_C is an ideal ground; if any noise in the power-supply couples onto the gate of MN_C, it would be transferred without attenuation to the loading system at its source, producing trace '1' in Fig. 4.1. In other words, since MN_C acts like a voltage follower for noise at its gate, it is critical to shield the gate of MN_C from supply fluctuations. This function is performed by an RC filter at the gate of MN_C, which is used to shunt supply ripple to ground. Referring to Fig. 4.3, the RC filter, comprising of R_F and C_F, filters out high frequency fluctuations in the power-supply to attenuate power-supply noise reaching the gate of the NMOS

cascode and hence to the regulator through Path A. In other words, the RC filter adds a pole to the Path A, affecting the PSRR curve in a manner similar to that of an RC filter in series with the supply. However, since this RC filter is placed in a path that does not carry any dc current, the resistor can be made as large as practically possible, to yield a pole extremely close to dominant zero (BW_A) of the PSRR trace '1' in Fig. 4.1. Hence, the effective PSRR of the system, following trace '1' at low frequencies and trace '3' at high frequencies, is traced by trace '4' in Fig. 4.1.

4.2.2 Circuit Design

The charge pump boosts the voltage at the gate of the NMOS cascode to an optimal voltage level above the supply to produce low dropout across the cascoding device and the loading circuit. It is implemented as a simple voltage doubler presented in [66]. The crude bias reference consumes a total current of 30µA and establishes a stable bias of 2.7V for the cascode by forcing a temperature-independent current of 10µA into a diode-connected NMOS and resistor. The schematic of the charge pump and reference are presented in Fig. 4.4. The RC filter, composed of a 500K resistor and 15pF capacitor, establishes a filter pole of roughly 20kHz to effectively attenuate supply noise. The entire scheme utilizes 50pF of on-chip capacitance making it relatively compact.

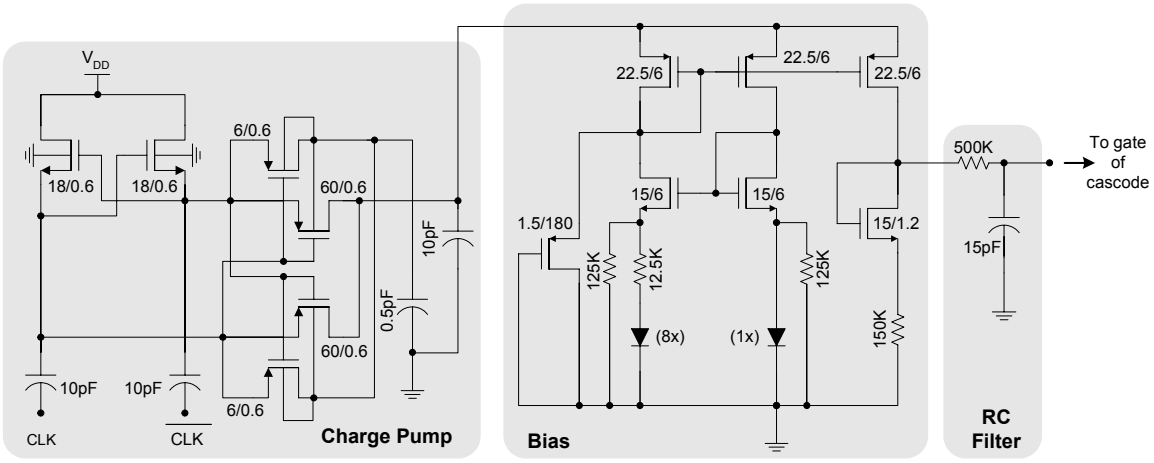


Fig. 4.4. Schematic of charge pump, bias for NMOS cascode, and RC filter.

4.2.1 Measurements Results

The proposed strategy was implemented in a 0.6µm CMOS technology (V_{TN}=0.7V, V_{TP}=-0.9V), measured, and evaluated. For the IC prototype, a 5mA, 0.6µm-CMOS, Miller-Compensated, low-dropout (LDO) regulator was used as a vehicle to demonstrate the effectiveness of the strategy in improving the PSRR performance of noise-sensitive analog blocks. The regulator had the characteristics typical of an SoC regulator deployed at the point of load [1], [24], [29], [67]-[69] – it was internally compensated, had a maximum load current in the range of 3-10mA, and was completely integrated (i.e., had no external capacitors). The schematic of this test regulator is presented in Fig. 4.5. The error amplifier of the LDO consumes 40µA of quiescent current for meeting the transient specifications (and if the 500K-15pF RC filter were inserted in series with it for ripple-rejection, the resistive drop across the filter would be 20V). The die photograph is shown in Fig. 4.6.

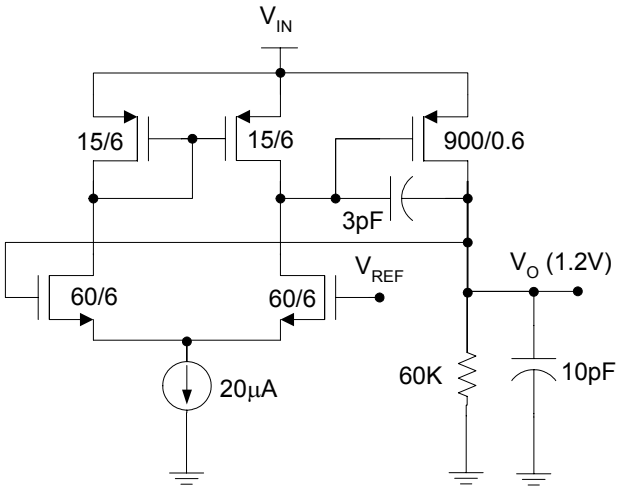


Fig. 4.5. Schematic of test low-dropout regulator.

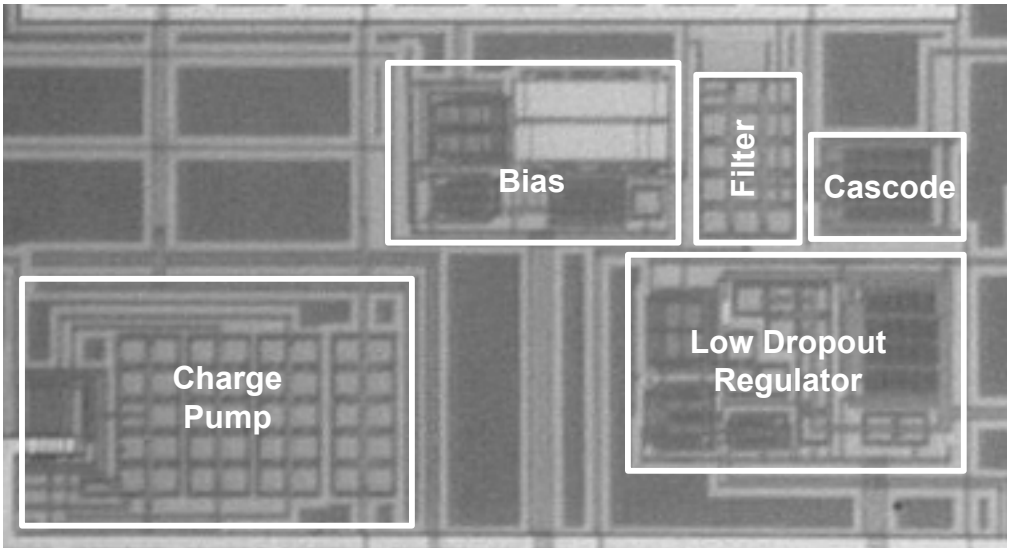


Fig. 4.6. Die photograph of high PSRR prototype IC.

Experimental Results

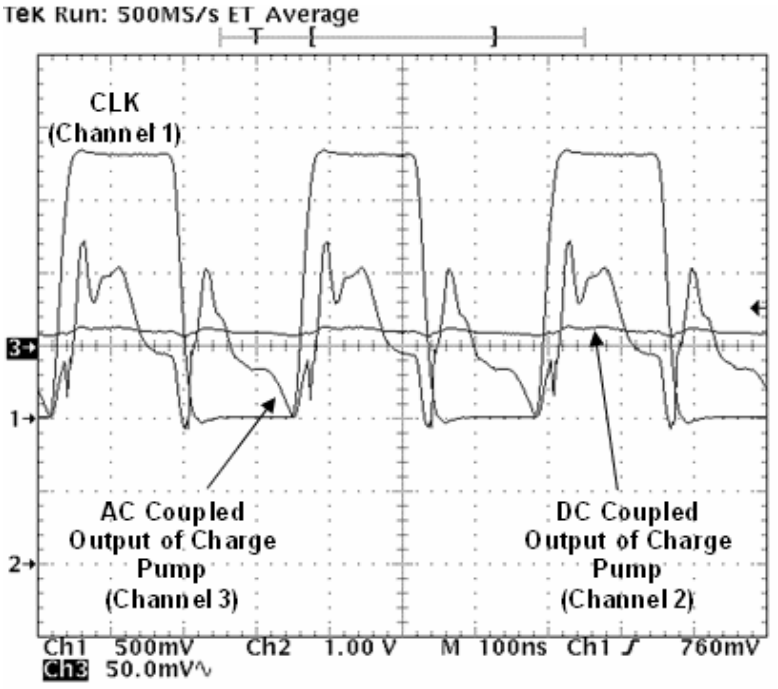


Fig. 4.7. Measured charge pump waveforms.

The individual blocks in the high PSRR strategy were first tested independently to verify their functionality. The output of the charge pump is presented in Fig. 4.7 – it shows the doubler generating an output voltage of roughly 3.5V for an input of 1.8V with

an associated ripple because of the small quiescent current consumed by the bias reference. The line regulation of the bias, showing the stable output voltage of 2.7V, and the core LDO, showing a minimum required voltage headroom of 1.6V, is presented in Fig. 4.8.

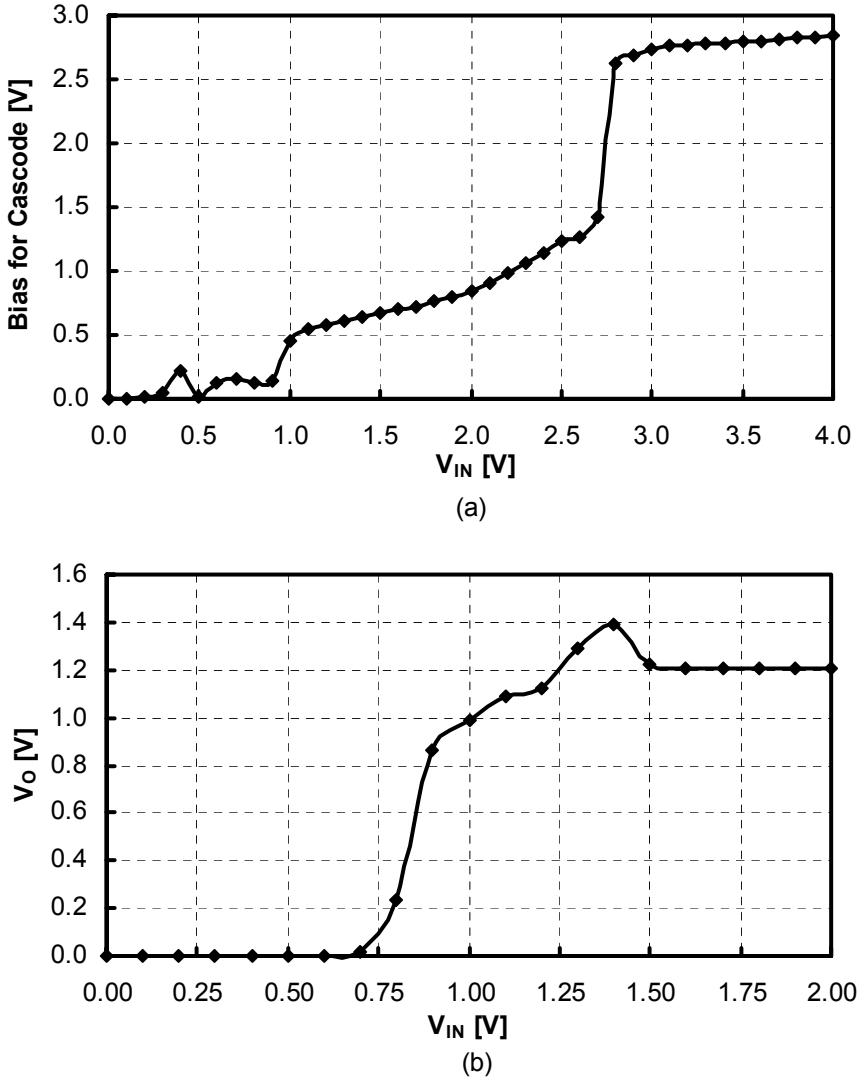


Fig. 4.8. Measured line regulation of (a) crude reference for biasing cascode and (b) core LDO regulator.

The measured worst-case PSRR of the Miller-compensated LDO was 3dB, as shown in Fig. 4.9. In other words, the LDO was *amplifying* supply ripple near its unity-gain frequency (UGF), as many Miller-compensated systems are known to do [52]-[53].

The cascoding strategy enhanced the worst-case PSRR of the LDO by 30dB, in other words, the PSRR performance at the UGF improved to -27dB.

The PSRR of the bias reference is roughly -20dB and starts rolling off after 10MHz; the RC filter in series, however, ensures that the roll off takes place at a much lower frequency of 20KHz. When the supply of MN_C and CP is decoupled and noise is introduced only in the latter (Path A in Fig. 4.3), the system rejects noise through the combined PSRR of the voltage reference, RC filter, and test regulator. When noise is introduced only at the drain of MN_C (Path B in Fig. 4.3), which is in saturation, its high drain-resistance shields the Miller-compensated core regulator ultimately leading to a 30dB improvement at the worst case. The cascode strategy impacts the transient response of the regulator and degrades the accuracy by approximately 171mV for a 5mA load step as shown in Fig. 4.10. The minimum voltage headroom required by the system is given by

$$V_{DD-min} = \max\{V_{TP} + 4V_{DS-sat}, V_{OUT} + 2V_{DS-sat}\}, \tag{4.1}$$

which, given an output voltage of 1.2V and V_{TP} of 0.9V for this process, is approximately 1.8V.

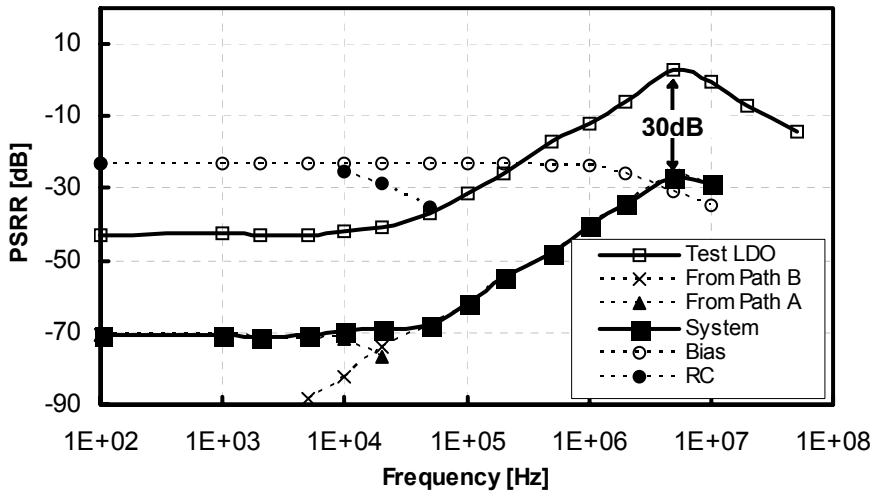


Fig. 4.9. Measured PSRR performance without and with cascoding strategy.

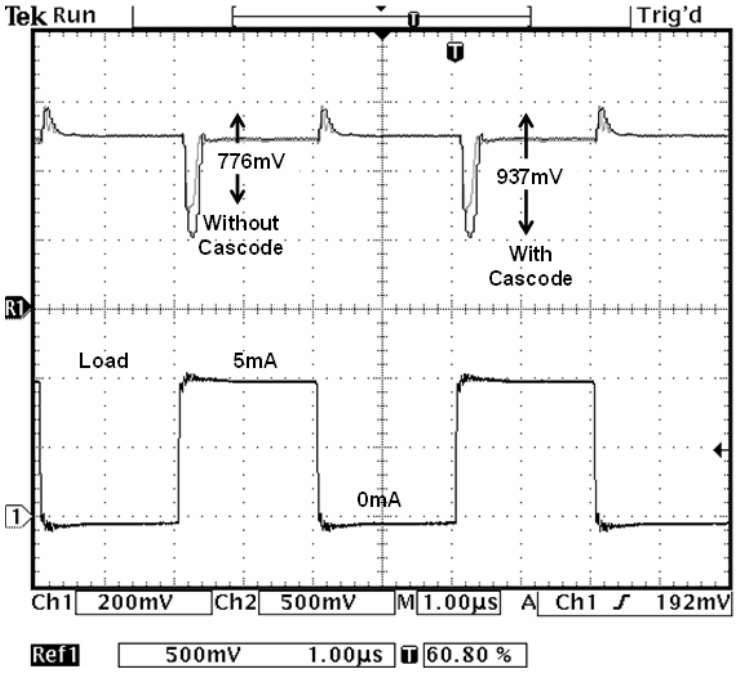


Fig. 4.10. Measured impact of cascode on LDO transient response.

4.3 Synopsis

State-of-the-art techniques to achieve high PSRR require bulky external capacitors, consume large voltage headroom, or compromise transient response significantly for conserving silicon area. The proposed technique uses strategically placed RC filters to suppress supply noise and thereby achieve high PSRR without impacting voltage headroom requirements significantly. The technique uses a charge pump to power a crude voltage reference that biases the gate of an NMOS cascode that shields the entire reference from fluctuations in the power-supply. An IC prototype, that used a 5mA CMOS SoC LDO regulator as the load for the high PSRR strategy, demonstrated the effectiveness of the strategy in achieving a 27dB improvement in worst-case PSRR performance. The entire scheme uses only 50pF of on-chip capacitance and is therefore considerably compact. In conclusion, an integrated, compact, low-voltage, and high-bandwidth scheme for obtaining high PSRR performance for SoC voltage references has been presented.

CHAPTER 5

LOW OUTPUT IMPEDANCE

Low output impedance enables a voltage reference to shunt noise and source currents and thereby maintain high dc and ac accuracy despite variations in loading conditions. This is why, as is evident from a number of datasheets [47]-[51], most of the references used in industry for noise-sensitive sub-system like an analog-to-digital converter or voltage-controlled oscillators are variations of the regulated references presented in [5], [8]. Reported state-of-the-art regulated (i.e., low output impedance) references, however, only produce the conventional 1.2V bandgap voltage, or a higher voltage [6], [5], [8], [10]-[11], [41], [70] which is increasingly incompatible with the low breakdown voltages of the modern CMOS processes typically used for SoCs. This chapter discusses the challenges in achieving low output impedance in a CMOS reference before presenting a CMOS bandgap reference that is concurrently low-voltage and low-impedance. Measured data on a prototype of the proposed reference is then discussed and evaluated.

5.1 Challenges in an SoC Environment

Generating sub-bandgap voltages for modern CMOS environments, which typically exhibit low breakdown voltages and are consequently constrained to low supply voltages, normally require current- [13]-[14], [22], [71]-[75] or current-voltage hybrid-mode [15], [76] approaches, as shown in Fig. 5.1, where regulated currents are sourced and summed into resistors, leading to relatively high output impedance levels (i.e., unregulated output voltages). Since these strategies are current-driven, shunt sampling, which is typically used to decrease output impedance and shunt ac noise, is not easily implemented.

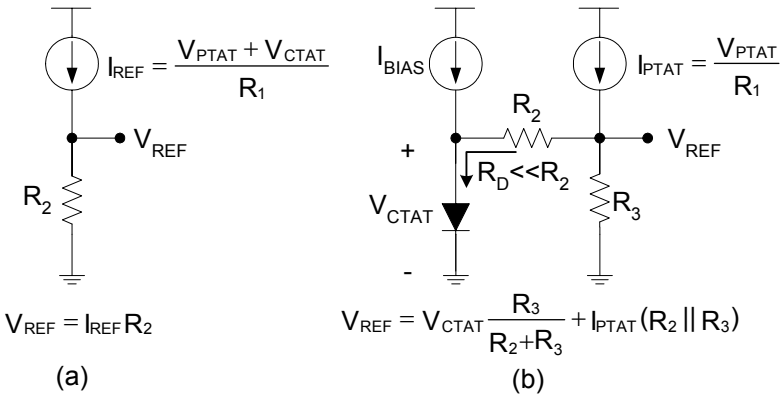


Fig. 5.1. Reported (a) current- and (b) hybrid-mode sub-bandgap approaches.

As shown in Fig. 5.2, a series linear regulator or amplifier in unity-gain configuration can be used to buffer the output of a low-voltage, high output impedance reference and thereby increase its current sourcing ability. The buffer, however, introduces additional systematic and process-induced random offset components to the reference, significantly degrading the dc accuracy performance of the system [39], [77]-[80]. For instance these offsets, which mostly result from finite loop gain and device mismatch, caused an additional ±4mV error in [39]. The error, which already takes up 0.4% of a 1V reference, leaves little in the total error budget for the reference.

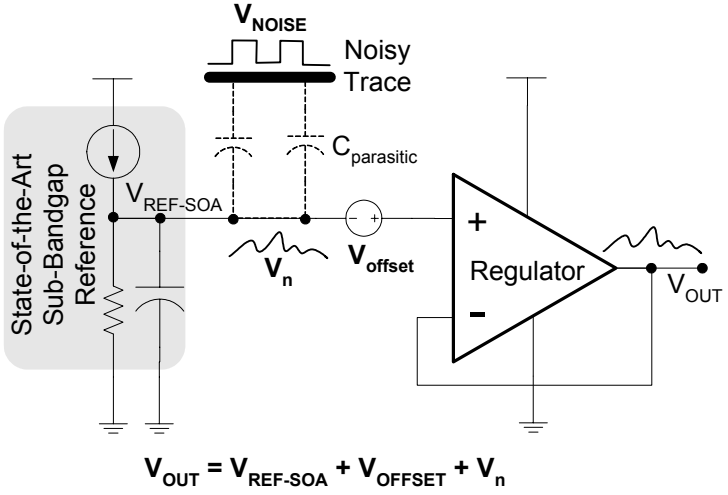


Fig. 5.2. Reference-regulator low-impedance circuit and its adverse treatment of noise and offset.

This phenomenon is particularly troubling in CMOS technologies because MOS

offsets have a non-linear dependence to temperature, which cannot be properly compensated with trim [41]. Even if this accuracy degradation were acceptable, a low output impedance buffer, which is nothing more than an operational amplifier in non-inverting feedback-gain configuration, does little to attenuate the noise already present in the high-impedance reference, since it simply propagates the disturbance to the output unabated.

5.2 Proposed CMOS Bandgap Reference

5.2.1 Topology

For shunt feedback, which is necessary for low output impedance, the reference must be the sum of temperature-dependent voltages (not currents), as illustrated in the proposed circuit of Fig. 5.3, where a PTAT voltage is sampled and regulated via amplifier OA_1 and power PMOS MP_O. The amplifier has a pre-set PTAT offset voltage and the loop regulates and impresses this voltage across R_{13}. The temperature-compensated output is the sum of this PTAT voltage ($V_{R\text{-}PTAT}$), the CTAT diode-derived voltage across R_{12} ($V_{X\text{-}CTAT}$), and the additional PTAT voltage component across R_{12} ($V_{X\text{-}PTAT}$), that results from running R_{13}'s PTAT current through R_{12} and is given by

$$V_{REF} = V_{R-PTAT} + V_X = V_{R-PTAT} + (V_{X-PTAT} + V_{X-CTAT}) = V_{PTAT} + V_{CTAT}. \quad (5.1)$$

Neglecting relatively small second- and higher-order curvature effects, the forward-biased voltage of diode D decreases linearly with temperature and hence has a CTAT behavior. This CTAT voltage is attenuated by the potential divider comprised of resistors R_{11} and R_{12} to produce CTAT voltage component $V_{X\text{-}CTAT}$ at node V_X.

Amplifier OA_1 and pass device MP_O constitute the high loop-gain, shunt-feedback path ($A_{ol}\beta$) around V_{REF}. This negative feedback loop regulates the output against variations in the input supply and load. Since MP_O is a large PMOS device, the

regulated reference can sustain low supply voltages under relatively high load currents; in other words, it incurs a low dropout voltage.

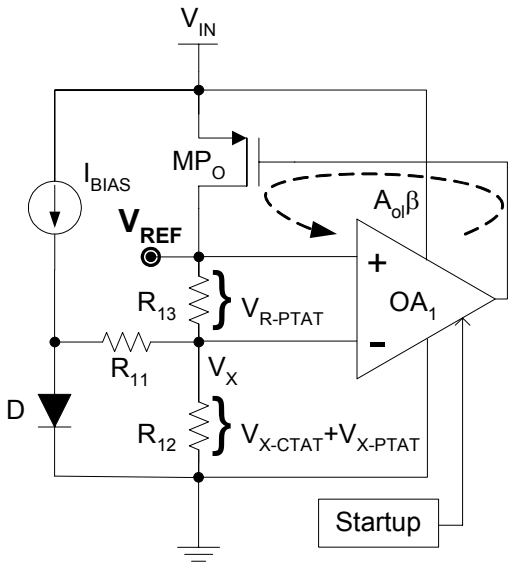


Fig. 5.3. Block diagram of the proposed low-impedance sub-bandgap reference.

5.2.2 Lateral PNP Transistors

A PTAT voltage is normally generated with bipolar transistors, but standard CMOS process technologies do not have optimized bipolar devices. Parasitic vertical PNP bipolar transistors in p-substrate technologies, for instance, are more like diodes because their collectors are necessarily tied to the substrate (i.e., the negative supply or ground). Lateral PNP transistors inherently present in PMOS devices, on the other hand, are not limited in this way, and in spite of their typically low Early voltages, they have been successfully used in a host of analog applications like bandgap references, oscillators, variable gain amplifiers, etc. [10], [81]-[83]. Having access to all three terminals allows the designer to use feedback control and more efficiently process analog signals.

The lateral PNP devices available in the standard CMOS technology used for the foregoing design were characterized using 15 samples over 2 fabrication runs from which SPICE-model parameters were extracted and verified (e.g., Early voltage (VAF), current

gain β (BF), reverse-saturation current (IS), etc.) [84]. Reverse-saturation current was measured to be 3fA and Early voltage and β were found to be 6V and 100A/A, respectively, which are not compatible for simple common-emitter high voltage gain stages but useful in current-gain applications, to drive low-impedance nodes. The simple electrical model used for this device shows reasonably good correlation in the forward-active region (Fig. 5.4), which is where these devices will be designed to operate.

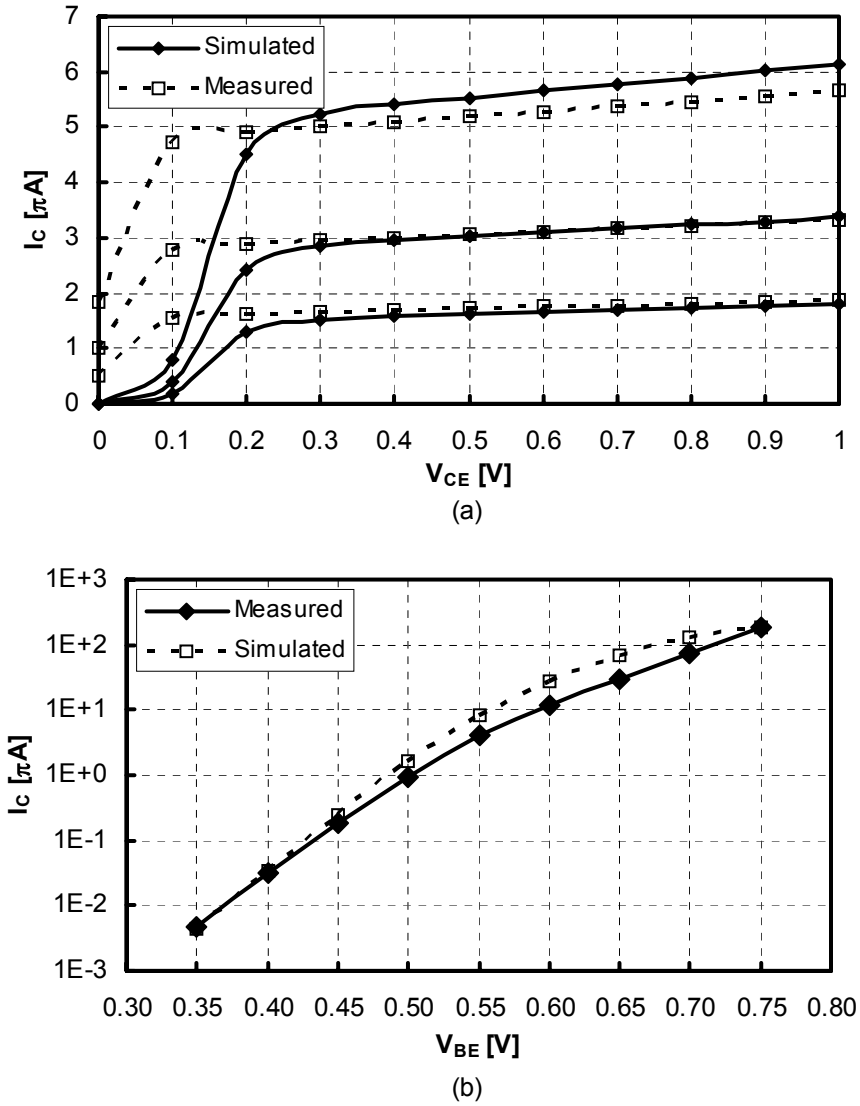


Fig. 5.4. Measured and simulated (a) I_C vs. V_{CE} vs. V_{BE} and I_C vs. V_{BE} curves for lateral PNP transistors.

5.2.3 Complete Circuit Realization

The complete circuit shown in Fig. 5.5 is comprised of a biasing block and the output stage and amplifier presented in Fig. 5.3. Lateral PNP devices QP_{21}-QP_{22}, current-mirror MP_{21}-MP_{22}, current sources MN_{21}-MN_{22}, and cascode transistors MN_{23}-MN_{24} constitute amplifier OA_1. Resistors R_{14} and R_{15} implement a voltage divider circuit whose total resistance and series combination is modeled by R_{12}. The bias current is defined by a conventional PTAT generator block using lateral PNP devices QP_{B1}-QP_{B2} with R_{B1} and a current-mirror comprised of MN_{B1} and MN_{B2}, in addition to long-channel start-up device MN_S.

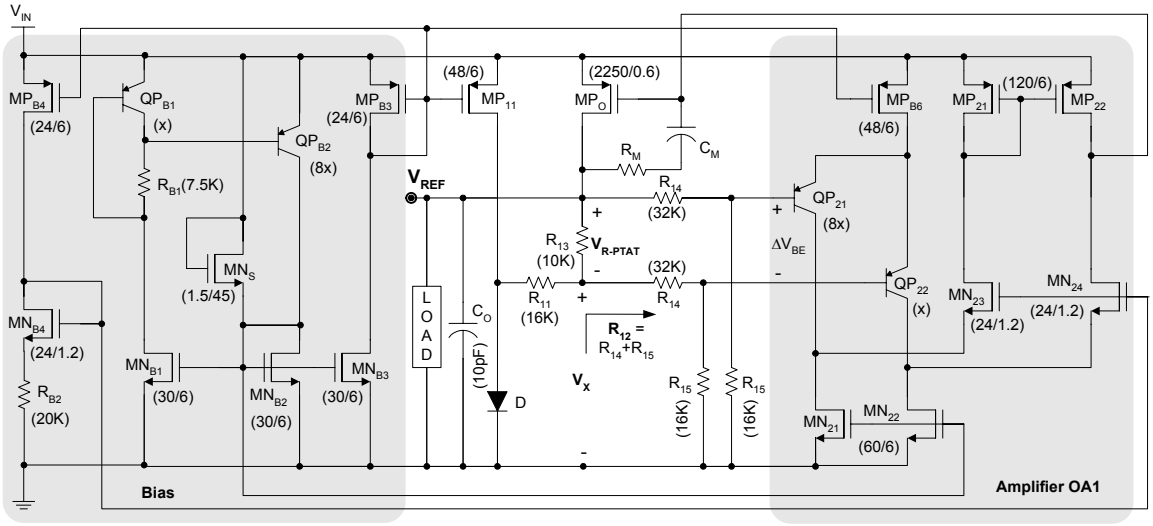


Fig. 5.5. Schematic of proposed low-impedance bandgap reference.

Key to this circuit is OA_1's PTAT offset voltage, which is intrinsically defined by input pair QP_{21}-QP_{22} and current-mirror MP_{21}-MP_{22}. The current-mirror ensures equal currents flow through QP_{21}-QP_{22}, whose emitter areas are $8\times$ and $\times$, respectively. The resulting difference in the collector-current densities of QP_{21}-QP_{22} (i.e., $I_C/8\times$ and $I_C/\times$) produces a PTAT difference across their base-emitter voltages, much like a traditional PTAT generator (i.e., $\Delta V_{BE} = V_T \ln(8)$), through a manifestation of the well-known Gilbert principle [7].

Neglecting base currents (i.e., r_π), since current-gain β is approximately 100A/A, the offset voltage across the bases of QP_{21}-QP_{22} is the voltage divided version of the voltage across R_{13}; or equivalently, the voltage across R_{13} ($V_{R\text{-}PTAT}$) is an amplified version of the PTAT voltage present at the bases of QP_{21}-QP_{22},

$$V_{R-PTAT} = \left(\frac{R_{14} + R_{15}}{R_{15}} \right) \Delta V_{BE} . \tag{5.2}$$

This voltage defines R_{13}'s PTAT current I_{PTAT}, which ultimately flows into node V_X. Using superposition, the PTAT and CTAT components of V_X are

$$V_{X-PTAT} = (R_{11} \| R_{12}) \frac{V_{R-PTAT}}{R_{13}} = \left(\frac{R_{11} \| R_{12}}{R_{13}} \right) \left(\frac{R_{14} + R_{15}}{R_{15}} \right) \Delta V_{BE} \tag{5.3}$$

and

$$V_{X-CTAT} = \left(\frac{R_{12}}{R_{12} + R_{11}} \right) V_{BE} , \tag{5.4}$$

where

$$R_{12} = R_{14} + R_{15} . \tag{5.5}$$

Since the ac-impedance into diode D is negligibly small, substituting Eqns. (5.2)-(5.5) in Eqn. (5.1) and simplifying yields a first-order temperature compensated reference voltage,

$$V_{REF} = K_1 V_{BE} + K_2 K_3 \Delta V_{BE} = K_1 \left(V_{BE} + \frac{K_2 K_3}{K_1} \Delta V_{BE} \right), \tag{5.6}$$

where ΔV_{BE} is PTAT and K_1, K_2, and K_3 are

$$K_1 = \frac{R_{12}}{R_{12} + R_{11}} = \frac{R_{14} + R_{15}}{(R_{14} + R_{15}) + R_{11}}, \tag{5.7}$$

$$K_2 = \frac{R_{14} + R_{15}}{R_{15}}, \tag{5.8}$$

and

$$K_3 = 1 + \frac{R_{11} \| R_{12}}{R_{13}} = 1 + \frac{R_{11} \| (R_{14} + R_{15})}{R_{13}}. \quad (5.9)$$

To design the reference, coefficients K_1, K_2, and K_3 are first determined, after which the resistors are appropriately sized. R_{15} must be significantly smaller than small signal base-emitter resistance r_π to ensure Eqn. (5.2) and therefore Eqns. (5.3)-(5.9) hold, which is not difficult because β is high.

To ensure the lateral PNP devices only drive low-impedance points, given their low Early voltages, a folded cascode topology comprised of MN_{21}-MN_{24} and MP_{21}- MP_{22} is used in this design. The dominant low frequency pole of the loop is consequently established at the gate of MP_O through Miller-compensating capacitor C_M. Resistor R_M is a nulling resistor used to push the right-hand plane (RHP) zero associated with Miller capacitor C_M and power transistor MP_O to high frequencies. It is noted that QP_{B1}-QP_{B2} in the bias circuit also drive low-impedance nodes.

5.2.4 Results of Measurements on Prototype

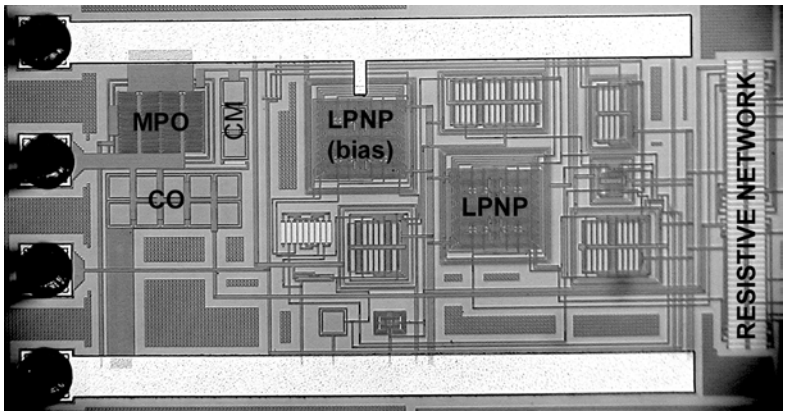


Fig. 5.6. Die photograph of prototype of low-impedance bandgap reference.

The proposed circuit was fabricated with AMI's 0.6μm CMOS process technology ($V_{TN} \approx 0.7$V and $|V_{TP}| \approx 0.9$V) through the MOSIS design facility. A chip photograph of the die is shown in Fig. 5.6. The lateral PNP devices used were a combination of several minimum-sized "emitter-dot" PNP transistors whose individual

base-widths are set by the rings of the poly-silicon gates surrounding the dots. The gates were connected to the positive supply to prevent the PMOS devices inherent to the structure from inverting the n-well region directly underneath the gate and creating a p-channel. The combined measurement results of 26 samples are presented in Figs. 5.7-5.12 a summary of which is also shown in Table 5.1.

Table 5.1. Performance summary of the proposed low-impedance, sub-bandgap CMOS reference (unless otherwise stated, V_{DD} = 1.5V, T_A = 25°C, and I_{LOAD} = 0A).

Parameter	**Conditions**	**Measured**		**Unit**
		(mean)	**(σ)**	
Untrimmed V_{REF}		911.4	2.9	mV
Trimmed V_{REF}		890.5	0.9	mV
TC (trimmed)	-40°C ≤ T_A ≤ 125°C	13.9	6.9	ppm/°C
Load Regulation	0 ≤ I_{LOAD} ≤ 5mA; V_{DD} = 1.5V	1.57	0.06	mV/mA
Line Regulation	1.4V ≤ V_{DD} ≤ 2.5V	1.72	0.35	mV/V
Start-up Time		500.0	49.3	μs
Quiescent Current		128	3	μA
Minimum Supply Voltage		1.25	0.01	V

For the prototype, accuracy across process variations and temperature was achieved by trimming the two R_{15} resistors connected to the base terminals of QP_{11}-QP_{12}. Appendix C describes the procedure for obtaining this 'magic voltage', in other words, the value of the reference voltage for which the least temperature variation is experienced across several samples. The measured TC performance of the circuit across 20 samples is presented in Fig. 5.7. Using the "box method," whereby the TC of the reference is calculated by taking the difference of the absolute maximum and minimum reference voltages for all measured samples across the entire temperature range, the combined

effective TC of the reference was 34.7ppm/°C with a mean of 13.9ppm/°C and a 1-sigma variation of 6.9ppm/°C.

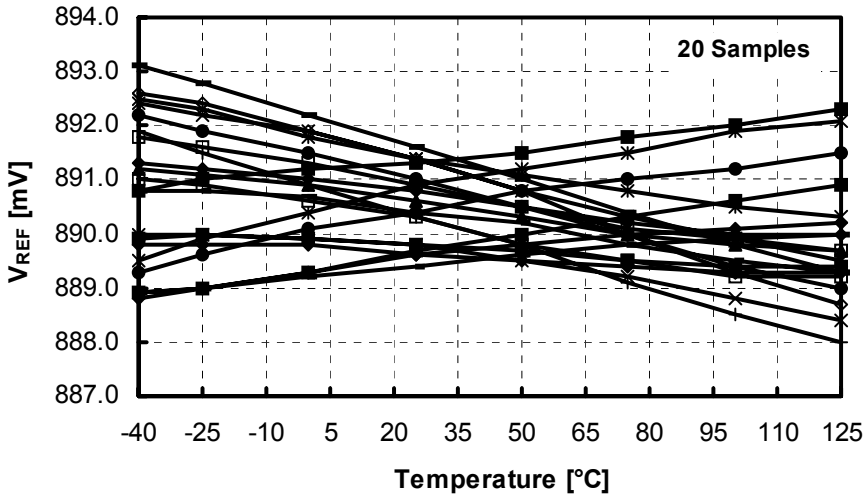


Fig. 5.7. Measured temperature dependence of trimmed samples.

The magic voltage of the prototype circuit was approximately 10mV off its ideal target of 900mV. The reason for this deviation is inaccuracies in the model of diode D (in Fig. 5.5) across temperature. The circuit could have been trimmed to 0.9V but the temperature-dependence would have increased. In practice, the magic voltage is usually centered with a second fabrication run. A more accurate model for the diode geometry used would also mitigate this offset.

Load regulation (LDR) was 1.57mV/mA up to a maximum current of 5.0mA, as shown in Fig. 5.8. The voltage droop in the reference, which was less than 12mV over the entire load-current range, is the result of finite loop gain. Increasing this gain would decrease this variation but at the possible cost of compromised stability. The transient load-induced variation of the reference when subjected to a load current step of 0-5mA with 100ns rise and fall times was +300 and -500 mV, as shown in Fig. 5.9, which is a measure of the circuit's ability to suppress load dump effects.

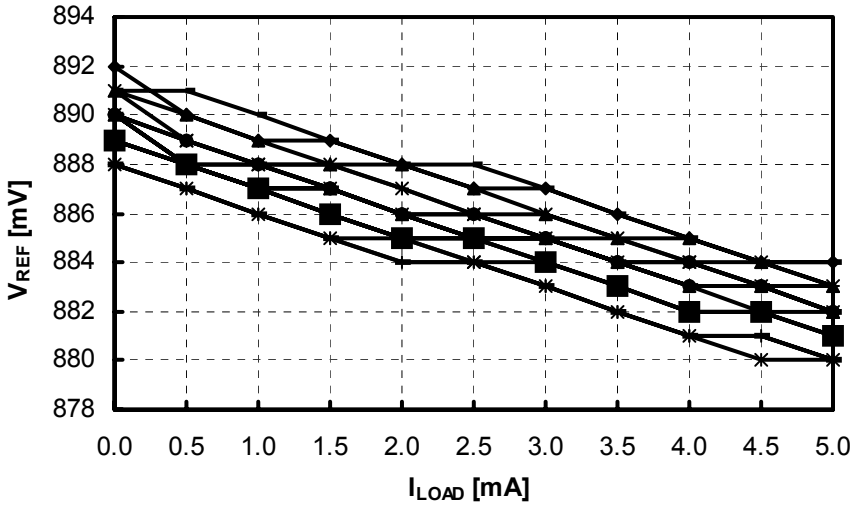


Fig. 5.8. Measured load regulation performance of trimmed samples up to a DC load current of 5mA.

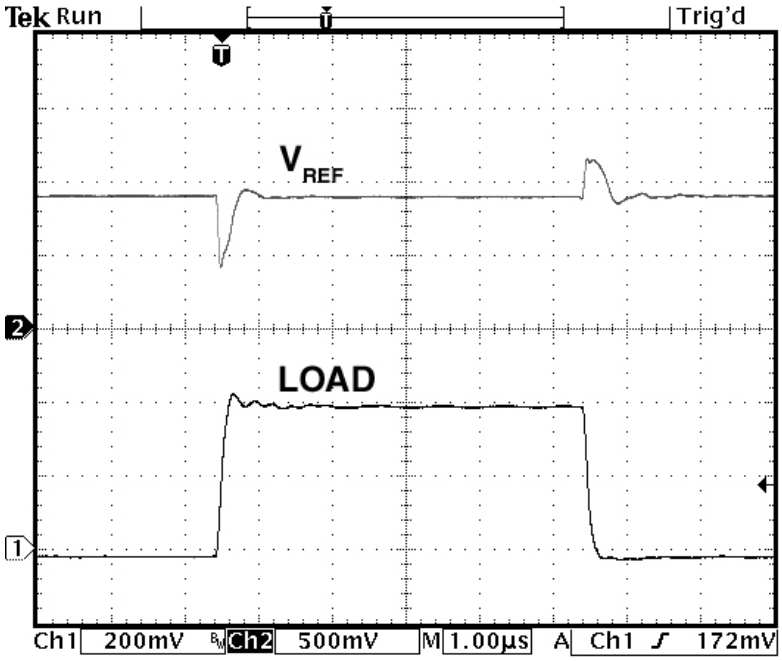
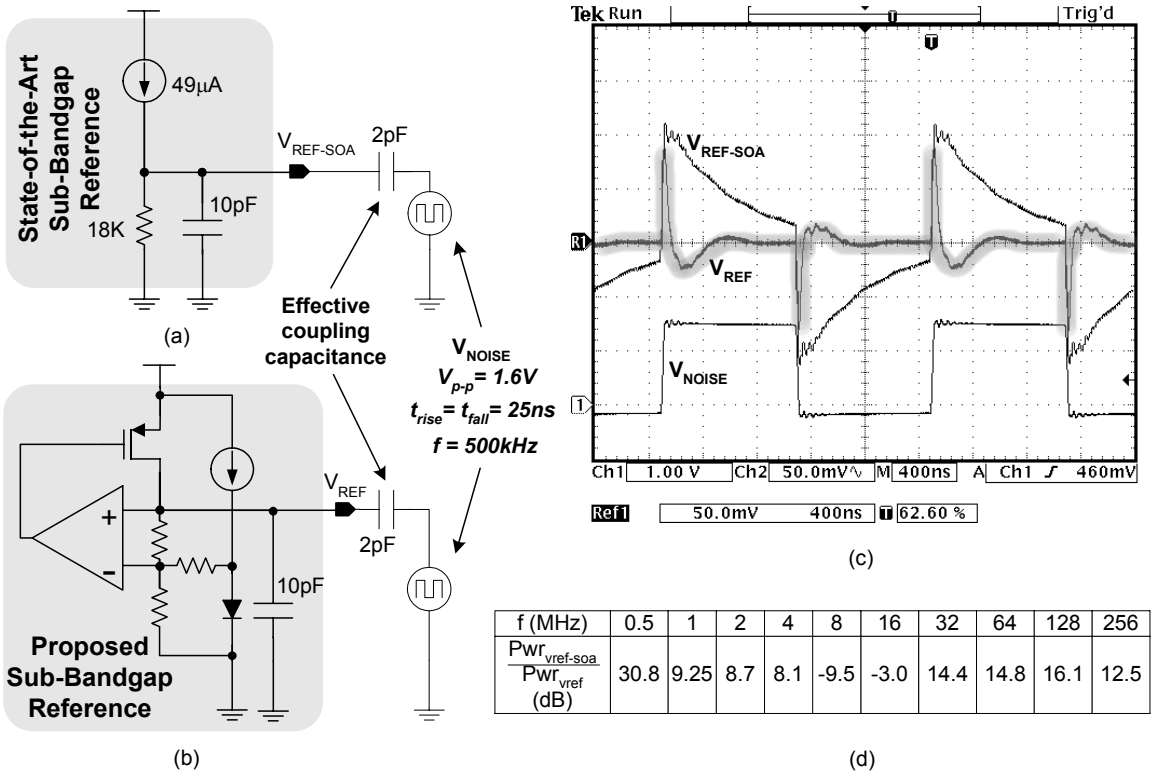


Fig. 5.9. Measured load regulation performance of a trimmed sample for a transiently varying load of 5mA.

To gauge the noise-shunting capabilities of the proposed circuit against the state-of-the-art, a current-mode 890mV sub-bandgap reference was built by sourcing 49µA into an 18kΩ-10pF output resistor-capacitor combination, as illustrated in Fig. 5.10(a). To emulate noise injection through parasitic coupling capacitors, a noise current of

roughly 125μA was injected into the reference (state-of-the-art $V_{REF\text{-}SOA}$ and proposed V_{REF}) by coupling a $1.6V_{p\text{-}p}$ square-wave signal with rise and fall times of 25ns via a 2pF coupling capacitor, as shown in Figs. 5.10(a) and (b), where the output capacitance of the proposed reference is also 10pF.



f (MHz)	0.5	1	2	4	8	16	32	64	128	256
$\frac{Pwr_{vref\text{-}soa}}{Pwr_{vref}}$ (dB)	30.8	9.25	8.7	8.1	-9.5	-3.0	14.4	14.8	16.1	12.5

Fig. 5.10. Noise rejection measurements: set-up for (a) the state-of-the-art sub-bandgap reference and (b) proposed circuit and corresponding ac-coupled (c) transient and (d) frequency ($V_{REF\text{-}SOA}$-to-V_{REF} noise power ratio) response.

A comparison of the transient response of the two circuits (Fig. 5.10(c)) shows how the proposed reference suppresses most of the broadband ac noise injected, quickly recovering its output to the desired level. The instantaneous (high frequency) peak, however, was approximately the same for both circuits because the high frequency components of the noise (25ns rise and fall times produce up to 40MHz harmonics) exceed the bandwidth of the proposed circuit (3.3MHz), where shunt feedback no longer helps. The frequency spectra of the two waveforms (Fig. 5.10(d)) reveal similar

conclusions, that the proposed circuit (V_{REF}) further rejects noise by a factor of 30.8 to 8.1dB ($V_{REF\text{-}SOA}$-to-V_{REF} noise power ratio) from 500kHz to 4MHz. The noise rejection trend is again seen to be favorable for the proposed circuit at 32-256MHz, but the setup was not optimized for these frequencies and the results for these frequencies are therefore inconclusive. It is noted that while increasing the output capacitance of the state-of-the-art sub-bandgap reference reduces the initial peak in $V_{REF\text{-}SOA}$, it simultaneously increases settling time thereby still exhibiting the inability of the reference to suppress noise at low-moderate frequencies.

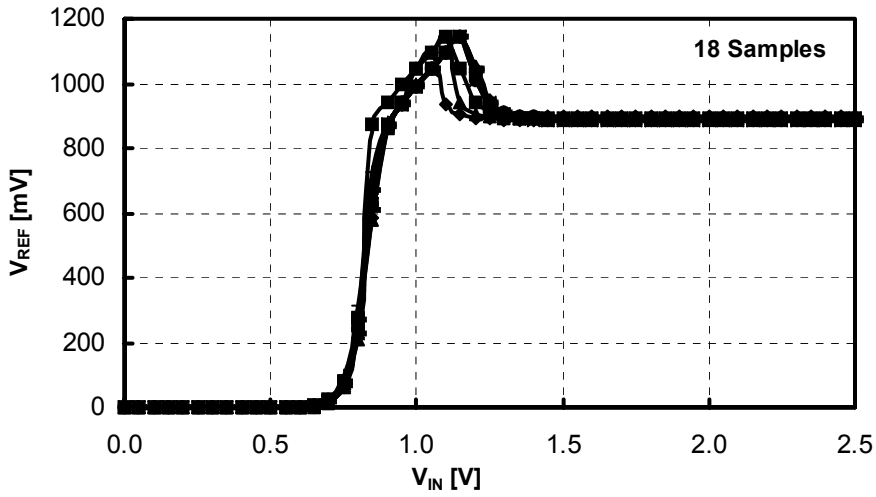


Fig. 5.11. Measured line regulation performance of trimmed samples.

The line regulation (LNR) performance of the circuit was 3.5mV/V, as illustrated in Fig. 5.11. Given a 1.25V minimum input voltage, the merits of a sub-bandgap reference are less obvious, since a conventional 1.2V bandgap reference could viably be designed under a minimum supply voltage of 1.25V, from which a resistor ladder could generate a lower voltage tap-point. If this were to be the case, the resistance values in the ladder would have to be high to cater to the low power demands of portable electronics, thereby establishing a relatively high output impedance, sub-bandgap reference, which goes against the teachings of the foregoing low-impedance argument.

Perhaps more important to note, however, is that the chip prototype built is limited to 1.25V only because of the unusually high PMOS threshold voltage V_{TP} of the process technology used. The circuit's minimum supply voltage is constrained by the threshold voltage of PMOS transistor MP_{21} ($|V_{TP}| \approx -0.9V$) and the saturation voltages of MP_{21}, MN_{23}, and MN_{21}. Using the lower threshold voltages inherent in mainstream CMOS technologies (e.g., 0.4-0.7V) would relax the dependence of the circuit's minimum input supply voltage on V_{TP}, further justifying the merits of the proposed circuit.

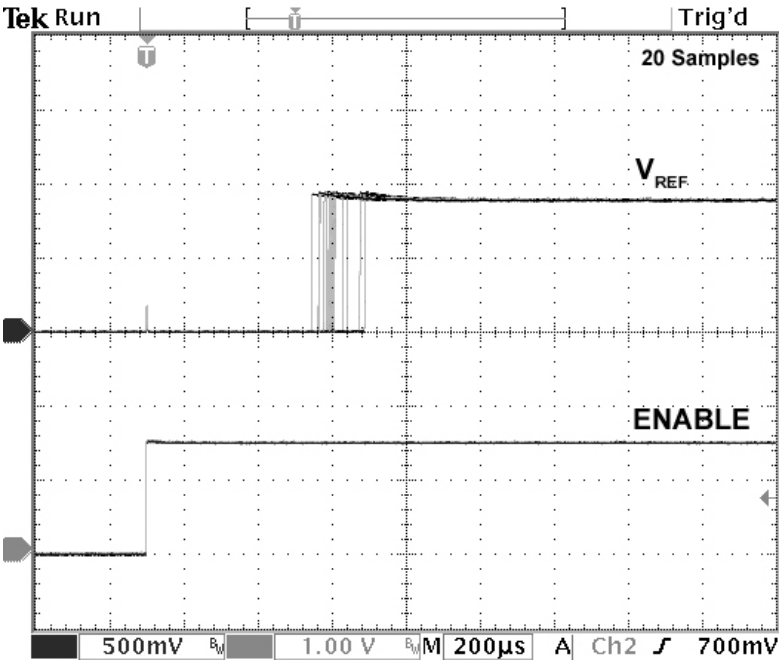


Fig. 5.12. Measured start-up time delay of trimmed samples (obtained by superimposing several individual snapshots).

The circuit was "enabled" with a digital signal and its mean start-up time was 500µs, as shown in Fig. 5.12. Start-up time delay could have been reduced by increasing the width or reducing the length of start-up device MN_S. Increasing this start-up current would adversely alter the PTAT characteristics of the bias current and therefore slightly change the magic voltage and overall accuracy performance of the reference.

5.3 Synopsis

Along with being independent of process, temperature, and line variations, references in state-of-the-art SoC applications must be low-impedance, tolerant of low supply voltages, and in many cases, low-voltage (i.e., sub-bandgap or less than 1.2V). Low output impedance is particularly important to not only source steady state DC and transient load currents without compromising accuracy but also shunt noise that would otherwise cause overall system instabilities and degrade accuracy. A buffer in series with a conventional, sub-bandgap, high impedance reference shunts load noise but not the coupled noise resulting from SoC integration, which is injected directly into the reference and propagated to the output and consequently the rest of the system via the buffer. A 0.5μm CMOS reference circuit that, unlike reported circuit topologies, adopts a voltage-mode approach to generate a sub-bandgap reference voltage and is therefore concurrently low-voltage and low output impedance, is designed, fabricated, and evaluated. For over 20 sample ICs measured, the proposed reference, which is capable of sourcing up to 5mA of load current while producing a first-order temperature compensated voltage of 890mV, exhibited a combined worst-case temperature coefficient of 34.7ppm/°C and a load and line regulation performance of 1.57mV/mA and 1.72mV/V with a sigma variation of 0.06mV/mA and 0.35mV/V, respectively.

CHAPTER 6

SYSTEM DESIGN

Three strategies that can potentially improve the accuracy of bandgap reference circuits have been proposed thus far. The Survivor strategy proposed in Chapter 3 promises a low-cost, noiseless technique to mitigate process- and package-induced mismatch effects [59]. With regards to bandgap references in particular, it can also improve accuracy across temperature by reducing the effects of mismatch on the PTAT component of the reference voltage. The cascoding strategy presented in Chapter 4 proved effective in improving the immunity of its loading circuit, which can possibly be a bandgap reference, to line variations by as much as 30dB [64]-[65]. Finally, the all-voltage-mode shunt-feedback approach proposed in Chapter 5 allowed a CMOS bandgap reference, which is inherently immune to temperature variations to the first order, to withstand load and line variations. The same reference had the added advantage of having the capability to generate any desired sub-bandgap reference voltage compatible with modern low-voltage CMOS environments. This chapter presents system- and circuit-level considerations for integrating all these techniques to build an accurate, trimless, high PSRR, low-voltage, CMOS bandgap reference IC, the conceptual diagram of which is presented in Fig. 6.1. After reviewing the operation of the each of these three techniques, system-level design issues are discussed. The measurement results on an IC that support these proposed techniques are then presented and evaluated.

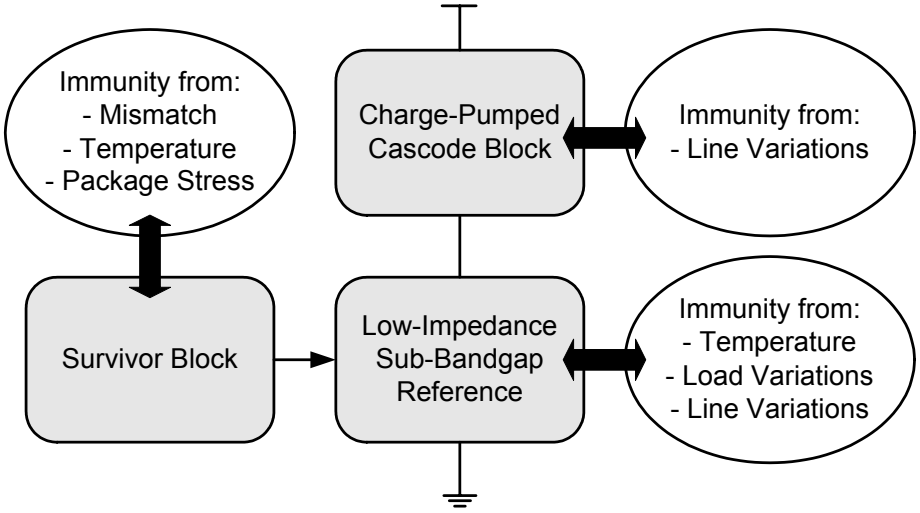


Fig. 6.1. Conceptual block diagram of the trimless reference.

6.1 Review of Proposed Techniques

The primary objective of this research is to design a highly accurate CMOS sub-bandgap reference that is immune to dc and ac process- and package-induced mismatch, temperature, load, and line variations. The target applications for this reference are modern System-on-Chip (SoC) solutions that concurrently require accuracy, low manufacturing cost, and high levels of integration, and are typically characterized by low-voltage and noisy conditions. To this end, the proposed system uses techniques that are cost-effective, noiseless, integration-oriented, and have a minimal impact on voltage headroom requirements. The proposed system consists of three primary components, as shown in Fig. 6.2.

A bandgap reference circuit adds a voltage that increases linearly with temperature to one that decreases linearly with temperature. This synthesis generates a reference voltage that is inherently temperature-independent to the first order. In the proposed bandgap reference circuit, the component of the reference voltage that increases linearly with temperature is generated through a difference in the base-emitter voltage of lateral PNP transistors that carry dissimilar current densities and form the input differential pair of operational amplifier OA_1. This voltage, when impressed upon R_{13}, is

added to voltage across R_{12}, which is a scaled version of the forward-biased voltage of diode D that decreases linearly with temperature. The result is a sub-bandgap reference voltage at V_{REF} that is compensated to the first order against temperature variations. The design of a higher order reference would be warranted only after the effects of process, package shift, line, and load variations have been accounted for, since their deleterious effects on accuracy are considerably more severe than those of temperature variations, as was discussed in Chapter 2. The effect of load variations on the accuracy of the bandgap reference is minimized using a voltage-mode approach that lowers output impedance through a feedback loop, (comprising of OA_1 and pass device MP_O) which regulates the output of the system. The reference has been designed in a standard CMOS process that incurs lower manufacturing costs than a BiCMOS process since it typically involves fewer fabrication steps.

To mitigate the effects of process- and package-induced mismatches on the initial dc accuracy of the reference, the system utilizes a technique called the Survivor strategy in which critical devices in the system are implemented using the best-matched pairs of devices chosen from a set of similar pairs during start-up. A switching network connects two pairs of devices at a time at two different positions in a comparator-based circuit. This circuit compares the matching of these pairs and its output assumes one of two possible states depending on the position occupied by the pair that exhibits lower matching, i.e., the *loser* pair. This output is subsequently processed through digital logic that controls the switching network to replace the *loser* by placing another pair in its position. This new pair is, in turn, is compared to the *winner* of the previous comparison. The digital logic thus sequentially connects each of the pairs of devices to replace the *loser* of each comparison until all the pairs have been tested. It follows that the pair that exhibits the lowest mismatch among all the tested pairs is the *winner* of the final comparison. This “survivor” pair is connected through appropriate switches to critical portions of a circuit, which is subsequently enabled. In this case, a number of NMOS

and/or PMOS transistor pairs are compared for their relative mismatch and the best-matched pairs are chosen to implement critically-matched current-sources and mirrors for the bandgap reference circuit.

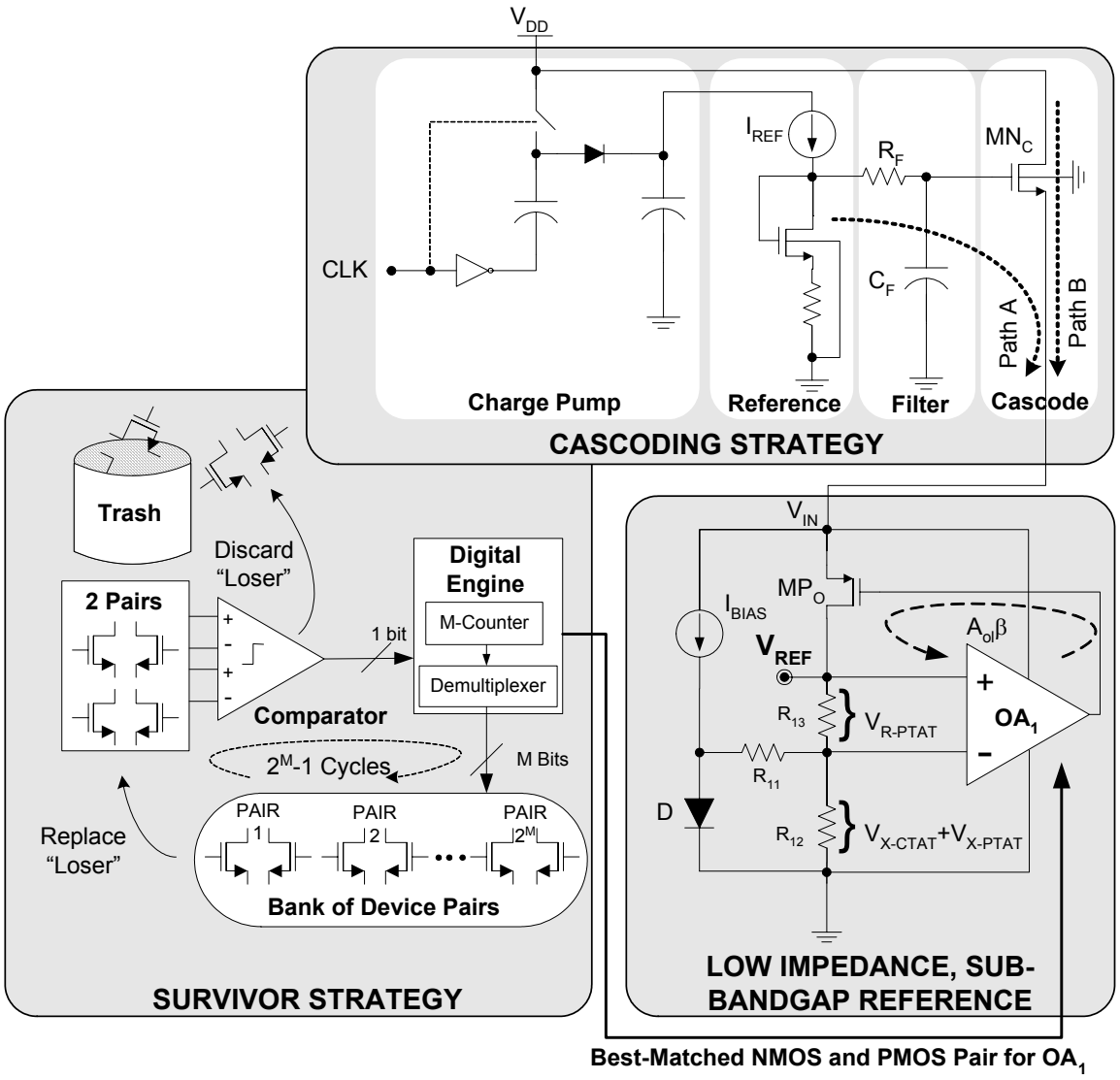


Fig. 6.2. Block diagram of system.

The most effective means of enhancing the PSRR performance of a circuit is by isolating it from the noisy power-supply. This function is performed by cascoding device MN_C in Fig. 6.2. The high channel resistance of this device is considerably effective in decoupling the system from its noisy supply. However, introducing MN_C increases the

voltage headroom required by the system because its gate voltage needs to be at least a threshold voltage above its source, which is connected to the supply of the bandgap reference. To relax this requirement, a charge pump is used to boost the voltage at the gate of MN_C to a level above that of the supply. The RC filter following the charge pump filters the systematic noise of the charge pump and, more importantly, the component of power-supply noise that is conducted through the charge pump. Since the gate of MN_C does not draw any dc current from the charge pump, resistor R_F can be very large without taking on a large voltage drop. This is advantageous because the size of R_F can now be increased, thereby decreasing the filter corner frequency to make it more effective in filtering power-supply noise, without increasing the voltage headroom required by the system.

6.2 System-Level Issues

6.2.1 Identifying Critical Pairs

The accuracy of the proposed reference hinges on the PTAT quality of OA_1's input-referred offset, which depends on resistive network R_{11}-R_{15}, input pair QP_{21}-QP_{22}, current-mirror MP_{21}-MP_{22}, and current sources MN_{21}-MN_{22}, as shown in Fig. 6.3. Resistors can be matched to 0.1% through careful layout [43], and the high β of the lateral PNPs present negligible offset currents. MOS transistors MN_{21}-MN_{22} and MP_{21}-MP_{22}, however, cannot be matched as well as resistors or bipolar transistors, and the temperature dependence of their offsets is not linear, given their square-law and therefore high dependence to threshold voltage V_T and non-linear temperature dependence of transconductance parameter K' [41]. While their matching performance can be improved by increasing their active area, this approach lowers the bandwidth of the reference by increasing the parasitic capacitances of the devices that are present in the feedback path, thereby degrading its ac accuracy against transient load and supply variations. MN_{21}-

MN_{22} and MP_{21}-MP_{22} are therefore the most critical devices in the proposed reference and shall be targeted by the Survivor strategy. The strategy circumvents the accuracy-bandwidth tradeoff by selecting the best matching pair (for high accuracy) of small-geometry devices (for high bandwidth) out of a bank of similarly sized pairs without introducing noise in the process (as DEM does).

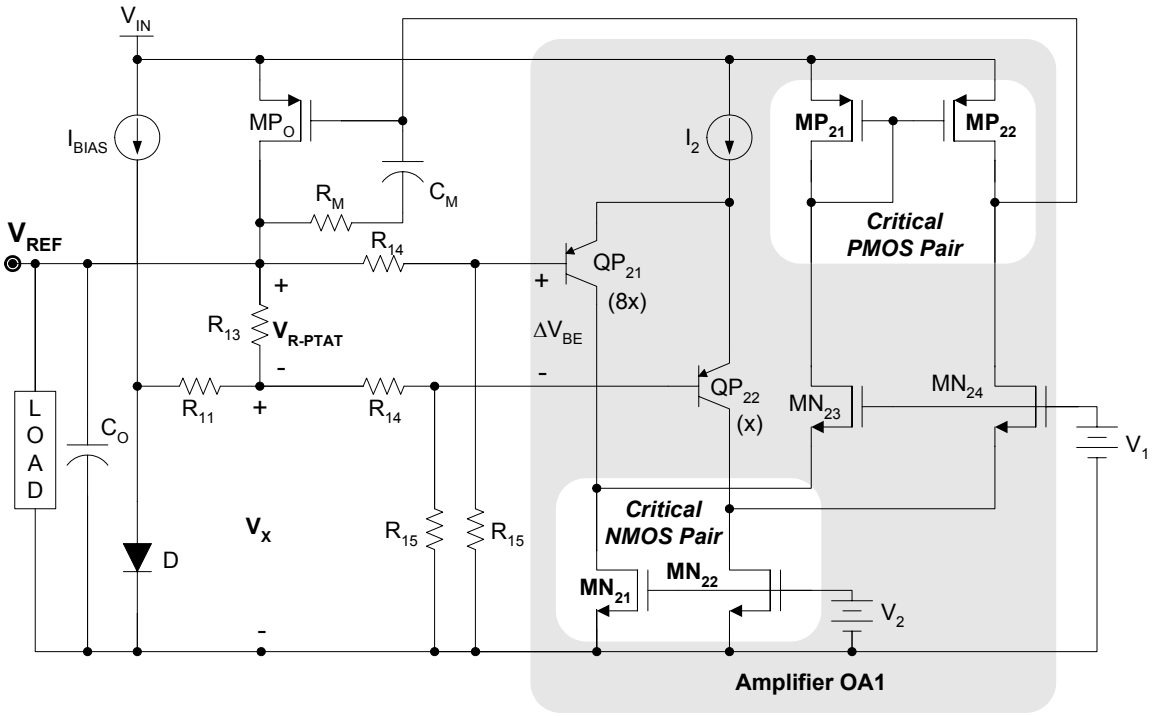


Fig. 6.3. Schematic of low-impedance reference showing critical pairs.

6.2.2 Minimum Supply Voltage

Referring to Figs. 6.2 and 6.3, the minimum supply voltage the system can sustain is dependent on the minimum voltage required by the core sub-bandgap reference, which is dependent on the output voltage and/or the feedback amplifier OA_1, and the saturation voltage across cascode NMOS MN_C, all of which simplifies to

$$V_{DD(min)} = \max\left\{V_{OUT} + V_{SD.MP_O(sat)} + V_{DS.MN_C(sat)}, V_{TP.MP_O} + 3V_{DS(sat)} + V_{DS.MN_C(sat)}\right\}. \quad (6.1)$$

More specifically, $V_{DD(min)}$ is constrained by the headroom voltages associated with MP_O's V_{SG} (i.e., $V_{T.MPo}$+$V_{SD.MPo(sat)}$) and MN_{23}'s and MN_{21}'s $V_{DS(sat)}$'s. Additionally, given

a 0-5mA load-current range, $V_{DD(min)}$ increases considerably with load current, as the saturation voltage of MP_O ($V_{SD.MPo(sat)}$) increases. $V_{DD(min)}$ is consequently lowest at light load currents and highest at maximum load currents.

The gate bias of cascoding device MN_C (output of the crude reference in Fig. 6.2) should therefore track variations in $V_{SD.MPo(sat)}$, as it changes with load current. However, conforming the design to a 5mA load while maintaining reasonable bandwidth performance (i.e., constraining the size of power PMOS MP_O) limited its minimum supply to the high-current case, which is the worst possible condition. The crude reference is therefore designed to bias MN_C under a 5mA load, yielding a minimum supply voltage of 1.8V, given a relatively high PMOS threshold voltage (V_{TP}) of 0.9V. Had the load-current requirement been alleviated to maybe 0-250μA, however, which is more compatible with standard references, and a process with a more mainstream PMOS threshold voltage (0.6V) been used, $V_{DD(min)}$ would have been constrained to 1.2V.

6.2.3 Start-up Sequence

An important advantage of the Survivor strategy is that it is operated only at start-up and/or power-on-reset events and can be disabled once the best-matched pairs have been chosen, at which point the system can resume normal operation. Utilizing this advantage requires a timing block that controls the start-up of the system and ensures that each of the three primary components of the system shown in Fig. 6.2 is enabled at an appropriate time. The start-up sequence of the system is initiated by an external enable signal. On receiving this signal, a timing block enables the Survivor strategy for choosing the best-matched NMOS and PMOS pairs for the bandgap reference. After these critical pairs are chosen and connected to the bandgap reference, the comparators in the Survivor strategy along with their DEM clock are disabled. The timing block then provides the start-up signal for the charge pump in the high PSRR cascoding strategy and the sub-bandgap reference itself. Subsequently, when the charge pump boosts the gate of the

cascode to a voltage required to support the bandgap reference, a 900mV reference voltage appears at the output of the system.

6.2.4 Testability

The system is tested in three unique modes, the Mirror mode, Bandgap mode, and System mode, each of which is used to assess important performance parameters. These modes are determined by external inputs to two pins which are subsequently decoded in a simple 2-4 decoder. The functionality of these three modes is as follows:

Mirror Mode

The functionality of the cascoding strategy and the low-impedance reference has been tested in its entirety via IC prototypes (described in Chapters 4 and 5, respectively). In the prototype IC for the Survivor strategy presented in Chapter 3, the function of the digital engine that processes the output of the comparator to connect the next pair in the device bank in the *loser's* place was implemented manually and therefore needs to be tested once it is integrated into the proposed system. This functionality is tested by operating the system in the Mirror mode, by measuring the offset of all the pairs in the PMOS bank, and subsequently verifying if the digital engine is indeed converging on the best-matched pair. In the Mirror mode, the bandgap reference and the cascoding strategy are not required and are therefore disabled.

Bandgap Mode

The improvement in accuracy performance provided by the Survivor and cascoding strategy can only be assessed by comparing the accuracy of the reference with and without these strategies in action. In the Bandgap mode, only the core bandgap reference is activated while the Survivor and cascoding strategies are disabled. The inherent initial accuracy, temperature coefficient, and PSRR performance of the bandgap reference are measured in this mode.

System Mode

In the System mode, all three system modules, i.e., the bandgap reference, Survivor strategy, and cascoding strategy are activated and the initial accuracy, temperature coefficient, and PSRR of the reference due to these techniques are measured (and subsequently compared to the inherent performance of the reference in the Bandgap mode). In the System mode, the timing block automatically activates each component of the IC, thereby verifying the start-up sequence of the proposed system. When manufactured for use in a "real-world" application, the IC is used only in the System mode.

6.3 Measurement Results

The proposed circuit was fabricated with AMI's 0.6μm-CMOS process technology ($V_{TN} \approx 0.7V$ and $|V_{TP}| \approx 0.9V$) through the MOSIS design facility. A chip photograph of the die is shown in Fig. 6.4. The chip comprises of all three primary modules of the system, namely, the low-impedance sub-bandgap reference, the Survivor strategy, and the charge-pumped cascode. The combined measurement results of 30 samples are presented in Figs. 6.5-6.11.

Overall, the circuit yielded a 3-σ untrimmed accuracy of 0.84% across -40^{o}C to 125^{o}C. Load-regulation (LDR) effects on the reference were 1.57mV/mA for a 0-5mA load, the same as that shown in Fig. 5.8. Line-regulation (LNR) effects were 0.9mV/V for a 1.8-3V supply, as shown in Fig. 6.5. The voltage droops in the reference, which were less than 8mV and 1.5mV over the entire load-current and supply voltage range on average (12mV and 2.7mV for multiple samples), respectively, were the result of finite loop gain - including these errors in the overall trimless, 3-σ dc-accuracy performance yielded 2.74%. Increasing the loop gain would decrease the effects of these variations, but at the possible cost of compromised stability.

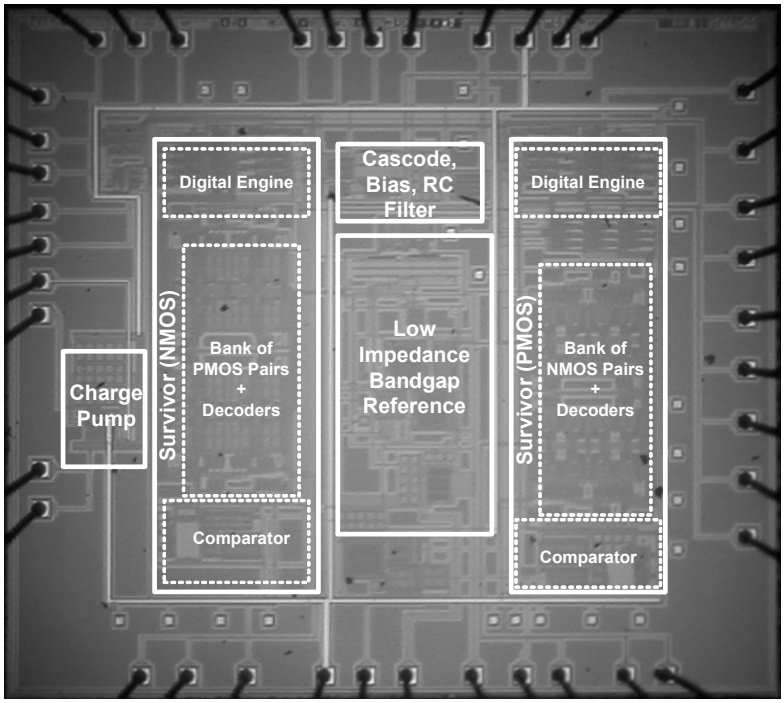


Fig. 6.4. Die photograph of system.

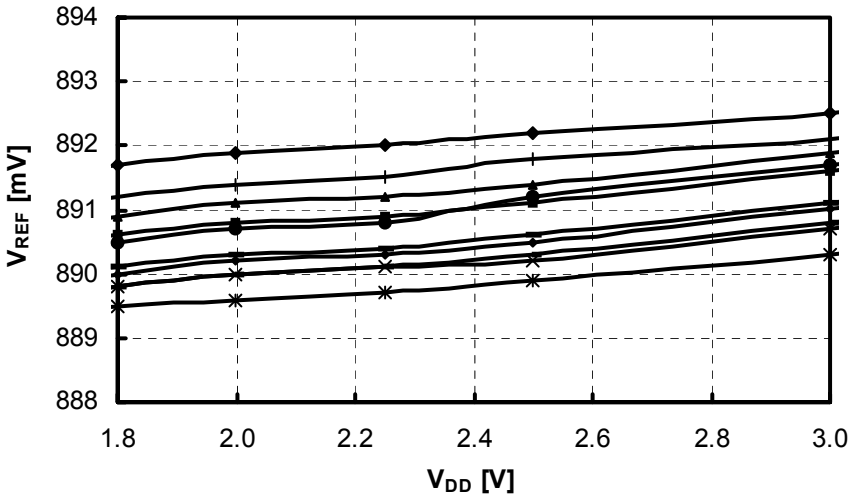


Fig. 6.5. 1.8-3V line-regulation results from 10 samples.

A key feature of this research is the Survivor strategy, which is how a 3-σ trimless accuracy of 0.84% was achieved. To verify the functionality of the strategy, that is, whether or not the circuit converged on the best matching pair of devices, the IC was operated in the Mirror mode and the PMOS pairs in the banks of five samples were tested independently, as current-mirrors, and their offset results compared against the survivor

output (i.e., identity of the surviving pair). The experimental offset measurements of one such bank of devices from a single die sample are presented in Table 6.1, showing Pair 12 as the best matching pair. Fig. 6.6 shows the experimental code progression of the Survivor circuit, which converged on Pair 12 as the surviving pair. Similarly, four other banks of devices were tested and the circuit again converged on the best matching pair. To add context to these results, the 3-σ offset performance of a single PMOS pair, when measured over 30 samples without the Survivor scheme, was 1.95% whereas the Survivor pair was 0.31% (as shown in Fig. 6.7), showing more than a 6× improvement in accuracy with the same geometry dimensions, in other words, achieving the accuracy performance of a larger device with a smaller geometry (higher bandwidth).

Table 6.1. Measured offsets of pairs in bank of devices in one sample of one lot.

Pair	Code	Offset [%]	Pair	Code	Offset [%]
0	0000	0.40	8	1000	0.36
1	0001	0.82	9	1001	0.74
2	0010	1.25	10	1010	0.38
3	0011	0.80	11	1011	1.03
4	0100	0.49	12	1100	0.04
5	0101	0.48	13	1101	0.13
6	0110	0.35	14	1110	0.78
7	0111	0.10	15	1111	0.40

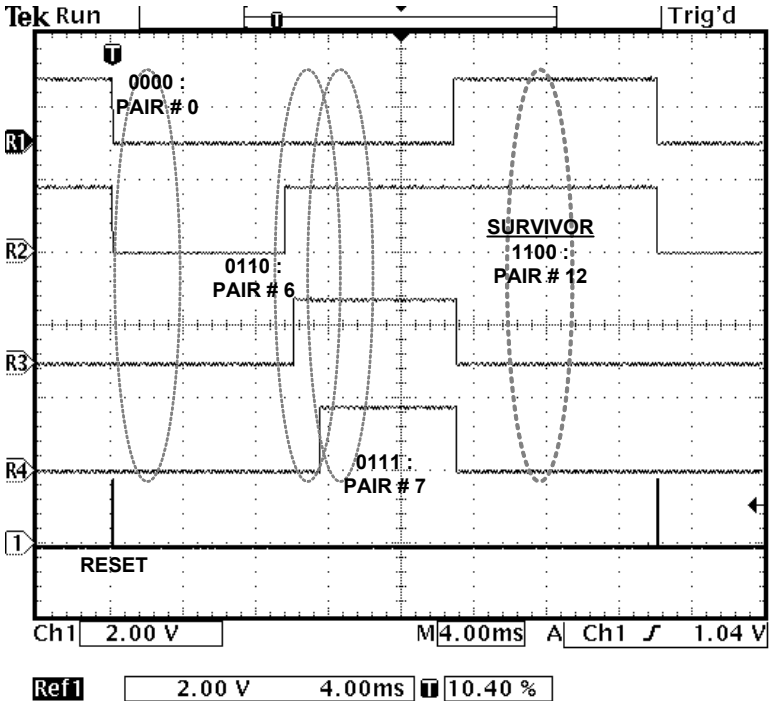
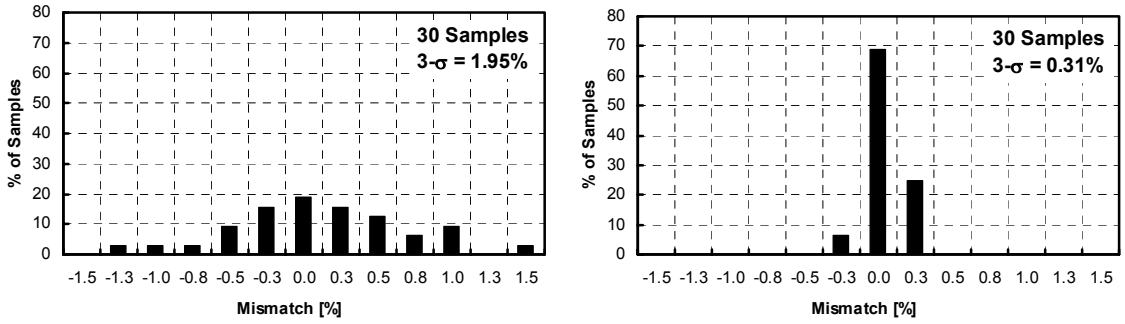


Table 6.6. Experimental results showing the digital code of the winner of each cycle with convergence to Pair 1100 (Pair 12).



(a) (b)

Fig. 6.7. Measured statistical offset performance of (a) a single PMOS pair and (b) the survivor out of 16 pairs for 30 samples.

The effectiveness of the Survivor strategy in improving the accuracy of the low-impedance, sub-bandgap reference was tested by measuring the output voltage and temperature coefficient (TC) of 30 samples of the reference before and after the application of the Survivor strategy, i.e., in the Bandgap and System mode, respectively. Fig. 6.8 shows the results of two such samples, where the temperature-induced variation over the span of -40°C to 125°C decreased by approximately 2× when applying the

Survivor scheme (from 2mV and 4mV to 0.7mV and 2.2mV, respectively). Fig. 6.9 presents the accuracy of the output voltage of the sub-bandgap reference before and after the Survivor strategy at -40°C, 25°C, and 125°C. For these temperatures, the 3-σ accuracy of the output voltage improved from 1.30% to 0.75%, 1.26% to 0.34%, and 1.12% to 0.71%, respectively. The overall spread of the reference is 14.9mV, which corresponds to ±0.84% 3-σ accuracy over temperature and process.

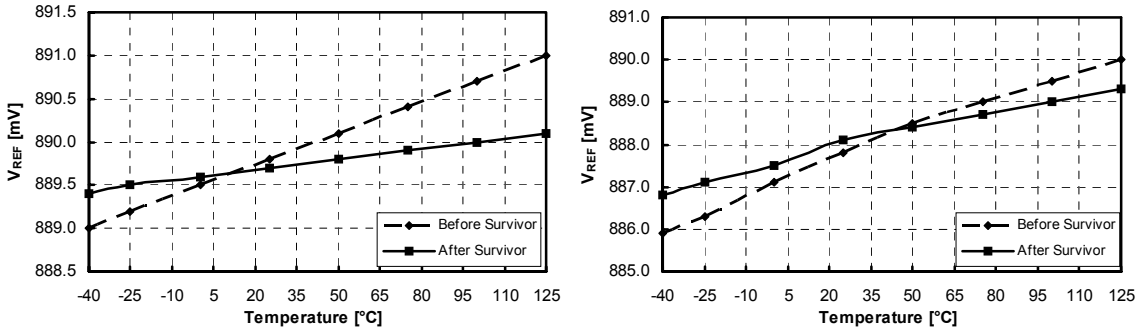


Fig. 6.8. Measured improvement in temperature coefficient of two samples due to Survivor strategy.

To verify if the Survivor strategy could viably used to design a trimless bandgap reference, the accuracy of the reference with the Survivor strategy was compared to that of the prototype IC that used 4 trim bits (described in Chapter 5). As shown in Fig. 6.9, the two approaches achieved similar dc accuracy performance: 0.75%, 0.34%, and 0.71% with the Survivor strategy and 0.67%, 0.30%, and 0.61% without it but with 4 bits of trim. The Survivor scheme, as proposed, therefore circumvents the test-time and dedicated-pin (or pad) costs normally associated with pre- and post-package trimming of bandgap references.

The techniques used in the proposed system –the Survivor strategy, charge-pumped cascode, and shunt-feedback regulation– all improve the dc and ac accuracy of the reference. The dc accuracy of the reference, in particular, is ultimately extrapolated as the linear sum of the initial 3-σ tolerance over process and temperature (ΔV_{TC}) and the average systematic load- and line-induced changes in the reference (ΔV_{LDR} and ΔV_{LDR},

respectively). The foregoing design, as noted from Figs. 5.8, 6.5, and 6.9, produced an overall 3-σ, 0-5mA, 1.8-3V trimless accuracy of 2.74%:

$$\Delta V_{REF.DC-3\sigma} = \Delta V_{TC} + \Delta V_{LDR} + \Delta V_{LNR} = 14.9\text{mV} + 8\text{mV} + 1.5\text{mV} = 24.4\text{mV} \equiv 2.74\% . \quad (6.1)$$

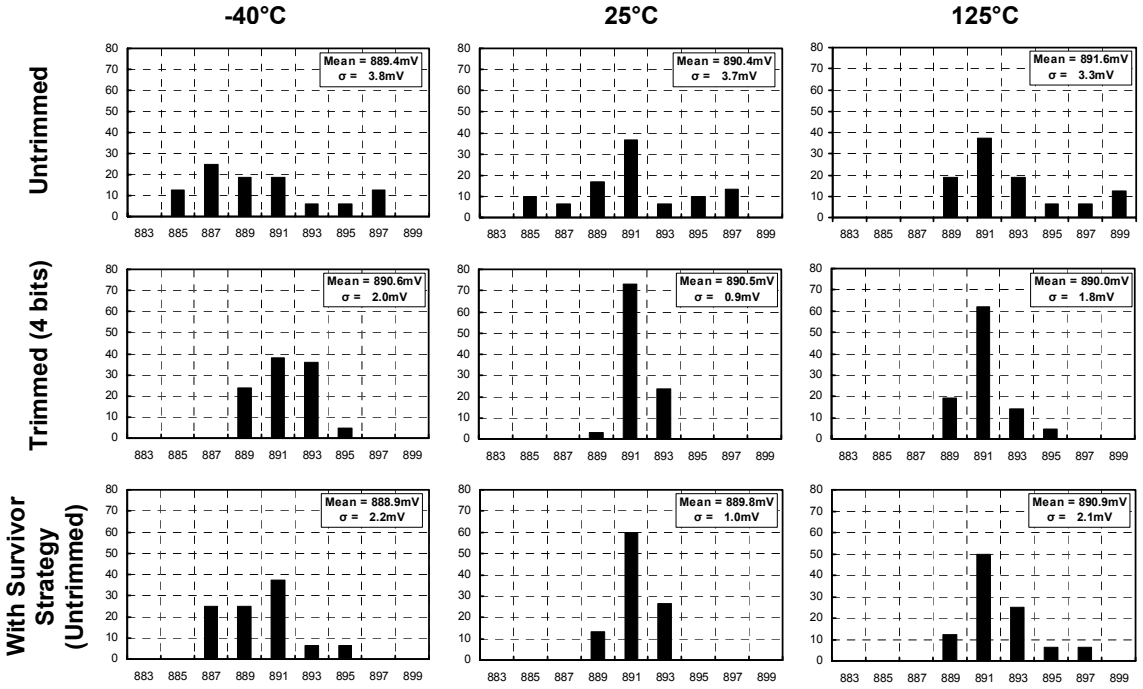


Fig. 6.9. Measured improvement in accuracy due to Survivor strategy across entire temperature range.

Another key feature of the design was its ability to reject supply ripple, i.e., ac line variations. Along with verifying the effectiveness of the Survivor strategy in improving the dc accuracy of the bandgap reference over mismatch and temperature, the performance of the cascoding strategy for improving the accuracy of the reference over line variations was also measured by operating the reference in the Bandgap and System mode. The worst-case power-supply ripple-rejection (PSRR) performance of the proposed sub-bandgap reference was -30dB, which represents a 32dB improvement over its non-cascoded counterpart, as shown in Fig. 6.10. The crude reference presented a PSRR attenuation of -20dB at dc and the series RC filter a -3dB roll-off frequency of 20kHz to the supply and charge-pump output ripple. The low-frequency ripple that ultimately reached the gate of cascoding device MN_C, which was then impressed at its

source, was attenuated by the loop gain of the shunt-feedback sub-bandgap reference, achieving an overall dc PSRR of approximately -70dB. At and past the unity-gain frequency of the reference, however, the loop gain is negligible, leaving the source-drain resistance of cascoding device MN_C ($r_{ds.MNc}$) the job of attenuating the supply ripple by -32dB, which constitutes the worst-case PSRR point (around 3.3MHz, which is the unity-gain of the reference). Beyond this point, the 10pF output capacitor presented a shunting pole, reducing the ripple at the output at 20dB per decade, as shown in the figure. In all, the PSRR performance shown was achieved with a combined on-chip capacitance of 60pF.

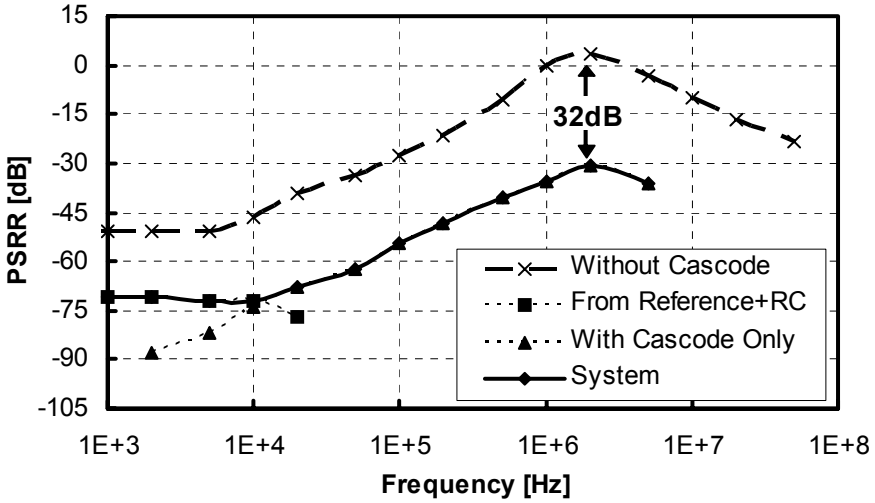


Fig. 6.10. Improvement in PSRR due to cascoding strategy.

The start-up sequence of the complete system begins with an external RESET pulse, at the onset of which the low-impedance, sub-bandgap reference and cascoding circuit are disabled and the Survivor sequence for choosing the NMOS and PMOS pairs begins. After the NMOS and PMOS survivor pairs are automatically determined, the chosen pairs are connected to the sub-bandgap reference and the DEM circuit and accompanying high-resolution comparator are disabled, at which point the reference is allowed to start. After a reset pulse, the system requires 15 comparisons to converge on

the best matching pairs, taking 1.5ms for each comparison and a total of 22.5ms for the entire start-up time, as shown in Fig. 6.11.

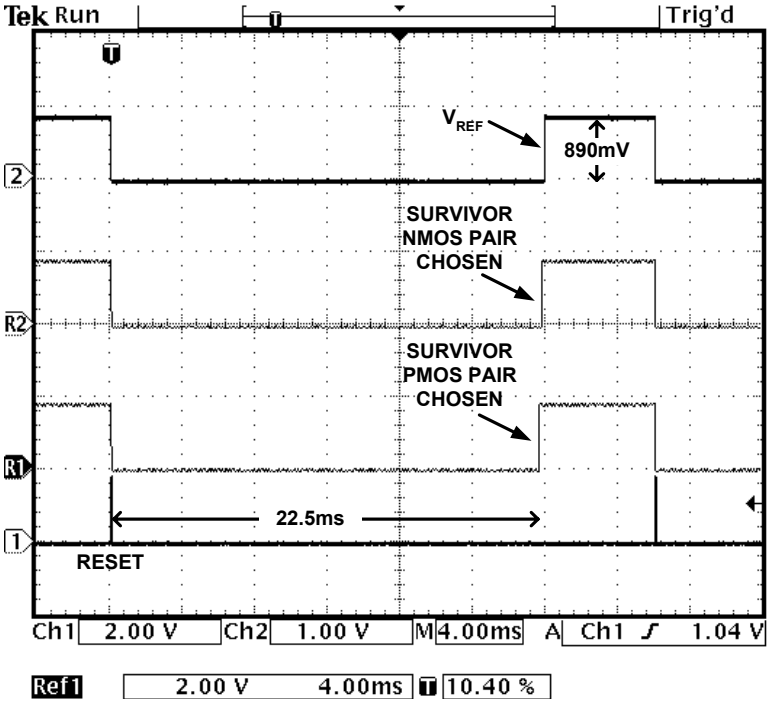


Fig. 6.11. Measurement results showing the start-up time of the Survivor and reference system.

6.4 Discussion: Impact of the Survivor Strategy

The primary trade-off of the Survivor strategy is silicon area. While the circuit improved the 3-σ matching performance of a 120/6 PMOS pair from 1.95% to 0.31% (6.3×), a bank of similar, yet unused or redundant pairs of devices were left on the silicon die. Assuming the offset performance is inversely proportional to the square root of the gate area [41]-[42], the resulting offset performance of the surviving 120/6 pair was equivalent to that of a 720/36 pair, which is $6.3^2\times$ or 40× the gate area of a 120/6 pair. To put it in perspective, as shown in Fig. 6.12, the bank of 16 120/6 pairs and the comparator and digital engine used in the survivor scheme required an area of 960,000μm^2 whereas the equivalent matching pair of 720/36 would have used 62,500μm^2, which means the survivor strategy used approximately 15× the area of a

720/36 device. While a layout area of 960,000μm^2 may seem large, it is more reasonably compared against the number of fuses or EEPROM electronics used to trim a 120/6 device to yield the matching performance of a 720/36 transistor, which is expected to yield similar tradeoffs as the Survivor strategy. Even if the proposed scheme demands more silicon real estate than trimming schemes, its resulting cost is arguably easier to absorb than the test-time costs associated with the increasingly dense CMOS ICs used to supply volume-intensive markets like the mobile business.

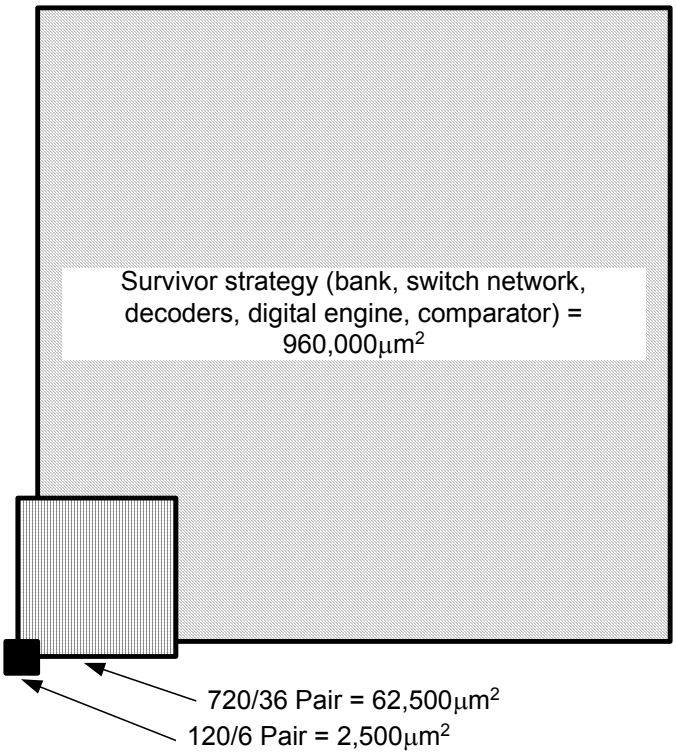


Fig. 6.12. Silicon die area comparisons of a 120/6 pair, Survivor strategy with 16 120/6 pairs and additional circuitry, and 720/36 pair (having equivalent matching performance).

The benefits of trimming and the Survivor strategy are, in the end, higher bandwidth. Increasing the size of a pair of devices from 120/6 to 720/36 to achieve better matching performance increases their respective gate-source capacitances by roughly 40×, reducing in the process their bandwidth by the same factor. The proposed Survivor scheme circumvents this tradeoff by selecting a 120/6 mirror that has the offset

performance of its 720/36 counterpart, while not resorting to trim and therefore not increasing test time. Fig. 6.13(a) shows the measured load-dump response of the proposed reference for a 0-5mA load dump with 100ns rise and fall times whereas Fig. 6.13(b), to better ascertain the effects of the proposed strategy, shows that the simulated settling time of the same reference with the 120/6 PMOS and 60/6 NMOS surviving devices is four times faster than the circuit with their 720/36 PMOS and 360/36 NMOS equivalents. Further dedicating the entire 960,000μm^2 area to a single critically-matched pair not only incurs a prolonged response time but could also compromise the stability of the circuit, since these mirrors are normally non-dominant poles in the feedback loop and adding this much capacitance may pull these poles to lower frequencies, near or below the unity-gain frequency of the reference.

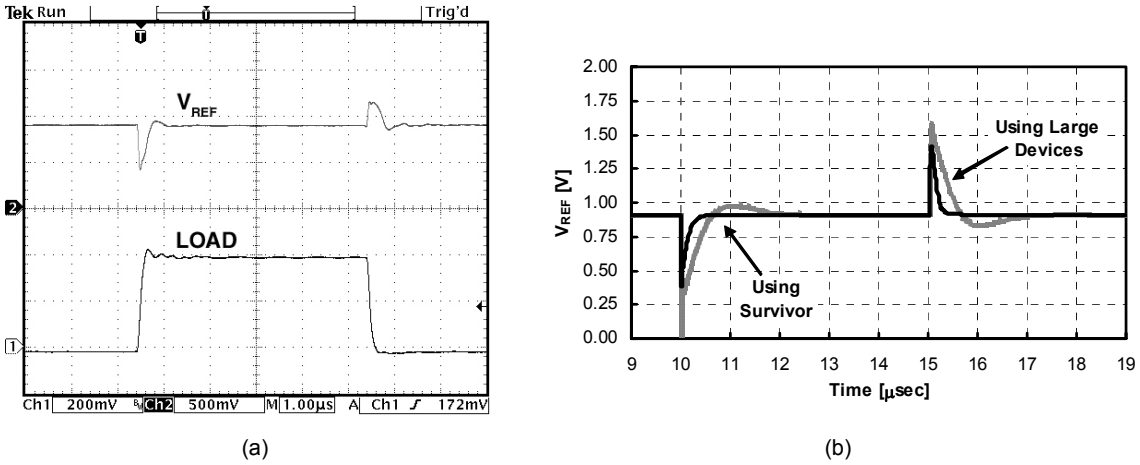


Fig. 6.13. (a) Measured transient performance of bandgap reference for 5mA load dump and (b) simulated response using large area devices and devices chosen by Survivor strategy.

6.5 Synopsis

A 0-5mA, 890mV, low-impedance, sub-bandgap 0.6μm CMOS reference with a 3-σ trimless accuracy of 0.84% across -40^{o}C to 125^{o}C (2.74% when including 0-5mA load and 1.8-3V line effects) and a worst-case power-supply ripple-rejection of -30dB for up to 50MHz was designed, fabricated, tested, and evaluated. The system is tested in

three modes: the Mirror mode, which tests the functionality of the Survivor strategy; the Bandgap mode, which measures the performance of the low-impedance, sub-bandgap reference; and the System mode, in which the improvements in the initial accuracy, temperature coefficient, and PSRR performance of the bandgap reference due to the Survivor strategy and cascoding technique are determined. The IC consists of three parts, each of which enhances the dc and ac accuracy of the overall reference. The core sub-bandgap reference can withstand 5mA of load variations while generating a reference voltage of 890mV that is accurate with respect to temperature to the first order (a higher order reference was not needed since the errors induced by temperature variations was relatively small compared to those due to other error sources). By automatically selecting best matching pairs during non-recurring start-up events, the Survivor-based reference achieves the performance of trimmed references while circumventing the test-time costs associated with trimming and the switching noise associated with dynamic-element matching (DEM). By charge-pumping the gate of an NMOS and strategically filtering the noise present at its gate, the proposed cascode circuit improved worst-case ripple-rejection by 32dB, which normally occurs around the unity-gain frequency of the reference (where the shunt-feedback benefits of the reference are non-existent) while only increasing the minimum supply voltage by a single $V_{DS(sat)}$. The combined trimless dc and ac CMOS accuracy performance of the proposed low-impedance, sub-bandgap reference, in the end, meets the stringent performance requirements and low-cost (low test-time) demands of increasingly complex system-on-chip (SoC) solutions, with its tradeoff being silicon real estate, similar to the tradeoffs of trimming and EEPROM, except no test time is required.

CHAPTER 7

CONCLUSIONS

This research has analyzed the various sources of error that impact bandgap reference circuits and developed novel strategies to overcome their debilitating effects on dc and ac accuracy. This chapter discusses the challenges that were overcome while devising these various techniques before discussing their contributions that have been made. Moreover, the effectiveness of these techniques is studied by comparing the proposed system to reported bandgap reference circuits. Finally, recommendations for future work are discussed.

7.1 Challenges

More often than not, the accuracy of a bandgap reference imposes a fundamental limit on the accuracy of the system it is used in (which may be an analog-to-digital converter, linear regulator, dc-dc converter, among a host of others). This makes it imperative to analyze the various sources of error that degrade the dc and transient, i.e. ac, accuracy of a bandgap reference with the ultimate aim of devising viable techniques to mitigate, if not eliminate, their detrimental impact. Each of these error sources affect the reference uniquely and therefore pose a variegated set of challenges towards their compensation.

Offsets imposed by process variations and package shift have a strong random component; in other words, the magnitude of the error they induce varies from one die sample to the next. This is why these errors have conventionally been reduced by trimming, which involves measuring the dc bandgap reference voltage *on each IC sample* and tweaking circuit components using on-chip fuses or EEPROM circuits till the reference voltage falls within its accuracy specification. While trimming enjoys wide

popularity because of its effectiveness, the considerable increase in test times, silicon area, and ultimately manufacturing costs it incurs has prompted designers to look into more cost-effective strategies to achieve high dc accuracy. This has led to the use of techniques like dynamic-element matching (DEM) schemes in which the effects of process- and package-induced mismatches are virtually eliminated at the circuit design level (as opposed to the manufacturing phase in the case of trimming). DEM strategies interchange the electrical positions of devices in a critical pair periodically to duplicate the same offset in both positions and thereby, effectively, cancel it. The primary drawback of DEM is the switching noise it inherently generates, because of the periodic interchange of the devices, which forces DEM schemes to use large output capacitors and ultimately operate at lower bandwidths. Self-calibration schemes, in which the system calibrates its performance at start-up, are another set of circuit techniques that have been used successfully to improve accuracy and offer a promising strategy to circumvent the costs of trimming without withstanding the noise of DEM. However, all reported self-calibrated systems require an accurate bandgap reference against which their performance is gauged. An important challenge of this research was, therefore, to develop a self-calibration strategy for the bandgap reference itself and thereby design an accurate reference that was trimless, noise-free, and high-bandwidth.

High bandwidth is crucial to the ability of a reference to maintain its ac accuracy in a noisy environment where transient fluctuations in its power-supply and load are rampant and have frequency components in the range of tens of kiloHertz to hundreds of megaHertz. These fluctuations can couple onto the output directly via parasitic capacitance or disturb internal nodes and thereby generate deviations in the reference voltage. Obviously, large capacitors offer a simple and effective solution to mitigate the effects of these noise sources. However, given the constraints on silicon area imposed by modern ICs, using large on-chip capacitors is often unviable. The situation is exacerbated by the low-voltage environments characteristic of modern systems, which make the use

of conventional cascoding techniques to achieve high power-supply ripple-rejection (PSRR) virtually impossible. This research aimed to overcome these obstacles to devise a compact, low-voltage strategy that alleviates the effects of power-supply fluctuations, i.e., achieves high PSRR performance.

Along with using large capacitors at the output, load variations can also be suppressed by lowering the output impedance of a reference using a buffer. Because the process- and package-induced offsets of the buffer add to the inherent errors of the reference and degrade dc accuracy, a more effective technique is to lower the output impedance and achieve high load regulation (LDR) performance using feedback instead. The primary challenge from this aspect, however, is to achieve low impedance and concurrently produce a sub-bandgap reference voltage, which has traditionally been generated using current-mode approaches that are not conducive to conventional shunt feedback.

A recurring theme throughout this work is the obstacles posed by modern System-on-Chip (SoC) applications, which are the ultimate target for the proposed research. Modern SoCs lower design costs by integrating different sub-systems on a single substrate to lower the bill-of-materials (BoM) while incurring low manufacturing costs by using standard CMOS processes that use fewer masking steps than their BiCMOS counterparts. Integrating different circuits implies fabricating noisy digital circuits in close proximity to noise-sensitive analog blocks, heightening the importance of achieving low output impedance and high PSRR performance for the reference. Using modern CMOS processes exacerbates the challenges to achieving high accuracy against process-variations (since MOS transistors exhibit higher mismatch than bipolar transistors) and high PSRR (since these processes typically exhibit low breakdown voltage and, consequently, require low supply voltages, making the use of conventional cascodes difficult to adopt). The cost-consciousness of SoCs also precludes the use of trimming, which is implicitly expensive since it involves testing and adjusting each die sample for

high accuracy. In light of these multitudinous challenges, this research aims to design a trimless, high PSRR, low-voltage, regulated CMOS reference IC for state-of-the-art SoC applications, in other words, a low-cost, CMOS sub-bandgap reference circuit that has high dc and ac accuracy.

7.2 Enabling Techniques

7.2.1 Survivor Strategy

The Survivor strategy is a self-calibration technique that mitigates process- and package-induced mismatch by choosing the best-matched pair from a bank of similar pairs at start-up and subsequently uses it to implement a critical pair in a circuit once the circuit resumes normal operation. The strategy compares the mismatch performance of two pairs at a time in a comparator whose output is processed by a digital engine. This digital circuit discards the pair with the higher mismatch and replaces it with another pair in the bank. The winner of the last comparison is the survivor, i.e., the pair with the best matching performance. By adopting the self-calibration approach, the high costs of trimming are entirely avoided. Moreover, since the comparator uses DEM to cancel its intrinsic offset and is disabled once the survivor is chosen, the strategy benefits from the high resolution afforded by DEM without being afflicted by its associated switching noise. Also, since the actual mismatch of the individual pairs is not being measured, the Survivor strategy can be implemented without using extensive memory banks or precision instrumentation amplifiers, which would increase die area and complexity.

Even though the Survivor strategy can, in principle, be used in any circuit that requires precisely matched pairs (the prototype was tested on a mirror, a fundamental building block), it yields additional advantages with regards to bandgap references in particular. Firstly, by choosing the best-matched MOS pair, it mitigates the effect of MOS offsets, which have a non-linear temperature coefficient (TC), on the accuracy of

the reference and improves the TC performance of the reference overall. Secondly, by effectively enhancing the mismatch performance of a pair with a given geometry to that of a larger geometry pair, the Survivor strategy increases the initial dc accuracy of the reference without hampering its bandwidth by the parasitic capacitance of large geometry devices, i.e., degrading its ac accuracy.

There are primarily two costs associated with the Survivor strategy. The first is the increase in required silicon area, needed to accommodate the digital engine, switches, and bank containing multiple device pairs. The true burden of this cost can only be assessed after the area needed by the Survivor strategy to achieve a particular dc accuracy performance is compared to the corresponding area required for trimming (fuses or EEPROM electronics) which, notably, has an added manufacturing cost of higher test time. The second limitation of the strategy, as with all self-calibration techniques, is the increase in system start-up time, needed to allow the strategy to converge on the best-matched pair in the device bank. The impact of this limitation shall need to be revisited from one application to the next – stand-alone power-supply modules that have start-up times of 15-100ms may find the Survivor strategy unacceptable while portable devices like cellular phones, which take several seconds to start, may viably withstand a 20-30ms increase in start-up time needed for self-calibration.

7.2.2 Cascoding Technique for High PSRR

The proposed cascoding technique shields the entire loading circuit, in this case, the bandgap reference, from fluctuations in the power-supply, thereby increasing its accuracy across line variations. To alleviate the required voltage headroom requirements, the cascode is biased by boosting its gate voltage above the supply using a charge pump. While the drain-source resistance of the cascode naturally shields the reference from high frequency power-supply variations, the gate-source path (which is critical since the NMOS cascode is a voltage follower for signals at its gate) is protected by an RC filter in

series with the charge pump. This RC filter shields the gate of the cascode from the systematic noise of the charge pump and random noise in the power-supply. To maximize this filter's effectiveness, its pole frequency needs to be as low as possible. In conventional topologies, this RC filter carries a dc current that constrains the size of its resistor because of the resulting voltage drop and power dissipation across it; these topologies therefore require large, area-consuming capacitors to maximize their filters' effectiveness. In the proposed topology, however, the filter is utilized in series with the gate of the cascode and therefore does not carry any dc current. Consequently, its filter pole can be minimized by increasing the resistance as much as practically possible without reducing efficiency or increasing required voltage headroom. This approach allows the proposed strategy to increase the PSRR of the reference by as much as 30dB *at the worst case* while using only 50pF of on-chip capacitance, ultimately leading to an effective high PSRR methodology that is both low-voltage and significantly compact.

The effectiveness of the charge-pumped cascode is fundamentally limited by its drain-source resistance r_{ds}, the magnitude of which ultimately determines the extent to which the loading circuit, in this case the bandgap reference, is isolated from the noisy supply. To increase r_{ds}, the cascode is operated in the saturation mode, consequently increasing the voltage headroom requirement of the system by its saturation voltage $V_{ds\text{-}sat}$ and lowering efficiency due to the inevitable power losses in r_{ds}. Moreover, r_{ds} inherently decreases as the current flowing through the cascode rises, lowering the potency of the technique. The scope of increasing the channel-length of the cascode to enhance r_{ds} is limited by the area consumed by the cascoding device, which will consequently increase to maintain the same aspect ratio.

7.2.3 Low-Impedance, Sub-Bandgap CMOS Reference

At the heart of the proposed system is a CMOS sub-bandgap voltage reference that generates a first-order temperature compensated voltage of 900mV. Unlike

conventional sub-bandgap references that require a series buffer to lower their output impedance, however, the proposed reference uses shunt feedback to regulate its output. This approach provides it the unique capability of generating a sub-bandgap reference voltage while concurrently exhibiting low output impedance. In particular, the reference can source 5mA of load current without using a series buffer that inevitably degrades the accuracy of conventional references because its intrinsic offset. The reference also leverages the potential of CMOS technologies by using parasitic lateral PNP devices, available in all standard CMOS processes, to generate the Proportional-to-Absolute Temperature (PTAT) component of the reference voltage while acting as the input differential pair of the amplifier that regulates the output.

The output stage of the proposed sub-bandgap reference is of the Class A type, in other words, it consists of a large regulated PMOS device. Therefore, even though the reference's current-sourcing ability is limited only by the size of the PMOS pass device, the current it can sink is intrinsically limited to the quiescent current of its output stage. Obviously, this current-sinking ability can be increased by increasing the bias current at the cost of higher power consumption.

7.2.4 Summary of Contributions

The primary contributions of this research lie in improving the dc and ac accuracy of bandgap reference circuits. Table 7.1 summarizes the specific contributions in these two broad categories. It is followed by the list of publication that this research has generated. Thus far, this research has generated 1 journal publication, 6 conference publications, and over 5 trade articles (trade article [4] was the seventh most-read publication in 2005 in *Power Management Design Line*). 2 more journal publications are under preparation.

Table 7.1. List of contributions.

CATEGORY	CONTRIBUTIONS
DC Accuracy	Trimless, noise-free, high-bandwidth CMOS bandgap reference.
	Quantitative analysis of process-induced error sources.
AC Accuracy	Compact, low-voltage CMOS reference with high power-supply ripple-rejection (PSRR) over wide-band frequencies.
	Low-impedance, sub-bandgap, CMOS voltage reference.
	Quantitative analysis of power-supply ripple on ac accuracy.
	Technique to improve dc accuracy (Survivor strategy) without sacrificing bandwidth, i.e., degrading ac accuracy.

Published Journal Publications

[1] V. Gupta and G. A. Rincón-Mora, "Achieving less than 2% 3-σ mismatch with minimum channel-length CMOS devices," *IEEE Trans. Circuits Sys-II.*, vol. 54, pp. 232-236, Mar. 2007.

Journal Publications under Preparation

[1] V. Gupta and G. A. Rincón-Mora, "A low-impedance sub-bandgap 0.6µm CMOS reference with 0.84% trimless 3-σ accuracy and -30dB worst-case PSRR up to 50MHz," *IEEE J. of Solid-State Circuits*, being prepared for publication.

[2] V. Gupta and G. A. Rincón-Mora, "0.9V, 34.7ppm/°C, low output impedance 0.6µm-CMOS sub-bandgap reference," *IEE Electronics Letters*, being prepared for publication.

Published Conference Publications

[1] V. Gupta and Rincón-Mora, "A 5mA 0.6µm CMOS Miller-compensated LDO regulator with -27db worst-case power-supply rejection using 60pf of on-chip capacitance," in *Digest IEEE Intl. Solid-State Circuits Conf.*, San Jose, CA, Feb. 2007, pp. 520-521.

[2] E. O. Torres, M. Chen, H. P. Forghani-Zadeh, V. Gupta, N. Keskar, L. A. Milner, H. Pan, and G. A. Rincón-Mora, "SiP integration of intelligent, adaptive, self-sustaining power management solutions for portable applications," in *Proc. IEEE Intl. Symp. Circuits Systems*, Kos, Greece, May 2006, pp. 5311-5314.

[3] V. Gupta and G. A. Rincón-Mora, "A low dropout, CMOS regulator with high PSR over wideband frequencies," in *Proc. IEEE Intl. Symp. Circuits Systems*, Kobe, Japan, May 2005, pp. 4245-4248.

[4] V. Gupta and G. A. Rincón-Mora, "Predicting and designing for the impact of process variations and mismatch on the trim range and yield of bandgap references," in *Proc. IEEE Intl. Symp. Quality Electronic Design*, Santa Clara, CA, Mar. 2005, pp. 503-508.

[5] V. Gupta and G. A. Rincón-Mora, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *Proc. IEEE SOC Conf.*, Santa Clara, CA, Sept. 2004, pp. 311-315.

[6] V. Gupta and G.A. Rincón-Mora, "Predicting the effects of error sources in bandgap reference circuits and evaluating their design implications," in *Proc. IEEE Midwest Symp. Circuits Systems,* Tulsa, OK, Aug. 2002, pp. 575-578.

Trade Articles

[1] V. Gupta and G.A. Rincón-Mora, "Bandgaps in the crosshairs: what's the trim target?" *Planet Analog*, Oct. 18, 2006.

[2] V. Gupta and G.A. Rincón-Mora, "Reduce transistor mismatch errors without costly trimming and noisy chopping schemes," *Planet Analog*, Mar. 24, 2006.

[3] G. A. Rincón-Mora and V. Gupta, "Power supply ripple rejection and linear regulators: What's all the noise about?" *Planet Analog*, Sept. 20, 2005.

[4] G. A. Rincón-Mora and V. Gupta, "Power supply ripple rejection and linear regulators: What's all the noise about?" *Power Management Design Line*, Sept. 20, 2005.

[5] V. Gupta and G. A. Rincón-Mora, "Inside the belly of the beast: A map for the wary bandgap reference designer when confronting process variations," *Power Management Design Line*, Feb. 18, 2005.

7.3 Comparison to State-of-the-Art

Table 7.2 compares the performance of the proposed circuit with other CMOS bandgap reference circuits that have been designed for high accuracy. Minimum supply voltage $V_{DD(min)}$ for the core sub-bandgap circuit at no load was 1.25V, as shown in Fig. 5.11. However, the minimum supply for the entire circuit was 1.8V because it was designed to sustain a 5mA load. Had the load-current been reduced, the circuit could have been designed to sustain a $V_{DD(min)}$ of approximately 1.4-1.5V, which when comparing it against the state-of-the-art (Table 7.2), would have been compatible with [21] and only been second to current-mode sub-bandgap topologies like in [15], both of which suffer from relatively poor ac accuracy, that is, low PSRR and low coupled-noise-shunting capabilities. As shown in Fig. 5.2, current-mode sub-bandgap references like in [15], while able to generate sub-bandgap voltages (e.g., 0.6V), cannot produce low impedance, which makes them vulnerable to load noise and incapable of sourcing any dc current. The difference in $V_{DD(min)}$ to [15], however, would have been lower had a more conventional PMOS threshold voltage been used (1.1V versus 0.95V in [15]). Even with this aside, 1.8V was still lower than the one presented in [10] (2.2V), which used an NPN emitter follower at the output to alleviate the coupled-noise sensitivity of the circuit.

The initial accuracy and TC performance of the foregoing design is nearly twice that presented in [10] (Table 7.2), but the latter was achieved with 8 trim bits, the test-time costs of which are relatively severe. The proposed circuit achieved better initial

accuracy than [21], and without the noise associated with the DEM used in [21]. [30] also used a cascoding scheme to improve PSRR, but their worst-case PSRR performance (-15dB) and associated dropout voltage (1.464V above output voltage 1.236V) were worse than in the proposed circuit (-30dB and 0.910V above output voltage 0.890V). In the 2.048V buffered bandgap reference of [39], low-power biasing resulted in a low gain-bandwidth product (80kHz), which when compared to the proposed scheme (3.3MHz), results in poorer ripple-noise immunity around the 50kHz-5MHz range. More importantly, however, the buffer used in [39] degrades the overall accuracy performance of the reference by introducing an additional error component (the input-referred offset of the buffer) that is normally non-linear with respect to temperature.

Table 7.2. Performance comparison against state-of-the-art.

Parameter	Proposed Circuit	Degrauwe [10]	Ceekala [21]	Tham [30]	Doyle [15]	Manetakis [39]
Strategies Used	a. Survivor b. Cascode c. Shunt Feedback	a. Trimming b. Shunt Feedback	DEM	Cascode	Trimming	Buffer
CMOS Technology	0.6µm	4µm	0.18µm	0.9µm	0.5µm	0.35µm
V_{REF}	0.890V	1.228V	1.225V	1.236V	0.631V	2.048V†
Initial Accuracy @ 25°C	1mV	0.15mV*	3.5mV	N/A	0.5mV	$\sqrt{1.3^2+\sigma^2_{reference}}$ mV‡
Box-Method TC	52ppm/°C	24ppm/°C*	-	-	-	-
Minimum Supply Voltage	1.80V	2.2V	≈ 1.5V**	2.7V	0.95V	2.5V†
PSRR @ 10kHz	-75dB	-30dB	-	-80dB	-	-37dB†
Worst-Case PSRR	-30dB	-	-	-15dB	-	-
Maximum load current	5mA	-	NA	NA	NA	±20mA†
Load Regulation	1.570mV/mA	3.6mV/mA	NA	NA	NA	0.010mV/mA†
Gain-Bandwidth of Loop	3.30MHz	-	NA	NA	NA	80kHz†

*8 trim bits, $^{**}V_{REF}+V_{DS(sat)}$, †Simulation results, ‡1.3mV is the error introduced by the buffer.

("NA" indicates data not applicable and "-" indicates data not available).

7.4 Conclusions and Recommendations

The techniques proposed in this research significantly reduce the dependence of modern bandgap reference circuits on expensive trimming, noisy switching techniques, and large external capacitors for achieving high accuracy and allow them to retain this accuracy while operating in low-voltage conditions and sourcing load currents. While this research has focused primarily on improving the accuracy of bandgap references, the strategies proposed can be used towards others circuits as well. For example, since the offset of a multi-stage amplifier is dominated by the mismatch in the first stage, the Survivor strategy can potentially be used to choose the best-matched devices for implementing the amplifier's input differential pair and its current-mirror. The high PSRR strategy can also be applied to linear regulators, as was demonstrated in the prototype, and holds promise to improve the PSRR performance of amplifiers and other circuits, in general. Exploring the applicability of the proposed techniques to other circuits is an interesting direction for subsequent research. At the same time, improving the implementation of the proposed strategies is also a pertinent area for future work.

The Survivor strategy is a self-calibration technique that chooses the best-matched pair for implementing the bandgap reference during start-up. In its current form, the strategy can only be used for a matching ratio of 1:1 – expanding its scope to obtain 1:N matching would be interesting. Reducing the time required by the Survivor strategy to select the best-matched pair is also important and this could be achieved by improving the delay of the comparator and/or using a random search that stops when a pair that meets the desired accuracy is found instead of sequentially searching all the pairs in the bank for the best-matched pair. A caveat is that random search will increase the complexity of the digital circuitry and switch network used and inevitably increase their area consumption and thereby lower the viability of the Survivor strategy overall. However, using of auto-routing software for these non-critical blocks should allow a

compact layout; the resulting reduction in layout overhead and area may offset the complexity introduced and needs to be explored.

The charge-pumped cascode isolates the bandgap reference from power-supply ripple through its channel resistance. In the proposed implementation, the current drawn by the loading circuit limits the effectiveness of the cascode since its channel resistance decreases with increasing current. This restricts its use to circuits with relatively low load current requirements – the bandgap reference implemented could source a maximum load current of 5mA. Modifying the strategy to enable it to support higher load currents (50 – 200mA) would broaden its scope from Point-of-Load (PoL) circuits with relatively low load current requirements to discrete regulators that need to source hundreds of mA of current.

The proposed bandgap reference exhibits low output impedance by regulating a PMOS output stage through shunt feedback – the output voltage is sensed by two lateral PNP devices that also generate the PTAT voltage for the reference. The ac accuracy of the bandgap reference could be improved and its output impedance further lowered by changing the output stage from Class A, which limits its current-sinking ability, to Class B or Class AB, which would allow it to sink and source large currents. Also, if the topology is to be used with CMOS processes in which lateral PNPs exhibit a low forward current-gain (β), the effect of base-current cancellation circuitry on the initial accuracy and temperature coefficient of the bandgap reference will need to be analyzed. Since MOS transistors do not draw any gate current, another approach to this problem would be to explore the use of MOS devices operating in the sub-threshold regime to generate the PTAT voltage instead of lateral PNPs – obviously, the higher mismatch of these MOS devices shall need to be accounted for.

7.5 Future Technical Trends

The inexorable advance towards higher levels of system integration will

inevitably increase the technical complexity of SoCs, in which analog, digital, and RF blocks will all be integrated onto the same substrate. Testing each of the individual sub-systems that comprise these "super-SoCs" to ensure they are meeting their respective specifications while reigning in test times and manufacturing costs will therefore become increasingly challenging. In this environment, integrated self-test and self-calibration strategies, like the proposed Survivor strategy, will play an important role in curbing test times and manufacturing costs. Shrinking feature sizes, with their resultant rise in digital computing power, will accelerate the adoption of these strategies by reducing their area overhead and easing the processing of their on-chip measurements. At the same time, higher switching frequencies of digital blocks, also a consequence of shrinking feature sizes, will increase the range of frequencies that noise-sensitive circuits will need protection from, making high PSRR strategies critical for noise-sensitive blocks. Finally, since standard CMOS processes, with the fewest masking steps, are the most economically viable, designing analog circuits using these "vanilla" CMOS processes while leveraging the basic devices and features they offer will become crucial to maintain lower costs. All in all, the harsh environments characteristic of SoCs will pose interesting challenges in all stages of IC development in general and analog circuit design in particular.

APPENDIX A

ERRORS DUE TO PROCESS VARIATIONS AND MISMATCH

Referring to Fig. 2.1, the base-emitter voltage of a transistor is given by

$$V_{BE} = V_T \ln\left(\frac{I_C}{J_S \cdot \text{Area}}\right), \tag{A.1}$$

where I_C and J_S are the collector current and reverse saturation current per unit area of the transistor, respectively. The PTAT current is

$$I_{PTAT} \equiv I_{C2} = \frac{V_T}{R} \ln\left(C \cdot \frac{I_{C1}}{I_{C2}}\right), \tag{A.2}$$

where C is the ratio of the areas of transistors Q_2 to Q_1, and I_{C2} and I_{C1} are their collector currents, respectively. Also, the error in V_{REF} is

$$\Delta V_{REF} = \Delta V_{BE1} + 2\Delta I_{PTAT} R_{PTAT}, \tag{A.3}$$

MOS Mismatch

A mismatch in any one of the transistors of the MOS current-mirror changes the current in all the branches of the circuit. Assuming a mismatch of δ_M in the mirror currents ($I_{C1} = (1+\delta_M)I_{C2}$) and using Eqn. (A.2), the erroneous PTAT current is

$$I_{PTAT-x} = \frac{V_T}{R} \ln\left[\frac{I_{C2}(1+\delta_M)C}{I_{C2}}\right] = \frac{V_T}{R} \ln C + \frac{V_T}{R} \ln(1+\delta_M) \approx I_{PTAT} + \frac{V_T}{R}\delta_M, \tag{A.4}$$

hence

$$\Delta I_2 = \frac{V_T}{R}\delta_M, \tag{A.5}$$

where ΔI_2 is the error in the current flowing through both branches. The current through Q_1 has a further error due to the actual mismatch of the current-mirror,

$$\Delta I_1 = I_{PTAT-x}\,\delta_M = \frac{V_T}{R} \ln[(1+\delta_M)C]\delta_M \approx \frac{V_T}{R} \ln C\left(1 + \frac{\delta_M}{\ln C}\right)\delta_M, \tag{A.6}$$

From (A.1),

$$\Delta V_{BE1} = V_T \ln\left[\frac{I_{PTAT-x}(1+\delta_M)}{I_{PTAT}}\right] = V_T \ln\left[(1+\delta_M)\frac{\ln(1+\delta_M)C}{\ln C}\right], \quad (A.7)$$

hence

$$\Delta V_{BE1} \approx V_T \delta_M \left(1+\frac{1}{\ln C}\right). \quad (A.8)$$

Consequently,

$$\Delta V_{REF} = \Delta V_{BE1} + (\Delta I_1 + 2\Delta I_2) R_{PTAT},$$

i.e.,

$$\Delta V_{REF} = V_T \delta_M \left(1+\frac{1}{\ln C}\right) + \frac{V_T}{R}\left[\ln C\left(1+\frac{\delta_M}{\ln C}\right)\delta_M + 2\delta_M\right] R_{PTAT},$$

and, therefore,

$$\Delta V_{REF} \approx V_T \frac{R_{PTAT}}{R}[2+\ln C]\delta_M. \quad (A.10)$$

Resistor Tolerance

From (A.1) and (A.2),

$$\Delta V_{BE1} = V_{BE1-x} - V_{BE1} = V_T \ln\left[\frac{R}{R(1+\delta_{RA})}\right] \approx V_T \ln(1-\delta_{RA}), \quad (A.11)$$

hence,

$$\Delta V_{REF} = \Delta V_{BE1} \approx -V_T \delta_{RA}, \quad (A.12)$$

BJT Mismatch

For a fractional error of δ_Q in the ratio of the areas of transistors Q_1 and Q_2,

$$I_{PTAT-x} = \frac{V_T}{R}\ln(C(1+\delta_Q)) = I_{PTAT} + \frac{V_T}{R}\ln(1+\delta_Q), \quad (A.13)$$

hence

$$\Delta I_{PTAT} \approx \frac{V_T}{R}\delta_Q. \quad (A.14)$$

The error in the base-emitter voltage is given by

$$\Delta V_{BE1} = V_{BE1-x} - V_{BE1} = V_T \ln\left(\frac{I_{PTAT-x}}{I_{PTAT}}\right),$$

hence

$$\Delta V_{BE1} = V_T \ln\left\{\frac{\ln[C(1+\delta_Q)]}{\ln C}\right\} \approx V_T \ln\left(1+\frac{\delta_Q}{\ln C}\right),$$

or

$$\Delta V_{BE2} \approx \frac{V_T \delta_Q}{\ln C}. \tag{A.15}$$

The error in V_{REF} is thus given by

$$\Delta V_{REF} = \frac{V_T \delta_Q}{\ln C} + 2\frac{V_T}{R} R_{PTAT} \delta_Q = \frac{1}{\ln C}(V_T + V_{PTAT})\delta_Q \approx \frac{1}{\ln C} V_{PTAT} \delta_Q . \tag{A.16}$$

APPENDIX B

REDUCING ERRORS IN FOLDED-CASCODE TOPOLOGIES

The folded topology is a well-known structure that is often used in low-voltage circuits, including amplifiers and bandgap references. Fig. B.1 presents the basic architecture of the bandgap reference under discussion, where a folded-cascode is used as a feedback error amplifier. Here, shunt feedback from the folded-cascode amplifier decreases the output impedance of the bandgap, a critical specification for load regulation and shunting noise. However, within the context of a bandgap circuit, the entire folded-cascode structure functions as the effective current-mirror of the bandgap core.

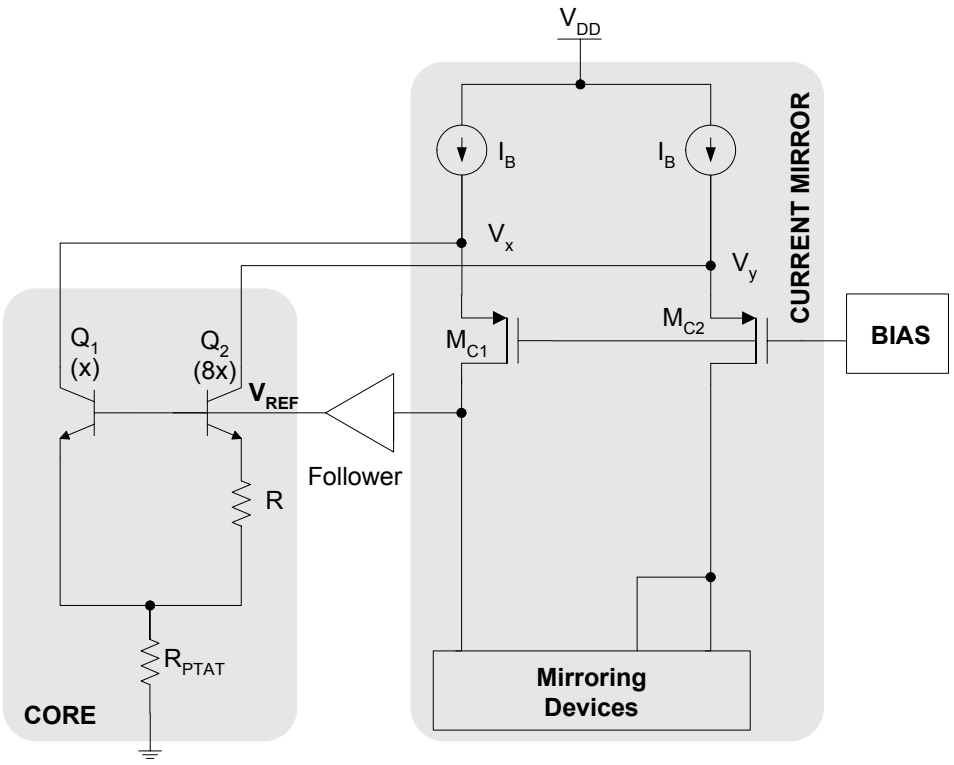


Fig. B.1. Block diagram of folded cascode bandgap reference.

Due to emitter degeneration, the transconductance of the bandgap cell (Q_1 and Q_2) is much lower than the transconductance of a conventional input differential pair. This makes the bandgap reference extremely vulnerable to current-mirror mismatch, which

produces large voltage offsets in the core. Hence, although a folded-cascode or Norton amplifier topology is well known, its design constrictions and tradeoffs differ in bandgap circuits, which are extremely sensitive to mismatch of the collector currents of the bipolar transistors (Q_1 and Q_2). In other words, the folded-cascode amplifier has to be optimized for low offsets.

B.1 Reducing Current-Mirror Mismatch

B.1.1 Proportioning the Currents

In the circuit of Fig. 2.1, if the current-mirror is simply implemented using PMOS devices connected to the supply, a mismatch in the mirror currents directly causes a mismatch in the core collector currents. Thus, to reduce current-mirror mismatch errors, a technique is needed to desensitize the mismatch in the core currents to those of the mirroring devices. In Fig. B.1, consider a mismatch in the currents through cascodes, M_{C1} and M_{C2}, which will lead to a difference in their absolute values. This difference, or surplus current, will be reflected as the difference between the currents in the core, i.e., the collector currents of Q_1 and Q_2. Now, if these core currents are higher than the currents in the cascodes, the percentage mismatch of the core currents will be lower than the percentage mismatch in the cascode currents. Further, if the core currents are raised while keeping the cascode currents constant, the same absolute (and fractional) mismatch in the cascodes will now produce an even smaller fractional mismatch in the core. Mathematically,

$$I_B = I_{MC2} + I_{C2} = I_{MC1} + I_{C1},$$

hence

$$I_{MC2} + I_{C2} = I_{MC2}(1+\delta_{MIRROR}) + I_{C2}(1-\delta_M),$$

and therefore

$$\delta_M = \delta_{MIRROR} \frac{I_{MC2}}{I_{C2}} = \delta_{MIRROR} K_I , \tag{B.1}$$

where δ_M and δ_{MIRROR} are the fractional mismatches in the currents in the core bipolar devices and the mirror cascodes, respectively, and K_I is the ratio of the current in the cascode to that in the core. Thus, by lowering the ratio K_I, the same fractional mismatch between the currents in the cascodes (and hence the mirroring devices), δ_{MIRROR}, produces a smaller mismatch in the core, δ_M. Hence, through a folded topology, the mismatch between the current-mirror devices is effectively *attenuated*.

The benefits of the folded topology, and hence of Eqn. (B.1), have costs and limits. Note that current-mirror mismatch in the circuit of Fig. B.1 stems from a mismatch in three pairs of devices, namely, mismatch in the I_B-current sources (ΔV_{REF-IB}), V_T mismatch between the cascoding devices M_{C1} and M_{C2} (ΔV_{REF-VT}), and mismatch in defining mirroring devices themselves ($\Delta V_{REF-MIR}$). It is reasonable to expect the total current-mirror mismatch error to approximately equal the root sum squared (RSS) of these individual random errors, i.e.,

$$\Delta V_{REF} \approx \sqrt{(\Delta V_{REF-IB})^2 + (\Delta V_{REF-VT})^2 + (\Delta V_{REF-MIR})^2} . \tag{B.2}$$

Thus, a reduction in the error predicted by Eqn. (B.1) would only prove effective if mismatch error of the mirroring devices is dominant. Fig. B.2 shows how the total induced error decreases with the ratio K_I. The error reduces proportionally till it reaches the "floor" set by V_T mismatch errors.

Further, the cascodes and mirroring devices form a high-gain amplifier that equalizes the collector voltages of the bipolars through feedback. Hence, decreasing the cascode current to very low levels would decrease finite gain errors caused by this amplifier by increasing the loop gain, but would also increase δ_{MIRROR} and the V_T mismatch Thus, in order to obtain the attenuation predicted by Eqn. (B.1), a sufficiently high current in the cascode would be required, with a correspondingly larger current in the core, leading to the tradeoff of larger power dissipation for improved accuracy.

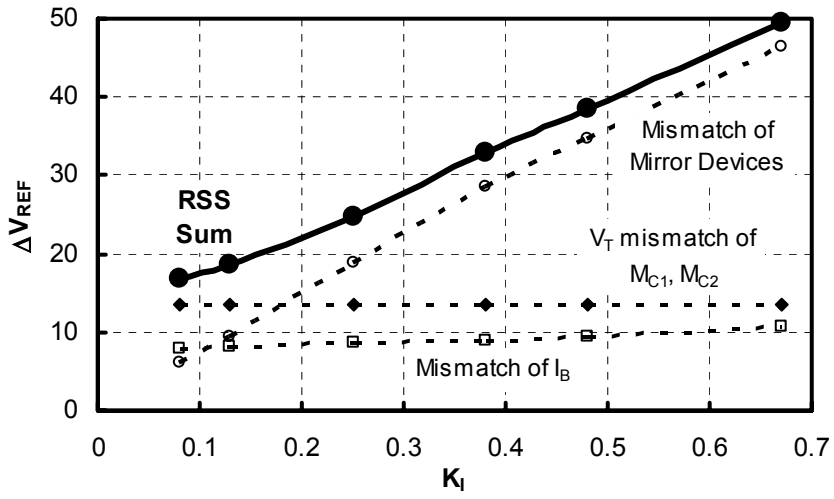


Fig. B.2. Current-mirror mismatch error and its relation to the ratio of the current in the cascode to the core (K_I).

B.1.2 Implementing the Current Sources and Current-Mirror

The I_B-current sources in Fig. B.1 play a crucial role in the bandgap reference. The devices used to implement these sources should be extremely well matched to reduce current-mirror mismatch errors. A mismatch in these devices can decrease the effectiveness of folding the currents (shown in Eqn. (B.1)) and can also cause its own current-mirror mismatch, even if the cascodes and mirroring devices are well matched. On the other hand, increasing the output resistance of these current sources reduces the sensitivity of the bandgap core to V_T and K' mismatches of cascoding devices M_{C1} and M_{C2} (a higher output resistance increases the source-degenerating effects on M_{C1} and M_{C2}).

Resistors often exhibit superior matching properties to MOS devices [43]. The latter, however, have higher output resistance. Thus, a delicate tradeoff exists in the design of the I_B-current sources, and the designer must therefore ascertain how these devices will match before making a design decision. For example, consider a 300 mV voltage drop across the I_B-current sources, a 1% resistor mismatch (R_{mis}), 2% transconductance parameter mismatch (K'_{mis}), 2% W/L mismatch (W/L_{mis}), and a 10 mV

threshold voltage mismatch ($V_{T\text{-}mis}$). The current through the I_B-current sources implemented as resistors would depend on the magnitude of their resistance and the voltage across them. Hence, the mismatch between the I_B-current sources if they are implemented as resistors, ($I_{B\text{-}mis\text{-}R}$), would be a root sum squared (RSS) of the random mismatch in the resistor values and of the voltage across them. Thus,

$$I_{B-mis-R} \approx \sqrt{(R_{mis})^2 + (V_{T-mis})^2} = \sqrt{(1\%)^2 + \left(\frac{10}{300}\times 100\right)^2} \approx 3\%. \qquad \text{(B.3)}$$

Assuming MOS devices, the mismatch ($I_{B\text{-}mis\text{-}MOS}$) is given by the RSS of the mismatch between transconductance parameter, K', W/L ratio, and threshold voltage, V_T. Hence,

$$I_{B-mis-MOS} \approx \sqrt{(K'_{mis})^2 + (W/L_{mis})^2 + (2V_{T-mis})^2}$$

$$\approx \sqrt{(2\%)^2 + (2\%)^2 + \left(2\times\frac{10}{300}\times 100\right)^2} \approx 6\%. \qquad \text{(B.4)}$$

The overdrive voltage can be increased to attenuate the effect of V_T mismatch [41], at the cost of voltage headroom and current consumption. The factor of "2" arises for the V_T mismatch term because it is assumed that the MOS devices used to implement the current sources are operating in the saturation regime, where the drain current is proportional to the square of the overdrive voltage, or difference between the gate-source and threshold voltage. Intuitively, this can be seen by viewing the square overdrive term as two terms, each depending on V_T, and thereby doubling its mismatch effect.

Mismatches due to lambda effects and other MOS parameters (that have been ignored in (41)) further degrade the matching performance of these devices. Consequently, resistors would be a better design choice in implementing the I_B-current sources (balancing matching versus source-degenerating performance). Ultimately, mismatches between the I_B-current sources can be notably reduced through the use of dynamic-element matching (DEM) techniques [21]-[23], which have an implied cost of higher noise. This would significantly reduce the $\Delta V_{REF\text{-}IB}$ and $\Delta V_{REF\text{-}VT}$ terms in Eqn.

(B.2). The implementation of the current-mirror itself is critical and careful attention must be paid to its accurate and robust implementation. The designer must ascertain the best-matched devices available, in a manner similar to the procedure for choosing the I_B-current sources.

B.1.3 Practical Topology

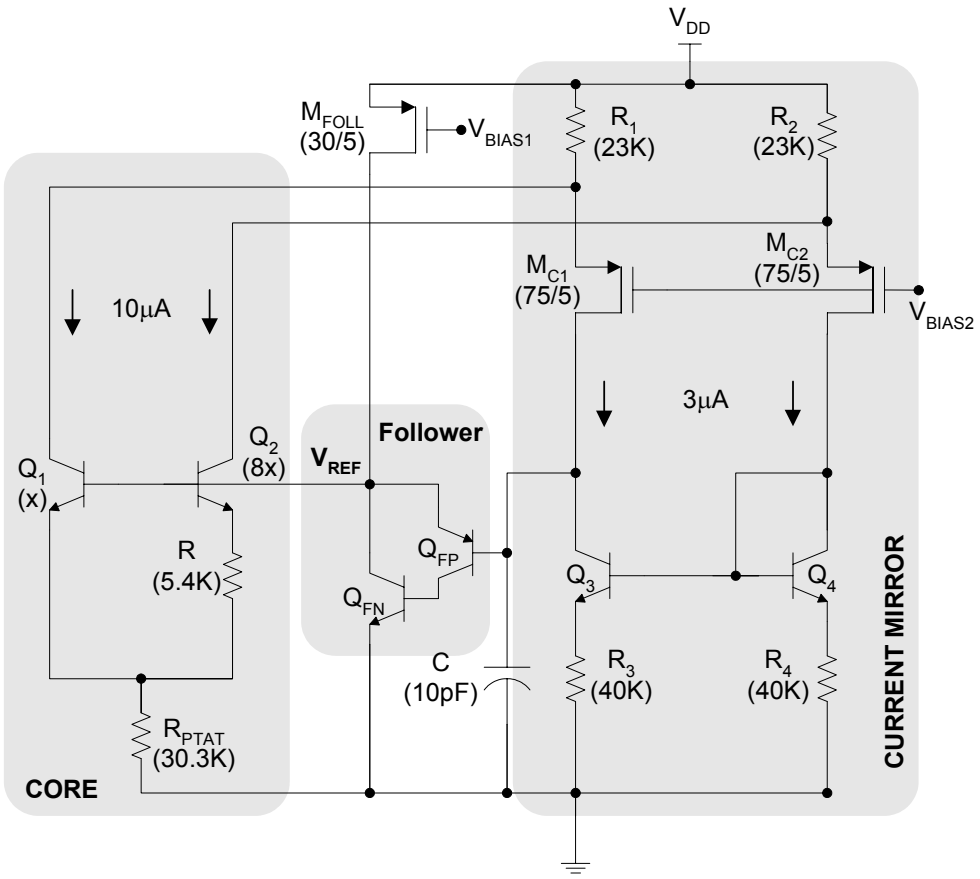


Fig. B.3. Circuit embodiment of a high-accuracy bandgap reference.

Fig. B.3 presents the complete schematic of the proposed bandgap reference. High-β NPN devices, Q_3 and Q_4, along with their degenerating resistors, R_3 and R_4, form a well-matched, high output impedance current-mirror. Transistors Q_{FN} and Q_{FP} create a super-beta voltage follower, i.e., unity-gain buffer which is used to close the feedback loop and prevent the bandgap core from loading the current-mirror. Transistor M_{FOLL}

provides the bias current for the super-β buffer. Finally, capacitor C establishes the dominant pole and hence the loop bandwidth of the circuit. Table B.1 presents the simulated functional specifications of the circuit. Standard models compatible with 1.5μm process obtained from MOSIS were used for the simulations.

Table B.1. Simulated circuit characteristics of folded cascode bandgap reference.

Circuit Parameter	**Simulated Value**
V_{REF} (T = 27°C)	1.23 V
Minimum supply voltage	1.41 V
TC performance (after trim)	0.34 %
Quiescent Current	60 μA
Line regulation	1.27 mV/V
Power-Supply Ripple Rejection (f = 100 Hz)	-55 dB

APPENDIX C

DETERMINING THE MAGIC VOLTAGE

Theoretically, trimming to the magic voltage produces the concave shape of V_{REF} shown in Fig. 1.1, where the minimum voltage occurs at both the low and high temperature extremes and the mid-point exhibits a zero temperature coefficient (TC). The curvature is generated because of the non-linear temperature dependence of the base-emitter voltage. The PTAT component of the reference voltage, however, is not plagued by these non-idealities, in other words, it is virtually free of second-and higher-order temperature dependence and can therefore be used conveniently to trim the voltage reference. Consequently, a bandgap reference is tuned or trimmed by varying the PTAT voltage, which is designed to vary linearly with the trim code.

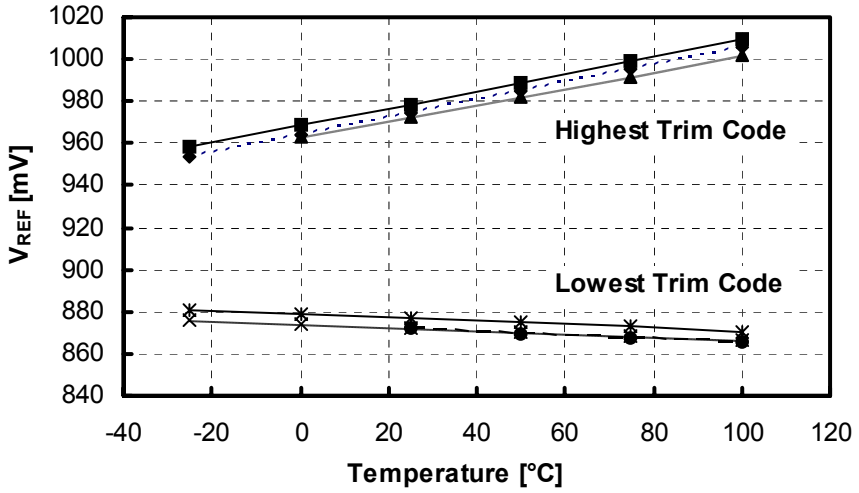


Fig. C.1. Six samples of V_{REF} at trim-code extremes.

The voltage that exhibits the lowest TC, or the magic voltage, is determined by measuring the TC of various samples at the maximum and minimum trim codes (Fig. C.1) and subsequently extrapolating the zero TC point from the least-square-fit line (Fig. C.2), which in the case of the foregoing prototype, was 890.5mV. It must be noted that

the magic voltage was determined using a total of 6 data points from 6 different samples. In other words, since increasing the number of samples increases the statistical confidence of the magic voltage, the three low temperature data points are not derived from the same devices that produce the three high temperature data points.

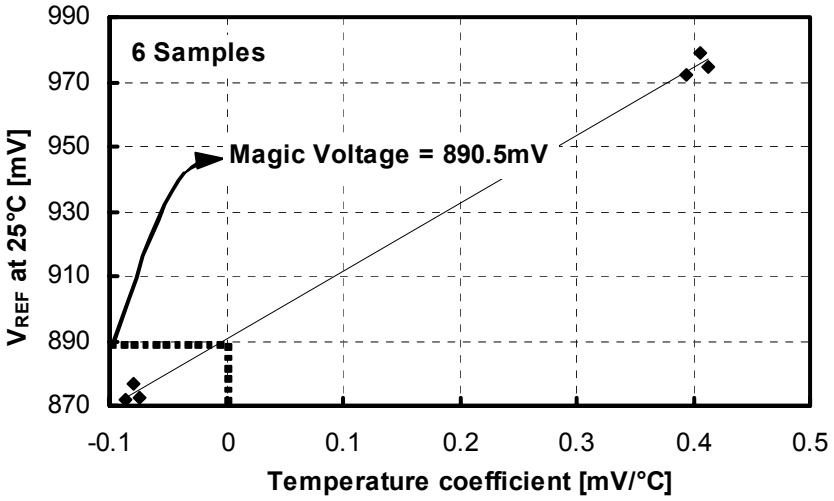


Fig. C.2. Extrapolating the magic voltage from measured TC data of the reference at room temperature for trim code extremes.

REFERENCES

[1] C. Lee, K. McClellan, and J. Choma Jr., "A supply-noise-insensitive CMOS PLL with a voltage regulator using dc-dc capacitive converter," *IEEE J. of Solid-State Circuits*, vol. 36, pp. 1453-1463, Oct. 2001.

[2] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Oxford Univ. Press, 2002, ISBN: 0195116445.

[3] Dallas Semiconductor/Maxim, Appl. Note 754, "Selecting the right series voltage reference for absolute-accuracy voltage-output DAC designs" [Online] Available: http://www.maxim-ic.com/appnotes.cfm/appnote_number/754 (Date accessed: Apr. 2007).

[4] R. J. Widlar, "New developments in IC voltage regulators," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 2-7, Feb. 1971.

[5] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 388-393, Dec. 1974.

[6] G. A. Rincón-Mora, *Voltage References – From Diodes to Precision High-Order Bandgap Circuits*, IEEE Press, John Wiley & Sons, Inc., 2002, ISBN: 0471143367.

[7] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," IEEE J. Solid-State Circuits, vol. 3, pp. 365-373, Dec. 1968.

[8] K. E. Kuijk, "A precision reference voltage source," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 2-7, June 1973.

[9] C. Avoinne, T. Rashid, V. Chowdhury, W. Rahajandraïbe and C. Dufaza, "Second-order compensated bandgap reference with convex correction," *IEE Electronics Letters*, vol. 41, pp. 276-277, 3 Mar. 2005.

[10] M. G. R. Degrauwe, O. N. Leuthold, E. A. Vittoz, H. J. Oguey, and A. Descombes, "CMOS voltage references using lateral bipolar transistors," *IEEE J. Solid-State Circuits*, vol. 6, pp. 1151-1157, Dec. 1985.

[11] I. M. Filanovsky and Y. F. Chan, "BiCMOS cascaded bandgap voltage reference," in *Proc. IEEE Midwest Symp. Circuits Systems*, Ames, IA, Aug. 1996, pp. 943-946.

[12] M. M. Martins and J. A. S. Dias, "CMOS shunt regulator with bandgap reference for automotive environment," *IEE Proc., Circuits Devices Systems*, vol. 141, pp. 157-161, June 1994.

[13] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference with sub-1-V operation," *IEEE J. Solid-State Circuits,* vol. 34, pp. 670-674, May 1999.

[14] K. N. Leung and P. K. T. Mok, "A sub-1V 15ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits,* vol. 37, pp. 526-530, April. 2002.

[15] J. Doyle, Y. J. Lee, Y. Kim, H. Wilsch, and F. Lombardi "A CMOS subbandgap reference circuit with 1-V power supply voltage," *IEEE J. Solid-State Circuits,* vol. 39, pp. 252-255, Jan. 2004.

[16] R. Tummala, *Fundamentals of Microsystems Packaging,* New York, NY: McGraw-Hill, 2002, ISBN: 0071371699.

[17] S. Bruederle (2002, Nov. 04), "System on Chip: Driver of next generation wireless growth." [Online] Available: http://www3.gartner.com/pages/story.php.id.2916.s.8.jsp (Date accessed: Apr. 2007).

[18] C.C. Chen and C. Cheng, "Future SOC design challenges and solutions," in *Proc. IEEE Intl. Symp.Quality Electronic Design,* San Jose, CA, Mar. 2002, pp. 534-537.

[19] W. Krenik, D. D. Buss, P. Rickert, "Cellular handset integration – SIP versus SOC," *IEEE Jour. of Solid-State Circuits*, vol. 40, pp. 1839-1846, Sept. 2005.

[20] B. S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE J. Solid-State Circuits,* vol. SC-18, pp. 634-643, Dec. 1983.

[21] V. G. Ceekala, L. D. Lewicki, J. B. Wieser, D. Varadarajan, and J. Mohan, "A method for reducing the effects of random mismatch in CMOS bandgap references," in *Digest IEEE Intl. Solid-State Circuits Conf.*, San Jose, CA, Feb. 2002, pp. 318-319.

[22] M. A. T. Sanduleanu, A. J. M. van Tuijl, and R. F. Wassenaar, "Accurate low power bandgap voltage reference in 0.5μm CMOS technology," *IEE Electronics Letters,* vol. 34, pp. 1025-1026, 14th May 1998.

[23] A. Bakker, "CMOS smart temperature sensors – An overview," in *Proc. IEEE Sensors,* Orlando, FL, June 2002, pp. 1423-1427.

[24] Dallas Semiconductor/Maxim, Appl. Note 898, "Selecting LDO linear regulators for cellphone designs." [Online] Available: http://www.maxim-ic.com/appnotes.cfm/appnote_number/898 (Date accessed: Apr. 2007).

[25] Dallas Semiconductor/Maxim, Appl. Note 883, "Improved power supply rejection for IC linear regulators." [Online] Available: http://www.maxim-ic.com/appnotes.cfm/appnote_number/883 (Date accessed: Apr. 2007).

[26] L. R. Zheng, B. X. Li, and H. Tenhunen, "Efficient and accurate modeling of power supply noise on distributed on-chip power networks," in *Proc. IEEE Intl. Symp. Circuits Systems*, Geneva, Switzerland, May 2000, pp. 513-516.

[27] S. Zhao and K. Roy, "Estimation of switching noise on power supply lines in deep sub-micron CMOS circuits," in *Proc. 13th Intl. Conf. VLSI Design,* Calcutta, India, Jan. 2000, pp. 168-173.

[28] P. Larsson, "Power supply noise in future ICs: A crystal ball reading," in *Proc. IEEE Custom Integrated Circuits Conf.,* San Diego, CA, May 1999, pp. 467-472.

[29] J. M. Ingino and V.R. von Kaenel, "A 4-GHz clock system for a high-performance system-on-a-chip design," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1693-1698, Nov. 2001.

[30] K. Tham and K. Nagaraj, "A low-voltage high PSRR voltage reference in CMOS process," *IEEE J. Solid-State Circuits*, vol. 5, pp. 586-590, May 1995.

[31] G. Giustolisi and G. Palumbo, "A detailed analysis of power-supply noise attenuation in bandgap voltage references," *IEEE Trans. Circuits Sys.- I*, vol. 50, pp. 185-197, Feb. 2003.

[32] S. Mehrmanesh, M. B. Vahidfar, H. A. Aslanzadeh, and M. Atarodi, "A 1-volt, high PSRR, CMOS bandgap voltage reference," in *Proc. IEEE Intl. Symp. Circuits Systems*, Bangkok, Thailand, May 2003, pp. 381-384.

[33] H. Yamu, and M. Sawan, "A 900mV 25μW high PSRR CMOS voltage reference dedicated to implantable micro-devices," in *Proc. IEEE Intl. Symp. Circuits Systems*, Bangkok, Thailand, May 2003, pp. 373-376.

[34] M. Ozbas, D. Patru, and P.R. Mukund, "Power supply noise coupling in a standard voltage reference circuit," in *Proc. IEEE SOC Conf.,* Portland, OR, Sept. 2003, pp. 319-322.

[35] V. Gupta and G.A. Rincón-Mora, "Predicting the effects of error sources in bandgap reference circuits and evaluating their design implications," in *Proc. IEEE Midwest Symp. Circuits Systems,* Tulsa, OK, Aug. 2002, pp. 575-578.

[36] F. Fruett, G.C.M. Meijer, and A. Bakker, "Minimization of the mechanical-stress-induced inaccuracy in bandgap voltage references," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1288-1291, July 2003.

[37] B. Abesinga, G.A. Rincón-Mora, and D. Briggs, "Voltage shift in plastic-packaged bandgap references," *IEEE Trans. Circuits Sys – II*, vol. 49, pp. 681-685, Oct. 2002.

[38] D. Spady and V. Ivanov, "A CMOS bandgap voltage reference with absolute value and temperature drift trims," in *Proc. IEEE Intl. Symp. Circuits Systems*, Kobe, Japan, May 2005, pp. 3853-3856.

[39] K. Manetakis, "CMOS micro-power output stage for integrated voltage references," *IEE Electronics Letters*, vol. 40, pp. 917-918, 22 July 2004.

[40] M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature-corrected low-voltage bandgap reference," *IEEE J. Solid-State Circuits*, vol. 28, pp. 667-670, June 1993.

[41] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog* Integrated Circuits, John Wiley & Sons, ISBN: 0471321680.

[42] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits,* vol. 24, pp. 1433-1440, Oct. 1989.

[43] A. Hastings, *The Art of Analog Layout*, Prentice Hall, 2000, ISBN: 0130870617.

[44] J. J. Wortman, J. R. Hauser, and R. M. Burger, "Effects of mechanical stress on p-n junction device characteristics," *J. Appl. Physics*, vol. 35, pp. 2122-2130, 1964.

[45] R. C. Jaeger, J. C. Suhling, R. Ramani, A. T. Bradley, and X. Jianping, "CMOS stress sensors in <100> silicon," *IEEE J. of Solid-State Circuits*, vol. 35, pp. 85-95, Jan. 2000.

[46] R. C. Jaeger, R. Ramani, and J. C. Suhling, "Effect of stress-induced mismatches in CMOS analog circuits," in *Proc. VLSI Tech., Systems, and Applications,* Taipei, pp. 354-360, May 1995.

[47] AD780 datasheet, Analog Devices, "2.5V/3.0V High precision reference," [Online] Available: http://www.analog.com/UploadedFiles/Data_Sheets/87683462AD780_e.pdf (Date accessed: Apr. 2007).

[48] ADR420 datasheet, Analog Devices, "Ultraprecision, low noise, 2.048 V/2.500 V/3.00 V/5.00 V XFET ® voltage references," [Online] Available: http://www.analog.com/UploadedFiles/Data_Sheets/164129577ADR420_1_3_5_g.pdf (Date accessed: Apr. 2007).

[49] REF2912 datasheet, Texas Instruments, "100ppm/°C, 50μA in SOT23-3 CMOS voltage reference," [Online] Available: http://focus.ti.com/lit/ds/symlink/ref2912.pdf (Date accessed: Apr. 2007).

[50] REF3020 datasheet, Texas Instruments, "50ppm/°C max, 50μA in SOT23-3 CMOS voltage reference," [Online] Available: http://focus.ti.com/lit/ds/symlink/ref3020.pdf (Date accessed: Apr. 2007).

[51] LM4120 datasheet, National Semiconductor, "Precision micropower low dropout voltage reference," [Online] Available: http://www.national.com/ds/LM/LM4120.pdf (Date accessed: Apr. 2007).

[52] M. S. J. Steyaert and W. M. C. Sansen, "Power supply rejection ratio in operational transconductance amplifiers," *IEEE Trans. Circuits Sys.*, vol. 37, pp. 1077-1084, Sept. 1990.

[53] E. Säckinger, J. Goette, and W. Guggenbűl, "A general relationship between amplifier parameters, and its application to PSRR improvement," *IEEE Trans. Circuits Sys.*, vol. 38, pp. 1173-1181, Oct. 1991.

[54] D.B. Ribner and M. A. Copeland, "Design techniques for cascoded CMOS op amps with improved PSRR and common-mode input range," *IEEE J. of Solid-State Circuits*, vol. 6, pp. 919-925, Dec. 1984.

[55] V. Gupta and G. A. Rincón-Mora, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *Proc. IEEE SOC Conf.*, Santa Clara, CA, Sept. 2004, pp. 311-315.

[56] Dallas Semiconductor/Maxim, Appl. Note 672, "Power supplies for Pentium, Power PC, and beyond." [Online] Available: http://www.maxim-ic.com/appnotes.cfm/appnote_number/672 (Date accessed: Apr. 2007).

[57] C. Toumazou, F. J. Lidgey and D. G. Haigh (Editors), *Analogue IC Design: The Current-Mode Approach*, Peter Peregrinus Ltd., ISBN: 0863412971.

[58] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE J. of Solid-State Circuits*, vol. 35, pp. 1877-1883, Jan. 2000.

[59] V. Gupta and G. A. Rincón-Mora, "Achieving less than 2% 3-σ mismatch with minimum channel-length CMOS devices," *IEEE Trans. Circuits Sys-II.*, vol. 54, pp. 232-236, Mar. 2007.

[60] T. Das, A. Gopalan, C. Washburn, and P. R. Mukund, "Self-calibration of input-match in RF front-end circuitry," *IEEE Trans. on Circuits and Systems II*, vol. 52, pp. 821-825, Dec. 2005.

[61] G. Zhang, S. Saw, J. Liu, S. Sterrantino, D. K. Johnson, and S. Jung, "An accurate current source with on-chip self-calibration circuits for low-voltage current-mode differential drivers," *IEEE Trans. on Circuits and Systems I*, vol. 53, pp. 40-47, Jan. 2006.

[62] M. P. Flynn, C. Donovan, and L. Sattler, "Digital calibration incorporating redundancy of Flash ADCs," *IEEE Trans. on Circuits and Systems II*, vol. 50, pp. 205-213, May 2003.

[63] E. Sackinger and W. Guggenbuhl, "A versatile building block: The CMOS differential difference amplifier," *IEEE J. of Solid-State Circuits*, vol. 23, pp.1437-1440, Dec. 1988.

[64] V. Gupta and G. A. Rincón-Mora, "A low dropout, CMOS regulator with high PSR over wideband frequencies," in *Proc. IEEE Intl. Symp. Circuits Systems*, Kobe, Japan, May 2005, pp. 4245-4248.

[65] V. Gupta and Rincón-Mora, "A 5ma 0.6μm CMOS Miller-compensated LDO regulator with -27db worst-case power-supply rejection using 60pf of on-chip capacitance," in *Digest IEEE Intl. Solid-State Circuits Conf.*, San Jose, CA, Feb. 2007, pp. 520-521.

[66] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE Jour. Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.

[67] V.R. von Kaenel, "A high-speed, low-power clock generator for a microprocessor application," *IEEE Jour. of Solid-State Circuits*, vol. 33, pp.1634-1639, Nov. 1998.

[68] G.W. den Besten and B. Nauta, "Embedded 5V-to-3.3V voltage regulator for supplying digital IC's in 3.3V CMOS technology," *IEEE Jour. of Solid-State Circuits*, vol. 33, pp. 956-962, July 1998.

[69] G. Heftman, "Powering the communications infrastructure." [Online] Available: http://findarticles.com/p/articles/mi_hb3021/is_200402/ai_n13112724 (Date accessed: Apr. 2007).

[70] B. Razavi, *Design of Analog CMOS Integrated Circuits,* New York, NY: McGraw-Hill, 2000, ISBN: 0072380322.

[71] G.A. Rincón-Mora and P.E. Allen, "1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference," *IEEE. J. Solid-State Circuits*, vol. 33, pp. 1551-1554, Oct. 1998.

[72] P. Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, "Curvature-compensated BiCMOS bandgap with 1-V supply voltage", *IEEE. J. Solid-State Circuits*, vol. 36, pp. 1076-1081, July 2001.

[73] T. Kaya, H. Koser, and E. Culurciello, "Low-voltage temperature sensor for micro-power harvesters in silicon-on-sapphire CMOS," *IEE Electronics Letters*, vol. 42, pp. 526-528, 27 Apr. 2006.

[74] G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutrì, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *IEEE J. Solid-State Circuits,* vol. 38, pp. 151-9154, Jan. 2003.

[75] T. Ytterdal, "CMOS bandgap voltage reference circuit for supply voltages down to 0.6V," *IEE Electronics Letters*, vol. 39, pp. 1427-1428, 2 Oct. 2003.

[76] K. Lasanen, V. Korkala, E. Raisanen-Ruotsalainen, and J. Kostamovaara, "Design of a 1-V low power CMOS bandgap reference based on resistive subdivision," in *Proc. IEEE Midwest Symp. Circuits Systems*, Tulsa, OK, pp. 564-567, Aug. 2002.

[77] V. Balan, "A low-voltage regulator circuit with self-bias to improve accuracy," *IEEE J. Solid-State Circuits*, vol. 38, pp. 365-368, Feb. 2003.

[78] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, pp. 365-368, Feb. 2003.

[79] I. Ali and R. Griffith, "A fast response, programmable PA regulator subsystem for dual mode CDMA/AMPS handsets," in *IEEE Radio Frequency Integrated Circuit Sym. Digest*, Boston, MA, pp. 321-234, June 2000.

[80] R. Antheunis and I. van Loo, "Simple scalable CMOS linear regulator architecture," in *Proc. European Solid-State Circuits Conf.*, pp. 380-383, Sept. 2001.

[81] E.A. Vittoz, "MOS transistors operated in the linear bipolar mode and their application in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 18, pp. 273-289, June 1983.

[82] W.T. Holman and J.A. Connelly, "A compact low noise operational amplifier for a 1.2μm digital CMOS technology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 710-714, June 1995.

[83] T. Pan and A.A. Abidi, "A 50-dB variable gain amplifier using parasitic bipolar transistors in CMOS," *IEEE J. Solid-State Circuits*, vol. 24, pp. 951-961, Aug. 1989.

[84] D. MacSweeney, K.G. McCarthy, A. Mathewson, and B. Mason, "A SPICE compatible subcircuit model for lateral bipolar transistors in a CMOS process," *IEEE Electron Devices,* vol. 45, pp. 1978-1984, Sept. 1998.

VITA

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In 1997, he obtained an All-India-Rank of 245 among over 100,000 students seeking admission to the Indian Institute of Technology for an undergraduate professional degree. He holds 1 patent and has authored over 8 publications and 8 trade articles on integrated power management circuits. He is the recipient of the Texas Instruments Fellowship and is a member of the IEEE. In 2006, he received the distinction of Competent Toastmaster from Toastmaster's International.

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