# Design, Simulation and Analysis of Novel Types of Unipolar Diodes

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# Design, Simulation and Analysis of Novel Types of Unipolar Diodes

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# Abstract

Nearly all power electronic circuits use power semiconductor devices as switches or rectifiers. The output rectifiers with two terminals (to avoid complexity) and very low threshold voltage as well as low reverse leakage current levels become essential in power supplies for modern and future low voltage applications (output rectifiers with a blocking capability of about or below 200 V). The first part of this work presents the concept and simulation results of a novel unipolar diode named as Regenerative diode which is normally-on i.e. it has almost zero threshold voltage thereby enabling low on-state losses. The Regenerative diode acts as a unipolar diode at low forward current densities (normal operating current densities) and becomes bipolar at higher current densities. This feature ensures the surge current capability of the device in its applications. In this work, the comparison of the I-V characteristics between the Regenerative diode and the classical competitive device Junction Barrier controlled Schottky (JBS) rectifier has also been investigated.

The first part of this thesis is mainly devoted to a novel Regenerative diode structure based on Silicon semiconducting material. Its main advantages are reduction or removal of forward threshold voltage and much improved reverse characteristics without the necessity of a gate control like in synchronous rectifiers. The silicon unipolar device application is, however, restricted to relatively low voltages because of on-state and blocking problems at device blocking capabilities above 200 V.

For high voltage applications (> 200 V), SiC Schottky or JBS rectifiers have demonstrated a good differential on-state resistance and reasonable blocking behavior. In principle, one could try to construct a Regenerative diode like device (to reduce or remove the threshold voltage without sacrificing the blocking capability), but bad hole mobility and much less developed integrated device technology seem to discourage such efforts.

However, based on material and junction interface properties obtained from the literature, a simulation study on a Si/6H-SiC heterojunction is presented in the second part of this thesis. This is the possibility to combine N-6H-SiC with an anode p-Silicon layer to obtain a p-Si/N-6H-SiC heterojunction diode. This heterojunction diode behaves like a Schottky Barrier Diode (SBD) but with much lower threshold voltage than that of the 6H-SiC SBD. Therefore, the heterojunction diode has better on-state characteristics than 6H-SiC SBD without sacrificing in blocking. To ensure the surge current capability and thereby the reliable operation of the diode in its applications, the merged p-i-n Si/6H-SiC heterojunction diode has been proposed and investigated. This merged p-i-n heterojunction diode acts a unipolar diode at normal operating current densities and becomes bipolar at higher current densities. In spite of the unavoidable uncertainties on the physical parameters of the heterostructure diode, the simulation results may encourage further experimental work on such a Schottky – like heterostructure device.

# Kurzfassung

Fast alle leistungselektronischen Schaltungen verwenden Leistungshalbleiter als Schalter oder Gleichrichter. Ausgangs-Gleichrichter mit zwei Anschlüssen (um die Komplexität zu reduzieren) und geringer Schwellenspannung sowie Sperrstrom sind für neue und zukunftsweisende Niederspannung-Anwendungen (Ausgangsgleichrichter mit der Sperrfähigkeit um oder unter 200 V) wesentlich geworden. Der erste Teil dieser Arbeit stellt das Konzept und die Simulationsergebnisse einer neuen unipolaren Diode dar, der Regenerativen Diode, welche selbstleitenden Charakter hat; d.h.diese Diode zeichnet sich durch fast keine Schwellenspannung und somit sehr niedrigen Verlusten im eingeschalteten Zustand aus. Die Regenerative Diode wirkt wie eine unipolare Diode bei niedrigen Vorwärtsströmen (bei typischen Betriebsstromdichten) und wird bipolar bei höheren Stromdichten. Dieses Merkmal sorgt für die Stoßstrombelastbarkeit des Schalters während des Betriebs. Außerdem wurde in dieser Arbeit die Strom-Spannungs-Kennlinie der Regenerativen Diode und des klassischen konkurrierendes Bauelements “Junction Barrier controlled Schottky (JBS)“ Gleichrichter untersucht, und beide wurden miteinander verglichen.

Der erste Teil dieser Arbeit widmet sich vor allem der neu entwickelten Regenerativen Diode, basierend auf dem Halbleitermaterial Silizium. Die wichtigsten Vorteile dieser Diode, bestehen in der Verminderung bzw. dem Verschwinden der Schwellenspannung in eingeschalteten Zustand und in einer deutlich verbesserten Blockierfähigkeit, ohne die Notwendigkeit einer Gate-Steuerung wie in Synchrongleichrichtern. Auf Silizium basierende unipolare Bauelemente sind jedoch auf Anwendungen mit relativ niedrigen Spannungen unterhalb 200 V beschränkt, da sich für Spannungsklassen überhalb 200 V der Leitwiderstand und der Sperrstrom erhöhen.

Für Hochspannungs-Anwendungen (> 200 V), haben SiC-Schottky-oder JBS Gleichrichter nachweisbar einen guten differenziellen Leitwiderstand und zeichnen sich durch ein vernünftiges Sperrverhalten aus. Im Prinzip könnte man versuchen, eine Regenerative Diode für diese Spannungsklasse zu entwickeln (zur Verringerung bzw. zum Verschwinden der Schwellspannung ohne Abstriche bei der Blockierfähigkeit), aber die schlechte Löcherbeweglichkeit und eine viel zu wenig entwickelte Fabrikationstechnologie demotivieren diese Bemühungen.

Allerdings, basierend auf den Material- und Übergangsgrenzflächeneigenschaften, die man in der Literatur findet, wird eine Simulationsstudie auf einem Si/6H-SiC Heteroübergang im zweiten Teil dieser Arbeit vorgestellt. Diese Kombination einer N-6H-SiC- mit einer p-Silizium Anoden-Schicht verhält sich wie eine Schottky Barrier Diode (SBD), aber mit deutlich geringerer Schwellenspannung als diejenige der 6H-SiC-SBD. Daher besitzt die Heteroübergang-Diode einen niedrigeren Widerstand im eingeschalteten Zustand als die 6H-SiC SBD ohne Abstriche in den Blockierfähigkeiten. Um die Stoßstrombelastbarkeit zu

gewährleisten und dadurch einen zuverlässigen Betrieb der Diode in der Anwendung zu garantieren, wurde die “merged p-i-n Si/6H-SiC“ Heterodiode vorgeschlagen und untersucht. Diese “merged p-i-n“ Heteroübergangsdiode funktioniert wie eine unipolare Diode unter normalen Betriebsstromdichten und wird bipolar bei höheren Strömen. Trotz der unvermeidbaren Unsicherheiten im Hinblick auf die physikalischen Parameter der Heteroübergangsdiode, sollten die hier vorgestellten Ergebnisse weitere experimentelle Arbeiten an solchen Schottkydioden - artigen Heterostruktur - Bauelementen motivieren.

# Contents

# Chapter 1

# Introduction

Power semiconductor devices are the heart of the modern power electronic circuits. Most of the power electronic circuits use power semiconductor devices as switches or rectifiers. With the growing demand of low and medium voltage switch-mode power supplies (SMPS) for use in the state-of-the-art integrated circuits, the development of output rectifiers with low forward voltage drop and low reverse leakage current becomes essential.

In low voltage SMPS applications (5 V), the on-state loss of the fast recovery p-i-n diode rectifier contributes greatly to the total power loss in power supplies. This is due to high threshold voltage (about 0.6 V) and also reverse recovery (due to stored charge or electron-hole plasma) behavior of the p-i-n diode rectifiers. Schottky Barrier Diode (SBD) or Schottky diode rectifiers (with the blocking capability of 25 V) have got much attention in these low voltage applications because of low on-state losses (due to low threshold voltage of about 0.3 V) and faster reverse recovery behavior (no stored charge because of its unipolar nature) compared to that of the p-i-n diode rectifiers causing an increase in efficiency of power converters in power supplies [Bali'84, NXP'96]. However, the reverse leakage current is higher in Schottky diode rectifiers compared to that of the p-i-n diode rectifiers and the leakage current increases with the reverse voltage due to barrier height lowering. The on-state losses (mainly threshold voltage) and the reverse leakage current in Schottky diode rectifiers can be controlled by the barrier height of the metal-semiconductor junction. In Schottky diode rectifiers, the on-state losses can be reduced further by decreasing the barrier height but the reverse leakage current increases which degrades the performance of power converters especially at elevated temperatures [Bali'84]. A better trade-off between on-state losses and reverse leakage current can be achieved with the Junction Barrier controlled Schottky (JBS) rectifier [Wila'83], [Bali'84], [Bali'87], [Mohr'94], [Hoss'99] which is a combination of p-i-n diode and Schottky diode.

Most of the modern microprocessors and other portable communication devices require output voltages between 1 V to 3.3 V. In these very low voltage applications, even the Schottky diode rectifiers contribute significantly to the total power loss in power supplies. Therefore, Synchronous rectifier (MOSFET as a rectifier with the proper control of the gate signal) gained much attention and becomes the device of choice in these low voltage applications [Pano'01], [Yee'99], [Naka'98]. This is due to the low on-state losses (resistive like characteristics) of the MOSFET in low voltage applications.

In State-of-the-art automotive applications such as electronic power steering, electric braking, starter/alternator systems and other automotive and telecommunication system applications,

the semiconductor devices with the blocking capability of about 80 – 150 V are required [Moen'02]. The power MOSFETs also gained much attention in the automotive applications [McNe'05], [Kane'06] because of its low on-state losses and especially low reverse leakage current compared to Schottky diode rectifiers. However it increases the cost and complexity (proper control circuit to avoid shoot through current, body diode conduction losses and unlimited reverse current).

The output rectifiers with two terminals to avoid complexity and with very low threshold voltage and low reverse leakage current become essential in power supplies for modern and future low and medium voltage applications (output rectifiers with the blocking capability of about or below 200 V). This is the motivation to the first part of this thesis work.

This work presents a novel unipolar diode which is normally-on i.e., no threshold voltage (thereby low on-state losses) and lower reverse leakage current than existing two terminal rectifiers like Schottky diodes and JBS rectifiers. This novel diode could be the device of choice in low and medium voltage applications (automotive, telecommunication and ORing function applications) to achieve high efficiency in power supplies without any complexity. We named this novel normally-on device as Regenerative diode. This diode can be realized with two normally-on JFETs which are complementary to each other. The operation of this diode is completely different from the operation of the conventional diodes. The conventional diodes conduct reasonable current after some forward voltage (threshold voltage) whereas the Regenerative diode blocks which means it does not allow the current flow after some reverse voltage/current. This device acts as a unipolar diode at low forward currents (normal operating current densities) and becomes bipolar (current conduction mechanism changes from majority carrier type to minority carrier type) at higher currents. This feature ensures the surge current capability of this novel diode.

In high power applications, the Silicon (Si) power devices are considered to be approaching their performance limit, thereby wide research works are being carried out on wide band gap semiconductor materials which can replace Si in this field. In the last few years, Silicon Carbide (SiC) has got much attention in solid state electronics due to its interesting physical properties. SiC is one of the most appropriate semiconductor materials for high power and/or high temperature applications due to its advantageous material properties, such as high electric breakdown field, high thermal conductivity, wide band gap and native thermal oxide [Bhat'93], [Neud'93], [Palm'93].

The higher breakdown field of the 6H-SiC allows for higher doping and thinner drift regions for a given voltage than is required in Si devices, thereby reducing the on-state resistance of SiC power devices. The higher thermal conductivity allows better heat dissipation and wide band gap energy allows higher junction operating temperatures. In addition, SiC is one of the most suitable materials for high frequency applications due to its high saturation velocity and low dielectric constant. The energy efficiency of the power electronic systems can be

improved with the SiC power devices due to their excellent material properties than that of the Si power devices.

SiC p-i-n rectifiers are attractive when compared to that of the Si p-i-n rectifiers in high power, high temperature and high switching speed applications. The higher switching speed of the SiC p-i-n rectifiers over Si p-i-n rectifier is due to thinner drift regions. SiC p-i-n rectifiers are having higher on-state voltage drop compared to that of the Si p-i-n rectifiers at small current densities due to high threshold voltage which is about 2.5 V at 300k. SiC Schottky Barrier Diodes (SiC SBDs) offer lower threshold voltage than that of the SiC p-i-n rectifiers and it is in the range between 0.9 V and 1 V. SiC SBDs become competitive with SiC p-i-n rectifiers at frequencies higher than 100-150 KHz [Ranb'02].

SiC SBDs draw much attention because of their unipolar nature, thereby free from stored charge and hence have a high switching frequency. However, threshold voltage of the SiC SBDs is still high (about 1 V). In addition these devices offer poor surge current capability because of their unipolar nature [Treu'06]. The above two issues are the motivation to the second part of this thesis work. The first part of the thesis work is devoted to novel unipolar diode "Regenerative diode" based on Si. The main advantages of this diode are reduction or removal of forward threshold voltage and much improved blocking characteristics than that of the SBDs or JBS rectifiers. In principle one could try to construct a Regenerative diode like device based on SiC, but the bad hole mobility and much less developed integrated device technology seem to discourage such efforts.

In the second part of the thesis work, a Si/SiC heterojunction diode which offers low threshold voltage and thereby better on-state characteristics than that of the 6H-SiC SBDs has been investigated. To ensure the surge current capability and thereby reliable operation of the diode in its applications, merged p-i-n Si/SiC structure has been proposed and investigated. This merged p-i-n heterojunction diode acts as a unipolar diode at normal operating currents and becomes bipolar (injection of minority carriers) at higher currents.

The outline of this thesis work is as follows: A brief introduction of conventional devices such as p-i-n diode, SBD, JBS rectifier, Merged p-i-n Schottky (MPS) rectifier, Field Effect Transistors (FETs), Synchronous rectifier and heterojunction devices is given in Chapter 2.

Chapter 3 presents the concept and simulation results of a normally-on novel power diode named as "Regenerative diode" which is having regenerative blocking capability. This chapter also presents the different integrated versions of the Regenerative diode and compares the simulated I-V characteristics between them. It also compares the electrical characteristics of the considered Regenerative diode with that of the JBS/MPS rectifier at different temperatures. It also reports on some of the applications of the Regenerative diode as a current limiter and as a protection device for the circuits when they are connected to wrong polarities. Finally it describes the operation and presents the electrical characteristics of the Regenerative diode with Silicon-On-Insulator Technology.

Chapter 4 provides the necessary insights into the properties of the Si/6H-SiC heterojunction interface and presents a simulation study on 600 V p-Si/N-6H-SiC heterojunction diode. This chapter also compares the simulation results of the electrical characteristics of p-Si/N-6H-SiC heterojunction diode with that of the 6H-SiC SBD. Finally, it presents the structure and simulation results of the novel merged p-i-n Si/6H-SiC heterojunction diode which acts as a unipolar diode up to certain current densities (at low and nominal current densities) and becomes bipolar at higher currents.

Chapter 5 presents the summary of this thesis work.

# Chapter 2

# Theoretical Background

This chapter gives a brief introduction about conventional devices such as p-i-n diode, Schottky Barrier Diode (SBD), Junction Barrier Controlled Schottky (JBS) rectifier, Merged p-i-n Schottky (MPS) rectifier, Field Effect Transistors (FETs), Synchronous rectifier and Heterojunction devices.

## 2.1 Diodes

Conventional diodes such as p-i-n diodes and SBDs (Schottky diodes) are normally off devices. They need some forward voltage (threshold voltage), which is around 0.7 V and 0.35 V for silicon based p-i-n diodes and SBDs respectively, to start conducting reasonable current. For low voltage applications, SBDs are preferable because of low threshold voltage and hence low on-state voltage drop when compared to that of the p-i-n diodes. However, for high voltage applications, increase in the on-state resistance (drift region resistance) of the SBDs causes high on-state voltage drop when compared to that of the p-i-n diodes. The typical (simulated) forward bias I-V characteristics of the p-i-n diode and SBD at low and high voltage applications are shown in Fig. 2.1. The detailed description of the I-V characteristics of the p-i-n diode and SBD will be discussed later in this section.

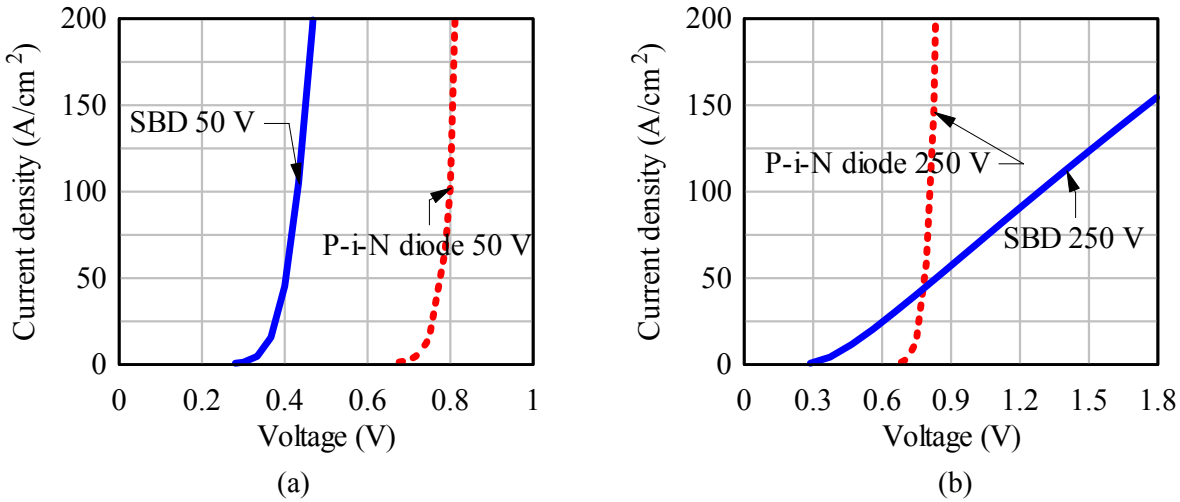



**Fig. 2.1** Forward bias I-V Characteristics of p-i-n diode and SBD **(a)** 50 V blocking capability devices **(b)** 250 V blocking capability devices

All these simulations have been performed at room temperature and for SBD simulations, 0.7 eV was considered as a Schottky barrier height. As shown in Fig. 2.1(a), for the breakdown voltage of 50 V (for low voltage applications), the on-state voltage drop of the p-i-n diode and SBD are 0.8 V and 0.42 V respectively at on-state current density of

100 A/cm$^2$. As shown in Fig. 2.1(b), for the breakdown voltage of 250 V, the on-state voltage drop of the p-i-n diode and SBD are 0.8 V and 1.3 V respectively at on-state current density of 100 A/cm$^2$. In addition, for high voltage SBDs the blocking stability is main concern as the leakage current is high especially at higher temperatures. The leakage current in SBDs is mainly due to the thermionic process which is a strong function of barrier height and temperature [Bali'08].

### 2.1.1 P-i-N Diode

In a p-n junction diode, the electrons move from n-side to p-side and holes move from p-side to n-side across the junction when it is forward biased. Both electrons and holes are involved in the current conduction process. Therefore it is called a bipolar device. For high voltage applications, an intrinsic "i" region (in most cases low doped n region; $n^-$-region) is introduced between heavily doped p and n regions. This region is called a drift region or middle region. The blocking voltage of the device depends upon the thickness and doping of the drift region. The schematic structure of a p-i-n diode is shown in Fig. 2.2.

In reverse bias, a p-i-n diode behaves much more like a normal p-n junction diode, whereas in the forward direction, the current transport mechanisms are different. In a p-n junction diode, from low current densities to high current densities, the current-voltage relation is as follows,

$$J = J_S.\left(\exp\left(\frac{qV_F}{kT}\right)-1\right) \tag{2.1}$$

where $J_S$ is the saturation current density, q is the elementary charge, $V_F$ is the forward voltage, k is Boltzmann's constant and T is the absolute temperature. At very low current levels, the recombination current within the depletion layer of the p-n junction dominates. In this case, the relationship between the current and voltage is as follows,

$$J \propto \exp\left(\frac{qV_F}{2kT}\right) \tag{2.2}$$

In the p-i-n diode, the relationship between the current density and voltage drop across the p-i-n diode depends upon the carrier injection level. The forward I-V characteristics of the p-i-n diode can be explained by three current transport mechanisms.

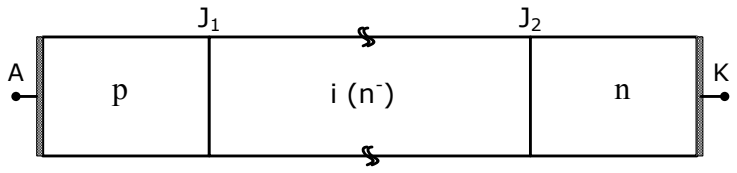



**Fig. 2.2** The Schematic Structure of a p-i-n diode

(i) At very low current levels, the current flow is mainly due to the recombination process within the depletion layer of the p-n junction. In this case, the relationship between the current and the voltage across the diode is as follows,

$$J \propto \exp\left(\frac{qV_F}{2kT}\right) \tag{2.3}$$

(ii) At low current levels, the current flow is mainly due to the diffusion process (low level injection). At low level injection process, the diffusion of minority carrier (hole) concentration in the drift region is well below the background doping concentration of the drift region. In this case, the relationship between the current and the voltage across the diode is as follows ($R_{n^-}$= drift region resistance x area),

$$J \propto \exp\left(\frac{q}{kT}(V_F - J \cdot R_{n^-})\right) \tag{2.4}$$

(iii) At medium and high current levels, the current flow is dominated by the high level injection process. In this process the diffusion of the minority carriers (holes) injected into the drift region exceeds the doping concentration of the drift region. In this state the electron concentration would be equal to the hole concentration to maintain the charge neutrality in the drift region. Therefore, the drift region is flooded with the plasma. The plasma is defined as the high concentration of the injected carriers, where n(x) = p(x) and whose concentration is well above the background doping concentration of the drift region. As a result of plasma the conductivity modulation occurs in the drift region meaning the resistance of the drift region becomes small and hence low on-state voltage drop. In high level injection process, the total current density can be represented with sum of the recombination currents which are the recombination current in the middle region (drift region) and the recombination current in the emitter regions (p and n regions).

$$J = J_M + J_E \tag{2.5}$$

where $J_M$ is the recombination current in the middle region and $J_E$ is the sum of the recombination current in the emitter regions. The total voltage drop across the diode can be represented with the sum of the voltage drop across the middle region and the total junction voltage.

$$V_F = V_M + V_J \tag{2.6}$$

where $V_M$ is the voltage drop across the middle region and $V_J$ is the total junction voltage. The total junction voltage $V_J$ (Appendix A) can be expressed with the following equation,

$$V_J = \frac{kT}{q} \ln\left(\frac{P_{pl}^{\ 2}}{n_i^{\ 2}}\right) \tag{2.7}$$

where $P_{pl}$ is the average plasma concentration in the middle region. In high level injection process, until some current densities the recombination current in the middle region dominates. Therefore the total current density J which is flowing through the diode is equal to $J_M$. In this case, the plasma concentration in the middle region increases proportionally with the current density and hence the voltage drop across the middle region is independent of the current density flowing through the diode. At these current densities, the voltage drop across the middle region $V_M$ is negligibly small (assume high ambipolar diffusion length) and therefore the voltage drop across the diode $V_F$ is approximately equal to the junction voltage $V_J$. In this case, from the above equations, the relation between the current density and voltage is as follows,

$$J \propto \exp\left(\frac{qV_J}{2kT}\right) \approx \exp\left(\frac{qV_F}{2kT}\right) \tag{2.8}$$

For further increases of the current densities, the recombination current in the emitter regions dominates. In this case, the plasma concentration in the middle region, no longer increases proportionally with current density but as the square root of the current density. At these current densities, the voltage drop across the middle region is no longer independent of the current density. The relationships between the current density and the voltage drops across the diode are given by (these relations contain some reasonable simplifications)

$$V_M \propto \sqrt{J} \tag{2.9}$$

and

$$J \propto \exp\left(\frac{qV_J}{kT}\right) \tag{2.10}$$

In case of reverse bias, it prevents the current flow from going through it by moving the carriers away from the junction (electrons in the n-region and holes in the p-region move away from the junction). However, a small reverse leakage (saturation) current is flowing through it. The reverse leakage current flowing through the p-n diode can be explained with the combination of two current transport mechanisms. One is space charge generation current and other one is diffusion current.

(i) Space charge generation current: This is produced by the generation of electron-hole pairs within the depletion layer and swept out by the electric field (the electrons to the n-side and holes to the p-side). In most cases it is reasonable to express the space-charge generation current with the following equation [Bali'08]

$$J_{SC} = \frac{q \cdot W \cdot n_i}{\tau_{SC}} \tag{2.11}$$

where W is the width of the depletion layer and $\tau_{SC}$ is the space-charge generation lifetime. In case of a p-i-n diode, it can be expressed with the following equation

$$J_{SC} = \frac{q \cdot W_{n^-} \cdot n_i}{\tau_{SC}} \tag{2.12}$$

where $W_{n^-}$ is the width of the drift region. The reason being that the whole drift region ($W_{n^-}$) is depleted at a small reverse bias voltages.

(ii) Diffusion current: This is produced by minority carriers which are generated within the neutral regions diffuse to the depletion region boundary and swept out to the opposite side of the junction by the electric field. Diffusion current can be expressed in the n and p regions with following equations

$$J_{DN} = \frac{q \cdot D_P \cdot P_{0N}}{L_P}\left(e^{\frac{qV_F}{kT}} - 1\right) \tag{2.13}$$

where $J_{DN}$ is diffusion current in n region, $D_P$ is the hole diffusion coefficient and $P_{0N}$ is hole concentration in n region at thermal equilibrium.

$$J_{DP} = \frac{q \cdot D_N \cdot N_{0P}}{L_N}\left(e^{\frac{qV_F}{kT}} - 1\right) \tag{2.14}$$

where $J_{DP}$ is diffusion current in p region, $D_N$ is the electron diffusion coefficient and $N_{0P}$ is electron concentration in p region at thermal equilibrium.

In case of reverse bias, the voltage $V_F$ is negative and for large reverse bias voltages $J_{DN}$ and $J_{DP}$ become as follows,

$$J_{DN} = -\frac{q \cdot D_P \cdot P_{0N}}{L_P} \tag{2.15}$$

$$J_{DP} = -\frac{q \cdot D_N \cdot N_{0P}}{L_N} \tag{2.16}$$

where $L_P$ and $L_N$ are diffusion length of the holes and electrons respectively. The above two equations are valid only when the width of the emitter regions, $W_P$ and $W_N$ are much greater than the $L_N$ and $L_P$ respectively, otherwise $L_N$ and $L_P$ are replaced by $W_P$ and $W_N$ respectively. From equations (2.15) and (2.16), the total diffusion current $J_{Diff}$ is,

$$J_{Diff} = -q \cdot \left( \frac{D_P \cdot P_{0N}}{L_P} + \frac{D_N \cdot N_{0P}}{L_N} \right) \tag{2.17}$$

The total reverse leakage current of the p-i-n diode is the sum of the space-charge generation current and diffusion current. However, until certain temperatures (about 450$^o$ C), the reverse leakage current in the p-i-n diode is dominated by the space-charge generation current and beyond this temperature it is dominated by the diffusion current. The reverse leakage current of a diode is a temperature dependent and increases with the temperature owing to the fact that both space-charge generation and diffusion currents are temperature dependent. It can clearly be observed, from equation (2.12) that the space charge generation current is dependent on $n_i$ and $\tau_{SC}$ which are temperature dependent but $n_i$ is much more temperature dependent than the $\tau_{SC}$ (it is true only when the traps are in the midgap) . Therefore, we can write the temperature dependence of the space charge generation current as [Stef'06],

$$J_{SC} \propto n_i \propto \exp\left( -\frac{E_g}{2kT} \right) \tag{2.18}$$

whereas from equation (2.17), the diffusion current is dependent on diffusion constants ($D_P$ and $D_N$), diffusion lengths ($L_N$ and $L_P$) and minority carrier concentrations ($P_{0N}$ and $N_{0P}$). All these three components are temperature dependent. Among these three, the minority carrier concentrations have much more dependence on temperature and thereby we can assume that the diffusion current is proportional to the minority carrier concentration. The minority carrier concentrations are in turn dependent on intrinsic carrier concentration. Therefore, we can write the temperature dependence of the diffusion current as [Stef'06],

$$J_{Diff} \propto n_i^{\,2} \propto \exp\left( -\frac{E_g}{kT} \right) \tag{2.19}$$

The reverse leakage current of a p-i-n diode is less when compared to that of a SBD. However, in switching applications, the switching loss of the p-i-n diode is high when compared to that of the SBD because of the reverse recovery behavior of the p-i-n diode. When a reverse voltage is applied to the conducting p-i-n diode, it needs some time to change its state from conducting to blocking. This is called reverse recovery behavior. The p-i-n diode has plasma in the drift region when it is in the conduction state and to switch the diode from conducting state to blocking state, plasma must be extracted (holes to the p-side and electrons to the n-side) before it can block the voltage. This is the reason for the reverse

recovery behavior in the p-i-n diode. The SBD does not have a reverse recovery behavior like p-i-n diode, because it is a unipolar device (no plasma in the device). At high frequencies, the main performance limitation of the p-i-n diode is the reverse recovery because of high power losses during this period not only in the diode and also in the switch used in the power circuits [Bali'98].

### 2.1.2 Schottky Barrier Diode

Schottky diode or Schottky barrier diode (SBD) is similar to that of the p-i-n diode but it is having metal and n-type semiconductor (low doped semiconductor and whose work function is smaller than the metal work function) interface/junction instead of having the junction between p-type material and n-type material. The schematic structure of a SBD and its band diagram for the junction at equilibrium are shown in Fig. 2.3. The energy-barrier height $q\varphi_b$, as shown in Fig. 2.3(b), is defined as the energy difference between the semiconductor conduction-band edge at the interface and the Fermi level in the metal. This is the key parameter of the junction. The threshold voltage of the SBD depends on this barrier (Schottky barrier) height. The on-state voltage drop of the SBD depends on the Schottky barrier height and drift region ($n^-$-region) resistance. The SBD consists of an ideal diode in series with the resistance (drift region resistance).

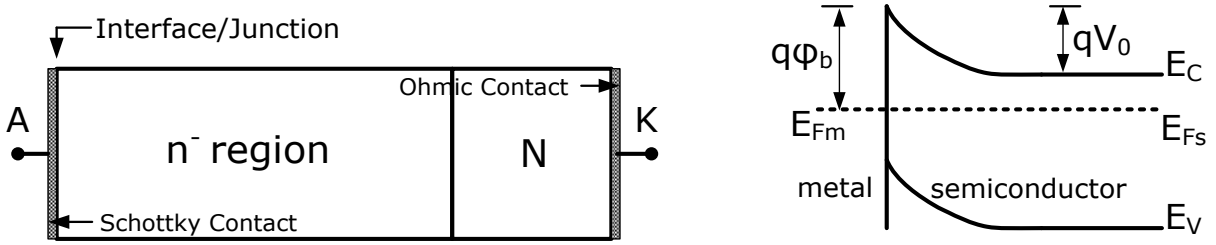



**Fig. 2.3** Schottky barrier diode **(a)** Schematic structure **(b)** Energy band diagram at the junction for an equilibrium case

In a Silicon SBD, under forward and reverse directions, the current flow is mainly due to the thermionic emission process. In a SBD, the current-voltage relation is as follows [Mich'98],

$$J = J_S \cdot \left( \exp\left( \frac{V_F - JR_S}{\eta V_{th}} \right) - 1 \right) \tag{2.20}$$

where $J_S$ is the Schottky diode saturation current, $R_S$ is the series resistance, $\eta$ is the ideality factor and $V_{th}$ is the thermal voltage. The Schottky diode saturation current can be expressed as,

$$J_S = A^* \cdot T^2 \cdot \exp\left( -\frac{q\varphi_b}{kT} \right) \tag{2.21}$$

where $A^*$ is the Richardson constant. In the forward direction, the first term on the right hand side of equation (2.20) dominates. In the reverse direction, the second term on the right hand side of equation (2.20) dominates because of the negative voltage in the first term on the right hand side of the equation (2.20). In the forward direction, a SiC SBD behaves much more like a Silicon SBD (The thermionic emission process is the dominant current transport mechanism). Nevertheless, in the reverse direction, there are significant differences. Detailed description of a SiC SBD will be discussed in the SiC SBD section.

In a SBD, there is only one type of carrier (majority carriers that are electrons in an n-type SBD) involved in the current conduction process and hence it is called unipolar device or majority carrier device. The SBD does not have reverse recovery characteristics because there is no stored charge or plasma in the device and hence very low turn-off losses. This makes the SBD more attractive for high frequency switching applications. The transition or switching time from conduction state to blocking state is only dependent on the parasitic capacitance of the device. The threshold voltage of the SBD is lower compared to that of the p-i-n diode but the reverse leakage (reverse saturation) current is higher in the SBD. The reverse leakage current of the SBD is temperature dependent and increases with the temperature. SBDs are not suitable for high voltage applications because of high on-state losses and high reverse leakage current. The reverse leakage current increases considerably resulting from the Schottky barrier lowering at high blocking voltages. In addition, for high voltage applications, the on-state voltage drop increases due to the increase of the series resistance of the drift region.

Silicon SBDs are useful for low voltage (up to 200 V) applications such as switch mode power converters because of low on-state voltage drop and fast switching speed. However, they can not be used in high voltage applications as explained in the above paragraph. For high voltage (> 200 V) applications, p-i-n diode or SiC SBD has been the device of choice. Nevertheless, due to poor reverse recovery transient behavior of p-i-n diodes, high reverse leakage current of SiC SBDs at high voltages and poor surge current capability of SBDs, several alternative structures have been proposed. JBS/MPS is one among them and the detailed description and operation of this device will be discussed later in this chapter.

## 2.2 JBS/MPS rectifier

The schematic structure of a JBS rectifier shown in Fig. 2.4 is a combination of a p-i-n diode and a Schottky diode or is a cascode connection between Schottky diode and n-channel JFET/Static-Induction-Transistor [Wila'83], [Bali'84], [Bali'87], [Mohr'94], [Held'98], [Dahl'98], [Bali'98], [Hoss'99], [Ran'02]. The JBS rectifier has better characteristics than that of the p-i-n diode in the forward direction until certain current densities. In addition, it has better characteristics than that of the Schottky diode in the reverse direction. If the anode (A) is raised to a positive potential with respect to the cathode (K), the Schottky contact conducts the current from an approximate voltage of 0.3 V and the current flow is due to the majority carriers. Until certain current densities, the forward voltage drop is low when

compared to that of the p-i-n diode, due to its lower threshold voltage. In the forward direction, the I-V characteristics of the JBS rectifier are similar to that of the Schottky diode. The JBS rectifier acts as a unipolar device until the voltage across the p-n junction reaches an approximate value of 0.6 V/0.65 V at room temperature. JBS rectifier is meant for unipolar action.

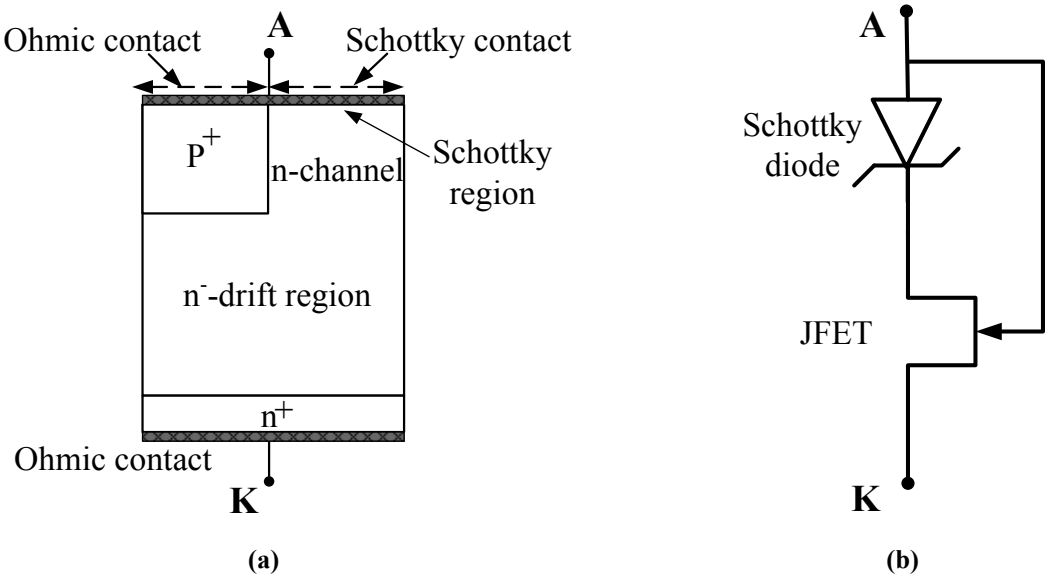



**Fig. 2.4** JBS rectifier **(a)** Schematic Structure **(b)** Equivalent circuit

If the anode is raised to a negative potential, the Schottky barrier and p-n junction become reverse biased. With the increase of the anode potential in the negative direction, the depletion-layers penetrate into the channel and pinch off the channel. Therefore a potential barrier is formed in the channel with the increase of the anode potential when the depletion-layers pinch off the channel. After formation of the potential barrier in the channel, any further increase in the anode potential causes the depletion-layer to extend into the $n^-$-drift region towards the cathode. However the potential barrier shields the Schottky barrier from the applied reverse voltage (high electric fields) and prevents the Schottky barrier-lowering phenomenon. Therefore, unlike the Schottky diodes, the reverse leakage current remains relatively constant even with increasing anode potential until the avalanche breakdown [Bali'98]. The reason being that once the potential barrier is formed in the channel, the electric field at the Schottky contact is nearly constant and independent of the anode potential. Like in Schottky diodes, there is no reverse recovery transient behavior because there is no minority carrier injection in the device. Therefore, JBS rectifier offers similar forward and switching characteristics like Schottky diode and blocking characteristics like p-i-n diode [Ranb'02]. However, Si-JBS rectifier is limited to low voltage range applications like Si-Schottky diode and it can not be used for high voltage applications (>200 V) because of high on-state losses. This voltage range certainly depends on the material that is used in the fabrication of the device and for a 4H-SiC-JBS rectifier it is approximately 3000 V [Ran'02].

MPS rectifier is meant for bipolar action and can be used for high voltage applications. The schematic structure of an MPS rectifier is similar to that of the JBS rectifier (as shown in Fig. 2.4) but the grid spacing and doping of the p-region may be different. In the reverse bias, like in JBS rectifier, the p-n junction is used to reduce the reverse leakage current and hence it can block high voltages in spite of the presence of the Schottky region. At low forward voltages (below 0.5 V to 0.6 V) or low/nominal current densities, the I-V characteristics of the Si-MPS rectifier are similar to that of the Si-Schottky diode or Si-JBS rectifier. However at high current densities or when the voltage across the p-n junction is about 0.6 V, the forward bias I-V characteristics are similar to that of the characteristics of the p-i-n diode. In Si-MPS rectifier, when the voltage across the junction is about 0.6 V, the p-n junction becomes forward biased and starts injecting minority carriers (holes) into the drift region. This results in a conductivity modulation of the drift region, like in a p-i-n diode. The injection level required to reduce the drift region resistance is not as large as that observed in the p-i-n diode [Bali'98]. As a result, the stored charge in the drift region of the MPS rectifier is much smaller than that of the p-i-n diode. The MPS rectifier is having superior reverse recovery transient behavior compared to that of the p-i-n diodes because of the reduced stored charge. Therefore the MPS rectifier offers better trade-off between forward voltage drop and turn-off losses compared to that of the normal p-i-n diodes [Nand'99].

## 2.3 Field Effect Transistors

Field effect transistor (FET) is a voltage controlled transistor unlike the bipolar transistor which is a current controlled transistor. In a FET, the current flow between the drain and source is controlled by the gate voltage. There are several types of FETs like Junction FET (JFET), Metal-Semiconductor FET (MESFET) and Metal-Oxide-Semiconductor FET (MOSFET) [Sze'81], [Stre'00]. The main goal of these FETs is to control the current flow between the drain and source by using the gate voltage but they use different kind of gate system to control it. In a JFET they use a p-n junction, in a MESFET they use a metal-semiconductor junction and in a MOSFET they use an insulator between the gate and semiconductor. They all are majority carrier devices (except bipolar mode JFETs) because the current conduction is due to only one type of carriers that are majority carriers. Therefore, these devices are usually called unipolar devices. FETs have positive temperature coefficient of resistance and this effect prevents the current localization phenomenon in FETs. Therefore, many devices can be connected in parallel to increase the current handling capability [Bali'87]. These devices are useful in high frequency applications because of the absence of the minority carrier injection.

### 2.3.1 Junction Field Effect Transistor

The schematic structure of a lateral JFET and a vertical power JFET are illustrated in Fig. 2.5. Lateral JFETs are used for low voltage applications whereas vertical power JFETs are used for high voltage applications. In both of them, the channel length (L) is much larger than the

width (W) of the channel. Therefore, they have pentode like characteristics; that is the drain current ($I_D$) saturates at high drain voltages ($V_{DS}$) [Bali'87]. The drain current-voltage characteristics of a JFET as varying the gate voltage are illustrated in Fig. 2.5(c).

In normally-on JFETs (without applying any gate potential which means the gate is short-circuited to the source, $V_{GS} = 0$) there is a conducting channel between the drain and source and hence the current flows from the drain to the source (in n-channel devices, the drain is at positive potential with respect to the source). The voltage variable depletion layer width of a junction between $p^+$-gate and n-channel is used to control the effective cross sectional area of the conducting channel. The channel resistance varies with the changes in the effective cross sectional area of the channel since the resistivity of the channel is fixed by its doping.

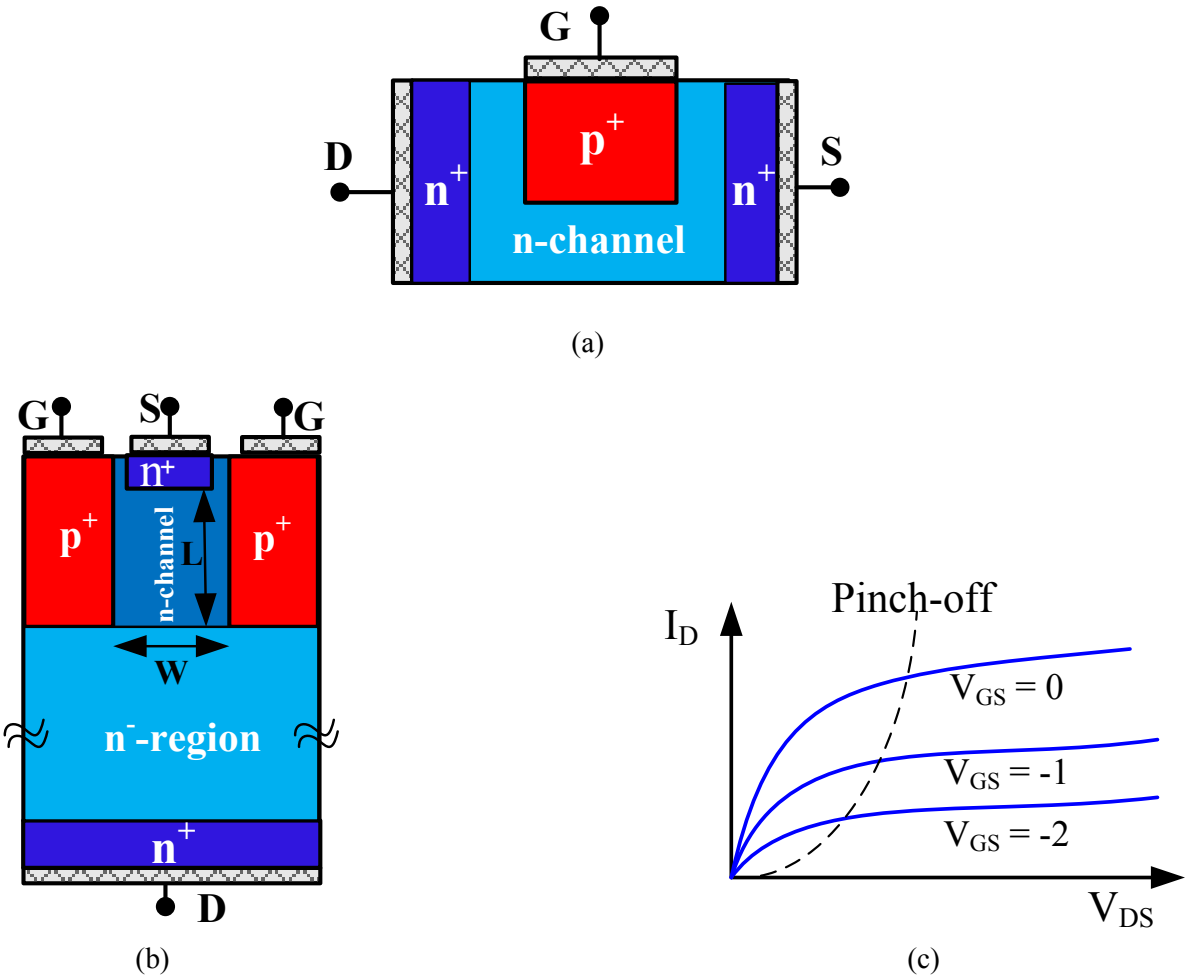



**Fig. 2.5 (a)** Schematic structure of a later JFET **(b)** Schematic structure of a vertical power JFET **(c)** I-V characteristics of a JFET

JFETs exhibit resistive like characteristics at low drain voltages as shown in Fig. 2.5(c), and after that the drain current ($I_D$) saturates. The drain current saturates at high drain voltages because the width of the depletion layer (due to the reverse bias between $p^+$-gate and n-channel) increases at the drain side of the channel with the increase of the drain voltage and pinch off the channel at the drain side. The resistance of the channel increases with the negative gate potential because the effective cross sectional area of the channel decreases due

to increase of the depletion layer width of a junction between $p^+$-gate and n-channel. Therefore, the pinch-off condition is reached at lower drain voltages and at lower drain currents with the increase of the negative gate potential as illustrated in Fig. 2.5(c).

In normally-off devices, there is no conducting channel at $V_{GS} = 0$, i.e., the effective channel width is zero and hence there is no current flow from drain to the source. The effective channel width will be increased with the sufficient positive gate voltage, $V_{GS}$ and hence the current to flow from the drain to source with the positive gate voltage, $V_{GS}$. These devices also have similar type of characteristics as shown in Fig. 2.5(c) for positive gate voltages, $V_{GS}$.

### 2.3.2 Static Induction Transistor

The schematic structure of a Static Induction Transistor (SIT) as shown in Fig. 2.6(a) looks similar to that of the JFET (shown in Fig. 2.5(b)) but the significant difference lies in the length of the channel.

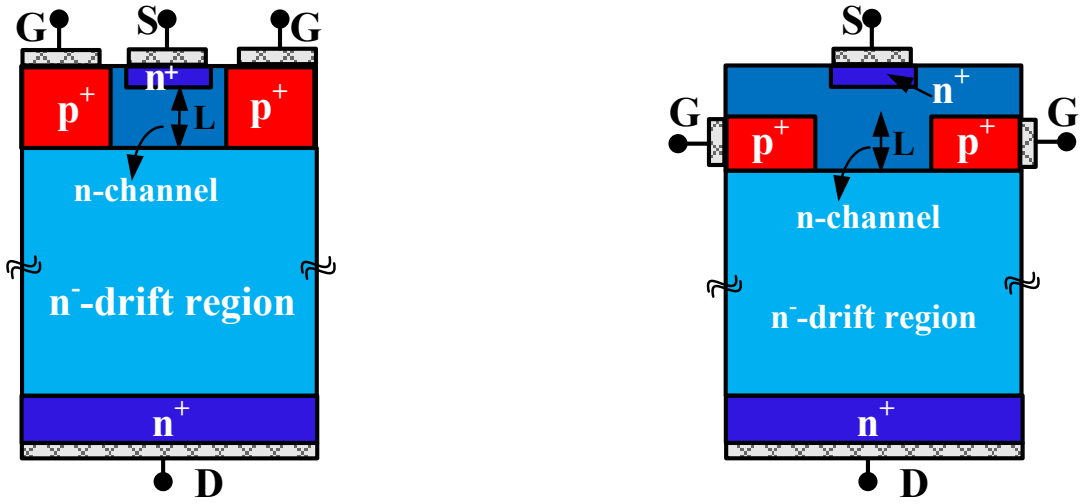



**Fig. 2.6** The schematic structures of a SIT **(a)** Planer gate SIT **(b)** Buried gate SIT

The length of the channel is short in the SIT compared to that of the JFET. This difference makes the output characteristics of the SIT completely different from the JFET. The SIT shows the non-saturated output characteristics [Nish'75], whereas the JFET shows the saturated output characteristics. Fig. 2.6 illustrates two different schematic structures of a SIT. In a SIT, the current flow between the drain and source is controlled by an induced electrostatic potential barrier [Wila'99]. The potential barrier is appeared in the channel region between the gate regions and in a SIT it is influenced by both the gate as well as the drain potentials [Nish'78].

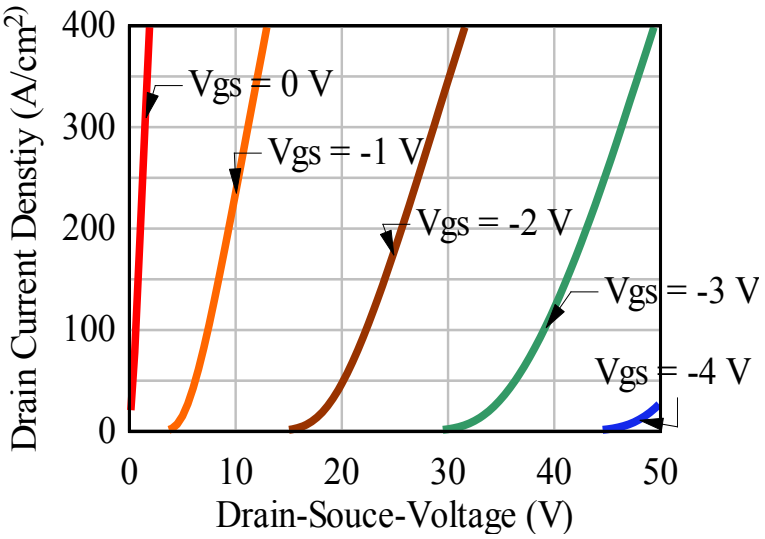



**Fig. 2.7** The simulated output I-V characteristics of the planer gate SIT

Fig. 2.7 illustrates the simulated output characteristics (drain current vs. drain-source voltage) of the planer gate SIT. The SIT is a normally on device in which the channel is not pinched-off by the gate to channel built in voltage. In this case, the device can operate as a good variable resistor and the characteristics are ohmic [Nish'75]. The channel is pinched-off (depleted) by applying the negative gate voltage ($V_{GS}$). In this case, at low drain to source voltages ($V_{DS}$), there is no current flow between the drain and source because the potential barrier is formed in the channel region by the negative gate voltage (The device starts conducting currents at defined voltages as shown in Fig. 2.7). This potential barrier prohibits the carriers to flow from the source to the drain. However, with a further increase of the drain to source voltage, the potential barrier height which controls the carriers flow is gradually reduced and at the same time the position of the potential barrier is moved towards the source [Nish'78]. This results in a current flow between the drain and source and increases continuously with the increase of the drain to source voltage. This happens in the SIT because of the short channel and thereby it exhibits non-saturating I-V characteristics. Fig. 2.8 illustrates the potential distribution of the planer gate SIT from the source to the drain side through the middle of the channel for the gate-source voltage $V_{GS}$ = -3 V. The cut is made through the middle of the channel from the source to the drain. As shown in Fig. 2.8, there is a high potential barrier in the channel for the carriers to flow from the source to the drain for the gate-source voltage Vgs = -3 V and drain-source voltage Vds = 0. In this case, as shown in Fig. 2.7, there is no current flow in the device. It can clearly be seen from Fig. 2.8, that the potential barrier height decreases as the drain-source voltage increases and hence the current starts to flow when the drain-source voltage reaches around 30 V (as shown in Fig. 2.7, for the gate-source voltage $V_{GS}$ = -3 V).

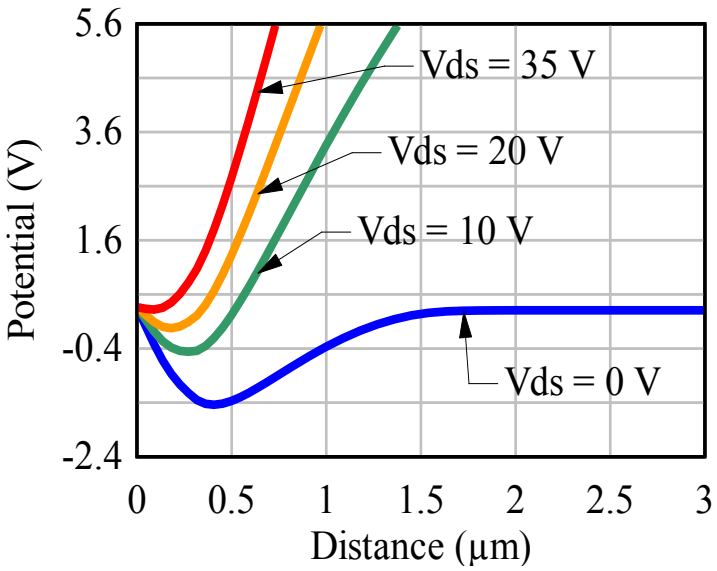



**Fig. 2.8** Potential distribution of the planer gate SIT from source to drain side through the middle of the channel for the gate-source voltage $V_{GS}$ = -3 V while varying drain-source voltage $V_{DS}$. In this simulation, the depth of the gate regions is 0.3 µm i.e. the channel length is approximately 0.3 µm.

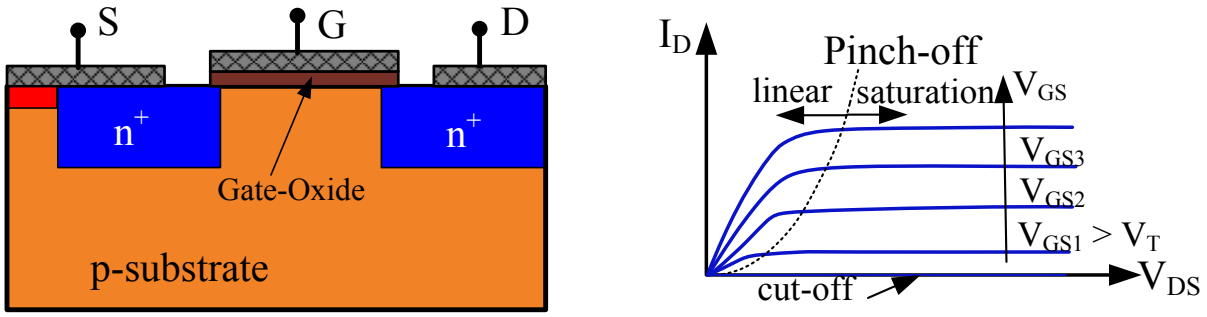
However, it is also possible to design a SIT as a normally-off device and is called bipolar mode SIT (BSIT) [Nish1'78]. In a BSIT, the channel is completely pinched-off by the gate to channel built-in voltage and as a result potential barrier appears in the channel. The potential barrier height is lowered by applying a positive gate-source voltage. For further increase of the gate-source voltage, the gate-source junction becomes forward biased and injects minority carriers in to the channel. The planer gate SIT as shown in Fig. 2.6(a), is a very promising device for high frequency and high power applications because of its short channel length, low gate series resistance and small gate-source capacitance. The operation frequency of the buried gate SIT, as shown in Fig. 2.6(b), is limited to 2-5 MHz because of high parasitic capacitance [Nish'78].

### 2.3.3 MOSFET

In the modern electronics, the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) [Sze'02], [Stef'06], [Stre'00] is a dominant semiconductor device and can be used for amplifying or switching electronic signals. Like in all other FETs, the current conduction is only due to majority carriers and the current conduction between the drain (D) and source (S) is controlled by the gate (G) terminal. However, in the MOSFET, the gate terminal is separated from the semiconductor material by an insulator. As a result it has high gate input impedance compared to other FETs and BJTs. Since it has high gate input impedance and fast switching speed (no plasma in the device because it is a unipolar device), the power MOSFET became an attractive semiconductor switch for power electronic applications. There are two types of MOSFETs: enhancement-mode and depletion-mode MOSFETs, each of which can be n-channel or p-channel.

The structure of a conventional n-channel enhancement-mode MOSFET is shown in Fig. 2.9(a). The conduction or inversion channel is formed in the p-substrate under the gate

between the drain and source when a positive voltage, which is higher than the threshold voltage $V_T$, is applied to the gate. When $V_{GS} > V_T$, the drain current $I_D$ linearly increases with the drain-source voltage $V_{DS}$ and this is only true at low $V_{DS}$ where $V_{DS} < V_{GS}-V_T$. As shown in Fig. 2.9(b), this region is called linear region. As the drain current increases, there is more ohmic voltage drop along the channel and therefore the channel potential varies from zero at the source end to the applied drain potential at the drain end (assume there is no voltage drop in the source and drain regions). As a result the potential difference between the gate and the inversion channel reduces from $V_{GS}$ at the source end to the $V_{GS}-V_{DS}$ at the drain end. The inversion channel is pinched-off at the drain end when the potential difference $V_{GS}-V_{DS}$ is equal to threshold voltage $V_T$. This drain voltage is called pinch-off voltage $V_{Dsat}$.




(a) (b)

**Fig. 2.9** Conventional n-channel enhancement-mode MOSFET **(a)** Schematic structure **(b)** Output I-V characteristics

As shown in Fig. 2.9(b), the region beyond this pinch-off is called saturation region because the drain current is constant and is independent of $V_{DS}$. However, there is a slight increase of the drain current with the $V_{DS}$ due to effects like channel length modulation and drain-induced barrier lowering. When $V_{GS}<V_T$, there is no conducting channel between the drain and source which causes no current flow between them. The junction between the drain ($n^+$-region) and p-substrate is reverse biased and as a result the depletion layer penetrates into the p-substrate towards the source side with the increase of the $V_{DS}$. However, the structure as shown in Fig. 2.9(a) cannot be used for high voltage applications as it has high on-state losses due to high channel resistance (because of long channel and low substrate doping to support high voltages) and dependency of the breakdown voltage on the thickness of the gate oxide (the gate oxide thickness must be sufficiently large near the drain to support high voltages). Consequently, the threshold voltage $V_T$ of the device is constrained by the blocking voltage requirement of the device since it is a function of the channel length, channel doping and gate oxide thickness. The vertical power MOSFETs such as Vertical Double-Diffused MOSFET (Vertical DMOS – Fig. 2.10(a)), Trench MOSFET (also called U-MOSFET - Fig. 2.10(b)) and CoolMOS (also called Super Junction MOSFET - Fig. 2.10(c)) are used for high voltage applications [Stef'06], [Bali'08], [Lutz'11]. The vertical Power MOSFET is a dominant semiconductor switch for power electronic applications in the voltage ranges below 600 V.

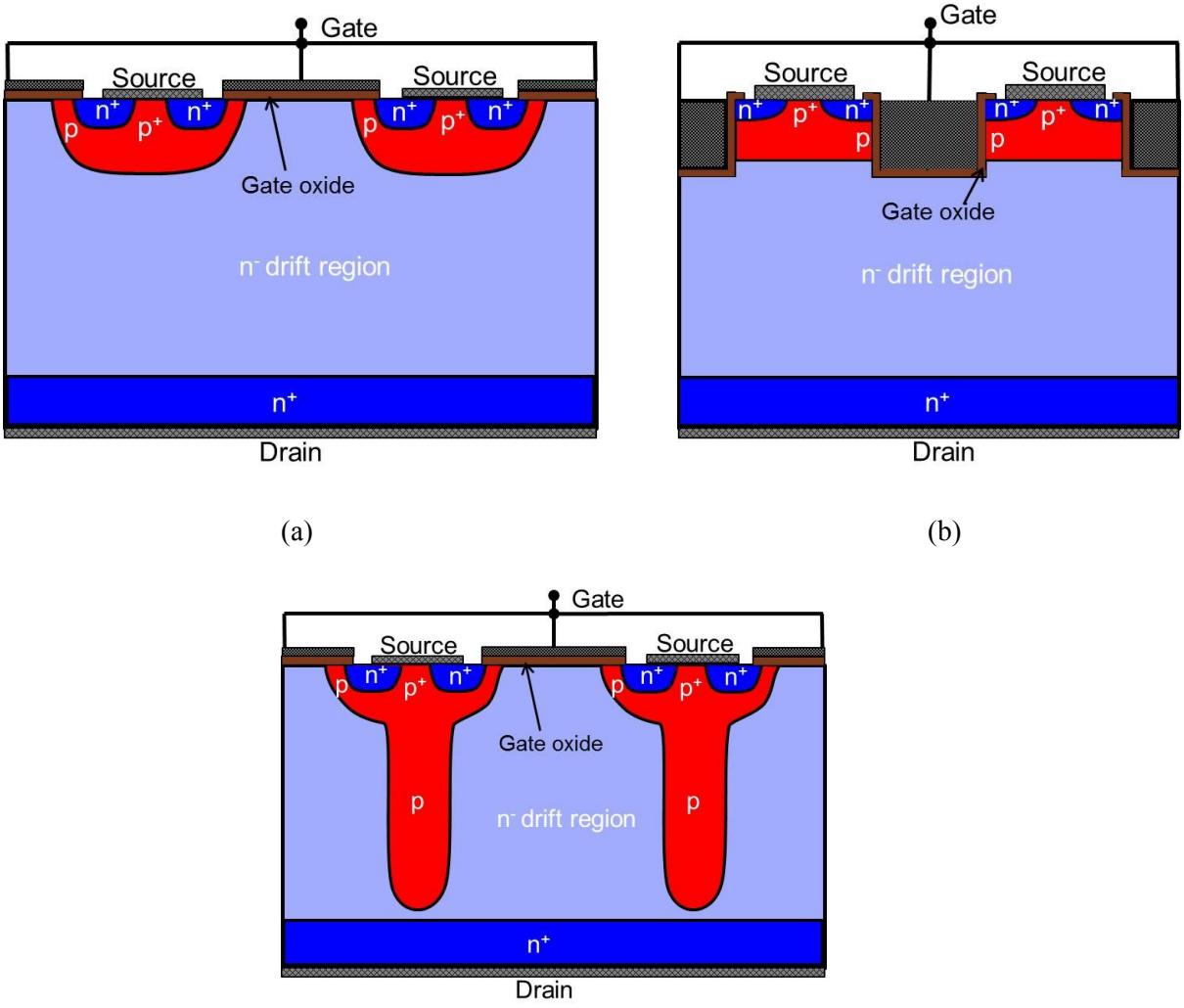
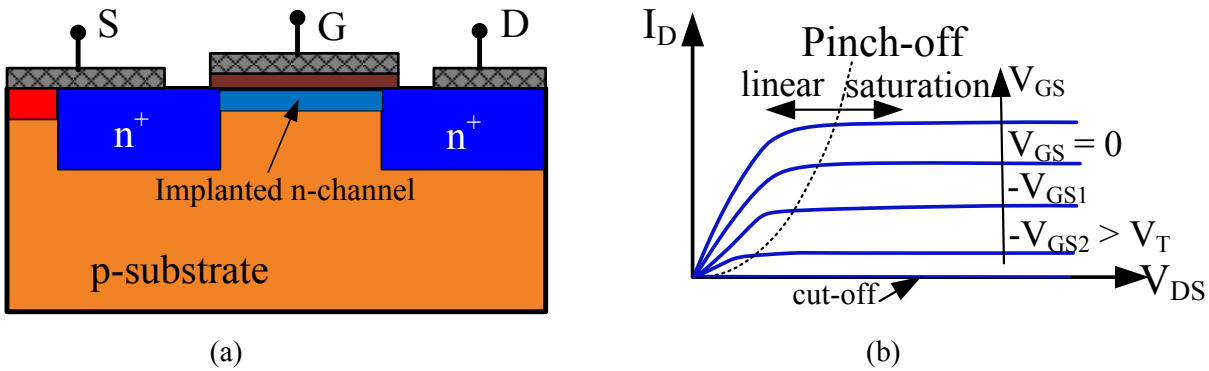



**Fig. 2.10** Schematic structures of power MOSFET **(a)** Vertical DMOS **(b)** Trench MOSFET **(c)** Super Junction MOSFET

The structure of a conventional n-channel depletion-mode MOSFET is illustrated in Fig. 2.11(a). Its structure is same as n-channel enhancement-mode MOSFET except that the channel (n-type) is physically implanted in depletion-mode rather than being induced.

The n-channel exists between the drain and source under the gate in the p-substrate and conducts even when the gate- source voltage $V_{GS} = 0$. For a positive gate-source voltage ($V_{GS} > 0$), the channel is further enhanced by attraction of more electrons into it and its conductivity increases. For a negative gate-source voltage ($V_{GS} < 0$), the channel conductivity decreases due to repelling of electrons, and this phenomenon is referred to as channel depletion. For further increase of negative gate-source voltage $V_{GS}$, the channel is completely depleted i.e., the device is said to be in cut-off mode. The value of the $V_{GS}$ at which the channel is completely depleted is called threshold voltage $V_T$ of the depletion-mode MOSFET.



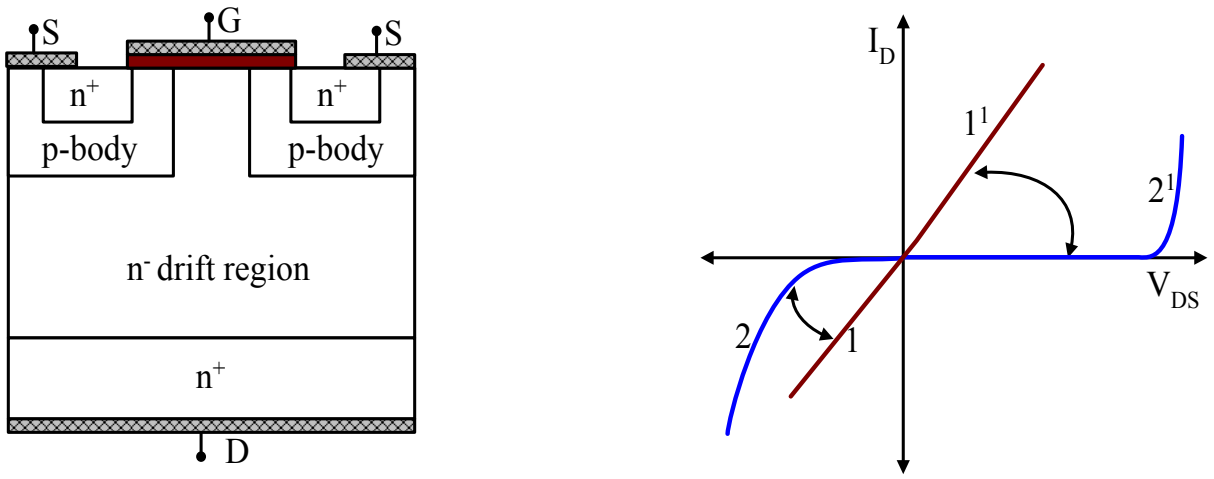

(a) (b)

**Fig. 2.11** Conventional n-channel depletion-mode MOSFET **(a)** Schematic structure **(b)** Output I-V characteristics

Like in enhancement-mode MOSFET, to have a conducting channel the $V_{GS}$ should be greater than the threshold voltage $V_T$ i.e., $V_{GS}$-$V_T$ > 0. The output I-V characteristics of the n-channel depletion-mode MOSFET are shown in Fig. 2.11(b), and they look similar to that of the output I-V characteristics of the n-channel enhancement-mode MOSFET which are illustrated in Fig. 2.9(b).

## 2.4 Synchronous rectifier

Synchronous rectification can be done by using power MOSFET as a rectifier. Synchronous rectification improves the efficiency of the switch mode power supply, particularly in low voltage applications [Bali'87].




(a) (b)

**Fig. 2.12** Synchronous rectifier **(a)** Schematic structure **(b)** I-V characteristics

The schematic structure and I-V characteristics of a Synchronous rectifier are shown in Fig. 2.12. A Power MOSFET (n-channel MOSFET) can be used as a Synchronous rectifier in the third quadrant [Bali'87]. It has characteristics like curve "1", when the drain (D) is at negative potential and the gate (G) is at positive potential (greater than threshold voltage) with respect to that of the source (S). It exhibits resistive on-state characteristics like curve "1" at low $V_{DS}$. The on-state resistance of the MOSFETs can be lowered, either by increasing the

size of the device or by paralleling discrete devices. As a result until certain current densities, the forward voltage drop (the conduction losses) of the Synchronous rectifier can be lowered than that of the p-i-n diode or Schottky diode. Therefore, the efficiency of the power supply system can be increased as the conduction loss of the rectifier/diode contributes significantly to the overall power loss in power supply system/circuit. The main problem to use power MOSFET as a Synchronous rectifier in the circuits, is to provide a gate signal in synchronism with the supply voltage.

The Synchronous rectifier changes its characteristics from curve "1" to curve "2", when the gate-source voltage ($V_{GS}$) is smaller than the threshold voltage or $V_{GS}$ is zero. In this case, there is no channel for the current to flow from source to the drain because of the absence of the gate potential. Therefore there is no current flow in the device until certain voltage i.e., approximately 0.5 to 0.6 V at 300 K. Afterwards the junction between p-body and $n^-$-drift region becomes forward biased and injects minority carriers (holes) into the $n^-$-drift region. Therefore, after this voltage the device starts conducting current like normal p-i-n diode. However, this body diode has very poor reverse recovery characteristics due to the high lifetime in the $n^-$-drift region. Therefore, in some circuits, where the synchronous rectification is needed, an external Schottky diode can be used in parallel with the Synchronous rectifier to shunt this body diode and prevent it from affecting the circuits performance [Yee'99]. Nevertheless, in some applications, to avoid additional cost of external diode, its internal body diode can be used since the reverse recovery characteristics of the internal body diode can be improved either by lifetime killing methods like electron or α-particle or proton irradiation or platinum diffusion [Bali'08], [Stef'06] or with the controlled emitter efficiency which is achieved by the MOS inversion channel techniques [Dirk'01].

The I-V characteristics of the power MOSFET in the first quadrant are illustrated in Fig. 2.12(b). It has characteristics like curve "$1^1$", when the drain is at positive potential and the $V_{GS}$ is greater than the threshold voltage. It changes its characteristics from curve "$1^1$" to curve "$2^1$" when the $V_{GS}$ is smaller than threshold voltage or zero. In this case, there is no conductive channel which causes no current flow and the junction between p-body and $n^-$-drift region becomes reverse biased. This junction can support higher voltages and the break down voltage of the device depends on the doping and thickness of the $n^-$-drift region.

## 2.5 Dual Thyristor

Dual Thyristor is a power device which has a regenerative turn-off capability [Rose'07], [Vemu'07]. The regenerative turn-on action is a well-known feature of power devices like Shockley diode/ Thyristor. Thyristor can be developed from the combination of two normally-off current controlled transistors (BJTs) which are complementary to each other. Thyristor has over voltage turn-on capability and can be used for both power control and over voltage protection. Dual Thyristor is a device which exhibits over current turn-off capability and can be used for over current protection. Dual Thyristor can be realized by the dualization of a Thyristor equivalent circuit. Fig. 2.13 illustrates the equivalent circuit of a Thyristor and

Dual Thyristor, while Fig. 2.14 illustrates their I-V characteristics. Dual Thyristor is a series combination of two normally-on JFETs which are complementary to each other. The device with similar properties like Dual Thyristor can also be realized from the combination of two normally-on MOSFETs which are complementary to each other [Sanc'99].


(a) (b)

**Fig. 2.13** Equivalent structure of (a) Thyristor (b) Dual Thyristor


(a) (b)

**Fig. 2.14** I-V characteristics of (a) Thyristor (b) Dual Thyristor

In a Thyristor, the regenerative turn-on action occurs from the current amplification, meaning the current obtained at breakdown condition stimulates the turn-on action. In a Dual Thyristor, the regenerative turn-off action occurs from the voltage amplification, meaning the voltage created at certain current limit stimulates the turn-off action. The turn-on condition is obtained in a Thyristor, when the differential current gains of the transistors are current dependent. This is normally obtained by appropriate emitter shunting of n-p-n transistor. The turn-on condition of the Thyristor is fulfilled with the following relation:

$$\vec{\beta_1} * \vec{\beta_2} \geq 1$$

where $\vec{\beta_1}$ and $\vec{\beta_2}$ are the common-emitter differential current gains of the bipolar transistors $T_1$ and $T_2$ respectively.

In contrast, the turn-off condition is obtained in a Dual Thyristor, when the differential voltage gain of one of the transistors is voltage dependent. The turn-off condition of the Dual Thyristor is fulfilled with the following relation:

$$\vec{A_1} * \vec{A_2} \geq 1$$

where $\vec{A_1}$ and $\vec{A_2}$ are the differential voltage gains of the field effect transistors $T_1$ and $T_2$ respectively.

## 2.6 Heterojunction Devices

In modern solid state physics, heterostructures play an important role. Heterostructures are the building blocks of the most modern semiconductor devices such as LASERs, High Electron Mobility Transistors (HEMTs) and BJTs. Heterostructures consists of a single or multiple heterojunctions. Heterojunction is a junction between two different semiconductors which have different band gaps, permittivities and electron affinities [Stre'00], [Sze'81].

The heterojunction interface between such semiconductors may be virtually free of defects especially when those semiconductors have matched lattice structures and not too different lattice constants. At thermal equilibrium, the Fermi level is continuous and the mismatch in energy band gap $\Delta E_g$ of the two semiconductors must be accommodated by discontinuities in the conduction and valance band edges. The resulting discontinuities in the conduction band $\Delta E_C$ and valance band $\Delta E_V$ are the most important parameters for the behavior and performance of the heterojunction devices. For an ideal heterojunction, according to the electron affinity rule, the conduction band off set is equal to the difference in the electron affinities between two semiconductors and the valance band off set would be found from $\Delta E_g$ - $\Delta E_C$. This is clearly demonstrated in Fig. 2.15. When two different semiconductors have the same type of conductivity, the junction is called an isotype heterojunction and if they differ in conductivity, the junction is called an anisotype heterojunction [Sze'81]. The Fig. 2.15 illustrates the band diagrams of an anisotype (n-P) heterojunction interface. Unlike the homojunction structures, the barrier for the electrons to move from n-side to the P-side is quite different than that of the barrier for the holes that move from P-side to the n-side (The small band gap material is labeled with a small letter and wide band gap material is labeled with a capital letter).

As shown in Fig. 2.15, the barrier for the electrons $qV_n$ to move from n-side to P-side is higher compared to that of the barrier for the holes $qV_p$ to move from P-side to n-side. Fig. 2.16 illustrates the energy band diagrams of an isotype (n-N) heterojunction. In this, the barrier for the holes to move from n-side to the N-side is higher compared to that of the barrier for the electrons to move from N-side to the n-side. There are inherent difficulties in fabricating heterojunctions due to the mismatch in lattice constants and thermal expansion coefficients [Calo'67]. However, heterojunction devices show potential benefits in many applications.

The main advantages of the heterojunction interface(s) are summarized below

a. Blocking of the minority carrier injection (example is heterojunction Bipolar Transistor)

b. Channel formation or 2D electron gas formation (example is HEMT)

c. Quantum well formation (example is LASER)

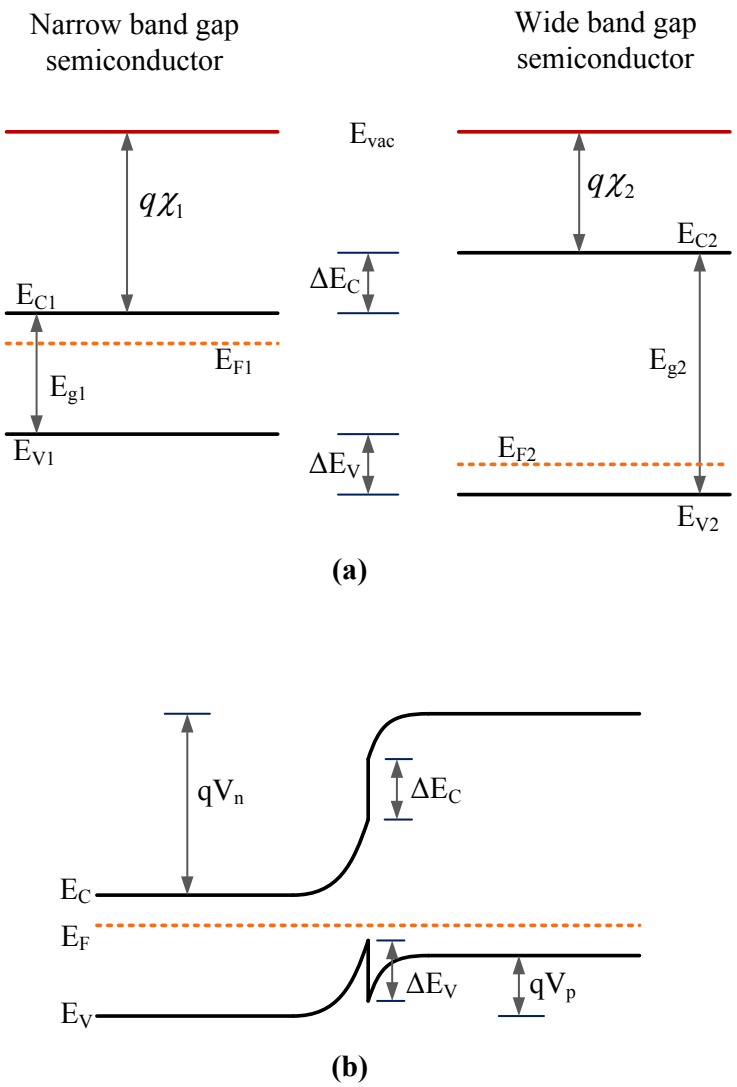



**Fig. 2.15** Heterojunction between an n-type narrow band gap semiconductor and a P-type wide band gap semiconductor **(a)** Energy band diagrams of the two semiconductors before in contact to each other **(b)** Energy band diagram of the heterojunction at thermal equilibrium

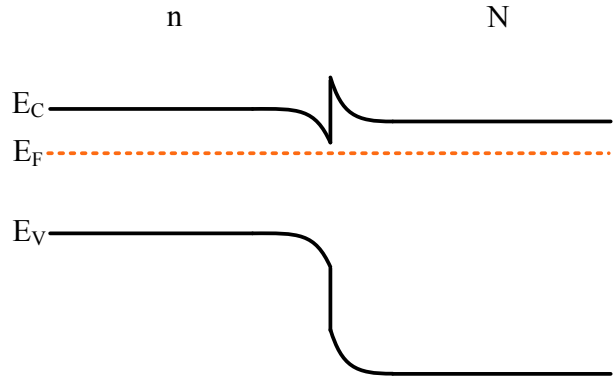



**Fig. 2.16** Heterojunction between an n-type narrow band gap semiconductor and an N-type wide band gap semiconductor

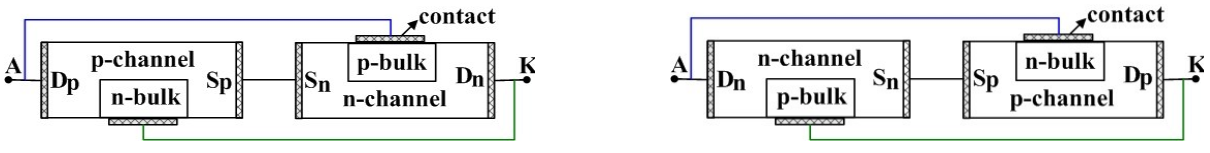
# Chapter 3

# Regenerative Diode

This chapter presents the concept and simulation results of a Novel power diode named as "Regenerative diode" which is having regenerative blocking capability. Regenerative diode is a diode which operates completely different from the "normal" diodes/rectifiers such as p-i-n diode, Schottky Barrier Diode (SBD) and Junction Barrier Controlled Schottky (JBS)/Merged p-i-n Schottky (MPS) rectifier. Normal diodes open meaning they start conducting reasonable current after some forward voltage i.e., around 0.6 V and 0.3 V for p-i-n diodes and SBDs respectively whereas Regenerative diode closes meaning it starts blocking after some reverse voltage/current. This chapter presents the comparison of the electrical characteristics (simulation results) between Regenerative diode and JBS/MPS rectifier at different temperatures. It also reports on some of the applications of the Regenerative diode as a current limiter and as a protection device for the circuits when they connect to wrong polarities. Finally it describes the operation and presents the electrical characteristics of the Regenerative diode with Silicon-On-Insulator Technology.

## 3.1 Concept of a Regenerative Diode

Regenerative diode is a diode meaning it can be operated with two terminals. Unlike, conventional diodes, it is a normally-on device. Like Dual Thyristor, Regenerative diode can be developed from a series combination of two complementary JFETs which are normally-on. However, the applications of these two devices are entirely different. Dual Thyristor can be used in over current protection applications, as a circuit breaker or current limiter whereas the Regenerative diode could be used as a rectifier or a protection device for the low voltage systems from the wrong polarity. Regenerative diode can also be used as a current limiter in the third quadrant. Fig. 3.1 illustrates the schematic structure of the Regenerative diode and Dual Thyristor.

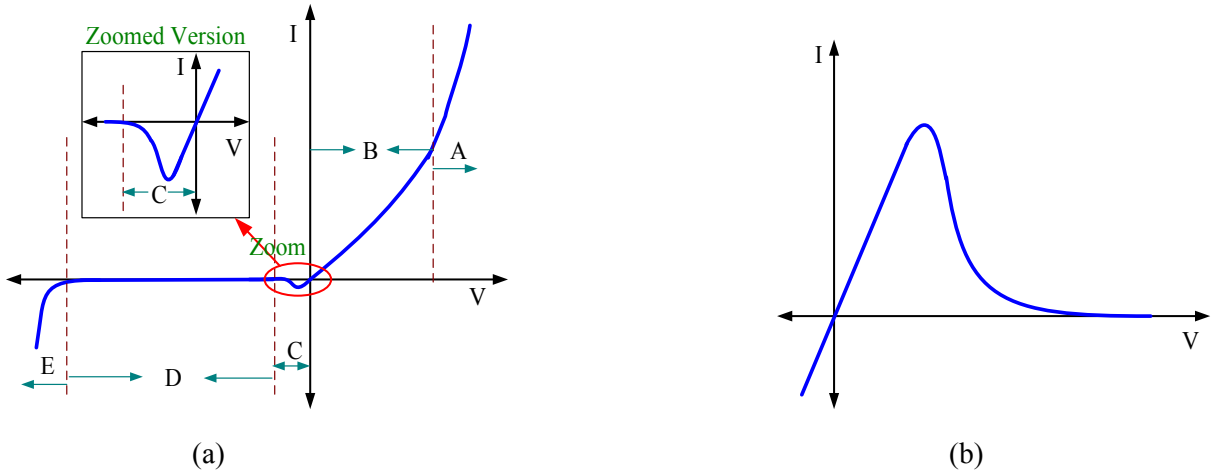



(a) (b)

**Fig. 3.1** Schematic structure of a **(a)** Regenerative diode **(b)** Dual Thyristor

The schematic structure of the Regenerative diode looks similar to that of the Dual Thyristor. Nevertheless, the drain of the p-channel JFET and n-channel JFET act as anode (A) and cathode (K) respectively in the case of Regenerative diode whereas they are exchanged in the

case of Dual Thyristor. Therefore, the I-V characteristics of the Regenerative diode lie exactly in opposite co-ordinates when compared to the I-V characteristics of the Dual Thyristor. The I-V characteristics of the Regenerative diode and the Dual Thyristor are shown in Fig. 3.2. The forward characteristics of the Regenerative diode have been obtained by applying a positive voltage to the anode (A) with respect to the cathode (K). These are similar to the forward characteristics of the normal diode (in the beginning i.e. at low current densities, Regenerative diode characteristics follow SBD characteristics but without threshold voltage and at higher current densities, follow P-i-N diode characteristics) but the current flow in the Regenerative diode starts without threshold voltage unlike in the normal diodes. The Silicon based Regenerative diode as shown in Fig. 3.1(a) acts as a unipolar device at low/nominal current densities (until the voltage across the device reaches about 0.6 to 0.7 V at 300 K) and becomes bipolar at higher current densities.




(a) (b)

**Fig. 3.2** The I-V characteristics of a **(a)** Regenerative diode **(b)** Dual Thyristor

The reverse characteristics of the Regenerative diode have been obtained by applying a negative voltage to the anode (A) with respect to the cathode (K). As shown in zoomed version of the Fig. 3.2(a), the Regenerative diode starts blocking after some reverse voltage/current meaning there is some reverse peak current flowing in the device till some voltage/current, due to the normally-on behavior of the device. It requires some negative voltage/current to close the channels and after that the current flow reduces nearly to zero and the device enters into the blocking state. After this negative voltage/current, the device I-V characteristics are similar to that of the reverse I-V characteristics of the p-i-n diode.

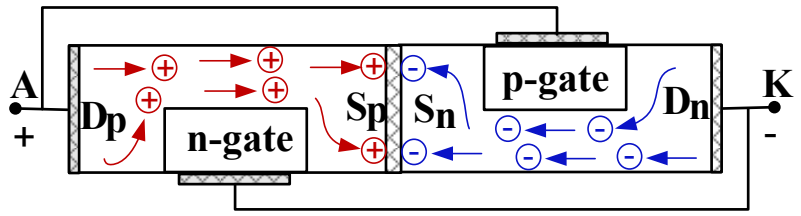
As shown in Fig. 3.2(a), the region A exhibits the bipolar state of the device, region B exhibits the unipolar state of the device, region C exhibits the flow of a small reverse peak current through the device till an approximate value of -1 V, region D exhibits the blocking state of the device i.e. very small reverse leakage current (reverse saturation current like in normal p-i-n diodes) is flowing through the device and finally region E exhibits breakdown state of the device.

## 3.2 Operation of the Regenerative Diode

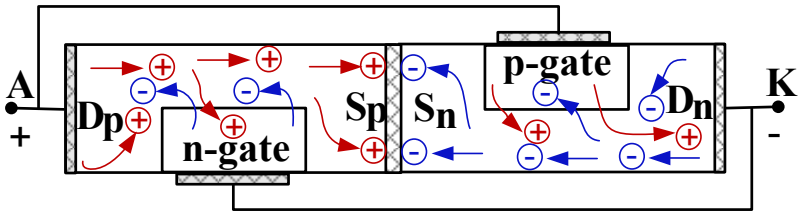
This section describes the operation of the Regenerative diode in the forward and reverse directions.

### 3.2.1 Forward direction

As shown in Fig. 3.3 the device is the combination of normally-on (depletion type) p-channel JFET and n-channel JFET. In normally-on JFETs, the channel is open at thermal equilibrium (the channel is not completely depleted by the built in potential of the gate to channel). As shown in Fig. 3.3, the drains ($D_p$ and $D_n$) of the p-channel JFET and n-channel JFET act as anode (A) and cathode (K) respectively and the sources ($S_p$ and $S_n$) of both the transistors are connected together (shorted by a contact). The n-gate (n-bulk) of the p-channel JFET is connected to the cathode terminal and the p-gate (p-bulk) of the n-channel JFET is connected to the anode terminal. In the forward direction, a positive voltage is applied to the anode with respect to the cathode. When a positive voltage is applied to the anode, in the p-channel JFET, the holes flow from the drain ($D_p$) to the source ($S_p$) through the p-channel and in the n-channel JFET, the electrons flow from the drain ($D_n$) to the source ($S_n$) through the n-channel. The flow of the carriers in the device is illustrated in Fig. 3.3. Both holes and electrons which come from the drains of the transistors reach the sources of the transistors. The hole (electron) current is transformed to electron (hole) current through the metal contact which is ohmic and usually approximated as an interface with infinite generation-recombination velocity. The Regenerative diode acts as a unipolar device at low current densities because the current flow is only due to the majority carriers (as shown in Fig. 3.3(a), the current flow is only due to holes in the p-channel JFET and is due to electrons in the n-channel JFET).




(a)




(b)

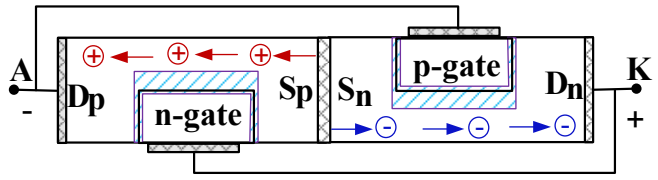
**Fig. 3.3** The Regenerative diode in the forward direction **(a)** at lower current densities **(b)** at higher current densities

With an application of positive anode potential, the channels resistance decreases and hence the conductance of channels increases when compared to that of the equilibrium case. At thermal equilibrium, the depletion layer is present at the junction between gate and channel due to the built in potential and is decreased in the forward direction (the p-gate in the n-channel JFET is at positive potential when compared to the drain of the n-channel JFET and the n-gate in the p-channel JFET is at negative potential when compared to the drain of the p-channel JFET). The current flow in the device increases with an increase of the anode voltage. With the further increase of the anode voltage (at higher currents), the junctions between n-gate and p-channel, p-gate and n-channel become forward biased and inject minority carriers as shown in Fig. 3.3(b). These junctions become forward biased and inject minority carriers when the voltage across the junction reaches about 0.6 V. The Regenerative diode acts as a unipolar device until these junctions become forward biased after which it changes its state from unipolar to bipolar. The I-V characteristics of the Regenerative diode are shown in Fig. 3.2(a).

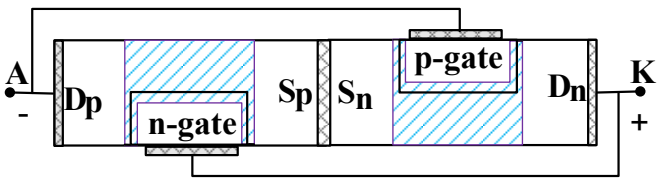
For low voltage applications, usually unipolar diodes are preferable with low reverse leakage current because they have better reverse recovery transient characteristics. The device should become bipolar at higher currents to ensure a surge current capability. The Regenerative diode has such type of characteristics.

### 3.2.2 Reverse direction

In the reverse direction a negative voltage is applied to the anode with respect to the cathode. When a negative voltage is applied to the anode, due to the normally-on state behavior of the device, a small reverse peak current as shown in Fig. 3.2(a) is flowing in the device. In the reverse direction, as shown in Fig. 3.4(a), the holes flow from the source ($S_p$) to the drain (anode terminal) of the p-channel JFET and electrons flow from the source ($S_n$) to the drain (cathode terminal) of the n-channel JFET.




(a)




(b)

**Fig. 3.4** The Regenerative diode in reverse bias **(a)** at very low voltages **(b)** at low, intermediate and high voltages

However, after a small anode voltage (~ - 1V), this reverse peak current reduces to a very small value as shown in Fig. 3.2(a). The reason is that the junctions between the gates and the channels become reverse biased. Therefore, the depletion layer across these junctions increases and penetrates into the channels[1]. This is illustrated in Fig. 3.4(a). This process is a regenerative action and has a positive feedback meaning with increasing reverse bias, the junctions are more reverse biased and therefore the depletion layer across the junctions increases further and penetrates more into the channels. Therefore, the effective width of the channels decreases and there by the reverse peak current decreases. For further increase of the anode voltage, the channels are completely closed by the depletion layer and hence there is no current flow through the channels and thereby no current flow in the device. This is illustrated in Fig. 3.4(b). However, after certain reverse voltage, a very small reverse leakage current (reverse saturation current), like in normal p-i-n diodes, is flowing in the device due to the thermal generation of the carriers.

## 3.3 Regenerative Diode for High Voltage Applications

The basic Regenerative diode (shown in Fig. 3.4) cannot be used for high voltage applications because this structure does not have a low doped region (usually $n^-$-drift region) to support high voltages. For high voltage applications, the basic schematic structure of the Regenerative diode is slightly modified and is illustrated in Fig. 3.5. In this structure, the $n^-$-drift region is introduced to support high blocking voltages. The blocking voltage of the device depends on the thickness and doping of the $n^-$-drift region.

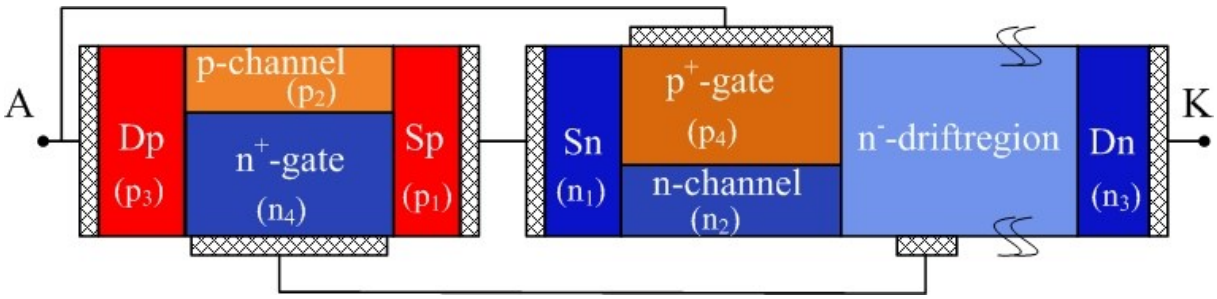



**Fig. 3.5** Schematic structure of the Regenerative diode for high voltage applications

As shown in Fig. 3.5, the $n^+$-gate of the p-channel JFET is connected to the $n^-$-drift region of the n-channel JFET. Therefore the potential to the $n^+$-gate is supplied from the $n^-$-drift region. Fig. 3.6 illustrates one of the possible integrated versions of the Regenerative diode for high voltage applications. The possible integrated version of the Regenerative diode (shown in Fig. 3.6) is developed from the schematic structure of the Regenerative diode which is shown in Fig. 3.5. Two dimensional iso-thermal simulations have been performed to the integrated structure at room temperature to obtain the forward and reverse I-V characteristics which are illustrated in Fig. 3.7.

[1] The gates are more heavily doped than the channels. At the junction, with an increasing reverse bias, the depletion layer or space charge layer penetrates more into the low doped region.

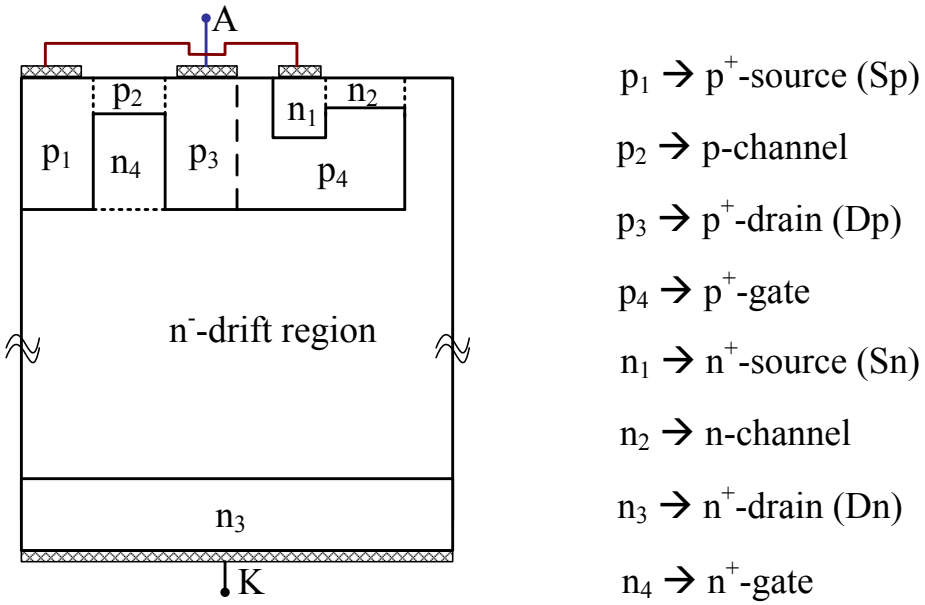



**Fig. 3.6** One of the possible integrated versions of the Regenerative diode

Here it describes the operation of the integrated structure in the forward and reverse directions. In the forward direction, the holes flow from the region $p_3$ to the region $p_1$ through the channel region $p_2$. The potential of the region $p_1$ is transferred to the region $n_1$. However, the region $n_1$ is at positive potential when compared to that of the region $n_3$. Therefore the electrons flow from the region $n_3$ to the region $n_1$. Fig. 3.7(a) illustrates the forward I-V characteristics of the Regenerative diode. The Regenerative diode acts as a unipolar device (the current flow in the device is only due to majority carriers) until the voltage across the device reaches 0.65 V after which it becomes bipolar. The reason being that the junction between the region $p_3$ and $n^-$-drift region becomes forward biased and injects minority carriers into the drift region and now the device is filled with electron-hole plasma.

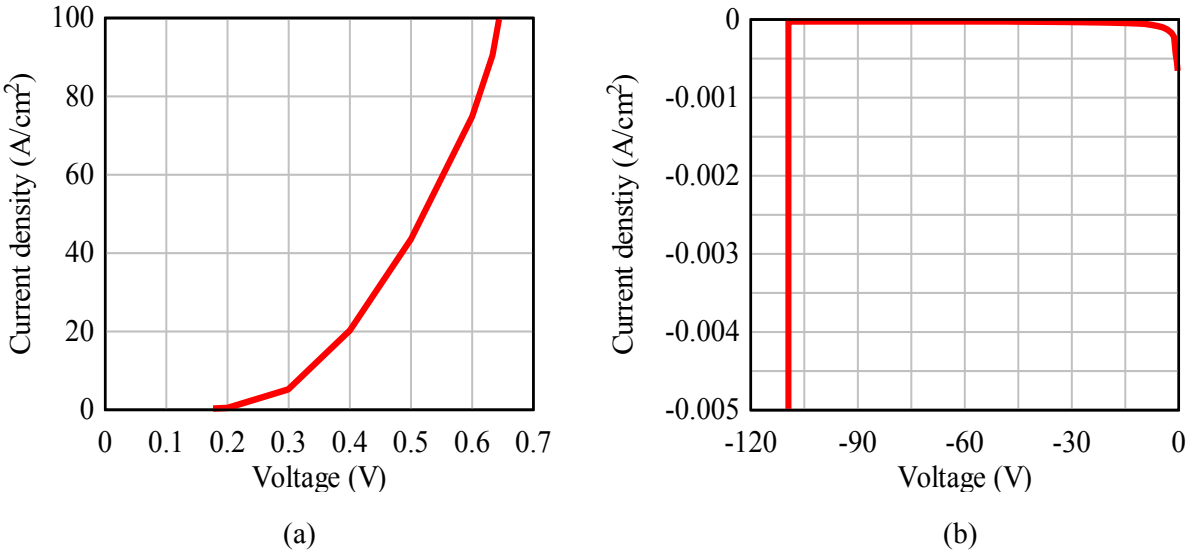



**Fig. 3.7** The I-V characteristics of the Regenerative diode **(a)** Forward bias **(b)** Reverse bias

In the reverse bias, a small reverse peak current is flowing in the device (0.7 mA/cm$^2$ @ -0.25 V), as shown in Fig. 3.7(b), due to the on-state behavior of the device. However, the region $n_4$ ($n^+$-gate) is at positive potential compared to that of the channel $p_2$ and the region $p_4$ ($p^+$-gate) is at negative potential compared to that of the channel $n_2$. Therefore the depletion layer builds up across the junctions between $n_4$ and $p_2$, $p_4$ and $n_2$. This results in a reduction of the effective width of the channels and hence the current flow decreases. With the increase of anode voltage, the reverse peak current reduces to a very small value because the depletion layer width increases across both the channels and depletes the channels completely. In addition, the junctions between $p_3$ and $n^-$-drift region, $p_4$ and $n^-$-drift region, $p_1$ and $n^-$-drift region are also reverse biased. Therefore with the increase of the anode voltage, the depletion layer penetrates into the $n^-$-drift region and sustains (blocks) high voltages. For further increase of the anode voltage, the device enters into the breakdown condition at certain voltage when the electric field at the junction ($p_3$ and $n^-$-drift region) reaches the breakdown electric field. After this voltage the device is no longer in blocking condition and huge amount of current is flowing in the device due to the avalanche generation of the carriers at the junction ($p_3$ and $n^-$-drift region). As shown in Fig. 3.7(b), this device can block or support about 100 V after which it enters into the breakdown condition.

### 3.3.1 Adding an additional MOS-gate to the n-channel of the device

The forward I-V characteristics of the Regenerative diode is improved considerably by adding an additional MOS-gate (it is treated as an $n^+$-polysilicon gate), as shown in Fig. 3.8, to the n-channel ($n_2$) of the device. As shown in Fig. 3.8, the MOS-gate is connected to the anode terminal and therefore the potential to the MOS-gate is supplied from the anode contact.

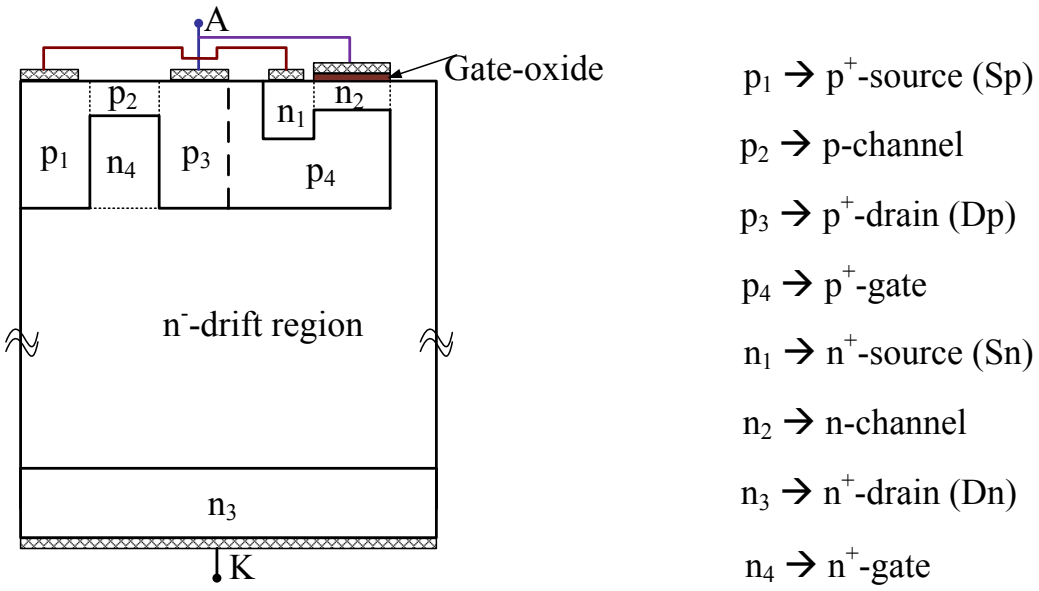



**Fig. 3.8** Integrated version of the Regenerative diode with the MOS gate

In the forward bias, the MOS-gate at positive potential causes accumulation of electrons in the n-channel (in fact, even at thermal equilibrium there is an accumulation of electrons in the n-channel due to the work function difference between $n^+$-polysilicon gate and n-channel. In the reverse bias, the MOS-gate at negative potential causes depletion of electrons in the channel. Therefore, even higher doping of the n-channel is possible.

Fig. 3.9 illustrates the comparison of the I-V characteristics between the Regenerative diode with MOS-gate (shown in Fig. 3.8) and the Regenerative diode without MOS-gate (shown in Fig. 3.6), in the forward direction. As shown in Fig. 3.9(a), there is a considerable improvement in the forward I-V characteristic by adding MOS-gate to the basic structure of the Regenerative diode (the device doping and dimensions remain the same).

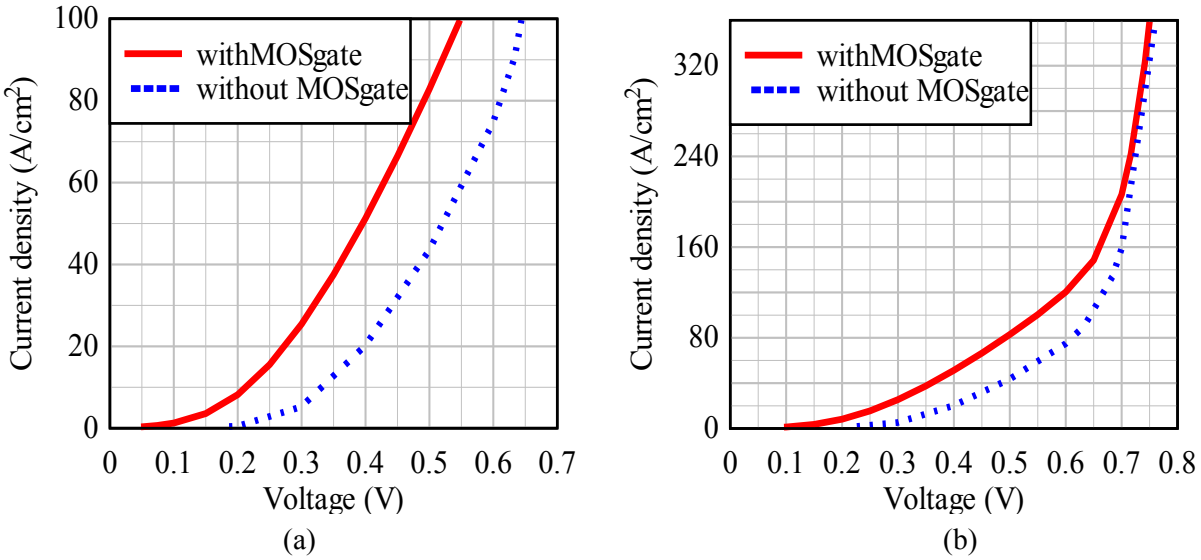



**Fig. 3.9** Comparison of the forward bias (simulated) I-V characteristics between the Regenerative diode with and without MOS-gate **(a)** at low current densities **(b)** at higher current densities

As shown in Fig. 3.9(a), at 0.4 V, the device with MOS-gate carries 2.5 times higher current than that of the device without MOS-gate. However, in both the cases (the device with and without MOS-gate), the device changes its state from unipolar to bipolar nearly at the same current density i.e. about 140 A/cm$^2$. The reason is that the junction between $p_3$ and $n^-$-drift region becomes forward biased and starts injecting minority carriers. Beyond 0.7 V, as shown in Fig. 3.9(b), the current density is same in both the cases because of the bipolar action. The MOS-gate has much influence on the current flow until the device change its state from unipolar to bipolar because the current flows through the channels only when the device is in unipolar state and the MOS-gate enhances the channel conductivity by accumulating the charge carriers (electrons).

In the reverse direction, however, the reverse peak current (0.34 A/cm$^2$ @ -0.25 V), as shown in Fig. 3.10(b), increases with the MOS-gate but this peak current is not high and is still in the reasonable limits. After -0.25 V, the reverse peak current reduces to a small value and beyond -1 V, the reverse leakage current is same as in the case of without MOS-gate. The blocking capability of the device, as shown in Fig. 3.10(a), is same in both the cases because the drift

region doping and dimensions are same in both the cases. The device blocking capability depends on the doping and dimensions of the drift region of the device.

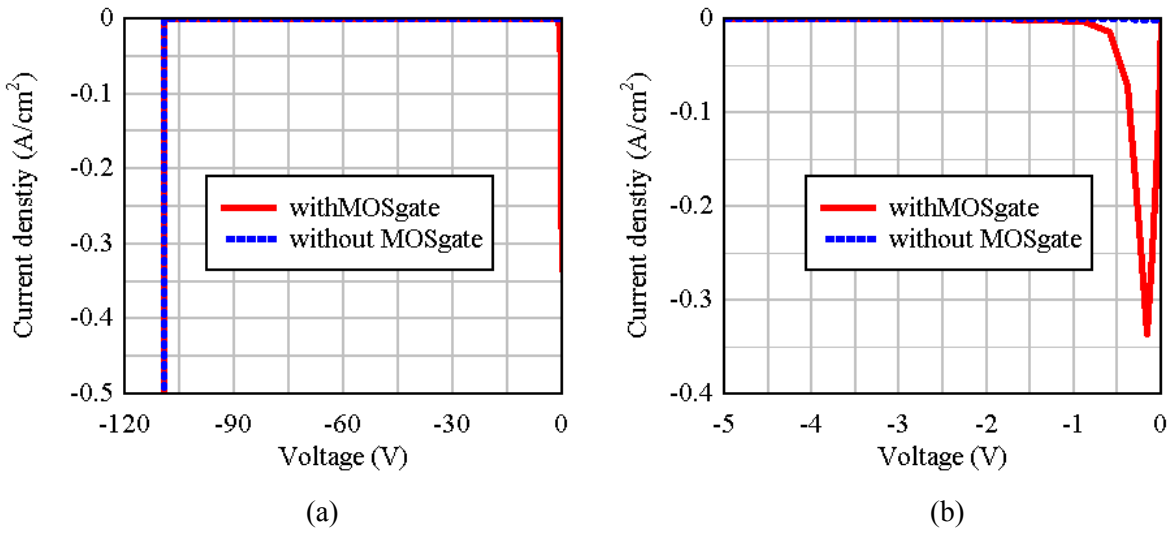



**Fig. 3.10** **(a)** Comparison of the reverse bias (simulated) I-V characteristics between the Regenerative diode with and without MOS-gate **(b)** zoomed version of the right side figure at low voltages

### 3.3.2 The trench Regenerative diode

Still there is room to improve the on-state behavior (reduce the conduction losses) of the Regenerative diode by shrinking the area of the device. To obtain this, the planar MOS-gate structure has to be replaced by the trench-MOS-gate structure.

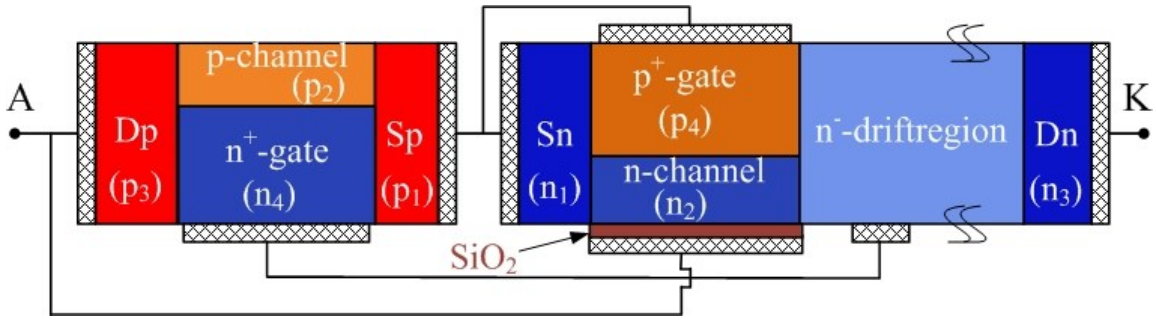



**Fig. 3.11** Schematic structure of the trench Regenerative diode

The basic schematic structure of the Regenerative diode (Fig. 3.5) for high voltage applications has been slightly modified to obtain the schematic structure of the trench Regenerative diode which is illustrated in Fig. 3.11. In this structure, unlike as in Fig. 3.5, the potential to the $p^+$-gate is supplied from the sources of the transistors. Therefore, the current flow in the n-channel JFET is only controlled by the trench MOS-gate of the n-channel JFET. Fig. 3.12 illustrates one of the possible integrated versions of the trench Regenerative diode (shown in Fig. 3.11).

In the integrated structure, in forward bias, the holes flow from the region $p_3$ to the region $p_1$ and the electrons come from the region $n_3$ to the $n_1$ (the regions $n_1$ and $p_1$ are heavily doped and shorted by a contact). The hole (electron) current is transformed to electron (hole) current

through the metal contact which is ohmic and usually approximated as an interface with infinite generation-recombination velocity.

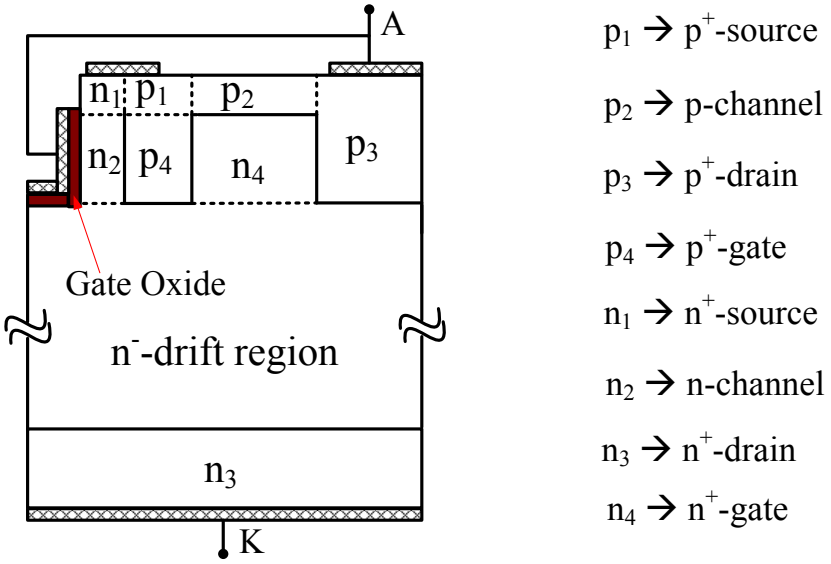



**Fig. 3.12** Integrated version of the trench Regenerative diode

In reverse bias, a small reverse peak current is flowing in the device and after a very small voltage (about -0.5 V), the reverse current reduces to a small value because the depletion layer (the junction between the region $n_4$ and channel $p_2$ is reverse biased) closes the channel $p_2$ and the MOS gate depletes the channel $n_2$.

Two dimensional iso-thermal simulations have been performed to the integrated structure (shown in Fig. 3.12) to obtain the I-V characteristics and these characteristics have been compared with that of the I-V characteristics of the planar Regenerative diode (shown in Fig. 3.8). The channels length, width and doping are considered same in both the devices. In addition, both devices have the same doping and thickness of the $n^-$-drift region. Fig. 3.13 illustrates the comparison of the I-V characteristics between the planar Regenerative diode and trench Regenerative diode at 300 K.

As shown in Fig. 3.13(a), the conduction losses are low in the trench Regenerative diode compared to that of the planar Regenerative diode. The reason is that the trench Regenerative diode can be constructed in a smaller chip area compared to that of the planar Regenerative diode. As shown in Fig. 3.13(a), like the planar Regenerative diode, the trench Regenerative diode also becomes bipolar when the voltage across the device reaches about 0.65 V but the current densities are different. As shown in Fig. 3.13(b), the blocking capability is nearly the same in both the devices but the reverse peak current is slightly higher in case of the trench Regenerative diode compared to that of the planar Regenerative diode.

In fact, here the main aim is to improve the on-state (forward) characteristics of the Regenerative diode in the unipolar state (before the device becomes bipolar). For low voltage applications, generally unipolar diodes are preferable with low reverse leakage current because they have better reverse recovery transient characteristics (no plasma in the device).

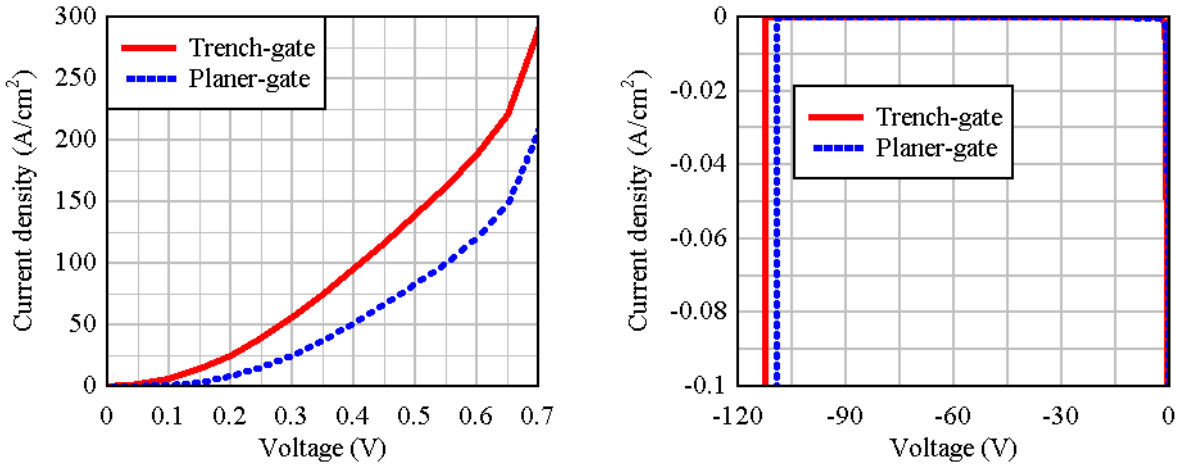



**Fig. 3.13** Comparison of the I-V characteristics between the planar and trench Regenerative diode **(a)** Forward bias **(b)** Reverse bias

To further improve the on-state behavior of the trench Regenerative diode in unipolar state, the channel charge has been increased. The channel charge can be increased either by widening the width of the channel or increasing the doping of the channel. Fig. 3.14 illustrates the comparison of the I-V characteristics at 300 K between two trench Regenerative diodes which have the same structure except the doping of the channels (p-channel and n-channel).

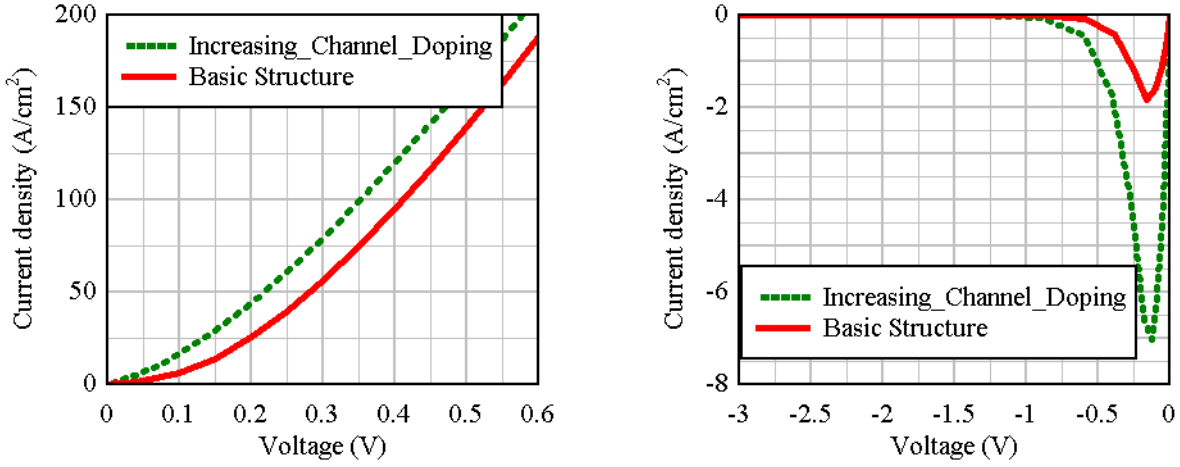



**Fig. 3.14** Comparison of the I-V characteristics at 300 K between two trench Regenerative diodes which have the same structure except the doping of the channels **(a)** Forward bias **(b)** Reverse bias

In one structure (i.e., the basic structure), the doping of the channels is $4e^{16}$ $cm^{-3}$ and the Gummel number[2] of the channels is $4e^{11}$ $cm^{-2}$, whereas in another structure the doping of the channels is increased from $4e^{16}$ $cm^{-3}$ to $4.5e^{16}$ $cm^{-3}$ meaning the Gummel number of the channels is increased from $4e^{11}$ $cm^{-2}$ to $4.5e^{11}$ $cm^{-2}$. As shown in Fig. 3.14(a), the conduction

[2] Gummel number of the n-channel is $\int_0^{Wn} N_D.dx$; where Wn is the width of the n-channel and $N_D$ is the donor concentration in the n-channel.

losses are further reduced (i.e. the on-state behavior is improved) with the increase of the charge in both the channels by increasing the doping of the channels. However, as shown in Fig. 3.14(b), the reverse peak current increases with the increase of the doping of the channels but the reverse leakage current (after -1.5 V) is nearly the same as in the case of basic structure. However, the reverse peak current is relatively higher (about 3.5 times) in this case and it should be minimized.

### 3.3.3 Delay in the bipolar action of the trench Regenerative diode

The trench Regenerative diode as shown in Fig. 3.12 becomes bipolar when the junction between $p_3$ ($p^+$-drain) and $n^-$-drift region becomes forward biased and injects minority carriers. This occurs when the voltage across the device reaches about 0.65 V. The bipolar action of the device could be delayed by changing the design of the device structure. Fig. 3.15(a) illustrates the trench Regenerative diode in which the bipolar action is delayed i.e., the device will not become bipolar at 0.65 V or 200 A/cm$^2$ but it does at higher voltages/current densities. Therefore, the operation area of the device is improved considerably in the unipolar state. Fig. 3.15(b) illustrates the equivalent circuit of this structure. Here the regions $p_3$, $n_4$, $p_4$ are represented by a p-n-p transistor, the junction between $p_4$ and $n^-$-drift region is represented by a diode, the region $p_2$ is represented by a p-channel resistor, the region $n_2$ is represented by a n-channel resistor and the drift region is represented by a $n^-$-drift region resistor.

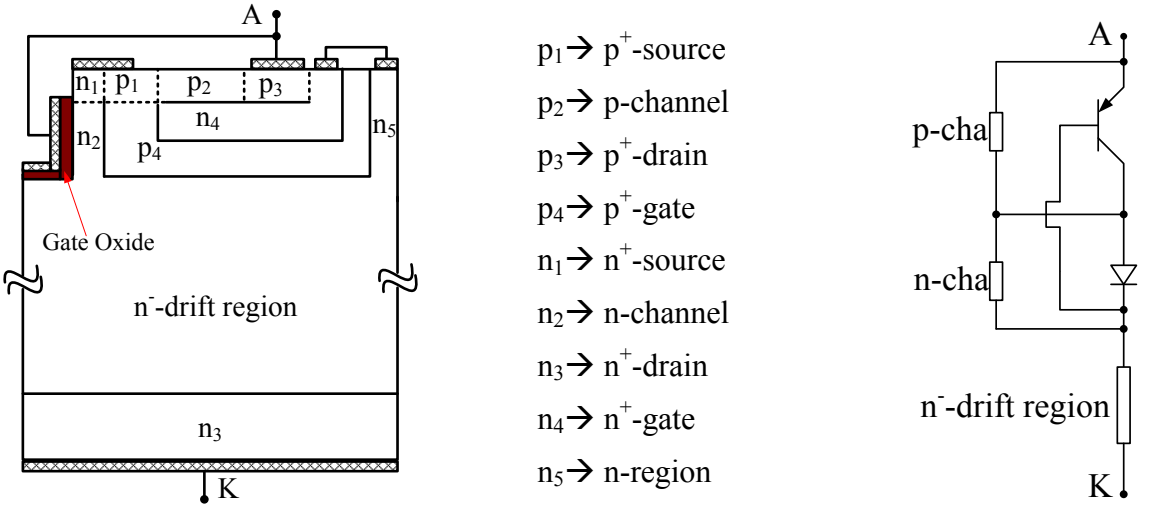



**Fig. 3.15** Delayed bipolar action of the trench Regenerative diode **(a)** Schematic structure **(b)** Equivalent circuit

Unlike in the structure shown in Fig. 3.12, there is no direct junction between $p_3$ ($p^+$-drain) and $n^-$-drift region but the junction exists between $p_4$ and $n^-$-drift region. As shown in Fig. 3.15, the potential to the region $n_4$ ($n^+$-gate) is supplied from the region $n_5$ (n-region). This structure becomes bipolar when the junction between $p_4$ and $n^-$-drift region becomes forward biased and injects minority carriers. This happens when the voltage across this

junction is about 0.5 to 0.6 V. This takes place only at higher currents or at high voltages across the device. In this structure initially the current flow is unipolar (like in the structure shown in Fig. 3.12) and flows from anode to cathode via p-channel, n-channel and $n^-$-drift region. At higher currents, the voltage drop in the channels become high and the diode will be forward biased and also the pnp transistor is activated. The pnp transistor is operated in saturation region (both emitter-base and collector-base junctions are forward biased). As shown in Fig. 3.16, when it changes from unipolar to bipolar, the voltage remains constant until some current density in spite of increasing the junction potential of the diode. The reason being that the $V_{CE}$ of the pnp transistor decreases nearly to zero and also the drift region is conductivity modulated (the drift region is filled with electron-hole plasma).

The comparison of the simulated I-V characteristics between two different structures (Fig. 3.12 and Fig. 3.15) of the Regenerative diode are illustrated in Fig. 3.16. For the comparison, the same doping and dimensions of the channels are considered in both the structures. In addition, the same doping and dimensions of the $n^-$-drift region is considered in the both the structures.

As shown in Fig. 3.16(a), the on-state characteristics are almost same in both the structures until the structure shown in Fig. 3.12 becomes bipolar. In addition, as shown in Fig. 3.16(b), the blocking characteristics such as the reverse peak current and reverse leakage current are also the same in both the structures. As shown in Fig. 3.16(a), the structure shown in Fig. 3.12 becomes bipolar around 0.65 V or 200 A/cm$^2$, whereas the structure shown in Fig. 3.15 becomes bipolar around 0.9 V or 300 A/cm$^2$. Therefore, the current handling capability of the device in the unipolar state is increased by delaying the bipolar action of the device. Fig. 3.17 illustrates the hole and electron current densities of the trench Regenerative diode (shown in Fig. 3.12) whereas Fig. 3.18 illustrates the hole and electron current densities of the trench Regenerative diode (shown in Fig. 3.15) in which the bipolar action is delayed.

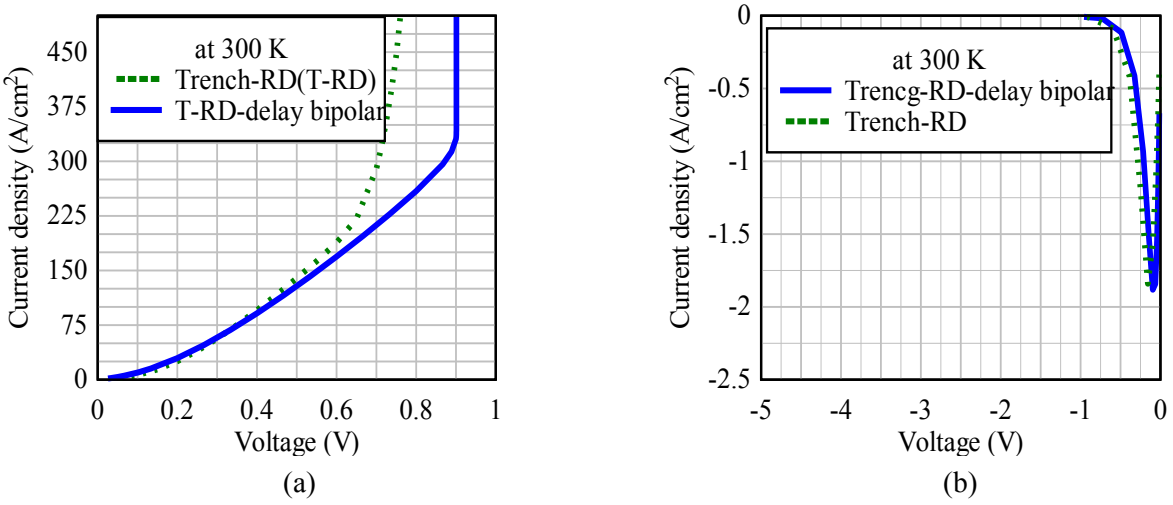



**Fig. 3.16** Comparison of the I-V characteristics between two different Regenerative diodes (trench RD and trench RD in which the bipolar action is delayed) at 300 K **(a)** Forward bias **(b)** Reverse bias

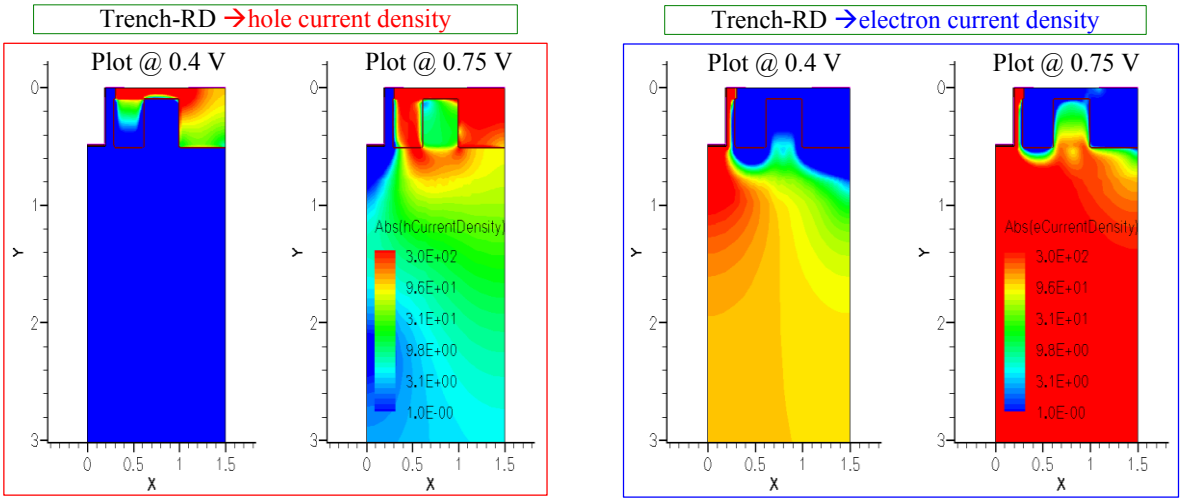
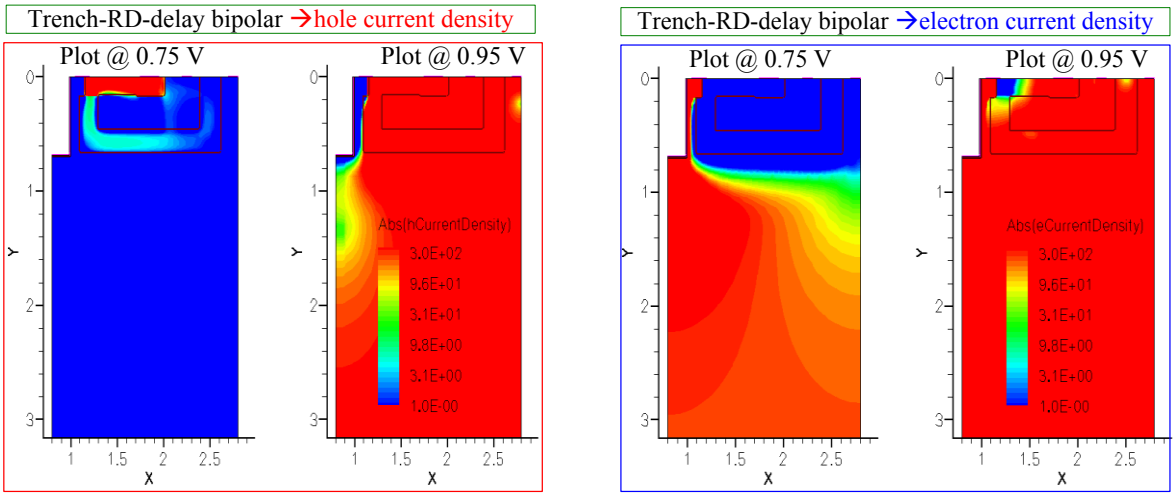
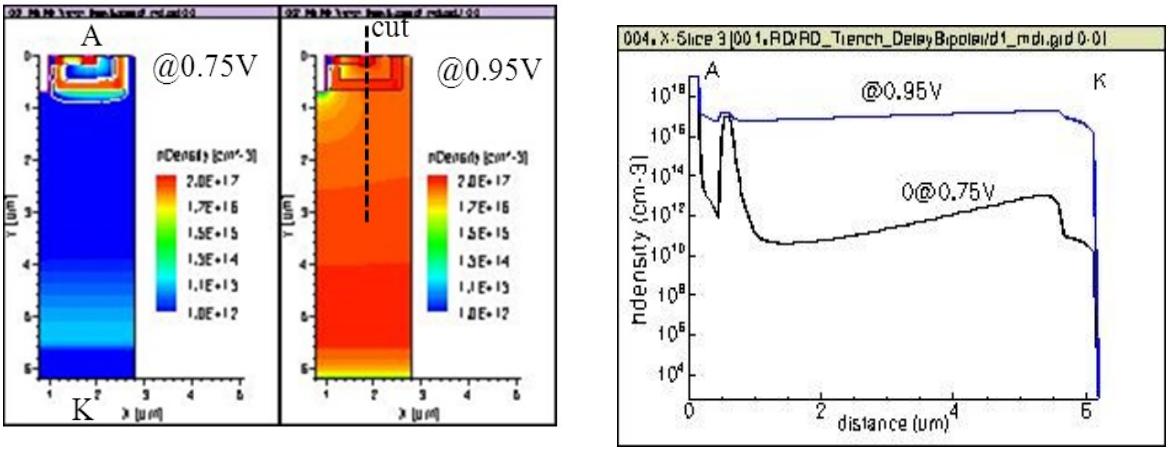



**Fig. 3.17** Hole and electron current densities of the trench Regenerative diode (shown in Fig. 3.12)




(a) (b)




(c) (d)

**Fig. 3.18** Trench Regenerative diode in which the bipolar action is delayed (shown in Fig. 3.15) (a) and (b) Hole and electron current density distribution (c) and (d) hole density @0.75 V and 0.95 V

As shown in Fig. 3.17, at 0.4 V (plot @ 0.4 V), the device (shown in Fig. 3.12) is in unipolar state because the holes flow only from p-drain to p-source through the p-channel and electrons flow only from n-drain to n-source through the n-channel (there is no carrier injection across the p-n junction). At 0.75 V (plot @ 0.75 V), the device is already in bipolar state because there is a carrier injection across the p-n junction (p-drain and p-source injects holes into n-drift region and n-drift region injects electrons into p-region). However, the structure shown in Fig. 3.15 is still in unipolar state even at 0.75 V (this can be seen from plot @ 0.75 V in Fig. 3.18) but becomes bipolar after 0.9 V (from plot @ 0.95 V in Fig. 3.18). Fig. 3.19 illustrates the comparison of the I-V characteristics between two different structures (shown in Fig. 3.12 and Fig. 3.15) at 400 K. It can be seen from Fig. 3.19 that even at 400 K the bipolar action of the device is delayed in structure shown in Fig. 3.15 when compared to that of the structure shown in Fig. 3.12.

Unipolar devices with low on-state losses and less blocking current are preferable compared to that of the bipolar devices due to their good reverse recovery transient characteristics. This results in less switching losses and hence the devices can be used in high switching frequency applications.

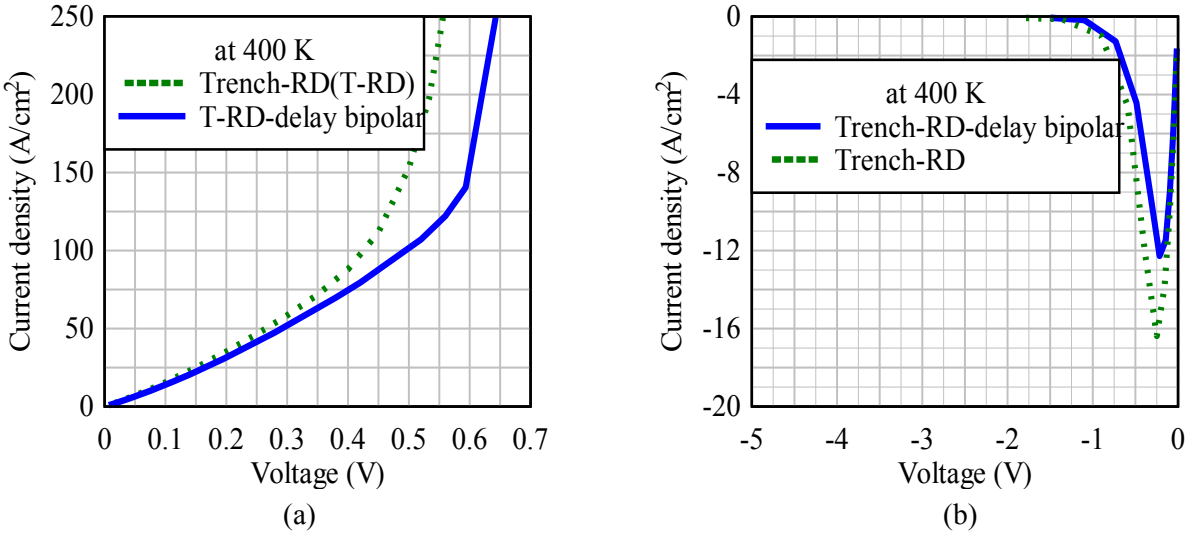



**Fig. 3.19** Comparison of the I-V characteristics between two different Regenerative diodes (trench RD and trench RD in which the bipolar action is delayed) at 400 K **(a)** Forward bias **(b)** Reverse bias

## 3.4 Considered Regenerative Diode

As explained in the section 3.3.2, the on-state characteristics can be improved by increasing the channel doping or widening the channel but at the same time the reverse peak current also increases. There is a trade-off between on-state characteristics and reverse peak current. The aim is to improve further, the on-state characteristics of the Regenerative diode in unipolar state without increasing the reverse peak current. This can be achieved by increasing the channels doping and adding an additional MOS-Gate (it is treated as an $n^+$-polysilicon gate) to the p-channel.

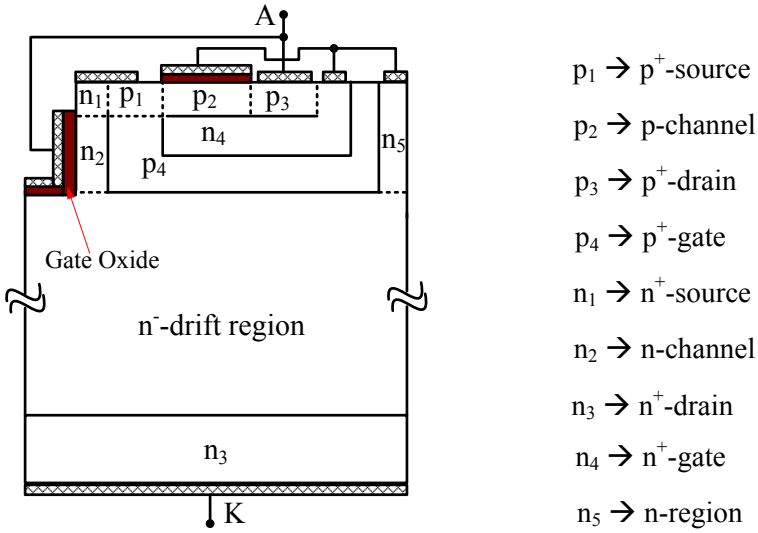
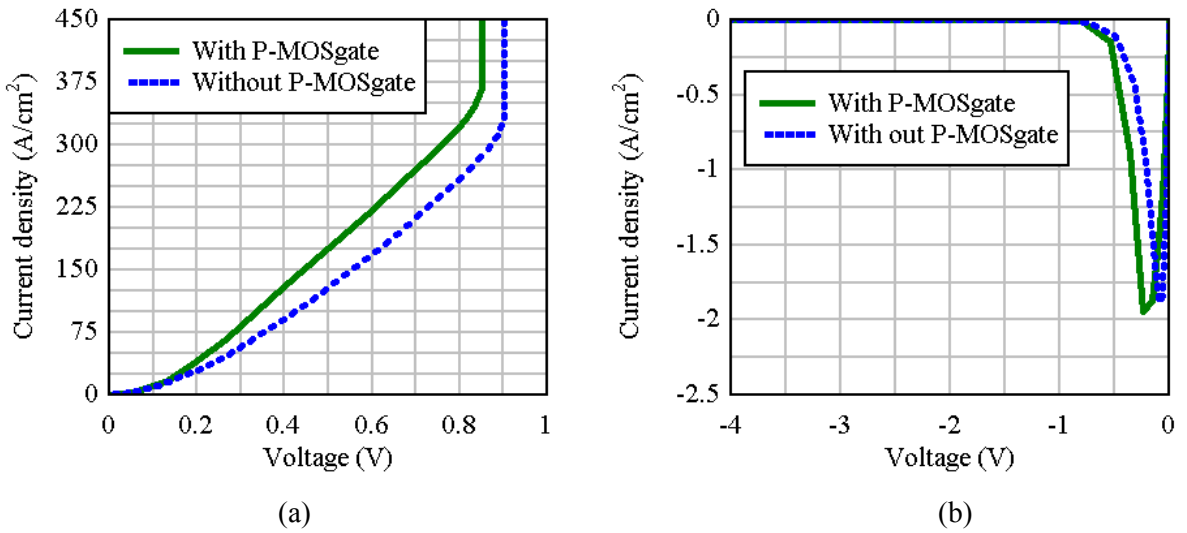



**Fig. 3.20** Integrated structure of the considered Regenerative diode

An integrated version of the modified and considered Regenerative diode is illustrated in Fig. 3.20. In this structure, the potential to the p-MOS-Gate is supplied from the n-region ($n_5$) as shown in Fig. 3.20. Fig. 3.21 illustrates the comparison of the I-V characteristics between with and without p-MOS-Gate Regenerative diodes. As shown in Fig. 3.21(a), there is not much difference in forward characteristics between with and without p-MOS-Gate devices till 0.1 V, though the doping is high in the channels in case of the device with p-MOS-Gate. In without p-MOS-Gate device, at thermal equilibrium, the effective width of the p-channel is reduced due to the diffusion potential from $n_4$ (n-gate region) whereas in the device with p-MOS-Gate, the effective width of the p-channel is much reduced due to diffusion potential from $n_4$ and depletion of the channel from p-MOS-Gate (at thermal equilibrium, the p-channel is depleted due to the work function difference between $n^+$-polysilicon gate and p-channel). However, the effective width of the channel increases with the increase of the positive anode potential. Therefore, the device with the p-MOS-Gate has better on-state characteristics compared to that of the device without p-MOS-Gate after 0.1 V until device becomes bipolar. After the devices become bipolar, the on-state characteristics are nearly the same in both the devices.




(a) (b)

**Fig. 3.21** Comparison of the I-V characteristics between with and without p-MOS-Gate of the Regenerative diode **(a)** Forward bias **(b)** Reverse bias

As shown in Fig. 3.21(b), the magnitude of the reverse peak current is nearly the same in both the devices, though the doping of the channels is high in case of the device with p-MOS-gate. In addition, the reverse leakage current is also nearly the same in both the devices. For the same reverse peak current, the on-state characteristics are improved as shown in Fig. 3.21 with the p-MOS-Gate (considered Regenerative diode).

## 3.5 Temperature Dependence of the Regenerative diode

This section investigates the temperature dependence of electrical characteristics of the considered Regenerative diode. Two dimensional iso-thermal device simulations have been performed at different temperatures. Fig. 3.22 illustrates the forward I-V characteristics of the Regenerative diode at 300 K, 400 K and 450 K. Fig. 3.22(b) is the zoomed version of the Fig. 3.22(a) but the I-V characteristics are illustrated only for two temperatures that are 300 K and 400 K. It can be observed from Fig. 3.22(b) that the conductivity of the device increases with the temperature until a certain voltage i.e., 0.2 V after which the conductivity decreases until the device becomes bipolar. The cause for increase in conductivity with the temperature until 0.2 V is the decrease of the diffusion voltage (built in potential). This causes channels to be more open and hence high conductivity. The dependence of the diffusion voltage on temperature can be explicitly seen from the following equations [Sze'81]

$$V_d = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^{\,2}}\right) \tag{1}$$

$$n_i^{\,2} = N_C N_V \exp\left(-\frac{E_g}{kT}\right) \tag{2}$$

insert equation (2) into equation (1) and then

$$V_d = \frac{E_g}{q} - \frac{kT}{q}\ln\left(\frac{N_C N_V}{N_A N_D}\right) \tag{3}$$

where $V_d$ is the diffusion voltage, q is elementary charge, $E_g$ is the band gap energy, k is the Bolltzmann constant, T is the absolute temperature, $n_i$ is the intrinsic carrier concentration, $N_A$ and $N_D$ are the acceptor and donor concentrations respectively and $N_C$ and $N_V$ are effective density of states in the conduction and valence bands respectively. It can be observed from equation (3) that the diffusion voltage decreases with increase in temperature.

As shown in Fig. 3.22(b), after 0.2 V, the conductivity decreases with the temperature until the device becomes bipolar. The reason being that the mobility decreases with the temperature. Like in unipolar device, this device has a positive temperature co-efficient of resistance until the device becomes bipolar. This device becomes bipolar at 0.85 V, 0.53 V and 0.4 V in case of 300 K, 400 K and 450 K respectively.

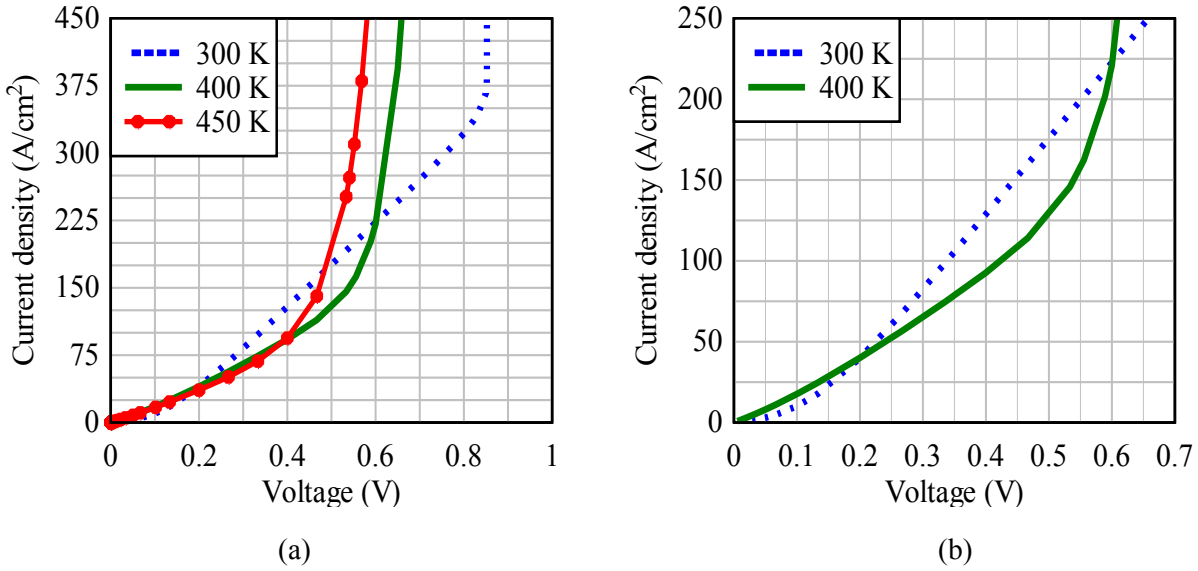



**Fig. 3.22 (a)** Forward bias I-V characteristics of the trench Regenerative diode at different temperatures **(b)** Zoomed version of the left side figure.

The reverse I-V characteristics of the Regenerative diode at different temperatures are illustrated in Fig. 3.23. The breakdown voltage of the device increases with the temperature. This is due to the decrease of the avalanche generation at the p-n junction with the temperature. However, the reverse leakage current increases with the temperature as shown in Fig. 3.23(b). This is due to the increase of the intrinsic carrier concentration with the temperature. Due to the normally-on state behavior of the device, there is a small reverse peak current flowing in the device which increases with the temperature as shown in Fig. 3.23(c). The maximum of this peak current is flowing only at very low voltages (less than -0.5 V). After -1.5 V, this reverse peak current reduces to a very small value (reverse leakage current)

due to the regenerative blocking capability of the device. The reverse leakage current of the Regenerative diode at 90 V is ~ 0.24 mA/cm$^2$ and 8 mA/cm$^2$ at 400 K and 450 K respectively.

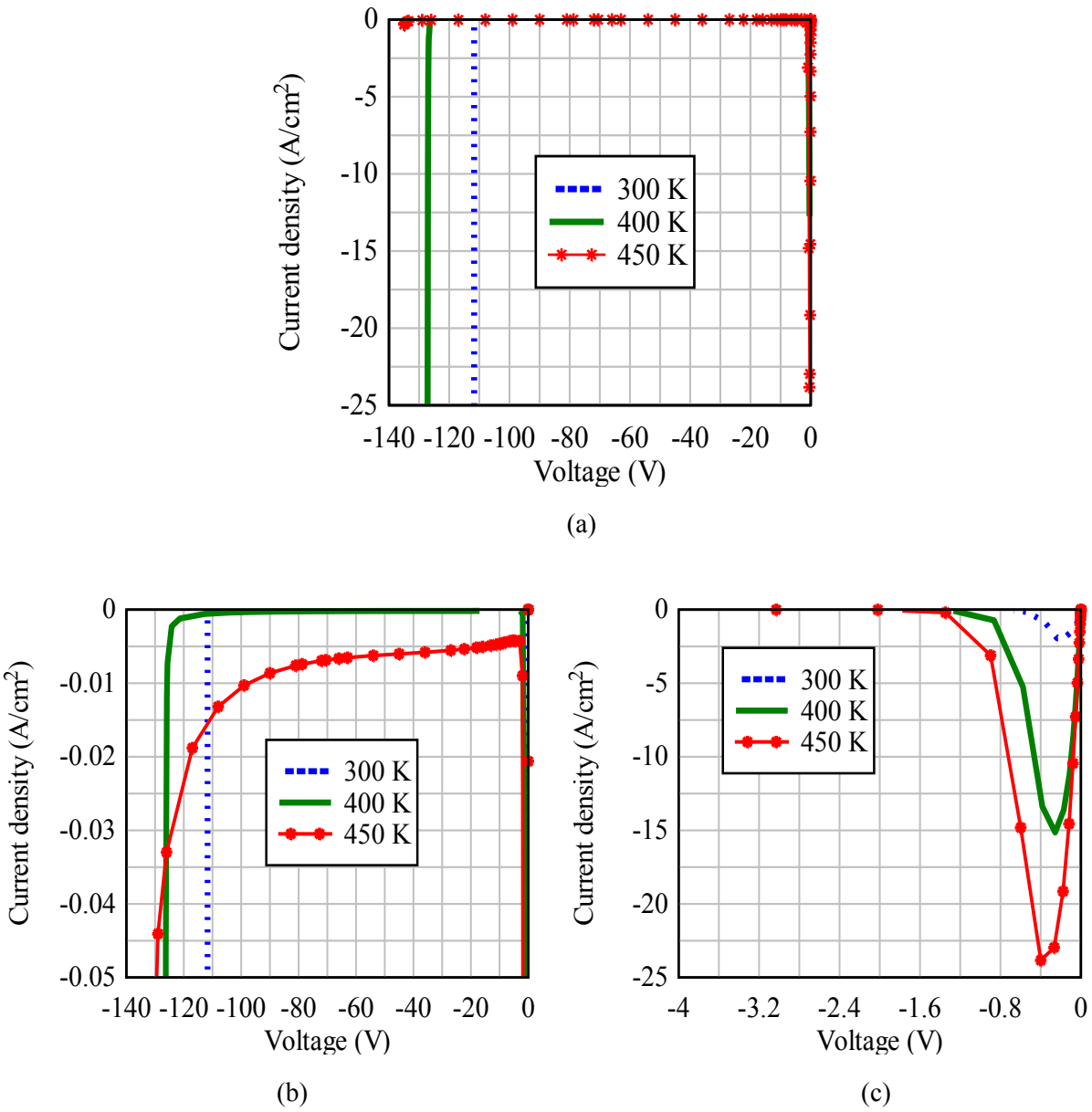



**Fig. 3.23 (a)** Reverse bias I-V characteristics of the Regenerative diode at different temperatures **(b)** Zoomed version of figure (a) at low currents **(c)** Zoomed version of figure (a) at low voltages

## 3.6 Comparison between Regenerative Diode and JBS/MPS Rectifier

This section presents the comparison of the static and dynamic characteristics between considered Regenerative diode and JBS/MPS rectifier at different temperatures. As explained in section 2.2, JBS/MPS rectifier is a combination of P-i-N diode and SBD or is a cascode connection between SBD and n-channel JFET. JBS rectifier is meant for low voltage applications (unipolar device applications) where as MPS rectifier is meant for high voltage applications (bipolar device applications). JBS also becomes bipolar when the voltage across the junction between p-gate and n-drift region is sufficient to inject carriers.

### 3.6.1 Static characteristics

This section describes the comparison of the static I-V characteristics between considered Regenerative diode (as shown in Fig. 3.20) and JBS rectifier (as shown in Fig. 2.4). For the comparison, it is considered that the doping and dimensions of the drift region are same in both the devices which can support 100 V. The doping and thickness of the drift region were $2.5e^{15}$ $cm^{-3}$ and 5 µm respectively.

Fig. 3.24(a) illustrates the comparison of the forward bias I-V characteristics between the Regenerative diode and the JBS rectifier. In the simulation the barrier height of the Schottky contact ($\Phi_{Bn}$, height of the potential barrier between the metal and the n-type semiconductor) in the JBS rectifier is considered 0.72 V [Stef'06]. The Schottky contact in the JBS rectifier conducts current from an approximate value of 0.3 V (threshold voltage) at 300 K and the current conduction is due to the majority carriers which are electrons in this case. JBS rectifier acts as a unipolar device until the voltage across the device reaches 0.6 V and 0.35 V at 300 K and 400 K respectively as shown in Fig. 3.24(a) after which the device becomes bipolar. The Regenerative diode is a normally-on device and acts as a unipolar device until the voltage across the device reaches 0.85 V and 0.53 V at 300 K and 400 K respectively. As shown in Fig. 3.24(a), the Regenerative diode is having better on-state characteristics compared to that of the JBS rectifier as long as the devices are in unipolar state. The forward current density values of the Regenerative diode and JBS rectifier at different voltages and temperatures are plotted in Table 3.1.

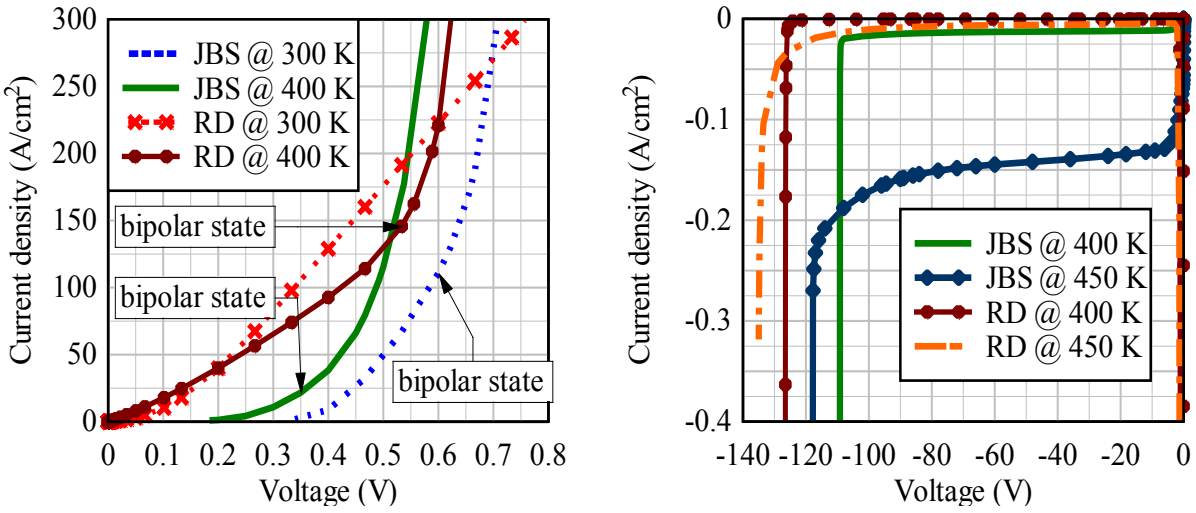



**Fig. 3.24** Comparison of the I-V characteristics between the Regenerative diode and the JBS rectifier **(a)** Forward bias **(b)** Reverse bias

Fig. 3.24(b) illustrates the comparison of the reverse bias I-V characteristics between the Regenerative diode and the JBS rectifier. Unlike in SBD, the reverse leakage current in JBS rectifier is relatively constant even with the increase of the anode potential as shown in Fig. 3.24(b). The reason being that the potential barrier which is formed by the reverse biased p-n junction in the channel, shields the Schottky contact from the applied reverse voltages and

prevents the Schottky barrier lowering. However, as shown in Fig. 3.24(b), the reverse leakage current in the Regenerative diode is small compared to that of the reverse leakage current in the JBS rectifier. The reverse leakage current density values of the Regenerative diode and JBS rectifier at -50 V and for different temperatures are plotted in Table 3.2. As shown in Fig. 3.24(b), both the devices are having positive temperature coefficient of breakdown voltage due to the decrease of the avalanche generation with the temperature.

| **Forward current density values** | | |
|---|---|---|
| Voltage @ Temperature | Regenerative Diode | JBS Rectifier |
| At 0.5 V @ 300 K | 178 A/cm$^2$ | 50 A/cm$^2$ |
| At 0.35 V @ 400K | 79 A/cm$^2$ | 22 A/cm$^2$ |

**Table 3.1** Forward current densities of the Regenerative diode and the JBS rectifier

| **Reverse leakage current density values at -50V** | | |
|---|---|---|
| Temperature | Regenerative Diode | JBS Rectifier |
| At 400 K | 0.2 mA/cm$^2$ | 11 mA/cm$^2$ |
| At 450K | 6 mA/cm$^2$ | 136 mA/cm$^2$ |

**Table 3.2** Reverse leakage current densities of the Regenerative diode and the JBS rectifier

In addition to the better on-state characteristics, the Regenerative diode is also having superior blocking characteristics than that of the JBS rectifier though a small reverse peak current is flowing in the device at very low reverse voltages. The reverse peak current of the Regenerative diode reduces to a small value at very low reverse voltages (less than 1 V). The reverse peak current of the Regenerative diode is not a problem when it comes to dynamic applications of the devices because the capacitive current of the device dominates and occurs in all the diodes (unipolar and bipolar).

### 3.6.2 Dynamic characteristics

This section presents the comparison of the dynamic current characteristics between considered Regenerative diode and JBS/MPS rectifier. The main aim of this section is to show that the reverse peak current that is flowing in the Regenerative diode is not a problem when it comes to the dynamic applications.

For the comparison of the dynamic characteristics between Regenerative diode and JBS/MPS rectifier, 200 V blocking capability devices (Regenerative diode and MPS rectifier) have been considered in the simulations. Fig. 3.25 illustrates the comparison of the static I-V characteristics between 200 V Regenerative diode and MPS rectifier in the forward direction at 300 K.

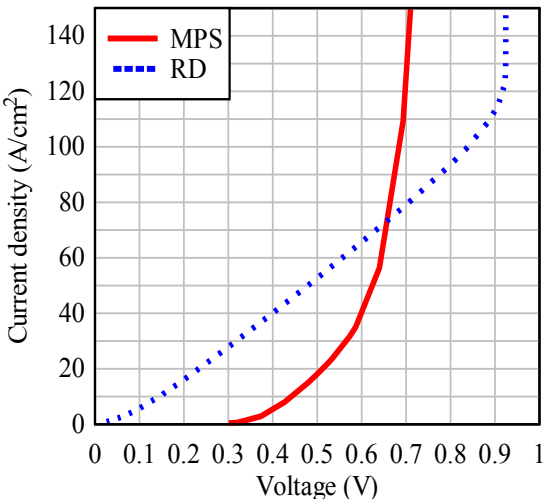



**Fig. 3.25** Comparison of the forward bias I-V characteristics between 200 V Regenerative diode and MPS rectifier at 300 K

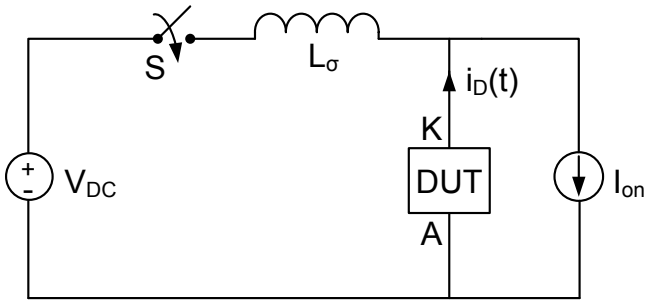



**Fig. 3.26** The circuit which is used to simulate the dynamic characteristics of the Regenerative diode and JBS/MPS rectifier

Fig. 3.26 illustrates the circuit which is used to simulate the dynamic characteristics of the devices. The comparison of the dynamic characteristics between Regenerative diode and MPS rectifier takes place at two different cases. In one case, the load current is 15 A/cm$^2$ and the other case it is 100 A/cm$^2$. In both the cases, an ideal switch (S) is used in the simulations and the values of the supply voltage ($V_{DC}$) and parasitic inductance are 50 V and 5 nH respectively.

When the switch is in off-state (open position), the device under test (DUT) is in forward bias and carries the load current. In the first case (i.e., the load current is 15 A/cm$^2$), the device under test (either Regenerative diode or MPS rectifier) carries 15 A/cm$^2$ and in this case both devices (show in Fig. 3.25) are in unipolar state (no minority carrier injection and hence no plasma in the device). Fig. 3.27 illustrates the comparison of the current waveforms between Regenerative diode and MPS rectifier for the first case. In the first case, until 10 µs, the device under test is in forward bias and carries the load current which is 15 A/cm$^2$. At 10 µs, the switch is turned-on (changed its state from OFF to ON) and therefore the current through the switch increases with the di/dt (it is determined by the supply voltage source and parasitic inductance in the circuit) of 10 kA/cm$^2$µs. As a result, the current through the device (device under test) decreases with the same di/dt to maintain the constant load current which is 15 A/cm$^2$. However, it can be observed from Fig. 3.27 that the peak reverse recovery current

is nearly the same in both the devices and here the reverse recovery current is only due to parasitic capacitance of the devices since there is no plasma in both the devices for this case. The above simulation results (Fig. 3.27) show that the reverse peak current of the Regenerative diode during static characteristics (Fig. 3.21) is not a problem when it comes to the dynamic applications.

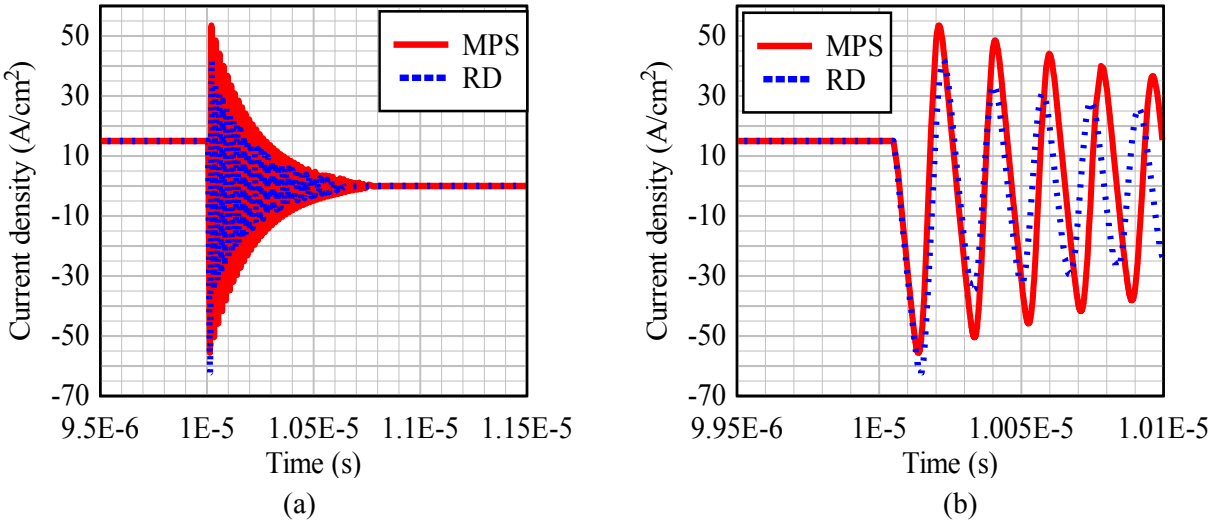



**Fig. 3.27 (a)** Comparison of the current waveforms between Regenerative diode and MPS rectifier for the first case (15 A/cm$^2$) **(b)** Zoomed version of the left side figure. The reason for the oscillations is that the simulations have been performed with the ideal conditions i.e. without any additional resistances in the circuit

In the second case (i.e., the load current is 100 A/cm$^2$) when the switch is in off-state, the device under test (either Regenerative diode or MPS rectifier) carries 100 A/cm$^2$. As shown in Fig. 3.25, the Regenerative diode is still in unipolar state at this current density (100 A/cm$^2$) but the MPS rectifier has already become bipolar(drift region is in high injection and filled with plasma). Fig. 3.28 illustrates the comparison of the current waveforms between Regenerative diode and MPS rectifier for the second case (100 A/cm$^2$).

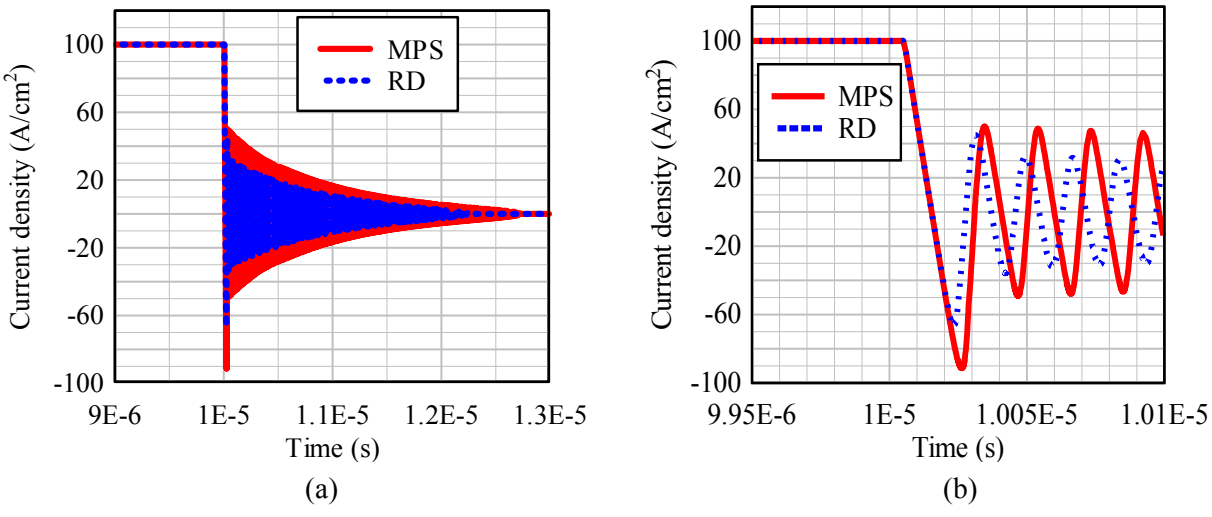



**Fig. 3.28 (a)** Comparison of the current waveforms between Regenerative diode and MPS rectifier for the second case (100 A/cm$^2$) **(b)** Zoomed version of the left side figure

In the second case, until 10 µs, the device under test is in forward direction and carries the load current which is 100 A/cm$^2$. At 10 µs, the switch is turned-on and therefore the current through the switch increases with the di/dt of 10 kA/cm$^2$µs. As a result, the current through the device (device under test) decreases with the same di/dt to maintain the constant load current which is 100 A/cm$^2$. However, it can be observed from Fig. 3.28 that the peak reverse recovery current is high in MPS rectifier when compared to that of the Regenerative diode. The reason being that the reverse current in the Regenerative diode is only due to its parasitic capacitance whereas in MPS rectifier it is due to the extraction of the plasma in the device. In fact, it can be observed from Fig. 3.27 and Fig. 3.28 that the peak reverse recovery current of the Regenerative diode is nearly the same in both load current cases (i.e., 15 A/cm$^2$ and 100 A/cm$^2$). Consequently, it can be concluded that the reverse current in the Regenerative diode is only due to the capacitive current and is not dependent on the load current as long as the device is in unipolar state.

The above simulation results show that, in case of dynamic applications, the reverse peak current of the Regenerative diode during static characteristics (Fig. 3.21) is not a problem in the Regenerative diode because the reverse recovery current dominates (reverse recovery current due to the parasitic capacitance as long as the device in unipolar state otherwise reverse recovery current is due to the charge extraction when the device is in bipolar state) and the reverse recovery current is present in all diodes and rectifiers during turn-off.

## 3.7 Regenerative Diode as a Protection Device

One more application of the Regenerative diode is that it can also be used as a protection device for the circuits/devices when they connect to wrong polarities. In this section, the simulation results show under which conditions it can fulfill this application and under which it cannot.

Fig. 3.29 illustrates the circuit which is used in the simulations. The Regenerative diode as shown in Fig. 3.20 is used as a device under test in the simulation. In the reverse direction, due to the on-state (normally-on) behavior of the device, a small reverse peak current is flowing in the device. It needs a small reverse voltage across the device to enter into the full blocking condition (very small reverse saturation current). When the reverse voltage across the device is not sufficient, this device can not enter into the full blocking condition and carries a small reverse peak current through it.

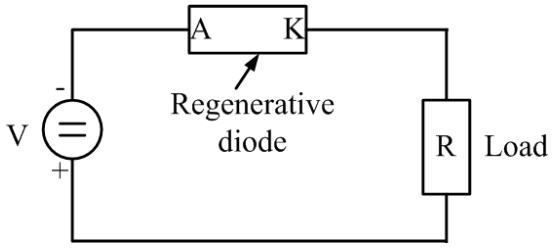
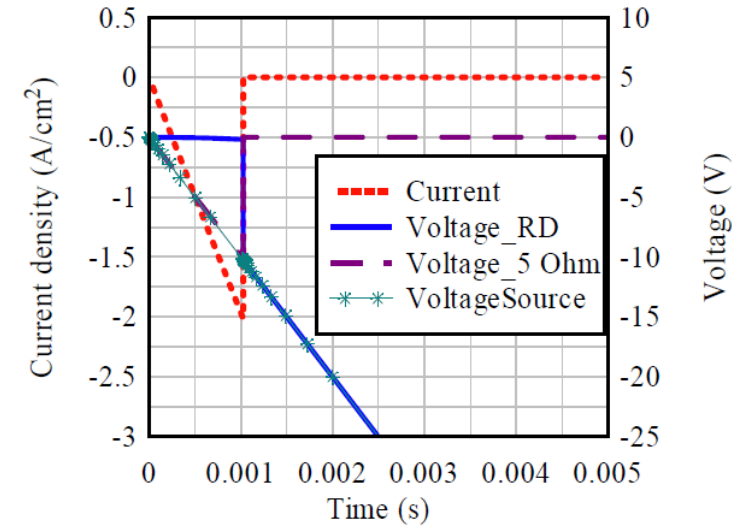


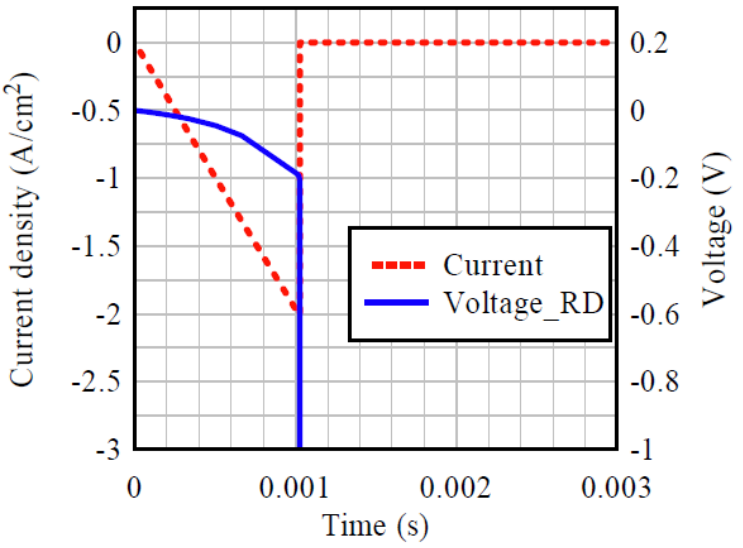

**Fig. 3.29** The circuit which is used in the simulation to test the device application as a protection device

The device as shown in Fig. 3.23 needs a minimum reverse voltage of 0.22 V across the device to enter into the blocking condition. The minimum voltage which is required for the device to enter into the blocking condition can be changed depending on the application by changing the channels width and doping of the device.

Two simulations have been performed at room temperature to test the device application as a protection device. In both the simulations, the voltage source and the Regenerative diode (device under test) are the same but the load resistance is different. In one simulation, the load resistance is 5 Ω and in the other simulation it is 50 Ω. In both the simulations, the voltage source is ramped from 0 to -50 V in 5 ms and is constant at -50 V from 5 ms to 10 ms. As shown in Fig. 3.29, the device is connected in the reverse direction (anode of the device is connected to the negative terminal of the voltage source).



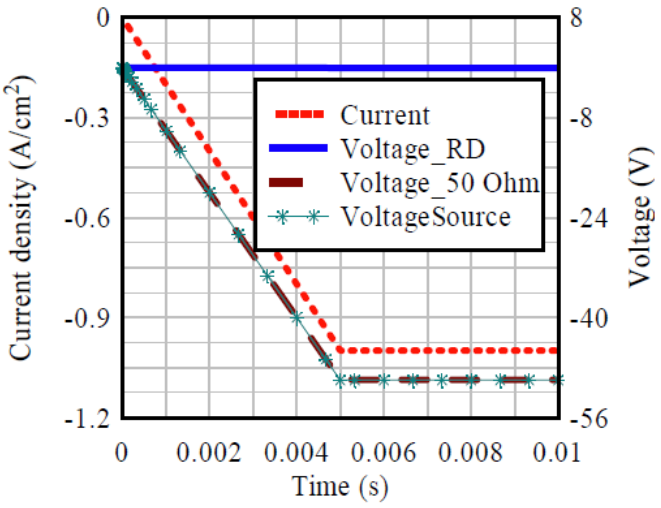

(a)



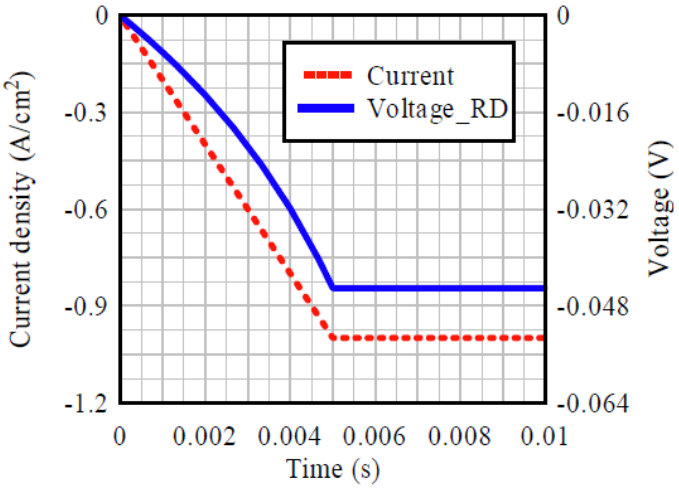

(b)

**Fig. 3.30 (a)** Simulation results of the circuit shown in Fig. 3.29, in which the load resistance is 5 Ω **(b)** Zoomed version of the above figure at very low voltages (only current and voltage of RD)

Fig. 3.30(a) illustrates the simulation results of the circuit (shown in Fig. 3.29) at room temperature and in this case the load resistance is 5 Ω. Fig. 3.30(b) is a zoomed version of Fig. 3.30(a) at very low voltages and illustrates only the current flowing in the circuit and the voltage across the Regenerative diode. As shown in Fig. 3.30, the reverse current that is flowing in the circuit increases as the source voltage ramps from 0 V to -10 V. This current builds up the voltage drop in the Regenerative diode and when the voltage across the device is sufficient which means when the voltage across the device reaches 0.22 V, the device enters into the blocking condition causing the current to go to zero. The reverse current increases until 0.001 s and most of the source voltage appears across the load resistor. As shown in Fig. 3.30(b), at 0.001 s, the voltage across the device is 0.22 V which is sufficient to block the device and therefore from this instant the current flowing in the circuit decreases to zero. Therefore, the voltage across the load goes to zero and now all the source voltage appears across the Regenerative diode. From this simulation result, it shows that the Regenerative diode can also be used as a protection device for the circuits/systems when they connect to wrong polarity.




(a)




(b)

**Fig. 3.31 (a)** Simulation results of the circuit shown in Fig. 3.29, in which the load resistance is 50 Ω **(b)** Zoomed version of the above figure at very low voltages (only current and voltage of RD)

Fig. 3.31(a) illustrates the simulation results of the circuit (shown in Fig. 3.29) at room temperature and in this case the load resistance is 50 Ω. Fig. 3.31(b) is a zoomed version of Fig. 3.31(a) at very low voltages and illustrates only the current flowing in the circuit and the voltage across the Regenerative diode. As shown in Fig. 3.31(a), the reverse current that is flowing in the circuit increases as the source voltage ramps from 0 V to -50 V. This current builds up the voltage drop in the Regenerative diode. The device to enter into the blocking condition, it needs a minimum voltage drop of 0.22 V (a minimum current density of ~ 2 A/cm$^2$ should flow in the device) across the device. However, this is not happened in this simulation. At 0.005 s, the source voltage reaches its maximum value of 50 V and the maximum current that can flow in the circuit is 1A (50 V/50 Ω). This current builds up the voltage drop of only ~ -0.048 V across the Regenerative diode as shown in Fig. 3.31(b). Therefore, the voltage across the device is not sufficient to enter into the blocking condition which could cause the current to flow through it and hence all the source voltage appears across the load resistor.

From the simulations results, it can be seen that it needs a sufficient amount of reverse voltage across the device or a minimum amount of reverse current that should flow through the device to act as a protection device otherwise it fails to act as a protection device for the circuits/systems when they connect to wrong polarities. The minimum voltage or current limit of the device can be changed according to the applications by changing the doping and width of the channels.

## 3.8 Regenerative Diode as a Current Limiter

Actually Regenerative diode can be used as a rectifier or as a protection device for the circuit/system when it is connected to wrong polarity. In addition, it can also be used as a perfect current limiter (very flat differential resistance and temperature independent) just by changing the doping and width of the channels. The Regenerative diode can be used as a current limiter in the reverse direction (i.e., anode is at negative potential). The current limit of the device can be changed according to the applications by changing the channel parameters.

Fig. 3.32 illustrates the characteristics of the Regenerative diode as a current limiter for 200 A/cm$^2$ current limiting applications. In fact, the current limiter or the current source should have infinite (very high) differential resistance. From the simulation (as shown in Fig. 3.32), the current flowing in the device is 2.951 μA and 2.973 μA at 18 V and 65 V respectively. From this, the differential resistance at 300 K is around 2 GOhm. Therefore, Regenerative diode acts as a perfect current limiter in the voltage range between 18 V and 65 V at 300 K because it has a high differential resistance in this voltage range. In addition one more simulation has been performed at higher temperature i.e., at 400 K to see the temperature dependence of the I-V characteristics of the device.

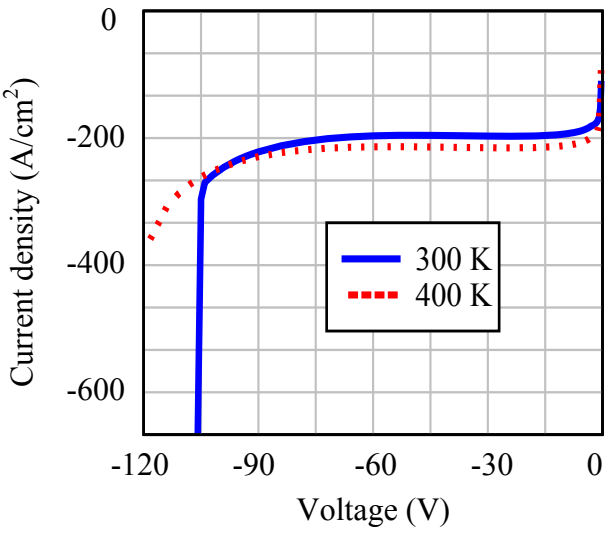



**Fig. 3.32** The I-V characteristics of the Regenerative diode which acts as a current limiter

It can be observed from Fig. 3.32 that the temperature dependence of the device is very less i.e., there is a small change in current when the operating temperature changes from 300 K to 400 K. The reason for the temperature independent characteristics of the device is compensation between the mobility of the carriers and the diffusion voltage of the channels. The mobility of the carriers reduces with the temperature therefore the current should decrease but this effect is compensated by the decrease of the diffusion voltage with the temperature. The reason being that the diffusion voltage decreases with the temperature causing channels to be more open and hence the conductivity of the channels increases.

## 3.9 Unipolar Regenerative Diode with Silicon-on-Insulator Technology

The Regenerative diode structures as shown previously in this chapter become bipolar at a certain forward voltage across the device (for example, the structure shown in Fig. 3.20 becomes bipolar when the voltage across the device reaches about 0.85 V or 350 A/cm$^2$ at 300 K). The reason being that the junction between $p^+$-drain/$p^+$-gate and $n^-$-drift region becomes forward biased and injects minority carriers into the $n^-$-drift region causing the $n^-$-drift region to be filled with plasma. This device can act as a unipolar device when there is no minority carrier injection into $n^-$-drift region. This could be done by avoiding a junction between p-region and $n^-$-drift region.

Fig. 3.33 illustrates the Regenerative diode structure with the Silicon-on-Insulator (SOI) technology in which the p-region ($p^+$-drain/$p^+$-gate) is separated or isolated from the $n^-$-drift region by an insulator. Therefore, this device can act as a unipolar device even at higher current densities. Here the insulator (oxide) is only need to isolate the p-region ($p^+$-drain/$p^+$-gate) and $n^-$-drift region and not for blocking. As shown in Fig. 3.33, the unipolar Regenerative diode is a series combination of p-channel JFET and n-channel depletion type MOSFET. Therefore this device is also a normally-on device. It can be seen from Fig. 3.33 that, the $p^+$-source and $n^+$-source regions are shorted and the potential to the $n^+$-gate is

supplied from the $n^+$-source region, whereas the potential to the n-channel MOS-Gate is supplied from the anode (A) terminal.

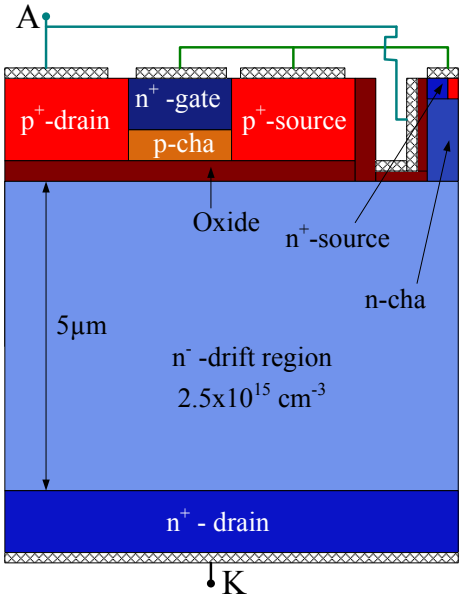



**Fig. 3.33** Unipolar Regenerative diode with SOI technology

In the forward direction, the holes flow from $p^+$-drain to the $p^+$-source through p-channel and electrons flow from $n^+$-drain to the $n^+$-source through an n-channel. The effective width of the p-channel increases with the anode potential because the junction between $n^+$-gate and p-channel is forward biased. In addition, the n-channel conductivity also increases with the positive anode potential because the n-channel MOS-Gate is at positive potential causing the accumulation of the electrons in the channel.

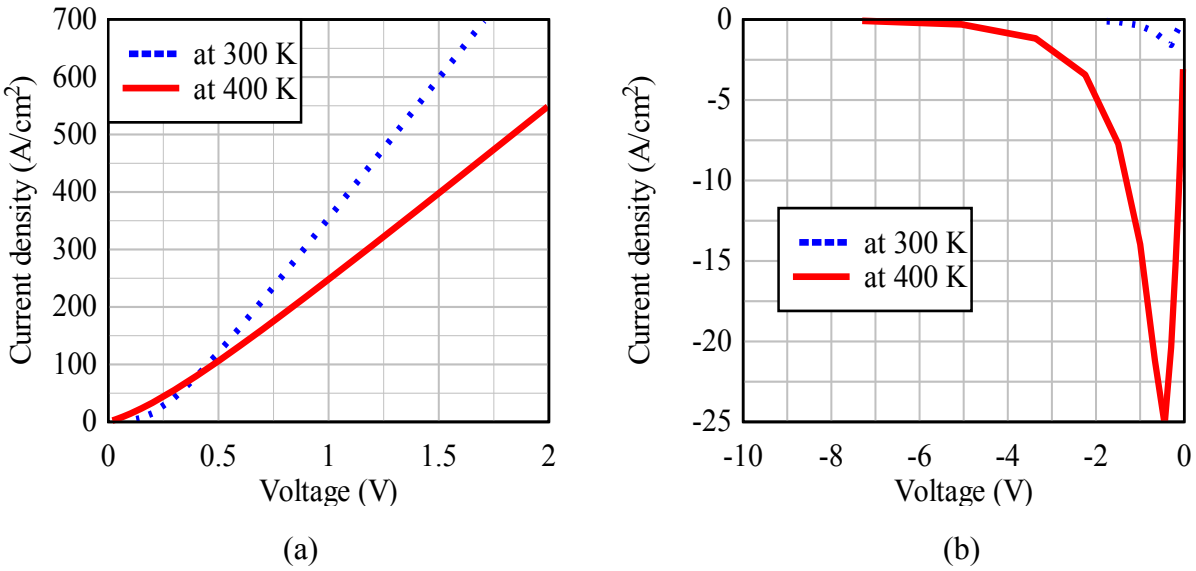



**Fig. 3.34** I-V characteristics of the unipolar Regenerative diode with SOI technology at different temperatures **(a)** Forward bias **(b)** Reverse bias

As shown in Fig. 3.33, the junction between p-region and n-drift region is avoided by placing an oxide (insulator) layer in between them. As a result there is no minority carrier injection

into the $n^-$-drift region. Fig. 3.34(a) illustrates the forward I-V characteristics of the unipolar Regenerative diode with SOI technology at 300 K and 400 K. It can be seen from Fig. 3.34(a) that, the Regenerative diode with SOI technology has a positive temperature coefficient of on-state characteristics even at higher current densities. This feature enables the reliable parallel operation of the devices.

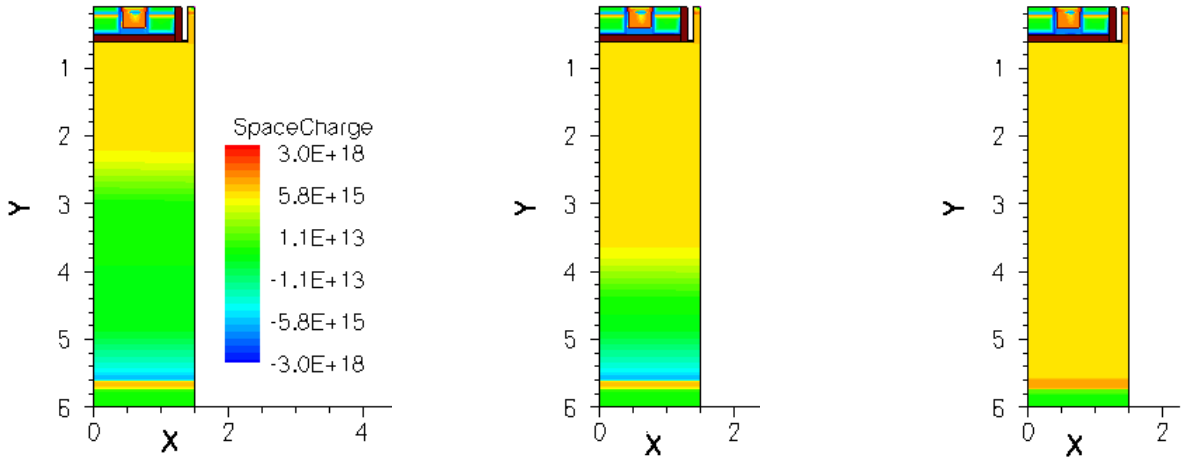



**Fig. 3.35** Distribution of the space charge layer at different anode voltages **(a)** -7 V **(b)** -25 V **(c)** -90 V

Fig. 3.34(b) illustrates the I-V characteristics of the unipolar Regenerative diode in the reverse direction. In the reverse direction, due to normally-on state behavior of the device, a small reverse peak current is flowing in the device and with the increase of the anode potential, the current flow reduces to a very small value as shown in Fig. 3.34(b). The reason being that the effective width of the channels decreases (in case of p-channel JFET, the junction between $n^+$-gate and p-channel is reverse biased which causes the depletion layer to penetrate into the p-channel reducing the effective width of the p-channel. In case of n-channel depletion MOSFET, the n-channel MOS-Gate depletes the n-channel since the n-channel MOS-Gate is at negative potential).

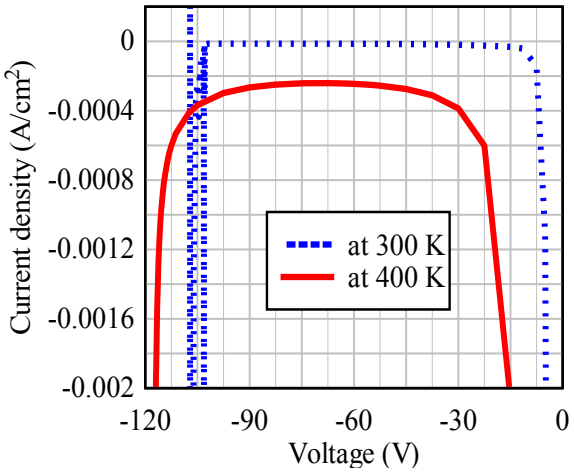



**Fig. 3.36** Reverse bias I-V characteristics of unipolar Regenerative diode with SOI technology at different temperatures

With the increase of the anode potential, the channels are completely closed by the depletion layers and thereby the current flow reduces to a very small value (reverse leakage current is flowing in the device due to the thermal generation of the carriers). With the further increase of the anode potential, the space charge (depletion) layer penetrates into the $n^-$-drift region and supports the voltage across the device. Fig. 3.35 illustrates the distribution of the space charge at different anode voltages. The reverse leakage current flowing in the device is small and is about 0.24 mA/cm$^2$ at 90 V, 400 K. The breakdown mechanism in the device is due to the avalanche generation at the bottom corner of the trench-gate. Therefore, this device also has a positive temperature coefficient of breakdown voltage as shown in Fig. 3.36 due to the decrease of avalanche generation with the temperature.

## 3.10 Experimental Results

Regenerative diode I-V characteristics have been realized experimentally with two normally-on discrete JFET devices. The schematic structure of the Regenerative diode which can be realized with two normally on JFETs is shown in Fig. 3.37

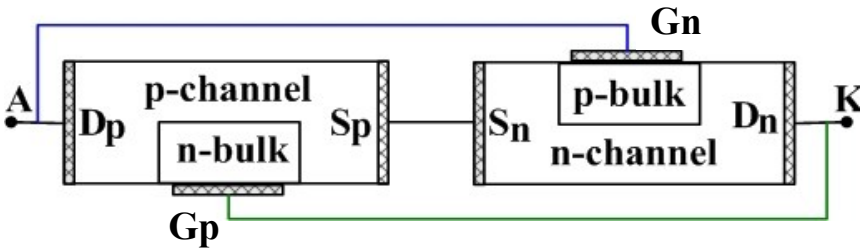



**Fig. 3.37** Schematic structure of the Regenerative diode

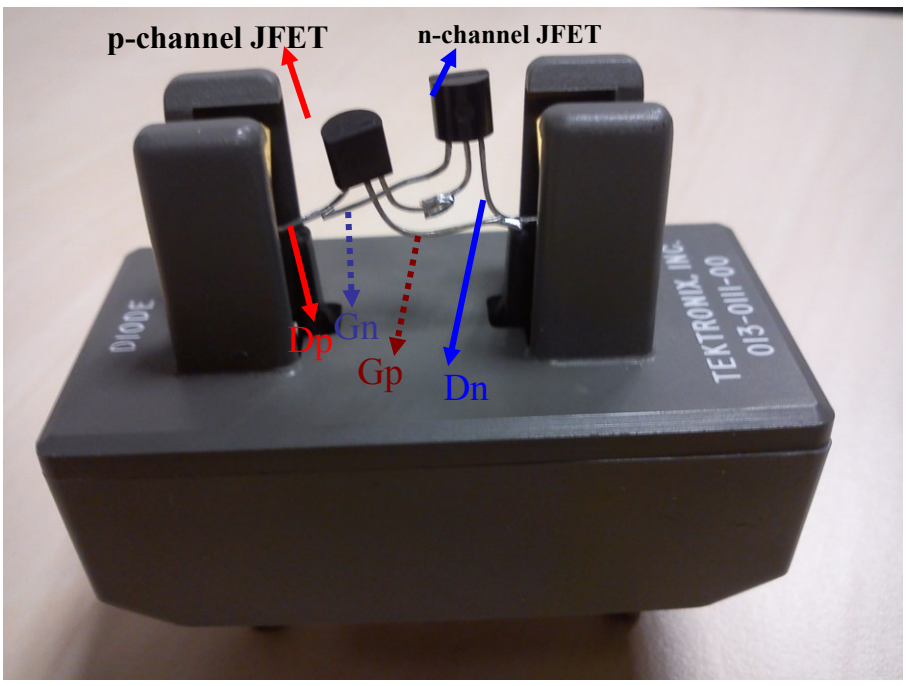



**Fig. 3.38** Experimental setup where the p-channel JFET and n-channel JFET (both are normally-on) are connected as shown in Fig. 3.37

Fig. 3.38 illustrates the experimental results of the Regenerative diode which is realized by the two normally-on discrete JFET devices p-channel (J270 from Fairchild) and n-channel (J201 from Fairchild). Fig. 3.39 illustrates the forward and reverse bias I-V characteristics of the Regenerative diode. As shown in Fig. 3.39, the current starts to increase from zero voltage (no threshold voltage) and acts like unipolar device until the forward voltage reaches 0.6 V (current reaches 750 μA). After 0.6 V, as shown in Fig. 3.39, the device becomes bipolar (the current slope changes at 0.6 V).

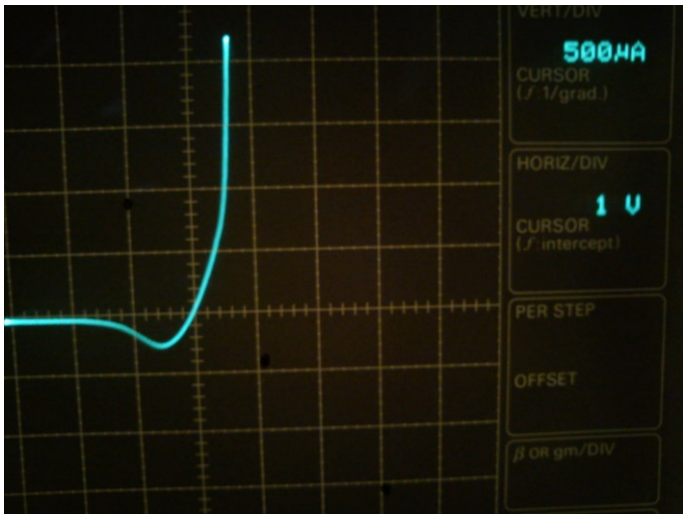



**Fig. 3.39** Experimental results – The I-V characteristics of the Regenerative diode at 300 K

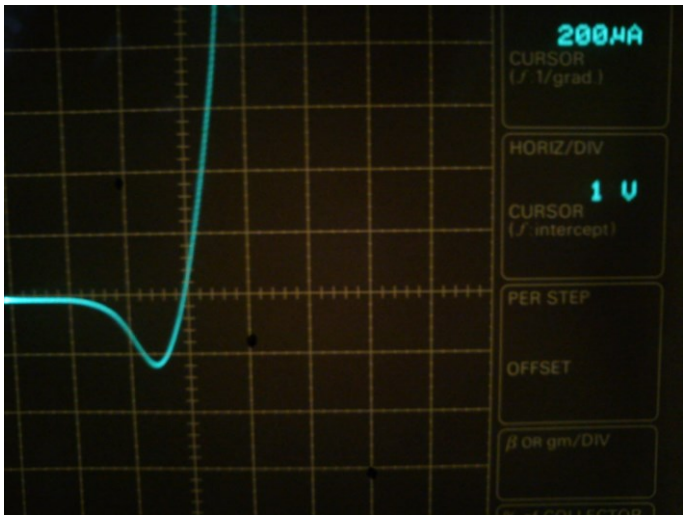



**Fig. 3.40** Experimental results – Zoomed version of the Fig. 3.39

In the reverse direction, there is some reverse peak current flowing in the device at very low voltages. After -0.5 V, the current starts to decrease and after -2 V, the current is nearly zero and the device is in blocking state.

# Chapter 4

# Si/6H-SiC Heterojunction Diode

This chapter presents a simulation study on a Si/6H-SiC heterojunction diode based on material and junction interface properties obtained in literature. In spite of the unavoidable uncertainties on the physical parameters of the heterostructure diode, the results may encourage further experimental work on such a Schottky – like heterostructure device. In this chapter, the influence of the p-Si doping on the interface traps as well as the electrical characteristics of the Si/6H-SiC heterojunction has been investigated. This chapter also presents the simulation results of the 6H-SiC Schottky Barrier Diode (SBD) and compares the electrical characteristics with that of the p-Si/N-6H-SiC heterojunction diode. The simulation results show that the p-Si/N-6H-SiC heterojunction diode offers low threshold voltage thereby better on-state characteristics than that of the 6H-SiC SBD. The influence of the electron affinity of the 6H-SiC on threshold voltage of the p-Si/N-6H-SiC heterojunction diode has also been investigated. Finally, it presents the simulation results of the novel merged p-i-n Si/6H-SiC heterojunction diode which acts as a unipolar diode at normal forward operating currents and changes its current conduction mechanism to bipolar at higher currents. This feature ensures the surge current capability of the device and there by reliable operation of the device in its applications.

## 4.1 Si/6H-SiC Heterojunction

This section provides the necessary insights to understand the electrical properties of the p-Si/N-6H-SiC heterojunction diode by analyzing the interface between p-Si/N-6H-SiC (the n-Si/N-6H-SiC heterojunction has also been investigated and the simulation results can be found in Appendix C). In this work small band gap material is represented with the small letter and wide band gap material is represented with the capital letter. Some of the important physical properties of the Si and 6H-SiC at room temperature are depicted in Table 4.1 according to the data provided in the device simulator DESSIS [Dess'03]. The other material properties of the Si and SiC can be found in Appendix B.

| Property | Si | 6H-SiC |
|---|---|---|
| Electron affinity (eV) | 4.07 | 4.09 |
| Band gap (eV) | 1.12 | 3.02 |
| Electron DOS ($cm^{-3}$) | $2.85e^{19}$ | $1.19e^{19}$ |
| Hole DOS ($cm^{-3}$) | $3.10e^{19}$ | $2.50e^{19}$ |

**Table 4.1** Physical properties of the Si and 6H-SiC at room temperature

Interface states or traps are expected at the heterojunction interface (the junction between Si and 6H-SiC) due to the mismatched lattice structure. In this work, it considers two types of interface traps which are donor and acceptor type traps. Donor traps possess positive charge [Dess'03] and they become neutral when they are below the Fermi level [McWh'88]. Acceptor traps possess negative charge [Dess'03] and become neutral when they are above the Fermi level [McWh'88]. In these simulations unless otherwise stated, it considers the traps are in the mid gap of the smaller band gap semiconductor (Si) and the concentration of the traps at the heterojunction interface is $5x10^{12}$ $cm^{-2}$ (assumed the largest value) with the capture cross section of about $1x10^{-15}$ $cm^2$. In this work, all simulations have been performed at 400 K unless otherwise stated. The authors L. Chen et al. [Chen'07] considered the concentration of the donor interface traps up to $1x10^{12}$ $cm^{-2}$ at Si/4H-SiC heterojunction interface.

### 4.1.1 p-Si/N-6H-SiC Heterojunction Diode

This section presents the simulation results of the electrical characteristics of p-Si/N-6H-SiC heterojunction diode. The I-V characteristics of heterojunction diode have been simulated for two different dopings of p-Si (low doped and high doped cases to investigate the influence of the p-Si doping on electrical characteristics of the heterojunction diode). For each doping case, it considers, without interface states (ideal) and with interface states (donor or acceptor type traps) at the heterojunction interface. In case one doping i.e., low doped p-Si, the doping of the p-type Si and N-type 6H-SiC are nearly the same and it is $2x10^{16}$ $cm^{-3}$. In case two doping i.e., high doped p-Si, the doping of the p-type Si and N-type 6H-SiC are $5x10^{19}$ $cm^{-3}$ and $2x10^{16}$ $cm^{-3}$ respectively. Table 4.2 depicts the type of the simulations that have been simulated in this section for the I-V characteristics of the heterojunction diode. Fig. 4.1 illustrates the schematic structure of p-Si/N-6H-SiC heterojunction diode. The Fig. 4.2 illustrates the energy band diagram of p-Si/N-6H-SiC heterojunction interface at thermal equilibrium.

| | | | |
|---|---|---|---|
| **Low doped p-Si (case one doping):**<br>p-Si doping: 2 to 3 $x10^{16}$ $cm^{-3}$<br>N-6H-SiC doping: $2x10^{16}$ $cm^{-3}$ | Without interface traps (assumed the interface is ideal) | With donor traps at the interface<br>Concentration: $5x10^{12}$ $cm^{-2}$ | With acceptor traps at the interface<br>Concentration: $5x10^{12}$ $cm^{-2}$ |
| **High doped p-Si (case two doping):**<br>p-Si doping: $5x10^{19}$ $cm^{-3}$<br>N-6H-SiC doping: $2x10^{16}$ $cm^{-3}$ | | | |

**Table 4.2** The type of the simulations that have been performed in this section for the I-V characteristics of the heterojunction diode

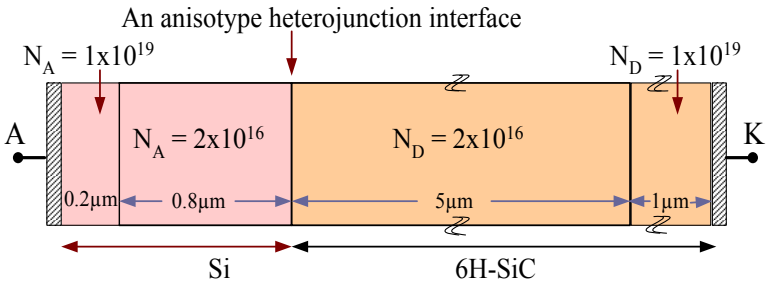



**Fig. 4.1** The schematic structure of p-Si/N-6H-SiC heterojunction diode

**Low doped p-Si:** The following I-V characteristics as shown in Fig. 4.3 are obtained when the diode is in forward bias (anode voltage is ramped to 2 V). The heterojunction diode starts conducting reasonable current after reaching the threshold voltage of about 0.4 V. The p-Si/N-6H-SiC heterojunction diode shows Schottky-like unipolar diode characteristics. The reason for the unipolar action is the difference in barrier heights for the electrons and holes as shown in Fig. 4.2. Here the electrons have much lower barrier height ($qV_n$) compared to that of the holes ($qV_p$).

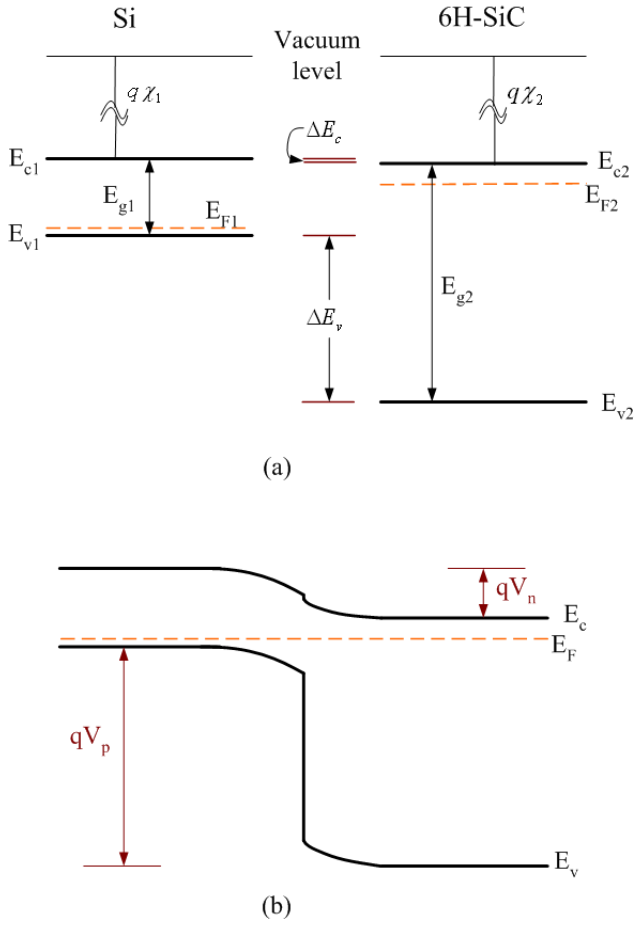



**Fig. 4.2** Energy band diagram of p-Si/N-6H-SiC heterojunction interface (a) Schematic energy band diagrams of the two semiconductors before in contact to each other **(b)** Energy band diagram of the heterojunction without traps at thermal equilibrium and looks similar even with the traps (whereas in n-Si/N-6H-SiC band diagram looks different in case of with and without traps; see Fig. C(2))

Therefore, only the electrons can easily flow from N-6H-SiC to p-Si but not the holes from p-Si to N-6H-SiC. Fig. 4.3(b) illustrates the carrier density across the heterojunction diode at anode voltage of 2 V. It can also be observed from Fig. 4.3(b) that the low doped p-Si is conductivity modulated due to the injection of the electrons from N-6H-SiC whereas the N-6H-SiC region is not modulated with the carriers since no holes are injected from p-Si to N-6H-SiC. The forward I-V characteristics as shown in Fig. 4.3(a) are nearly the same for with and without interface traps.

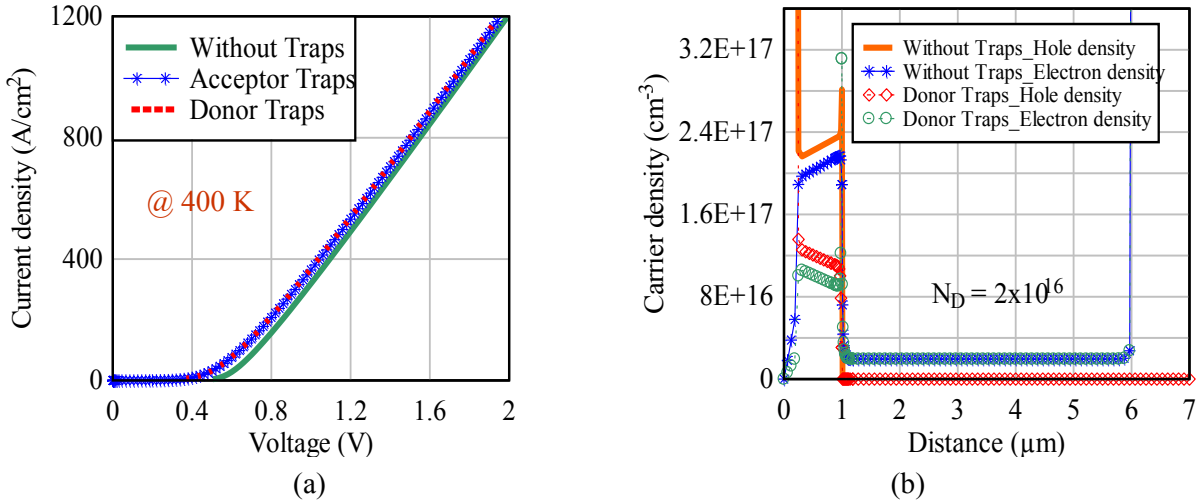



**Fig. 4.3** (a) Forward I-V characteristics of p-Si/N-6H-SiC heterojunction diode where the doping of the p-Si and N-6H-SiC are the same and doping concentration is $2x10^{16}$ $cm^{-3}$ (b) Carrier density across the heterojunction diode at anode voltage of 2 V

The following I-V characteristics as shown in Fig. 4.4 are obtained when the p-Si/N-6H-SiC heterojunction diode is in reverse bias (blocking state).

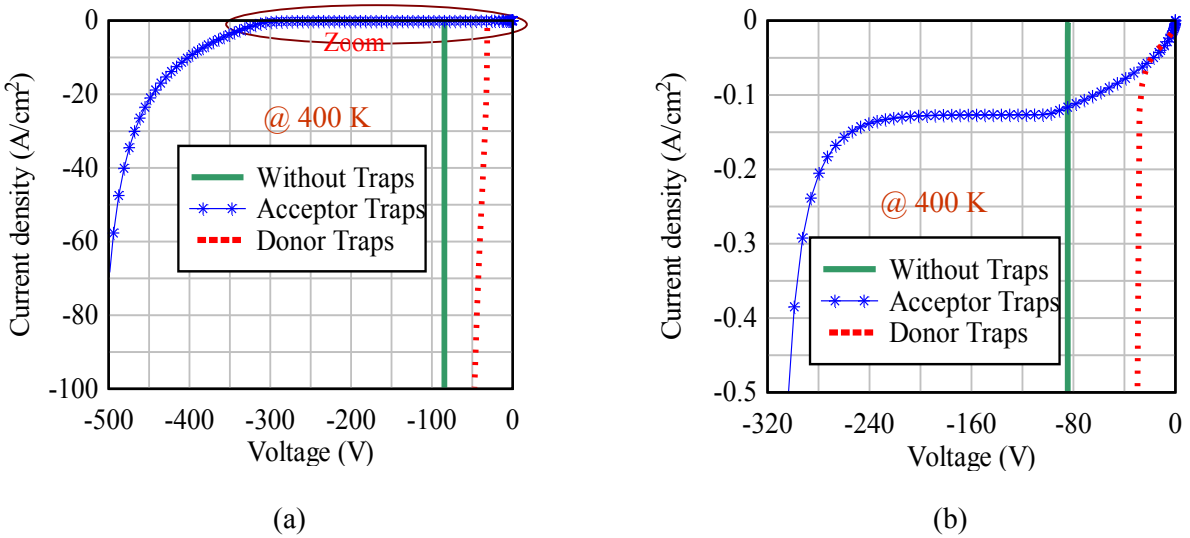



**Fig. 4.4** (a) Reverse bias I-V characteristics of p-Si/N-6H-SiC heterojunction diode where the doping of the p-Si and N-6H-SiC are the same and doping concentration is $2x10^{16}$ $cm^{-3}$ (b) Zoomed version of the left side figure at low current densities

The blocking characteristics of the heterojunction diode are quite different for with and without interface traps. The leakage current (blocking current) is higher in case of with traps and it is purely a generation current which is due to the interface traps. In case of without traps, the blocking current is very small and sustains voltages up-to 82 V. Afterwards, breakdown occurs due to the avalanche generation at the heterojunction interface. The reason for the lower breakdown voltage is that the depletion layer starts at the heterojunction interface and extends equally on both sides of the interface (i.e., into p-Si and N-6H-SiC due to the same doping concentration of both the layers) as shown in Fig. 4.5(a). The avalanche breakdown occurs inside the p-Si at the heterojunction interface when the electric field reaches a critical value in the Si. The Fig. 4.5(b) illustrates the electric field distribution at different anode voltages for the case of without interface traps.

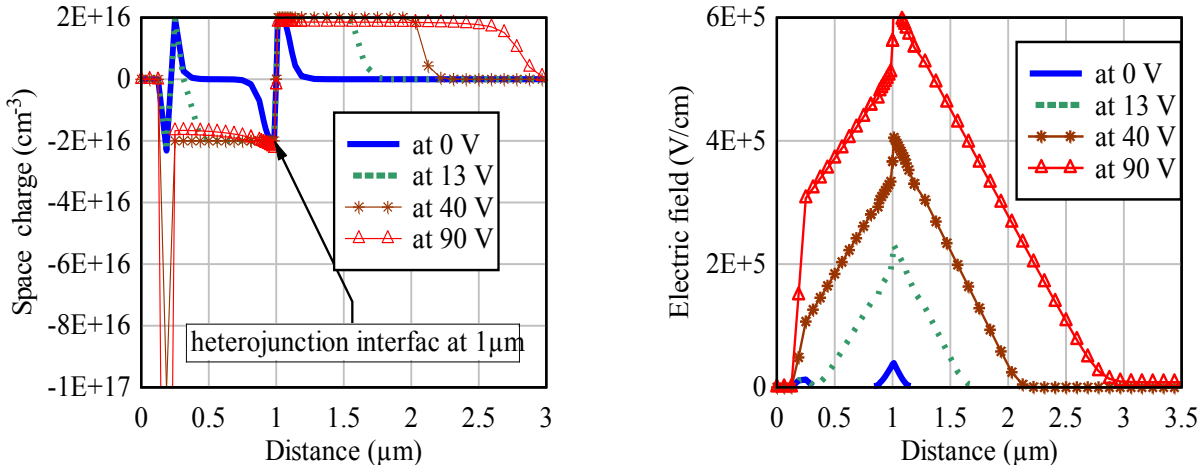
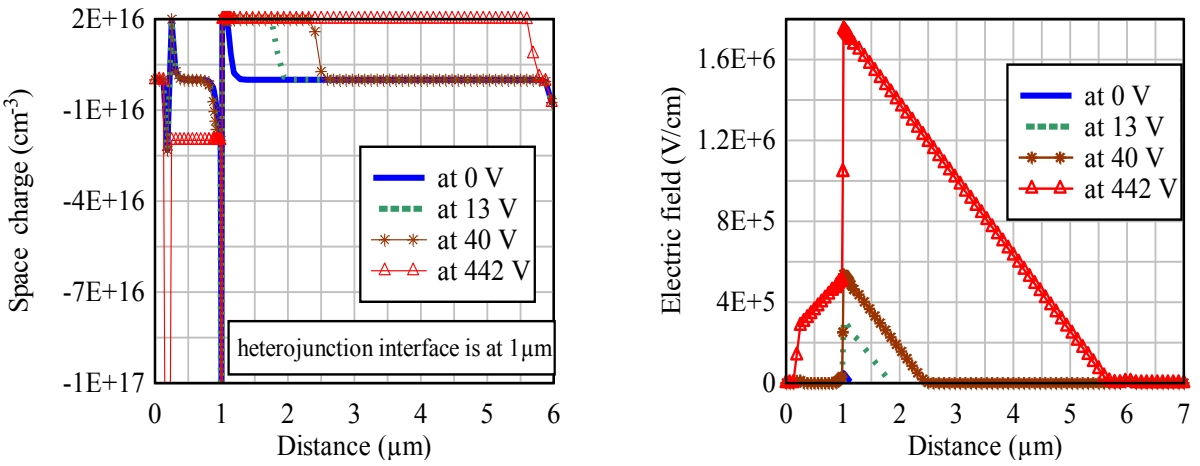



**Fig. 4.5** (a) Space charge distribution (b) Electric field distribution in p-Si/N-6H-SiC heterojunction diode for without interface traps. Here the doping of the p-Si and N-6H-SiC are the same and doping concentration is $2x10^{16}$ $cm^{-3}$.

In case of acceptor type traps, as shown in Fig. 4.6(a), unlike without traps case, the space charge layer mainly penetrates into N-6H-SiC at low voltages despite of having same doping concentration in p-Si and N-6H-SiC at the heterojunction interface. The reason is that there is a high magnitude of negative space charge layer at the heterojunction interface due to the acceptor type traps. However, at higher voltages, the space charge layer also penetrates into p-Si. Fig. 4.6(b) illustrates the electric field distribution at different anode voltages. In case of acceptor type traps, the device can block more voltage when compared to that of the without traps case but the leakage current is higher.

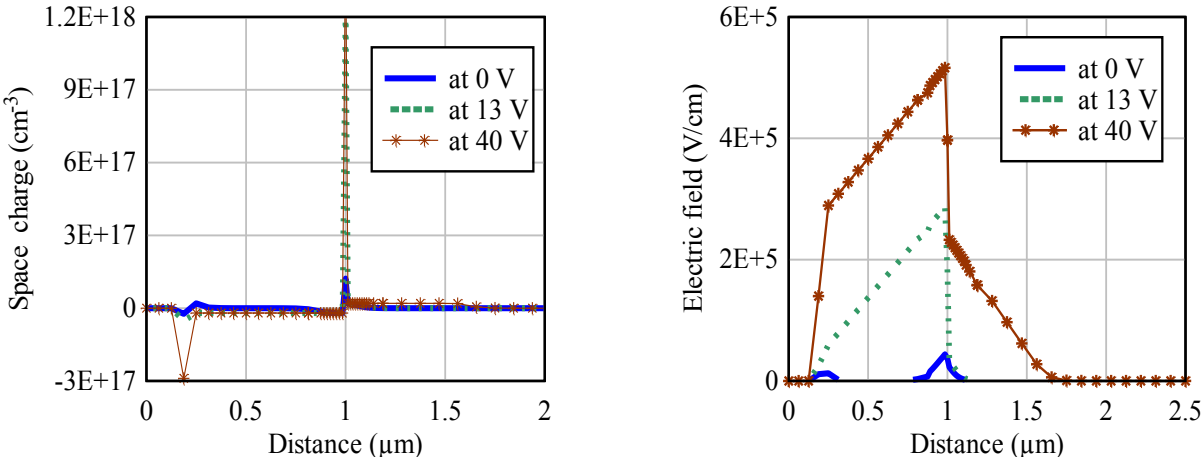
In case of donor type traps, as shown in Fig. 4.7(a), unlike without traps case, the space charge layer penetrates into p-Si at low voltages despite of having same doping concentration in p-Si and N-6H-SiC at the heterojunction interface. The reason is that there is a high magnitude of positive space charge layer at the heterojunction interface due to the donor type traps. However, at high voltages, the space charge layer also penetrates into N-6H-SiC but as shown in Fig. 4.7(b), the electric field is high in p-Si compared to that of the N-6H-SiC and

breakdown occurs at the heterojunction interface when the electric field reaches critical value in the p-Si. The blocking voltage of the device is less when compared to that of the without traps case where the depletion layer penetrates into both sides of the heterojunction interface equally.




(a) (b)

**Fig. 4.6** (a) Space charge distribution (b) Electric field distribution in p-Si/N-6H-SiC heterojunction diode for the case of acceptor interface traps. Here the doping of the p-Si and N-6H-SiC are the same and doping concentration is $2x10^{16}$ $cm^{-3}$.




(a) (b)

**Fig. 4.7** (a) Space charge distribution (b) Electric field distribution in p-Si/N-6H-SiC heterojunction diode for the case of donor interface traps. Here the doping of the p-Si and N-6H-SiC are the same and doping concentration is $2x10^{16}$ $cm^{-3}$.

**High doped p-Si:** In this case, the doping of the p-Si and N-6H-SiC are different. Here the p-Si is heavily doped and the doping concentration is about $5x10^{19}$ $cm^{-3}$ whereas the doping concentration of the N-6H-SiC is $2x10^{16}$ $cm^{-3}$. Fig. 4.8(a) illustrates the forward I-V characteristics of p-Si/N-6H-SiC heterojunction diode for the case of high doped p-Si. In this case, the heterojunction diode starts conducting reasonable current after reaching the threshold voltage of about 0.5 V. Fig. 4.8(b) illustrates the comparison of the forward I-V

characteristics between low and high doped p-Si for the case of acceptor traps. There is a slight increase of the threshold voltage as well as on-state voltage drop in high doped p-Si case compared to that of the low doped p-Si. This is because of the increase of the barrier height for the electrons to come from N-6H-SiC to p-Si with the increase of the p-Si doping. The influence of the p-Si doping on the forward bias characteristics of the p-Si/N-6H-SiC heterojunction diode is negligible but it is quite high on the reverse bias characteristics of the heterojunction diode.

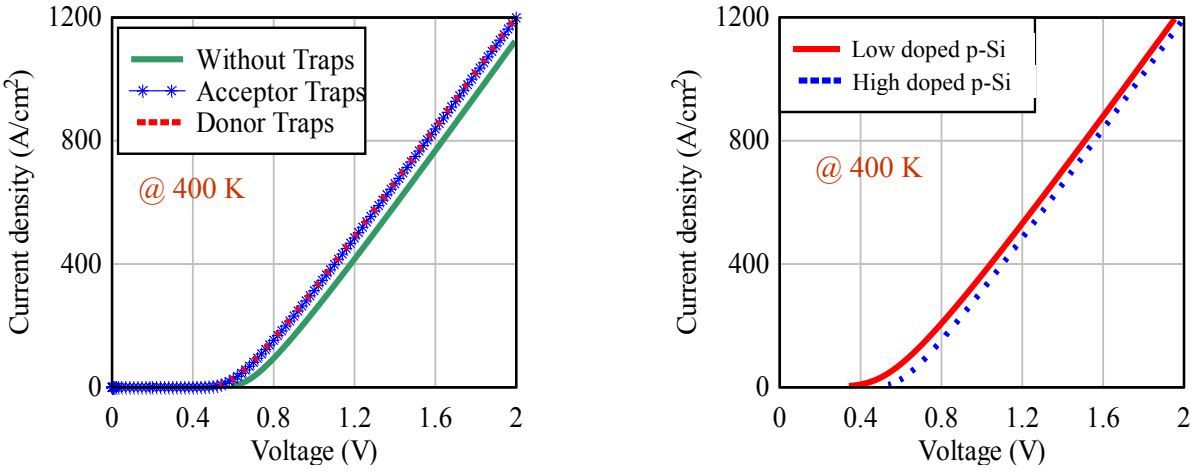



**Fig. 4.8** (a) Forward bias I-V characteristics of p-Si/N-6H-SiC heterojunction diode in case of high doped p-Si (b) Comparison of the forward bias characteristics between low doped p-Si and high doped p-Si for the case of acceptor traps.

The blocking or the reverse bias I-V characteristics of the p-Si/N-6H-SiC heterojunction diode in case of high doped p-Si are illustrated in Fig. 4.9. Unlike in low doped p-Si case, the blocking characteristics (breakdown occurs ~ 650 V) are similar for with and without interface traps. However, the leakage current is slightly higher in case of with interface traps.

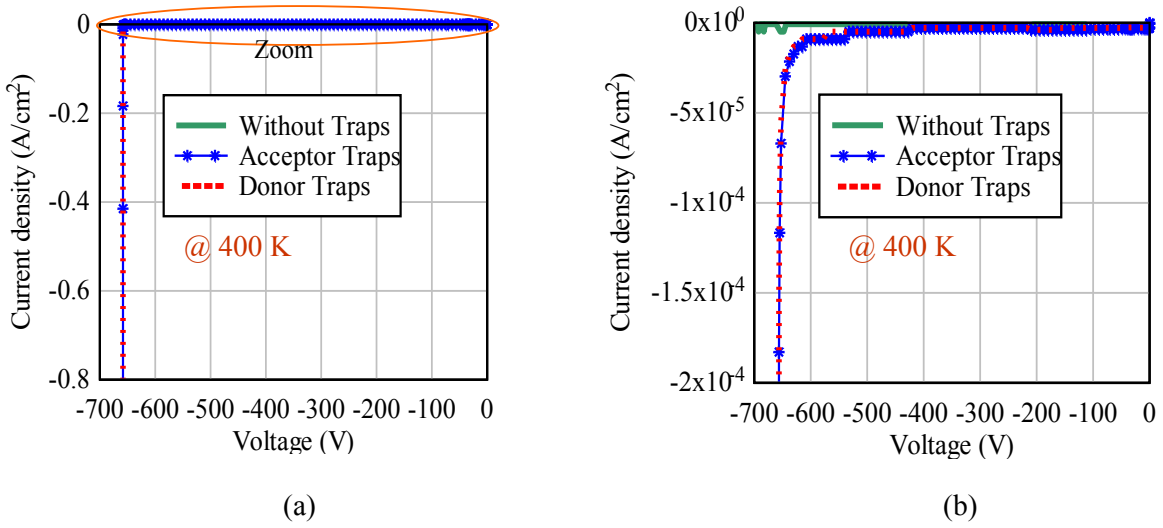



**Fig. 4.9** (a) Reverse bias I-V characteristics of p-Si/N-6H-SiC heterojunction diode in case of high doped p-Si (b) Zoomed version of the left side figure at low current densities

In case of high doped p-Si, the p-Si/N-6H-SiC heterojunction diode can block about 650 V after which avalanche breakdown occurs at the heterojunction interface when the electric filed reaches critical value in the 6H-SiC. This shows a nearly ideal breakdown voltage of the 6H-SiC. In case of high doped p-Si, for all three cases (without traps, donor type traps and acceptor type traps), the space charge (depletion) layer penetrates into N-6H-SiC since p-Si is heavily doped. Fig. 4.10(a) illustrates the space charge distribution in heterojunction diode in case of high doped p-Si at different anode voltages and is almost similar for with and without interface traps.

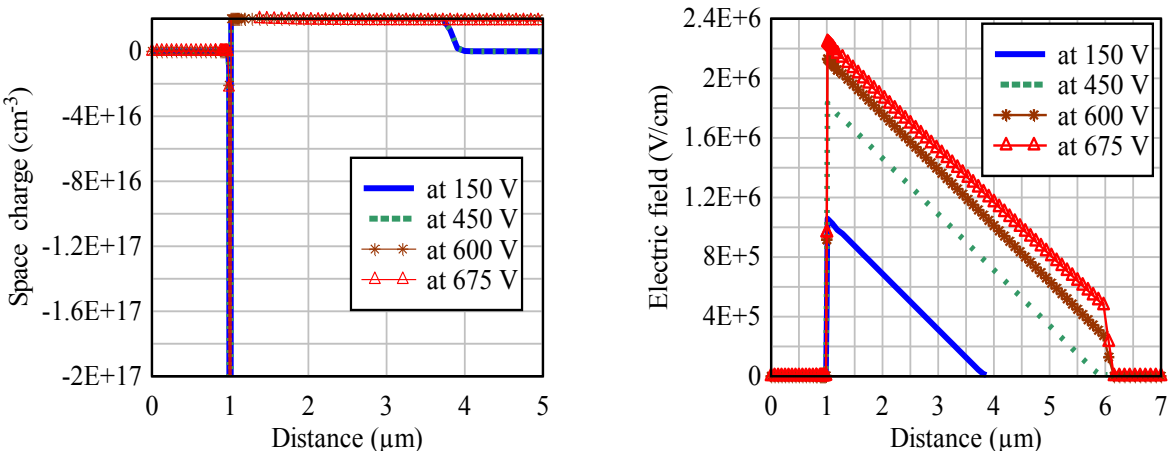
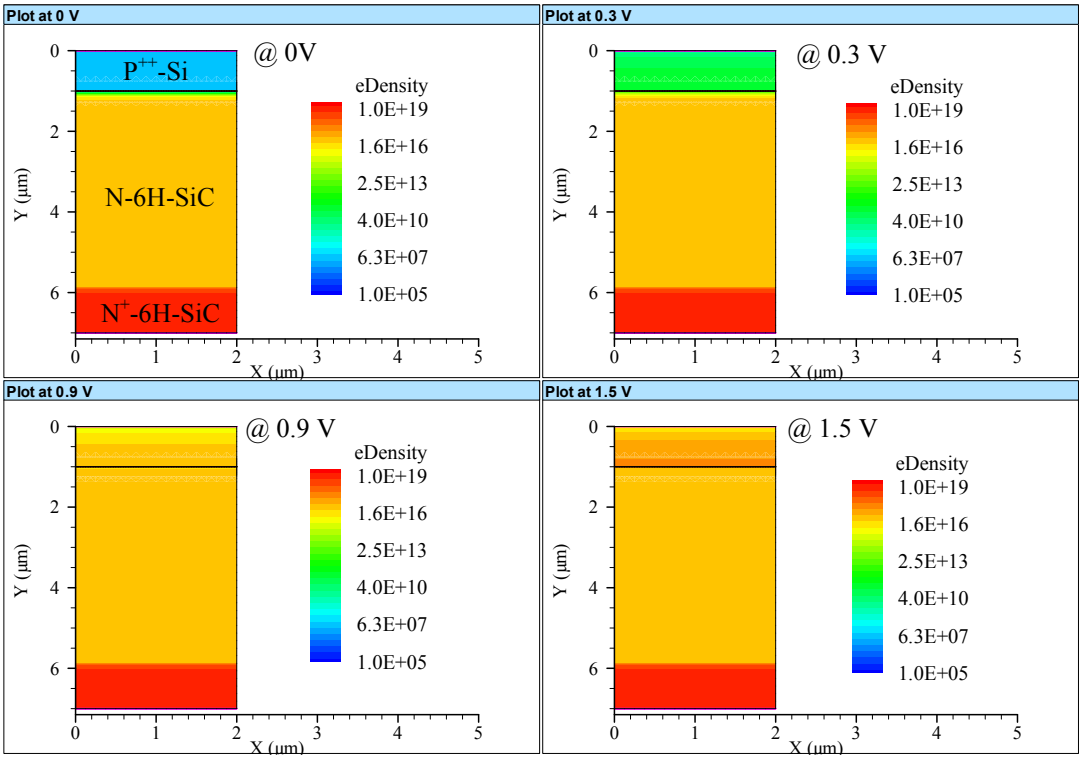



**Fig. 4.10** (a) Space charge distribution (b) Electric field distribution in p-Si/N-6H-SiC heterojunction diode in case of high doped p-Si.

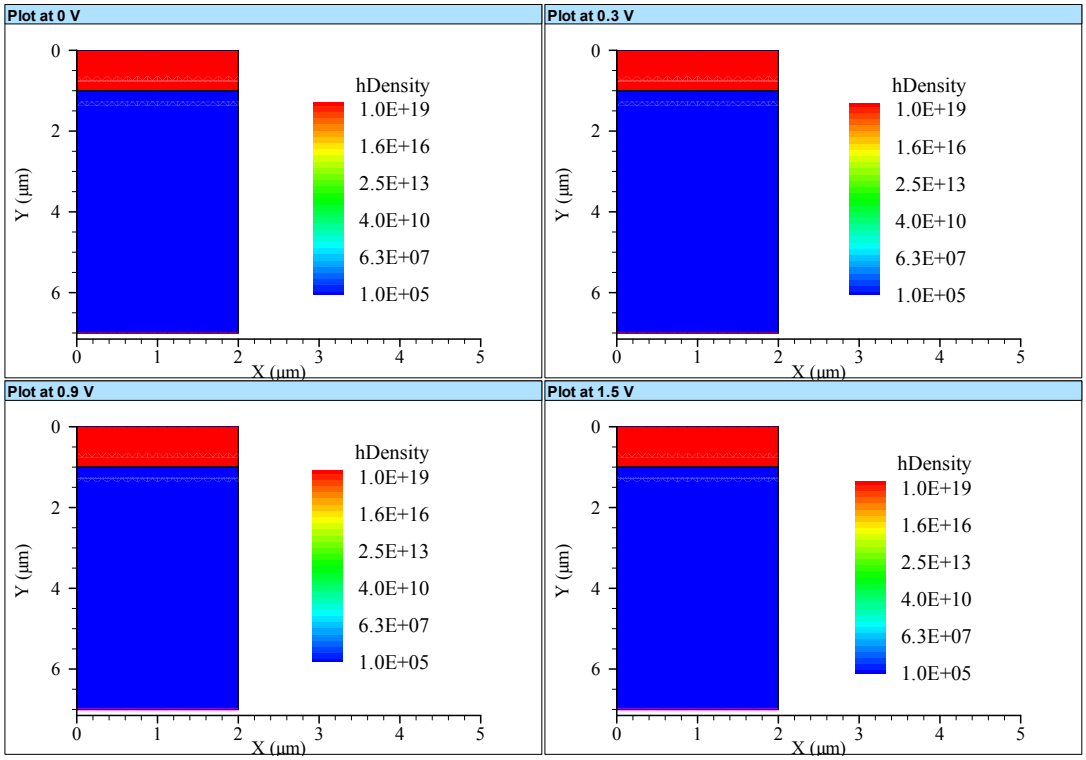
Fig. 4.10(b) illustrates the enhancement of the electric field with the increase of the anode voltage in case of high doped p-Si and is almost similar for both with and without interface traps. Unlike in low doped p-Si case, the blocking voltage of the heterojunction diode is not influenced by the interface traps because the doping of the p-Si is much higher than that of density of the interface traps. However, the leakage current is slightly higher with the interface traps compared to without interface traps.

As explained before, the p-Si/N-6H-SiC heterojunction diode behaves as a unipolar diode since the drift region (N-6H-SiC region) is not flooded with the plasma during conduction (forward biased) state. This can be observed from Fig. 4.11, which illustrates the electron and hole density distribution during conduction state at different anode voltages. As shown in Fig. 4.2, only the electrons can flow from N-6H-SiC to p-Si but not the holes from p-Si to N-6H-SiC since the barrier height is very high for holes compared to electrons.

This p-Si/N-6H-SiC heterojunction diode can block about 650 V and afterwards the diode enters into breakdown condition due to avalanche generation of carriers. Fig. 4.12 illustrates the impact ionization in p-Si/N-6H-SiC heterojunction diode during blocking before (at 567 V) and after (at 658 V) breakdown voltage.




(a)




(b)

**Fig. 4.11** (a) Electron density distribution (b) Hole density distribution of p-Si/N-6H-SiC heterojunction diode during conduction (forward bias) state at different anode voltages (0, 0.3, 0.9 and 1.5 V)

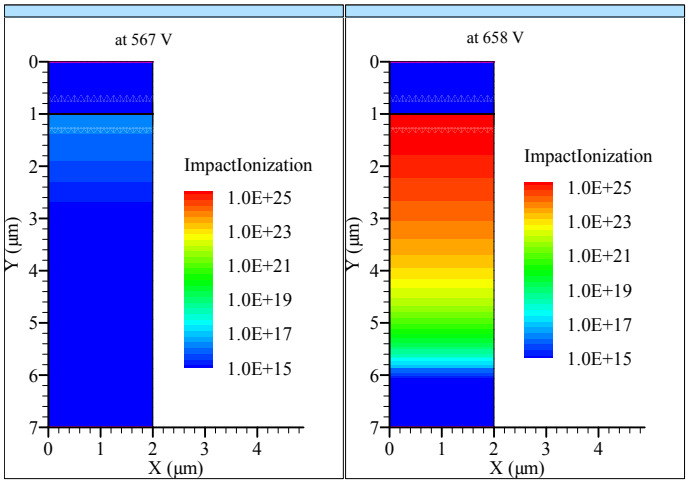



**Fig. 4.12** Impact Ionization in p-Si/N-6H-SiC heterojunction diode during blocking state at different anode voltages

### 4.1.2 Temperature Dependency of p-Si/N-6H-SiC Heterojunction Diode

To analyze the temperature dependence of electrical characteristics of heterojunction diode, isothermal simulations have been performed to the structure shown in Fig. 4.1 for the case two doping i.e., high doped p-Si, as the heterojunction diode has better blocking characteristics with the high doped p-Si. Fig. 4.13 illustrates the forward and blocking I-V characteristics of p-Si/N-6H-SiC heterojunction diode at different temperatures. In the forward biased state, at low current densities, the conduction loss (on-state loss) slightly reduces with the increasing temperature since the threshold voltage decreases (barrier height for the electrons to go from N-6H-SiC to p-Si decreases) with the increasing temperature. However, at higher current densities the conduction loss increases with the increasing temperature since the mobility of the carriers decreases with the increasing temperature (it shows a positive temperature coefficient of on-state resistance at higher current densities).

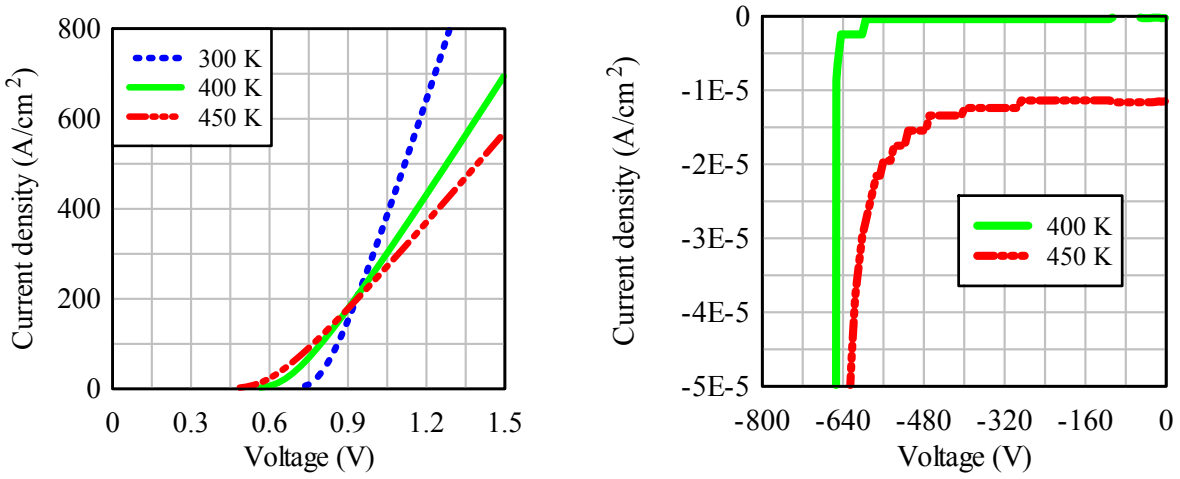



**Fig. 4.13** (a) Forward (b) Blocking characteristics of p-Si/N-6H-SiC heterojunction diode at different temperatures (isothermal simulations)

As shown in Fig. 4.13(b), the reverse leakage current increases with the increasing temperature since the space charge generation current increases with the increasing temperature. Fig. 4.14 illustrates the space charge generation current in p-Si/N-6H-SiC heterojunction diode at 400 K and 450 K.

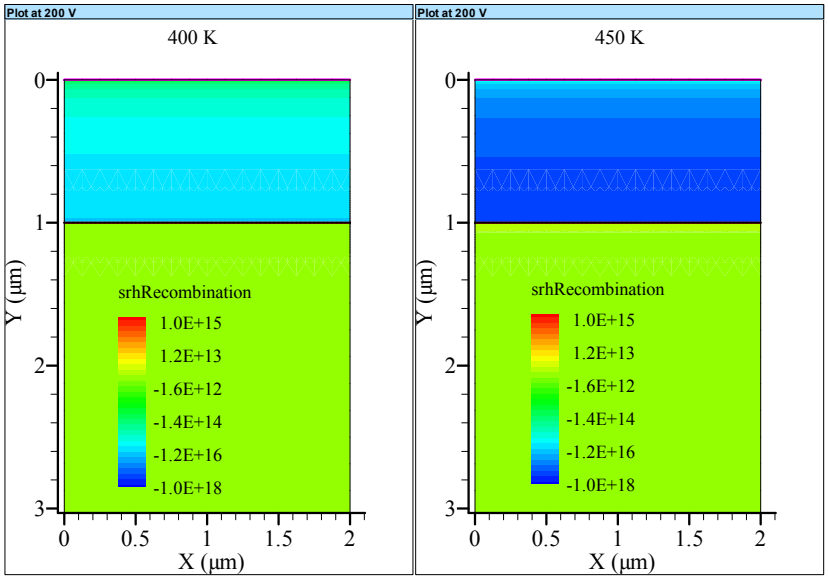



**Fig. 4.14** Space charge generation current at 200 V (the values with the negative sign represents the generation current and the positive values represents the recombination current) in p-Si/N-6H-SiC heterojunction diode during blocking at different temperatures

## 4.2 Comparison of p-Si/N-6H-SiC Heterojunction Diode and 6H-SiC Schottky Barrier Diode

In this section, a brief over view is given on 6H-SiC Schottky Barrier Diodes (SBDs) and after that the static and dynamic I-V characteristics of p-Si/N-6H-SiC heterojunction diode and 6H-SiC SBD are compared at isothermal conditions.

### 4.2.1 6H-SiC Schottky Barrier Diode

SBDs consist of metal-semiconductor junction and they are called majority carrier devices because no minority carrier injection is involved and current conduction is due to only one type of carriers. Therefore there is no reverse recovery current and hence fast switching frequency. Most important parameters that affect SiC SBDs characteristics are the metal work function, drift region doping and the width of the drift region. Fig. 4.15 illustrates the schematic structure of 6H-SiC SBD. For the simulations, the Schottky barrier height $\varphi_B$ (1.33 V), drift region doping ($2x10^{16}$ $cm^{-3}$) and the width of the drift region (5 µm) are taken from [Gheo'1]. Two dimensional simulations have been performed with DESSIS simulator at isothermal conditions and for the simulations the incomplete ionization, barrier tunneling and barrier lowering effects are taken into consideration.

In the simulations, dopants can be considered to be fully ionized at room temperature in Si because the impurities levels are sufficiently shallow, so the carrier concentration equals the dopant concentration. In SiC they are deeper compared to the thermal energy at room temperature, so only a fraction of the substitutional (active) dopant atoms are ionized at room temperature, giving a carrier concentration lower than the active dopant concentration. In the simulation, the ionization energies of the donor and acceptor dopants in SiC are considered to be 100 meV and 200 meV respectively. About the same values of ionization energies are considered in [Fröj'99, Calc'02].

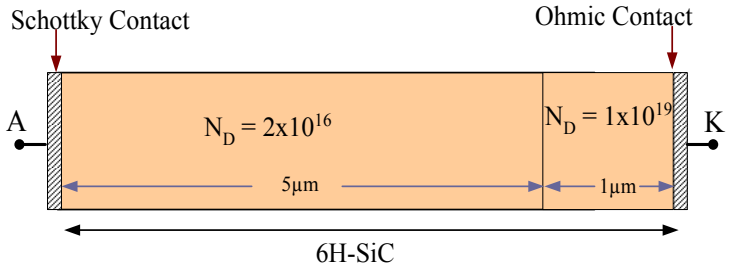



**Fig. 4.15** Schematic structure of 6H-SiC Schottky Barrier Diode

The concentration of electron or hole (ionized impurity atoms) is given in [Calc'02 & Dess] as:

$$n = \frac{N_D}{1 + g_D \frac{n}{N_C} \exp\left(\frac{\Delta E_D}{K_B T}\right)}, \text{ with } \Delta E_D = E_C - E_D \qquad (4.1)$$

$$p = \frac{N_A}{1 + g_A \frac{p}{N_V} \exp\left(\frac{\Delta E_A}{K_B T}\right)}, \text{ with } \Delta E_A = E_A - E_V \qquad (4.2)$$

where $N_{D/A}$ is the active donor/acceptor dopant concentration, $g_{D/A}$ is the degeneracy factor for the impurity level, $N_{C/V}$ is the effective density of states in the conduction/valance band, $E_{D/A}$ is the donor/acceptor dopant ionization energy, $E_{C/V}$ is the conduction/valance band edges, $K_B$ is the Boltzmann constant and T is the temperature.

In this work, the incomplete ionization for Si/6H-SiC heterojunction diode is also considered and for the doping concentration of $1x10^{19}$ $cm^{-3}$, the fraction of the ionized donor and acceptor dopants are 50% and 13% respectively at 400K. At the same temperature, dopants

ionization rate increases when it is low doped and donor dopants ionization rate is 99% for the doping concentration of $2x10^{16}$ $cm^{-3}$.

Forward characteristics of the SiC SBD can be explained by thermionic emission theory and the forward voltage drop of the SBD depends on the barrier height and series resistance (drift region resistance). The forward voltage drop $V_F$ is [Kipp'98]

$$V_F = \frac{nK_BT}{q}\ln\left(\frac{J_F}{A^*T^2}\right) + n\Phi_B + R_sJ_F \tag{4.3}$$

or

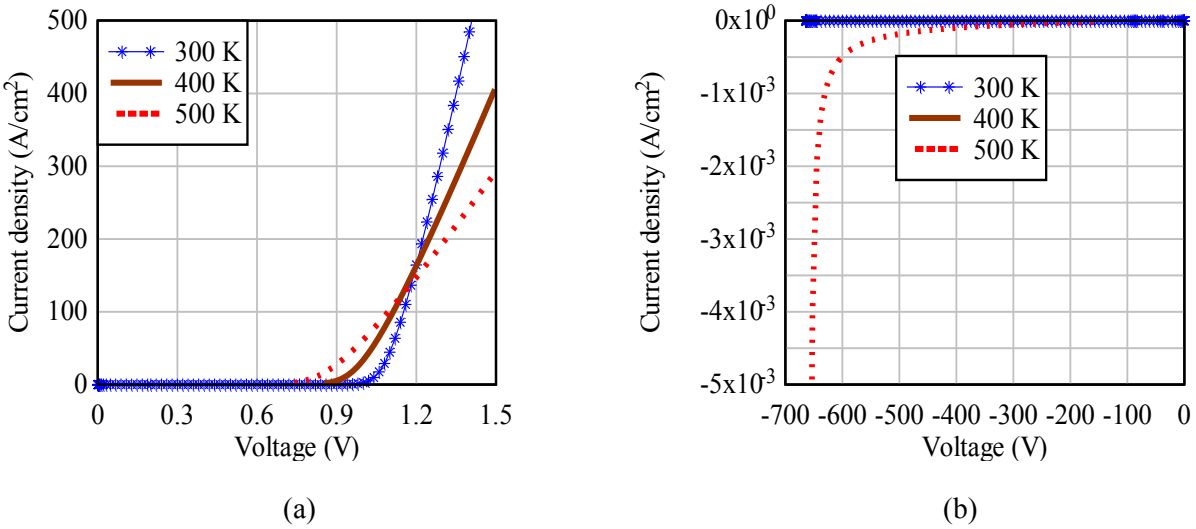
$$J_F = A^*T^2\exp\left(\frac{-q\Phi_B}{K_BT}\right).\exp\left(\frac{q\left(V_F - R_sJ_F\right)}{nK_BT}\right) \tag{4.4}$$

where $J_F$ is the forward current density, $A^*$ is the Richardson constant, n is the ideality factor, $\varphi_B$ is the Schottky barrier height and $R_s$ is the series resistance. The breakdown voltage of SBD depends on the doping and width of the drift region. The reverse leakage current of the SBD depends mainly on barrier height, electric field at the Schottky contact and the temperature. The reverse leakage current in Si SBDs is mainly due to the thermionic emission and generation current in the space charge region but in SiC SBDs, because of the high electric field, it is also due to the thermionic field emission and field emission in addition to the thermionic emission and generation current in the space charge region [Kipp'98]. Reverse leakage current due to the thermionic emission depends on the barrier height and the temperature. In addition, the leakage current increases by the image force barrier height lowering $\Delta\varphi_B$. Barrier height lowering decreases the effective Schottky barrier height by an amount that depends on the electric field at the Schottky contact. Reverse leakage current density $J_L$ due to the thermionic emission with the consideration of barrier height lowering is [Kipp'98]

$$J_L \approx -A^*T^2.\exp\left(\frac{-q\left(\Phi_B - \Delta\Phi_B\right)}{K_BT}\right) \tag{4.5}$$

Reverse leakage current in SiC SBD due to the thermionic field emission and field emission depends on the barrier height, barrier width and electric field at the Schottky contact. Barrier tunneling mechanism is the main mechanism in these two processes. In thermionic field emission, excited electrons above the Fermi level of the metal tunnel through the barrier whereas in field emission, electrons tunnel through the barrier at the Fermi level of the metal. Therefore, thermionic field emission is dependent on temperature whereas field emission is independent of the temperature.

Two dimensional isothermal simulations have been performed to the structure shown in Fig. 4.15 at different temperatures. Fig. 4.16 illustrates the simulated I-V characteristics of the 6H-SiC SBD in the forward and reverse directions.

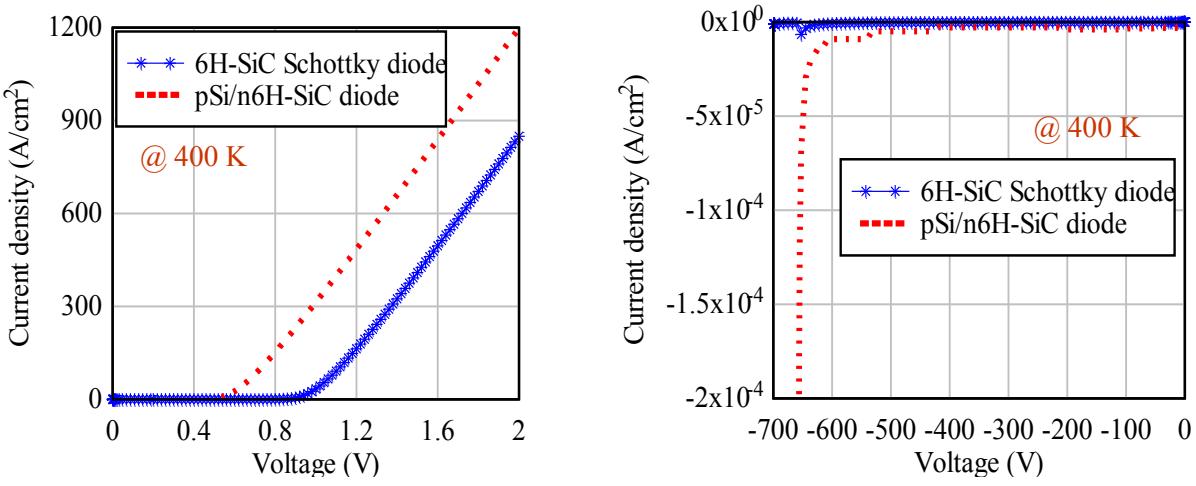



(a) (b)

**Fig. 4.16** I-V characteristics of 6H-SiC Schottky Barrier Diode at different temperatures (a) forward bias (b) reverse bias

### 4.2.2 Comparison of Static Characteristics

This section presents the comparison of the simulated static I-V characteristics between p-Si/N-6H-SiC heterojunction diode and 6H-SiC SBD. In the simulations it is considered that the doping and width of the drift region (N-6H-SiC) are the same for both the devices. Here p-Si/N-6H-SiC heterojunction diode is considered with the interface traps and the density of the traps at the Si/6H-SiC interface is $5x10^{12}$ $cm^{-2}$ (as explained in section 4.1). Fig. 4.17 illustrates comparison of the simulated static I-V characteristics between p-Si/N-6H-SiC heterojunction diode and 6H-SiC SBD at 400 K.




(a) (b)

**Fig. 4.17** Comparison of static I-V characteristics between p-Si/N-6H-SiC heterojunction diode and 6H-SiC SBD at 400 K (a) in On-State (b) in Blocking state (breakdown voltage is ~ 650 V for both the devices)

As shown in Fig. 4.17(a), the 6H-SiC SBD starts conducting reasonable current only after 0.9 V whereas p-Si/N-6H-SiC heterojunction diode starts conducting reasonable current after

0.5 V. Therefore, the on-state voltage drop is lower by ~ 0.4 V in p-Si/N-6H-SiC compared to that of the 6H-SiC SBD for the same current density. This 0.4 V difference is only coming from the differences in threshold voltages of the devices. It can be observed from Fig. 4.17(a) that the differential resistance (dV/dJ) is the same for both the devices as the doping and width of the drift region are the same for both the devices. The blocking capability (breakdown voltage is about 650 V for both the devices) and the reverse leakage current of the p-Si/N-6H-SiC heterojunction diode are nearly the same as 6H-SiC SBD.

Therefore, it can be concluded from the simulation results that the p-Si/N-6H-SiC heterojunction diode could be an alternative to conventional SiC SBD in low to medium voltage and high frequency applications since heterojunction diode has better on-state characteristics than that of the 6H-SiC SBD.

### 4.2.3 Comparison of Dynamic Characteristics

This section presents the comparison of the simulated dynamic (switching) characteristics between p-Si/N-6H-SiC heterojunction diode and 6H-SiC SBD at 400 K. As shown in Fig. 4.18, both the devices are in conduction state and carrying current of 360 A/cm$^2$ and at around 1µs, a negative voltage of 250 V is applied with the dv/dt of 250/µs to examine the reverse recovery behavior of these devices. It can be observed from Fig. 4.18 that the switching characteristics of p-Si/N-6H-SiC heterojunction diode are nearly the same as the switching characteristics of the 6H-SiC SBD. As shown in Fig. 4.18, both devices have fast switching speed with negligible reverse recovery current since both devices have unipolar nature (majority carrier devices therefore no stored charge or plasma). The authors [Tana'05] also claim that the heterojunction diode based on p-type polycrystalline silicon and n-type 4H-SiC exhibits almost zero reverse recovery similar to that of the SBD.

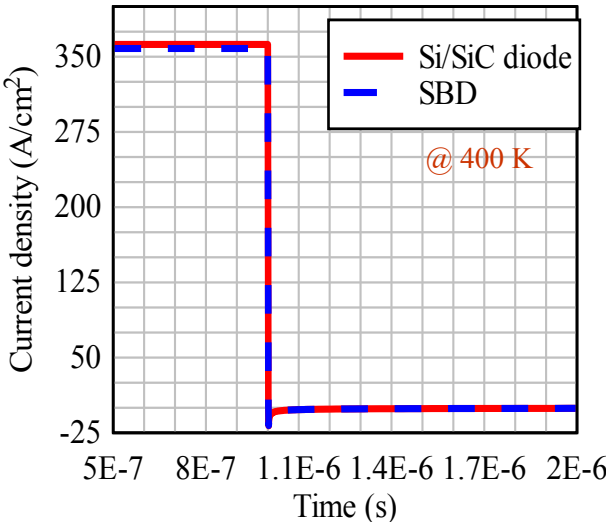



**Fig. 4.18** Comparison of dynamic characteristics between p-Si/N-6H-SiC heterojunction diode and 6H-SiC SBD at 400 K

## 4.3 Effect of Electron Affinity on I-V Characteristics of p-Si/N-6H-SiC Heterojunction Diode

In this section, it describes the influence of the electron affinity of the 6H-SiC on the I-V characteristics of the p-Si/N-6H-SiC heterojunction diode. The simulated I-V characteristics of the p-Si/N-6H-SiC heterojunction diode at 400 K are shown in Fig. 4.19 for different electron affinities of the 6H-SiC while the electron affinity of the Si is same for all the cases and is 4.08 eV at 400 K.

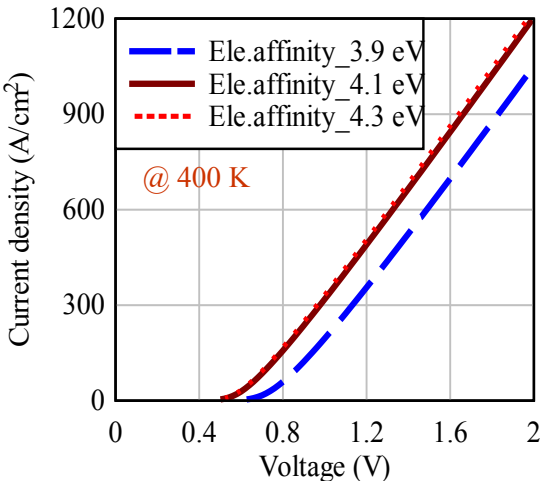



**Fig. 4.19** Forward I-V characteristics of p-Si/N-6H-SiC heterojunction diode for different electron affinities of the 6H-SiC

The default electron affinity of the 6H-SiC in DESSIS simulator is 4.1 eV at 400 K and also found in the literature [Batt'06] [Ward'99] that the electron affinity of the 6H-SiC is about 4 eV. So far the simulations have been performed with electron affinity of 4.1 eV for 6H-SiC. The difference between the I-V characteristics of p-Si/N-6H-SiC heterojunction diode is very small, if the electron affinity of the 6H-SiC is higher than the default value of the 6H-SiC (>4.1 eV). In other case, where the electron affinity of the 6H-SiC is smaller than the default value of the 6H-SiC (<4.1 eV), the I-V characteristics deviate from the default characteristics and are shown in Fig. 4.19. This is due to the shape of the energy band diagram of the heterojunction interface. If the electron affinity is higher than the default value (>4.1 eV), the energy band diagram of the heterojunction interface looks quite similar to the band diagram of the heterojunction interface in default case which is shown in Fig. 4.2, whereas it differs from that of Fig. 4.2, if the electron affinity is smaller than that of the default value (<4.1 eV). Fig. 4.20 illustrates the band diagram of the heterojunction interface when the electron affinity of the 6H-SiC is smaller than the default value of the 6H-SiC (<4.1eV). In other words, the energy band diagram of the heterojunction (p-Si/N-6H-SiC) interface looks similar to the one shown in Fig. 4.2 when the electron affinity of the 6H-SiC is greater than that of the Si otherwise it looks similar to the one shown in Fig. 4.20 when the electron affinity of the 6H-SiC is less than that of the Si. The threshold voltage and conduction losses of the p-Si/N-6H-SiC heterojunction diode increase when the electron affinity of the 6H-SIC is less than that of the Si.

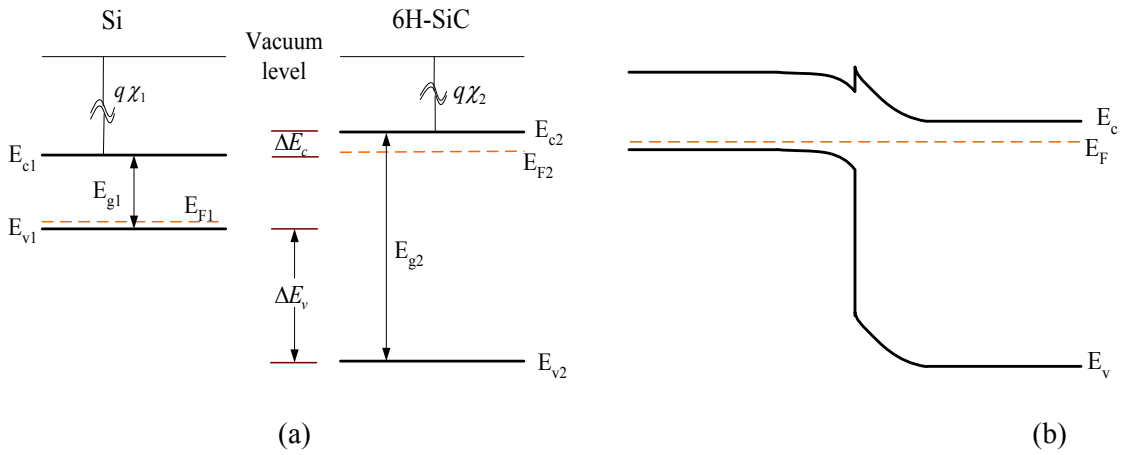



**Fig. 4.20** (a) Energy band diagram of isolated Si and 6H-SiC where the electron affinity of the 6H-SiC is smaller than the default value of the 6H-SiC as well as smaller than the Si (b) Energy band diagram of the p-Si/N-6H-SiC heterojunction interface at thermal equilibrium.

## 4.4 Merged p-i-n Si/6H-SiC Heterojunction Diode

This section describes the operation of the merged p-i-n Si/6H-SiC heterojunction diode. The difference between p-Si/N-6H-SiC heterojunction diode and merged p-i-n Si/6H-SiC diode is that the merged p-i-n Si/6H-SiC heterojunction diode has additional p-doped islands in SiC at the heterojunction interface as shown in Fig. 4.21. This merged p-i-n heterojunction diode acts as a unipolar diode up to certain current densities and it becomes bipolar diode at (very) high current densities when the junction between P-SiC and N-SiC is forward biased. For the diode to work more efficient in bipolar mode, the heterojunction between p-Si and P-6H-SiC should have an ohmic contact behavior. Therefore, to understand the operation of this heterojunction diode, first one should understand the heterojunction interfaces that are involved in the diode. As shown in Fig. 4.21, there are two kinds of heterojunction interfaces which are p-Si/N-6H-SiC and p-Si/P-6H-SiC. The former one is already explained in the previous section and the later one will be explained in the following section.

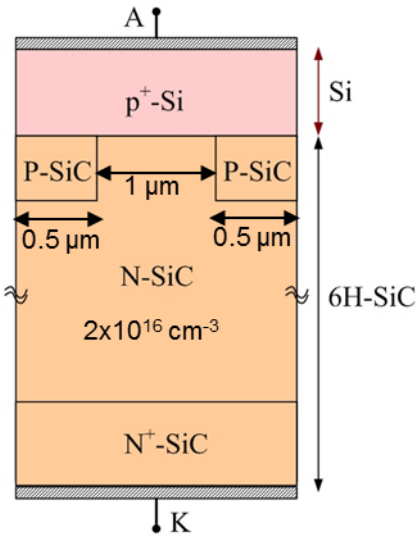



**Fig. 4.21** Schematic structure of a merged p-i-n Si/6H-SiC heterojunction diode

### 4.4.1 p-Si/P-6H-SiC Heterojunction

This section describes an isotype heterojunction interface between p-Si/P-6H-SiC by energy band diagrams for two different doping cases. In case one doping, the doping of the P-6H-SiC is about $1x10^{17}$ $cm^{-3}$ whereas for the case two doping it is about $5x10^{19}$ $cm^{-3}$. For both the cases the p-Si doping is about $5x10^{19}$ $cm^{-3}$. The type of simulations that have been performed to analyze the electrical characteristics of the p-Si/P-6H-SiC heterojunction interface are depicted in Table 4.3. The schematic structure of p-Si/P-6H-SiC heterojunction diode is illustrated in Fig. 4.22. The energy band diagrams of p-Si/P-6H-SiC heterojunction interface are illustrated in Fig. 4.23 for case one (low doped 6H-SiC) and case two (high doped 6H-SiC) doping. 2D simulations have been performed to the structure shown in Fig. 4.22 to examine the current transport mechanism (I-V characteristics) for the two doping cases.

| | | | |
|---|---|---|---|
| **Low doped P-6H-SiC (case one):**<br>p-Si doping: ~$5x10^{19}$ $cm^{-3}$<br>P-6H-SiC doping: ~$1x10^{17}$ $cm^{-3}$ | Without interface traps (assumed the interface is ideal) | With donor traps at the interface<br>Concentration: $5x10^{12}$ $cm^{-2}$ | With acceptor traps at the interface<br>Concentration: $5x10^{12}$ $cm^{-2}$ |
| **High doped P-6H-SiC (case two):**<br>p-Si doping: ~$5x10^{19}$ $cm^{-3}$<br>P-6H-SiC doping:~$5x10^{19}$ $cm^{-3}$ | | | |

**Table 4.3** The type of the simulations that have been performed to analyze the electrical characteristics of the p-Si/P-6H-SiC heterojunction interface

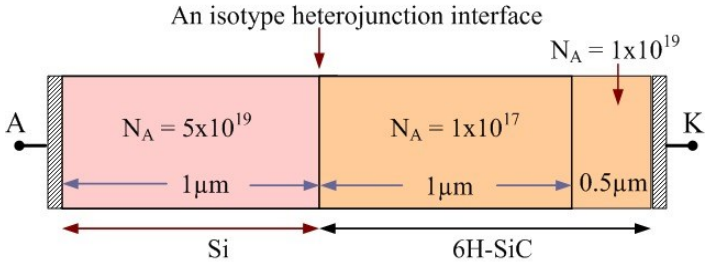



**Fig. 4.22** Schematic structure of p-Si/P-6H-SiC heterojunction interface

Fig. 4.24 illustrates the forward bias I-V characteristics of the p-Si/P-6H-SiC heterojunction interface (the characteristics are nearly the same for with and without interface traps). It can be observed from Fig. 4.24 that there is a huge difference in I-V characteristics for case one and case two doping. In case one doping, where the SiC is low doped ($1x10^{17}$ $cm^{-3}$), the current flow in the diode is almost zero even up to 4 V since there is a large barrier for holes to go from p-Si to P-6H-SiC as shown in Fig. 4.23.

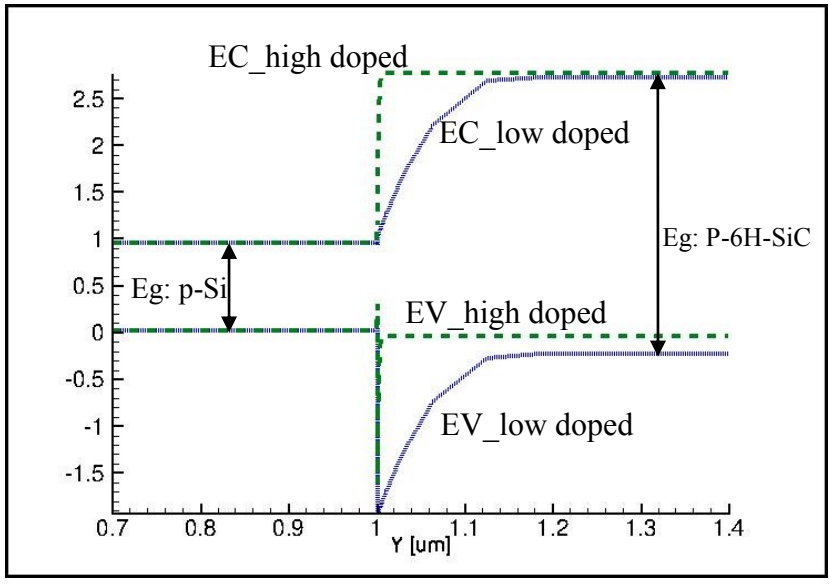



**Fig. 4.23** Energy band diagrams of p-Si/P-6H-SiC heterojunction interface for two different dopings of P-6H-SiC (low doped and high doped P-6H-SiC). For both the doping cases, the doping of the p-Si is same and it is about $5x10^{19}$ $cm^{-3}$.

Whereas, in case two doping (the doping of the SiC is ~ $5x10^{19}$ $cm^{-3}$), the p-Si/P-6H-SiC heterojunction interface behaves like ohmic contact i.e., the conduction losses are very low even at very high current densities, despite of large barrier for holes to go from p-Si to P-6H-SiC. The reason being that, the tunneling mechanism at the heterojunction interface i.e., the carriers (holes) are tunneling through the heterojunction interface since both Si and SiC are heavily doped.

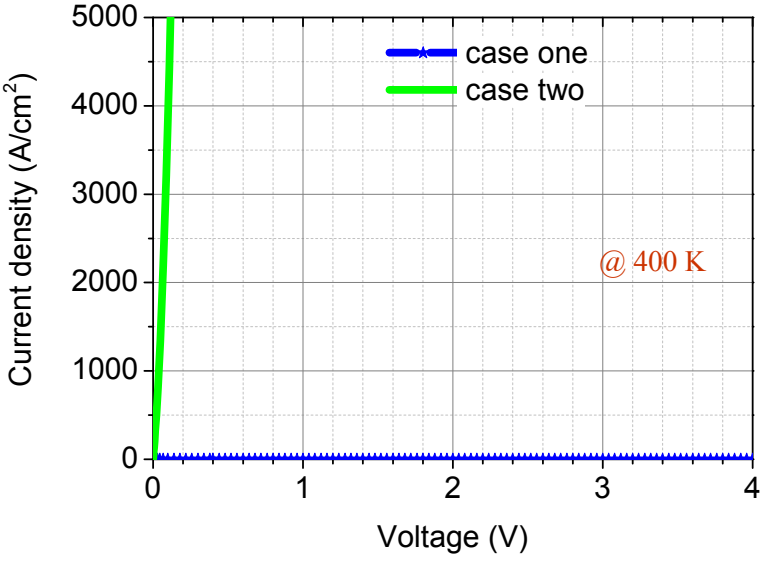



**Fig. 4.24** Forward I-V characteristics of p-Si/P-6H-SiC heterojunction diode for case one and case two doping. In case one, SiC doping is $1x10^{17}$ $cm^{-3}$ whereas in case two it is about $5x10^{19}$ $cm^{-3}$. For both the cases Si doping is the same and it is about $5x10^{19}$ $cm^{-3}$.

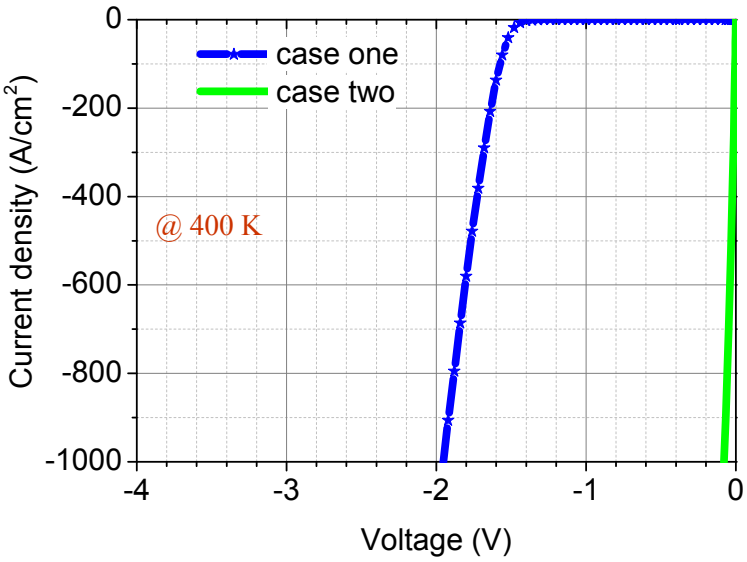



**Fig. 4.25** Reverse I-V characteristics of p-Si/P-6H-SiC heterojunction diode for case one and case two doping. In case one, SiC doping is $1x10^{17}$ $cm^{-3}$ whereas in case two it is about $5x10^{19}$ $cm^{-3}$. For both the cases Si doping is the same and it is about $5x10^{19}$ $cm^{-3}$.

Fig. 4.25 illustrates the reverse bias I-V characteristics of the p-Si/P-6H-SiC heterojunction interface (the characteristics are nearly the same for with and without interface traps). It can be observed from Fig. 4.25 that there is a huge difference in I-V characteristics for case one and case two doping. In case one doping, where the SiC is low doped ($1x10^{17}$ $cm^{-3}$), the diode starts conducting reasonable currents only after 1.5 V since there is a large barrier for holes to go from P-6H-SiC to p-Si as shown in Fig. 4.23. Whereas, in case two doping (the doping of the SiC is ~ $5x10^{19}$ $cm^{-3}$), the p-Si/P-6H-SiC heterojunction interface behaves like ohmic contact i.e., very low (negligibly low) conduction losses even at very high current densities, despite of large barrier for holes to go from p-Si to P-6H-SiC owing to the tunneling mechanism at the heterojunction interface, like in forward bias.

From these simulations it can be observed that p-Si/P-6H-SiC heterojunction interface has an ohmic contact behavior (negligible conduction losses even at high current densities) if both Si and SiC regions are heavily doped. Therefore, this can be employed in merged p-i-n Si/SiC heterojunction diode.

### 4.4.2 Operation Principle of Merged p-i-n Si/6H-SiC Heterojunction Diode

This section describes the operation principle of merged p-i-n Si/6H-SiC heterojunction diode and presents the simulated I-V characteristics of 600 V merged p-i-n Si/SiC heterojunction diode. The schematic structure of merged p-i-n Si/SiC heterojunction diode is illustrated in Fig. 4.21. Here the p-Si and P-SiC are heavily doped resulting in an ohmic contact behavior of heterojunction interface between p-Si and P-SiC (i.e. potential of the P-SiC is nearly the same as p-Si). As explained in section 4.1, the effect of interface traps on the I-V characteristics of p-Si/N-6H-SiC diode is quite small when the p-Si is heavily doped. Therefore the interface

traps are not considered in the simulations of merged p-i-n Si/SiC heterojunction diode since p-Si is heavily doped (the doping of the drift region i.e., N-SiC is $2x10^{16}$ $cm^{-3}$).

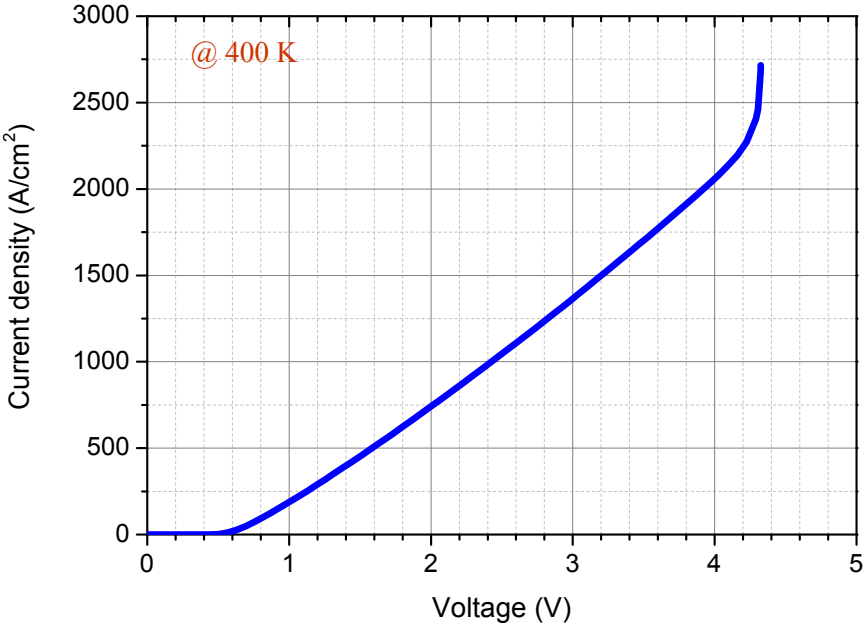



**Fig. 4.26** Forward bias I-V characteristics of merged p-i-n Si/SiC heterojunction diode at 400 K

Fig. 4.26 illustrates the forward bias I-V characteristics of merged p-i-n Si/SiC heterojunction diode at 400 K. The I-V characteristics of the merged p-i-n Si/SiC heterojunction diode are similar to that of the characteristics of p-Si/N-6H-SiC heterojunction diode (i.e. unipolar like Schottky diode characteristics) up to certain current densities (in this case about 2000 $A/cm^2$). However, at higher current densities, the merged p-i-n Si/SiC heterojunction diode becomes bipolar since the junction between P-SiC and N-SiC becomes forward biased and starts to inject carriers. This feature ensures the surge current capability of the device. Nevertheless, in this case, it is to be noted that the simulation stopped converging once the device entered into the bipolar mode and it seems that there is a tendency for a snapback in voltage at higher current densities (the snapback effect could be eliminated by changing the distance between two $p^+$-SiC regions and width of these regions).

Fig. 4.27 illustrates the hole density distribution in the merged p-i-n Si/SiC heterojunction diode at different anode voltages (or at different current densities). It can be seen from Fig. 4.27 that there is no injection of holes neither from p-Si nor from P-SiC (i.e. negligibly small amount of hole concentration in SiC drift region (N-SiC)) at anode voltage of 3 V. Therefore, this device acts as a unipolar diode. However, at 4 V, P-SiC starts to inject holes into drift region. The merged p-i-n Si/SiC heterojunction diode changes its behavior from unipolar to bipolar at/around 4 V. Therefore, changes its I-V characteristics from linear behavior to exponential behavior as shown in Fig. 4.26.

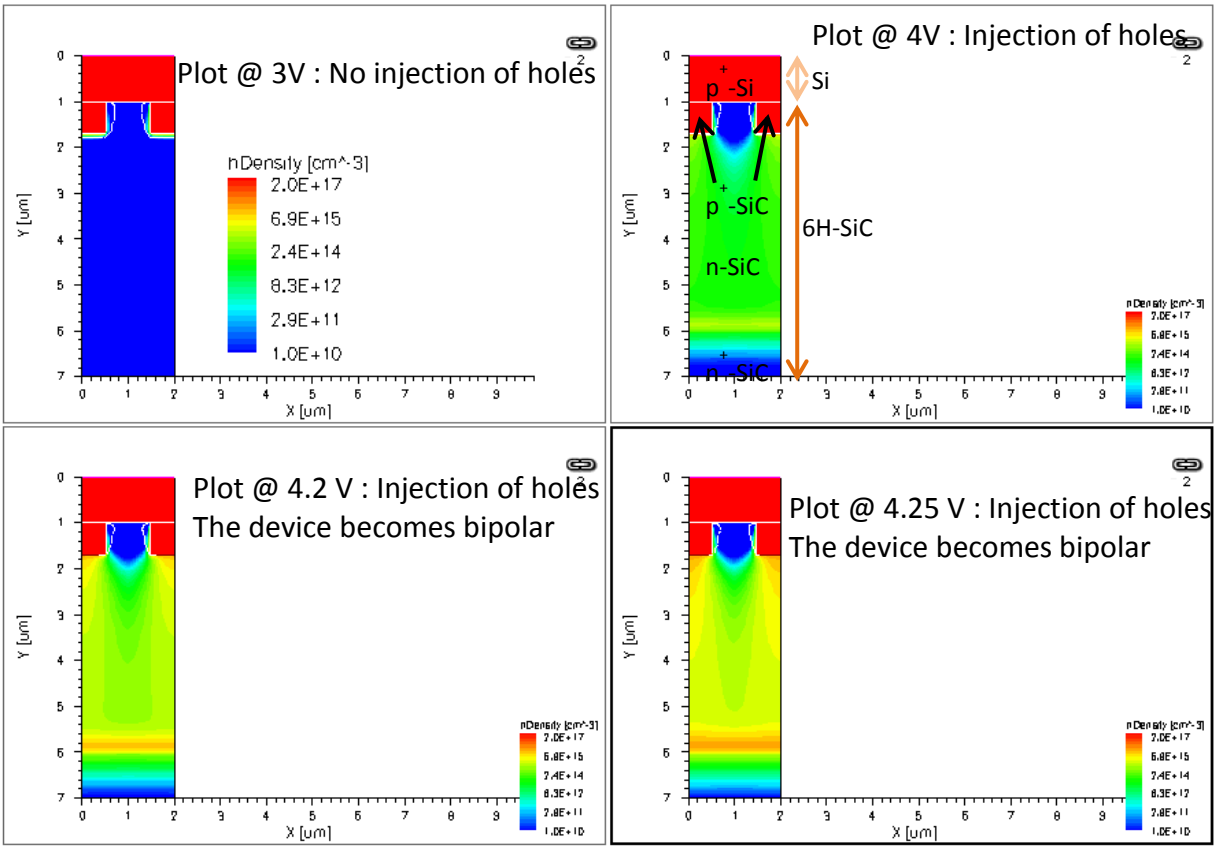



**Fig. 4.27** Hole density distribution in the merged p-i-n Si/SiC heterojunction diode at different anode voltages

# Chapter 5

# Summary

This work presented the concept of two novel types of unipolar diodes which have low threshold voltage and thereby low conduction losses. Both the Regenerative diode and merged p-i-n Si/SiC heterojunction diode have shown unipolar diode I-V characteristics up to certain current densities (at nominal current densities) and become bipolar at high current densities. This feature ensures the surge current capability of the devices and thereby reliable operation of these devices in their applications.

## 5.1 Regenerative Diode

In this work, the concept and simulation results of the novel power diode named as "Regenerative diode" have been presented. Regenerative diode is a normally-on diode (i.e. zero threshold voltage) which is having regenerative blocking capability. The main advantages of this diode are reduction or removal of the threshold voltage and unipolar diode like characteristics. Regenerative diode can be developed with a series combination of two complementary JFETs which are normally-on. The possible integrated versions of the Regenerative diode have been discussed. The simulation results have shown that the trench Regenerative diode has a better on-state characteristics compared to that of the planar Regenerative diode. It has been observed from the simulation results that the Regenerative diode behaves as a unipolar diode (with almost zero threshold voltage) at low and nominal current densities and become bipolar at higher current densities. This feature ensures the surge current capability of the device and hence reliable operation of the device in its applications.

The temperature dependence of I-V characteristics of the considered Regenerative diode has been investigated. It has been observed from the simulation results that the Regenerative diode shows a positive temperature coefficient of I-V characteristics in unipolar region. The static and dynamic characteristics of the considered Regenerative diode have been compared with that of the JBS/MPS rectifier. The simulation results have shown that the Regenerative diode has a better on-state as well as blocking characteristics than that of the JBS/MPS rectifier. Therefore, the Regenerative diode could be an interesting alternative to the p-i-n diodes, SBDs or JBS rectifiers in the low voltage regime. The Regenerative diode can be fabricated with existing or available technology but it might be expensive to fabricate when compared to that of the JBS rectifier or SBD. The simulation results have shown that the Regenerative diode with Silicon-on-Insulator technology can act as a unipolar diode even at higher current densities. In this structure, the insulator is only needed to prohibit the minority carrier injection in the drift region and not for blocking. In this work the other applications of the Regenerative diode as a protection device or as a current limiter have also been discussed.

## 5.2 Si/6H-SiC Heterojunction Diode

In this work, a simulation study on 600 V Si/6H-SiC heterojunction diode is presented. The device simulations have been performed to analyze the heterojunction interface between n-Si/N-6H-SiC, p-Si/N-6H-SiC and p-Si/P-6H-SiC. The influence of doping and interface states (traps) on the I-V characteristics of Si/SiC heterojunction diode has been investigated. The simulation results have shown that the effect of interface traps on the I-V characteristics of Si/6H-SiC heterojunction diode can be negligible if the Si is heavily doped. The p-Si/N-6H-SiC heterojunction diode (in case of heavily doped Si) has a lower threshold voltage than that of the 6H-SiC SBD thereby better on-state characteristics than that of the 6H-SiC SBD for nearly the same blocking characteristics (600 V blocking capability). The simulations have been performed at different temperatures and the p-Si/N-6H-SiC heterojunction diode shows a positive temperature coefficient of resistance at higher current densities like Schottky diode. The static and dynamic characteristics of the p-Si/N-6H-SiC heterojunction diode are similar to that of the 6H-SiC SBD (unipolar diode characteristics) with better on-state characteristics than that of the 6H-SiC SBD. The simulation results have also shown that the threshold voltage of the p-Si/N-6H-SiC heterojunction diode increases if the electron affinity of the 6H-SiC is smaller than that of the Si.

The simulation results have also shown that the novel type of heterojunction diode called merged p-i-n Si/SiC can be implemented if both p-regions of the Si and SiC are heavily doped (The interface between p-Si and P-6H-SiC has an ohmic contact behavior if both Si and SiC are heavily doped). The merged p-i-n Si/SiC heterojunction diode is a p-Si/N-6H-SiC heterojunction diode with additional p-islands in the SiC at the heterojunction interface. The I-V characteristics of the merged p-i-n Si/SiC heterojunction diode are similar to that of the I-V characteristics of p-Si/N-6H-SiC heterojunction diode (i.e. unipolar like Schottky diode characteristics) up to certain current densities and at very high current densities the merged p-i-n Si/SiC heterojunction diode becomes bipolar. This feature ensures the surge current capability of the device and hence reliable operation of the device in its applications. In spite of unavoidable uncertainties on the physical parameters of the Si/6H-SiC heterojunction diode, the results may encourage further experimental work on such a Schottky-like heterostructure device.

# Appendix A

# The relation between the current density and the junction voltage in a P-i-N diode

There are two junctions in a p-i-n diode which are denoted by $J_1$ and $J_2$ as shown in Fig. A.1. $V_{J1}$ is the junction voltage at $J_1$ and $V_{J2}$ is the junction voltage at $J_2$. It would be easy to understand the relation between junction voltage and current density if there is one common junction voltage instead of two.

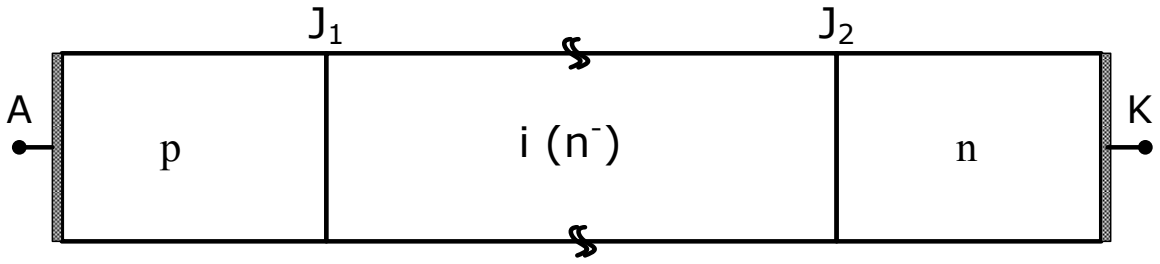



**Fig. A.1** The schematic structure of a p-i-n diode

In case of high level injection; the injected hole concentration from region p to region $n^-$ at junction $J_1$ is

$$P_{n^-} = P_{pl} = P_{0n^-}.e^{\frac{qV_{J1}}{kT}} \text{ -----(1)}$$

where $P_{on^-}$ is the hole concentration in the middle region at thermal equilibrium. $P_{n^-}$ is the minority carrier (hole) concentration in the middle region at junction $J_1$ for a forward bias voltage $V_{J1}$. In case of high level injection, $P_{n^-} = P_{pl}$, where the injected hole concentration is higher than the doping concentration of the middle region. $P_{pl}$ is the plasma concentration. In this state, the injected electron concentration from region n to region $n^-$ at junction $J_2$ is

$$N_{pl} = N_{0n^-}.e^{\frac{qV_{J2}}{kT}} \text{ ------ (2)}$$

where $N_{0n^-}$ is the electron concentration in the middle region at thermal equilibrium. From equations (1) and (2)

$$V_{J1} = \frac{kT}{q}.\ln\left(\frac{P_{pl}}{P_{0n^-}}\right) \text{ ---- (3)}$$

$$V_{J2} = \frac{kT}{q}.\ln\left(\frac{N_{pl}}{N_{0n^-}}\right) \text{ ---- (4)}$$

From equations (3) and (4), the total junction voltage $V_J$ is,

$$V_J = V_{J1} + V_{J2} = \frac{kT}{q}.\ln\left(\frac{P_{pl}.N_{pl}}{N_{0n^-}.P_{0n^-}}\right) \text{----(5)}$$

In case of high level injection, $N_{pl}$ is approximately equal to $P_{pl}$ to maintain charge neutrality. $N_{pl}$ can be written as $P_{pl} + N_{0n^-}$ where $P_{pl} >> N_{0n^-}$. Therefore, $N_{pl}$ = $P_{pl}$ and then the equation (5) becomes as,

$$V_J = \frac{kT}{q}.\ln\left(\frac{P_{pl}.P_{pl}}{N_{0n^-}.P_{0n^-}}\right) = \frac{kT}{q}.\ln\left(\frac{P_{pl}^{\ 2}}{n_i^{\ 2}}\right) \text{---- (6)}$$

where $n_i$ is the intrinsic carrier concentration. In high level injection process, until some current densities the recombination current in the middle region dominates and the total current flow is approximately equal to the recombination current in the middle region. Therefore it can be written as $J = J_M$; where J is the total current density and $J_M$ is the recombination current density in the middle region. In this condition, the plasma concentration in the middle region increases proportionally with the current density. From this one can get a relation between junction voltage and current density by replacing $P_{pl}$ in equation (6) with the current density "J". Then the junction voltage $V_J$ is,

$$V_J \propto \frac{kT}{q}.\ln\left(J^2\right) \text{ ----(7)}$$

At these current densities, the voltage drop across the middle region is independent of the current density flowing through the diode. In this case, the voltage drop across the middle region $V_M$ is negligibly small (assume high ambipolar diffusion length) and therefore the voltage drop across the diode $V_F$ is approximately equal to the junction voltage $V_J$. In this case, from equation (7), the relation between the current density and voltage drop across the diode is as follows,

$$J \propto \exp\left(\frac{qV_F}{2kT}\right) \text{---- (8)}$$

For further increases of the current densities, the recombination current in the emitter regions (p and n regions) dominates (injection and recombination of the minority carriers in the emitter regions). The plasma concentration in the middle region, no longer increases proportionally with the current density but as the square root of the current density. At these current densities, from equation (6), the junction voltage can be written as

$$V_J \propto \frac{kT}{q}.\ln(J) \quad \text{---- (9)}$$

If the equation (9) is rearranged, the relation between the current density and the junction voltage is as follows,

$$J \propto \exp\left(\frac{qV_J}{kT}\right) \text{-----(10)}$$

# Appendix B

# Material Properties at 300 K

| Material | Band gap Eg [eV] | Carrier Mobility [$cm^2/(V.s)$] | | Dielectric constant $\varepsilon_r$ | Breakdown field $E_{br}$ [kV/cm] |
|---|---|---|---|---|---|
| | | Electrons, $\mu_n$ | Holes, $\mu_p$ | | |
| Si | 1.12 | 1450 | 450 | 11.9 | 300 |
| 6H-SiC | 3.02 | 400 | 101 | 9.66 | 2500 |
| 4H-SiC | 3.26 | 1000 | 115 | 9.66 | 2200 |
| $SiO_2$ | 9 | - | - | 3.9 | 8000 |

*Reference: [Stef'06]*

# Appendix C

# n-Si/N-6H-SiC Heterojunction

This section presents, an isotype heterojunction interface between n-Si/N-6H-SiC by energy band diagrams for two different doping cases. For each doping case, it considers without interface states (ideal) and with interface states (donor and acceptor type traps) at the heterojunction interface.

In case one doping, n-regions of the two semiconductors are doped equally and it is about $2x10^{16}$ $cm^{-3}$ as shown in Fig. C.1(a). In case two doping, n-type Si is heavily doped and the doping concentration is about $5x10^{19}$ $cm^{-3}$ and n-type 6H-SiC doping is $2x10^{16}$ $cm^{-3}$ as shown in Fig. C.1(b).

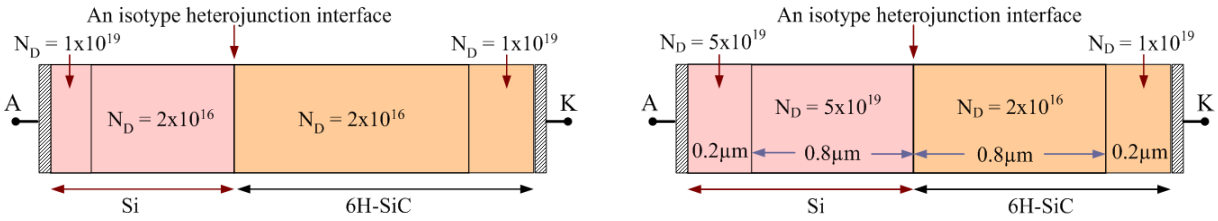



**Fig. C.1** The schematic structure of n-Si/N-6H-SiC heterojunction diode (a) for case one doping (low doped n-Si) (b) for case two doping (high doped n-Si)

**Case one doping (n-Si:$2x10^{16}$ $cm^{-3}$ and N-6H-SiC: $2x10^{16}$ $cm^{-3}$):** The energy band diagrams of an isotype n-N heterojunction between Si/6H-SiC at thermal equilibrium are depicted in Fig. C.2 for the case one doping.

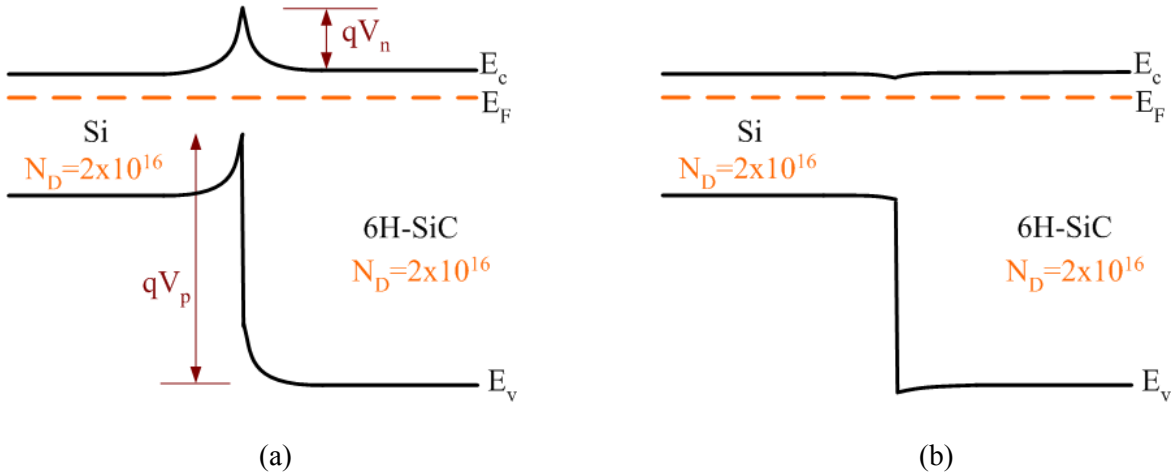



**Fig. C.2** Energy band diagram of an isotype n-N heterojunction between Si/6H-SiC **(a)** In case of acceptor traps **(b)** In case of donor traps and/or without traps

As shown in Fig. C.2(a), acceptor type traps at the interface resulted in depletion layers on both sides of the heterojunction interface thereby a barrier like Schottky is created at the

interface for the electrons to go from n-type 6H-SiC to n-type Si and vice versa. The similar type of effect was observed for the n-N heterojunction between Ge/Si in case of acceptor type traps by Oldham and Milnes [Oldh'64], [Calo'67]. In case of donor type traps and/or without traps, there is no barrier for electrons in either way as shown in Fig. C.2(b). The energy band diagram is almost same for both donor type traps and without traps case but it differs for the acceptor type traps case. As explained in Chapter 4, it is assumed that the traps are in the mid gap of the Si semiconductor and the concentration of the traps at the interface is about $5x10^{12}$ $cm^{-2}$ with capture cross section of about $1x10^{-15}$ $cm^2$. As shown in Fig. C.2, the energy band diagram of an isotype n-N heterojunction interface between Si/6H-SiC is not influenced by donor type traps but acceptor type traps. The reason is that almost all donor type traps are neutralized since they are located below the Fermi level, whereas in the case of acceptor type traps, they possess negative charge since they are below the Fermi level. In case of InGaAs/GaAs heterojunction interface, the authors [Jich'87] considered the interface traps becoming negatively charged below the Fermi level at thermal equilibrium. Fig. C.3 illustrates the space charge distribution of an isotype n-N heterojunction interface between Si/6H-SiC at thermal equilibrium.

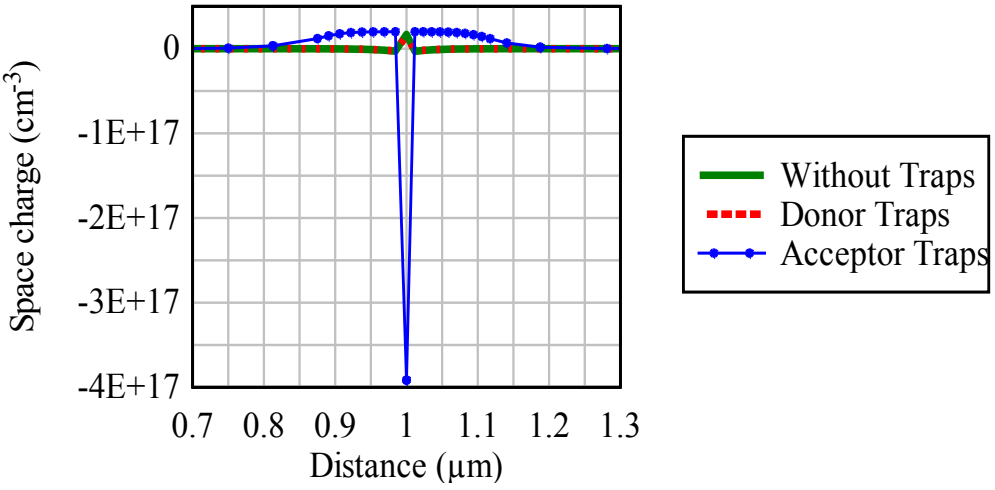



**Fig. C.3** Space charge distribution of n-N heterojunction interface between Si/6H-SiC

The space charge distribution is almost same for both donor type traps and without traps case. The electron trapped charge (acceptor type trap density) is about 4e17 $cm^{-3}$ acts as a negative charge sheet at the interface in case of acceptor type traps. This is higher than the doping concentration of the n-Si and N-6H-SiC regions. Therefore, to compensate this negative charge, positive space charge regions are formed on both sides of the heterojunction interface as shown in Fig. C.3. The n- N heterojunction interface between Si/6H-SiC is at 1µm. The structure shown in Fig. C.1(a) has been simulated in device simulator DESSIS at 400 K to analyze the effect of interface traps on the I-V characteristics of the n-Si/N-6H-SiC heterojunction diode. In these simulations, the charge effects of the interface states are included in the Poisson and charge-carrier balance equations. Three different simulations have been performed to the structure shown in Fig. C.1(a). One simulation has been performed without any traps and other simulations with consideration of traps at the interface (one

simulation with the donor type traps and another simulation with the acceptor type traps). For all these simulations, a positive voltage is applied to the anode (A) with respect to the cathode (K) to obtain forward bias I-V characteristics as shown in Fig. C.4(a), whereas the reverse bias I-V characteristics as shown in Fig. C.4(b) are obtained by changing the polarity of the anode and cathode.

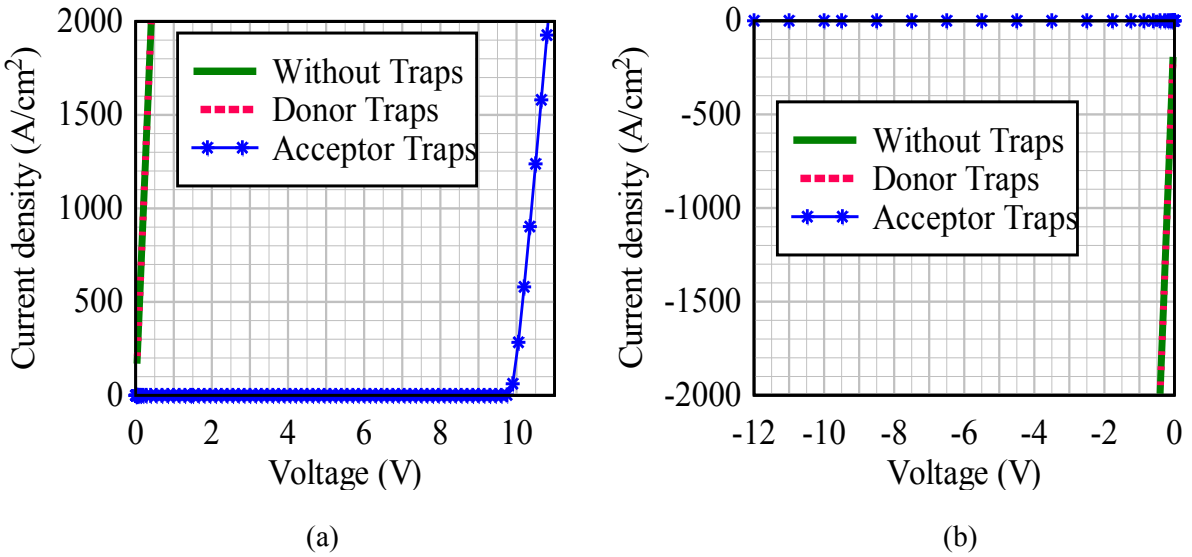



**Fig. C.4** The I-V characteristics of the n-Si/N-6H-SiC heterojunction diode for case one doping (n-Si:$2x10^{16}$ $cm^{-3}$ and N-6H-SiC: $2x10^{16}$ $cm^{-3}$) **(a)** Forward bias **(b)** Reverse bias

As shown in Fig. C.4(a), the I-V characteristics are exactly the same for without traps and/or with the donor type traps. In this the current flow starts from the zero voltage i.e. there is no threshold voltage because there is no barrier as shown in Fig. C.2 (b) for the electrons to move from N-6H-SiC to n-Si. However, the I-V characteristics are different in case of acceptor type traps and it blocks the current flow until breakdown occurs at the heterojunction. In the case of acceptor type traps as shown in Fig. C.2 (a), there is a barrier for electrons to move from N-6H-SiC to n-Si at thermal equilibrium. In this case, the interface between n-Si/N-6H-SiC acts as two metal-semiconductor diodes connected metal-metal. The similar type of behavior was observed in n-N heterojunction interface between Ge and Si with the acceptor type traps by Oldham and Milnes [Oldh'64]. Therefore in n-Si/N-6H-SiC heterojunction diode, the depletion layer starts penetrating into n-Si with the increase of the positive anode voltage. With the further increase of the anode potential, break down occurs due to the avalanche generation of the carriers at the heterojunction when the electric field reaches critical value (about $2x10^5$ V/cm) in Si. In case of acceptor type traps, Fig. C.5 (a) and Fig. C.6 (a) illustrate the electric field distribution and impact ionization at different positive anode voltages. However, in this case, the breakdown voltage of the n-N heterojunction between Si/6H-SiC depends on the doping and width of the n-Si region. It blocks more voltage when n-Si region is less doped and has more width.

In the reverse bias, as shown in Fig. C.4(b), the I-V characteristics are exactly the same for without traps and/or with the donor type traps. In addition, they are exactly similar to that of the forward bias characteristics as shown in Fig. C.4(a). The reason being that in either

direction, there is no barrier (shown in Fig. C.2 (a)) for electrons to move from n-Si to N-6H-SiC and vice versa. Like in the forward bias, the I-V characteristics are different in case of acceptor type traps from that of the without traps case. However, in the reverse bias, in case of acceptor type traps, it blocks more voltage when compared to that of the forward bias case. The reason is that, in the reverse bias, the depletion layer penetrates into the N-6H-SiC with the increase of the anode potential. Therefore, it blocks more voltage because 6H-SiC has about 10 times higher breakdown electric field (about $2x10^6$ V/cm) than that of the Si. In case of acceptor type traps, the breakdown (avalanche generation) occurs at about 10 V in the forward bias case whereas it occurs at about 120 V in the reverse bias. In case of acceptor type traps, Fig. C.5 (b) and Fig. C.6 (b) illustrate the electric field distribution and impact ionization at different negative anode voltages.

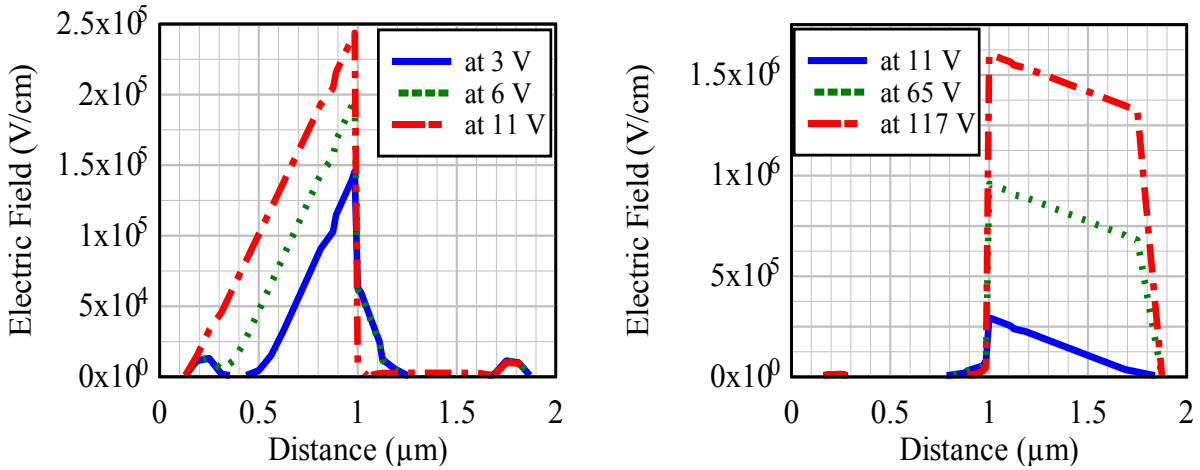



**Fig. C.5** Electric field distribution in n-N heterojunction diode between Si and 6H-SiC **(a)** Forward bias **(b)** Reverse bias

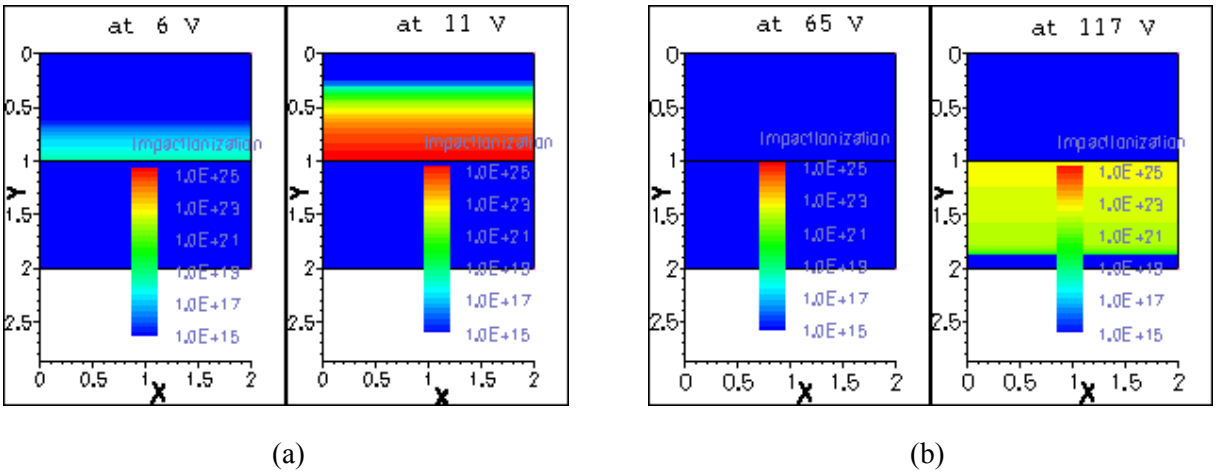



**Fig. C.6** Impact Ionization (avalanche generation) in n-N heterojunction diode between Si and 6H-SiC **(a)** Forward bias **(b)** Reverse bias

**Case two doping (n-Si:5x10$^{19}$ cm$^{-3}$ and N-6H-SiC: 2x10$^{16}$ cm$^{-3}$):** Fig. C.7 illustrates the energy band diagram of an isotype n-N heterojunction between Si and 6H-SiC at thermal equilibrium for the case two doping in which n-Si doping is 5x10$^{19}$ cm$^{-3}$ and N-6H-SiC doping is 2x10$^{16}$ cm$^{-3}$. In this case, unlike in case one doping, the energy band diagram looks similar for without traps and with traps case. In this case, unlike in case one doping, the space charge is almost same for without traps and with traps case and it is positive in the Si side and negative in the SiC side at the heterojunction interface. Like in case one doping, donor type traps have no influence on the energy band diagram of the n-N heterojunction interface because they are neutralized. However, unlike in case one doping, even acceptor type traps have no influence on the energy band diagram of the heterojunction interface though they possess negative charge since the Si region is heavily doped.

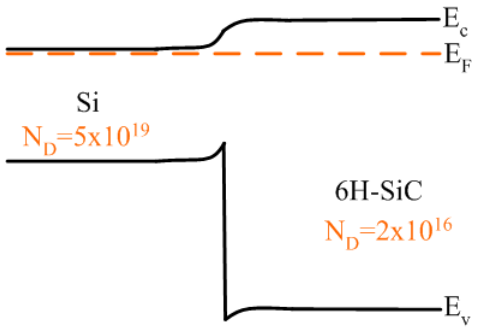



**Fig. C.7** Energy band diagram of an isotype n-Si/N-6H-SiC where the doping of the n-Si and N-6H-SiC are 5x10$^{19}$ and 2x10$^{16}$ cm$^{-3}$ respectively

Here also the above three different simulations (without traps, donor type traps and acceptor type traps) have been performed to the structure shown in Fig. C.1(b). It can be seen from Fig. C.8 (a) that there is no difference in forward bias I-V characteristics between without traps case and with traps (donor or acceptor type) case and the current flow starts from zero voltage (i.e., no threshold voltage) because there is no barrier for electrons to move from N-6H-SiC to n-Si.

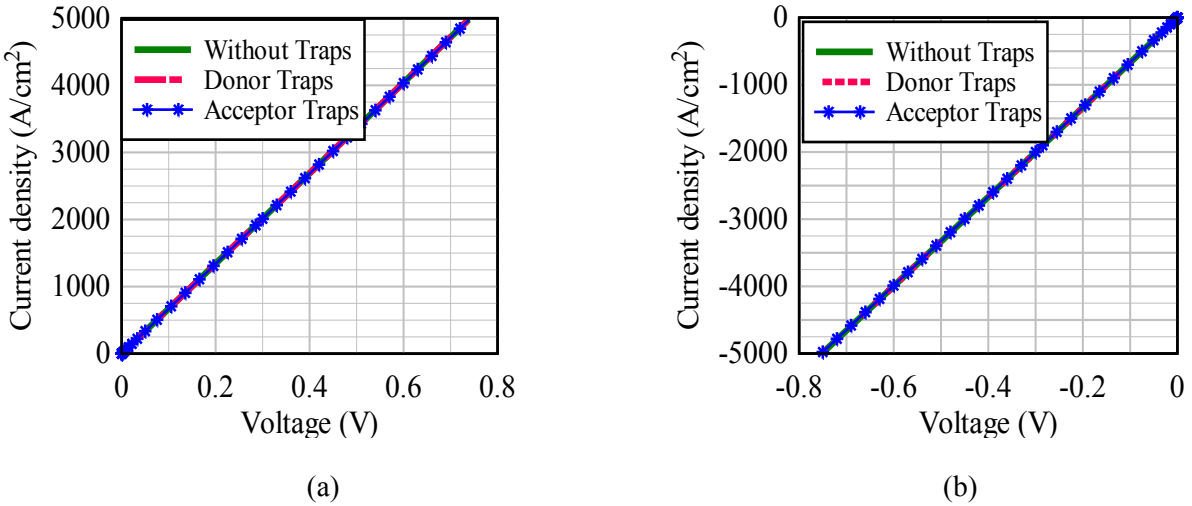



**Fig. C.8** The I-V characteristics of the n-Si/N-6H-SiC heterojunction diode in case two doping **(a)** Forward bias **(b)** Reverse bias

A similar type of I-V characteristics can also be observed in the reverse direction as shown in Fig. C.8 (b) and the characteristics are exactly the same for without traps and with traps case. When the I-V characteristics between forward bias and reverse bias are compared, a very small increase of on-state voltage can be observed in the reverse bias compared to that of the forward bias. The reason being that, in the reverse bias case the electrons must move from n-Si to N-6H-SiC but there is a very small barrier for electrons as shown in Fig. C**.7** whereas in the forward bias case, there is no barrier for electrons to move from N-6H-SiC to n-Si.

# Appendix D

# Symbols

| | |
|---|---|
| $A^*$ | Richardson constant |
| $D_N$ | Electron Diffusion Coefficient |
| $D_P$ | Hole Diffusion Coefficient |
| $E_{C/V}$ | Conduction/Valence Band Edges |
| $E_{D/A}$ | Donar/Acceptor Dopant Ionization Energy |
| $E_g$ | Bandgap Energy |
| $g_{D/A}$ | Degenracy Factor |
| $J$ | Current Density |
| $J_{Diff}$ | Total Diffusion Current |
| $J_{DN}$ | Diffusion Current in N Region |
| $J_{DP}$ | Diffusion Current in P Region |
| $J_E$ | Recombintion Current in Emitter Region |
| $J_F$ | Forward Current Density |
| $J_L$ | Reverse Leakage Current Density |
| $P_{pl}$ | Plasma Concentration |
| $q$ | Elementary Charge |
| $R_S$ | Series Resistance |
| $T$ | Absolute Temperature |
| $V_d$ | Diffusion Voltage |
| $V_F$ | Forward Voltage |
| $V_J$ | Junction Voltage |
| $V_M$ | Voltage Drop across Middle Region |
| $V_{th}$ | Thermal Voltage |
| $W$ | Width of Depletion Layer |
| $W_n$ | Width of Drift Region |
| $W_P$ | Width of P Region |
| $W_N$ | Width of N Region |
| $\eta$ | Ideality Factor |
| $\tau_r$ | Recombination Life Time |
| $\tau_{SC}$ | Space Charge Generation Life Time |
| $\varphi_b$ | Barrier Height |

# Appendix E

# Acronyms

| | |
|---|---|
| BJT | Bipolar Junction Transistor |
| BSIT | Bipolar mode SIT |
| Cool MOS | Superjunction MOSFET |
| DMOS | Double-Diffused Metal-Oxide-Semiconductor |
| DUT | Device Under Test |
| FET | Field Effect Transistor |
| HEMT | High Electron Mobility Transistor |
| JFET | Junction FET |
| JBS | Junction Barrier Controlled Schottky |
| LASER | Light Amplification by Stimulated Emission of Radiation |
| MESFET | Metal-Semiconductor FET |
| MPS | Merged P-i-N Schottky |
| MOS | Metal-Oxide-Semiconductor |
| MOSFET | Metal-Oxide-Semiconductor FET |
| SBD | Schottky Barrier Diode/Schottky Diode |
| SOI | Silicon-On-Insulator |
| SIT | Static Induction Transistor |
| U-MOSFET | Trench MOSFET |
| SMPS | Switch Mode Power Supply |

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