DESIGN OF DIGITAL MOVING TARGET INDICATION RADAR PROCESSORS

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DESIGN OF DIGITAL MOVING TARGET INDICATION

RADAR PROCESSORS

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SUMMARY

This dissertation develops design procedures for improved MTI (Moving Target Indication) radar processors for systems utilizing PRF's (Pulse Repetition Frequencies) which are either constant or varying.

Early MTI radar processors had outputs which varied significantly with changes in target radial velocity or Doppler frequency. The interpulse period was often varied from pulse-to-pulse (staggering the PRF) to reduce these fluctuations, but appreciable variations remained.

The advent of modern radar systems employing step scan antennas and large scale digital signal processing offers a new flexibility which permits design of MTI systems having substantially improved performance. However, many processors used with these systems continue to use designs which are holdovers from earlier, less flexible, MTI systems.

Improved design procedures which utilize the flexibility and capability of modern radar systems are described. These design procedures specify a desired and achievable value of MTI Improvement, I, and, subject to this constraint, minimize variations of processor response as a function of target Doppler frequency. Processors have been designed for both the staggered and the unstaggered PRF case.

While the unstaggered PRF case may be considered a special

case of the staggered PRF case for which the interpulse period is constant, there are certain mathematical simplifications which are possible for the unstaggered PRF case. These simplifications permit some classes of processors to be specified which are unique to unstaggered PRF's. Three classes of processors have been designed for the unstaggered PRF case. These processors are: the Equal Ripple Processor, the Maximally Flat Processor, and the Constrained Improvement Processor. The first uses simplex methods for a solution, the second involves solution of a set of simultaneous linear equations, while the third makes use of Lagrange multiplier techniques. Each of these processors offers considerable improvement in uniformity of response when compared with earlier designs.

Two classes of staggered PRF processors have been developed; the Maximum Improvement Processors (MIP's), and the Constrained Improvement Processors (CIP's). Lagrange multiplier methods are used to design the processors, and the Fletcher-Powell method to arrive at a solution. The MIP's maximize I while keeping the average response equal to one. Examination of the resulting responses shows significant increases in I over previous designs, with no degradation (and in some cases an improvement) in uniformity of Doppler frequency response. The CIP's limit I to some desirable (and achievable) value, and subject to this constraint, minimize the mean square deviation of processor response from unity with changes in target Doppler frequency. The design procedure involves selection of both processor weight functions and interpulse periods.

Representative CIP's are compared with earlier processors, and

a considerable improvement in uniformity of frequency response is achieved with a CIP. A complete absence of blind speeds may often be achieved over the desired range of target Doppler frequencies, and fluctuations in processor response with changes in target Doppler frequency are considerably reduced over previous designs. A number of representative processor parameters are tabulated, and effects on processor performance of such variables as clutter spectral width, number of pulses processed, and maximum and minimum interpulse spacing are considered.

LIST OF FREQUENTLY USED SYMBOLS

Symbol	Description
C	total clutter input power.
C_i	shape of clutter spectrum at processor input.
C_{out}	total power at processor output due to clutter input.
f	normalized frequency, $f = F/PRF$.
f'	highest normalized Doppler frequency of interest.
F	frequency.
F_r	PRF.
$G(\omega)$, $G(f)$, $G(F)$	processor power response as a function of argument.
$\overline{G(\omega)}$, $\overline{G(f)}$, $\overline{G(F)}$	average processor power response as a function of argument.[2]
$h(t)$	processor impulse response.
$H(\omega)$	processor voltage response.
I	MTI Improvement.
T	interpulse period for unstaggered PRF system. Nominal Interpulse period for staggered PRF system.
$\overline{T}_{in}$	average target input power, averaged over all target Doppler frequencies of interest.
$\overline{T}_{out}$	average processor output power due to target, averaged over all target Doppler frequencies of interest.
X_i	weight of the $i^{\underline{th}}$ pulse.

LIST OF FREQUENTLY USED SYMBOLS (Continued)

Symbol	Description
$\delta(t)$	unit impulse function.
ΔT_i	shift in time of the $i^{\underline{th}}$ pulse from its nominal (unstaggered) point in time.
$\Delta(i)$	normalized parameter $\Delta(i) = \Delta T_i/T$.
ϵ	an amount, $0 \leq \epsilon \leq 1$, by which the interpulse period is varied.
η	an amount, $0 \leq \eta \leq 0.5$, which establishes the frequency range of interest for a Constrained Improvement Processor in an unstaggered PRF system.
λ_c	the transmitted wave length.
λ	the Lagrange multiplier.
σ_c	standard deviation of clutter spectrum in Hertz, $\sigma_c = 2\sigma_v/\lambda_c$.
σ_v	standard deviation of clutter spectrum, in meters/sec, $\sigma_v = \sigma_c \lambda_c/2$.
σ	normalized standard deviation of clutter spectrum, $\sigma = \sigma_c T$.
ω	radian frequency, $\omega = 2\pi F$.

CHAPTER I

INTRODUCTION

This dissertation develops improved Moving Target Indication (MTI) processor design techniques for use in modern radar systems. These systems often employ advanced digital signal processing techniques and utilize step-scan phased array antennas to search, acquire, and track a number of targets simultaneously. For these high performance radars, it is desirable that the MTI processor (or filter) have sufficient clutter rejection to operate in a heavy clutter environment, that the target detectability remain relatively constant over the expected range of target Doppler frequencies, and that the processing be performed using some specified number of received pulses from the target. Conventional MTI processor designs usually have adequate average clutter rejection, but evidence substantial variations in target detectability as target Doppler frequency changes. If conventional digital filter design techniques are applied in an attempt to develop processors having more uniform detectability, an unacceptably large number of pulses usually need to be processed and radar performance in a clutter environment is degraded.

The design procedures which are developed in this work emphasize processing a specified (small) number of received pulses, achieving the required value of MTI improvement, I, for acceptable system performance,

and, within these constraints, minimizing variations in detectability as a function of target velocity. Improved designs have been developed for both the staggered and unstaggered PRF case.

The unstaggered PRF processors which have been developed are the following: Equal Ripple Processors, which maximize I while bounding variations in processor response; Maximally Flat Processors, which constrain I to some specified value and then set appropriate derivatives of processor response equal to zero; and Constrained Improvement Processors which minimize the mean square fluctuations in frequency response while keeping I equal to a specified constant.

The staggered PRF processors which have been developed are the following: Maximum Improvement Processors (MIP's), which maximize I while keeping the average response equal to one; and Constrained Improvement Processors (CIP's), which minimize the mean square fluctuations in processor response while keeping I equal to some specified value.

Chapter II of this thesis reviews the basics of the MTI radar problem in some detail and summarizes previous work in MTI processor design. Chapter III discusses the development and performance of improved MTI processors for both unstaggered and staggered PRF systems. Comparisons of performance of improved processors with earlier designs are also given in Chapter III as are some tables of representative processor designs. Chapter IV presents Conclusions and Recommendations based on these investigations.

CHAPTER II

BACKGROUND

This chapter presents background information on MTI radar in general, and on pertinent previous investigations in particular. First, MTI radar operating principles are reviewed with emphasis on MTI processor performance. During this review, limitations on system performance of earlier MTI systems are outlined, and characteristics of modern step-scan digital MTI radars are discussed.

Second, the use of techniques from statistical detection theory to develop optimum unstructured MTI processors is reviewed. This unstructured approach has not been successful in developing MTI processors for more than two received pulses, so a more structured approach has been used by a number of investigators.

Third, several previous structured approaches to MTI processor design are discussed. The optimization of MTI processors using weighted sums of sampled signals is one example of such a structured approach, but these processors suffer from a lack of uniformity of processor response with changes in target Doppler frequency. Another example of such a structured approach is the consideration of processor design as a digital filter optimization problem. Unfortunately, conventional digital filter design procedures do not emphasize processing a fixed number of pulses nor achieving the required value of MTI improvement.

Finally, several specialized MTI processor design procedures which have been developed by earlier investigators for both staggered and unstaggered PRF systems are discussed.

This chapter shows that practical MTI processor design procedures must: (1) achieve the required value of MTI improvement for operation in a clutter environment, (2) minimize variations in processor response with changes in target Doppler frequency, (3) process a specified number of received pulses, and (4) bound pulse spacings in a staggered PRF system. Previous design methods have not emphasized one or more of these criteria. The material presented in this chapter leads to the topics treated in Chapter III, which discusses improved processors which incorporate these requirements into the design procedures.

MTI Radar Systems

The problem of the detection of desired radar targets in the presence of unwanted signals is one of continuing interest to the radar designer. These unwanted signals may arise from a number of sources, such as thermal noise, interference from nearby radars, or reflections from such objects as trees, ground, and precipitation. The problem of reliable detection of targets of interest in the presence of the signals reflected from trees, water, and various natural features on the earth's surface is especially difficult. These unwanted signals, commonly called clutter, normally fluctuate with time and may vary over a dynamic range as large as 70 dB; in many situations of interest the average clutter signal may be much larger than the signals from desired targets. Thus, these clutter returns may severely limit radar system performance.

Fundamental Operating Principles

If the desired target has an appreciable radial velocity with respect to the radar, it is possible to use the fact that the target and clutter have different Doppler frequency shifts in order to differentiate between the desired targets and the unwanted clutter. Systems which utilize this concept have been built for a number of years; a representative block diagram of one such MTI (Moving Target Indication) radar is shown in Figure 1. The basic frequency of operation is established by the rf oscillator; energy from this rf oscillator is fed through a pulsed rf amplifier and duplexer to the antenna where it is radiated. The rf energy propagates through space and is reflected from both the desired targets and the unwanted clutter and the back-scattered energy is received by the antenna. This received energy then passes through the duplexer to a phase-sensitive detector. There the received signal is mixed with a reference signal derived from the rf oscillator. The output of the phase-sensitive detector is a bipolar video signal; signals corresponding to stationary targets will be unchanging with time, while the video signals corresponding to targets having a non-zero radial velocity with respect to the radar location will exhibit amplitude fluctuations at the Doppler frequency of the target. These video signals then go to a MTI processor (also called a MTI canceller or MTI filter). One such processor, shown in Figure 1, successively subtracts the video signals on a pulse-to-pulse basis.

This processor, or filter, is a crucial portion of the MTI radar. The first such processors used analog signal processing and analog

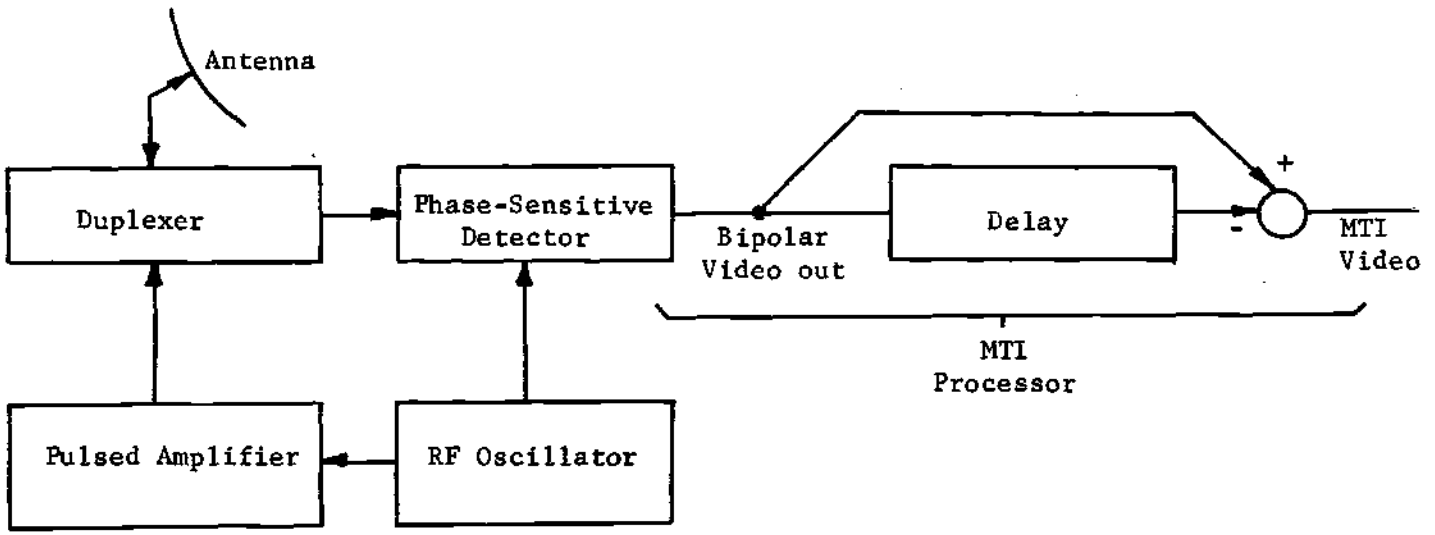


Figure 1. Simplified Block Diagram of an MTI Radar System.

delay lines in order to suppress the clutter returns. In practice, in order to more fully suppress clutter, MTI processors often process more than two received pulses; these higher order cancellers are obtained by cascading additional processors as shown in Figure 2. The transfer function of these higher order processors may be easily derived using z-transform methods. The transfer functions of some of these higher order processors are tabulated in Table 1. These will be referred to as conventional processors in the remainder of the thesis. The frequency response of a conventional three pulse processor is given in Figure 3.

Limitations on System Performance

An MTI radar system which incorporated an MTI processor as described above represented a substantial improvement over systems without MTI. However, a number of factors limit its performance. Clutter returns from such features as trees, the sea, or weather are not truly stationary, that is, they have some non-zero spectral width and, therefore, the canceller does not remove all of the clutter and some residue remains. Barlow [1]*, Nathanson [2], and Kerr [3] all note that much of this type of clutter is composed of a non-fluctuating and a fluctuating component and the relative magnitudes of the two components are a function of the type of clutter being considered. The non-fluctuating component may be cancelled completely, but the fluctuating component cannot be completely suppressed, and may considerably degrade system performance.

*Numbers in brackets refer to references in the bibliography in the back of this thesis.

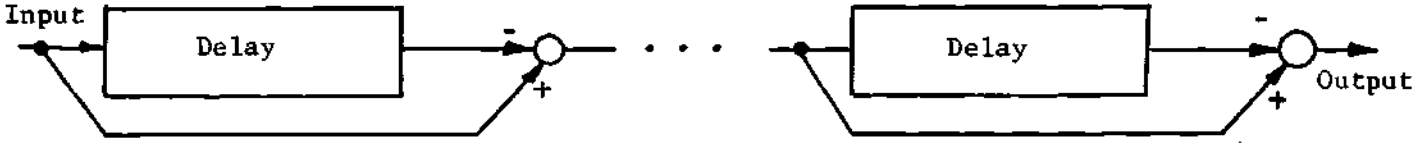


Figure 2. Higher Order MTI Processors Obtained by Cascading Two Pulse MTI Processors.

Table 1. Transfer Functions for Conventional MTI Processors

Number of Pulses Processed	Transfer Function (z-transform)
2	$1 - z^{-1}$
3	$1 - 2z^{-1} + z^{-2}$
4	$1 - 3z^{-1} + 3z^{-2} - z^{-3}$
5	$1 - 4z^{-1} + 6z^{-2} - 4z^{-3} + z^{-4}$

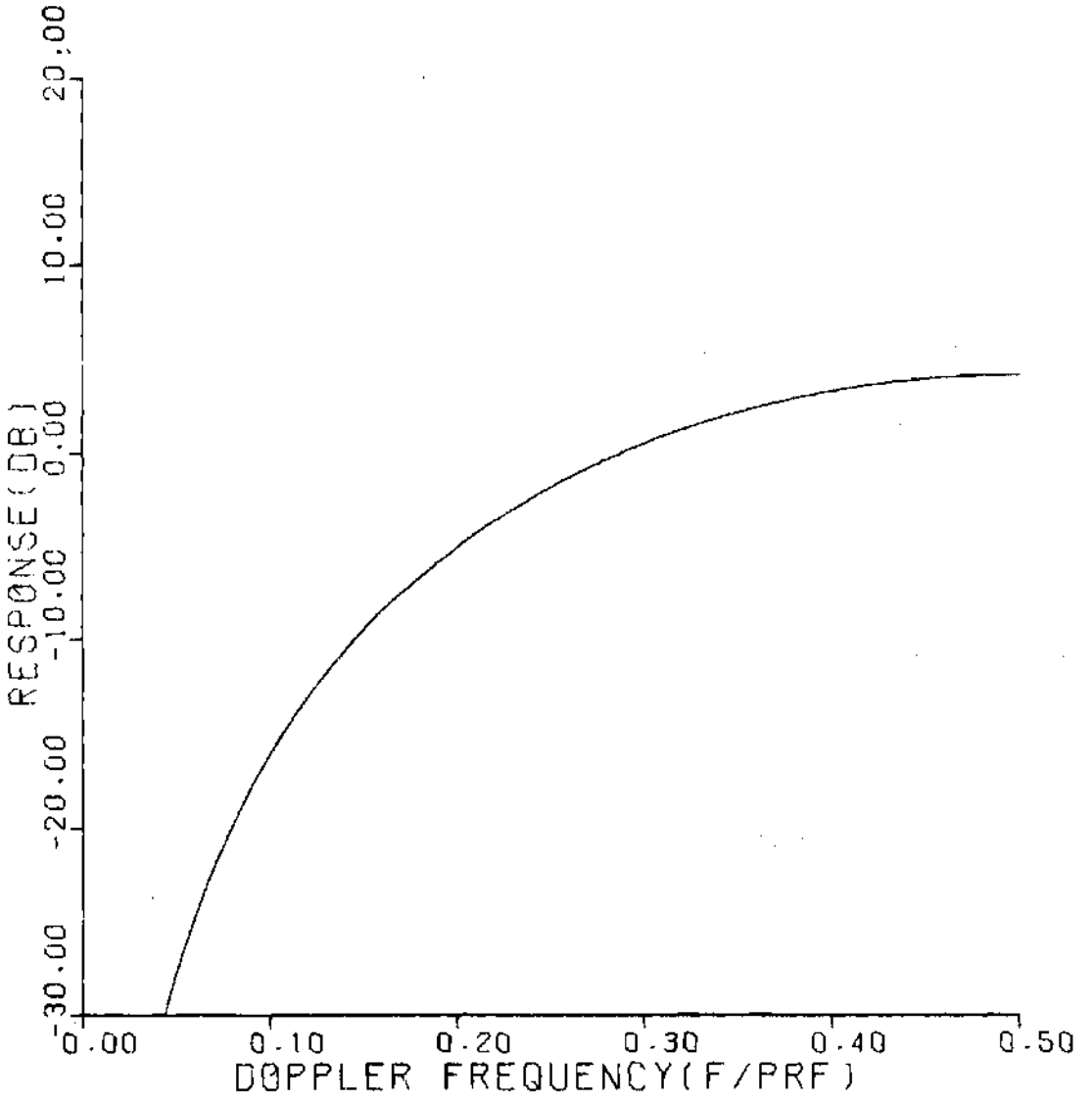


Figure 3. Frequency Response of Conventional Three Pulse MTI Processor. The Frequency Axis is Presented as the Ratio of the Doppler Frequency to the Pulse Repetition Frequency (PRF).

Barlow [1], Nathanson [2], Kerr [3], Barton [4], and Shrader [5] have all observed that the shape of the spectrum for clutter associated with woods, the sea or with rain clouds is approximately zero-mean Gaussian, with a spectral spread which is related to operating frequency, clutter type, and environmental conditions. It has been observed that the standard deviation of clutter spectrum, expressed in meters/sec, σ_v, is approximately independent of frequency. Then the standard deviation of the clutter spectrum, σ_c, expressed in Hz, is

$$\sigma_c = \frac{2\sigma_v}{\lambda_c} ,$$

where λ_c is the operating wavelength in meters. For scanning systems, this width may be further broadened by scan-modulation, but this effect is absent in step-scan systems. Some representative values of σ_v are summarized in Table 2.

Gaussian clutter power spectra have been reported by the majority of researchers. However, Fishbein, et al., [6], report that clutter spectra of a wooded area measured using a relatively short pulse, high frequency, radar exhibited high frequency components larger than would be predicted by Gaussian spectra. Fishbein found that a $1/(1 + (F/F_c)^3)$ (where F is the frequency and F_c is the "corner frequency") frequency dependence more closely fitted these experimental data. For this reason, a brief examination of the consequences of this type of clutter spectra was conducted. As correctly stated by Fishbein, system performance is degraded from what would be achieved if the clutter spectra were Gaussian. However, this degradation

Table 2. Summary of Standard Deviations of Clutter Spectra [4,5]

Clutter Source	Wind Speed, Knots	σ_v, m/sec
Sparse Woods	Calm	0.017
Wooded Hills	10	0.04
Wooded Hills	20	0.22
Wooded Hills	25	0.12
Wooded Hills	40	0.32
Sea Echo	*	0.7
Sea Echo	*	0.75-1.0
Sea Echo	8-12	0.46-1.1
Sea Echo	Windy	0.89
Rain Clouds	*	1.8-4.0
Rain Clouds	*	2.0

*Not included in original references.

becomes appreciable only if large numbers of pulses are being processed. Therefore, since our concern is primarily with systems processing small numbers of pulses, the performance of processors discussed in this thesis is not particularly sensitive to which spectral shape accurately describes the clutter. However, if desired, all of the design procedures carried out in this thesis may be modified for use with $1/(1 + (F/F_c)^3)$ clutter spectral shapes, but only minor changes in results would be produced.

One widely used measure of the ability of an MTI system to operate in a clutter environment is the Improvement Factor, or MTI Improvement, I. I is "...a power ratio which is defined as $I = r_o/r_i$, where r_o is the output ratio of target to clutter, and r_i is the target-to-clutter ratio at the input to the receiver, averaged over all target speeds." [5]

If the frequency region of interest is given by $0 \leq F \leq F'$, the input clutter power spectral density by $C_i(F)$, and the power response of the processor by $G(F)$, then the total time-average clutter power at the receiver input is

$$C = \int_{-\infty}^{\infty} C_i(F)\ dF,$$

and the total power at the output of the MTI processor is given by

$$C_{out} = \int_{-\infty}^{\infty} C_i(F)\ G(F)\ dF.$$

The input time-average target-to-clutter ratio is given by T_{in}/C,

where T_{in} is the input target signal strength. Taking the frequency average of the target-to-clutter ratio at the input (assuming all target velocities are equally probable),

$$r_i = \frac{\frac{1}{2F'}\int_{-F'}^{F'} T_{in}\, dF}{C} = \frac{\frac{1}{F'}\int_{o}^{F'} T_{in}\, dF}{C} .$$

If $\overline{T}_{in}$ is defined as

$$\overline{T}_{in} = \frac{1}{F'}\int_{o}^{F'} T_{in}\, dF,$$

r_i may be expressed as

$$r_i = \frac{\overline{T}_{in}}{C} .$$

For most cases of interest, $\overline{T}_{in} = T_{in}$.

Similarly, r_o may be expressed as

$$r_o = \frac{\frac{1}{F'}\int_{o}^{F} T_{in}\, G(F)\, dF}{C_{out}} .$$

Defining the quantity $\overline{T}_{out}$ as

$$\overline{T}_{out} = \frac{1}{F'}\int_{o}^{F'} T_{in}\, G(F)\, dF,$$

r_o becomes

$$r_o = \frac{\overline{T}_{out}}{C_{out}} .$$

Then the definition of I becomes

$$I = \frac{r_o}{r_i} = \frac{\overline{T}_{out}}{C_{out}} \Big/ \frac{\overline{T}_{in}}{C} = \frac{\overline{T}_{out}}{\overline{T}_{in}} \cdot \frac{C}{C_{out}} \quad ,$$

using the notation

$$\overline{T}_{out} = \frac{1}{F'} \int_o^{F'} T_{in}\, G(F)\, dF$$

$$\overline{T}_{in} = \frac{1}{F'} \int_o^{F'} T_{in}\, dF$$

$$C = \int_{-\infty}^{\infty} C_i(F)\, dF$$

$$C_{out} = \int_{-\infty}^{\infty} C_i(F)\, G(F)\, dF,$$

where

T_{in} is the input signal power

$C_i(F)$ is the clutter power spectral density

$G(F)$ is the power gain of the MTI processor.

I is sometimes expressed in decibels as 10 $\log_{10}$ of the quantity defined above. Also, $\overline{T}_{out}$ is often referred to as the (frequency) average target power output, and $\overline{T}_{in}$ as the (frequency) average target power input.

The use of the Improvement, I, (also called the improvement factor, or the Reference Gain, G) rather than some of the earlier performance measures is recommended, since I is independent of any constant gain factors in the MTI processor.

The response of an MTI system to targets having a wide range of Doppler frequencies is a function of the specific target Doppler shift;

for some radial velocities for which the Doppler frequency equals an integral multiple of the PRF (pulse repetition frequency) the system is "blind" (the response is zero). This problem may be avoided by changing the interpulse period from pulse-to-pulse (commonly called "staggering" the PRF). However, in systems which employ analog delay lines, there is little flexibility in the choice of interpulse periods.

Thus, simple analog MTI systems have a number of limitations. Among these limitations are: limited values of I due to clutter spectral width or antenna beam motion; blind speeds and phases; amplitude instabilities in receiver signal processing circuits; variations in time delays; and variations in target detectability with changes in radial velocity.

Modern Step-Scan Digital MTI Radar

The introduction of step-scan phased array antennas and the advent of large scale digital signal processing in recent years has revolutionized MTI radar systems. The use of phased array antennas provides a step-scan capability which permits the rapid examination of a large area without the degradation in performance due to beam motion during the time the received signals are being processed. The use of digital techniques for signal storage and processing has permitted significant flexibility in both processing of the received signal and in the choice of the interpulse periods in PRF stagger sequences.

These step-scan MTI systems which utilize digital processing have a number of advantages including: elimination of fluctuations

due to antenna beam motion; increased amplitude stability in signal processing circuits; stability of time delays; compatibility with other digital operations; flexibility in antenna beam scanning format; and compatibility with staggered PRF.

However, the performance of the digital MTI processor may be limited by the need to minimize the number of pulses processed, by variations in target detectability with changes in target radial velocity, and by system cost and complexity. There is another limitation on performance which is due to the conversion of analog signals to digital format. This limitation is due to quantization errors and may appreciably limit the achievable value of I; this effect has been analyzed [7] and is a function of the number of bits in the digital word. Table 3 presents these improvement limits due to analog-to-digital quantization errors. For smaller numbers of bits, one can see that the achievable improvement could easily become limited by quantization errors rather than by uncancelled components of clutter.

With this background in MTI radar systems, previous work in the design of MTI processors will now be reviewed.

Use of Statistical Detection Theory in Developing Optimum Receivers

Development of optimum receivers has been of substantial interest since radar was first developed. The earliest optimum receiver was for detection of a single pulse in white noise. This concept led to the development of the so-called "matched filter" [8,9,10], namely,

Table 3. Limitation of MTI Improvement, I, Due to Analog-to-Digital Quantization Errors

Number of Bits (including sign)	Maximum Value of I (dB)
4	22.3
5	28.6
6	34.7
7	40.8
8	46.9
9	52.9
10	59.0

one which maximizes the peak signal-to-noise ratio, and has a frequency response given by the complex conjugate of the voltage spectrum of the received pulse.

If the power spectrum of the noise plus received clutter varies with frequency (so-called colored noise), then the optimum filter response becomes (except for a constant time delay) the complex conjugate of the voltage spectrum of the received pulse divided by the power spectrum of the received clutter [11,12]. This fact was used by Urkowitz [13] to derive optimum receivers for detection of targets in clutter.

Rihaczek [14] has pointed out that the class of filters developed by Urkowitz is optimum only when thermal noise may be neglected, and that the presence of both fluctuating clutter and thermal noise requires more complex filters than those developed by Urkowitz.

If desired targets and unwanted clutter returns are separated in time (range) and/or in frequency, substantial improvement in performance is possible using combined signal and filter optimization. Delong and Hofstetter [15,16] consider the problem of detection of a point target in random clutter using combined signal-receiver optimization. The detection of a target of known Doppler shift has been treated by Westerfeld, et al., [17] and by Van Trees [18]. Spafford [19,20], Stutt and Spafford [21], and Rummler [22] have treated the optimum receiver when clutter and target signals have different areas of occupancy on the range-frequency plane.

In many cases the expected Doppler shift of the received signal

is not known, a priori, and the expected range of signals overlaps the clutter in both range and in frequency. The optimum estimation receiver for this case becomes essentially a bank of matched filters, one for each expected Doppler frequency [23]; this configuration is very similar to the pulse Doppler radar which employs a comb filter or filter bank followed by a threshold for both velocity estimation and target detection.

The optimum detection receiver corresponding to the conventional MTI radar system appears to have been first discussed by Wainstein and Zubakov [24]. The optimum receiver derived by Wainstein and Zubakov for processing the received signal for the two-pulse case consists of optimum processing of both the in-phase and quadrature components of the received signal, pairwise subtraction of these in-phase and quadrature samples, formation of the square of each of these differences, and comparison of the sum of these squares with the threshold [25]. This processing corresponds to the conventional two channel, two pulse MTI canceller. Extension of these results to cases involving more than two pulses has not been successfully carried out for cases of practical interest.

Selin [26] has obtained some optimum detection receivers for the case when the interfering signal is largely uncorrelated from pulse-to-pulse; unfortunately, clutter does not normally exhibit such behavior. Brennan, Reed and Sollfrey [27] have performed analyses for more practical cases, but their approximations resulted in receiver structures which are extremely complex due to the large number of

comb filters required.

From this review, it becomes evident that the specification of the optimum processor from the point of view of statistical detection theory is a formidable task, and one which has been solved exactly only for the case of the two pulse processor. Because of the difficulty in specifying the performance of the optimum receiver, considerable attention has been focused on the design of MTI receivers which form optimum weighted sums for processing sampled signals from moving targets in a clutter environment.

Optimization of MTI Processors Using Weighted Sums of Sampled Signals

It was brought out in the previous section that the optimum MTI receiver, from the point of view of statistical detection theory, is known only for the two-pulse case. The receiver for larger numbers of received pulses has often been approximated as a linear combination of a number of sample values of either the in-phase or the quadrature component of the received signal.

Maximization of the ratio of average output signal (averaged over all expected values of Doppler frequency shifts) to interfering signal (for unstaggered PRF processors) has been treated by Capon [28]. Capon shows that the optimum weight functions, defined as those which maximize the average increase in signal-to-interfering signal ratio (called the reference gain, $\overline{G}_n$, or more commonly the MTI improvement I) depend only upon the covariance matrix of the interfering signal. For highly correlated pulse-to-pulse interference, such as that due to

slowly moving clutter, these optimum weight functions reduce to the conventional three-pulse canceller for the case of processing three received pulses. Capon also shows that the improvement for the three-pulse canceller closely approximates the improvement achieved using a large number of received pulses when processing signals in a background of strongly correlated clutter.

There are three objections to Capon's approach. First, Capon did not demonstrate that the optimum processor may be realized in the assumed linear processing format. It is perhaps appropriate to note that if the linear processing format discussed by Capon were the configuration of the optimum processor, then the optimum Neyman-Pearson test would be the one which maximizes I (see, for example, Spafford [20]).

The second objection is that the improvement, I, is maximized by increasing gain at frequencies where clutter return is small and decreasing gain at frequencies where clutter is significantly present, resulting in substantial variations in response with changes in target Doppler frequency. The response for two and five pulse processors is given in Figure 4, clearly showing these fluctuations which are characteristic of both conventional processors and those of Capon. Increasing the number of pulses does not reduce these fluctuations, but rather increases them. Capon observed that as the number of pulses increases, the response approaches an impulse located at the minimum of the sampled clutter power spectrum. Thus, processors designed to maximize I may have unacceptably small responses to targets with

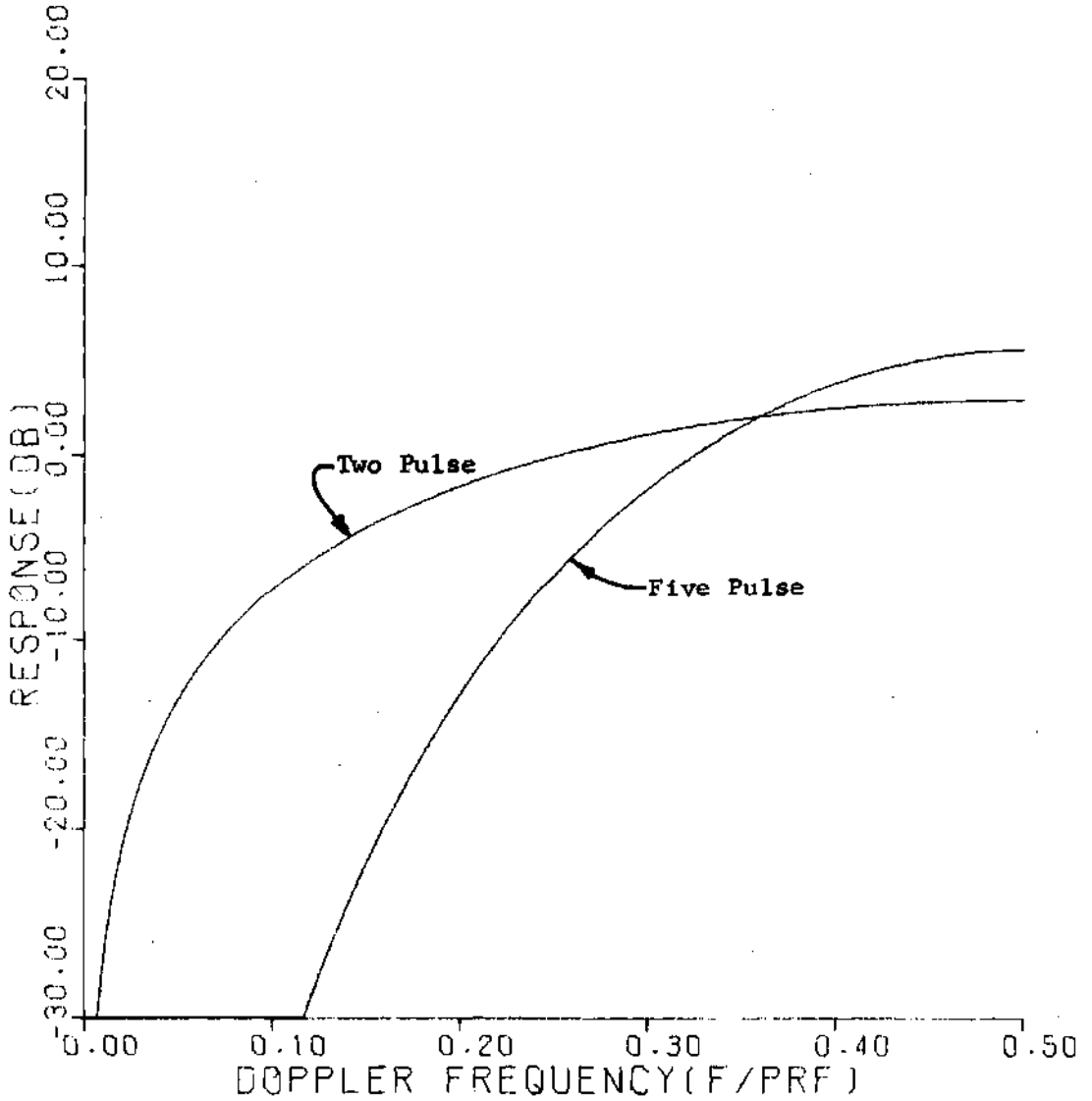


Figure 4. Frequency Responses of Conventional Two Pulse and Five Pulse MTI Processors.

Doppler frequencies in or near the same region as the clutter.

The third objection is that there are substantial practical limitations which are not included in the theory. Most modern high-performance MTI processors utilize digital processing. While round-off error in the computational process does not usually appreciably limit performance, as pointed out earlier in this chapter, analog-to-digital quantization errors usually constrain I to be substantially less than its theoretically achievable maximum value.

MTI Processor Design as a Filter Optimization Problem

As discussed in the preceding section, maximization of the MTI Improvement, I, is often not a satisfactory method for optimizing the processing scheme for an MTI radar, since this results in poor detectability of targets having some particular range of Doppler frequency shifts. This fact leads one to consider uniformity of response of the processor as a function of Doppler frequency as an important consideration in system design. This approach leads naturally to considering the processor to be a filter having as inputs a signal at the Doppler frequency and a signal from clutter plus thermal noise with known power spectral density. Then the filter output can be plotted as a function of input Doppler frequency; one such representation was shown in Figure 4 for conventional processors.

The following discussion of digital filtering will be largely confined to consideration of transversal filters [29,30] (nonrecursive filters or those with no internal feedback loops), because in any practical application only limited numbers of pulses may be processed

from each target. Several constraints determine the number of pulses that may be processed from a given target. In a beam-agile radar such as a phased array system, minimizing the number of pulses from a given target maximizes the number of targets the radar can accommodate. If frequency agility is used, the radar must remain at a given frequency for a sufficient number of pulses to extract the desired information concerning a target; minimizing the number of pulses on target thus maximizes the number of available frequencies the radar may radiate in a specified time. While a recursive filter (one containing feedback loops) could be used and its transient response truncated after the desired number of pulses, the response of such a truncated recursive filter may always be realized as a transversal filter. The difference between the two lies in the practical implementation of the filter.

Various methods have been developed for designing digital filters [31-33]. Their design is often approached by defining an analog filter prototype and appropriately transforming the response to obtain the z-transform of the desired filter. Another approach uses direct search methods to minimize a distance function between actual filter response and desired filter response. In general, either of these approaches yields recursive filters; while these filters' outputs may be truncated after the desired number of pulses, there is generally little control over the number of pulses required to closely approximate the desired steady-state response.

To illustrate the errors in filter response which may occur due

to truncation of a recursive filter designed for a certain steady-state response, a four-pole Butterworth filter response was considered. Its z-transform was expanded in powers of z^{-1} by long division and the series truncated after a selected number of terms. The impulse response of the filter represented by this series was then calculated to determine the truncated frequency response. Figure 5 compares the steady-state response with the response truncated after 3, 5, and 7 pulses. As can be seen, the response of the truncated series is a poor approximation to the steady-state value. Admittedly, this is an extreme case, due to the rapid low-frequency roll-off of the filter, but it serves to illustrate the need for specialized design procedures where the number of available samples is limited.

Three procedures are commonly used in designing transversal digital filters [37-40]. The first involves specifying the sampled finite impulse response of a filter (obtained as an input specification or as a transform of a frequency-sampled response) and utilizing an impulse-invariant transformation to specify the digital filter. Various weighting windows may be used to smooth the ripples in the resulting frequency response. The second method uses a Fourier series approximation (with appropriate windows often incorporated) to a desired response, while the third method is a direct-search method using linear programming techniques to optimize the desired response. These techniques are not particularly applicable to the design of MTI processing filters, since they do not incorporate clutter characteristics into the filter design procedure as a design specification. In

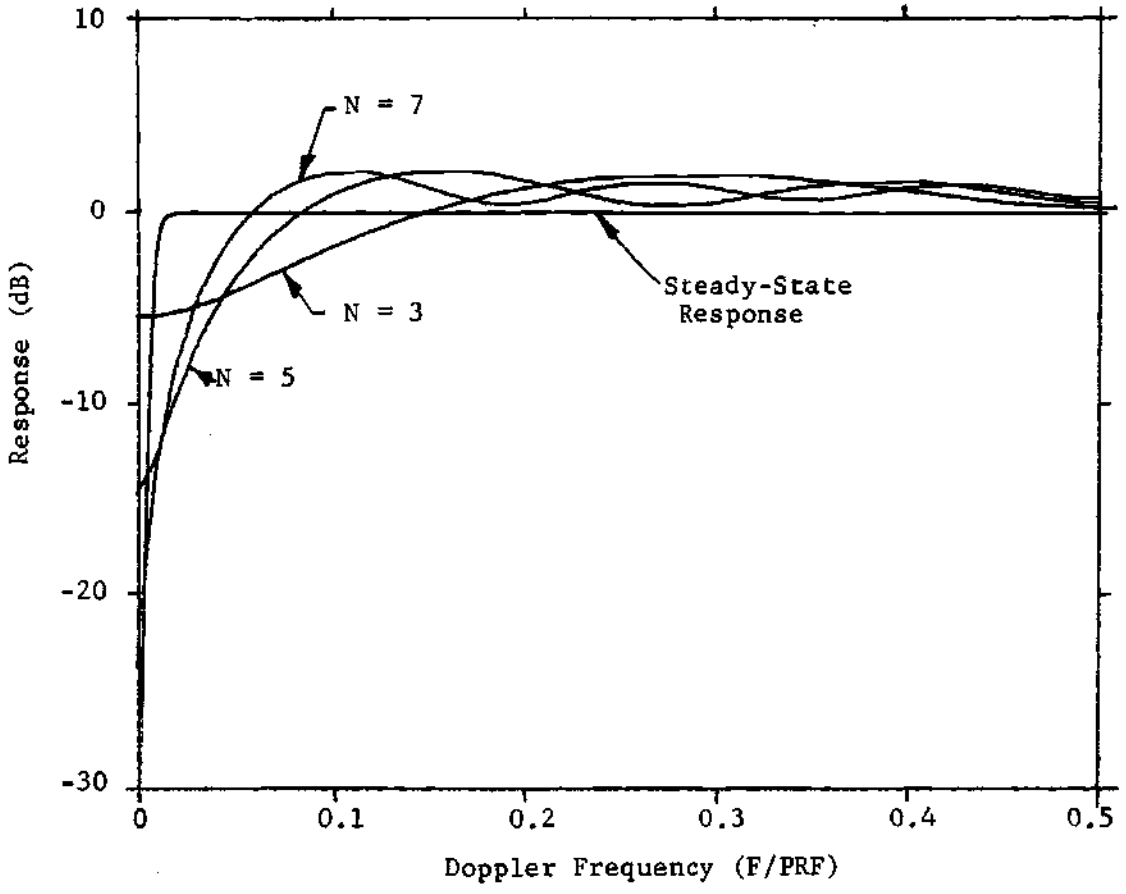


Figure 5. Response for a Four Pole Butterworth High-Pass Filter (labeled Steady-State Response) and the Output of the Same Recursive Filter Terminated After N=3,5, and 7 Pulses were Processed. The Steady-State Response has been Offset for Clarity.

many cases they accept a specific filter response as the design goal, rather than developing optimum processing for a predetermined number of received pulses, a constraint which is determined by the performance requirements of the overall radar system.

The fact that conventional digital filter design techniques are not entirely suitable for the design of MTI processors has led to the development of some specialized procedures for this application. Several of these specialized procedures for unstaggered PRF MTI processors are discussed in the next section.

MTI Processors for Unstaggered PRF Systems

Filter Initialization Techniques

Fletcher and Burlage [41] have observed that a substantial reduction in the settling time of conventional recursive filters may be obtained by setting appropriate initial conditions into the various filter elements. While this technique effectively reduces the settling time of the filter, this approach offers no guarantee that the resulting responses are optimum. In addition, this approach depends upon conventional filter design techniques to produce the basic filter designs, such as Butterworth filters, and clutter rejection is usually not a design parameter of such filters.

"Cost" Minimization MTI Processors

Jacomini [42] has developed a design procedure that takes into account the clutter attenuation in the pass band, the response in a stop-band, and ripple in the pass band. A "cost" is assigned to each

of these factors, and designs developed which minimize the overall "cost" of the filter. This approach has the disadvantage that there is no straightforward means for selecting the various costs. In practice, when the filter is being designed, the improvement, I, is constrained to be some constant, and the cost is apportioned between the pass and stop bands; relative costs are then adjusted until an intuitively satisfying filter response is obtained. More straightforward means for obtaining the same types of results are described in the next chapter.

Staggered PRF MTI Processors

The MTI processors discussed earlier still exhibit blind speeds; the conventional method for reducing the effects of these blind speeds is to stagger the PRF, that is, to change the interpulse period in a systematic method from pulse to pulse. Roy and Lowenschuss [43] discuss the selection of PRF stagger sequences for a specific integral weight processor but do not consider the clutter rejection of the filter as one of the design criteria. Rihaczek [44] discusses choice of PRF stagger for a Doppler system employing a comb filter of known characteristics. Prinsen [45] discusses the maximization of I without regard for the shape of the processor response as a function of target Doppler frequency. Brennan and Reed [46] discuss a procedure for maximizing the average improvement for a given PRF stagger sequence but do not carry out the required analysis. Shrader [47] presents some empirical rules of thumb for designing staggered PRF systems which use processors of the type described by Roy and

Lowenschuss.

Watters [48] has investigated the problem of minimizing the low frequency response of an MTI processor employing integral weights (a conventional four pulse canceller) by selection of appropriate PRF stagger sequences. He determined that a sinusoidal variation in the interpulse period minimized the low frequency response of the filter when conventional integral weights were used in the processor. Taylor [49,50] investigated the problem of minimizing the low frequency response by varying the signal processor weights when a sinusoidal variation in interpulse period was employed. However, neither of these investigations considered uniformity of response to various target Doppler returns as a design criterion and did not consider the clutter rejection, per se, as a design parameter. In addition, the problem of the joint optimization of filter weights and PRF stagger sequences has not been considered in these investigations.

Jacomini [51] has developed processors for the staggered PRF case which are similar to those he discussed for the unstaggered PRF case. That is, a "cost" is assigned to a number of factors and filter weights and PRF stagger sequences selected which minimize the overall filter "cost": The problem of selecting various "costs" for acceptable performance is still a trial and error procedure with this method. In addition, no bounds are placed on the PRF stagger sequence, resulting in required pulse spacings which may be impractically small.

The responses of processors suggested by Shrader, Taylor, and by Jacomini will be discussed in more detail in the next chapter where these processors are compared with improved MTI processors.

CHAPTER III

DESIGN OF IMPROVED DIGITAL MTI RADAR PROCESSORS

A number of factors enter into the design and specification of the MTI processor for a radar system. Among the design requirements are: (1) the system must have sufficient MTI improvement for operation in a heavy clutter environment; (2) target detectability should remain relatively constant for the range of expected Doppler frequencies; and (3) processing should be performed using some specified number of received pulses. The motivation for the first two requirements is rather obvious, and the third requirement is dictated by the desire to minimize the number of pulses required on a given target (and consequently to maximize the number of targets which can be investigated) in a beam-agile radar such as a phased-array radar, or by the desire to optimize performance when frequency agility is used (by minimizing the number of pulses transmitted at one frequency).

Staggered PRF systems have the additional requirement that the pulse spacing variations must be carefully controlled in order to preserve the required unambiguous range of the radar, or to remain within the duty cycle limits of the transmitter. These unique requirements call for specialized design procedures. Several design procedures for improved structured MTI processors which emphasize the above criteria are developed in this chapter. First, unstaggered designs are discussed, since their mathematical development is more straightforward and provides insight into the more complex designs

which follow. Three types of unstaggered processors are discussed: the Equal Ripple Processors; the Maximally Flat Processors; and the Constrained Improvement Processors. The performance of these processors is presented, and it is observed that their performance is no longer optimum when the PRF is staggered.

Second, design procedures for staggered PRF systems are presented. Two classes of processors are developed; Maximum Improvement Processors (MIP's) and Constrained Improvement Processors (CIP's). MIP's provide a substantial increase in MTI improvement over previous designs, but more satisfactory processors result from applying CIP design procedures. These CIP's emphasize uniformity of processor response and achieve the required value of MTI improvement for desired system performance. The performance of CIP's is compared with previous designs and representative CIP designs are tabulated.

Unstaggered PRF MTI Processors

The unstaggered PRF MTI processors may be considered to be special cases of staggered PRF processors for which the pulse spacing is constant. However, the fact that the pulse spacing is uniform permits simplification of a number of mathematical expressions describing processor performance. This simplification permits development of certain classes of processors for the unstaggered PRF case only, and a significant simplification in the mathematical design procedures for others.

The processors described in this section all were designed using a "structured" approach; that is, a transversal filter form was

assumed, and weights determined which produced the desired filter characteristics. The design criteria which were used emphasize processors which have the required MTI improvement (which is consistent with the quantization limit discussed earlier) and which minimize variations in processor response while processing a fixed number of pulses.

As mentioned earlier, three classes of improved processors for unstaggered PRF systems are discussed in this section. The first are the Equal Ripple Processors, the second are the Maximally Flat Processors, and the third are the Constrained Improvement Processors. There are several properties of the unstaggered processors which are used in the development of all of these processors; they are derived in the following section.

Properties of Unstaggered PRF MTI Processors

The frequency response of the processor is a characteristic of considerable importance. The general form of the processor is given in Figure 6. It follows directly from Figure 6 that h(t), the impulse response of the processor, is given by

$$h(t) = X_1 \delta(t) + X_2 \delta(t-T) + X_3 \delta(t-2T) + \ldots + X_N \delta(t-(N-1)T)$$

$$= \sum_{k=1}^{N} X_k \delta(t-(k-1)T), \qquad (1)$$

where $\delta(t)$ represents a unit impulse, X_N is the weight of the n^{th} sample, and T is the interpulse period, 1/PRF.

To compute the complex frequency response of the network, $H(\omega)$, the Fourier Transform is applied to (1), yielding

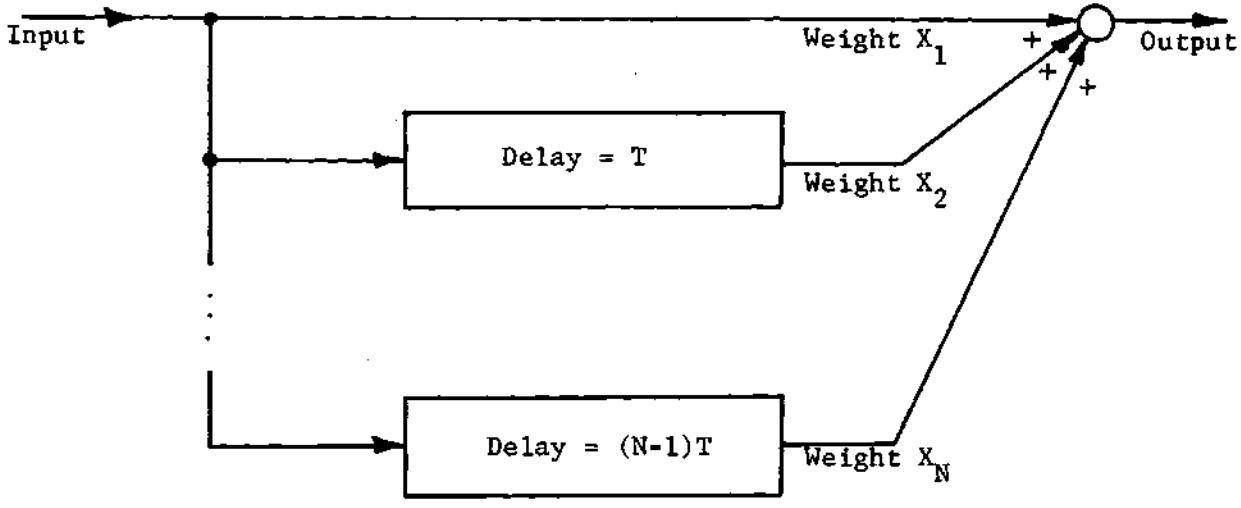


Figure 6. General Form of Unstaggered PRF MTI Processors. T = 1/PRF.

$$H(\omega) = \sum_{k=1}^{N} X_k \, e^{-j\omega T(k-1)} \qquad (2)$$

The power response of the filter, $G(\omega)$, is then

$$G(\omega) = H(\omega)\, H(\omega)^* = C_o + 2 \sum_{q=1}^{N-1} C_q \cos(q\omega T), \qquad (3)$$

where $C_q = \sum_{j=1}^{N-q} X_j \, X^*_{j+q}$, $\qquad 0 \leq q \leq N-1.$

It is appropriate to note that since T = 1/PRF, and since the Doppler frequency is given by $F = \omega/2\pi$, the response may be expressed in terms of f = F/PRF. In the remainder of this thesis, this normalized frequency will be used when discussing frequency response characteristics. It is the combination of the weighting coefficients, the X's, to form the C's which permits the simplifications in the unstaggered PRF expressions.

Another characteristic of unstaggered PRF MTI processors is the MTI improvement, I. As discussed in Chapter II, a Gaussian clutter power spectral density is assumed.

$$C_I = \frac{C}{\sigma_c \sqrt{2\pi}} e^{-F^2/2\sigma_c^2} .$$

The clutter output power is given by C_{out}, where

$$C_{out} = \int_{-\infty}^{\infty} G(F)\, C_I \, dF.$$

Making the substitution $2\pi F = \omega$ in Equation 3, the above relation becomes

$$C_{out} = 2\int_o^\infty (C_o + 2\sum_{q=1}^{N-1} C_q \cos(2\pi\, FqT)) \left(\frac{C}{\sigma_c\sqrt{2\pi}} e^{-F^2/2\sigma_c^2}\right) dF,$$

or

$$C_{out} = \frac{2C}{\sigma_c\sqrt{2\pi}}\left[\int_o^\infty C_o e^{-F^2/2\sigma_c^2}\, dF + 2\sum_{q=1}^{N-1}\int_o^\infty (C_q \cos(2\pi FqT))(e^{-F^2/2\sigma_c^2})\, dF\right],$$

and

$$C_{out} = C\left[C_o + 2\sum_{q=1}^{N-1} C_q\, e^{-2q^2\pi^2T^2\sigma_c^2}\right].$$

The average target output power, $\overline{T}_{out}$, is

$$\overline{T}_{out} = \frac{1}{F_r}\int_o^{F_r} \overline{T}_{in}\, G(F)\, dF$$

$$= \frac{\overline{T}_{in}}{F_r}\int_o^{F_r}\left[C_o + 2\sum_{q=1}^{N-1} C_q \cos 2\pi FqT\right] dF$$

$$= C_o\, \overline{T}_{in}.$$

Then, substituting into the definition of improvement, one obtains

$$I = \frac{C_o}{C_o + 2\sum_{q=1}^{N-1} C_q\, e^{-2q^2\pi^2T^2\sigma_c^2}}. \qquad (4)$$

This expression checks with results obtained by other authors for conventional processors, if the exponentials are expanded in a Taylor series and the first non-zero terms retained. Consider the three-pulse canceller where $C_o = 6$, $C_1 = -4$, $C_2 = 1$. Then

$$\frac{1}{I} = \frac{1}{6}\left[6 - 8\, e^{-2\pi^2 T^2 \sigma_c^2} + 2e^{-8\pi^2 T^2 \sigma_c^2}\right]$$

substituting $e^{\alpha} \approx 1 + \alpha + \frac{\alpha^2}{2}$,

$$I = \frac{f_r^4}{8\pi^4 \sigma_c^4}$$

which agrees with the result given by Nathanson [52], where $f_r = 1/T$.

It is appropriate to note that, from Equation (4), the effects of clutter spectrum width may be expressed as a normalized variable σ,

$$\sigma = \sigma_c T.$$

The use of this form in data presentation permits a large range of PRF and σ_c to be summarized with a few carefully chosen values of σ.

Equal Ripple Processors

A simplex procedure was implemented using a well-known linear programming scheme [53] to design equal ripple MTI processors. The procedure used was to identify a number of frequencies at which the frequency response would be controlled. At each of these frequencies,

minimum and maximum values of frequency response were specified. In addition, a linear objective function (LOF) was defined. For this procedure, C_0 divided by I was chosen as the LOF; since $C_0 \approx 1$ for most practical filters, minimizing the LOF corresponded to maximizing I. The linear programming technique which was used minimized the LOF, subject to the constraint that the frequency response remain within the bounds established earlier.

One substantial problem encountered in designing equal ripple processors was that roundoff error seriously influenced the maximum value of I which could be calculated. Nevertheless, practical filter responses were developed using these techniques. A second difficulty involved the large number of equations that had to be entered into the program. Successful results were obtained for three- and five-pulse processors, but processors for more than five pulses were beyond the scope of this computer program.

This linear programming scheme has been used to design a number of equal ripple processors. Most of the results discussed here will be for five pulse processors. The filter responses for these five pulse processors were specified in 250 Hz intervals from zero to 2500 Hz, and the constraint at zero frequency was that the response be non-negative.

Figure 7 shows three of the Equal Ripple Processor responses developed using the program. The tradeoff between ripple and improvement can be seen clearly. The 3-dB ripple processor has sharper low-frequency cutoff than the 0.8- and 1.8-dB ripple processors, thus

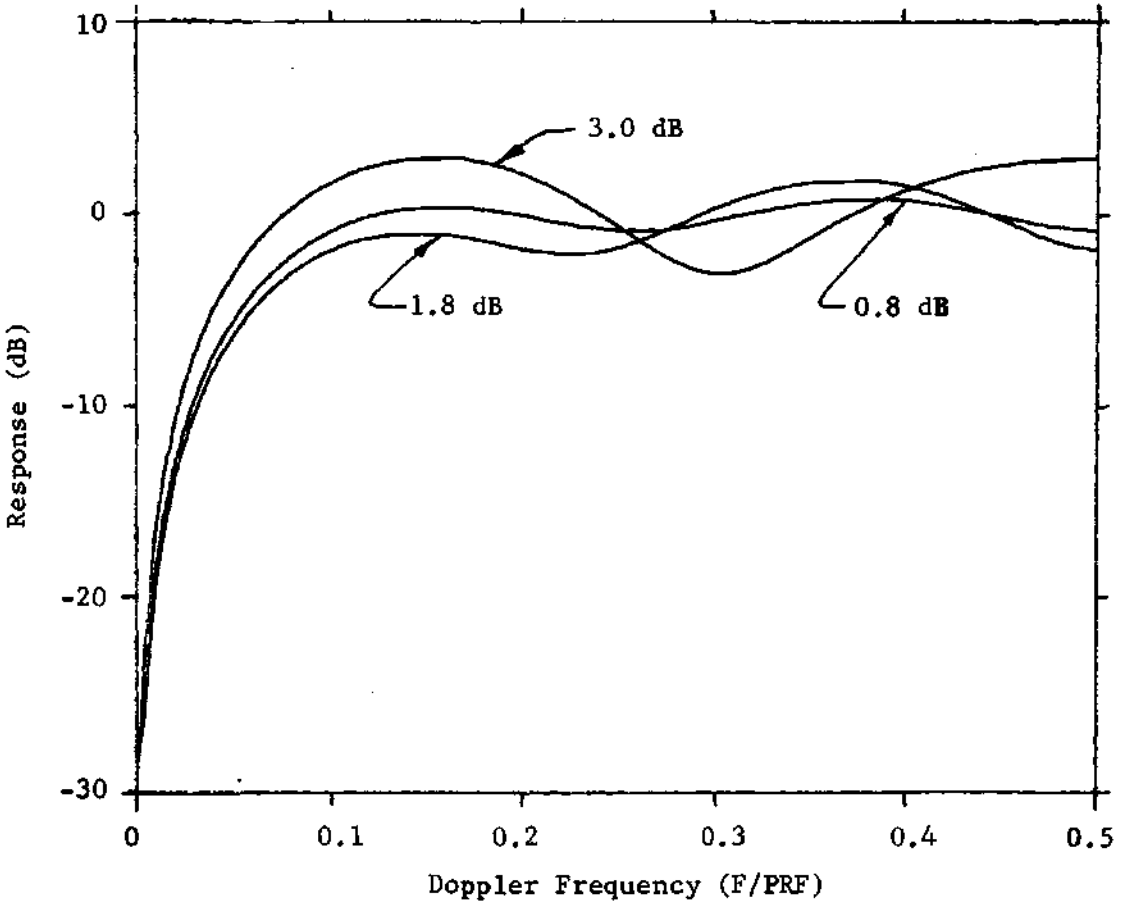


Figure 7. Equal Ripple Processor Responses Developed Using Linear Programming Techniques; 0.8, 1.8, and 3.0 dB Ripple Specification. See Text for Details.

increasing the attenuation for clutter and slowly moving targets. With more available pulses, the cutoff slope could be further increased (thus increasing I) while retaining constant ripple.

The ripple constraint in the pass band can be made so restrictive that the processor provides essentially no improvement, as is seen in Figure 8. When the ripple constraint for this particular filter was changed from 3 dB to 0.8 dB, it failed to provide appreciable attenuation for low frequencies. The minimum specified frequency was 250 Hz.

This relationship between ripple and improvement was investigated for five pulse processors, resulting in the relationship shown in Figure 9. The curves show the ripple vs improvement relationship for 500 Hz and 750 Hz low frequency cutoff processors.

These cases show the relationship which exists between ripple and improvement for some practical processors and give guidelines for processor performance. In all of these Equal Ripple Processors, performance was ultimately limited by the number of pulses available, and processing larger numbers of pulses would have resulted in processors having more desirable performance.

Maximally Flat Processors

In order to develop processors which circumvent some of the difficulties associated with the Equal Ripple Processors, a set of Maximally Flat Processors were developed.

By a "Maximally Flat" processor is meant one having a number of its derivatives with respect to frequency set equal to zero at

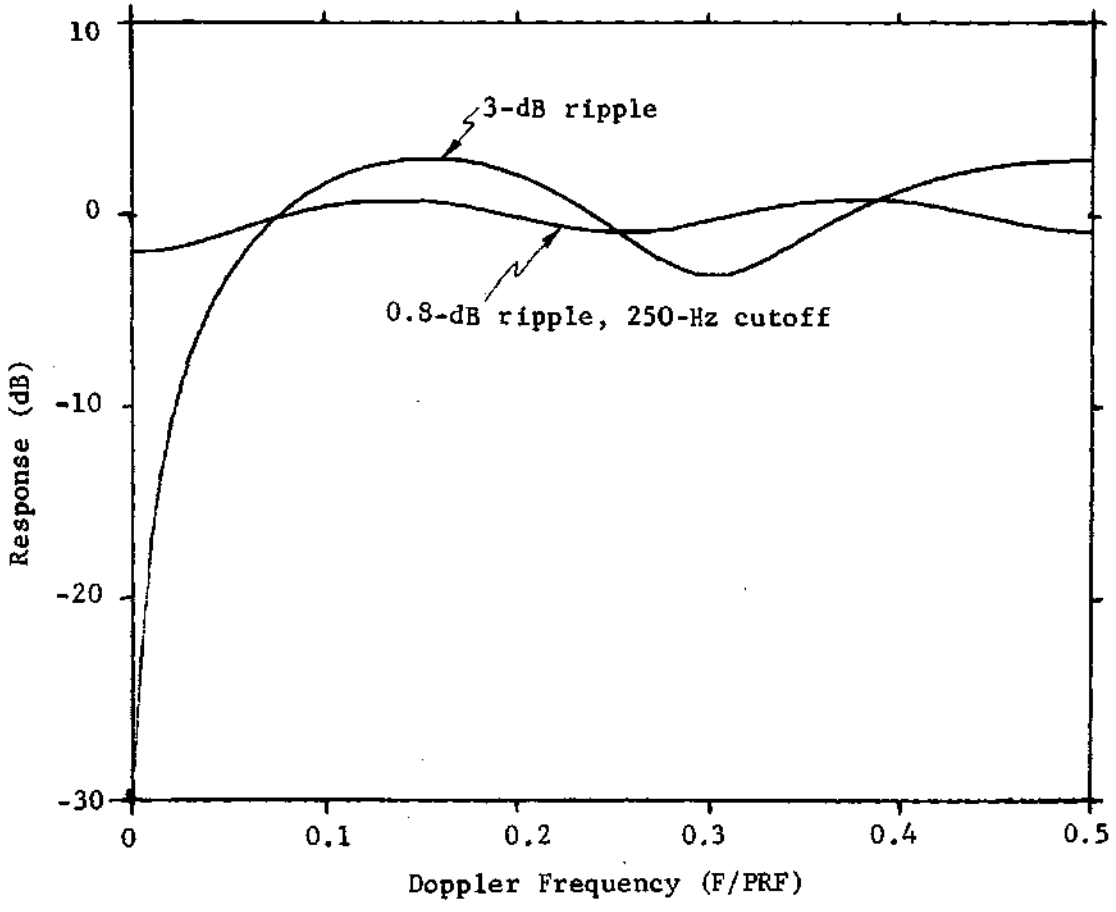


Figure 8. Effects on Equal Ripple Processor Response of too Stringent a Ripple Specification. See Text for Details.

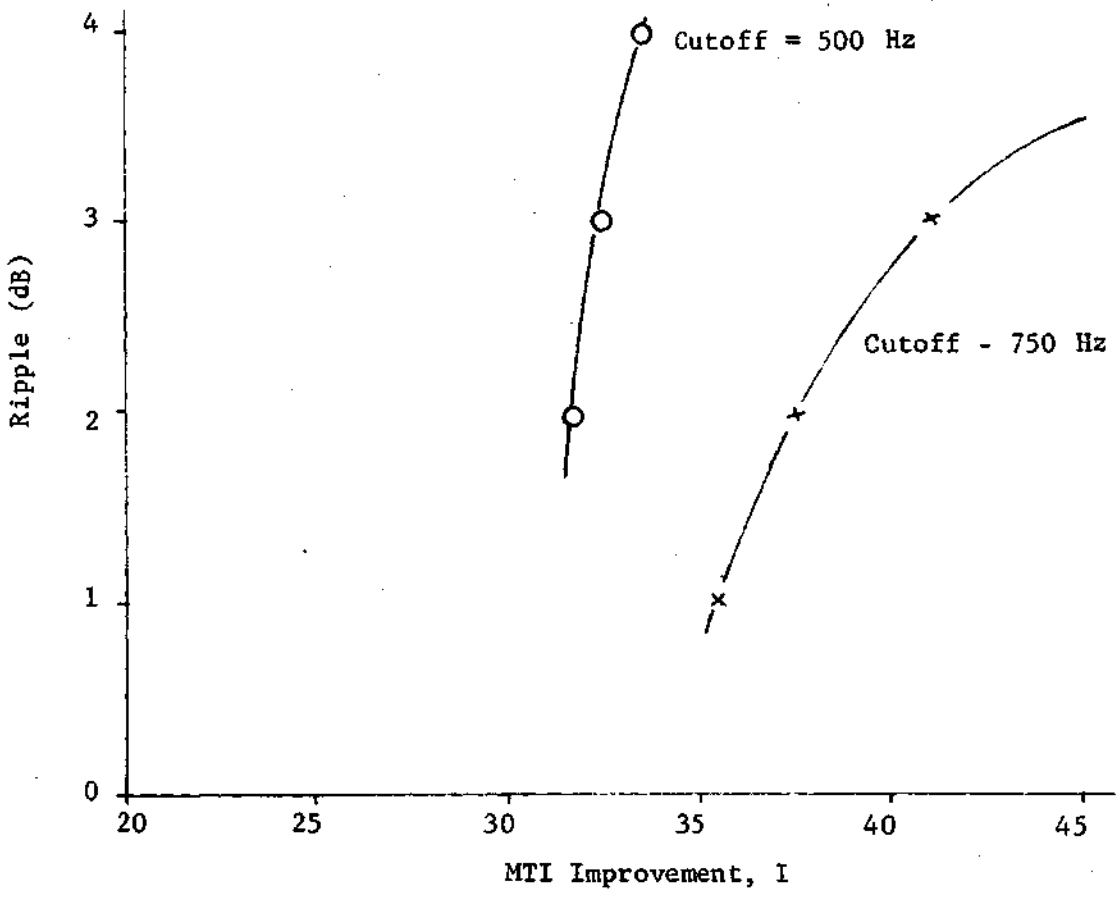


Figure 9. Ripple as a Function of MTI Improvement, I, for Five Pulse Equal Ripple Processors with 500 and 750 Hz Lower Cutoff Frequencies.

some specified frequency or frequencies [54]. For the MTI case, it is also required that these processors have a certain specified amount of MTI improvement. In addition, the filter must have a non-zero amplitude response specified at a given frequency, in order to prevent a solution which is identically equal to zero.

The procedure which was used to derive the Maximally Flat non-recursive digital MTI processors is described below. From Equation (3), the power response of the filter is given by

$$G(\omega) = C_o + 2 \sum_{q=1}^{N-1} C_q \cos q\omega T ,$$

and the MTI improvement, I, is given by

$$I = \frac{C_o}{C_o + 2 \sum_{q=1}^{N-1} C_q \exp (-2q^2\pi^2\sigma^2)} .$$

Following the above discussion, choose a value for $I = 1/\gamma$, and choose $G(\pi F_r) = 1$, where F_r = PRF. Then there are N-2 derivatives which may be set equal to zero. The points at which to set these derivatives equal to zero were chosen to be $\omega = 0$ and/or $\omega = \pi F_r$. The way that these derivatives are apportioned between these two frequencies determines the shape of the filter characteristic.

A three-pulse canceller has only one derivative to set equal to zero; in order to obtain a high-pass filter characteristic this derivative must be zero for $\omega = \pi F_r$. For the three-pulse canceller,

the equations become

$$G(\pi F_r) = 1$$

$$\left.\frac{\partial G(\omega)}{\partial \omega}\right|_{\omega = \pi F_r} = 0$$

$$I = \frac{1}{\gamma} \quad .$$

A four-pulse Maximally Flat Processor has two derivatives which may be set equal to zero. Responses for three and four pulse Maximally Flat Processors are shown in Figure 10, illustrating the improved flatness obtainable over conventional processors.

Constrained Improvement Processors

While the Maximally Flat Processors provide a more uniform response than conventional processors, and require much less computation time than the Equal Ripple Processors, the Maximally Flat Processors do not make an attempt to directly minimize variations in processor response. Therefore, a class of processors, called Constrained Improvement Processors (CIP's), have been developed. The procedure used was to constrain I to be some selected value while minimizing the function

$$\int_{\eta F_r}^{F_r/2} (G(F) - \overline{G(F)})^2 \, dF \quad ,$$

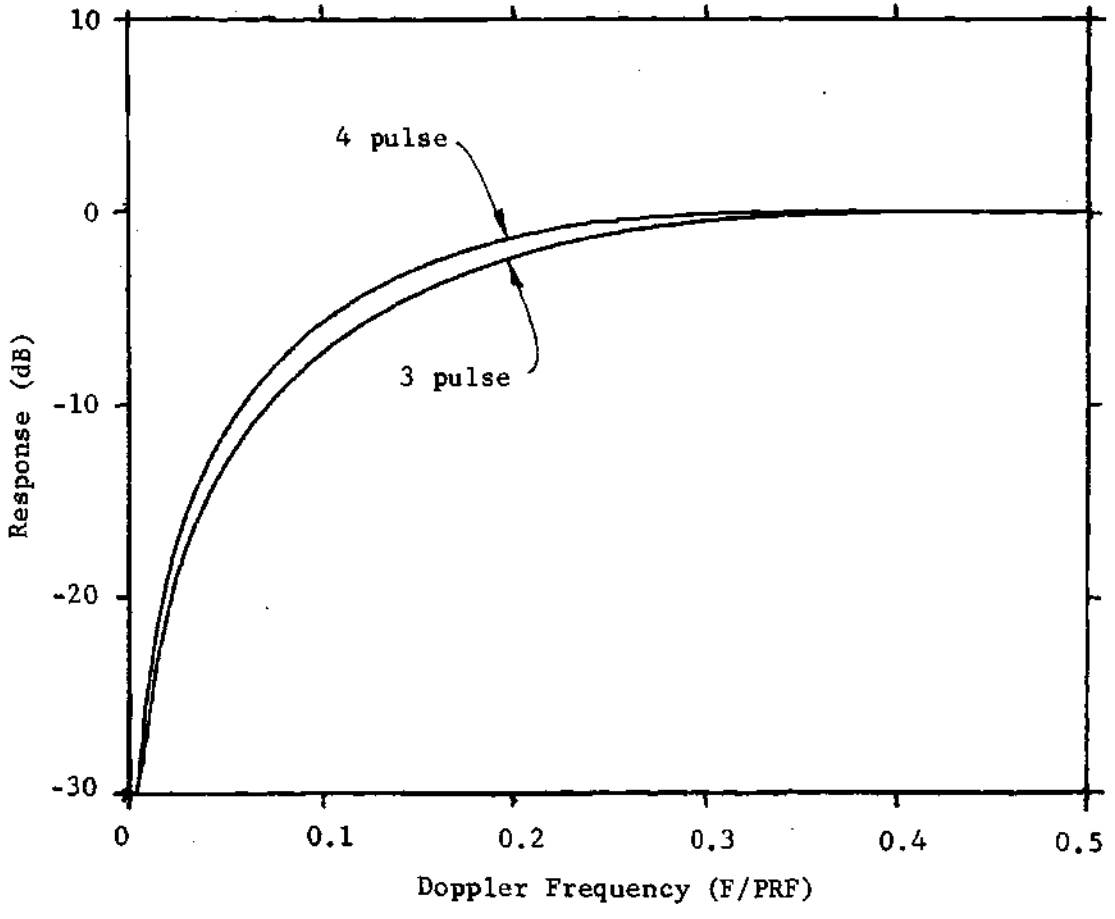


Figure 10. Maximally Flat Processor Responses for Three and Four Pulses Processed.

where

F_r = the pulse repetition frequency,

η = a fraction $0 < \eta < 0.5$,

$G(F)$ = the power response of the filter, and

$\overline{G(F)}$ = average response of the filter.

The choice of η amounts to establishing a pass band of interest, and the value of $\overline{G(F)}$ was chosen equal to one.

This problem is one which may be attacked by Lagrange multiplier techniques. It is worth noting a related analysis has been performed by Martin [55]. Martin evaluated the integrals leading to Equation (4) numerically, and his analysis is a special case of the work which follows for $\eta = 0$.

The error to be minimized over the region ηF_r to $F_r/2$ is the function

$$E = \int_{\eta F_r}^{F_r/2} (G(F) - 1)^2 \, dF,$$

where F_r is the PRF.

Making the substitution $\omega = 2\pi F$ in Equation (3),

$$[G(F) - 1]^2 = [C_o - 1 + 2 \sum_{q=1}^{N-1} C_q \cos(2\pi FqT)]^2$$

$$= (C_o - 1)^2 + 4C_o \sum_{q=1}^{N-1} C_q \cos(2\pi FqT) - 4 \sum_{q=1}^{N-1} C_q \cos(2\pi FqT) +$$

$$4 \sum_{q=1}^{N-1} \sum_{\substack{k=1 \\ k \neq q}}^{N-1} C_q C_k \cos(2\pi FqT) \cos(2\pi FkT).$$

Therefore,

$$E = \int_{\eta F_r}^{F_r/2} [G(F) - 1]^2 \, dF$$

$$= (C_o - 1)^2 (F_r/2)(1 - 2\eta) - 2C_o \sum_{q=1}^{N-1} \sum_{\substack{k=1 \\ k \neq q}}^{N-1} C_q C_k F_r \alpha_{qk} ,$$

where

$$\alpha_{qk} = \begin{cases} -\frac{\sin 2\pi\eta(q-k)}{4\pi(q-k)} - \frac{\sin 2\pi\eta(q+k)}{4\pi(q+k)} & q \neq k \\ \frac{1}{4}\left[1 - 2\eta - \frac{\sin 4\pi q\eta}{2q\pi}\right] & q = k \end{cases}$$

Next, using standard Langrange multiplier techniques, minimize

$$P = E + \lambda \left(\frac{1}{I} - \gamma\right) F_r C_o ,$$

subject to the constraint that

$$\frac{1}{I} = \text{constant} = \gamma .$$

In these expressions, λ is the Lagrange multiplier. This is done by solving the system of equations

$$\frac{\partial P}{\partial C_o} = 0$$

$$\vdots$$

$$\frac{\partial P}{\partial C_{N-1}} = 0$$

$$\left(\frac{1}{I} - \gamma\right) = 0 \ .$$

Noting that $\alpha_{qk} = \alpha_{kq}$, these expressions are somewhat simplified; for a three-pulse processor, they become

$$C_o(1 - 2\eta) - 2C_1 \frac{\sin 2\pi\eta}{\pi} - 2C_2 \frac{\sin 4\pi\eta}{\pi} + \lambda(1 - \gamma) = 1 - 2\eta$$

$$-2C_o \frac{\sin 4\pi\eta}{\pi} + C_1 8\alpha_{11} + C_2 8\alpha_{22} + \lambda\left(2e^{-8\pi^2 T^2 \sigma_c^2}\right) = -2 \frac{\sin 4\pi\eta}{2\pi}$$

$$(1 - \gamma) C_o + C_1 2e^{-2\pi^2 T^2 \sigma_c^2} + C_2 2e^{-8\pi^2 T^2 \sigma_c^2} = 0 \ .$$

The system of equations readily expands for larger numbers of received pulses. A computer program was written to solve for the C's for an arbitrary number of pulses.

Responses for a conventional three-pulse MTI processor and a CIP designed for I = 60 dB is shown in Figure 11. The improvement in detectability for targets having low-frequency Doppler returns is evident.

The ideal response of any of these processors would be a constant, independent of frequency. The requirement that the processor

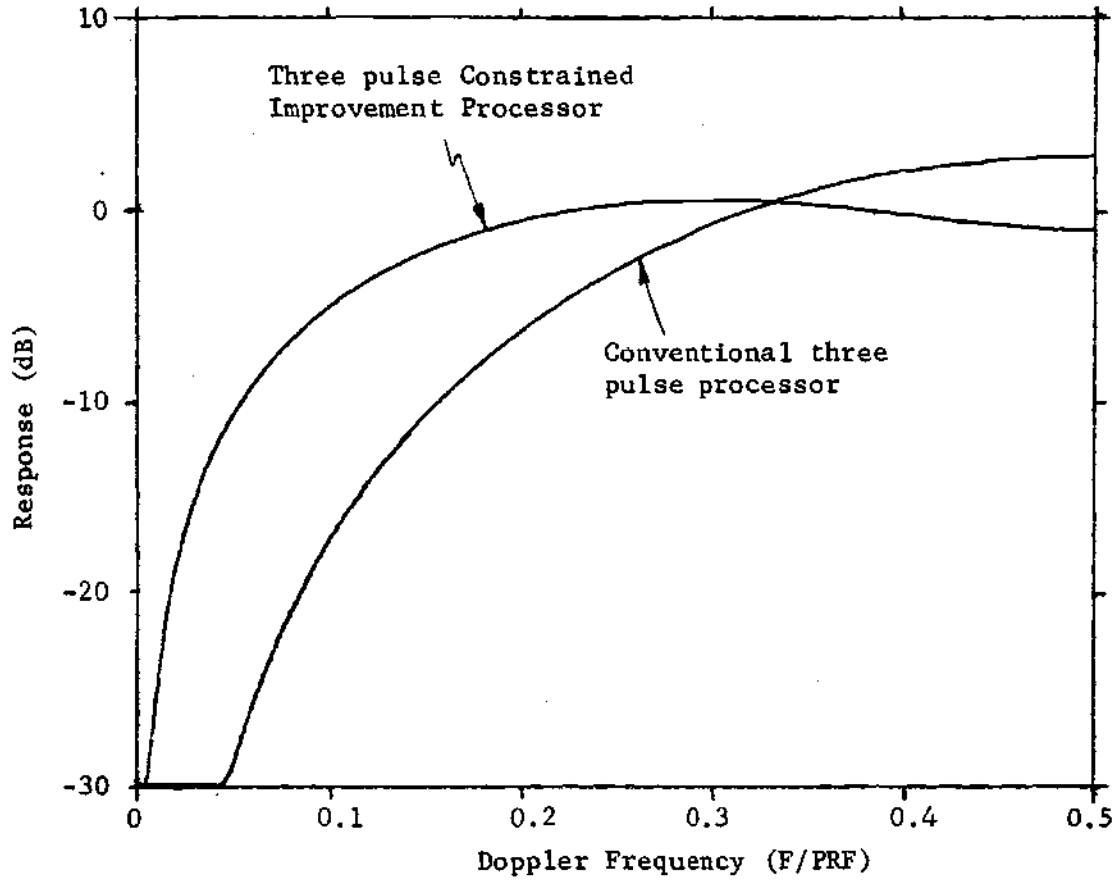


Figure 11. Comparison of the Responses of a Conventional Three Pulse Processor and a Constrained Improvement Processor Designed for I = 60 dB and $\eta = 0.1$.

have a degree of MTI improvement requires the response be reduced over the frequency range of the clutter spectrum, thus preventing this ideal response from being attained. In order to make meaningful comparisons of the non-uniform responses of the various processors, some measures of uniformity of response are desirable. One measure is to make a direct comparison of the shapes of the responses for processors under consideration, but this approach generally requires considerable effort, particularly for processors which have complex frequency responses. Since one objective of the design procedures is to increase the fraction of the frequencies of interest for which responses stay within certain bounds, it is appropriate to use the fraction of frequencies for which the response stays within some small range of values as a measure of uniformity. In particular, if this information is graphically displayed with the fraction of frequencies for which the response stays within some small interval as the abscissa, and with the response as the ordinate, the way in which the response is distributed over its range of values is illustrated. The ideal constant response would be represented by an impulse at the value of processor response; deviations from constant response are shown by a spreading or redistribution of the response over the range of its excursion. Since this presentation bears some similarity to the familiar probability density function, in the rest of this thesis it will be referred to as the probability density function of response, and the ordinate will be labeled as probability.

The fraction of frequencies for which the response is less than

some specified value is another suitable measure to determine the uniformity of processor response. In particular, if the relationship between response and the fraction of frequencies for which the return is less than the specified response is presented graphically, with the response as the abscissa and the fraction of frequencies as the ordinate, a particularly useful presentation is obtained. If a uniform response were obtained with a value of 0 dB, this presentation would be a step function at 0 dB; deviations from ideal behavior are indicated by a "tilting" or "smearing" of this ideal step (see Figures 13 and 15, for example). For these non-uniform responses, reduction of the fraction of frequencies for which the response lies below any value less than 0 dB would be a desirable feature. This form of presentation bears some similarity to the more familiar cumulative probability distribution; such presentations will be referred to as cumulative distributions of response, and the ordinate will be labeled as probability.

These two measures have more than an incidental similarity to more familiar measures from probability theory. If the input to the processor were single frequency sinusoids whose frequency was a random variable having a uniform probability density over the frequencies of interest, then the two measures would represent the probability density function of response, and the cumulative probability distribution of response, respectively. This is an additional reason for referring to these two measures as the cumulative distribution of response and the probability density function of response. Rather

than calculate these functions in continuous form, they will be approximated in the form of histograms.

Figure 12 shows the probability density and Figure 13 the cumulative probability of the response for a conventional three pulse processor. Figures 14 and 15 show the same measures for a CIP three pulse MTI processor.

The utility of the use of cumulative probabilities and probability densities of response as a means of comparing uniformity of processor response is clearly shown by a careful consideration of Figures 11 through 15. Figure 11 clearly shows the additional uniformity obtained with a constrained improvement processor over a conventional processor. Comparison of the probability density functions of response for these same processors (Figures 12 and 14) clearly shows the increased uniformity obtained with the constrained improvement processor, providing approximately a three-to-one increase in occurrence of responses close to unity, with a substantial reduction in occurrence of responses near zero. Comparison of the cumulative distributions of response given in Figures 13 and 15 again illustrate both the superiority of constrained improvement processors and the utility of the cumulative distribution of response as a means of comparing processor responses. The fact that the curve in Figure 15 more closely approaches the ideal step function indicates the desirability of the constrained improvement processor over conventional designs. For example, from Figures 13 and 15, use of a constrained improvement processor results in a reduction of approximately three-to-one in the fraction of

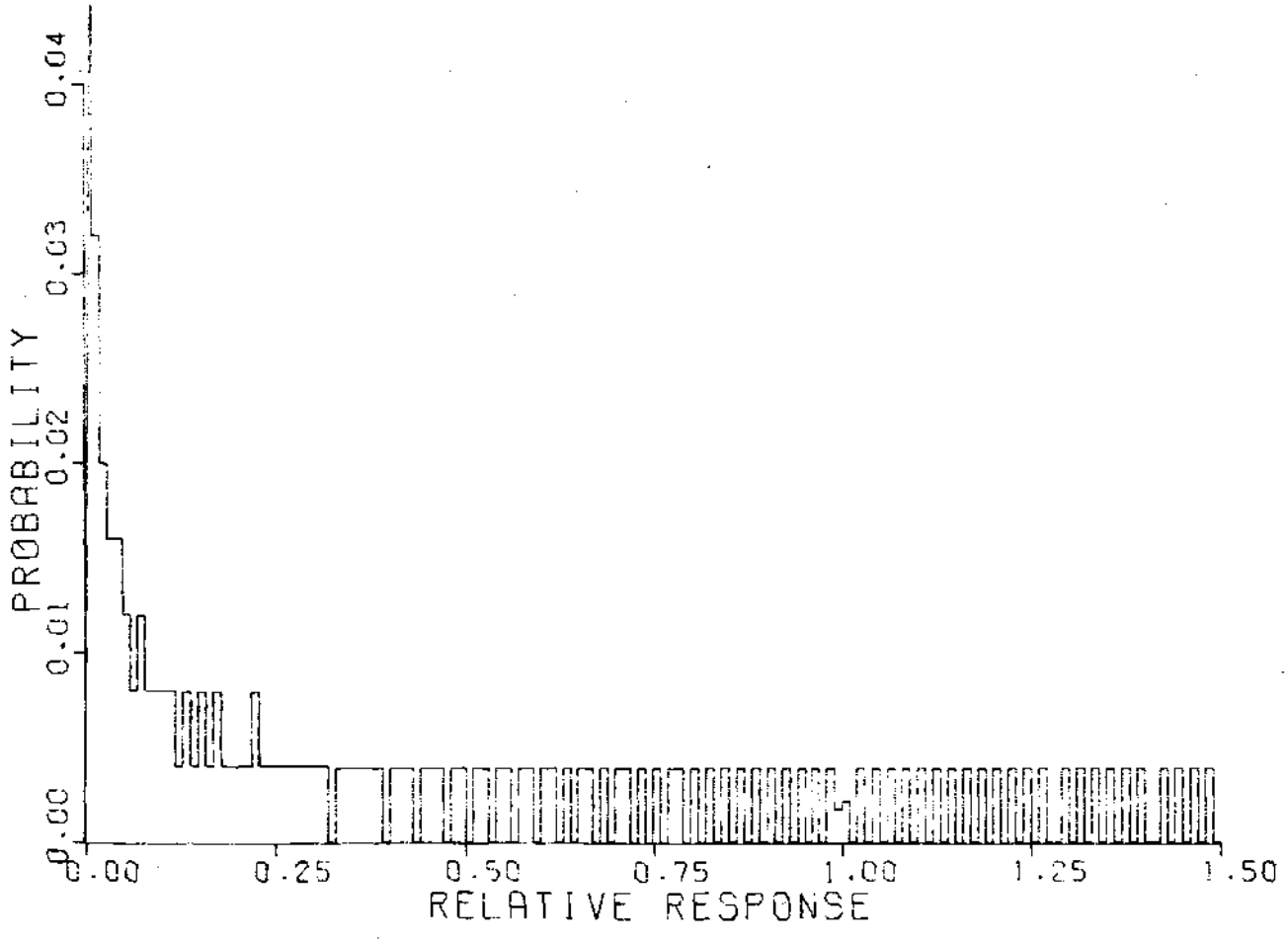


Figure 12. Probability Density Function of Response for Conventional Three Pulse Processor.

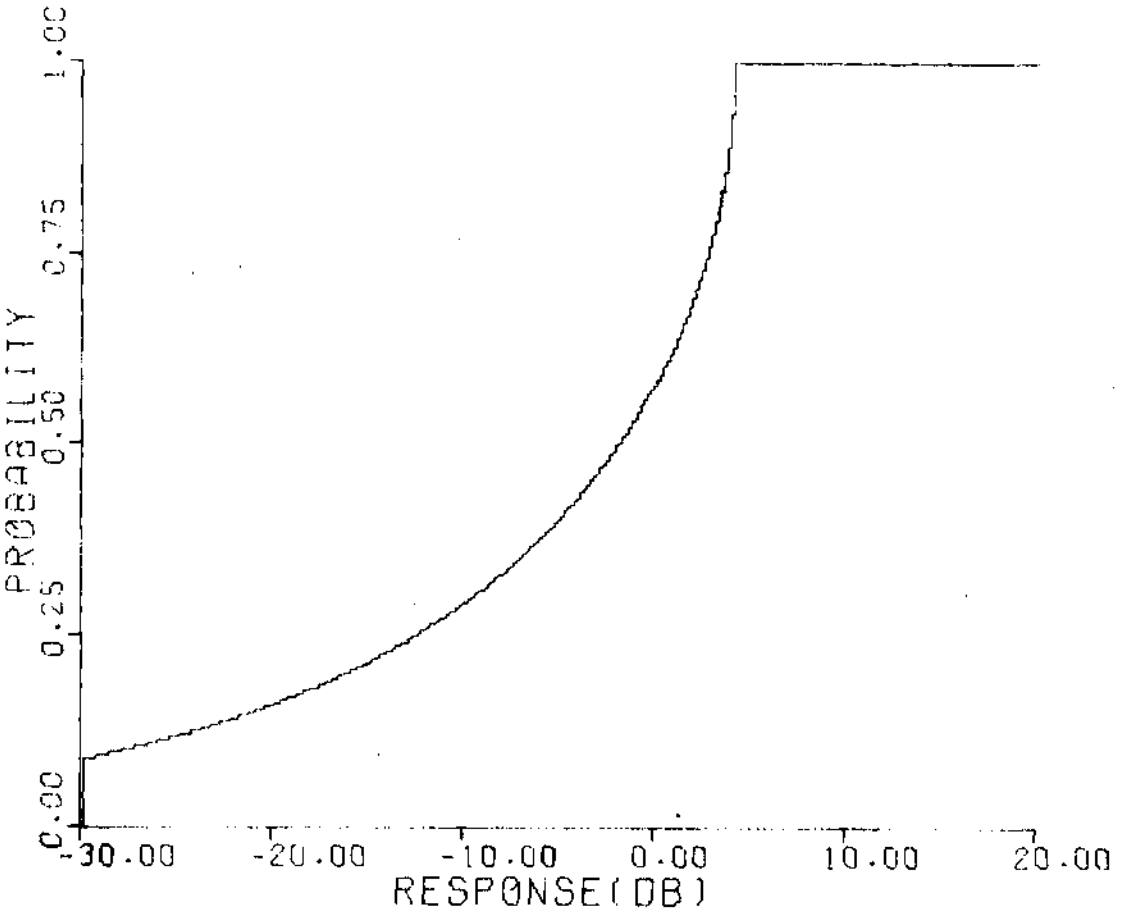


Figure 13. Cumulative Distribution of Response for Conventional Three Pulse Processor.

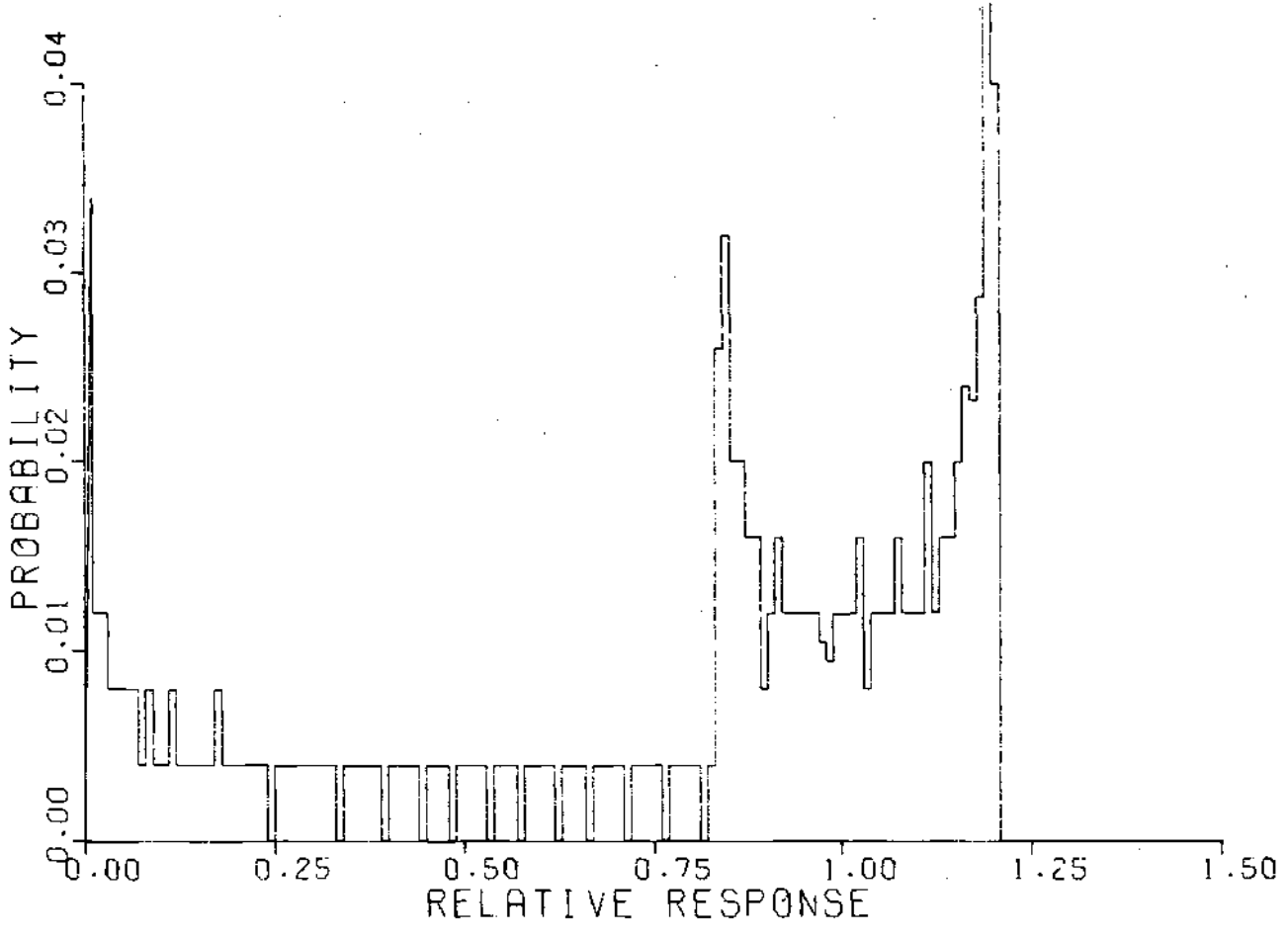


Figure 14. Probability Density Function of Response for a Three Pulse Constrained Improvement Processor.

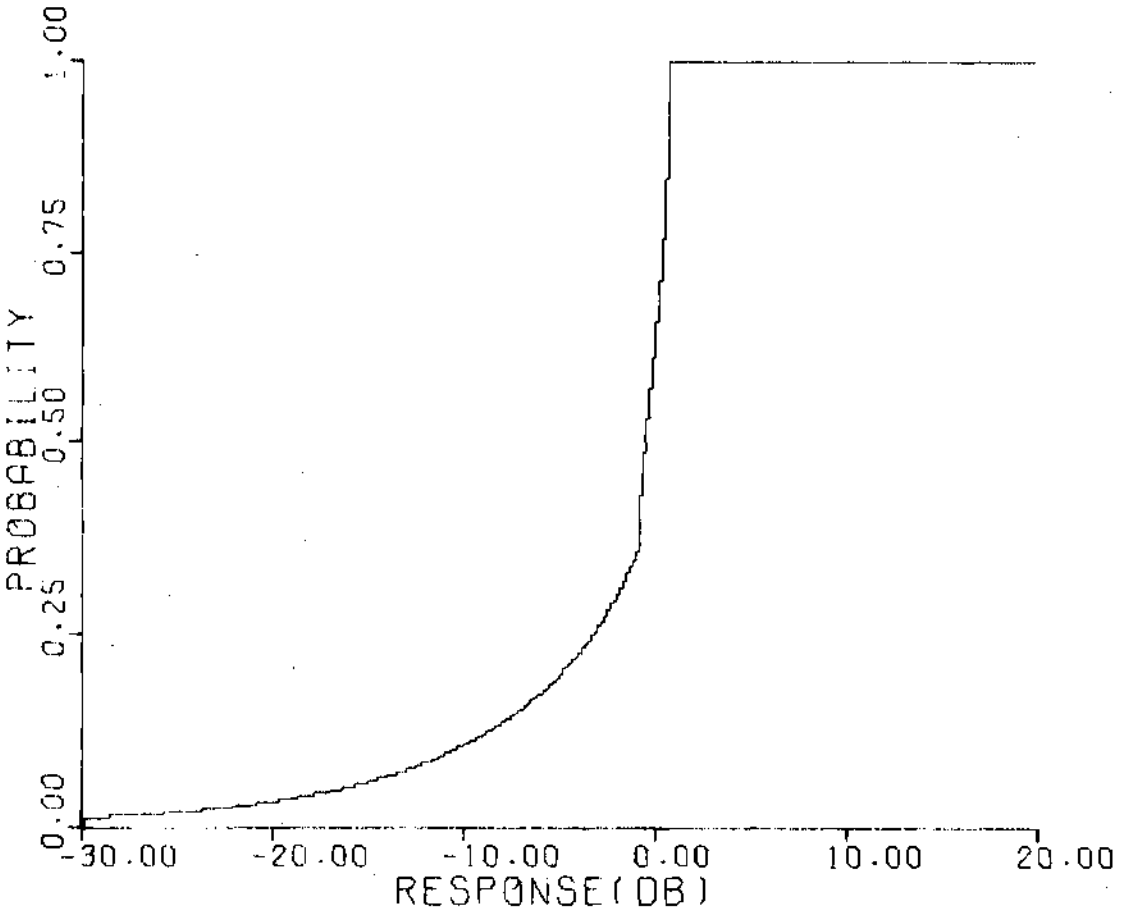


Figure 15. Cumulative Distribution of Response for a Three Pulse Constrained Improvement Processor.

frequencies for which the response is less than -10 dB, certainly a most desirable feature.

Thus, not only does the constrained improvement processor provide a more uniform response as a function of frequency than conventional processors, but the probability density function of response and the cumulative distribution of response clearly point out this increased uniformity. While not absolutely essential for these relatively simple response shapes, these measures will be extremely useful when comparing the more complex responses obtained with staggered PRF processors.

The shape of the CIP response for a Constrained Improvement Processor is a function of the exact value of I specified; Figure 16 gives results for I = 10 dB, 30 dB, and 60 dB, showing the increased ripple associated with larger values of I. This illustrates the desirability of choosing I no greater than necessary because of the consequent compromises in processor response.

The flatness of the response increases as the number of pulses processed increases, but the number of ripples also increases. This is illustrated in Figure 17 which shows responses for I = 60 dB for three, five, and seven pulses processed.

Differences in responses for $\eta = 0$ and $\eta = 0.1$ are not particularly great, but the case $\eta = 0.1$ does show a slight improvement in flatness of response. Figure 18 compares results for a five-pulse CIP with I = 60 dB for $\eta = 0$ and $\eta = 0.1$.

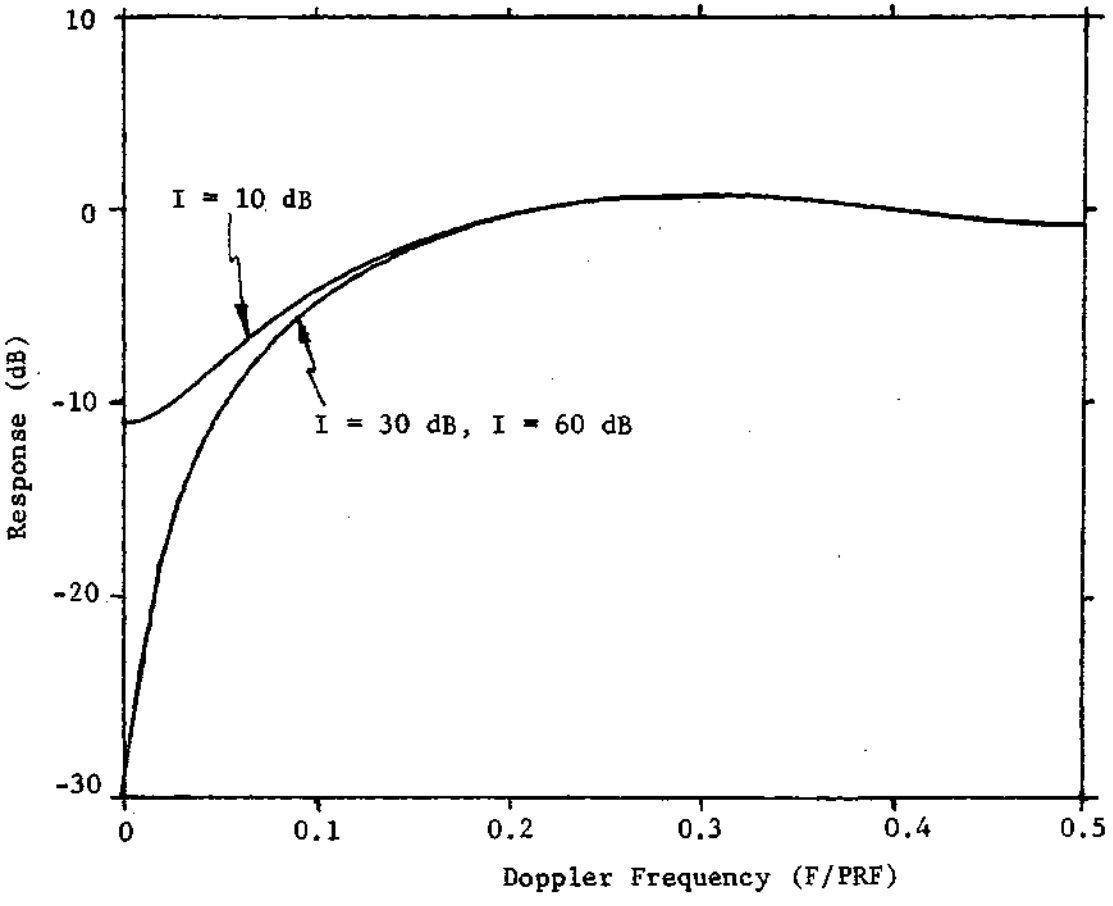


Figure 16. Responses of Constrained Improvement Processors Designed for η = 0.1 and I = 10, 30, and 60 dB.

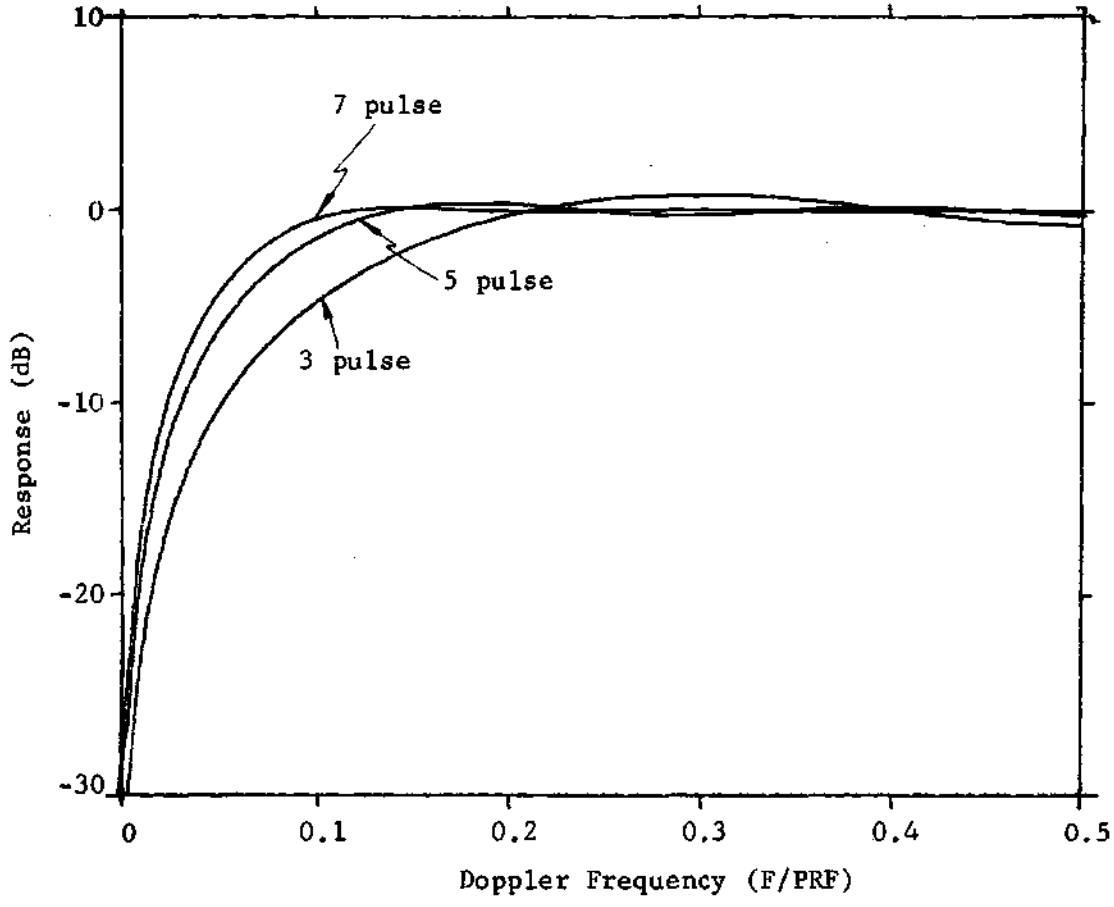


Figure 17. Constrained Improvement Processor Responses for Three, Five and Seven Pulses Processed. I = 60 dB, η = 0.1.

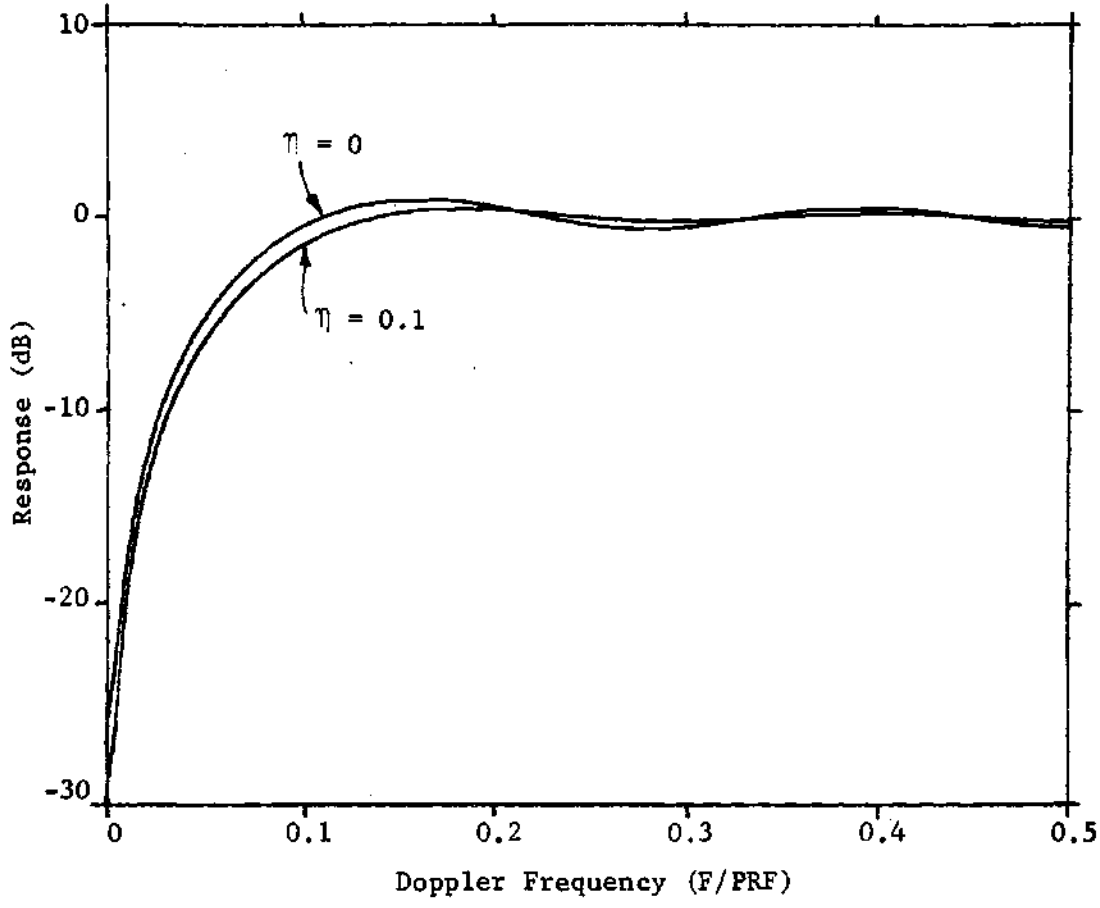


Figure 18. Comparison of Responses of Five Pulse Constrained Improvement Processors for $\eta = 0$ and $\eta = 0.1$.

Blind Speeds

The improved processors designed up to this point, while providing more uniform detectability than conventional processors, still exhibit blind speeds. This is a characteristic of any unstaggered PRF system which operates at a single frequency. Figure 19 shows the response of a conventional four pulse processor for an unstaggered PRF system.

If the requirements on the radar system are such that Doppler frequencies higher than the system PRF are anticipated, some means of reducing or eliminating these blind speeds is required. Two methods of reducing these blind speeds are the use of frequency agility and staggered PRF.

The effects of frequency agility on blind speeds have been analyzed by Ewell [6], and, in addition to requiring a large number of pulses be processed, frequency agility is only effective in eliminating the higher blind speeds.

The other commonly used method for eliminating these blind speeds is to "stagger" the PRF (vary the inter-pulse spacing). Figure 20 shows the effects on the frequency response of a conventional processor of changing the interpulse period by a fraction, ϵ. As one can see, this approach does eliminate the first blind speed. Figure 21 shows the effect of PRF stagger on the response of the three pulse Constrained Improvement Processor developed earlier. This would lead one to believe that these improved processors are no longer optimum when they are used in a staggered PRF system. In fact,

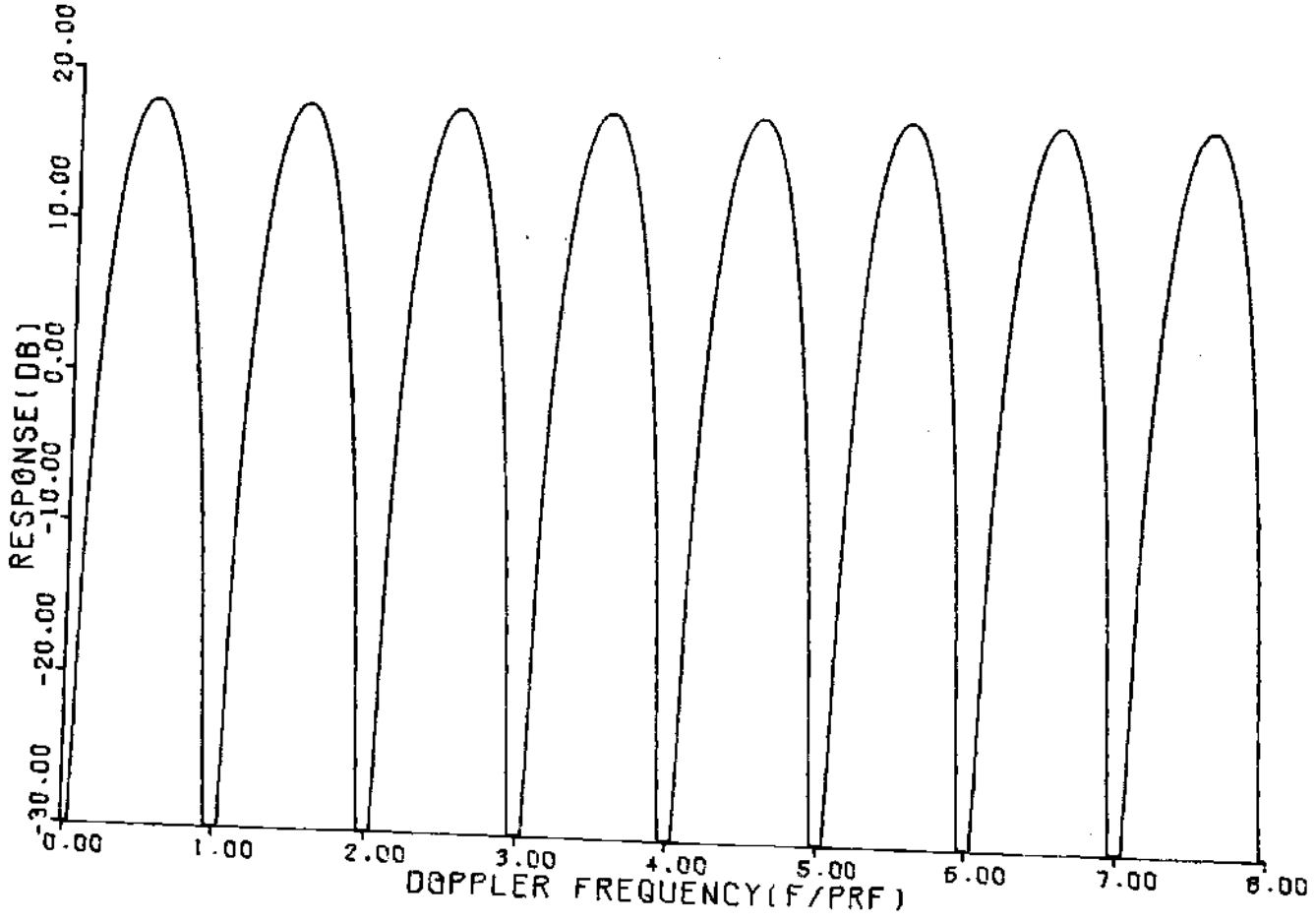


Figure 19. Response of Conventional Four Pulse MTI Processor without PRF Stagger.

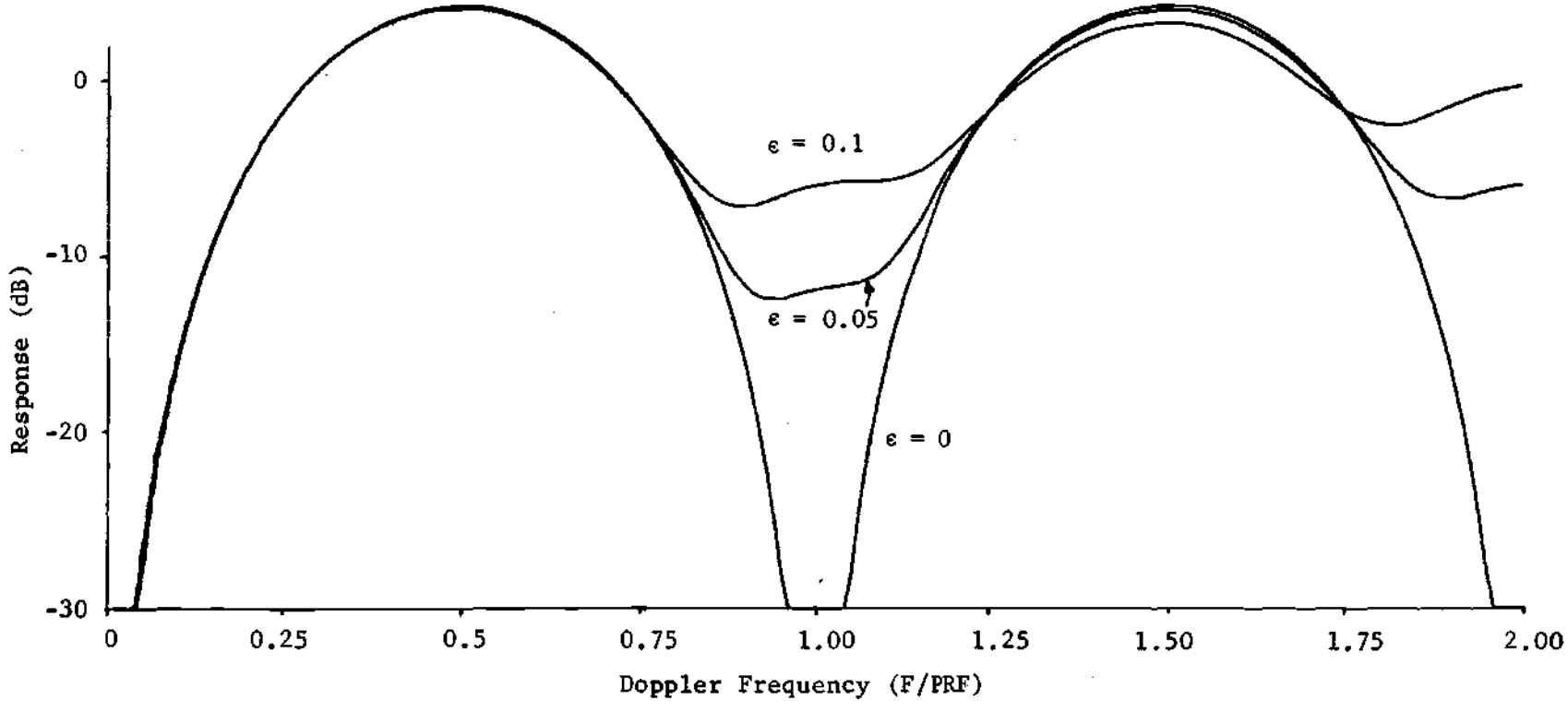


Figure 20. Responses of a Conventional Three Pulse MTI Processor when Various Values of Stagger, ε, are Used.

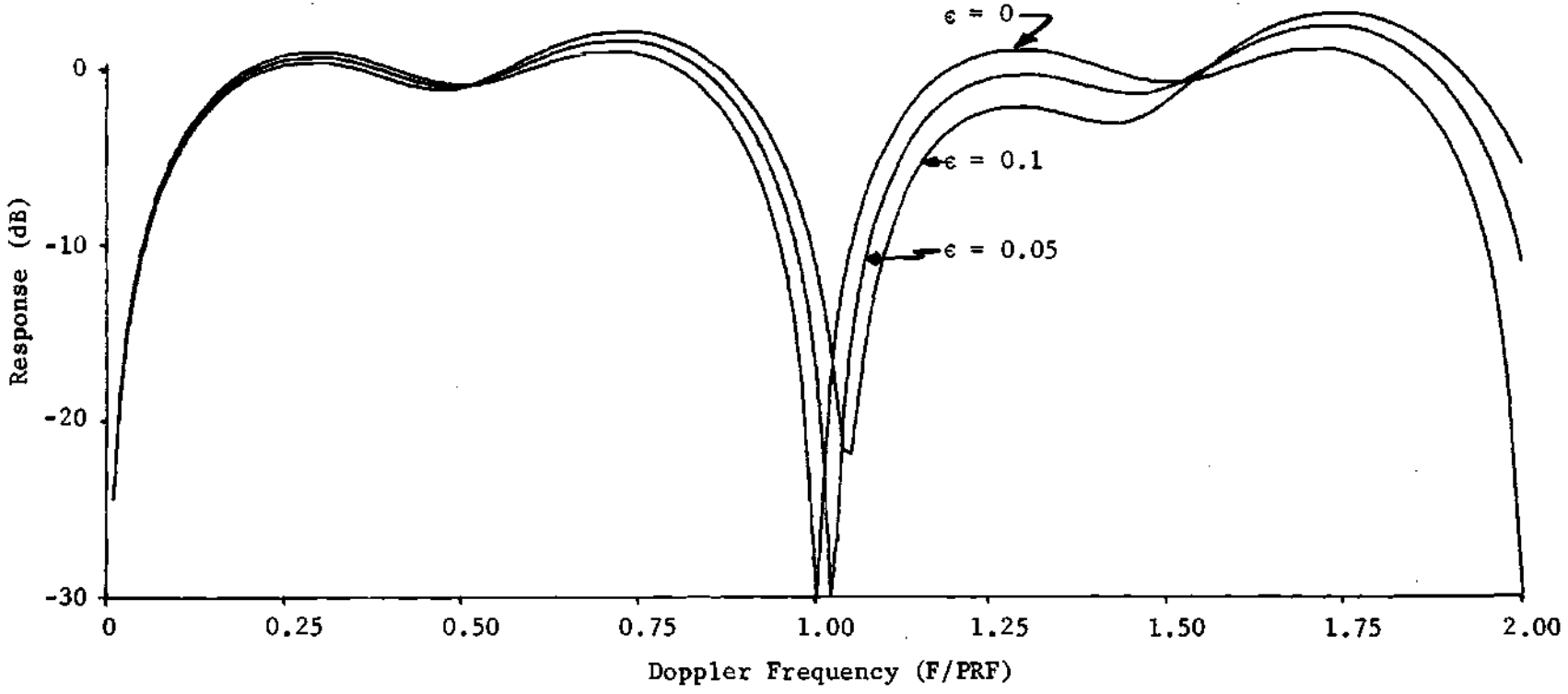


Figure 21. Response of a Constrained Improvement Processor for an Unstaggered System when Used with Various Amounts of PRF Stagger, ε.

the response might be considered inferior to the conventional case, illustrating the need for specialized design procedures for staggered PRF systems.

Staggered PRF MTI Processors

The design of staggered PRF MTI processors is somewhat more complicated than the unstaggered PRF case described in the preceding sections. The mathematical simplifications which were possible for the unstaggered PRF case no longer are possible for the staggered PRF case; in fact, a number of the resulting equations are nonlinear. The second difficulty is that there is an additional set of parameters, the pulse spacings, to be optimized. The pulse spacings must be controlled to fall within certain limits; if the interpulse spacings become too small, either the unambiguous range requirement of the system will be violated, or the transmitter duty cycle limits will be exceeded.

In spite of these additional difficulties, two general classes of improved structured MTI processors have been developed during the course of this research: the first are called Maximum Improvement Processors (MIP's), and the second are called Constrained Improvement Processors (CIP's).

The design procedure for MIP's involves maximizing the MTI improvement, I, while keeping the average response equal to one. The method of solution involves the use of Lagrange multiplier techniques and the Fletcher-Powell method to solve the resulting sets of simultaneous nonlinear equations in order to determine the required filter weights for a specified PRF stagger sequence.

The CIP's are designed by specifying a desired value of MTI improvement, I, and selection of processor weights and/or PRF stagger sequences which minimize the mean square deviation of processor response from a constant. Again, the procedure involves use of Lagrange multiplier techniques and the Fletcher-Powell method to solve the resulting sets of simultaneous nonlinear equations.

Since a number of general properties of staggered PRF MTI processors are used in development of both classes of processors, they will be discussed in the next section, followed by a discussion of MIP's, and the chapter concludes with the treatment of the CIP's.

Properties of Staggered PRF MTI Processors

The structured processor format which is being considered is illustrated in Figure 22, which shows the i^{th} pulse displaced from its unstaggered position by an amount ΔT_i. The general form of the MTI processor is also shown in Figure 22, illustrating the delays $(i-1)T+\Delta T_i$ of the i^{th} pulse, which is weighted by an amount X_i.

It follows directly from Figure 22 that h(t), the impulse response of the processor, is given by

$$h(t) = X_1\,\delta(t-\Delta T_1) + X_2\,\delta(t-(T+\Delta T_2)) + \ldots + X_N\,\delta(t-((N-1)T+\Delta T_N)).$$

The frequency response of this processor, H(ω), is given by

$$H(\omega) = X_1 e^{-j\omega(\Delta T_1)} + X_2 e^{-j\omega(T+\Delta T_2)} + \ldots + X_N e^{-j\omega((N-1)T+\Delta T_N)}$$

$$= \sum_{i=1}^{N} X_i e^{-j\omega((i-1)T+\Delta T_i)}.$$

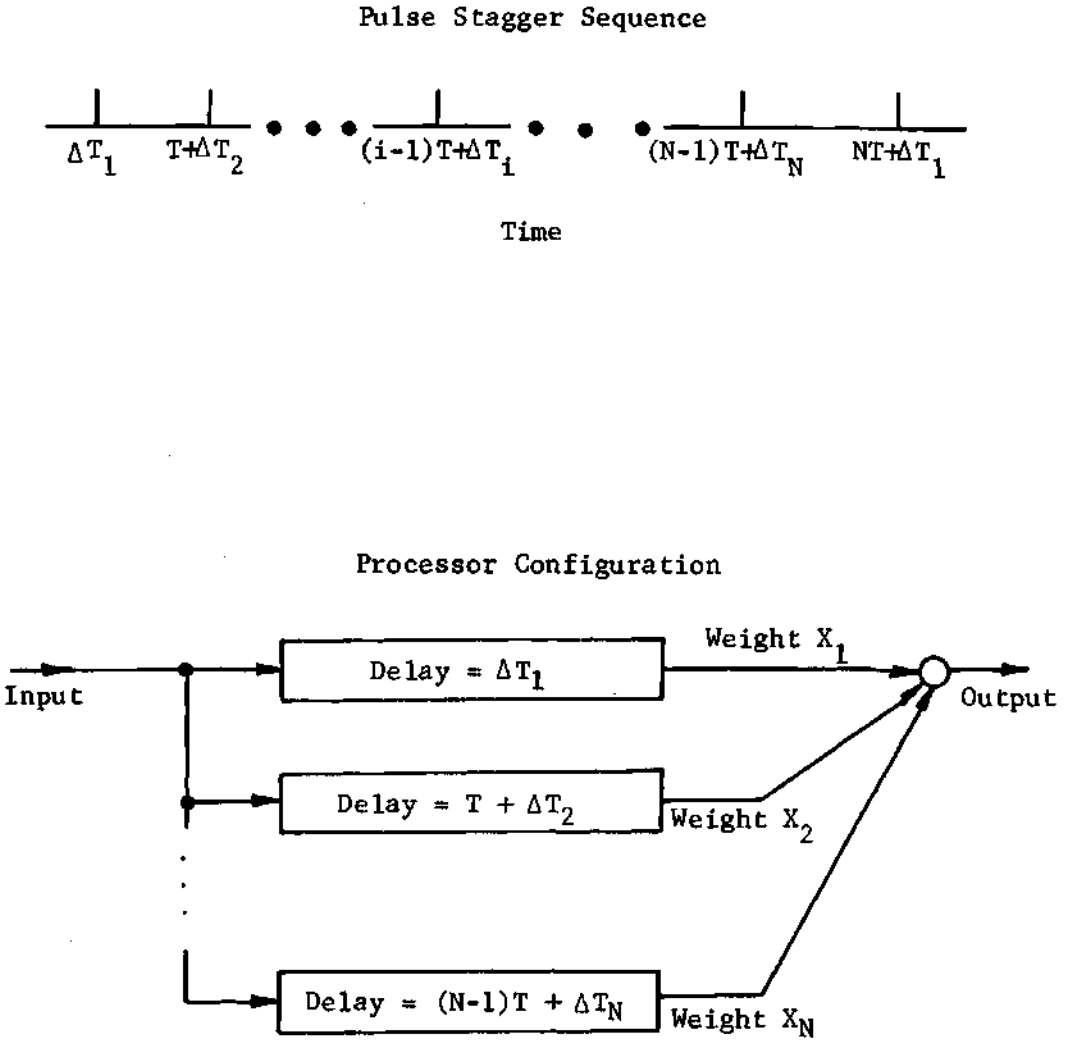


Figure 22. Pulse Stagger Sequence and Processor Configuration for Staggered PRF Processors.

The power response of the processor, $G(\omega)$, is given by

$$G(\omega) = H(\omega) \cdot H(\omega)^{*} \quad ,$$

where * denotes complex conjugate. Substituting,

$$G(\omega) = \left[\sum_{i=1}^{N} X_i e^{-j\omega((i-1)T+\Delta T_i)}\right] \cdot \left[\sum_{i=1}^{N} X_i e^{j\omega((i-1)T+\Delta T_i)}\right]$$

$$= \sum_{i=1}^{N} \sum_{j=1}^{N} X_i X_j \cos[\omega((i-j)T+\Delta T_i - \Delta T_j)] \quad .$$

It is possible to simplify this notation somewhat by noting $\omega = 2\pi F$, where F is the Doppler frequency, and that $T = 1/PRF$. Dividing the argument of the cosine by T, one obtains

$$G(F) = \sum_{i=1}^{N}\sum_{j=1}^{N} X_i X_j \cos\left[\frac{2\pi F}{PRF}\left((i-j) + \frac{\Delta T_i}{T} - \frac{\Delta T_j}{T}\right)\right].$$

Making the substitution

$$f = F/PRF$$

$$\Delta(i) = \Delta T_i/T$$

$$\Delta(j) = \Delta T_j/T,$$

G(f) may be expressed as

$$G(f) = \sum_{i=1}^{N}\sum_{j=1}^{N} X_i X_j \cos[2\pi f((i-j)+\Delta(i) - \Delta(j))]. \qquad (5)$$

Due to the fact that the cosine is an even function, Equation (5) may be rewritten as

$$G(f) = \sum_{i=1}^{N} X_i^2 + \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} 2X_i X_{i+k} \cos(2\pi f(k-\Delta(i) + \Delta(i+k))). \qquad (6)$$

While Equations (5) and (6) are numerically equivalent, Equation (6) requires approximately one-half the computation time required by Equation (5) to evaluate G(f) for a given set of parameters.

The average value of G(f), $\overline{G(f)}$, assuming the averaging is performed over a frequency interval much greater than the PRF, is given by

$$\overline{G(f)} = \sum_{i=1}^{N} X_i^2 \ . \qquad (7)$$

The MTI improvement, I, for the staggered PRF case is derived in a manner similar to the unstaggered case discussed earlier. A Gaussian clutter spectrum is assumed,

$$C_I = \frac{C}{\sigma\sqrt{2\pi}} e^{-f^2/2\sigma^2}$$

where $f = F/PRF$ and $\sigma = \sigma_c T$.

The clutter output power is given by C_{out}, where

$$C_{out} = \int_{-\infty}^{\infty} G(f)\, C_I \, df$$

or

$$C_{out} = 2\int_{0}^{\infty} \left(\sum_{i=1}^{N} X_i^2 + \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} 2X_i X_{i+k} \cos(2\pi f(k-\Delta(i)+\Delta(i+k))) \right) \cdot \left(\frac{C}{\sigma\sqrt{2\pi}} e^{-f^2/2\sigma^2} \right) df \ ,$$

thus,

$$C_{out} = C\left[\sum_{i=1}^{N} X_i^2 + 2 \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} X_i X_{i+k} e^{-2\pi^2\sigma^2(k-\Delta(i) + \Delta(i+k))^2} \right] . \quad (8)$$

The average target output power, $\overline{T}_{out}$, is

$$\overline{T}_{out} = \frac{1}{f'} \int_o^{f'} \overline{T}_{in} G(f) \, df,$$

where f' is the highest Doppler frequency of interest. Assuming $f' \gg 1$,

$$\overline{T}_{out} = \overline{T}_{in} \sum_{i=1}^{N} X_i^2 . \quad (9)$$

Then directly from the definition of MTI improvement, I, by the use of Equations (8) and (9),

$$I = \frac{\sum_{i=1}^{N} X_i^2}{\sum_{i=1}^{N} X_i^2 + 2 \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} X_i X_{i+k} e^{-2\pi^2\sigma^2(k-\Delta(i) + \Delta(i+k))^2}} . \quad (10)$$

These expressions will be used in the MTI processor designs outlined in the following sections.

Maximum Improvement Processors

As noted earlier, Maximum Improvement Processors (MIP's) are those which maximize I while keeping $\overline{G(f)}$ equal to a constant. Using properties of staggered PRF processors developed in the preceding section, the MIP design methods are set forth, and results verified, in

the next section. Then the design methods are used to specify some MIP's and results compared with those of earlier designs. A brief discussion showing how results of this comparison form part of the motivation for the design procedures for the CIP's (which are the other class of staggered PRF processors discussed in this chapter) concludes the discussion of MIP's.

MIP Design Methods. The design procedure which was used was to minimize 1/I while keeping $\overline{G(f)} = 1$. One approach was to directly minimize the function

$$\varphi = \frac{1}{I} + (1 - \overline{G(f)})^2 \quad . \tag{11}$$

The second approach was to use Lagrange multiplier techniques to solve a truly constrained problem.

Using Lagrange multiplier techniques, it is desired to minimize the function

$$\psi = 1/I + \lambda(1 - \overline{G(f)})^2 \quad , \tag{12}$$

where λ is the Lagrange multiplier.

In principle, minimization of Equations (11) and (12) should yield equivalent results, since $1/I \ll 1$. In practice, the Lagrange multiplier approach converged more rapidly with smaller error, and was used for the subsequent analysis.

The minimization of Equation (12) is attacked by setting partial derivatives with respect to the desired variables equal to zero, and

solving the resulting set of simultaneous nonlinear equations. Noting that since

$$\overline{G(f)} = \sum_{i=1}^{N} X_i^2 = 1, \tag{13}$$

from Equation (10)

$$1/I = \sum_{i=1}^{N} X_i^2 + 2\sum_{k=1}^{N-1}\sum_{i=1}^{N-k} X_i X_{i+k}\, e^{-2\pi^2\sigma^2(k-\Delta(i)\,+\,\Delta(i+k))^2}, \tag{14}$$

Substituting Equations (13) and (14) into Equation (12), the function to be minimized becomes

$$\psi = k\left(\sum_{i=1}^{N} X_i^2 + 2\sum_{k=1}^{N-1}\sum_{i=1}^{N-k} X_i X_{i+k} e^{-2\pi^2\sigma^2(k-\Delta(i)\,+\,\Delta(i+k))^2}\right)^2$$

$$+ \lambda\left(1 - \sum_{i=1}^{N} X_i^2\right),$$

where k is a constant to adjust the initial size of the terms.

Taking appropriate partial derivatives, the minimum will be a set of values for which, using notation of Van Trees [56],

$$\nabla_{\underline{A}}\,\psi = \underline{0}^T, \tag{15}$$

where $\underline{A} = (X_1, X_2, \ldots, X_N, \lambda)$, and $\underline{0} = (0, 0, \ldots, 0)$.

These resulting equations are in general nonlinear and their solution was accomplished by use of the Fletcher-Powell search procedure [57,58]. The Fletcher-Powell method does not solve sets of simultaneous linear equations, but instead minimizes the value of a single

function. Therefore, the relation 15 was transformed into a single function

$$\nu = (\nabla_{\underline{A}} \psi)\cdot(\nabla_{\underline{A}} \psi)^{T} . \tag{16}$$

The value of $\underline{A}$ for which $\nu = 0$, is a solution of Equation (15). Also, since ν is non-negative (being the sum of squares of real numbers), $\nu = 0$ is also a minimum of ν.

The method of Fletcher and Powell is an iterative procedure for minimizing a function. It uses the fact that near a minimum of a function the second order terms of its Taylor series dominate. Therefore, the class of methods which minimize quadratic functions rapidly should provide rapid convergence in the neighborhood of the minimum. If the function were indeed quadratic, a knowledge of the inverse of the Hessian matrix would enable one to arrive at the minimum in one step. Rather than calculate the inverse directly, in the method of Fletcher and Powell, it is approximated by an iterative procedure. If the function variables during the i^{th} iteration are denoted by $\underline{A}_i$, the i^{th} approximation to the inverse of the Hessian matrix by $\underline{\underline{H}}_i$, and the gradient corresponding to the values $\underline{A}_i$ by $\underline{G}_i = \nabla_{\underline{A}} \nu$, then one step of the iteration is summarized by [58]:

(1) Compute

$$\underline{d}_i = -\underline{\underline{H}}_{i-1} \underline{G}_i$$

(2) Find λ_i which minimizes

$$\nu(\underline{A}_i + \lambda_i \underline{d}_i)$$

(3) Set

$$\underline{A}_{i+1} = \underline{A}_i + \lambda_i \underline{d}_i$$

(4) Define

$$\underline{Y}_i = \underline{G}_{i+1} - \underline{G}_i$$

(5) Compute

$$\underline{\underline{H}}_i = \underline{\underline{H}}_{i-1} + \lambda_i \frac{\underline{d}_i \underline{d}_i^T}{\underline{G}_i^T \underline{\underline{H}}_{i-1} \underline{G}_i} - \frac{\underline{\underline{H}}_{i-1} \underline{Y}_i \underline{Y}_i^T \underline{\underline{H}}_{i-1}}{\underline{Y}_i^T \underline{\underline{H}}_{i-1} \underline{Y}_i} .$$

Then the iteration is repeated; the process was terminated when the magnitude of $\underline{G}$ became less than some specified value. The method of determining the λ_i is not critical; cubic interpolation was used for this implementation of the Fletcher Powell algorithm. Usually $\underline{\underline{H}}_0$ is chosen equal to the identity matrix so that the first step is in the direction of steepest descent.

The required equations were programmed on the UNIVAC 1108 computer, and a number of MIP designs were calculated. The first step in arriving at these MIP processors was to compare results with those of earlier investigations. The only earlier results which are available are in an article by Capon [28], where the weights which maximize I were derived for the unstaggered PRF case. Capon's results are given in terms of the covariance matrix of the clutter spectrum, rather than the power spectrum of clutter discussed earlier. However, since Gaussian spectra were assumed, the transformation from power spectra to the autocovariance function, ρ, is straightforward. Nathanson [59] shows that the autocovariance function of the clutter, $\rho(\tau)$, is given by

$$\rho(\tau) = e^{-\tau^2/2\sigma_\tau^2}$$

where

$$\sigma_\tau = \frac{1}{2\pi\sigma_c} .$$

Noting that for the unstaggered PRF case, $\tau = nT$, then

$$\rho(nT) = e^{-2n^2\pi^2(nT\sigma_c)^2} .$$

For the three pulse case, Capon's optimum weights for unstaggered PRF systems are given by [8],

$$1, \frac{-\rho(2T) + \sqrt{\rho^2(2T) + 8\rho^2(T)}}{2\rho(T)}, 1.$$

In order to calculate some representative check cases, consider an S-band system (one operating at 10 cm or 3.0 GHz) with a PRF of 1000 Hz. Data summarized in Table 2 indicate typical values of σ_v from 0.01 to 2.0 meter/second. A value of 2.0 meters/second corresponds to σ_c of 40 Hz ($\sigma_c = 2\sigma_v/\lambda_c$), where λ_c is the wavelength or $\sigma = .04$. Then

$$\rho(T) = .968910791$$

$$\rho(2T) = .881323137$$

and the optimum weights become

$$1, -1.961790501, 1$$

or renormalizing to $\overline{H(\omega)} = 1$, these become

$$0.413497820, -.81119695, 0.413497820$$

Calculations for a three-pulse MIP using the method described in this section agree with these results to 4 significant figures and values of I calculated using the weights calculated by the two methods agree to within 0.2 dB.

Comparison with Earlier Designs. Once the MIP design algorithms were verified, these MIP designs were used to calculate a number of improved processors, and performance of these MIP's compared with performance of earlier designs. Three general classes of previous designs were selected for comparison purposes; conventional integral weight processors, a processor of Shrader [5], and a processor of Taylor [45,46].

Initially, the performance of a conventional 3 pulse integral weight canceller was compared with that of the MIP designs when $\Delta(2)$ only was varied. Figure 23 compares MTI improvement, I, as a function of $\Delta(2)$ for both conventional processors and MIP's for $\sigma = 0.04$. As can be seen, considerable improvements in I are possible using these MIP's.

Rather than vary $\Delta(2)$ alone, the more conventional approach is to vary both $\Delta(2)$ and $\Delta(3)$ together by choosing $\Delta(2) = -\epsilon$ and $\Delta(3) = \epsilon$, where $0 \leq \epsilon \leq 1.0$. Plots of I vs ϵ are presented in Figure 24 for both conventional processors and MIP's, again indicating substantial improvements using MIP's for $\epsilon \geq 0.05$.

The amount of additional improvement obtainable by use of a MIP rather than a conventional processor is a function of both σ and ϵ. In order to illustrate this dependence on σ, I was plotted as a function

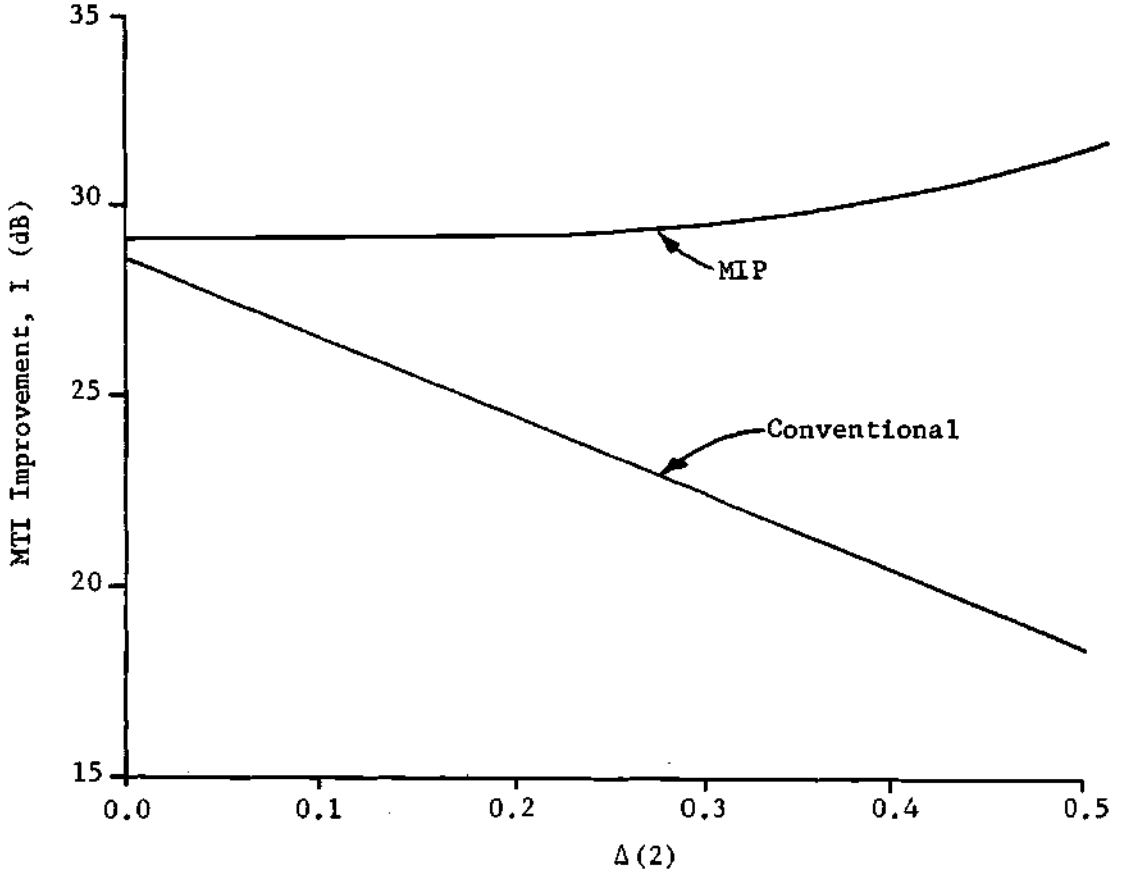


Figure 23. I for Conventional Three Pulse Processor and Three Pulse MIP as a Function of $\Delta(2)$. $\sigma = 0.04$.

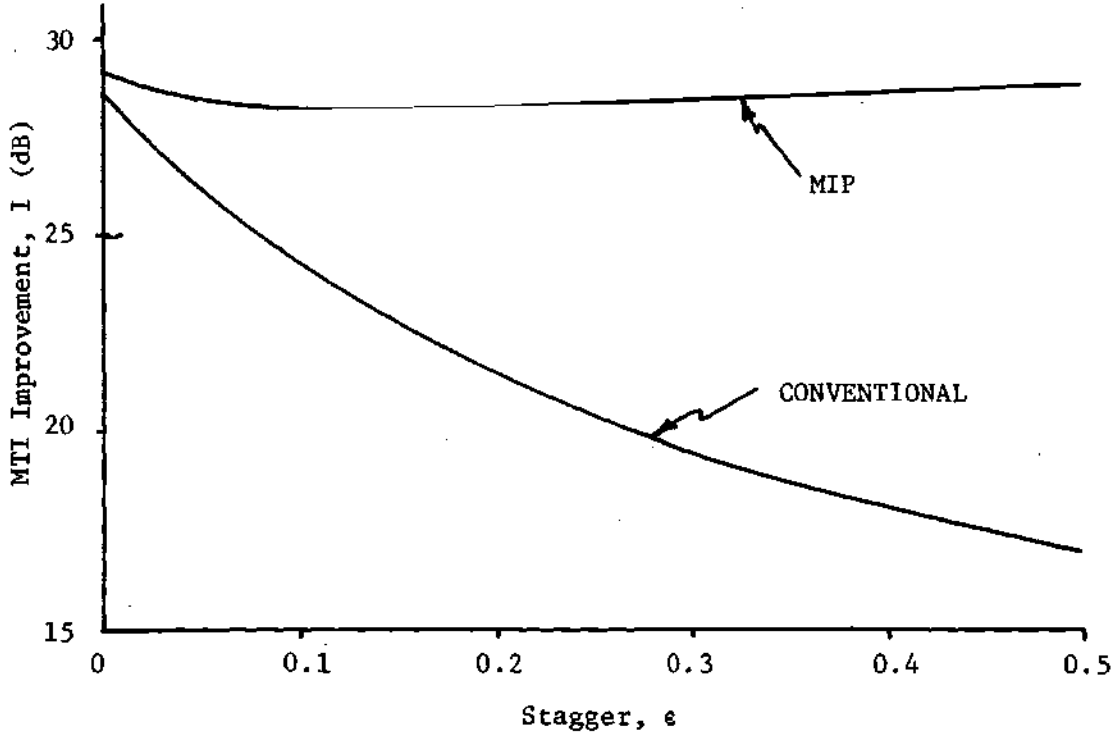


Figure 24. I for Conventional Three Pulse Processor and Three Pulse MIP as a Function of Stagger, ϵ. $\sigma = 0.04$.

of σ for both a conventional processor and a MIP for $\epsilon = 0.3$. The results are shown as Figure 25, indicating that the improvements in I are most significant for values of $\sigma > 0.02$. For values of σ less than this, conventional processors and MIP's have values of I which are relatively close to each other; however, this is also the region where I becomes so large as to be limited by the quantization errors discussed in Chapter II.

A comparison of a four-pulse processor designed using procedures outlined by Shrader with a four pulse MIP has been carried out. Shrader's rule for selection of the stagger sequence for a four pulse processor is to add the values -3, 2, -1, 3 to the value of V_b/PRF, where V_b is the desired first blind Doppler frequency [5]. Selecting $V_b/PRF = 8$ (corresponding to the first blind speed at approximately the speed of sound for our earlier S-band example) results in ratios of 5:10:7:11 or values for $\Delta(i)$ of -0.06, 0.15, 0.0 and 0.33. Figure 26 compares improvement for the design of Shrader and a MIP as a function of σ using the same PRF stagger sequence for each case. Again, for relatively large values of σ, substantial increases in I over conventional design procedures are possible, approaching 20 dB in some cases. Thus, the behavior for the three pulse case is also reflected in this particular four pulse case, again showing significant improvement for large values of σ and illustrating, since improvement becomes large for small σ, the practicality of constraining improvement for small values of σ in order to obtain more uniform response.

The frequency response of the processor specified by Shrader is

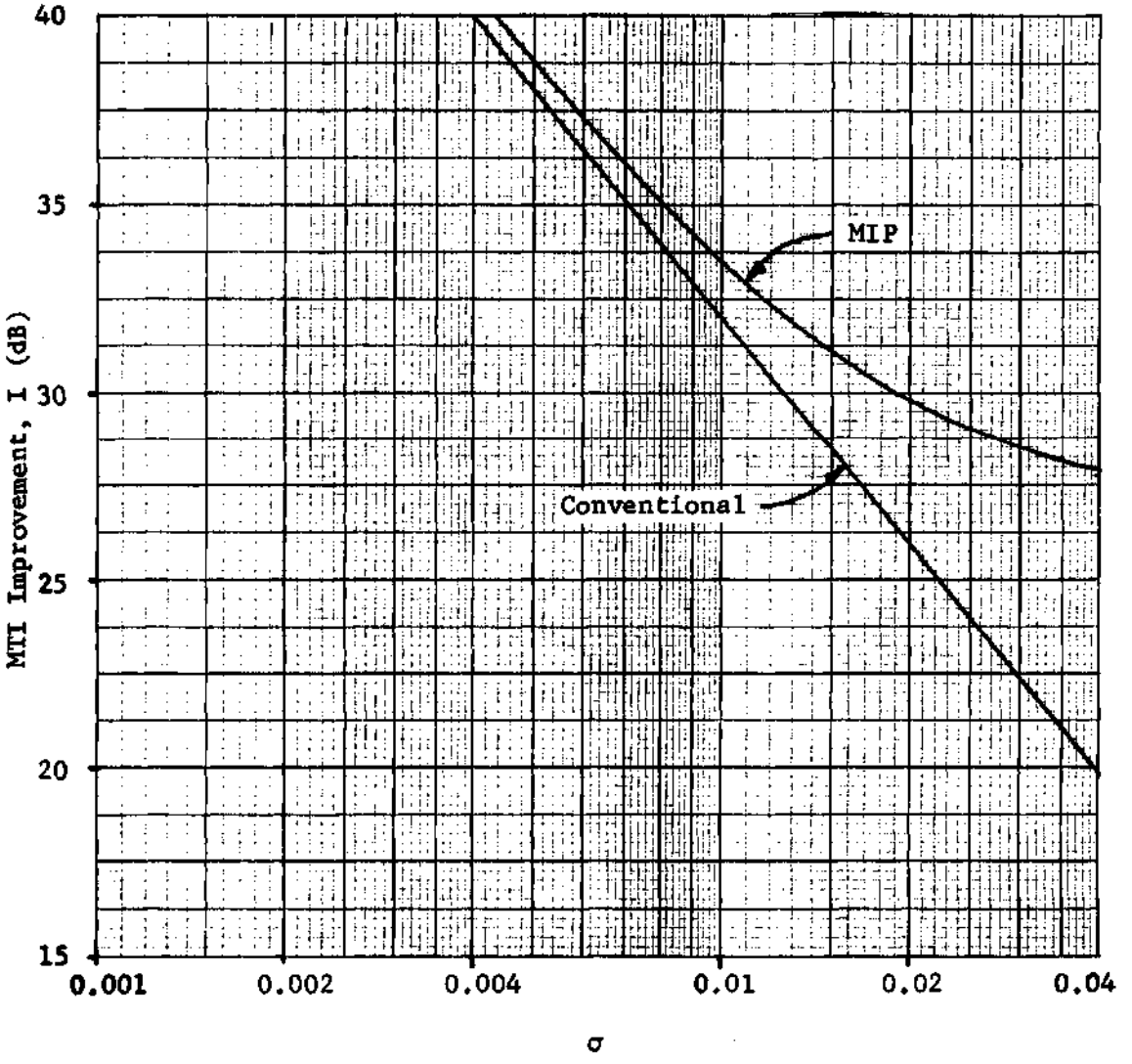


Figure 25. I for Conventional Three Pulse Processor and Three Pulse MIP as a Function of Spectral Width, σ. $\epsilon = 0.3$.

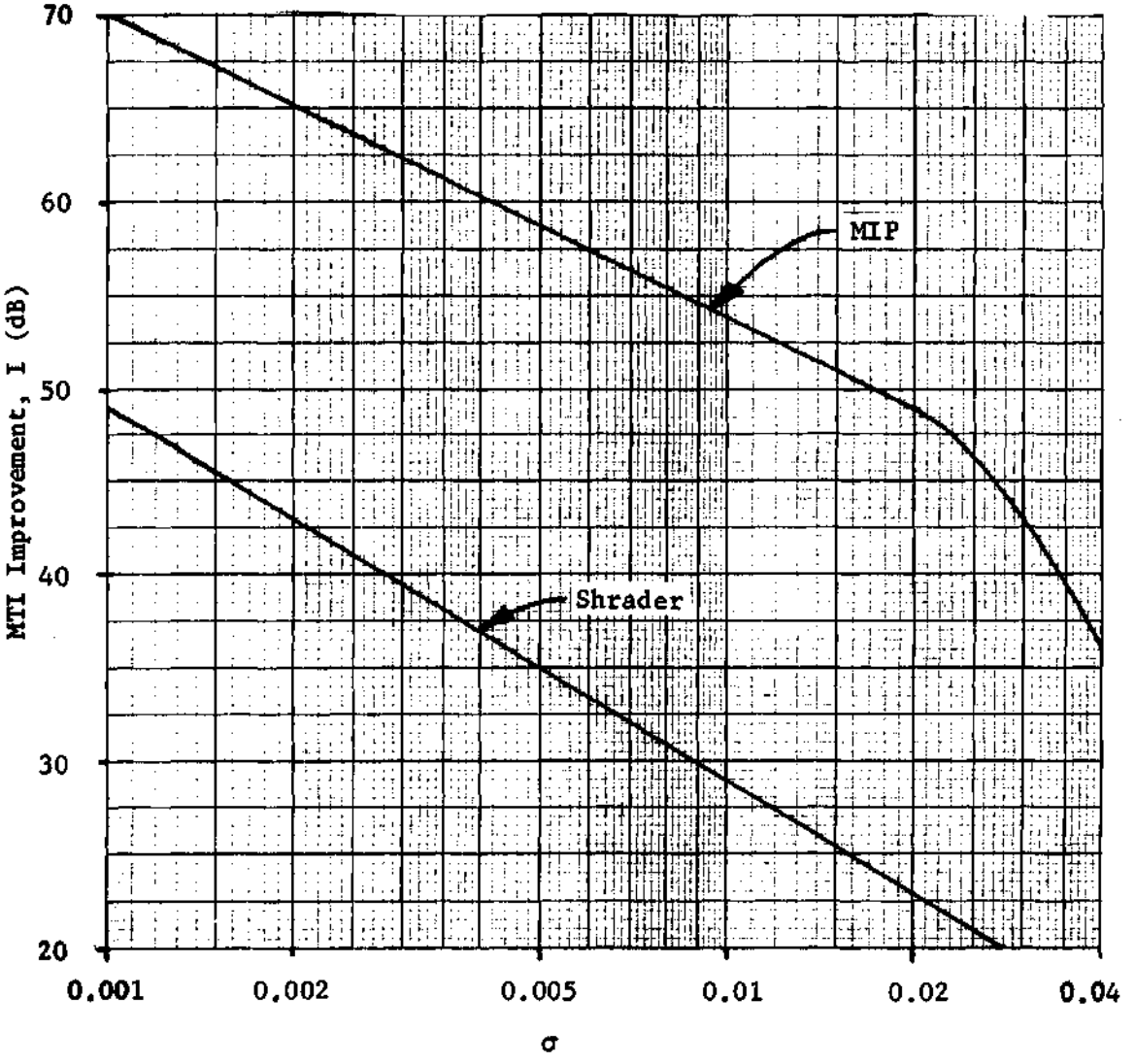


Figure 26. I as a function of σ for a MIP and a Processor of Shrader. Value of $V_b/PRF = 8$ was used, Resulting in Δ's of -0.06, 0.15, 0.0, and 0.33.

presented in Figure 27, and it is interesting to compare this with the frequency response of the MIP shown in Figure 28 (σ = 0.01). In spite of the fact that the processor of Figure 28 has approximately 26 dB more MTI improvement (for σ = 0.01, see Figure 26) than processors designed with Shrader's procedure, frequency responses of the two systems are certainly comparable. In fact, due to lower high-amplitude ripples, some might find the MIP response more desirable than that of Shrader.

A four pulse processor proposed by Taylor [49,50] was selected for comparison purposes. Both exact and rounded weights are given by Taylor. Calculated improvement for the exact case (weights .3323, -.7796, .5893, -.1511) was 26.83 dB and for the rounded weights (.3207, -.7434, .5685, -.1458, after normalization) was 26.86 dB; also there was little difference in shape of the frequency response curves for the two cases, so the following discussion is applicable to both the exact and rounded processor of Taylor. The MIP design procedure was used to calculate optimum weights for the PRF stagger sequence of Taylor (-.25, 0, .25, 0) and σ = 0.04. Resulting weights were .25521, -.63276, .67295, -.28532, resulting in an improvement of 34.56 dB.

In order to compare performance of the Taylor processors and the MIP, frequency responses were calculated for both processors. Figure 29 compares the frequency response of the MIP with the response of Taylor's processor; the MIP used the same PRF stagger sequence as Taylor, and a value of σ = 0.04 was assumed. In spite of the fact that the MIP has approximately 8 dB more improvement than Taylor's design, the frequency response of the MIP is even more uniform (and desirable)

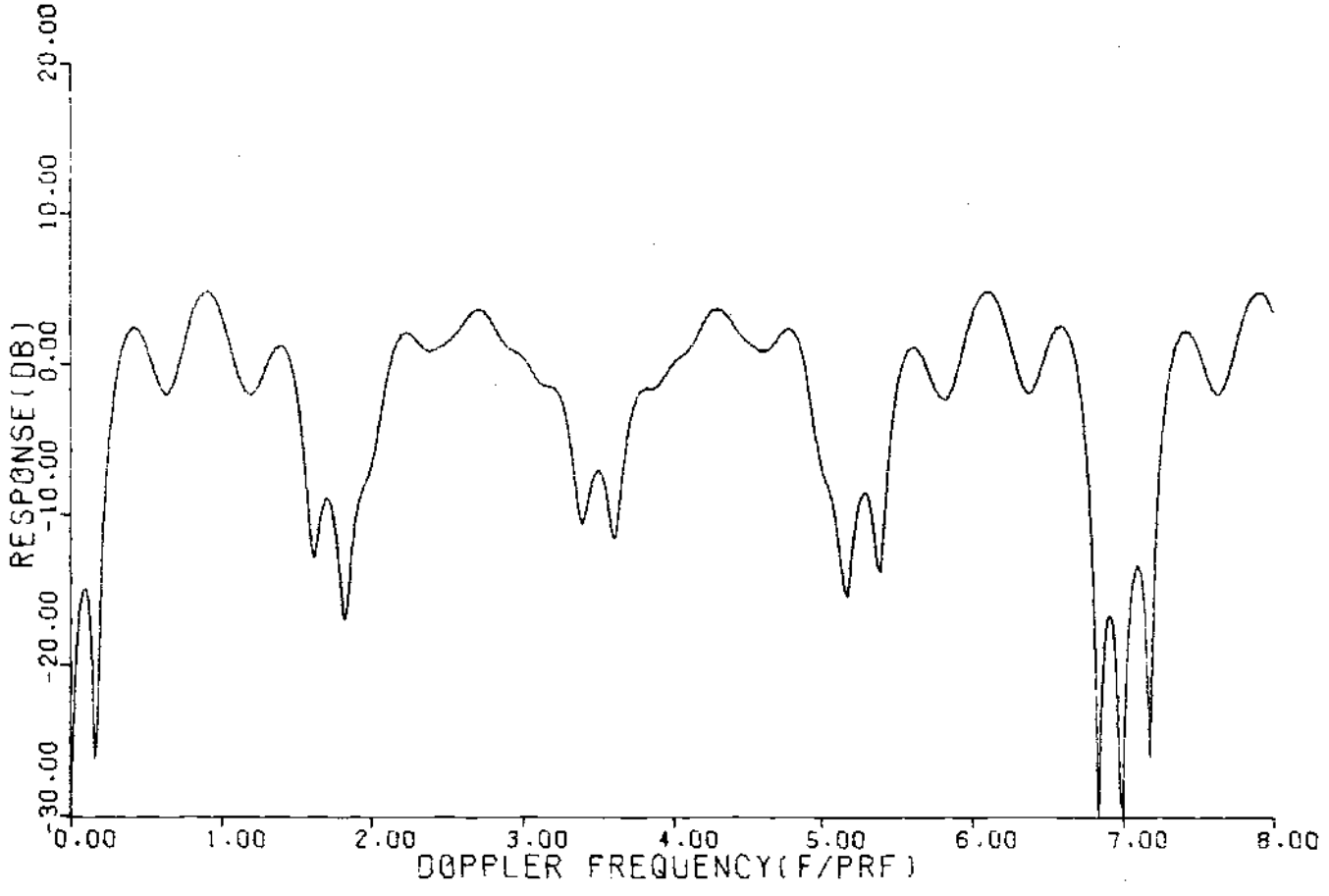


Figure 27. Response of Four Pulse Processor Designed Using the Method of Shrader.

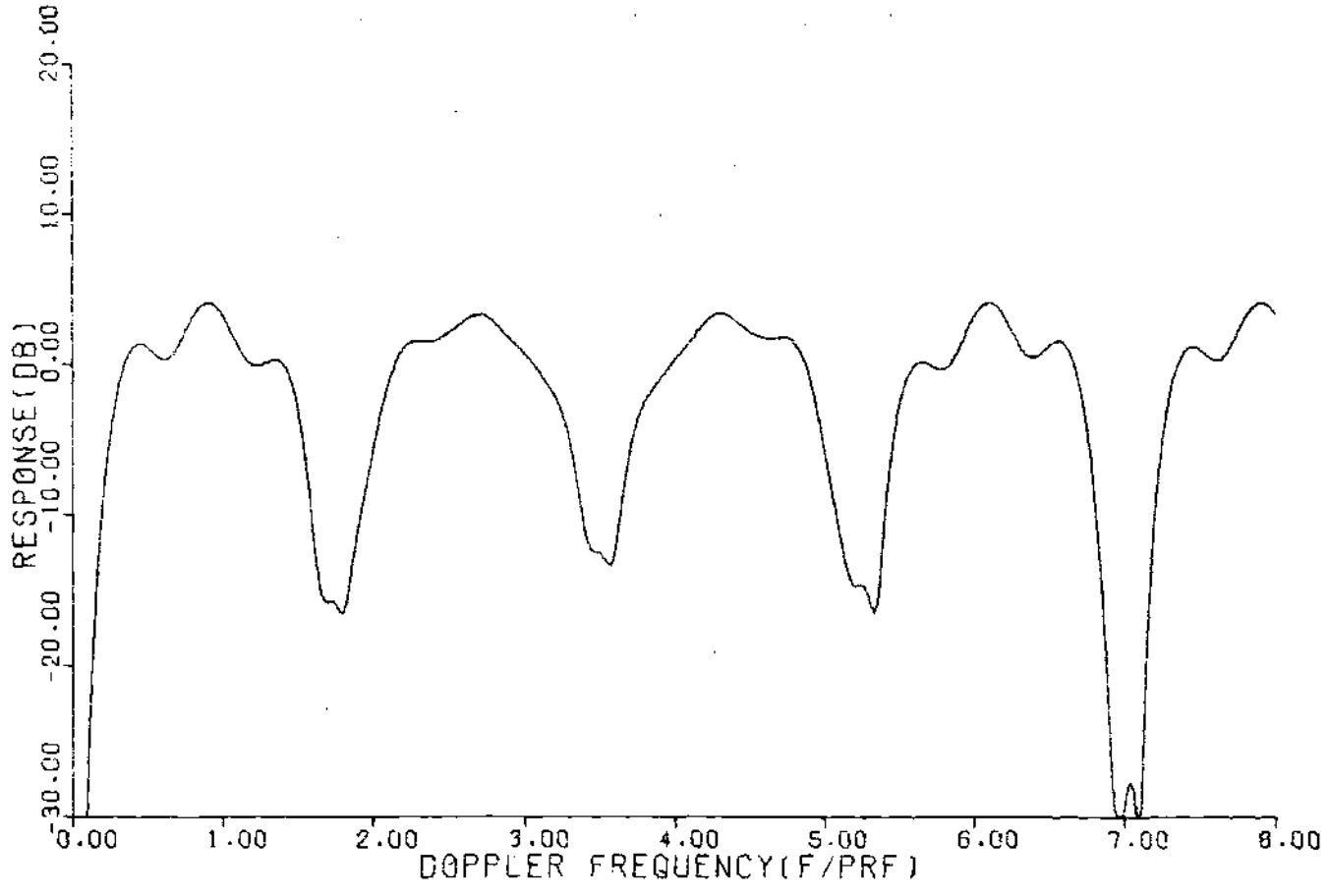


Figure 28. Response of Four Pulse MIP Using PRF Stagger Sequence of Shrader.

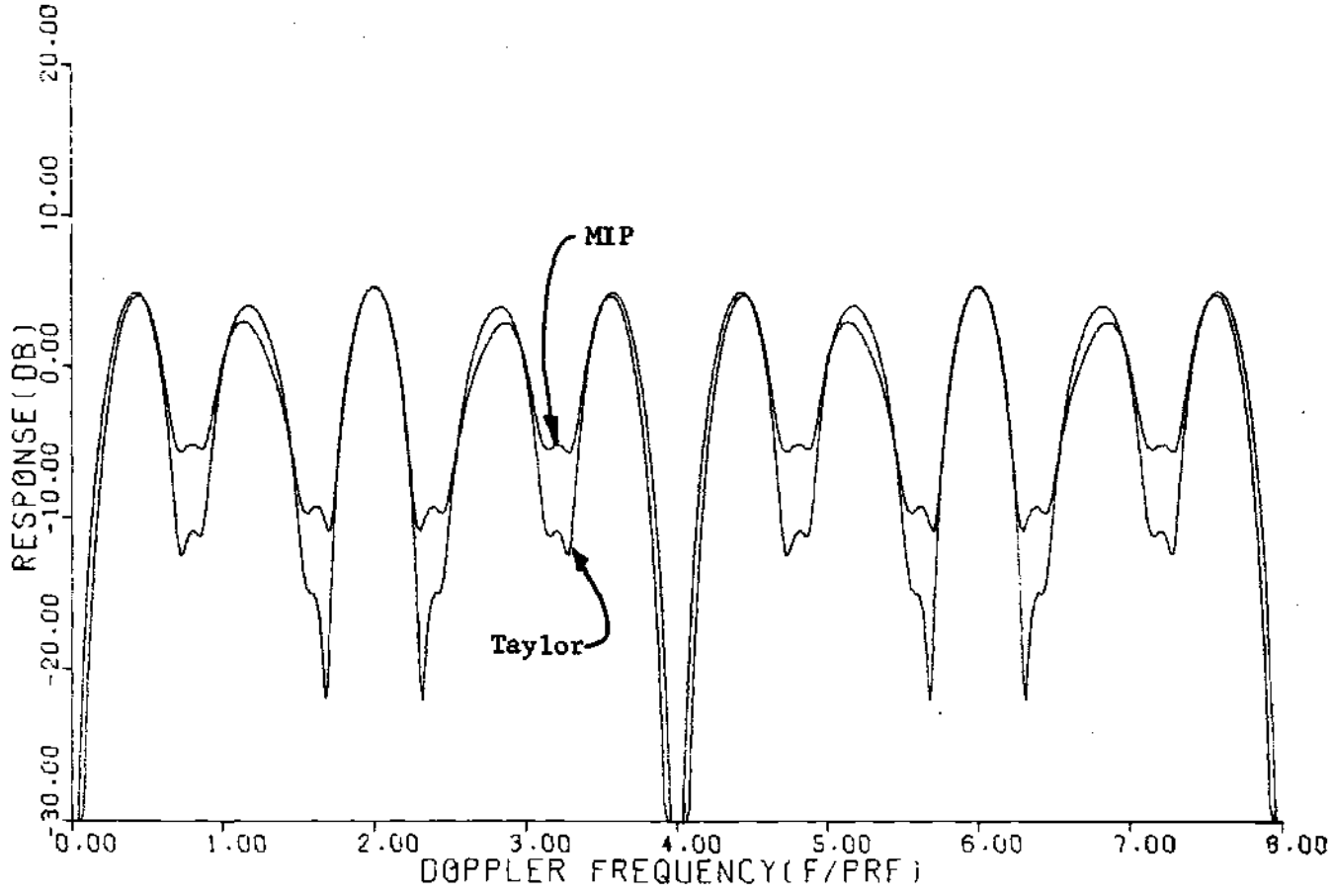


Figure 29. Frequency Responses for Processor of Taylor and for a MIP Using the Same PRF Stagger Sequence.

than Taylor's, having approximately 10 dB shallower dips in response than the processor of Taylor.

In order to more clearly illustrate the advantages of the MIP over the design of Taylor, cumulative distributions of response (discussed earlier in Chapter 3 and in Figure 13) for the two processors are presented as Figure 30, showing the reduced frequency of occurrence of low amplitude responses for the MIP. For example, use of the MIP results in a 2:1 reduction in the occurrence of responses more than 10 dB below the average response, and a slightly reduced probability of responses above 0 dB. These two facts indicate the MIP clusters more closely about the average value than the Taylor processor, certainly a most desirable feature.

Thus we can see that substantial increases in MTI improvement over previous design techniques are possible using these MIP design techniques, without an appreciable sacrifice (and in some cases, an improvement in) Doppler frequency response. The improvement in performance is largest for large values of σ, which is the real problem area for MTI systems. For smaller values of σ, the differences in improvement become less pronounced, but at the same time the improvement becomes sufficiently large that equipment-related problems (transmitter or receiver stability, analog-to-digital quantization errors, etc.) usually become the factor limiting MTI system performance. This fact is a portion of the motivation for the next step in the research.

The next step will capitalize on the fact that there is an equipment related limit placed on MTI improvement, regardless of the

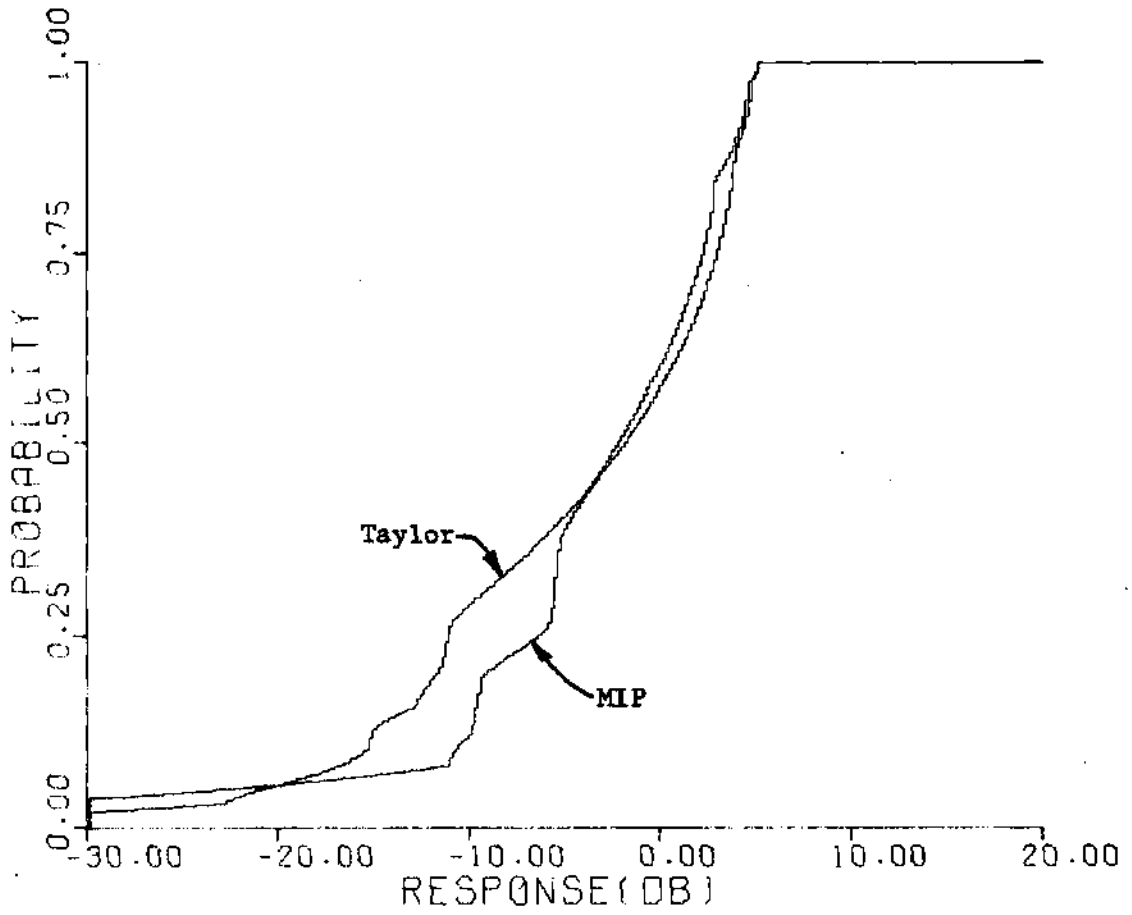


Figure 30. Cumulative Distributions of Response for Processor of Taylor and a MIP Using the Same PRF Stagger Sequence.

calculated improvement based on the clutter spectra and frequency response alone. The concept which will be used will constrain the MTI improvement to some practical and achievable value (often much less than the theoretical maximum), and use the resulting flexibility to optimize the shape of the frequency response curve. This concept is developed at length in the next section.

Constrained Improvement Processors

Discussions in the preceding section show that a considerable improvement in performance over conventional processors is possible using MTI's. MTI improvement may be appreciably increased over conventional designs using MTI's with no degradation, and, in some cases, an improvement in the shape of the frequency response curve. As was discussed earlier, this fact leads one to the development of a class of MTI processors which limit improvement to some specified (and presumably achievable) value, and uses the flexibility thus gained to achieve a more uniform amplitude response as a function of target Doppler frequency. Such a class of processors will now be discussed, and will be referred to as Constrained Improvement Processors (CIP's).

While the staggered PRF CIP's are similar in many ways to unstaggered PRF Constrained Improvement Processors, in addition to the weights, the PRF stagger must also be controlled. This spacing of the pulses may not be arbitrarily selected in order to optimize performance, but must remain within some bounds. If the interpulse period becomes too small, the unambiguous range specification, or the transmitter duty cycle limitation, may be exceeded.

Thus, the design procedure for CIP's for staggered PRF systems is: first, specify a desirable and achievable improvement, I; second, specify the number of pulses to be processed; third, establish the desired characteristics of the PRF stagger sequence; and finally, subject to these three constraints, minimize the mean square deviation from constant response for all frequencies of interest.

There are two broad categories of CIP's which will be considered: for the first, the PRF stagger sequence is fixed and the filter weights allowed to vary to optimize response, while the second class of CIP's fixes the weights and allows the stagger sequence to vary within specified limits in order to optimize performance. Both classes of processors will be treated in detail in the following discussions.

The section is subdivided into a number of separate, but related sections: first, CIP design methods are discussed; second, the search strategy for CIP's is presented; third, CIP's are compared with earlier designs; finally, some representative CIP's are presented and effects of changes in design parameters are investigated.

CIP Design Methods. As outlined earlier, the design of CIP's uses Lagrange multiplier techniques to minimize the mean square deviation of processor response from constant over a specified frequency interval, while keeping I equal to some specified value.

The frequency response, G(f), of the processors, is given by Equation (6) as

$$G(f) = \sum_{i=1}^{N} X_i^2 + \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} 2X_i X_{i+k} \cos[2\pi f(k-\Delta(i)+\Delta(i+k))]$$

It is now desired to minimize the mean square deviation of the frequency response from a constant value over the range of normalized frequency from zero to f'. The mean square error (mse) is given by

$$\text{mse} = \frac{1}{f'} \int_0^{f'} (1-G(f))^2 \, df, \tag{17}$$

where f' is the highest frequency of interest. Performing the indicated multiplication and integration, Equation (17) becomes

$$\begin{aligned}\text{mse} = &\sum_{i=1}^{N} \sum_{j=1}^{N} X_i^2 X_j^2 - \sum_{i=1}^{N} X_i^2 + 1 \\ &+ 4\left(\sum_{j=1}^{N} X_j^2 - 1\right) \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} X_i X_{i+k} \frac{\sin(2\pi f'(k-\Delta(i)+\Delta(i+k))}{2\pi f'(k-\Delta(i)+\Delta(i+k))} \\ &+ 2 \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} \sum_{j=1}^{N-1} \sum_{L=1}^{N-j} X_i X_{i+k} X_L X_{L+j} \\ &\cdot \left[\frac{\sin(2\pi f'(k-\Delta(i) + \Delta(i+k) - j + \Delta(L) - \Delta(L+j)))}{2\pi f'(k-\Delta(i) + \Delta(i+k) - j + \Delta(L) - \Delta(L+j))} \right. \\ &\left. + \frac{\sin(2\pi f'(k-\Delta(i) + \Delta(i+k) + j - \Delta(L) + \Delta(L+j)))}{2\pi f'(k-\Delta(i) + \Delta(i+k) + j - \Delta(L) + (L+j))} \right],\end{aligned} \tag{18}$$

and the desired value of I, designated by γ,

$$\gamma = \frac{\sum_{i=1}^{N} X_i^2}{\sum_{i=1}^{N} X_i^2 + 2 \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} X_i X_{i+k} e^{-2\pi^2 \sigma^2 (k-\Delta(i)+\Delta(i+k))^2}}, \tag{19}$$

is a constraint of the problem.

The Lagrange multiplier solution to this problem is obtained by introducing the Lagrange multiplier, λ. The function to be minimized, designated by Φ, is given by

$$\Phi = \text{mse} + \lambda k \left[\gamma \sum_{i=1}^{N} X_i^2 + 2\gamma \sum_{k=1}^{N-1} \sum_{i=1}^{N-k} X_i X_{i+k} e^{-2\pi^2\sigma^2(k-\Delta(i)+\Delta(i+k))^2} - \sum_{i=1}^{N} X_i^2 \right], \tag{20}$$

where k is a constant introduced to adjust the relative initial size of the terms of Equation (20).

The desired solution is obtained when the partial derivatives of Equation (20) are simultaneously equal to zero. The appropriate partial derivatives depend upon which set of variables are being used to minimize Equation (20).

If the weights are being varied to minimize Equation (20), the solution is obtained when

$$\nabla_{\underline{A}} \Phi = \underline{0}^T, \tag{21}$$

where $\underline{A} = (X_1, X_2, \ldots, X_N, \lambda)$.

If the PRF stagger sequence is being used to minimize Equation (20), the required condition is still given by Equation (21), but $\underline{A}$ would be given by $\underline{A} = (\Delta_1, \Delta_2, \ldots, \Delta_N, \lambda)$.

Unfortunately, satisfying Equation (21) in general requires solution of a set of simultaneous nonlinear equations. As in the MIP case discussed earlier, the Fletcher-Powell algorithm [57,58] was used

to arrive at a solution. In order to use the Fletcher-Powell algorithm to solve Equation (21), as before, define a new variable

$$\nu = (\nabla_{\underline{A}} \Phi)\cdot(\nabla_{\underline{A}} \Phi)^{T} . \tag{22}$$

As was the case for Equation (21), if a solution of Equation (22) is being sought by varying the weights, $\underline{A} = (X_1, X_2, \ldots, X_N, \lambda)$, and if the stagger sequence is to be varied, $\underline{A} = (\Delta_1, \Delta_2, \ldots, \Delta_N, \lambda)$. The solution $\nu = 0$, which is also a solution of Equation (21), was then determined using the Fletcher-Powell search procedure. Details are given in the earlier discussion of MIP design methods and in references 57 and 58.

The Fletcher-Powell method easily located zeros (which are global minima; see Equation (22)) of Equation (22) with adequate accuracy. The search was generally terminated when the magnitude of the gradient vector was less than .0001, corresponding to a value of the function being minimized of between 10^{-8} and 10^{-12}.

CIP Search Strategy. A zero of Equation (22) does not necessarily define the CIP. There are several possible conditions which may correspond to a zero, including a minimum, a maximum, or an inflection point of Equation (20). In case the zero corresponds to a minimum, this minimum may be either a local or a global minimum. Thus, a rational search strategy is required in order to arrive at reasonable processors. As an aid to identifying which condition exists at a given solution point, the mean square error and improvement, I, were calculated and printed when the search procedure terminated.

The type of solution determined by the search procedure is dependent upon the initial starting point, and whether minimization is being accomplished by varying the X's or the Δ's. The minimization for the X's is generally more straightforward and will be discussed first.

The solution obtained to Equation (21) by varying the X's is dependent on the initial values chosen to begin the search; note that there are at least two global minima, the variables for one being the negative of the other (see Equation (20)). The choice of initial point strongly effects the type of solution which results; the choice of initial parameters is not entirely arbitrary, however, since it is known that $\sum_{i=1}^{N} X_i^2 \approx 1$ and $\sum_{i=1}^{N} X_i \approx 0$. The first of these conditions is because the average response will usually lie close to one, while the second results from the fact that the processor must generally exhibit a substantial value of MTI improvement. It was found that for initial points which satisfied these two conditions, the proper choice of signs of the initial X's almost always resulted in a minimum being reached. The fact that this minimum is a global minimum has been verified by exhaustive search for several test cases. Once a solution has been determined, CIP's for small variations in I or in the stagger sequence may be obtained by using the original CIP as the starting point for the new search.

The question of achieving a minimum for Equation (20) by varying the stagger sequence (the Δ's) is somewhat more difficult. One reason for this difficulty is due to the fact that in order to preserve the unambiguous range of the radar or to stay within transmitter limitations,

the values of the interpulse period must be constrained, and the second reason is the highly oscillatory nature of Equation (20) as the Δ's are varied.

The highly oscillatory nature of Equation (20) as the Δ's are varied is at least partially due to Gibbs phenomenon. These oscillations may be reduced by the use of appropriate weighting functions, in a manner similar to conventional digital filter design practice [32]. It was found that a raised cosine weight function rather effectively reduced the tendency toward oscillatory behavior. It was also found that relaxing the improvement constraint, i.e., allowing the search to deviate slightly from the hypersurface I = constant during the search, produced the same end result. This was easily accomplished by selecting appropriate values of $K < 1$ in Equation (20).

The second problem in minimization of Equation (20) was the need to bound the variation in interpulse period. If the variation was not bounded, the pulse spacing would adjust itself so that one interpulse period would become extremely small. This spacing would be selected so that a term in Equation (5) would be non-zero over the expected range of target Doppler frequencies. Such spacing would almost certainly violate system specifications.

In order to bound the interpulse period, initially certain Δ's (usually two) were held constant while the others were allowed to vary. This could have been accomplished by setting certain terms in the inverse of the Hessian matrix of the Fletcher-Powell algorithm equal to zero [60]. Equivalent results were obtained by setting selected

elements of the gradient matrix equal to zero. This approach was successful, but required that a large number of fixed values be investigated in order to determine the optimum value which falls within the stated constraint.

A more satisfactory approach to PRF stagger optimization was to select an initial set of Δ's which satisfy the design constraints, and then look for the local minimum of Equation (20) near this set of initial values. This local minimum then corresponds to the optimized PRF stagger sequence closely corresponding to the constraints which were expressed in the initial values of Δ.

Comparison with Earlier Processors. The selection of suitable earlier designs for comparison purposes presents some difficulties. While the concept of staggered PRF has been discussed by a number of authors, the question of optimization of processor design has been treated by only a few. Most of these earlier attempts at processor design have involved processing a large number of received pulses, which is not the case of most interest when discussing modern, high performance radars.

Processors for staggered PRF systems proposed by Taylor [50], Shrader [5] and Jacomini [51] were selected for comparison with four pulse CIP's designed using parameters

$$\sigma = 0.01$$

$$f' = 8$$

$$I = 30 \text{ dB}.$$

The frequency response of a four pulse processor designed using

the procedures set forth by Taylor is given in Figure 31 and that of a four pulse CIP in Figure 32. The CIP was designed using the PRF stagger sequence of Taylor, and weights were selected to optimize the response. As can be clearly seen, the CIP has a response which clusters more closely about 0 dB with much shallower null depths than the processor of Taylor. Figures 33 and 34 give the probability densities of response for the two processors, and Figure 35 compares the cumulative distributions of response for the CIP and Taylor processors. From Figures 33 and 34, the CIP offers a significant reduction in probability of low frequency response and at the same time a corresponding increase in occurrence of responses near one. Figure 35 illustrates the fact that with the CIP there is approximately a three-to-one reduction in the fraction of frequencies for which the response is less than -10 dB.

The PRF stagger sequence of Taylor is not optimum, however, since processors having even more uniform responses may be designed. Figure 36 gives the frequency response of one such four pulse CIP, having a maximum variation of $\pm$ 20% in interpulse period (a smaller variation than the variation for the processor of Taylor); comparison of this response with the response shown in Figure 31 clearly illustrates the advantage of the CIP, achieving more uniform response with smaller variations in interpulse period.

A ten pulse processor of Shrader was next selected for comparison with a four pulse CIP. Response for the Shrader 10 pulse processor is shown in Figure 37, and may be compared with the CIP response shown in Figure 36. As is shown in Figures 36 and 37, all of the null depths

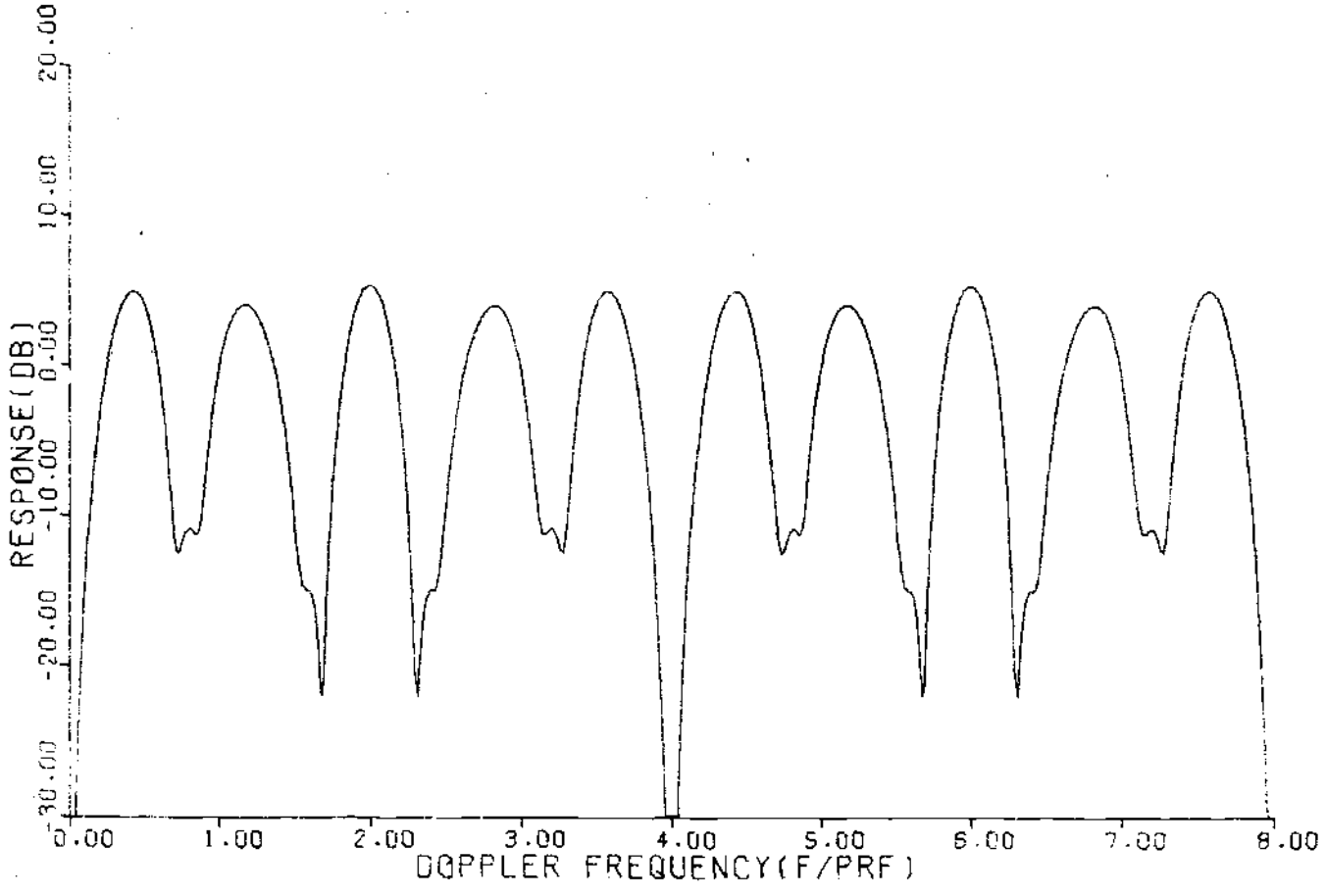


Figure 31. Response of Four Pulse Processor of Taylor.

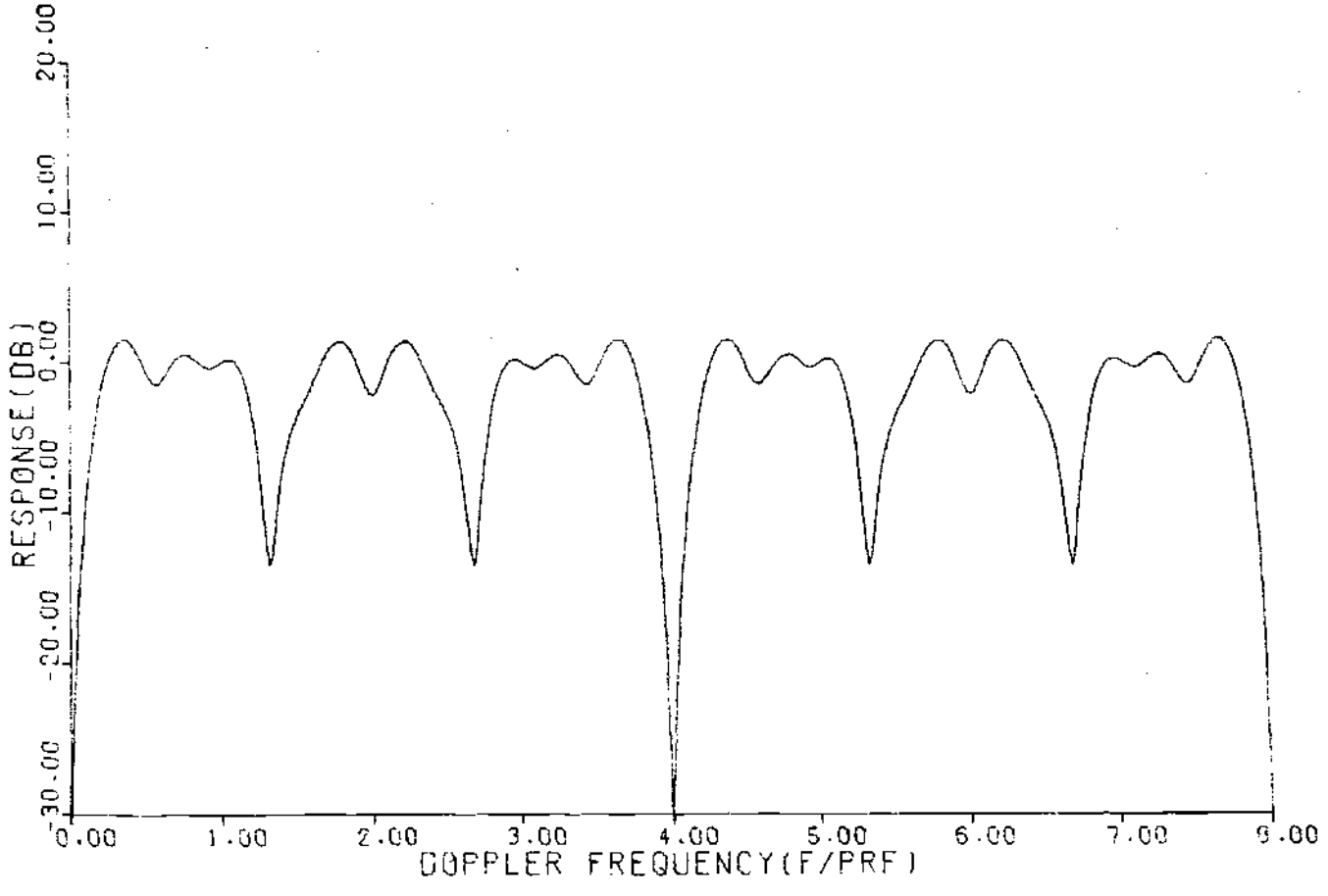


Figure 32. Response of Four Pulse CIP Using Stagger Sequence of Taylor.

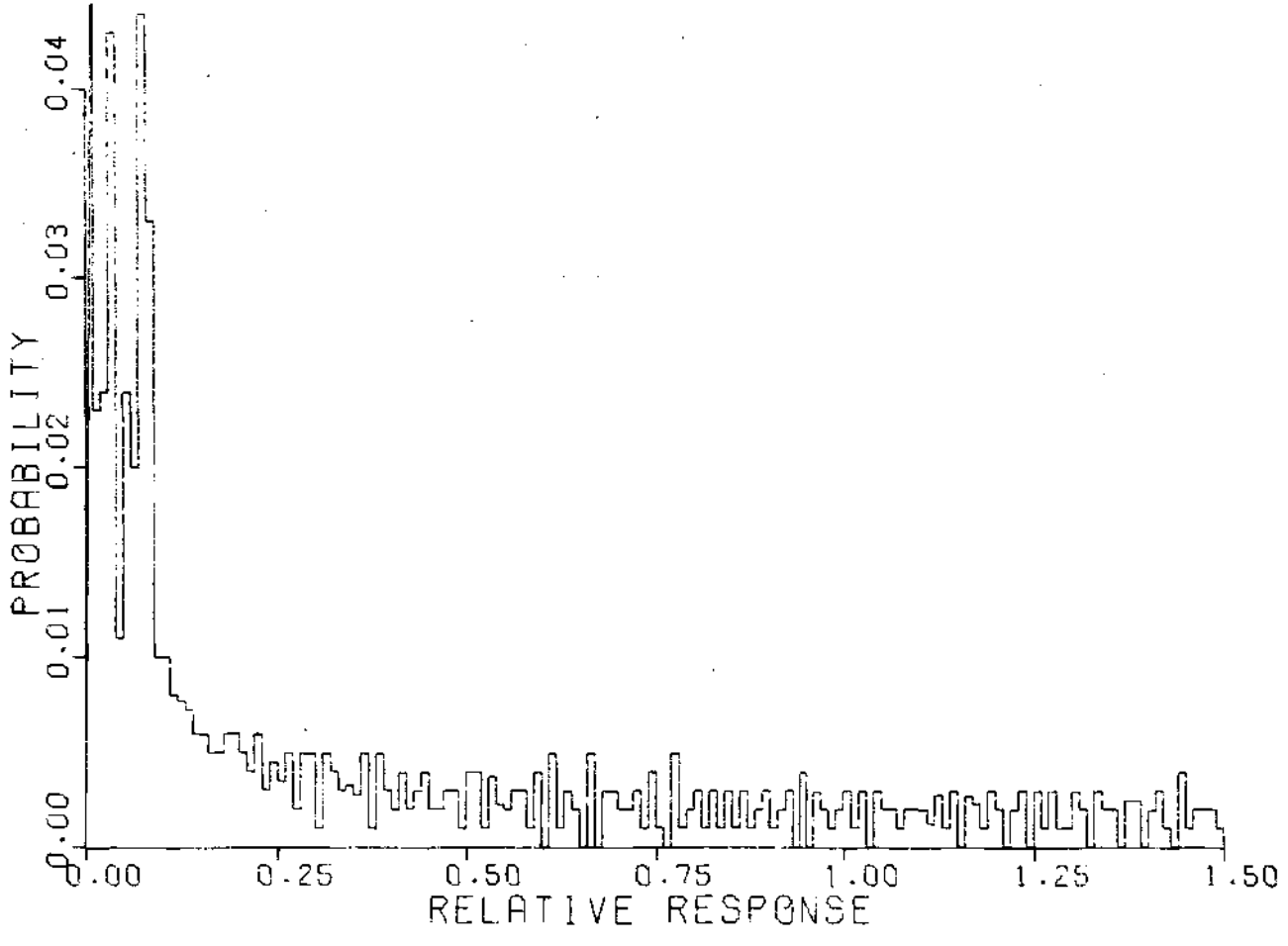


Figure 33. Probability Density Function of Response for Four Pulse Processor of Taylor.

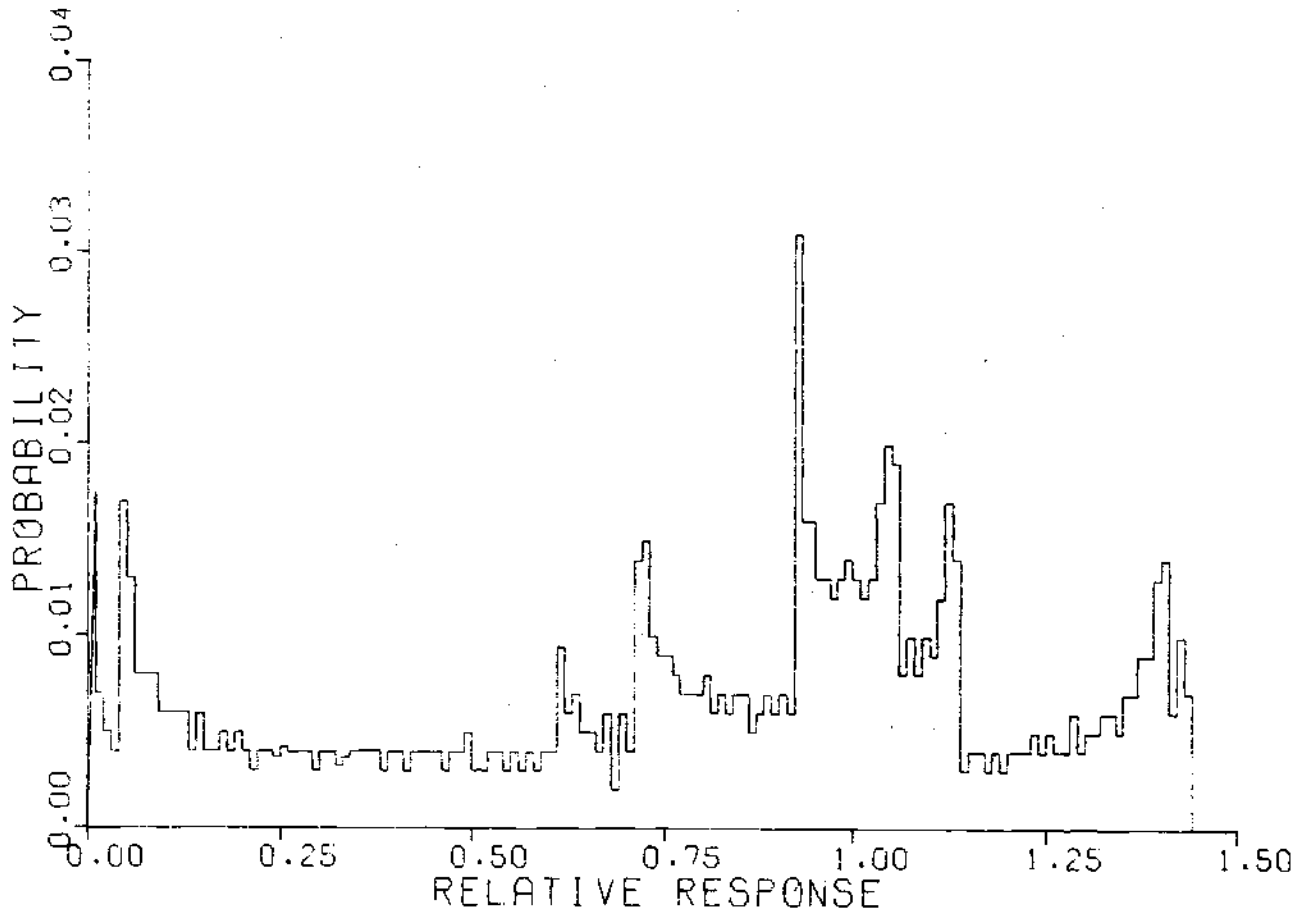


Figure 34. Probability Density Function of Response for CIP Using Stagger Sequence of Taylor.

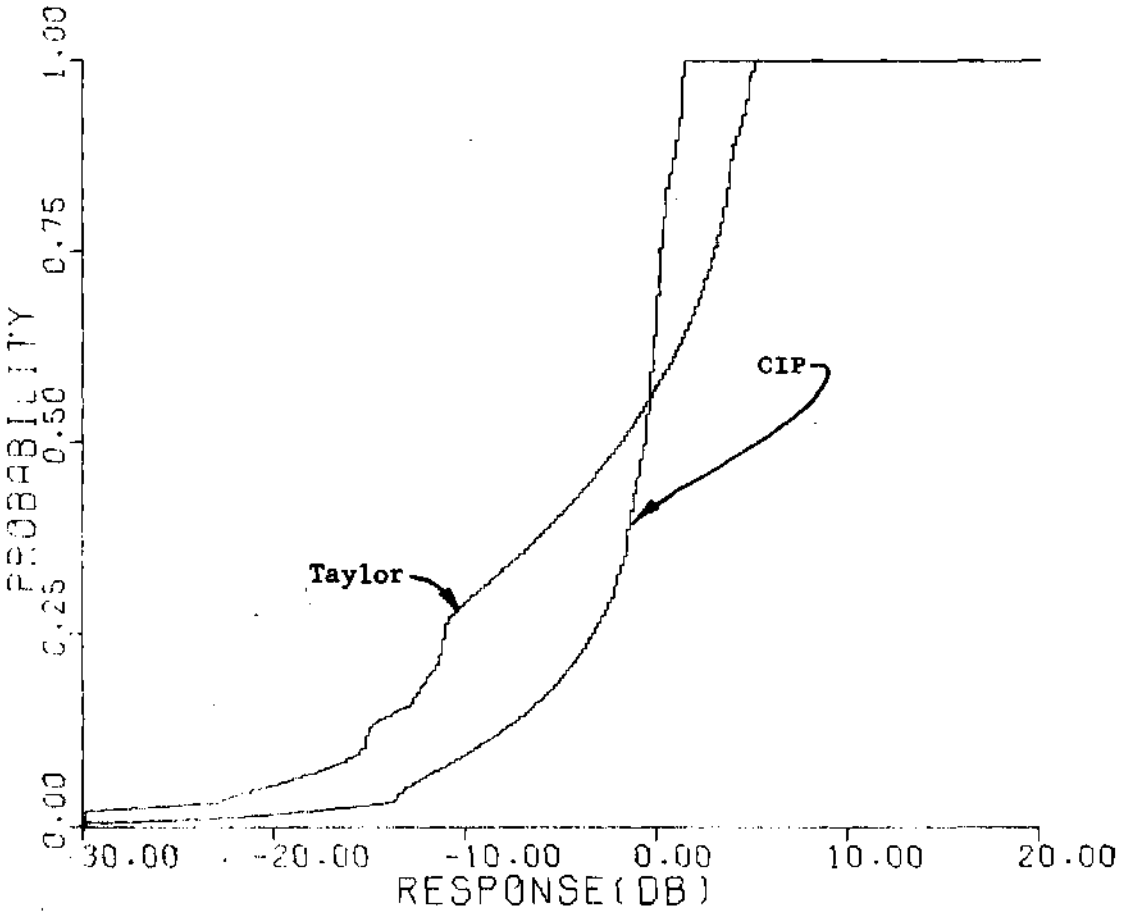


Figure 35. Cumulative Distributions of Response for Processor of Taylor and Four Pulse CIP Using Stagger Sequence of Taylor.

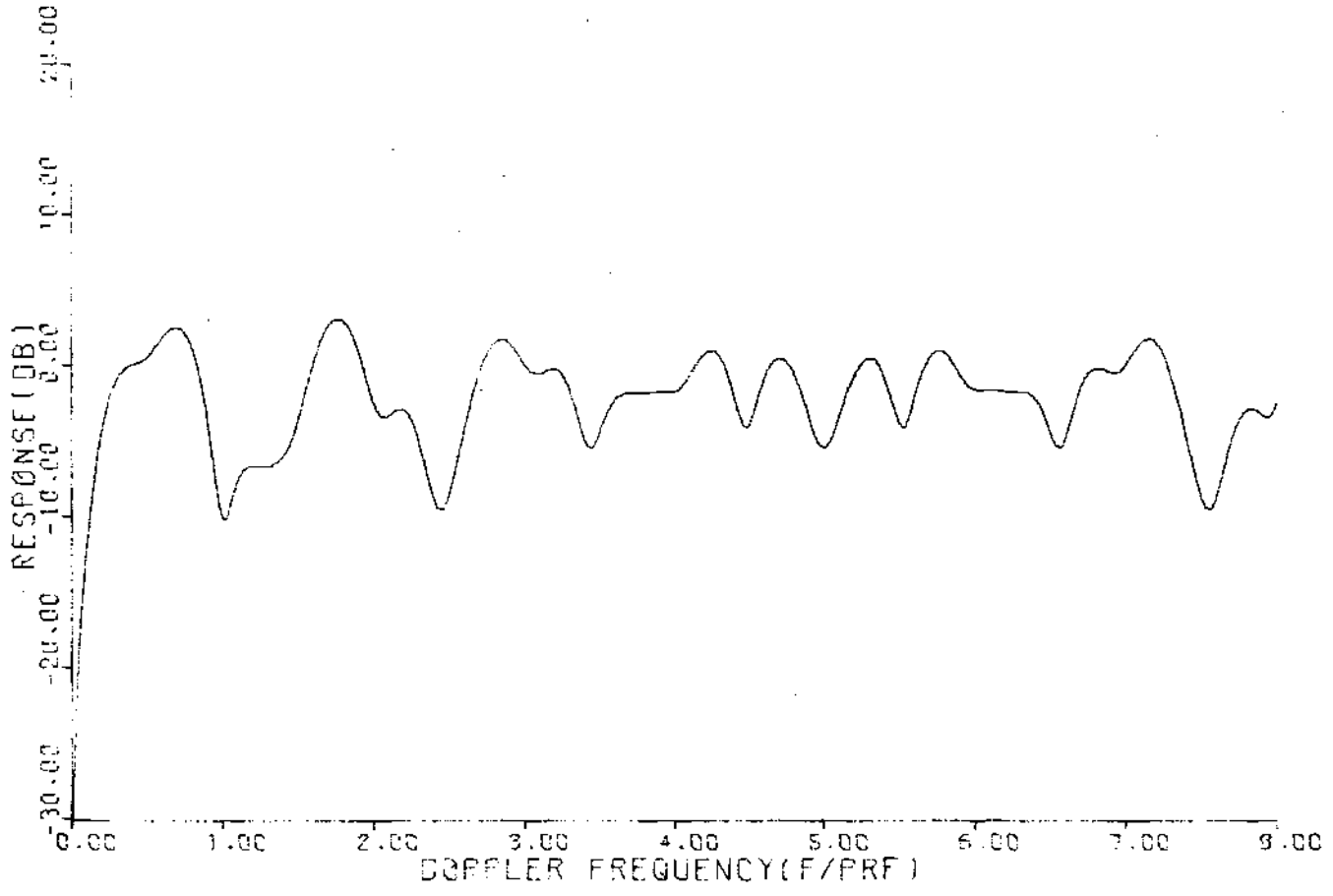


Figure 36. Response of Four Pulse CIP Using Sinusoidal PRF Stagger with ±20% Variation in Interpulse Period. σ = 0.01, I = 30 dB, f' = 8.

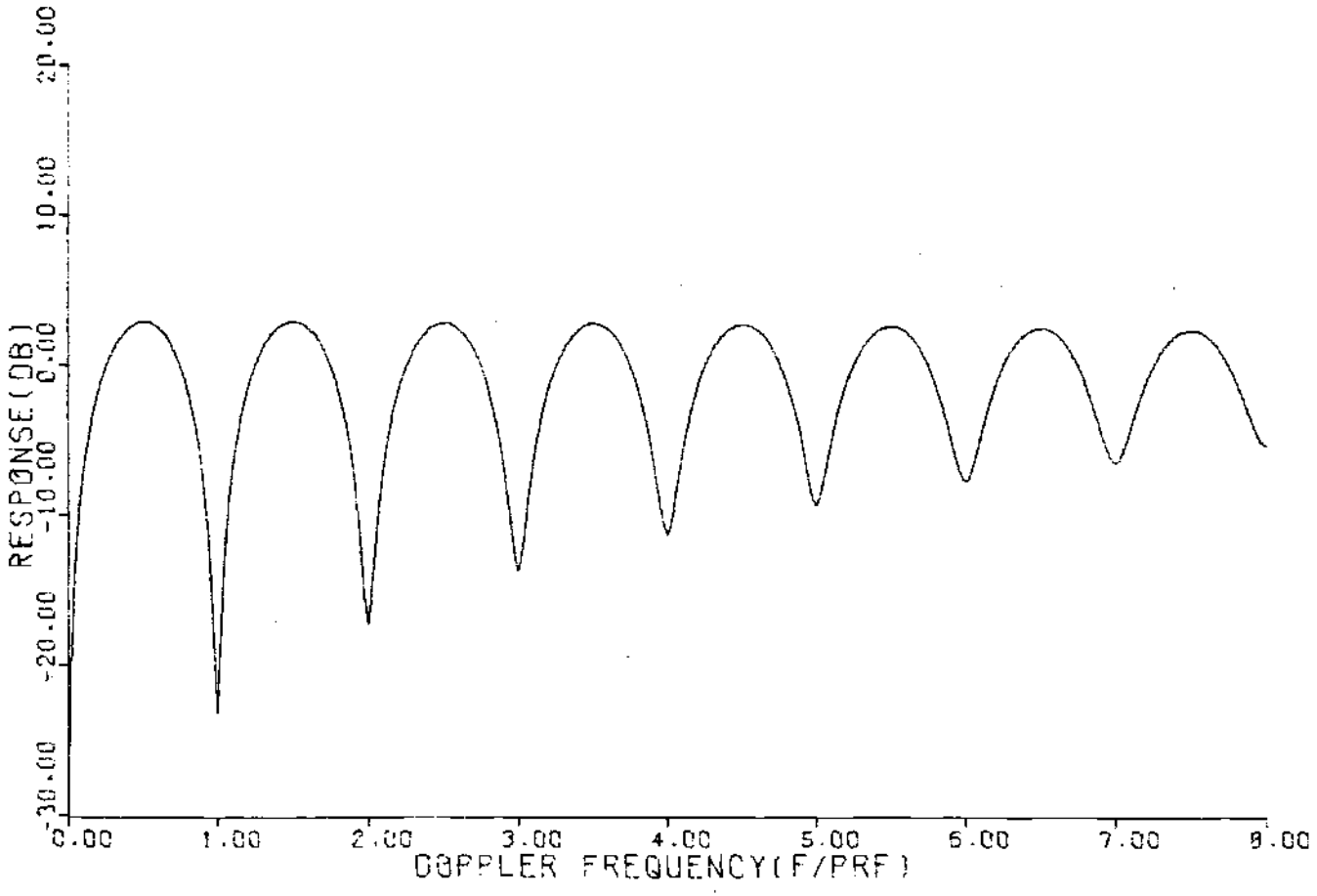


Figure 37. Frequency Response for Ten Pulse Processor of Shrader.

are substantially reduced with the CIP and the top of the CIP is flatter; again the CIP showing a more uniform (and desirable) response, but using only four pulses compared to the ten for Shrader.

Figure 38 shows the frequency response of a processor discussed by Jacomini (a six pulse processor); comparison of this response with the CIP response in Figure 36 illustrates that, in spite of the fact that Jacomini used rather large variations in interpulse period (a totally unrealistic assumption for many cases), the responses are certainly comparable. This is illustrated by the comparison of the cumulative distributions of response for the CIP and Jacomini's processor which is given as Figure 39. One can see the CIP has a lower probability of response below -5 dB than Jacomini's processor, and clusters more closely about the 0 dB point than the processor of Jacomini. Thus, a comparable (or superior) response is obtained using a CIP, while processing four rather than six pulses and using a more reasonable PRF constraint than the processor of Jacomini.

These three comparisons serve to illustrate the superiority of CIP's over previous processors. The CIP's generally; (1) achieve frequency responses which are more uniform than earlier designs, (2) require fewer pulses to be processed, and (3) constrain the PRF stagger sequence to conform to reasonable system requirements. A number of representative CIP designs are presented in the next section.

Some Representative CIP's. The selection of a representative set of designs is rather difficult since each radar system has a unique set of requirements which require separate consideration. The use of

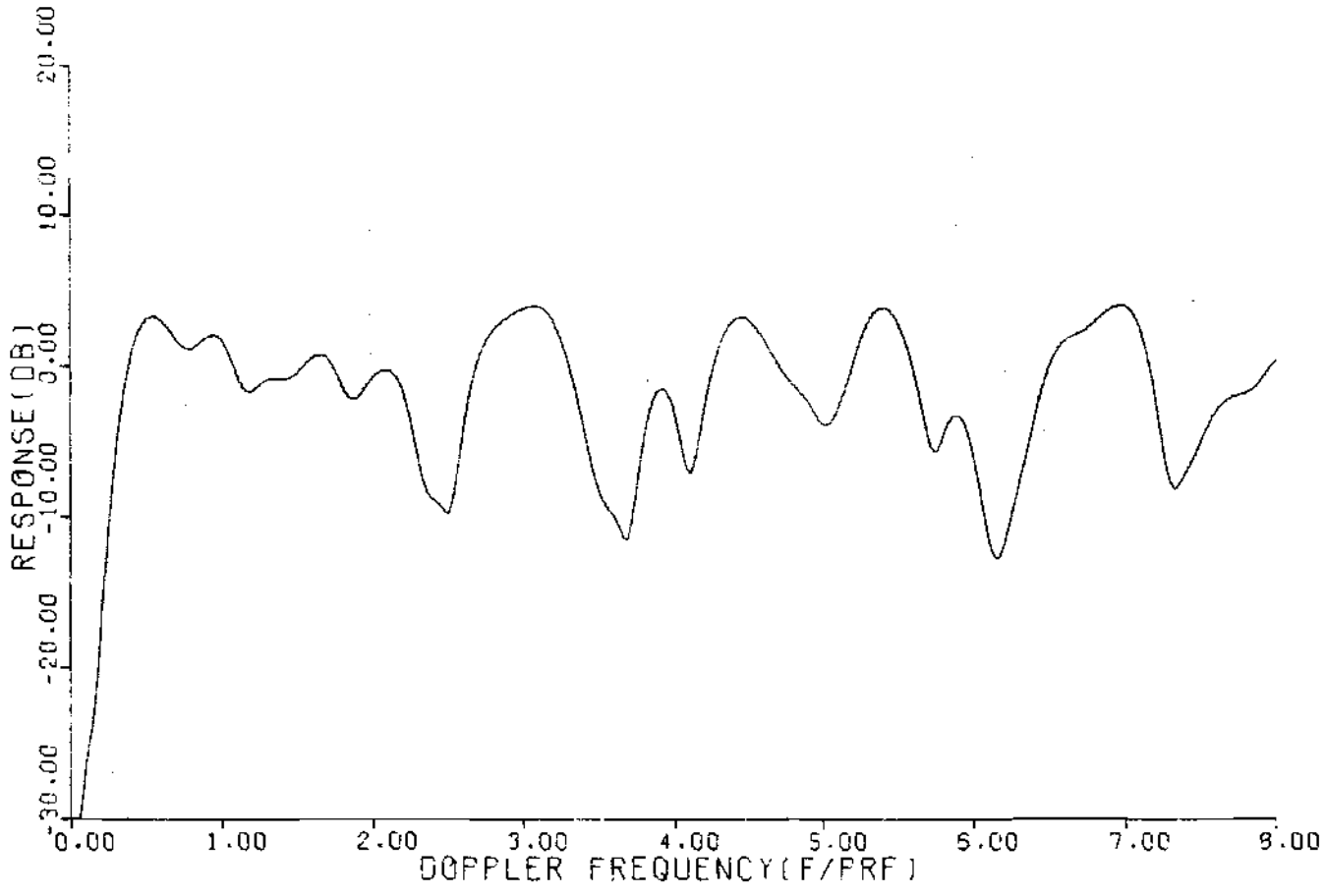


Figure 38. Frequency Response of Six Pulse Processor of Jacomini.

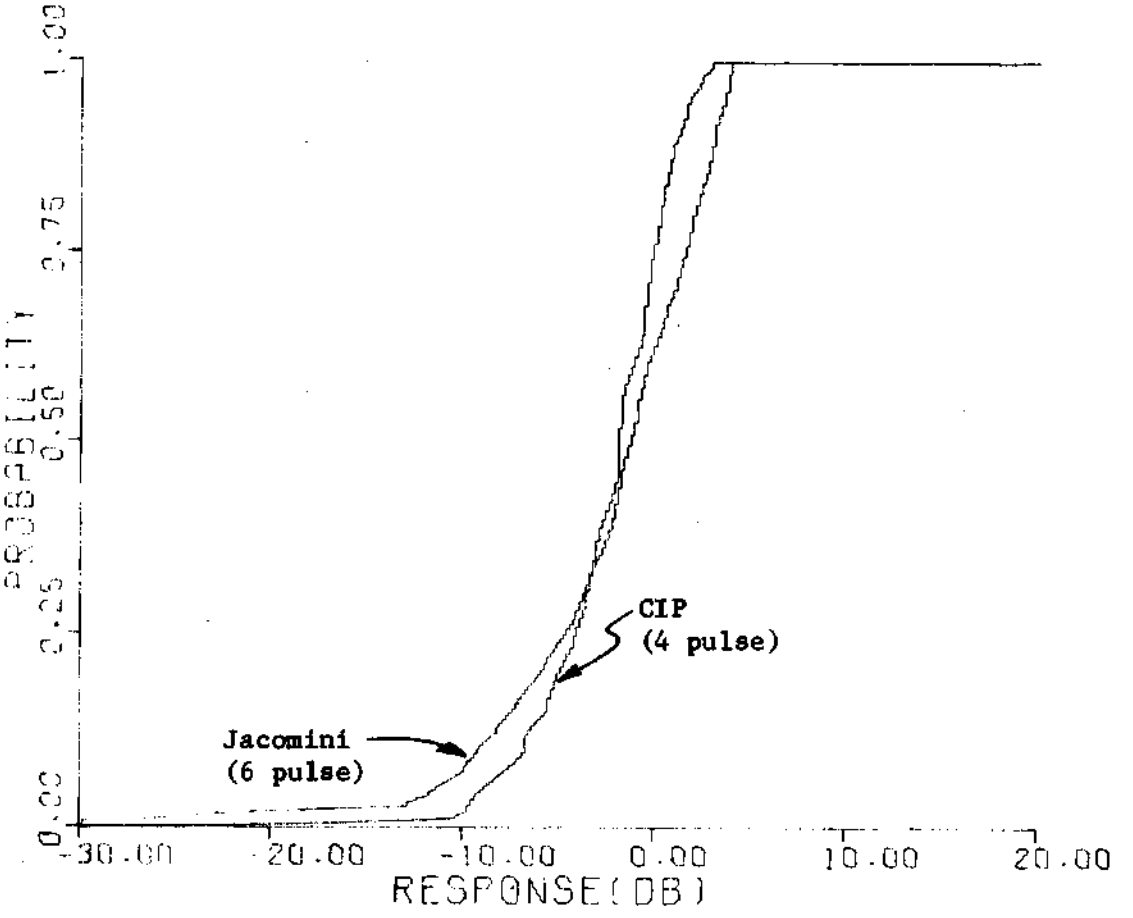


Figure 39. Cumulative Distribution of Response for Four Pulse CIP of Figure 36 and Six Pulse Jacomini Processor of Figure 38.

such normalized values as f and σ help reduce the number of cases to be considered, but many cases remain. A number of designs are discussed in this section; design parameters of $f' = 8$ and $\sigma = 0.01$ for these processors were taken from the representative systems discussed earlier in this chapter. A value of $I = 30$ dB was selected to be consistent with a six-bit analog-to-digital converter. These designs illustrate effects of various parameter choices and to serve as starting points for design of processors which are similar, but which have different design requirements.

The selection of the PRF stagger sequence is first discussed, followed by presentation of a number of representative designs. Influences of changes in maximum and minimum interpulse period spacings, f', σ, and a number of pulses processed are next investigated. Finally, the effects of optimization of the PRF stagger sequence are discussed.

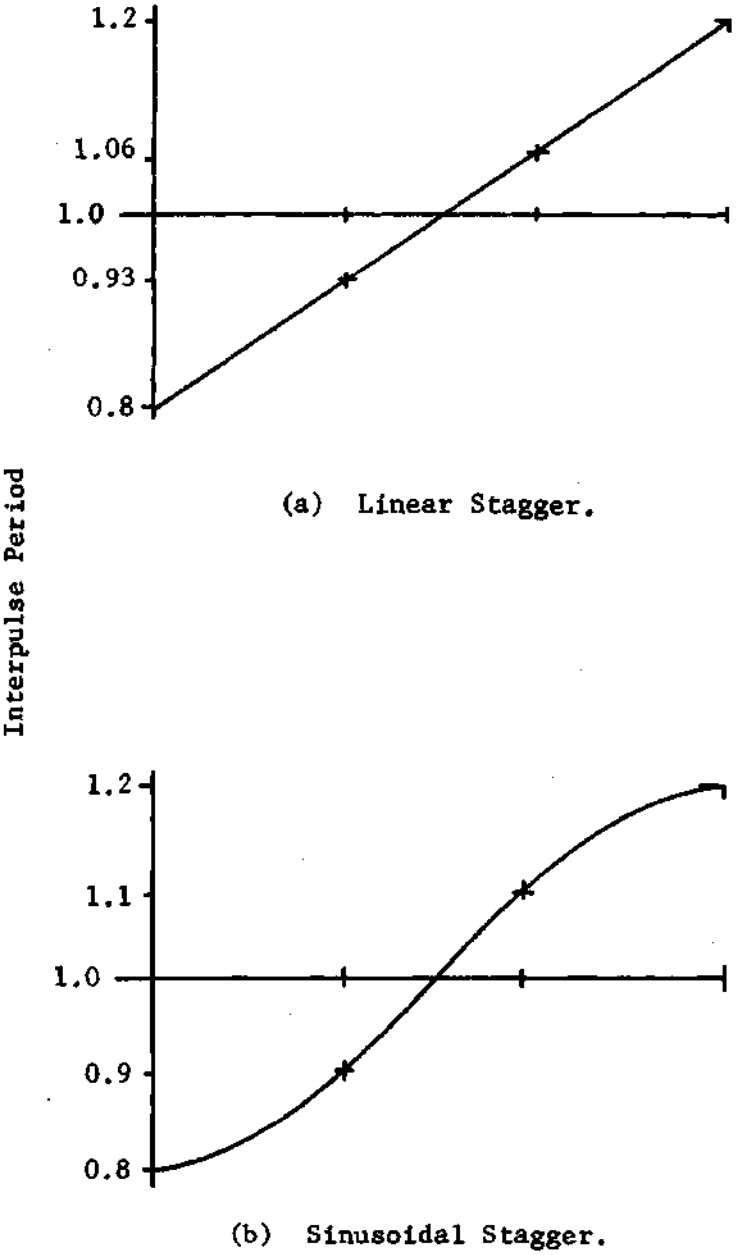
A central concept when specifying CIP's is the need for controlling the interpulse period and the transmitter duty cycle. Both of these objectives may be satisfied by selecting suitable maximum and minimum interpulse periods, and then selecting the remaining pulse spacings to fall within these bounds. However, if the remaining spacings are inappropriately chosen, blind speeds may still exist. These blind speeds may be avoided by selecting spacings which are not simply related to each other; for example, selecting a sinusoidal or a exponential variation of interpulse period, as opposed to a linear variation.

In order to illustrate the above statements, CIP's for both sinusoidal and linear variation in interpulse period were designed.

First, the spacings for linear and sinusoidal variation in interpulse spacing for a $\pm$ 20% variation in interpulse period were selected as shown in Figure 40. Thus, for the four pulse processor, sinusoidal spacing results in a required normalized spacing of 0.8, 0.9, 1.1, and 1.2; corresponding Δ's are 0., -0.2, -0.3, and -0.2. Linear variation requires pulse spacings of 0.8, 0.93, 1.07, and 1.2, resulting in deltas of 0., -0.2, -0.27, and -0.2. Next, CIP processors were designed using these PRF stagger sequences for linear and sinusoidal variations. Response for the linear variations is given in Figure 41 and for the sinusoidal variation in Figure 36. Finally, a comparison of these two responses illustrates the desirability of choosing a sinusoidal variation of interpulse period in order to produce a more uniform response, lacking blind speeds over the frequency range of interest.

The detailed shape of the processor response is a function of bounds on interpulse period variation, f', σ, and number of pulses processed. Table 4 presents four pulse CIP designs for σ = 0.01, I = 30 dB and f' = 8 for a number of extreme variations in interpulse spacing from $\pm$ 10% to $\pm$ 90%. Figure 42 shows the processor response for $\pm$ 10% variation and Figure 43 illustrates the response for the $\pm$ 90% variation. Figure 36 shows the response for the $\pm$ 20% case; comparison of these three responses clearly shows the increased uniformity in response shape and reduction in low frequency null depths obtained as the variation in interpulse period becomes larger.

In order to illustrate dependence of processor response on



(a) Linear Stagger.

(b) Sinusoidal Stagger.

Figure 40. Method for Determining Interpulse Periods for Linear and Sinusoidal PRF Stagger. Maximum Interpulse Period Variation is ± 20% in Each Case.

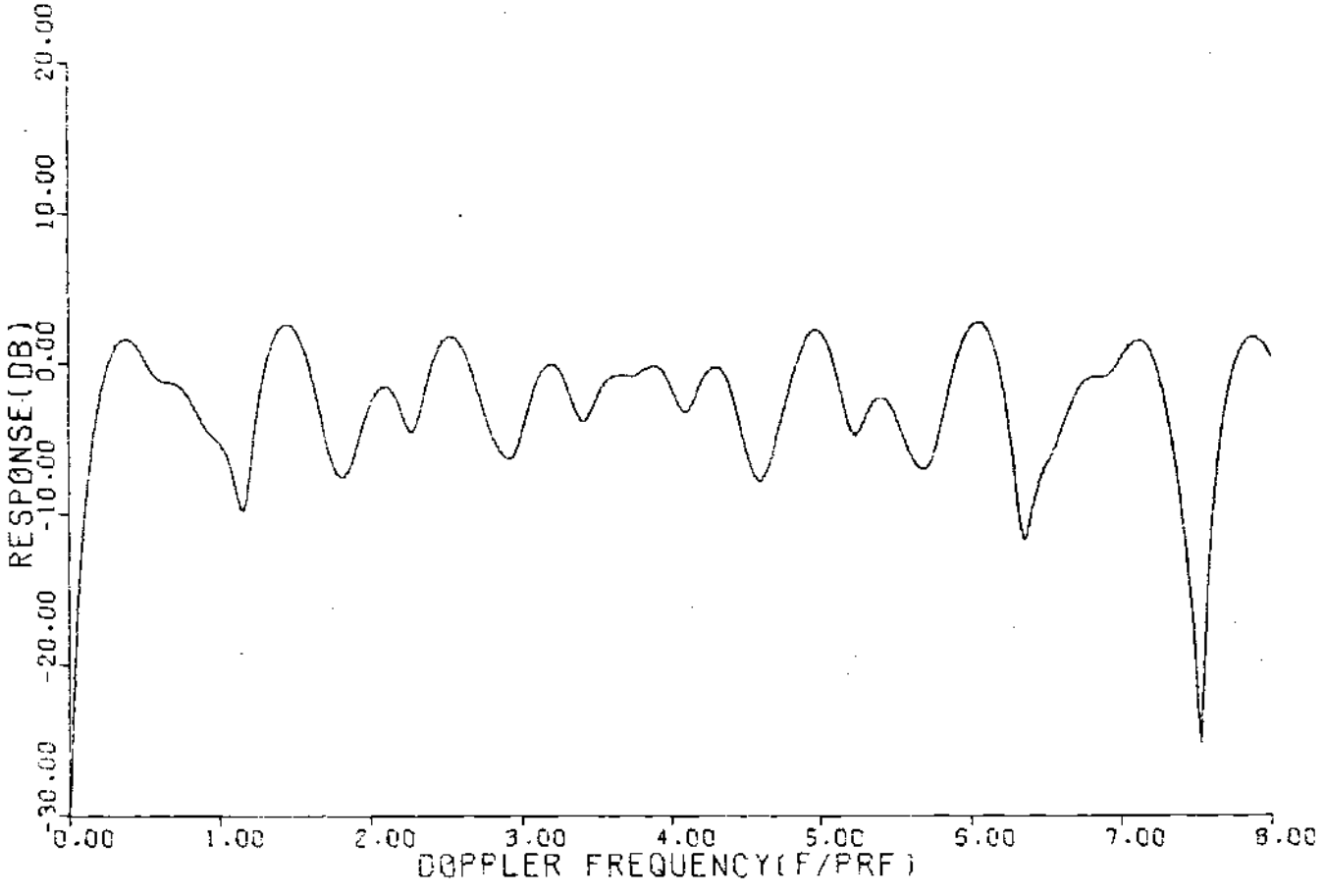


Figure 41. Frequency Response of a Four Pulse CIP Using Linear PRF Stagger with ± 20% Interpulse Period Variation.

Table 4. Representative CIP Parameters for a Range of Variation in Interpulse Period
$\sigma = 0.01$, $f' = 8$, $I = 30$ dB

Variation in Interpulse Period	Weights				PRF Stagger			
	X_1	X_2	X_3	X_4	Δ_1	Δ_2	Δ_3	Δ_4
± 10%	0.3094	-0.7141	0.1391	0.2557	0.00	-0.10	-0.15	-0.10
± 20%	0.3082	-0.7514	0.2591	0.1677	0.00	-0.20	-0.30	-0.20
± 30%	0.3002	-0.7117	0.2005	0.2004	0.00	-0.30	-0.45	-0.30
± 40%	0.3105	-0.7276	0.2338	0.1691	0.00	-0.40	-0.60	-0.40
± 50%	0.3344	-0.7178	0.1838	0.1861	0.00	-0.50	-0.75	-0.50
± 60%	0.2935	-0.7264	0.2548	0.1717	0.00	-0.60	-0.90	-0.60
± 70%	0.3214	-0.7400	0.2399	0.1697	0.00	-0.70	-1.05	-0.70
± 80%	0.3106	-0.7036	0.2318	0.1530	0.00	-0.80	-1.20	-0.80
± 90%	0.4421	-0.6638	0.1054	0.0949	0.00	-0.90	-1.35	- .90

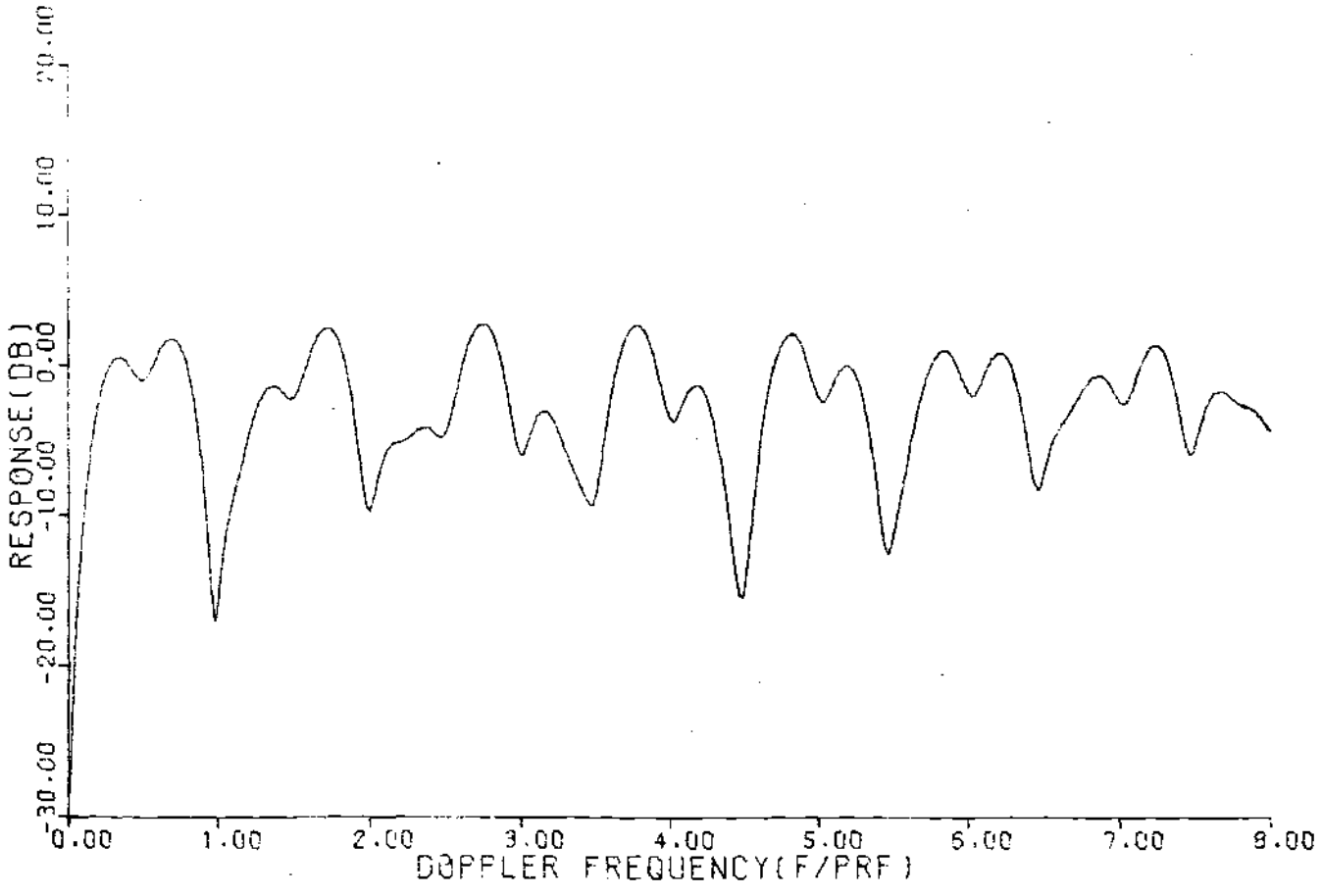


Figure 42. Frequency Response for Four Pulse CIP Using Sinusoidal PRF Stagger with ± 10% Interpulse Period Variation.

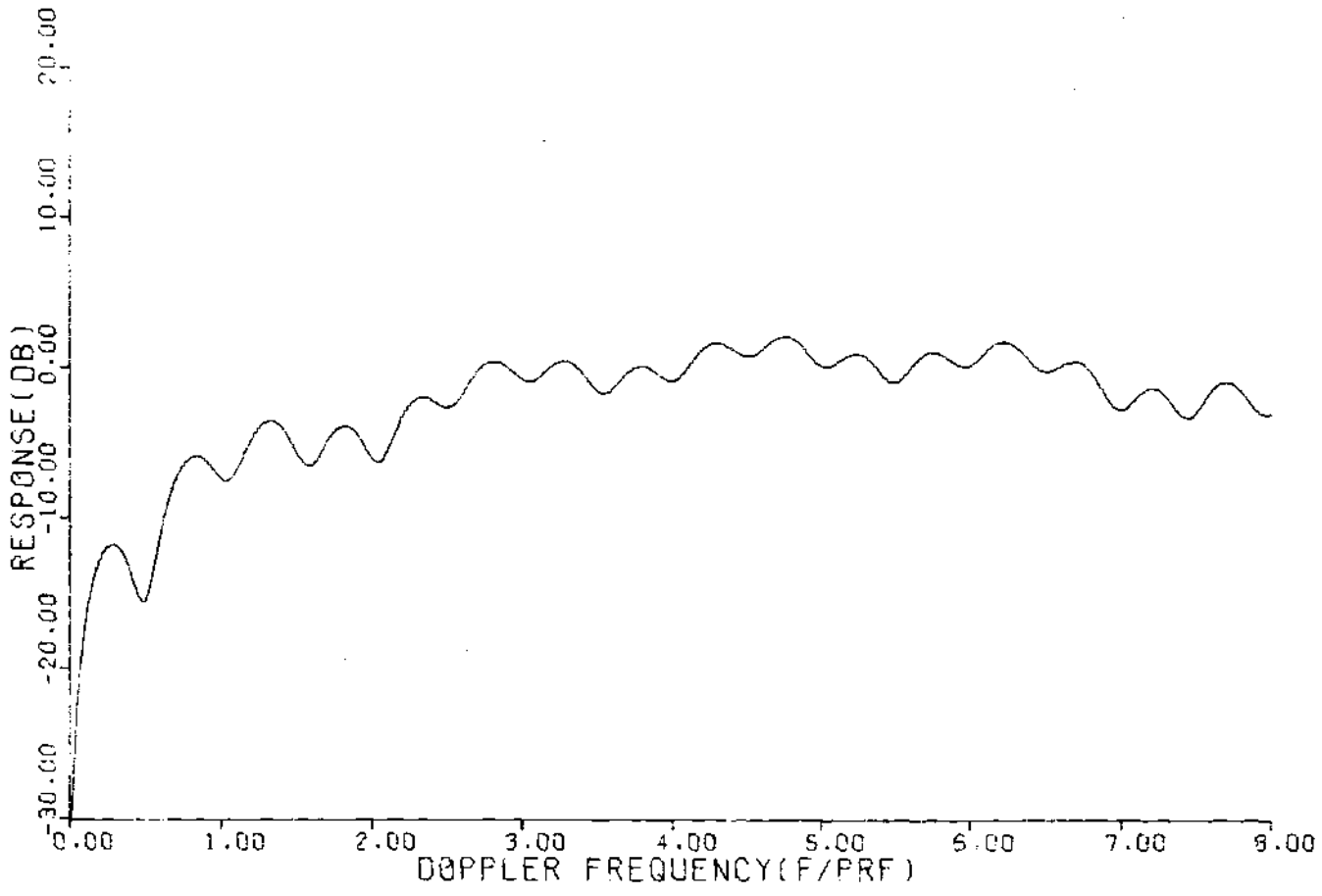


Figure 43. Frequency Response for Four Pulse CIP Using Sinusoidal PRF Stagger with ± 90% Interpulse Period Variation.

values of f', a CIP was calculated for f' = 12, and response of this processor is shown in Figure 44. The response for a similar processor with f' = 8 was given earlier in Figure 36. Comparison of responses for these two processors shows the responses are very similar, but there are some slightly deeper high frequency nulls in Figure 44, indicating desirability of making f' no larger than necessary. These two figures also point out that the shape of the response curve is partially due to the region over which minimization occurs, and partially due to the fact that this particular stagger sequence and optimization criteria were employed.

CIP's have been designed for values of σ = 0.001 and σ = 0.0 in order to investigate sensitivity of processor response to changes in values of σ. The shape of the resulting response for σ = 0.0 is shown in Figure 45. The shape of the response is virtually indistinguishable from that for σ = 0.01 shown in Figure 36, indicating that, while the value of I achieved is a function of clutter spectral width, there is little sensitivity of the shape of the frequency response to the exact shape of the clutter spectra. This further illustrates the statements made earlier in Chapter II, that for small numbers of pulses processed, processor responses are not critically dependent on details of clutter spectral shape.

In order to explore the effects of number of pulses processed on processor performance, CIP's were designed for a $\pm$ 20% variation in interpulse period for three, four, five, and six pulses processed. The response for the three pulse CIP is given in Figure 46, for the

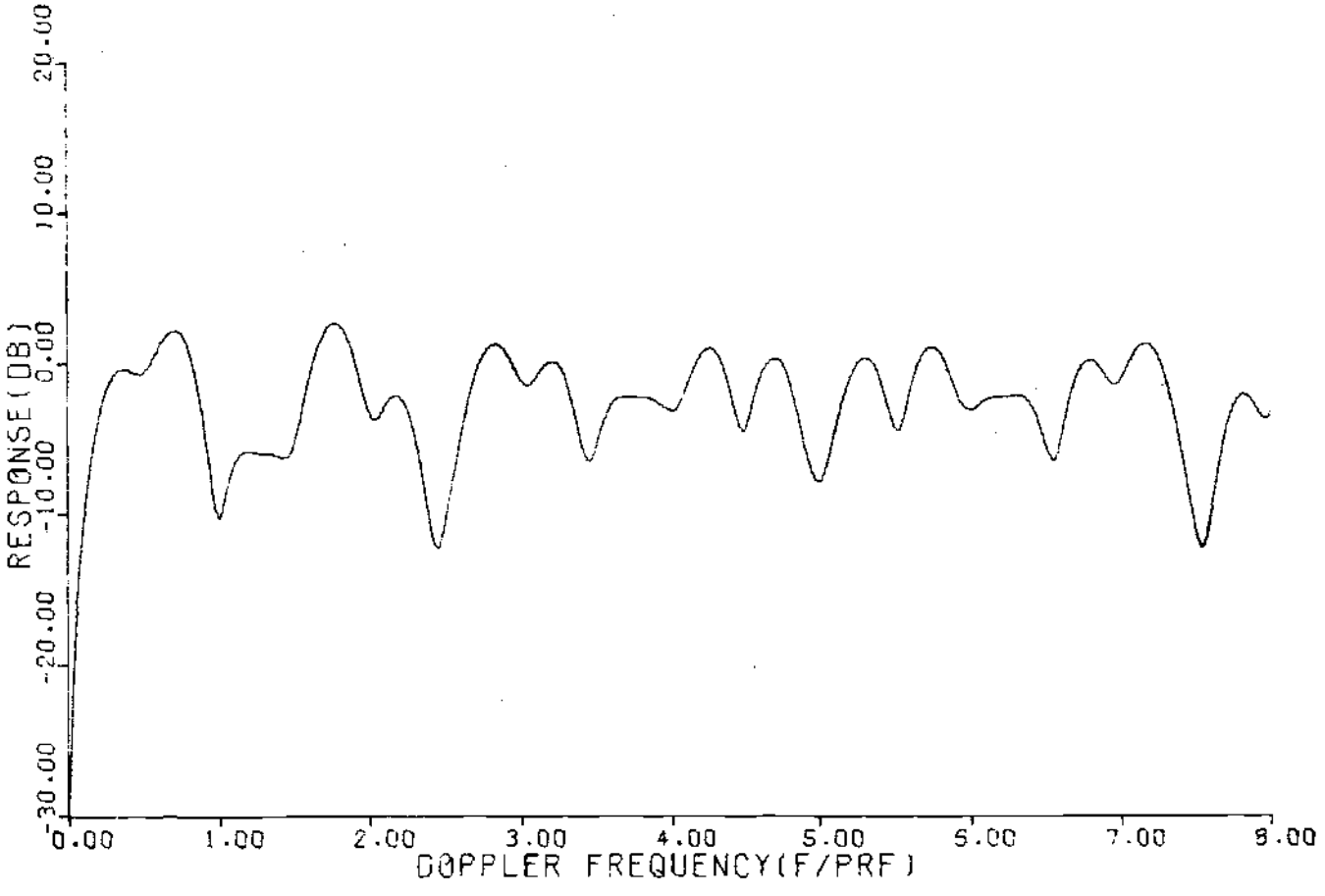


Figure 44. Response of Four Pulse CIP Using Sinusoidal PRF Stagger with $\pm$ 20% Variation in Interpulse Period. σ = 0.01, I = 30 dB, $\bar{f}'$ = 12.

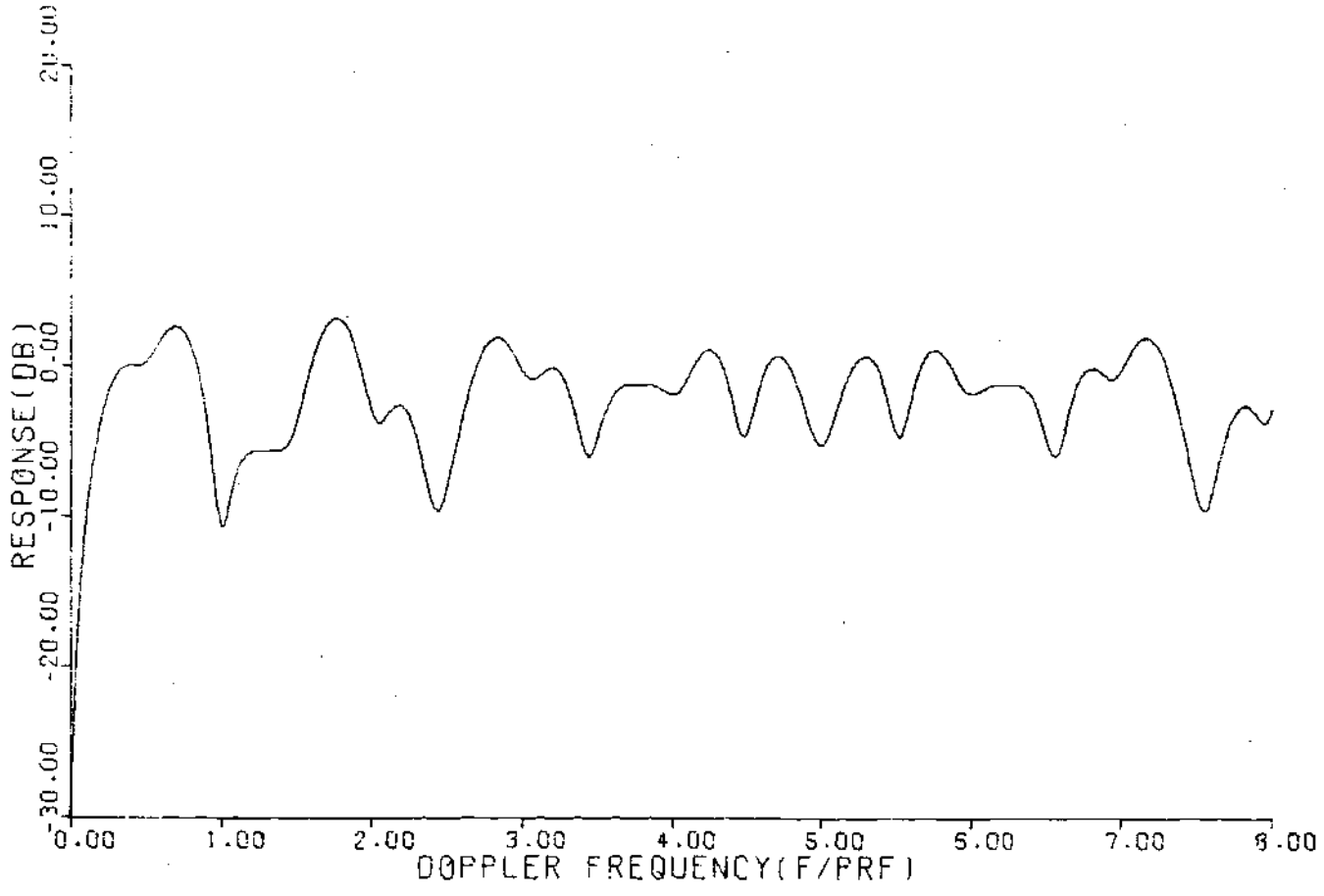


Figure 45. Response of Four Pulse CIP Using Sinusoidal PRF Stagger with ± 20% Interpulse Period Variation. σ = 0.0, I = 30 dB.

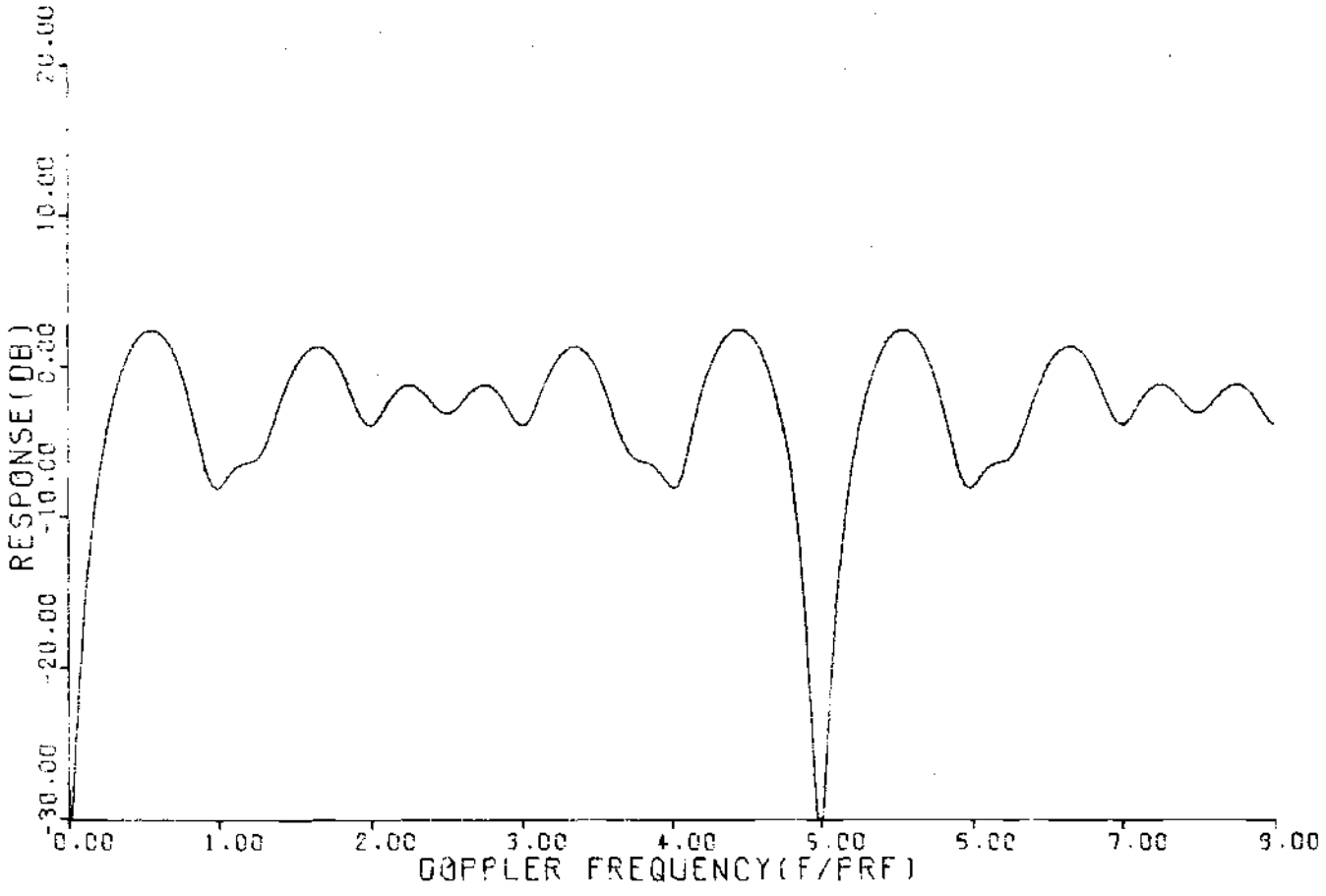


Figure 46. Frequency Response for Three Pulse CIP with ± 20% Interpulse Period Variation.

five pulse CIP in Figure 47, and the six pulse processor in Figure 48. The response of the four pulse CIP is given in Figure 36. The case for three pulses shows a blind speed, due to the fact that the sinusoidal interpulse period variation and the linear interpulse period variation degenerate to the same case. The case for five pulses processed is rather similar to the four pulse response shown in Figure 36, which is reflected in the fact tha $X_5 = 0.0763$. The small value for X_5 indicates that improvement due to inclusion of this additional term is rather small. The response of the six pulse processor shown in Figure 48 shows somewhat increased uniformity of response when compared with processors having fewer numbers of pulses. This is pointed out in Figure 49 which compares the cumulative distributions of response for the six pulse CIP (response given in Figure 48) and the four pulse CIP (response given in Figure 36). The six pulse CIP has slightly reduced probability of low amplitude responses and clusters more closely about 0 dB, thus more closely approaching the ideal step function occurring at 0 dB.

The local optimization of the PRF stagger sequence for the processors given in Table 4 was then carried out; the resulting designs are given in Table 5. The processor response for the $\pm$ 20% nominal variation in interpulse period is shown in Figure 50. Comparison of responses in Figures 50 and 36 shows the detailed improvement in processor response shape, principally over the region $5 < f < 7$, obtained by optimization of PRF stagger.

The representative processors discussed in the preceding

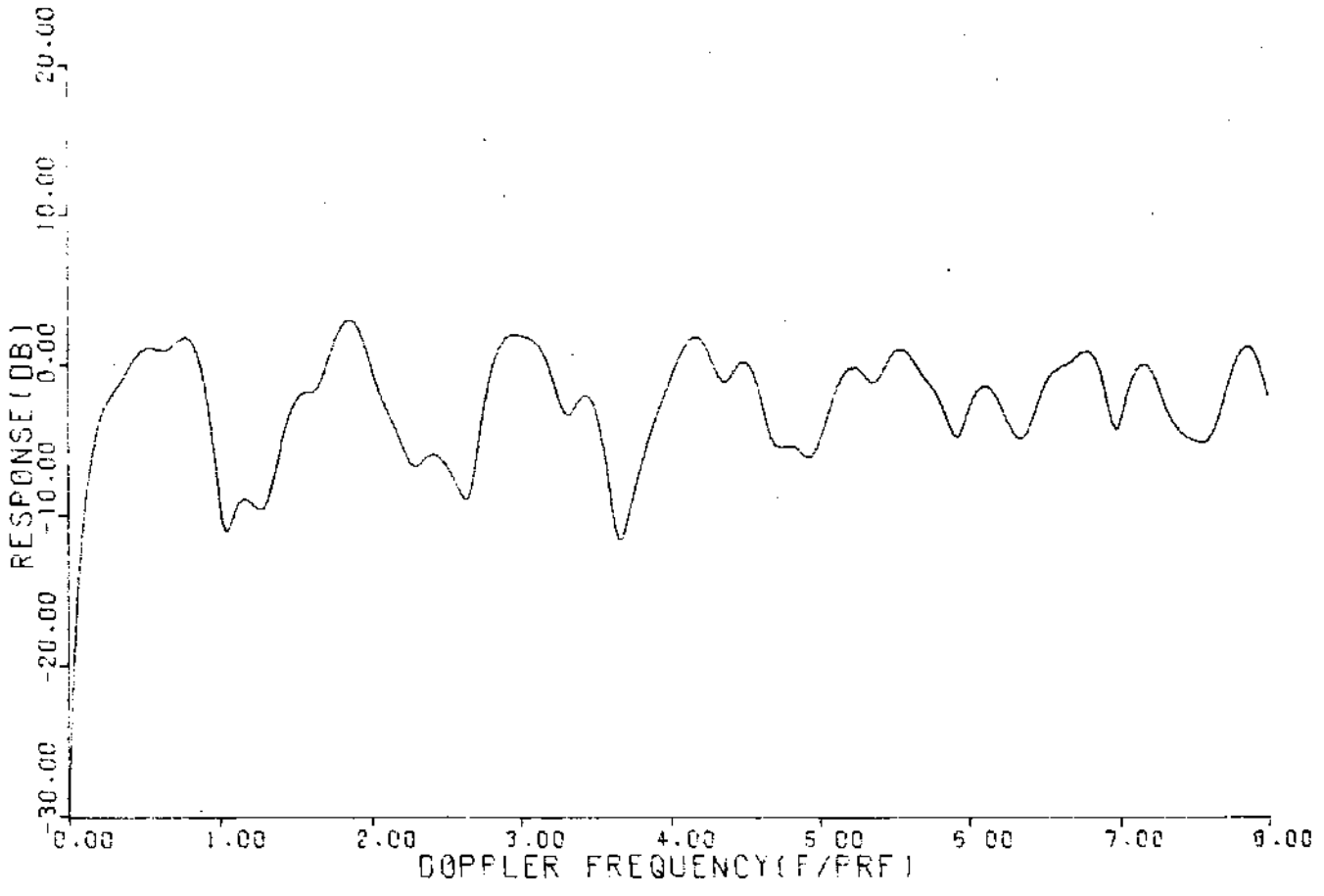


Figure 47. Frequency Response of Five Pulse CIP Using Sinusoidal PRF Stagger with ± 20% Interpulse Period Variation.

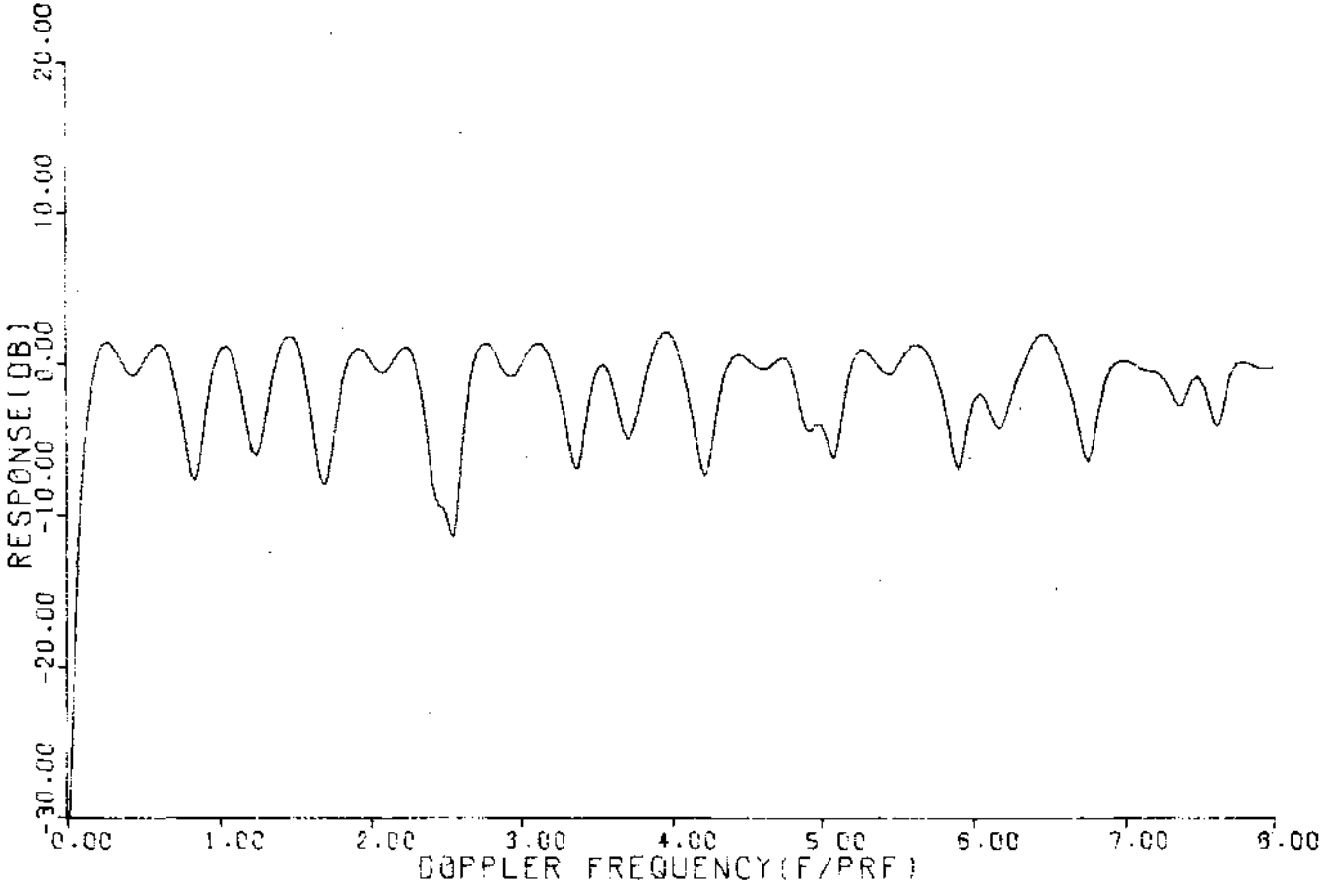


Figure 48. Response of Six Pulse CIP Using Sinusoidal PRF Stagger with ± 20% Variation in Interpulse Period.

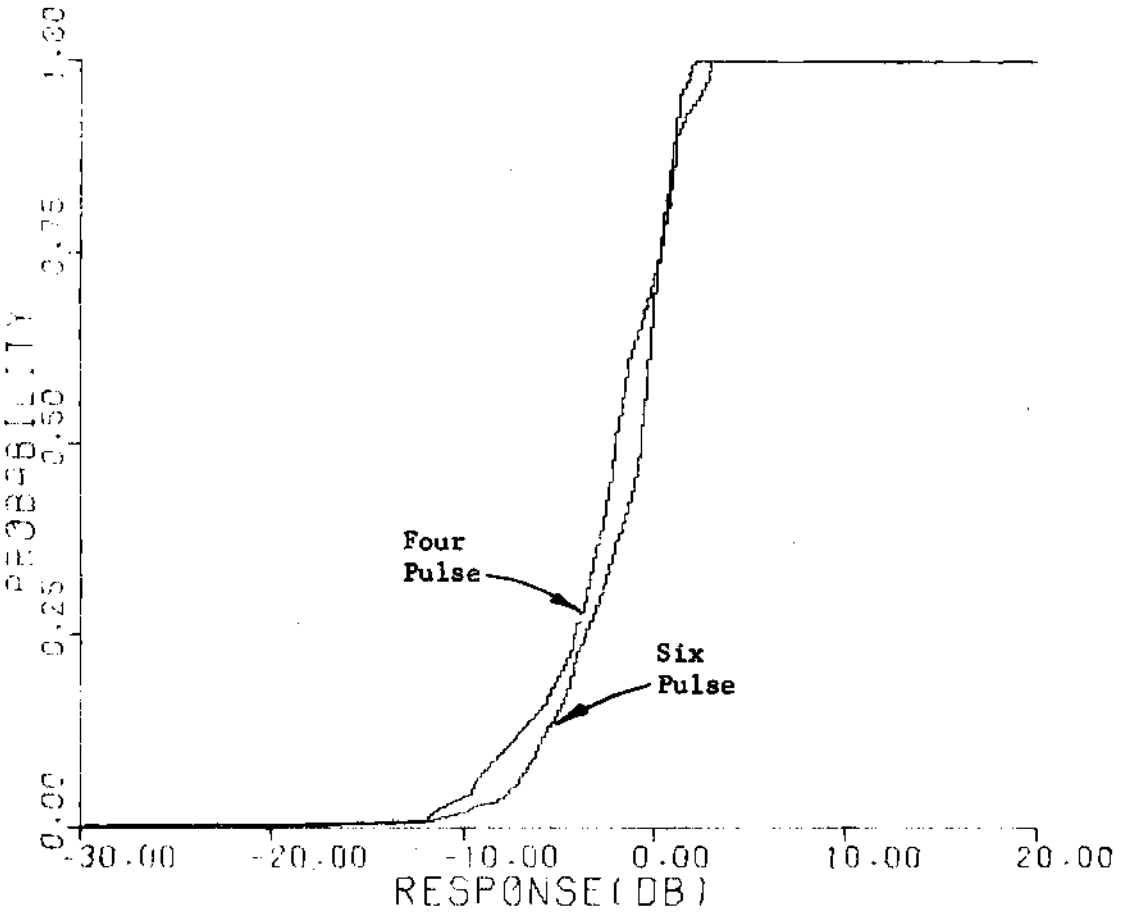


Figure 49. Cumulative Distribution of Response for Four and Six Pulse CIP's.

Table 5. Representative CIP Parameters for Processors Optimized Using Weights and PRF Stagger
Nominal Interpulse Period Variations ± 10% - ± 90%
$\sigma = 0.01$, $f' = 8$, $I = 30$ dB

Nominal Variation of Interpulse Period	Weights				PRF Stagger			
	X_1	X_2	X_3	X_4	Δ_1	Δ_2	Δ_3	Δ_4
± 10%	0.3094	-0.7141	0.1391	0.2557	0.0540	-0.1420	-0.1741	-0.0879
± 20%	0.3073	-0.7514	0.2590	0.1689	0.0275	-0.1911	-0.3223	-0.2142
± 30%	0.3002	-0.7117	0.2005	0.2004	0.0067	-0.3208	-0.4403	-0.2957
± 40%	0.3105	-0.7276	0.2338	0.1691	-0.0084	-0.4055	-0.5860	-0.4001
± 50%	0.3344	-0.7178	0.1838	0.1861	-0.1271	-0.7809	-0.6228	-0.5468
± 60%	0.2935	-0.7264	0.2548	0.1717	0.0243	-0.6198	-0.9121	-0.5923
± 70%	0.3214	-0.7400	0.2399	0.1697	-0.0298	-0.7272	-1.1390	-0.5540
± 80%	0.3106	-0.7036	0.2318	0.1530	-0.3221	-0.7516	-1.6200	-0.7506
± 90%	0.4421	-0.6638	0.1054	0.0949	-0.0103	-0.9120	-1.3340	-0.8942

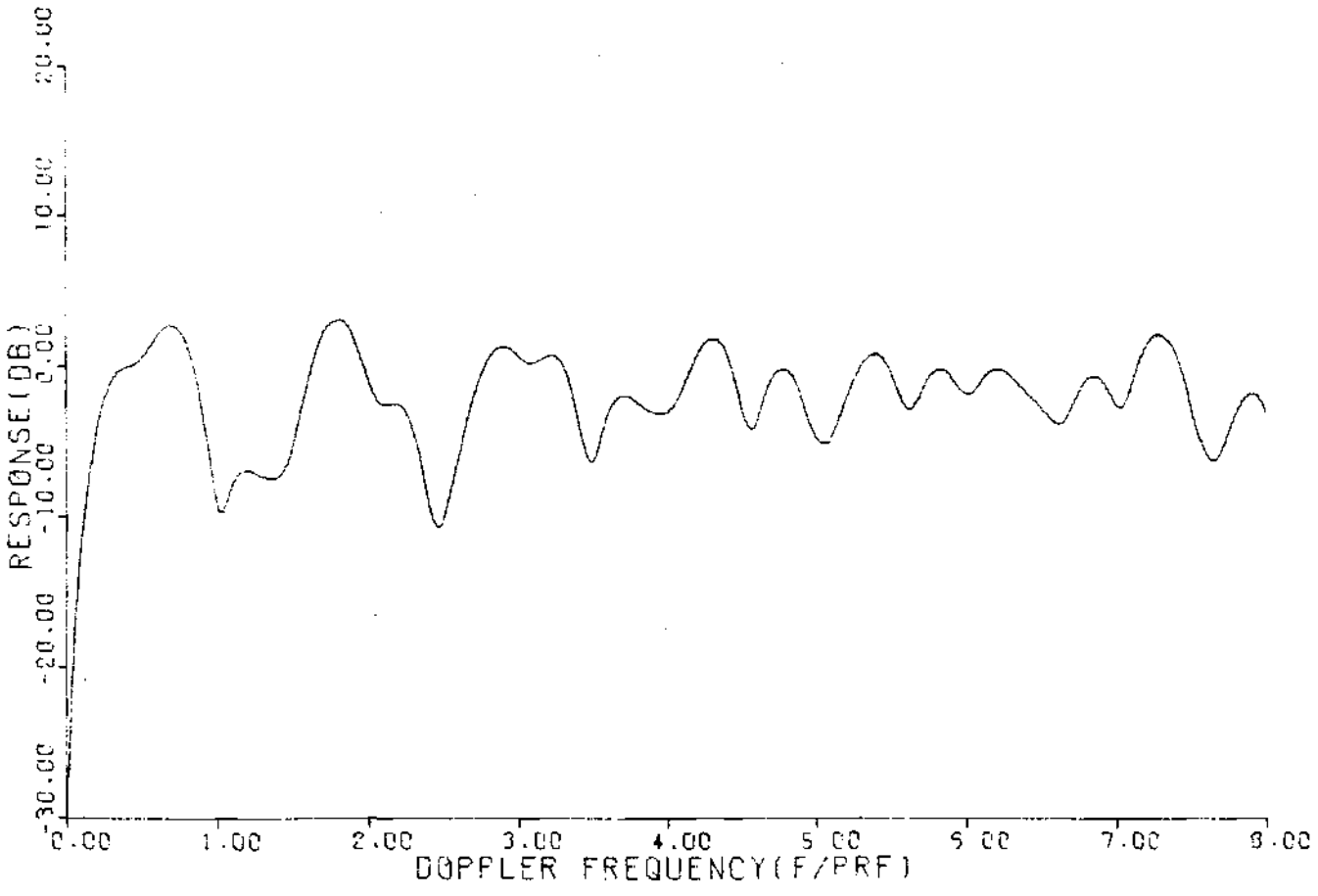


Figure 50. Response of Four Pulse CIP Optimized with Both Weights and Stagger for a Nominal ± 20% Variation in Interpulse Period.

paragraphs illustrate the results which are achieved with some representative design parameters, and effects of changes of these parameters on processor performance. Equally important is the fact that these representative designs provide a starting point for the designer who wishes to develop similar processors for differing sets of design requirements.

CHAPTER IV

CONCLUSIONS AND RECOMMENDATIONS

The research reported in this dissertation resulted in design procedures for improved MTI processors for radar systems utilizing either staggered or unstaggered PRF's. These design procedures utilize the new flexibility and capability of modern step-scan radar systems employing digital signal processing in order to specify MTI processors of substantially improved performance.

Three classes of processors for unstaggered PRF systems have been developed: the Equal Ripple Processor, the Maximally Flat Processor, and the Constrained Improvement Processor. The first uses simplex methods for a solution, the second involves solution of a set of simultaneous linear equations, while the third makes use of Lagrange multiplier techniques. Each of these processors offers considerable improvement in uniformity of response when compared with earlier designs.

Two classes of staggered PRF processors have been developed; the Maximum Improvement Processors (MIP's), and the Constrained Improvement Processors (CIP's). Lagrange multiplier methods are used to design the processors, and the Fletcher-Powell method to arrive at a solution. The MIP's maximize I while keeping the average response equal to one. Examination of the resulting responses shows significant increases in I over previous designs, with no degradation (and in some cases an improvement) in uniformity of Doppler frequency response. The CIP's limit I to some desirable (and achievable) value and, subject to this

constraint, minimize the mean square deviation of processor response from unity with changes in target Doppler frequency. The design procedure involves selection of both processor weight functions and interpulse periods.

Representative CIP's are compared with earlier processors, and a considerable improvement in uniformity of frequency response is achieved with a CIP. A complete absence of blind speeds may often be achieved over the desired range of target Doppler frequencies, and fluctuations in processor response with changes in target Doppler frequency are considerably reduced over previous designs. A number of representative processor parameters are tabulated, and effects on processor performance of such variables as clutter spectral width, number of pulses processed, and maximum and minimum interpulse spacing are considered.

Conclusions

A number of significant facts concerning the design of improved MTI processors have been pointed out during this research.

First, previous MTI processors have exhibited a number of undesirable features, principally significant variations in processor response with changes in target radial velocity and the need to process a large number of received pulses from the target.

Second, practical MTI processor designs can be specified which emphasize both achieving the required value of MTI improvement and minimizing fluctuations in processor response with changes in target Doppler frequency.

Third, these improved processor designs offer substantial improvements in uniformity of response when compared with conventional processor designs.

Fourth, a number of factors, such as clutter spectral width, range of target velocities of interest, allowable minimum and maximum interpulse periods, and number of pulses processed all effect the shape of the processor responses. Uniformity of processor response generally improves as the desired range of target velocities and clutter spectral width decrease, and as the number of pulses processed and the allowable range of interpulse periods increase.

Fifth, the designs developed are useful, not only as guidelines for the system designer, but also as the starting point for development of new designs for the same types of processors having different sets of design requirements.

Recommendations

During the course of this research, it has become obvious that performance of many systems is limited by the quantization errors in the analog-to-digital conversion process. Improvements in speed and accuracy of analog-to-digital converters would substantially benefit system performance.

The implementation of these improved processors is a non-trivial problem. Computation algorithms and hardware implementation approaches require considerable sophistication in order to minimize cost, complexity, and processing time. The method of interfacing the processor output data with the central control and computational system

is also a rather difficult problem.

The extension of the results of Wainstein and Zubakov to determine unstructured processors for more than two received pulses for both the staggered and unstaggered case would be a significant contribution to the MTI signal processing field.

The extension of these results to include both the use of staggered PRF and frequency agility for blind speed reduction would considerably enhance performance of radars which must use frequency agility for other purposes, such as glint or multipath reduction. However, the meaningful specification of the additional variable of frequency, with all of its other constraints, is a formidable task.

BIBLIOGRAPHY

1. E. J. Barlow, "Doppler Radar," Proceedings of the IRE, Vol. 37, pp 340-355, April 1949.

2. F. E. Nathanson, Radar Design Principles, p 274, McGraw-Hill Book Co., 1969.

3. D. E. Kerr (ed), Propagation of Short Radio Waves, Vol. 13, Radiation Laboratory Series, p 585, Boston Technical Publishers Edition, 1964.

4. D. K. Barton and H. R. Ward, Handbook of Radar Measurement, p 24, Prentice-Hall, Inc., Englewood Cliffs, N. J., 1969.

5. M. I. Skolnik (editor), Radar Handbook, Chapter 17 by N. W. Shrader, pp 38-45, McGraw-Hill Book Co., New York, N. Y., 1970.

6. W. Fishbein, S. W. Graveline and D. E. Rittenbach, "Clutter Attenuation Analysis," Technical Report ECOM-2808, U.S. Army Electronics Command, Ft. Monmouth, N. J., March 1967, AD 665 352.

7. G. W. Ewell, N. T. Alexander and E. L. Tomberlin, "Investigation of Target Tracking Errors in Monopulse Radars," Final Technical Report on Contract DAAH01-71-C-1192, July 1972.

8. D. O. North, An Analysis of the Factors which Determine the Signal/Noise Discrimination in Radar, Technical Report PtR-6C, RCA Laboratories, Princeton, N. J., June 25, 1943.

9. J. Van Vleck and D. Middleton, "A Theoretical Comparison of the Visual, Aural, and Meter Reception of Pulsed Signals in the Presence of Noise," Journal of Applied Physics, Vol. 17, pp 940-971, November 1946.

10. H. L. Van Trees, Detection, Estimation and Modulation Theory, Part I, p 249, John Wiley and Sons, Inc., New York, N. Y., 1968.

11. T. S. George, Report No. 159, Philco Corp. Research Division.

12. B. M. Dwork, "Detection of a Pulse Superimposed on Fluctuation Noise," Proceedings of the IRE, Vol. 38, pp 771-774, July 1950.

13. H. Urkowitz, "Filters for Detection of Small Radar Signals in Clutter," Journal of Applied Physics, Vol. 24, No. 8, pp 1024-1031, August 1953.

14. A. W. Rihaczek, "Optimum Filters for Signal Detection in Clutter," IEEE Transactions on Aerospace and Electronics Systems, Vol. AES-1, No. 3, pp 297-299, December 1965.

15. D. F. DeLong, Jr., and E. M. Hofstetter, "The Design of Clutter-Resistant Radar Waveforms with Limited Dynamic Range," IEEE Transactions on Information Theory, Vol. IT-15, No. 3, pp 376-385, May 1969.

16. D. F. DeLong, Jr., and E. M. Hofstetter, "On the Design of Optimum Radar Waveforms for Clutter Rejection," IEEE Transactions on Information Theory, Vol. IT-13, No. 3, July 1967.

17. E. C. Westerfeld, R. H. Prager, and J. L. Stewart, "Processing Gains Against Reverberation (Clutter) Using Matched Filters," IEEE Transactions on Information Theory, Vol. IT-6, pp 342-348, June 1960.

18. H. L. Van Trees, "Optimum Signal Design and Processing for Reverberation Limited Environments," IEEE Transactions on Military Electronics, Vol. MIL-9, pp 212-229, July 1965.

19. L. J. Spafford, "Optimum Radar Signal Processing in Clutter," IEEE Transactions on Information Theory, Vol. IT-14, No. 6, pp 734-743, September 1968.

20. L. J. Spafford, Optimum Radar Signal Processing in Clutter, Ph.D. dissertation, Polytechnic Institute of Brooklyn, Brooklyn, N. Y., June 1967.

21. C. A. Stutt and L. J. Spafford, "A 'Best' Mismatched Filter Response for Radar Clutter Discrimination," IEEE Transactions on Information Theory, Vol. IT-14, No. 2, pp 280-287, March 1968.

22. W. D. Rummler, "Clutter Suppression by Complex Weighing of Coherent Pulse Trains," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-2, No. 6, pp 689-699, November 1966.

23. H. L. Van Trees, Detection, Estimation and Modulation Theory, Vol. 3, p 278, John Wiley and Sons, Inc., New York, N. Y., 1971.

24. L. A. Wainstein and V. D. Zubakov, Extraction of Signals from Noise, Chapter 6, Prentice-Hall International, London, 1962.

25. Reference 24, Section 6.2.

26. I. Selin, "Detection of Coherent Radar Returns of Unknown Doppler Shift, " IEEE Transactions on Information Theory, Vol. IT-11, pp 396-400, July 1965.

27. L. E. Brennan, I. S. Reed, and W. Sollfrey, "A Comparison of Average Likelihood and Maximum Likelihood Ratio Tests for Detecting Radar Targets of Unknown Doppler Frequency," IEEE Transactions on Information Theory, Vol. IT-10, pp 152-159, April 1965.

28. J. Capon, "Optimum Weighting Functions for the Detection of Sampled Signals in Noise," IEEE Transactions on Information Theory, Vol. IT-10, pp 152-159, April 1964.

29. H. E. Kallman, "Transversal Filters," Proceedings of the IRE, pp 302-310, July 1940.

30. L. R. Rabiner and R. W. Schafer, "Recursive and Nonrecursive Realizations of Digital Filters Designed by Frequency Sampling Techniques," IEEE Transactions on Audio and Electroacoustics, Vol. Au-19, No. 3, September 1971.

31. A. G. Deczky, "Synthesis of Recursive Digital Filters Using the Minimum p-Error Criterion," IEEE Transactions on Audio and Electroacoustics, Vol. AU-20, No. 4, pp 257-263, October 1972.

32. B. Gold and C. M. Rader, Digital Processing of Signals, Chapter 3, McGraw Hill Book Company, New York, N. Y., 1969.

33. R. M. Golden, Parametric Design of Digital Filters, Course Notes, Technology Service Corp., January 1970.

34. L. R. Rabiner, B. Gold, and C A. McGonegal, "An Approach to the Approximation Problem for Nonrecursive Digital Filters," IEEE Transactions on Audio and Electroacoustics, Vol. 18, No. 2, pp 83-106, June 1970.

35. D. W. Tufts, D W. Rorabacher, and W. E. Moser, "Designing Simple, Effective Digital Filters," IEEE Transactions on Audio and Electroacoustics, Vol. AU-18, No. 2, pp 142-158, June 1970.

36. H. D. Helms, "Digital Filters with Equiripple or Minimax Response," IEEE Transactions on Audio and Electroacoustics, Vol. AU-19, No. 1, pp 87-93, March 1971.

37. A. A. G. Requicha and H. G. Voelcker, "Design of Nonrecursive Filters by Specification of Frequency Domain Zeros," IEEE Transactions on Audio and Electroacoustics, Vol. AU-18, No. 4, pp 464-470, December 1970.

38. B. Gold and K. L. Jordan, Jr., "A Direct Search Procedure for Designing Finite Duration Impulse Response Filters," IEEE Transactions on Audio and Electroacoustics, Vol. AU-17, No. 1, pp 36-86, March 1969.

39. G. C. O'Leary, "Nonrecursive Digital Filtering Using Cascade Fast Fourier Transformers," IEEE Transactions on Audio and Electroacoustics, Vol. AU-18, No. 2, pp 177-183, June 1970.

40. L. R. Rabiner, "Linear Program Design of Digital Filters," 1972 IEEE Convention Record, paper 6H.2, pp 336-337, March 1972.

41. R. Fletcher and D. Burlage, Personal Communication, Redstone Arsenal Alabama, July 1972.

42. O. J. Jacomini, "Optimum Symmetrical Weighing Factors for a Video MTI Radar," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-7, No. 1, pp 204-209, January 1971.

43. R. Roy and O. Lowenschuss, "Design of MTI Detection Filters with Non-Uniform Interpulse Periods," IEEE Transactions on Circuit Theory, Vol. CT-17, No. 4, pp 604-612, November 1970.

44. A. W. Rihaczek, "A Systematic Approach to Blind-Speed Elimination," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-9, No. 6, pp 940-947, November 1973.

45. P. J. A. Prinsen,"Elimination of Blind Velocities of MTI Radar by Modulating the Interpulse Period," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-9, No. 5, pp 714-724, September 1973.

46. L. E. Brennan and I. S. Reed, "Optimum Processing of Unequally Spaced Radar Pulse Trains for Clutter Rejection," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-4, No. 3, pp 474-477, May 1968.

47. Reference 5, page 17-40.

48. E. C. Waters, Jr., "Apparatus and Method for Improving the Velocity Response of an MTI Radar by Sinusoidally Varying the Interpulse Period," U.S. Patent 3,588,898, June 28, 1971.

49. J. W. Taylor, "MTI Radar System Utilizing Unique Patterns of Interpulse Period Choices to Simplify Weighting Coefficients for Individual Echo Pulses," U.S. Patent 3,566,402, February 23, 1971.

50. J. W. Taylor, "Apparatus for Flexibly Weighting Received Echos in a Moving Target Indicator Radar," U.S. Patent 5,560,972, February 2, 1971.

51. O. J. Jacomini, "Weighting Factor and Transmission Time Optimization in Video MTI Radar," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-8, No. 4, pp 517-527, July 1972.

52. Reference 2, page 335.

53. H. G. Daellenbach and E. J. Bell, User's Guide to Linear Programming, Prentice Hall, Inc., Englewood Cliffs, N. J., 1970.

54. L. Weinberg, Network Analysis and Synthesis, p 491, McGraw-Hill Book Company, New York, N. Y., 1962.

55. R. G. Martin, Optimum Synthesis of Transversal Filter Radar Moving-Target Indicator, Ph.D. Dissertation, The Johns Hopkins University, Baltimore, Maryland, 1970.

56. H. L. Van Trees, Detection, Estimation, and Modulation Theory, Part I, p 76, John Wiley and Sons, Inc., New York, N. Y., 1968.

57. R. Fletcher and M. J. D. Powell, "A Rapidly Convergent Descent Method for Minimization," Computer Journal, Vol. 6, pp 163-168, 1963.

58. J. Nowalik and M. R. Osborne, Methods for Unconstrained Optimization Problems, pp 45-48, American Elsevier Publishing Co., Inc., New York, N. Y., 1968.

59. Reference 2, page 89.

60. W. C. Davidon, "Variable Metric Method for Minimization," ANL-5000 Rev, AEC Research and Development Report, Argonne National Laboratory, Lemont, Illinois, November 1959.

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From 1959 through 1963 he was employed by Scientific-Atlanta, Inc., as a co-operative student. Since 1963 he has been employed by The Georgia Tech Engineering Experiment Station, where he currently holds the title of Senior Research Engineer. During his employment by Georgia Tech he has taught courses in the School of Electrical Engineering, and has been involved in numerous research programs concerned with radar system analysis, design, fabrication and evaluation.