Reversed Switch-On Dynistor Switches of Gigawatt Power Microsecond Pulses

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Abstract

A high-power (250 kA and 25 kV) compact switch based on an assembly of reversed switch-on dynistors (RSDs) connected in series and a coaxial saturable-core choke, which is necessary for their effective switching, is described. An essential feature of this switch is a drastic reduction of the duration of RSDs control pulse, which allows using minimum dimensions and low inductance saturable core choke and obtain high rise rate (more than 30 kA/μs) of the switched current. The increased RSDs control pulse amplitude and rise rate that are required for RSDs switching on by reduced duration triggering pulse are attained by using a fast switch based on new type semiconductor devices—deep-level dynistors (DLDs).

Keywords

Semiconductor, Assembly, Switch

1 Introduction

Power silicon thyristors are conventional semiconductor switches in high power devices of pulsed power engineering. These thyristors are characterized by a low steady-state voltage drop after termination of the transient switching process and are comparatively inexpensive. Two-electrode semiconductor devices — reversed switch-on dynistors (RSDs) [1-3] that are switched on by control plasma layer — represent a promising alternative to pulsed thyristors.

Due to uniform over device area switching on process the switching capability of RSDs is 1.5 - 2 times higher than those of the best modern pulsed thyristors with the same diameter of semiconductor structure.

2 Reversely switch-on dynistor structure

Reversely switch-on dynistor (RSD) is a four-layer two-electrode silicon semiconductor thyristor-type device (Figure 1). The design of its anode emitter consists of alternating p^+ and n^+ sections with a characteristic size smaller than the thickness of the n-base.

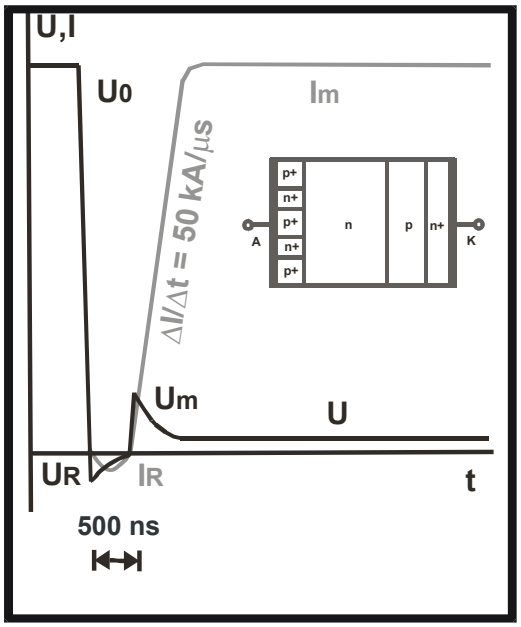


***Figure 1**: Schematic structure of reversely switch-on dynistor as well as voltage and current pulse forms during switching on process*

In the initial state, RSD blocks the voltage of power circuit U_0 (2…2.5 kV). To turn-on the device the low reverse voltage $U_R << U_0$ is applied across RSD for a short time while U_0 voltage is blocked by saturable core choke. As a result, the control current I_R flows through n^+-n-p-n^+ reverse conducting channels. This current provides the carrier injection into n-base uniformly all over the device area.

After the control current stops flowing and the initial voltage polarity restores, holes are being moved by the field from the plasma layers into the p-base, causing electron injection from cathode n^+-emitter and the fast turn-on of RSD.

Small peak voltage U_m occurs on RSD during the process of n and p bases modulation. The duration of this peak voltage is less than 1 μs and is determined by width of base layers and charge stored into the structure while control current flows through RSD. After that few volts steady-state voltage U remains on RSD.

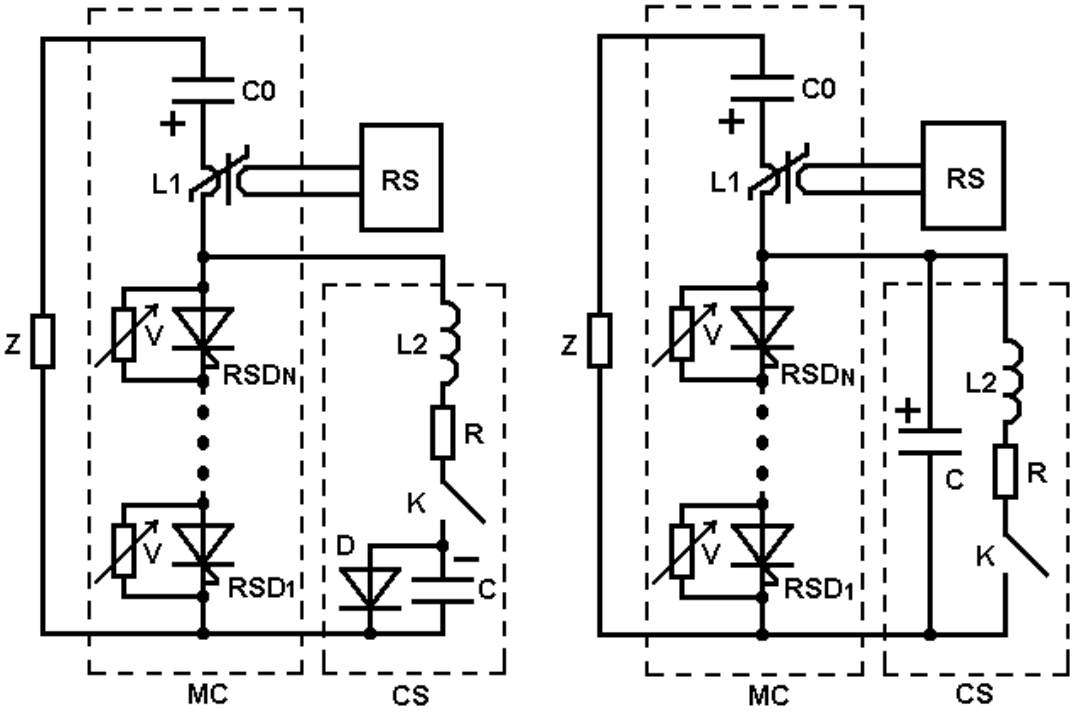
Under the sufficient density of control current and sufficient density of injection reverse conducting channels RSD switching occurs uniformly all over the device area. As a result, the switching capability of RSD increases practically proportionally to the device operating area. RSD turns on without any delay between control and main current pulses, therefore in case of serial connection all RSDs are turned-on simultaneously and high reliability of RSD stack operation is guaranteed.

Power RSD switches are able to switch current pulses with amplitude of several hundreds kiloamperes and dI/dt of tens kiloamperes per microsecond under the voltage of

tens kilovolts. They have high efficiency, small dimensions and low cost. The latter is determined by simple manufacturing technology of reversely switch-on dynistors.

3 Main electronic design principles of RSD based switches

Two principal electrical circuits of power switches based on high voltage RSD assembly RSD1-RSDN and energy storage capacitor C0 are shown on Figures 2 and 3. MC is the main circuit, CS is the control system, RS is the remagnetization system for saturable core choke and Z is a load.



***Figures 2 (left) and 3 (right)**: Principal electrical circuits of power switches based on RSD stack and energy storage capacitor C_0*

In the circuit on the Figure 2 power capacitor C_0 and triggering capacitor C are charged initially up to U_0 and U voltages correspondingly (U_0>>U). RSD stack RSD_1-RSD_N blocks voltage U_0. Triggering switch K blocks voltage U_0+U. Varistors V equalize the voltage drops between RSDs in stack.

When triggering switch K is turned on capacitor C discharges through RSDs and reverse control current I_R passes through RSD structures. Negative voltage which occurs on capacitor C due to LC recharge is blocked by diode D and control current decays slowly with time constant L_2/R.

Saturable core choke L_1 blocks U_0 voltage during RSD switching on process and prevents passing of I_R current through load Z. Then inductance L_1 drastically reduces after saturation of the core, initial polarity U_0 voltage is applied to RSD stack, RSDs switch on simultaneously without delay and power capacitor C_0 discharges through load Z. Resistor R prevents discharge of C_0 capacitor through the control system circuit.

In the circuit on the Figure 3 power capacitor C_0 and triggering capacitor C are charged initially up to U_0 voltage. Then triggering switch K is turned on and capacitor C recharges through the circuit RL_2. RSD stack blocks negative voltage on capacitor C when the voltage on capacitor C changes the polarity. I_R triggering current forming by L_2 inductance passes through RSDs structures and decays slowly with time constant L_2/R. Saturable core choke L_1 has large inductance during this process and prevents discharge of C_0 capacitor through the load, but after saturation of the core U_0 voltage is applied to RSD stack and RSDs switch on simultaneously without delay.

The parameters of control system elements L_2, R, C in both circuits of Figures 2 and 3 provides the duration of I_R triggering current higher than time of L_1 choke core saturation. This is very important to prevent the delay between reverse triggering pulse current and main forward pulse current through RSD. Otherwise due to recombination process the charge stored into RSD structures by reverse current may decrease below the lowest acceptable limit.

Remagnetization system is necessary to put the core of L_1 choke into initial unsaturated state.

Single-turn coaxial construction of choke L_1 allows to obtain very low inductance of L_1 in saturated state and therefore obtain high increase rate of power current. The size of the choke may be reduced by using short triggering pulses. But the amplitude of triggering current in this case should be high. For example, for 500 ns duration of triggering pulse current and 3" diameter RSD the triggering pulse amplitude should be more than 1.5 kA. To obtain so high triggering pulse parameters and eliminate high loses we should use special semiconductor devices for triggering switch K.

4 Deep level dynistors – new nanosecond range power semiconductor devices.

It is possible to use pulsed thyristors for RSD triggering, but more promising devices are Deep Level Dynistors (DLD) which have been developed recently at Ioffe Physico-Technical Institute (Russia). The most advantages of DLD are subnanosecond switching on time, dI/dt capability up to 250 kA/μs, operating current up to few tens kA and relatively low cost provided due to simple technology process.

Deep Level Dynistors (DLD) is a four layers two electrodes thyristor type device (Figure 4) on the base of silicon doped by the impurities, forming deep levels at the middle of the band-gap.

In initial state the voltage U_0 (2…2.5kV) is applied across DLD forming the space-charge region near the collector junction. Switch-on process is initiated by short (1,5-2 ns) overvoltage pulse with dU/dt not less than one kilovolt per nanosecond applied to the dynistor. The electric field at the collector region in this case essentially exceed the critical value of static avalanche breakdown field because there are no free carriers which can cause the impact ionization of silicon lattice in this region.

When electric field exceeds ~$3 \cdot 10^5$ B/cm, the tunnel ionization of impurity centers occurs, electrons appear in the super-high field region and cause the intensive impact ionization. The front of impact ionization moves with velocity 3-5 times higher than saturated velocity, leaving electron-hole plasma behind itself. This plasma with a high

conductivity fills the base layer and causes fast DLD switching into conductive state. Typical duration of this process does not exceed several hundreds of picoseconds.

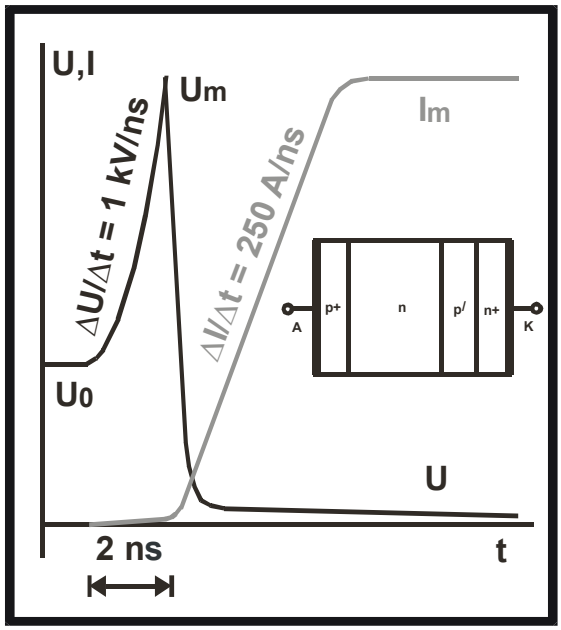


***Figure 4**: Schematic structure of deep level dynistor as well as voltage and current pulse forms during switching on process*

After switching, high conductivity state of dynistor is supported by carriers injection of from p^+ and n^+ injectors. Very fast switching time and low voltage across the device in the on-state lead to very low switching energy losses; as a result dI/dt capability of FID can be as high as several hundreds kiloampere per microsecond.

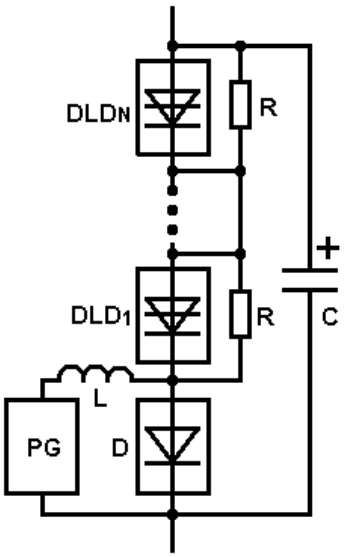


***Figure 5**: Principal electrical circuits of DLD based switch*

The principal electrical circuit of high voltage DLD based switch is shown on Figure 5. DLD_1-DLD_N are serially connected dynistors. Nanosecond pulse of overvoltage for DLD triggering is formed by inductance L, capacitor C and Drift Step Recovery Diodes (DSRD) assembly D.

DSRD is nanosecond high voltage (1-1.5kV) switching-off diode with deep diffusion pn junction. Nanosecond current interruption by DSRD is possible under special commutation conditions. At first 100 ns pulse of direct current formed by PG generator passes through DSRD, provides electron-hole plasma in base layer and store the charge inside diode structure. After that reverse pulse current pulls of plasma from the diode and result in very fast DSRD switching-off for a few nanoseconds. Nanosecond rise time high voltage pulse is applied to DLD_1-DLD_N -C circuit and result in DLD stack switching on.

Resistors R are used to equalize static voltage drops between DLD_1-DLD_N.

5 Design of RSD based switches and experimental results

Photo of power RSD switch with DLD based triggering system is shown on Figure 6. Principal electrical circuit of the switch is shown on Figure 3.

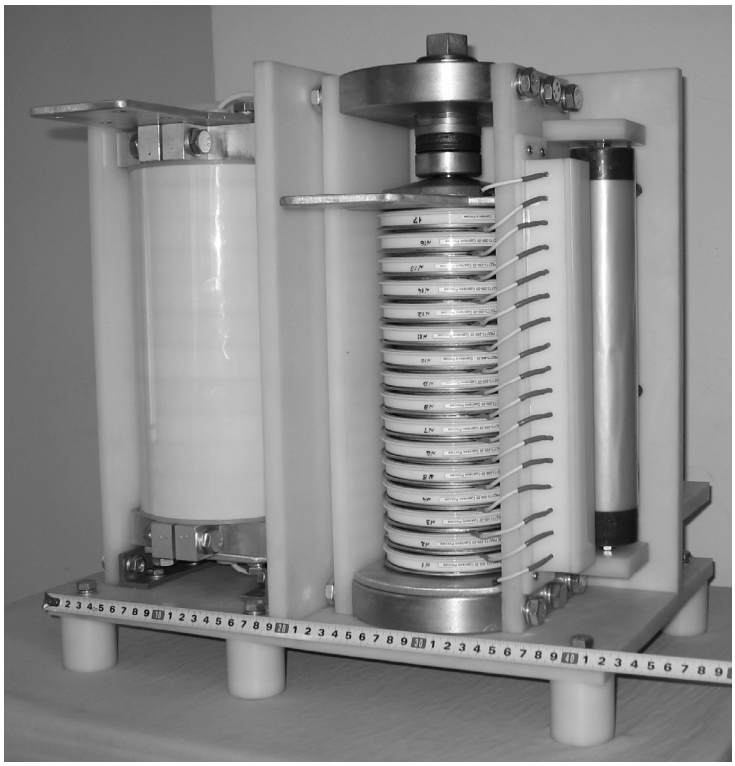


***Figure 6**: 250 kA 25 kV RSD based switch with DLD triggering system*

One can see at left side single-turn saturable core choke, at right side RSD stack with varistor divider and triggering capacitor C behind the RSD stack.

Main parameters of the switch are the following:

- Maximum pulse current 250 kA
- Pulse duration 300 μs
- Maximum operation voltage 25 kV
- RSD stack 16 RSDs with 3" diameter of semiconductor structure

Triggering DLD based switch has maximum operation voltage 25 kV. Triggering pulse current amplitude is 2.5 kA, pulse rise time is 200 ns. DLD stack consists of 12 serial connected 12mm diameter DLDs. Photo of DLD switch is shown of Figure 7.

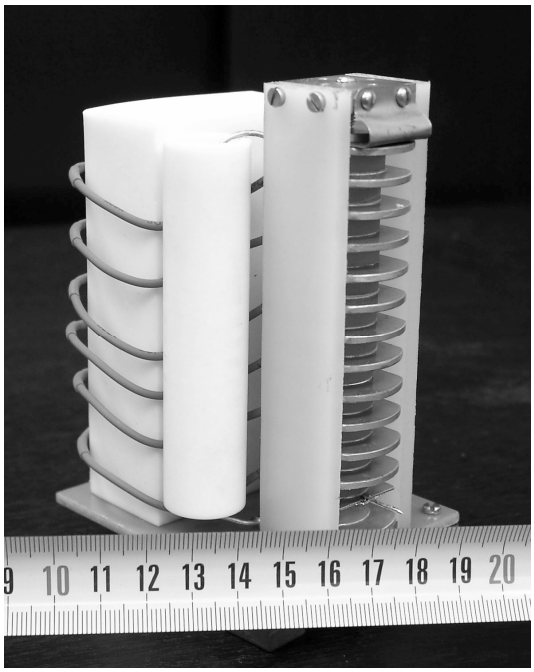


***Figure 7**: 25 kV DLD based switch with few nanosecond pulse rise time*

Principal electrical circuit of DLD switch is shown on Figure 5. One can see at the photo DLD_1- DLD_{12} stack with diode overvoltage pulse former based on DSRD assembly (bottom device in the stack), triggering capacitor C. Resistors R and inductance L are placed into compound filled box (behind the stack and capacitor).

The oscillograms of RSD based switch pulse current I_0 and voltage drop U at RSD stack during commutation process are shown of Figure 8.

One can see that negative pulse voltage drop on RSD stack is relatively higher. Small total square of RSD reverse conductivity channels limits the maximum amplitude of reverse pulse current at 10-15% level of forward pulse current.

The circuit shown on Figure 9 is used to form slowly decay alternating-sign pulses in the load. Saturable core chokes L_1 and L_2 have high inductance during RSD triggering and separate control system CS from power circuit and diode stack D. Choke L_1 block U_0 voltage of capacitor C_0, choke L_2 blocks reverse voltage U_R on RSD which occurs in RSD stack during triggering process. The size of choke L_2 is small because U is much less than U_0. When core of choke L_1 saturates forward U_0 voltage is applied to RSD stack, RSD stack switches on and commutates power pulse current through the load R_0L_0.

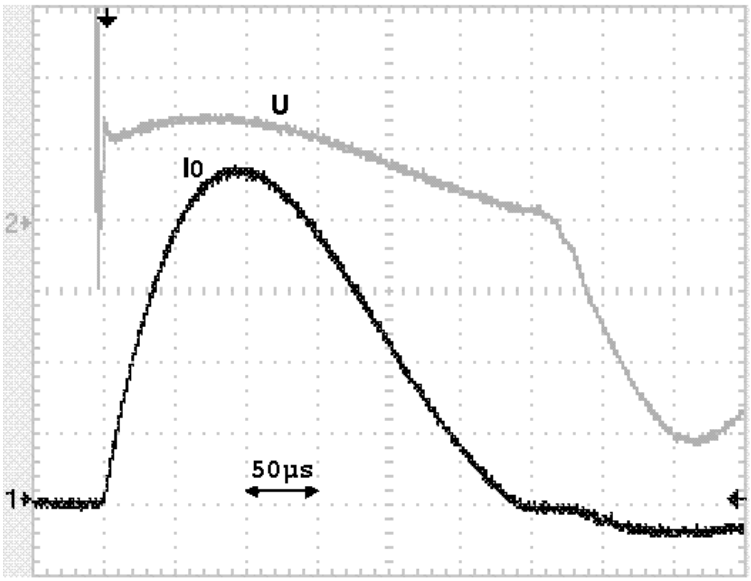


***Figure 8**: Oscillograms of RSD based switch pulse current I_0 and voltage drop on RSD stack during commutation process. Time scale of X-axes is 50 µs/div, Y axes scales are 50 kA/div and 5V/div.*

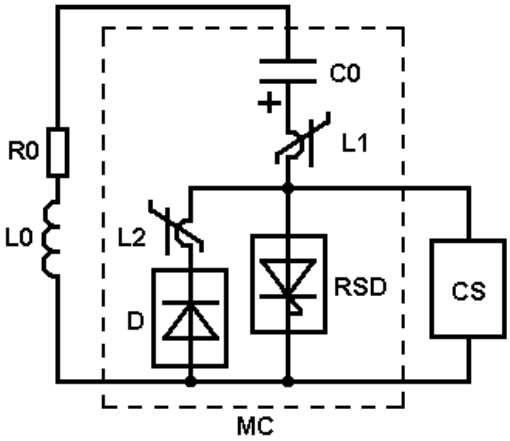


***Figure 9**: Principal electrical circuit of RSD based switch with additional diode stack to form slowly decay alternating-sign pulses on the load*

When capacitor C_0 recharges to negative polarity, chokes L_1 and L_2 block reverse voltage and after saturation of L_1 and L_2 cores negative pulse current passes through parallel connection of RSD stack and diode stack D. Reverse power current through RSD stack is low because conductivity of diodes in open state are higher than reverse conductivity of RSD. But this small current keeps RSDs in open state and prevents RSD stack switching off. Therefore slowly decay alternating-sign pulses passes through the load.

Power current rise rate for all described above RSD switches is determined by saturated inductance of L_1 choke and stray inductance of RSD stack. The coaxial construction of choke L_1 is used to increase the power current rise rate (see Figure 10).

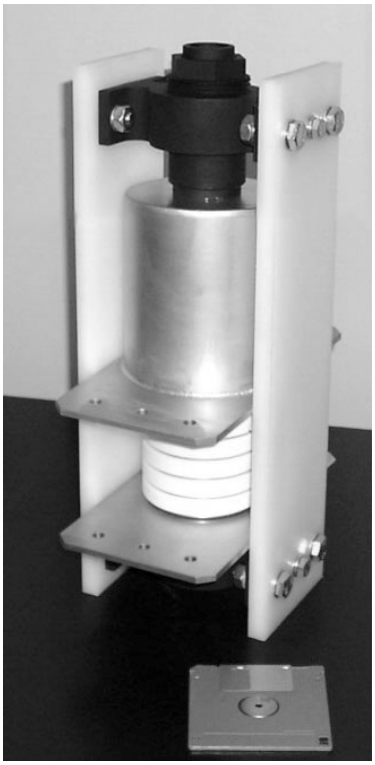


***Figure 10**: 200kA 12 kV RSD based switch with coaxial saturated core choke. dI/dt=30kA/μs*

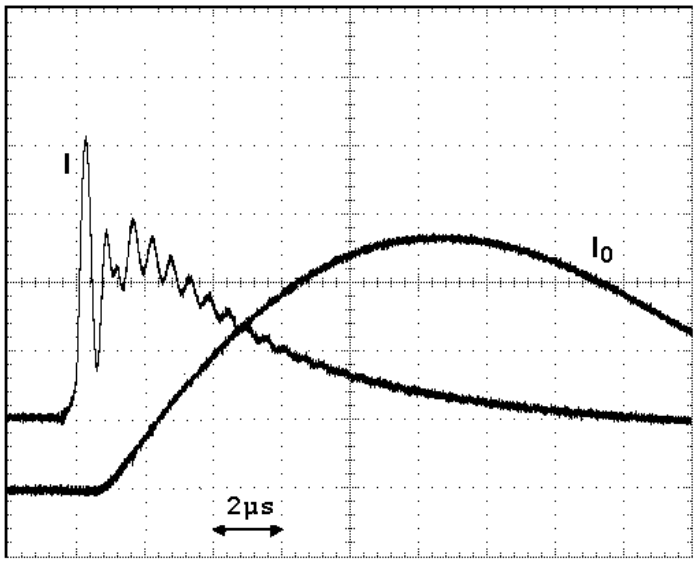


***Figure 11**: Oscillograms of RSD based switch with coaxial choke pulse current I_0 and triggering pulse current I. Time scale of X-axes is 2 μs/div, Y axes scales are 50 kA/div and 500A/div correspondingly.*

Main parameters of RSD based switch with coaxial saturated core choke are the following:

- Maximum pulse current 200 kA
- Pulse duration 30 μs
- Maximum operation voltage 12 kV
- Current rise rate 30 kA/μs
- RSD stack 7 RSDs with 2" diameter of semiconductor structure

The oscillograms of power pulse current through the load I_0 and triggering pulse current I are shown of Figure 11.

It is possible to increase energy of the pulses commutated by RSD switches by increasing operation voltage U_0 or by increasing pulse current I_0. Both are possible. Reliability of RSD stack, simple construction and simultaneous switching on series connected RSDs allow to increase operation voltage up to 50 kV and more. Maximum pulse current commutated by 4" diameter RSD is more than 400 kA. The simple parallel connection of RSD stacks is possible to increase pulse current additionally.

6 Conclusion

Up to gigawatt pulse power compact switches with up to 50 kA/μs current increase rate is possible to build based on assembly of series connected reversed switch-on dynistors (RSDs) and coaxial saturable-core choke. Due to uniform over device area switching on process the switching capability of RSDs is 1.5 – 2 times higher than those of the best modern pulsed thyristors with the same diameter of semiconductor structure. Simple and reliable construction of RSD based switches are designed and described in the article.

The possible area of RSD switches application are pulsed electromagnetic and electro hydraulic technologies, laser technologies, nuclear research, purification of industrial gases and water by electrical discharge etc.

References

[1] *Gorbatyuk, A.V., Grekhov, I.V., Korotkov, S.V., and Yakovchuk,N.S.,* USSR Inventor's Certificate no. 1 003 699, Byull. Izobret., 1983, no. 39, p. 259.

[2] *Gorbatyuk, A.V., Grekhov, I.V., Korotkov, S.V., et al.*, Pis'ma Zh. Tekh. Fiz., 1982, vol. 8, no. 11, p. 685 [Sov. Tech. Phys. Lett. (Engl. Transl.), vol. 8, no. 6, p. 298].

[3] *Korotkov, S.V.*, Prib. Tekh. Eksp., 2002, no. 4, p. 5 [Instrum. Exp. Tech. (Engl. Transl.), 2002, no. 4, p. 437].