Design of High-Speed SiGe HBT BiCMOS Circuits for Extreme Environment Applications

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2007

Design of High-Speed SiGe HBT BiCMOS Circuits for Extreme Environment Applications

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To my family

and friends.

ACKNOWLEDGEMENTS

This research work that I commenced four years ago would not have culminated into this dissertation without the help and constant support of many people. I am grateful to my advisor, Professor John D. Cressler, for providing me with this wonderful and exciting opportunity. His deep love and enthusiasm for research and his passion for life is very infectious. His efforts towards ensuring the progress and well-being of his students is truly remarkable and I am a very happy beneficiary of that. I am immensely proud to have been associated with him and his SiGe Research Group.

I would like to express my gratitude to Professor Joy Laskar, Professor John Papapolymerou, Professor Kevin T. Kornegay, and Professor Thomas D. Morley for serving as members of my Defense Examination Committee. I would like to thank Dr. Guofu Niu and Mr. Michael J. Palmer of Auburn University for continuing to help with my research work in all possible manner, even after leaving Auburn University.

I would like to thank my colleagues in the SiGe Research Group: Dr. Wei-Min Kuo, Dr. Yuan Lu, Dr. Jonathan Comeau, Mr. Akil Sutton, Ms. Becca M. Haugerud, Ms. Laleh Najafizadeh, Mr. Mustayeen Nayeem, Mr. Joel Andrews, Dr. Enhai Zhao, Mr. Tushar Thrivikraman, Mr. Curtis Grens, Dr. Zhenrong Jin, Dr. Qingqing Liang, Dr. Tianbing Chen, Dr. Ying Li, Dr. Gang Zhang, Dr. Shiming Zhang, Mr. Xiangtao Li, Dr. Chendong Zhu, Mr. Marco Bellini, Mr. Tom Cheng, Mr. Steven Finn, Mr. Aravind Appaswamy, Mr. Jiahui Yuan, Mr. Ryan Diestelhorst, Mr. Ming Teng Han, Mr. Adnan Ahmed, Mr. Mustansir Pratapgarhwala, Ms. Ragad Al-Huq, Mr. Man-Chun Lam, Mr. Gustavo Espinel, Mr. Anuj Madan, Dr. Amit Bavisi, Dr. Rao Rapeta, Mr. José-Luis Olvera Cervantes, Dr. Gnana Prakash, Dr. Bongim Jun Dr. Jarle Johansen, Dr. Jongsoo Lee, and Dr. Seung-Yun Lee; as well as colleagues in the Microwave Applications Group: Dr. Bhaskar Banerjee, Ms. Sunitha Venkataraman, Mr. Saikat Sarkar, Ms. Soumya Chandramouli, Dr. Youngsik Hur, Dr. Moonkyun Maeng, Dr. Chang-Ho Lee, Dr. Hyoungsoo Kim, Dr. Franklin Bien,

Mr. Bevin George, Mr. David Yeh, Dr. Rajarshi Mukhopadhyay, Dr. Sebastien Nuttinck, Dr. Sangwoong Yoon, and Dr. Yunseo Park for their significant contributions.

I would like to thank the support staff at the Georgia Electronic Design Center: Ms. DeeDee Bennett, Mr. Chris Evans, Ms. Korinne Lassiter, Ms. Tammy Scott, Ms. Gwen Satchel, Ms. Joi Adams, and Dr. Chris Scholz for their help; as well as our research affiliates: Dr. Paul Marshall, a consultant to NASA-GSFC, Dr. Robert Reed of Vanderbilt University, Dr. Cheryl Marshall and Martin A. Carts of NASA-GSFC, Mr. Zach Sparling of MOSIS, Dr. David Hansen, Dr. Kay-Carol M. Jobe, and Mr. Anthony L. McKay of Boeing Satellite Systems, Dr. Benjamin Blalock, Ms. Chandradevi Ulaganathan, and Mr. Suheng Chen of University of Tennessee, Ms. Beth Woods and Dr. Alan Mantooth of University of Arkansas, Dr. Foster Dai of Auburn University, Ms. Barbara A. Randall and Mr. Charles A. Burfield of Mayo Clinic, Dr. Emery Chen at National Taiwan University, Dr. Hans Gustat at Innovations for High Performance Microelectronics, and Dr. Alvin Joseph at International Business Machines for their cooperation.

I am grateful to my friends Dr. Rajkumar Sankaralingam, Mr. Pradeepkumar Kuttuva, Mr. Aravind Ganesan, Dr. Aniruddhan Sankaran, Mr. Vikas Datta, Mr. Archith Mahadevan, Dr. Prem Kishore, Dr. Vivek Krishnan, Mr. Karthik Narayanan, Mr. Varun Rupela, Dr. Pradeep Prasad, Mr. Anand Sankarraj, Mr. Shankar, Mr. Raghu Viswananthan, Mr. Kashyap Yellai, Mr. Rajan Pachapakesan, Dr. Bobby Sebastian, Mr. Jitto Titus, Mr. Ranjit David, and Mr. Manu Parmar for their encouragement.

The unwavering support and encouragement from my loving family throughout my graduate study made this day possible. The sacrifices that my parents Krithivasan and Sathyabama have made in raising their kids cannot be described in words. I am what I am today because of them. My brother Vijay has been a pillar of support in all my endeavors. I am forever indebted to my family.

TABLE OF CONTENTS

DEDICATION . . . . **iii**

ACKNOWLEDGEMENTS . . . . **iv**

LIST OF TABLES . . . . **x**

LIST OF FIGURES . . . . **xi**

SUMMARY . . . . **xv**

I INTRODUCTION **1**

1.1 SiGe: An Extreme Environment Technology 3

1.2 Single Event Upset in SiGe HBT Logic 4

1.3 SiGe HBT Technology for Cryogenic Application 7

1.4 Organization of Dissertation 9

II AN SEU HARDENING APPROACH FOR HIGH-SPEED SIGE HBT DIGITAL LOGIC **13**

2.1 Introduction 13

2.2 Device Technology 14

2.3 Device Simulations and Circuit Modeling 14

2.4 Circuit Descriptions 15

2.4.1 NAND-Based D-Flipflop 16

2.4.2 Standard CML MS D-Flipflop 17

2.4.3 Current-Shared Hardened D-Flipflop 18

2.4.4 Dual-Interleaved D-Flipflop 19

2.5 Circuit Simulations 20

2.6 Results and Discussion 21

2.6.1 Performance Analysis 21

2.6.2 Understanding the Results 24

2.7 Summary 30

III APPLICATION OF RHBD TECHNIQUES TO SEU HARDENING OF THIRD-GENERATION SIGE HBT LOGIC CIRCUITS 31
3.1 Introduction 31
3.2 SiGe HBT BiCMOS Technology 32
3.3 SiGe RHBD Techniques 32
3.3.1 Circuit-Level Techniques 32
3.3.2 Device-Level RHBD Techniques in SiGe HBTs 35
3.4 Test Setup 38
3.5 Heavy Ion Data & Analysis 39
3.6 Summary 45
IV ON THE FEASIBILITY OF USING 120 GHZ SIGE HBT TECHNOLOGY FOR CRYOGENIC BROADBAND ANALOG APPLICATIONS 48
4.1 Introduction 48
4.2 Device Technology 48
4.3 Experiment 49
4.4 Results and Discussion 49
4.4.1 *dc* Characteristics 49
4.4.2 *ac* Characteristics 51
4.5 Summary 52
V DESIGN OF A 24 GHZ BROADBAND SIGE HBT LIMITING AMPLIFIER 56
5.1 Introduction 56
5.2 Device Technology 57
5.3 Circuit Design and Layout 57
5.3.1 Broadband Amplifier Techniques 58
5.3.2 Amplifier Architecture 59
5.3.3 Amplifier Layout 61
5.4 Measurement Results 61
5.4.1 RF Measurements 62
5.4.2 Time-Domain Measurements 62

5.4.3 Performance Comparison 63

5.5 Summary 65

VI CRYOGENIC CHARACTERIZATION OF A 24 GHZ BROADBAND SIGE HBT LIMITING AMPLIFIER 67

6.1 Introduction 67

6.2 Experiment 69

6.2.1 Cryogenic RF Response 69

6.2.2 Cryogenic Time Domain Response 72

6.3 Design Guidelines 74

6.4 Summary 76

VII DESIGN OF A HIGH-SLEW RATE SIGE BICMOS OPERATIONAL AMPLIFIER FOR OPERATION DOWN TO DEEP CRYOGENIC TEMPERATURES 77

7.1 Introduction 77

7.2 Device Technology and Cryogenic Operation 78

7.3 Circuit Design 79

7.3.1 Amplifier Core Design 80

7.3.2 Slew-Enhancement Technique 81

7.3.3 Biasing Schemes 82

7.4 Measurement Results and Discussion 84

7.4.1 *dc* Characteristics 84

7.4.2 Slew-Rate and Gain-Bandwidth 86

7.5 Summary 88

VIII HALF-TERAHERTZ OPERATION OF SIGE HBTS 90

8.1 Introduction 90

8.2 SiGe HBT Technology 91

8.3 Measurement Setup 92

8.4 Electrical Results 92

8.5 Summary 95

IX CONCLUSION AND FUTURE WORK **97**

REFERENCES **99**

VITA **107**

LIST OF TABLES

1 Power consumption and number of transistors in the circuits. 21

2 Comparison of hardening techniques. 38

3 Comparison of power consumption, area, and speed. 38

4 Estimated threshold LET for the shift registers. 46

5 Summary of the SiGe limiting amplifier characteristics. 65

6 Comparison with published amplifiers. 66

7 Transistor performance summary at 300 K, 77 K, and 4.5 K, for an emitter geometry of 0.12 x1.0 μm^2. 96

LIST OF FIGURES

1 The schematic cross-section of the SiGe HBT, showing the two potential damage regions during exposure to ionizing radiation (after [23]). 4

2 A typical warm box in a lunarcraft to protect on-board electronics from large temperature fluctuations (courtesy J.D. Cressler). 10

3 An equivalent circuit model for including the ion-induced terminal currents in the circuit simulations. 16

4 Logic diagram of a conventional rising edge-triggered D-flipflop with the schematic of a two-input NAND gate in the inset. 17

5 The standard CML MS D-flipflop. 18

6 Illustration of current-sharing hardening (CSH) concept using a basic CML gate. 19

7 The dual-interleaved D-flipflop with minimal cross-coupling in the storage cell. 20

8 Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 2 Gbit/s (LET=0.5 pC/μm and switch current is 1.5 mA). 22

9 Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 4 Gbit/s (LET=0.5 pC/μm and switch current is 1.5 mA). 23

10 Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 6 Gbit/s (LET=0.5 pC/μm and switch current is 1.5 mA). 24

11 Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 2 Gbit/s (LET=0.5 pC/μm and switch current is 0.5 mA). 25

12 Summary comparison of the four circuit architectures using as a metric, the number of upset bits/ unit power consumption as a function of data rate. . . 26

13 Single-ended and differential output voltages for the differential pair in the storage cell struck by heavy ion in standard CML MS D-flipflop (switch current is 0.5 mA). 27

14 Single-ended and differential output voltages for the differential pair in the storage cell struck by heavy ion in dual-interleaved D-flipflop (switch current is 0.5 mA). 28

15 Single-ended and differential output voltages for the NAND gate struck by heavy ion in NAND-based D-flipflop (switch current is 0.5 mA). 29

16 Block diagram of the 16-bit shift registers. 33

17 Schematic of master stage of the GFC D-flipflop. 35

18 Block diagram of the triple module redundancy (TMR) implementation. . . 36

19 (a) RHBD C-B-E transistor and (b) C-B-E-B-C transistor used in the baseline Std. SR. 37

20 Die micrograph of a 16-bit shift register (a) and its TMR implementation (b). 39

21 Block diagram of the heavy-ion test-setup for SEU characterization of 16-bit RHBD shift registers. 40

22 Device cross-section (σ) as a function of effective LET for data rate = 1.0 Gbit/s. 42

23 Device cross-section (σ) as a function of effective LET for data rate = 0.1 Gbit/s. 43

24 Device cross-section (σ) as a function of effective LET for data rate = 0.05 Gbit/s. 44

25 Device cross-section σ as a function of data rate for LET = 8.5 MeV-cm^2/mg. 45

26 Device cross-section σ as a function of data rate for LET = 53 MeV-cm^2/mg. 45

27 Average errors per error events as a function of data rate for LET = 8.5 MeV-cm^2/mg. 46

28 Average errors per error events as a function of data rate for LET = 29 MeV-cm^2/mg. 47

29 Average errors per error events as a function of data rate for LET = 53 MeV-cm^2/mg. 47

30 The Gummel characteristics of 0.12×2.56 μm^2 SiGe HBT at 300 K and 82 K. 50

31 Transconductance as a function of collector current at 300K and 82K. . . . 51

32 Current gain (β) as a function of collector current at various temperatures. . 52

33 The peak current gain (β_{max}) as a function of inverse of temperature. 53

34 The high-injection output characteristics at 300 K. 53

35 The high-injection output characteristics at 85 K. 54

36 $M - 1$ versus V_{CB} measured at low-injection (I_E=1 μA) at 300K and 85K. 54

37 Cut-off frequency versus collector current density at 300 K and 85 K. . . . 55

38 Maximum oscillation frequency versus collector current density at 300 K and 85 K. 55

39 f_T and f_{max} versus collector current density of a 0.2 × 2.5 μm^2 SiGe HBT. . 57

40 Limiting amplifier block diagram showing gain stages and emitter followers. 58

41 Schematic of an emitter follower pair. 59

42 Schematic of the amplifier core used in all the stages of the limiting amplifier. 60

43 Micrograph of the SiGe limiting amplifier chip. 61

44 Measured single-ended S-parameters for the limiting amplifier. The 3-dB bandwidth (of S_{21}) is greater than 24 GHz. 63

45 Single-ended 10 Gbit/s limiting amplifier eye diagram. The accumulation time was 60 min. 64

46 Superconductor-semiconductor hybrid system showing the placement of the cooled SiGe HBT broadband amplifier in the high-speed, low-power data path (after [40]). 68

47 Simulated gain-bandwidth product (a) and input sensitivity (b) behavior across the limited temperature range over which transistor model from the design kit are valid. 68

48 Measured S_{11} across temperature showing slight degradation in input matching with cooling. 70

49 Measured S_{22} across temperature showing slight degradation in output matching with cooling. 71

50 Measured S_{12} across temperature showing no evidence of degradation in isolation with cooling. 72

51 Measured S_{21} across temperature showing increased gain peaking and bandwidth extension at low temperatures. 73

52 A common emitter gain stage with load inductance and its simplified small-signal equivalent circuit. 74

53 Single-ended 10 Gbit/s limiting amplifier eye diagram measured at 77 K showing significant closure compared to the eye at 300 K (Fig. 45). The accumulation time was 30 min 75

54 Bathtub plot for the limiting amplifier at 77 K and 300 K. 76

55 Peak g_m and peak β versus temperature of the SiGe HBT with emitter area of 0.5×2.5 μm^2. 79

56 The op-amp block diagram showing the core amplifier (A), the slew-buffer, and a typical load condition. 80

57 Folded cascode amplifier core with bias block and SiGe HBT input stage. . 81

58 Slew-buffer with load transistors biased in the linear region. 83

59 Weak-T current bias circuit with SiGe HBT PTAT chain and a transconductor (start-up circuit not shown). 84

60 Simulated input SiGe HBT g_m of the two circuits versus temperature for the corresponding bias tail current. 85

61 Chip micrograph of the slew-enhanced operational amplifier. 86

62 Measured total bias current and normalized input-referred offset voltage versus temperature for the two circuits. 87

63 The positive and negative slew rates of the circuits across temperature. . . . 88

64 Gain-bandwidth of the SiGe op-amps versus temperature. 89

65 Measured *dc* gain and phase margin as a function of temperature. 89

66 The current-voltage characteristics of a 0.12×1.0 μm^2 SiGe HBT at 300 K, 77 K, and 4.5 K. 93

67 Peak current gain (β) at V_{CB} = 0.0 V and peak f_T at V_{CB} = 0.5 V for a 0.12×1.0 μm^2 SiGe HBT, as a function of temperature. 94

68 The small-signal current gain at 300 K and 4.5 K for a 0.12×1.0 μm^2 SiGe HBT, at peak f_T. Inset shows the inferred f_T as a function of extrapolation frequency. 95

69 Measured peak f_T as a function of bias current for a 0.12×1.0 μm^2 SiGe HBT at 300 K, 77 K, and 4.5 K (V_{CB} = 0.5 V). 96

SUMMARY

The objective of this work is to investigate the suitability of applying silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) bipolar complementary metal oxide semiconductor (BiCMOS) technology to extreme environments and to design high-speed circuits in this technology to demonstrate their reliable operation under these conditions. This research focuses on exploring techniques for hardening SiGe HBT digital logic for single event upset (SEU) based on principles of radiation hardening by design (RHBD) as well as on the cryogenic characterization of SiGe HBTs and designing broadband amplifiers for operation at cryogenic temperatures. Representative circuits ranging from shift registers featuring multiple architectures to broadband analog circuits have been implemented in various generations of this technology to enable this effort.

For SEU hardening through RHBD in SiGe HBT technology, the dissertation covers:

1. An SEU hardening approach for high-speed SiGe HBT digital logic (Chapter II, also published in [1]).

2. Application of RHBD techniques to SEU hardening of third-generation SiGe HBT logic circuits (Chapter III, also published in [2]).

For investigation of suitability of SiGe HBT technology for cryogenic operation, the dissertation covers:

3. On the feasibility of using 120 GHz SiGe HBT technology for cryogenic broadband analog applications (Chapter IV, also published in [3]).

4. Design of a 24 GHz broadband SiGe HBT limiting amplifier (Chapter V, also published in [4]).

5. Cryogenic characterization of a 24 GHz broadband SiGe HBT limiting amplifier (Chapter VI).

6. Design of a high-slew rate SiGe BiCMOS operational amplifier for operation down to deep cryogenic temperatures (Chapter VII, also published in [5]).

7. Half-teraHertz operation of SiGe HBTs (Chapter VIII, also published in [6]).

CHAPTER I

INTRODUCTION

Silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology has found application in several terrestrial electronic systems ranging from high-speed digital systems to analog and radio-frequency (RF) systems [7]. The superior device performance offered by SiGe HBTs and their integrability with the best of breed Si CMOS devices make them attractive for these applications. This BiCMOS approach benefits from the maturity of Si fabrication, enabling large-scale integration at high yields. Though SiGe technology has been making serious inroads into several terrestrial applications, applying this technology to "extreme environments" is not without challenges. "Extreme environments" are usually characterized by the presence of high levels of radiation, extreme thermal conditions, or a combination of these and other factors such as high pressure, high humidity, dust, etc. However, as will be demonstrated in this proposal, SiGe HBT technology offers a unique opportunity for operating electronic systems reliably in extreme environments, particularly in high radiation and cryogenic environments [8].

SiGe HBT technology has generated considerable interest in the space community because of its robustness to total ionizing dose (TID) radiation without any additional hardening [9]–[12]. Recent studies on the effects of proton irradiation on critical analog and RF circuits, and passive elements implemented in various generations of SiGe HBT technology concluded that the degradation associated with the exposure of these circuits to extreme proton fluences (as high as 5×10^{13} p/cm^2) is minimal [13]–[15]. However, the tolerance of SiGe devices and circuits to TID levels typically experienced by satellite systems does not translate into improved single event response in SiGe HBT digital logic. Digital circuits designed in this technology were, unfortunately, shown to be sensitive to single event upset

(SEU) [16], and circuit-level hardening based on the current-shared hardening (CSH) [17] technique proved ineffective in mitigating SEU in these circuits.

SiGe HBTs also exhibit several interesting thermal properties, especially at cryogenic temperatures [18], [19]. The key device parameters of SiGe HBTs are favorably impacted by cooling. The results of investigating the cryogenic performance of a 200 GHz SiGe HBT technology [20] that was not optimized for cryogenic operation indicates that SiGe HBTs, apart from maintaining *dc* ideality down to 85 K, show considerable improvement in their *dc*, *ac*, and noise performances [21]. This not only portends well for terrestrial cryogenic applications such as superconductor-semiconductor hybrid systems and low-noise receivers for astronomy, but also for specific space applications such as NASA's upcoming lunar mission. The lunar surface is a classic case of an extreme environment where the on-board electronics is subjected to huge temperature variations and high radiation levels simultaneously, and SiGe HBT technology, with all the salient extreme environment properties, has the potential to become the preferred technology for such niche applications.

Silicon (Si) integrated circuit (IC) technology was developed exclusively for application in terrestrial electronic systems. Such electronic systems rarely operate in an environment whose ambient temperature falls outside the mil-spec temperature range of -55 °C to 125 °C. Also, the amount of radiation encountered by these systems seldom exceeds the typical background radiation levels. Thus, to be able to apply Si technology primarily meant for terrestrial applications to extreme environment electronics without further costly process enhancements would prove highly profitable for the multi-billion dollar space industry. The search for such a Si technology has not been without impediments, given that low-temperature operation has traditionally been forbidden for conventional Si bipolar junction transistors (BJTs) and CMOS devices, and that radiation tolerance cannot be achieved without special process changes. However, with the advent of SiGe HBT technology, the search might well be over. The superior cryogenic properties of SiGe HBT combined with its unique TID-tolerant structural attributes make it attractive for extreme

environment applications.

1.1 SiGe: An Extreme Environment Technology

SiGe HBT technology was primarily developed as a low-cost alternative to III-V technologies. It is a very successful attempt at bandgap engineering Si. Bandgap engineering is achieved by introducing small amounts of germanium (Ge) into the base of a Si BJT. The introduction of Ge (and the resulting freedom to choose a high base doping profile) not only enhances several device parameters such as current gain (β), output conductance (function of early voltage, V_A), parasitic base resistance (r_{bb}), peak cut-off frequency (f_T), and maximum oscillation frequency (f_{max}), but also makes them strong functions of temperature. The placement of the temperature variable in the device equations is such that the device performance improves naturally with cooling. In addition, the physical construction of SiGe HBT device renders it "hard" to several types of TID radiation. The effect is not so much the result of the presence of Ge in base as it is due to the location of the emitter-base (EB) spacer oxide and the shallow-trench isolation, and the confinement of radiation-induced damage to these regions (Fig. 1) [22], [23]. Hence, a comparably constructed BJT sans Ge in the base would show similar tolerance to TID radiation. The superior intrinsic performance of SiGe HBTs aside, what makes SiGe technology even more attractive is the ease of its integration with high-performance CMOS processes.

The robustness to various types of ionizing radiation and the superior cryogenic properties are the reasons SiGe technology has aroused lot of interest in the extreme environment community. However, there still remain some issues that need to be addressed before this technology can be certified for extreme environment applications. First is the single-event sensitivity observed in SiGe HBT logic. What is of utmost interest to the space community is the demonstration of reasonable tolerance in SiGe HBT digital logic to SEU while preserving the cost effectiveness of using this technology. Second is demonstrating the functionality of SiGe HBT-based broadband circuits at cryogenic temperatures. This in

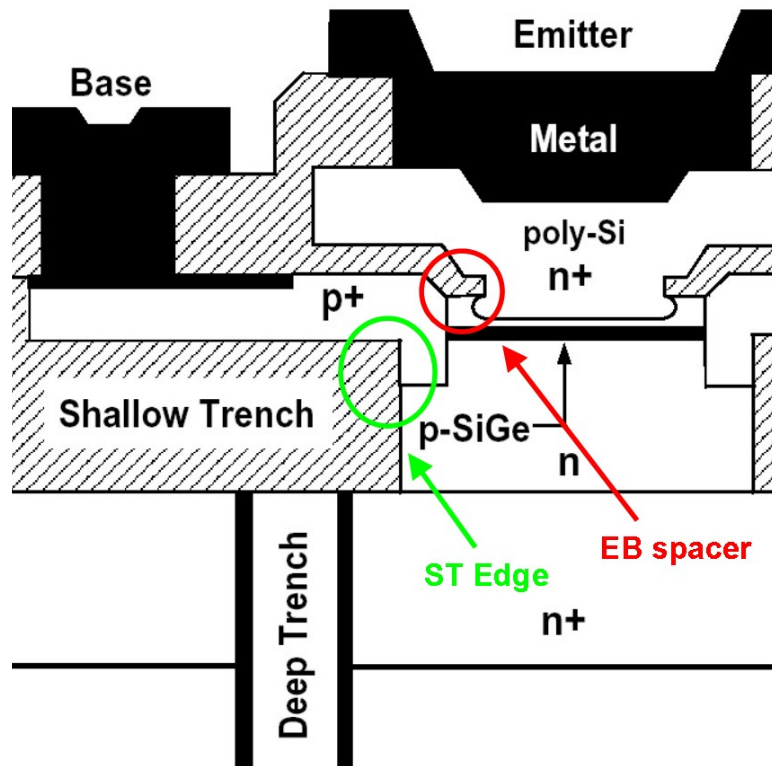


Figure 1: The schematic cross-section of the SiGe HBT, showing the two potential damage regions during exposure to ionizing radiation (after [23]).

turn could aid in the investigation of whether the remarkable cryogenic properties observed in SiGe HBTs translate into superior circuit performance at cryogenic temperatures.

1.2 Single Event Upset in SiGe HBT Logic

SEU occurs when radiation, like the alpha particles or cosmic rays, cause undesired bit flips in a digital circuit, thus corrupting the latch states. When an energetic particle of radiation traverses through semiconductor devices, it generates charges in its wake in the form of electron-hole pairs. Though the electron-hole pairs last for very short periods of time, there might just be enough time to collect these electrons and holes at various terminals, thus causing transient current pulses to flow in or out of the device terminals. These spurious current pulses, if large enough in magnitude, can cause the terminal voltages

to change, sometimes by as much as the full-scale of logic swing, resulting in a bit flip.

The number of ionizations caused by the impinging ion is a function of the energy it dissipates in traversing through the target material. This energy that it imparts to the semiconductor is given in terms of linear energy transfer or LET and is normalized by the density of the target material. The units of LET is MeV-cm^2/mg. As it takes a known amount of energy to generate an electron-hole pair in a given material, LET can also be expressed as charge "deposited" per unit path length. Thus, for Si with density of 2,328 mg/cm^3, an LET of 97 MeV-cm^2/mg corresponds to charge deposition of 1 pC/μm. The probability of an ion strike causing an "upset" to occur in the digital logic increases with an increase in LET and is expressed as the upset cross-section (σ), given by [24]

$$\sigma = \frac{N}{\phi}, \tag{1}$$

where N is the number of observed upsets (errors) and ϕ the particle fluence (number of incident particles per unit area, p/cm^2).

Notwithstanding the stellar TID response of SiGe HBTs, like other bipolar digital circuits, SiGe HBT digital circuits are quite sensitive to SEU. Unfortunately, this sensitivity only degrades as the data rates increase. In the heavy ion experiment on the shift registers designed in the first-generation SiGe HBT technology, which employed the CSH technique, it was noted that even with circuit hardening, the SEU immunity displayed by this technology falls below the expectations of the space community [16]. Therefore, the grand entry and the eventual prevalence of SiGe HBT technology in space electronics would depend on the demonstration of SEU immunity in this technology.

To achieve SEU immunity in any technology, a good theoretical understanding of the underlying single-event mechanism, both at circuit and device levels, is requisite. To enable such investigations in SiGe HBT technology, a combination of device and circuit simulations and ion beam experiments is required. Simulations of ion strike at device level help in estimating the amount the charge collected at various device terminals [25], [26]. However, the estimated charge needs to be calibrated with measured charge collection to gain

confidence in the device structure and the doping profiles of the device model used in these simulations. This calibration is also essential for validating the charge collection mechanism as modeled in the simulator, thus increasing the confidence in the results of these simulations. One would ideally want to use a full mixed-mode simulator with either 2D or 3D device simulation capability to understand the circuit response to an ion strike. But such simulators do not often support the advanced transistor models that circuit designers use and are not very time efficient. Therefore, an alternate approach involving separate device and circuit simulations is adopted. The upset currents obtained from the device simulation is ported into circuit simulation via an equivalent circuit model for the transistor being subjected to an ion strike [27].

Traditionally, the mitigation of SEU at device level has required expensive process changes to limit ion-induced local charge collection. At circuit level, mitigation has been achieved by (1) building in redundancy into logic circuits, (2) connecting large capacitances to ground at sensitive circuit nodes, or (3) using high-drive devices that present large parasitic capacitances [28]. While redundancy helps mitigate SEU by allowing majority voting between replicas of basic circuit blocks, large capacitive loads at sensitive nodes suppress ion-induced transient spikes by diverting the spurious current pulses to ground. Often times a combination of these techniques is required for improving SEU immunity. While these techniques work well for low-frequency applications (typically in the sub-GHz range), with the growing demands for high-speed operations at lower cost, the use of redundancy, large capacitances, high-drive devices, or expensive process modifications are not viable options for upset mitigation.

With growing trend in the field of space electronics to use commercial-off-the-shelf (COTS) parts as a cost-reducing measure along with the need for preserving the high performance of the commercial IC technology when applied in space-borne systems, the idea of radiation hardness by design (RHBD) has been gaining immense popularity in this field. It is envisioned through RHBD that radiation hardening of space electronic systems be

achieved purely through circuit design and layout techniques and without having to resort to process modifications or design rule violations [29]. In addition, these design techniques aim to achieve hardening with minimal compromise of the high performance offered by the commercial IC technologies. Thus, it is logical to develop techniques of RHBD for SiGe HBT logic to improve its SEU immunity while not sacrificing the performance advantage offered by this technology.

SiGe HBT logic falls under bipolar logic family. It is known that the SEU response of bipolar logic circuits is influenced by the circuit implementation, meaning a given logic function block implemented with different circuit architectures would show variable SEU responses. This observation could be used in developing design techniques to achieve immunity to SEU in SiGe HBT logic.

1.3 SiGe HBT Technology for Cryogenic Application

The low-temperature characteristics of SiGe HBTs are enhanced because of the bandgap engineering practiced in these devices. This enables SiGe HBTs to operate in temperature regimes traditionally forbidden to Si BJTs. Excellent cryogenic frequency response, low-noise performance, and analog properties of SiGe HBTs could be exploited in designing cryogenic systems. Further, circuits designed using a combination of scaled Si CMOS and SiGe HBTs could be the low-power solution for cryogenic systems.

To fully appreciate the performance advantage gained from operating SiGe HBTs at cryogenic temperatures, a comparison of cryogenic characteristics of SiGe HBTs and Si BJTs is drawn [30]. Though the cryogenic properties of Si BJTs depend strongly on the technology generation and profile design, certain common trends can be noted in their cryogenic characteristics. These include strong decrease in current gain (β), degradation in frequency response, strong increase in base resistance, increase in turn-on voltage, and strong increase in transconductance, among other less important low-temperature characteristics. SiGe HBTs also show a strong increase in transconductance and a modest increase

in turn-on voltage at low temperatures. However, the band-edge effects couple strongly into the bipolar equations of SiGe HBTs. In fact, they couple into terminal currents as exponential functions of bandgap changes divided by the thermal energy, kT, where k is the Boltzmann's constant and T the temperature. As a result there is a dramatic increase in the current gain (β) at low temperatures. The ratio of β_{SiGe} to β_{Si}, given by

$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} \simeq \left\{ \frac{\tilde{\gamma}\tilde{\eta}\triangle E_{g,Ge}(grade)/kT e^{\triangle E_{g,Ge}(0)/kT}}{1 - e^{-\triangle E_{g,Ge}(grade)/kT}} \right\}, \tag{2}$$

where $\tilde{\gamma}$ and $\tilde{\eta}$ are the position-averaged effective density-of-state and minority electron diffusivity ratio between SiGe and Si, respectively, $\triangle E_{g,Ge}(grade)$ is the Ge grading-induced bandgap offset, and $\triangle E_{g,Ge}(0)$ Ge-induced bandgap offset at the emitter end of the neutral base [30]. The Ge grading-induced drift field in the base of SiGe HBTs tends to offset the inherent degradation in the base transit time (τ_b) with cooling. Thus, the frequency response either improves or does not degrade at low temperatures [30]. The ratio of $\tau_{b,SiGe}$ to $\tau_{b,Si}$ is given by

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\eta}\frac{kT}{\triangle E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\triangle E_{g,Ge}(grade)} \left[1 - e^{-\triangle E_{g,Ge}(grade)/kT} \right] \right\}. \tag{3}$$

The base resistance in SiGe HBTs can be controlled far more easily at cryogenic temperatures than in Si BJTs because of the minimal carrier freeze-out occurring in the base of SiGe HBTs at low temperatures. The reason behind the immunity to carrier freeze-out is the highly doped thin base region, which is made possible by the reduced thermal cycle nature of the epitaxial growth process.

Though the key device parameters of SiGe HBTs show remarkable improvement at cryogenic temperatures, it remains to be demonstrated that this device-level performance enhancement translates to superior circuit performance at low temperatures. This calls for circuit-level cryogenic demonstrations of SiGe HBTs. To achieve this objective and to cater to certain niche applications detailed below, it is proposed that a cryogenic broadband amplifier and a high-slew rate operational amplifier be designed. While a broadband amplifier could be used for investigating the speed performance at low temperatures, a purely analog

circuit such as an operational amplifier could help test the feasibility of using SiGe HBTs for cryogenic precision analog circuits.

NASA's upcoming lunar mission presents a unique venue for practicing low-temperature electronics. With temperatures on the lunar surface varying from -230 °C to +120 °C, electronics on-board are subjected to huge temperature changes, sometimes in short intervals of time. Traditionally, the electronic systems on-board lunarcrafts are housed in a centralized location, inside what is called a "warm box" (Fig. 2), which shields the electronics from dramatic changes in temperature, thus always maintaining the ambient temperature within a narrow temperature range required for its reliable operation. These warm boxes, apart from being power hungry, bulky, and heavy, limit the distributiveness of on-board electronics. With SiGe HBTs exhibiting stellar cryogenic performance and built-in radiation tolerance, electronic systems based on this technology could be deployed outside the warm box in a remote electronics unit (REU) required for data acquisition and control. The REUs have several mixed-signal systems to perform data acquisition. The realization of key circuit blocks in these systems, such as voltage and current references, operational amplifiers, and analog-to-digital converters (ADC) in SiGe HBT technology, could aid in demonstrating the feasibility of using this technology for this application. This research will focus on developing a high-slew rate, wideband operational amplifier, a key building block in several mixed-mode systems, to operate in deep cryogenic temperature regimes.

1.4 Organization of Dissertation

Chapter II (also published in [1]) presents a new circuit-level SEU hardening approach for high-speed SiGe HBT digital logic. The workhorse current mode logic (CML) D-flipflop circuit architecture is modified to significantly improve its SEU immunity. Partial elimination of the effect of cross-coupling at the transistor level in the storage cell of this new circuit decreases its vulnerability to SEU. The SEU response of the new circuit is qualitatively compared with three other D-flipflop architectures. The results suggest that

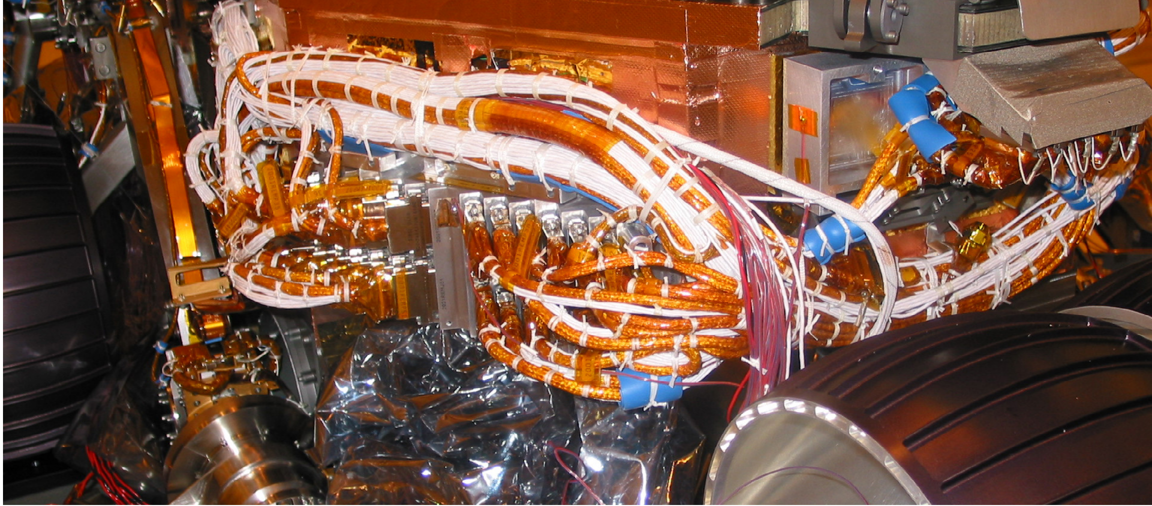


Figure 2: A typical warm box in a lunarcraft to protect on-board electronics from large temperature fluctuations (courtesy J.D. Cressler).

this new circuit architecture exhibits sufficient SEU tolerance, low layout complexity, and modest power consumption, and thus should prove suitable for many space applications requiring very high-speed digital logic.

Chapter III (also published in [2]) presents the application of RHBD techniques to SEU hardening of third-generation SiGe HBT logic circuits. Shift registers featuring RHBD techniques are realized in IBM 8HP SiGe BiCMOS technology [39]. Both circuit and device-level RHBD techniques are employed to improve the overall SEU immunity of the shift registers. Circuit-level techniques include dual-interleaving and gated-feedback that achieve SEU mitigation through local latch-level redundancy and correction. In addition, register-level RHBD based on triple module redundancy (TMR) versions of dual-interleaved and gated-feedback cell shift registers is also realized to gauge the performance improvement offered by TMR. The SEU performance of these shift registers was then tested using heavy ions and standard bit error rate testing methods.

Chapter IV (also published in [3]) is on the feasibility of using 120 GHz SiGe HBT technology for cryogenic broadband analog applications. Many salient features of SiGe HBTs, such as its increase in transconductance, current gain, and peak cut-off frequency

with cooling, can be exploited when designing high-gain (>55 dB), broadband (>20 GHz) cryogenic amplifiers. To demonstrate this device-level performance enhancement, extensive *ac* and *dc* characterization of representative transistors from a commercial 180 nm, 120 GHz peak f_T SiGe HBT BiCMOS technology [41]. The cryogenic performance of this second-generation SiGe technology is presented and its suitability for attaining high-gain, broadband cryogenic amplifiers is assessed.

Chapter V (also published in [4]) presents the design of a 24 GHz broadband SiGe HBT limiting amplifier. The amplifier achieves a saturated differential mid-band gain of more than 42 dB and a 3-dB bandwidth in excess 24 GHz for a 10 mV_{pp} (-40 dBm) input. A clear and wide-open eye diagram was measured under 10 Gbit/s operation. The limiting amplifier has a simulated input sensitivity of less than 12 mV_{pp} at a bit error rate (BER) of 10^{-9}. All of the stages of the amplifier employ the modified differential Cherry-Hooper architecture to achieve a broadband gain response. The total power consumption of the chip is 550 mW off of a -5 V power supply. The total chip area is 0.945×0.720 mm^2. This amplifier is compared with other published amplifiers based on a newly proposed figure-of-merit.

Chapter VI presents the Cryogenic characterization of a 24 GHz broadband SiGe HBT limiting amplifier. The S-parameters and the BER of the amplifier was measured across various temperatures from 300 K down to 4.3 K. While the amplifier operated reliably at deep cryogenic temperatures, the BER performance of the amplifier degraded, which is possibly due to increased peaking in the gain response of the amplifier at low temperatures.

Chapter VII (also published in [5]) presents the design of a high-slew rate op-amp in SiGe BiCMOS technology capable of operation across very wide temperature ranges, and down to deep cryogenic temperatures. The first monolithic op-amp (for any material system) capable of operating reliably down to 4.3 K is achieved. Two variants of the SiGe BiCMOS op-amp were implemented, using alternative biasing schemes, and the effects of temperature on these biasing schemes and their impact on the overall op-amp performance,

are investigated.

Chapter VIII (also published in [6]) presents the first demonstration of a SiGe HBT capable of operation above one-half TeraHertz (500 GHz) frequency. An extracted peak unity-gain cutoff frequency (f_T) of 510 GHz at 4.5 K was measured for a 0.12×1.0 μm^2 SiGe HBT (352 GHz at 300 K), at a BV_{CEO} of 1.36 V (1.47 V at 300 K), yielding an $f_T \times BV_{CEO}$ product of 693.6 GHz-V at 4.5 K (517.4 GHz-V at 300 K).

Chapter IX concludes the dissertation with a discussion on possible future work.

CHAPTER II

AN SEU HARDENING APPROACH FOR HIGH-SPEED SIGE HBT DIGITAL LOGIC

2.1 Introduction

SiGe HBTs have proven to be robust to various types of total dose ionizing radiation, as fabricated, in terms of both *dc* and *ac* electrical characteristics, making them potentially attractive for space applications. Recently, however, high-speed SiGe HBT digital logic circuits were found to be potentially vulnerable to single event upset (SEU), and have been examined through both ion beam testing and charge collection modeling. SEU sensitivity in SiGe HBT digital logic, as it is for any bipolar logic, depends on the circuit implementation, and hence one can in principle alter the circuit configuration in order to minimize SEU sensitivity. Previously, a comparison of SEU response in multiple SiGe HBT digital logic circuits indicated that cross-coupling at the transistor level in the storage cell negates any moderate SEU immunity achieved through circuit-level hardening using the current-shared hardening (CSH [17]) technique [16], [31]. Based on this principle an implementation of D-flipflop digital logic with a new circuit architecture featuring limited transistor-level decoupling in the storage cell is proposed and its predicted SEU response is compared with three other circuit architectures [1]. While maintaining the basic functionality of the storage cell of the D-flipflop, the new circuit achieves considerable SEU immunity over the CSH version and the unhardened version of the D-flipflop [31] with little power or real estate overhead.

2.2 Device Technology

The first-generation SiGe HBT employed in this study has a planar, self-aligned structure with a conventional polysilicon emitter contact, silicided extrinsic base, and deep- and shallow-trench isolation. The p-type substrate and the n-p-n layers of the intrinsic transistor form a n-p-n-p multi-layer structure, complicating the charge collection process during ion strikes. This SiGe HBT technology features a peak f_T of 50 GHz and a peak f_{max} of 70 GHz [32]. The p-type substrate is biased at the lowest potential (-5.2 V and -3.3 V in this case) for isolation.

2.3 Device Simulations and Circuit Modeling

MEDICI [33] was used for quasi-3D device simulations of the charge collection mechanisms, which involved using MEDICI in cylindrical symmetric mode [26]. The SiGe HBT doping profile and Ge profile in the base were constructed using measured SIMS data and calibrated to measured *dc* and *ac* electrical characteristics. The ion charge track was generated over a period of 10 ps using a Gaussian waveform. The Gaussian has a 1/e characteristic time scale of 2 ps, a 1/e characteristic radius of 0.2 μm, and the peak of the Gaussian occurs at 4 ps. The depth of the charge track is assumed to be 10 μm, and as substrate doping of $5 \times 10^{15}/cm^3$ was used. A uniform LET of 0.5 pC/μm was used along the charge track in this work. (An LET of 97 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/μm in silicon.) To ensure that the simulated charge profiles were reasonable, the simulations were compared to actual microbeam data for a 36 MeV oxygen ion. The SRIM program was used to estimate the actual LET profile inside the device. As the spatial distribution of this LET profile was non-uniform, it is difficult to compare the net LET to the uniform LET used in the device simulations. However, the total collector-collected charge via device simulation was approximately 800 fC in this case, which is close to the value of 700 fC obtained for the peak charge collected in the collector for an actual 36 MeV oxygen

ion in the microbeam experiment [34]. This agreement between the simulated collector-collected charge and that from actual microbeam data establishes the predictive capability of the model and hence lends credence to the circuit results presented.

The SEU response of the circuits was determined by integrating the ion-induced transient terminal currents obtained from device simulation into a circuit simulation tool via an equivalent circuit model, as shown in Fig. 3 [27]. The current sources in the equivalent circuit model represent the transient terminal currents. The ion-induced transient currents at the emitter and collector are denoted as i_{en} and i_{cn}, where the subscript *n* indicates "electron collection," while those at the base and substrate are denoted as i_{bp}, and i_{sp}, where *p* indicates "hole collection." As the sum of all of the terminal currents is always zero, only three of the four currents need to be included, and the other current is automatically accounted for. Therefore, ion-induced collector current, i_{cn}, is given by

$$i_{cn} = -(i_{bp} + i_{sp} + i_{en}). \quad (4)$$

Thus, this equivalent circuit model allows quasi-mixed-mode SEU simulation in to be performed in a robust manner.

2.4 Circuit Descriptions

A new D-flipflop circuit (called dual-interleaved D-flipflop) was implemented by incorporating duplicate pass and storage cells to effectively produce decoupling of the differential inputs and outputs in the storage cell. The SEU response of dual-interleaved D-flipflop was compared with that of three other D-flipflop circuits, including two unhardened circuits, the standard current mode logic (CML) master-slave (MS) D-flipflop and NAND-based D-flipflop, and a CSH-hardened version of standard CML MS D-flipflop. All of the four circuits have the identical logical functionality of a rising edge-triggered D-flipflop under normal operating conditions (i.e., without SEU).

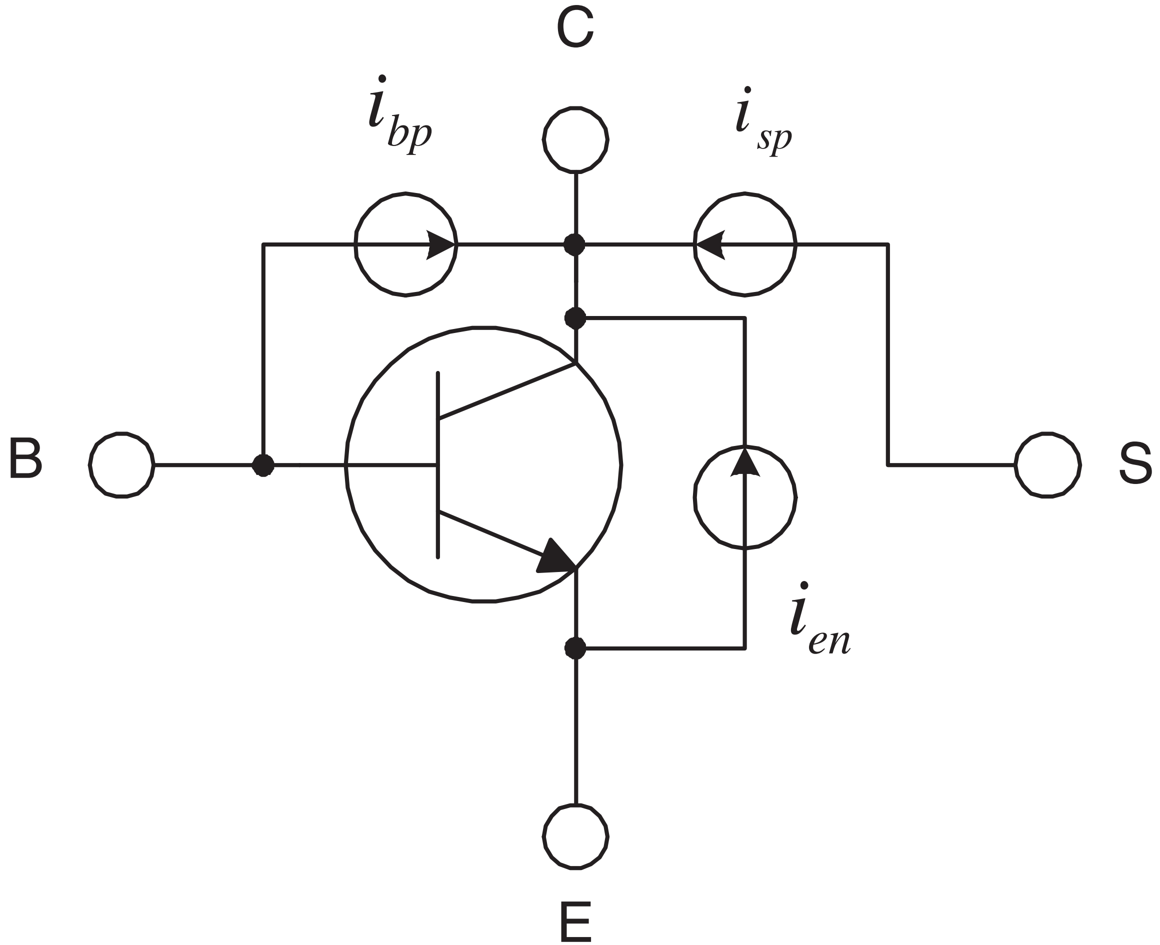


Figure 3: An equivalent circuit model for including the ion-induced terminal currents in the circuit simulations.

2.4.1 NAND-Based D-Flipflop

A straightforward gate-level implementation of the standard rising edge-triggered D flip-flop logic diagram shown in Fig. 4. Each NAND gate in the D-flipflop is implemented using standard differential ECL circuit as shown in inset in Fig. 4. The inputs to the multilevel NAND gate are accordingly level shifted (using level shifters, not shown for brevity) to ensure that all transistors operate in non-saturating region. IN1 and IN2 are the two inputs, and IN1* and IN2* indicate their logic complement. V1 is the NAND gate output, while V2 is the compliment of V1. VCS sets the switching current.

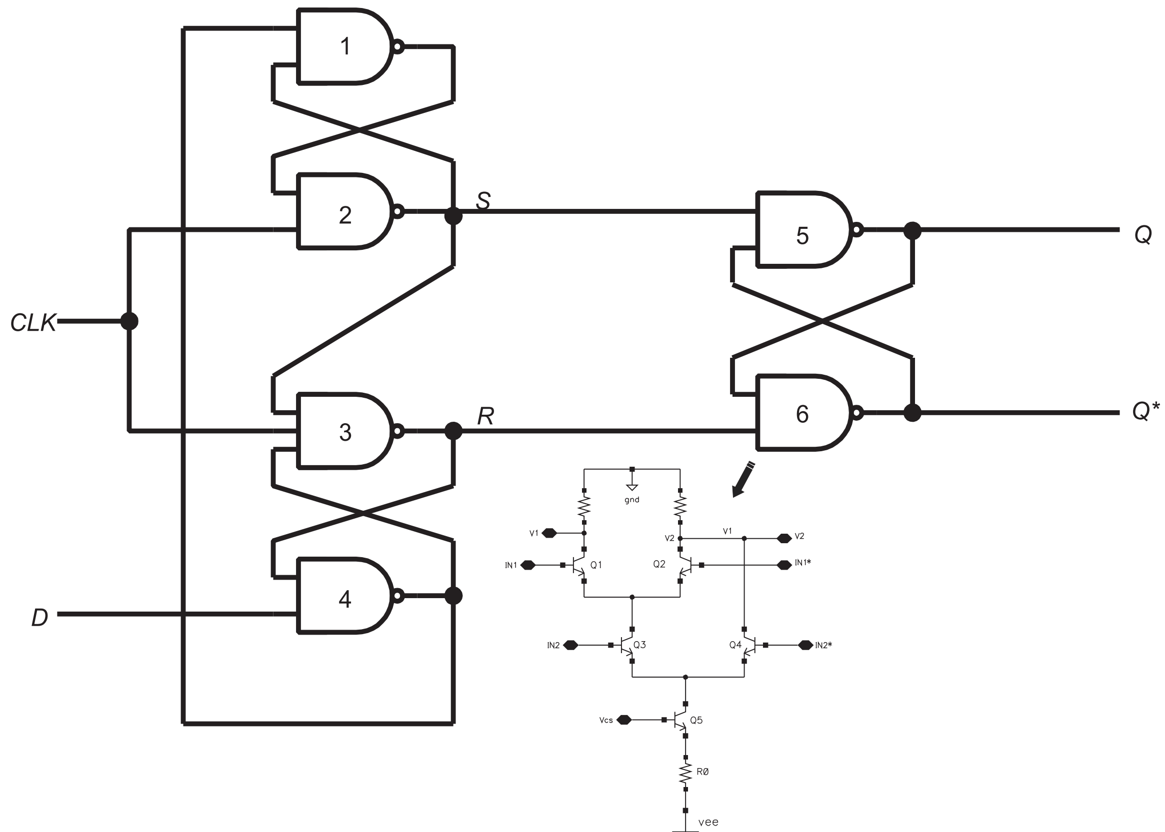


Figure 4: Logic diagram of a conventional rising edge-triggered D-flipflop with the schematic of a two-input NAND gate in the inset.

2.4.2 Standard CML MS D-Flipflop

The standard CML MS D-flipflop is the unhardened version of the D-flipflop used in the shift registers tested in [26]. The transistor level circuit is shown in Fig. 5. Unlike NAND-based D-flipflop, this circuit is not a gate-level implementation of the D-flipflop logic. In addition, it uses a lot fewer transistors than the NAND-based D-flipflop. While NAND-based D-flipflop has 56 transistors, the standard CML MS D-flipflop has 14 transistors, and consumes much less power. The delay in the standard CML MS D-flipflop is only that needed for switching currents in the differential ECL cells, as opposed to individual gate delays in NAND-based D-flipflop and hence best suited for high-speed logic circuits [35]. The circuit consists of a master stage and a slave stage. The master stage consists of a pass cell (Q1 and Q2), a storage cell (Q3 and Q4), a clocking stage (Q5 and Q6), and a biasing

control (Q7). The transistors in the pass and storage cells are stacked over the CLK and control transistors. Hence, the input levels at the clock stage and the control have to be level shifted for the transistors to operate in forward active mode while conducting. The slave stage has a similar circuit configuration. The storage cell of the master stage and the pass cell of the slave stage are controlled by CLK, and the pass cell of the master stage and the storage cell of the slave stage are controlled by CLK*.

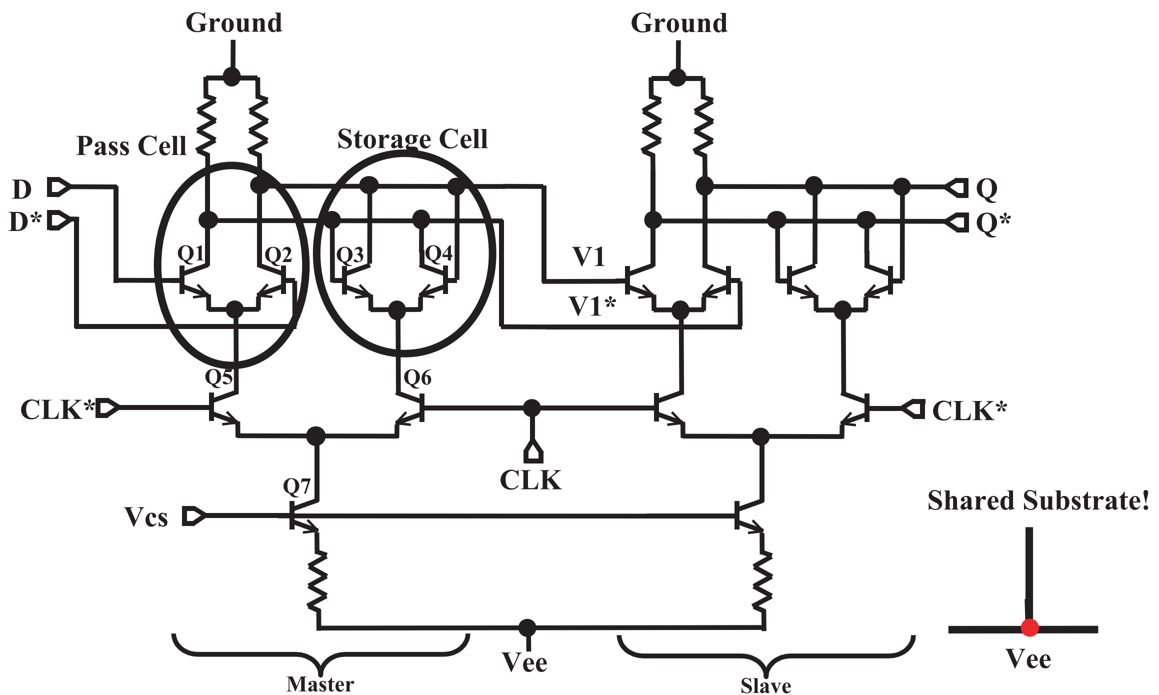


Figure 5: The standard CML MS D-flipflop.

2.4.3 Current-Shared Hardened D-Flipflop

The current-shared hardened (CSH) version of the standard CML MS D-flipflop was used as a basic building block of the 32 stage shift-register tested in [16]. Each transistor element in Fig. 5 was implemented with a five path CSH scheme (Fig. 6). These five current paths remain separate through the clocking stage and through the storage and pass cells until the load. The transistors in the storage and pass cells, however, eventually share the same load.

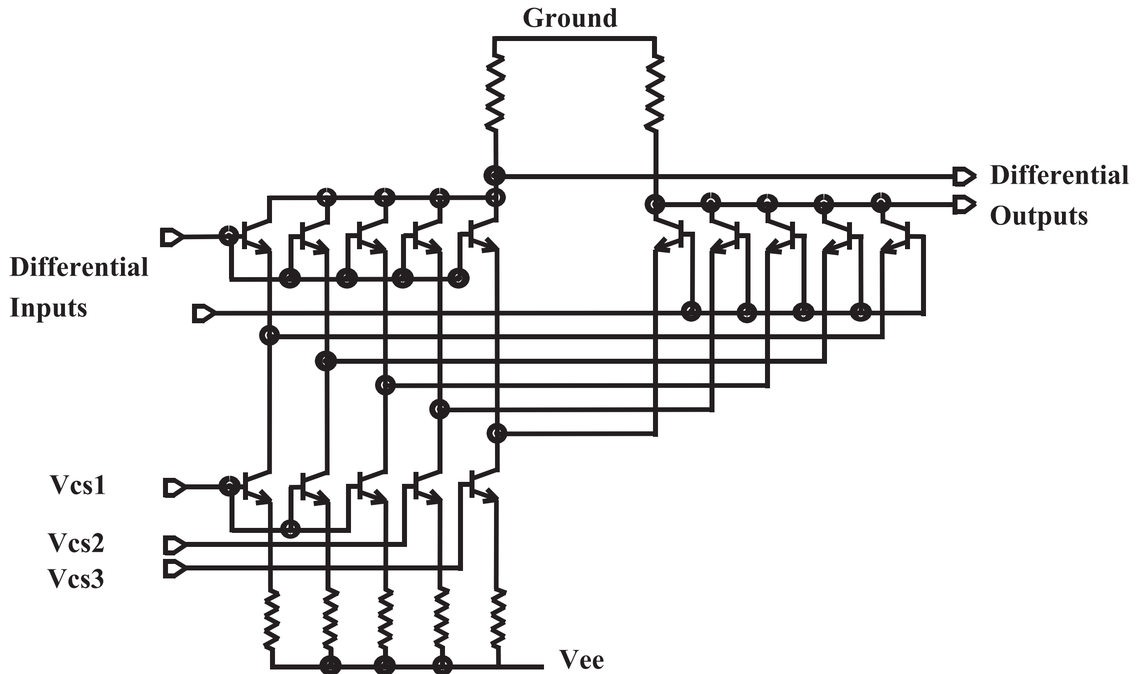


Figure 6: Illustration of current-sharing hardening (CSH) concept using a basic CML gate.

2.4.4 Dual-Interleaved D-Flipflop

Dual-interleaved D-flipflop, the new circuit, implements limited decoupling of the storage cell transistor inputs (base) and outputs (collector) in the master and the slave stages of the flip-flop, as shown in Fig. 7. This circuit is very similar to the standard CML MS D-flipflop, except for the presence of duplicate pass and storage cells. Although the dual-interleaved circuit may appear simply to be two standard CML MS D-flipflops wired in parallel, a careful examination of the connections in the storage cell shows that this is not the case. While the collectors of Q5 and Q6 are connected to the collectors of Q3 and Q4, the bases are connected to the collectors of Q1 and Q2, respectively. In the case of two D flip-flops wired in parallel, however, one would expect the collectors and bases of Q5 and Q6 to be connected to the collectors and bases of Q1 and Q2 in Fig. 5, and likewise for Q7 and Q8.

This new configuration maintains the basic functionality of the storage cell of storing

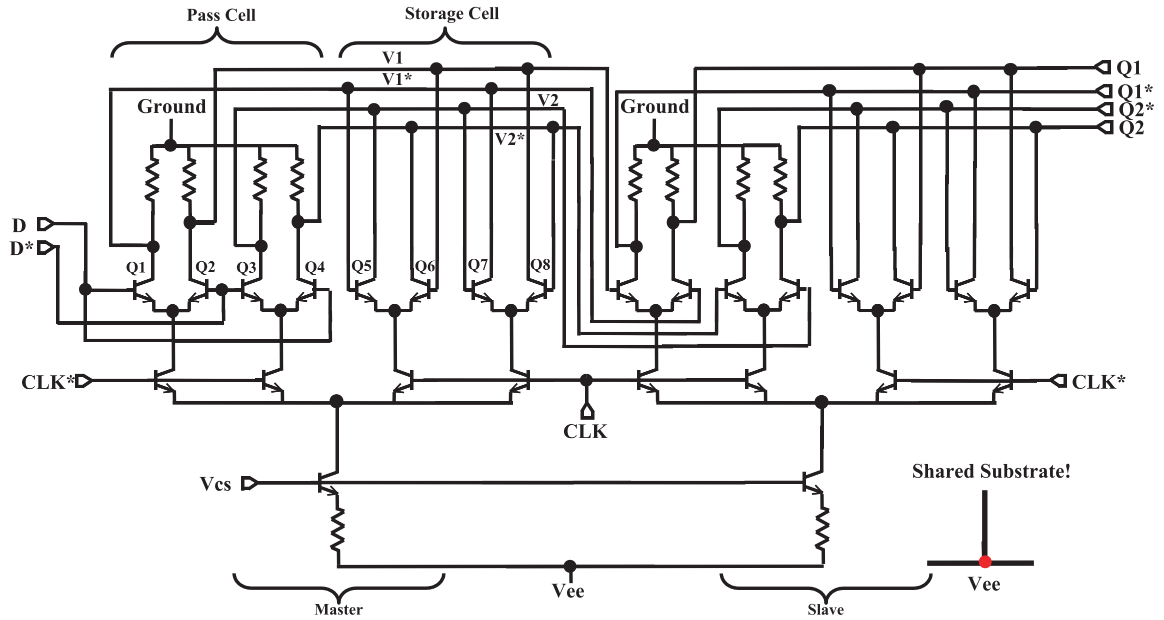


Figure 7: The dual-interleaved D-flipflop with minimal cross-coupling in the storage cell.

data when the clock goes high. Effective decoupling is achieved by not connecting the base and the collector of the transistors in the storage cell to the same differential pair in the pass cell. For example, the base of Q5 is connected to the collector of Q1, whereas the collector of Q5 is connected to the collector of Q3 (note that the base and collector of each transistor in the storage cell are connected to complementary outputs from the pass cell, which is essential for storage cell functionality). Thus, if SEU transient current flows through the collector of the transistor Q5, the base is unaffected by this current flow. The voltage drop due to this transient flow does affect the base Q7, however, which might indirectly affect the base of Q5, potentially leading to upset.

2.5 Circuit Simulations

Circuit transient response simulations were performed using the Spectre simulator in Cadence, using calibrated VBIC compact models for the SiGe HBT in the SiGe BiCMOS design kit from IBM. The transistor being subjected to an ion strike is replaced with the equivalent circuit model (Fig. 3) and the ion-induced transient terminal currents are turned

on during the course of the transient simulation.

Simulations were performed at three different data rates (2, 4, and 6 Gbit/s). The simulations for the various circuits were made at a constant switching current of 1.5 mA. To study the effect of variable switching current on SEU response, simulations were also performed at a 0.5 mA fixing the data rate at 2 Gbit/s. The input data was an alternating train of '1' and '0' bits, and the voltage swing was maintained at 300 mV (swinging between -300 mV and 0 V) in all the circuits, irrespective of the switching current or the data rate.

The upset-sensitive transistors in each D-flipflop circuit were identified (as described in [31]) and ion-induced transient currents were activated on these transistors. In each circuit, the transient currents were triggered just before the rising clock edge, when the data is still '0', since this condition was determined to be worst case. Such conditions occur at 5.460 ns after the start of the simulation for data rates of 2 and 6 Gbit/s for 1.5 mA switch current, and at 5.535 ns for 4 Gbit/s at 1.5 mA switching current.

2.6 *Results and Discussion*

2.6.1 Performance Analysis

Table 4 shows the trade-off between power consumption and the number of transistors required to implement the various circuits. The power consumption of all the circuits are computed relative to the power consumption of the standard CML MS D-flipflop (Fig. 5) at a switching current of 0.5 mA (designated as P).

Table 1: Power consumption and number of transistors in the circuits.

Topology	Power Consumption		Number of transistors
	Switching Current=1.5mA	Switching Current=0.5mA	
Std. CML MS	3P	P	14
CSH CML MS	3P	P	70
Dual-interleaved	6P	2P	26
NAND MS	12P	4P	56

The SEU response of each circuit at three different data rates were compared for a fixed

switching current of 1.5 mA. Figures 8-10 show the simulated SEU responses for standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at three data rates simulated here. The SEU response is measured in terms of bit error rate (BER) (or alternatively, recovery time).

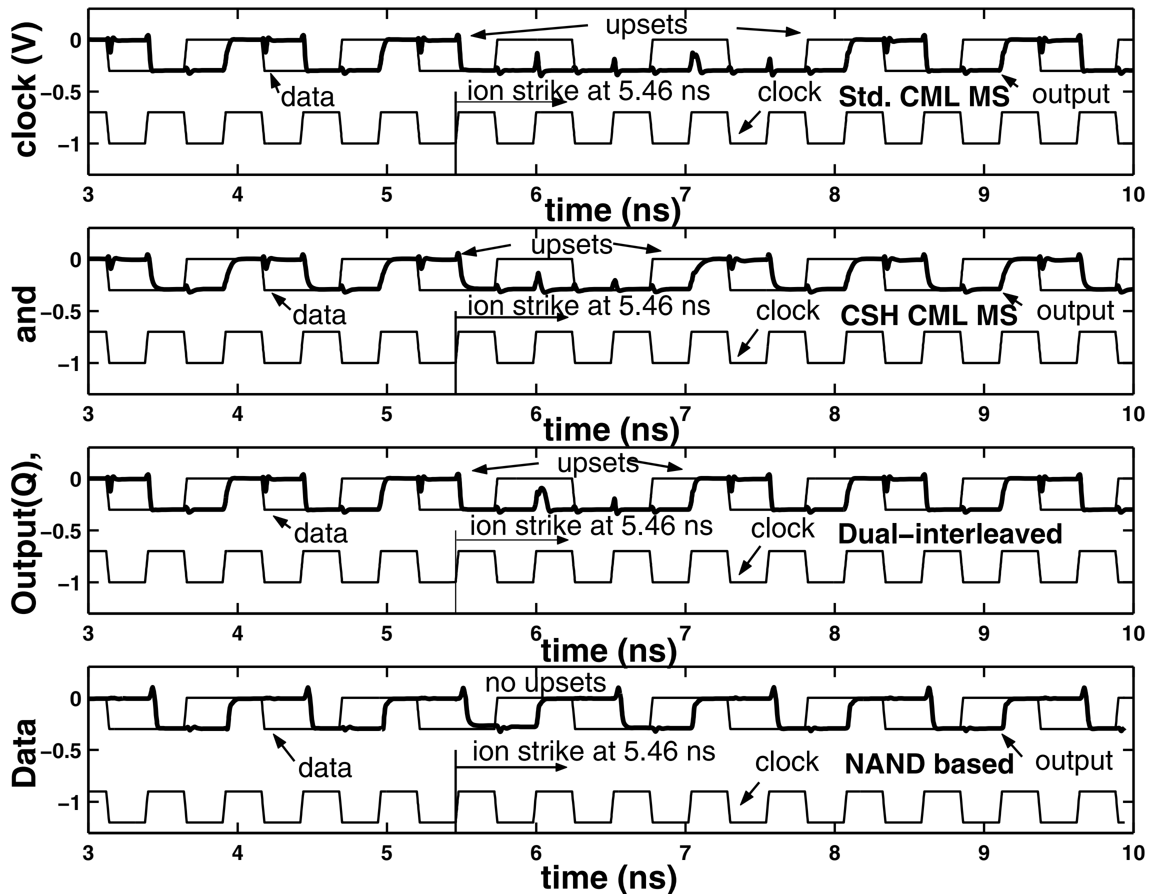


Figure 8: Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 2 Gbit/s (LET=0.5 pC/μm and switch current is 1.5 mA).

The standard CML MS D-flipflop, as expected, shows the maximum number of upset bits across all data rates. Although CSH CML MS D-flipflop shows slightly better SEU response at 2 Gbit/s, at 4 Gbit/s and 6 Gbit/s, it has a performance similar to the standard CML MS D-flipflop. NAND-based D-flipflop shows the best performance compared to all the circuits, with no upsets at any data rate. It is clear from the SEU response at higher data

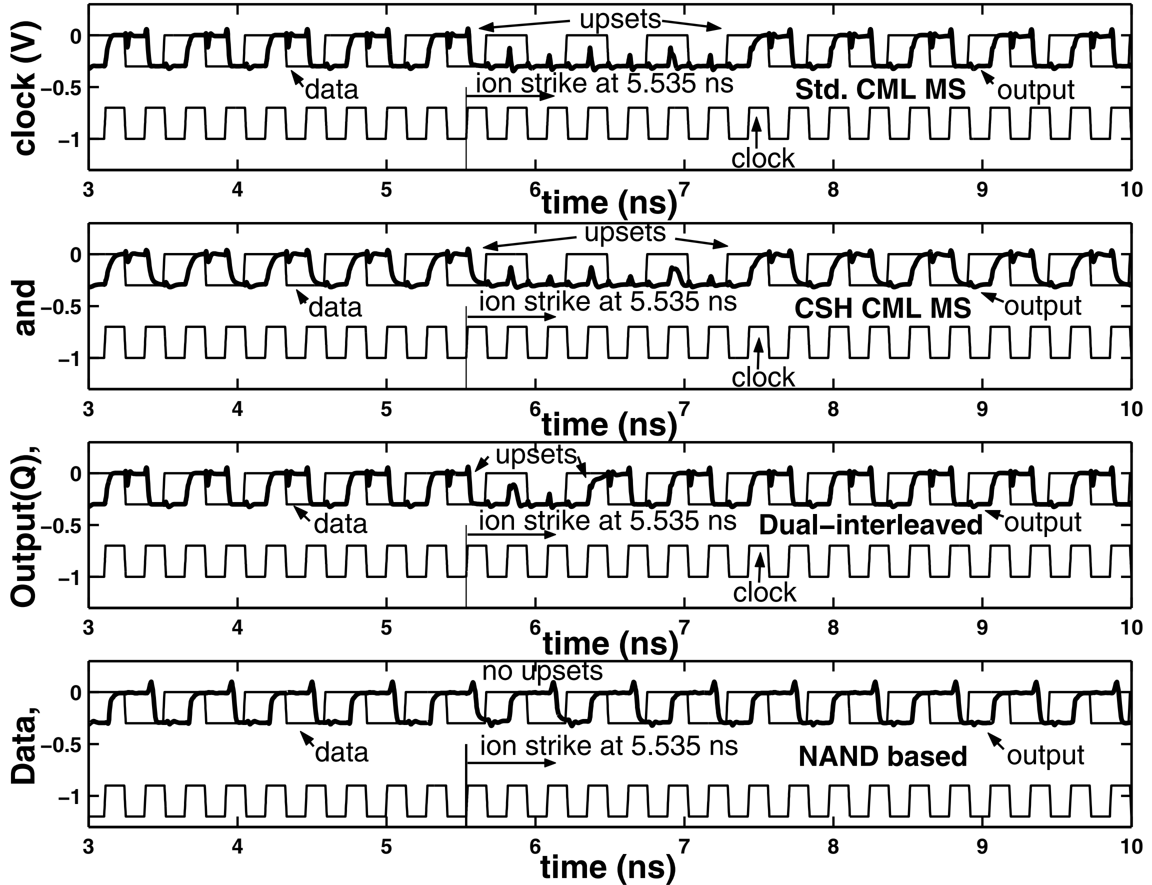


Figure 9: Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 4 Gbit/s (LET=0.5 pC/μm and switch current is 1.5 mA).

rates, however, that with just half the power consumption of NAND-based D-flipflop and with many fewer transistors, a significant improvement in SEU response can be achieved (BER or recovery time) using the new dual-interleaved architecture.

The circuits were also operated at a switching current of 0.5 mA with the data rate maintained at 2 Gbit/s, as shown in Fig. 11. It can be seen that in general the SEU performance has degraded significantly in all of the circuits, with NAND-based D-flipflop (which showed no upsets for any data rate at 1.5 mA switching current) now showing upsets.

Figure 12 summarizes the SEU results of the four circuit architectures using as a metric the number of upset bits/unit power consumption as a function of data rate.

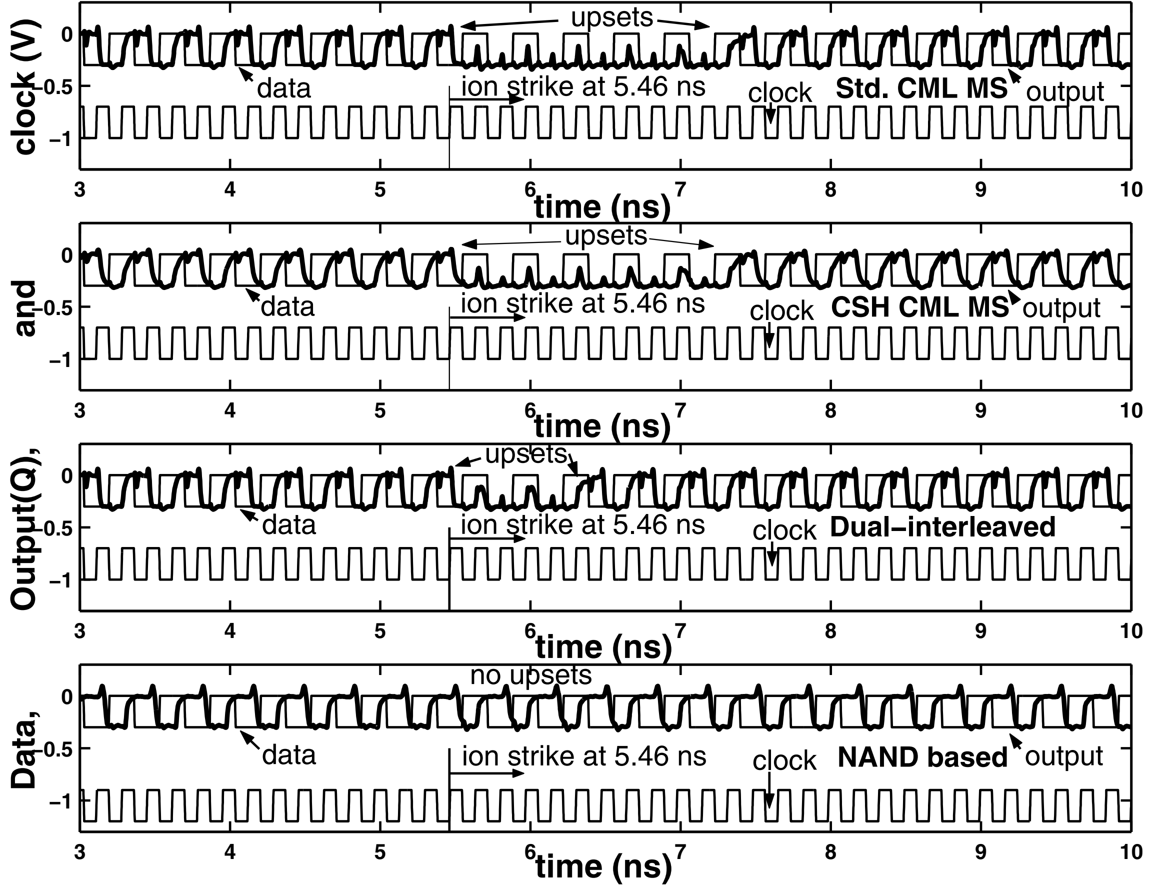


Figure 10: Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 6 Gbit/s (LET=0.5 pC/μm and switch current is 1.5 mA).

2.6.2 Understanding the Results

In any current-steering logic, the input signal to one of the transistors of the differential pair is compared with either a static reference voltage (single-ended input) or the complementary input signal (differential input) at the input of the other transistor. All the circuits investigated in this work operate with a differential input signal. In the storage cell of standard CML MS D-flipflop (and its CSH version), the input (base) of the transistor Q3 is connected to the output (collector) of the transistor Q4 (and Q1) (Fig. 5). Similarly, the input to transistor Q4 is connected to the output of the transistor Q3 (and Q2). This cross-coupling of the inputs and outputs of the differential pair in standard CML MS D-flipflop

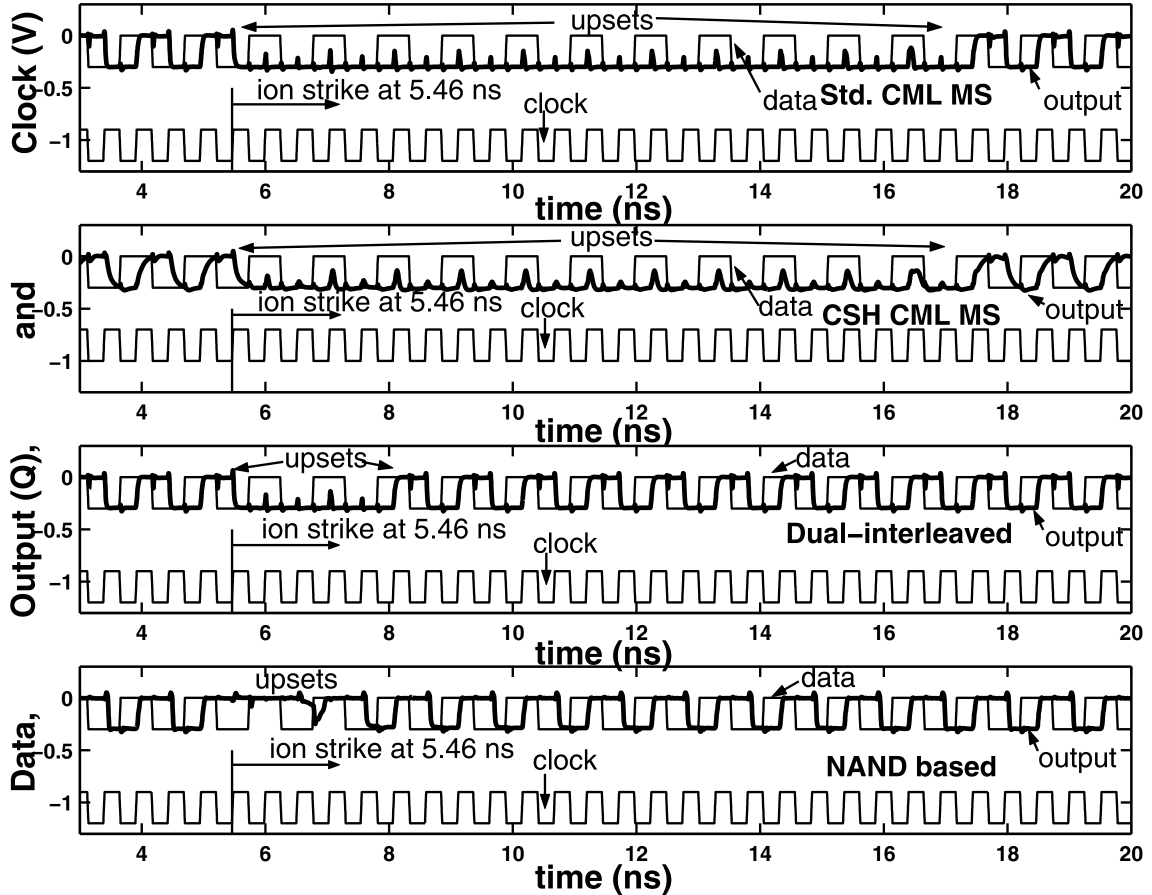


Figure 11: Data, output, and clock waveforms of standard CML MS, its CSH version, dual-interleaved, and NAND-based D-flipflops at a data rate of 2 Gbit/s (LET=0.5 pC/μm and switch current is 0.5 mA).

and its CSH version, which is essential for latching, presents a strong positive feedback, as previously pointed out [31]. As a result, an upset occurring at the output of any of the transistors in the storage cell influences the other transistor to an equal and opposite extent, reinforcing the upset in the differential output. This explains the poor SEU tolerance in the standard CML MS D-flipflop and its CSH version at both switching currents and at all data rates. In the CSH version, although the current paths are maintained as separate through the clocking stage, and pass and storage cells, the loads are shared (as in standard CML MS D-flipflop), effectively making this circuit equally vulnerable to SEU.

In NAND-based D-flipflop, however, where this transistor-level cross-coupling within

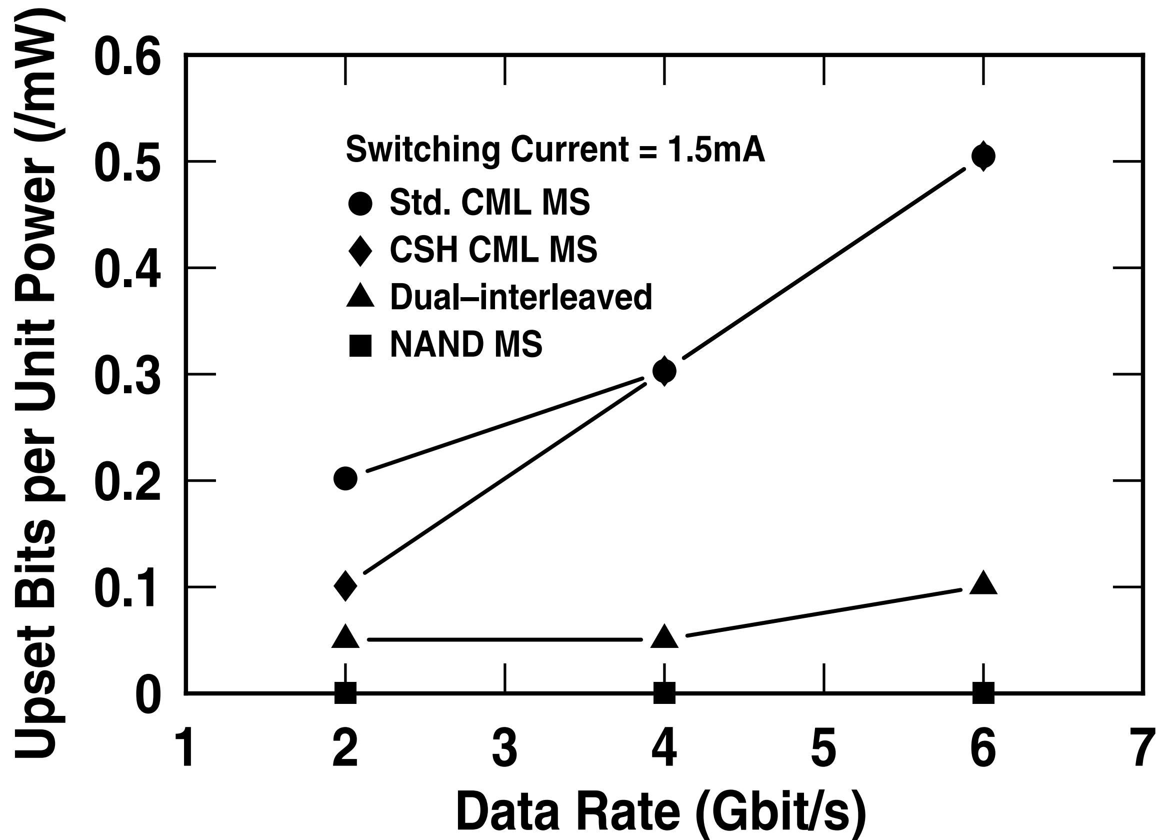


Figure 12: Summary comparison of the four circuit architectures using as a metric, the number of upset bits/ unit power consumption as a function of data rate.

a differential pair is entirely absent, there is no significant upset at the output due to SEU transient currents. The differential outputs are independent of each other, and therefore upset occurring in one of the outputs does not affect the complement output. As long as the differential output is above the cell switching threshold, the output remains unaffected, and no SEU upset occurs. However, it is worth pointing out that the storage cells in this type of D-flipflop still incorporate cross-coupling between gates required for latching, but there is no cross-coupling within a differential pair as such.

The analysis of the SEU response in standard CML MS, its CSH version, and NAND-based D-flipflops indicate that if one of the inputs to the storage cell differential pair is unaffected by SEU, no significant SEU is seen at the differential output. In NAND-based

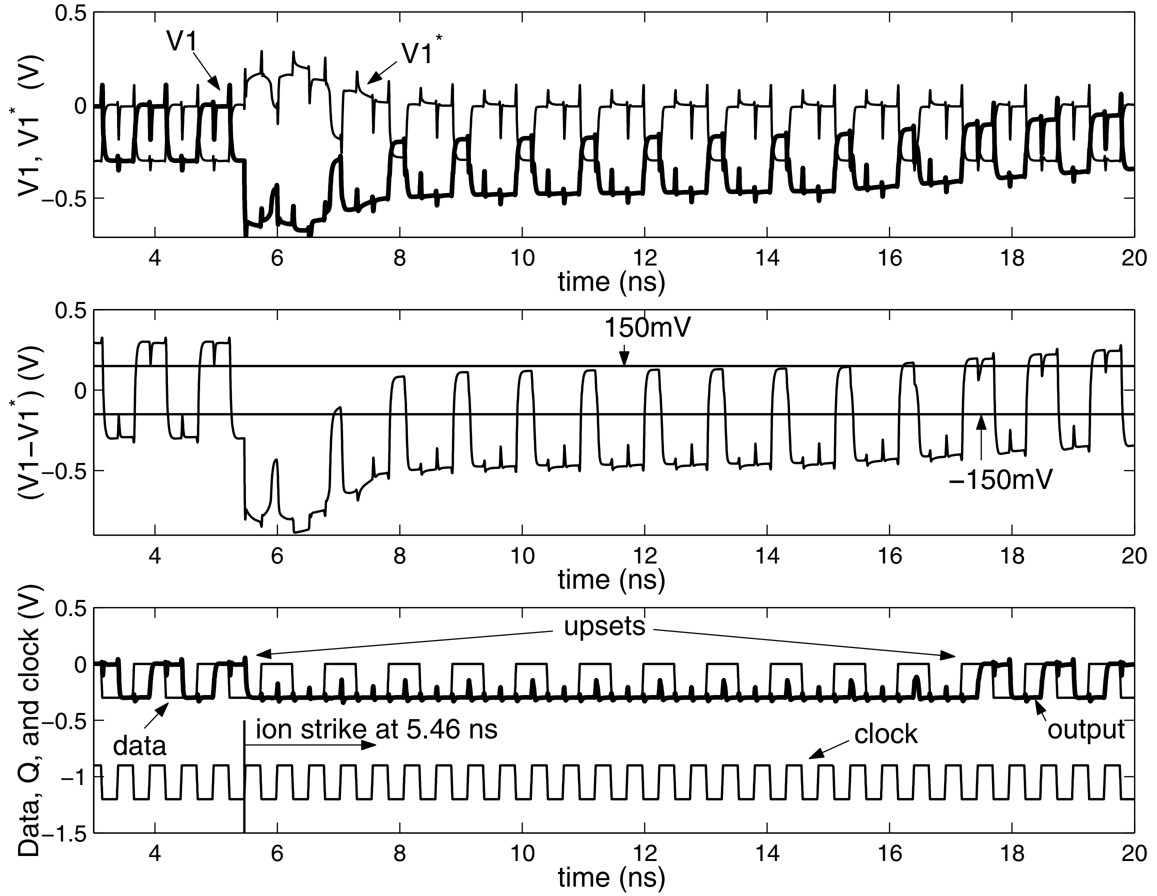


Figure 13: Single-ended and differential output voltages for the differential pair in the storage cell struck by heavy ion in standard CML MS D-flipflop (switch current is 0.5 mA).

D-flipflop this condition is always satisfied, while in standard CML MS and its CSH version, it is always violated. The very high power consumption of NAND-based D-flipflop (Table 4), however, might preclude its use in space applications. In dual-interleaved D-flipflop, the above-mentioned condition for SEU tolerance is partially satisfied due to the use of duplicate pass and storage cells (Fig. 7). The use of duplicate pass cells present independent loads to the input and output of transistors in the storage cell. To maintain the basic functionality of the storage cell, however, a positive feedback is still needed, and therefore, cross-coupling between transistors having same logic level but from different storage cells (as explained above) is required. Hence, upsets, although significantly fewer

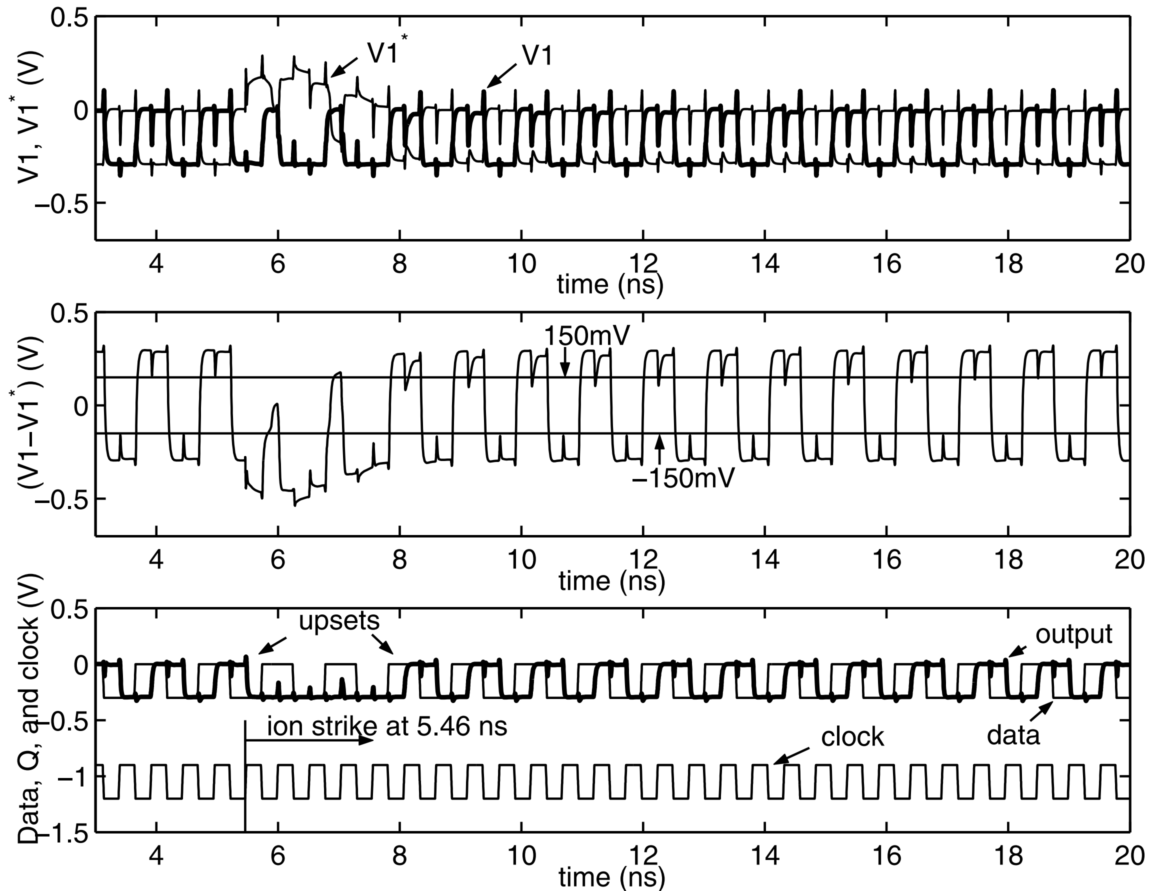


Figure 14: Single-ended and differential output voltages for the differential pair in the storage cell struck by heavy ion in dual-interleaved D-flipflop (switch current is 0.5 mA).

than in standard CML MS and its CSH version, can still be seen at the output.

Figures 13-15 show the differential output of the storage cell at 0.5 mA switching current. It is clear from these figures that both the outputs are affected to an equal and opposite extent in standard CML MS D-flipflop. In dual-interleaved and NAND-based D-flipflops, however, only one of the outputs is affected. In dual-interleaved D-flipflop (Fig. 14), soon after triggering the SEU transient currents, when the clock goes high and when there is upset in one of the terminals, there is also upset in the opposite terminal (for example, the change in V1 slightly after 6 ns). This upset occurs due to pass cell of the slave stage turning on as a result of the clock going high, and since V1* is high (due to upset), V1 goes low.

The degradation of the overall SEU response at low switching current is due to large load resistance needed to maintain the voltage swing, and hence due to a lower switching threshold. The same SEU transient current now flows through this larger load resistance, leading to a more pronounced upset. In dual-interleaved (and NAND-based) D-flipflop, however, the differential output of one of the storage cells, V1 and V1* (V2 and V1 in NAND-based D-flipflop), are not affected to the extent to which they are affected in standard CML MS D-flipflop and its CSH version. Therefore, fewer upsets occur in dual-interleaved and NAND-based D-flipflops at low switching current.

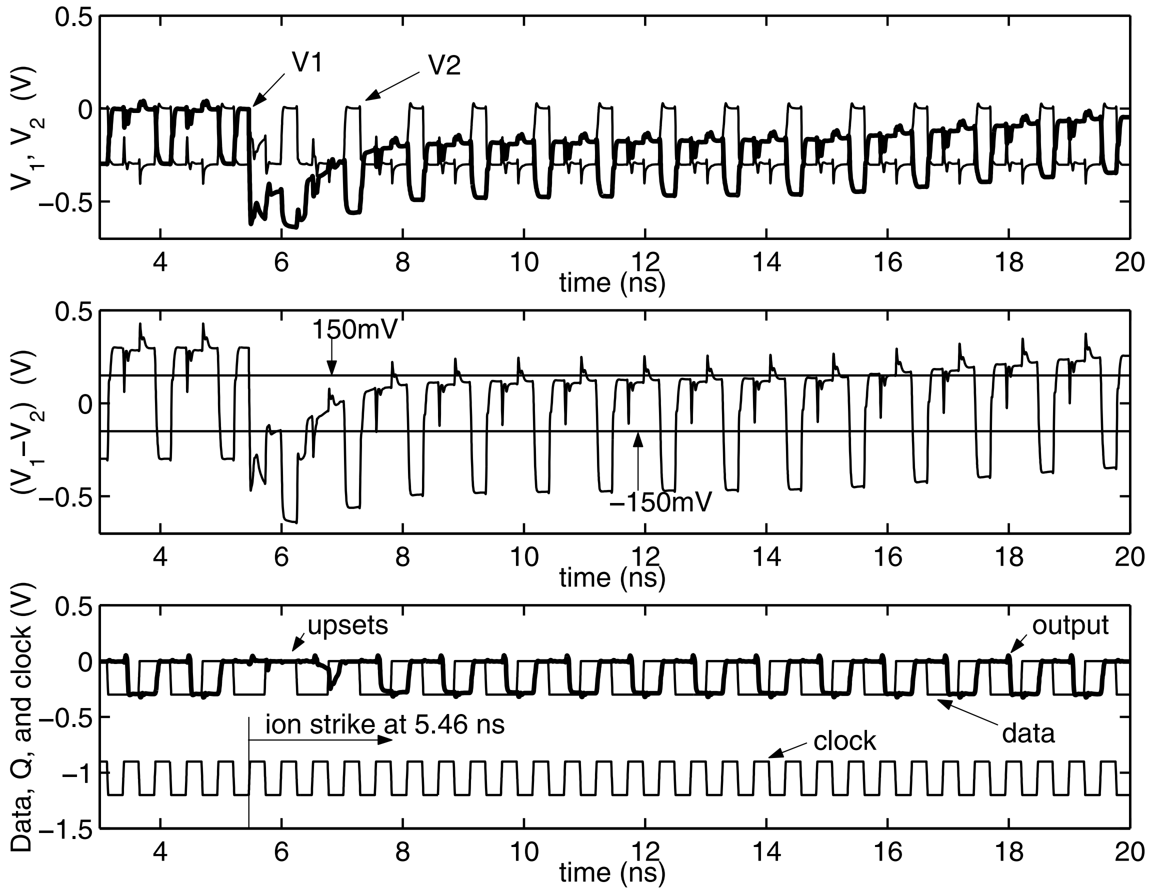


Figure 15: Single-ended and differential output voltages for the NAND gate struck by heavy ion in NAND-based D-flipflop (switch current is 0.5 mA).

2.7 Summary

A new circuit architecture for high-speed SiGe HBT digital logic having moderate SEU tolerance is implemented by partial decoupling of the differential output. The SEU response of this circuit architecture is compared with the response of three SiGe HBT D-flipflop architectures, including two unhardened D-flipflops and the CSH version of the standard CML MS D-flipflop. The performance of this new circuit is comparable to the NAND-based D-flipflop that has no transistor level cross-coupling, but at much lower power consumption and fewer transistor count. The significant improvement in SEU response seen in the new circuit, which is obtained by guidelines laid out in [31], further validates these earlier conclusions. Together, these results suggest a potential path for achieving sufficient SEU tolerance in high-speed SiGe HBT digital logic for many space applications. The realization of 16-bit shift registers based on these D-flipflops and the ion beam results obtained for these shift registers will be discussed in the next chapter.

CHAPTER III

APPLICATION OF RHBD TECHNIQUES TO SEU HARDENING OF THIRD-GENERATION SIGE HBT LOGIC CIRCUITS

3.1 Introduction

Silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology has generated considerable interest in the space community due to its robustness to total ionizing dose (TID) radiation, without any additional hardening [30]. This TID tolerance does not, unfortunately, translate into improved single event upset (SEU) response for SiGe HBT logic. Digital circuits designed in first-generation (50 GHz) and second-generation (120 GHz) SiGe technology have been shown to be very sensitive to SEU [16], [36], [37], [38], and circuit-level hardening using the current-shared hardening (CSH) [17] technique proved ineffective in mitigating single event upsets in these circuits.

Radiation-hardening-by-design (RHBD) employs layout and circuit architecture changes for the radiation hardening of space electronic systems using commercial foundry processes, without requiring design rule violations or process modifications [29]. In this work, the RHBD techniques have been applied to improve the SEU immunity of SiGe HBT high-speed logic circuits [2].

3.2 SiGe HBT BiCMOS Technology

Shift registers featuring these RHBD techniques were realized for the first time in the commercially-available IBM SiGe 8HP BiCMOS technology platform. This process incorporates a 130 nm "raised extrinsic base" SiGe HBT structure with an $in-situ$ doped polysilicon emitter, deep- and shallow-trench isolation. The SiGe HBT has a peak unity-gain cutoff frequency (f_T) of 200 GHz [39]. The technology also integrates 130 nm CMOS devices as well as a wide array of passive elements and seven layers of metalization.

3.3 SiGe RHBD Techniques

3.3.1 Circuit-Level Techniques

Three different types of 16-bit shift registers in the current mode logic (CML) family were investigated. The clock "tree" architecture in these shift registers was identical to the one used in shift registers reported in [36], with a master clock buffer driving four intermediate clock buffers, each in turn providing clock inputs to a set of 4 D-flipflops (Fig. 16). Thus, as was noted in [36], an upset occurring in the clock tree has the potential to cause multiple bit upsets. Therefore, to improve their SEU immunity, the clock buffers in the present designs featured circuit-level hardening based on the gated-feedback cell (GFC) RHBD technique [28]. Two RHBD local circuit-redundancy-based circuit-level hardening techniques were employed in the design of the constituent D-flipflops in two of the three shift registers, while the remaining shift register, referred to as "standard MS SR" ("std. SR"), featured unhardened conventional CML master-slave (MS) D-flipflops (Fig. 5), and was used as the baseline circuit (control) to enable meaningful comparisons. To study the effects of reduced bias current on the SEU characteristics of the shift registers, low-power (I_{tail} = 0.5 mA) and high-power (I_{tail} = 1.0 mA) versions were implemented. I_{tail} is the tail current of any differential pair in the D-flipflops. Upon complete switching the current flowing through the load resistor connected to the transistor that is on is very close to I_{tail}.

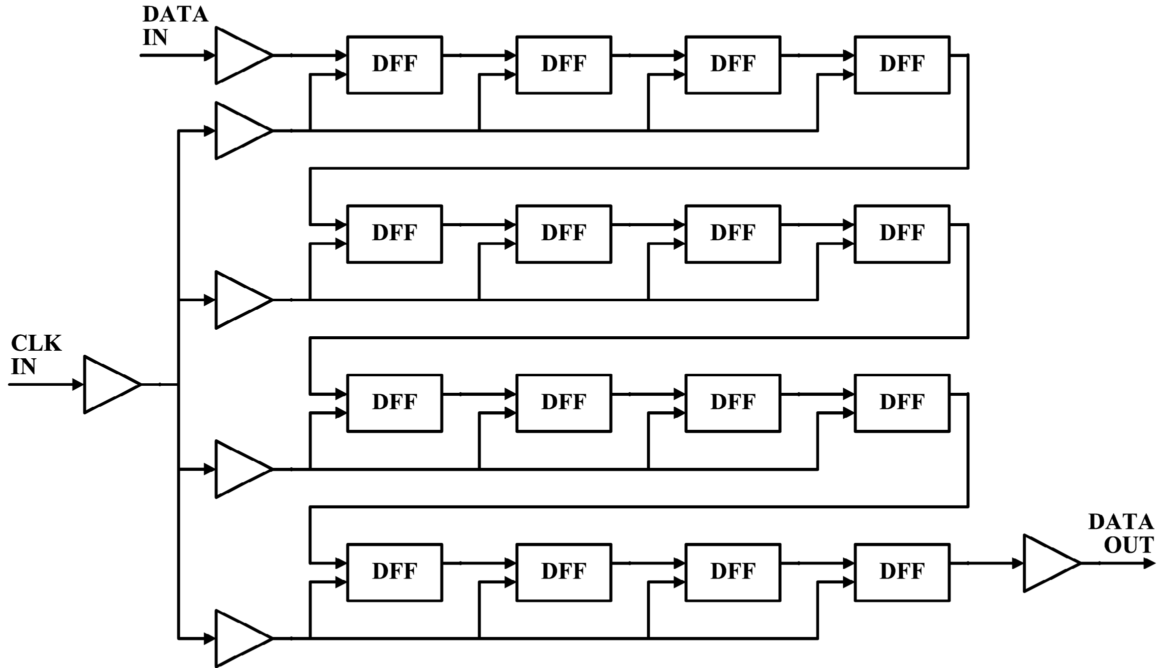


Figure 16: Block diagram of the 16-bit shift registers.

3.3.1.1 Dual-Interleaving-Based RHBD

One of the RHBD shift registers incorporated D-flipflops based on the newly proposed circuit implementation [1], introduced in Chapter II, referred to here as "dual-interleaved SR" or "DI SR" (Fig. 7). A previous study [31] on the dependence of SEU response on circuit architecture in the CML logic family indicated that cross-coupling at the transistor-level, required for the storage cell functionality in the standard master-slave D-flipflop (Fig. 5), increases the vulnerability of this circuit to SEU. Thus, local redundancy was built into the standard master-slave D-flipflop, which consumes the least power and occupies the smallest area, to incorporate limited transistor-level decoupling in the storage cell, thereby mitigating its SEU sensitivity with only a moderate increase in power consumption and circuit complexity.

Unlike the standard MS SR, the base and the collector of the transistors in the storage cell of the DI SR are not connected to the same differential pair in the pass cell, thus achieving effective decoupling of the base and collector terminals of the transistors in the

storage cell. For instance, the base of Q5 in DI SR storage cell is connected to the collector of Q1 in the pass cell, whereas the collector of Q5 is connected to the collector of Q3 of the alternate differential pair in the pass cell. However, to maintain the storage cell functionality, the base and collector of each transistor in the storage cell are connected to complementary outputs from the pass cell. Thus, an SEU transient current flowing through the collector of the transistor Q5 does not affect the base directly. The voltage drop due to this transient flow, however, does affect the base of Q7, which might indirectly affect the base of Q5, potentially leading to upset [1].

3.3.1.2 Gated-Feedback Cell-Based RHBD

The other RHBD shift register featured a slightly modified gated-feedback cell (GFC)-based master-slave D-flipflop [28], referred to here as "GFC SR" (Fig. 17). The OR-gates available in the GFC architecture perform a logical OR operation on identical logic outputs from the pass cell pair and feed the result back to the appropriate inputs of the duplicate storage cell pair. The OR operation, enabled by a pair of emitter followers, helps transmission of the correct logic to the storage cell inputs even when one of the OR gate inputs is in error via an ion strike.

The output of a two input OR gate changes state only when both the inputs change state from high to low or low to high. An ion strike on an npn transistor, in general, causes ion-induced current to flow into the collector, thereby pulling the collector potential low. Therefore, an ion strike on a storage cell transistor such as Q5 causes its collector and in turn the input to transistor Q9 to go low. This spurious transition, however, does not affect the output of the OR as the other input to Q10 is unaffected. In addition, the inputs to Q11 and Q12 (transistors in the alternate OR gate) are also unaffected, thereby ensuring the correct logic at the input (or base) of Q5. Thus, the OR-gate-based feedback to the storage cell inputs, in addition to local redundancy, is in principle expected to offer SEU immunity that is higher than that provided by dual-interleaving. In addition, there are diode voltage

clamps positioned across the load resistors to increase the current onto an upset collector node, thus reducing the upset duration [28], [43].

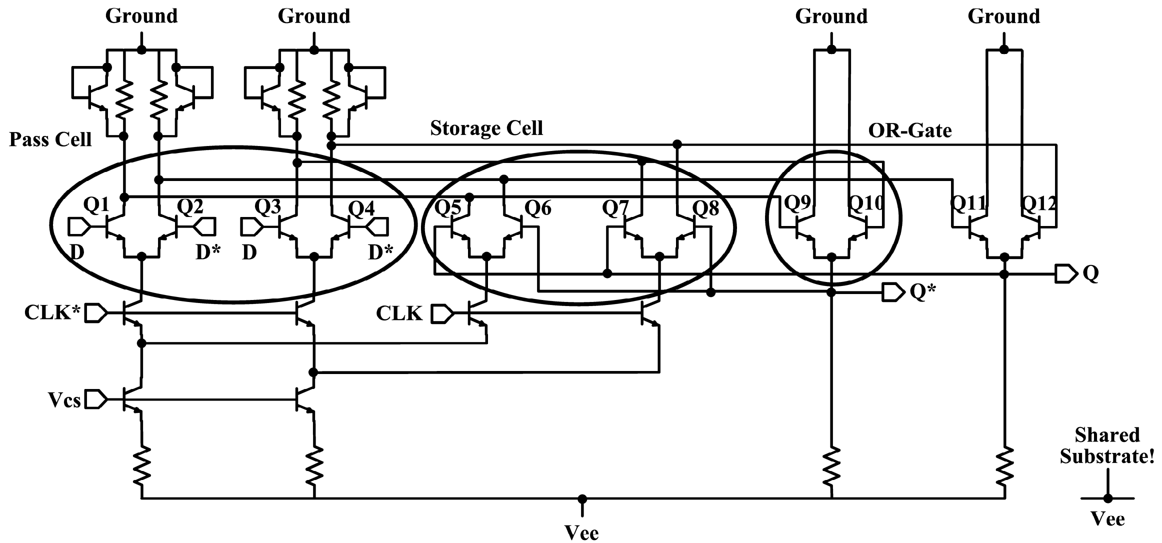


Figure 17: Schematic of master stage of the GFC D-flipflop.

3.3.1.3 Register-Level RHBD

Additional register-level RHBD based on triple module redundancy (TMR) was applied to the low-power versions of DI SR and GFC SRs (referred to as DI TMR and GFC TMR, respectively), to gauge the performance improvement achieved from this additional level of RHBD. The output was selected based on majority voting between three redundant shift registers using GFC-hardened and unhardened voters working in parallel (Fig. 18). Separate select lines (S1-S3) were provided for enabling or disabling individual shift registers in the circuit to test their functionality.

3.3.2 Device-Level RHBD Techniques in SiGe HBTs

A previous microbeam study on second-generation SiGe HBTs concluded that the active region defined by the deep-trench (DT) boundary is only a portion of the upset sensitive volume and that the remaining sensitive volume encompasses the region of substrate several micrometers away from the trench [37]. Despite this observation, reduction in

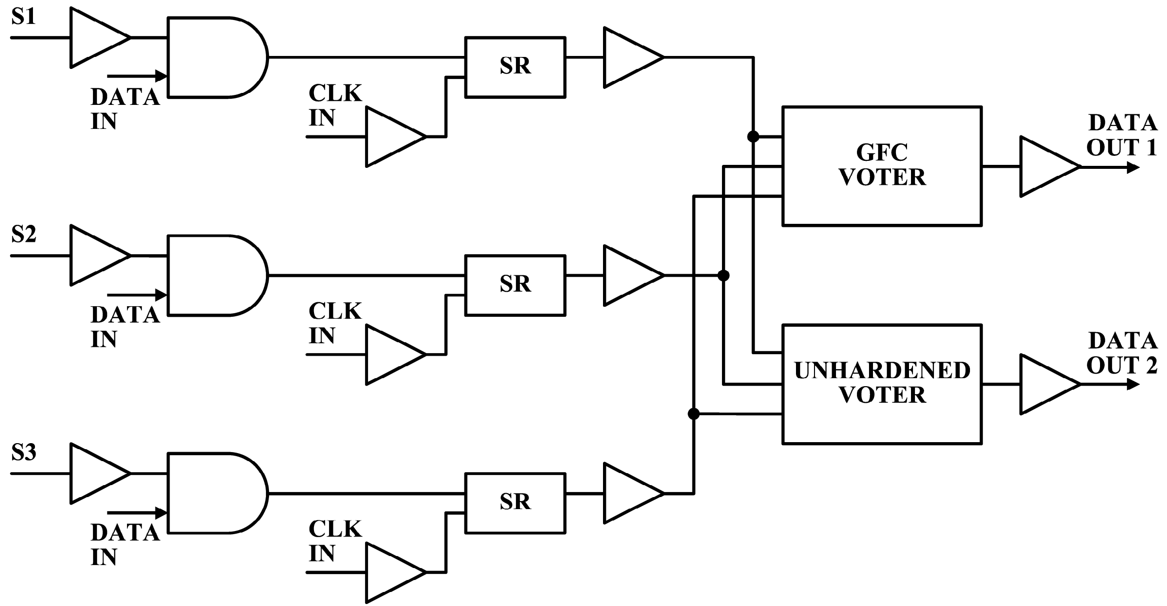
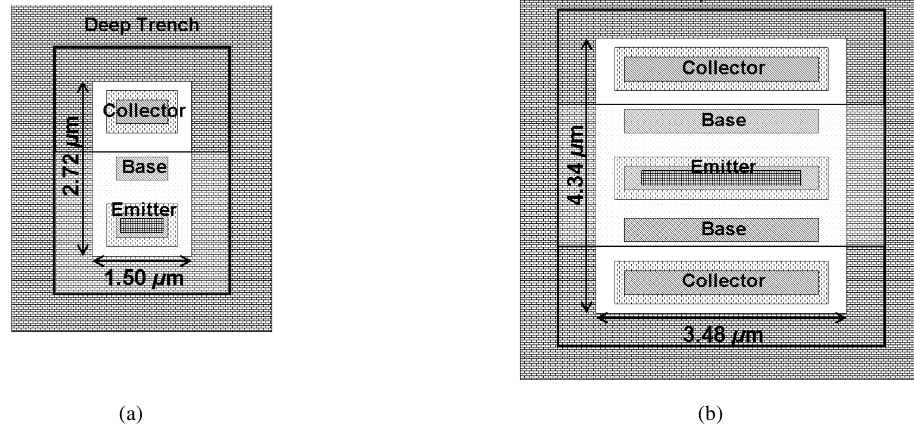


Figure 18: Block diagram of the triple module redundancy (TMR) implementation.

area enclosed by DT is expected to significantly improve the net upset cross-section of the transistor by reducing the effective sensitive area [44]. Thus, a transistor with minimum feature size, and with only a single collector, base, and emitter contacts (C-B-E), as opposed to the standard device with double collector and base contacts (C-B-E-B-C), was selected as the workhorse RHBD device to minimize local ion-induced upset cross-section within the RHBD latches. While the C-B-E-B-C device with an emitter area (A_E) of 0.12 × 2.50 μm^2 was used in the baseline standard MS SR, the RHBD (C-B-E) device with A_E of 0.12 × 0.52 μm^2 was employed in all other shift registers. Only a slight *ac* device performance penalty resulted. The internal trench area for the C-B-E-B-C was 15.10 μm^2 while that for the RHBD C-B-E devices was 4.08 μm^2. Thus, the net reduction in trench enclosed area for the RHBD SiGe HBT was about 73%. A bigger C-B-E-B-C device was intentionally used in the baseline circuit to demonstrate the degradation in upset cross-section associated with larger trench volume (Fig. 19(a) and (b)).

The various hardening techniques investigated are summarized in Table 2. In addition,



(a) (b)

Figure 19: (a) RHBD C-B-E transistor and (b) C-B-E-B-C transistor used in the baseline Std. SR.

the total power consumption of the various shift registers, the contribution of individual D-flipflop to the total power consumption, the D-flipflop area, and the maximum post-layout simulated speed are tabulated in Table 3. Clearly, the operating speed of low-power DI SR and the power consumption of its constituent D-flipflops are comparable with those of the standard SR with only a slight area penalty overhead and with minimal increase in layout complexity, suggesting that dual-interleaving can potentially be applied to other technology nodes. RHBD shift registers with much higher operating speeds than those presented here are clearly possible in this technology [45]. The primary reason for the more modest operating speeds for the present shift registers lies in the (intentional) overdesign of the latch output buffers, which caused significant internal capacitive loading. This can easily be altered as needed for specific speed requirements without compromising SEU performance. For instance, simulations using more standard buffers for the DI SR can be clocked to well above 20 GHz speeds. The die photomicrographs of a 16-bit shift register and its TMR implementation are shown in Figs. 20(a) and (b). The die area of 16-bit shift registers is 2.356×1.586 mm^2 and the die area of the TMR version is 2.636×2.686 mm^2, and dictated by the high-speed packaging fixture used.

Table 2: Comparison of hardening techniques.

Topology	Circuit Technique
Std SR	unhardened
DI SR	latch-level redundancy + limited decoupling
DI SR Low-P	latch-level redundancy + limited decoupling
DI TMR	three DI SR + voting at end
GFC SR	latch-level redundancy + OR-gate feedback + load diode clamps
GFC TMR	three GFC SR + voting at end

Topology	Device Technique	
	Type	Emitter Area (μm^2)
Std SR	C-B-E-B-C	0.12×2.50
DI SR	C-B-E	0.12×0.52
DI SR Low-P	C-B-E	0.12×0.52
DI TMR	C-B-E	0.12×0.52
GFC SR	C-B-E	0.12×0.52
GFC TMR	C-B-E	0.12×0.52

Table 3: Comparison of power consumption, area, and speed.

Topology	D-flipflop I_{tail} (mA)	Power (mW)		D-flipflop Area ($\times 10^3$ μm^2)	Max. Sim. Speed (Gbit/s)
		Total	Flipflop		
Std SR	0.5	257	11	10	6
DI SR	1.0	506	19	16	8
DI SR Low-Power	0.5	399	12	16	7
DI TMR	0.5	1136	19	16	5
GFC SR	1.0	729	40	25	8
GFC TMR	0.5	1945	33	25	5

3.4 Test Setup

The shift registers (devices under test – DUT) were designed at Georgia Tech, and packaged at the Mayo Foundation. Two sets of heavy ion tests were performed at the Texas A&M Cyclotron Institute. In the first iteration the DUTs were subjected to Ne, Ar, and Xe ions at 15 MeV/amu. This was followed up with a second iteration where the DUTs were subjected to 15 MeV/amu Kr ion to obtain SEU response at the intermediate LET values. The angle of incidence of ion beam was increased from normal incidence (0°) to 45° and 60° to vary the effective LET for a given ion. The DUTs, being serial shift registers, are

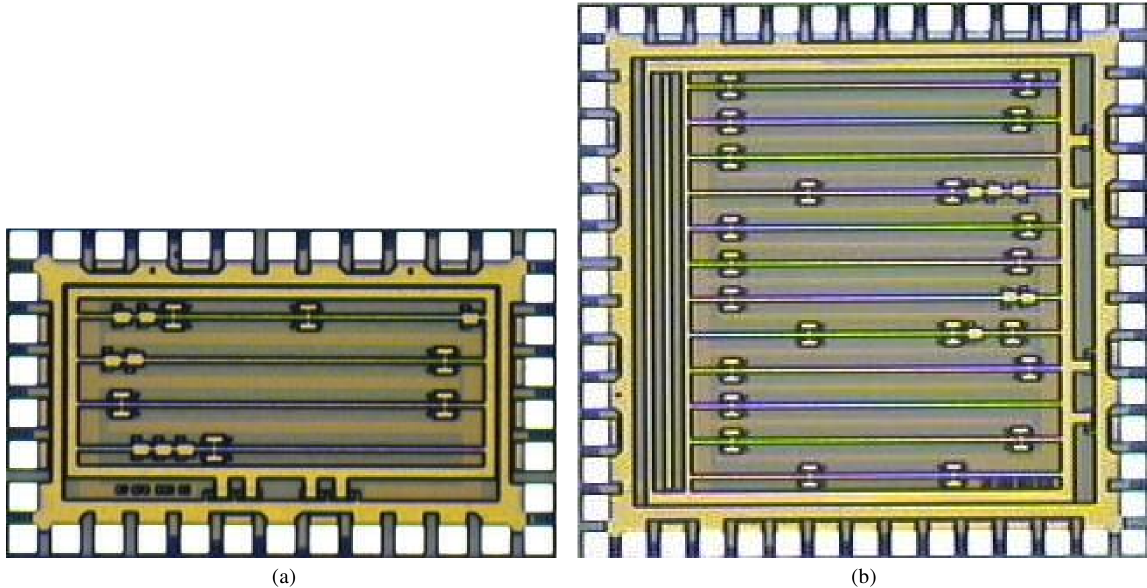


Figure 20: Die micrograph of a 16-bit shift register (a) and its TMR implementation (b).

ideal for standard bit error rate test (BERT) methods. The test set consisted of, fundamentally, a data source and an analyzer to examine the output of the DUT (Fig. 21). The data source was a custom-built, pseudorandom number (PRN) generator, which generated $2^7 - 1$ long bit patterns. An Anritsu MP1764A, a 12.5-Gbit/s BERT analyzer, which can count bit errors and save the transmitted data stream in the vicinity of errors, was used. The data rates were continuously variable from 50 Mbit/s up to the maximum frequency of operation of a given DUT, and error information was acquired at several data rates of interest. A computer running Labview under Windows XP controlled the equipment, gathered the data, and provided some real-time data analysis. Further, the clock and data inputs were driven differentially with voltage swings compatible to CML voltage levels. Additional equipments such as a balun, 6 dB splitters, delaylines, and bias-Ts were used to derive differential clock and data signals from a single RF source.

3.5 Heavy Ion Data & Analysis

Figures 22-24 show the heavy ion-induced event cross-section (σ) as a function of effective LET for all circuits tested in this work, at various data rates. Event cross-section is

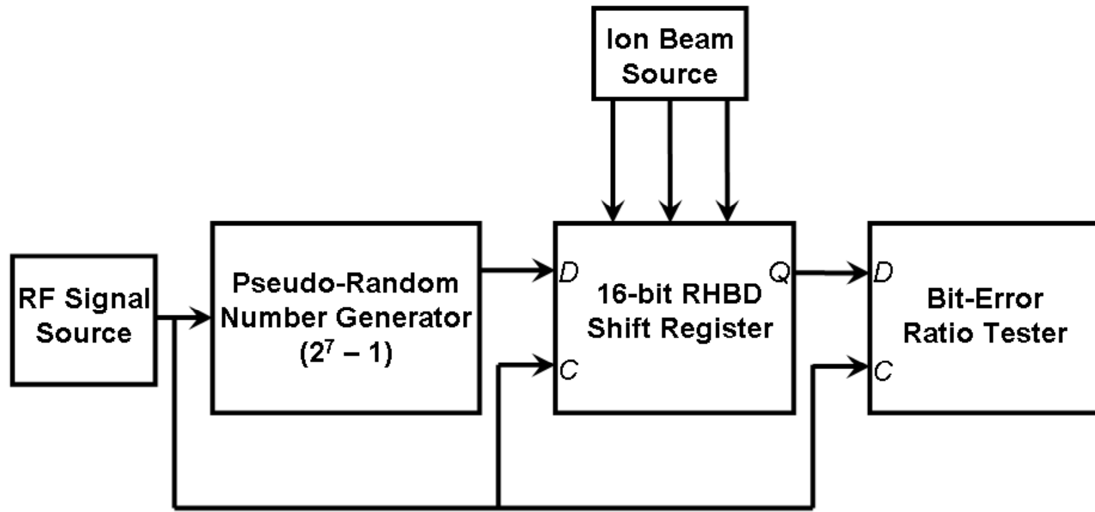


Figure 21: Block diagram of the heavy-ion test-setup for SEU characterization of 16-bit RHBD shift registers.

chosen for representation of upsets to decouple the effect of varying error durations and to present only the physical ion-circuit interactions. As expected, the baseline standard MS SR displays the highest saturated device cross-section (σ_{sat}) across all data rates (Fig. 22-24). The downward pointing arrows at LETs of 2.8, 5.8, and 12 MeV-cm^2/mg in Fig. 22 correspond to limiting cross-sections (i.e., no upset bits) associated with the RHBD DI TMR, GFC SR, and DI SR, respectively. Interestingly, the low-power version of the DI SR, despite having the same I_{tail} as the standard MS SR, but with twice as many sensitive nodes, shows >2.5x lower σ or equivalently 60% reduction in σ (Fig. 22-24) at almost all data rates. This improvement in σ is, however, higher than the estimated 1.85x improvement or equivalently 46% net reduction in σ. The 1.85x improvement in σ was estimated by combining the 73% "reduction" in transistor upset cross-section associated with using RHBD CBE SiGe HBTs in DI SR and the expected 2x degradation in σ attributable to

the 2x more sensitive nodes in the DI SR compared to standard MS SR. The potential reason for higher achieved improvement could be due to the "immunity" provided by the circuit hardening technique. This simplified analysis does not account for charge collection from outside the deep-trench, which was concluded to be significant in second-generation SiGe HBTs [37]. This simplification further disregards the "function-related" sensitivity of individual transistors in the circuit observed in a previous work, which, however, also concluded that larger transistors present larger sensitive area [44]. The high-power version of the DI SR, as expected [46], showed significantly better performance over the low-power DI SR version at lower data rates, to a lesser extent at higher data rates, across all ion LETs. The high-power GFC SR showed the better σ_{sat} performance over DI SR at low data rates and progressively degraded as the frequency increases, but always remained better than or comparable to that of the DI SR.

The heavy ion test data showed limiting cross-sections in both "double RHBD" DI TMR and GFC TMR at 1 Gbit/s (and at higher data rates) up to an LET of 75 MeV-cm^2/mg (Fig. 22). However, at data rates below 100 Mbps in GFC TMR and below 50 Mbps in DI TMR the SEU response degraded considerably. Despite this anomalous low data rate behavior, the fact that TMR offers significant improvement in the SEU response of the shift registers is in itself an important and encouraging result. Interestingly, the TMR in GFC SR did not provide as much improvement in σ at low speeds as the TMR in the DI SR (Figs. 23 and 24). In addition, the σ of GFC TMR was worse than that of high-power GFC SR at low data rates. Although this observation could possibly be explained based on the reduced bias current in the constituent shift registers, it is still puzzling to note that register-level redundancy and voting had little effect in improving the overall SEU immunity at low data rates, given that the GFC SR in itself had the best performance among non-TMR shift registers. That said, cross-section data for low-power GFC SR would be required for a more meaningful comparison.

Figures 25 and 26 show that the event cross-section of all the shift registers except

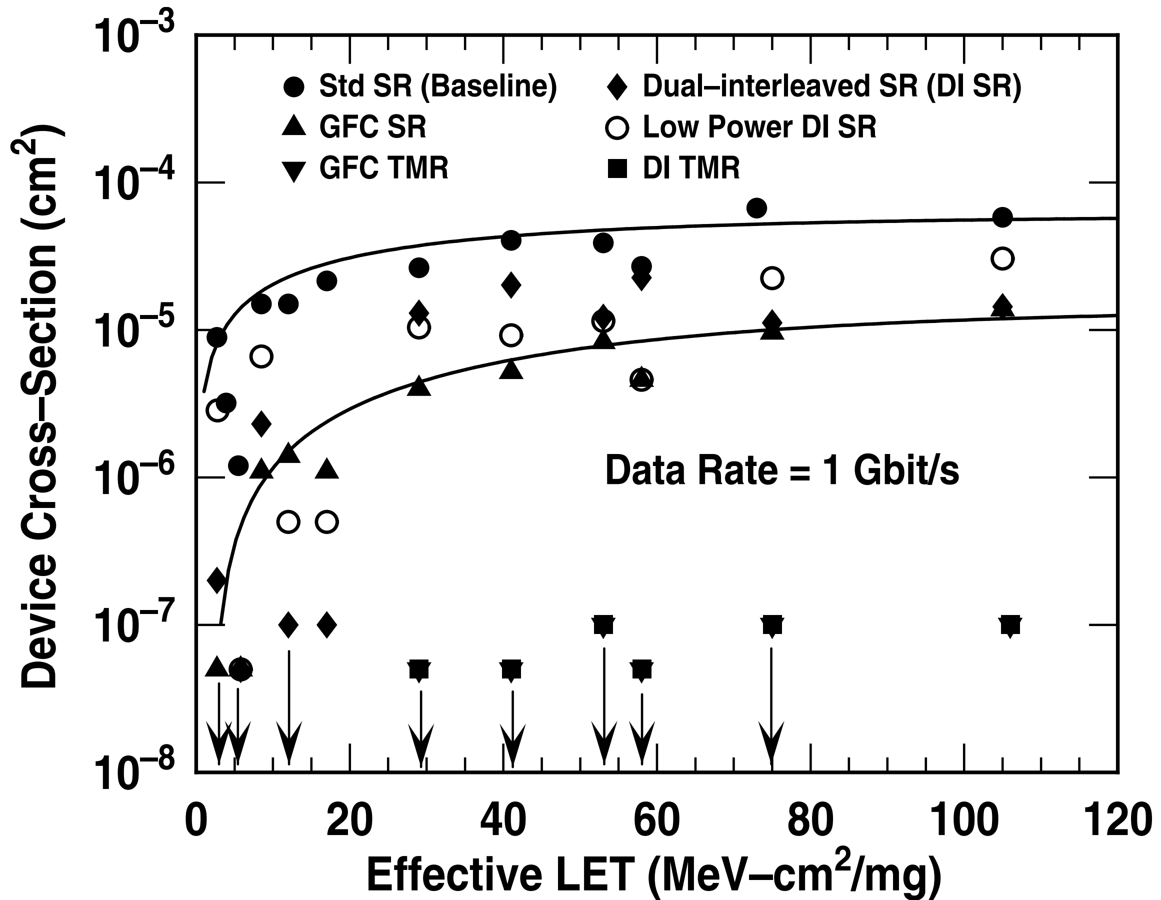


Figure 22: Device cross-section (σ) as a function of effective LET for data rate = 1.0 Gbit/s.

the DI TMR and GFC TMR increases with frequency at LETs values of 8.5 and 53 MeV-cm^2/mg, respectively, which is in agreement with a previous study in first-generation SiGe shift registers [16] and consistent with clock edge related SEU sensitivity. This result is evidently in disagreement with results from a previous study using second-generation SiGe technology [38], in which even though σ increased with data rate at low frequencies, a saturation of σ was noted at higher frequencies.

Figures 27, 28, and 29 capture the average error per error event as it varies with the data rate, at LETs of 8.5, 29, and 53 MeV-cm^2/mg, respectively. It is clear at LETs of 29 and 53 MeV-cm^2/mg that average errors in all of the circuits except the TMRs increases with data rate, linearly from a value of 1 at low data rates to as high as 8 at 4 Gbit/s in the

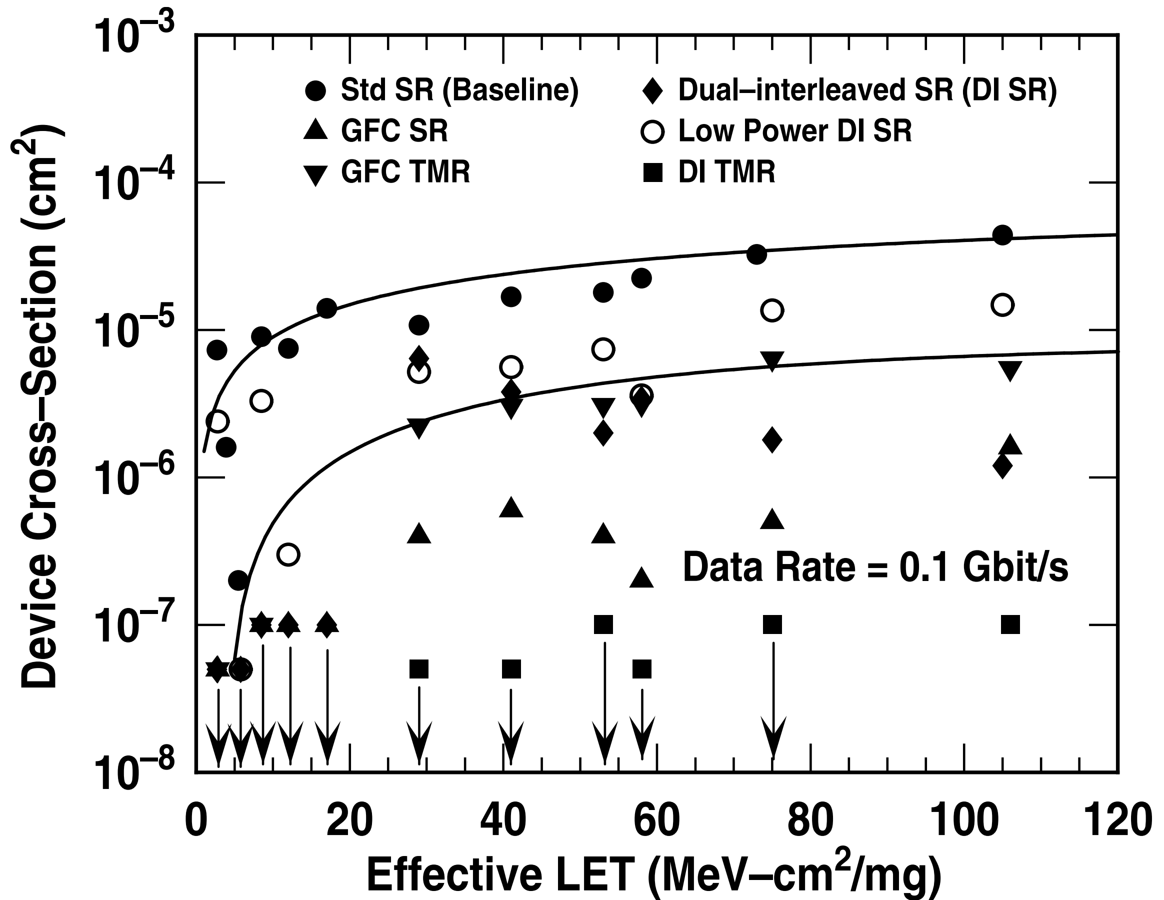


Figure 23: Device cross-section (σ) as a function of effective LET for data rate = 0.1 Gbit/s.

unhardened standard SR. All other circuits show relatively lower average errors per event compared to the standard SR, which could possibly be due to lower upset durations in these circuits, hence resulting in lower temporal multiple bit errors. At low LETs (Fig. 27), however, average errors did not show a linear increase with data rate, except in the case of the standard SR. In fact, the average errors remained close to 1 to data rates as high as 2 Gbit/s, indicating short upset durations. Interestingly, there were no errors observed at data rates above 100 Mbps for LETs as high as 75 MeV-cm^2/mg in the TMR shift registers and at low data rates for lower LET values in GFC SR and DI SR (Figs. 27, 28, and 29). Under such conditions average errors per event was assumed to be 0.

Table 4 gives a summary of the SiGe RHBD results, including threshold LETs of the

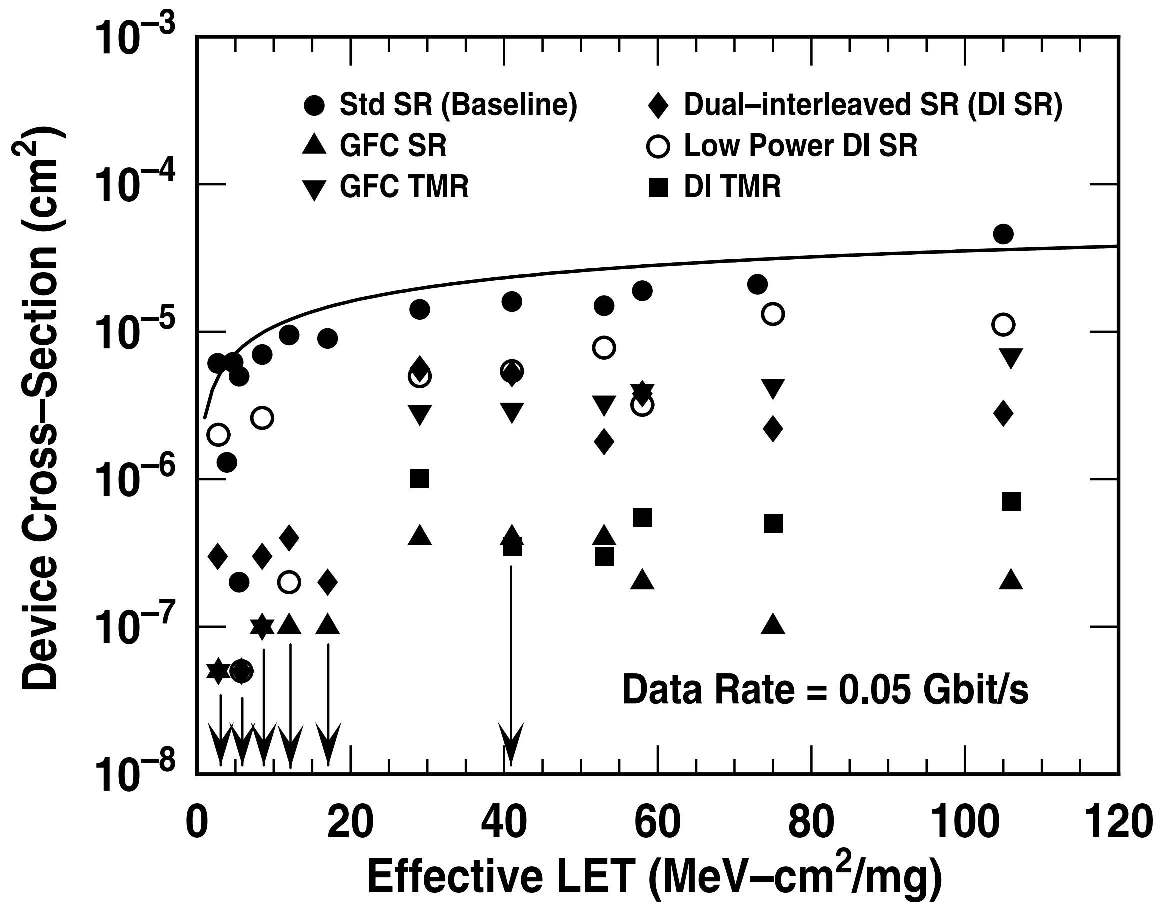


Figure 24: Device cross-section (σ) as a function of effective LET for data rate = 0.05 Gbit/s.

various circuits. These LET thresholds were estimated in two different ways; by fitting of a standard Weibull curve to the data (L_{th}), and by using the LET value at 10% ($L_{0.1}$) of the estimated saturated cross-section. For reference, at 1 Gbit/s comparison of the standard MS SR to the Dual-interleaved TMR SR (worst to best case), yields an improvement in threshold LET over of 7500x based on Weibull fit parameter, L_{th}. This is clearly a significant improvement, and represents the first successful SEU hardening of SiGe logic circuits. These results are encouraging, and they represent a step forward towards a potentially effective mitigation path for SEU hardening of SiGe logic using purely RHBD techniques.

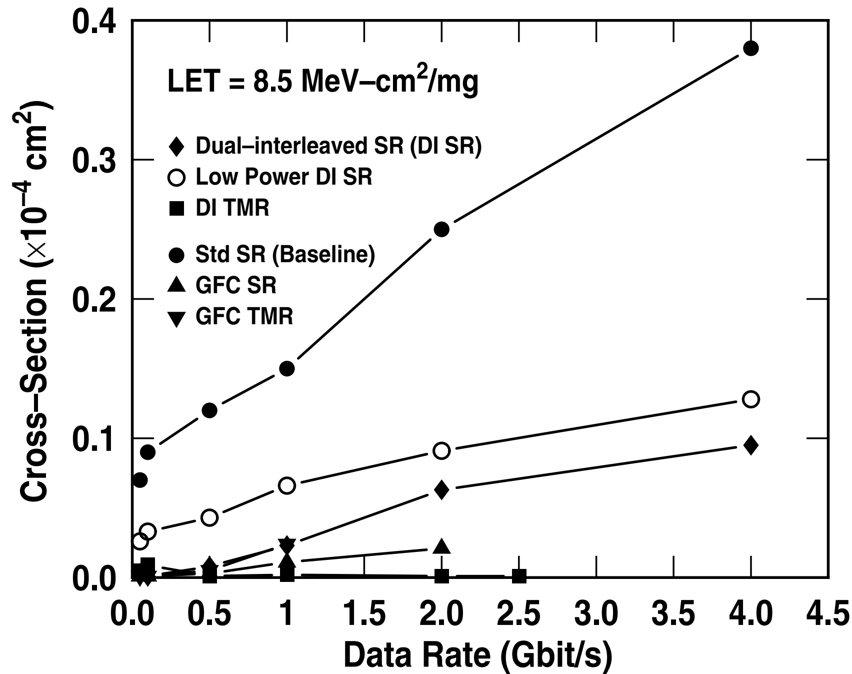


Figure 25: Device cross-section σ as a function of data rate for LET = 8.5 MeV-cm^2/mg.

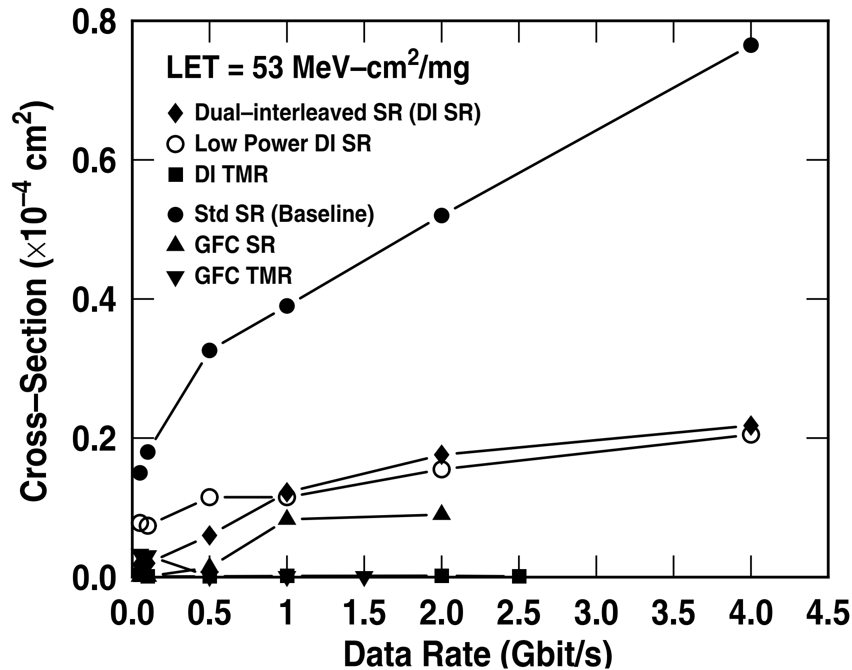


Figure 26: Device cross-section σ as a function of data rate for LET = 53 MeV-cm^2/mg.

3.6 *Summary*

A combination of circuit- and device-level RHBD techniques was successfully applied in the realization of high-speed shift registers for the first time in IBM SiGe 8HP BiCMOS

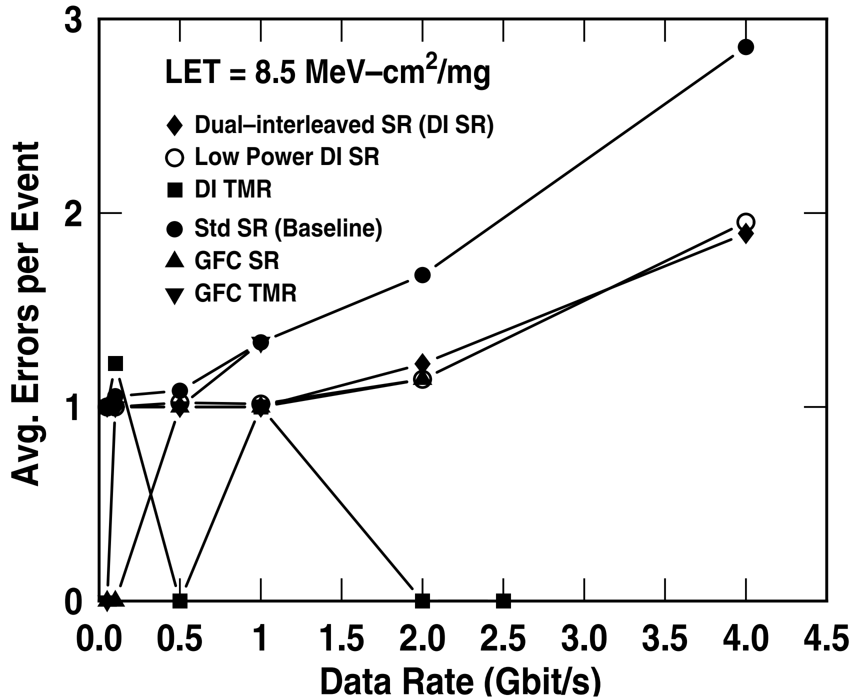


Figure 27: Average errors per error events as a function of data rate for LET = 8.5 MeV-cm^2/mg.

Table 4: Estimated threshold LET for the shift registers.

Topology	L_{th}		$L_{0.1}$	
	0.1 Gbit/s	1 Gbit/s	0.1 Gbit/s	1 Gbit/s
Std SR	0.01	0.01	4.0	1.8
DI SR	6.0	2.0	10.0	6.2
DI SR Low-Power	0.05	0.4	1.8	3.4
DI TMR	>75	>75	-	-
GFC SR	6.0	2.2	10.0	10.0
GFC TMR	4.0	>75	10.0	-

technology. The use of RHBD C-B-E SiGe HBTs with 73% smaller trench-enclosed (DT-enclosed) area than conventional C-B-E-B-C devices, and circuit RHBD techniques such as the dual-interleaving, gated-feedback, and TMR, proved effective in improving the overall SEU immunity of the shift registers, to high LET values. Limiting cross-sections were observed to a LET value of 75 MeV-cm^2/mg at 1 Gbit/s data rate in DI TMR. In addition, a significant improvement in threshold LET was observed in RHBD circuits compared to the unhardened standard CML shift register.

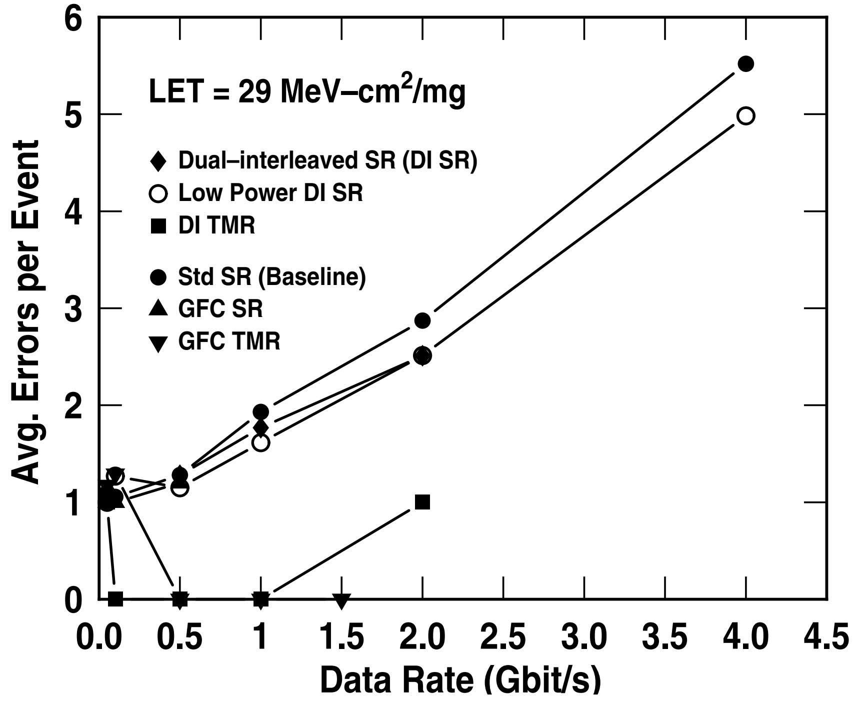


Figure 28: Average errors per error events as a function of data rate for LET = 29 MeV-cm^2/mg.

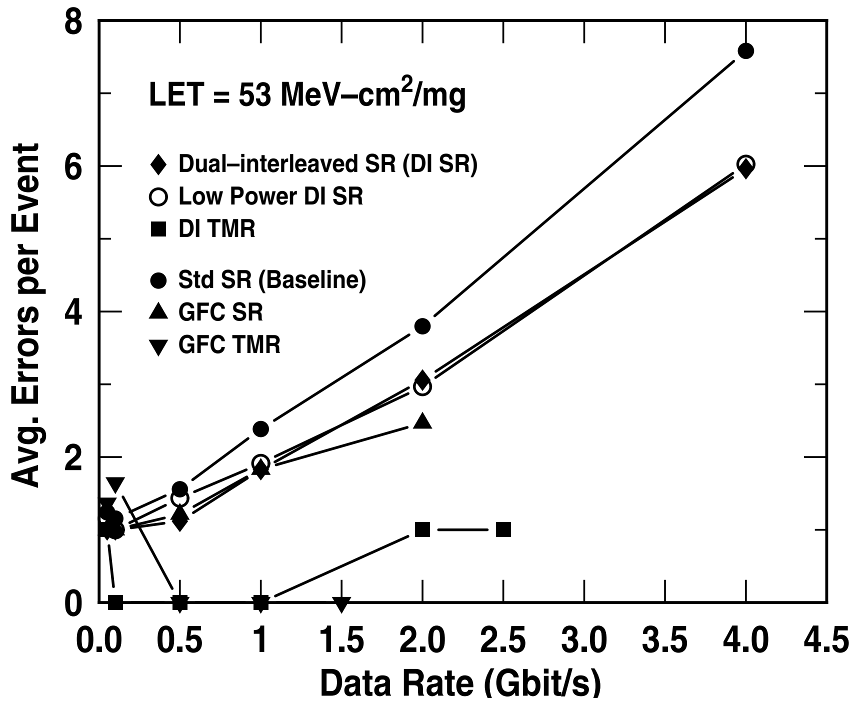


Figure 29: Average errors per error events as a function of data rate for LET = 53 MeV-cm^2/mg.

CHAPTER IV

ON THE FEASIBILITY OF USING 120 GHZ SIGE HBT TECHNOLOGY FOR CRYOGENIC BROADBAND ANALOG APPLICATIONS

4.1 Introduction

SiGe HBT technology, which has III-V devices like performance at room temperature, exhibits superior cryogenic properties [18], [19] and hence is a natural choice for designing broadband amplifiers for operation at cryogenic temperature. Many salient features of SiGe HBTs, such as their increase in transconductance, current gain, and peak cut-off frequency with cooling, can be exploited when designing high-gain, broadband cryogenic amplifiers. Such SiGe amplifiers are also expected to exhibit lower noise and hence lower bit error rates when cooled to low temperatures. To assess the suitability of second-generation SiGe HBT BiCMOS technology for designing high-gain, broadband cryogenic amplifiers, extensive *ac* and *dc* characterization was performed on a representative transistor with an emitter geometry of 0.12×2.56 μm^2 from 120 GHz SiGe HBT technology [41], [3].

4.2 Device Technology

The second-generation SiGe HBT BiCMOS technology investigated here is a commercial 180 nm, 120/100 GHz (f_T/f_{MAX}) and 2 V BV_{CEO} technology, with five levels of metallization, aggressively scaled 0.11 μm L_{eff}, 1.8 V Si CMOS, and a full suite of passive elements [41]. This SiGe HBT BiCMOS technology employs 100% Si processing compatibility with shallow- and deep-trench isolation, and a thermodynamically stable, graded UHV/CVD epitaxial SiGe base. This technology was developed for room-temperature

broadband applications with no intentional optimization for cryogenic operation.

4.3 Experiment

Transistors with an emitter of geometry of 0.2×2.56 μm^2 were chosen as the representative devices for the intended application. A Blanz Model l02 liquid-nitrogen-based cryogenic probe station with on-wafer probing capability was used to perform *dc* measurements over a temperature range of 300 K to 82 K. The small-signal ac (S-parameters) measurements were performed using custom-designed cryogenic on-wafer probing system, capable of microwave measurements from room temperature down to 18 K [47]. S-parameters were measured to 42 GHz using an Agilent 8510C VNA. Calibration and parasitic de-embedding was performed at each temperature using standard techniques. The thermometry of both of the cryogenic test systems was verified by comparing transistor I-V characteristics from these systems at 77 K to that obtained for the same transistor immersed in liquid-nitrogen.

4.4 Results and Discussion

4.4.1 *dc* Characteristics

A liquid-nitrogen-based on-wafer probe station (Blanz Model l02) was used to perform *dc* measurements over a temperature range of 300 K to 82 K. The SiGe HBT from this second-generation SiGe HBT BiCMOS technology maintained reasonable base current ideality down to cryogenic temperatures (Fig. 30). As expected, the transconductance (g_m) of the device increased with cooling to a peak value of over 50 mA/V at 82 K, because of its inverse relation to temperature, making the device attractive for high-gain analog applications at low temperatures (Fig. 31). The base-emitter turn-on voltage (V_{BE}), however, increased at low temperatures because of the exponential decrease in the intrinsic carrier concentration with cooling. The current gain (β) increased monotonically with cooling (Fig. 32) while maintaining useful gain over nine orders of magnitude of collector bias current. The peak current gain at 82 K was more than 1900, compared to a 300 K value of

400 (Fig. 33). This dramatic increase in current gain with cooling is due to the exponential dependence of the ratio of Ge-induced band offset to the thermal energy "kT."

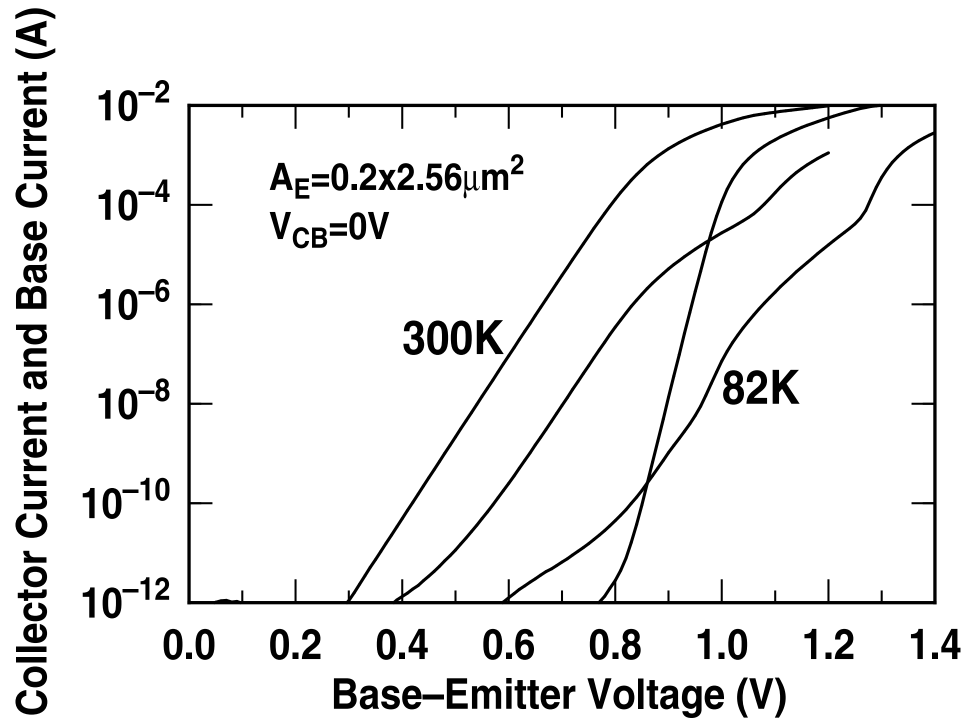


Figure 30: The Gummel characteristics of 0.12×2.56 μm^2 SiGe HBT at 300 K and 82 K.

The forced base current output characteristics were measured in the high-injection regime where the transistor will operate in circuit applications, at both 300 K and 85 K (Figs. 34 and 35 respectively). The current gain for the chosen ranges of base currents at 85 K was higher than that at 300 K, which is consistent with current gain measurements reported above. While the nominal value of BV_{CEO} at room temperature is around 2 V, at 85 K, the BV_{CEO} decreased slightly to a value of about 1.8 V. This decrease in BV_{CEO} is further confirmed by a modest increase in avalanche multiplication factor ($M - 1$) with cooling (Fig. 36). A forced-emitter current (I_E) method for $M - 1$ measurement was employed to limit the feedback mechanism for avalanche multiplication during the presence of self-heating that could cause permanent damage to the device due to thermal runaway. A low value of emitter current of 1 μA was chosen to minimize self-heating and the influence

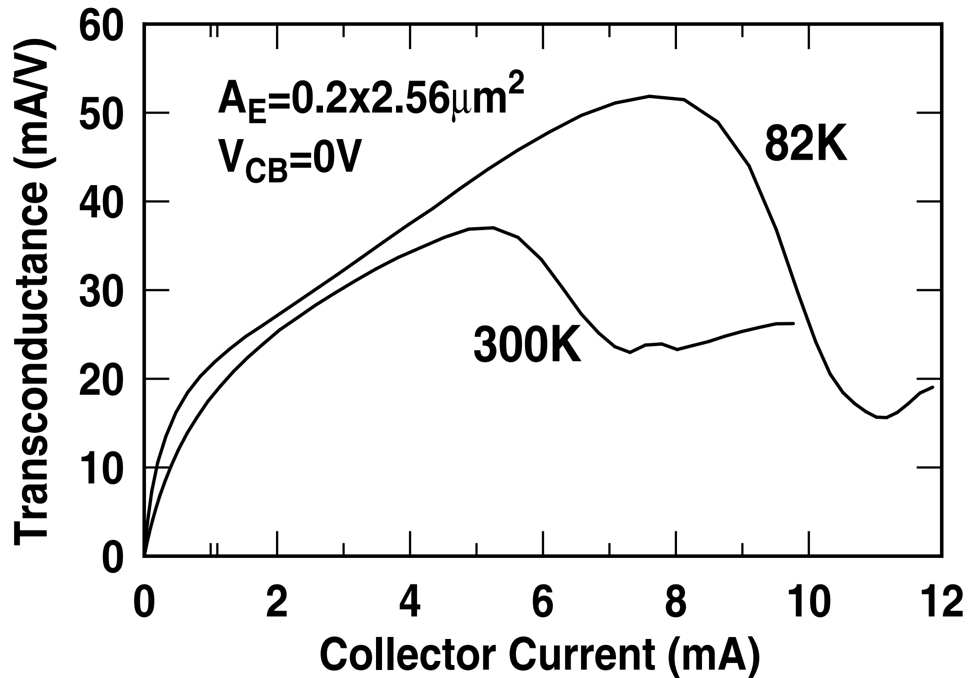


Figure 31: Transconductance as a function of collector current at 300K and 82K.

of Early effect on M-1 data. The output characteristics showed an improvement in Early voltage (decrease in output conductance) at low temperatures, and thus the product of the current gain and Early voltage (βV_A), an important figure-of-merit for amplifier gain, was significantly higher at 82 K than at 300 K.

4.4.2 *ac* Characteristics

S-parameters were measured to 42 GHz using an Agilent 8510C VNA. Calibration and parasitic de-embedding were performed at each temperature using standard techniques. The small-signal short-circuit current gain (h_{21}) was calculated from this de-embedded data and cut-off frequency was obtained by extrapolating this data. The peak cut-off frequency (f_T) at 85 K increased by about at 20 GHz with cooling from 300 K (Fig. 37), indicating that the intended broadband amplifier should be realizable at low temperatures. The peak maximum oscillation frequency (f_{max}) also showed an increase from its 300 K value of about 20 GHz when cooled to 82 K (Fig. 38), demonstrating that the heavily doped base profiles are successful in mitigating base freeze-out. The temperature dependence of peak

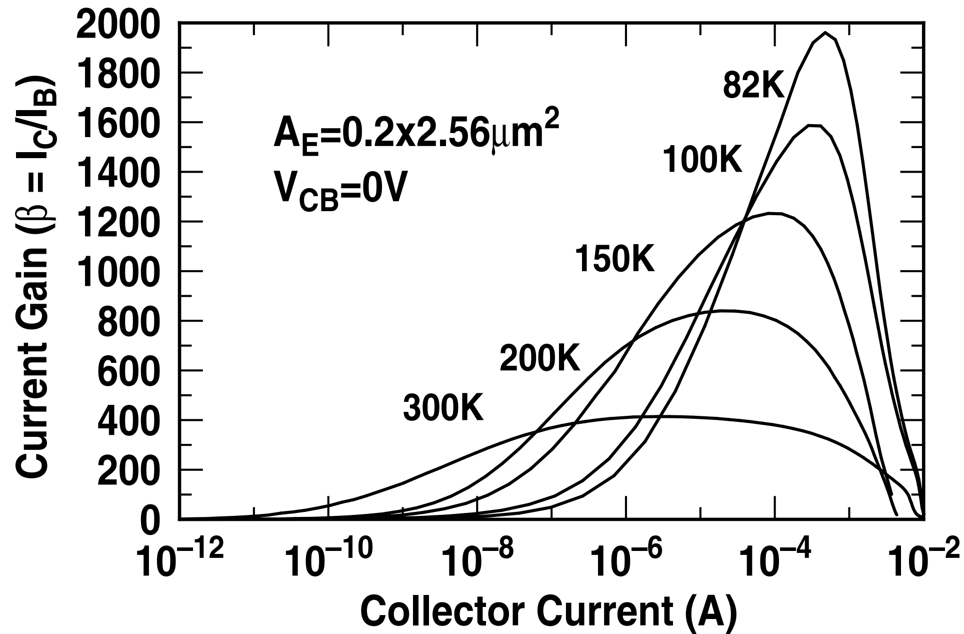


Figure 32: Current gain (β) as a function of collector current at various temperatures.

cut-off frequency was somewhat weaker than that reported for first-generation SiGe HBTs [48].

4.5 Summary

A significant increase in current gain and transconductance, with cooling in SiGe HBTs, indicates that high-gain amplifiers should be realizable at cryogenic temperatures. The enhancement in cut-off frequency with cooling will prove conducive for broadband circuit design at low temperatures. However, the transistors in cryogenic circuits need to be carefully biased to operate well within the nominal BV_{CEO} limit to account for its slight decrease with cooling. Thus, the measured cryogenic *dc* and *ac* performance of a commercial 120 GHz SiGe HBT successfully demonstrates the feasibility of applying this technology to high-gain, broadband cryogenic amplifiers.

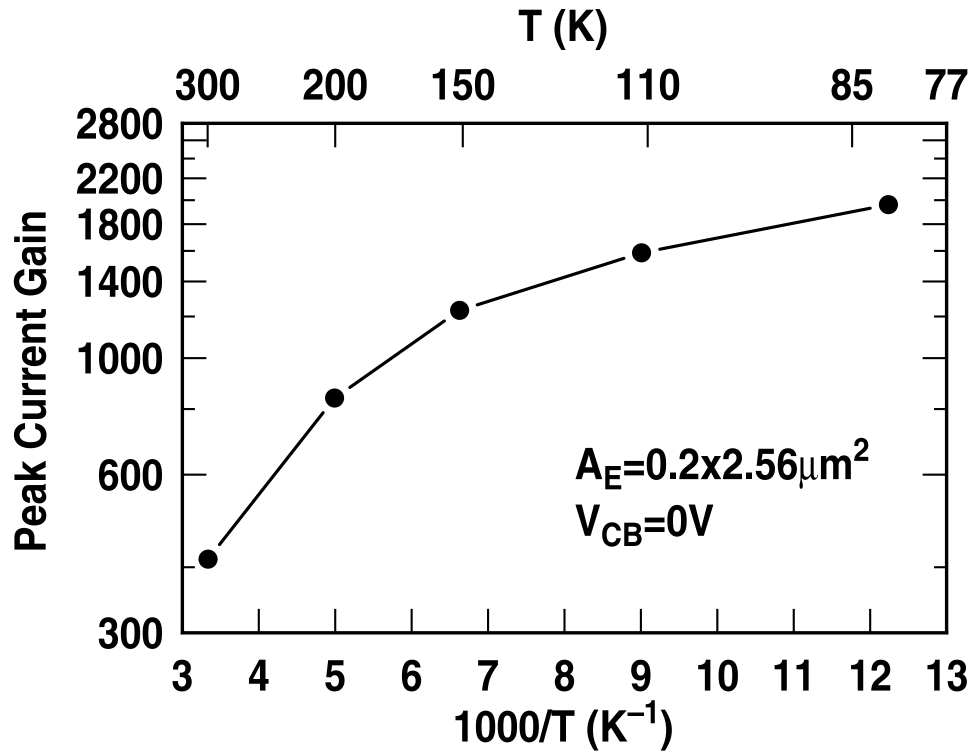


Figure 33: The peak current gain (β_{max}) as a function of inverse of temperature.

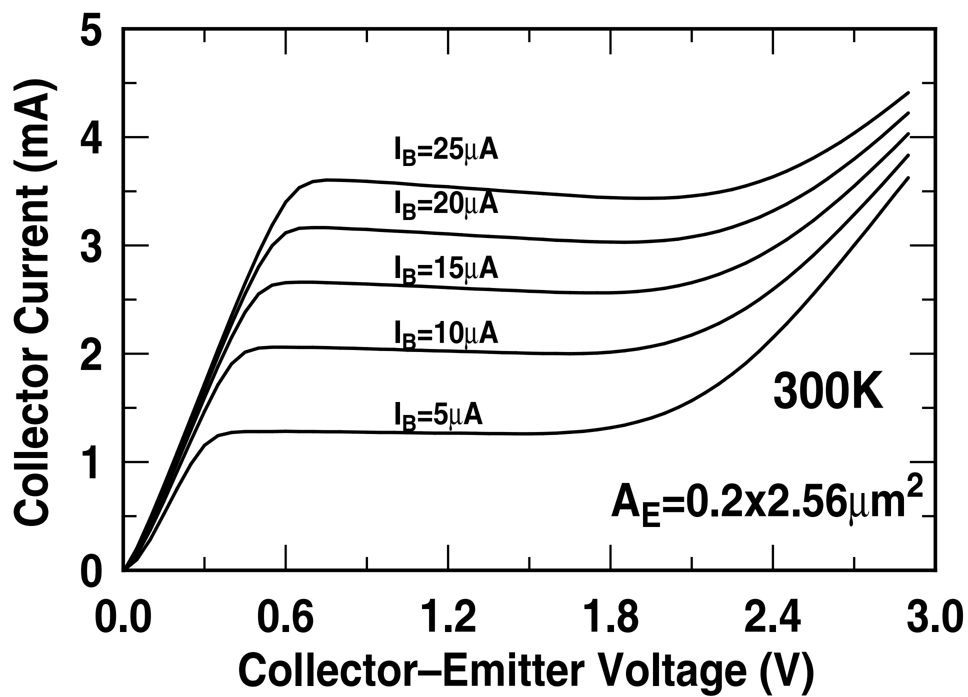


Figure 34: The high-injection output characteristics at 300 K.

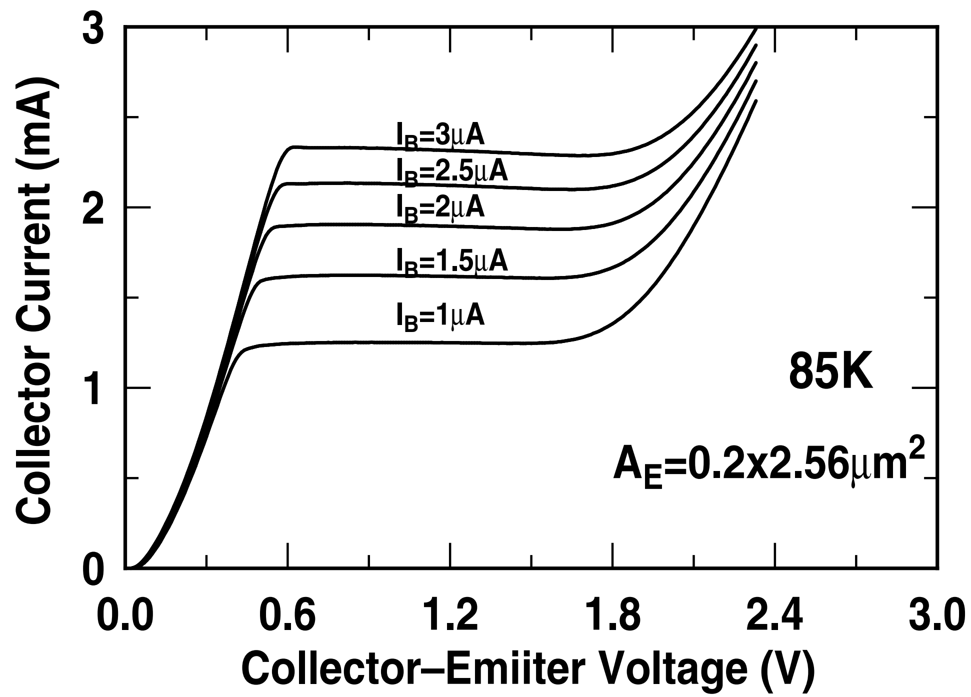


Figure 35: The high-injection output characteristics at 85 K.

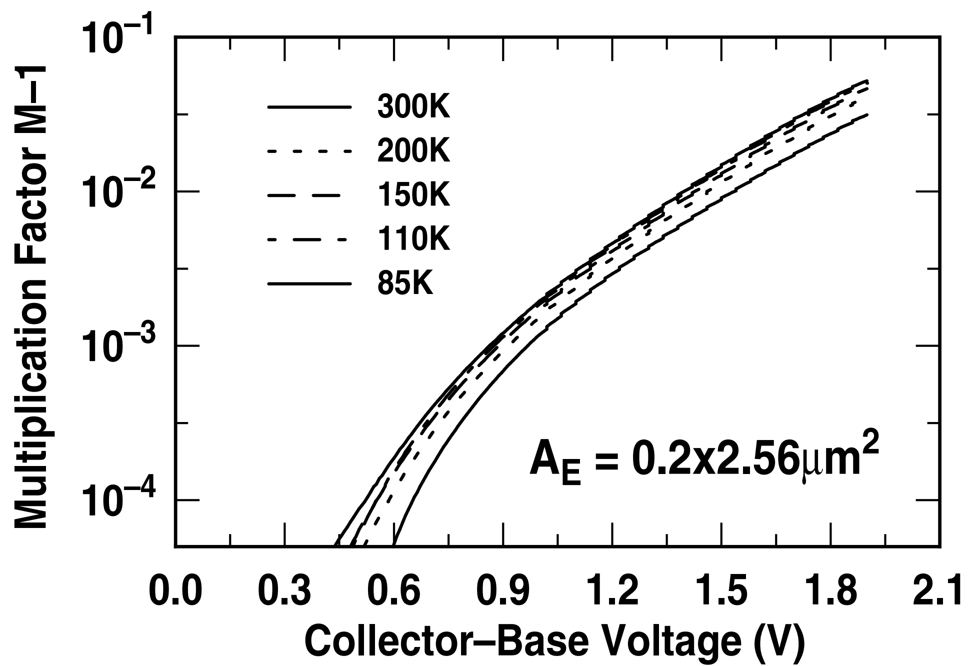


Figure 36: $M-1$ versus V_{CB} measured at low-injection (I_E=1 μA) at 300K and 85K.

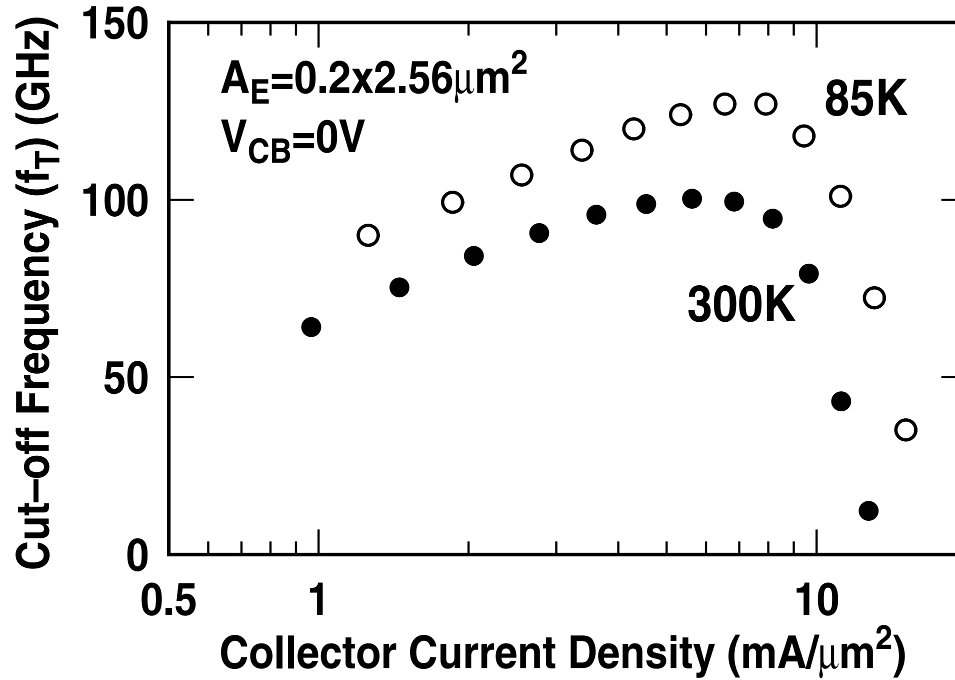


Figure 37: Cut-off frequency versus collector current density at 300 K and 85 K.

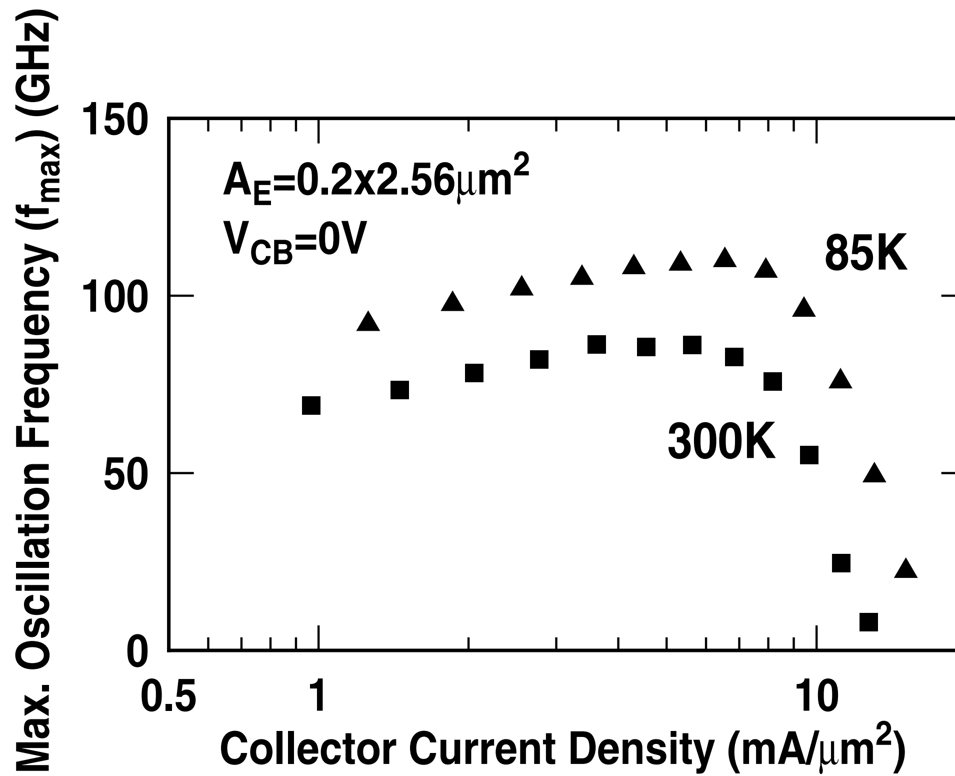


Figure 38: Maximum oscillation frequency versus collector current density at 300 K and 85 K.

CHAPTER V

DESIGN OF A 24 GHZ BROADBAND SIGE HBT LIMITING AMPLIFIER

5.1 Introduction

The inherently superior cryogenic properties of SiGe HBTs [18], [19] make them suitable for a niche application, such as cooled broadband interface circuits to link superconducting electronics (4 K) to room temperature electronics [40]. A broadband amplifier, one of the key interface circuits, is required to operate at an intermediate temperature (e.g., 77 K), and have high-gain (> 55 dB) and wide bandwidth (> 20 GHz). The second-generation of SiGe HBT was chosen for realizing this circuit. The high gain ensures that weak signals generated by the superconducting logic, which is typically 1-2 mV, are amplified to the ECL voltage levels required to operate the room-temperature logic. Wide bandwidth helps the transmission of high-speed data with minimal distortion, thus preserving the speed advantage of processing data using superconducting logic. Further a differential design ensures adequate common-mode rejection. The input and output of the amplifier need to be matched to 50 Ω with reasonable input sensitivity.

The design methodology used in amplifier realization is based on broad guidelines prescribed in [55], [56], and [57] for the design of Si-based high-speed ICs. As with most limiting amplifier architectures, broadband response is achieved through the use of the modified Cherry-Hooper architecture [58], and high gain and 50 Ω drive capability are achieved by cascading three gain stages, followed by an output buffer. A comparison is drawn between the limiting amplifier [4] realized in this work and other Si and non-Si [59], [60] broadband amplifiers using a newly proposed figure-of-merit [4].

5.2 Device Technology

This limiting amplifier was fabricated in a commercial SiGe HBT BiCMOS technology, which is deep- and shallow-trench isolated, and integrates 0.20 μm, 1.8 V BV_{CEO}, 120 GHz f_T SiGe HBTs, 4.3 V BV_{CEO}, 35 GHz f_T SiGe HBTs with lower RF performance, together with 0.18 μm, 1.8 V Si CMOS devices (Fig. 39) [41]. It supports a full suite of passive elements including metal-insulator-metal (MIM) capacitors and thin film resistors. This is a seven metal layer process with 5 copper metal layers and two top thick aluminum layers that enable high-Q inductors and transmission lines.

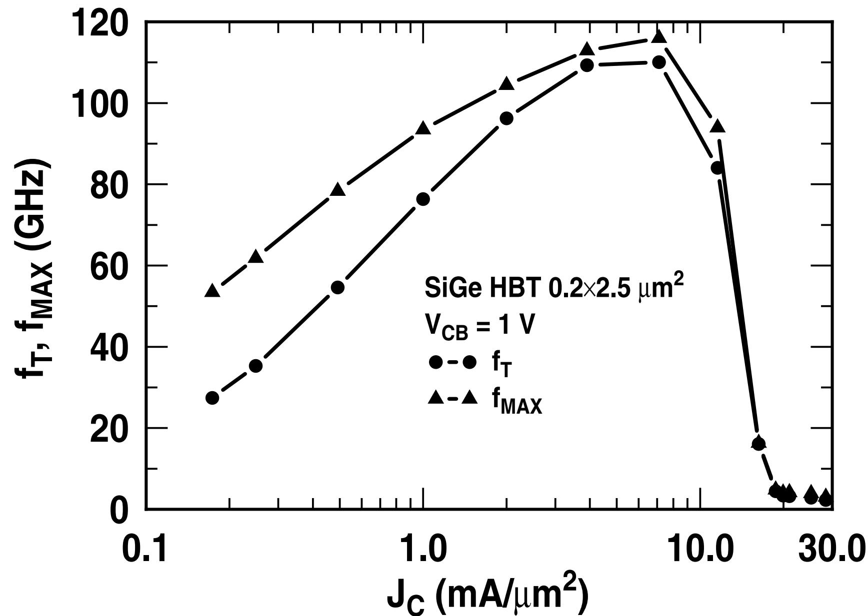


Figure 39: f_T and f_{max} versus collector current density of a 0.2 × 2.5 μm^2 SiGe HBT.

5.3 Circuit Design and Layout

The block diagram in Fig. 40 depicts the various blocks in the limiting amplifier. The gain is provided by the input buffer and the two gain stages that follow. The output buffer is capable of driving a 50 Ω load. The design was kept fully differential to adequately reject any common-mode signals. The amplifier is designed to work with a single power supply V_{EE} of -5 V. However, the power supplies to the gain blocks (V_{EE}) and the output buffer

(V_{EEBuff}) were isolated to mainly gauge the power consumed by the output buffer. A pair of emitter followers was used at both of the input channels of each block.

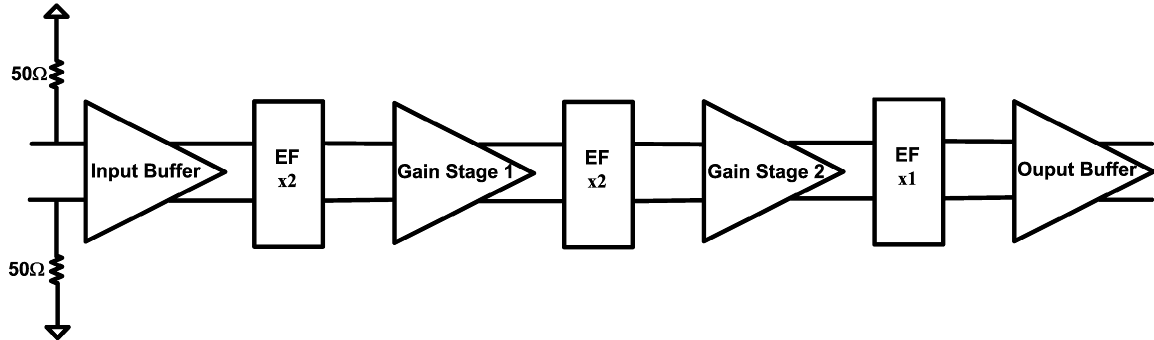


Figure 40: Limiting amplifier block diagram showing gain stages and emitter followers.

5.3.1 Broadband Amplifier Techniques

One of the broadband techniques employed in this design was the principal of maximal impedance mismatch between gain stages [55]. This effect is realized by cascading the transadmittance stage (TAS) and the transimpedance stage (TIS) in an alternating fashion and by interposing chain of emitter followers between each TAS-TIS combination (Fig. 40). Apart from providing isolation and level shifting, emitter followers also help improve the bandwidth of the gain response (Fig. 41). The output impedance (Z_{OUT}) of the emitter followers can be adjusted to look inductive, resulting in peaking in the frequency response at the upper frequency limit [61]. However, adequate care needs to be exercised in adjusting the bias currents I_1 and I_2 to avoid too much ringing at the output. One corrective measure would be to reduce the bias current I_2 to diminish the inductive peaking associated with the second emitter follower [55]. On the whole the emitter follower bias was chosen such that the observed ringing at the output is minimal while still enough to achieve wide bandwidth. Though the level-shifting requirements dictated the use of three emitter followers, this was avoided by using simple diode (D1) level shifting. By this measure further degradation in stability was averted, while taking only a small hit on the gain. Diode D2 is in place to prevent V_{CE} from exceeding the breakdown voltage.

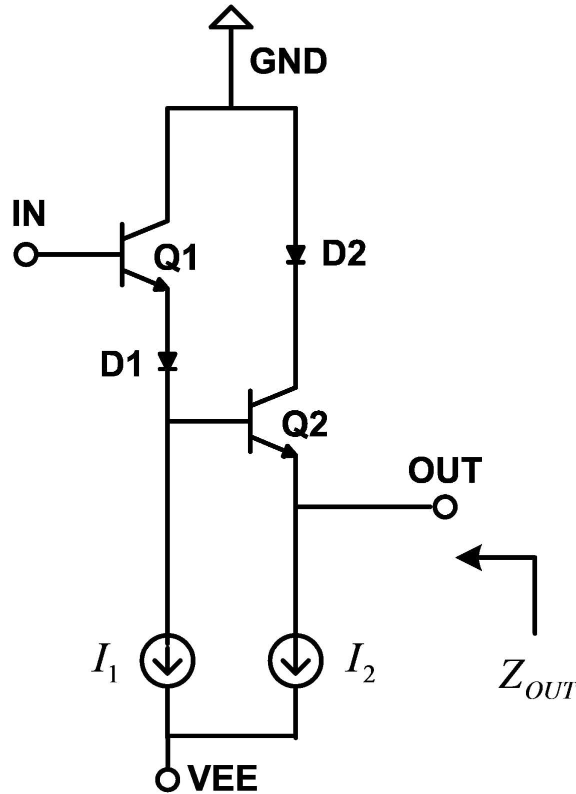


Figure 41: Schematic of an emitter follower pair.

5.3.2 Amplifier Architecture

All the blocks of the limiting amplifier incorporated the same architecture, namely the differential Cherry-Hooper architecture [58] with emitter followers in the feedback path [56] (Fig. 42). The Cherry-Hooper amplifier comprises of a transadmittance stage and a transimpedance stage (TAS-TIS) combination as discussed above. This parallel feedback architecture implements shunt-shunt feedback in the transimpedance stage. The presence of an emitter follower in the feedback path of the transimpedance stage not only provides better isolation between the feedback resistor and the load, but also offers inductive peaking in the gain response.

In addition, the paths for the bias currents through the transadmittance and transimpedance

stages are isolated. This helps realize a *dc*-coupled output, making this architecture attractive for output buffer design as well [59]. It has also been recently reported that the large-signal performance improves when the conventional resistive load output buffer is replaced with the modified Cherry-Hooper architecture based output buffer [60].

All stages except the output buffer used a transistor of emitter size $0.2 \times 1.0\ \mu m^2$. The TIS transistors in the output buffer had an emitter geometry of $0.2 \times 10.0\ \mu m^2$, while the TAS transistors were of $0.2 \times 5.0\ \mu m^2$ in size. The current source transistors were proportionately bigger than the core cell transistors. Since all the transistors in the signal path were biased at near peak f_T current density of 7 mA/μm^2, the desired gain and bandwidth were obtained mostly by adjusting the feedback and load resistors.

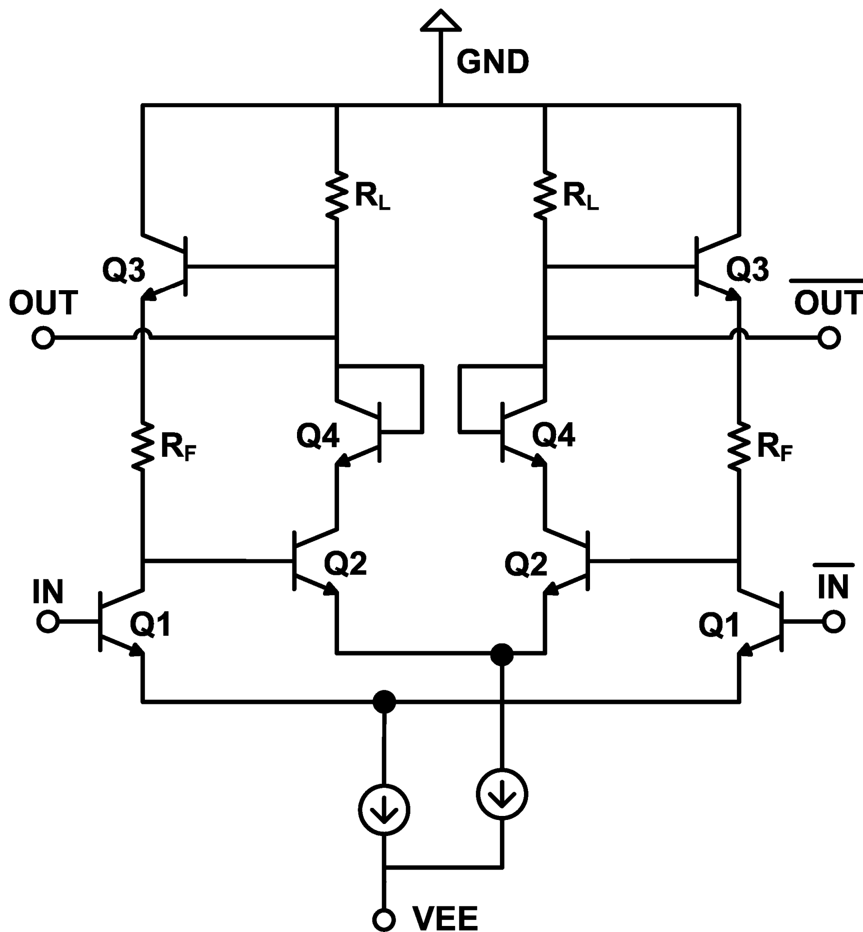


Figure 42: Schematic of the amplifier core used in all the stages of the limiting amplifier.

5.3.3 Amplifier Layout

The chip photomicrograph is shown in Fig. 61. The layout of the limiting amplifier was kept as compact as possible to minimize parasitics. The metal interconnects in the signal path were kept short to minimize RC delays. The layout of the complementary signal paths were kept symmetrical to obtain matching delays in these signal paths. Special attention was paid to minimizing metal overlap on critical signal paths. On-chip decoupling capacitors were added to prevent spurious power supply oscillations from coupling into the circuit. The pad-limited chip area is 0.945×0.720 mm^2.

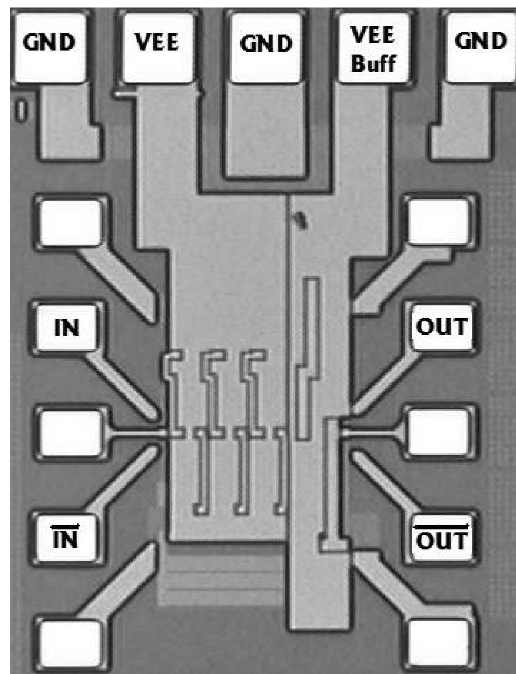


Figure 43: Micrograph of the SiGe limiting amplifier chip.

5.4 Measurement Results

The measured operating point voltages and currents were very close to the simulated values, which is in large part due to the accurate device models available in the design kit. The gain blocks drew a current of 54 mA, while the bias current measured for the output buffer was 55 mA.

5.4.1 RF Measurements

Single-ended two-port S-parameters were measured using the Agilent 8510C VNA with the unused input and output terminals terminated with broadband 50 Ω terminations. On-wafer probing was performed using 40 GHz probes and cables. The saturated S-parameters obtained for the limiting amplifier are shown in Fig. 44. Since the measured S_{21} is single-ended, 6 dB is added to obtain the mid-band single-ended to differential gain of 42 dB. The measured 3-dB bandwidth is in excess of 24 GHz. The gain peaking of less than 3 dB above the mid-band gain is observed in S_{21}.

While the S_{11} almost always remained less than -15 dB, S_{22} was around a value of -10 dB across the frequency, indicating reasonable matching at both input and output ports. The linear range of the amplifier was simulated using an input *dc* sweep to be within ±200 μV, indicating that the amplifier saturates below the simulated input equivalent noise of about 950 μV_{rms}. Thus, an input power of -40 dBm is not sufficiently low to prevent saturating the amplifier. Obtaining calibration below this input power to be able to make reliable measurements proved challenging. Assuming a Gaussian distribution for input noise, the signal-to-noise ratio (SNR) for a bit error rate (BER) of 10^{-9} is 12 [62]. Therefore, with the simulated equivalent input referred noise of 950 μV_{rms}, the worst-case input sensitivity of the limiting amplifier can be calculated to be less than 12 mV_{pp}.

5.4.2 Time-Domain Measurements

Time-domain (large-signal) measurements were taken using an Agilent 70843A 12.5-Gbit/s pattern generator. The output of the amplifier was then viewed and measured using an Agilent 86100 20-GHz sampling oscilloscope. Figure 45 shows a wide-open 10 Gbit/s data eye measured for a 2^{23}-1 pseudorandom input pattern. The eye was accumulated over a period of 60 minutes. The single-ended output amplitude is around 185 mV_{pp} for an input of ~15 mV_{pp}. Thus, the differential output is about 370 mV_{pp}, which is sufficient to drive the succeeding CML-based digital logic blocks. Open eye diagrams were observed

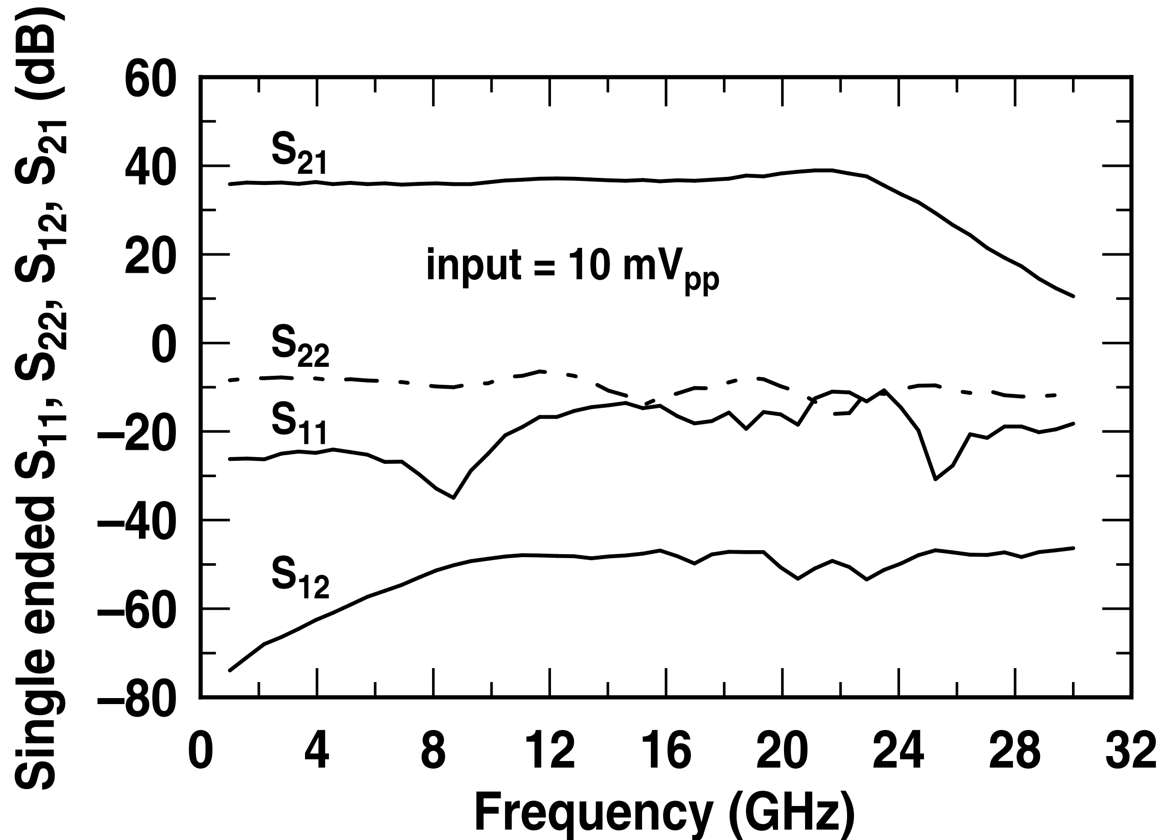


Figure 44: Measured single-ended S-parameters for the limiting amplifier. The 3-dB bandwidth (of S_{21}) is greater than 24 GHz.

for inputs down to as low as 4 mV_{pp}. However, at these very low power settings, the input exhibited poor SNR, thereby causing the output SNR to be marginal. Because of the bandwidth restrictions of the available pattern generator and the sampling oscilloscope, the eye could not be measured at higher speeds; however, the amplifier is expected to work at least to a speed of 24 Gbit/s, if not higher [57].

5.4.3 Performance Comparison

The characteristics for the limiting amplifier are listed in Table 5. The amplifier was then compared with other published amplifiers for similar operating frequencies and gain ranges in Table 6. Gain-bandwidth product has been the traditional figure-of-merit for

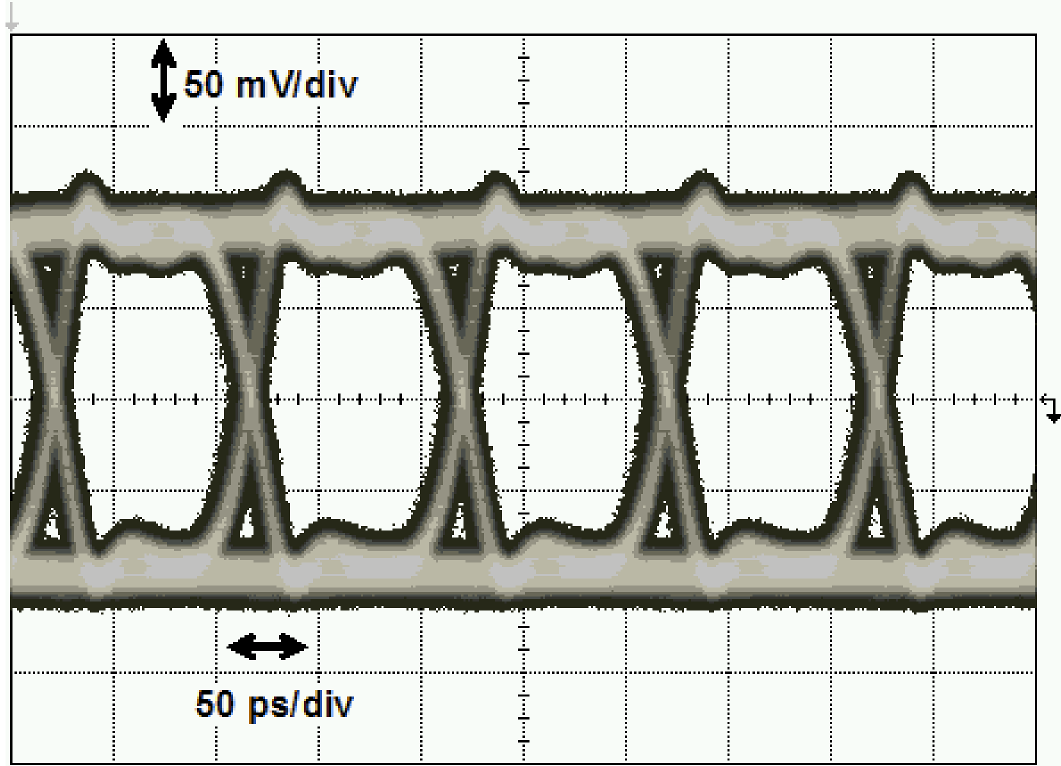


Figure 45: Single-ended 10 Gbit/s limiting amplifier eye diagram. The accumulation time was 60 min.

comparing high-gain amplifiers. However, this figure-of-merit does not include the large-signal performance of an amplifier or the power dissipation associated with achieving the targeted large-signal performance. When comparing amplifier performance across different technologies and/or across different technology generations, the major part played by the device performance in obtaining broadband response is often ignored. Therefore, to be able to compare the performance of various amplifiers across technology, the following figure-of-merit (FoM) is proposed:

$$FoM_1 = \frac{gain \times BW(GHz) \times output\ swing(mV_{pp})}{f_T(GHz) \times P_{diss}(mW)}, \quad (5)$$

where $gain$ is the small-signal gain, BW is the bandwidth in GHz, f_T is peak cut-off frequency in GHz, and P_{diss} is power dissipation in mW. Clearly this FoM described above should not be interpreted as an absolute parameter for comparing amplifiers across all required specifications, since it does not include, for instance, the noise performance, and

all components in the FoM are assigned equal weight, ignoring the application-specific constraints on individual system and circuit specifications. Nevertheless, this FoM offers a convenient tool for comparing amplifiers based on output swing, small-signal gain and bandwidth, f_T, and power consumption. The units of the proposed FoM are [A^{-1}], and the larger the value of the FoM the better its overall performance. Comparing across published amplifiers based on the gain-bandwidth product and this proposed FoM, this new SiGe limiting amplifier is quite competitive, achieving a value of 16.93. This FoM can also be easily modified to include input sensitivity (clearly relevant in this context) by factoring in the dynamic range of the amplifier. The modified FoM would then be expressed as

$$FoM_2(dB) = gain(dB) + 20\log\left(\frac{BW}{f_T}\right) - P_{diss}(dBm) + DynamicRange(dB). \quad (6)$$

The SiGe amplifier presented in this work achieves 30.4 dB for FoM_2, although unfortunately the other published amplifiers do not include sufficient data for meaningful comparison.

Table 5: Summary of the SiGe limiting amplifier characteristics.

S_{21} Bandwidth (3dB)	> 24 GHz
Differential Gain (S_{21})	> 42 dB
S_{11}, S_{22} 0-30 GHz	< -10 dB
Differential Output Voltage	~370 mV_{pp} at 50 Ω Load
Simulated Sensitivity	< 12 mV_{pp} at BER = 10^{-9}
Power supply	-5 V
Total Power Consumption[a]	~550 mW
Die Area	0.945 × 0.720 mm^2

[a] including output buffer

5.5 Summary

A high-gain, broadband, limiting amplifier designed using 120 GHz SiGe BiCMOS process is presented. The amplifier achieves a saturated differential gain of 42 dB and has a 3-dB bandwidth of 24 GHz. The amplifier offers a competitive gain-bandwidth product of 3021 GHz and a value of 16.93 A^{-1} for a newly proposed figure-of-merit.

Table 6: Comparison with published amplifiers.

Reference	Amplifier Type	Bandwidth (BW) [GHz]	Gain (S_{21}) Diff. [dB]	Swing [mV_{pp}]	Supply [V]	P_{diss} [mW]	Process / f_T [/GHz]	Gain×BW [GHz]	Proposed FoM_1 [A^{-1}]
[50]	Limiting	38	21	600	-6.0	720	SiGe/150	426	2.37
[51]	Limiting	26	36	600	-4.3	390	SiGe/120	1640	21.02
[52]	Broadband Amp.	62	16	1500	-5.0	770	SiGe/200	392	3.82
[53]	Transimpedance	50	12	700	-5.2	200	SiGe/200	199	3.48
[54]	Transimpedance	44	21	600	-5.2	460	SiGe/160	494	4.03
[57]	Auto Gain Ctrl.	32.7	19	800	-7.5	725	SiGe/92	291	3.49
[59]	Transimpedance	42	34	800	-5.2	600	InP/150	2105	18.71
[60]	Limiting	46	26	400	-5.5	660	InP/135	918	4.12
This work	Limiting	24	42	370	-5.0	550	SiGe/120	3021	16.93

CHAPTER VI

CRYOGENIC CHARACTERIZATION OF A 24 GHZ BROADBAND SIGE HBT LIMITING AMPLIFIER

6.1 Introduction

A cryogenic broadband amplifier designed using SiGe HBT technology could serve as a high-speed, low-noise conduit for the weak signals generated by ultra-fast superconducting logic (Fig. 46) [40]. Until recently the speed advantage offered by superconducting logic could not be tapped for use in commercial applications because of the inability of room-temperature amplifiers to provide both high-speed and low-noise performance simultaneously. The amount of noise added by a room temperature amplifier is usually higher than the typical strength of signals from the superconducting logic, thus prohibiting their usage in such systems. Since cooling usually improves the noise response of electronic systems, an amplifier operating at an intermediate cold temperature is expected to improve the overall system noise performance. Such an amplifier designed in SiGe HBT technology, apart from having better noise performance, is also expected to benefit from the performance enhancement observed in SiGe HBTs at cryogenic temperatures.

The unique constraint for the broadband link for the superconductor-semiconductor hybrid system is that the broadband amplifier operate at an intermediate temperature in the vicinity of 77 K. Unavailability of deep cryogenic transistor models precludes any kind of circuit simulation to tweak the amplifier design to ensure reliable operation at such low temperatures. However, the design kits do permit circuit simulation over a narrow temperature range around room temperature. While the simulated small-signal gain-bandwidth product

Figure 46: Superconductor-semiconductor hybrid system showing the placement of the cooled SiGe HBT broadband amplifier in the high-speed, low-power data path (after [40]).

for the broadband amplifier showed an increase with cooling (Fig. 47(a)), the input sensitivity decreased (Fig. 47(b)), indicating a favorable trend for both the key parameters. These simulations however only indicate the possible trend at low temperature provided the extrapolations hold down to such low temperatures. Thus, as a first step towards having functional amplifiers operating reliably at low temperatures, a broadband amplifier designed for room-temperature operation can be characterized at low temperatures to gauge the performance change at these temperatures. This in turn would provide guidelines for circuit design at room temperature for low-temperature applications.

(a) (b)

Figure 47: Simulated gain-bandwidth product (a) and input sensitivity (b) behavior across the limited temperature range over which transistor model from the design kit are valid.

6.2 *Experiment*

The broadband amplifier was measured on a customized, on-wafer, open-cycle, liquid helium cryogenic probe system. The system thermometry was verified by comparing base-emitter diode of a transistor measured within the system with those measured directly immersed in both liquid nitrogen (77.3 K), and liquid helium (4.2 K). The temperature accuracy is believed to be better than 1 K [6].

On-wafer calibrated single-ended S-parameters were measured to 35 GHz using an Agilent 8510C Vector Network Analyzer (the practical upper frequency limit of the test system). The through-reflect-reflect-match (LRRM) technique was used to calibrate out the cable and probe-induced losses at each temperature. The unused input and output ports of the amplifier were terminated with broadband 50 Ω terminations. Further, on-wafer time-domain characterization of the broadband amplifier was performed using an Agilent 70843A 12.5-Gbit/s error performance analyzer. The input data was a 2^{23}-1 pseudorandom bit pattern at a data rate of 10 Gbit/s. The output of the amplifier was simultaneously viewed using an Agilent 86100 20-GHz sampling oscilloscope and the bit error rate (BER) was measured using the tester in the Agilent 70843A.

6.2.1 Cryogenic RF Response

As evidenced by S_{11} measured across various temperatures (Fig. 48), the amplifier input matching degraded with cooling. Despite the degradation in S_{11} at low temperatures, the amplifier still maintained reasonable matching across all temperatures. The input matching for the amplifier was achieved by a simple resistor divider network with the net resistance exhibiting a positive temperature coefficient. Hence, with cooling, the input resistance dropped, causing the input matching to deteriorate at low temperatures.

The output buffer of the amplifier was a Cherry-Hooper stage (as described in Chapter

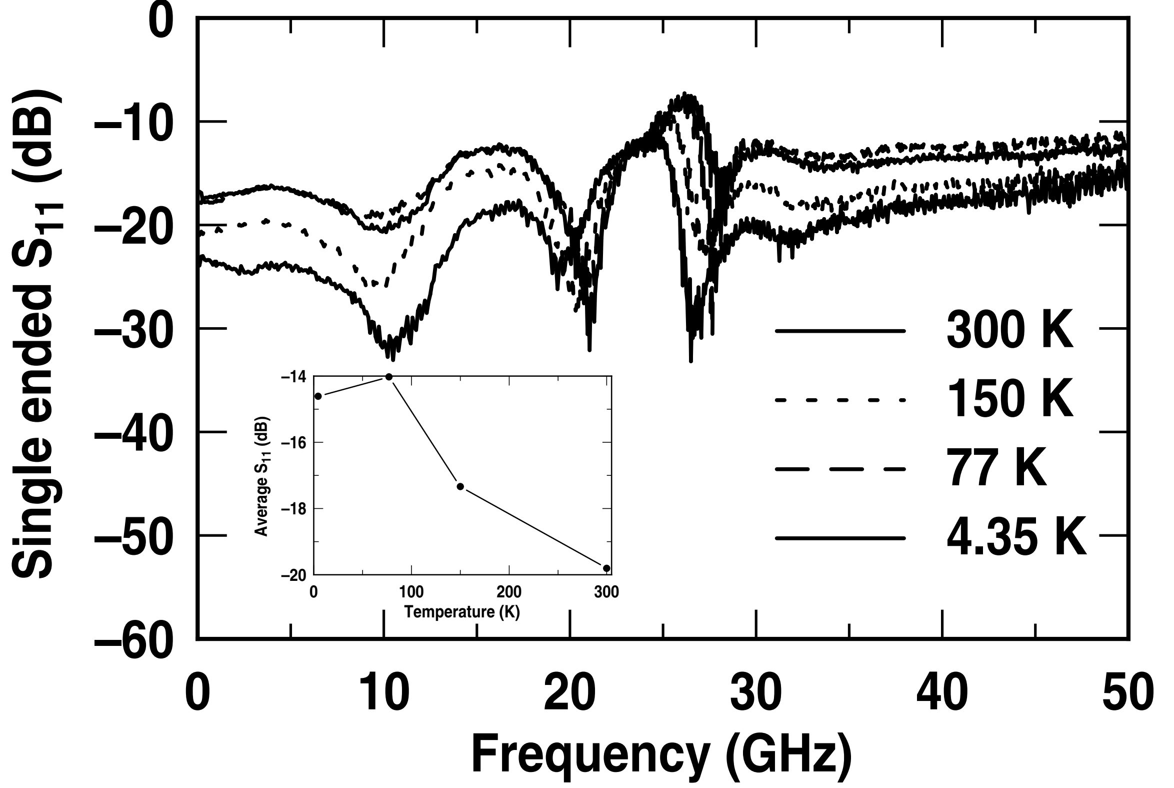


Figure 48: Measured S_{11} across temperature showing slight degradation in input matching with cooling.

V). Thus the single-ended small-signal output resistance, R_{out}, of this stage is given by

$$R_{out} \approx \frac{1}{\frac{1}{R_L} + \frac{1}{\frac{2}{gm} + R_L}} \rightarrow \frac{R_L}{2}, \tag{7}$$

where R_L is the load resistance of the Cherry-Hooper output buffer and g_m the transconductance of the transistor in the transimpedance stage of the output buffer. The transconductance g_m is large even at room temperature and hence the output resistance tends towards $R_L/2$. Further, with cooling, g_m increases thereby rendering R_{out} an even weaker function of g_m. Thus the output resistance temperature behavior largely depends on the temperature coefficient of the load resistance, which is positive for the load resistor in the output buffer. Therefore, a degradation in the output matching with cooling (Fig. 49) similar to the one seen for input matching is observed.

The input to output isolation measured by S_{12} does not show any appreciable change

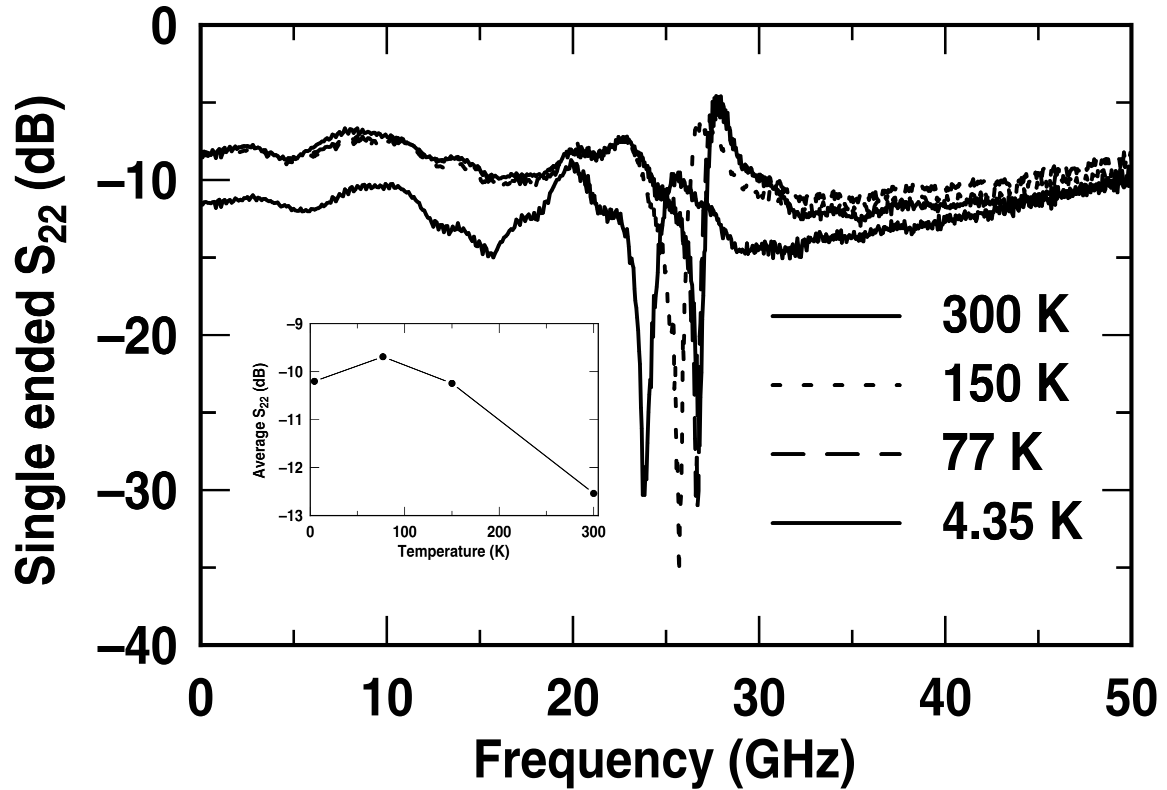


Figure 49: Measured S_{22} across temperature showing slight degradation in output matching with cooling.

with cooling (Fig. 50). On the other hand, the forward gain, measured here through single-ended S_{21}, shows changes both in magnitude and bandwidth with cooling (Fig. 51). The bandwidth increased by about 3 GHz when cooled to 77 K and did not show appreciable increase when further cooled down to 4.35 K. This increase in bandwidth, however, was accompanied by increase in gain peaking at low temperatures. The increased gain peaking at low temperatures might be originating from the enhancement of inductive peaking behavior associated with the emitter follower. With cooling, the g_m of the SiGe HBTs increases, and in emitter followers this causes the output impedance to appear more inductive than at room temperature, thereby rendering the amplifier less stable at low temperatures than at room temperature.

In addition to peaking introduced by emitter followers, series inductance of the positive supply lines to a gain stage could also cause inductive peaking behavior. A simple common

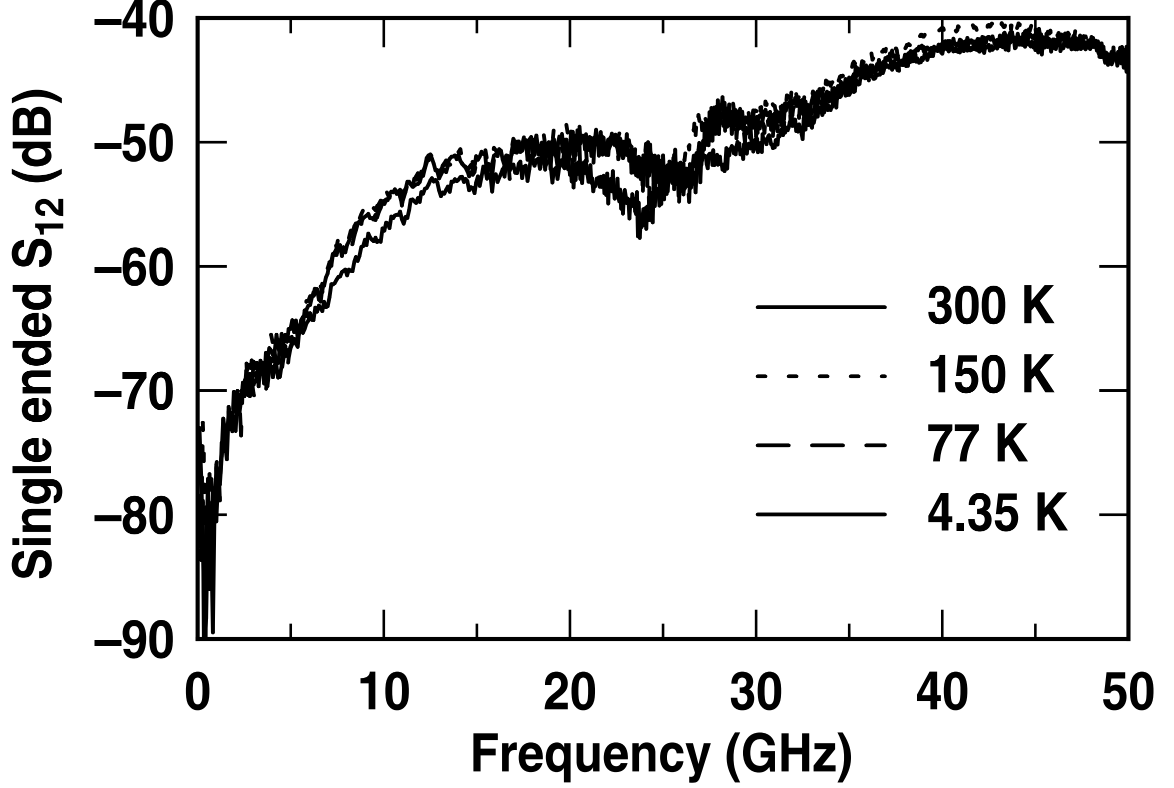


Figure 50: Measured S_{12} across temperature showing no evidence of degradation in isolation with cooling.

emitter amplifier with series inductance and its simplified small-signal equivalent circuit is shown in Fig. 52. The transfer function of this circuit is given by [63]

$$\frac{V_{OUT}}{V_{IN}} = -g_m \frac{L_L s + R_L}{L_L C_L s^2 + R_L C_L s + 1} \tag{8}$$

$$= -g_m R_L \cdot \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n + \omega_n^2} \cdot \frac{\omega_n}{2\zeta}, \tag{9}$$

where damping factor $\zeta = (R_L/2)\sqrt{C_L/L_L}$ and natural frequency $\omega_n = 1/\sqrt{L_L C_L}$. With cooling, R_L drops and effective L_L increases thereby causing ζ to drop. Decrease in ζ could cause small-signal gain peaking to aggravate at low temperatures.

6.2.2 Cryogenic Time Domain Response

Figure 53 shows the eye for a 10 Gbit/s input data measured at 77 K and for a power supply voltage of $V_{EE}= -5$ V. The eye was accumulated over a period of 30 minutes.

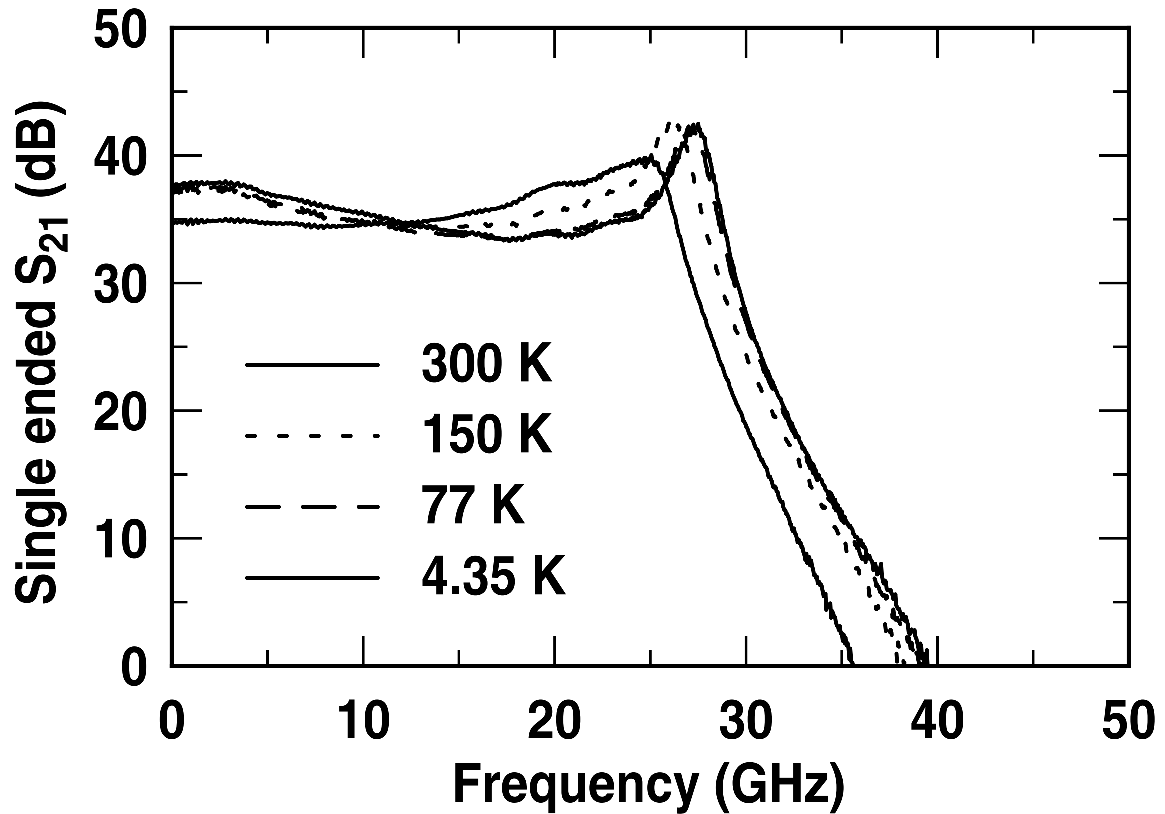


Figure 51: Measured S_{21} across temperature showing increased gain peaking and bandwidth extension at low temperatures.

Clearly, the eye at 77 K shows significant closure compared to the eye measured at room temperature (Fig. 45). The smaller eye opening at lower temperatures is because of the increased ringing in the time-domain response and longer settling time compared to that at room temperature. This increase in ringing in the time-domain response is a sign of aggravated instabilities at low temperature, which is consistent with increase in gain peaking behavior observed in S_{21} at low temperature.

The closure of eye diagram directly corresponds to a degradation in BER performance. BER behavior is represented using what are called bathtub plots where BER is plotted in log scale as a function of sampling point in the unit interval. The bathtub plot for the limiting amplifier for a 10 Gbps 2^{23}-1 pseudorandom bit pattern at 300 K and 77 K is shown in Fig. 54. It is clear that the bathtub plot at 77 K is significantly shallower than

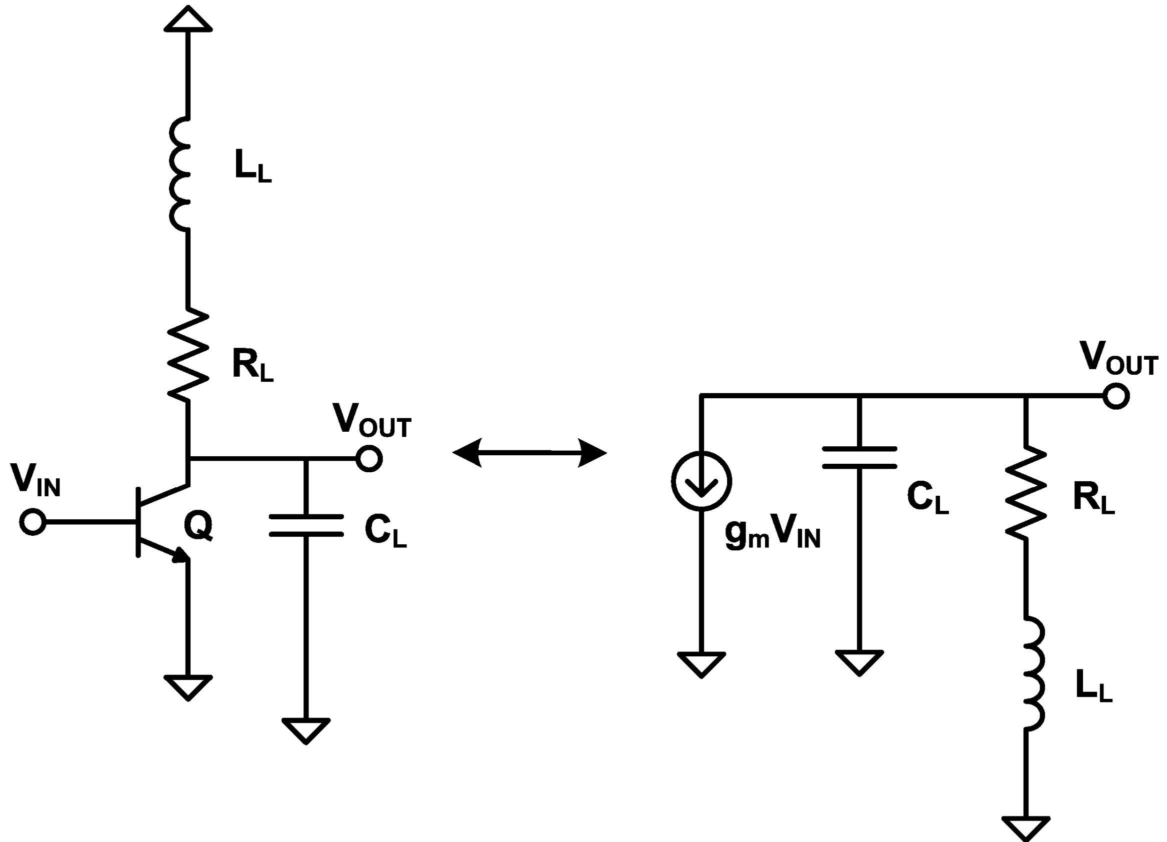


Figure 52: A common emitter gain stage with load inductance and its simplified small-signal equivalent circuit.

that at 300 K. The BER at mid sampling point at 77 K is four orders magnitude higher than that at 300 K. A qualitative comparison of the eye diagram at 77 K and the corresponding bathtub plot further indicates that the degradation in the BER response is associated with increased output ringing.

6.3 Design Guidelines

Based on the observations made from the cryogenic RF and time-domain response of the limiting amplifier, some broad guidelines are proposed for designing a room-temperature limiting amplifier intended for low-temperature application.

1. Minimize or eliminate gain peaking in small-signal gain response at room temperature introduced intentionally to improve the bandwidth.

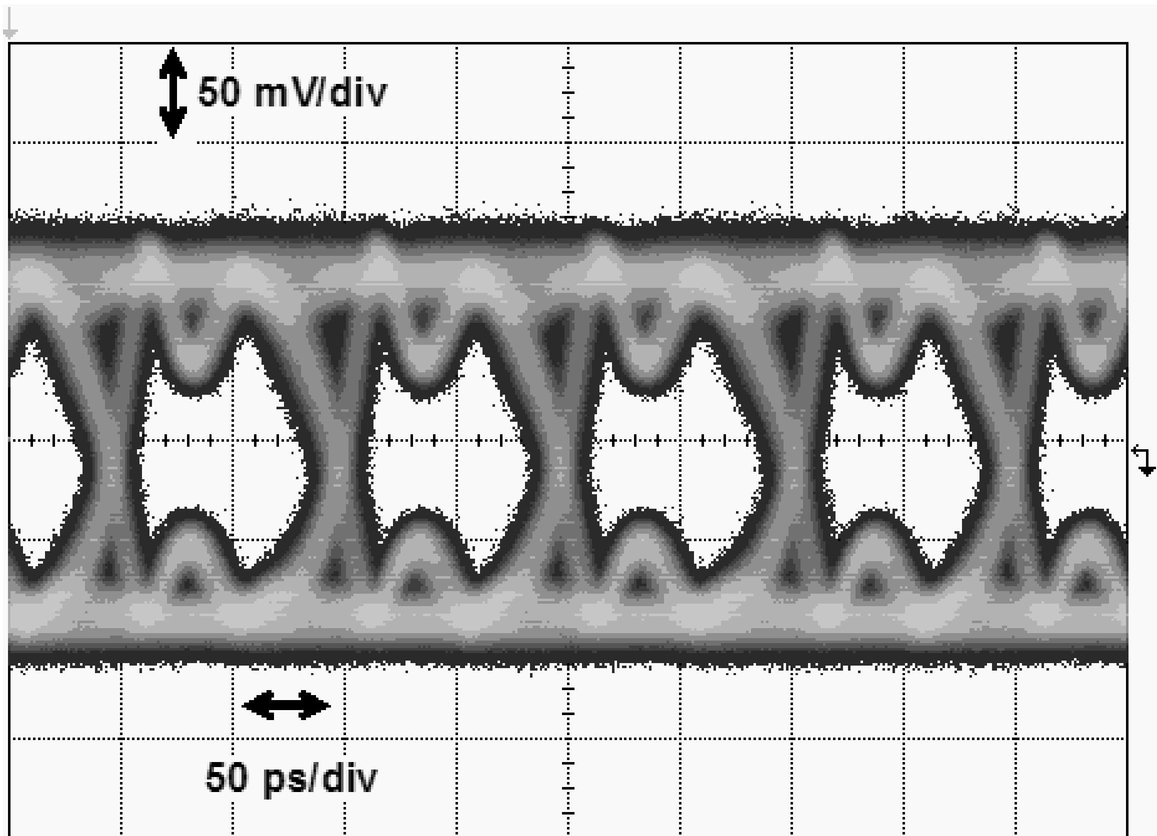


Figure 53: Single-ended 10 Gbit/s limiting amplifier eye diagram measured at 77 K showing significant closure compared to the eye at 300 K (Fig. 45). The accumulation time was 30 min

2. Minimize the inductance of the supply lines by using thick metal lines to reduce series inductive peaking in small-signal gain response.

3. Use lowest temperature coefficient resistances for load and feedback resistors.

4. Bias the emitter followers with current sources that are proportional to absolute temperature (PTAT) to maintain constant g_m across temperature.

5. Bias the gain stages with PTAT current sources if sufficient gain-bandwidth is available at room temperature and its enhancement at low temperature is not required or undesirable.

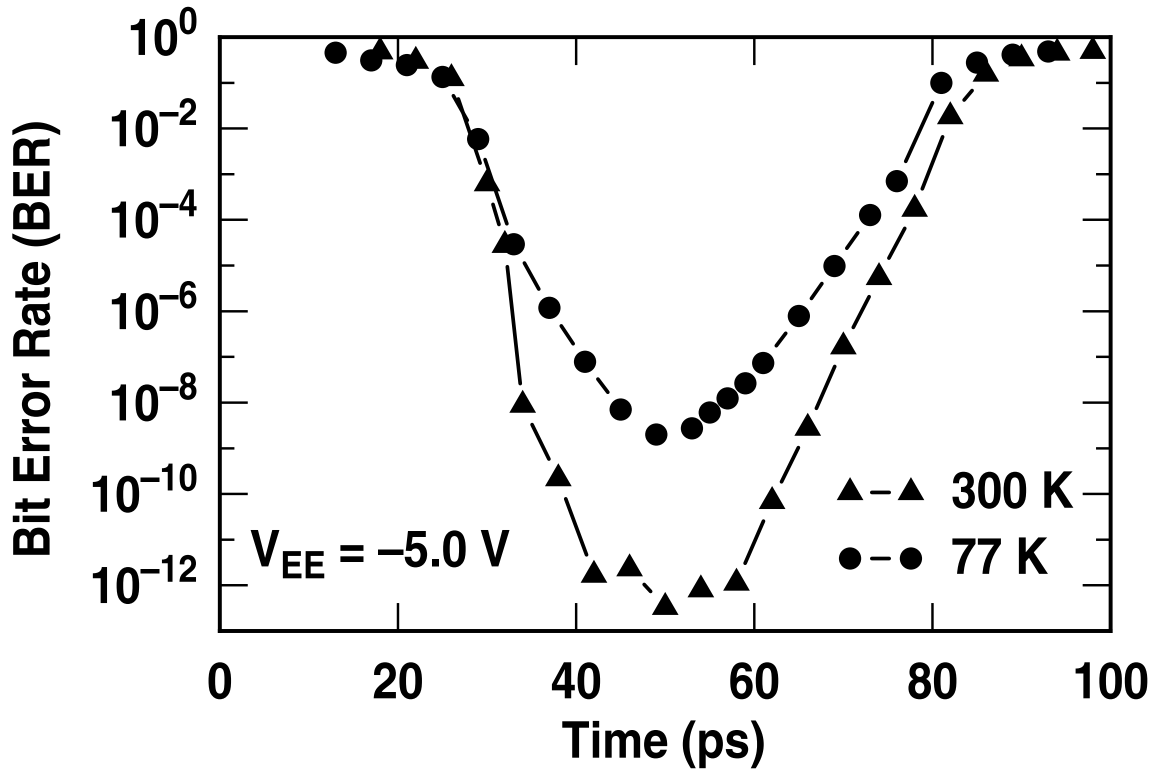


Figure 54: Bathtub plot for the limiting amplifier at 77 K and 300 K.

6.4 Summary

The low-temperature measurement results of a high-gain, broadband, limiting amplifier designed using 120 GHz SiGe BiCMOS process is presented. This limiting amplifier was designed for operation in a narrow temperature range around 300 K. The amplifier shows aggravated gain peaking behavior at low temperature and therefore shows increased ringing in its time domain response at these temperatures. Based on the observed measurement results broad guidelines for room-temperature limiting amplifier design intended for low temperature application is proposed.

CHAPTER VII

DESIGN OF A HIGH-SLEW RATE SIGE BICMOS OPERATIONAL AMPLIFIER FOR OPERATION DOWN TO DEEP CRYOGENIC TEMPERATURES

7.1 Introduction

Operational amplifiers (op-amps) represent a ubiquitous and essential analog building block that finds application in a wide variety of high-performance precision analog circuits such as switched-capacitor filters, analog-to-digital converters, and precision sensors. Recently, there has been a growing interest in using such high-performance analog circuits for niche applications such as "extreme environment" electronics, and in particular for electronics capable of operating down to deep cryogenic temperatures, as might, for instance, be encountered on the Moon (+120 °C to -180 °C, and even down to -230 °C) [8].

The key device parameters of bandgap-engineered silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs), such the transconductance (g_m), current gain (β), and Early voltage (V_A), that are critical to op-amp performance are favorably impacted by cooling [30]. Thus, analog building blocks such as op-amps, designed using a combination of scaled Si CMOS and SiGe HBTs, could potentially offer an optimal solution for such cryogenic applications. Although the key device parameters of well-designed SiGe HBTs show remarkable improvement down to cryogenic temperatures, it remains to be demonstrated that this device-level performance in fact translates to superior circuit performance at low temperatures. NASA's upcoming lunar missions present a unique venue for practicing low temperature electronics in the SiGe material system. The envisioned lunar robotic electronics systems will be subjected to very large temperature variations (> 300 °C), and are cyclic

in nature. As mentioned in Chapter I, the on-board electronics are housed in a centralized warm box (Fig. 2), which shields them from temperature changes, thus maintaining a narrow temperature range required for their reliable operation. Such warm boxes, apart from being power hungry, bulky, and heavy, compromise the ability to realize distributed system architectures [8].

Because of its attractive cryogenic performance and inherent robustness to ionizing radiation, SiGe-based mixed-signal electronic systems could potentially be deployed outside the spacecraft warm box in so-called remote electronics units (REUs), for needed sensing and data acquisition functions. Realization of key circuit blocks such as voltage and current references, op-amps, and ADCs in SiGe technology are a critical first step.

In this chapter the design of a SiGe BiCMOS op-amp for such extreme temperature range lunar electronic systems is presented [5]. This is the first monolithic op-amp (for any material system) capable of operating reliably down to 4.3 K. The design methodology used in the present work is based on a circuit architecture described in [64]. The high-slew rate capability is achieved by using an auxiliary slew-buffer that enhances the output drive capability during slewing. Two variants of the SiGe BiCMOS op-amp were implemented using alternative biasing schemes, and the effects of temperature on these schemes and the overall performance of the op-amp, is carefully examined.

7.2 Device Technology and Cryogenic Operation

This SiGe BiCMOS op-amp was fabricated in a commercial, deep- and shallow-trench isolated SiGe HBT BiCMOS technology, which integrates 0.5 μm, 3.3 V BV_{CEO}, 50 GHz f_T, 3.3 V BV_{CEO}, and 55 V V_A SiGe HBTs (at 300 K), together with 0.5 μm, 3.3 V Si CMOS devices [32]. It supports a full suite of passive elements including metal-insulator-metal (MIM) capacitors and low T_C poly resistors. This is a five metal layer process (all aluminum) with a top thick aluminum layer that enables high-Q spiral inductors.

The SiGe HBTs from this technology generation show a strong monotonic increase in

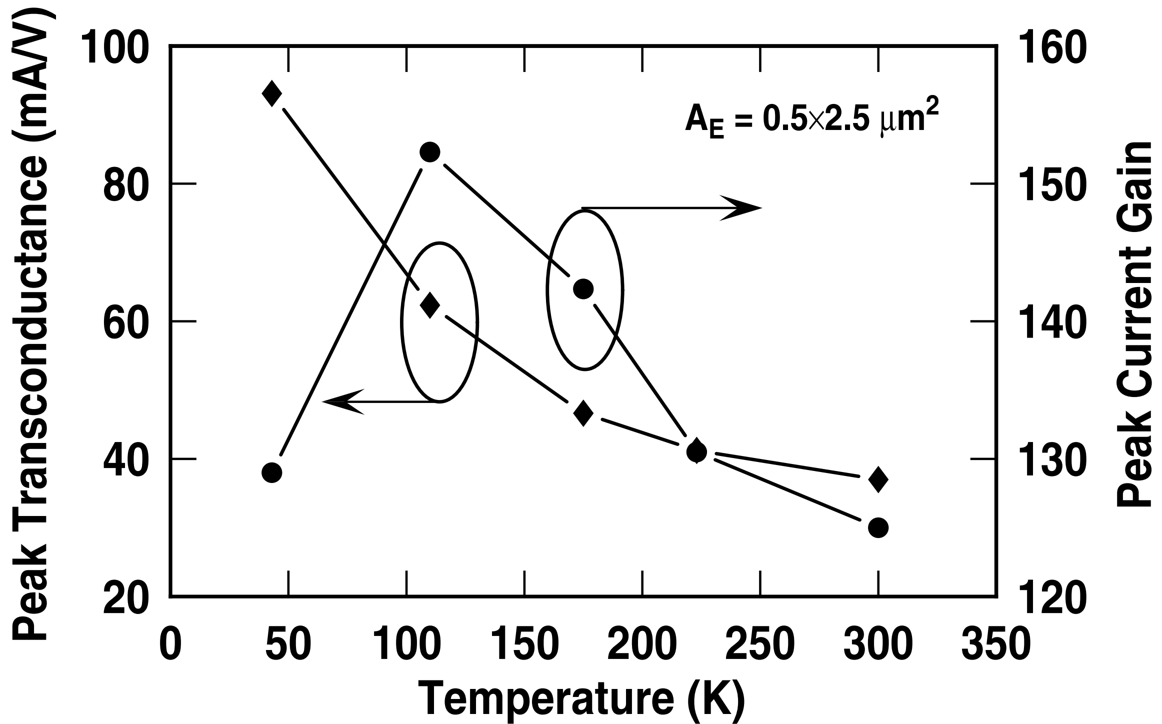


Figure 55: Peak g_m and peak β versus temperature of the SiGe HBT with emitter area of $0.5 \times 2.5\ \mu m^2$.

peak g_m with cooling (Fig. 55). In addition, with the Ge-induced base bandgap changes coupling strongly to the device equations in SiGe HBTs, β either increases or stays close to its room-temperature value down to deep cryogenic temperatures (Fig. 55). Although the increase in peak g_m should favorably translate into improved gain-bandwidth and slew rate performance in op-amps at low temperatures, this is highly dependent on the behavior of the bias current over temperature, as addressed below.

7.3 Circuit Design

The block diagram of the SiGe BiCMOS slew-enhanced op-amp is shown in Fig. 56. The overall amplifier consists of an amplifier core, which provides all of the small-signal amplifier gain, and the auxiliary slew-buffer, which comes into action when the input is slewing, thus enabling the fast slewing of the output under very large capacitive loads. The amplifier is designed to work off of a single power supply V_{cc} of 3.3 V. The unity-gain

buffer configuration of the amplifier is obtained by connecting the output of the op-amp to the negative input.

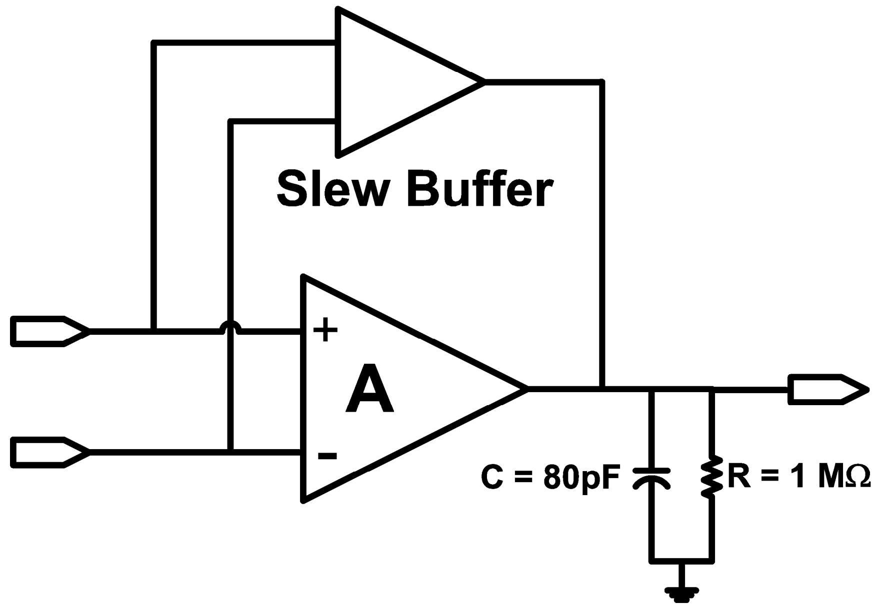


Figure 56: The op-amp block diagram showing the core amplifier (A), the slew-buffer, and a typical load condition.

7.3.1 Amplifier Core Design

The amplifier core was implemented using a conventional folded cascode topology (Fig. 57) [65]. The folded cascode architecture achieves a wider input common mode range (ICMR), higher gain, more stable control over gain-bandwidth (due to self-compensation), higher output impedance, and higher power supply rejection, than a two stage op-amp with active loads. SiGe HBTs were used in the input differential pair to exploit their large g_m and inherent enhancement with cooling, as well as their superior matching properties. Due to the large output resistance of the SiGe HBT, the dominant pole of the op-amp is at the output, and hence the small-signal gain-bandwidth product (GB) of the self-compensated op-amp (including the slew-buffer) is given by,

$$GB = \frac{g_m}{C_L} \tag{10}$$

where g_m is the transconductance of a SiGe HBT in the input differential pair, and C_L is the load capacitance.

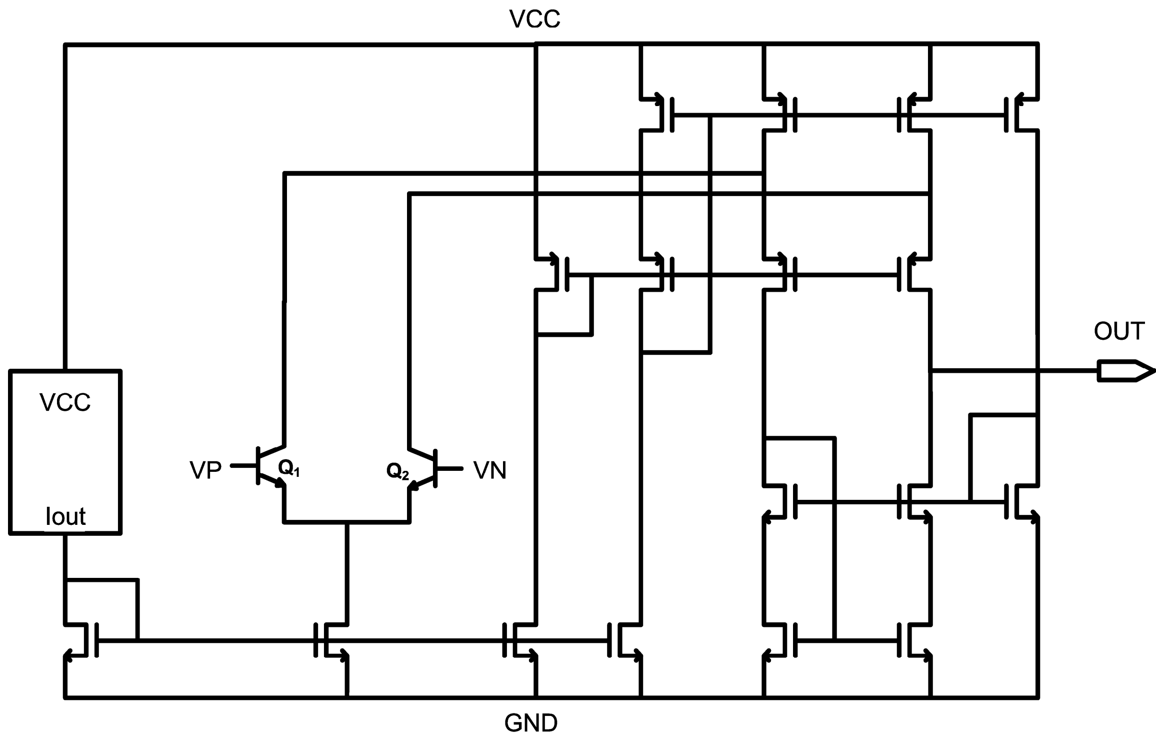


Figure 57: Folded cascode amplifier core with bias block and SiGe HBT input stage.

7.3.2 Slew-Enhancement Technique

There are several techniques available for slew-enhancement of conventional op-amps, each with differing trade-offs. The technique described in [66] achieves slew-enhancement by internally switching the output buffer to high-drive mode when the inputs are slewing. This technique, however, can not be easily extended to the amplifier cores in a folded cascode architecture, and has been reported to have large variations in quiescent current with varying temperature [64], and is thus not suitable for the wide temperature range operation needed here. Another slew-enhancement technique employs an adaptive biasing scheme [67] where the bias current to the amplifier core is increased by a factor of the difference in the branch currents of the input differential pair. When the input slews, there

is a large mismatch in the branch current, resulting in large core bias current, thus providing a higher drive at the output. This technique suffers from high power dissipation in the amplifier core during transients.

The slew-enhancement used in the present design is achieved by using a slew-buffer (Fig. 58) whose load transistors ML1 and ML2 are biased in the triode region. This condition is achieved by sizing ML1 and ML2 such that $I_1 < I_2$, where I_1 is half the tail current and I_2 is the saturation current in ML1 and ML2. Thus, under small-signal conditions when the input terminals VP and VN are nearly equal, the gates of MO1 and MO2 (the output transistors) are pulled close to V_{cc}, turning them off. However, when the input is slewing, there is a large difference in the potentials of VP and VN, causing one of the load transistors to saturate, thereby pulling the gate terminal of the corresponding output transistor closer to ground potential. This turns-on the output transistor very hard, causing it to deliver large currents to the output. Hence, during slewing the bias to the amplifier core is unaffected, which is clearly desirable. The threshold input differential voltage ($V_{in,th}$) required for triggering the slew-buffer is given by [64],

$$V_{in,th} = \alpha\sqrt{\frac{I_1}{\kappa}} \tag{11}$$

where α is defined such that $I_2 = (1 + \alpha)I_1$, and κ is the MOS conductance parameter of the input transistors of the slew-buffer.

7.3.3 Biasing Schemes

The SiGe op-amp was implemented using two different bias schemes, each with a varying temperature response, for the output bias current. The first bias scheme utilizes a conventional wide-swing cascode bias circuit [68]. This bias scheme features a wide-swing bias current loop and a start-up circuit to avert the zero current bias condition. The efficacy of the start-up circuit was checked via simulations down to -55 °C, and worked well down to 4.3 K.

The second bias scheme, called "weak-T bias" here, is based on a resistor-free current

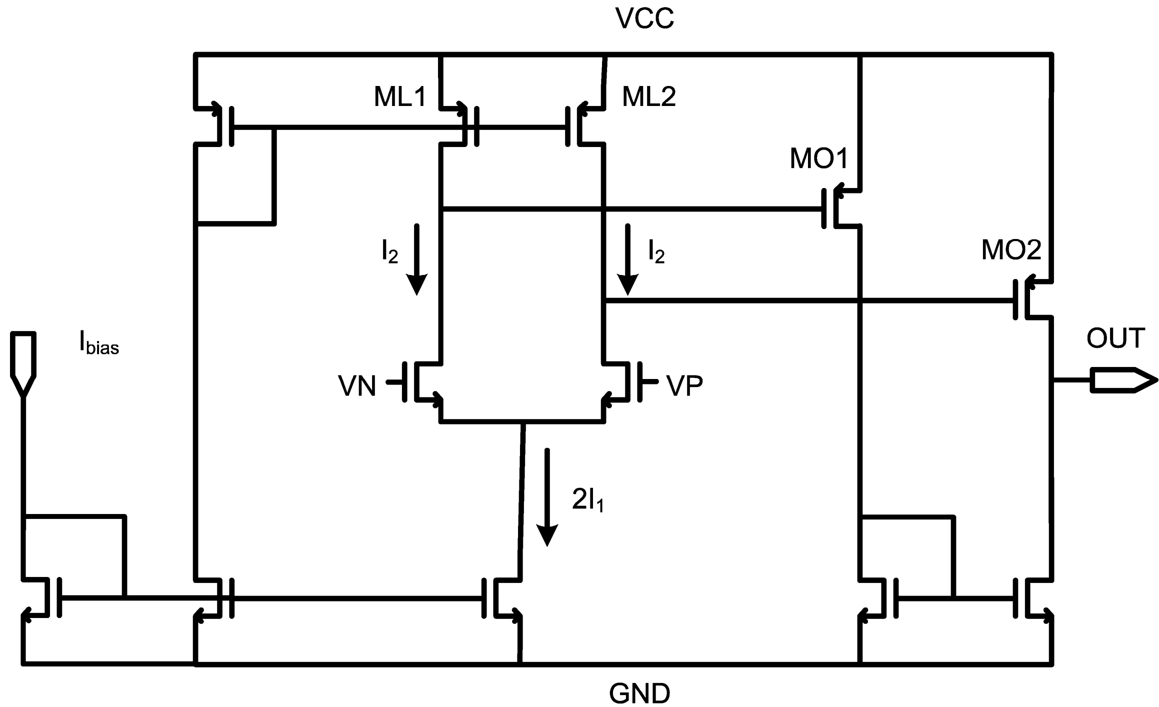


Figure 58: Slew-buffer with load transistors biased in the linear region.

reference that is designed to reduce overall analog performance variation over a wide temperature ranges (Fig. 59) [69]. The output bias current of this current source is given by, $2m\mu C_{ox}U_T^2$ where m is a temperature independent scaling factor, μ is the mobility ($\propto T^{-1.5}$ for PMOS), C_{ox} is the oxide capacitance, and U_T is the thermal voltage. It is therefore expected that the resultant g_m of the SiGe HBT biased using this current source will be proportional to $\mu C_{ox}U_T$ ($\propto T^{-0.5}$) and the corresponding slew rate will be proportional to $\mu C_{ox}U_T^2$ ($\propto T^{+0.5}$). Thus, the residual temperature dependence of these key parameters are rendered weak by this biasing scheme, ensuring reduced small-signal and large-signal performance variations over temperature. The simulated SiGe HBT g_m behavior over temperature for weak-T bias is in qualitative agreement with the above analysis (Fig. 60). In addition, observe the opposite trends in g_m response for the two different bias schemes. The chip micrograph of the op-amp is shown in Fig. 61.

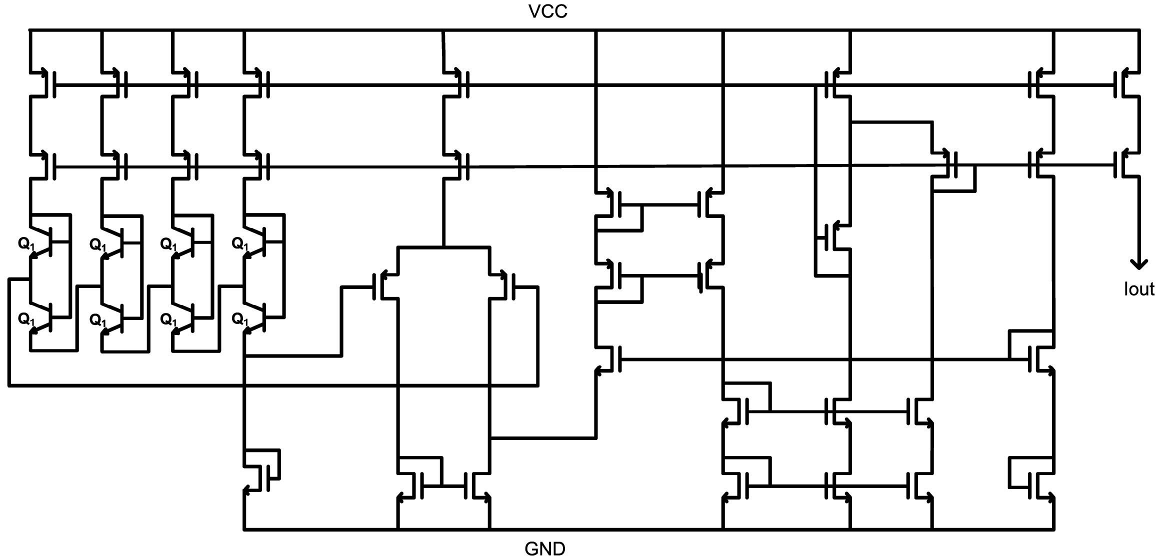


Figure 59: Weak-T current bias circuit with SiGe HBT PTAT chain and a transconductor (start-up circuit not shown).

7.4 Measurement Results and Discussion

The *dc* and *ac* characterization was performed on the unity-gain buffer configuration of the op-amp using a custom-designed cryogenic probe station capable of operating down to 4.3 K.

7.4.1 *dc* Characteristics

The op-amps with either of the current sources drew a total bias current of 4.3 mA nominally at room temperature. The total bias current dropped monotonically with cooling in the conventional bias case and to 143 K in the weak-T-based circuit (Fig. 62). There was, however, an anomalous increase in bias current below 143 K in the weak-T op-amp. The input-referred offset voltage tracked the temperature behavior of the bias current. The input-referred offset power for the op-amp can be approximated as [70],

$$V_{os}^2 = V_{os,core}^2 + V_{os,slew}^2, \quad (12)$$

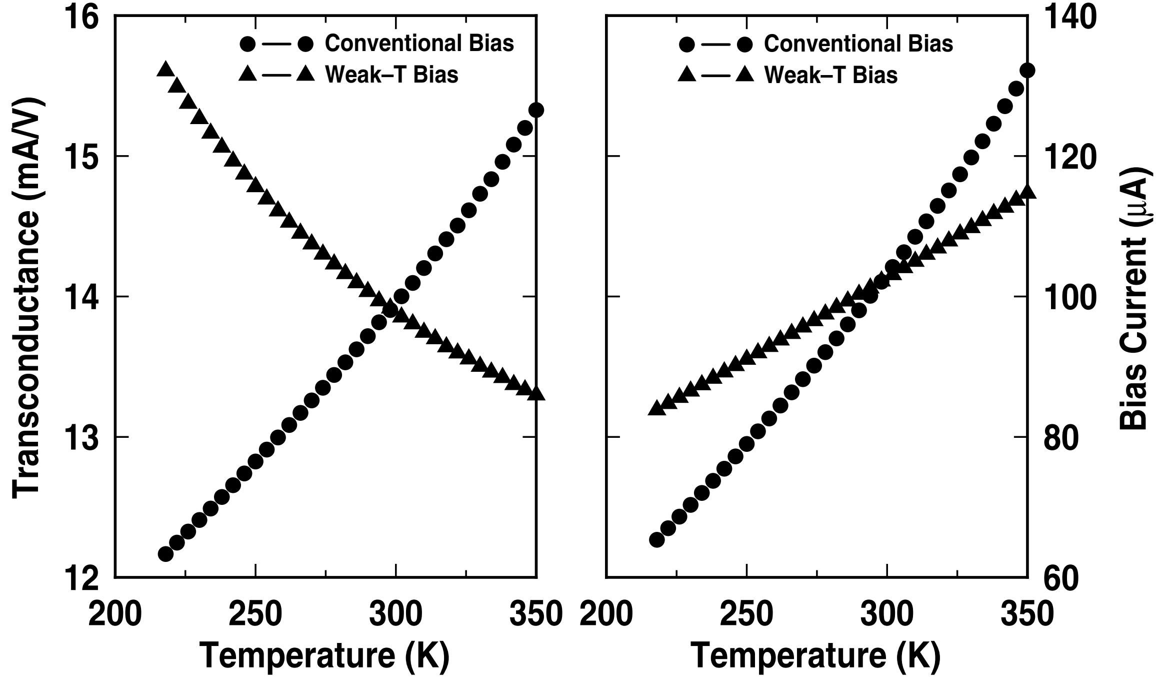


Figure 60: Simulated input SiGe HBT g_m of the two circuits versus temperature for the corresponding bias tail current.

where,

$$V_{os,core}^2 \simeq U_T^2 \left[\frac{\triangle V_{TP}^2}{\left(\frac{V_{ov,p}}{2}\right)^2} + \frac{\triangle (W/L)_P^2}{(W/L)_p^2} + \frac{\triangle I_S^2}{I_S^2} \right], \quad (13)$$

and

$$V_{os,slew}^2 \simeq \triangle V_{TN}^2 + \left(\frac{V_{ov,N}}{2}\right)^2 \times \left[\frac{\triangle V_{TP}^2}{\left(\frac{V_{ov,N}}{2}\right)^2} + \frac{\triangle (W/L)_P^2}{(W/L)_P^2} + \frac{\triangle (W/L)_N^2}{(W/L)_N^2} \right]. \quad (14)$$

Therefore, the offset contribution from the core amplifier is expected to drop naturally with cooling ($\propto U_T^2 \propto T^2$) and with the decrease in bias current ($\propto V_{ov}^2 \propto I_{bias}^2$), and for the same reason the contribution from the slew-buffer is expected to also drop with bias current. Thus, the overall offset decreases with temperature for both bias schemes; clearly good news. The higher offset voltage in the op-amp with weak-T bias is possibly due to the additional current mismatches introduced by PTAT chain and the transconductor.

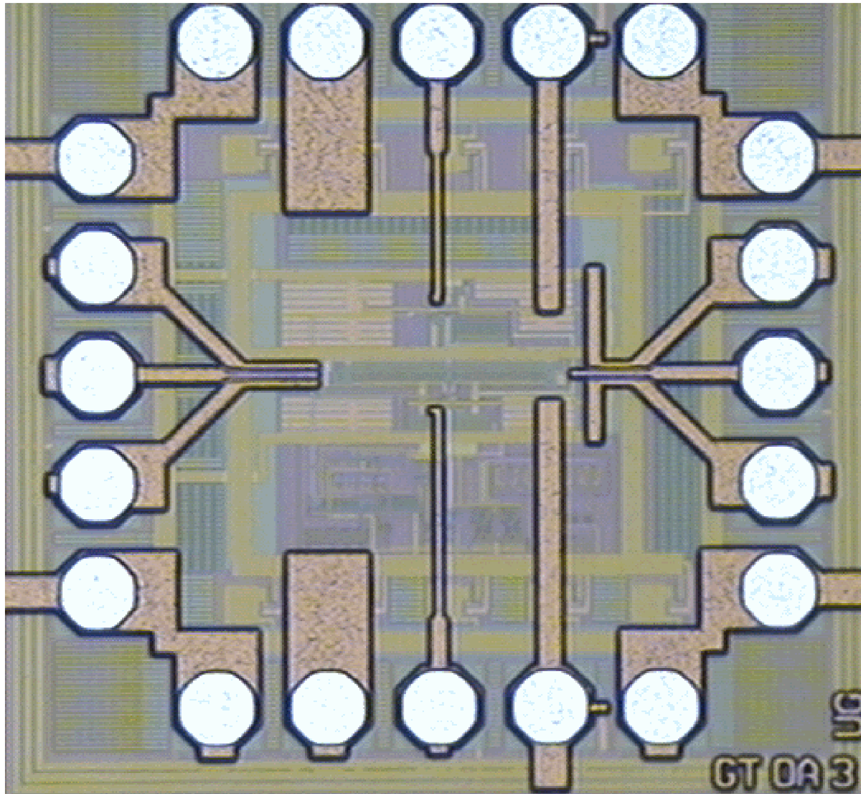


Figure 61: Chip micrograph of the slew-enhanced operational amplifier.

The ICMR of both variants of the SiGe op-amp remained fairly constant across temperature. Closer examination of the $ICMR_{min}$ does indicate a moderate increase attributable to the (expected) increase in the base-emitter turn-on voltage of the input differential pair with cooling.

7.4.2 Slew-Rate and Gain-Bandwidth

The op-amp with conventional bias displayed robust start-up down to 4.3 K, and had useful gain-bandwidth and appreciable slew rate at this temperature. To the author's knowledge, this is the first monolithic op-amp capable of operating at this low a temperature. The op-amp with weak-T bias showed a moderate increase in both positive and negative slew rates down to 143 K and further down in temperature a dramatic increase was observed in slew rate, which can be ascribed to the bias current behavior at these temperatures (Fig. 63). The op-amp with conventional bias, on the other hand, showed only a moderate decrease

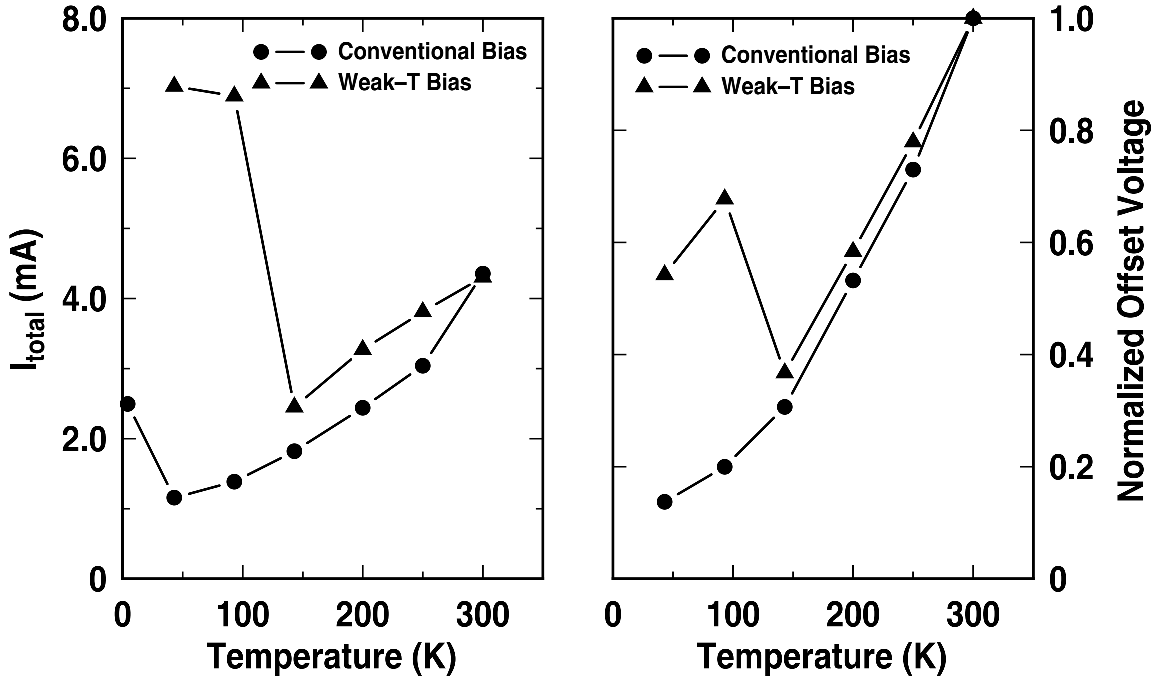


Figure 62: Measured total bias current and normalized input-referred offset voltage versus temperature for the two circuits.

in both the slew rates not readily explained using the bias current decrease. This slew rate behavior suggests that the slew-buffer effectively decouples the output slewing from the tail bias currents, and thus making it a weak function of temperature, a desirable attribute for the op-amp.

The small-signal gain-bandwidth is still tied intimately to the input transconductance of the op-amp. This observation was confirmed qualitatively by the comparing the simulated g_m of the input SiGe HBTs (Fig. 60) with the measured gain-bandwidth of the two circuits (Fig. 64). While the gain-bandwidth of the op-amp with weak-T bias increases with cooling down to 143 K, the gain-bandwidth of the conventional bias op-amp degrades steadily with cooling. The *dc* gain, however, did not track the input transconductance of the op-amp for both bias schemes, suggesting the possible influence of the slew-buffer at low temperatures in small-signal gain enhancement (Fig. 65). The op-amp maintained excellent stability across temperature, as evidenced by the overshoot and the inferred phase margin (Fig. 65).

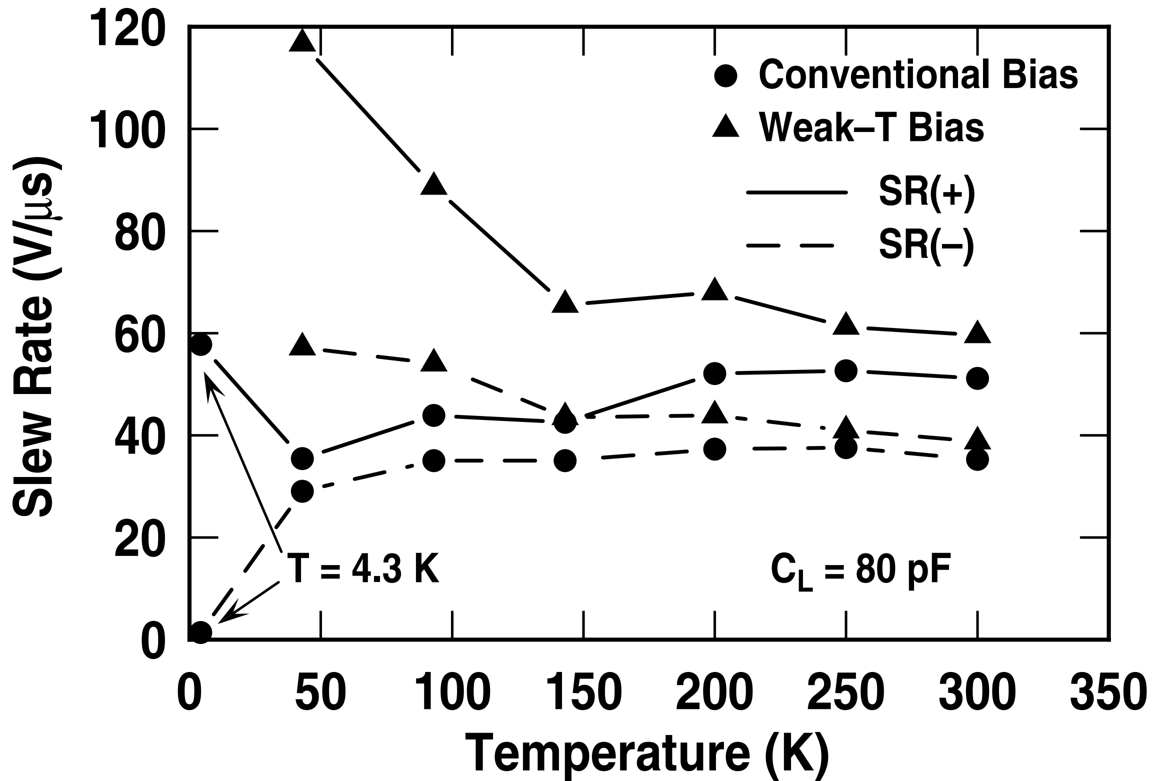


Figure 63: The positive and negative slew rates of the circuits across temperature.

7.5 Summary

A SiGe BiCMOS op-amp capable of operating across a very wide temperature range, and down to temperatures as low as 4.3 K was designed and implemented. Thus it can be concluded that SiGe technology offers an ideal approach for developing a wide variety of analog and mixed-signal building blocks for emerging extreme environment electronics applications.

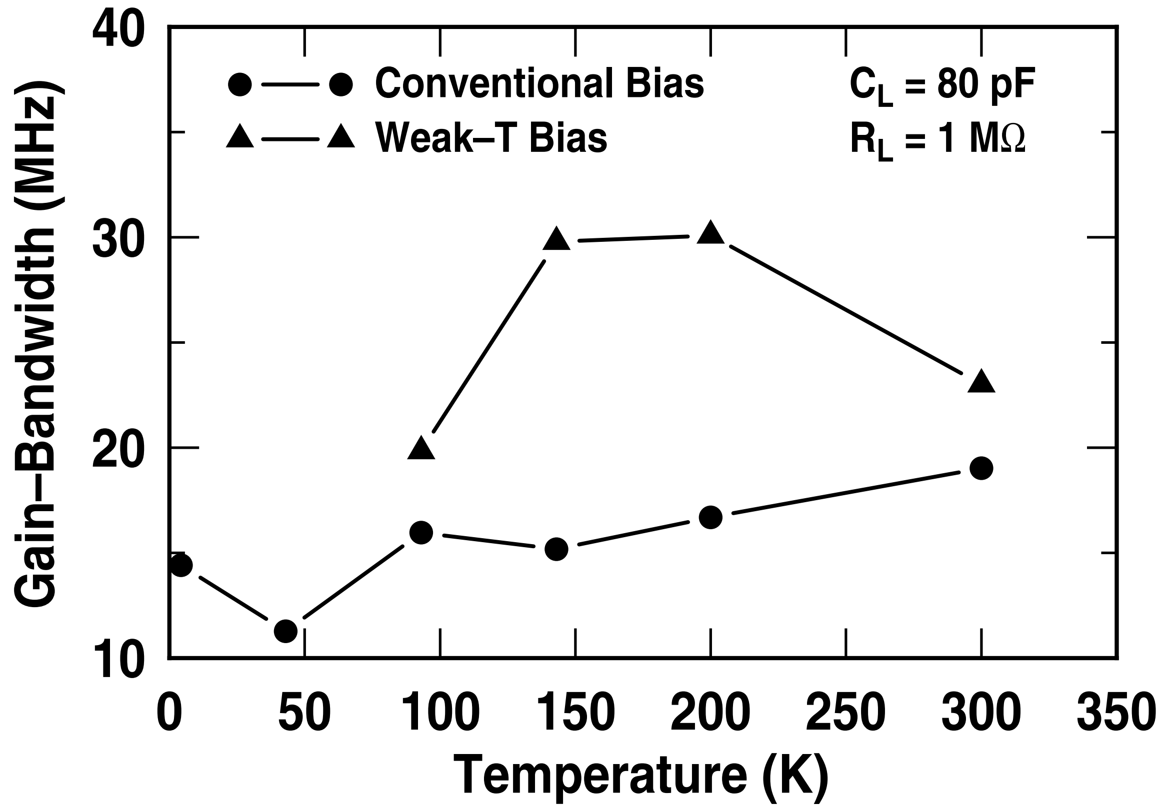


Figure 64: Gain-bandwidth of the SiGe op-amps versus temperature.

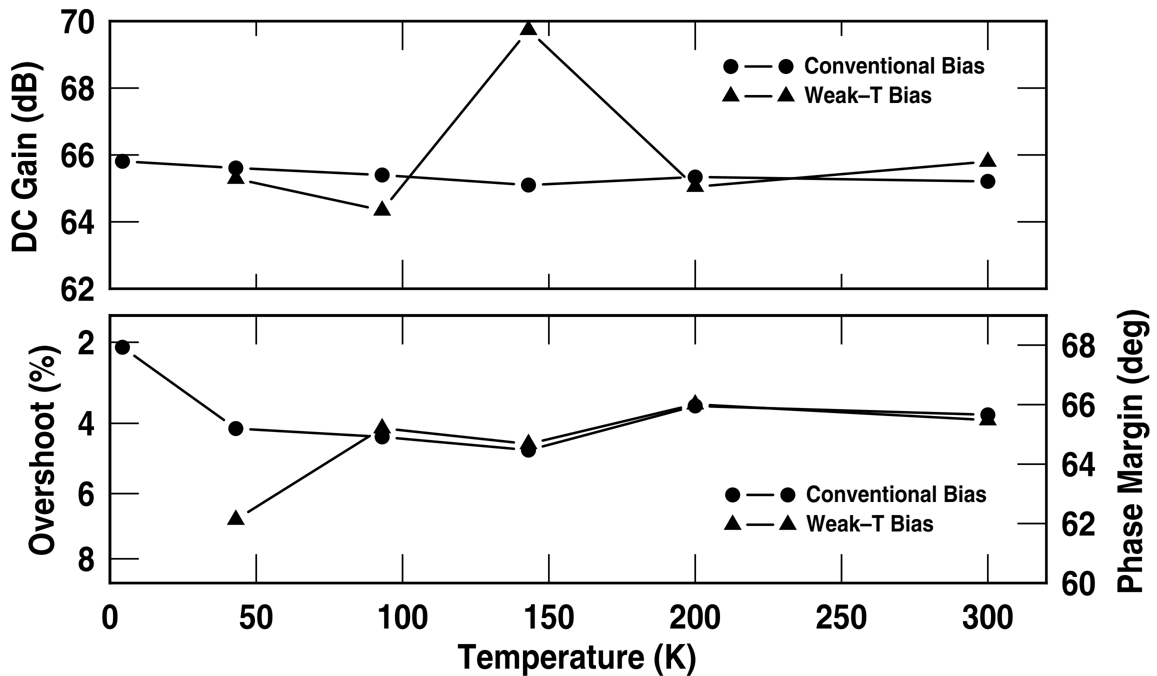


Figure 65: Measured *dc* gain and phase margin as a function of temperature.

CHAPTER VIII

HALF-TERAHERTZ OPERATION OF SIGE HBTS

8.1 Introduction

Electronic systems operating at near-optical, TeraHertz frequencies (10^{12} Hz = 1.0 THz = 1,000 GHz), have recently generated significant interest in the remote sensing community, and can potentially enable a host of intriguing applications. At present such prototype THz systems utilize either passive elements or 2-terminal electronic devices (e.g., Schottky diodes). Clearly, however, it would prove extremely beneficial to have a 3-terminal semiconducting device (i.e., something exhibiting gain – a transistor) for such ultra-high-frequency systems. For instance, a transistor with usable gain could in principle be used for active sensing systems, as opposed to purely passive sensing systems. Not surprisingly, achieving a 1,000 GHz transistor for such purposes has proven to be an exceptionally challenging and elusive goal.

Nevertheless, there has been steady progress over the past few years in improving the frequency response in III-V HBTs, work primarily centering on the InP/InGaAs material system [71]–[77], and culminating in the present record for bipolar transistor performance of 710 GHz peak f_T at 300 K (with f_{max} = 340 GHz, β = 115, and BV_{CEO} = 1.75 V). Clearly, however, there are compelling reasons for attempting to achieve these extreme levels of performance in a low-cost, highly-integrated, integrated circuit manufacturing platform: i.e., in a silicon-based material system.

Scaling of SiGe technology has also rapidly progressed, with multiple commercial SiGe BiCMOS technology platforms presently achieving 200 GHz peak f_T (e.g., [39]), while facilitating the merger of these SiGe HBTs, 130 nm CMOS, 5-7 layers of metal interconnect, and a full suite of passive elements, all on 200 mm Si wafers, enabling robust silicon-based

monolithic RF through mm-wave circuit design. Recent research demonstrations of npn SiGe HBTs with peak f_T of 350-375 GHz [42] and 380 GHz [78] represent the present performance records for SiGe technology.

It has been recently suggested, albeit via simulation, that TeraHertz-level (intrinsic) device frequency response should in fact be possible in suitably scaled SiGe HBTs [79], [80]. Recently SiGe HBT peak f_T of as high as 430 GHz at 50 K has been reported in the literature [81]. The work presented in this chapter, takes one more step in that direction, by demonstrating for the first time that SiGe HBT performance above 500 GHz is indeed possible in a fully silicon-manufacturing-compatible SiGe platform [6].

8.2 SiGe HBT Technology

The device structure utilized here for this prototype fourth-generation SiGe HBT is very similar topologically to that of a commercially-available, third-generation device, and utilizes a reduced thermal cycle, "raised extrinsic base" structure [42]. The device is deep- and shallow-trench isolated, has an $in-situ$ phosphorus-doped polysilicon emitter, and a compositionally-graded, carbon-doped, unconditionally stable, 25% peak Ge content, UHV/CVD SiGe base. Aggressive vertical profile scaling and careful collector implant tailoring were used to maximize f_T. This device is 100% silicon (CMOS) fabrication compatible, and was fabricated on a 200-mm wafer.

Given that the emphasis in this study is on vertical profile optimization, these devices were fabricated using a pre-existing third-generation (130 nm) SiGe HBT maskset, and thus should be considered unoptimized with respect to lateral device parasitics (both resistance and capacitance), negatively impacting the maximum oscillation frequency (f_{max}). Thus it is believed that the f_{max} values presented here can be significantly improved.

8.3 Measurement Setup

The transistors were measured on a customized, on-wafer, open-cycle, liquid helium cryogenic probe system. The system thermometry was verified by comparing devices measured within the system with those measured directly immersed in both liquid nitrogen (77.3 K), and liquid helium (4.2 K). The temperature accuracy is believed to be better than 1 K.

On-wafer calibrated S-parameters were measured to 35 GHz using an Agilent 8510C Vector Network Analyzer (the practical upper frequency limit of the test system). The through-reflect-reflect-match (LRRM) technique was used to calibrate out the cable and probe-induced losses at each temperature. Conventional on-chip "open" and "short" calibration structures located adjacent to the device under test were used at each temperature to de-embed the pad capacitance and inductance from the measured S-parameters. The results presented are repeatable.

8.4 Electrical Results

Due to its bandgap-engineered base, cooling is well-known to favorably affect the performance of SiGe HBTs [18]–[21], [3], [81]–[83]. The present SiGe HBTs exhibit near-ideal current-voltage characteristics down to 4.5 K (Fig. 66). As expected, the decrease in intrinsic carrier concentration with cooling causes the base-emitter turn-on voltage to increase as the temperature decreases [30], but the device output current drive is not degraded with cooling, and the transistor is able to source greater than 75 mA/μm^2 current density at 4.5 K. The peak transconductance (g_m) rises with cooling, as expected, from 65 mS at 300 K to 102 mS at 4.5 K, demonstrating that SiGe HBTs can achieve extremely high g_m per unit area (in this case, 850 mS/μm^2 at 4.5 K) compared to FETs (Si CMOS or III-V). Because the base, emitter, and significant portions of the collector are heavily doped (well-above the Mott transition of $3 - 4 \times 10^{18}$ cm^{-3} in silicon), carrier freeze-out

is minimized down to 4.5 K. The base current ideality in advanced SiGe HBTs at low temperatures is limited by field-assisted generation/recombination and trap-assisted tunneling processes [30], but is held in check in these devices via careful emitter-base spacer design to reduce the local field. The current gain (β) increases monotonically with cooling, as expected, down to 4.5 K (Fig. 67). The BV_{CEO} degrades only slightly with cooling (from 1.47 V at 300 K to 1.36 V at 4.5 K).

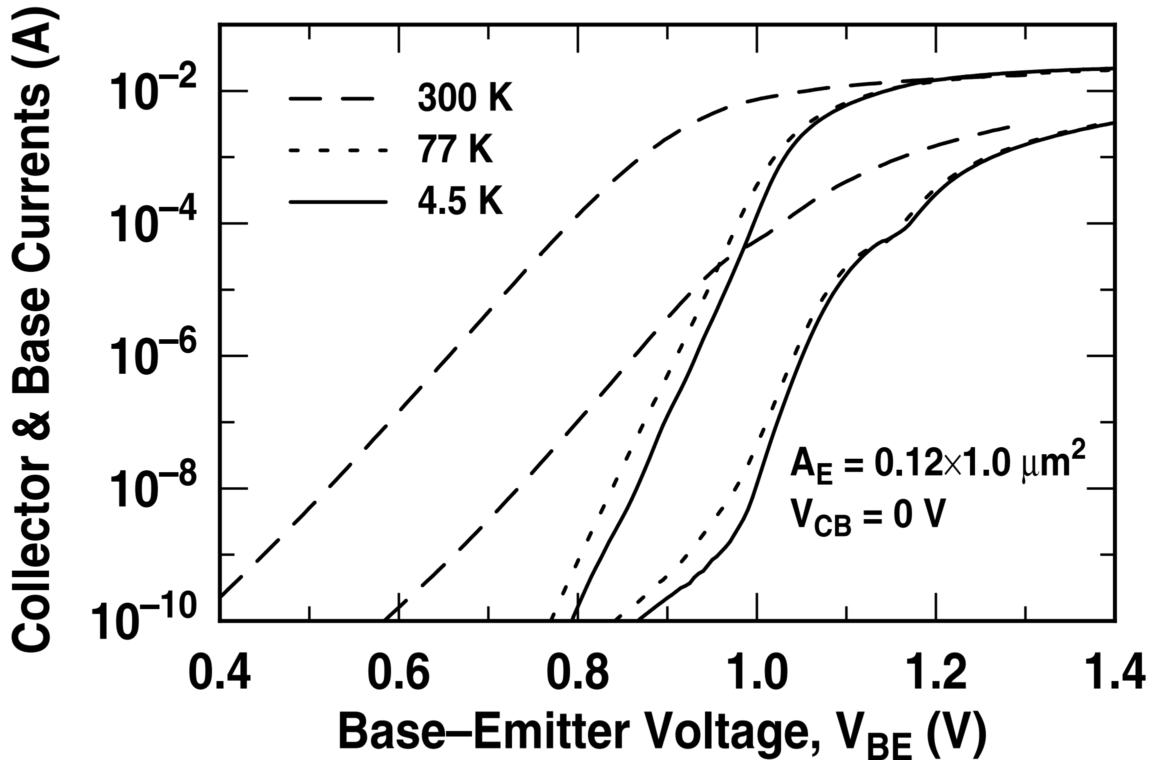


Figure 66: The current-voltage characteristics of a 0.12×1.0 μm^2 SiGe HBT at 300 K, 77 K, and 4.5 K.

Figure 68 shows the small-signal current gain (h_{21}), extracted from the de-embedded S-parameters at 300 K and 4.5 K, for the 0.12×1.0 μm^2 device biased at peak f_T (a 0.12×2.5 μm^2 device has also been measured, with similar results). The f_T value was then inferred using a -20 dB/dec extrapolation from the measured h_{21} value at a given frequency. The inset in Fig. 68 shows the inferred f_T as a function of extrapolation frequency at 300 K and 4.5 K, indicating that the inferred peak f_T is independent of frequency, as expected for a robust extraction process. This SiGe HBT achieves a record peak f_T of 510 GHz at 4.5 K,

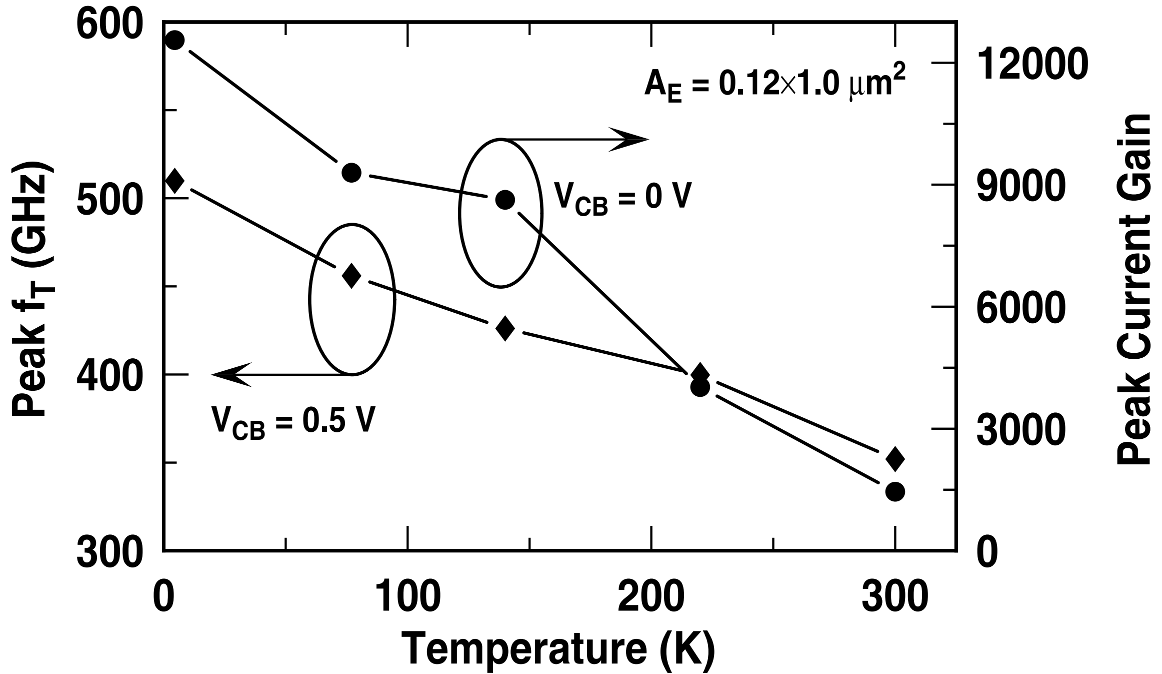


Figure 67: Peak current gain (β) at $V_{CB} = 0.0$ V and peak f_T at $V_{CB} = 0.5$ V for a $0.12\times1.0\ \mu m^2$ SiGe HBT, as a function of temperature.

at a collector current density of 21 mA/μm^2 (352 GHz at 300 K at 27 mA/μm^2), as shown in Fig. 69. The extrapolated emitter-to-collector delay is 0.27 ps at 4.5 K (0.36 ps at 300 K). The slight decrease in J_C at peak f_T with cooling is due to the interplay between the temperature dependence of the onset of Kirk effect (which increases slightly with cooling) and the onset of heterojunction barrier effects, (which decreases with cooling) [30]. The transistor f_{max} was inferred using the unilateral power gain (U), in a manner similar to that for f_T. Transistor performance at 300 K, 77 K, and 4.5 K is summarized in Table 7. It is worth noting that the transistor peak f_T is increased significantly with cooling without sacrificing its breakdown voltage. The slight degradation in observed f_{max} from 77 K to 4.5 K is believed to be due to r_{bb}, and driven by the temperature dependence of the majority carrier mobility.

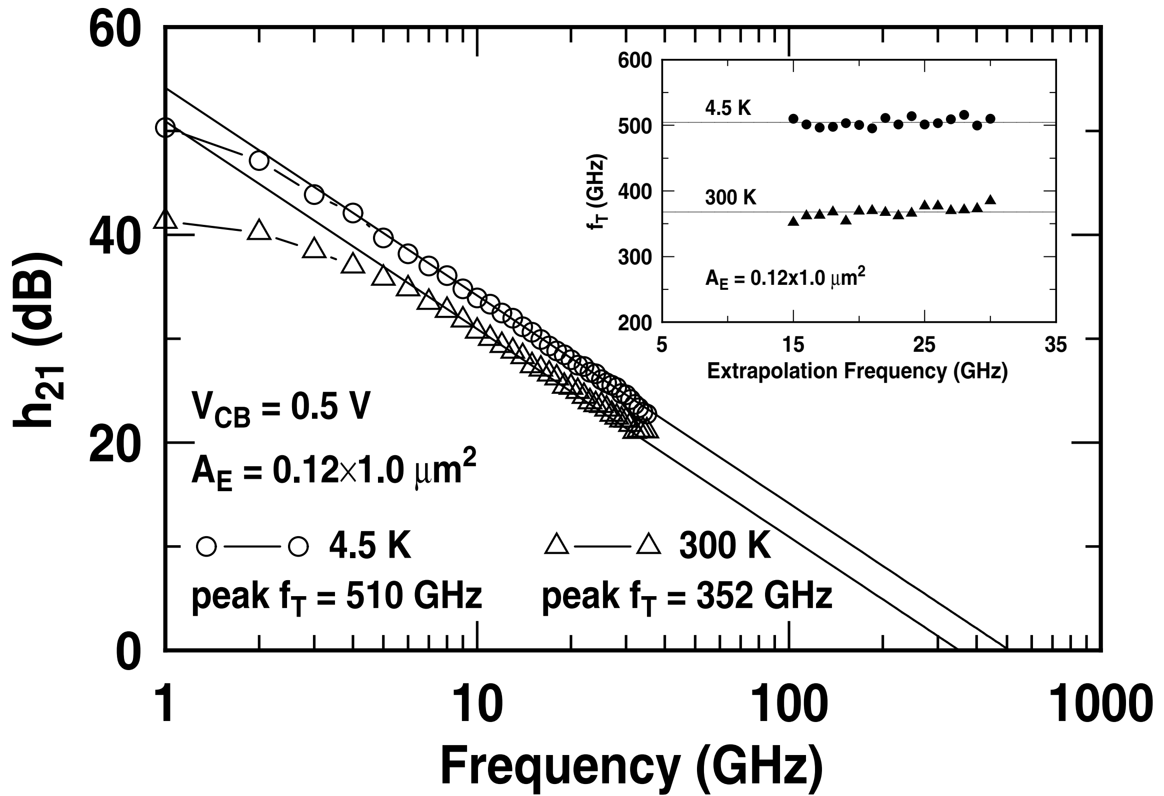


Figure 68: The small-signal current gain at 300 K and 4.5 K for a 0.12×1.0 μm^2 SiGe HBT, at peak f_T. Inset shows the inferred f_T as a function of extrapolation frequency.

8.5 Summary

A record peak f_T is achieved in SiGe HBT technology at 4.5 K. These SiGe HBTs maintain excellent *dc* ideality down to 4.5 K, with a peak β of 12,554 at 4.5 K. The peak f_T increases monotonically with cooling, attaining a value of 510 GHz at 4.5 K, up from 352 GHz at 300 K. These results suggest that half-TeraHertz performance should be possible in highly-manufacturable, silicon-based integrated circuit platforms.

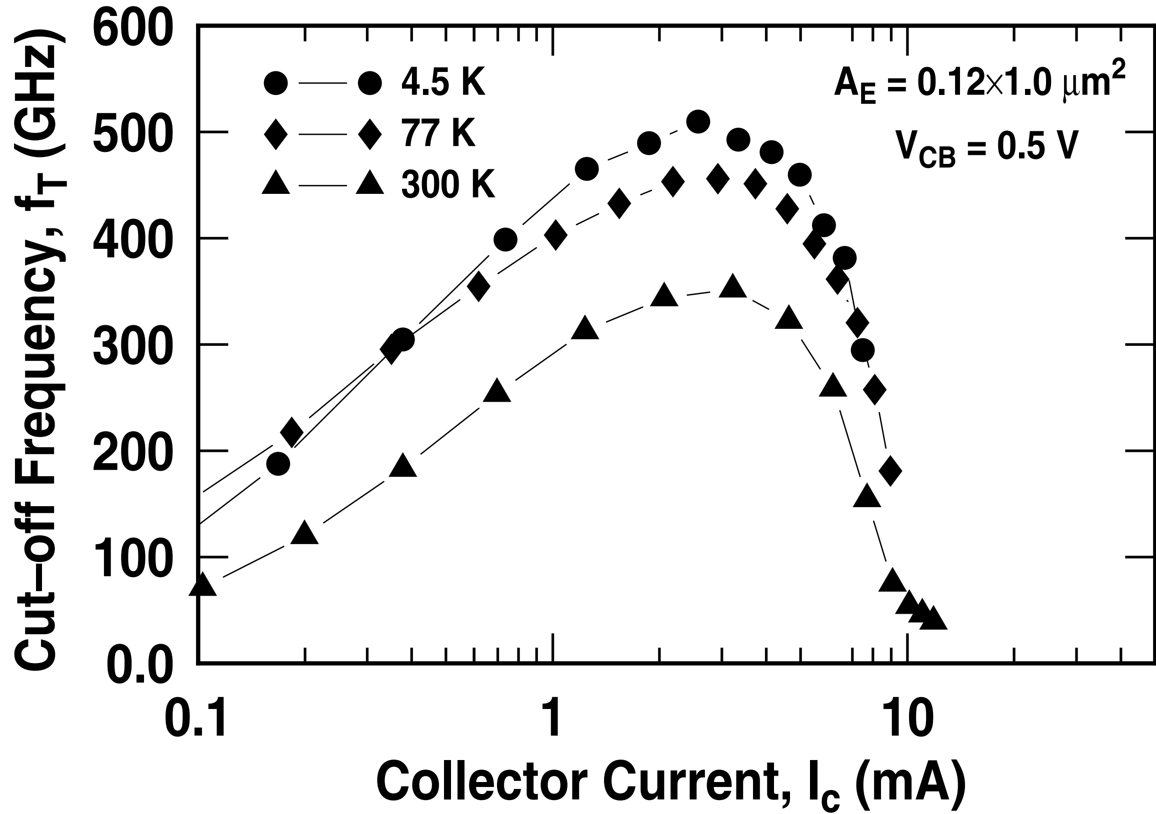


Figure 69: Measured peak f_T as a function of bias current for a 0.12×1.0 μm^2 SiGe HBT at 300 K, 77 K, and 4.5 K ($V_{CB} = 0.5$ V).

Table 7: Transistor performance summary at 300 K, 77 K, and 4.5 K, for an emitter geometry of 0.12 x1.0 μm^2.

Parameter	300 K	77 K	4.5 K
Peak β	1,449	9,297	12,554
Peak f_T (GHz)	352	456	510
Peak f_{max} (GHz)	241	295	276
r_{bb} at peak f_T (Ω)	304	206	305
Transit time (τ_f, ps)	0.36	0.33	0.27
J_C @ peak f_T (mA/μm^2)	27	24	21
BV_{CEO} (V)	1.47	1.43	1.36

CHAPTER IX

CONCLUSION AND FUTURE WORK

The contributions of this research in SEU hardening in SiGe HBT technology are:

1. Investigated the relative SEU tolerance in D-flipflops with multiple circuit architectures. Based on this study guidelines for hardening CML D-flipflops to achieve improved SEU immunity were proposed (Chapter II, also published in [31]).

2. Proposed architectural changes to the standard CML D-flipflop to improve its SEU immunity with minimal increase in power consumption and layout complexity (Chapter II, also published in [1]).

3. Developed circuit-level and device-level RHBD techniques for SiGe HBT logic circuits to improve its SEU sensitivity. Further, 16-bit shift registers featuring D-flipflops hardened using RHBD techniques were realized and tested with ion beam (Chapter III, also published in [2]).

The contributions of this research in cryogenic operation of SiGe HBT technology are:

4. Tested the feasibility of second-generation SiGe HBTs for cryogenic broadband data link by demonstrating the enhancement in *dc* and *ac* performance of these devices at cryogenic temperatures (Chapter IV, also published in [3]).

5. Realized a 24 GHz broadband limiting amplifier in second-generation SiGe HBT technology (Chapter V, also published in [4]). The amplifier achieved a saturated differential gain of 42 dB, a gain-bandwidth product of 3021 GHz, and a value of 16.93 A^{-1} for a newly proposed figure-of-merit.

6. Characterized the 24 GHz broadband amplifier at low temperature (Chapter VI).

7. Realized and characterized a slew-enhanced op-amp in first-generation SiGe BiCMOS technology capable of operating over a very wide temperature range and down to 4.3 K (Chapter VII, also published in [5]).

8. Demonstrated a record peak f_T in excess of one half-THz in fourth-generation SiGe HBTs at 4.5 K (Chapter VIII, also published in [6]).

In the future, the RHBD work can be extended by:

1. Investigating the device-level modifications to the SiGe HBT, such as adding shunt collector contacts for upset charge collection, without violating design rule check (DRC) rules to improve SEU immunity.

2. Investigating alternative circuit-level hardening techniques to improve SEU immunity with minimal increase in circuit complexity or power consumption.

3. Realizing larger shift-registers (>16-bit) for robust SEU immunity qualification.

4. Realizing shift-registers with faster switching speeds (>40 Gbit/s).

The cryogenic work can be extended by:

5. Developing reliable low-temperature models for all SiGe HBTs, FETs, and passives across all generations of this technology.

6. Realizing cryogenic limiting amplifier in third-generation SiGe HBT for data rates in excess of 40 Gbit/s.

7. Realizing improved slew-enhanced operational amplifiers with temperature independent bias schemes.

8. Investigating cryogenic *ac* and *dc* performance of fourth-generation for new device physics phenomena.

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