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AUTHOR: **Vishal Ajit Shah** DEGREE: **Ph.D.**

TITLE: **Reverse Graded High Content (x>0.75) $Si_{1-x}Ge_x$ Virtual Substrates**

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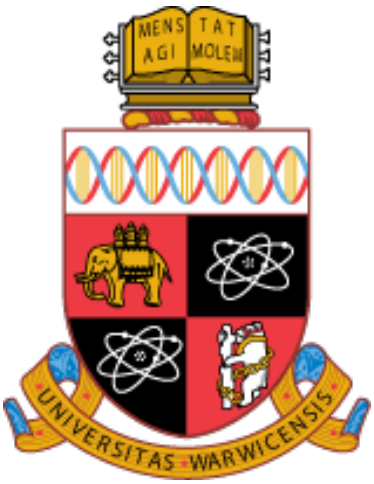

Reverse Graded High Content ($x>0.75$) $Si_{1-x}Ge_x$ Virtual Substrates

by

Vishal Ajit Shah

Thesis

Submitted to the University of Warwick

in partial fulfilment of the requirements

for admission to the degree of

Doctor of Philosophy

Department of Physics

THE UNIVERSITY OF WARWICK

Declaration

This thesis is submitted to the University of Warwick in support of my application for the degree of Doctor of Philosophy. All experimental data presented was carried out by the author, or (where stated) by specialists under the author's direction.

Abstract

Silicon germanium alloy layers can be grown epitaxially on a silicon substrate to provide a means of adjusting the lattice parameter of the crystal. Such a platform, known as a virtual substrate, has a number of potential applications. For instance, it allows for subsequent overgrowth of highly strained layers of silicon, or germanium, that could enable very high speed transistors, similarly it could be used as the starting point of a range a silicon-based optoelectronic devices. In this work, a novel adaptation has been made to a recently proposed reverse grading technique to create high Ge composition SiGe virtual substrates. The proposed structures consist of a relaxed, highly defected, pure Ge underlayer on a Si (001) substrate prior to reverse grading where structures have final compositions of $Si_{0.2}Ge_{0.8}$. Additionally, two grading schemes are studied, reverse linear grading and reverse terrace grading. All buffers are grown by reduced pressure chemical vapour deposition. The relaxation, defect levels and surface roughness of the fabricated buffers have been quantified whilst varying the grading rate.

An ideal grading rate has been found where the quality of the buffer is very high, due to the highly defected Ge underlayer and that the buffer relaxes under tensile strain. Outside of this ideal grading rate three dimensional growth, stacking fault formation and crack generation can occur. Cracking of the buffer has been modelled and some conditions where the buffer is stable have been found. This study experimentally investigates this proposed solution and a crack-stable high quality buffer is fabricated. Comparisons have been drawn with other more popular buffer fabrication techniques and it is found that this technique has very competitive qualities.

Publications and Presentations

(Resulting directly from the study presented:)

Refereed Publications

1) V. A. Shah, A. Dobbie, M. Myronov, D. J. F. Fulgoni, L. J. Nash, and D. R. Leadley, *Reverse graded relaxed buffers for high Ge content SiGe virtual substrates,* Applied Physics Letters **93, 3** (2008).

2) V. A. Shah, A. Dobbie, M. Myronov, D. J. F. Fulgoni, L. J. Nash, and D. R. Leadley, Reverse graded SiGe/Ge/Si buffers for high-composition virtual substrates*,* Journal of Applied Physics (submitted 2009)

Conference Presentations

1) Reverse graded relaxed buffers for high Ge content SiGe virtual substrates (oral)

European Materials Research Society (E-MRS) 2008, May 26-30, 2008, Strasbourg, France

V. A. Shah, D. R. Leadley, E. H. C. Parker, J. Parsons, D. Fulgoni

2) Epitaxial growth of compressive strained Ge layers on reverse linearly graded virtual substrate by RP-CVD (oral)

European Materials Research Society (E-MRS) 2009, June 8-12, 2009, Strasbourg, France

M. Myronov, A. Dobbie, **V.A. Shah**, X.C. Liu, Van H. Nguyen and D.R. Leadley

3) Low temperature epitaxial growth of compressive strained Ge layers on reverse linearly graded virtual substrate by RP-CVD (oral)

6th International Conference on Silicon Epitaxy and Heterostructures (ICSI-6), May 17 - 22, 2009, Los Angeles, California, USA

M. Myronov, A. Dobbie, **V.A. Shah**, X.C. Liu, Van H. Nguyen and D.R. Leadley

4) Compressively strained Ge channel heterostructures grown by RP-CVD for the next generation CMOS devices (to be accepted)

2009 International Conference on Solid State Devices and Materials (SSDM 2009)*,* October 7-9, 2009, Miyagi, Japan

M. Myronov, **V.A. Shah**, A. Dobbie, Xue-Chao Liu, Van H. Nguyen and D.R. Leadley

5) Reverse graded virtual substrates for strained Ge devices (oral)

UK Semiconductors 2009, Sheffield, UK, July 1-2, 2009

D.R. Leadley, **V.A. Shah**, A. Dobbie, and M. Myronov

(Resulting from other work carried out during the duration of the thesis:)

Refereed Publications

1) P. M. Gammon, A. Perez-Tomas, M. R. Jennings, G. J. Roberts, M. C. Davis, **V. A. Shah**, S. E. Burrows, N. R. Wilson, J. A. Covington, and P. A. Mawby, Characterization of n-n Ge/SiC heterojunction diodes, Applied Physics Letters **93** (2008).

2) A. Perez-Tomas, M. R. Jennings, M. Davis, **V. Shah**, T. Grasby, J. A. Covington, and P. A. Mawby, *High doped MBE Si p–n and n–n heterojunction diodes on 4H-SiC*, Microelectronics Journal **38,** 1233-1237 (2007).

3) A. Perez-Tomas, M. R. Jennings, M. Davis, J. A. Covington, P. A. Mawby, **V. Shah**, and T. Grasby, Characterization and modelling of n-n Si/SiC heterojunction diodes, Journal of Applied Physics **102,** 5 (2007).

Conference Proceedings

1) Characterisation of p-n and n-n heterojunction diodes with high doped MBE Si on 4H-SiC

Proceedings of Workshop on Compound Semiconductor Devices and Integrated Circuits in Europe (WOCSDICE) 2007, May 20-23, 2007, Venice, Italy

A. Pérez-Tomás, M. R. Jennings, M. Davis, **V. Shah**, T. Grasby, J. A. Covington and P. A. Mawby

2) Molecular beam epitaxy Si/4H-SiC heterojunction diodes

Proceedings of the International Workshop on the Physics of Semiconductor Devices (IWPSD) 2007, December 17-20, 2007, Mumbai, India

A. Pérez-Tomás, M. R. Jennings, M. Davis, **V. Shah**, T. Grasby, J. A. Covington and P. A. Mawby

Meeting Presentations

1) Inducing Uniaxial Strain though Virtual Substrates

Institut fur Halbleitertechnik, Universitaet Stuttgart. 18th Dec. 2006

V.A. Shah, T. Grasby, E. H. C. Parker.

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Lastly, I would like to thank my parents, sister, brother and my girlfriend for all their support and patience throughout my academic career.

1 Introduction

1.1 The Semiconductor Industry

The microelectronics industry was born in 1947 when scientists at Bell Labs invented the *transistor,* which revolutionized the world of electronics. Shortly after, it was realised that enhancements could be made with the research of *semiconductors,* leading to the formation of the semiconductor industry in 1960. Today the industry is worth $249 billion [1].

In 2000, silicon accounted for 98% of the industry [2]. It's suitability over other materials is due to two reasons: its low cost is due to its abundance in the earth's crust and secondly its native oxide, silicon dioxide (SiO_2), has excellent material properties which have been utilised in transistors over the years. The most employed device on Si material has been the *metal-oxide-semiconductor-field-effect-transistor* (MOSFET). The industry has grown by following Moore's law as a basis for expansion which predicts that "the density of transistors on an integrated chip (IC) will double every 18 months" [3]. Figure 1.1 shows Moore's law and the commercial processors which have been produced by Intel. The traditional method to enhance the performance of transistors is by simply scaling their dimensions, the most important of these dimensions was the gate length. By this method not only is the density of transistors on a chip increased but so is the performance of each transistor. However, fundamental limitations in device performance and processing limit the future scaling of transistors [4].

Research into new materials [5] have been a major drive to find new ways to enhance the performance of semiconductor technologies. This is indicated by the drop of the use of silicon within the industry to 93% [6] in 2006. However, most of the semiconductor industry utilises silicon processing based fabrication plants, therefore using substrates of completely different materials would drive the cost of electronics up and is not viable. Therefore, materials deposited on a Si substrate for different applications are the best solution to the scaling problem. Germanium and silicon-germanium alloys have been studied for the last 30 years and can be processed with current fabrication facilities.

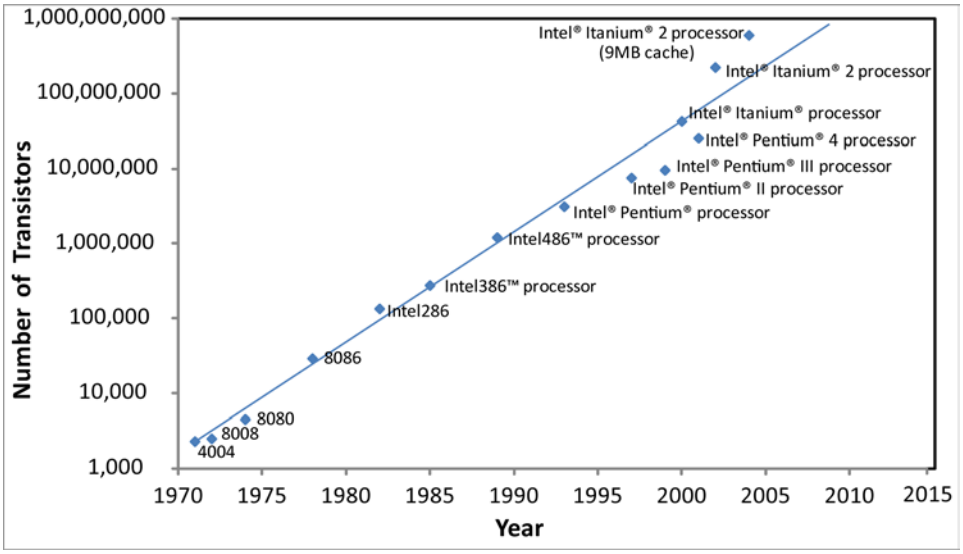

Figure 1.1: A graph showing Moore's law in action by plotting all the commercial transistors' release date versus the number of transistors per chip [7].

1.2 Introduction to Strain Engineering

The carrier *mobility* characterises the ease of charged carrier transport through a material. Increasing the mobility of carriers within the channel will enhance transistor performance. Electrons (negative charge) and holes (positive charge) are

the complementary carriers used in semiconductors and their mobilities in *bulk* silicon and bulk germanium are listed in Table 2.1. Mobility is defined as:

$$\mu = \frac{\upsilon}{E} \qquad \textbf{Equation 1.1}$$

Where μ is mobility, υ is the carrier drift velocity and E is the lateral electric field applied. It can be surmised that to achieve higher drift velocities for performance enhancements at lower electric fields, a *higher mobility material* is required. It can be seen from Table 2.1 that bulk pure germanium has higher mobilities for both holes and electrons.

Electron rich material is labelled n-type, and hole rich material is labelled p-type. If MOSFET devices are fabricated on these types of materials they are labelled nMOS and pMOS respectively. *Complementary-metal-oxide-semiconductor* (CMOS) technology requires that the performances of nMOS and pMOS devices are similar. Within current IC design, this is accomplished by increasing the device geometry of the pMOS device due the difference in hole and electron mobility in bulk Ge material, with hole mobility (p-type) lagging behind. If the mobility of holes within Ge is increased then the pMOS device geometry can be decreased, thereby increasing device density on an IC.

Mobility can also be defined by the electronic charge (e), mean free time between scattering events (τ) and the effective mass of the carriers (m^*) by:

$$\mu = \frac{e\tau}{m^*}$$ **Equation 1.2**

Therefore, in addition to incorporation of a new material, mobility can be increased by either increasing the time between scattering events and/or decreasing the effective mass of the carriers. This can be accomplished if the material is *strained*. Therefore the research of Ge incorporation into the channel region has been geared toward a strained p-type channel (pMOS) [8]. It has been shown that hole mobilities in *compressively* strained Ge are similar to the mobility of electrons in relaxed Ge [9].

When a p-type material starts to conduct, the *valence band* is populated by holes and is responsible for the carrier flow along the channel. The valence band has a twofold degeneracy at the zone centre; the *heavy hole* (HH) and *light hole* (LH) sub-bands, shown in Figure 1.2a). During carrier conduction, inter-valley carrier scattering can occur where holes can transfer between the LH and HH bands [10].

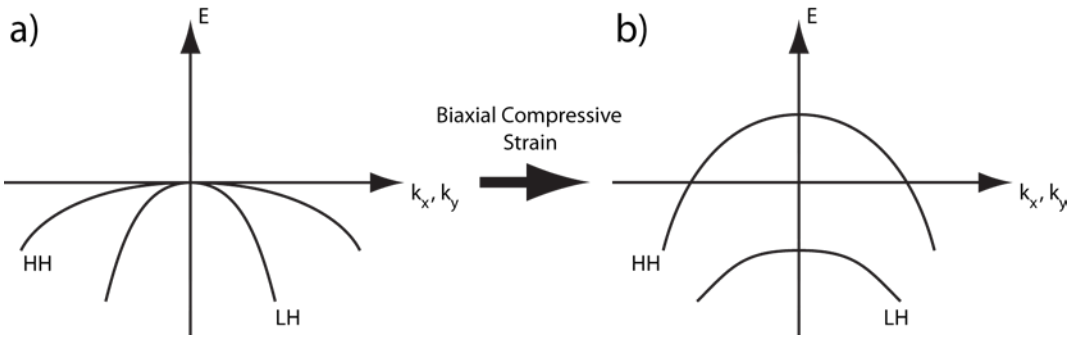

Figure 1.2: The heavy hole (HH) and light hole (LH) valence bands in a) bulk germanium and b) compressively strained germanium.

Section 1.3 introduces *virtual substrates* (VS) as global strain inducing platforms. Only SiGe virtual substrates are studied in this thesis, therefore a Ge layer can only ever be under *biaxial compressive* strain (Section 2.4). Only the effect of *compressive* strain on the valence band structure is briefly explained.

The effect of applying a compressive strain on the valence band decreases the *hole* energy of the HH band and increases the hole energy of the LH band (Figure 1.2b)) thereby mainly populating the HH band and reducing the inter-valley scattering [2]. This *increases* the mean free time between scattering effects. An additional effect of strain is that the curvature of the bands are changed by constraining the HH band and broadening the LH band (Figure 1.2b)), which indicates a reduction in effective mass [2]. Both of these effects increase the mobility of the material. For a further explanation of strain on the band structure see Paul [2].

1.3 Inducing Strain

The two main techniques to induce strain in the channel region of a MOSFET device are: production induced *local strain* and platform induced *global strain* [11]. The problems with local strain are outlined in Section 2.6. Due the limitations with local strain, a technique to impart global strain over the wafer is increasingly attractive. The most common approach to a global strain inducing technique is a *relaxed strain buffer* (RSB) [12] which is also called a *virtual substrate* (VS).

Virtual substrates [13] are a method of growing a high quality *relaxed* composition of SiGe on a Si wafer. A tuneable surface lattice parameter can be achieved by varying the final layer Ge composition. Once this relaxed material is grown, a

desired channel material can be *biaxially* strained by simply growing a *thin* layer on top, below that of the *critical thickness* [14]. The critical thickness of the strained layer is the thickness at which the layer begins to relax; this is explained in depth in Section 2.4.6.

A thick strained Ge layer is required without the early onset of relaxation. This requires a higher content ($x > 0.7$) $Si_{1-x}Ge_x$ virtual substrate due to the critical thickness (Section 2.4.6) of the strained layer.

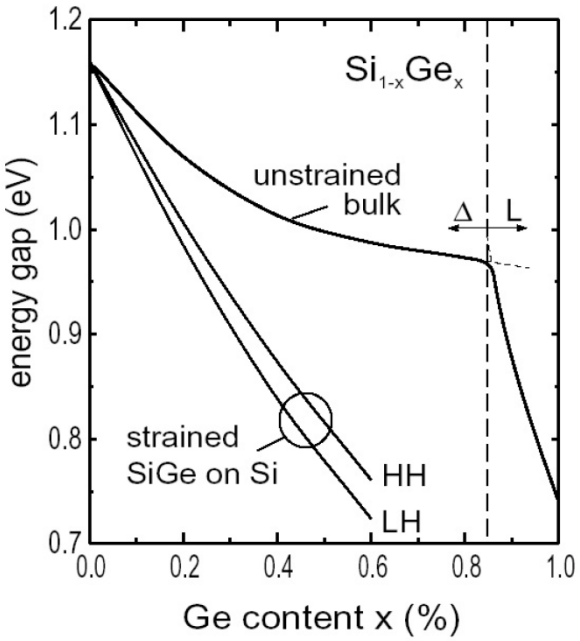

Figure 1.3: The bandgap dependence of $Si_{1-x}Ge_x$ alloys on the Ge content (x) of the alloy. Taken from Paul [2].

The bandgap dependence of SiGe alloys is shown with respect to Ge composition [15] in Figure 1.3. It is seen that for Ge compositions of $x > 0.84$ the bandgap of $Si_{1-x}Ge_x$ alloys become more like Ge than Si and severely decreases with composition towards the bandgap of pure Ge (0.66 eV). Therefore if the final composition of the

virtual substrate is kept below $x = 0.84$ a two-dimensional hole gas [9] can be achieved in the strained Ge layer which will prevent thermal carrier diffusion into the virtual substrate layer.

From these constraints, a trade-off is found where a virtual substrate of final composition $0.7 \leq x \leq 0.84$ is required. If a p-type strained Ge channel is to be grown on a global strain relaxed buffer the ideal composition of the buffer is thought to be $x = 0.8$ by the author and will be aimed for in this investigation.

1.4 Incorporation of Optoelectronic Materials

Virtual substrates also allow the incorporation of III-V semiconductor materials on a Si wafer [2]. Figure 1.4 shows the variation of the bandgap of III-V materials with their lattice parameter and the associated emission wavelength. The green lines shown between compounds are the variation of the bandgap as alloys are created of the compounds shown.

Light emitting diodes (LEDs) are the most basic optoelectronic device. The materials and alloys of certain compounds which are used in optoelectronic applications are seen with wavelengths (λ_{LED}) from $0.38\ \mu m \leq \lambda_{LED} \leq 0.75\ \mu m$. It is shown that AlAs, GaAs, AlP and GaP are lattice matched with SiGe alloys. In simple terms this allows LEDs made of these materials to be fabricated on Si substrates which have applications within the optoelectronic industry. Recently [16], there has been a great drive for the incorporation of optical receivers and modulators, so that a “system on chip” (SOC) can be fabricated on a Si wafer which will greatly enhance IC technology progress.

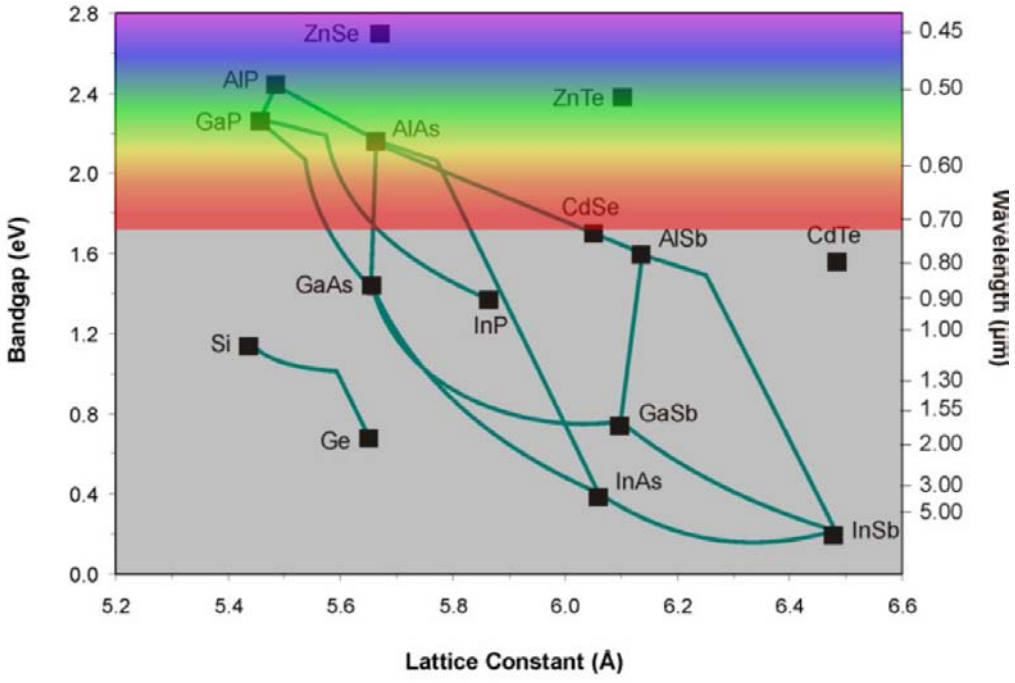

Figure 1.4: A graph of various semiconductors' bandgaps and their lattice parameters. Adapted from Veeco[17].

1.5 Scope of Work

This thesis is a general investigation of an adaptation to reverse graded buffers [18] to fabricate high quality, high composition ($x > 0.75$), $Si_{1-x}Ge_x$ virtual substrates. Unlike conventional virtual substrates the proposed structures relax under tensile strain, which provides both enhancements and extra difficulties. The relaxation mechanism of the technique is studied in detail and compared to other buffers to discuss their suitability to be used as a lattice tuneable platform. All buffers were grown by chemical vapour deposition (CVD) by an ASM Epsilon 2000 reduced pressure CVD (RP-CVD) at the University of Warwick.

1.5.1 Chapter Summaries

Chapter 2: Consists of the theoretical aspects of the work presented, which will be built up from first principles. The chapter will then go on to explain the growth method chosen and the growth mechanics required to grow the buffers. Dislocation dynamics are explained, which are the conventional relaxation mechanism for most SiGe strain relaxed buffers. Next any additional theory required to understand the effects seen through observational techniques for reverse graded buffers will be explained. Finally, a literature review of the most reported strain relaxed buffer fabrication techniques will be performed which will be summarised in a table to compare the critical values of all techniques.

Chapter 3: All the experimental techniques used in this study are explained along with any relevant theory on how to interpret the data received. The microscopy techniques used are: transmission electron microscopy (TEM), atomic force microscopy (AFM), differential interference contrast (DIC) microscopy and optical microscopy. x-ray diffraction (XRD) is used to determine the composition and relaxation of the buffers, selective wet chemical etching is used as a quick technique to characterise the dislocation density in the buffers. Lastly, SIMS is used to determine the compositional profiles of the wafers.

Chapter 4: The intended structures are outlined and reasons for certain methodologies will be given. The characteristics of the grown buffers will then be listed and each parameter of interest will then be measured and reported in turn. The parameters which are to be discussed are: compositional profiles of the buffer, relaxation and composition of the top layer, defect densities observed and the final

surface roughnesses incurred. One major detriment to buffer quality which is to be examined is cracking; additionally a solution will be suggested. The relaxation mechanism will be discussed and will be compared to previous models for conventional methods of buffer fabrication. The overall parameters of quality will then be compared to the other buffer techniques which were critiqued in *Chapter 2*.

Chapter 5: The solution to cracking proposed in Chapter 4 will be explored by thinning the underlying layer and the cap layer. Firstly, the underlayer thicknesses will be varied and the quality is to be reported. Secondly, with an optimal underlayer and graded region, the top layer thickness is to be reduced and the quality of the buffer is to be examined. From these two sub-experiments two “optimal” reverse graded buffers will be designed, grown and characterised. From the knowledge gained about the underlying layer, further discussion will be made about the contribution of buffer quality from the graded layer. Lastly, the method to reduce cracking of the top layer will be confirmed and commented on.

Chapter 6: Discussions and conclusions of the whole study are to be made.

Chapter 7: References used are listed.

2 Theoretical Discussion

In this chapter the theory of all aspects of reverse grading will be described and explained from basic principles. Material properties of silicon and germanium are described alongside the theory of epitaxy. After the basics are covered the role of dislocations and their interaction and associations within materials are accounted for. All theoretical quirks of reverse grading are then covered in detail and finally a literature review of other buffer fabrication techniques is then drawn.

2.1 Basic Properties of Silicon Germanium

A crystal structure is where atoms are bonded and positioned in a regular periodic arrangement which is referred to as a crystal lattice. Silicon (Si) and Germanium (Ge) both have a face centred diamond cubic crystal structure (Figure 2.1). This lattice structure is composed of two face centred cubic (fcc) structures which have a *displacement* of a quarter of the diagonal of the cubic unit cell *along* the diagonal. Each atom in the crystal lattice is covalently bonded to four neighbouring atoms. This lattice has cubic symmetry when relaxed and tetragonal symmetry when strained along the <100> directions.

The parameter *a* which is shown within Figure 2.1 is termed the lattice parameter which is the distance between unit cells in a crystal structure. The lattice parameter of silicon (a_{Si}) has a value of 5.431 Å and for germanium (a_{Ge}) is 5.658 Å [19]. This shows that Ge has a lattice constant which is 4.17 % larger than that of Si.

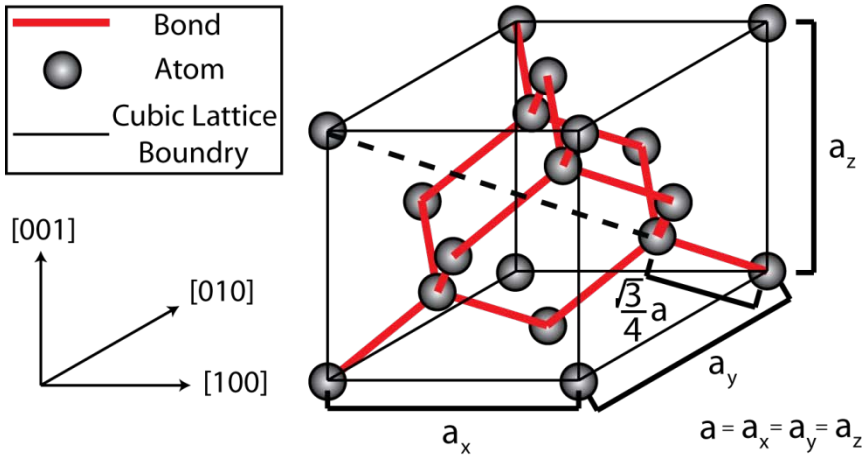

Figure 2.1: A schematic of a face centred diamond cubic crystal. The quantity *a* is defined as the lattice parameter.

When Ge is intermixed with Si to make $Si_{1-x}Ge_x$ alloys the order of atoms which occupy lattice sites is random, and any stated compositions (x for $Si_{1-x}Ge_x$) are an *average composition* of a macroscopic view. The lattice parameter of any relaxed $Si_{1-x}Ge_x$ alloy can be determined by the Kasper-corrected-Vergard's law:

$$a_{Si_{1-x}Ge_x} = a_{Si}(1-x) + a_{Ge}x + 0.02733x^2 - 0.02733x \qquad \textbf{Equation 2.1}$$

Vergard's law is a linear interpolation between a_{Si} and a_{Ge} [20], however, for the SiGe system this was empirically corrected by Kasper [21] for discrepancies encountered when experimentally measuring the lattice parameters at room temperatures. The variations with other temperatures are described in Section 2.5.4.

2.1.1 Other Parameters of Si, Ge and SiGe alloys

Table 2.1 shows properties of Si, Ge and $Si_{1-x}Ge_x$ alloys which are used in this study. All values and expressions were gathered by Schäffler and are taken directly from his

article in "Properties of Advanced Semiconductor Materials" [19]. Note that in several cases the variation with alloy composition (*x)* is non-linear.

	Silicon (Si)	Germanium (Ge)	Si(1-x)Ge(x) Alloy
Lattice Constant (Å)	5.431	5.658	Equation 2.1
Energy Band Gap (eV)	1.12	0.66	Figure 1.3
Mobility ($cm^2 V^{-1} s^{-1}$)			
Electrons	1450	3900	
Holes	450	1900	
Elastic Moduli			
C_{11} (GPa)	165.8	128.5	165.8-37.3x
C_{12} (GPa)	63.9	48.3	63.9-15.6x
C_{44} (GPa)	79.6	66.8	79.6-12.8x
Bulk Modulus	98	75	98-23x
Poisson Ratio ((100) Orientation)	0.28	0.26	0.28-0.02x
Melting Point (°C)	1412	937	$1412-738x+263x^2$ (solidus)
			$1412-80x-395x^2$ (liquidus)
Linear Thermal Expansion (K^{-1})	2.6E-06	5.9E-06	$(2.6+2.55x)x10^{-6}$ (x<0.85)
			$(7.53x-0.89)\ x10^{-6}$ (x>0.85)

Table 2.1: Properties of relaxed Si, Ge and SiGe alloys at 300 K which are relevant to this study and its applications. [19]

2.2 Epitaxial Growth Techniques

Epitaxial growth is the process where the growth of a crystal material occurs on the crystal face of another material so that the crystalline lattices of both materials have the same structure and orientation [22]. When transistors were first conceived they were constructed of polycrystalline materials but have now advanced to single crystal

structures. [23] It has been shown that single crystal materials have higher carrier mobility than polycrystalline structures [24].

There are two main types of growth processes used to grow epitaxial layers, molecular beam epitaxy (MBE) and chemical vapour deposition (CVD). Both processes deposit material on the crystalline substrate in different ways. Within MBE the material is deposited on the surface of the substrate through an atomic or molecular beam. Each parameter of growth (e.g. temperature, growth rate, etc.) can be varied independently during MBE growth, therefore the effect of changing one parameter can solely be investigated, which makes it a powerful research tool.

CVD growth occurs through localised chemistry when the substrate is heated and a *precursor* gas is passed over the surface. Each growth parameter within CVD is dependent on each other, and the localised chemistry allows fast growth rates. The CVD system allows a fast throughput of wafers due to fast growth rate of Si and a good uniformity of structures. These qualities make CVD the favoured growth method for industry and it is the method of growth for this study.

2.2.1 Reduced Pressure Chemical Vapour Deposition (RP-CVD)

There are many different types of CVD systems which allow different variations in growth temperature (from 100°C to 1300°C) and also allow a variation in growth chamber pressures (from ntorr to atmosphere). An ASM Epsilon 2000 reduced pressure CVD (RP-CVD) is used to fabricate layers which are investigated in this study. A schematic of a generic RP-CVD growth chamber is shown in Figure 2.2.

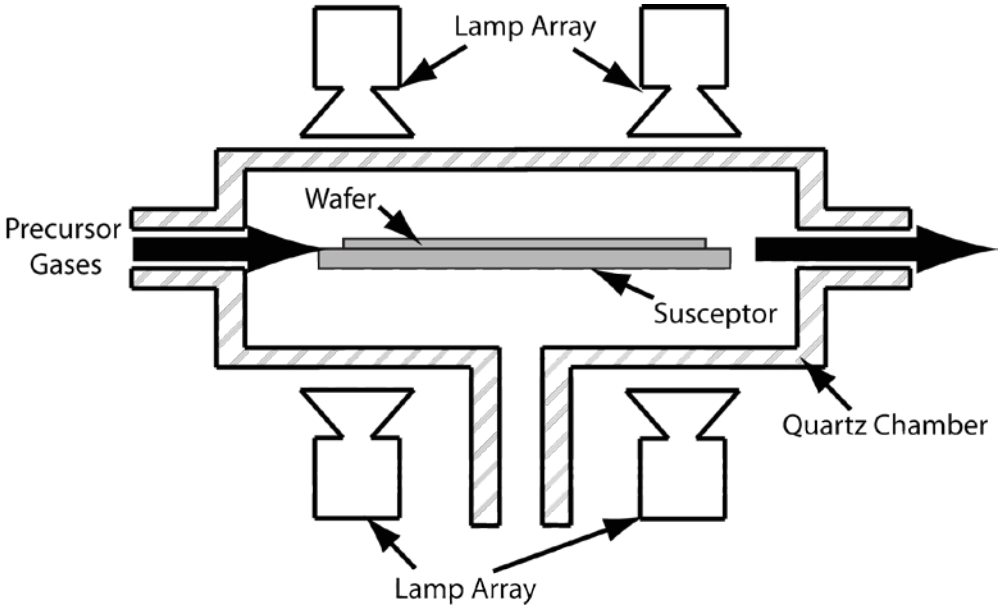

Figure 2.2: A simple schematic representation of a generic CVD chamber.

In RP-CVD the growth rate and composition of material produced are both very sensitive to substrate temperature and precursor gas flow rate, so these both have to be controlled accurately and consistently over the period of growth. During growth the wafer is heated by infra-red radiation which is generated by the lamp array shown, Figure 2.2, then passed through the infra-red transparent quartz growth chamber. Substrate temperature is controlled by thermocouples below the wafer which control the output power of the lamp array.

2.2.2 Substrate Surface Preparation

High quality Si (001) substrates were used with a root mean squared (RMS) surface roughnesses of approximately 0.1 nm. A thin (~1 nm) native silicon dioxide layer is unavoidably formed on the surface of the Si substrate prior to being placed within the CVD system. Additionally, organic or metal contaminants could be present on the surface if wafers are handled incorrectly. Two methods are generally used to remove

the oxide and contaminants; *ex-situ* wet chemical cleaning and/or high temperature oxide desorption. All wafers used in this study are handled in a clean room and are at no point exposed to other environments prior to growth therefore are deemed only to have native oxide on the surface. An *in-situ* bake of 1150°C is used to desorb any surface oxide. After desorbtion the surface is left with a hydrogen passivated surface. The wafer is then ready for growth.

2.2.3 Precursors

Precursors are defined as compounds that participate in chemical reactions which produce other compounds. These compounds are introduced into the CVD chamber in a gaseous state. Gas flow rates are measured in standard cubic centimetres per minute (sccm) and standard litres per minute (slm). The precursors used for this study are germane (GeH_4) for Ge deposition and dichlorosilane (SiH_2Cl_2) for Si deposition. When gases are introduced into the chamber a number of chemical reactions can take place. These are demonstrated by Equation 2.2 and Equation 2.3 [25] which show the chemical processes of GeH_4 as it interacts with the surface of the Si (001) wafer:

$$GeH_4(g) + 2* \rightarrow H_2(g) + 2H* + Ge(b)* + 2(b) \qquad \textbf{Equation 2.2}$$

$$2H* + 2(b) \leftrightarrow H_2(g) + 2* \qquad \textbf{Equation 2.3}$$

* represents a free surface site and X* represents a chemical species which is bonded to a surface site, see Figure 2.3. (g) represents a gaseous state and (b) represents a solid bulk lattice atom. These equations are taken from Hierlemann *et al* [25], who

have modelled the deposition process as a dehydrogenation of the germane molecule which is then added to the surface. Generally, when a precursor breaks down into its *stable* compounds it cannot revert to its previous state. When the dehydrogenated molecule is added to the surface the remaining two hydrogen atoms will then act as surfactant molecules, covering the surface to prevent dimer bond formation during the growth. The process is then left with an interchangeable reaction where the two surfactant hydrogen atoms can then be desorbed to form a hydrogen molecule to leave two free surface sites or vice versa. These reactions are shown pictorially in Figure 2.3.

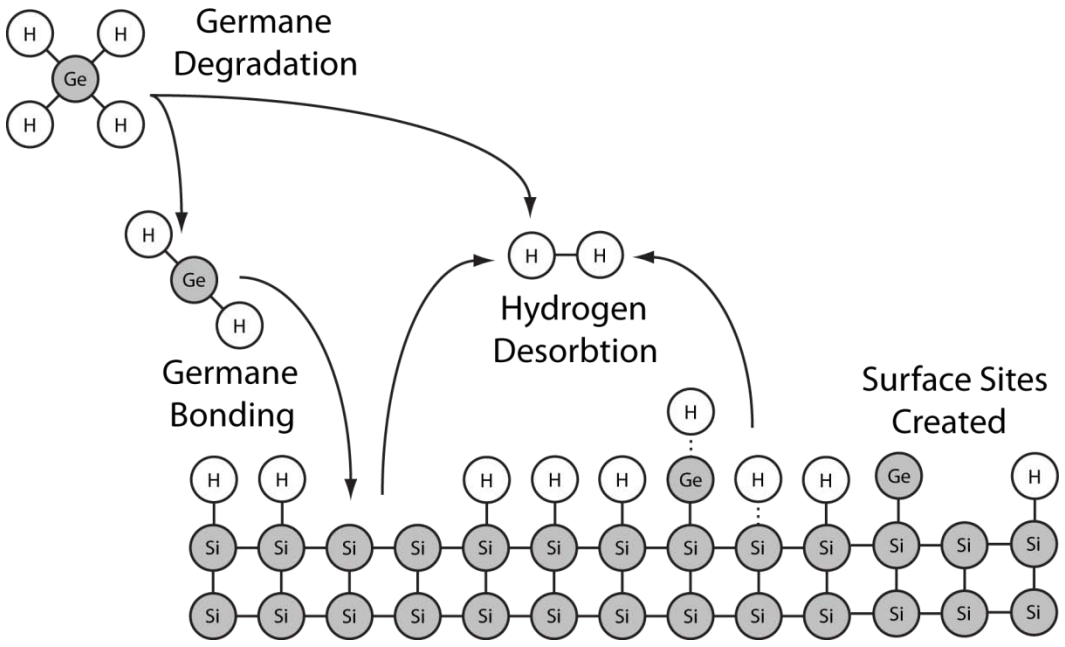

Figure 2.3: A diagram showing the different stages of precursor deposition of germane on a Si (001) substrate during epitaxy.

Similar reactions take place when SiH_2Cl_2 is introduced to a Si (001) substrate surface. These are shown in Equation 2.4 to Equation 2.7, where Equation 2.4 is the irreversible breakdown of the precursor gas. Equation 2.5, Equation 2.6 and Equation 2.7 show the reversible reactions which produce more gaseous compounds than

GeH_4. See Hierlemann et al [25] for the more complicated reactions when both GeH_4 and SiH_2Cl_2 precursors are mixed for growth of SiGe alloys.

$$SiH_2Cl_2(g) + 4* \rightarrow 2H* + 2Cl* + Si(b)* + 4(b) \quad \textbf{Equation 2.4}$$

$$2H* + 2(b) \leftrightarrow H_2(g) + 2* \quad \textbf{Equation 2.5}$$

$$Cl* + H* + 2(b) \leftrightarrow HCl(g) + 2* \quad \textbf{Equation 2.6}$$

$$2Cl* + Si(b)* + 2(b) \leftrightarrow SiCl_2(g) + 2* \quad \textbf{Equation 2.7}$$

The growth rate of precursors generally have two regimes; if the temperature is relatively low then it is dependent on the temperature applied (temperature limited). However, when the temperature is relatively high the growth rate is limited by the ratio of precursor gas flow (mass-flow limited). This is shown in Figure 2.4 by the comparative SiH_2Cl_2 and GeH_4 growth rate graphs. SiH_2Cl_2 has a transition temperature of approximately 960°C and GeH_4 of about 400°C. When SiH_2Cl_2 and GeH_4 are mixed an average growth rate trend is observed, with a different transition temperature. See Hartmann et al [26] for growth rate information for a mixture of SiH_2Cl_2 and GeH_4.

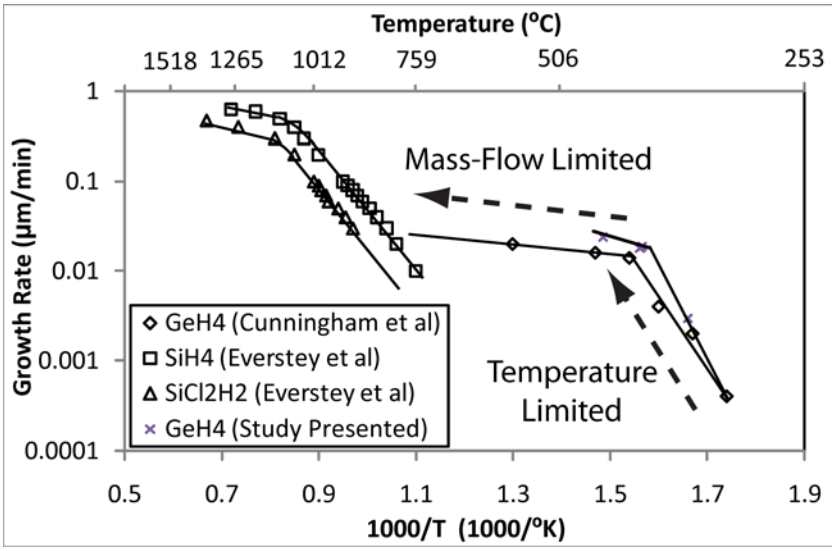

Figure 2.4: Growth rates as a function of temperature when compared to work performed on SiH_4 (silane, Everstey [27]), SiH_2Cl_2 (Everstey [27]) and GeH_4 (Cunningham [28]). Work done by Cunningham *et al* was performed within an *ultra high vacuum CVD*.

HCl gas is one of the gaseous compounds which are created by SiH_2Cl_2. Hartmann et al [29] show that an addition of HCl gas to the GeH_4 and SiH_2Cl_2 mixture decreases the growth rate when grown under low temperatures. Therefore the temperature of growth must be kept high (> 700°C) to avoid this detrimental effect.

2.2.4 Chamber Etching

Section 4.2 outlines the growth parameters used in this study. Due to the high GeH_4 flow and the relatively high growth temperatures SiGe deposition on the quartz wall of the CVD chamber occurs. Increasing the wall deposition decreases the amount of IR radiation reaching the substrate which results in a lower growth-temperature. The delay of the temperature control system and the deposition on the side of the chamber alters the growth kinetics by lowering the applied growth temperature for a small period of time. This results in lowering the growth rate and therefore the Ge composition of the layers. In addition, flaking of the chamber deposition can add

contamination during growth [30]. Most importantly, the difference in thermal expansion between a *thick* layer of chamber deposition and quartz chamber can crack the chamber itself [31]. The solution to these problems is a regular etching of the growth chamber deposition during the growth process itself, whilst taking care *not* to etch the wafer. To keep wall deposition within acceptable thicknesses (~1 µm) a HCl etch step was instigated during the growth of layers. This was performed either between constant composition layers and the graded region, or at every 1 µm of growth on the substrate. Etching of the chamber was performed by cooling the substrate to 400°C, and removing it from the growth chamber. The chamber was kept under a H_2 ambient atmosphere then exposed to an HCl etch. This continual etching of the chamber during growth provides a thermal cycle to the wafer. This thermal cycle is thought to induce an extra thermal strain(Section 2.5.4) and with the addition of contaminants during growth may produce cracking (Section 2.5.5) of the epitaxial layer.

2.3 Growth Kinetics of Silicon-Germanium

The growth process is defined as an exchange of molecules from a vapour phase and adsorbed surface molecules. The surface molecules are then subject to surface diffusion until incorporated within a substrate lattice site. The kinetics of the growth process determines the quality of epitaxial layer and how layers are formed.

2.3.1 Adatom Transport

Regardless of growth method, when mobile atoms/molecules are deposited on the surface they are known as adatoms. A diagram of adatom sites and defects which

outline adatom transport is shown in Figure 2.5. The temperature applied to the substrate allows the adatoms to travel on the epitaxial surface until they are chemisorbed into a lattice site or defect. The distance travelled an adatom until incorporation is defined as the migration length (of the order μm) which is dependent on many factors during growth. The most important of these factors is the chemical species of adatom and the substrate temperature. The migration length of Ge adatoms is greater than that of Si as the bond strength of Ge atoms is lower than Si. An increase in substrate temperature increases the transport energy of the adatoms. This increase in transport energy allows the adatom to overcome the energy barriers between adjacent surface sites which in turn increases the migration length.

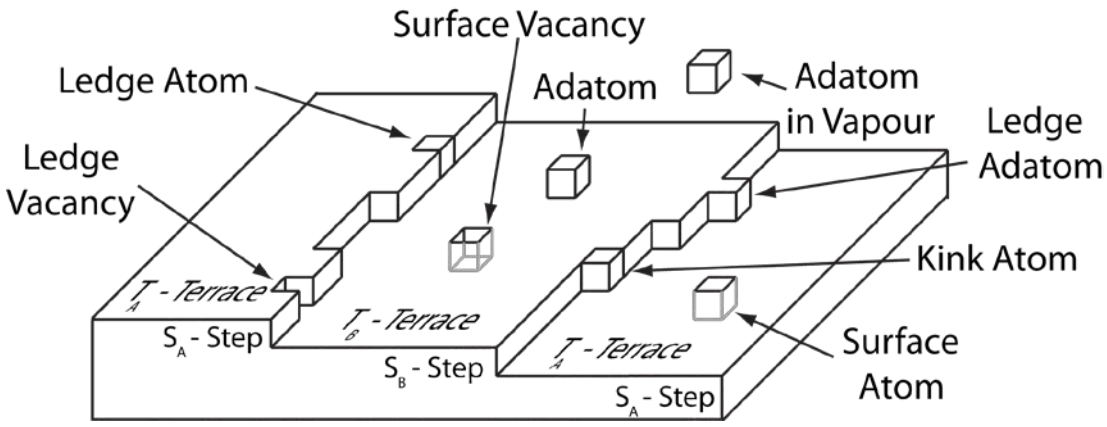

Figure 2.5: Diagram of typical adatom sites and defects which outline adatom transport. Taken from Hudson [32].

The surface of the Si substrates used in this study, and generally by industry, are composed of atomic terraces as depicted in Figure 2.5. Dangling bonds can form a temporary *dimer* bond with each other on the surface if adatoms and *surfactants* are not present. A terrace with dimerisation parallel to its edge is denoted as type A, with step S_A and the terrace above it denoted T_A. In contrast a terrace with bond dimerisation perpendicular to its edge is denoted as type B, with step S_B and terrace

T_B. The surface potential well created by either step is a preferential incorporation site for adatoms due to the extra bonds available. When an adatom incorporates itself to this step vacancy site it is termed a ledge adatom (Figure 2.5). Other sites for adatom incorporation are (from most preferential to least) bulk vacancy, surface vacancy, ledge vacancy, kink vacancy and step vacancy. Adatoms become atoms when their transport energy is not great enough to free them from an incorporated site which has a deeper potential well than the surrounding site. Two dimensional epitaxial growth typically occurs by an extension of the terraces if the adatom migration length is greater than the terrace width. The Si (001) substrates used in this study have a typical substrate off-cut of < 1° which characterises the angle at which the terrace steps are aligned. For more information about adatom transport see Hudson [32].

2.3.2 Growth Modes

Homoepitaxial growth is where the material deposited is of the same species as the substrate and heteroepitaxial growth is where the chemical species are different. In a homoepitaxial system there is no mismatch between the lattice constants of the deposited material and the substrate, therefore no strain is induced. To minimise the total surface free energy, homoepitaxial growth occurs in a 2-D Frank van der Merwe [33] growth mode by extension of the terraces (Figure 2.6) to minimise the surface area grown.

An adatom can travel along the surface of the substrate and not be incorporated into a step vacancy if the average migration length is less than the terrace width. Adatom migration is limited if adatoms; encounter any other vacancies, do not have enough

thermal energy or if a high mismatch strain between the deposited chemical species and the substrate is present (Section 2.4). Without sufficient energy to travel to the step vacancy adatoms are incorporated onto the surface forming their own local potential wells. Other adatoms can in turn by trapped by these wells and become another incorporation site for the majority of mobile adatoms. This mechanism is the starting point for the formation of 3-D islands. In the case of heteroepitaxial growth where the material deposited is not the same at the substrate (i.e. Ge on Si), a highly strained mismatch can result in Volmer-Weber growth [34] (Figure 2.6). This is where adatoms cluster to form islands as it is energetically favourable for them to chemisorb onto their own species rather than incorporate into the lattice step vacancies. The surface undulations are also a mechanism of strain relief which occurs as a variation of lattice parameters along the surface (Section 2.4.1).

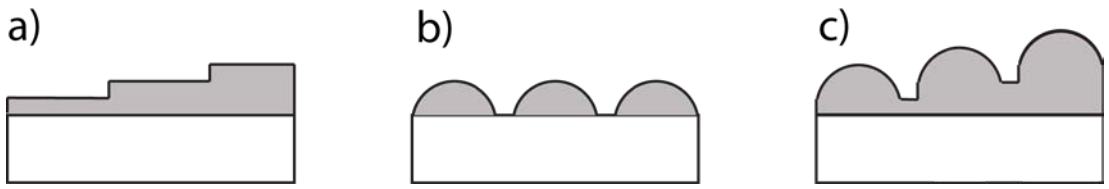

Figure 2.6: Schematic representation of the tree different epitaxial growth modes with are achievable; a) Frank van-der Merwe, b) Volmer-Weber and c) Stranski-Krastanov.

If the material strain is high, but not enough so to induce Volmer-Weber growth, the growth mode will occur in a Frank-van der Merwe mode of growth until the accumulated strain energy is high enough to induce a Volmer-Weber growth mode. This is termed the Stranski-Krastanov growth mode [35] and occurs if no other relaxation mechanism has enough energy to take place. This 2-D to 3-D growth mode transition can be suppressed if the adatom migration length is increased to

allow adatoms to reach the lowest possible energy states, possibly by increasing the thermal budget applied.

In general, 2-D Frank van der Merwe epitaxial growth occurs unless a high strain coupled with a low growth time or low growth temperature is used where 3-D islands are able to form [36].

2.4 Relaxation and Dislocations

Strain is induced in a layer if it is epitaxially deposited and has a lattice parameter different to that of the substrate. Each layer by layer growth of a strained material forces the deposited monolayer of adatoms to arrange themselves to the *in-plane* lattice parameter (a_x) of the underlying layer (Figure 2.7).

The misfit or bulk mismatch between the layers is characterised by the ratio (*f*) of *unstrained* lattice parameters of the layer ($a_{layer(bulk)}$), and the substrate ($a_{substrate}$):

$$f = \frac{a_{substrate} - a_{layer(bulk)}}{a_{substrate}} \qquad \textbf{Equation 2.8}$$

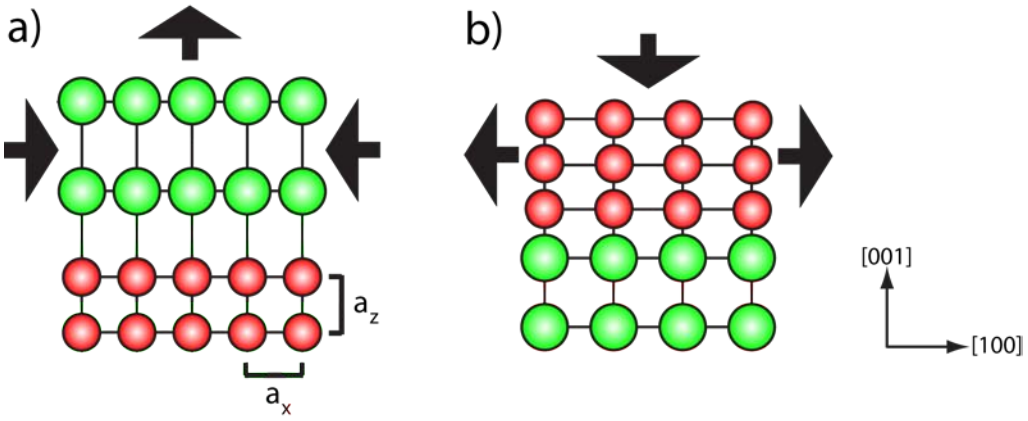

Figure 2.7: Diagram showing the tetragonal distortion of a cubic lattice and the resultant effect on the lateral and vertical lattice parameters under a) compressive and b) tensile strain. Adapted from Parsons [37].

The mismatch between a pure Ge layer and a Si substrate is f = -0.0417, using the lattice parameters defined in Table 2.1. As SiGe alloys are randomly organized the strain induced is assumed to be *bi-axial* with no preference in either the [100] or [010] directions. Therefore the in-plane lattice parameters a_x and a_y are considered to be equal. If the layer is under any magnitude of strain the out-of-plane lattice parameter will be tetragonally distorted when compared to the in-plane lattice parameter (Figure 2.7). This relationship is described by the elastic modulii C_{11} and C_{12} (Table 2.1):

$$a_z = a_{bulk} + \frac{2C_{11}}{C_{12}}(a_{bulk} - a_x) \qquad \textbf{Equation 2.9}$$

Where a_z is the out-of-plane lattice parameter in the <001> direction, a_{bulk} is the lattice parameter of the unstrained material and a_x is the in-plane lattice parameter in either the <100> or the <010> direction. This expression can also be described by the Poisson's ratio (v) which describes the ratio of the strain applied to the strain induced in the perpendicular direction.

As the thickness of the misfit layer increases, the strain energy stored within the layer also increases. Strain within the layer with respect to the substrate is defined as:

$$\varepsilon = f(1-R) = \frac{a_{layer} - a_{layer(bulk)}}{a_{substrate}} \qquad \textbf{Equation 2.10}$$

Where ε is the strain, R is the relaxation and a_{layer} is the in-plane lattice parameter (a_x or a_y) of the epitaxial layer. When $a_{layer} > a_{layer(bulk)}$, ε is positive and the layer in question is under tensile strain, if ε is negative the layer is under compressive strain. This therefore means that relaxation of the layer is defined as:

$$R = \frac{a_{substrate} - a_{layer}}{a_{substrate} - a_{layer(bulk)}} \qquad \textbf{Equation 2.11}$$

When a layer has an R value over 100% it means that the layer is over-relaxed, and if $a_{substrate} < a_{layer(bulk)}$ it indicates that the layer is under tensile strain, if $a_{substrate} > a_{layer(bulk)}$ the layer it is under compressive strain.

The growth process usually occurs under a 2-D Frank van der Merwe mode and the resulting crystalline lattice is of high quality. Therefore the relaxation process of mismatched fcc materials can occur through two main mechanisms: surface roughening and dislocation dynamics.

2.4.1 Surface Roughening

Thermodynamical equilibrium is defined as the point where no thermal, mechanical or chemical processes take place in a system. It is achieved in a material when the total free energy of the system is kept at a minimum.

The total free energy of a mismatched system is the sum of the strain energy stored within the layers added to the surface free energy of its interfaces and surfaces. A single mismatched layer on a smooth substrate is considered. The type of strain within the layer defines its sign; a compressive strained layer is defined as having a *negative* potential energy. Therefore the formation of surface undulations can *increase* the surface free energy, returning the total free energy of the system towards equilibrium. Tensile strained layers have positive strain energy and the formation of undulations will not minimise the free energy of the system (Section 2.5.1).

Undulation formation indicates a change of growth mode into a Stranski-Krastanov 3-D mode, which consists of cusps and mounds. At the top of these mounds the lattice constant is increased indicating increased local relaxation. This is counter balanced by the decreased lattice constant at the cusps. However, due to the ratio of cusp profile length to mound profile length the *overall difference in lattice parameters* show a relaxation of compressive strained layers. The roughening mechanism is thermodynamic in nature and induced only if excessive thermal energy is applied to overcome the kinetic barriers of surface reconstruction. Therefore when layers are under tensile strain (rather than compressive) higher growth temperatures can be used and surface roughening is avoided. This dual approach to reducing roughening will be used in the current work.

2.4.2 Defects

Material quality is of the utmost importance when designing virtual substrates and the presence of defects can severely reduce the performance of transistors which are fabricated on them. Discontinuities within the crystal lattice can be zero-, one-, two- and three-dimensional. Zero-dimensional defects are typically vacancies or interstitials and three-dimensional defects are volumes of the crystal which do not fit to make a regular structure, such as polycrystalline layers, voids or large precipitates. When the layer is grown epitaxially these defects do not occur. A one-dimensional defect is typically a dislocation which is formed as a strain relieving mechanism. An example of a two-dimensional defect is a stacking fault (Section 2.5.2) which also relieves strain and only occurs under tensile strain relaxation.

2.4.3 Dislocations and Burgers Vectors

The following description is only for the dislocation processes for face centred cubic (001) orientated layers. The strain energy stored within pseudomorphic layers increases as the thickness of the layer is increased. A dislocation is a row of broken covalent bonds and will only form when the energy stored within the layer is greater than the energy required to break those bonds and create a one dimensional plastic deformation in the lattice. An example of the deformation which occurs is shown in Figure 2.8 for a tensile strained layer.

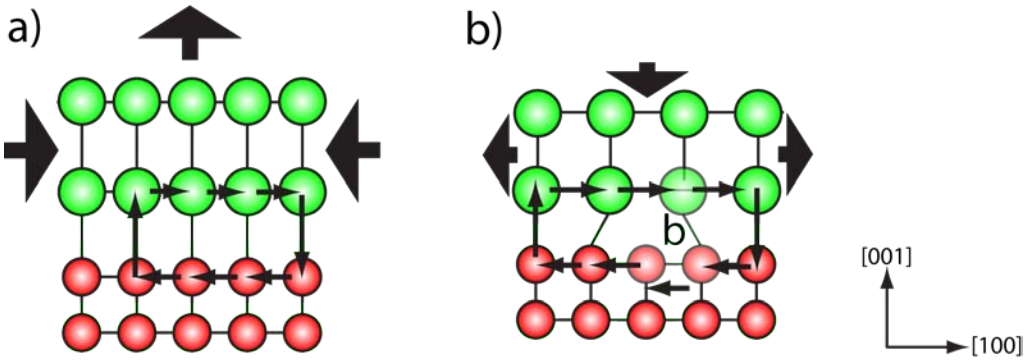

Figure 2.8: An example of plastic relaxation from a) a tensile strained layer to b) relaxation via formation of a perfect edge dislocation. The direction of the dislocation is shown to be going into the page. The Burgers vector, b, is shown as the extra displacement needed to create a complete circuit around the dislocation when equal amounts of bonds in opposite directions are taken into account.

The Burgers vector of a dislocation is the magnitude and direction of the distortion of the crystal lattice caused by the deformation. The Burgers vector can be determined by first creating a closed loop circuit following the bonds around an area prior to dislocation formation, as shown in Figure 2.8a). Secondly, if the same circuit is made around an area with a single dislocation it will not close and the remaining displacement is defined as the Burgers vector, as shown in Figure 2.8b). If the Burgers vector is perpendicular to the dislocation line direction it is termed an *edge* dislocation, and if it is parallel to the line direction it is termed a *screw* dislocation. Any other angle of the Burgers vector defines the dislocation as a *mixed* dislocation.

The Burgers vector for typical dislocations in a SiGe system is $b_{60} = \frac{a}{2} < 011 >$ which forms an angle of 60° with a line direction of <110> as shown in Figure 2.9. Hence dislocations in a SiGe system are normally mixed dislocations. The main reason for the typical formation of 60° dislocations is that the closest packed atomic *direction* is the <011> direction. The Burger vectors of the other dislocations type

which can form in a SiGe system is $b_{edge} = \frac{a}{2} < 1 - 10 >$ for a pure edge dislocation, however these are less common as they require higher energies to form, see Phillips [38] for a greater explanation.

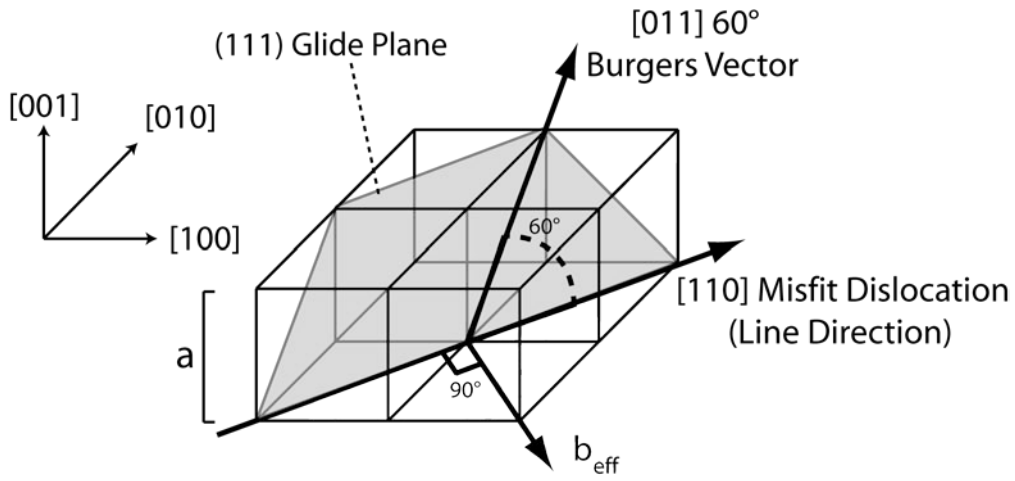

Figure 2.9: A schematic of the 60° dislocation Burgers vector direction. Also shown is b_{eff}, the effective Burgers vector which participates in strain relaxation. Adapted from Nash [39]

Dislocations are the boundaries of a slipped plane and generally comprise of two components; *misfit* dislocations and *threading* dislocations (Figure 2.10). Slip allows a row of atoms to move past each other and usually occurs on the closest packed plane as it has the lowest energy barrier to motion, the *Peierls* energy barrier [38]. In a face centred cubic diamond crystal structure the set of slip planes is the {111} family. Dislocations are widely referred to as single lines to make simple analytical models easier to understand; however, there is a danger of over simplification and the reader is referred to Figure 2.10 to understand the orientation of the row of broken bonds in a face centred cubic diamond system.

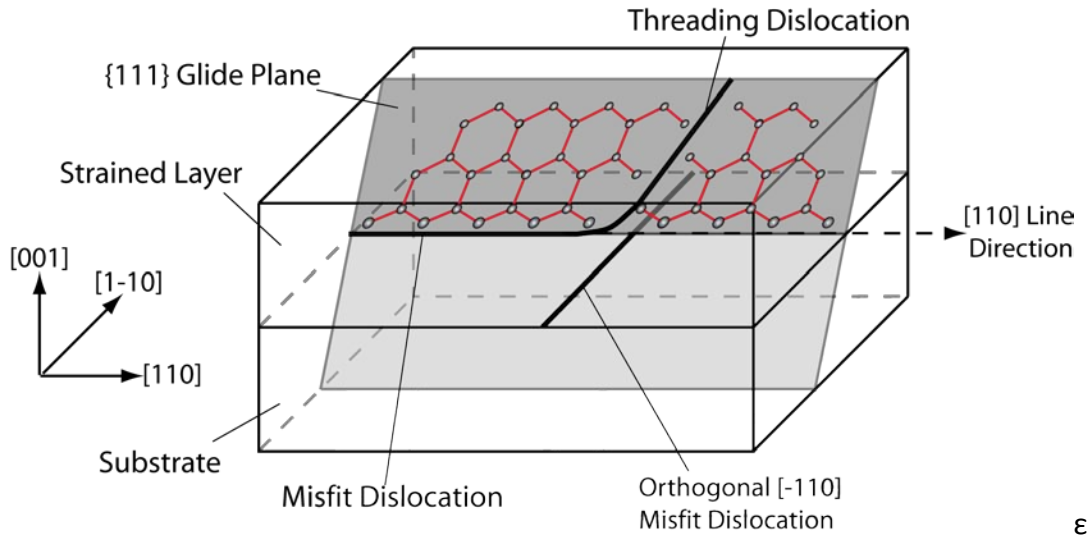

Figure 2.10: A physical representation of the threading and misfit dislocations as the boundary of a slipped plane which shows the order of bonds which are broken. Adapted from Parsons [37].

The dislocation segment which forms at the interface between mismatched layers to relieve the strain is the misfit dislocation. The direction of the misfit dislocations is in the <110> direction due to the formation on the (001) plane and the intersection with the {111} slip plane. Each misfit dislocation which is formed partially relieves the strain in the layer by the deformation it induces. However, only the component of the deformation which is on the (001) plane and perpendicular to the line direction of the dislocation contributes any effective relaxation (Figure 2.9). This component is named the *effective Burgers vector*, b_{eff}, and its magnitude is calculated through the dot product equation:

$$b_{eff} = \frac{b \bullet \underrightarrow{b_{dir}}}{\left\| \underrightarrow{b_{dir}} \right\|} \qquad \textbf{Equation 2.12}$$

Where b is the Burgers vector of the dislocation and b_{dir} is the vector perpendicular to the line direction of the dislocation.

If the composition of a layer is known and the dislocation line density is found for dislocations along line directions of <110> for a (001) orientated system then the relaxation of the layer can be calculated. The relaxation caused by dislocations on the (001) plane is calculated by:

$$R_{<110>} = \frac{\rho_{<110>} b_{eff}}{f} \qquad \textbf{Equation 2.13}$$

Where $R_{<110>}$ is the relaxation of the layer, $\rho_{<110>}$ is the line density of dislocations running in the <110> direction per unit area of the (001) plane, b_{eff} is the effective Burger's vector for the dislocations running in the <110> directions and f is the maximum misfit as defined in Equation 2.8.

As dislocations are boundaries they cannot simply terminate within the lattice, termination only occurs if dislocations are in a closed loop or if they terminate at a free surface (such as another defect or the epitaxial surface). The arms of the misfit dislocations that terminate at a free surface are called threading dislocations and due to their geometry do not relieve much of the strain. Threading dislocations do not lie at the (001) strain interface and have vectors with the components in the [001] direction, this allows them to terminate at the epitaxial surface. When threading dislocations are present at the growth surface the lattice continuum is preserved by adatom incorporation around the threading dislocations preserving and extending them into the epitaxially grown layers. The threading dislocation density (TDD) is an

important measure of the quality of an epitaxial layer. TDD is the density of threading arms which reach the surface of a layer is usually quoted in cm^{-2}.

2.4.4 Dislocation Motion

Dislocations can propagate through two mechanisms: *climb* or *glide*. Glide of dislocations is usually the preferred mechanism of motion as it only requires the local rearrangement of the dangling bonds. Glide only occurs when there is a presence of both strain *and* thermal energy. The rearrangement occurs around the dislocation in a motion which is parallel to the Burgers vector [38]. It is a process whereby the dangling bonds of the slipped plane (within the threading dislocation) attach onto the neighbouring column of atoms to remove them from the neighbouring unslipped plane (Figure 2.11). This action is seen to allow the threading dislocation to glide and extend the misfit dislocation thereby increasing the associated relaxation of the layer. The *glide plane* of a dislocation is any plane which contains both the line direction and the Burgers vector of the dislocation. This is also the slip plane in a face centred cubic diamond system, which as described previously are the {111} planes. Therefore there are only four possible glide planes in which 60° dislocations are able to glide.

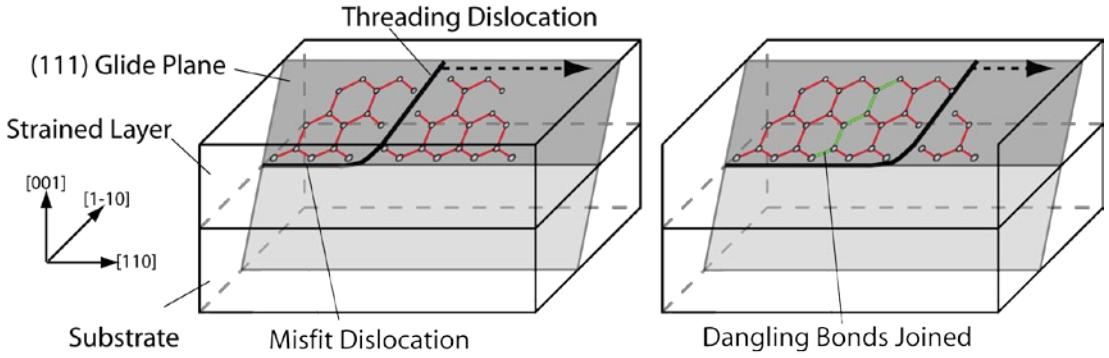

Figure 2.11: A diagram of the plane of the closest packed atoms showing the threading dislocation glide through the strained layer and the associated extension of the misfit dislocation.

Regardless of which glide plane a dislocation is in, the glide velocity of a dislocation is thermally activated and related to the mismatch strain through [19]:

$$v_{glide} = B\varepsilon \exp\left(-\frac{E_{glide}}{kT}\right) \qquad \textbf{Equation 2.14}$$

Where v_{glide} is the glide velocity, B is a constant related to the initial velocity, ε is the strain, k is Boltzmann's constant, T is the temperature applied and E_{glide} is the glide activation energy which has been determined empirically by Tuppen and Gibbings [40]:

$$E_{glide} = (2.16 - 0.7x)\ \text{eV} \qquad \textbf{Equation 2.15}$$

It was also mentioned previously that 90° edge dislocations can form within the system (Section 2.4.3); however, the dangling bonds of this dislocation are perpendicular to the Burgers vector. Propagation of the edge dislocation therefore can only occur through *climb* which involves mass transport of atoms around the

dislocation in a motion perpendicular to the Burgers vector. The mass transport involves processes such as interstitial-vacancy generation and diffusion [38]. Both of these processes require higher temperatures than glide and are only possible if the glide of dislocations is blocked. Therefore the generation and glide of 60° dislocations are the preferred method of strain relaxation in a SiGe system.

2.4.5 Nucleation of Dislocations

If no threading dislocations are initially present in a strained layer, relaxation through glide can only happen if dislocations are generated, or *nucleated*. The TDD values of high quality Si substrates, which are used in this study, are to the order of 10^{-2} cm^{-2}, whereas it has been suggested that a TDD of $10^{7} – 10^{11}$ cm^{-2} is required [41] to relax high composition (x>0.7) $Si_{1-x}Ge_x$ layers. Nucleation can occur homogeneously, heterogeneously and through multiplication, with the growth conditions and the material properties determining which mechanism(s) nucleate dislocations.

Homogeneous nucleation is usually in the form of dislocation half loop formation from a point source on the surface of the wafer; this mechanism is described in detail in Section 2.4.6. This mechanism also requires high activation energies of approximately 40 eV [42] which is achieved either through a relatively high growth temperature or by a high mismatch strain of $f \sim 0.02$. Due to the high activation energy required [43] this type of nucleation only occurs if other relaxation mechanisms do not relax the layer and strain energy is accumulated within the layer.

Heterogeneous nucleation occurs when another type of defect is present within the layer and that defect is used as a free surface on which further dislocations can

nucleate. This mechanism is still not well understood due to the many sources which can induce the heterogeneous nucleation of half loop dislocations. These nucleation sources have been suggested to be precipitates or voids within the layer [36] or/and point defects which arise from contaminants within the growth chamber. An indirect source of heterogeneous nucleation is when excessive surface roughness is incurred during growth [44]. Generally, if the epitaxial layer is highly crystalline heterogeneous nucleation does not take place.

Dislocation multiplication occurs by the interaction of dislocations already present in the layer to produce even more dislocations and so enhance relaxation. Many multiplication mechanisms have been summarised by Vdovin [45], however the modified Frank-Read (MFR) mechanism [46] proposed by LeGoues is the most widely accepted multiplication process. An in-depth explanation of the mechanism is explained in Section 2.4.8. The strain energy required within a layer to induce multiplication is approximately 4 eV [47] which is only twice that of the activation energy for the glide of dislocations (~ 2 eV).

2.4.6 Critical Thickness and Dislocation Energetics

The critical thickness of a strained layer is usually thought of as being the maximum thickness for which it remains fully strained, but it is also useful to think of it as the minimum thickness required to generate misfit dislocations that initiate the relaxation process. A simple constant composition layer on a mismatched substrate is considered. When a pseudomorphic layer is epitaxially deposited on a relaxed substrate it has an associated areal energy density (E_h) at the misfit interface which is given by:

$$E_h \approx 2G\left(\frac{1+\nu}{1-\nu}\right)h\varepsilon^2 \qquad \textbf{Equation 2.16}$$

Where G is the bulk shear modulus, ν is Poisson's ratio, h is the thickness of the pseudomorphic layer and ε is the strain in the layer. Two models have been widely reported at either ends of the energy spectrum required to generate misfit dislocations, the Matthews-Blakeslee model and the People-Bean model.

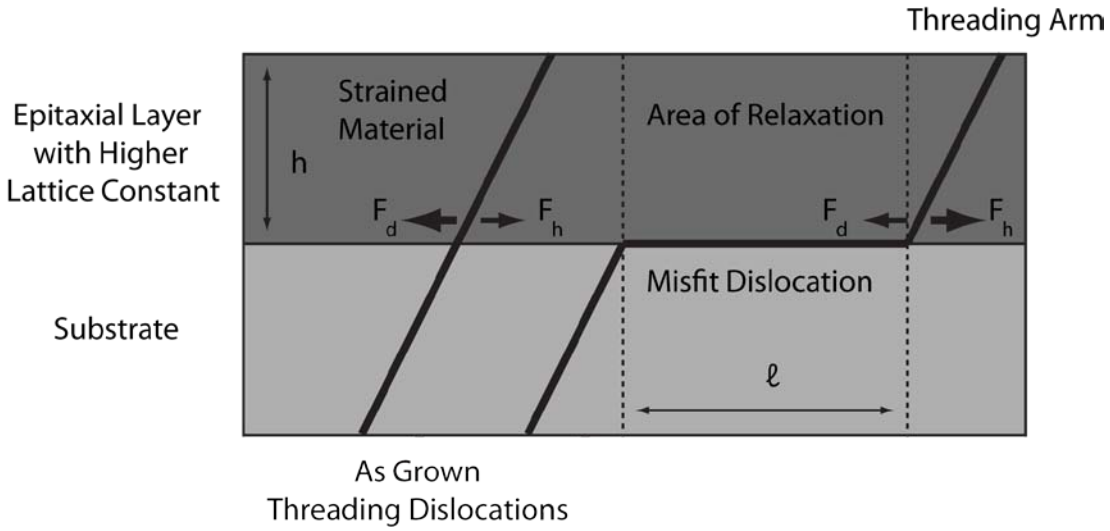

Figure 2.12: The Matthews-Blakeslee model for the generation of misfit dislocations. Shown are the forces acting on a threading dislocation arm. Adapted from People and Bean [14]

Historically, Si substrates were of much lower quality when epitaxial techniques were first introduced and the number of pre-existing threading dislocations was significantly high. Therefore, Matthews and Blakeslee [14] reported a critical thickness model where a misfit dislocation is generated when a pre-existing threading dislocation glides at the mismatch interface.

Figure 2.12 shows the forces acting on a threading dislocations which has been "grown into" the strained layer for the Matthews and Blakeslee model which considers the mechanical *force equilibrium* of the system. The force labelled F_h is the driving force applied on the dislocation from the strained layer and can be derived from Equation 2.16:

$$F_h \approx 2G\left(\frac{1+\nu}{1-\nu}\right)bh\varepsilon \qquad \textbf{Equation 2.17}$$

Where b is the Burgers vector and h is the thickness of the layer. The resistance to dislocation motion is termed the Peierls barrier [38], the effective drag force. This represents the force F_d required to displace material from an unslipped plane and allow the glide of the threading dislocation arm:

$$F_d \approx \frac{Gb^2(1-\nu\cos^2\theta)}{4\pi(1-\nu)}\ln\left(\frac{h}{b}\right) \qquad \textbf{Equation 2.18}$$

θ is the angle between the Burgers vector and the dislocation line direction. When the force on the dislocation is equal to the drag force of the material threading dislocations are able to glide at the strain interface to create misfit dislocations, hence starting relaxation of the layer. Therefore, when $F_d = F_h$ the thickness of the layer (h) becomes h_c, the critical thickness, combining Equation 2.17 and Equation 2.18 creates:

$$h_c \approx \frac{b(1-\nu\cos^2\theta)}{8\pi(1+\nu)\varepsilon}\ln\left(\frac{h_c}{b}\right) \qquad \textbf{Equation 2.19}$$

When Si substrates became much higher in quality the number of pre-existing threading dislocations decreased. This resulted in the increase of critical thicknesses of SiGe layers which deviates from the Matthews-Blakeslee critical thickness. People and Bean [14] then proposed a critical thickness model where the system is relaxed when a misfit dislocation evolves from the homogeneous nucleation of a dislocation half loop from a point source, requiring no pre-existing threading dislocations.

The *homogeneous* nucleation of dislocations from point sources requires much higher energies with magnitudes of approximately 40 eV being reported. Equation 2.15 states that the energy for activation of glide within a system is about 2 eV assuming that there are a significant number of threading dislocations grown into the material. The model proposed by People and Bean considers the *energy* required to nucleate dislocations from point sources in initially dislocation free layers.

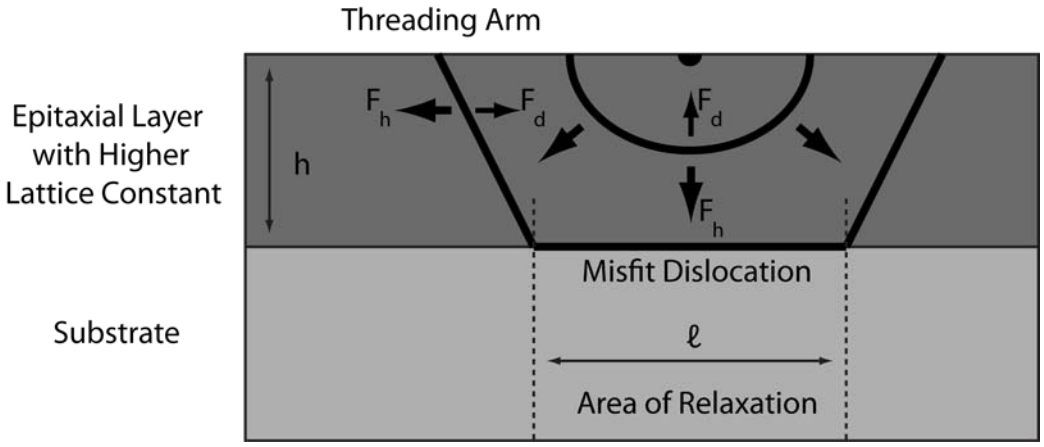

Figure 2.13: The model proposed by People and Bean to nucleate dislocation half loops in a dislocation free mismatched material system. Taken from People and Bean [14].

Figure 2.13 shows the model proposed by People and Bean. As mentioned in Section 2.4.3 a dislocation must terminate at a free surface, therefore it must also *nucleate* at a free surface. When the strain within a layer increases to nucleate dislocations in a high quality epitaxial layer they form as dislocation half loops on the {111} glide plane. The forces on the half loop are subject to the same forces as described by the Matthews-Blakeslee model; tension and drag. Assuming the strain energy within the layer is still of a magnitude to induce glide, the half loop will expand until it reaches the misfit interface. When it reaches the interface a misfit dislocation segment forms with threading arms at both ends which can then glide and increase the misfit dislocation length. The areal energy density required for the nucleation of a single dislocation half loop is:

$$E_d \approx \left(\frac{Gb^2}{8\pi\sqrt{2}a}\right)\ln\left(\frac{h}{b}\right) \qquad \textbf{Equation 2.20}$$

a is the relaxed lattice constant of the strained layer. When the areal energy density of the strain within the layer (Equation 2.16) is equated to the areal energy density required to nucleate a dislocation (Equation 2.20) so that $E_h = E_d$ the People-Bean critical thickness (h_c) is given:

$$h_c \approx \left(\frac{1-\nu}{1+\nu}\right)\left(\frac{b^2}{16\pi\sqrt{2}a\varepsilon^2}\right)\ln\left(\frac{h_c}{b}\right) \qquad \textbf{Equation 2.21}$$

The Matthews-Blakeslee and the People-Bean critical thicknesses are calculated in Figure 2.14 for a strained Ge layer on a relaxed $Si_{1-x}Ge_x$ layer or a strained $Si_{1-x}Ge_x$ layer on a relaxed Ge layer. The negative values of misfit strain indicate a

compressive strain for the Ge layer on SiGe substrate case; however, the absolute misfit values can be used for the SiGe layer on Ge substrate situation, where the layer is under tensile strain. The constant values used were $b = 4\text{Å}$ for a pure Ge layer and $\theta = 60°$. The values used which varied with Ge composition were *a* which is defined in Equation 2.1; *f* defined in Equation 2.8 and *v* defined in Table 2.1.

Figure 2.14 shows three theoretically calculated regions where the critical thickness of a strained Ge on a $Si_{1-x}Ge_x$ relaxed layer is determined. The region below the Matthews-Blakeslee curve shows the material properties which lack sufficient force for threading dislocations to glide and form misfit dislocations. This region is considered stable as thermal treatment is not likely to encourage significant relaxation. The region labelled the metastable region is where the growth temperature for these layers is critical to the relaxation induced, with lower temperature growth suppressing the relaxation of these layers. The region above the People-bean curve shows layers which nucleate dislocations by half loop generation and even with low temperature growth are likely to relax.

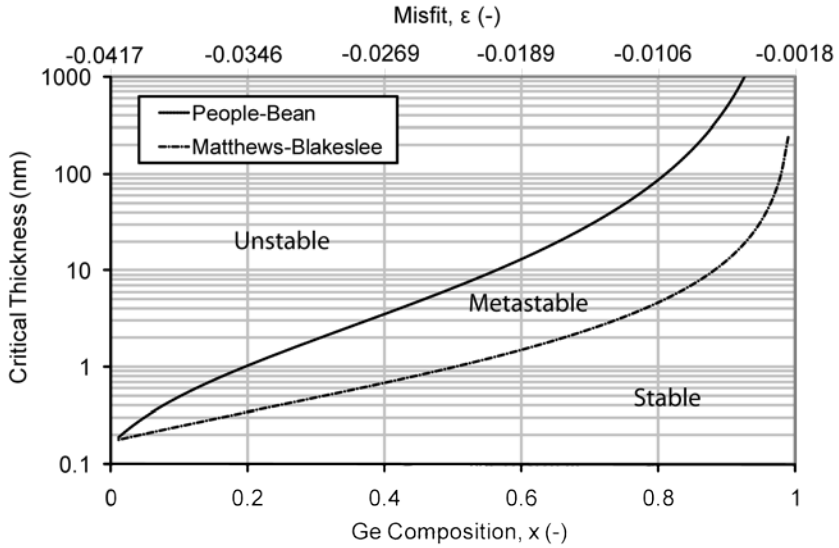

Figure 2.14: The calculated critical thicknesses from the People-Bean and Matthews-Blakeslee criterion for SiGe layers grown on a relaxed Ge layer.

Many investigations have been performed on the relation of strained *Si* on various $Si_{1-x}Ge_x$ buffers for different SiGe compositions, x. However, few sources report the relaxation of strained Ge on high (x>0.7) $Si_{1-x}Ge_x$ buffers. Therefore empirical evidence cannot be compared to the theoretically generated metastable regime for strained Ge.

2.4.7 Interactions Between Dislocations

When dislocations are allowed to glide freely it is highly probable that interactions between threading dislocations and misfit dislocations will occur. All surface undulations and dislocations have an associated radial strain field, as depicted by Figure 2.15. The strain field arises from the local distortion of the bonds around the defect [48], or from surface undulations. Threading arm segments can interact with either the strain field or the underlying orthogonal misfit dislocation, depending on the growth conditions and the driving strain force.

The strain field from either relaxation mechanism is thought to add a retarding force to the motion of dislocations. Dislocation pinning can occur when the threading arm of a dislocation encounters a dislocation strain field or a large surface undulation (>15 nm) [49]. When the strain within a layer is insufficient to overcome the retardation from the strain field all orthogonal threading dislocations can be pinned against the strain field [50] and are within a *blocking regime*. This pinning action will then result in the pile up [51] of threading dislocations alongside the strain field.

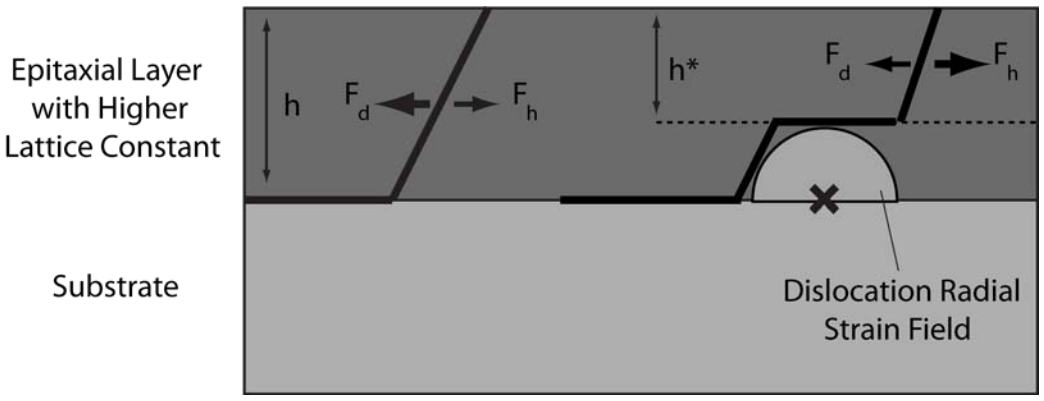

Figure 2.15: The interaction of a threading dislocation with the strain field of another orthogonal misfit dislocation. Splitting of the threading arm can occur and the effective channel for glide is then reduced. Taken from Parsons [37].

As the driving strain force is increased the interaction outcome depends on the orientation of the relative Burgers vectors of the threading and misfit dislocations. The retardation force of the strain fields is thought to be at a maximum when the Burgers vectors are perpendicular and at a minimum when they are parallel. At high strains the dislocations with perpendicular Burgers vectors allow the reading arm to glide in a reduced glide channel [50] of height h^* (Figure 2.15). The radius of the strain fields and therefore the reduced glide channel height are dependant on the macroscopic strain which is related to the thickness of the layer. The shortened

threading arm will have a reduced glide velocity due to the reduced driving force of the thinner glide channel.

When the Burgers vectors are parallel and the driving force is large enough, a threading dislocation can cause an orthogonal misfit dislocation to split on the (001) plane and connect with the threading arm. This creates two dislocation corners, where a corner is two misfit segments on the (001) plane which are 90° to each other. The two outcomes of this interaction are dependent on the gliding direction of the threading dislocation. Simplistically, if the threading dislocation *direction* is normal to the glide plane of the orthogonal misfit dislocation, then corner formation and the subsequent glide of the threading arm will occur. However, if the approaching threading dislocation is orientated so that it is parallel to the glide plane of the misfit dislocation it will be pinned by the intersection of both glide planes [50]. It has been found that the energy required to unpin any dislocation after forming a corner is more than that of unpinning a dislocation which has been pinned purely by interactions with a radial strain field.

When threading dislocation arms with anti-parallel Burgers vectors which are on the same glide plane head toward each other they can join together to *annihilate.* Annihilation of two threading arms simply connects two misfit dislocations together and removes the threading arm segments as they effectively terminate on each other and are regarded as free surfaces. When the TDD is high ($>10^8$ cm^{-2}) the probability of annihilation is high and is the main source of TDD reduction. When TDD is low ($<10^5$ cm^{-2}) the main TDD reducing mechanism is glide of threading dislocations

until they reach a free surface and the dislocation glides out of the system leaving behind a perfect 60° misfit dislocation.

2.4.8 The Modified Frank-Read (MFR) Multiplication Mechanism

The Frank-Read (FR) mechanism [46] is a process whereby a pinned misfit dislocation under an excessive strain can be unpinned by bowing into the substrate to turn the misfit dislocation into a dislocation half loop. Further half loops can then be generated by this method until the layer is fully relaxed.

The modified Frank-Read (MFR) nucleation mechanism was proposed by LeGoues *et al* [46] and is shown schematically step by step in Figure 2.16. The mechanism involves two misfit dislocations which have formed two corner misfit dislocations (Section 2.4.7) and lie on orthogonal glide planes. The two corner misfit dislocations have a mutual repulsion. This repulsion forces the corner to bow into the substrate as both corners have parallel Burgers vectors, Figure 2.16a). Both misfit dislocations are locked to the vector of glide plane intersection as they cannot simply terminate within the lattice. As the dislocation corner is warped it will adopt the motion of a dislocation loop, Figure 2.16 b).

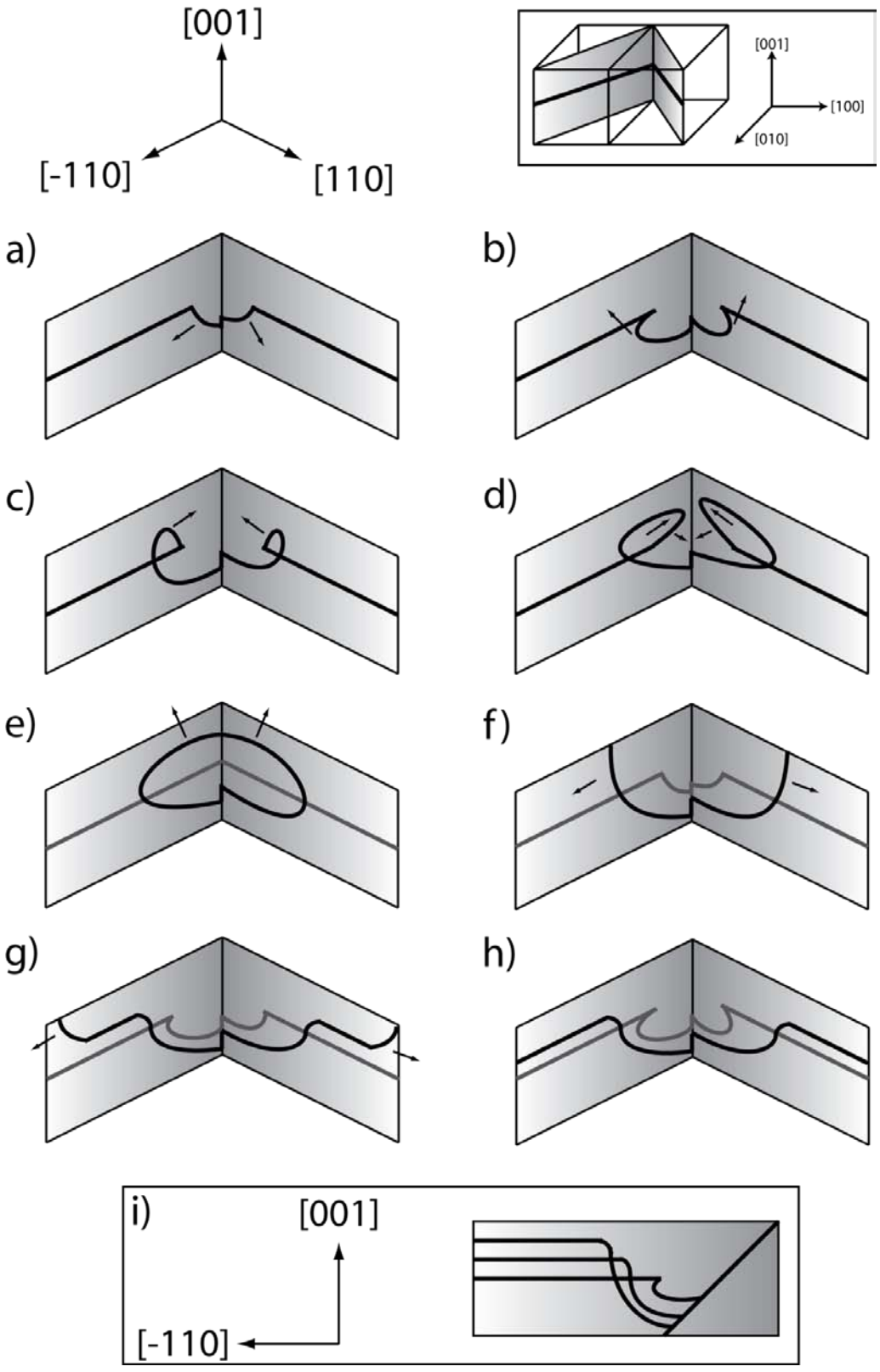

Figure 2.16: A schematic representation of the modified Frank-Read (MFR) dislocation multiplication mechanism process. Two misfit dislocations which have formed a corner are pushed into the substrate and each misfit dislocation moves on different glide planes. A they are pushed further into the substrate they then form a dislocation loop which then in turn creates a misfit dislocation with threading arms. i) shows the characteristic <110> profile of the MFR mechanism. Adapted from Capewell [52]

The warped segments of the dislocations will then loop back in the [001] direction above the misfit segments, Figure 2.16c). Further extension of these loops will then allow an annihilation of segments of both loops which run on the intersection of the glide planes, Figure 2.16d). This annihilation produces two dislocations: one complete dislocation loop and another corner dislocation, Figure 2.16e). The dislocation loop then expands on both glide planes until it reaches the epitaxial growth surface where the loop segments running on the (001) plane can terminate, Figure 2.16f). This leaves a dislocation half loop with a misfit segment and threading arms which can then glide away from the intersection, Figure 2.16g) and h).

This process can then be *duplicated* by both corner dislocations which remain at the site, if a repulsive force is still imparted on them. This process allows a rapid relaxation of a layer and only requires an activation energy of ~4 eV, much less than that of homogeneous nucleation. It exponentially increases the TDD within the layer but as they lie on the same glide plane annihilation tends to occur which reduces the TDD. The main problem with the MFR mechanism is that if pile-up of threading dislocations occurs on the same glide plane they will increase the local surface roughness. If this roughness is added to the surface undulation from the high density of local misfit dislocations at a MFR site a large surface step can be induced [49].

2.5 Relaxation of Reverse Graded Virtual Substrates

The relaxation of most conventional buffer fabrication techniques requires the epitaxial growth of a SiGe layer on a Si (001) substrate (Section 2.6). Therefore the relaxation of these layers occurs under compressive strain through dislocation dynamics. The proposed structure (Section 4.2) relaxes under *tensile* strain with a

significant number of "grown-in" threading dislocations. Within this section the potential enhancements and pitfalls of these features are discussed.

2.5.1 Tensile Strain Enhanced Smoothing

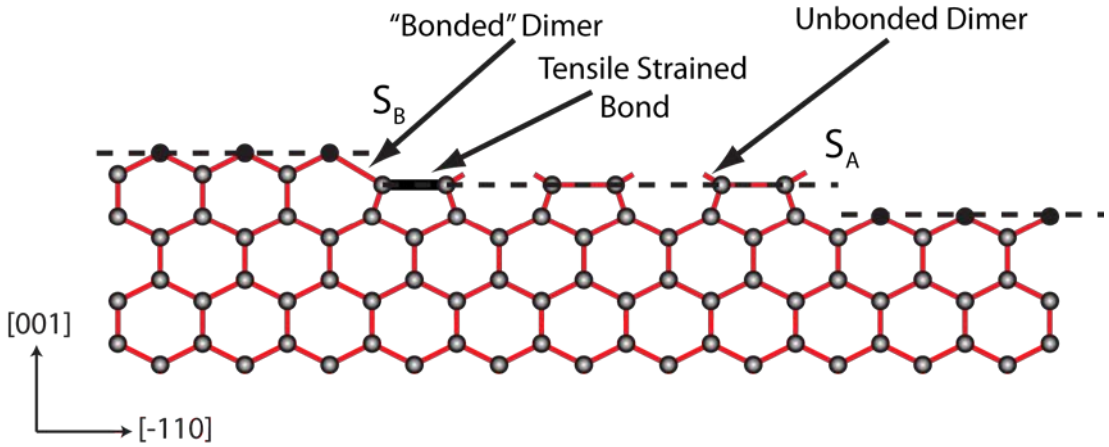

Figure 2.17: A schematic of the surface steps S_A and S_B on an *unstrained* (001) surface, the [110] direction is viewed. The dimer bonds which are perpendicular to the steps on the S_A terrace are shown as horizontal black lines. Dimer bonds parallel to the S_B terrace are shown as black dots. Taken from Xie [53].

Figure 2.17 shows a schematic of the terraces on the wafer surface which allow epitaxial growth on Si(001) wafers, a description of these terraces are given in Section 2.3.1. The step free energy is the *difference* between the surface free energy of a surface with, and without, a step. What is important to note is that in an *unstrained* epilayer the row of dimers next to the S_B step edge have a perpendicular "bonded" dimer. This dimer bond induces a tensile strain in the bond beside it; this is highlighted as a black line in Figure 2.17. This bond has a surface step energy of 44 meV per ledge atom. The S_A step energy is relatively small (<5 meV per ledge atom) when compared to the S_B step energy. It can be concluded that the S_B step energies are the limiting factor in the surface free energy of the epilayers.

The surface is now considered when strain is applied to the layer. The sign of stored strain energy is dependent on the type of strain induced, where compressive strain is defined with energies below zero. Surface undulations will only form as a relaxation mechanism to *increase* the surface area and therefore increase the surface free energy of the system to restore the system to equilibrium (Section 2.4.1).

The simulations of Xie *et al* [53] show that for a strain of *magnitude* $\varepsilon = 0.02$ the energy of the S_B step when the layer is under tensile strain was ~ 100meV per ledge atom and ~ *-150meV* per ledge atom when under compressive strain. Compressive strain further lowers the step free energy, therefore relaxation by surface roughening is promoted to increase the surface free energy and restore the system to equilibrium. Additionally, it shows that tensile strain increases the S_B step energy which implies that surface roughening will not occur as a relaxation mechanism, as it can only *increase* the surface free energy which would not restore the system to equilibrium. This effect is confirmed by experimental data reported by Xie *et al* [53] where SiGe pseudomorphic layers of different compositions were grown on smooth (> 1 nm) virtual substrates . The experimental results show that roughnesses greater than 2 nm were incurred for compressive strains larger than $\varepsilon = -0.014$. However, layer under tensile strain showed no signs of surface roughening, regardless of the magnitude of strain applied.

2.5.2 Partial Dislocations and Stacking Faults

It is stated in Section 2.4.3 that the most common dislocation within the SiGe system is a 60° type. The 60° dislocation is actually formed by two components; the 30° and 90° *Shockley partial dislocations* [38]. The Burgers vector for a 60° dislocation (b_{60})

is defined in Section 2.4.3 and the Burgers vector for the 90° and 30° partial dislocations are $b_{90} = \frac{a}{6} < -112 >$, and $b_{30} = \frac{a}{6} < 121 >$ respectively.

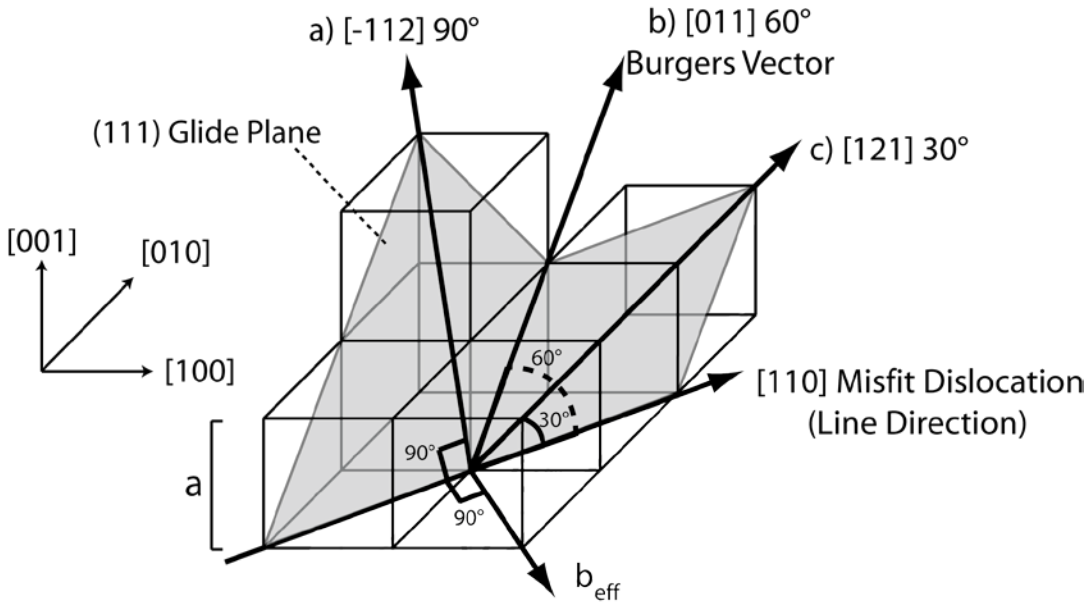

Figure 2.18: A schematic of the directions of the different dislocation Burgers vectors; a) 90°, b)60° and c) 30°. Also shown is b_{eff}, the effective Burgers vector which participates in strain relaxation. Adapted from Nash [39]

Figure 2.18 shows the orientation of the Burgers vectors of the partial dislocations. If a Burgers vector circuit of both the partial dislocations was performed a 60° dislocation Burgers vector would be found. Therefore the Burgers vector of a 60° dislocation is still conserved:

$$b_{60} \rightarrow b_{30} + b_{90}$$

$$\frac{a}{2}[011] \rightarrow \frac{a}{6}[121] + \frac{a}{6}[-112]$$

Equation 2.22

Both partials propagate on the {111} glide plane and the Peierls drag force associated with dislocation glide along the plane is directly proportional to b^2 by Equation 2.18.

The 60° dislocation glides by a two step process of its separate partials and it is seen that the resistance to motion is reduced [54]:

$$b_{60}{}^{2} > b_{90}{}^{2} + b_{30}{}^{2} \qquad \textbf{Equation 2.23}$$

Within *compressive* strained layers the 30° partial dislocation leads the 90° dislocation and vice versa for tensile strained layers; the 90° partial dislocation leads the 30° dislocation. In both cases the 90° partial experiences a lower Peierls barrier to motion as calculated by Equation 2.18 and therefore has a larger associated glide force.

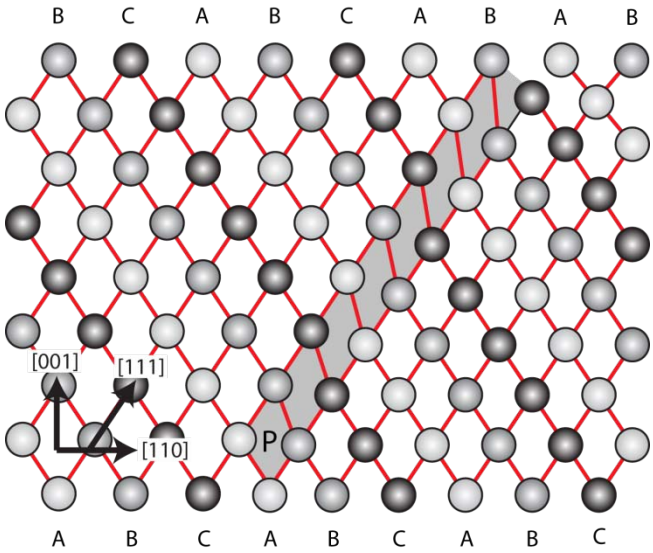

Figure 2.19: A schematic cross sectional view of a stacking fault which is seen as the shaded region. This is caused by one 90° partial dislocation at point P where the dislocation line direction is [1-10]. The 30° is not shown in the diagram and would be positioned off the page. Taken from Parsons [37].

The region in between the 30° and 90° components is called the *stacking fault* region. A stacking fault is a two dimensional defect which disrupts the stacking order of atomic planes. Figure 2.19 shows the disruption caused by a partial dislocation

running into the page in the [1-10] direction at point P. This generates a stacking fault region where the order of the planes goes from "ABCABCA**BCA**" to "ABCABCA**BAB**". The 30° partial would normally close this area but is not shown in Figure 2.19 to exaggerate the effect of a stacking fault.

In compressive strained layers the 90° partial cannot pass the 30°partial due to dislocation repulsion. Therefore due to the balance between partial dislocation repulsion and dislocation glide the stacking fault area has been found to have an equilibrium distance of 0.3-0.5 nm [55]. As a result the stacking fault area is normally ignored in *compressive* strained layers as both components are very close together and is regarded purely as a 60° dislocation.

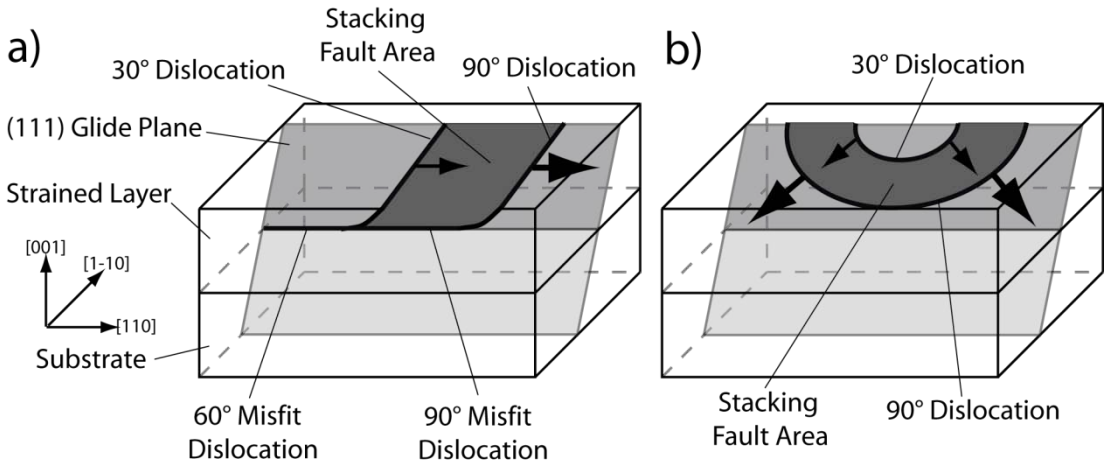

Figure 2.20: The formation of extended stacking faults and their features which are formed by a) glide and b) nucleation. Adapted from Marée [56]

In *tensile* strained layers the 90° dislocation leads the 30° dislocation and has a reduced drag force, therefore it is able to glide away from the 30° partial to *extend the stacking fault* area, this is shown schematically in Figure 2.20a). Stacking fault extension will only occur if the driving force from the strain within a layer (F_h) is

greater than the sum of the force required to form a stacking fault (F_{SF}) in addition to the Peierls drag force required to move the 90° leading arm (F_d). Therefore the point where extension will occur is $F_h = F_{SF} + F_d$, as postulated by Parsons [37]. F_{SF} is the force required to create a stacking fault and is defined by: $F_{SF} = h\gamma$ where h is the height of the layer and γ is the areal energy density for stacking fault formation. Using these expressions with Equation 2.17 and Equation 2.18 the critical thickness for stacking fault formation through glide is found:

$$h_c = \frac{Gb^2(1-v\cos^2\theta)}{4\pi[G(1+v)b\varepsilon - \gamma(1-v)]}\ln\left(\frac{h_c}{b}\right) \qquad \textbf{Equation 2.24}$$

Where θ is 90°, b is the Burgers vector for 90° dislocations and is γ is a value found by Hull [57] of 55-75 mJ m^{-2}. Figure 2.21 shows a comparison between the critical thicknesses for the creation of a stacking fault through glide and the Matthews-Blakeslee critical thickness. The region which is marked as stacking fault generation is where stacking faults will be preferentially generated to relax the layer, rather than the two step glide process of a 60° dislocation. This occurs during higher misfits as the force required to create the stacking fault is much smaller than those acting on the partial dislocations, and the reduced drag force on the 90° partial when compared to the 60° allows the 90° partial to glide faster.

As can be seen from Figure 2.20, the 90° partial dislocation is the bounding edge of the region and is therefore responsible for all relaxation induced by a stacking fault. The relaxation of the layer from stacking faults can be calculated from Equation 2.13

if the effective Burgers vector for a 90° partial dislocation is calculated from its Burgers vector by Equation 2.12.

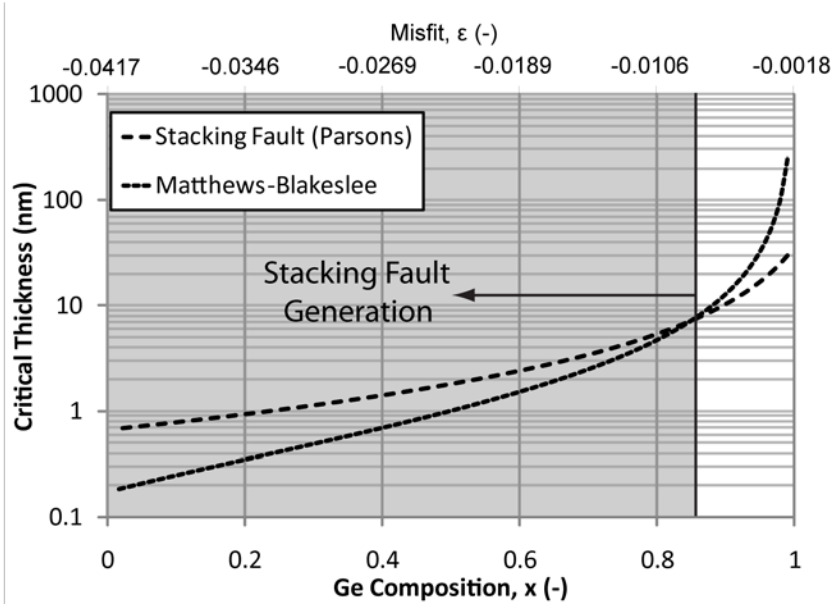

Figure 2.21: Shows the critical thickness for the formation of a stacking fault through glide and the Matthews-Blakeslee critical thickness for a $Si_{1-x}Ge_x$ layer on a relaxed Ge (001) surface.

2.5.3 Graded Layer Critical Thicknesses

As the Matthews-Blakeslee critical thicknesses are modelled on constant composition layers they are not accurate enough to model graded layers, see Section 2.6.3. Ayers [58] has produced a critical thickness model which encompasses the gradual incorporation of strain within a layer. The model reported by Ayers also encompasses reverse grading (Section 2.6.10) and "jump graded" heterostructures, where there is an initial misfit at the substrate interface prior to grading of the layer. The dislocation glide force which is exerted on a dislocation is modified by an integration of the strain which accumulates over the thickness of the layer:

$$F_h = 2Gb\left(\frac{1+\nu}{1-\nu}\right)\int_0^h \varepsilon\, dh$$
$$= 2Gb\left(\frac{1+\nu}{1-\nu}\right)\left[\varepsilon_0 h + \frac{C_f h^2}{2}\right]$$

Equation 2.25

Where ε_0 is the initial misfit at the start of the grade, this is equal to zero if the composition of the start of the graded region is equal to the composition of the relaxed layer on which it is grown. C_f is the grading rate which is usually commented in (% μm^{-1}) and is negative if the layer is reverse graded (2.6.10). When this glide force is equivalent to the drag force (Equation 2.18) so that $F_h = F_d$ the critical thickness for a reverse graded region can be calculated using Equation 2.26 and Equation 2.18 (*the initial misfit (ε_0) has been assumed to be zero when deriving this condition*):

$$h_c = \sqrt{\frac{b(1-\nu\cos^2\theta)}{4\pi C_f(1+\nu)}\ln\left(\frac{h_c}{b}\right)}$$

Equation 2.26

This condition is examined for a reverse graded system which is grown on a relaxed pure Ge layer and graded up to a composition of 0.8 as a variation of grading rate versus critical thickness. The values used are $\theta = 60°$, $b = 4$ Å and ν is set to be an average value of 0.27. The results of this calculation are shown in Figure 2.22 with the relevant Matthews-Blakeslee critical thickness of ~5 nm value also shown for a constant composition layer. The region for which Ayers' model is deemed to be valid are values below an absolute grading rate of 200 % μm^{-1}, where the critical thickness values for a graded layer are shown to be greater than the Matthews-Blakeslee critical thickness. As can be seen the actual calculated layer thicknesses are all

greater than the critical thicknesses and are thought to be well within the glide regime of dislocations. When the Matthews-Blakeslee and People-Bean curves are referred to (Figure 2.14), the region of stable layers can be enhanced due to the increase of critical thicknesses when using graded layers. This is speculated to allow higher temperature growth.

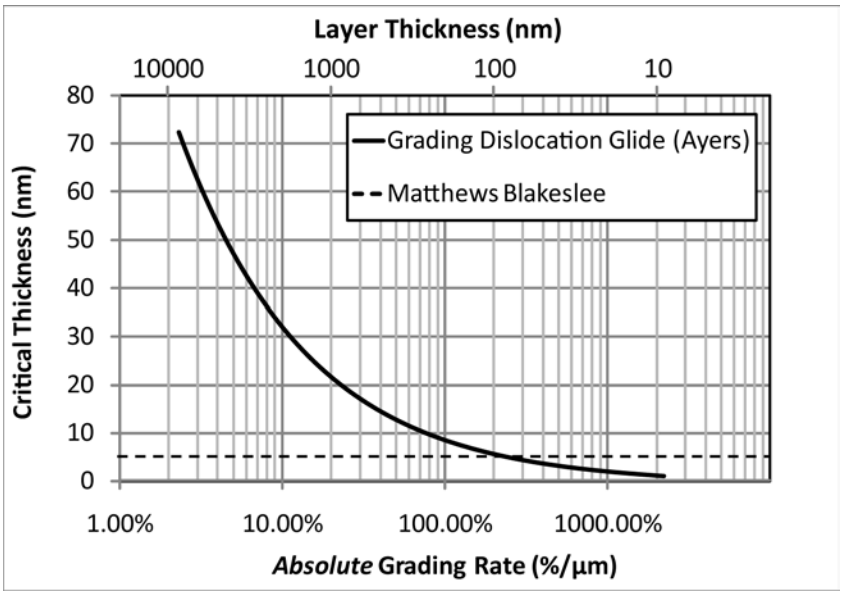

Figure 2.22: The critical thicknesses of a (reverse) graded substrate which starts on a pure Ge layer with a final composition of 0.8.

2.5.4 Thermal Expansion

The thermal expansion of SiGe alloys on Si substrates during growth at high temperatures has been shown to induce additional tensile strain within the layers. The largest thermal mismatch has been shown to result from a pure Ge layer grown on Si substrate at temperatures between 600-700°C [59]. This mismatch results in an over-relaxation of the Ge of ~104 % compared to the Si substrate. It is thought that during growth dislocation dynamics allow full relaxation of the Ge layer and the greater thermal contraction of Ge compared to Si induces tensile strain within the Ge layer

as it cools. The variation of the lattice parameters of pure Si (a_{Si}) and pure Ge (a_{Ge}) with temperature are empirically measured and reported by Yim [60] and Singh [61]:

$$a_{Si}(T) = 5.4304 + 1.8138 \times 10^{-5} T + 1.542 \times 10^{-9} T^2 \qquad \textbf{Equation 2.27}$$

$$a_{Ge}(T) = 5.6569 + 34.22 \times 10^{-6} T + 10.17 \times 10^{-9} T^2 - 0.66 \times 10^{-12} T^3 \qquad \textbf{Equation 2.28}$$

Where T is the absolute temperature in Kelvin. These expressions can then be placed into the Kasper-corrected Vergard's law (Equation 2.1) to derive an expression for the lattice parameter of SiGe alloys at any composition (from 0 to 1) and at any temperature until the melting point of the alloy (<900°C). The lattice parameter of a pure Ge layer at a temperature of 600°C is used in Equation 2.11 which results in a relaxation of 104.2 % compared to a Si substrate at room temperature, this agrees with the results previously reported by Hartmann [59]. The thermal expansion results in a minor strain and will not play a significant role in the dislocation dynamics of a buffer.

2.5.5 Cracking

Cracking is a relaxation mechanism which physically fractures the material with features which are much larger than dislocations. If tensile strained layers are not allowed to relax by dislocation dynamics another much lower temperature process occurs where the top epitaxial layer can shear and produce *ordered cracking*. Cracking has not widely been reported in SiGe materials due to most processes

relaxing under compressive strain and having relatively thin layers (> 300 nm). The crack density (ρ_{CD}) is defined as the line density of epitaxial layer cracks on the (001) surface. Currie *et al* [62] are the only source which the author has found who characterised and reported a cracking density of 47 cm^{-1} in their forward linear graded SiGe structures which were graded to a pure Ge layer. Murray *et al* [63] have studied the effects of cracking on III-V materials such as GaAs and InP and have produced a sophisticated model to calculate the relaxation of the layer due to cracking and also to find the effective "*cracking critical thickness*".

The cracking critical thickness can be found as an energy balance condition. The upper energy limit which is required to create a crack is the sum of the areal energy densities required to create two free surface planes in the [110] directions, as used by Murray [63]:

$$E_s = \frac{Y_{[110]} a}{\pi^2} \qquad \textbf{Equation 2.29}$$

Where Y is the Young's modulus in the [110] direction and a is the relaxed lattice constant of the layer. However, the lower limit of the crack surface formation can be found using the Morse or Lennard-Jones potentials as used by Kelly et al [64], which is half the value of Equation 2.29. To keep the crack calculation simple the layer is modelled as a single constant composition layer on a Ge (001) substrate and the strain energy accumulated within the layer is equivalent to Equation 2.16. When the strain energy within the layer is equivalent to the (upper limit) energies used by Murray to form cracks the critical thickness is found:

$$h_c = \frac{E_s(1-\nu)}{Y_{[110]}\varepsilon^2} = \frac{a(1-\nu)}{\pi^2\varepsilon^2} \qquad \textbf{Equation 2.30}$$

When the Morse or Lennard-Jones potentials as used by Kelly [64] are applied, the lower limit of crack critical thicknesses are half the value of Equation 2.30. Figure 2.23 shows the crack critical thicknesses which are found using both the potentials by Murray and Kelly for *pseudomorphic* $Si_{1-x}Ge_x$ layers on a Ge (001) surface with compositions from x = 0 to x = 1:

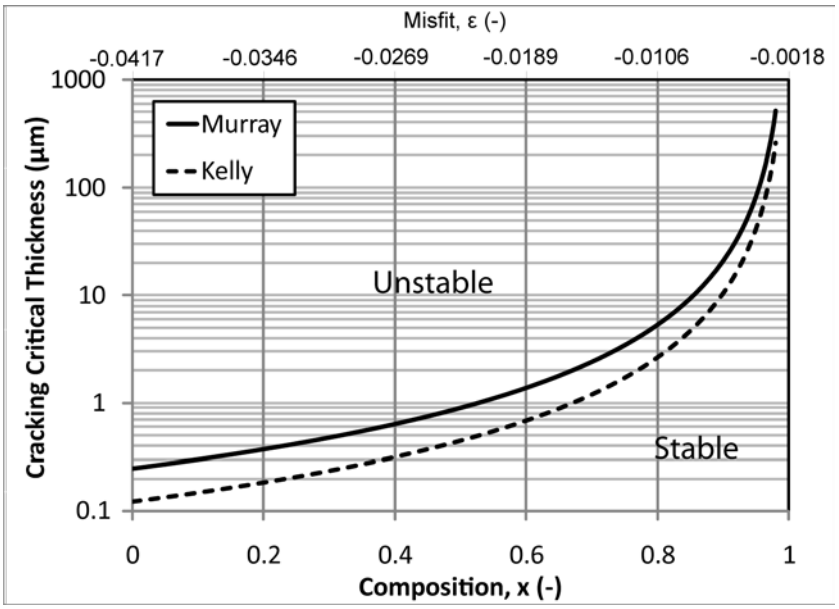

Figure 2.23: The cracking critical thicknesses for various pseudomorphic SiGe layer compositions on a Ge (001) surface.

The region below the Kelly curve denotes where pseudomorphic epitaxial layers are stable and will not crack regardless of external forces applied. The area above the Murray curve shows the region where the strain energy within the layer is greater than the energy required to create two free surfaces in the [110] direction for generation of a crack. Cracking will only occur in this region if they are grown beyond the critical thickness *and no other relaxation mechanism is present*.

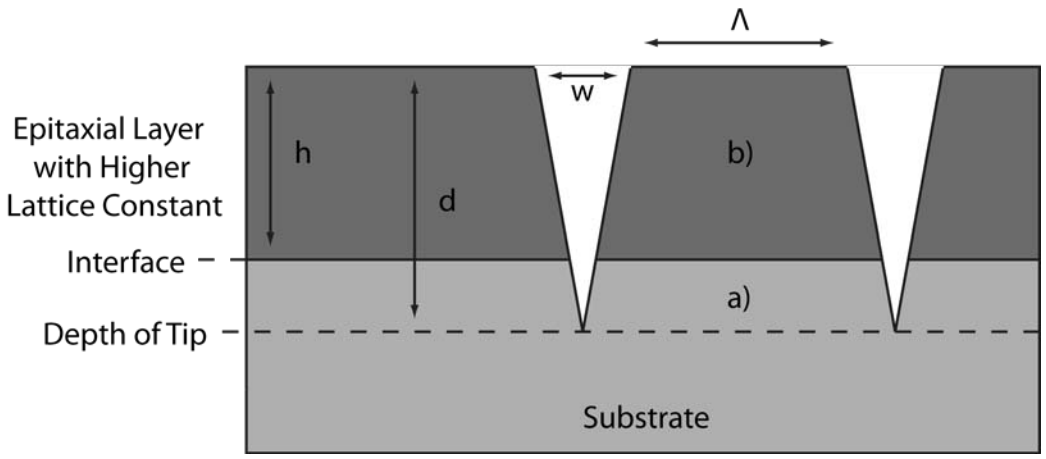

Figure 2.24: A cross section view of a "V" shaped crack, the dimensions used in calculating the relaxation are labelled. Taken from Murray[63].

Figure 2.24 shows the typical dimensions of a "V" shaped crack which runs in the <110> directions. *h* is the thickness of the strained layer, *d* is the penetration of the crack tip below the surface of the epilayer, *w* is the average width of a crack and Λ is the average spacing between the crack channels. Λ is related to the crack line density by:

$$\Lambda = \frac{1}{\rho_{\mathrm{CD}}} \qquad \textbf{Equation 2.31}$$

Where ρ_{CD} is the crack density. The dimensions of a crack relate to the layer relaxation it provides. The model used to calculate relaxation is shown by Murray [63] as a two layer system and is shown in Figure 2.24. Assuming relaxation of the layer occurs by cracking *and not dislocation dynamics* the strain which is left within the epilayer is calculated by:

$$\varepsilon_{epilayer} = \left(f + \frac{w}{\Lambda}\frac{z}{d} \right)$$ **Equation 2.32**

Where *f* is the misfit between the epilayer and the substrate as calculated by Equation 2.8, and z is the depth from the epilayer surface. Equation 2.32 is only valid for the depth range $0 \leq z \leq h$. The strain caused within the *substrate* due to the penetration of the crack is calculated by:

$$\varepsilon_{substrate} = \frac{w}{\Lambda}\frac{z}{d}$$ **Equation 2.33**

This expression is only valid for the depth range $h \leq z \leq d$. The potential areal elastic energy which is stored in a graded strain field can then be derived from Equation 2.25:

$$E_c = 2Gb\left(\frac{1+\nu}{1-\nu}\right)\int_0^z \varepsilon^2 \, dz$$ **Equation 2.34**

E_c is the residual areal strain energy stored within the layer. Once this has been calculated for both the epilayer and the substrate the relaxation (α) of a uniaxial array of V-shaped cracks can be calculated:

$$\alpha = \frac{E_h - E_c}{E_h}$$ **Equation 2.35**

When Equation 2.32, Equation 2.33 and Equation 2.34 are placed into Equation 2.35 the relaxation of the layer due to ordered crack formation can be evaluated:

$$\alpha = \frac{w}{\Lambda f}\left(\frac{d}{h}\right)^{-1} - \frac{2w}{\Lambda f} - \frac{w^2}{3\Lambda^2 f^2}\left(\frac{d}{h}\right) \qquad \textbf{Equation 2.36}$$

The ratio $\left(d/h\right)$ represents the dimensionless penetration depth of the cracks and is the same for all orientations. In conjunction $\left(-w/\Lambda f\right)$ represents the fractional retraction at the crack mouth. No previous publications were found that specifically characterise the crack dimensions within SiGe systems.

2.6 Relaxed Strain Buffers (RSB)

It was mentioned in Section 1.3 that there are currently two main types of strain induction, global and local. In this section a literature review is performed for a local strain technique and its long term viability. Further on, other literature reviews are performed for the global strain buffer techniques which have proven to yield good results.

Selective growth for source/drain stressors is a local strain technique which has been implemented in the 90nm node technology fabricated by Intel [65]. This generically involves growing a material in the source-drain regions of a MOSFET which is different to that of the substrate to impose a uni-axial strain on the channel. Examples of materials/techniques which have been successfully employed as stressors are nitride spacer deposition [66] and SiGe source/drain selective growth [67]. However,

the strain for each device with different dimensions must be optimised during CMOS architecture design. Therefore future scaling and device geometries will involve major redesign and development of the stressor for each new transistor node [68]. Additionally, limited strain can be achieved using this technique due to the channel length needed to impart strain [69] and this particular technique is only applicable to MOSFET type structures. Therefore global relaxed strain buffers are far more attractive for long-term enhancements.

Global relaxed strain buffers, also called virtual substrates, allow a strained layer with a different relaxed lattice constant or a III-V material with a similar lattice constant to be epitaxially grown on top. Commercial SiGe alloy wafers are expensive and are still low quality. Si(001) wafers are of high quality and are inexpensive, therefore they are assumed to be the initial starting point of most global strain tuning platforms. The techniques outlined in this section only use the SiGe material system with *in-situ* and/or *ex-situ* processes. The properties required from relaxed buffers for industrial applications are: low RMS roughness to the order of a few angstroms, full relaxation in excess of 95 %, and a threading dislocation density of 10^7 cm^{-2} for majority carrier devices and a value of 10^4 for minority carrier devices [41].

2.6.1 Thick Constant Composition Layers

When a thick constant composition $Si_{1-x}Ge_x$ layer is grown on a Si substrate well beyond the People-Bean critical thickness (> 1 μm) to ensure full relaxation it can be considered as a virtual substrate buffer. The best layers have been shown to be grown under a low temperature (< 600°C) and then be subjected to various anneals to further enhance the relaxation and annihilate threading dislocations. If the layer is

grown at a high temperature, 3D growth has been shown to occur [70]. The literature on thick high Ge content (x>0.5) $Si_{1-x}Ge_x$ layers is limited due to the undesirable properties seen in $Si_{0.5}Ge_{0.5}$ layers. This technique generates all dislocations at the misfit interface and generally achieves smooth layers with RMS roughness to sub-nm orders [71]. However, due to dislocation pinning and the resulting dislocation pile up at the interface (Section 2.4.7) a high TDD to the order of > 10^9 cm^{-2} is incurred [72]. Due to the dislocation blocking only marginally high relaxation levels are achieved (<85%)

2.6.2 Step Graded Buffers

Step grading is achieved by growing thick constant compositional layers on top of each other, where the composition of each layer increases as the structure progresses as shown in Figure 2.25. This process reduces the chances of misfit dislocation interaction by separation of the misfit interfaces.

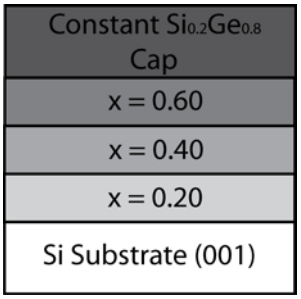

Figure 2.25: A forward step graded $Si_{1-x}Ge_x$ structure, graded up to $Si_{0.2}Ge_{0.8}$ in x = 0.2 compositional jumps.

The main drawback of this process is that thicker layers are required depending on; the final composition, the composition steps and the thickness of each step. A final layer of composition 100% typically takes 4-6 µm of epitaxial growth where the

layer is almost fully relaxed (>95 %) [73]. For 80 % step graded buffer it has been reported that the surface RMS roughness increases up to 10 nm [74]. Additionally in low composition (<30%) step graded buffers the TDD ranges from 10^6 cm^{-2} to 10^7 cm^{-2} and this value is expected to increase to levels up to 10^8 cm^{-2} with increasing Ge composition.

2.6.3 Linear Graded Buffers

Inserting a graded composition layer between a final composition layer and the Si(001) substrate has been a well documented technique, and has been performed with both MBE and CVD growth with consistently good characteristics, an example of a forward graded structure is shown in Figure 2.26. Dislocation pinning is a major impediment to the final TDD of a buffer. As the misfit strain is dispersed over a distance, the nucleation and glide of dislocations will also be spread over this graded thickness, as each atomic layer will have its own equilibrium lattice parameter. Due to this separation of dislocations the probability of blocking from dislocation-dislocation strain field interactions will be drastically reduced.

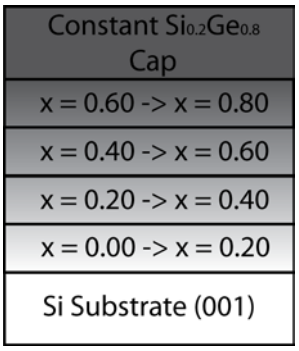

Figure 2.26: An example of a forward linear graded $Si_{1-x}Ge_x$ structure, graded up to $Si_{0.2}Ge_{0.8}$ with a thick constant composition cap.

Fitzgerald *et al* [75] have covered a great deal of ground and initiated major interest in this particular technique. Modelling that was carried out revealed that the threading dislocation density depends on three major growth related parameters which are controllable when growing the buffer structure. These controllable parameters are growth temperature, growth rate and grading rate, where all three are interdependent when growth by CVD is performed. The relationship between these parameters is shown in Equation 2.37 [76]where ρ is the final TDD achieved.

$$\rho = \frac{2R_g R_{gr} \exp(E_{glide} / kT)}{bBY^m \varepsilon_{eff}^m} \qquad \textbf{Equation 2.37}$$

R_g is the growth rate and is dependent of the growth temperature and the precursors used when layers are grown by CVD. R_{gr} is the grading rate and will determine the [001] separation of the misfit dislocations, E_{glide} is the activation energy for dislocation glide. k is Boltzmann's constant, T is the growth temperature used, b is the Burger's vector of 60° dislocations. B is a constant related to the initial velocity (Equation 2.14), Y is the Young's modulus for the alloy layer, ε_{eff} is the effective strain in the system and m is an exponent which is generally between 1 and 2.

A study by Dutartre *et al* [77] shows the dependence of TDD with grading rate. In the study, graded layers had a final composition of x = 0.32 with a top layer constant composition thickness of 1.1 µm. As reported by Larsen [41] a reduction in TDD of 10^3 should be received if a graded layer with a grading rate of 10 % µm^{-1} is implemented; however, this was not shown by Dutartre *et al*. This optimal grading rate has been revealed to yield dislocation densities of 10^6 to 10^7 cm^{-2} when grading to high Ge compositions (x > 0.9).

This inhomogeneous behaviour has been attributed to two main mechanisms. Firstly, the malleability of pure Ge [44]. This was proposed by Isaacson *et al*, who state that when grading to pure Ge layers, mechanical weakening due to a loss of the solid-solution strengthening effect lowers the nucleation energy barrier allowing relaxation through half loop formation. This was shown to be avoided by using a lower growth temperature.

Secondly, if the misfit dislocation network is close to the growth surface their strain fields will re-arrange mobile adatoms during growth, which results in surface undulations which are more commonly known as crosshatch [78]. A higher TDD was shown to be present as dislocations are pinned due to the surface crosshatch of the layer [49]. Blocking will produce pile up, and as reported by Samevedam *et al* will be a part of a vicious cycle [49] which reduces the local growth rate around arrested dislocations which in turn creates a rougher surface and induces more pileup.

Mid-growth chemical mechanical polishing (CMP) has been shown to prevent pileup and hence further reduce the final TDD by allowing trapped threading dislocations to glide. Currie *et al* [62] compare traditional linear grading of different grading rates and a graded buffer with mid-growth CMP performed. It should be noted when buffers are graded with a grading rate of 10 % μm^{-1} to a pure Ge layer with a growth temp of 750 to 800°C a TDD of 1-7 x 10^7 cm^{-2} is achieved with a surface RMS roughness of 47 nm.

In an effort to reduce the TDD, the buffer was grown to a composition of 51 % Ge and a CMP step was employed to reduce the RMS roughness from 37.3 nm to 0.4 nm. When growth was resumed and graded to a pure Ge layer the final TDD reported was 2.1 x 10^6 cm^{-2} alongside a final RMS of 24.2 nm. Bogumilowicz *et al* [30] record the roughness of the graded buffer at different final compositions after CMP was performed on a linear graded 51 % Ge virtual substrate. Growth of the graded region was continued at a temperature of 850°C with a grading rate of 9 % μm^{-1}. With a final Ge composition of 55-60 % an RMS roughness of 5 nm is acquired, and continued growth of the linear graded region observes a 75 % Ge layer with a 15 nm RMS roughness. In very high compositions of 88 % and pure Ge a graded layer RMS roughness of 17 and 20 nm respectively were observed. The TDD during this process is also characterised, ranging from 5 x 10^5 cm^{-2} at the CMP polished 51 % Ge layer to 10^5 cm^{-2} at high compositions of 88 % to 96 %.

Other issues to note are that linear grading produces buffers with large thicknesses for high Ge compositions, this can lead to wafer bowing due to the thermal gradient over the wafer during growth [79]. Currie *et al* [62] have noted as-grown cracks are generated in buffer thicknesses of 23 µm which are slightly tensile strained due to the thermal contraction between the Si substrate and the final pure Ge layer. Furthermore when device structures are fabricated on virtual substrates it has been reported that the reduced thermal conductivity of the buffer causes devices to a suffer body heating effect [80], reducing the mobility enhancements received.

Overall the linear grading technique has been proved to have low TDD values through thick graded regions and relatively high growth temperatures. Although the

layers achieve full relaxation the surface roughness cultivated during growth is a major setback to the quality of the buffer. A CMP step can be employed intermediate to the growth; however, this requires an ex-situ process, and in conjunction with the long growth times associated with the thick layers this will lead to long production times. This technique is thought to be an excellent means to induce strain in a layer which is intended to be transferred onto another layer; however, for this technique to be used as a device platform a thin high composition buffer is required.

2.6.4 Terrace Grading

Terrace grading was a concept which was designed by Capewell *et al* [52]. Terrace graded structures consist of both linear graded and constant composition layers. The terrace graded structure is then extended by alternating from linear graded layer to constant composition layer until the desired composition layer is reached; an example of this is seen in Figure 2.27.

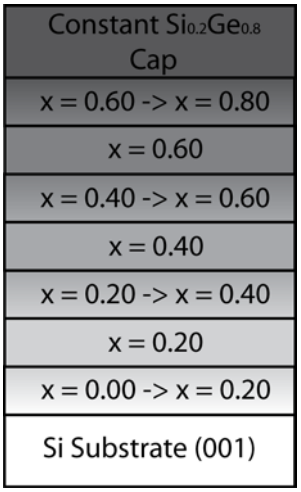

Figure 2.27: An example of a forward terrace graded $Si_{1-x}Ge_x$ structure, graded up to $Si_{0.2}Ge_{0.8}$ in x = 0.2 terraces with a thick constant composition cap.

The linear graded region spatially separates the misfit dislocations to avoid interactions. However, pile up still occurs due to surface roughness and accumulates as with linear graded buffers. Within certain growth temperatures the constant composition cap of a graded buffer has been shown to have a smoothing effect on the graded region [81]. The addition of the constant composition layers smoothes the surface of the graded layers, allowing the glide of pinned threading arms hence avoiding pile-up and its associated roughening effect. This reduces the need for nucleation of further threading dislocations to relax the buffer. Terrace graded structures have been investigated up to a composition of 100 % by Nash [39] with thicknesses ranging from 10 to 20 µm. The associated TDD of buffers with compositions up to $Si_{0.5}Ge_{0.5}$ range from 10^6 to 10^4 cm^{-2} with roughnesses of approximately 3 to 2 nm and top layer relaxations of 95 % [82]. However TDDs greater than 10^7 cm^{-2} were observed for terrace graded buffers graded to pure Ge with RMS roughnesses of 13 nm. While terrace grading shows smoother surfaces and much lower TDDs than linear graded buffers up to compositions of $Si_{0.5}Ge_{0.5}$, continued grading to pure Ge severely reduces buffer quality.

2.6.5 Ge Condensation

Silicon-On-Insulator (SOI) substrates of high quality are created through wafer bonding and the smart cut process. They are widely commercially available; however, creating a SiGe alloy-on-Insulator (SGOI) using the same technique has proved to succumb to increased surface roughness, Ge diffusion and poor thermal conductivity [83] & [84]. The Ge condensation method allows a smooth $Si_{1-x}Ge_x$ alloy layer to be formed on top of a buried oxide (BOX).

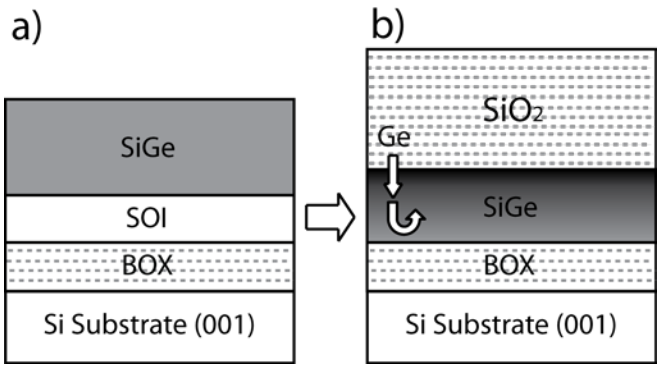

Figure 2.28: A schematic representation of the Ge condensation technique, from a) growth of a SiGe layer on SOI which is then oxidised to form b) an oxide layer on top of a higher Ge composition SiGe layer due to selective oxidisation. Taken from Nakaharai [85].

The general methodology involves a thin pseudomorphic SiGe alloy to be grown on a SOI substrate, Figure 2.28a). It is then subjected to a selective oxidation [86] of the Si on the surface of the SiGe alloy. As the Si is consumed to form the SiO_2, Si diffuses towards the oxidisation interface and Ge is rejected and diffused toward the buried oxide to increase the overall composition of the alloy layer, which becomes thinner [87], this is shown in Figure 2.28b). It is possible to achieve any composition of SiGe desired through this technique purely by varying the oxidation time.

As oxidation occurs the relaxation of the SiGe layer also occurs through misfit dislocation and stacking fault formation [85]. Though much work has been done on conventional high composition Ge condensation, threading dislocation densities have not been widely published. Nakaharai *et al* [85] report a range of threading dislocation densities from 0.9×10^8 cm^{-2} to 1.5×10^8 cm^{-2} for Ge compositions ranging from x = 0.23 to x = 1. Alongside the threading dislocations, stacking faults and microtwins were reported. Due to the formation of these defects a high degree of relaxation occurs in the layers, Nakaharai reports a relaxation of ~78 %. A low roughness of 1.3 nm was reported for a pure germanium-on-insulator layer and the

main mechanism for roughening was thought to be from the crosshatch formed on the surface. A two step condensation method has been reported where a TDD value of 1 x 10^3 cm^{-2} has been reported for low composition (x~0.2) layers [88]. However, different defect types alongside the threading dislocations were reported.

It has been shown that devices fabricated on various platforms-on-insulator (POI) will be subject to reduced thermal conductivity due to the oxide layer [80]. This reduces the efficiency of the mobility enhancements from inducing strain in the new channel material. The standard Ge condensation technique which forms a high composition relaxed layer buffer has a high degree of relaxation and a very low roughness; however, the defect levels are extremely high and are comparable with high composition SiGe layers that are deposited directly on Si (001) substrates [89] (Section 2.6.1).

2.6.6 Ion implantation

The ion implantation method is another way achieving very low RMS roughness buffers. Ion bombardment of the substrate is performed prior or post growth of a metastable pseudomorphic layer which is grown at low temperatures [11]. Examples of different species of implant that have been demonstrated to achieve effective relaxation in layers are He, Ar, Si and Ge [90]. After implantation the layers are subjected to a high temperature anneal to induce relaxation. The implantation introduces point defects which mainly consist of vacancy clusters that act as nucleation sources and as dislocation absorbers. The introduction of defects effectively reduces the energy barrier to dislocation nucleation [91]. Therefore when layers are annealed, dislocation half loops are formed and allowed to glide

throughout the structure. Development of this technique geared towards high composition SiGe buffers has been limited as presented by Hoshi *et al* [92].

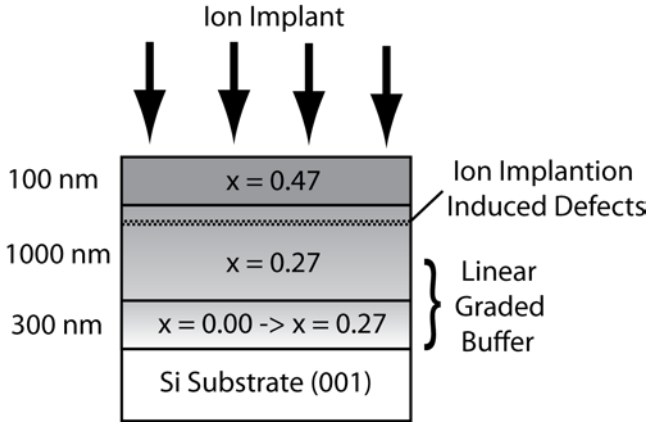

Figure 2.29: The ion implantation process as reported by Hoshi [92].

A fully relaxed 27 % Ge content graded region buffer was used as a platform in the study by Hoshi *et al* which was implanted with Si^+ ions. This platform was then subjected to a re-crystallisation anneal of 700°C for 10 mins and subsequently had a 100 nm 47 % Ge layer grown on top, as shown in Figure 2.29. The implant showed an improvement in roughness when two samples, one with the implant (0.45 nm) and one without (0.67 nm) were grown on; however, at these low levels of roughness the error in the AFM measurement is comparable to the actual values. The relative relaxation of the layer compared to the underlying layer was 0 % prior to annealing which indicates the $Si_{0.53}Ge_{0.47}$ layer was fully strained. Annealing post-growth shows the relaxation to be 50 % and 61 % for the un-implanted and the implanted samples respectively; it was thought the implant performed was not optimised for the composition, but the relaxation induced is typical of ion implanted buffers. This method of achieving relaxed buffers is limited due to the implant that is required.

Even though a low RMS roughness is achieved the relative relaxation improvements are still to be optimised.

2.6.7 Low Temperature Method

The low temperature buffer technique utilises grown in nucleation centres to relax the buffer layers. Reported structures by Peng *et al* [93] are grown by MBE.

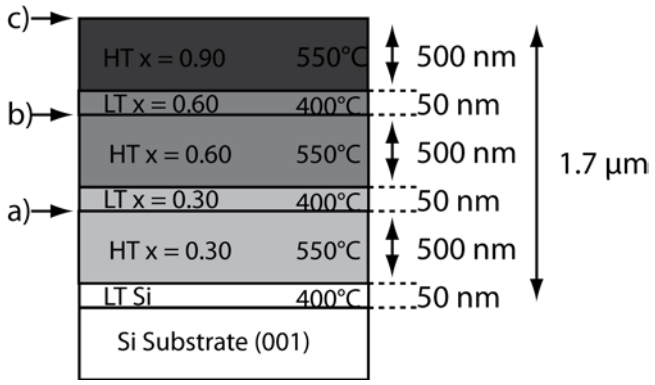

Figure 2.30: The low temperature (LT) buffer as reported by Peng [93]. The LT layers are grown at 400°C and the high temperature (HT) layers are grown at 550°C.

The structure grown by Peng et al, shown in Figure 2.30, is typical of low temperature (LT) buffers. Initially, a thin 50 nm layer of Si was deposited at a low growth temperature (LT) of 400°C. MBE growth of LT layers allows introduction of point defects which mainly consist of vacancy clusters that act as nucleation sources and as annihilation centres for dislocations. After which a 500 nm $Si_{0.7}Ge_{0.3}$ layer was grown at a higher temperature (HT) of 550°C. This allows dislocations to glide and relax the layer then subsequently terminate at a void or point defect, reducing the final TDD of the layer. At this interface, shown in Figure 2.30a), the TDD range was 1–2.5 x 10^5 cm^{-2}, with an RMS roughness of 1.8 nm and a relaxation of 90 %. The same LT/HT cycle was performed with two more composition steps for HT layers of

composition $Si_{0.4}Ge_{0.6}$ and $Si_{0.1}Ge_{0.9}$. At Figure 2.30b) a TDD of 5 x 10^5 cm^{-2} and a roughness of 2.4 nm was reported and the layer was 89 % relaxed. The complete structure (Figure 2.30c)) showed a high degree of relaxation, 5.9 nm RMS roughness and a TDD of ~3 x 10^6 cm^{-2}. The authors showed the full $Si_{0.1}Ge_{0.9}$ structure with a thickness under 1.7 µm.

When compared to other techniques this method allows a fully relaxed good quality high composition layer which has a low roughness and low defect levels. An issue that was noted was that MBE was used, whereas industrial institutions employ CVD growth for mass produced growth. If CVD growth was utilised, due to the temperature limited regime of precursors at low temperatures there would be difficulties of high surface segregation [94] and low growth rate in deposition of the LT layers.

2.6.8 Two Temperature Growth Method

The two temperature method has been refined to give high quality layers, and mainly performed to give smooth and relatively defect free Ge layers directly on a Si(001) wafer [41] & [95]. A schematic of the two temperature method is shown in Figure 2.31.

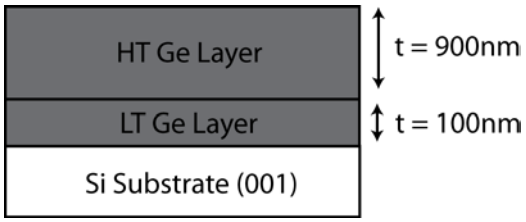

Figure 2.31: A schematic of the two temperature layer, as reported by Hartmann [59].

The first Ge layer is deposited at a low temperature (LT) of about 400°C, this is to keep the surface as smooth as possible whilst proceeding in a Frank-van der Merwe growth mode and not to enter 3D islanding or Volmer-Weber growth form. This step also generates a vast amount of dislocations, of the order of 10^8 to 10^9 cm^{-2}, for the next step to fully relax the maximum amount of strain possible in a SiGe system where $\varepsilon = -0.0417$ [96]. After a 100 nm LT layer has been deposited a high temperature (HT) layer of growth temperature of 670°C allows the Ge on Ge adatom transport to minimise the surface energy and smoothen the layer [94]. The final step to the technique is annealing at a high temperature which will allow dislocations to glide. The high density of dislocations prior to the anneal (~10^8 cm^{-2}) gives a high probability that most threading arms will annihilate, significantly reducing the TDD [97]. This will allow some surface adatoms to become mobile and thus incur some increase in surface RMS roughness. It has been shown that this method allows a comparatively thin fully relaxed pure Ge layer to be grown with a sub-nanometre RMS roughness and a relatively low TDD with values in the vicinity of ~10^7 cm^{-2}.

2.6.9 Summary of Existing High Ge Content Buffers

Technique	Thickness of buffer (μm)	Final Composition (% Ge)	Relaxation (%)	RMS Roughness (nm)	TDD Values (cm^-2)	Author(s)	Notes
Ge Condensation	0.2 to 0.035	82%	78%	1.3	(0.9 to 1.5) x 10^8	Nakaharai *et al*[85]	Si-on-Ge platforms and oxidisation needed
Ion Implantation	1.4	47%	Induces an extra 10% relaxation.	0.45	-	Hoshi *et al*[92]	Mid-growth ion implantation needed
Low Temperature Method	1.65	90%	> 90%	5.9	3 x 10^6	Peng *et al*[93]	Developed on a 27% fully relaxed buffer and anneals were performed
2-Temperature Method	1.1	100%	104%	0.7	2 x 10^7	Luan *et al*.[98]	Segregation effects possible for SiGe alloys
Linear Grading	12	100%	99%	47	(1 to 5) x 10^7	Currie *et al*.[62]	CVD grown samples, pile-up observed
Linear Grading with CMP	~10	88%	104%	17	1 x 10^5	Bogumilowicz *et al*[30]	Mid-growth CMP employed, no pile-up observed.

Table 2.2: The comparison of critical parameters for a high composition (>75 % Ge) buffer structure for different methods

Table 2.2 shows a comparison of all the buffer techniques which have been mentioned in this section comparing all their parameters which determine their quality as strain tuning platforms. It can also be deduced that the most effective way of reducing threading dislocation densities is by allowing dislocations to glide during the growth of thick layers (> 500 nm) giving a high dislocation annihilation probability. However, it is also surmised that to achieve a smooth surface it is better to grow epitaxial layers which are then subjected to high temperature anneals (as with the ion implantation technique) so that the dislocation strain fields do not re-arrange mobile adatoms during growth (as with the linear grading technique). If *ex-situ* processes are utilised, the cost per wafer and also processing time will increase

which is not favourable for a fast-throughput process, making Ge condensation, ion implantation and mid-growth CMP less desirable.

It can be seen that, generally, thicker buffers have low defect densities and higher surface roughness, but will consequentially have longer growth times. Additionally, thinner buffers generally require low temperature growth, annealing and ex-situ processes (e.g. ion implantation or layer transfer) which are impractical if CVD growth is employed. Therefore a technique which could be grown with high temperatures and allow dislocations to glide during growth whilst having a smooth surface would be a very attractive overall solution to the relaxed strain buffer problem.

2.6.10 Previous work on Reverse Grading

Reverse grading is defined as an epitaxial graded layer where the Ge composition of the start of the grade is higher than the Ge composition at the end of the grade. Work to date on reverse graded (RG) structures has only been done on low composition buffers. Wong *et al* [99] have produced work on RG structures which are grown directly on a Si(001) substrate without a relaxed underlayer. Low pressure (LP-) CVD was used to deposit a 90 nm RG layer of starting composition $Si_{0.65}Ge_{0.35}$ and ending composition $Si_{0.86}Ge_{0.14}$ on the Si(001) substrate. A 200 nm constant composition layer of $Si_{0.75}Ge_{0.25}$ was then deposited, ending with a 20 nm strained Si cap, this structure is shown in Figure 2.32.

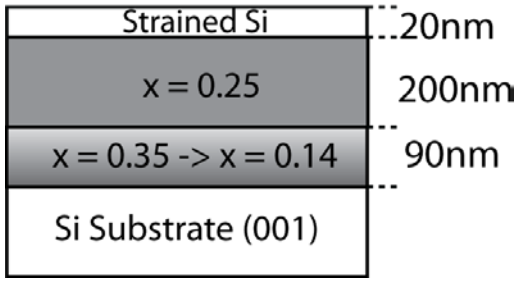

Figure 2.32: The reverse graded $Si_{1-x}Ge_x$ structure reported by Wong [99].

A TDD density of $<1 \times 10^5$ cm^{-2} with a RMS surface roughness of 1.1 nm is reported. The relaxation of the layer was found to be 65 % compared to the Si(001) substrate. In further works by Liu *et al* [18] when the top constant composition SiGe was increased to 32 % Ge the TDD was found to be 8×10^5 cm^{-2} with a higher degree of relaxation of 85 %, the surface roughness was reported to be unchanged. Within these layers is it thought that most misfit and threading dislocations would be generated within the Si(001) substrate at the Si(001)/RG interface and annihilation would be the main mechanism for threading dislocation density reduction. Secondly the threading arms reaching the surface would then be split to form further misfit dislocations at the RG/SiGe layer interface and further reduce threading dislocations. Modelling of these buffers was performed by Ayers [58] to find that due to the composition jump of the reverse graded region and the Si(001) substrate multiple critical thickness were possible due to the relaxation in the graded layer.

3 Experimental Techniques

In this chapter the experimental techniques used in this thesis are described. The techniques described are transmission electron microscopy (TEM), atomic force microscopy (AFM), differential interference contrast (DIC) microscopy, selective etch pit (EPD) chemistry, high resolution x-ray diffractometry (HR-XRD) and secondary ion mass spectroscopy (SIMS). The operating principals are described along with basic theory of each technique and their limitations.

3.1 Transmission Electron Microscopy (TEM)

TEM allows high resolution (~2 nm) microscopy of epitaxial layers where the thickness and defects within buffers can be quantitatively examined. The TEM used within this study was a JEOL JEM-2000FX TEM. The description given below is the specifics used in this study but is generally accepted as the main operating principals of a TEM.

There are two general orientations of the sample which can be viewed within the TEM. These allow different planes within the crystal structure to be accessed for analysis. To assess the thicknesses of layers (in the [001] direction) and the [001] spacing of misfit dislocations the sample is viewed *along* the (110) planes in cross sectional TEM (XTEM). To measure high threading dislocation densities ($>5 \times 10^8$ cm^{-2}) the sample can be viewed *along* the [001] direction as plan view TEM (PVTEM).

3.1.1 Sample Preparation

Semiconductor materials placed within the TEM must be of the order of a few hundred nanometres thick in order to allow electrons to pass through the sample for image formation. This is accomplished by mechanically grinding the sample to a few tens of microns followed by ion polishing and milling using a precision ion polishing system (PIPS), until the sample is perforated. For an in depth description on sample preparation see Goodhew [100].

Practical limitations of sample preparation only allow an electron transparent region, and hence viewable area, of a few hundred square microns. It is thought that the preparation technique could also induce additional dislocations, but if the dislocation density is low enough to be confirmed through EPD measurements (Section 3.5) this is deemed inconsequential. Cracking of the epitaxial buffer (Section 2.5.5) occurs with samples provided for this study and typical dimensions of cracks are measured directly from cross sectional TEM images. It must be considered whether the cracks viewed within the buffer are propagated from the preparation of the sample. Unfortunately as the cracks are thought to have a vertical scale of a few microns AFM does not have the vertical range to measure a crack profile. DIC observations are also limited as the plan view dimensions of cracks appear to be too small to be observable through DIC microscopy. One minor study was performed where the sample was subjected to a selective etch, the results are reported in Section 4.3.5. The study confirms that cracking does partially penetrate into the Si (001) substrate. It is concluded that due to the limitations of present characterisation techniques the measured dimensions of the crack are to be taken at face value. Murray *et al* [63]

have used the same reasoning for their observed profiles and are forced to accept that their images obtained are typical cracks within their buffers.

3.1.2 Image Formation

A schematic representation of a TEM is shown in Figure 3.1. Electrons are generated from thermionic emission from a heated tungsten filament within the electron gun. They are then accelerated towards a grounded anode at the bottom of the electron gun at a typical accelerating voltage of 200kV. This directs the electrons towards the bottom of the TEM column.

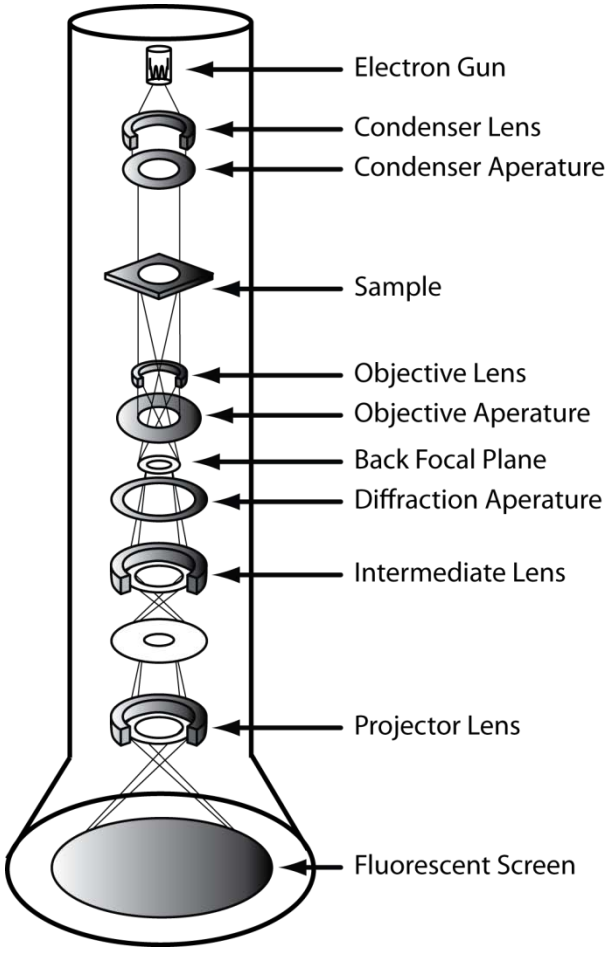

Figure 3.1: A schematic representation of a typical transmission electron microscope.

A Wehnelt cap shields the filament and focuses the beam to reduce electron scattering into the wall of the column. The whole column is kept under a high vacuum ($< 10^{-7}$ mbar) to reduce electron interaction with matter. Additionally, the whole system is water cooled to reduce the fluctuation of electron beam strength due to heating caused by the electron beam interactions with atoms within the TEM column.

Initially the beam is passed from the electron gun through the condenser lens to control the size of the beam. It is then passed through the condenser aperture to reduce the width and intensity of the beam, which is to be then passed through the sample. This condensing stage serves to collimate the beam. The lenses in the TEM are magnetic pole pieces which use electromagnetic fields to focus the electron beam, and act similar to conventional lenses in an optical microscope.

After passing through the sample as a collimated beam electrons are then directed through the objective stage. The objective lens serves to expand the beam as received from the sample thereby increasing magnification. The detail of the image can be enhanced by further reducing the width of the beam to stop excess reflections from the phosphorous screen which can shadow details within the images. The beam is passed through further lenses to correct aberrations incurred and to orientate the image in relation to the sample. The image is then shown on the phosphorous coated screen; the sample can then be manually moved to highlight different areas. Further on in this investigation the images were recorded by a CCD camera which replaced the phosphorous screen. For an exhaustive description of principals and practicalities of transmission electron microscopy see Agar [101].

3.1.3 Image Contrast and Diffraction

Using a built in goniometer the sample can be tilted in orthogonal directions within the electron beam. By placing the sample in different orientations electron diffraction is achieved causing image contrast. Contrast through diffraction transpires when there is a discontinuity within the crystal structure such as strain or when defects are present.

A diffraction mode is achieved within the TEM by adjusting the strength of the projector lens so that the image from the back focal plane is passed to the phosphorus screen. At the back focal plane all parallel rays cross splitting the electron beam into multiple beams of reflections from different planes. During normal imaging, all of these different reflections are superimposed on top of each other, giving only an image of any physical features within the sample. Within diffraction mode the multiple electron beams from different reflections are focussed so that images from different planes are represented as spots on the screen. The spots produced are positioned relative to the incident beam angle and therefore represent different crystallographic planes.

Tilting the sample allows electrons to diffract from certain crystal planes. The [000] diffraction spot is always seen and results from electrons passing straight through the sample. A two beam diffraction condition is achieved when the sample is tilted so that the [000] spot and only one other spot is highlighted. A bright field image is then formed when the diffraction aperture is used to select only the electrons in the [000] spot. Contrast is formed by the rejection of electrons in the other spot which are

reflected from the selected crystallographic plane. This causes a subtraction of electron intensity from any anomalies in that plane, resulting in contrast.

A dislocation contrast will only occur if the planes which are displaced by dislocations cause a diffraction of the electron beam. The displacement of the lattice by a dislocation is defined by its Burgers vector, b (Section 2.4.3 & 2.5.2). If the diffraction condition g is perpendicular to the Burgers vector ($g \bullet b = 0$) then the dislocation will not appear within the TEM. This is termed the invisibility criterion; a simple schematic of this is shown in Figure 3.2.

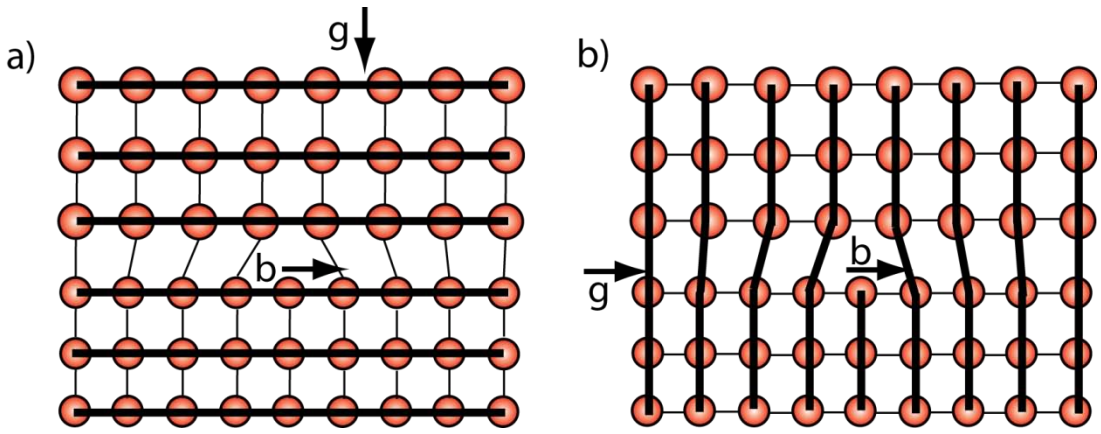

Figure 3.2: A physical representation of the $g \bullet b$ invisibility criterion. a) Shows that when $g \bullet b = 0$, the distortion caused by the perfect edge dislocation is not observable when the Burgers vector is perpendicular to the vector of view. b) Shows that when $g \bullet b \neq 0$ the dislocation is visible.

Dislocations in SiGe systems are generally mixed dislocations and as such have edge *and* screw components (Section 2.4.3). The screw component of the dislocations will form on the (111) plane and will therefore have an angle (θ) of $0° \leq \theta \leq 90°$ between the line direction u and the Burgers vector (Section 2.4.3). This modifies the invisibility criterion so that dislocations will only be in contrast if $g \bullet (b \times u) \neq 0$ *and*

$g \bullet b \neq 0$ [50]. Calculations show that both conditions are not often simultaneously fulfilled, and a dislocation is considered invisible if $g \bullet (b \times u) \leq 0.5$ *and* $g \bullet b \leq 0.5$

	|g.b|							
	90° Partial		60° Dislocation				30° Partial	
g\b	1/6 (112)	1/6 (1-12)	1/2 (101)	1/2 (-101)	1/2 (011)	1/2 (0-11)	1/6 (2-11)	1/6 (211)
(220)	0.7	0.0	1.0	1.0	1.0	1.0	0.3	1.0
(-220)	0.0	0.7	1.0	1.0	1.0	1.0	1.0	0.3

Table 3.1: The dot product for *perfect edge* dislocations within a f.c.c. crystal lattice at orthogonal diffraction conditions.

	|g.(b x u)|							
u = (1-10)	90° Partial		60° Dislocation				30° Partial	
g\b	1/6 (112)	1/6 (1-12)	1/2 (101)	1/2 (-101)	1/2 (011)	1/2 (0-11)	1/6 (2-11)	1/6 (211)
(220)	0.94	0.94	1.41	1.41	1.41	1.41	**0.47**	0.47
(-220)	**0.00**	0.00	0.00	0.00	0.00	0.00	0.00	**0.00**

Table 3.2: The dot product for *mixed* dislocations within a f.c.c. crystal lattice at orthogonal diffraction conditions.

Table 3.1 and Table 3.2 show the dot product of 60° dislocation and its 30° and 90° partials. Conditions which meet the invisibility criterion are highlighted in both tables. 60° dislocations are shown to appear in all orthogonal diffraction conditions. However, the 30° and 90° partials are only shown to appear in either (220) or (-220) diffraction conditions. As stacking faults are 90° partials (Section 2.5.2) they are subjected to the same invisibility criterion. This means that 60° dislocations and stacking faults can be differentiated by viewing the sample in orthogonal diffraction orientations. For more details on the diffraction conditions of dislocations see Goodhew [100]. All the samples for this work that were viewed within the TEM were subjected to the cross sectional <220> diffraction conditions to determine the type of dislocations viewed.

3.2 Atomic Force Microscopy (AFM)

AFM allows high resolution (0.2 nm) topographical vertical surface scans of epitaxial layers, and has a horizontal resolution of 4 nm. This permits quantification of the surface roughness of the samples, through its root mean squared (RMS) value and height range. The RMS roughness quantifies the density of surface features and the height range gives information about their magnitude. AFM was performed using a Digital Instruments Nanoscope III contact-mode AFM and the results were digitally recorded and analysed using Digital Instruments' NanoScope software. The operation of a general *contact-mode* AFM is described below.

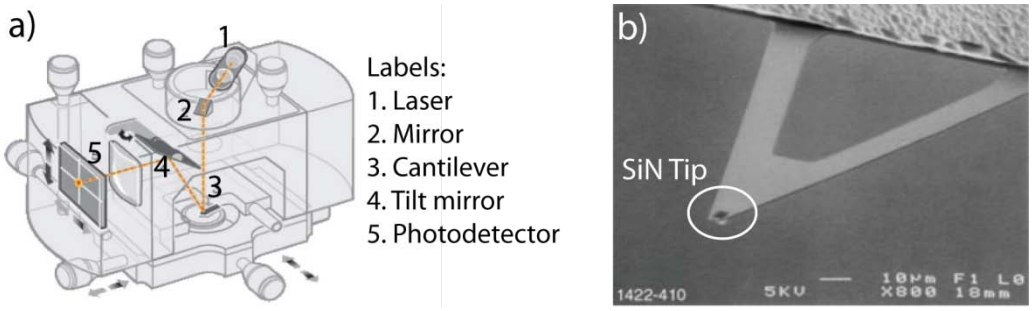

Figure 3.3: a) The AFM head where the laser system is mounted. b) a TEM micrograph of an AFM contact mode cantilever. The SiN tip can be seen on the end of this cantilever. Both images were taken from the Veeco Training manual [102].

Figure 3.4 shows a schematic of the AFM system. A 1 cm^2 sample was cleaved from a wafer and placed under the cantilever within the AFM head as seen in Figure 3.3a). A SiN probe with a tip of approximately 20 nm was situated on the end of the cantilever (Figure 3.3b)). The SiN tip is lowered onto the surface of the sample so that inter-atomic forces are experienced by the tip *without* making mechanical contact with the surface [103]. The piezoelectric ceramic stage with the sample on

top is then scanned along the x and y directions to build up a two dimensional image at a lateral resolution of approximately 4 nm. The piezoelectric stage has a vertical resolution of approximately 0.2 nm.

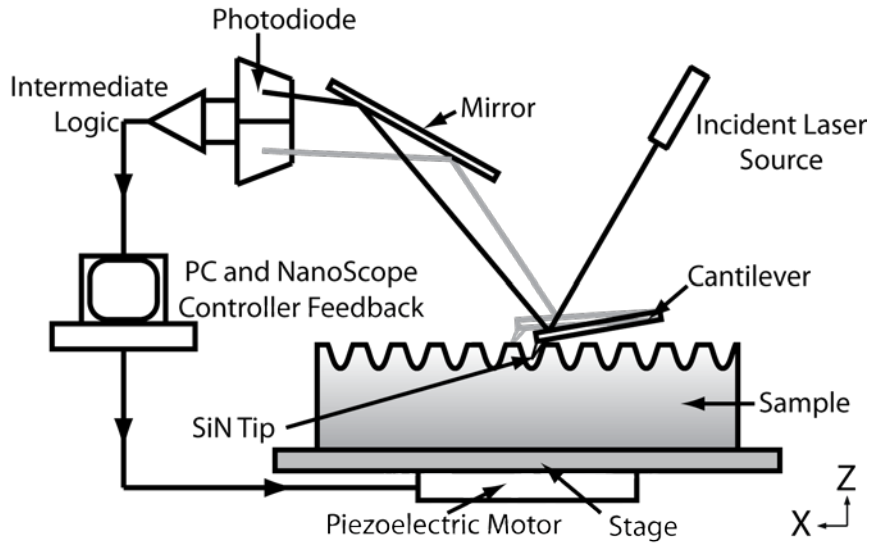

Figure 3.4: A schematic of the AFM system. The piezoelectric motor is moved laterally to perform a scan and when the cantilever is deflected the control system lowers the stage until no deflection of the reflected laser is measured.

As the sample is moved relative to the SiN tip the surface morphology imparts enough force to the SiN tip to bend the cantilever. This deflects the laser beam which is reflected into the photodiode. When the photodiode registers a change in the laser position the NanoScope software changes the height of the piezoelectric motor accordingly to maintain a constant height. This is called constant force mode, and is used throughout this work. This mode is set to restore the original position of the laser on the photodiode. During this mode two quantities are recorded; the deflection of the laser and the height moved by the stage. This gives information about the friction between the tip and the sample, and the sample's surface morphology respectively. Deflection scans are mainly used to give information about the friction of a surface and hence give better contrasts of smaller features which can be

observed, but height ranges cannot be evaluated from these scans. Therefore, lateral features are observable and are to scale in the x and y directions, but not the z direction (Figure 3.4). The samples were rastered at a scan rate of 1 Hz.

3.3 Differential Interference Contrast Microscopy (DIC)

DIC microscopy (or Nomarski microscopy) allows smaller surface features to be observed with a greater contrast and resolution than in conventional optical microscopy. DIC microscopy also allows fast observation of the surface of the wafer which can only provide non-quantitative information.

Samples were subjected to a selective chemical etchant to reveal dislocations (Section 3.5) and were imaged using DIC to calculate the threading dislocation density (TDD) from the average number of etch pits per image area. A Reichart-Jung DIC microscope with an attached CCD camera was used in this study. The typical operation of a general DIC microscope is described below.

A schematic of a typical DIC microscope is shown in Figure 3.5. The light from the source is first collimated and then polarised before entering the microscope system. After the initial polarisation the beam is reflected off a half mirror and passed through the Wollaston prism which splits the beam into two perpendicularly polarised beams.

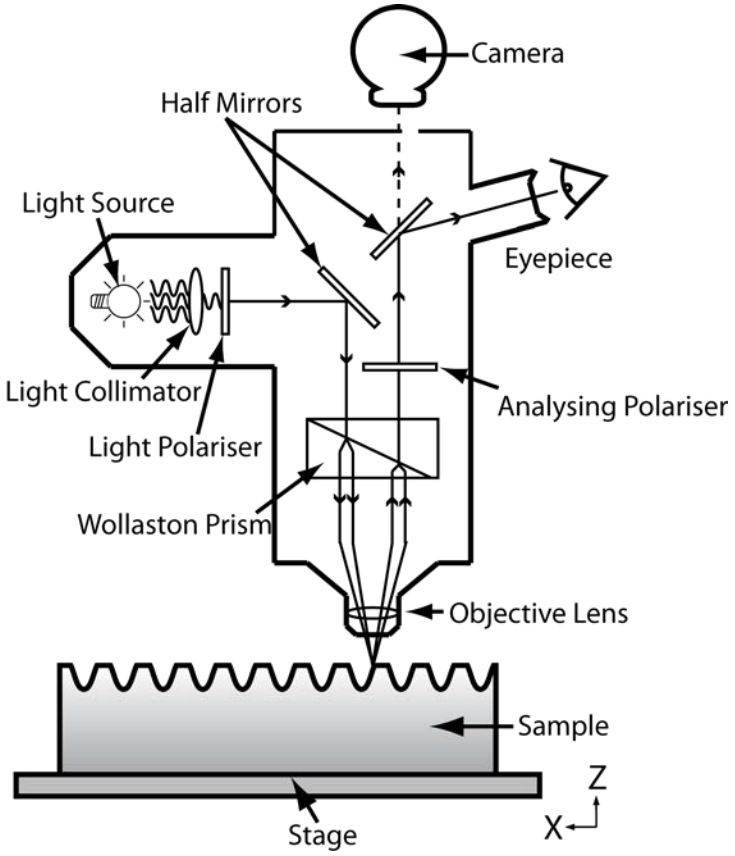

Figure 3.5: A schematic of a typical DIC microscope. Adapted from Nash [39].

This further polarisation prevents interference between the beams as they are then both focussed on the sample surface by an objective lens. Once the beams are reflected back from the sample to the objective lens they are then re-combined by the Wollaston prism and pass through an analysing polariser. This polariser is parallel when compared to the initial polariser. If a small feature on the surface is present then differing levels of interference will occur between the beams due to the path difference of the height of the feature, and the beams will recombine with a phase difference. This gives a bright field image in either the eyepiece or camera. The images recorded from the digital CCD camera are then digitally analysed.

3.4 High Resolution X-Ray Diffractometry (HR-XRD)

XRD allows the in-plane and out-of-plane lattice parameters of a crystal structure to be determined. Within a SiGe system the Ge composition and relaxation of buffers can be calculated if these lattice parameters are known. In this study a Phillips PW1835 high resolution diffractometer was used to produce reciprocal space maps from which the in-plane and out-of-plane lattice parameters can be calculated.

Figure 3.6 shows a schematic representation of the XRD system used in this study. The XRD system consists of three main parts, the x-ray source, the sample stage and the detector. A high power copper source was used which was operated at 40 kV and 40 mA, to produce the CuKα_1 wavelength (1.5406 Å). This beam was then passed through a hybrid Ge crystal monochromator and a collimating slit to produce a high intensity monochromatic x-ray beam. Once the x-rays are diffracted through the sample a collimating slit and monochromator on the detector serve to ensure that only x-rays which have been diffracted are counted, and not background x-rays. The counts per second (cps) of any diffracted x-rays are recorded.

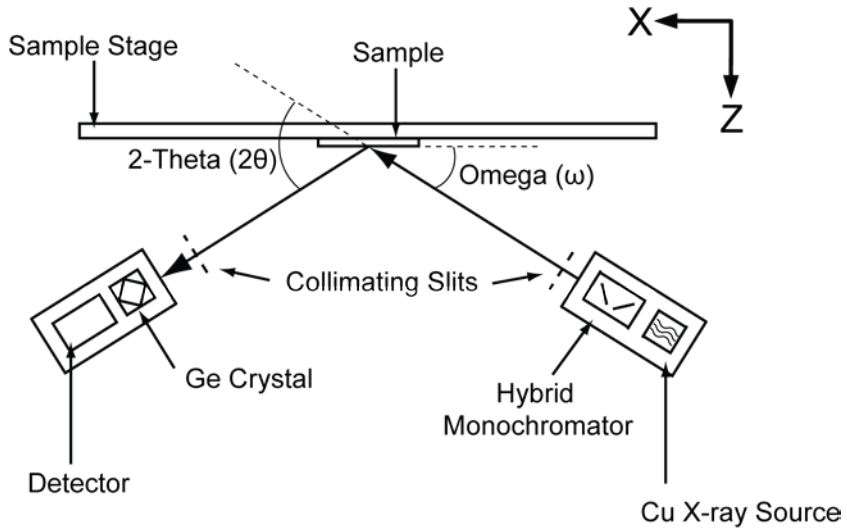

Figure 3.6: A schematic of the XRD system used in this study.

As the high intensity monochromatic collimated x-ray beam approaches the sample, the stage is orientated in five axes of freedom, as shown in Figure 3.7. The x, y and z correspond to the placement of the sample within the beam to ensure the highest possible diffraction count and have a resolution of 0.01 mm. The other two degrees of freedom are the rotation, phi (φ), and the tilt of the sample, psi (ψ) which are controlled to within 0.01°. These angles allow the rotation of the sample so that the intended diffraction plan is reached, as shown in Figure 3.7.

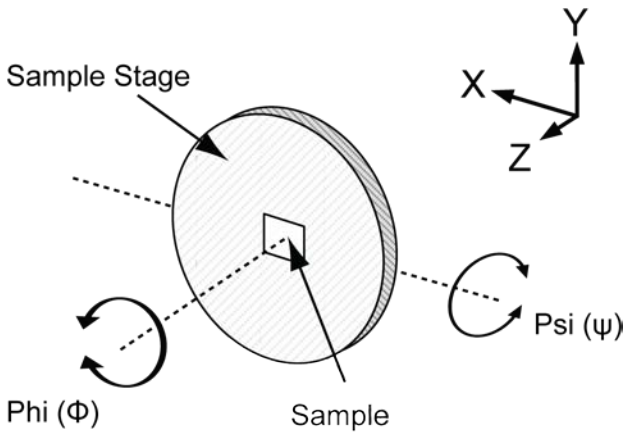

Figure 3.7: A schematic of the degrees of freedom that the diffracting stage was able to achieve.

Omega (ω) is the angle between the incident x-ray beam and the sample (001) crystal plane and 2theta (2θ) is the angle between the incident beam and the diffracted beam (Figure 3.6) and are controlled to a resolution of 0.0001°. Moving both these angles together produces an angle ratio omega-2theta (ω/2θ). The effect of moving ω/2θ is that the detector moves twice as fast as the stage to maintain the ω/2θ ratio. A rocking curve (RC) is measured when ω is kept constant and ω/2θ is scanned around a specified reflection. A reciprocal space map (RSM) is built by a series of rocking curves with different ω values which is then converted to reciprocal space by the corresponding software, PANalytical X'Pert Epitaxy.

3.4.1 Reciprocal Space Maps

A reciprocal space map is made up of a series of points, each of which represents different planes of a crystal lattice as defined by their surface normal vectors. Accessible reflections are limited by two physical factors, the x-ray wavelength and the incident angle (ω). The system cannot scan planes with an ω/2θ value beyond 2/λ, this is shown in Figure 3.8. The system also cannot scan planes for which the incidence angle cannot reach the intended planes (i.e., where $\omega<0$ or $\omega>2\theta$). A schematic of all the accessible reflections is shown in Figure 3.8 along with the physical scanning directions ω and 2θ.

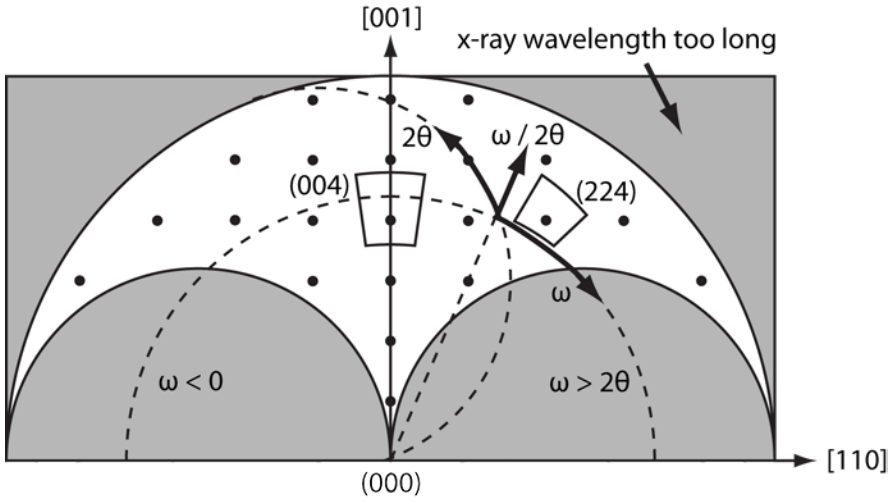

Figure 3.8: A schematic of the reciprocal space points which correspond to all the accessible different planes in a (001) orientated crystal lattice. The physical axes are shown along with the [004] and the [224] RSM points. Adapted from Bowen [104].

The relaxation and composition of a SiGe alloy layer can be calculated by the out-of-plane lattice parameter, a_z, and the in-plane lattice parameter, a_x, as described by Equation 2.9 and Equation 2.11. The layers can be tilted when compared to the Si (001) substrate due to material properties [105] or growth conditions [106], a schematic representation of this is shown in Figure 3.9a).

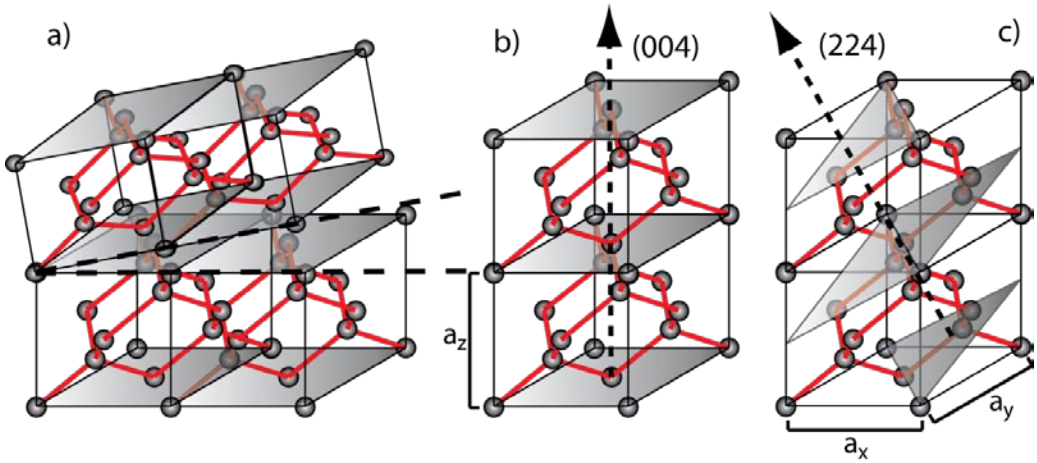

Figure 3.9: Crystal planes analysed by XRD. a) shows how the epitaxial layer can be tilted, b) shows the set of planes analysed by the (004) RSM and points out the out-of-plane lattice parameter. c) shows the (224) planes and the in-plane lattice parameter. The vectors shown are the surface normal vectors.

If no tilt occurs within the layers and the composition is known then a_z can be calculated solely from a (004) rocking curve. In this situation a_x can be calculated from a_z through Possions ratio (Equation 2.9) and therefore relaxation can be calculated. If a tilted layer of a random constant composition SiGe alloy is analysed, a_z can be derived from a symmetric (004) RSM together with the tilt of the layer. An asymmetric (224) RSM can then be used calculate a_x. These planes are shown schematically in Figure 3.9b) and Figure 3.9c). When a_x and a_z are known the composition of the layer can be determined. The perpendicular in-plane lattice parameters (a_x, a_y) are assumed to be equal due to general bi-axial relaxation. RSM positions of the (004) and (224) reflections are shown in comparison to all other reflections of a (001) orientated crystal in Figure 3.8. For in-depth calculations of lattice parameters from RSMs see Capewell [52].

3.4.2 Interpretation of Reciprocal Space Maps

Figure 3.10 shows the position of intensity peaks (represented by circles) of a typical SiGe system within the (004) and (224) RSMs. The effect of increasing a_z and a_x is shown to result in a vertical and horizontal shift of the peak position respectively. When a layer is fully relaxed its associated (224) peaks will lie on the [224] vector that is shown. If a peak lies to the left of the [224] vector it is under biaxial tensile strain i.e. a_x is larger and a_z is smaller than in the relaxed crystal of the same composition. Similarly it is under biaxial compressive strain when to the right of the [224] vector.

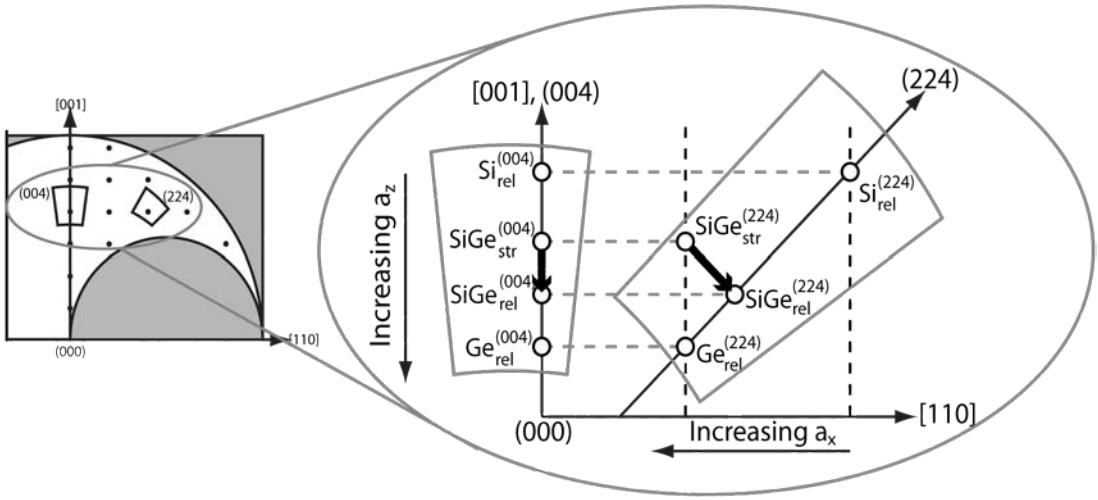

Figure 3.10: A magnification of the (004) and the (224) RSMs. Shown are the relevant intensity peaks of silicon, germanium and a generic SiGe alloy. Also shown are the positions of the fully SiGe layer when fully strained on a relaxed Ge layer. The movement of the SiGe peak as relaxation occurs is also shown. Adapted from Bowen [104].

The typical peaks associated with a reverse graded virtual substrate are the Si (001) substrate, the relaxed Ge underlayer and the SiGe constant composition cap. Figure 3.10 shows the peak positions of a fully *relaxed* Ge layer ($Ge_{rel}^{(004)}$ and $Ge_{rel}^{(224)}$) when compared to the Si substrate ($Si_{rel}^{(004)}$ and $Si_{rel}^{(224)}$). A general high composition relaxed SiGe alloy layer is also shown ($SiGe_{rel}^{(004)}$ and $SiGe_{rel}^{(224)}$). If the Ge composition of the SiGe layer is decreased the peaks of the relaxed SiGe layer would move closer to the Si peak.

If the SiGe alloy layer is fully strained on the relaxed Ge layer its a_x will be equal to that of the Ge layer. The peak shift associated with relaxation of a tensile *strained* SiGe alloy peak ($SiGe_{str}^{(004)}$ and $SiGe_{str}^{(224)}$) on a relaxed Ge layer is shown in Figure 3.10 with a black arrow. The movement of the (004) strained and relaxed SiGe peaks as relaxation occurs are explained by the tetragonal distortion of the lattice. As the vertical component of the (224) SiGe peak shift can be determined from the (004)

SiGe peak shift the horizontal component can be determined, allowing the shift in a_x to be determined. However, if neither the degree of relaxation nor alloy composition are known the full (224) RSM must be used. Traditionally, the *relative* position of these peaks compared to the *Si substrate peaks* allows determination of the relaxation and composition of a layer. However, for this work the *relative* position of the SiGe peaks compared to the *Ge peak* is used to calculate relaxation.

A high misfit dislocation density can create a distortion of the intensity peaks which can reduce the resolution of results and increase the experimental error. This distortion is a spreading of the peaks which is physically due to the periodic strain field which arises from small mono-crystalline blocks formed from the crossing of misfit dislocations, termed “mosaicity” [104]. The surface and interface roughness of each epitaxial layer also adds a general spreading of each peak long the omega direction. These effects can be seen from typical RSMs where the Si (001) substrate peak is very sharp indicating few defects, a high crystallinity and a smooth interface. Other peaks typically have distortion from defects and roughness. For a detailed account of other distortion effects see Bowen [104].

3.4.3 X-Ray Reflectivity (XRR)

XRR utilises the different refraction index of smooth layers (<5 nm RMS roughness) to calculate the layer thickness, roughness and density. In this study XRR is only used to calculate the thickness of thin (< 150 nm) layers.

XRR uses the same experimental equipment and setup as XRD as described previously. In XRR the source and detector angle to the surface of the sample are

equivalent so that $\theta = \omega$. This technique is also called grazing incidence reflectivity as the source and detector angles used are low (θ, $\omega < 1.5°$). When an XRR profile is obtained by scanning low angles the profile shows the response of the material during *specular* reflection to the normal of the sample surface. This technique uses *Snell's* law and is dependent upon the difference in density of a single layer and its substrate, unlike XRD which uses the crystal structure and *Bragg's* law. For the purposes of this study, knowledge of the composition of the layer from other techniques (i.e. XRD or SIMS) is required.

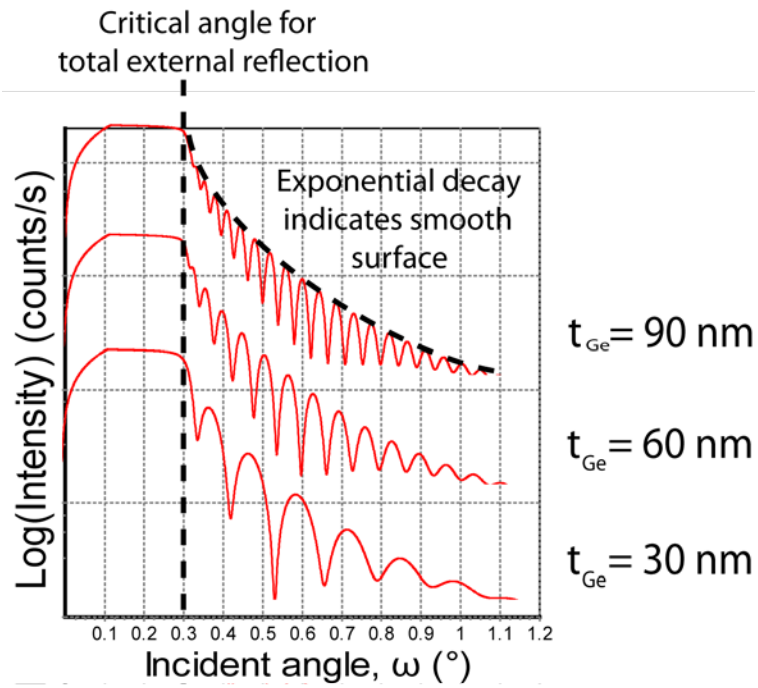

Figure 3.11: Examples of XRR simulations of a pure Ge layer upon a Si (001) substrate.

For the purposes of this description a single pure Ge layer upon a Si (001) structure will be used. As the scan is started from 0° to the *total external reflection* the x-ray signal is not able to penetrate the sample surface. Above this angle the signal is able to penetrate the material and the penetration depth increases rapidly with angle and the signal is absorbed within the layer. Above the total external reflection angle, the

incident beam is reflected from the Ge/Si(001) interface towards the surface of the sample. This signal may again be re-reflected towards the Ge/Si(001) interface. Figure 3.11 shows three example curves of simulated XRR profiles for a pure Ge layer on a Si(001) substrate as the layer thickness is increased. As the thickness of the layer is increased the frequency of oscillations increases and the spacing between fringes decreases along with their amplitudes, this spacing is used to calculate the thickness of the layer. The exponential decay of the overall profile shows a smooth sample surface, a rough surface will decrease the reflected signal and change the envelope of the overall oscillations. After an angle of approximately 1.5° no reflected intensity can be detected. The PANalytical X'Pert Reflectivity program is used in this study to fit the measured results to simulations to obtain layer thicknesses.

3.5 Selective Defect Etching

Defect etching allows the threading dislocation density (TDD) to be calculated. TDD is an important value as it directly affects all other qualities of the buffer (Section 2.6). Schimmel etchant has been used as a standard etchant for many years [107] to reveal dislocations in low Ge composition SiGe buffers. However, as the Ge composition increases in SiGe layers the reactivity of the etchant decreases and has no effect on pure Ge [37]. An Iodine based etchant has been used in recent years to reveal dislocations in pure Ge and has yielded much faster etch rates [108]. In this study it is shown that for high composition layers ($x > 0.75$) the dislocation selectivity of both Schimmel and Iodine etchant are similar. Iodine etchant is used to reveal dislocations in reverse graded buffers.

Selective defect etchants are defined as etchants which chemically etch the epitaxial material at a constant macroscopic etch rate, but, in the presence of a threading dislocation increase their local etch rate [109]. This mechanism creates a pit around the dislocation which can be viewed through a DIC microscope. These pits can then be counted and an etch pit density (EPD) can be calculated which represents the TDD of a layer. Many different selective etchants have been developed for use in TDD characterisation [110], but all lose reactivity as Ge composition is increased within SiGe buffers. All selective etchants, including the iodine etch, work under the same general principle by continual surface oxidisation and removal of the oxide from the surface [109].

Macroscopic etch rates were determined by measuring the thickness of material removed by etching. This consisted of selectively etching a sample that had half of the surface covered with chemically resistive Apiezon W black wax. All chemical work including etching and wax application was performed in a stable environment with an air flow stabilised temperature of 19±1°C. After the allotted time in the etchant all samples were subjected to a “hard” and “soft” deionised (DI) water rinse to remove all traces of etchant on the sample. The wax then removed by dissolving the compound with toluene and then allowing the toluene to evaporate in a fume cupboard. Once the wax had been removed from the selectively etched sample a step is revealed between the etched and unetched regions. This step was then measured by a Talystep line profiler with a vertical resolution of 10 nm

To determine TDD levels within a wafer a sample was cleaved and subjected to selective etching. The sample was then viewed though DIC microscopy and a

selection of 30 random images were recorded and an average TDD was determined from the average EPD of the images.

3.5.1 Dilute Schimmel Etchant

The *diluted* Schimmel etchant used for selectivity comparisons is chromium based. The etchant consisted of CrO_3 (0.75M) : HF (50%) : H_2O mixed with respective ratios of 2 : 4 : 3 [111]. The oxidising agent within this chemical formula is the chromium oxide (CrO_3) and was added to the formula in powder form. The oxide removal was accomplished by the hydrofluoric acid (HF), and the etch rate was controlled by the ratio of water added.

3.5.2 Dilute Iodine Etchant

An iodine etchant comprised of a HF : HNO_3 : CH_3COOH solution in the volume ratio 5:10:11 with 30 mg iodine dissolved per 26 ml solution [112]. This solution was found to etch the layers too aggressively and was diluted with DI water in the ratio 3:1. This diluted iodine etchant had two oxidising agents, the nitric acid (HNO_3) which was a general oxidising agent, and the dissolved iodine which allowed the reaction process to be reaction controlled and turn the etch into a selective process [109]. The oxide was removed by the hydrofluoric acid (HF), the rate of which was controlled by dilution of the etchant with acetic acid and DI water.

3.5.3 Comparison of Etchants on High Composition SiGe Layers

As iodine etchant has not previously been used for EPD measurements in high composition SiGe layers it is necessary to compare the selectivity and etch rates of the etchants with a standard selective chemical etchant, which is Schimmel in this section. Figure 3.14 shows the measured etch rates for high composition (Ge % > 75 %) SiGe alloy layers for Schimmel etchant and Iodine etchant. The Schimmel etch rate was observed by Parsons [37] to decrease approximately logarithmically when the Ge composition was increased from 20% to 100%. For more information on the Schimmel etch rates of *low* composition SiGe layers see Parsons [37].

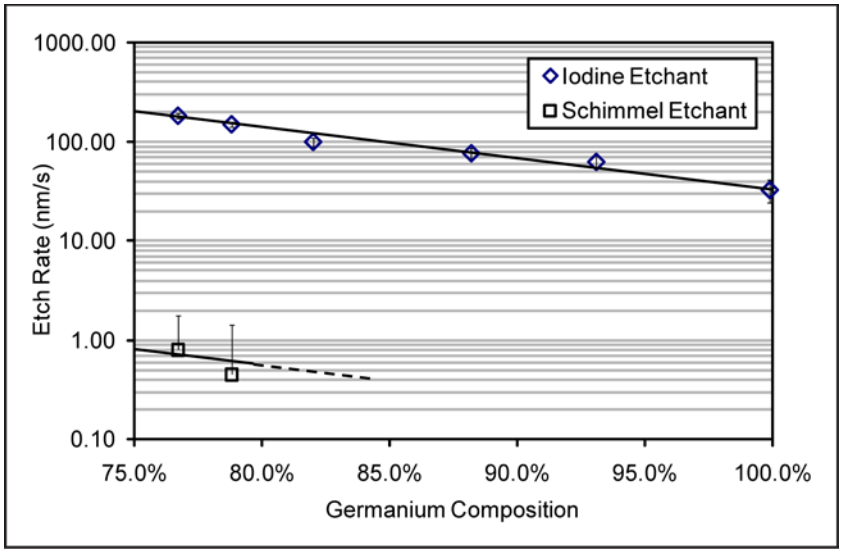

Figure 3.12: The measured etch rates of high composition SiGe layers. Shown are the diluted Schimmel etchant and the 3:1 diluted iodine etchant. Experimental data was measured by John Adams.

XRD measurements confirmed a Ge composition of 78.8 % for the top layer of the sample that was used for etching comparison trials. The Schimmel etch rate of layers above a Ge composition of 78.8 % was too low to be accurately measured. Schimmel

etchant was measured with a macroscopic etch rate of 0.45 nm s^{-1} and the sample revealed an EPD level of (2.3±0.4) x 10^6 cm^{-2}.

Iodine etchant shows a logarithmic decrease in etch rate as the Ge composition is increased from 78.8 % to 100 % Ge. However, the iodine etch rate is still over two orders of magnitude larger than found for Schimmel etchant. When the comparison sample is subjected to a diluted iodine etchant an etch rate of 154 nm s^{-1} and an EPD of (2.6±0.4) x 10^6 cm^{-2} is found. Clearly the EPD revealed by the Iodine and Schimmel etchants agree to within the experimental uncertainty, ±10 %. The selectivity ratio between etchants can be defined as:

$$Selectivity = \frac{EPD_{Iodine}}{EPD_{Schimmel}} \qquad \textbf{Equation 3.1}$$

When other samples of lower composition are compared the selectivity between both etchants averages to 1.001 indicating that both etchants reveal dislocations as well as each other. Figure 3.15 shows two DIC Nomarski photos of the comparison sample surface after etching in a) Schimmel for 5 mins and b) Iodine after etching for 5 seconds. The etch pits created by the Schimmel etchant are seen to be larger than those created by the iodine etchant. This is thought to be due the macroscopic lateral etching of the pit once it is formed and subsequently longer etch time the sample is exposed to.

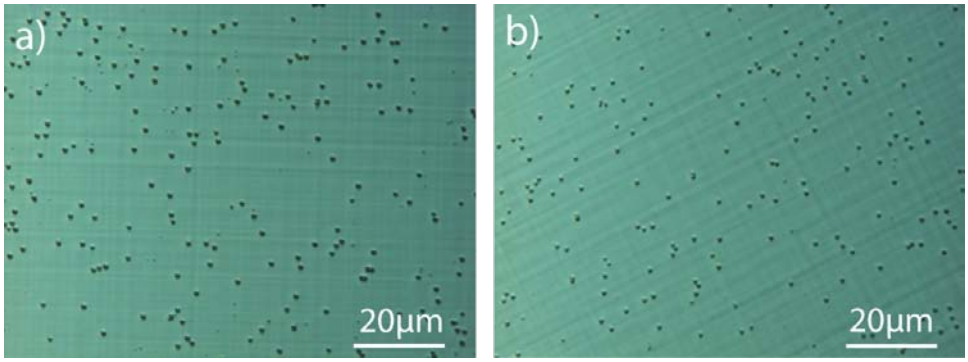

Figure 3.13: The surface of the 78.8 % Ge comparison sample after etching in a) Schimmel for 5 minutes and b) Iodine for 5 seconds. The features that can be seen are the etch pits created by threading dislocations.

An initial investigation of the comparisons between the Schimmel and Iodine etchants has been presented and it is shown that both etchants have similar selectivity. A longer study of the differences between the etchants could prove useful, but this is beyond the scope of this investigation.

To ensure that iodine etched samples with high dislocation content and hence high etch pit densities as shown in Figure 3.12a) were analysed sufficiently, the Adobe® Photoshop® software package was utilised to count the etch pits automatically. The Nomarski image from the etched sample was first transformed into a two colour (black and white) image by utilising a threshold filter, an example of the throughput image is shown in Figure 3.12b). The number of isolated groups of black pixels is then counted automatically by the program. By adjusting the threshold filter for each sample the surface roughness is not transformed along with the etch pits thus avoiding any distortion of the results. The TDD calculated from the automatic counting process for the sample shown in Figure 3.12 was calculated to be $(1.3\pm0.1) \times 10^{8}$ cm^{-2}.

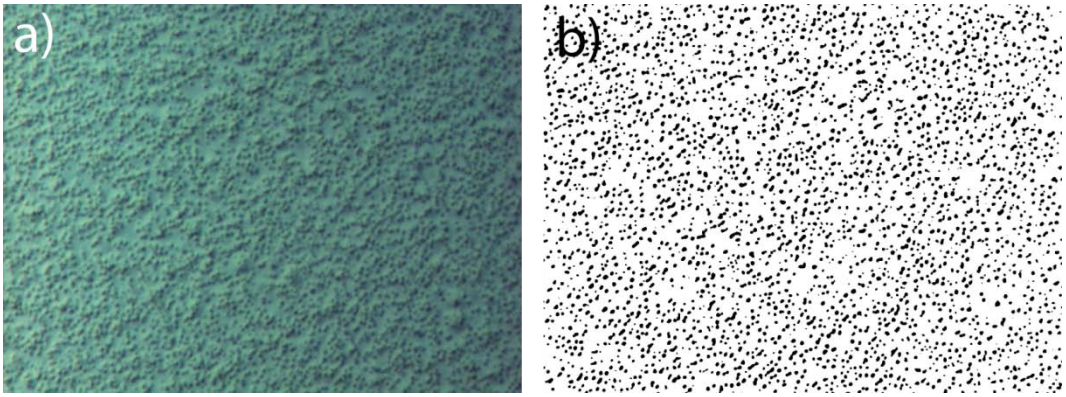

Figure 3.14: a) An iodine etched sample with a dense number of etch pits corresponding to a high density of threading dislocations, b) the transformed image using the threshold technique to convert pits into black dots. The Adobe® Photoshop® software package is then used to automatically count the number of dots.

The same sample was then viewed through plan view TEM (PVTEM) to ensure the defect level was accurately measured by the automated process. A micrograph of the PVTEM is shown in Figure 3.13 where examples of the threading dislocations are highlighted; all other lines in the micrograph are microscopy aberrations due to the inhomogeneous strain field in the sample.

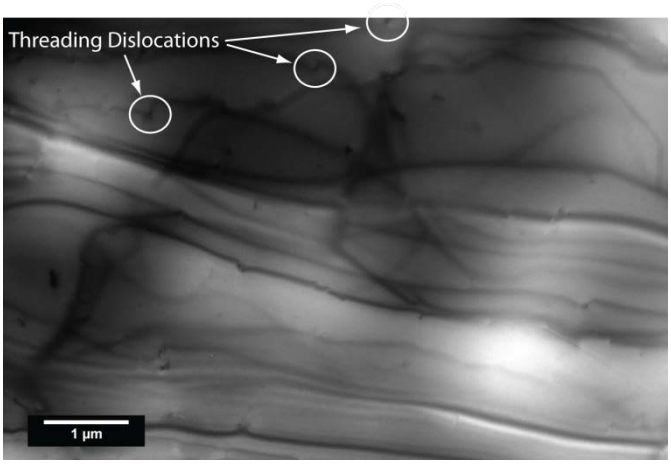

Figure 3.15: Plan-view TEM of the etched sample shown in Figure 3.12. Circled features are threading dislocations and the lines which are observed in the micrograph are microscopy aberrations due to the inhomogeneous strain field in the sample.

The TDD measured from PVTEM observation was calculated to be $(1.3\pm0.2) \times 10^{8}$ cm^{-2} which is equivalent to the level measured by the EPD automatic counting process. It should be noted that the error in measurement for observation through PVTEM is larger than the error when measurements are made through Nomarski observation as smaller areas are observable.

3.6 Secondary Ion Mass Spectroscopy (SIMS)

SIMS allows a profile of the material composition to be determined as a function of depth. The composition profile of buffers within this study is required to confirm the intended structures were grown. Growth side effects like diffusion or segregation can also be seen within profiles and additionally the thickness of layers can be confirmed.

High and low energy SIMS have been utilised in this study. High energy SIMS was performed by a Cameca 4F secondary ion mass spectrometer with a caesium (Cs^{+}) ion beam of energy 14.5 keV, which provides resolutions of approximately 5 nm. The High energy SIMS utilised in this study was performed by Dr. Andrew Simons within the Advanced Analytics at QinetiQ Ltd. Low energy SIMS was performed by an Atomika 4500 SIMS profilometer with a 500 eV oxygen (O_2^{+}) ion beam which provides sub-nanometre resolutions. The low energy SIMS was performed by Dr. Richard Morris within the Analytical Science Projects group at the University of Warwick.

SIMS is performed by irradiating the surface of the sample with an ion beam which is sufficiently energetic to ionize the surface atoms of the buffer. The ion beam is

directed at a normal incidence to the surface and scanned over an area of 250 μm^2. Once *secondary* ions are sputtered off the surface they are detected by a quadruple mass spectrometer (QMS). This analyses the current density produced by the sputtered ions and determines their chemical species and concentration. As ions are sputtered off the surface a crater is formed, which can then be analysed by a line profiler to determine the crater depth and therefore the erosion rate. From the erosion rate, the current density and the ion concentration a composition profile as a function of depth can be determined [113]. High energy SIMS ion sources generally give higher erosion rates than lower energy ion sources [113] and therefore a lower resolution (Figure 4.8). However, higher erosion rates also allow thicker layers to be practically scanned. Therefore low energy SIMS has been used to profile thinner layers with a higher resolution, but thicker layers are profiled with higher energy SIMS.

Other factors which limit the resolution of SIMS are the TDD, surface RMS roughness, chemical reactions [114] of incident ions interacting with surface atoms and intermixing of incident ions. The surface roughness can cause a shadowing or deflection of the sputtered ions which can limit the secondary ions reaching the QMS and distort results. Dislocations can cause preferential etching at the surface which will distort the erosion rate measured from the crater which is created by the incident ion beam. Chemical reactions of incident ions can also change the concentration of the sputtered ions and reduce the erosion rate which can broaden the SIMS profile [114]. Finally, intermixing of incident ions occurs when the incident ion beam pushes surface atoms further into the samples which are then sputtered as secondary ions later on, this again causes a broadening of the SIMS profile [115].

4 $Si_{0.2}Ge_{0.8}$ Relaxed Reverse Graded Strain Buffers

4.1 Introduction

A novel adaptation of forming high Ge content buffers is proposed and explored. Results are presented within this chapter from a succession of characterisation techniques for linear and terrace reverse graded buffers. As mentioned previously in Section 2.6 the requirements for a commercially viable virtual substrate are: low RMS surface roughness to the order of a nanometre, full relaxation in excess of 95 % and a threading dislocation density $< 10^7$ cm^{-2} for majority carrier devices and a value of $< 10^4$ cm^{-2} for minority carrier devices [41].

Fitzgerald *et al* [97] & [44] have shown threading dislocation densities of 10^5-10^7 cm^{-2} for forward graded structures (Section 2.6.3). However, when high Ge compositions are involved large thicknesses and longer associated growth times are required. If thinner structures are designed without losing final buffer quality then processing of devices could be faster leading to increased throughput in production. It will be shown that reverse graded buffers demonstrate significant quality enhancements which lead to low defect, smooth and significantly reduced thickness buffers when compared to forward grading.

Within this chapter all grading rates are presented as positive values to demonstrate their magnitude rather than emphasise the grading direction. To the author's knowledge this particular adaptation on reverse grading fabrication has not been demonstrated elsewhere.

4.2 Reverse Graded Structures

Reverse grading is defined as an epitaxial graded layer where the Ge composition at the start of the grade is higher than at the end (Section 2.6.10). It is termed "reverse grading" in contrast to the usual practice of starting from Si and slowly increasing the Ge content in a "forward" graded buffer of SiGe. The novel idea of reverse grading has already been introduced by Liu *et al* [18], however, the reported work was based on "jump-grading" [58] from the Si (001) substrate. This involved growth of a higher composition ($x = 0.35$) at the substrate surface whilst lowering the composition through grading to a composition of $x = 0.14$. On these layers they subsequently deposited constant composition SiGe caps which ranged from $x = 0.14$-0.32, additionally adding another jump in composition. This resulted in homogenous nucleation of dislocations at certain interfaces. See Section 2.6.10 for a greater explanation of their work.

The proposed idea presented here is to begin with a relaxed layer of pure Ge and then to reverse grade down to a composition of $Si_{0.2}Ge_{0.8}$. The initiative behind this is so that a thinner high Ge composition graded buffer can be fabricated with a high epi-quality top layer. If a high constant composition ($x > 0.7$) $Si_{1x}Ge_x$ alloy layer was deposited directly on the Si substrate the layer would be subject to strain based surface segregation due to growth kinetics and the large misfit of $\varepsilon > 0.0293$. Additionally a large dislocation density would be present if the thickness of the layer was greater than the critical thickness due to homogeneous and heterogeneous nucleation (Section 2.6.1). A pure Ge layer deposited on the Si substrate immediately removes the segregation problem as there would be no mobile Si adatoms. Huang *et al* [94] report that when a high composition alloy is further deposited on a pure Ge

layer the amount of segregation would be partially decreased due to the smaller misfit between the Ge layer and high composition SiGe alloy layer. This would allow a wider range of parameters to be varied for growth of the graded region.

4.2.1 Design of Base Layer for Reverse Graded Structure

A high quality Ge layer which has already been developed directly on a Si substrate utilising the two step method by Colace *et al* [116] & [41] & [95] was reported in Section 2.6.8. This was used as the base underlying Ge layer for the experiment and is shown in Figure 4.1. The low temperature Ge layer was grown at 400°C under a pressure of 100 torr with a GeH_4 flow of 150 sccm, which was carried by 20 slm of H_2 at a nominal growth rate of 0.24 nm s^{-1}. The low deposition temperature is to ensure growth proceeds in a Frank-van der Merwe growth mode. HCl chamber etches are required to remove chamber deposition to retain calibration of the growth temperature. The wafer is removed from the chamber whilst the etching process is performed; see Section 2.2.4 for a greater explanation of chamber etching. No etch of the chamber was performed between the low and high temperature depositions as the temperature and associated growth rate is too small to cause significant deposition on the growth chamber wall and lead to a deviation in the growth kinetics.

The high temperature Ge layer was deposited with the same growth parameters at a temperature of 670°C at a nominal growth rate of 1.26 nm s^{-1}. Then the substrate was subject to an *in-situ* anneal of 830°C for 600 seconds under a hydrogen atmosphere and kept at the same pressure to allow glide and annihilation of threading arms. Finally an HCl etch is performed to remove any deposition from the growth chamber (Section 2.2.4). For the purpose of the reverse linear grade (RLG) investigation in

this chapter, this two temperature Ge base (or underlayer) was kept as a constant platform for the reverse grade buffers.

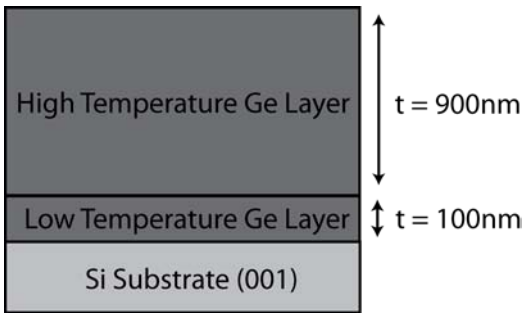

Figure 4.1: The base Ge layer on which the RLG has been based.

4.2.2 Base Layer Characteristics

A control sample consisting of the 1±0.05 µm Ge base layer was grown to determine the initial properties of the layer prior to design of the reverse graded regions. Figure 4.2 is a TEM micrograph (Section 3.1) and shows that within the Ge base layer, the initial 0.1±0.005 µm low temperature Ge layer seed has a high density of dislocations, whilst the 0.9±0.05 µm high temperature layer is seen to have no visible dislocations in the TEM photo indicating a TDD of less than $5\pm0.5 \times 10^{7}$ cm^{-2}. The characteristics of the base Ge layer are; a threading dislocation density of $\sim2\pm0.2 \times 10^{7}$ cm^{-2} which was measured by selective etching (Section 3.5) and DIC microscopy (Section 3.3) by an average of etch pit density in 30 images. A roughness of 0.7±0.1 nm was measured by AFM (Section 3.2) from an average of eight 10 µm x 10 µm scans. A tensile strain of 104.2±0.5 % was measured by XRD RSMs (Section 3.4) and is attributed to the difference in thermal expansion coefficients (see Section 2.5.4).

Figure 4.2: A cross sectional TEM micrograph of the control 1 µm Ge underlayer. Note that the low temperature seed contains a high density of dislocations.

4.2.3 Design of Reverse Linear Grade

Initially, the Ge fraction x in the reverse linear graded (RLG) layer was calibrated to decrease from the pure Ge underlayer (x = 1.0) to a composition of x = 0.8 over a 1 µm thickness, which corresponds to a grading rate of 20 % μm^{-1}. Growth of *forward* graded buffers generally occurs by keeping the SiH_2Cl_2 constant and varying the GeH_4 flow. As two precursors with different growth regimes (Section 2.2.3) were used the overall growth rate can be considered as a product of their individual growth rates. At the growth temperature of 850°C the growth rate of the SiH_2Cl_2 precursor is *temperature dependant* and the GeH_4 precursor is *flow dependant*. Therefore minimal control of the total growth rate would be achieved if the GeH_4 flow was increased. By considering the mass-flow of growth [30], the growth rate can be controlled by setting a constant GeH_4 flow and increasing the flow of SiH_2Cl_2 linearly. This allows control of the SiH_2Cl_2 growth rate and hence

the overall Si composition of the layer to achieve the reverse graded region in small 5 % Ge composition steps.

Figure 4.3 shows the overall design of the calibrated RLG buffer. The growth parameters used are shown in Section 4.2.5. After the graded region was deposited a chamber etch was performed to remove any chamber deposition caused by the high temperature. Finally a constant composition cap at x = 0.8 was deposited with the same growth parameters as the top of the graded region at a growth rate of 4.74 nm s^{-1} to achieve a 1 µm thick layer. To attain different reverse grading rates the time for each ramp was decreased linearly with desired thickness, with the assumption that average growth rate remained constant.

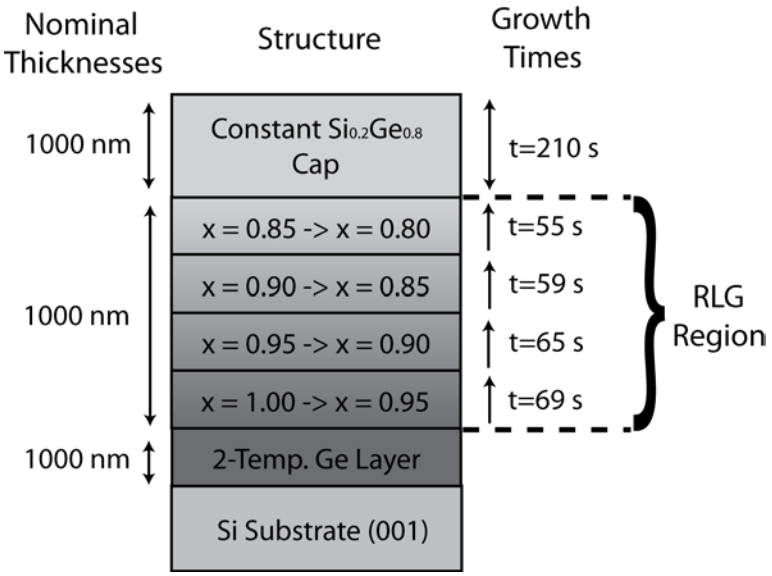

Figure 4.3: A schematic of the calibrated reverse linear graded structure, with grading rate 20 %/µm. Shown are the 5 % Ge steps the grade was split into. On the far left are the intended thicknesses and on the right is the growth times used for each step.

4.2.4 Design of Reverse Terrace Grade

The idea of terrace grading was proposed by Capewell *et al* [82] and was shown to generate smoother interfaces and hence enhance relaxation and lower TDD values by releasing pinned dislocations. The same principle was applied to the reversed graded buffer by growth of a series of the linear graded regions followed by constant composition layers. An initial reverse terrace graded (RTG) structure was grown and optimised for a 250 nm four terrace buffer which corresponds to an effective grading rate of 11±1 % μm^{-1}, as shown in Figure 4.4.

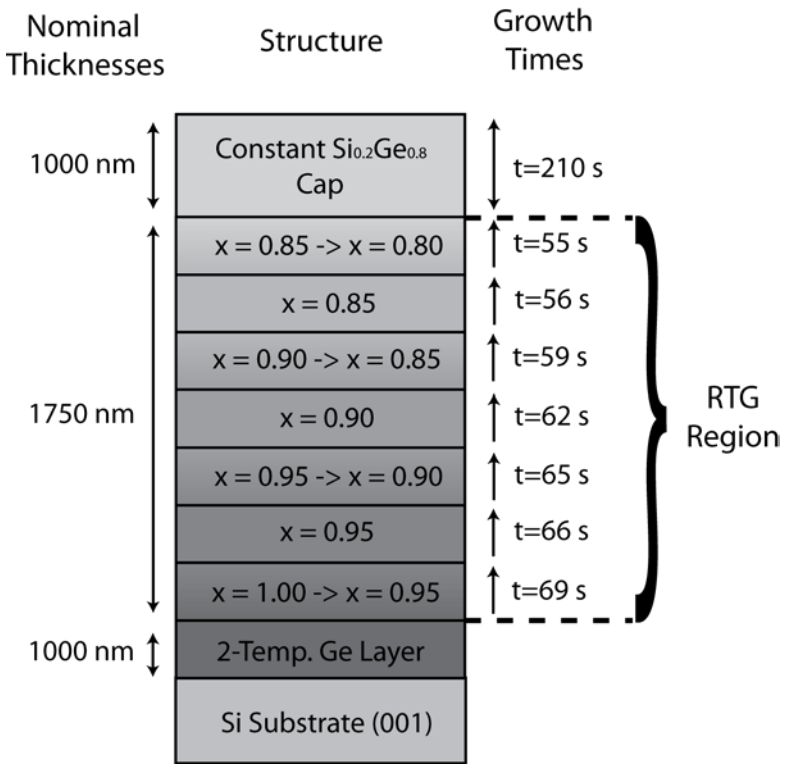

Figure 4.4: A schematic of the calibrated reverse terrace graded structure, with an effective grading rate of 11 % μm^{-1}. Shown are the 250 nm terraces used to separate the graded regions into 250 nm layers.

The calibrated RTG structure was achieved by inserting constant composition layers in-between 5 % Ge composition linear grade regions. The growth parameters are

mentioned in Section 4.2.5 and shown in Figure 4.5. All other growth parameters apart from SiH_2Cl_2 flow were kept constant.

In the rest of this chapter the RTG region is defined as the region from the top of the Ge base layer to the end of the final graded layer, as shown in Figure 4.4. This RTG region is varied to investigate the effect of changing the effective grading rate on roughness and dislocation density. The various thicknesses for each terrace and linear graded layer of the RTG region were achieved by linear interpolation of the deposition time for each layer. This action is assumed to have negligible effect on the nominal growth rates.

4.2.5 Growth Parameters

In this section the growth parameters for both the RLG and RTG structures are described. The growth temperature was set to 850±5°C throughout the graded region with the pressure reduced to 20 torr and the H_2 gas flow was kept constant at 20 slm. The SiH_2Cl_2 (DCS) flow rates and nominal growth rates for the calibrated RTG structures are shown in Figure 4.5. The same flow rates and nominal growth rates are used for the RLG structures with the exception that they contain no constant composition layers.

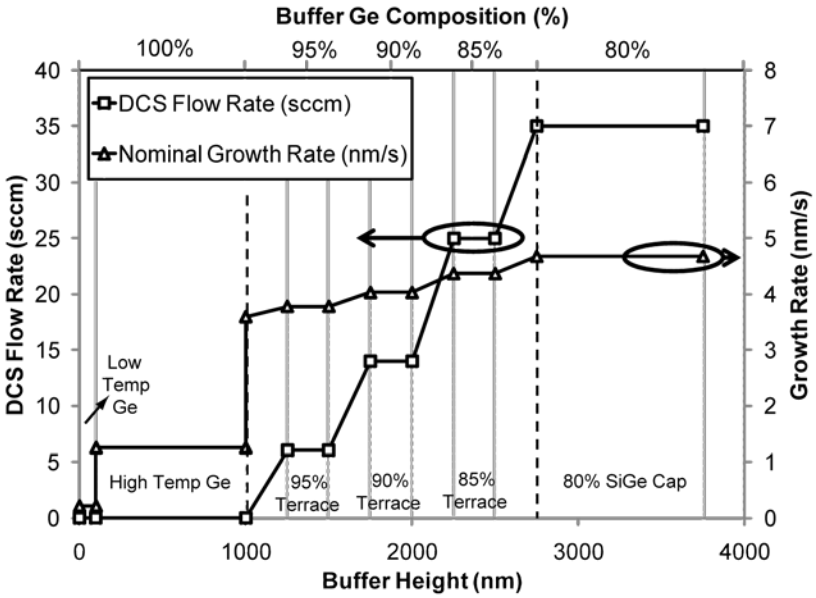

Figure 4.5: The DCS flow rates and nominal growth rates for the calibrated RTG structure. The shown values are the same for the RLG structure when the constant composition terraces are removed.

The growth rates shown are averages measured prior to the current investigation [31]. Growth of the graded layer is accomplished by linear ramping of the SiH_2Cl_2 precursor whilst keeping the GeH_4 precursor flow constant. As a result the growth rate increases linearly with precursor flow.

Within this study an HCl etch to remove chamber wall deposition was performed after the 1 µm Ge underlayer was deposited and again before deposition of the 1 µm $Si_{0.2}Ge_{0.8}$ constant composition cap. For thick graded layers the graded region growth process was interrupted after every 1 µm of growth on the substrate to perform an HCl additional etch. Unless otherwise stated, all anneals were performed *ex-situ*, after growth and in a ultra high vacuum (> 10^{-8} mbar).

4.3 Properties of Reverse Linear Graded (RLG) Buffers

In this section an investigation of the individual properties of relaxation, composition, defect densities and surface roughness of the RLG buffers and their interrelationship as a function of grading rate are reported.

For the purposes of this investigation, the Ge base layer which was reported in Section 4.2.1 will be referred to as the Ge underlayer, the graded region will be the RLG layer or RTG layer and the constant composition SiGe layer is referred to as the SiGe cap.

Unless otherwise stated or shown, the *experimental* errors of values which are characterised are; thicknesses are ±2 % of values given, compositions are reported to within ±0.005 and grading rates are calculated to ±1 % of values. *Note that grading rates for reverse graded buffers are shown as positive values for clarity.* Relaxation of the buffer is accurate to within ±0.005, root mean squared roughnesses are accurate up to ±0.2 nm and height ranges are within ±2 nm. Calculating defect density error is dependent on the area viewed and the density of the defects, but all the techniques and magnifications used for characterisation of defects in this study remain constant throughout. Therefore, unless otherwise stated, the error for threading dislocation density is to within ±10 % of value given, stacking fault densities are within ±5 % and due to the low densities of cracks which will be reported further on, crack densities are accurate to within ±25 %.

4.3.1 RLG Buffer Composition Profile

The thickness of each layer was confirmed through TEM observation and analysis. The overall thickness of each buffer, incorporating the Ge underlayer and the SiGe cap, was obtained in the (000) diffraction mode and defined from the Ge underlayer / Si(001) substrate interface to the surface of the sample. For this investigation the graded region is defined within the boundaries of the misfit dislocation network (Figure 4.6). This will give rise to a small experimental uncertainty, which could be quantified by performing a SIMS measurement on each sample, however, limited resources make this impractical for the current investigation.

A list of RLG samples and their graded layer thickness are given in Table 4.1 along with SiGe cap compositions and corresponding grading rates. Each sample composition was measured by HR-XRD RSMs, and an example of the dislocation network formed is shown in Figure 4.6. The grading rate (GR_{RLG}) for each sample is calculated by $GR_{RLG} = \frac{(composition - 1)}{layer\ thickness}$. An effective grading thickness of 10 nm was assigned to the sample with no graded region (sample 3695) as this the calculated diffusion length for a drop of 1% Ge composition in the Ge underlayer at a growth temperature of 850°C (see Mehrer [117]).

Wafer Number	Reverse Grading Thickness (±2 %) (nm)	Top Layer SiGe Composition (±0.005) (-)	Grading Rate (±1 %) (% μm^{-1})
4054	4594	0.785	4.69
4053	1885	0.786	11.4
4046	931	0.785	23.1
4050	736	0.787	29.0
4051	347	0.787	61.3
4128	193	0.759	124
4129	136	0.766	172
4052	117	0.797	174
4130	71	0.768	324
3695	10 (effective)	0.793	2069

Table 4.1: The RLG samples under investigation with the graded region thickness, top layer composition and corresponding grading rate. The grading layer thickness was measured from TEM photos. Compositions were calculated from XRD RSMs.

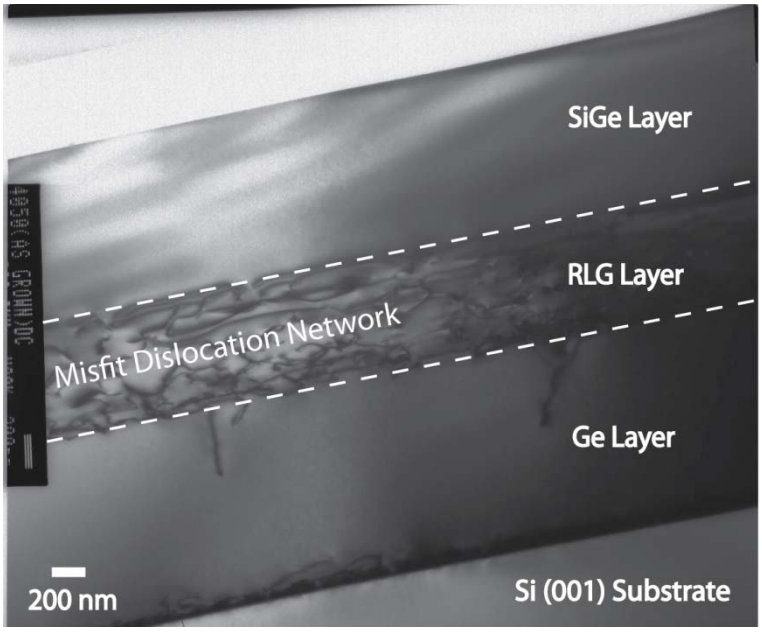

Figure 4.6: An example of an RLG structure sample 4050. Lines shown are only guides for the eye.

High energy SIMS using a caesium (Cs^+) ion beam with an energy of 14.5 keV was performed on samples 4050, 4046 and 4053 with RLG thicknesses (t_{RLG}) of 1885 nm, 931 nm and 736 nm respectively. Figure 4.7, Figure 4.8 and Figure 4.9 show TEM micrographs of these samples with their corresponding SIMS profiles. The SIMS profile shown in Figure 4.8 was measured more rapidly than the others

and shows random fluctuations of composition which is attributed to the measurement, rather than the growth technique. The linearity of the graded regions when analysed through SIMS gives coefficient of determination (r^2) values of ~0.995 indicating highly linear grading profiles. A composition drop within the Ge underlayer (effect number 2) is seen in all three samples and is observed to increase with graded layer thickness.

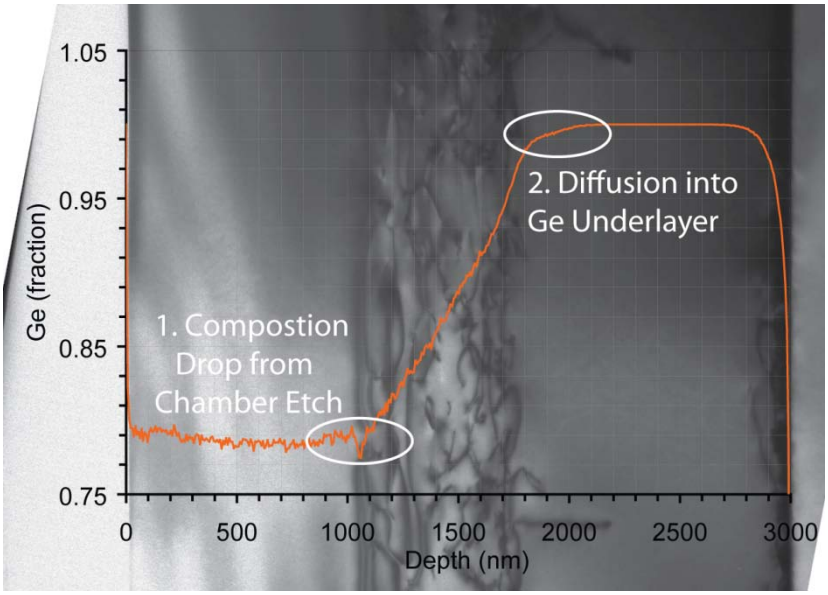

Figure 4.7: A SIMS profile over a TEM micrograph to show a profile comparison of sample 4050 with a linear graded region of thickness 736 nm with a grading rate of 29.0 % µm^{-1}.

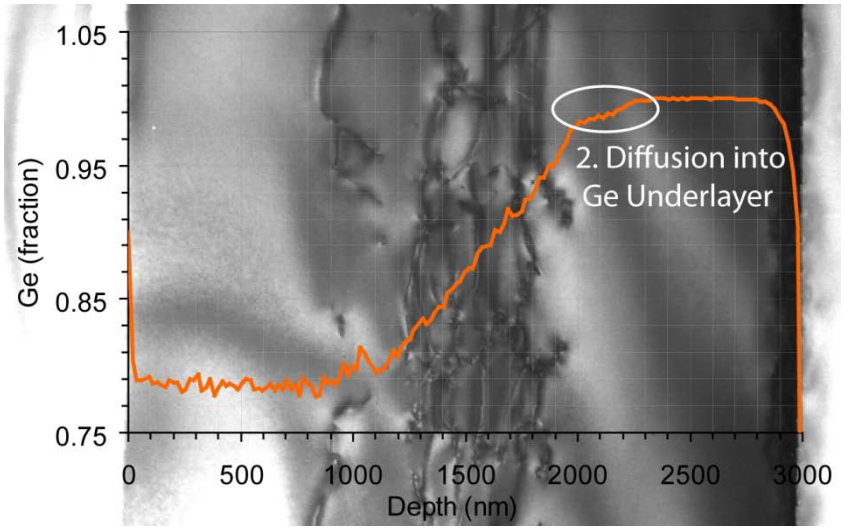

Figure 4.8: Composition profile of sample 4046 with a linear graded region of thickness 931 nm with a grading rate of 23.1 % µm^{-1}.

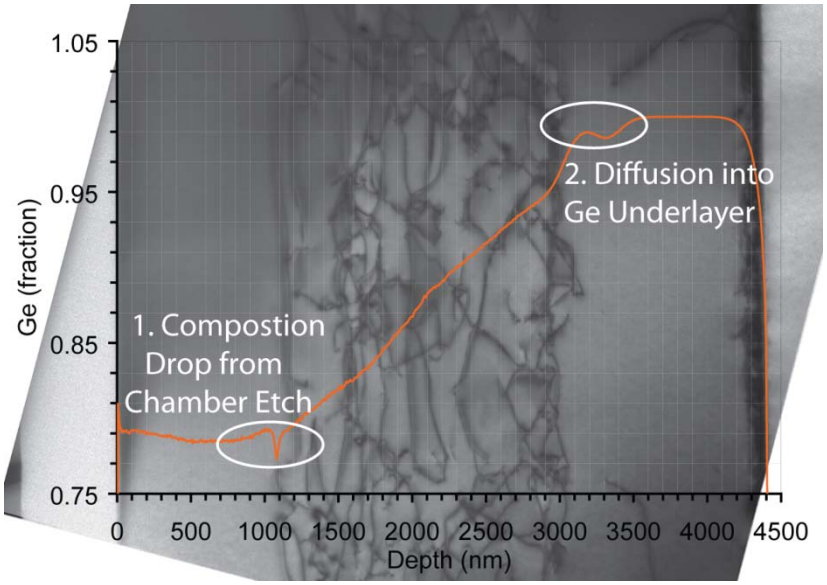

Figure 4.9: Composition profile of sample 4053 with a linear graded region of thickness 1885 nm with a grading rate of 11.4 % µm^{-1}.

Wafer Number (Figure)	Reverse Grading Thickness (±2 %) (nm)	Ge Composition Drop (±0.5) (%)	Distance of Composition Drop (±2 %) (nm)
4050 (Figure 4.7)	736	0.9	279
4046 (Figure 4.8)	931	1.7	329
4053 (Figure 4.9)	1885	1.0	424

Table 4.2: The measured Ge composition drop and distance over which the drop acts within the Ge underlayer labelled as composition drop 2 in Figure 4.7, Figure 4.8 and Figure 4.9, as measured by SIMS.

Table 4.2 shows the measured composition drop and the distances over which it occurs within the Ge underlayer for samples shown in Figure 4.7, Figure 4.8 and Figure 4.9. Within samples 4050 and 4046 the drop is linear. These drops in composition are speculated to be due to Si diffusion from the RLG region into the pure Ge underlayer [118].

Figure 4.9 shows a slightly different diffusion profile for sample 4053 where the drop is then followed by a rise in composition. This indicates that Si first diffuses into the Ge underlayer then a segregation process occurs. These diffusion and segregation effects are thought to be due to the high growth temperature of 850°C which is close to the melting point of pure Ge (See Table 2.1). When the reverse graded region is thicker the grading rates are lower, this means the surface of the buffer is kept at a higher Ge composition for a longer time during growth of the graded region. It is speculated that this is the main cause of enhanced diffusion, surface melting and segregation in the Ge underlayer.

The maximum observed composition drop due to diffusion or segregation of 1.7 % is equivalent to a misfit $\varepsilon = -0.0008$ when compared to the Ge underlayer. If the critical thickness for a constant composition layer with an equivalent misfit is found on Figure 2.14 the thickness required for glide of dislocations is 80nm and the thickness required for nucleation of dislocations is 32 µm. This shows that the composition drop into the Ge underlayer will induce dislocation glide and dislocations are unlikely to nucleate, and therefore will not have a significant effect on the TDD.

In all three samples for which composition profiles are presented two CVD chamber etches were performed within the growth. This leads to an inevitable change of the growth kinetics due to the control loop fluctuation (see Section 2.2.4). One of these etches was performed in-between the deposition of the Ge underlayer and the RLG layer and the other was performed in-between the RLG layer and SiGe cap. As the RLG/SiGe cap interface is grown at a higher temperature than the Ge underlayer a thicker chamber deposition occurs which will cause a larger reduction in growth temperature. When the deposition is removed, growth rate of the Si within the structure will increase as the SiH_2Cl_2 precursor is in a temperature limited growth mode. This results in a sudden decrease in Ge composition, which is rapidly quelled when the growth chamber is again coated with a few monolayers of deposition, resulting in an overall abrupt dip in composition. This is shown in the composition profiles of the uncalibrated structures (effect number 1 in Figure 4.7 and Figure 4.9) as dips of maximum 2 % over 110 nm. The associated misfit induces dislocation glide, but not nucleation of dislocations (Figure 2.14). The calibrated sample 4046 (Figure 4.8) was designed to have no mismatch at any interface. As the fluctuations in the profile shown are attributed to SIMS artifacts generated during the rapid measurement, it can be assumed that no composition drops occur during deposition.

The SIMS profiles in Figure 4.7, Figure 4.8 and Figure 4.9 were performed with a caesium (Cs^+) ion beam with a high energy of 14.5 keV, which allowed rapid lower vertical resolution measurements. With this SIMS technique, only the thicker RLG buffers could be analysed. Due to mass-flow considerations (Section 4.2.3) the thinner RLG buffers required profiling to ensure surface segregation was not a major effect and that a graded region was actually achieved. An oxygen (O^+) ion beam of a

lower energy (500 eV) was used to profile these buffers, the result of which is shown in Figure 4.10.

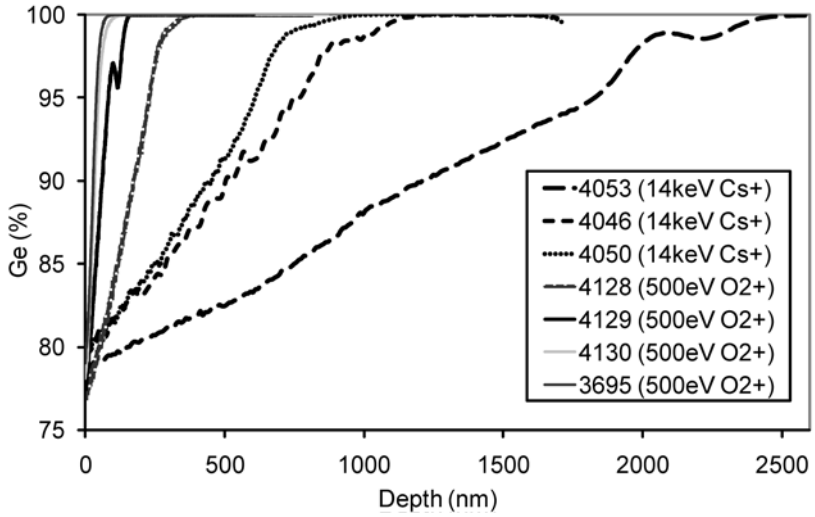

Figure 4.10: A comparison of all SIMS profiles for the RLG buffer samples. The depth shown is from the SiGe cap / RLG interface. The effect of diffusion can be seen to increase as buffer thickness is increased. Low energy SIMS measured by Dr. R. Morris. High energy SIMS measured by Dr. A. Simons.

Figure 4.10 shows the Ge profile taken from the SiGe cap / RLG interface into the Ge underlayer. Lower energy SIMS indicates the high linearity of the profiles and the extent of the diffusion at the RLG / Ge underlayer interface. The composition drop due to diffusion within the thinner graded layers is less than that of the thicker layers and is again found to be insignificant in terms of strain, only to induce dislocation glide. The anomalous drop in composition within sample 4129 (Figure 4.10) is speculated to be an effect of surface segregation where the high rate of increase of SiH_2Cl_2 precursor flow does not allow Si adatom incorporation. However, this effect is only seen to occur for a maximum of 0.5 % Ge over 10 nm and the misfit caused is insignificant in terms of affecting dislocation glide.

4.3.2 Surface Roughness of RLG Buffers

The surface roughness of the reverse graded buffers is determined from an average of eight 10 µm x 10 µm scans. The root-mean-squared (RMS) surface roughness and the height range are reported. The two-temperature Ge underlayer on which the graded layer is grown has been measured to have a RMS surface roughness of 0.7 nm and a height range of 6.2 nm.

Figure 4.11 and Figure 4.12 shows the measured RMS surface roughness and the height range respectively of the buffer with a variation in GR_{RLG}. Also shown is the Ge underlayer roughness which is represented by the horizontal grey line. Two different modes of growth are clearly observable; epitaxial 2D layer by layer growth and evolution into 3D <001> Stranski-Krastanov islands [106] & [119] & [120]. Figure 4.13 shows two AFM surface scans of two different samples, one which is grown under the Frank-van der Merwe growth mode and the other which is grown in the Stranski-Krastanov mode.

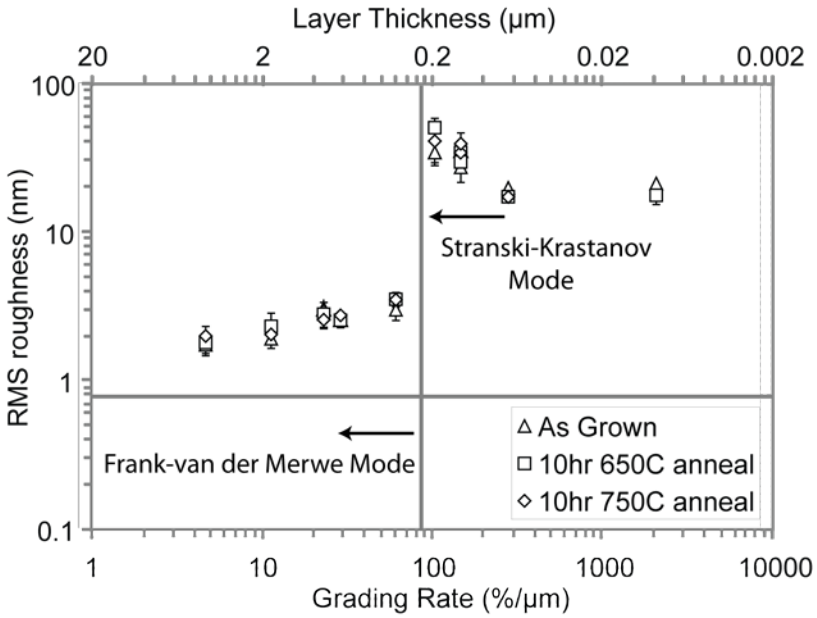

Figure 4.11: The RMS surface roughness of the SiGe cap layer with the variation in grading rate. The horizontal line represents the roughness of the Ge underlayer at 0.7 nm. The two different growth modes can be clearly seen. Roughnesses of 2-4 nm are achieved with grading rates of 4.69-61.3 % μm^{-1} are implemented.

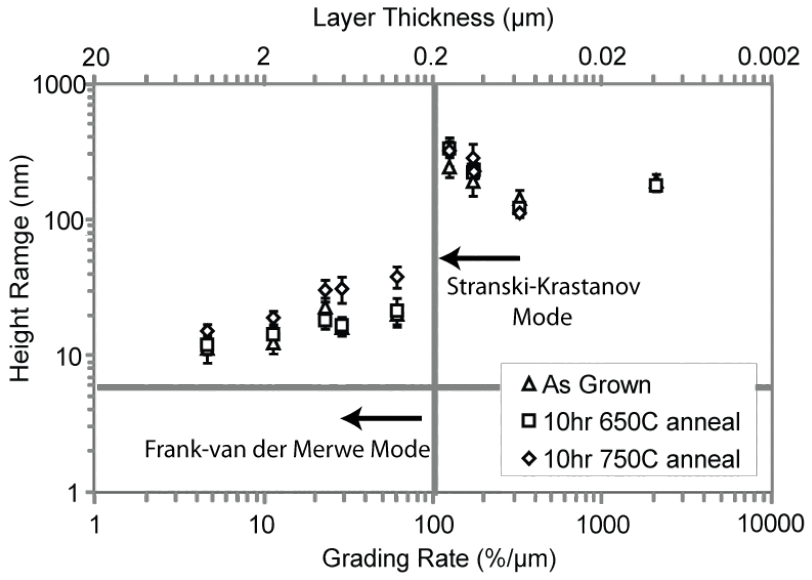

Figure 4.12: The variation of the height range with grading rate within RLG buffers. The horizontal line represents the height range of the Ge underlayer of 6.2 nm.

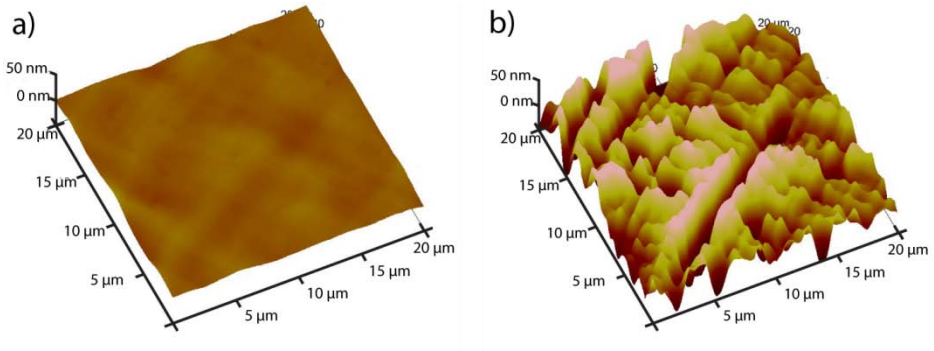

Figure 4.13: AFM 3D surface representation scans of two extremes a) shows the Frank van der Merwe growth mode on sample 4054 and b) shows the <001> Stranski-Krastanov Island formation on sample 4128.

Evolution into 3D islands is due to the relatively high growth temperatures, growth rates and interfacial strain. The <001> Stranski-Krastanov growth mode occurs when a SiGe constant composition cap is deposited directly on Ge underlayer (sample 3695) giving an RMS surface roughness (height range) of 21.5 nm (193 nm). When a thin grading layer is introduced the roughness and height range are reduced slightly. However, as the GR_{RLG} is reduced from 325 % μm^{-1} to 124 % μm^{-1} the RMS roughness (height range) increases linearly from 20.0 nm (144 nm) to 34.6 nm (246 nm). The surface of the sample with the maximum roughness (GR_{RLG} = 124 % μm^{-1}) is shown in Figure 4.13b). The increase in roughness is thought to be due to the longer growth time which is associated with thicker buffers. The increased growth time allows adatoms to reach positions of higher surface energy during the growth which increases the density of islands and their height. Annealing the wafers at 750°C for 10 hours increases the roughness of the wafers as GR_{RLG} is reduced to 124 % μm^{-1}. Annealing is thought to create surface adatoms which have an increased energy to travel along the surface of the buffer which increases the maximum RMS surface roughness (height range) from 34.6 nm (246 nm) to 41.4 nm (323 nm) for a GR_{RLG} of 124 % μm^{-1}.

The contrary is seen when the GR_{RLG} is reduced from 61.3 % μm^{-1} to 4.69 % μm^{-1}. The RMS surface roughness (height range) is shown to decrease linearly from 3.0 nm (20.2 nm) to 1.8 nm (11.4 nm). In this range the buffer is grown under a 2D layer by layer Frank-van der Merwe growth mode. Annealing the wafers at 750°C for 10 hours increases the roughness of the buffers as they did for higher grading rates. However, the RMS surface roughness (height range) of annealed samples still decreases linearly with decreasing GR_{RLG}, from 3.5 nm (38.4 nm) to 2.0 nm (15.4 nm). During annealing, the strain field associated with the underlying misfit dislocations are thought to cause the mobile adatoms to re-arrange in a higher energy configuration.

One particular advantage of relaxation under tensile strain which has been reported is that smoother epilayer surfaces are achieved due to the surface reconstruction [53] (Section 2.5.1). A comparison can be made between a $Si_{0.8}Ge_{0.2}$ forward linear graded buffer on a Si (001) substrate and the $Si_{0.2}Ge_{0.8}$ reverse graded buffer on a Ge underlayer as the misfit is similar. Bogumilowicz *et al* [121] have grown forward graded $Si_{0.8}Ge_{0.2}$ buffers through RP-CVD with a growth temperature of 850°C, a grading rate of 9 % μm^{-1} and a SiGe cap of thickness 1.05 µm. They report an RMS roughness of 3 nm which is grown on a Si (001) substrate (which is typically manufactured with an RMS surface roughness of 0.1 nm). Also when compared to $Si_{0.2}Ge_{0.8}$ linear graded buffers utilising a mid-growth CMP (Section 2.6.3), an RMS surface roughness of approximately 15 nm or greater is seen. Reverse linear grading has a distinct advantage, in terms of roughness, to forward grading [62] and the low temperature method [93] (Sections 2.6.3 & 2.6.7). However the ion implantation

method [92], Ge condensation [85] and the two temperature method [98] can achieve smoother buffer layers (Sections 2.6.5 & 2.6.6 & 2.6.7).

4.3.3 Dislocation Densities within RLG Buffers

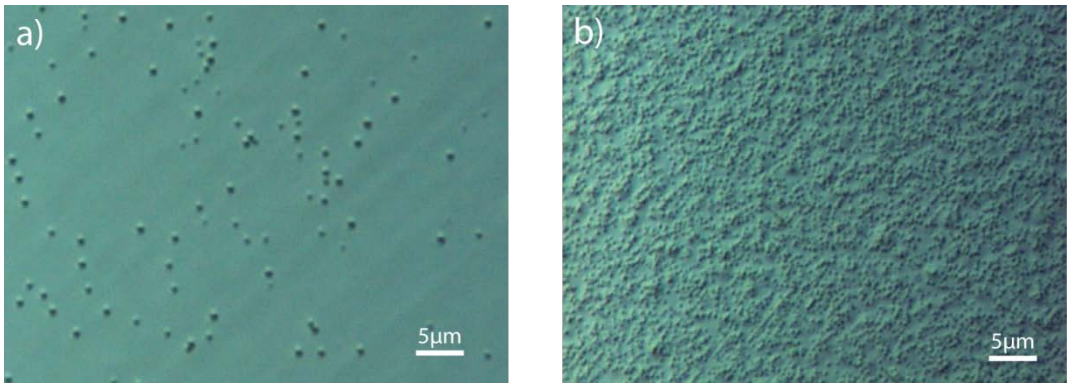

Figure 4.14: Examples of etched sample surfaces which have different TDD levels due to their different grading rates. a) Sample 4054 with a grading rate of 4.69 % µm^{-1} and TDD to the order of 10^{6} cm^{-2}. b) Sample 4130 with a grading rate of 324 % µm^{-1} and TDD to the order of 10^{8} cm^{-2}.

A 5 second diluted iodine etchant (3:1 ratio, Section 3.5) was used to reveal threading dislocations in the SiGe cap layer. An example of an etched sample is shown in Figure 4.14a) for sample 4054 with a low GR_{RLG} of 4.69 % µm^{-1} which has a low TDD of order 10^{6} cm^{-2}. Figure 4.14b) shows a DIC photo of etched sample 4130 with a high grading rate of 324 % µm^{-1} with a high TDD of ~10^{8} cm^{-2}

Figure 4.15 shows the measured TDD as a function of grading rate. The horizontal grey line represents the TDD of 2 x 10^{7} cm^{-2} from the Ge underlayer (sample 4045, Section 4.2.2). Increasing the grading rate within RLG buffers shows that the TDD shifts from dislocation gliding to the nucleation regime [44]. This conclusion is drawn because the TDD levels within the SiGe cap are greater than those grown into

the buffer from the Ge underlayer. The lower energy barrier to dislocation nucleation of high Ge composition SiGe alloys suggests that reverse graded buffers are more susceptible to nucleation of dislocations.

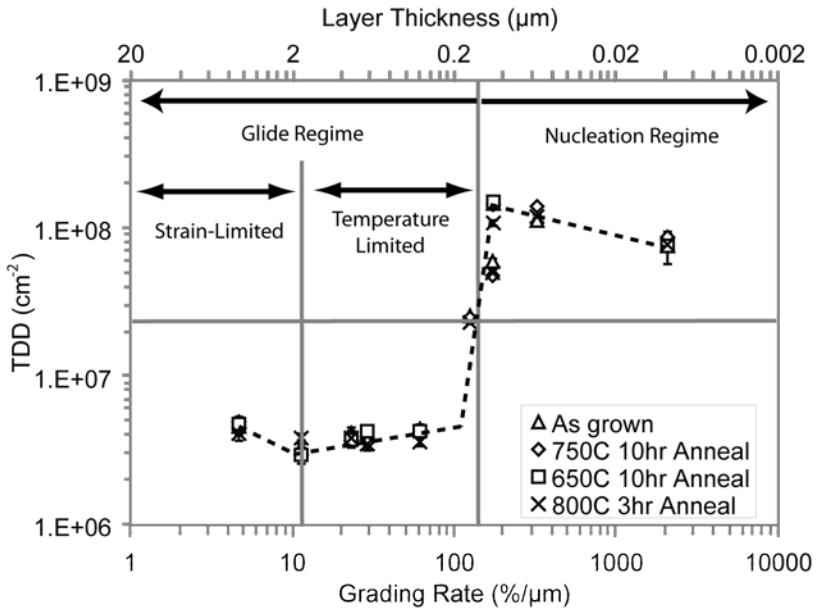

Figure 4.15: TDD variation with grading rate. The horizontal line shows the initial TDD within the Ge layer. A grading rate below 124 % μm^{-1} allows the system to enter the glide regime and hence achieve lower-than-initial layer dislocation densities. The lines shown are guides for the eye.

A constant composition $Si_{0.21}Ge_{0.79}$ cap which is deposited directly on the Ge underlayer (sample 3695) is calculated to have a GR_{eff} of about 2100 % μm^{-1} and is measured with a TDD of 7.7 x 10^7 cm^{-2}. This shows that a direct cap of constant composition material deposited at 850°C will have a higher dislocation nucleation rate than the threading arm annihilation rate, as it contains a TDD higher than that of the Ge underlayer (2 x 10^7 cm^{-2}). The misfit between the cap layer and the Ge underlayer is too low to homogeneously nucleate dislocations; therefore nucleation is proposed to be due to multiplication and heterogeneous nucleation.

As the grading rate is decreased, the TDD of the samples reaches a maximum value of 1.5 x 10^8 cm^{-2} at a GR_{RLG} of 174 % μm^{-1}. Section 4.4.2 reports that as the GR_{RLG} is decreased to 174 % μm^{-1} the roughness of the buffer surface increases. It is postulated that this high density of dislocations is likely to be due to the increase of the heterogeneous nucleation rate, promoted by the extra roughness incurred on the buffer surface.

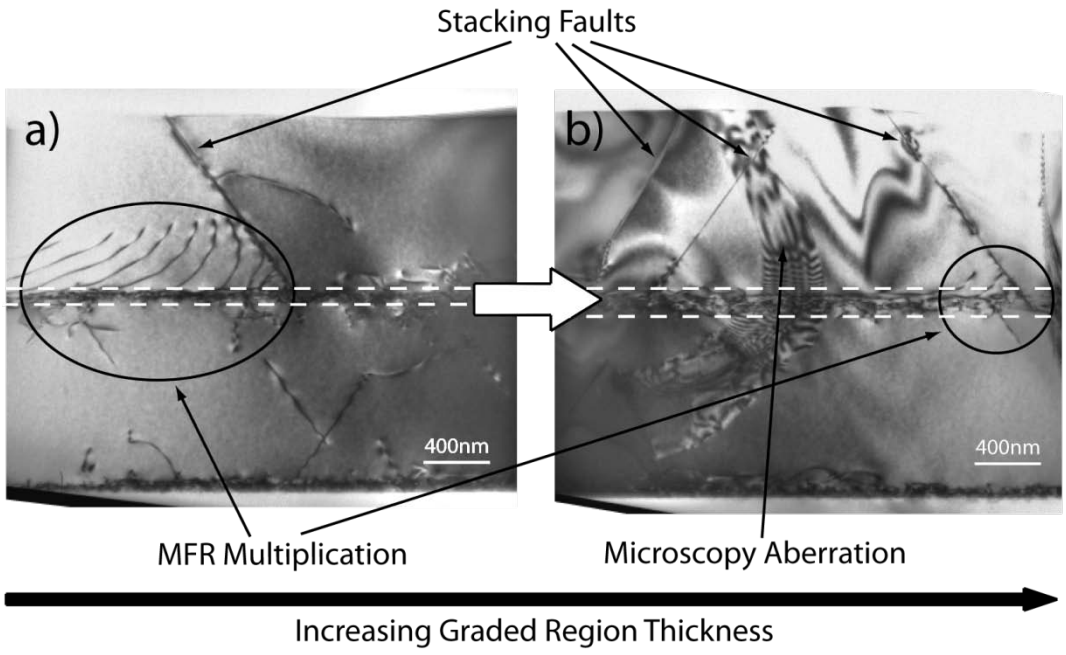

Figure 4.16: Cross sectional TEM micrographs of samples a) 4129 (t_{RLG} = 136 nm) and b) sample 4128 (t_{RLG} = 193 nm). It can be seen that the MFR mechanism decreases from a) to b) and that the number of resulting threading dislocations decrease as well. The second observation to be noted is that the stacking fault density increases from a) to b). Lines shown are only guides for the eye.

Further decreasing the GR_{RLG} to 124 % μm^{-1} (sample 4128) *reduces* the TDD to 2 x 10^7 cm^{-2}. This sample has been measured to have roughest surface (Section 4.3.2) and is speculated to have a high heterogeneous nucleation rate. As the TDD in the final SiGe cap layer is the same as the TDD from the underlying Ge layer the total nucleation and annihilation rates are assumed to be equal to each other. Therefore the reduction in TDD could only be due to a reduction in the multiplication nucleation

rate (Section 2.4.8). This mechanism is shown in Figure 4.16, where two TEM cross sectional micrographs of sample 4129 (GR_{RLG} = 172 % μm^{-1}) and sample 4128 (GR_{RLG} = 124 % μm^{-1}) are shown. It is seen that as the thickness of the graded layer is increased the MFR nucleation mechanism is lowered. As with forward graded buffers (Section 2.6.3) the thickness of the graded region will determine the [001] spacing between the misfit dislocations in the RLG region. This determines the interaction between misfit dislocations which directly affects the MFR multiplication nucleation.

Stacking faults are also seen within Figure 4.16a) and b) and are seen to increase in density as the graded region thickness is increased. Stacking fault density (SFD) is reported in Section 4.3.4. It is speculated that the SFD is too low to severely hinder the annihilation rate of dislocations by blocking mobile dislocations.

When the GR_{RLG} within the system reaches 61.3 % μm^{-1} and is decreased to 11.4 % μm^{-1} the buffers are grown in a 2D mode, therefore heterogeneous nucleation is assumed to be low. It is also seen in Figure 4.7, Figure 4.8 and Figure 4.9 that the nucleation of dislocations through multiplication is limited, as lower grading rates are used. Threading dislocations are not seen in TEM micrographs of thicker layers (Figure 4.7, Figure 4.8 and Figure 4.9), indicating a low TDD. As the GR_{RLG} is reduced from 61.3 % μm^{-1} to 11.4 % μm^{-1} the TDD is calculated from EPD measurements to reduce from 4.5 x 10^6 cm^{-2} to 3.3 x 10^6 cm^{-2}. This indicates that glide of threading arms is the main source of relaxation and that the annihilation rate is higher than the nucleation rate as the TDD levels are well below that of the Ge underlayer (2 x 10^7 cm^{-2}). As reported by Fitzgerald [76], dislocation glide will occur

only if there is a residual macroscopic strain in the layer and a high temperature is applied (Equation 2.14). It is reasonable to assume that the reduction of the TDD with reduced grading rates is due to the extra thermal budget applied to the buffer during the growth of the thicker structures. Within this GR_{RLG} range the system is thought to be within a temperature-limited sub-regime (Figure 4.15). Further reducing the GR_{RLG} to 4.65 % μm^{-1} increases the TDD to 4.6×10^6 cm^{-2}. It is surmised that the annihilation rate limited by the strain gradient of the RLG layer for this GR_{RLG} and is deemed to be in a strain-limited sub-regime.

An anneal of 750°C for 10 hours on a RLG buffer with a GR_{RLG} of 29.0 % μm^{-1} (sample 4050) lowers the TDD to a minimum of 2.4×10^6 cm^{-2}. These TDD values are comparable to the low temperature technique and traditional linear grading without a CMP mid-step (Sections 2.6.7 and 2.6.3) whilst superior to the Ge condensation technique and the two temperature method (Sections 2.6.5 and 2.6.8). However, when CMP is applied to conventional forward graded buffers (Section 2.6.3), dislocations in pile ups are no longer impeded, which allows mobile threading dislocations to achieve a TDD of 10^5 cm^{-2}.

Pile-up of defects has been shown in forward graded structures to result from severe crosshatch on the buffer [49]. Characterisation of pile up is accomplished by etching of the top layer as described in Section 3.5 and then observation though a DIC microscope. Pile up has not been observed on RLG buffers.

4.3.4 Extended Stacking Faults within RLG Buffers

Stacking faults are characterised through selective defect etching of the SiGe cap. This is followed by viewing the etched sample under a DIC microscope and assessing the line density of trenches formed by stacking faults. Figure 4.17 shows a DIC photo of an etched RLG buffer with stacking faults.

It was not possible to determine the stacking fault density (SFD) of RLG buffers with a TDD higher than 10^8 cm^{-2} as the etch pits formed from threading dislocations smothered the trenches formed from stacking faults making them indistinguishable. Additionally, the high surface roughness of the buffers (> 20nm) dwarf the surface steps created by stacking faults and are therefore not observable by AFM surface scans. TEM observations are also not quantifiable due to the relatively low SFD and limited viewable area within the TEM. However, evidence of stacking fault formation is shown in Figure 4.16 which shows cross sectional TEM micrographs of stacking faults in two different buffers.

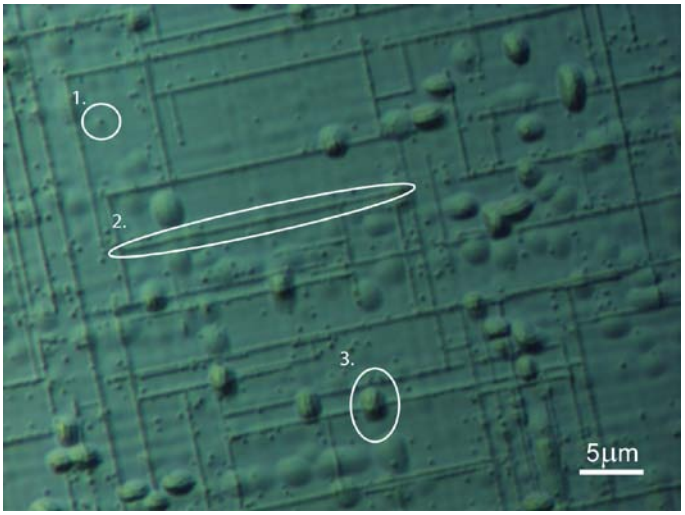

Figure 4.17: Sample 4128 with t_{LG} = 198 nm, etched in an Iodine etchant for 5 sec. The outlined features are: 1. a pit resulting from a threading dislocation, 2. an etch trench from a stacking fault, 3. a mound resulting from a hillock due to the <001> Stranski - Krastanov growth mode.

Figure 4.18 shows the SFD variation as a function GR_{RLG}. As the GR_{RLG} is decreased from 2100 % μm^{-1} to 124 % μm^{-1} the SFD within the buffer increases until a SFD value of 2.8 x 10^3 cm^{-1} is measured. The roughness of the RLG is also at a maximum when this GR_{RLG} is reached due to <001> Stranski-Krastanov growth (Section 4.4.2). It is speculated that the <001> Stranski-Krastanov growth is directly responsible for stacking fault formation. A hypothesis which could explain this mechanism is that the roughness of the surface will add a glide impediment to both the 30° and 90° partials which could force the 90° partial to enter a reduced glide channel (Section 2.4.7) and completely pin the 30° partial (Section 2.5.2). However, further studies of this effect are beyond the scope of this investigation.

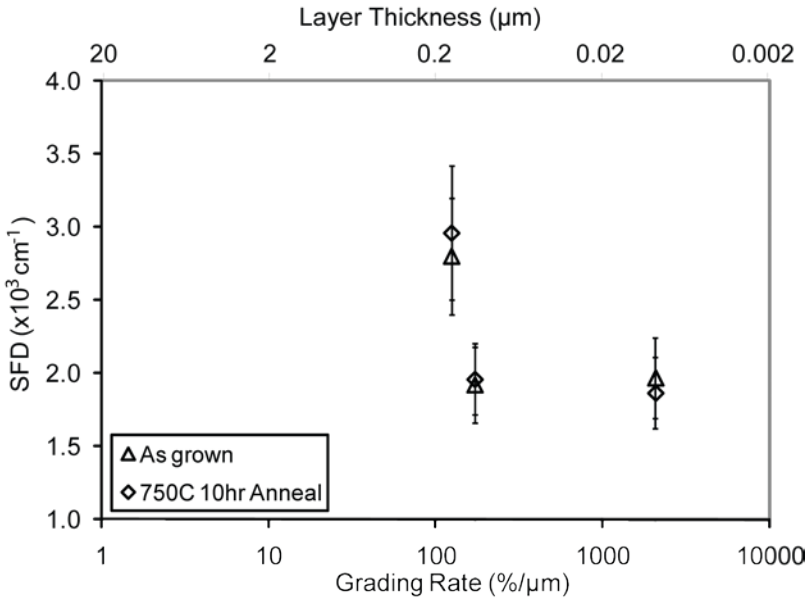

Figure 4.18: The stacking fault density variation as grading rate is changed, RLG layers of thickness $t_{RLG} \geq 0.35$ µm are observed to be stacking fault free.

Extended stacking faults are not observed for buffers with grading rates below 61.3 % µm^{-1}. These buffers exhibit Frank-van der Merwe growth and have lower grading rates, and are therefore speculated to have insufficient strain energy in the system.

Relaxation from stacking faults can be characterised from their line density (Sections 2.4.3 and 2.5.2). The relaxation ($R_{<110>}$) caused by the maximum density of stacking faults observed, with an effective Burgers vector (b_{SF}) of 1.32 Å is calculated to be 0.35 % compared to the Ge underlayer. Therefore the relaxation induced by stacking fault generation is negligible. Stacking faults are not normally observed within other buffer fabrication techniques as most relaxation occurs under compressive strain [122]. It has been found that with the growth conditions used a GR_{RLG} of 61.3 % µm^{-1} or lower do not show stacking fault formation within RLG structures.

4.3.5 Cracking of RLG Buffers

As Ge has a lower Young's modulus than Si, increasing the Ge content within SiGe buffers will reduce the Young's modulus [123] of the buffer. Therefore high Ge composition SiGe buffers are more susceptible to cracking if it is relaxed under *tensile* strain.

All samples were cleaved along the <110> directions with diamond-tipped scribes to induce a localised strain and propagate a supersonic crack throughout the whole Si (001) substrate [124]. This was done *intentionally* to create a sample for experimental analysis. This action is also seen to *unintentionally* induce cracks throughout the tensile strained reverse graded buffers and these cracks are seen to partially penetrate into the Si (001) substrate. This effect is expected to distort measured relaxation results as further local relaxation will occur due to crack induction.

The presence of cracks in strained layers is not desirable for device fabrication because they can resist in-plane electrical current flow and can introduce electrical shorting paths in vertical currents [125]. This could be detrimental to device fabrication as the devices and the connections between devices would be destroyed.

An investigation is necessary to correct any measured relaxation values as well as investigate the effect of cracking for device processing applications.

4.3.5.1 As-Grown Cracks

Characterisation of the *as-grown* crack density has been performed mainly through DIC microscope observation of the *uncleaved* wafers. Whilst wafers were in the DIC microscope, horizontal and vertical scans of the wafer were performed manually and views along these scans were recorded so that an average crack density could be calculated. An example of an as-grown crack which is seen through a DIC microscope is shown in Figure 4.19a). The measured features which are seen in Figure 4.19a) are faint and more distinguishable when viewed through a DIC microscope.

To ensure the features characterised through DIC microscopy were indeed cracks a selective etch was performed. If the features observed were assumed to be cracks then, theoretically, a liquid chemical etchant would enter the crack where lateral etching would take place causing a widening of the feature. To determine that the features seen on the surface of the wafer were indeed cracks a time delayed iodine etch was performed on a cleaved sample. The results of this etch are shown in Figure 4.19.

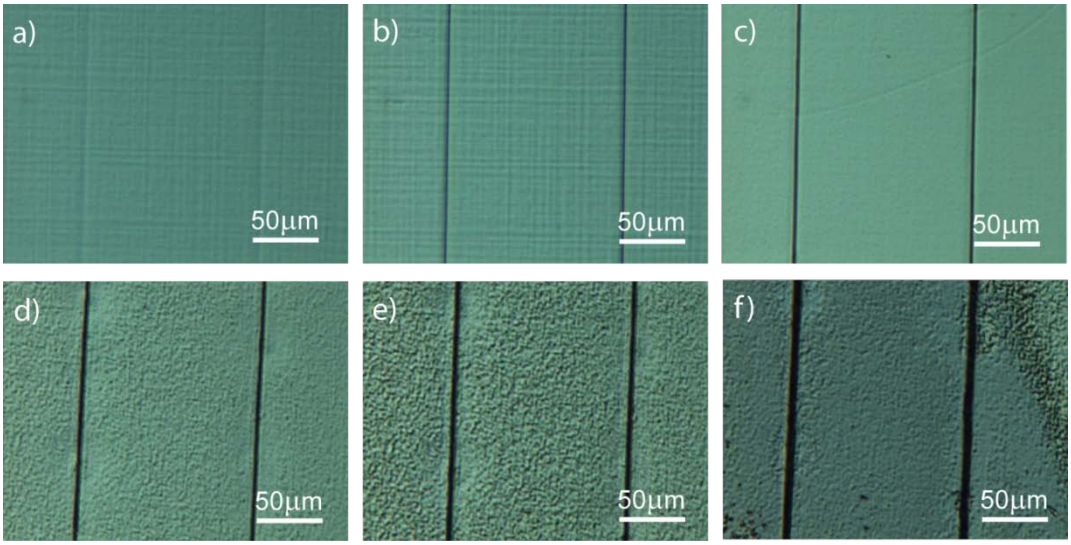

Figure 4.19: DIC images recorded after exposure to diluted Iodine etchant for a) 0 seconds, b) 2 seconds, c) 21 seconds, d) 34 seconds, e) 44 seconds and f) 59 seconds. The sample used was a cleaved piece of 4046 with an GR_{RLG} of 4.69 % µm^{-1}. The magnification was low, therefore any etch pits that have been formed were too small to be resolved. Experimental data was measured by Steve Huband.

It was determined from etching trials that the etch rate of the iodine solution is reduced as the Ge composition is increased (Section 3.5.2), therefore increasing etch intervals are required as the etch progresses down through the RLG region and into the pure Ge underlayer. The proposed crack widening effect can be seen through the different layers of the RLG buffer in Figure 4.19. In Figure 4.19b), the surface of the sample after an etch time of 2 seconds is shown. This etch is thought to remove approximately 300 nm from the SiGe cap. The crosshatch on the surface which is caused during growth of the graded region is still visible. Figure 4.19c) shows an etch time of 21 seconds which is thought to have removed most of the graded layer as no crosshatch is observed. Figure 4.19d) and e) shows etches of 34 and 44 seconds respectively. The roughening that is seen in these figures is thought to be due to the large density of etch pits created from the high TDD within the Ge underlayer. Figure 4.19f) shows an etch of 59 seconds, where the iodine etchant removes the entire RLG buffer including the Ge underlayer and the Si (001) substrate is observed.

From this figure it is shown that the crack within the buffer also partially enters into the Si (001) substrate.

Cross-sectional observation of the cracks through TEM was limited due to the relatively low crack density (ρ_{CD}) of the buffers. However a cross sectional TEM micrograph of a crack is shown in Figure 4.20 which shows the vertical profile of a crack. The TEM micrographs obtained were of cracks that were induced through sample preparation, but are assumed to be of the same dimensions as as-grown cracks. The crack shown in Figure 4.20 occurs in an RLG buffer with a total thickness of 2.2 μm. The dimensions of the crack are shown in the figure, where t_L is the thickness of the buffer and d_L is the vertical depth of the crack including the penetration into the Si (001) substrate. Λ is the average lateral distance between cracks and w is the crack opening at the mouth (Section 2.5.5). Another aspect within the figure which should be noted shows the (111) orientation of the crack beside the (111) stacking fault seen next to it. Relaxation of the top layer due to cracking was calculated through Equation 2.36 presented by Murray *et al* [63].

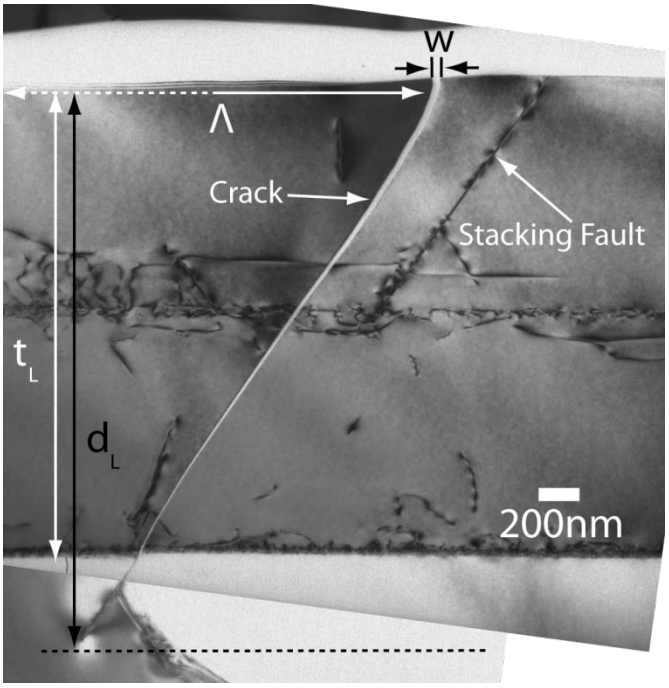

Figure 4.20: TEM micrographs of sample 4128 (GR_{LG} = 124. 97 % µm-1) showing the orientation of a crack. Alongside, a (111) stacking fault is shown. Cracking of this buffer was not observed in the as-grown wafer, but simply shows the orientation of a crack.

Only a handful of micrographs could be taken of the cracks formed within the reverse graded buffers. From these micrographs the following values were calculated; an average crack opening of 43 ± 1 nm is measured, and an average crack penetration (d/t), is measured to be 1.075 ± 0.01. The spacing between the crack arrays, Λ, was calculated from the inverse of the measured ρ_{CD} for each wafer (Equation 2.31).

A symmetric crack array formation was observed to form in the <110> directions perpendicular to each other, and appeared to have an ordered structure. The RLG buffers were only observed to form cracks during the growth of the thickest buffer, sample 4054. However, this is measured with an insignificant (<0.1 cm^{-1}) cracking density of 1.2 x 10^{-2} cm^{-1} and was thought to be an anomalous defect.

4.3.5.2 Induced Cracks

The ρ_{CD} within reverse graded buffers is generally low. Due to this low ρ_{CD} within the buffers a selection of 5 samples of similar size were taken from each wafer to ensure fair testing. Each sample was then viewed under the DIC microscope and was scanned vertically and horizontally where images were recorded. The ρ_{CD} was then measured as a line density from these images. The as-grown and induced ρ_{CD} for each RLG sample is shown in Figure 4.21. Note that *total* thicknesses of the buffer are used to characterise samples which is ~2 µm thicker than the buffer thicknesses reported in Table 4.1 due to the Ge underlayer and the SiGe cap. The thickest RLG buffer was measured with a maximum induced ρ_{CD} of 77.7 cm^{-1}; this was calculated to induce a relaxation of 4.8 % by Equation 2.31. Buffers with a total thickness of less than 2.7 µm were observed with insignificant cracking densities which were too low to quantify. These buffers are deemed to be free from induced cracks. Large errors in the ρ_{CD} are to be expected due to the low density and the limited field of view on the DIC microscope.

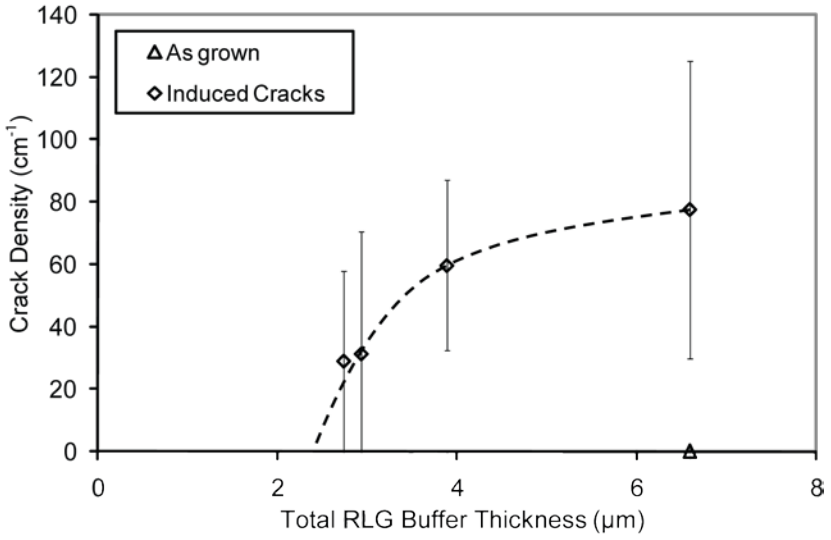

Figure 4.21: The crack density with variation of thickness of the RLG layer. The lines shown are guides for the eye. Experimental data was measured by Steve Huband.

The measured HR-XRD relaxation has been corrected with the calculated relaxation from cracking in all presented relaxation data (Section 4.3.6), unless otherwise stated. Crack densities within SiGe systems have not been widely reported due to most systems relaxing under compressive strain. Currie *et al* [62] have reported a conventional forward graded virtual substrate of thickness 23 µm and final composition of 100 % Ge which was 104 % relaxed indicating a small tensile strain due to thermal mismatch, this was measured to have a crack density of 47 cm^{-1}.

4.3.6 Relaxation and Composition of RLG Buffers

Relaxation and composition of the buffers was measured through HR-XRD RSMs from cleaved samples. An example of which is given in Figure 4.22 which are RSM scans of sample 4050.

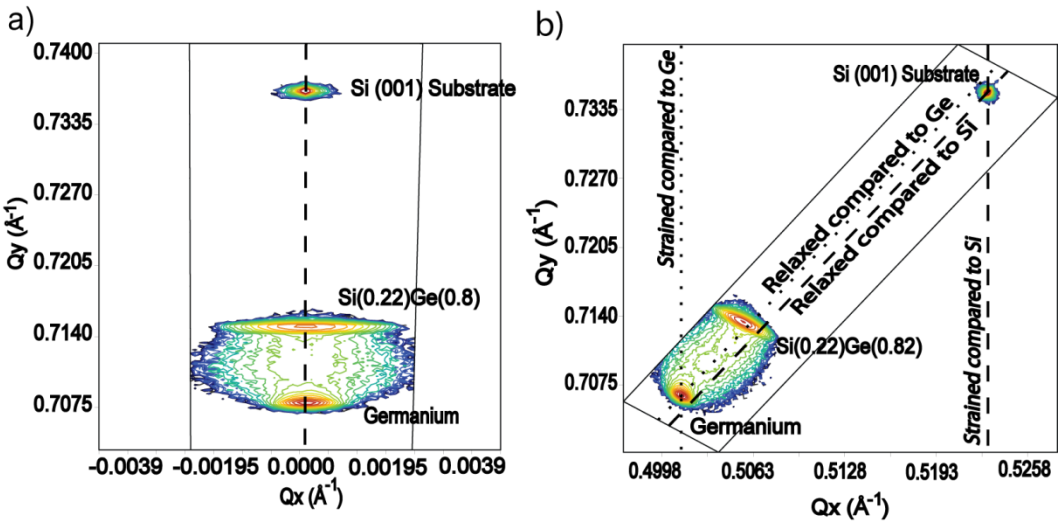

Figure 4.22: XRD RSMs of sample 4050 with a grading layer thickness of 736 nm corresponding to a grading rate of 29.0 %/µm. a) (004) reflection, b) (224) reflection

Analysis of the (004) reflection reveals virtually no tilt within the buffer structures as can be seen in Figure 4.22a) where the Ge underlayer and SiGe cap peaks are roughly aligned with the Si (001) substrate peak. In Figure 4.22a) and b) the peak from the Ge underlayer is broader when compared to the Si substrate peak which indicates a slightly less crystalline structure; most likely due to a high dislocation density. However, as with forward graded structures [104] mosaicity of the buffer is observed as the SiGe cap peak is broadened along the in-plane lattice parameter. This effect makes peak determination in reciprocal space less accurate which in turn reduces the accuracy of the results.

Figure 4.22b) shows the (224) reflection RSM for the same sample which is typical of the RLG buffers. The slight tensile strain in the Ge underlayer layer is represented in Figure 4.22b) by a deviation of the Ge underlayer peak from the diagonal dashed line that represents the full relaxation of a layer compared to the Si substrate. This will increase the tensile strain possible in the RLG and SiGe cap layer. A fully

pseudomorphic layer on a Si (001) substrate is represented by the vertical dashed line, and will hence be compressively strained. Similarly, the diagonal dotted line shows complete relaxation compared to the tensile strained Ge underlayer. Alongside this the vertical dotted line shows equal in-plane lattice parameters as the Ge underlayer, hence the maximum tensile strain available in the RLG system. *The relaxation of the SiGe cap will be reported relative to the Ge layer unless otherwise mentioned.*

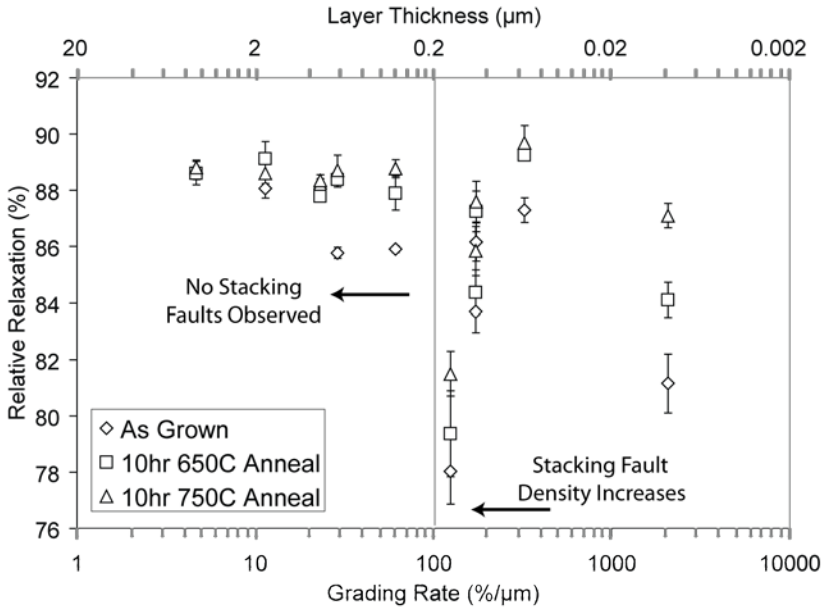

Figure 4.23: Relaxation of the top SiGe cap layer for RLG buffers as determined by x-ray diffraction without correcting for the relaxation due to cracks. The relaxation was compared to the tensile strained Ge underlayer. Due to stacking fault formation relaxation of layers with grading rates of ≥ 124 %/µm was hindered by the stacking fault interaction energy barrier.

Top layer compositions are shown in Table 4.1, and measured relaxation relative to the Ge underlayer is shown in Figure 4.23. A maximum measured relaxation of 88.6 % compared to the Ge underlayer has been recorded for the thickest RLG buffer with the lowest grading rate (GR_{RLG}) of 4.69 % μm^{-1}.

When samples under tensile strain are cleaved, depending on the amount of strain energy in the system, cracks can be induced within the buffer which can relieve strain. Cracks are observed within the thicker buffers and characterisation of cracks shows that the thickest buffer also contains the highest crack density (see Section 4.3.5). This buffer, sample 4054, is measured by XRD with a relaxation of 88.6 %. Relaxation from induced local cracking for this buffer accounts for 4.8 % of the measured relaxation which is calculated from Equation 2.36. Using this information the calculated relaxation of the as-grown SiGe can be calculated to be 83.8 % for the thickest buffer.

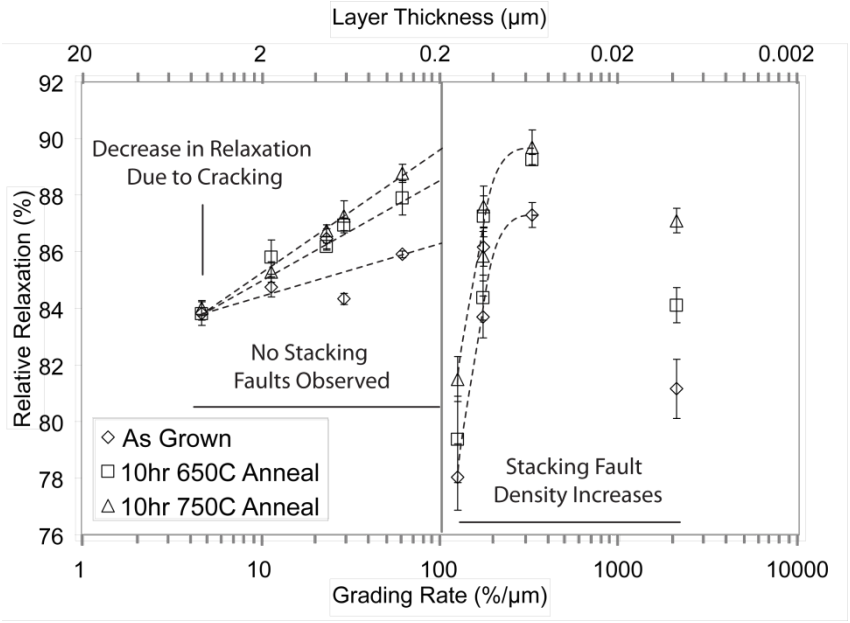

Figure 4.24: The actual relaxation for RLG wafers when induced local cracking is taken into account. Lines shown are guides for the eye only.

Figure 4.24 shows the relaxation for each wafer after correction for induced cracks within the buffer. The correction for cracking within the epitaxial layer shows that a logarithmic trend for relaxation occurs within the range $1\ \% \ \mu m^{-1} \leq GR \leq 100\ \% \ \mu m^{-1}$.It is speculated that within this range the RLG buffer

relaxation is under a strain-limited regime and relaxation can be enhanced if a steeper strain gradient is used. As the grading rate is increased to 61.3 % μm^{-1} (see points just left of the dividing line in Figure 4.24) the relaxation is 85.9 %.

Ex-situ annealing was performed to determine the thermal stability of the buffers. Cleaved samples from each wafer were annealed at temperatures of 650°C and 750°C for 10hrs, much higher than the typical temperatures of 550°C experienced in typical Ge device fabrication [8]. Annealing of the strain-limited sample 4051 (61.3 % μm^{-1}) at 750°C for 10 hours increases the relaxation from 85.9 to 88.8 %.

Stacking fault density is reported in Section 4.3.4 and it is shown that this buffer was also observed to have the maximum density of stacking faults. As the grading rate was increased from 124 % μm^{-1} to 2100 % μm^{-1} the stacking fault density (SFD) decreased. At a GR_{RLG} of 124 % μm^{-1} the as-grown relaxation of the buffer is measured to be 78.0 %, a minimum of all the RLG buffers. This relaxation was increased to 81.5 % by annealing the buffer at 750°C for 10 hours. Alongside this, the measured relaxation is shown to increase in a logarithmic trend. This increase in relaxation is postulated to be due to stacking faults blocking mobile threading dislocations, as reported by Lee *et al* [126] and Parsons *et al* [127]. An increased SFD is speculated to hinder the *relaxation* process.

When the relaxation of the buffer is considered two patterns are clearly observed, relaxation of the buffer when populated purely by threading and misfit dislocations (left side of Figure 4.24), and another when additionally populated by stacking faults (right side of Figure 4.24).Where only threading and misfit dislocations are

concerned, as GR_{RLG} is increased from 4.69 % μm^{-1} to 61.3 % μm^{-1}, the relaxation rate is increased due to the steeper strain gradient within the buffer.

The steepest grading rate which was not observed to from stacking faults was GR_{RLG} = 61.3 % μm^{-1} which measured to have an as-grown relaxation of 85.9 %, this showed the maximum relaxation in RLG buffers. It is possible that thermal expansion of the RLG layer and the SiGe cap relative to the Ge underlayer produces a compressive strain which partially limits the relaxation of the tensile strained layer during growth. This expansion of lattice parameters during growth and the relative contraction would produce a purely compressive strain, equivalent to 2 % relaxation (see Section 2.5.4). This means that a maximum relaxation of 87.9 % occurs during growth and that further relaxation that could still be encouraged by annealing of buffers. As dislocation velocity can increase by a few orders of magnitude with temperature (Equation 2.14), a higher temperature *in-situ* anneal has the potential to increase the relaxation above that of the longer 750°C anneal.

In summary, relaxation of all RLG buffers is high and an optimised GR_{RLG} of 61.3 % μm^{-1} is shown to avoid retardation of relaxation from stacking faults whilst maximising the strain gradient to induce further relaxation in RLG structures. When the as-grown relaxation of 85.9% relative to the Ge layer is compared to the Si (001) substrate, it is equivalent to a relaxation of 106.1%. A high degree of relaxation is achieved within all the RLG buffers grown, which have been shown to be just above the 100±5 % required for industry standard platforms. Other relaxation levels reported are greater than relaxation enhancements achieved in ion implantation of SiGe buffers [92] (Section 2.6.6). An optimised grading rate of 61.3 % μm^{-1} is shown

to maximise the strain gradient to induce further relaxation in RLG structures. Relaxation levels found though Ge condensation [85] (~80 %) and the LT method [93] (~90 %) are comparable to the work presented (Section 2.6.5 & 2.6.7). However, the 2-temperature method [98] and linear grading buffers [30] possess higher levels of relaxation (Section 2.6.8 & 2.6.3).

4.4 Properties of Reverse Terrace Graded (RTG) Buffers

In this section an investigation of the individual properties of relaxation, composition, defect densities and surface roughness of the RTG buffers and their interrelationship as a function of grading rate and effective grading rate is reported. Unless otherwise stated or shown, the errors for measurements made in this section are as described in Section 4.3. *(Note that grading rates for reverse graded buffers are shown as positive values for clarity.)*

4.4.1 RTG Composition Profile

RTG buffer thickness was determined through cross sectional TEM measurements and compositions were determined through HR-XRD RSMs. The individual terraces of the RTG region (Section 4.2.4) could not be resolved through TEM observations; therefore the overall RTG region thickness was recorded and is shown in Table 4.3. The effective grading rate is calculated by $GR_{eff} = \frac{(composition - 1)}{RTG\ region\ thickness}$, this allows a comparison of the thermal budgets used between RTG and RLG buffers. The *actual* grading rates (shown in Table 4.3) are calculated by $GR_{RTG} = (7/4)GR_{eff}$ as only 4 out of the 7 seven terraces are actually graded layers. The actual grading

rates are calculated with the assumption that all the separate terraces are of equal thicknesses, not including the SiGe cap layer.

Wafer Number	RTG region Thickness (±2 %) (nm)	Top Layer SiGe Composition (±0.005) (-)	Effective Grading Rate (±1 %) (% μm^{-1})	Grading Rate (±1 %) (% μm^{-1})
4135	7951	0.770	2.89	5.06
4134	5603	0.767	4.15	7.27
4133	3632	0.766	6.45	11.3
4346	3027	0.770	7.61	13.3
4345	1844	0.767	12.6	22.1
4344	1149	0.769	20.1	35.2
4132	863	0.767	27.0	47.2
4131	243	0.758	100	174
4343	136	0.764	173	303
3695	10 (effective)	0.793	2069	2069

Table 4.3: The samples grown for the RTG buffers. Thicknesses were measured from TEM micrographs and compositions were calculated through HRXRD RSM scans. Individual terraces could not be resolved therefore effective grading rates were calculated. Actual grading rates were calculated assuming that each terrace was of equal thickness.

Figure 4.25 and Figure 4.26 show the composition profile with the corresponding TEM micrographs for RTG region thicknesses (t_{RTG}) of 1844 nm and 3632 nm (samples 4345 and 4133). Note that the labels used in Figure 4.25 are the nominal values and are not the compositions measured.

Si from the graded layer is seen to diffuse into the Ge underlayer in both wafers and the diffusion depth is seen to increase with thermal budget, as observed in RLG buffers. A Ge composition drop of 0.7 % over a thickness of 210 nm for a t_{RTG} of 3632 nm is observed. The more significant drop of 1.5 % over a thickness of 178 nm for a t_{RTG} of 1844 nm has a misfit of ε = -0.0007 and is found to be too low to affect dislocation glide (Figure 2.14).

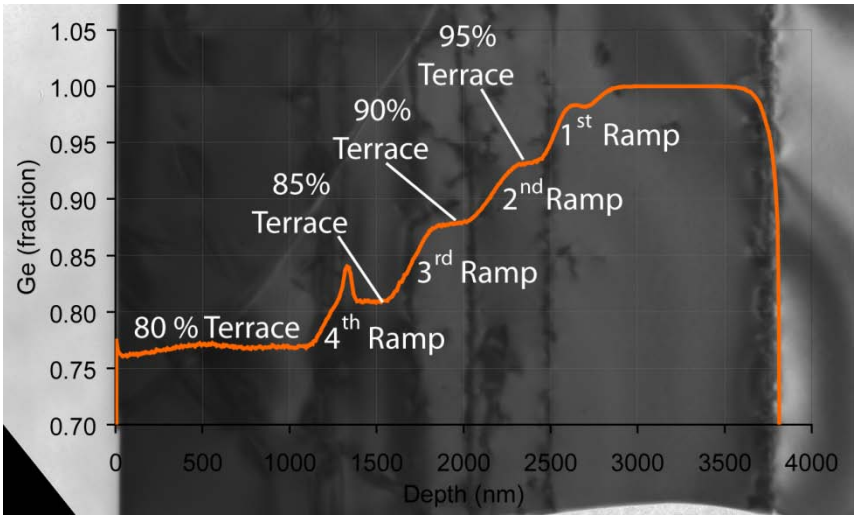

Figure 4.25: Composition profile of sample 4345 with a terrace graded region of thickness 1844 nm with an effective grading rate of 12.6 % µm^{-1}. (Terrace composition labels are nominal)

An example of an almost ideal RTG profile is clearly seen in Figure 4.25. Better control over the Ge profile within thinner RTG buffers is achieved when the terraces remain relatively thin (<250 nm) and chamber coating is minimal. The sample shown in Figure 4.25 (wafer 4345, t_{RTG} = 1844 nm) shows almost no composition drop during the grading of the constant composition terraces. However, a product of growth chamber deposition is seen in the thick 1180 nm SiGe cap labelled as the 80 % terrace as a slight decrease in composition. A total drop of 0.6 % Ge is seen from the depth of 520 nm until the surface of the buffer. This linear drop in composition shows the loss of control of the lamp array feedback loop (Section 2.2.4). The chamber wall deposition is so thick at that point of growth that the loop consistently increases the lamp power to keep the substrate temperature the same. From the decrease of Ge composition the growth temperature is expected to be slightly higher than intended during growth of the SiGe cap layer. The misfit of this linear drop is too small to induce glide of dislocations alone, but will add to the strain energy in the buffer and aid in the glide of mobile dislocations.

During growth of the thinner (t_{RTG} = 1844 nm) RTG buffer only *one* HCl chamber etch was performed *during the RTG region*, between the 85 % terrace and the 4th ramp. This etch step provides a composition peak at the interface. It is speculated that this peak is due to surface segregation of the Si adatoms from the increased growth kinetics and the increasing flow of SiH_2Cl_2 (due to the grading process within the CVD). The peak in Ge composition is measured to be 3.11 % corresponding to a misfit value of 0.0013, which is not likely to induce dislocation glide (Figure 2.14).

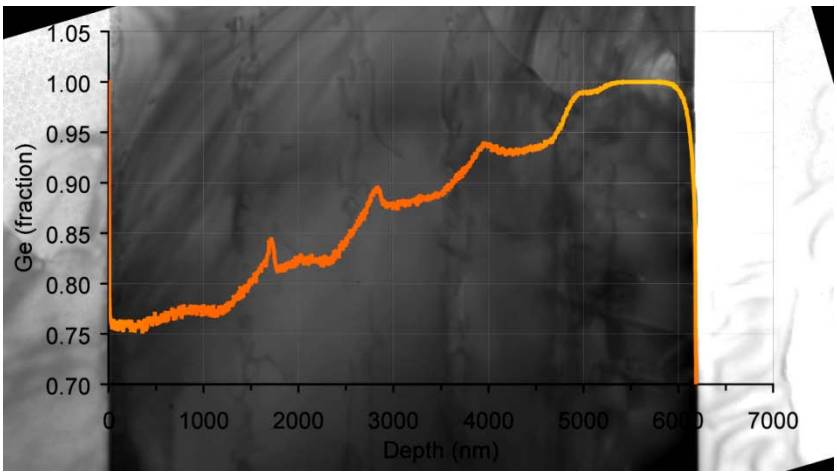

Figure 4.26: Composition profile of sample 4133 with a terrace graded region of thickness 3632 nm with an effective grading rate of 6.45 % µm^{-1}.

When the thickness of the RTG region is increased to t_{RTG} = 3632 nm (sample 4133) the effect of control loop loss is observed in all constant composition terraces. Figure 4.26 shows the increasing effect of control loop loss that is observed throughout the structure. The 95 % Ge terrace shows a composition drop of 1.4 % over 476 nm, corresponding to an *unintended* grade of 2.87 % µm^{-1}. This drop in composition is observed in each constant composition terrace and *unintended* grading rates (terrace) of 3.21 % µm^{-1} (90%), 2.36 % µm^{-1} (85 %) and 2.13 % µm^{-1} (80 %) are calculated.

All these *unintended* graded regions act over similar distances and it is determined that the control loop loss occurs at a deposition thickness of approximately 500 nm. This shows that thinner terraces are required to retain control of the temperature feedback loop and therefore the composition profile. Alternatively the CVD growth process could be optimised for thicker layer growth, but this is not the main investigation of this chapter.

HCl chamber etches were performed before *all* graded regions within sample 4133 and peaks are seen at the relevant interfaces in Figure 4.26. The combination of surface segregation *after the etch* and the loss of feedback control *prior to the etch* combine together to form larger composition differences at the interfaces. These composition differences are calculated to be (at terrace/ramp interface) 0.7 % (95 %/2nd), 1.1 % (90 %/3rd) and 3.1% (85 %/4th). These composition differences are not large enough to induce glide of dislocations.

4.4.2 Surface Roughness of RTG Buffers

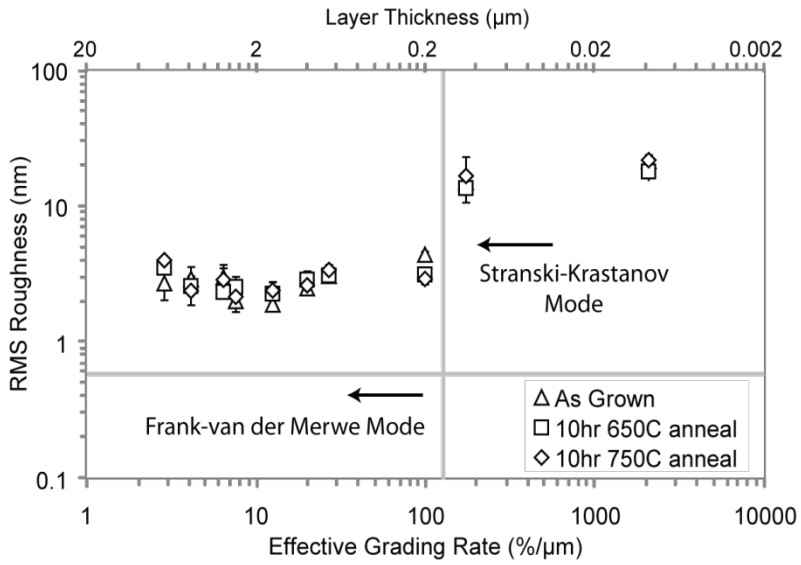

Figure 4.27: The relationship between RMS surface roughness and effective grading rate. An effective grading rate of 173 % µm^{-1} is the only RTG buffer to have been observed with <001> Stranski-Krastanov growth.

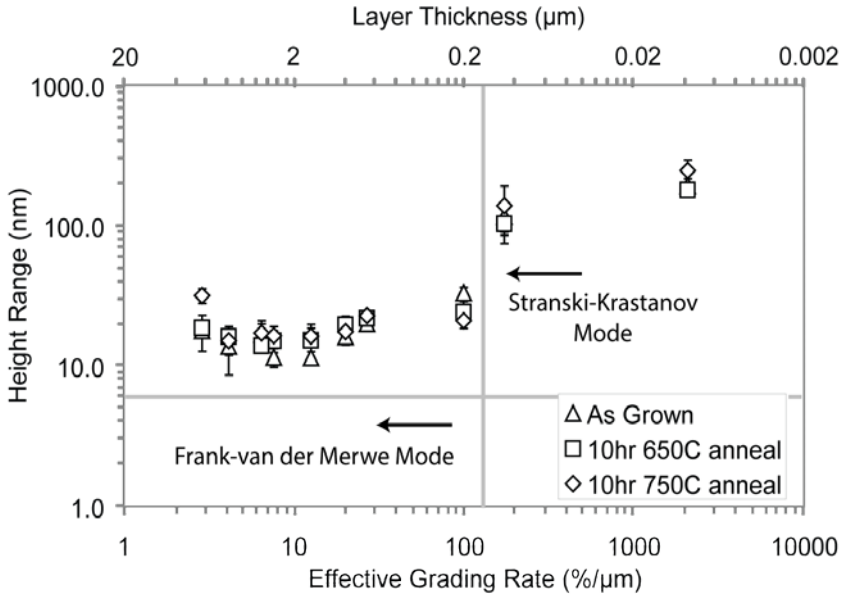

Figure 4.28: The height range measured for the RTG buffers shown against the effective grading rate of each buffer.

Figure 4.27 and Figure 4.28 show the RMS surface roughness and the height range of the RTG buffers as the GR_{eff} is varied. The horizontal grey line represents the

0.7 nm RMS roughness of the Ge underlayer. <001> Stranski-Krastanov islands are only seen within one RTG buffer with a GR_{eff} of 173 % μm^{-1} (sample 4343) where an RMS surface roughness (height range) of 15.1 nm (116 nm) is measured, the surface of this sample is shown in Figure 4.29b). Annealing of this buffer at 750°C for 10 hours increases the RMS surface roughness (height range) to 16.7 nm (139 nm). This roughness is approximately equal to that of the constant composition cap which was deposited directly on the Ge underlayer, sample 3695.

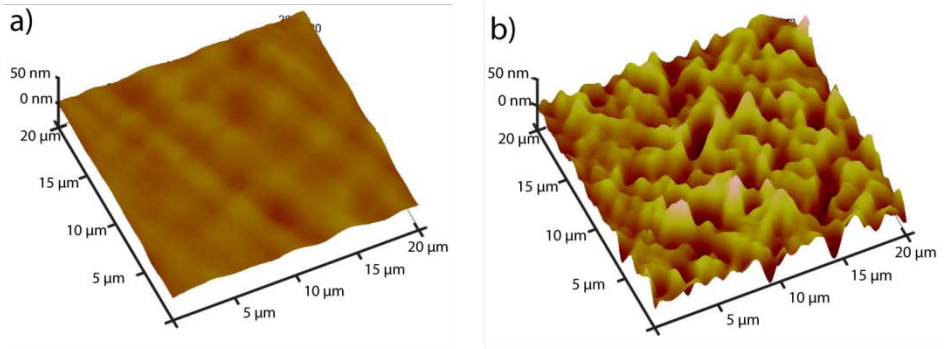

Figure 4.29: AFM 3D surface representation scans of two extremes a) shows the Frank van der Merwe growth mode on sample 4135 and b) shows the <001> Stranski-Krastanov Island formation on sample 4343.

When the GR_{eff} is reduced from 99.5 % μm^{-1} to 2.89 % μm^{-1} the RTG buffers are grown in a 2D growth mode, an example of this surface is shown in Figure 4.29a) for sample 4135 (GR_{eff} = 2.89 % μm^{-1}). The RTG buffers are thicker by nature and therefore have lower effective grading rates which lead to smoother surfaces. As the GR_{eff} is reduced from 99.5 % μm^{-1} to 12.6 % μm^{-1} the RMS surface roughness (height range) is observed to decrease linearly from 4.4 nm (33.1 nm) to 1.9 nm (11.5 nm). As the GR_{eff} is further decreased to 2.89 % μm^{-1} the RMS surface roughness (height range) of the buffer is seen to increase slightly to 2.7 nm (17.9 nm). This trend is speculated to be due to the trade-off between the thermal-

budget and strain gradient as described in Section 4.3.3. The thermal budget applied gives the adatoms energy to become mobile and travel on the surface. The strain gradient determines the strength of the strain field from the misfit dislocation network on the surface of the wafer.

During growth of the buffer the mobile adatoms will incorporate into the lower energy sites if a strong enough strain field from the misfit dislocation network is present, which will reduce the surface roughness of the layer. However, if adatom transport is affected by an increase in transport energy, a weaker homogeneous strain field from the misfit dislocation network and a stronger strain field from the increase of TDD (Section 4.4.3), the RMS surface roughness can be increased. The nano-scale fluctuations in strain from the crosshatch *and* threading dislocations will redirect mobile adatoms to amplify the morphology already on the surface of the wafer. An example of this is shown by the increase in roughness and the height range when an RTG buffer with a GR_{eff} of 2.89 % μm^{-1} is annealed and releases mobile adatoms. An anneal of 750°C for 10 hours increases the RMS surface roughness (height range) from 2.7 nm (17.9 nm) to 4.0 nm (31.8 nm).

It has been shown that whilst keeping growth rates constant a variation of grading rate and effective grading rate produce different surface roughnesses. These vary from the <001> Stranski-Krastanov growth mode to a minimal roughening due to the strain field of the misfit dislocation network, then leading back to excess roughening from crosshatch formation. RTG buffers show that thinner buffers can be grown with similar RMS roughness as RLG buffers. The lowest roughness obtained through RLG growth is 1.8 nm a GR_{RLG} of 4.69 % μm^{-1}, whilst the smoothest layer obtained

for an RTG structure is 1.9 nm a GR_{eff} of 12.6 % μm^{-1}. Compared to forward grade buffers these enhancements far surpass the RMS roughness obtained when grading under compressive strain [30] (Section 2.6.3).

4.4.3 Dislocation Densities within RTG Buffers

The same iodine etching procedure was used to reveal dislocations in RTG buffers as used in Section 4.3.3. Lower TDDs are expected because the constant composition terraces within the RTG structures increase the average [001] misfit dislocation spacing in the RTG region, reducing the probability of dislocation multiplication.

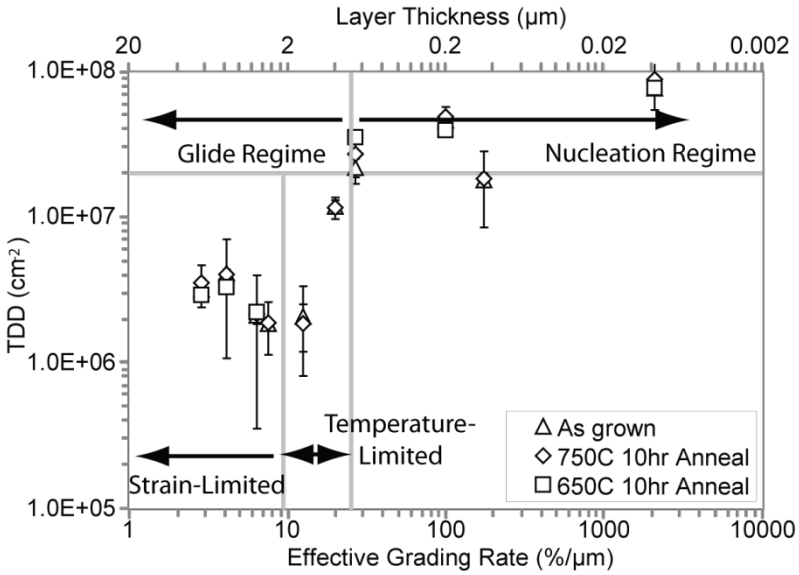

Figure 4.30: The threading dislocation density of the RTG buffers. Shown are the effective grading rates of the buffers. The horizontal grey line represents the TDD of the Ge underlayer.

Figure 4.30 shows the variation of TDD when the terrace thickness and therefore the effective grading rates are varied. The horizontal grey line shows the TDD value for the Ge underlayer. The results are comparable to those obtained for the RLG buffer (Figure 4.15). Two regimes of dislocation dynamics can be observed; the nucleation

and glide regimes. The TDD within RTG buffers does not exceed 7.7 x 10^7 cm^{-2} which is generated when a SiGe cap layer is deposited directly on the Ge underlayer. When the GR_{eff} is reduced from 2100 % μm^{-1} to 27.0 % μm^{-1} the layers are observed to have dislocation densities higher than that of the Ge underlayer, with one exception which is mentioned later. Within this regime the TDD is reduced linearly as GR_{eff} is reduced due to the decreased probability of interaction between misfit dislocations, hence lowering the multiplication nucleation rate. The reduction of the multiplication mechanism as GR_{eff} is reduced is shown in Figure 4.30 for samples 4131 and 4132. The heterogeneous nucleation rate is speculated to remain low throughout this range as all RTG buffers are of a low RMS roughness (<4 nm), with one exception (Section 4.4.2). The buffers within this GR_{eff} range are considered to be under a nucleation regime purely from dislocation multiplication.

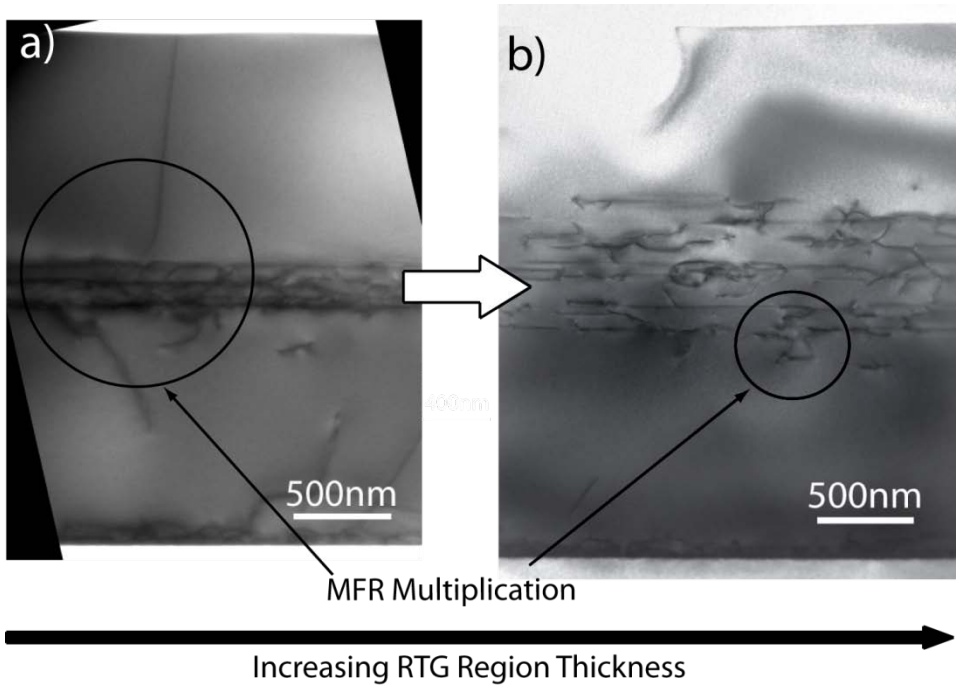

Figure 4.31: Cross sectional TEM micrographs of samples a) 4131 (t_{RTG} = 243 nm) and b) 4132 (t_{RTG} = 863 nm). It can be seen that the MFR mechanism decreases from a) to b).

The exception to these observations occurs at a GR_{eff} of 173 % μm^{-1} which was measured to have a TDD of 1.8 x 10^7 cm^{-2}. The RMS roughness for this sample (Section 4.4.2) is measured to be high (> 15 nm). The nucleation and annihilation rates are thought to be equal as the TDD of this buffer is approximately equal to that of the Ge underlayer. It is speculated that relaxation of this buffer occurs mainly under heterogeneous nucleation as the multiplication nucleation rate is reduced due to the relatively high roughness of each terrace.

As the GR_{eff} is reduced from 27.0 % μm^{-1} to 2.89 % μm^{-1} the RTG buffer system enters a dislocation glide regime. Within this regime, dislocations glide can be limited either by the amount of strain energy in the system or by the thermal energy applied, as explained in Section 4.3.3. When the GR_{eff} is reduced from 27.0 % μm^{-1} to 12.6 % μm^{-1} the system enters a temperature-limited sub-regime, shown on Figure 4.30. This is where dislocation glide is only limited by the thermal budget during growth. Further reducing the GR_{eff} from 12.6 % μm^{-1} to 2.89 % μm^{-1} enters the system to a strain limited sub-regime. The facilitation of relaxation in this sub-regime is only hindered by the strain gradient of the graded terraces. The optimised trade-off of these sub-regimes produces the lowest TDD of 2.1 x 10^6 cm^{-2} which is measured for sample 4345 (GR_{eff} = 12.6 % μm^{-1}).

The best value of TDD is obtained for a GR_{eff} of 12.6 % μm^{-1} which is calculated to have an actual grading rate (GR_{RTG}) of 22.1 % μm^{-1} within the graded layers of the RTG structure, as described in Section 4.4.1. A comparison between the GR_{eff} of RTG buffers and the GR_{RLG} of RLG buffers allows an equal evaluation of the thermal budgets applied. The best TDD values are obtained for an RTG buffer with

GR_{eff} of 12.6 % μm^{-1} and an RLG wafer with GR_{RLG} of 11.4 % μm^{-1}, which have almost equal thermal budgets.

In contrast, a comparison of the GR_{RTG} of RTG buffers and the GR_{RLG} of RLG buffers allows a fair evaluation of the strain gradients applied during grading. The RTG buffer of GR_{RTG} of 22.1 % μm^{-1} has a grading rate almost twice that of the RLG buffer with GR_{RLG} of 11.4 % μm^{-1}. Therefore, when the TDD value for these RTG (2.1 x 10^6 cm^{-2}) and RLG (3.3 x 10^6 cm^{-2}) structures are compared it is found that by doubling the grading rate and applying the same thermal budget reduces the TDD by approximately half.

In summary, it has been shown that a variation of grading rate and effective grading rate produces different regimes of dislocation dynamics. Two major regimes are seen in the systems presented, the nucleation and glide regimes. The nucleation regime is seen to be dominated by multiplication nucleation from dislocation interactions. The glide regime is seen to switch between two sub-regimes; a temperature limited sub-regime ending with a strain-limited sub-regime. Annealing of an RLG buffer can lower dislocation densities to 2.4 x 10^6 cm^{-2} for a GR_{RLG} of 29.0 % μm^{-1}. However, the best TDD level of 1.5 x 10^6 cm^{-2} is achieved for an annealed RTG buffer with a GR_{eff} of 6.45 % μm^{-1}. RTG buffers have been shown to achieve lower TDD values when compared to RLG buffers. This enhancement is thought to come from the increased strain gradient of the ramped terraces within the RTG structure and the increased thermal budget from the thicker buffer layer. Pile up is not observed within RTG buffers.

4.4.4 Extended Stacking Faults in RTG buffers

Only one sample in this RTG investigation has shown signs of stacking fault formation, sample 4343. This sample has been shown to grow under the <001> Stranski-Krastanov growth mode in Section 4.4.2 and in Figure 4.29b). This sample also has a high density of dislocations (1.8×10^7 cm^{-2}). When the sample is subjected to a selective chemical etch, any trenches which would indicate stacking faults are smothered by etch pits due to threading dislocations. Therefore selective etching cannot be used to characterise SFD.

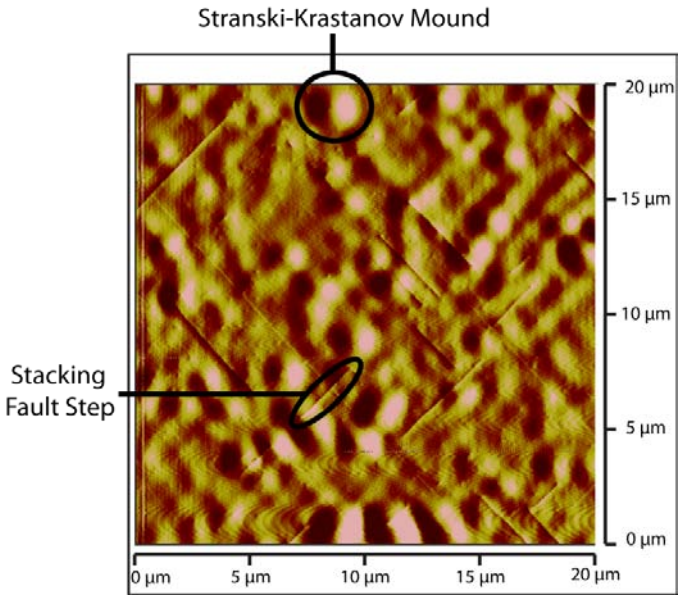

Figure 4.32: AFM deflection surface scan of RTG sample 4343 (173 % μm^{-1}). Due to the lower RMS roughness when compared to RLG buffers the surface step caused by stacking faults is observable.

However, the sample has a lower roughness than the RLG structures under the <001> Stranski-Krastanov growth mode (Section 4.3.2) and also contains a lower TDD (than RLG buffers) which allows the surface step caused by stacking faults to be observable by AFM *deflection* scans (Section 3.2). The deflection scan for sample 4343 is shown in Figure 4.32. From two AFM deflection scans a stacking fault

density of $1.7\pm0.2 \times 10^3$ cm^{-1} is measured which is consistent with the densities observed in RLG buffers (Section 4.3.4). This observation supports the theory that <001> Stranski-Krastanov growth promotes the formation of stacking faults in reverse graded buffers.

4.4.5 Cracking of RTG Buffers

As with RLG structures, cracks are induced in as-grown RTG wafers and also in RTG samples through cleaving. Therefore it is necessary to characterise the cracks so that measured relaxation results are not distorted.

4.4.5.1 As-Grown Cracking

Figure 4.33 shows the as-grown crack density for the RTG structures as the graded layer thickness was increased. Note that *total* thicknesses of the buffer are used to characterise samples are ~2 µm thicker than the buffer thicknesses reported in Table 4.3 due to the Ge underlayer and the SiGe cap. A critical thickness of 5.5 µm total RTG buffer thicknesses was measured for crack nucleation of the buffer during growth. When the thickness of the total RTG buffer was increased to 10 µm the as-grown crack density reaches 13.7 cm^{-1}. The average misfit between the SiGe cap and the Ge underlayer is f = -0.0074. Using this misfit value, the average values for the dimensions of a crack (Section 4.3.5) and the measured crack density, the relaxation due to cracking (Equation 2.36) of the buffer is 0.8 % relative to the Ge underlayer.

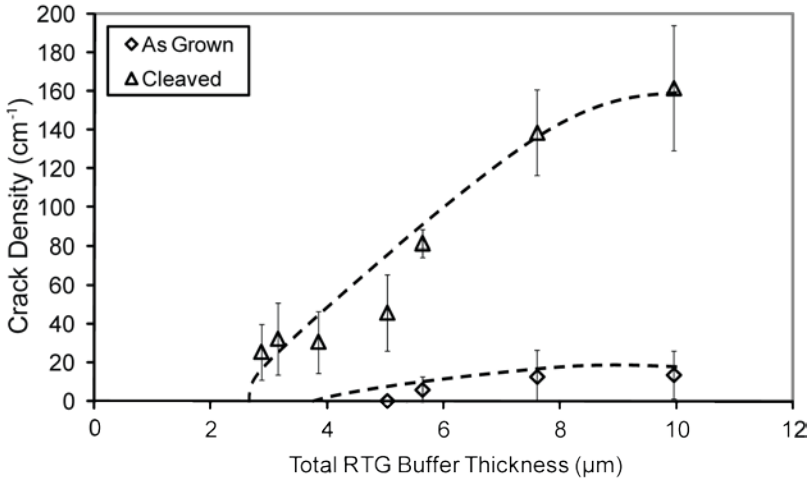

Figure 4.33: The measured crack density of RTG buffers against RTG layer thickness, it is observed that as-grown cracks are formed in significant densities. The lines shown are guides for the eye.

4.4.5.2 Induced Cracks

Figure 4.33 also shows the measured trend for induced cracks within RTG buffers. RTG structures are observed to be susceptible to induced cracking at similar buffer thicknesses as RLG buffers (Figure 4.21). A similar trend which is observed for RLG buffers between buffer thickness and ρ_{CD} is also observed for RTG buffers. Similarly, insignificant cracking densities are observed in wafers with total buffer thickness below 2.8 µm and are deemed to be free of induced cracks. The maximum induced ρ_{CD} observed within RTG buffers is 161.8 cm^{-1}. This occurs at a total buffer thickness of approximately 10 µm and equates to a relaxation of 9.6 % when compared to the Ge underlayer. The measured HR-XRD relaxation has again been corrected with the calculated relaxation from cracking in all presented relaxation data for RTG structures (Section 4.4.6)

4.4.6 Relaxation and Composition of RTG Buffers

An example of an RSM for an RTG buffer is shown in Figure 4.34 with separate peaks for each individual constant composition terrace shown. Note that the labels are the nominal compositions of each terrace.

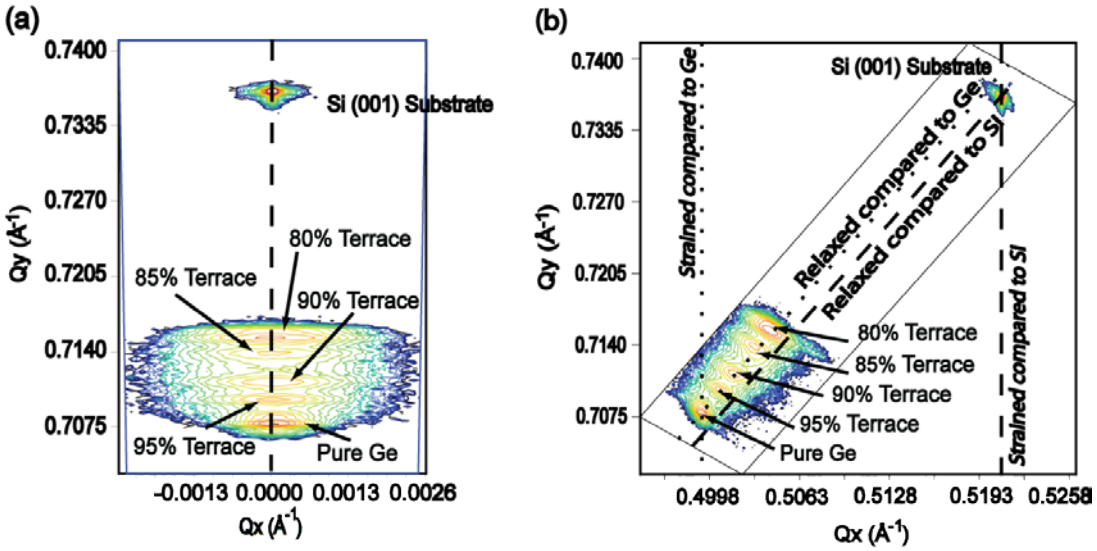

Figure 4.34: XRD RSMs of sample 4346 with a grading layer thickness of 3027 nm corresponding to an effective grading rate of 7.61 %/µm. a) (004) reflection, b) (224) reflection

Notice that the RSM of Figure 4.34 differs from that of Figure 4.22 for a RLG buffer in that features are now observed from each terrace of the RTG buffer. Thickness, SiGe cap (80 % terrace) compositions and effective grading rates are shown in Table 4.3. No significant tilt of the terrace is observed and high levels of relaxation for each terrace can be observed.

Figure 4.35 shows the crack corrected relaxation of the RTG buffers as effective grading rate is varied. Prior to crack correction the thickest buffer with an effective grading rate (RG_{eff}) of 2.89 % μm^{-1} was measured to have a relaxation of 88.6 %. Section 4.4.5 details the crack density within RTG buffers and an as-grown crack

relaxation of 0.84 % is calculated from those values. A relaxation of 9.6 % from induced cracking is also found. These calculated values lead to an *as-grown* relaxation of 79.8 % for the thickest RTG buffer.

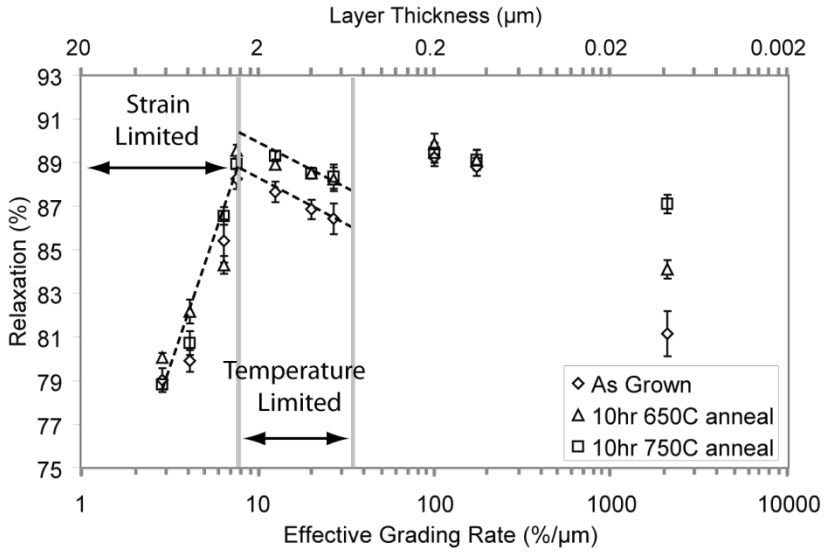

Figure 4.35: Relaxation of the top SiGe cap layer for RTG buffers as determined by HR-XRD. The relaxation was compared to the Ge underlayer and corrected for crack formation. A maximum relaxation is found at an effective grading rate of 7.61 % µm^{-1}. The lines shown are guides for the eye.

Two trends can clearly be seen in Figure 4.35, firstly as the effective grading rate (GR_{eff}) is increased from 2.89 % µm^{-1} to 7.61 % µm^{-1} the strain gradient within the buffer increases and is thought to be the limiting factor in this regime as relaxation is increased from 79.8 % to 88.3%. Secondly, as GR_{eff} is increased from 7.61 % µm^{-1} to 27.0 % µm^{-1} the relaxation decreases from 88.3 % to 86.4 %. This section of the trend is deemed to be the temperature limited regime. The higher GR_{eff} indicate thinner layers with shorter growth times and hence a reduced thermal budget. The optimal trade-off between minimal thickness indicating maximum strain gradient and maximum thermal budget is observed for a GR_{eff} of 7.61 % µm^{-1}. This GR_{eff} is shown to have a low TDD in Section 4.4.3 and corresponds to the optimal GR_{eff}

which is found. Annealing this buffer at 750°C for 10hrs increases relaxation to 89.6 %.

The thermal budget and strain gradient trade-off in RLG buffers occurs at GR_{RLG} = 61.3 % μm^{-1} with a maximum relaxation of 85 % (Section 4.3.6). Therefore the trade-off transition occurs in thinner RLG buffers, but a higher final relaxation of 88.3 % is achieved in RTG buffers. Stacking faults observed in sample 4343 (Section 4.4.4) do not show any retardation of relaxation and annealing does not increase relaxation. It is speculated that as the TDD level within RTG sample 4343 is an order of magnitude lower (~$10^7 cm^{-2}$) than that of RLG buffers containing stacking faults (~10^8 cm^{-2}) there are less mobile dislocations which can be hindered.

In summary, relaxation of all RTG buffers is high, as has been shown with RLG buffers. A GR_{eff} of 7.61 % μm^{-1} has been shown to maximise relaxation in RTG buffers through optimising the thermal budget and strain gradient. It has been shown that optimised relaxation occurs in thinner RLG buffers than RTG buffers.

4.5 Truncated RTG Structures

A separate set of wafers were grown to investigate the properties of the buffer throughout the RTG region at each constant composition terrace. The *overall* buffer thicknesses and final layer compositions are recorded in Figure 4.36. Sample 4339 was intended to be a copy of sample 4133 (Table 4.3) and was measured to have an effective grading rate of 6.30 % μm^{-1}, similar to that of sample 4133. The rest of this set of wafers was grown as truncated terraces from sample 4133 as demonstrated in

Figure 4.36. The average thickness of the Ge underlayer in Figure 4.36 is 1181 nm, as measured from TEM micrographs.

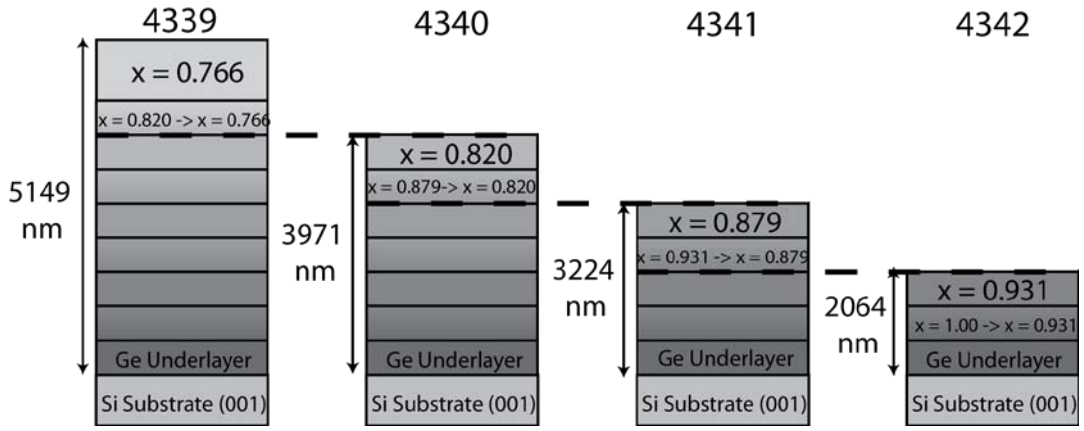

Figure 4.36: The overall buffer thicknesses and compositions for the set of truncated terraces. The average thickness for the Ge underlayer is measured to be 1181 nm. The overall structure, sample 4339 was intended to be a copy of sample 4133 with an effective grading rate of 6.30 % µm^{-1}.

4.5.1 Surface Roughness of Truncated RTG Buffers

Mobile adatoms will incorporate into the lower energy sites if a strong enough strain field from the misfit dislocation network is present, this will reduce the roughening of the layer. This can be confirmed by analysis of Figure 4.37 which shows the RMS surface roughness of the truncated set of RTG wafers.

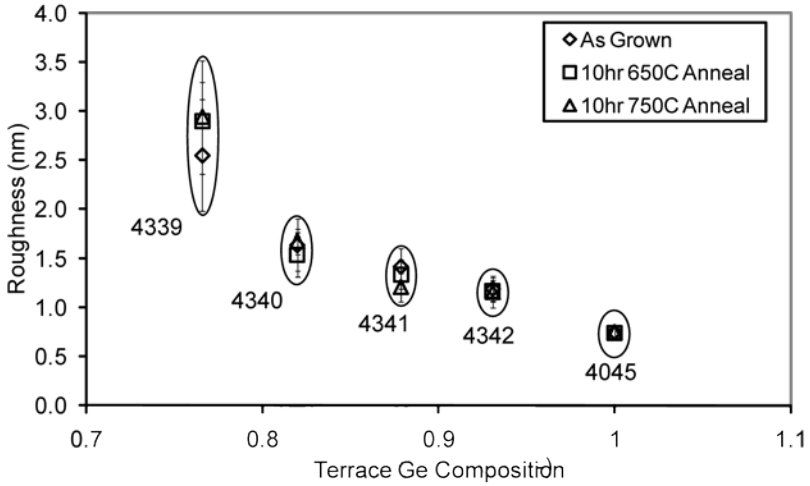

Figure 4.37: The RMS surface roughness of the top constant composition layers of the truncated RTG structures. The majority of the roughness of the buffer is observed to evolve within the final terrace of the RTG structure.

The surface evolution of the graded region can be seen through the 3D representations of the RTG buffer surface in Figure 4.38. The surface of the Ge underlayer is shown in Figure 4.38a), where crosshatch does not appear to be the main roughening mechanism. Continued growth on top of the Ge underlayer shows that the crosshatch becomes the prevalent roughening mechanism with a final roughness of 2.6 nm, seen in Figure 4.38e). The main increase in roughness is seen to be incurred from the deposition of the last terrace, which increases the RMS surface roughness (height range) from 1.6 nm (10.7 nm) to 2.6 nm (14.4 nm). Annealing of the truncated set of wafers at 750°C for 10 hours only shows an increase of roughness of the full structure, sample 4339, to 2.9 nm. This suggests that the thicker SiGe cap layer induces the most roughness as the mobile adatoms are not rearranged due to the strain field from the misfit dislocation network as it is further away from the surface of the wafer. However this 0.3 nm increase in roughness is at the limit of AFM scan resolution and is within error, so cannot be confirmed as a reliable result.

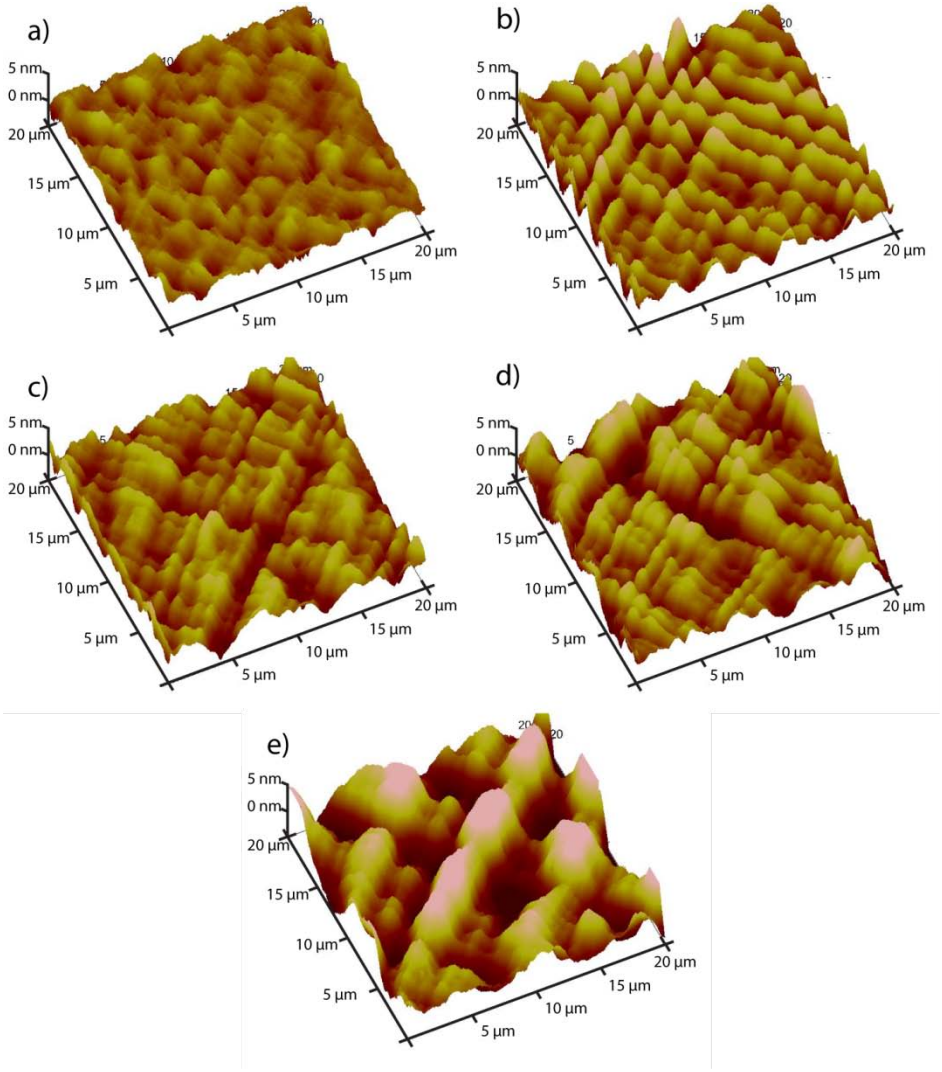

Figure 4.38: 3D representations of AFM scans for the truncated set of samples a) 4045, b)4342, c)4341, d)4340 and e)4339. The evolution of the sample surface can be observed to develop severe crosshatch within the last terrace of the RTG buffer.

4.5.2 Relaxation of Truncated RTG Buffers

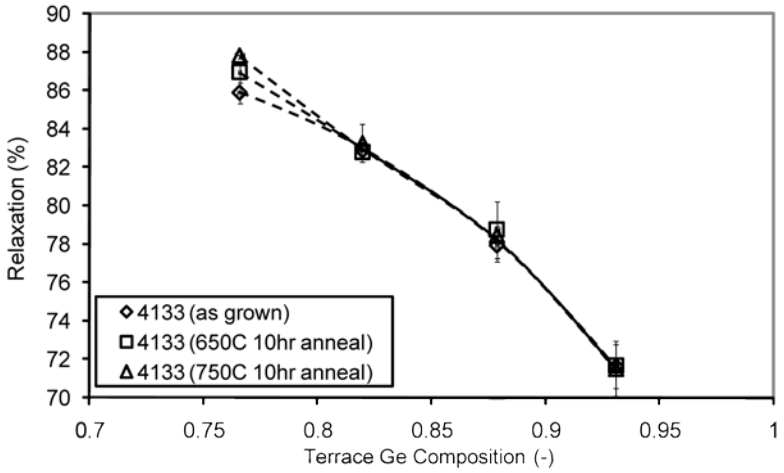

Figure 4.39: The crack corrected relaxation of sample 4339 with effective grading rate of 6.30 % µm^{-1}. As can be seen negligible relaxation occurs within the underlying terraces when post growth *ex-situ* anneals are performed. The lines shown are guides for the eye.

As individual terraces can be resolved through HRXRD an analysis of relaxation through the structure was performed for sample 4339, the "full" RTG structure in the truncated terrace set, these results are shown in Figure 4.39. The relaxation shown is corrected for induced cracks and compared to the Ge underlayer for the measured composition for the terrace. It is observed that most of the relaxation for the buffer occurs within the first terrace which has a composition of 0.931 and a relaxation of 71.5 %. The SiGe cap as-grown relaxation is calculated to be 85.8 %, which is increased to 87.8% after a 750°C anneal for 10 hours. The underlying terraces are not observed to change relaxation on annealing.

The set of truncated terraces are also analysed through HR-XRD, the overall buffer thickness and top layer compositions of these layers are detailed in Section 4.5. Figure 4.40 shows that the as-grown relaxation of each terrace is similar to that of the "full" RTG structure (sample 4339) and within experimental error (<0.7%).

Annealing these structures, however, is observed to increase the relaxation of the terraces. For the terrace of composition 0.931 the relaxation is enhanced from 71.5 % to 76.3% by annealing the buffer at 750°C for 10 hours. The same effect is observed within all truncated terrace samples, this is shown in Figure 4.40. It is postulated that the material grown on top of each terrace in the full buffer (sample 4339) increases the length of the threading arm and hence raises the energy barrier for the whole arm to glide which by definition increases resistance to motion (Equation 2.18). A similar effect was observed by Hull [43] where the dislocation velocity within lower composition forward graded samples was measured. A series of buffers both with and without constant composition caps were analysed and it was found that the buffers with caps had lower dislocation velocities.

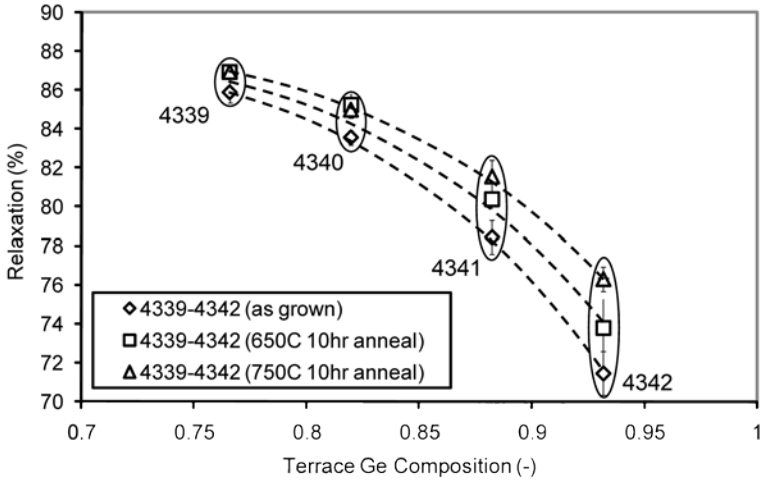

Figure 4.40: The relaxation of the top constant composition layers of the split RTG structures in which it is observed that intermittent annealing induces more relaxation than anneals performed post growth. The lines shown are guides for the eye.

Separate terraces were grown to investigate the effect of annealing on individual terraces and are found to induce further significant (>5 %) strain relaxation when compared to full RTG structures.

4.5.3 Dislocation Densities within Truncated RTG Buffers

Figure 4.41 shows the dislocation density within the truncated terrace set of RTG wafers. This provides a measure of the dislocation density throughout the graded region of a RTG buffer with a GR_{eff} of 6.30 % μm^{-1}. The first terrace with a Ge composition of 0.931 (sample 4342) was measured to have a TDD of 2.8 x 10^6 cm^{-2}. This is almost an order of magnitude lower than the Ge underlayer. It is therefore assumed that a large degree of annihilation occurred between these layers.

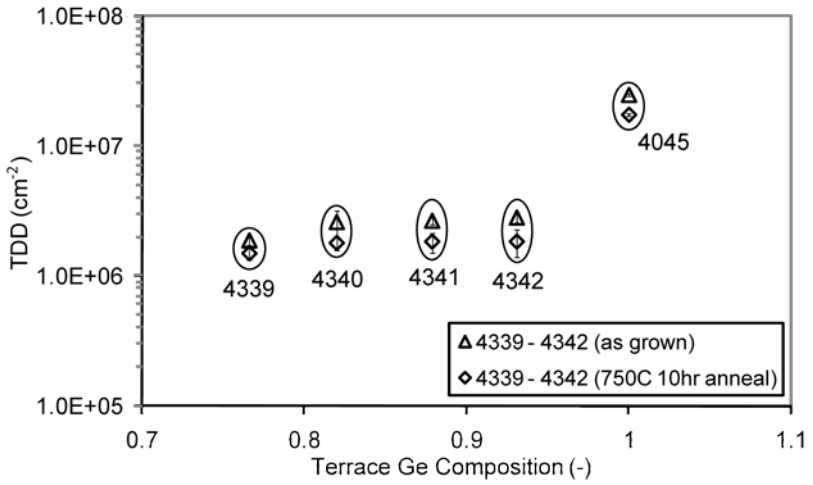

Figure 4.41: The dislocation density of the top constant composition layers of the truncated RTG structures. The majority of dislocations are shown to annihilate within the first terrace and subsequent terraces show reduction of dislocation density.

The final "full" RTG structure (sample 4339) is shown to contain a TDD of 1.9 x 10^6 cm^{-2}. This indicates that the dislocation annihilation rate is still larger than the nucleation rate after continued grading of the buffer. This observation coupled with the exponential decrease in probability of annihilation [128] corresponds with the dislocation density trend observed within the higher terraces. Additionally, these

measurements support the observation which is reported in Section 4.5.2 which states that the majority of the strain is relieved within the first terrace.

An anneal of 750°C for 10 hours shows that the TDD of each sample decreases. It is postulated that this reduction through annihilation is only possible when the terrace in question is the terminating surface. This postulation is again supported by the measured relaxation of separate terraces (Section 4.5.2), as relaxation of each terrace is only seen when it is annealed and is the *terminating surface*. Post-growth annealing lowers the dislocation density within the first terrace to 1.8×10^6 cm^{-2} and also lowers the TDD within the "full" structure to 1.5×10^6 cm^{-2}.

4.6 Modelling of Critical Thickness for Cracks

A solution presented to prevent cracking of the buffer was to grade at a higher rate, making the overall buffer thinner. This is thought to reduce the amount of strain energy in the buffer. Another solution presented was to reduce the amount of tensile strain in the top layer, or ensure the top layer was under compressive strain. The importance of the thickness of the buffer and its final relaxation is theoretically investigated in this section.

4.6.1 Dependence of Buffer Relaxation

During device fabrication the buffer may be subjected to high temperature processing and must remain stable. Relaxation under tensile strain, rather than compressive, has its benefits which are listed in Section 2.5. However, cracking of the layer can become a serious problem. In this section modelling is performed to find the

properties for a stable buffer using Equation 2.30 from Murray et al [63] (Section 2.5.5).

The critical cracking thickness throughout the graded region was calculated by Equation 2.30 which requires information about the strain (and therefore the relaxation) throughout the graded region. This information is provided in Section 4.5.2, which reports the relaxation of different terraces within the RTG region. From these results, relaxation was calculated as an empirical function of composition within the graded region. Functions of relaxation could then be found for different theoretical top SiGe cap layer relaxations of 0%, 60% and 90% for an RLG structure. Figure 4.42 shows the critical cracking thickness during grading of an RLG region which is calculated by Equation 2.30 utilising these empirical relaxation functions, a Ge underlayer thickness of 1 µm, a GR_{RLG} of 4.69 % μm^{-1} and a SiGe cap thickness of 1 µm.

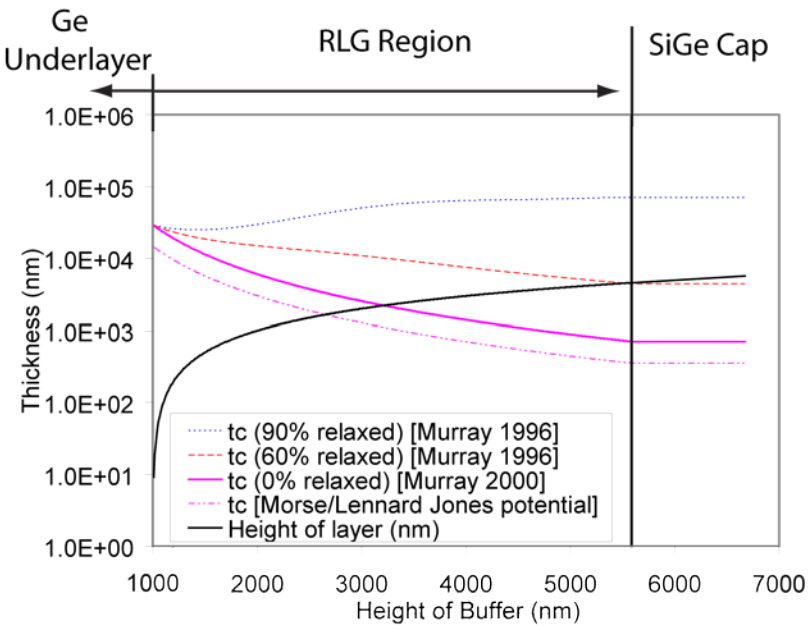

Figure 4.42: The critical thicknesses for cracking. Shown are the critical cracking thicknesses for different relaxations of the top constant composition cap layer. When the height of the buffer (black) is equivalent to the critical thickness in the layer cracks will start to form in the reverse graded buffer.

The pink lines indicate the critical cracking thickness for a fully strained *pseudomorphic* RLG layer (0% relaxation). The thicknesses at which these lines equal the height of the RLG buffer (black line) are where cracks are likely to form if no other relaxation mechanisms take place within the graded layer. The solid and dotted pink lines indicate different crack formation potentials, one used by Murray [63] and the Morse/Lennard-Jones potential used by Kelly [64] (Section 2.5.5). These equal the thickness of the graded layer at 3.3 µm and 2.7 µm respectively. The potential used by Murray is used within the other calculations of higher relaxation.

The red dashed line shows the critical crack thickness for a graded region with a top layer relaxation of 60 %. This relaxation is shown to be the "critical relaxation" of the calculated reverse graded buffer (GR_{RLG} = 4.69 % μm^{-1}) as the final critical crack

thickness is equal to the total thickness of the graded region. If the final relaxation of the buffer is lower than 60% then cracks are thought to form during growth.

The blue dotted line shows the critical cracking thickness throughout the graded region for a final SiGe cap layer relaxation of 90 %. This relaxation is close to the levels measured in the RLG buffers (Section 4.3.6). The critical thicknesses for this relaxation do not equal the actual layer thickness at any point within the structure, indicating that cracking should not occur during growth of a 4594 nm thick graded region. This is supported by the insignificant as-grown crack density of 1.2×10^{-2} cm^{-1} observed in wafer 4054, with $GR_{RLG} = 4.69$ % μm^{-1} (Section 4.3.5).

The calculation was then performed with a reduced graded region thickness of 0.7 µm ($GR_{RLG} = 28.6$ % μm^{-1}) and calculated together with the SiGe cap as pseudomorphic layers on the Ge underlayer. This calculation gave a critical cracking thickness of 2.7 µm, it is noted that this is almost equal to the height of the buffer. Therefore it is argued that a total thickness of approximately 2.7 µm is the critical cracking thickness for *pseudomorphic* reverse graded buffers. It is interesting to note that the measured buffer thickness at which cracks are actually induced within reverse graded buffers is around 2.7 µm to 2.8 µm (Section 4.3.5 & 4.4.5). This suggests that the cleaving process fully strains the epitaxially grown buffer before induced cracking actually occurs. These thicknesses are then considered as the worst-case scenario values for cracking in reverse graded buffers.

4.6.2 Dependence of Buffer Thickness

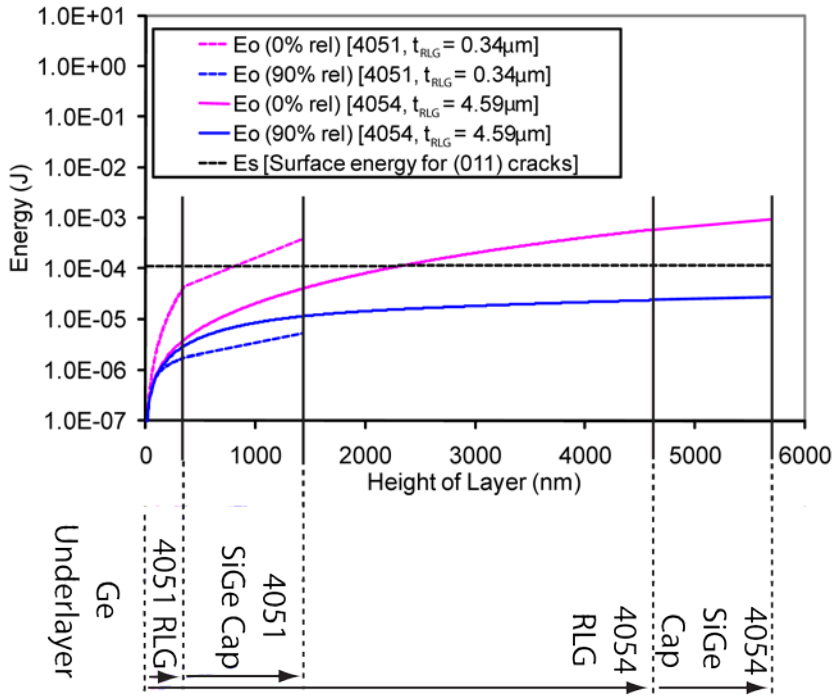

Figure 4.43: An energy diagram showing Es (dotted black) the energy needed to create a (011) free surface. Eo represents the accumulated tensile strain energy of the layer. Solid lines represent the tensile strain energy within the thickest sample, 4054, whereas coloured dotted lines represent a thinner sample. Pink lines imply no relaxation throughout the structure and blue lines imply the structure has a top layer relaxation of 90 %.

Only the grading region thickness is varied for the study performed in Section 4.3. Therefore the total thickness of the buffer can be minimised by reduction of the Ge underlayer and SiGe cap thicknesses. Currie *et al* proposed a method to suppress the formation of cracks by reduction of the graded layer thickness and hence the reduction of the potential energy stored within the system. Figure 4.43 shows a comparison of the accumulated energy stored within two samples with a graded layer thickness of 0.34 µm (dashed lines) and 4.59 µm (solid lines). These thicknesses were chosen to emulate actual RLG wafers 4051 and 4054 respectively (Section 4.3). These samples were calculated with a 1 µm $Si_{1-x}Ge_x$ cap of composition x = 0.78 and a top layer relaxation of 90 % along with fully pseudomorphic versions of the

same structures. The crack formation potential used by Murray (Equation 2.29) is used in these calculations. The energy accumulated in the 90 % relaxed buffers is shown using the blue lines within Figure 4.43. The pink lines show the accumulated strain energy if the buffers remain fully pseudomorphic and do not relax through dislocation dynamics. The black dotted line represents the energy required to create the free surface of a crack on the (011) plane.

The tensile strain energy stored within the thicker 90 % relaxed buffer does not acquire enough energy to create a free surface, and retains even less energy when the thickness is reduced. This indicates that if buffers were not strained during sample preparation or device processing the buffers would not be likely to crack.

If the graded region remains fully strained (pink lines), the thicker layer is shown to nucleate cracks during growth of the grading region at a thickness of 3.3 µm, which corresponds to the results for the previous calculation (Figure 4.42). Reduction of the graded layer thickness to 0.34 µm is shown only to delay crack generation. However, the thinner pseudomorphic sample is shown not to accumulate enough energy to nucleate cracks at the end of its *graded region*. It is the thick constant composition SiGe cap that stores the energy to form cracks within this sample. Within this chapter the thick constant composition SiGe cap layers are grown for ease of characterisation of the buffers. A study in Section 5.3 reduces the thickness of this layer.

Relaxation under tensile strain routinely occurs through misfit and threading dislocation nucleation and glide during growth of the reverse graded buffers. When the surface of buffer is rougher and the tensile strain gradient is of higher magnitudes

stacking faults are generated which allow a greater degree of relaxation per defect. However, if these processes do not achieve a suitable level of relaxation cracking of the buffer can occur and will penetrate into the Si(001) substrate. When samples are cleaved the buffer is speculated to be artificially locally fully strained and generate cracks. The crack densities which are shown in Figure 4.21 and Figure 4.33 are seen to increase as the thickness of the buffer is increased. The maximum induced ρ_{CD} for an RLG system was measured to be 77.7 cm^{-1} and the maximum induced ρ_{CD} for an RTG system was 161.8 cm^{-1}. This increase in ρ_{CD} is attributed to the increase of potential strain energy stored in thicker buffers. Calculations of strain within the reverse linear graded buffers show that if the thickness of the RLG layer is minimised and the relaxation from dislocation nucleation or glide is maximised then crack generation is suppressed. A critical crack thickness of 2.7 μm which is thought to withstand stress based fabrication techniques has been determined experimentally and theoretically for the reported reverse graded buffers.

4.7 Discussion and Conclusion

The mechanism for relaxation within the reported reverse graded structures is different to that proposed by Wong *et al* [99], in which low composition (<35 % Ge) "jump-graded" buffers are studied [58]. Due to the composition jump at the interface between the Si(001) substrate and the RLG layer it was reported to be the main site for relaxation through dislocation nucleation, glide and multiplication from the generation of modified Frank Read (MFR) loops within the Si(001) substrate while the strain acquired through the graded layer aided annihilation of threading dislocations.

Huang *et al* [94] have calculated the surface segregation of SiGe alloys on Si (001) and Ge (001) substrates. They found that SiGe growth on a Ge (001) substrate (or layer) has less surface segregation when compared to growth on a Si (001) substrate which will lower the roughness of the layer and have a minor effect in suppressing Stranski-Krastanov <001> growth. Surface segregation cannot occur during growth of pure Ge on Si(001) as no Si adatoms will be present during growth.

Dutartre *et al* [77] also showed that for forward graded buffers the grading rate must be increased to minimise the thickness of the layer and maximise the strain in the layer. This was to enhance dislocation glide velocity whilst maintaining a low enough grading rate as not to nucleate dislocations. However, when grading rates are too high the radial strain field generated by misfit dislocations is closer to the growth surface. This has been shown [44] to allow surface mobile adatoms to travel from low energy sites to higher energy sites, increasing the roughness achieved from crosshatch. This effect is seen in Section 4.3.2 when the growth occurs under a 2D Frank-van der Merwe growth mode. However when grading rates are even higher (GR_{RLG} > 124 % μm^{-1}), the prevalent roughening mechanism in buffers is 3D Stranski-Krastanov <001> hillock growth (Section 4.3.2). This is seen within the AFM surface scan in Figure 4.13b).

The crosshatch feature will expand across the surface of the wafer along the <110> direction and therefore will have a higher probability of blocking mobile dislocations when compared to <001> hillocks. It is suggested here that even though low roughness is required for dislocation glide, hillock formation is more preferable than crosshatch in terms of keeping the mobile dislocation density high.

Wafer Number	Graded Region Thickness (±2 %) (nm)	Grading Rate (±1 %) (% μm^{-1})	Threading Dislocation Density (±10 %) (cm^{-2})	Stacking Fault Density (±5 %) (cm^{-1})	Cleaved Crack Density (±25 %) (cm^{-1})	SiGe Layer Composition (±0.5) (%)	Relaxation compared to Ge Underlayer (±0.5) (%)	Rq (RMS Roughness) (±0.2 nm) (nm)
4345	1844	12.62	2.1 x 10^{6}	0	30.7	76.5%	89.2%	1.9
4053	1885	11.35	3.3 x 10^{6}	0	59.7	78.4%	84.7%	1.9

Table 4.4: The measured and calculated properties for the best RLG and RTG wafers. Notice that when the wafers are cleaved the top layer is susceptible to cracking.

From experiments Fitzgerald *et al* [129] and Dutartre *et al* [77] have shown that an optimal grading rate for low TDD forward graded SiGe systems is around 10 % μm^{-1}. If induced cracking of the reverse graded buffers is ignored then the best grading rate for the reverse graded wafers is shown to be of the same magnitude, the properties of these wafers are shown in Table 4.4. Dutartre reports the "critical grading rate" for full relaxation of the buffer to be 185 % μm^{-1} to avoid severe dislocation nucleation, for TDD densities of 10^{9} cm^{-2}. However, all TDDs levels measured in the present work are lower than 10^{9} cm^{-2}.

For TDD levels which are of the order of 10^{6} cm^{-2} a forward grading rate of ~10 % μm^{-1} must be used (Section 2.6.3). The presented study shows TDD values of 10^{6} cm^{-2} for reverse grading rates between 10 and 100 % μm^{-1}. As shown in Section 4.3.3 the glide regime occurs below a reverse grading rate of 124 % μm^{-1} in which TDD values are still of the order of 10^{6} cm^{-2}. It is speculated that the reason for the higher grading rates in reverse graded structures which produces a thinner graded region when compared to forward grading is due to two reasons. Firstly (and most importantly) the increase in dislocation glide velocity [43] from the higher composition of the buffer will increase the probability of annihilation within the graded region. Secondly, the decrease of resistance to glide from the thinner graded

region which will lower the Peierls barrier along the entire threading arm [38]. Tuppen and Gibbings [40] calculated misfit dislocation velocities through experimentation and found an increase of threading arm length decreases dislocation velocity.

For the reverse graded buffers which are studied in this chapter, homogeneous nucleation of dislocations is unlikely due to the small misfit ($\varepsilon < -0.01$) between the Ge underlayer and the SiGe cap, where a strain of $\varepsilon > -0.02$ is required for homogenous nucleation [43]. When thinner samples with a grading rate of above 124 % μm^{-1} were analysed using TEM, limited modified-Frank-Read (MFR) loops were observed (Section 4.3.3). This suggests dislocation nucleation above this grading rate is by both multiplication and heterogeneous nucleation from surface roughness.

The possibility of a high heterogeneous nucleation rate from surface roughening is indicated in Figure 4.15 as the roughness increases linearly from a GR_{RLG} of 2100 % μm^{-1} to 124% μm^{-1} (Figure 4.12). However, the maximum TDD is achieved for a GR_{RLG} of 174 % μm^{-1}. The RLG sample 4128 (GR_{RLG} = 124% μm^{-1}) has limited MFR loops (Figure 4.16b)) and a maximum RMS surface roughness of 34.6 nm with a TDD of $2.6 \times 10^{7} cm^{-2}$. As the TDD is equal to that of the Ge underlayer the nucleation rate and annihilation rate are equal. Therefore if the MFR mechanism is reduced then the high nucleation rate in this sample is speculated to be due to a heterogeneous nucleation.

It is shown within RLG layers that reverse grading rates of below 61.3 % μm^{-1} are grown in a 2D growth mode (Figure 4.11). The relatively higher growth temperature along with the smoother surface achieved from tensile strain [130] reduces MFR and heterogeneous nucleation. The reduction of TDD reduces the surface strain field associated with threading dislocations, which in turn further reduces surface roughness. This avoids the vicious cycle of surface morphology affecting dislocation glide [49], which produces a pileup of threading arms which sequentially reduces the local growth rate around arrested dislocations and creates a rougher surface.

Within the reverse graded structures the dislocations generated during the Ge underlayer deposition will be grown from the underlayer into the epilayers above it. This will provide threading dislocations which are able to glide at misfit interfaces to from misfit dislocations [131]. This requires less energy than heterogeneous dislocation half loop generation or multiplication [14]. The high density of dislocations is speculated to reduce the initial glide velocity of dislocations. As the layer relaxes, the misfit dislocation length required per threading arm will be shorter when compared to the length needed for strain to be relieved by a buffer with a low density of dislocations already generated. Equation 2.37 is a simplified version of a differential equation which will accurately model glide of dislocations within a forward graded layer [75]. The limitations on the equation are that it is a representation for thick graded buffers, it is a steady-state equation and only a model for glide of dislocations and as such assumes that annihilation and nucleation rates are equal. The reverse graded layers can be modelled by this equation by changing the fitting constant, B, in Equation 2.37. The constant B also represents the initial glide velocity of dislocations when compared to Equation 2.14. Grading rates of

above 61.3 % μm^{-1} in which the nucleation rate is higher than the annihilation rate cannot be modelled by this equation as they are too thin and the roughness of the layers becomes a limiting factor due to heterogeneous dislocation nucleation.

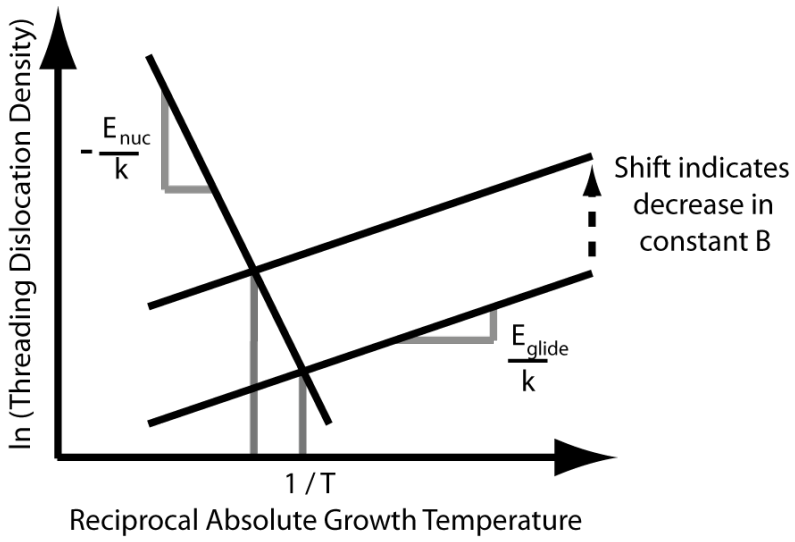

Figure 4.44: Adapted from Issacson *et al* [44]. A representation of the nucleation and glide limited regime. The grey vertical lines represent the different temperatures at which regimes are reversed, the right side of these boundaries is the glide dominated regime and the left is the nucleation dominated.

Isaacson *et al* [44] suggest the dislocation nucleation regime is partly temperature limited within forward graded structures with the effect of lower temperature growth limiting the nucleation of dislocations whilst encouraging glide. Figure 4.44 shows a schematic of the nucleation and glide limited regimes as a function of growth temperature. When the initial glide velocity B is reduced it increases the temperature of the regime transition, this is shown on Figure 4.44.

Layers in this study have a growth temperature of 850°C which is close to the melting point of the high composition alloys. A thermal energy (kT) of 0.1 eV is calculated from this growth temperature which is proportionally much lower than the 40 eV required for homogeneous dislocation nucleation (Section 2.4.5). Therefore as

the misfit in the studied buffers is low (< 0.02), the homogeneous nucleation in these buffers is low at these temperatures. Within *forward* graded buffers of sufficient misfit this relatively high temperature could start to nucleate half loops due to loss of solid-solution strengthening [132] and excessive strain. It is surmised in reverse graded buffers this temperature limited regime has been increased by the high initial TDD to allow higher relative growth temperatures. The increase in growth temperature will indirectly allow reduced growth times due to the resultant increase of glide velocity of dislocations and directly due to the faster growth rate of precursors through CVD.

$$\ln(\rho) = \frac{Eglide}{kT} + \ln(A) - \ln(B) \qquad \textbf{Equation 4.1}$$

Equation 4.1 shows the rearranged model presented in Section 2.6.3 which was reported by Fitzgerald *et al*. Where $A = (2R_g R_{gr})/(bY^m \varepsilon_{eff}^m)$. The reverse graded layers are modelled using values R_g = 4.5 nm s^{-1}, R_{gr} = -6.30 % μm^{-1}, b = 1.98 Å, B = 0.007 m s^{-1}, Y = 108.7 GPa, m = 1, ε_{eff} = -0.0017, E_{glide} = 1.72 eV and T = 850°C. The fitting constant B has been decreased from the value used by Fitzgerald, speculated to be due to the increase of the initial TDD. Figure 4.45 shows the calculated TDD values throughout the graded region alongside the values measured for the truncated set of RTG wafers (Section 4.4.3). It can be seen that the theoretical prediction of TDD is within error of measured values, excluding the very last terrace. Equation 4.1 produces a value of 3.2 x 10^6 cm^{-2} for the very last terrace and a total TDD 1.9 x 10^6 cm^{-2} has been found from measurements of the truncated RTG samples with a GR_{eff} of 6.30 % μm^{-1}. The difference between the values of the

modelled and measured layers can be explained by the increased thermal budget used to grow the thick constant composition SiGe cap, as the equation does not account for this or any subsequent annealing steps performed.

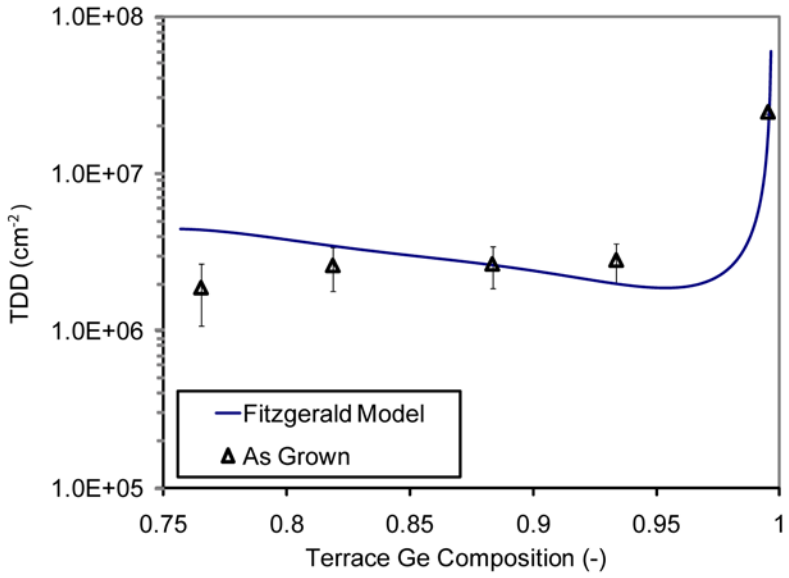

Figure 4.45: A comparison of the model presented by Fitzgerald *et al* with values measured in the truncated RTG set.

A variation of grading rates and effective grading rates, for reverse terrace graded buffers, allows the buffer to be grown in various modes and mechanisms which interact with each other. This method of buffer fabrication is unique in the fact that the relaxed Ge underlayer has a large density of threading dislocations which has been speculated to allow a higher growth temperature. Samples with total buffer thicknesses of up to 4 µm show excellent layer properties, and do not develop cracks during growth. A major concern is that cracking could occur during device processing but it has been shown that a total buffer thickness of 2.7 µm suppresses any cracking tendencies when the wafer is subjected to external stresses. Therefore it is suggested that a reduction of the Ge underlayer and the final SiGe constant cap

thickness is required to achieve the best overall properties within a reverse graded buffer and this is further investigated in Chapter 5.

4.8 Comparisons with other buffer fabrication techniques

Technique	Thickness of buffer (um)	Final Composition (% Ge)	Relaxation (%)	RMS Roughness (nm)	TDD Values (cm^-2)	Author(s)	Notes
Ge Condensation	0.2 to 0.035	82%	78 %	1.3	(0.9 to 1.5) x 10^8	Nakaharai *et al* [85]	Si-on-Ge platforms and oxidisation needed
Ion Implantation	1.4	47%	Induces an extra 10% relaxation.	0.45	-	Hoshi *et al* [92]	Mid-growth ion implantation needed
Low Temperature Method	1.65	90%	> 90 %	5.9	3 x 10^6	Peng *et al* [93]	Developed on a 27% fully relaxed buffer and anneals were performed
2-Temperature Method	1.1	100%	104 %	0.7	2 x 10^7	Luan *et al.* [98]	Segregation effects possible for SiGe alloys
Linear Grading	12	100%	99 %	47	(1 to 5) x 10^7	Currie *et al*. [62]	CVD grown samples, pile-up observed
Linear Grading with CMP	~10	88%	104 %	17	1 x 10^5	Bogumilowicz *et al* [30]	Mid-growth CMP employed, no pile-up observed.
Thinner Reverse Linear Grading	2.4	78%	107 %	3.0	4.5 x 10^6	Present work.	No cracks observed. Relaxation compared to Ge underlayer is 86 %.
Thicker Reverse Linear Grading	4.2	78%	106 %	1.9	3.3 x 10^6	Present work.	Cracks form when cleaved, relaxation compared to Ge underlayer is.85 %
Reverse Terrace Grading	3.9	77%	107 %	1.9	2.1 x 10^6	Present work	As above. Relaxation compared to Ge underlayer is.89 %

Table 4.5: The comparison of critical parameters for a high composition (>75 % Ge) buffer structure for different methods

A comparison of the best buffers characterised within this Chapter is presented in Table 4.5 alongside characteristics of other major strain tuning buffer techniques

which are described in Section 2.6. The thickness of the buffers is important as it determines the growth time and the amount of material used during growth. Many of the buffer techniques mentioned in Section 2.6 have thicknesses below 2 µm but require *ex-situ* processes to be performed and also have a reduced layer quality.

Ge condensation [85] requires oxidisation and SOI/SIMOX platforms and results in a TDD to the order of 10^8 cm^{-2}. Ion implantation [92] requires high energy implantation and only induces an insignificant further relaxation within the layer. The low temperature method [93] was grown on a fully relaxed 27 % SiGe buffer and *in-situ* anneals were performed, which resulted in a low TDD of 10^6 cm^{-2} but at a cost of the increased roughness of 5.9 nm. The two temperature method [98] has only been investigated for pure Ge layers, but is thought by the author to require complementary precursors to minimise surface segregation and is speculated to still incur strain based segregation effects [94]. All of these methods have lower thicknesses than reverse graded buffers. Forward graded buffers are very thick (> 10 µm) [129] due to the grading rate needed to avoid nucleation of dislocations in the buffer.

Surface roughnesses which are seen to be suitable for 45 nm node processing are around 1 nm [133]. The methods which are suitable for processing this node technology and yield an RMS surface roughness lower than the best reverse graded buffers, are the Ge condensation technique, Ion implantation and the two temperature method; however these methods have drawbacks which are mentioned above. The defect levels superior to the levels found in reverse grading are only seen in forward graded buffers which have had mid-growth CMP performed. As mentioned

previously the thickness of these buffers and the roughness incurred are too great to consider linear grading as a practical device platform with a fast throughput as CMP will be required post growth. Overall the method which can be comparable to reverse graded wafers for high Ge composition buffers is the low-temperature (LT) method. The thickness of the LT buffer is less than half of the best reverse graded region buffers with similar low TDD levels and high relaxation levels, although a higher roughness is incurred in the LT buffer.

4.9 Summary

A new adaptation of reverse grading for high composition ($x \approx 0.8$) $Si_{1-x}Ge_x$ buffers is proposed for strain tuning and optoelectronic applications. The difference between the work presented and previous studies is that high Ge compositions buffers are intended and a fully relaxed highly defected pure Ge underlayer is deposited prior to grading.

The effect of varying the grading rate by changing the graded region thickness with a constant end composition is reported. All samples have been measured with a thick 1.1±0.2 µm $Si_{0.22}Ge_{0.78}$ constant composition cap and a thick 1.1±0.2 µm tensile strained Ge underlayer. When the constant composition SiGe cap was deposited directly on the Ge underlayer <001> Stranski-Krastanov growth was observed. With the 3D growth came a severe increase in threading dislocation density and increased roughness.

A critical grading rate of 124 % μm^{-1} was found. When grading rates of less than 61 % μm^{-1} are used glide of dislocations is the prevalent relaxation mechanism. This

promotes annihilation of threading dislocations which reduces the dislocation density within the layer and stacking fault generation is avoided. Grading rates below this critical grading rate enter a 2D layer by layer growth mode, although crosshatching still occurs if the grading rate is kept relatively high. As can be seen in Table 4.5 a comparison of a thick and thinner RLG is compared as well as a thick RTG buffer along with other methods of high Ge composition buffer fabrication.

The best grading region which has been found within the study are RLG buffer 4053 (11.4 % μm^{-1}) and RTG buffer 4345 (12.6 % μm^{-1}), the properties of these buffers are seen in Table 4.4. The total thicknesses for these buffers are limited by the thick Ge underlayer and the SiGe cap. However, the best RLG and RTG buffers are still 60 % thinner than linear graded buffers with CMP employed and are also over 8 times smoother [49]. If the end application does not require a stress-based wafer division technique then these wafers are ideal as they have the best properties of the buffer and do not generate cracks during growth. However, if the wafer is to be cleaved or separated using a stress-based technique or requires the thinnest buffer then an RLG layer thickness of 0.34 µm can be used. The characteristics of this buffer are listed in Table 4.5. This buffer yields a roughness 50% rougher with twice as many dislocations but has a buffer thickness almost half that of the RLG and RTG buffers.

The reverse graded buffers have two main limitations firstly; it is postulated that the underlying dislocation density from the Ge underlayer limits the final TDD value. This limits the minimum TDD to 2×10^6 cm^{-2}, which has 20 times [62] the TDD when compared to linear graded buffers with mid-growth CMP. This TDD value is

still less than that of traditional forward graded buffers and requires no processing mid-growth. Secondly, the weakness to induced cracking of the top layer, this demonstrates a potential risk when buffers undergo device fabrication as the best RLG and RTG buffers are not observed to crack during growth of the buffer. Cracking does not occur within other methods of buffer fabrication as relaxation normally occurs under compressive strain. Modelling of the buffer structure demonstrates how a reduction in the thickness of the buffer below 2.7 μm can prevent induced cracking. This proposed solution is investigated in Chapter 5. RLG buffers have promising qualities though require a great deal of development before practical implementation can be achieved.

5 Development of Substrate Design

5.1 Introduction

The tensile strained germanium underlayer (Section 4.2.1) used throughout this work is grown by the two temperature method and reported in several sources [98] & [41] & [95] for its high quality. However, it is a thick layer and makes up a significant fraction of the reverse graded buffers. The SiGe cap also contributes additional thickness which is not necessarily required of the buffer and can therefore be reduced. Reduction of the buffer thickness will not only suppress induction of cracking but also reduce growth time and resources. The errors in measurement values which are used in this section are the same as stated for Section 4.3, unless otherwise stated.

5.1.1 Standard Relaxed Graded Layer

In order to study the effect of reducing the Ge underlayer and SiGe cap thickness in reverse graded buffers, the graded region must be reproducible in each sample. The growth-optimised graded region of wafer 4046 (Section 4.3.1) was used throughout this chapter in order to avoid growth related composition mismatch effects at epitaxial interfaces (Section 4.4.1). This wafer reported an overall buffer thickness of 3203±2% nm with a graded region thickness of 931±2% nm. The grading rate was calculated to be 23.1 % μm^{-1} with a SiGe cap of 78.4±0.5 % Ge composition. The as-grown TDD reported for this layer was $4.2\pm1 \times 10^{6}$ cm^{-2} and an RMS surface roughness of 3.1±0.2 nm was measured. The buffer does not develop cracks during growth but is seen to induce cracks when cleaved.

5.2 Optimising the Two Temperature Ge Underlayer

To the author's knowledge an in depth investigation of the two temperature Ge underlayer has not been published. Section 2.6.8 describes the dislocation dynamics and the growth mechanisms in this method of buffer fabrication. The low temperature (LT) Ge seed layer is thought to generate a high density of dislocations and keep the growth surface in a 2D growth mode, whilst retaining crystallinity within the layer. The high temperature (HT) layer is thought to purely reduce the roughness of the surface incurred during seed deposition. A final anneal is responsible for relaxation through dislocation glide and reducing the TDD through threading arm annihilation in the Ge layer.

The growth parameters used for the LT layer are a temperature of 400°C, a H_2 carrier gas flow of 20 slm and a pressure of 100 torr. A 1150°C bake was performed for two minutes prior to any deposition on the Si (001) substrate. The Ge deposition was achieved with a GeH_4 flow of 150 sccm for varied growth times. The HT layer was grown using the same growth parameters at an elevated temperature of 670°C. A set of wafers were prepared as shown in Table 5.1. Wafers 4786-4790 consisted of different thickness LT layers only and wafers 4791-4796 were grown with a standard LT layer (nominally 100 nm) with varying thickness HT layers.

5.2.1 Layer Thickness

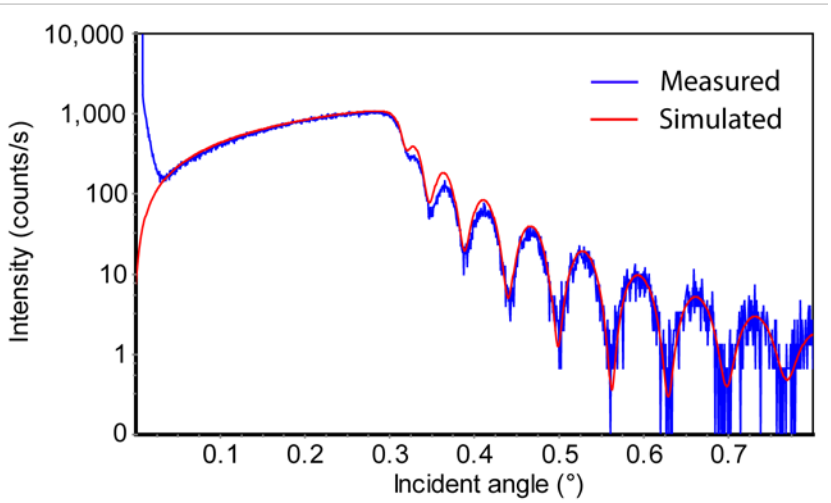

Figure 5.1: An XRR scan of wafer 4787. The blue line is the measurements taken and the red line is the simulated results. The thickness of the layer was measured to be 56.4 nm.

The LT Ge layer thickness was determined using x-ray reflectivity (XRR) measurements (Section 3.4.3) and simulations performed with the Philips PANalytical X'Pert Reflectivity program. An example of an XRR measurement is seen in Figure 5.1 for wafer 4787 which shows a thickness of 56.4 nm. Thicknesses were also confirmed through TEM measurements, an example of which is shown in Figure 5.2.

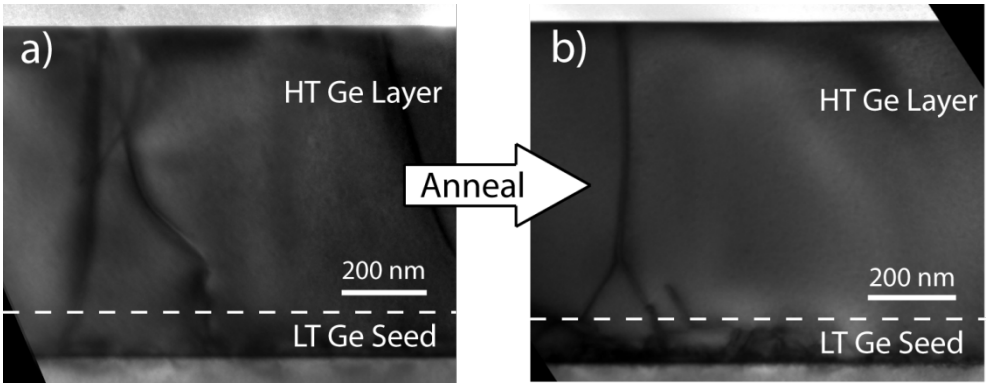

Figure 5.2: Cross sectional TEM micrographs of a) sample 4794 which has a 96.8 nm LT Ge seed layer and approx 665 nm HT Ge on top. b) shows sample 4797 which has the same structure, but has been annealed in-situ at 830°C for 10 mins. The lines shown are guides for the eye.

The HT Ge layers were measured using TEM. As there is little contrast in the TEM images between LT and HT regions the thickness of the HT layers was obtained by subtracting the measured LT thickness for sample 4788 (96.8 nm), as shown in Figure 5.2. The deposited layer thicknesses are listed in Table 5.1.

Wafer Number	Growth Temperature (±5°) (°C)	Thickness Grown (±2 %) (nm)	
		LT Layer	HT Layer
4786	400°C (LT)	27.6	
4787	400°C (LT)	56	
4788	400°C (LT)	97	
4789	400°C (LT)	118	
4790	400°C (LT)	149	
4791	670°C (HT)	97	136
4792	670°C (HT)	97	273
4793	670°C (HT)	97	392
4794	670°C (HT)	97	670
4795	670°C (HT)	97	860
4796	670°C (HT)	97	1130
4797	670°C + Anneal	97	670
4798	670°C + Anneal	97	1130
4799	400°C + Anneal	97	

Table 5.1: The measured thickness for the various two temperature Ge layer wafers. The HT layer thickness are the overall observed thickness less the seed thickness of 96.8 nm for wafer 4788.

Only three LT wafer thicknesses were confirmed through TEM imaging as the results obtained were in agreement to within 0.1% with XRR results. Post growth *in-situ* anneals of 830°C for 10 min were performed on three additional wafers: wafer 4799 was a 96.7 nm LT Ge layer, and wafers, 4797 and 4798 were composed of a 96.8 nm LT Ge seed capped with a HT Ge layer.

5.2.2 Relaxation

Due to the thin layers grown for the LT Ge layer investigation XRD RSMs on all samples was deemed impractical due to the low signal to noise ratio associated with the thin layer and the resulting time required to perform full scans. Instead, relaxation of the layer was calculated through the measurement of (004) rocking curves and calculation of the out-of-plane lattice parameter. RSMs were obtained from wafers 4786, 4790, 4796 and 4798 to confirm the relaxation calculated from the rocking curves for these samples and were within ±0.5 %. The error in relaxation which is reported in this section is a maximum of 3 %.

The relaxation of a Ge layer on a Si(001) substrate has been shown to be unstable to relaxation from homogeneous half loop nucleation of dislocations when the thickness of the layer is above 10 nm [14]. Figure 5.3 shows the rocking curve measurement from the LT wafers, 4786 to 4790. The LT Ge layer peak is seen to shift toward the Si (001) substrate peak indicating a decrease in the out-of-plane lattice parameter (Figure 3.10) with increasing LT Ge thickness. As the layer is pure Ge it is assumed the layer is tetragonally distorted therefore the in-plane lattice constant can be calculated through Equation 2.9 and then relaxation can be calculated from Equation 2.11. No tilt of the layers is observed in any of the RSMs obtained. The relaxation in

Figure 5.3 is seen to increase as the thickness of the layer is increased. There is also an increase of x-ray counts as the layer thickness is increased, which increases the signal to noise ratio and improves the accuracy of results.

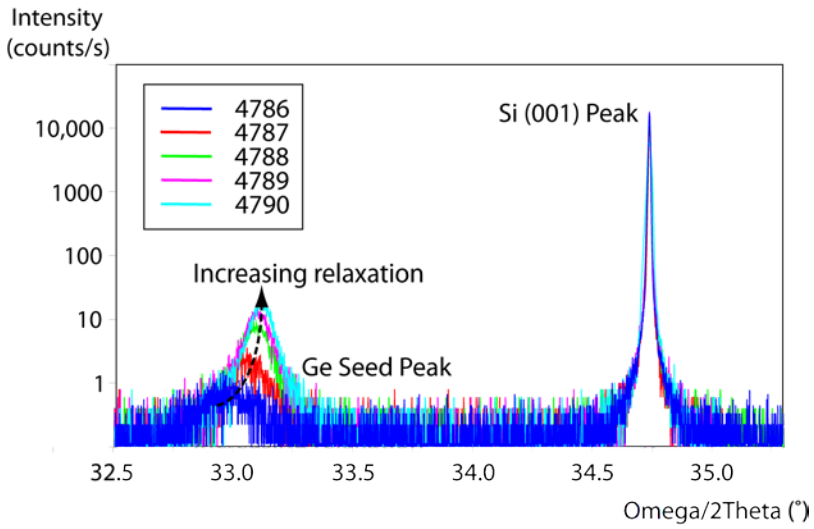

Figure 5.3: The x-ray rocking curves for the thin Ge seed layers. Note the shift along the Omega/2Theta axis which corresponds to a decrease in the out-of plane lattice constant indicating an increase in relaxation of the layer. The lines shown are guides for the eye.

The relaxation calculated from the rocking curve analysis is shown in Figure 5.4 where the relaxation is relative to the Si (001) substrate. Relaxation is observed to increase in an approximately logarithmic fashion from 83.3 % for the thinnest LT layer (sample 4786, thickness = 27.6 nm) to 95.8 % for the thickest layer (sample 4790, thickness =149.0 nm). The RSM calculated relaxation for these layers is 82.5 % and 96.3 % respectively, which is within error and of the same magnitude as the values obtained from rocking curve analysis. This logarithmic characteristic is expected as the drag force of a dislocation is related to the layer thickness through a logarithmic relationship (Equation 2.18). The relaxation calculated for the LT Ge seed layer which is grown prior to the HT layer is 93.4 % (wafer 4788, thickness 96.8 nm). When a seed layer is subjected to an *in-situ* anneal for 10 min at a

temperature of 830°C (wafer 4799) a relaxation of 112.6 % is measured. It is not known why this layer has this value of relaxation which indicates a significantly large degree of tensile strain. One speculation is that interdiffusion occurs between the layer and the Si (001) substrate such that the Ge layer becomes a SiGe layer which has a lower relaxed parameter. A larger over-relaxation will be calculated if a pure Ge is assumed and a larger relaxed lattice parameter is used.

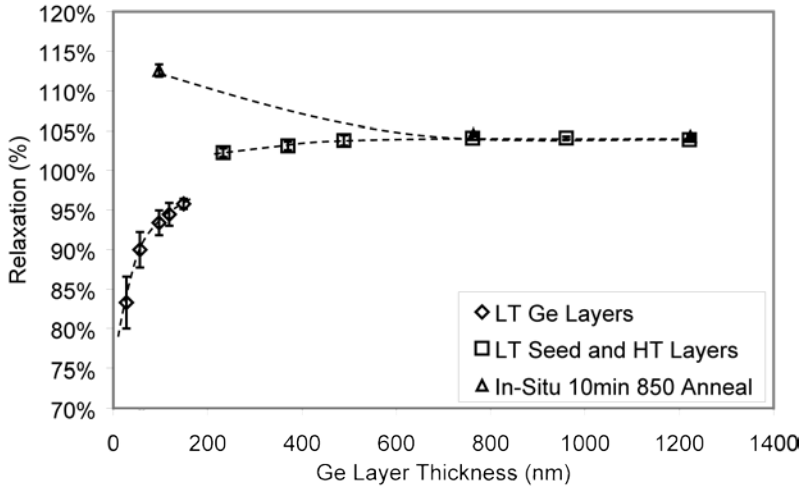

Figure 5.4: Relaxation of the two temperature Ge underlayer when compared to the Si (001) substrate, as calculated from rocking curve analysis. The lines shown are guides for the eye.

The relaxation of the HT layers is also shown in Figure 5.4 as a function of the *total* layer thickness (including the LT Ge seed layer). All HT layers are observed to be under tensile strain. Section 2.5.4 explains how the differences in thermal expansion coefficients can result in a relaxation of 104.2 % when a pure Ge layer is fully relaxed during growth and deposited at an average growth temperature of 535°C. When no thermal strain is induced during growth of the wafer, a relaxation level of 97.9 % is calculated for a total structure thickness 232.9 nm. The cooling of this layer to room temperature imparts a tensile strain within the layer which is measured to be 102.3 %. As layer thickness is increased the measured relaxation continues to

increase in a logarithmic trend until a value of 104.1% is reached for an overall structure thickness of 761.7 nm. HT wafer thicknesses which are greater than 761.7 nm do not receive a significant (>0.3 %) increase in relaxation.

An *in-situ* 10 min 830°C anneal of the HT layer increases the relaxation of sample 4797 with a total structure thickness of 763.5 nm from 104.1 % to 104.5 %. Under the same anneal a structure thickness of 1223.6 nm (sample 4798) increases relaxation from 103.9 % to 104.3 %. The anneal shows that further relaxation occurs, and under the high temperature the dislocation glide velocity would be greatly enhanced increasing the probability of dislocation annihilation.

5.2.3 Layer Dislocation Density

Section 4.7 speculates that the underlying TDD within the Ge underlayer is paramount to the final dislocation density within reverse graded buffers. The TDD within the HT layers was measured by etching of the samples in iodine solution for the increased etch time of 6 to 10 seconds due to the reduced etch rate of pure Ge in the iodine solution (Section 3.5) and to ensure the dislocations within the Ge layer are revealed. The sample was then viewed through a DIC microscope and the TDD was quantified from a selection of 30 images. Examples of these images are shown in Figure 5.5.

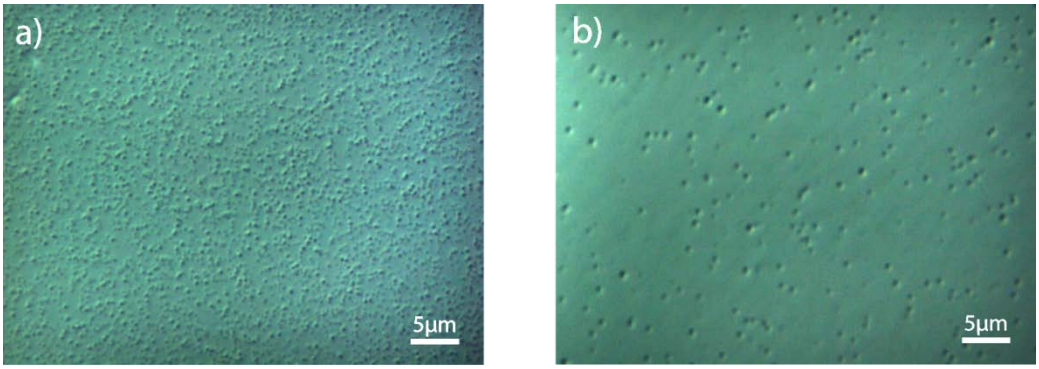

Figure 5.5: Examples of the etched surfaces of HT Ge layers a) shows sample 4798 which has a 98.6 nm LT layer with a 1124.8 nm HT layer on top. b) shows sample 4796 which has the same structure but has been subjected to an *in-situ* anneal.

The TDD within the LT seed is seen within cross-sectional TEM micrographs to be $> 10^8$ cm^{-2} (Figure 5.6). The mechanism to reduce TDD within the two temperature layer is through high temperature growth and its subsequent annealing. The investigation of TDD will be limited to the HT layers, with and without *in-situ* annealing.

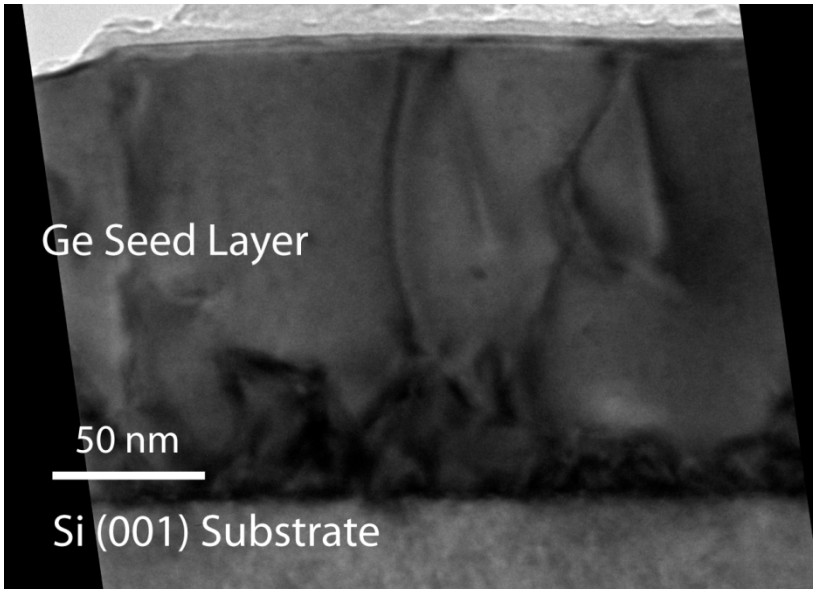

Figure 5.6: A cross sectional micrograph of sample 4790, a 149 nm thick LT Ge seed layer. It is observed that a high density of threading dislocations is present.

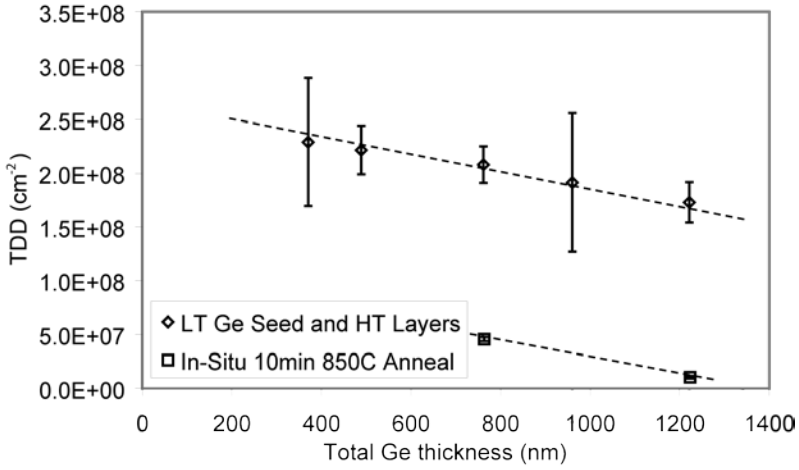

Figure 5.7: The dislocation density in the high temperature Ge layer, with a 96.8 nm seed layer. The shown Ge layer thickness is the total layer thickness of the layer, including the Ge seed. The lines shown are guides for the eye.

Figure 5.7 shows the variation of TDD within the Ge structure and the effect of an *in-situ* anneal. Note that the TDD axis is linear and that the relationship between the TDD and structure thickness is linear. Theoretical predications suggest that dislocation annihilation in constant composition layers has a logarithmic trend with an increase of thickness [128]. It is speculated that due to the high density of dislocations the relationship observed is only valid for the thicknesses investigated. Extrapolation from Figure 5.7 suggests the annihilation rate for the TDD within HT Ge layers is 6.6×10^{4} cm^{-2} per 1 nm of HT Ge deposited, with the assumption that no further dislocation nucleation occurs.

The thickest HT layer has a thickness of 1221.6 nm which has been measured to have a threading dislocation density of 1.7×10^{8} cm^{-2}. The annealing step is shown to reduce the TDD within this HT layer to 1.0×10^{7} cm^{-2} (wafer 4798). Annealing of the 761.7 nm thick layer (wafer 4797) also reduces the TDD from 2.0×10^{8} cm^{-2} to 4.6×10^{7} cm^{-2} which is not as effective at dislocation annihilation as the thicker HT layer. This shows that both annealing and thick HT layers are required to optimise

the annihilation rate. For an annealed wafer of total thickness 1000 nm a TDD of 2.4 x 10^7 cm^{-2} is interpolated, which is approximately the TDD recorded for the Ge underlayer within Section 4.2.1. The lowest TDD achieved was 1.0 x 10^7 cm^{-2} for a two temperature layer thickness of 1223.6 nm which was then subjected to an *in-situ* anneal of 830°C for 10 mins.

5.2.4 Roughness

Dislocation dynamics studies within the reverse graded layer assume that the heterogeneous dislocation nucleation rate is very low when the layer is grown in a 2D Frank-van der Merwe growth mode. If roughness of the LT and HT layers is significantly increased it is thought that a lower grading rate and hence a thicker graded layer will be required to suppress dislocation nucleation within the graded layer.

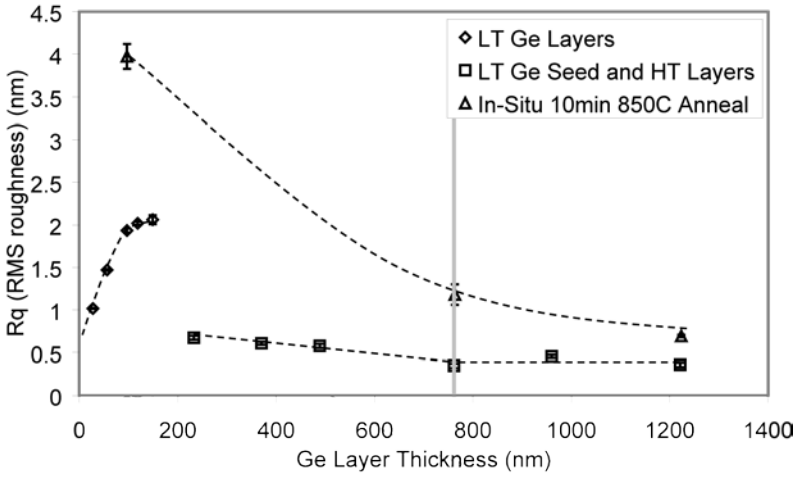

Figure 5.8: The RMS roughness of the Ge layer. The Ge layer thicknesses shown are the overall Ge layer thicknesses. The lines shown are guides for the eye.

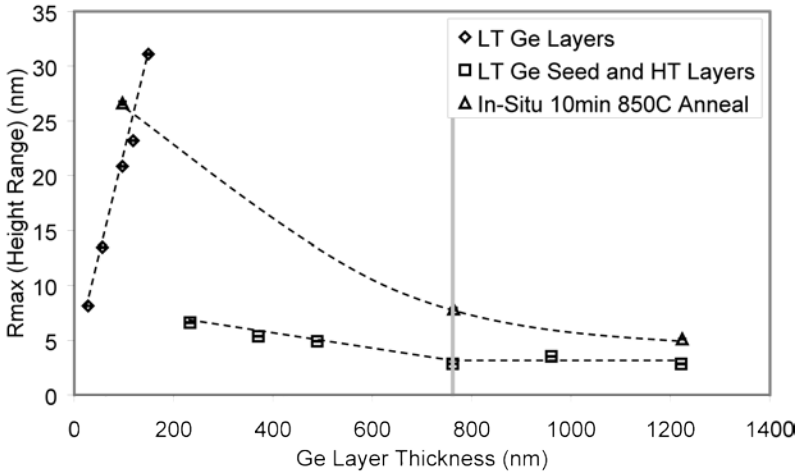

Figure 5.9: The height range of the LT Ge layers, HT Ge layers and the annealed wafers. The Ge layer thicknesses shown are the overall Ge layer thicknesses. The lines shown are guides for the eye.

Figure 5.8 shows the measured RMS roughness for the LT Ge layers, the HT layers and the annealed wafers, whilst Figure 5.9 shows the corresponding height ranges. When the 400°C Ge layers are grown a linear increase in roughness and height range is observed until a roughness of 1.9 nm and height range of 20.1 nm recorded for the LT Ge seed layer of 96.8 nm (sample 4788). This roughening effect is concluded to be a direct effect from the relaxation process (Section 5.2.2). A pictorial representation of the surface is shown in Figure 5.10, this increase in roughness is shown from Figure 5.10a) to Figure 5.10b) to Figure 5.10c). The surface features which can be seen are described as sharp peaks. The height range increase indicates that the height and depth of these surface features increases. Whilst the increase in RMS roughness indicates that surface features become increasingly dense.

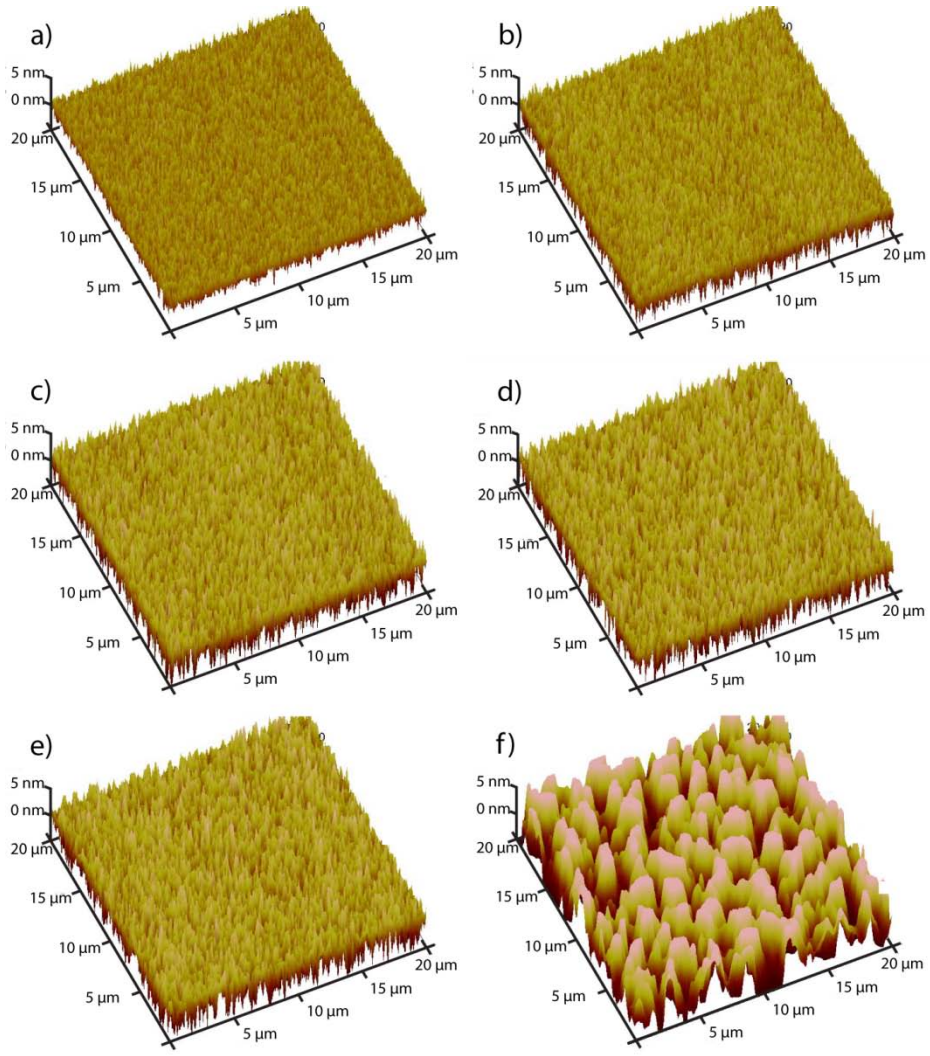

Figure 5.10: A pictorial representation of the Ge seed layer surface. The shown wafers are a)4796, b)4787, c)4788, d)4789, e)4790 and wafer f)4799.

Continued LT growth to a thickness of 149.0 nm only increases the RMS roughness to 2.1 nm, which again corresponds to the relaxation trend (Section 5.2.2). However, the height range continues to increase at the same rate until a height range of 31.1 nm is measured for the thickest LT layer. This is evidence to show that beyond a LT layer thickness of 96.8 nm a saturation of surface feature density occurs. However, their individual height and depth still continues to increase as layer thickness is increased.

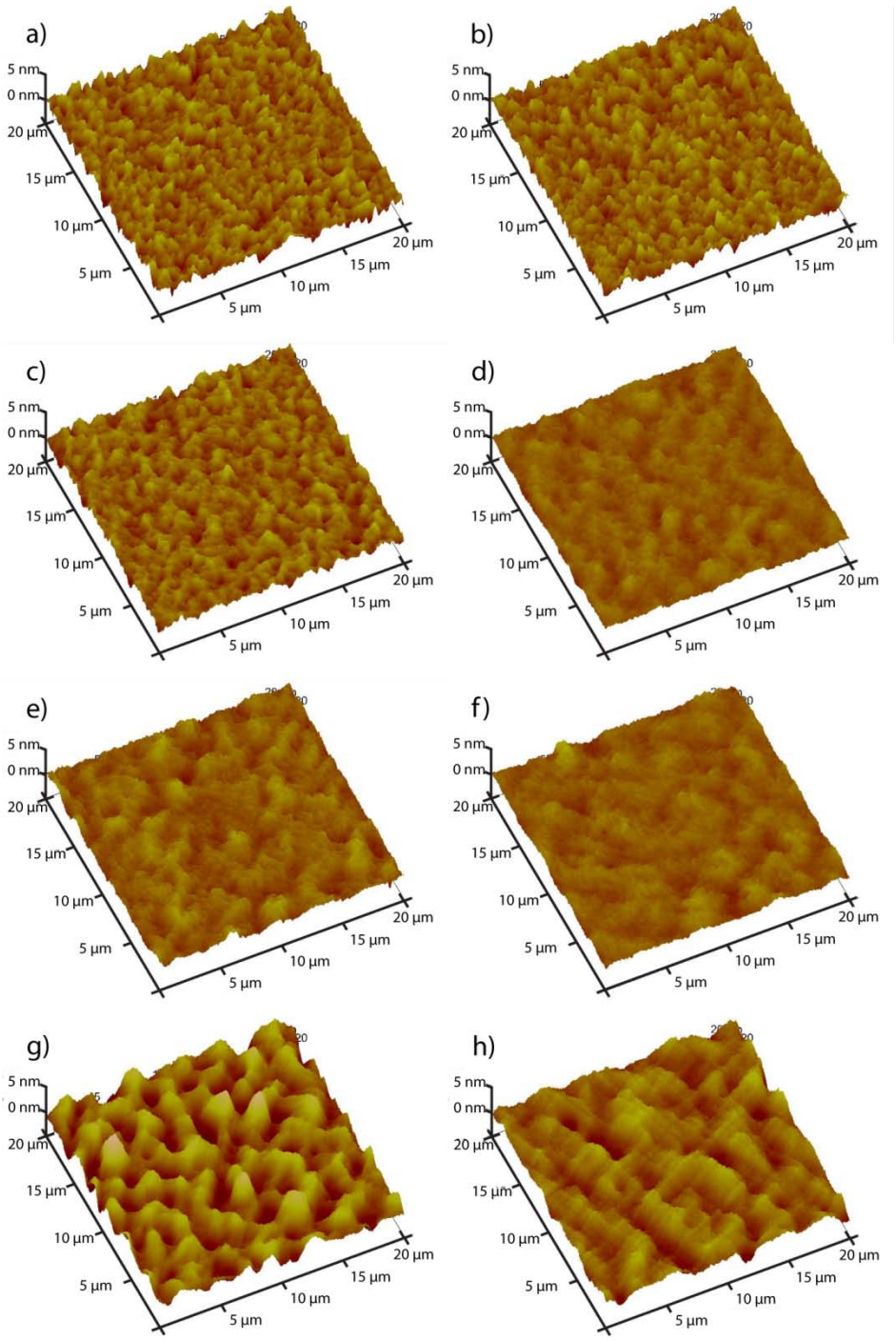

Figure 5.11: A pictorial representation of the high temperature Ge layer on the 96.8 nm Ge seed. The wafers shown are a)4791, b)4792, c)4793, d)4794, e)4795, f)4796, g)4797 and h)4798.

When a 96.7 nm LT layer is annealed *in-situ* the roughness rapidly increases from a value of 1.9 nm to a value of 4.0 nm, and the height range increases from 20.9 nm to 26.6 nm. The surface of this wafer is shown in Figure 5.10f). It is speculated that the

annealing induces surface melting. This coupled with a high annihilation rate of dislocations, creates multiple low energy sites for incorporation of mobile adatoms, dramatically increasing the density of features on the surface and therefore the RMS roughness.

HT Ge growth on the 96.7 nm Ge seed produces a smoothing effect and lowers the RMS roughness to sub nanometre values whilst lowering the height range values to below 10 nm (Figure 5.8). After a thickness of 136.1 nm is deposited for a total layer thickness of 232.9 nm the roughness is reduced from 1.9 nm to 0.7 nm and the height range is reduced from 20.9 nm to 6.6 nm. The RMS roughness and height range of the HT layer is then reduced as thickness of the Ge layer is increased until a thickness of 761.7 nm. Extrapolation shows a smoothing rate for RMS roughness of 0.3 nm per 500 nm of HT layer growth, and a rate of 3.5 nm per 500nm for the height range. The HT layer wafer of thickness 761.7 nm reduces the roughness to 0.4 nm with a corresponding height range of 2.8 nm. The smoothing effect is sequentially shown in Figure 5.11, from a layer thickness of 232.9 nm in Figure 5.11a) to a thickness of 761.7 nm in Figure 5.11d). No further smoothing effect is observed in HT layers with thicknesses above 761.7 nm (wafer 4794).

Annealing roughens the HT layers. A layer thickness of 763.5 nm is seen to increase from a roughness (height range) of 0.4 nm (2.8 nm) to 1.2 nm (7.8 nm). The thickest wafer of layer thickness 1224.0 nm is seen to increase from a roughness (height range) of 0.4 nm (2.8 nm) to 0.7 nm (5.1 nm). The cause of the increased roughening in the thinner layers is thought to be the higher dislocation density in the layer (Section 2.6.1). The increased strain field rearranges more of the mobile surface

adatoms to increase roughness. The RMS roughness of the thickest annealed HT layer is equivalent to that of the Ge layer used in Chapter 4.

HT growth lowers the roughness and height range significantly after the initial LT Ge seed deposition and no enhancement in smoothing is seen after a thickness of 761.7 nm. However, *in-situ* annealing leads to roughening of the layer. When the results for surface roughness (Figure 5.8) are compared with TDD values measured (Figure 5.7) it is shown that thinner layers with higher dislocation densities incur more roughness than a thicker layer with a lower TDD.

5.3 Optimisation of the SiGe Constant Composition Layer

The SiGe cap used in Chapter 4 was deposited on the investigated RLG structures to ensure full relaxation and to spatially separate the misfit dislocation network from the surface of the wafer. However, it was kept thick (~1 µm) for characterisation purposes; the thick layer allows large etch pits to be formed when selective defect etching is performed and allows higher signal to noise ratio during XRD. However, the thick layer allows tensile strain energy to be stored which lowers the energy barrier to crack formation. In this section the effect of reducing the thickness of the constant composition SiGe cap layer is investigated.

In Section 4.2 the growth-optimised buffer (wafer 4046) which consisted of a graded region thickness of 931 nm corresponding to a grading rate of 23.12 % μm^{-1} was investigated. The growth parameters used for this wafer are reported in Section 4.2.5 and were reproduced to fabricate a constant RLG layer platform for the SiGe cap reduction studies. A chamber etch was performed prior to deposition of the SiGe cap,

and the growth parameters used for the SiGe cap were a growth temperature of 850°C, hydrogen flow of 20 slm and growth pressure of 20 torr. A precursor flow of 500 sccm of GeH_4 and 35 sccm of SiH_2Cl_2 was used for varied times.

5.3.1 Layer Thickness

Thicknesses were determined by TEM measurements, an example of which is shown by Figure 5.12. Figure 5.12a) shows wafer 4800 which was grown with the Ge underlayer and RLG layer, but no SiGe cap. The cap thickness of subsequent wafers was calculated by subtracting the measured thickness of sample 4800 from the measured thickness of the overall buffer. Layer thicknesses are shown in Table 5.2.

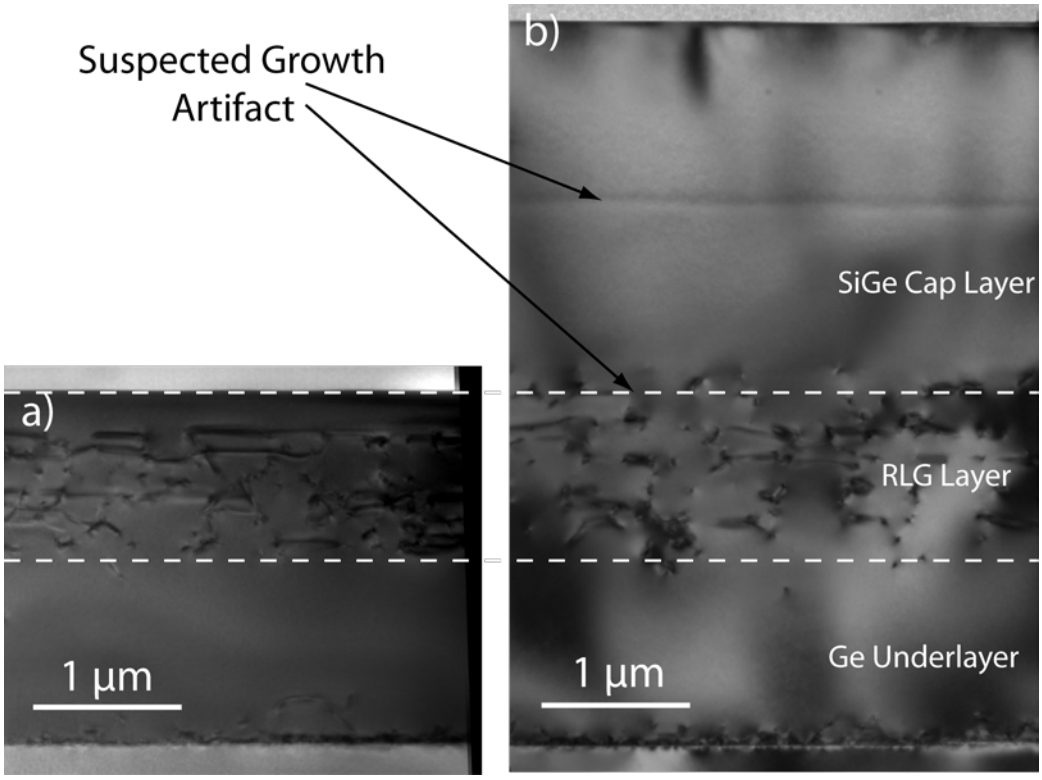

Figure 5.12: Cross sectional TEM images a) sample 4800 the RLG buffer with no SiGe cap and b) sample 4807 an RLG buffer with a 2.5 µm cap. The lines shown are guides for the eye.

Two sharp growth changes in contrast can be seen in Figure 5.12b) (sample 4807) which are labelled as growth artifacts. These both occur at thicknesses where a chamber etch was performed, it is suspected that these artifacts are changes in composition resulting from the change of growth kinetics due to chamber etching. This effect is seen throughout all TEM micrographs in wafers with thick SiGe cap layers where etching is performed during growth of the SiGe cap. It is shown that the change in composition at the top of the RLG layer can barely be resolved due to features from the misfit dislocation network.

Wafer Number	Total Buffer Thickness (±5 nm) (nm)	Constant Composition SiGe Cap Layer Thickness (±2 %) (nm)	Composition of the End of RLG Layer (±0.005) (-)	Composition of the Separated SiGe Cap (±0.005) (-)
4800	2548	0	0.807	-
4801	2660	112	0.812	0.800
4802	2786	238	0.808	0.800
4803	2900	352	0.808	0.800
4804	3180	631	-	0.801
4805	3906	1358	-	0.804
4806	4499	1951	-	0.801
4807	5079	2531	-	0.802

Table 5.2: The thickness and composition of the SiGe RLG constant composition wafer set.

5.3.2 Relaxation and Composition

Relaxation and composition of the buffer were both measured using XRD. Figure 5.13 shows the RSMs for a RLG buffer with SiGe cap thickness of 112 nm. The RSMs show a second peak close to the end of the RLG which is attributed to the SiGe cap. This slight drop in Ge composition between the SiGe cap and the final layers of the grading regions are attributed to a change in growth kinetics triggered by an HCl chamber etch (see Section 4.3.1) which is supported by TEM observations (Section 5.3.1). The compositions at the end of the RLG layer and the SiGe cap are

listed in Table 5.2. The peak intensity of the SiGe cap is observed to increase as the cap layer thickness increases. This effect occurs until the ratio between the intensities of the SiGe cap peak and RLG peak is large and both peaks are no longer individually distinguishable.

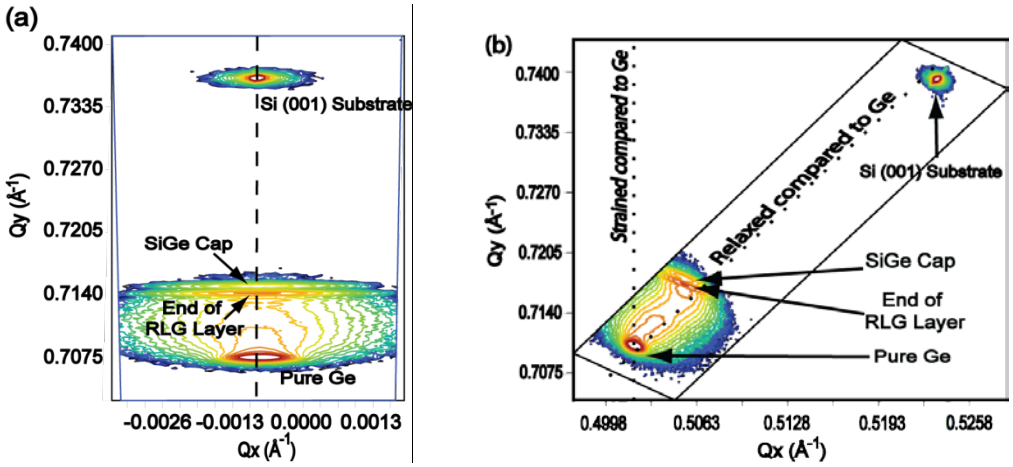

Figure 5.13: XRD RSMs of wafer 4801 where a) is the (004) reflection and b) is the (224) reflection. The separated SiGe cap and the END of the RLG region are labelled.

Figure 5.13a) shows that the tilt of the layers when compared to the Si (001) substrate is minimal. The Ge underlayer is 104.2 % relaxed when compared to the Si (001) substrate. Figure 5.13b) shows that the SiGe cap peak has a slightly higher magnitude of tensile strain than that of the end of the grading region. The strain between these layers of ~0.0001 is not enough to affect dislocation dynamics (Figure 2.14).

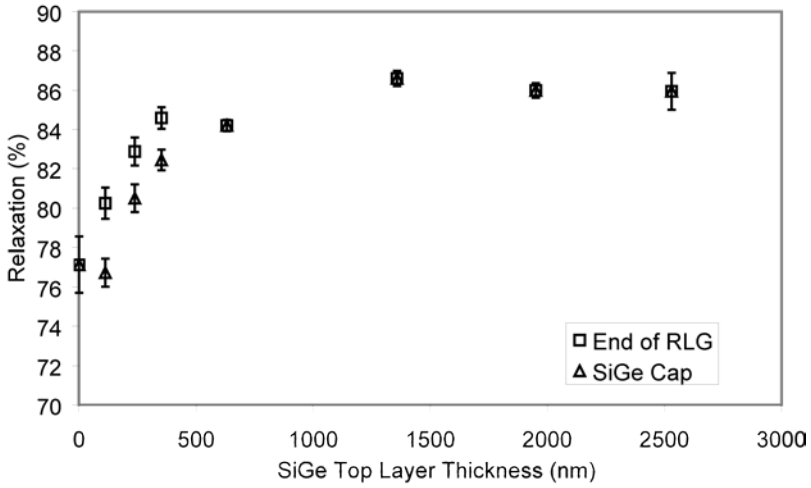

Figure 5.14: The crack corrected relaxation of the end of the RLG layer and the SiGe cap when relative to the Ge underlayer.

Figure 5.14 shows the crack corrected relaxation (see Section 5.3.3) at the end of the RLG layer and the SiGe cap when compared to the Ge underlayer. The relaxation of the RLG layer is measured in wafer 4800 which does not have cap and a value of 77.1 % was found for the end of graded region. When the SiGe cap layer is grown and the thickness is increased the relaxation increases in a logarithmic trend, similar to the relaxation of the LT Ge layer (see Section 5.2.2). The RSM constant composition cap peak and the peak associated with the end of the graded region cannot be resolved at a cap thickness of 631 nm. The maximum relaxation within the SiGe cap wafers is 86.6 % at a cap thickness of 1388 nm, and relaxation does not increase significantly once this thickness is exceeded.

5.3.3 Defect Densities

As relaxation is only partially increased by the SiGe cap a drastic reduction of TDD is not expected, but by reducing the cap thickness suppression of cracking is expected. To create etch pits for EPD measurement the buffers were submerged in an

iodine etchant for 1 to 5 seconds, depending on the cap thickness. The reason for the varied etch time is so that dislocations from the RLG region are not selectively revealed to avoid distortion of the results. Due to the low etch times small etch pits are created therefore higher magnifications are required which leads to smaller sampling statistics and larger errors. A selection of 30 images was taken to find an average EPD. The amount of etch pits in each image was approximately 25 per image. The error in TDD which is reported in this section is ±20 % of the values stated.

The TDD within the top SiGe cap layer as thickness is varied is shown in Figure 5.15. It is assumed that the TDD at the end of the RLG layer is equivalent to that in the thinnest SiGe cap layer (wafer 4801), 1.9×10^{6} cm^{-2}. The lowest dislocation density of 1.4×10^{6} cm^{-2} was measured within a SiGe cap thickness of 1358 nm. This corresponds to the highest relaxation in the layers, see Section 5.3.2. However, when the thickness is increased beyond this point the TDD increases to 3.1×10^{6} cm^{-2} when the cap thickness is 2531 nm. It is postulated that the People and Bean critical thickness (2.4.6) is exceed therefore dislocations are nucleated.

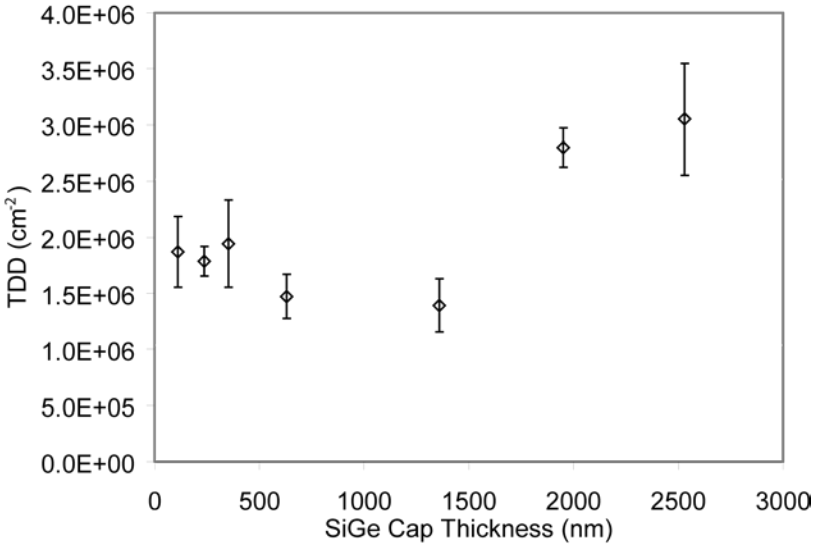

Figure 5.15: The variation of the TDD when SiGe cap thickness is reduced.

The crack densities of the wafers were measured as previously outlined in Section 4.3.5. Figure 5.16 shows the measured crack densities as a function of buffer thickness. Crack formation starts during the growth of the buffer when a buffer thickness of 3.9 µm is reached and minor crack densities of 2.6 cm^{-1} are formed. A maximum induced crack density of 41.7 cm^{-1} is found for the thickest buffer (with total thickness 5.1 µm) which corresponds to a relaxation of the top layer of 3.1 % when compared to the Ge underlayer. This is proof that a reduction of the SiGe cap thickness can reduce cracking tendencies, as suggested in Section 2.5.5. The induced crack densities show that only a total thickness of 2.8 µm or less is allowable before induced cracking of the top layer occurs.

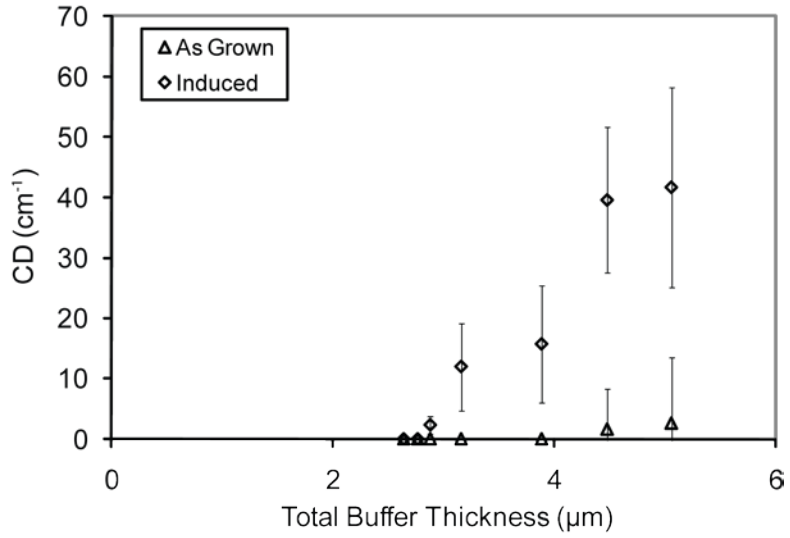

Figure 5.16: The grown in and induced crack density of the layers as the SiGe cap layer is increased.

5.3.4 Roughness

The RMS roughness of the SiGe cap on the RLG buffers was measured by AFM scans. Figure 5.17 and Figure 5.18 show the RMS roughness and height range of the SiGe cap as its thickness is increased.

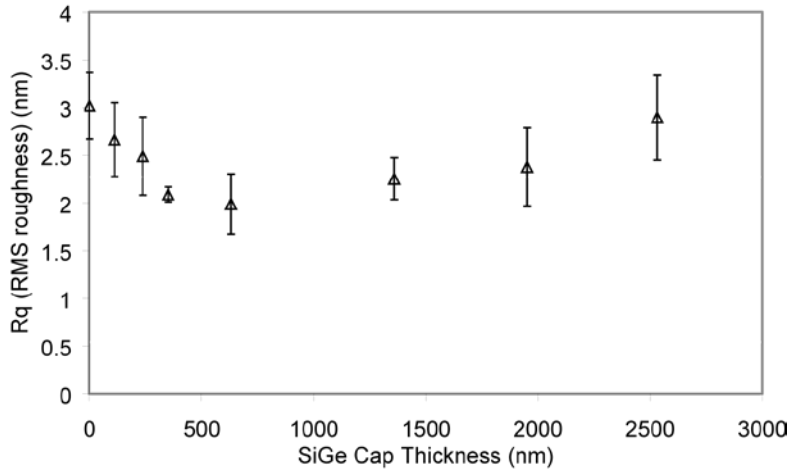

Figure 5.17: The measured RMS roughness of the SiGe cap as layer thickness is increased.

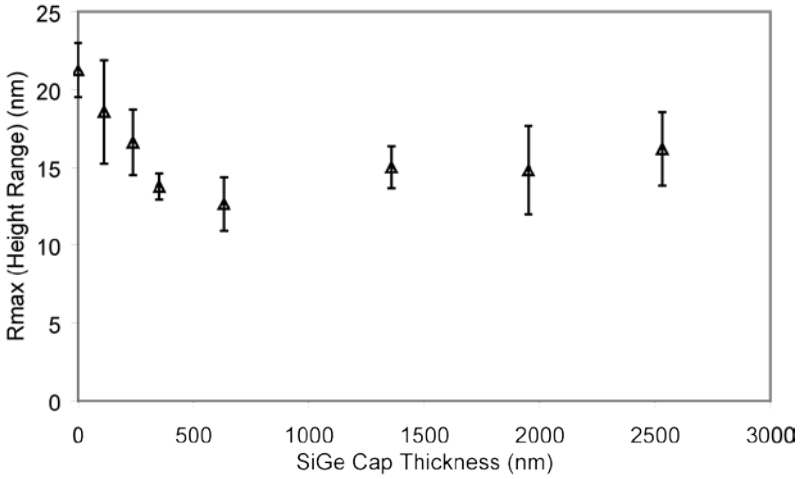

Figure 5.18: The associated height range as SiGe cap thickness is increased.

The roughness of the RLG layer (with no SiGe cap) is measured on sample 4800 to be 3.0 nm with a height range of 21.3 nm. As the SiGe cap thickness is increased to 352 nm the roughness decreases linearly at a rate of 2.4 nm per 1 µm SiGe cap growth. Alongside this the height range also decreases linearly at a rate of 20.6 nm μm^{-1}. The strain field from the underlying misfit dislocations are thought to arrange mobile adatoms into the lower energy sites in-between the crosshatch peaks, producing a smoothing effect. At the end of this smoothing effect when the SiGe layer thickness is 352 nm thick, the layer is shown to have an RMS roughness of 2.1 nm with a height range of 13.7 nm. Above a thickness of 631.4 nm the underlying strain field does not interact with the adatom transport. This is shown as the thickness of the cap is increased and roughness is *induced* at a lower rate of 0.5 nm μm^{-1}. The height range also increases at a lower gradient of 1.7 nm μm^{-1}. The RMS roughness measured for the thickest SiGe cap layer is 2.9 nm with a height range of 16.2 nm.

5.4 Optimising the Complete Reverse Graded Buffer

The reverse graded buffers which have been grown on the Si(001) are of interest due to their final layer properties of low TDD, extremely low RMS and high relaxation. However, the problem of cracking of the layer plays a substantial role in their development. Reducing the overall buffer thickness has been shown to suppress the as-grown *and* the induced cracking densities. The additional advantages of this action are the lower growth time per buffer and the reduced resources used, thereby reducing the cost per wafer.

5.4.1 Thickness Optimised Designs

Two wafers were designed to reduce the overall thickness of the reverse graded buffer. One design (sample 4946) was fabricated to examine the effect of reducing the HT Ge layer thickness in an RLG buffer. The Ge underlayer is designed to be a copy of wafer 4797 (see Section 5.2), which had nominal layer thicknesses for the LT Ge seed and HT Ge layer of 100 nm and 700 nm respectively. The RLG and SiGe cap layers which are deposited on this underlayer use the same growth parameters as wafer 4804 (see Section 5.3) and is intended to have a similar grading rate and SiGe cap thickness, the major difference being the thickness of the Ge underlayer. The design of wafers 4946 and 4804 is shown in Figure 5.19. The error in thicknesses which are reported in this section is ±2 % of the value given, compositions are reported to within ±0.005 and grading rates are within ±1 % of the value stated.

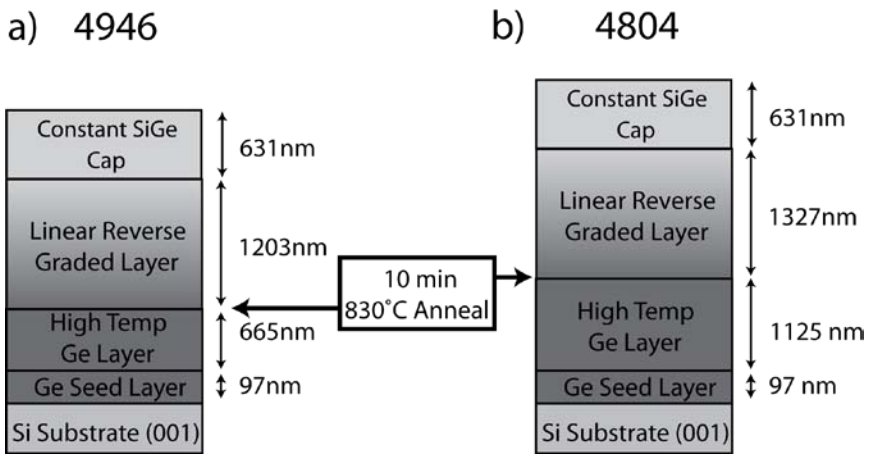

Figure 5.19: Schematic structure diagrams of a) The thicker design optimised structure, sample 4946, and b) reduced SiGe cap thickness sample 4804 which is reported in Section 5.3.

The second design (sample 4896) is intended to be the thinnest reverse graded buffer that can be fabricated by sacrificing buffer quality to reasonable values for thinner layers. It has been shown in Section 5.2 that the thickness of the two temperature Ge underlayer can be reduced and the TDD will be the same magnitude (~10^7 cm^{-2}) if high temperature annealing is performed. However, the roughness of the Ge underlayer has been shown to be mostly dependent on the thickness of the high temperature layer and the post-growth anneal performed. The relaxation of the base underlayer has also been shown to be generally high and is thought to depend on the thickness of the HT layer.

Using these observations a new design for the two temperature underlayer for sample 4896 was fabricated. A 28 nm LT seed layer was deposited, followed by a thin 136 nm HT layer and then a 10 min 830°C high temperature anneal. The lower roughness from the thinner LT Ge layer is intended to counteract any roughness not smoothed by the thinner HT Ge layer and roughness incurred from the high

temperature anneal. The annihilation of dislocations within the HT layer from annealing is intended to show TDD densities to the order of 10^7 cm^{-2}.

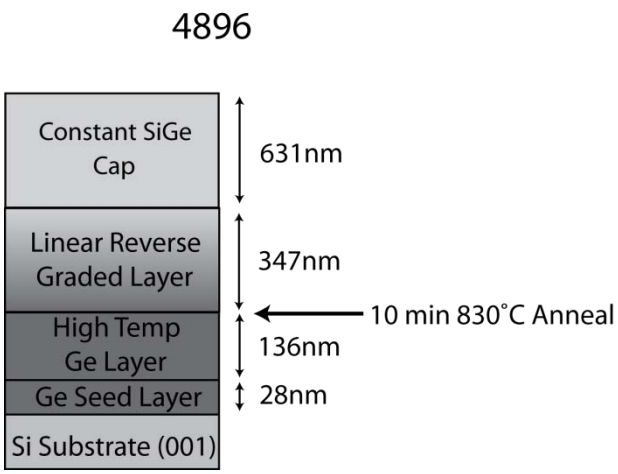

Figure 5.20: The schematic of the thinner design optimised structure, sample 4896

In Section 4.7 it was reported that the best grading rates for RTG and RLG buffers are 12.6 % μm^{-1} and 11.4 % μm^{-1} corresponding to layer thicknesses of approximately 1.8 µm. The optimised SiGe cap thickness is reported to be between 352 nm and 631 nm (Section 5.3). Therefore if a slightly thinner graded region is utilised for sample 4896 the smoothing effect and further dislocation annihilation of the SiGe cap can be exploited. It was observed in Section 4.3 that the Stranski-Krastanov growth mode and the dislocation nucleation regimes are avoided when a grading rate below 60 % μm^{-1} is used and a grading rate of 57 % μm^{-1} is intended. The design of the thinner optimised buffer (sample 4896) is shown in Figure 5.20. The growth parameters used to fabricate these buffers are the same as those in earlier sections which are listed in Sections 4.2.5, 5.2 and 5.3, only the deposition times were varied.

5.4.2 Characterisation of Thicker Optimised Buffer

TEM and XRD measurements were performed on wafer 4946 to determine thickness, composition and relaxation, and AFM measurements for RMS roughness and height range. A TEM micrograph of the sample is shown in Figure 5.21.

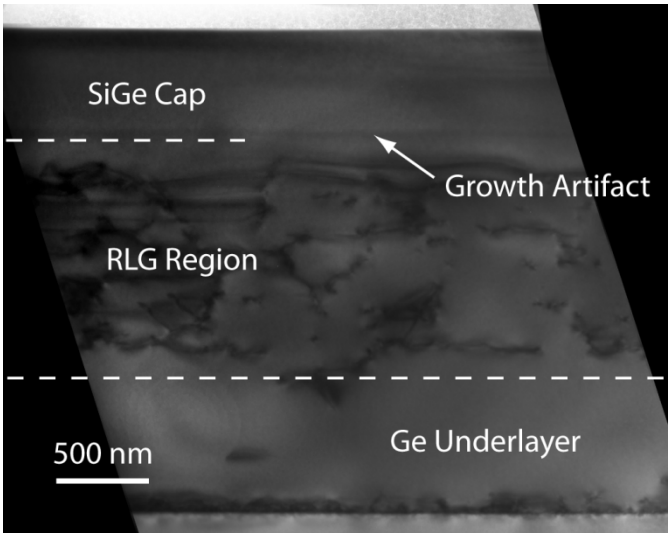

Figure 5.21: A TEM micrograph of the thicker design optimised buffer, wafer 4946. The lines shown are guides for the eye.

The measured properties of wafer 4946 are shown in Table 5.3, together with the properties of wafer 4797 which is an equivalent Ge underlayer as that used in wafer 4946 (see Section 5.2).

Wafer	Layer Thickness (nm)			SiGe Cap Composition (-)	Grading Rate (% μm^{-1})	SiGe Cap Relaxation (%)	TDD (cm^{-2})	RMS Roughness (nm)	Height Range (nm)
	Ge Under-layer	RLG Region	SiGe cap						
Error	±2 %	±2 %	±2 %	±0.005	±1 %	±0.5 %	±10 %	±0.2 nm	±2 nm
4946 (SiGe Cap)	762	1203	631	0.796	15.4	85.0	4.1 x 10^{6}	2.1	16.0
4797 (Ge)	762	-	-	0.997	-	104.5	4.6 x 10^{7}	1.2	7.8
4804 (SiGe Cap)	1222	1327	631	0.801	16.6	84.2	1.5 x 10^{6}	2.0	12.7
4798 (Ge)	1222	-	-	1.000	-	104.3	1.0 x 10^{7}	0.7	5.1

Table 5.3: A comparison of the characterisations performed for the thicker design optimised buffer, wafer 4946. The equivalent layer for the Ge underlayer for this optimised structure is wafer 4797. Also shown is a RLG buffer, wafer 4804, with an equivalent grading rate and cap thickness with a thicker Ge underlayer, wafer 4798.

The properties of wafer 4804 (Section 5.3) are also shown in Table 5.3. The Ge underlayer in wafer 4804 is thicker than that of the wafer 4946. The properties of the equivalent Ge underlayer within wafer 4804 are shown in Table 5.3, and are labelled as wafer 4798 (Section 5.2).

Reducing the Ge underlayer thickness and therefore quality has an effect on the RLG buffer quality, which can be studied. A graded region of approximately 16 % μm^{-1} and a SiGe cap thickness of approximately 600 nm is shown to reduce the TDD from the Ge underlayer to the SiGe cap by an order of magnitude, from 1.0 x 10^{7} cm^{-2} to 1.5 x 10^{6} cm^{-2}, in sample 4804. This effect is observed once again in 4946 when the Ge underlayer is reduced in thickness. The thinner Ge layer with a TDD of 4.6 x 10^{7} cm^{-2} is reduced by the RLG region and SiGe cap to 4.1 x 10^{6} cm^{-2}. The conclusion to be drawn from this observation is that the underlying TDD from the Ge underlayer is the limiting factor for the final TDD of the RLG structure as speculated in Section 4.7. No cracks are observed to form in wafer 4946 during growth or

sample preparation. Whilst in wafer 4804 cracks are induced during sample preparation, but not during growth.

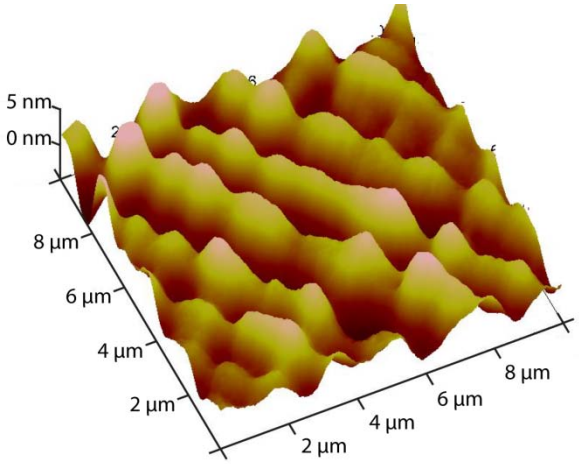

Figure 5.22: An AFM schematic representation of the surface of sample 4946

Another effect to be noted is the increased RMS roughness, from 0.7 nm to 1.2 nm, of the Ge underlayer as its thickness is reduced. However, after the deposition of the RLG layer and the SiGe cap, the thinner Ge underlayer buffer only shows a roughness 0.1 nm larger than that of the thicker Ge underlayer. This increase in roughness is deemed insignificant. This indicates that the final RMS roughness is due to the underlying dislocations within the graded region and that crosshatch is the main source of roughening, seen in Figure 5.22, not the Ge underlayer. The increase in height range from the Ge underlayer to the SiGe cap is 8.2 nm for sample 4946 (the thinner Ge underlayer) and this is only marginally larger than the increase of 7.8 nm for sample 4804. It can be concluded that the final height range of the buffer is directly dependent on the height range of the two temperature Ge layer. The relaxation of the thicker design optimised buffer does not show a significant enhancement of relaxation (> 1 %) compared to wafer 4804. Any enhancement in relaxation is speculated to directly increase the RMS roughness and height range.

A reduction in the Ge underlayer thickness of 460 nm is shown to increase the final RLG buffer TDD by a factor 4, although no significant increase in RMS roughness or relaxation is observed. It has been found that for this reduction in Ge thickness the height range of the buffer is directly dependent on the height range of the Ge underlayer. Cracks are not observed to form during growth of either wafer. However, the reduction of the Ge underlayer thickness shows a suppression of the cracking tendencies during sample preparation, and hence suggests that this method might suppress cracking during device fabrication.

5.4.3 Characterisation of Thinner Optimised Buffer

A TEM micrograph of the thinner optimised buffer design, wafer 4896, is shown in Figure 5.23. Table 5.4 shows all the measured properties of the buffer. The Ge underlayer in this structure contains a thinner LT layer when compared to the two temperature Ge structures previously studied in Section 5.2. Therefore only the observed properties of the Ge underlayer in sample 4896 can be used as a comparison. The TDD of the Ge underlayer can only be estimated from the cross sectional TEM images and no roughness values can be compared.

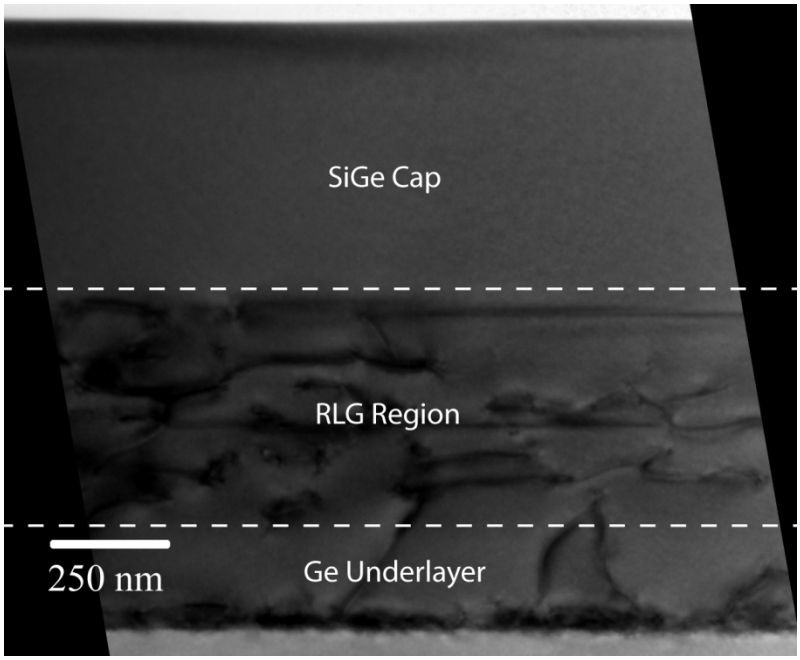

Figure 5.23; A TEM micrograph of the thinner design optimised buffer, wafer 4896. The lines shown are guides for the eye.

The composition of the Ge underlayer was measured by XRD to be 96.5 % which is significantly lower than any results previously measured. As the Ge underlayer is thin any diffusion of Si atoms from the RLG layer into the Ge underlayer would be more pronounced. However the diffusion profiles measured previously only showed composition drops up to 2 % Ge over a distance of approximately 300 nm (Section 4.3.1). It is speculated that the further decrease in composition could be due to the lower crystallinity (from the high dislocation content) of the thinner LT Ge seed and the resulting higher diffusion coefficient [134]. Therefore the SiGe cap will have a smaller misfit compared to this (Si)Ge underlayer and any relaxation values measured will be greater than those characterised previously. The relaxation is measured to be 84.2 % relaxed when compared to the tensile strained $Si_{0.035}Ge_{0.965}$ underlayer. Cross sectional TEM shows a TDD of approximately $> 5 \times 10^{8}$ cm^{-2} in the Ge underlayer. When the graded region and cap are deposited, the TDD value decreases to 6.2×10^{7} cm^{-2} which is measured by etch pit density measurements.

This result is similar to the effect found within the thicker optimised buffer (Section 5.4.2) as the TDD is reduced by roughly an order of magnitude after the growth of the RLG layer and the SiGe cap. The higher RMS roughness of 3.3 nm is thought to be due to the increased grading rate, whilst the increased height range of 24.7 nm is speculated to be due to a rougher relaxed underlayer.

Wafer 4896	Buffer Thickness (±5 nm) (nm)	SiGe Cap Composition (±0.005) (-)	Grading Rate (±1 %) (% um^{-1})	SiGe Cap Relaxation (±5 %) (%)	TDD (±10 %) (cm^{-2})	RMS Roughness (±0.2 nm) (nm)	Height Range (±2 nm) (nm)
SiGe Cap	1365	0.797	43.7	84.2	6.2×10^{7}	3.3	24.7
Ge Underlayer	317	0.965	-	106.3	~5×10^{8} (from XTEM)	-	-

Table 5.4: The characterised properties of the thinner design optimised RLG buffer, wafer 4896.

5.5 Discussion

In an effort to suppress the cracking tendencies of the reverse graded buffer the effect of reducing the Ge underlayer and SiGe cap thickness has been investigated and further enhancements have been demonstrated. Table 5.5 shows the most promising buffers which are reported in Chapters 4 and 5, these are listed in order of the thickness of the overall buffer. None of the listed buffers are observed to form stacking faults or cracks during growth, although cracks are observed to form during sample preparation in wafers 4804, 4345 and 4053. If induced cracking is not considered to be important, the wafer which is deemed to have the best trade-off between overall buffer quality and thickness is wafer 4804.

Wafer Number (Section Reported)	Overall Buffer Thickness (nm) (±5 nm)	Effective Grading Rate (%/um^{-1}) (±1 %)	TDD (cm^{-1}) (±10 %)	Cleaved Crack Density (cm^{-1}) (±25 %)	SiGe Cap Composition (±0.005)	Relaxation Compared to Ge Underlayer (%) (±0.5)	Rq (RMS Roughness) (nm) (±0.2 nm)	Rmax (Height Range) (nm) (±2 nm)
4896 (5.4.3)	1365	43.7	6.2 x 10^{7}	0.0	0.797	84.2	3.3	24.7
4051 (4.3)	2553	61.3	4.5 x 10^{6}	0.0	0.786	85.9	3.0	20.2
4946 (5.4.2)	2718	15.1	4.1 x 10^{6}	0.0	0.796	85.0	2.1	16.0
4804 (5.3)	3180	16.6	1.5 x 10^{6}	11.9	0.801	84.2	2.0	12.7
4345 (4.3)	3931	12.6	2.1 x 10^{6}	30.7	0.765	89.2	1.9	11.5
4053 (4.3)	4287	11.4	3.3 x 10^{6}	59.7	0.784	84.7	1.9	12.5

Table 5.5: A comparison of selected wafers that were examined in Chapters 4and 5 with promising qualities. All wafers shown do not form stacking faults or cracks during growth of the wafer.

A SiGe cap thickness of approximately 600 nm is shown to reduce roughness and dislocation density. A reduction in thickness of the Ge underlayer has been shown to increase the TDD density and hence lowers the quality of the final buffer. Table 5.5 shows the general trend of the reduction of RMS roughness and height range as the buffer thickness is increased, no matter what design is used. The RMS roughness and height range do not see any significant further improvements after a buffer thickness of 3180 nm (wafer 4804). Wafer 4804 inadvertently has these combined effects which give the buffer its excellent properties. However, the best grading rate which is found in Section 4.7 is not utilised in this buffer and so leaves room for further design improvement. Since, induced cracking could indicate that the reverse graded buffer is liable to cracking during fabrication of devices then wafer 4946 is the most suitable for device applications. This is the thicker optimised buffer, the TDD is slightly lower and the surface is smoother than wafer 4051, which is of similar thickness. It is argued that the reduction of the SiGe cap thickness of wafer 4051

could further improve the qualities of the buffer beyond that of wafer 4946, but no wafer to this effect has been fabricated and is left for further work.

5.6 Summary

Reverse graded buffers with overall thickness greater than 2.7 µm are observed to crack when prepared for experimental characterisation due to the cleaving process which induces additional local tensile strain (Section 4.3.5). Buffer thicknesses of approximately 4 µm are susceptible to crack formation during growth. It is suggested that a potential solution to suppress induced cracking is through reduction of the thickness of the overall buffer (Section 4.7). This solution is investigated in this section.

Reduction of the thickness of the Ge underlayer and the SiGe cap layer are studied as a solution to the cracking problem. It is shown in this chapter that both induced and as-grown cracking densities are reduced when the thickness of layers are reduced. Additional effects on the quality of the buffer are also found. The reverse graded layer is found to reduce the dislocation density from the Ge underlayer to the surface by an order of magnitude when the grading rate is kept within the glide regime (Table 5.3). Therefore the final TDD value within the SiGe cap is largely dependent on the TDD from the Ge underlayer. It has been discovered that reduction of the Ge underlayer thickness does indeed suppress induced cracking of the buffer, but reduces the quality of the final cap layer significantly. The reduction of the SiGe cap thickness shows all round improvement of the buffer when the thickness is reduced to approximately 600 nm. One wafer in particular has shown that these combined effects produce a high quality buffer, wafer 4804 (Figure 5.19). The properties of this

buffer are shown in Table 5.5. All comparisons with other buffer fabrication techniques and methods have been previously mentioned (Section 4.8).

6 Conclusion and Further Work

6.1 Conclusions

A unique method of reverse grading of silicon-germanium has been proposed, whereby a relaxed Ge layer with high dislocation content precedes the growth of a reverse graded region capped with a constant composition layer. The nominal composition of the $Si_{1-x}Ge_x$ buffer is intended to be $x = 0.8$. This structure was proposed as current high composition ($x > 0.7$) buffer fabrication techniques result in either very thick or low quality layers.

A reverse graded layer was grown on top of a relaxed pure Ge layer which was grown through the two temperature method (Section 2.6.8). The primary investigation in Chapter 4 was to solely change the grading rate within the buffer to determine its effect on the quality of the final structure. All other parameters were kept the same, including the growth rate.

A second investigation was performed in conjunction with the first which involved reverse *terrace* grading (Section 2.6.4). The linear graded regions within the buffer were graded in 5 % Ge steps and were repeated with increasing composition until a composition of $x = 0.8$ was achieved (Figure 4.4). Both the linear graded and constant composition layers within the terrace graded structure were designed to be the same thickness for each wafer and as with the primary investigation the grading rate was varied for this investigation.

It was observed in both the RLG and RTG structures that if the grading rate was too high (GR > 124 % μm^{-1}) the growth kinetics result in 3D Stranski-Krastanov growth (Figure 4.13). Within the grading regions this increases dislocation nucleation and surface roughness, which severely reduced the buffer quality (Figure 4.15). Additionally, extended stacking faults are seen to occur above this grading rate which hinders dislocation dynamics to relax the buffer (Figure 4.16).

When grading rates are too low (GR < 4 % μm^{-1}) cracking of the top epitaxial layer occurs during growth (Figure 4.20), which is detrimental to buffer fabrication. In addition to crack formation during growth, cracks were also induced during sample preparation from cleaving. Two "critical cracking thicknesses" have been observed in both RLG and RTG structures; 4 µm for cracks formed during growth and 2.7 µm for cracks induced during cleaving. It was calculated that the critical cracking thickness for a *fully strained* graded layer is predicted to be 2.7 µm (Section 4.6). Therefore it was concluded that the cleaving process fully strains the epitaxial layer, resulting in crack formation. To completely avoid cracking within the buffers, it was determined that the total thickness must be kept below 2.7 µm.

Grading rates of between 4 % $\mu m^{-1} \leq GR \leq 124$ % μm^{-1}, result in an improved high composition buffer, the measured parameters of which are listed in Table 6.1. All reverse graded buffers are of a high relaxation (> 85 %) when compared to the Ge underlayer. Generally, annealing does not significantly improve the qualities of the buffer (Sections 4.3.2 and 4.3.3). The conclusion drawn from the observed results is that due to relaxation under tensile strain, a smooth surface is achieved. Also, due to the high density of threading dislocations from the Ge underlayer dislocations are

able to glide and form misfit dislocations without significantly increasing nucleation processes. This results in low defect, low roughness high composition buffer which can be tailored to suit the purpose of the application (i.e. if cracking is a major issue and must be avoided; a thinner lower quality reverse graded buffer can be fabricated).

Wafer Number (Section Reported)	Overall Buffer Thickness (nm) (±2 %)	Effective Grading Rate (%/um^{-1}) (±1 %)	TDD (cm^{-1}) (±10 %)	Cleaved Crack Density (cm^{-1}) (±25 %)	SiGe Cap Composition (±0.005)	Relaxation Compared to Ge Underlayer (%) (±0.5)	Rq (RMS Roughness) (nm) (±0.2 nm)	Rmax (Height Range) (nm) (±2 nm)
4051 (RLG) (4.3)	2553	61.3	4.5 x 10^{6}	0.0	0.786	85.9	3.0	20.2
4345 (RTG) (4.3)	3931	12.6	2.1 x 10^{6}	30.7	0.765	89.2	1.9	11.5
4053 (RLG) (4.3)	4287	11.4	3.3 x 10^{6}	59.7	0.784	84.7	1.9	12.5

Table 6.1: A comparison of selected wafers that were examined in Chapter 4 with promising qualities. All wafers shown do not form stacking faults or cracks during growth of the wafer.

A comparison between RLG buffers and RTG buffers show no discernable difference between the surface roughnesses achieved by these techniques. However, a minuscule difference can be observed in the dislocation densities of buffers of similar thicknesses. RTG structures (wafer 4345, Table 6.1) have higher grading rates than RLG buffers for similar thicknesses, therefore the glide velocity of dislocations is higher resulting in the increased likelyhood of annihilation which leads to a lower TDD when compared to RLG structures (wafer 4053, Table 6.1). A separate set of truncated wafers were grown in addition to the varied grading rate set so that the quality of the buffer could effectively be tracked as it was grown. It was found that most of the dislocation annihilation, and therefore relaxation, occurs within the first 5% (Si composition) of the reverse graded region (Section 4.5.2).

It can be seen from Table 6.1 that an additional 1.3-1.7 μm in the thickness of the RLG graded region will yield an increased layer quality, but allow the formation of cracks if the buffer is cleaved. During this investigation the thick Ge underlayer and the thick SiGe cap were grown to allow ease of characterisation, but the significant increase in layer thickness is thought to induce cracking (Section 4.7). Therefore an investigation into reducing these layer thicknesses was performed.

The investigation of the pure Ge underlayer involved characterising the roughness and relaxation of the low temperature Ge (LT) layer, and the roughness, relaxation and dislocation density of the high temperature Ge (HT) layer on a ~100 nm LT layer as a function of thickness (Section 5.2). The roughness of the LT layer was found to increase with thickness and a thick LT layer was thought to be undesirable due to possible dislocation glide blocking effects. When reducing the HT layer thickness it was found that an anneal step after deposition of the HT layer is required to reach a low TDD of ~2 x 10^7. It was also then found that a HT Ge thickness of > 900 nm is required to keep the layer smooth (RMS surface roughness of 0.7 nm) after the 830°C anneal step. Therefore potential reduction of the two temperature Ge underlayer thickness is limited.

For the investigation of the SiGe cap thickness, the growth optimised Ge underlayer and RLG layer were used with varying SiGe cap thicknesses at a single growth temperature of 850°C (Section 5.3). It was found that the SiGe cap thickness which results in the highest quality buffer was ~630 nm with layer properties as shown in Table 6.2 (wafer 4804). This incidentally shows the best TDD achieved within this

thesis and did not show signs of cracking during growth, but did crack when cleaved. This optimal SiGe cap thickness had improvements both in roughness and defect level while a high level of relaxation was maintained.

Wafer Number (Section Reported)	Overall Buffer Thickness (nm) (±5 nm)	Effective Grading Rate (%/um^{-1}) (±1 %)	TDD (cm^{-1}) (±10 %)	Cleaved Crack Density (cm^{-1}) (±25 %)	SiGe Cap Composition (±0.005)	Relaxation Compared to Ge Underlayer (%) (±0.5)	Rq (RMS Roughness) (nm) (±0.2 nm)	Rmax (Height Range) (nm) (±2 nm)
4896 (RLG) (5.4.3)	1365	43.7	6.2×10^7	0.0	0.797	84.2	3.3	24.7
4946 (RLG) (5.4.2)	2718	15.1	4.1×10^6	0.0	0.796	85.0	2.1	16.0
4804 (RLG) (5.3)	3180	16.6	1.5×10^6	11.9	0.801	84.2	2.0	12.7

Table 6.2: A comparison of selected wafers that were examined in Chapter 5 with promising qualities. All wafers shown did not form stacking faults or cracks during growth of the wafer.

Two final structures were designed; one to limit the thickness of the buffer and another to be thinner than the 2.7 μm induced critical cracking thickness (Section 5.4). The characteristics of these buffers are shown in Table 6.2 as wafers 4896 and 4946. For the thinnest RLG buffer (wafer 4896) it is observed by XTEM that the severe reduction in thickness of the Ge underlayer increases the underlying defect density, and this in turn increases the final TDD of the buffer by more than an order of magnitude. Additionally, the surface roughness was measured to be 3.3 nm; over 1.5 times greater than shown previously. Reducing the buffer thickness is not a viable option for improvements in quality, and generally results in reduced quality. Wafer 4946 shows the properties of a buffer that is stable against cracking and has a low roughness and moderate defect level. It is deemed to be the best wafer which has been fabricated in this study.

In conclusion, reverse grading shows promising qualities for strain tuning platforms and potential opto-electronic integration of III-IV materials into standard Si technology. However, it is thought to require extra refinement to become a cheap viable platform.

6.2 Further Work

As this work comprises the first study on this proposed reverse graded technique there are many aspects that can be improved: material, growth, characterisation and application.

Material aspects:

1) The annealing trials performed in this study were done in an UHV system for high temperatures (T_{Anneal}> 550°C) at long times (> 30 mins). If even higher temperatures were used (850 >T_{Anneal} >1000°C) for short periods of time (< 5 mins) this would allow a transition of the Ge underlayer state from solid to liquid for a very brief period of time. It would be interesting to observe the effects of over-annealing. Additionally, thermal cyclic annealing and rapid thermal annealing (RTA) have been performed on other buffer techniques which yielded increased qualities of the buffer and could be applied to reverse graded buffers.
2) The TDD of the Ge underlayer has been shown to depend on the thickness of the HT layer (Section 5.2.3). In Section 5.4.2 a brief comparison was made showing the dependence of the defect level in the underlayer on the graded region. A further investigation would be required to confidentially quantify the effect of defect level in the Ge underlayer within the graded region.

Dislocation annihilation within the graded region could then be investigated. Additionally, it would be interesting to grow an optimised reverse graded structure on a high quality pure Ge (001) substrate to see the effect of completely removing the underlying dislocations.

3) It was shown in Section 5.3.4 that HT Ge layer growth on a rough LT layer showed significant smoothing of the surface. Subsequent annealing of the HT on LT Ge structures showed surface roughening which depended on the thickness of the HT layers. Further HT Ge growth and high temperature annealing on a thin Ge two temperature structure may possibly further lower the surface roughness and TDD levels might also further decrease. This would allow a thinner high quality Ge underlayer to be fabricated which would be applicable to the reverse graded structures.
4) It was shown in Section 4.5.3 that the majority of dislocations are annihilated in the first 5% of the reverse graded region. It has also been highlighted that dislocation velocity and hence the probability of annihilation increases with the strain gradient applied. Therefore if a reverse concave graded structure is designed so that low grading rates are applied at the start of the graded region and high grading rates are used at the end, a reduction of the buffer thickness *and* defect density may be observed.
5) If the final composition of the $Si_{1-x}Ge_x$ structure was graded to lower compositions ($0.2 \leq x \leq 0.8$) the enhanced smoothing effect and dislocation density from the underlying Ge layer could yield improved benefits for other alloy compositions which can then be used for other applications. An issue that could be studied is the grading rate required so that cracking of the buffer is avoided as this will have to be exceptionally high to keep the buffer thin.

This would allow a fuller experimental verification of the cracking model presented in Section 4.6.

Growth aspects:

1) For reverse grading to become a viable buffer technique for mass production the growth must take no longer than 30 mins per wafer [31]. This includes the time it takes to load and unload the wafer from the chamber. The studied buffers have a typical growth time of 2 hours, but can take up to 5 hours. Most of this time is taken by continual loading and unloading of the wafer to etch the wall deposition on the growth chamber, which is incurred during growth. An overall solution to stop chamber wall deposition is to replace GeH_4 with a germanium based precursor which requires a higher deposition temperature, for example $GeCl_4$; Germanium Tetrachloride. This will allow higher growth temperatures to be used as the transition temperature from the growth regimes (temperature limited regime to the flow limited) is much higher and therefore wall deposition could be limited.
2) It was mentioned in Section 4.7 that the dislocation annihilation rate within the graded region was much higher than the nucleation rate, which leads to the overall reduction in dislocation density. Since the growth temperature used in this study is very close to the melting point of pure Ge a lower growth temperature could further reduce the already low dislocation nucleation rate. This in turn could further reduce the final TDD in the buffer. Using the current precursors, a lower growth temperature could also reduce the wall deposition. Lower temperature growth is expected to slow growth rate and hinder the relaxation process within the reverse graded buffers. Therefore *in-*

situ post growth annealing will be required, which might additionally increase the growth time.

3) In Section 4.3.2 it is suggested that a fast growth rate is responsible for the Stranski-Krastanov 3D hillock formation whilst high grading rates are used. If the growth temperature of the reverse graded region was kept at 850°C whilst the precursor flow rates were calibrated for a slower deposition rate, very high grading rates could be achieved which result in a 2D Frank-van der Merwe growth mode. A comparison to the results already characterised in this study could then be made without the effect of heterogeneous dislocation nucleation due to surface roughening.
4) All growth parameters in this study were kept the same. A study on the effect of surfactant use could determine its contribution to surface smoothing. If optimised structures are fabricated with a variation in carrier gas flow, or even a change of carrier gas from nitrogen to hydrogen, a preliminary study could be performed.

Characterisation and Application

1) Many different techniques could be employed to further increase understanding of the current buffers. x-ray pole measurements on highly defected materials (i.e. LT Ge layers) could better determine the density and type of all dislocations in the layers.
2) Low energy SIMS on *all* samples used in this study could provide further insight into the mechanisms which occur during growth as layer thicknesses are changed.

3) X-ray topography will allow defects to be highlighted over a very large area (~100mm^2).
4) *In-situ* plan view TEM have been reported within MBE systems [50] which can provide real-time imagery for the formation and motion of dislocations within the structures.
5) The viability for strained Ge on reverse graded buffers for device applications could be studied. The critical thickness of strained Ge on RLG buffers, and oxide deposition studies would form the basis of an initial investigation.
6) The feasibility of optoelectronic III-V material integration (e.g. GaAs and AlAs) on reverse graded buffers could be performed.

A novel adaptation has been made to a recently proposed reverse grading technique to create high Ge composition SiGe virtual substrates. The proposed structures consist of a relaxed, highly defected, pure Ge underlayer on a Si (001) substrate prior to reverse grading where structures have nominal compositions of $Si_{0.2}Ge_{0.8}$. RLG and RTG structures have been grown by RP-CVD, using the growth parameters listed in Section 4.2.5. An investigation of the grading rates of these buffers was performed. Below a grading rate of 61.3 % μm^{-1} the system is grown in a 2D Frank-van der Merwe growth mode and relaxed under glide of dislocations. High quality layers are observed which are speculated to be due to the highly defected Ge underlayer and buffer relaxation under tensile strain. Above this grading rate three dimensional growth, stacking fault formation and crack generation can occur. Induced cracking is shown to occur in buffer thicknesses over 2.7 μm regardless of growth regime or grading rate. Cracking of the buffer has been calculated and some conditions where the buffer is stable have been found. This study experimentally

investigates this proposed solution and a crack-stable high quality buffer is fabricated.

Comparisons have been drawn with other buffer fabrication techniques and it is found that this technique has very competitive qualities. If further experimentation to improve buffer quality is performed, the buffer could quite realistically become a *fast-throughput industry favoured* technique for inducing global strain in MOSFET channel materials.

7 References

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