Probe Modules For Wafer-Level Testing Of Gigascale Chips With Electrical And Optical I/O Interconnects

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Probe Modules For Wafer-Level Testing Of Gigascale Chips With Electrical And Optical I/O Interconnects

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To my Parents,

Meena and Dilip,

and my sister, Reena,

for their endless support.

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The time I have spent in graduate school at Georgia Tech has been highlighted by innumerable positive interactions. These experiences have allowed me to grow as a student, as a researcher, and as a human being. I would like to take this opportunity to thank all those who have played a part in this.

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SUMMARY

The use of optical input/output (I/O) interconnects, in addition to electrical I/Os, is a promising approach for achieving high-bandwidth, chip-to-board communications required for future generations of high-performance chips. While numerous efforts are underway to investigate the integration of optoelectronics and silicon microelectronics, virtually no work has been reported relating to testing of such chips. The objective of this research is to explore methods that enable wafer-level testing of gigascale integration (GSI) chips with electrical and optical I/O interconnects. A major challenge in achieving this is to develop probe modules which would allow high-precision, temporary interconnection of a multitude of electrical and optical I/Os, in a chip-size area, to automated test equipment (ATE). A probe module would need to do this in a rapid, step-and-repeat manner across all the chips on the wafer. The design requirements of such a probe technology have been derived. Based on these requirements, two candidate probe modules have been devised, batch-fabricated on Si using microfabrication techniques, and successfully demonstrated. The probing techniques illustrated here would find application for testing a full range of devices with electrical and optical I/Os.

The first probe module consists of vertically compliant electrical probes alongside grating-in-waveguide optical probes. The compliant probes can contact an area-array of solder bump electrical I/Os; the grating-in-waveguide probes can interface with free space, quasi-free space, or guided-wave optical I/Os. A probe substrate with 10^3 electrical probes/cm^2 as well as grating-in-waveguide channels has been fabricated and demonstrated. The electrical probes have an average contact resistance of 0.5 Ω, and the grating-in-waveguide probes are shown to have a typical coupling coefficient, α, of 3.95 mm^{-1}. The design is scalable to higher probe densities. The second module is micro-opto-electro-mechanical-systems (MOEMS)-based and is designed to interface polymer pillar-based electrical and optical I/Os. Each probe resembles a microsocket, and is comprised of a through-substrate

via with thin-film cantilevers fabricated at the edge. Prototype probe substrates with microsocket probes at a 100 μm pitch (10^4 probes/cm^2) have been built. Probing of an area-array of optical and electrical polymer pillars has been demonstrated. Using a nanoindenter, the microsocket cantilever probes have been shown to survive $>$ 160,000 mechanical cycles without any change in mechanical performance.

High-density through-wafer interconnects are an essential attribute in both probe substrates for transferring electrical and optical signals to the substrate back-side. Fabrication and characterization of metal-clad, metal-filled, and polymer-filled through-wafer interconnects as well as process integration with probe substrate fabrication is described. Numerous possible redistribution schemes are explicated.

Chips with optical *and* electrical I/Os are an emerging technology, and one that test engineers are likely to encounter in the near future. The contributions of this thesis are to help understand and address the issues relating to joint electrical and optical testing during manufacturing.

CHAPTER I

INTRODUCTION

1.1 Motivation

The International Technology Roadmap for Semiconductors (ITRS) [1] projects that (some I/Os on) a GSI chip manufactured at the 14 nm technology node will have a chip-to-board speed of 88 GHz. To this end, it identifies optical interconnects as a potential enabling technology. Recent reports relating to the monolithic fabrication of photodetectors [2], modulators [3], and emitters [4] on Si have given rise to the *very* exciting prospect of combining optoelectronics and GSI in a high-volume manufacturing environment. Wafer-level, batch-fabricated, optical I/O interconnect technologies, which allow the juxtaposition of electrical and optical I/Os on a logic chip, have also been proposed [5, 6]. As these integration and interconnect technologies continue to evolve, it becomes essential to know how these chips with electrical *and* optical I/Os are to be tested in the manufacturing environment.

The die-under-test (DUT), in the context defined here, is a computing element with electrical and optical I/O interconnects (Figure 1.1 [7]). The logic remains at the core of the chip, and is surrounded by electrical and optical I/Os. An optoelectronic (OE) device and transmitter/receiver circuitry lie between the optical I/O and the logic. The optical I/O interconnect is essentially a very short optical link comprised of active OE devices (emitters, detectors, or modulators) as well as passive light guiding components (waveguides, mirrors, diffractive elements, optical I/O, etc.). Passive optical elements direct light from the source to the detectors. The placement of active devices is dependent on the application as well as the available technology. Possible implementations of such an OE-GSI chip are illustrated in Figure 1.2.

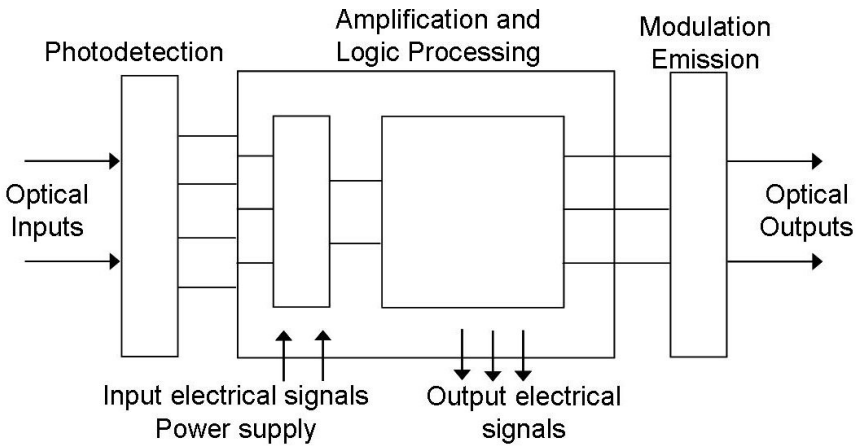
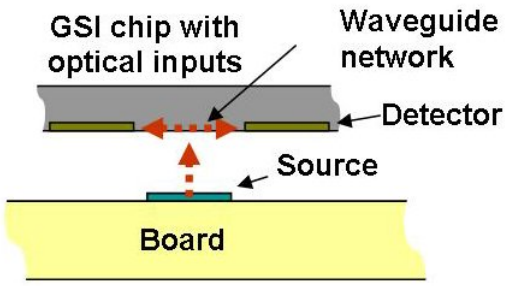


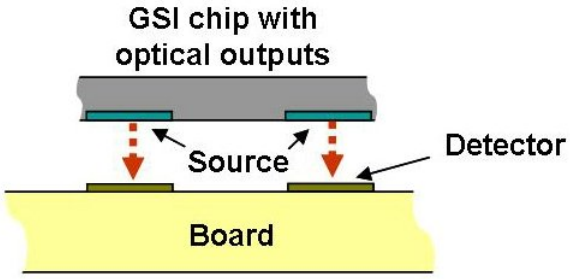
Figure 1.1: Block diagram of a chip with electrical and optical I/O interconnects.

A typical manufacturing process for an OE-GSI chip (Figure 1.3) would presumably begin with a bare silicon wafer, which at the conclusion of back-end-of-line (BEOL) processing is transformed into an area-array of OE-GSI chips with electrical and optical I/O interconnects. This is the first opportunity for testing a completely processed OE-GSI chip. Following convention, a probe module, under the control of ATE, would sequentially contact each die on the wafer in a step-and-repeat manner, and a series of short, decisive tests would be conducted at each touchdown. This is commonly referred to as wafer-sort testing or wafer probing [8]. Ideally, all bad dice would be identified during this step and discarded; all good dice would be sent onward for assembly and final testing.

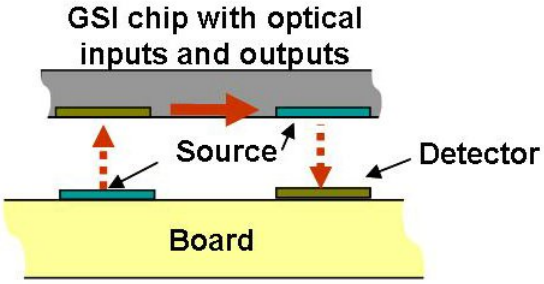
Wafer-sort testing directly impacts product yield, and therefore, needs to be as accurate as possible. Poor contact between even one I/O and it's corresponding probe can result in a chip being marked as non-functional. This possibility underlines the importance of having reliable probe hardware. To enable testing of OE-GSI chips in the near future, it is imperative to develop probe technologies that allow high-precision, temporary interconnections with electrical *and* optical I/Os in a rapid, step-and-repeat manner.



(a) Chip with optical inputs



(b) Chip with optical outputs



(c) Chip with optical inputs and outputs

Figure 1.2: Possible implementations of optoelectronic-GSI chips. In such chips, optical I/Os will exist alongside conventional electrical I/Os.

1.2 Background

The elementary purpose of testing in integrated circuit (IC) manufacturing is to assure that only known good dice (KGDs) are shipped to a customer. Unfortunately, the process of screening bad dice from good ones is a time-consuming and increasingly difficult task. Shrinking device geometries, increasing frequencies of operation, and the sheer magnitude of I/Os and transistors on a chip are all factors contributing to the increasing complexity of IC testing [9–11]. Figure 1.4 illustrates a typical sequence of tail-end-of-line (TEOL)

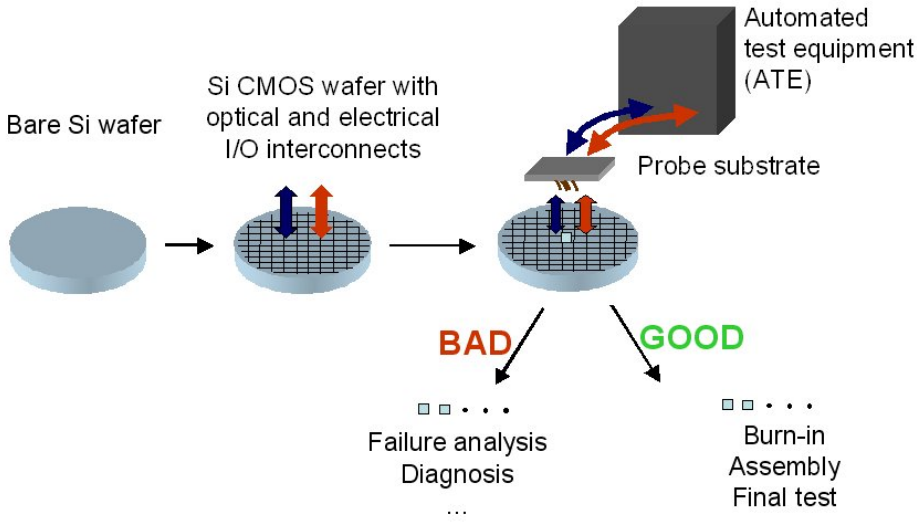


Figure 1.3: Schematic showing a typical manufacturing process for building an OE-GSI chip. Wafer-sort testing is performed immediately following the end of BEOL processing.

processes. It is economically advantageous to detect failures as early as possible during the production cycle [12]. The *rule of ten* is a common adage which states that the approximate cost of repairing a defect increases tenfold at each level [8]. As a result, chips are repeatedly tested following every major process in the TEOL.

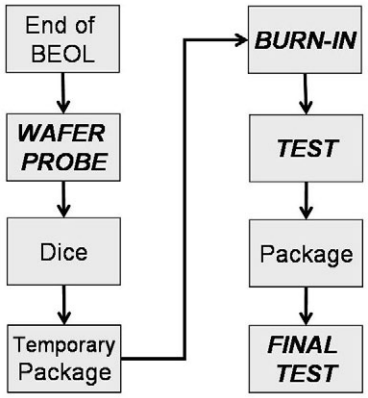


Figure 1.4: Flowchart of typical tail-end-of-line (TEOL) processes.

Wafer-sort testing is the first opportunity for testing a completely processed wafer. Figure 1.5 shows a typical probe test cell [13]. The test head and probe card are essentially high-quality interposers that help link the wafer-under-test to automated test equipment.

The design of these components entails careful consideration of electrical (high-quality signal transmission); mechanical (force exerted by probes on I/Os); and logistical (step-and-repeat as well as probe cleaning) issues [13].

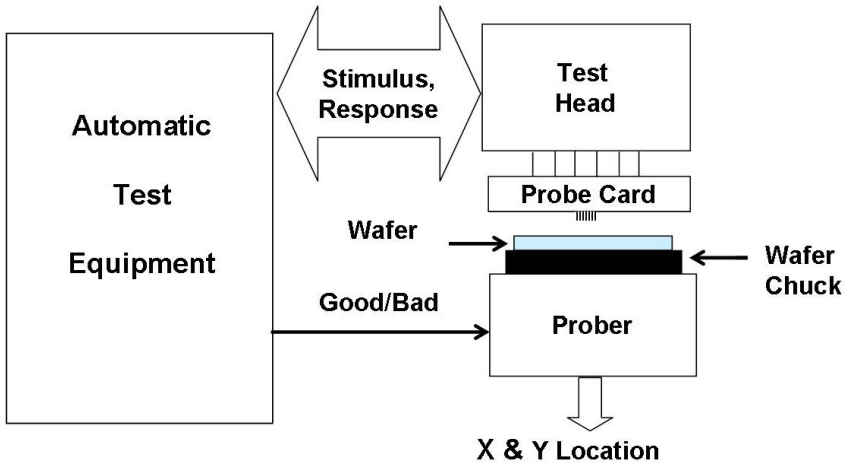
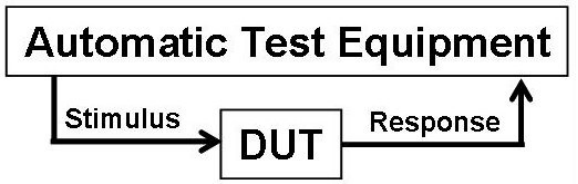


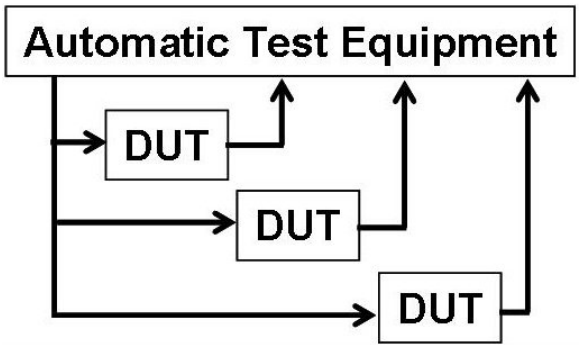
Figure 1.5: Schematic of a typical wafer-probe test cell.

From a test-plan perspective, a good balance must exist between cost-effectiveness and thoroughness of wafer-sort testing. Oftentimes, wafer-sort is an inadequate test, used only to detect the obviously defective chips; only between 75-95% of bad dice are typically detected during wafer-probing [14]. While this approach assures short wafer-test times and reduced wafer-probe costs, it could allow a significant percentage of chips (as high as 25%) to be sent onward for packaging. This is especially not acceptable for semiconductor companies whose business includes the sale of bare (unpackaged) dice. Longer tests are required for improving wafer-probe efficiency as well as for testing high-technology devices. To overcome the cost implications of this strategy, multi-die site testing [1, 15] and burn-in [13, 16] is gaining popularity. Short, inadequate tests on individual dice are being replaced by marginally longer, but more efficient, tests on multiple dice using the same test equipment. The concept is illustrated in Figure 1.6. The move towards multi-die wafer-testing has created a demand for multi-die site probe modules. Companies such as FormFactor, Inc. (Figure 1.7) and NanoNexus, Inc. (Figure 1.8) are producing probe modules able to contact >128

dice in parallel. Chips with optical I/Os will also need to traverse this same series of TEOL processes.



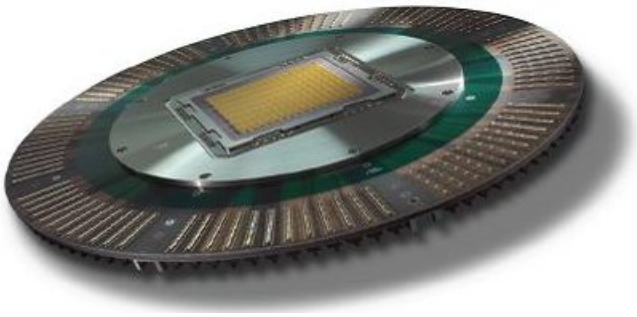
(a) Testing a single DUT



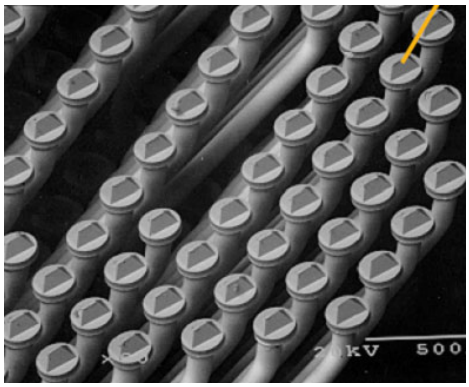
(b) Testing multiple DUTs

Figure 1.6: Implementation of (a) single DUT and (b) multi-DUT testing using the same ATE resources.

Stawiasz [17] describes the two basic approaches for automated testing of optoelectronic components: (a) a mixed-signal approach, and (b) an all-electrical approach. In the mixed-signal approach, both electrical and optical signals are used to test the DUT. It requires optical and electrical connection between the DUT and the ATE, and is most suitable for detailed electrical/optical characterization of components. Mixed-signal testing has been applied for testing parallel optical bus components [17] and metal semiconductor metal (MSM) receiver arrays [18]. It can be quite useful for component screening, sorting, and technology development. Using the all-electrical approach, the optical transmitter/receiver on the DUT is interfaced with a complementary *golden* (that is, of known performance) optoelectronic device during testing. For example, if the DUT has an OE emitter, then the *golden* device in the test setup is a photodetector. It captures the optical output from the emitter, and converts it into an electrical current. Conversely, the *golden* device is an OE emitter if the OE component on the DUT is a photodetector. The emitter converts



(a)



(b)

Figure 1.7: Images of microspring probes from FormFactor, Inc. (a) Probe array mounted on the redistribution interposer; (b) SEM image showing the high-density microspring probes.

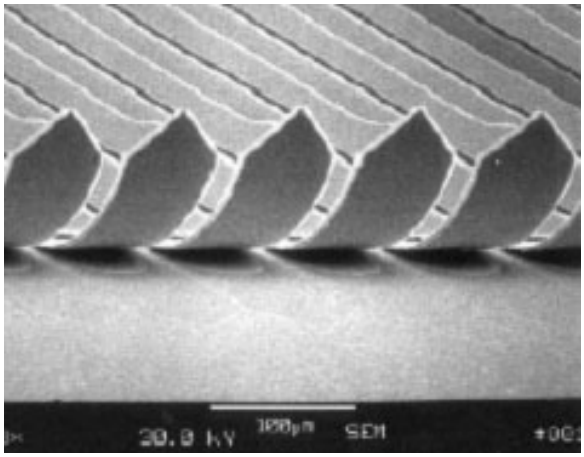


Figure 1.8: SEM image of self-assembled, stressed cantilever probes from NanoNexus, Inc. NanoNexus has built probe cards capable of contacting 128 chips in parallel.

electrical signals from the ATE to optical signals. All-electrical testing allows the use of standard ATE to be used for testing OE devices. This method has been used for wafer-level testing of lasers [19–22] and for testing parallel optical interconnect modules [23–25].

GSI chips with optical and electrical I/O interconnects are an emerging technology. As a result, at this time, no references discussing wafer-level testing of such chips were available. Achieving this will require a confluence of methods used for testing high-volume logic devices, optoelectronic devices, and optical interconnects.

Various probe module configurations for dual-signal (that is, electrical and optical) testing have been conceived as a result of this research. A probe module is typically comprised of a redistribution substrate and a probe substrate. It is assumed that the redistribution substrates will be implemented using standard organic or ceramic substrate technologies. Hence, their fabrication is not within the scope of this thesis. The contributions of this research include the design, fabrication, and demonstration of probe substrates for repeatably contacting DUTs with high-density electrical and optical I/O interconnects. All probe substrate fabrication was done on Si using standard IC and micro-electro-mechanical-systems (MEMS) processing methods. Solutions have been developed for interfacing both free-space and guided-wave optical I/O interconnects.

1.3 Objective of Thesis and Organization

The objective of this research is to explore prospects for wafer-level testing of chips with electrical and optical I/O interconnects. Virtually no work has been previously reported on this topic. As a result, there are two major areas where much innovation is needed: (a) developing short, high-confidence test methodologies that integrate the testing of optical components with current state-of-the-art digital and analog IC testing techniques, and (b) realizing practical, low-cost hardware to interface with chips having electrical and optical I/Os in a manufacturing environment. The latter is the focus of this dissertation.

This document is arranged as follows. The requirements of probe modules for testing OE-GSI chips are described in Chapter II. Electrical and optical through-substrate interconnects are an integral component for realizing the probe modules devised in this work. The design, fabrication, and characterization of electrical and optical through-substrate interconnects are detailed in Chapters III and IV, respectively. An all-electrical probe substrate

with vertically compliant probes is described in Chapter V. This probe substrate was enhanced to include grating-in-waveguide optical probes. The specifics of this integration and demonstration are provided in Chapter VI. The design and prototype fabrication of a novel MOEMS probe module for interfacing chips with polymer pillar-based I/Os are detailed in Chapters VII and VIII, respectively. The various experiments carried out to demonstrate successful probing of electrical and optical polymer pillar-based I/Os using this probe module as well as the results of mechanical characterization of the MOEMS structures are summarized in Chapter IX. Finally, conclusions of this research and a prospectus for future research in the area of joint wafer-level testing of chips with electrical and optical I/O interconnects are presented in Chapter X.

CHAPTER II

REQUIREMENTS FOR DUAL-SIGNAL HIGH-DENSITY PROBE MODULES

2.1 Introduction

Testing a GSI chip is a complex process, and one that carries with it immense cost implications – sometimes as much as 45% of the cost of production [8]. This cost is distributed over the entire manufacturing cycle from the design phase of the product to the cost of ATE. Therefore, much of the research in IC testing in recent times has been dedicated to making the test process more efficient.

Ultimately, the goal is to achieve maximum fault coverage with minimal effort (time and resources). For any DUT, the only way to assure 100% fault coverage is to apply every possible input pattern to the chip and compare the corresponding observed outputs to known good values. For a chip having N inputs, the number of input test vectors is given by 2^N. Needless to say, this process – labeled "exhaustive testing" – is quite impractical for chips with any significant number of inputs. As a result, most chip designers (if not all) have resorted to using design-for-testability (DFT) techniques, which increase controllability and observability during testing. Specifically, variations of *structured* DFT methods such as scan testing or built-in self test (BIST) are preferred. Using these methods, some extra logic and a few I/Os are added to the chip to conduct the test as per some defined procedure. The details of DFT will not be discussed here, and can be found in a book on digital IC testing such as [8].

Assuming that DFT techniques are employed, only a subset of the signal I/Os is needed, in addition to power and ground pins, for testing the logic [8, 26]. Then, one method for testing OE-GSI chips is to bypass the optical elements, and to use only electrical I/Os to

test the logic. However, this is not sufficient, and will need to be followed or preceded by tests designed to verify the operation of the non-DFT electrical I/Os as well as the on-chip optical elements (I/Os, OE devices). This disjoint approach is similar to the test strategy for testing optical channels recommended in [23, 25, 27]. Conversely, the test could also be performed using both electrical and optical I/O interconnects. By this method, correct operation of the logic implies that the I/Os (electrical and optical) used during testing are performing to specification. Additional testing to verify the functionality of the non-DFT I/Os (electrical and optical) would be needed.

Both approaches demand a probe module that can interface with high-density electrical and optical I/O interconnects. This is also identified as a long term goal in the ITRS [1].

In general, the probe modules conceived in this research are comprised of a probe substrate that is attached to a redistribution substrate (Figure 2.1). While the probe substrate maintains uniform contact with the I/Os of the DUT, the redistribution substrate routes test, power, and ground signals between the probe substrate and the ATE. The requirements of such a module are described in this chapter.

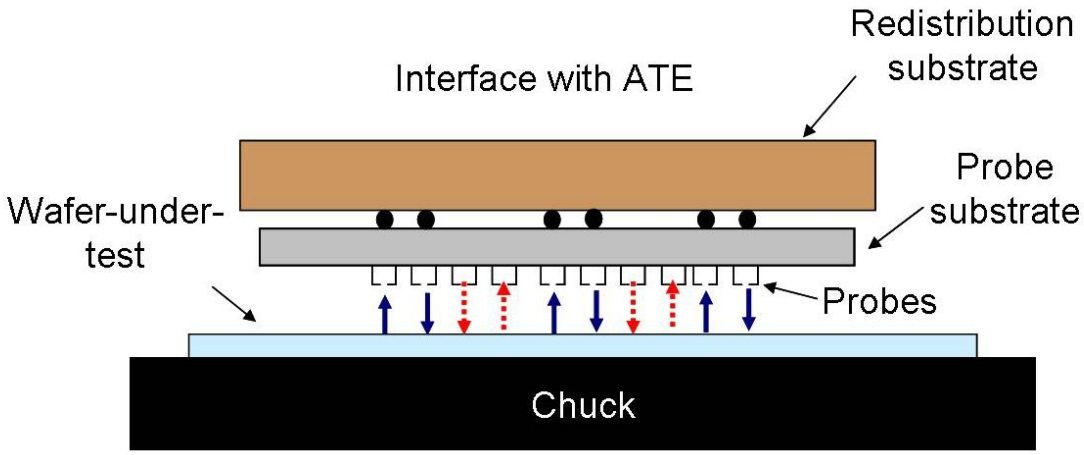


Figure 2.1: Schematic of a generic probe module that has been devised for dual-signal testing. It consists of a probe substrate attached to a redistribution substrate.

2.2 Requirements

The essential function of a probe is to interface with I/Os on the DUT. It should not load the DUT or cause any signal degradation [28]. In addition, it should be able to do this repeatedly (hundreds of thousands of touchdowns) [1] without damaging the I/Os. Of course, this delicate combination of high-quality electrical design and mechanical robustness needs to be achieved at the minimal possible cost. Adding optical testing capability to a high-density electrical probe substrate is a tall order. The requirements of such a probe substrate can be split into a three-level hierarchy: at the contact level, at the substrate level, and at the system level.

2.2.1 At the Contact Level

Following are the requirements at the immediate interface between the probe module and the I/Os of the DUT (Table 2.1):

- *Sufficient contact force:* Probes for electrical I/Os need to be in physical contact with them in order to complete an electrical path. The contact force exerted by the probes should be just enough to make good electrical contact, but not high enough to damage the I/Os or the interconnect stack and devices underneath.

- *Low contact resistance:* When two dissimilar materials are brought in contact with each other, their interaction causes an increase in the series resistance. This added resistive component is called *contact resistance* (R_{cont}). To minimize signal degradation, it is important that the design of the probes and the materials selected are such as to have the lowest R_{cont} possible. The ITRS [1] recommends a value of $R_{cont} < 1$ Ω.

- *Repeatability:* To minimize production-testing costs, it is mandatory that the selected probe technology be able to repeatedly make reliable contact with thousands of DUTs before cleaning or replacement of the probe substrate becomes necessary.

- *Out-of-plane compliance:* Out-of-plane compliance is needed to account for any surface non-planarity on the DUT and/or the probe substrate. This compliance can be built into the DUT I/Os, into the probe substrate, or both. Spring-loaded (vertical) and cantilever contact probes are well-suited for this purpose. However, with shrinking I/O pitches, new methods employing micromachining techniques are needed for manufacturing these cheaply. Industry requirements for out-of-plane compliance range anywhere between 20–100 μm [29, 30].

- *High-density:* It is imperative that the pitch of probes on a probe substrate keep up with that of the DUT I/Os. Beyond 2009, it is expected that area-array I/Os will have pitches < 90 μm; peripheral I/Os will have pitches < 20 μm [1].

- *Cleaning mechanism:* Oftentimes, the cause for degradation of probe contacts is the accumulation of tiny amounts of materials that attach to them during repeated contact with the DUT I/Os. Probe lifetimes can be extended by a brief cleaning process, which can be either mechanical (scrubbing) or chemical (etching). Therefore, as a value-adding feature, any new probe technology should also be easy to clean.

- *Optical I/O probing:* Probing an optical I/O is completely different from an electrical I/O, and not as straightforward. The simplest way to interface an optical I/O is to place a photodetector or photoemitter directly above the I/O. In this case, the optical-to-electrical (O/E) or electrical-to-optical (E/O) conversion occurs immediately at the point of contact and eliminates the need for any optical signal redistribution. It also means that chips with electrical and optical I/Os could be tested with conventional electrical test equipment. However, integration of high-density OE devices on the probe substrate could be quite challenging, and there would be some concern whether these heterogeneous assemblies could be reworked if they happen to fail during test operation.

  On the other hand, passive optical elements feeding into an optical waveguide network

could be used to transfer unadulterated optical signals between the DUT and ATE. Specifically, this includes reflective (metallic or total internal reflection (TIR) mirror) or diffractive (volume or surface grating) elements. The different optical probing methods are illustrated in Figure 2.2.

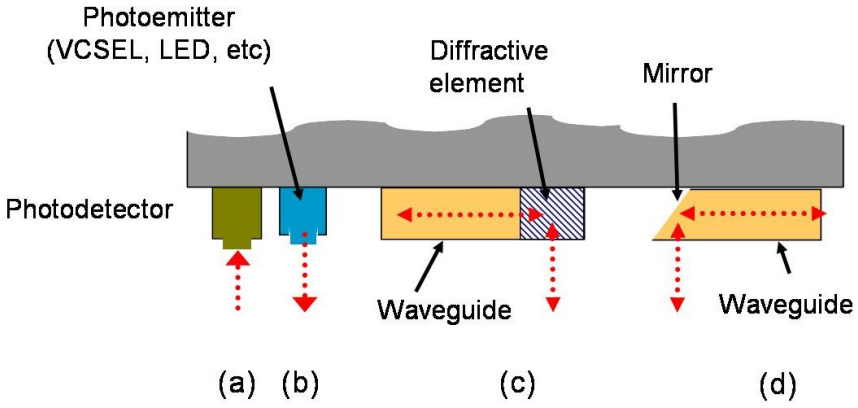


Figure 2.2: Various optical elements that may be used for capturing or transmitting an optical signal during testing: (a) photodetector, (d) photoemitter, (c) waveguide with a diffractive element, and (d) waveguide with a TIR or metallic mirror.

Table 2.1: Probe module requirements at the contact level.

Contact Level
Sufficient contact force
Low contact resistance
Repeatability
Out-of-plane compliance
High-density
Cleaning mechanism
Optical I/O probing

2.2.2 At the Substrate Level

Following are the requirements for the different substrates of the probe module (Table 2.2):

- *High-density interconnects:* Beyond 2012, it is estimated that a wafer-prober will need to contact as many as 2,000 signal I/Os (and 30,000 total I/Os), fabricated at a 90 μm pitch, per touchdown for a wafer of microprocessor chips [1]. High-density

interconnection technologies will be needed to redistribute these signals from the probe points.

- *Pin-count reduction:* As ATE units are built on a per-pin architecture, their cost scales linearly with pin-count. Therefore, it is not expected that ATE pin-counts will keep up with increasing DUT I/O counts. This mismatch calls for some pin-count reduction techniques to be implemented on the probe module. The use of common power and ground planes, combination of other common control signals, and signal multiplexing techniques are some ways of achieving this.

- *Matched coefficient of thermal expansion (CTE) to DUT:* Wafer-sort testing is done at a few different temperatures (-40°–140°C). A temperature difference between the probe substrate and DUT can cause them to expand at different rates if there is a mismatch in their respective CTEs. To avoid any missed contacts resulting from this, it is desirable that the two substrates have a closely matched CTE. Although in-plane compliance is another way of accounting for different rates of expansion, having in-plane compliant probes deteriorates their positional accuracy.

- *Integration of optical components:* A probe module configuration could call for the hybrid integration of active optical devices on the probe or redistribution substrate. Therefore, the substrate technology ought to be compatible with the appropriate device attachment technique as well as process compatible with optical waveguide and passive optical element fabrication.

Table 2.2: Probe module requirements at the substrate level.

Substrate Level
High-density interconnects
Pin-count reduction
Matched CTE between probe substrate and DUT
Integration of optical components (active and passive)

2.2.3 At the System Level

Following are the requirements of the probe module as it relates to the wafer prober system (Table 2.3):

- *Repeatable acceptable optical alignment:* Repeatable and accurate probe-to-pad alignment is an important requirement during electrical testing especially as target I/O dimensions become smaller. Alignment will be even more critical when trying to probe optical I/Os. The ITRS projects that wafer probers ought to have no more than 3.5 μm probe-to-pad misalignment beyond 2009 [1]. While this would certainly be acceptable for aligning multi-mode optical components, it may be too high for probing single-mode optical elements.

- *Multi-die/wafer-scale contact:* Multi-die site testing is already being used extensively for testing memory device wafers. Parallel testing of application-specific integrated circuits (ASICs) and microprocessor chips is not too far away [1]. Keeping with this trend, probe modules for testing chips with electrical and optical I/O interconnects should also be scalable for multi-die site testing.

- *Efficient thermal management:* While it is cost-efficient to test as many chips in parallel as possible, the wafer prober should have an effective way of removing the heat generated during testing. This is a huge overload on probing systems. In addition, thermal variations can also affect optical signal transmission and devices. Therefore, systems for testing chips with electrical and optical I/Os have an added importance for sound thermal management.

- *Minimal cost:* Probe modules can often run upwards of $100,000 [31]. While the addition of optical probing capabilities will add to the cost of probe modules as well as ATE systems, a low cost design mindset from the onset is recommended.

Table 2.3: Probe module requirements at the system level.

System Level
Repeatable acceptable optical alignment
Multi-die/wafer-scale contact
Efficient thermal management
Minimal cost

2.3 Conclusion

Based on the previous section, it is safe to conclude that the requirements of a probe module for dual-signal testing are very diverse in nature. These requirements have purposely been kept as universal as possible, and it is expected that there may be some additions to this list for specific DUTs and I/O interconnect structures. However, having knowledge of these general requirements forms a solid basis from which successful practical implementations of dual-signal probe modules can be realized.

CHAPTER III

ELECTRICAL THROUGH-WAFER INTERCONNECTS

3.1 Introduction

By virtue of the piece-wise design of the probe module illustrated in Figure 2.1, the bulk of the signal distribution network can be implemented on the redistribution substrate. However, at least the first level of signal redistribution – between the probes and redistribution substrate – has to be realized on the probe substrate. To achieve this, vertical through-wafer interconnects (TWIs) have been designed and fabricated. This chapter details the design, fabrication, and characterization of electrical TWIs. Optical TWIs are discussed in Chapter IV.

Prospects for using electrical and optical TWIs extend beyond the current application. Interconnects are the primary limiter to improving the performance of integrated circuits [32]. Three-dimensional (3D) integration has the potential to alleviate this problem through shortening the length of the interconnects [33]. In addition, there is growing interest in building heterogeneous microsystems with combined electrical and optical functionality. Vertical TWIs, as described in this thesis, would be a key enabling technology for interconnecting different substrates in a 3D-IC (all-electrical or heterogeneous).

Although a simple structure, numerous variations of TWIs have been previously proposed for use as electrical [34–37], optical [38, 39], and microfluidic [40–42] conduits. The novelty of this work is the realization of high-density electrical TWIs as well as guided-wave optical TWIs (Chapter IV).

3.2 Through-Wafer Interconnect Design

There are potentially two ways of transferring electrical signals from the probe substrate to the redistribution substrate. The first is to fan-out the signals from the probes to an array of

peripheral pads on the probe-side of the probe substrate. From here, an assembly technique, such as wire bonding, could be used to connect each of the pads to corresponding pads on the redistribution substrate. This approach is illustrated in Figure 3.1. Unfortunately, the height of the wire bond loop, which can range from 40 μm to 150 μm [43], would likely cause these wires to contact the DUT before the probes themselves. In addition, for high-density area-array probes, it could be quite challenging (if not impossible) to fan-out all the signals to a peripheral pad array configuration using a single metal level. An alternative method of redistribution is to fabricate vertical TWIs directly underneath the area-array of probes (Figure 3.2). Not only do vertical TWIs help overcome any density limitations, but a vertical interconnect is also the shortest path between the front- and back-side of the probe substrate.

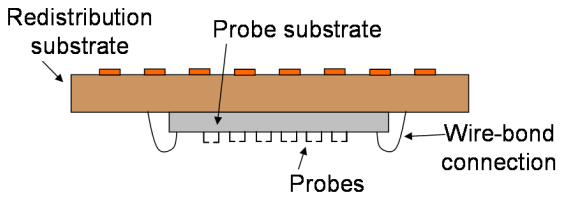


Figure 3.1: Schematic showing a probe substrate attached to a redistribution substrate by wire-bonding. If the radius of the wire-bond loop is larger than the height of the probes, then they would would make contact with the DUT before the probes, which is undesirable.

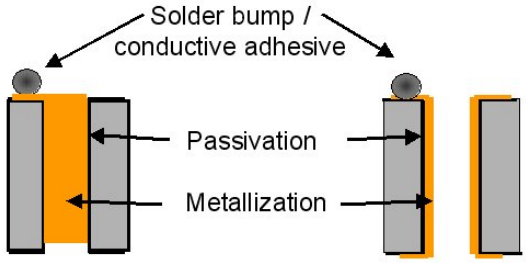


Figure 3.2: Electrical through-wafer interconnects consist of through-wafer vias; an insulating layer; and either a conductive filling or lining.

Through-wafer vias (TWVs) etched in the substrate form the building block for this

interconnection scheme. For electrical transmission, the vias can be lined or plugged with a conductive material such as copper (Figure 3.2). The metallization step would typically be preceded by deposition of a dielectric layer to isolate the signal interconnect from the substrate.

3.3 Fabrication

Through-wafer interconnects are made possible entirely due to advances in Si bulk micromachining techniques. The three major process modules required to achieve them are anisotropic via etching, via isolation, and via metallization.

3.3.1 TWV Etching and Isolation

3.3.1.1 Wet etching

Basic aqueous solutions of potassium hydroxide (KOH) or tetramethyl ammonium hydroxide (TMAH) etch the (100) plane of silicon preferentially over the (111) plane. As a result, they etch Si along the (111) plane yielding trenches with 54.7° sidewalls (for a (100) wafer) as shown in Figure 3.3 [44]. Detailed processing conditions for wet anisotropic etching of Si using KOH or TMAH are described in [44, 45]. Either SiO_2 or Si_3N_4 can be used as a masking layer for wet Si etching as they have very high selectivities; photoresist is etched almost immediately in these solutions and cannot be used as a masking material. If the via openings are made wide enough, a long wet process could be used to etch through the entire thickness of a wafer. Unfortunately, the sidewall angle severely limits the density of TWVs achievable by this process; a via would need to be approximately 710 μm wide for etching through a 500 μm wafer. As a result, this process was not suitable for fabricating TWIs in the probe substrate. A scanning electron microscope (SEM) image of a sample having an array of trenches etched in TMAH is shown in Figure 3.4.

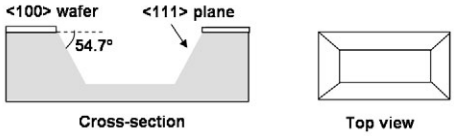


Figure 3.3: Aqueous solutions of KOH and TMAH etch (100) Si anisotropically along the (111) plane to produce trenches with 54.7° sidewalls.

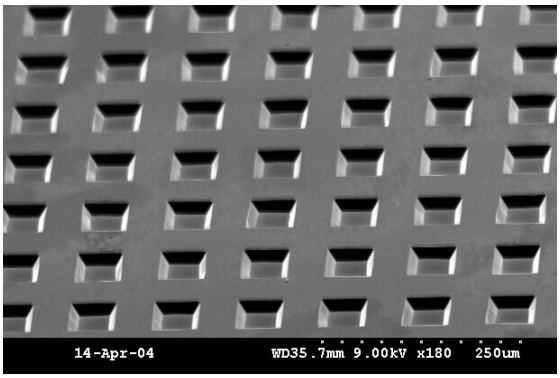


Figure 3.4: Array of trenches etched in silicon using TMAH. The sidewalls are inclined at a 54.7° angle.

3.3.1.2 Laser ablation

High-power laser pulses can also be used to drill vias in silicon. The high-energy beam incident on the silicon vaporizes the material, leaving behind a via with near-vertical sidewalls. However, laser ablation is a sequential process whereby a computer-controlled laser beam impinges the wafer at predefined locations. An advantage of laser ablation is that no photolithography is needed prior to via etching. The via dimensions are limited by the width of the laser beam. SEM images of vias drilled with an excimer and an infrared (IR) lasers are shown in Figures 3.5 and 3.6, respectively.

The diameter of vias etched using an excimer laser was roughly 72 μm. An IR laser produced vias with a diameter of approximately 35 μm. In both cases, the via sidewalls appeared to be quite rough. In addition, it was observed that some of the vaporized Si from the ablated via condensed on the back-side of the wafer (Figure 3.7). For these reasons,

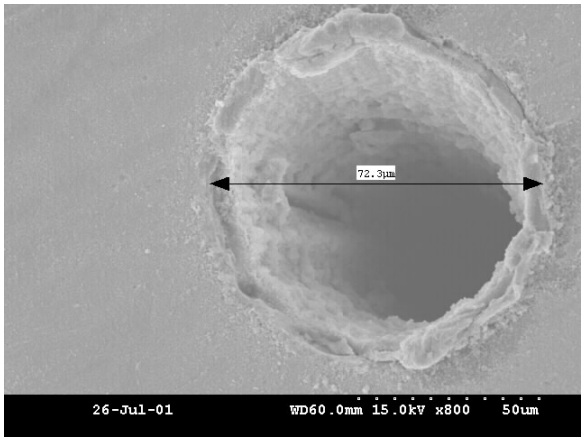


Figure 3.5: SEM image of a through-wafer via etched using excimer laser ablation.

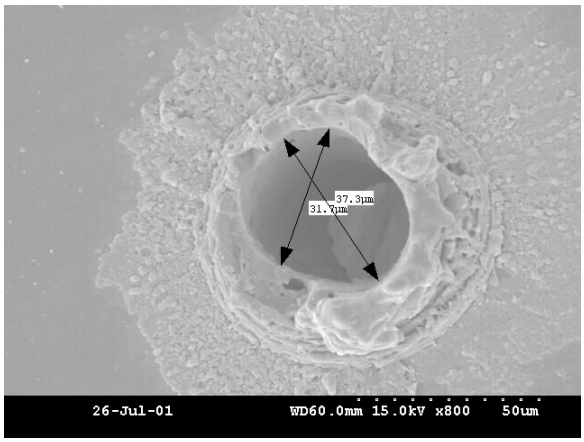


Figure 3.6: SEM image of a through-wafer via etched using IR laser ablation.

and the sequential nature of the process, laser ablation was also concluded to be unsuitable for high-density TWV fabrication.

3.3.1.3 Plasma etching

The Bosch process [46, 47] enables etching of high aspect-ratio (AR) features in Si. This is a much desired characteristic as it helps overcome the density limitations of wet etching. An optimized Bosch process will yield vias in Si with nearly 90° sidewalls. It is a dry etch process, typically performed in a high-density inductively-coupled-plasma (ICP) etching tool, wherein the etch profile is highly directional. All vias across an entire wafer are etched in parallel, which makes it advantageous over the sequential laser ablation process.

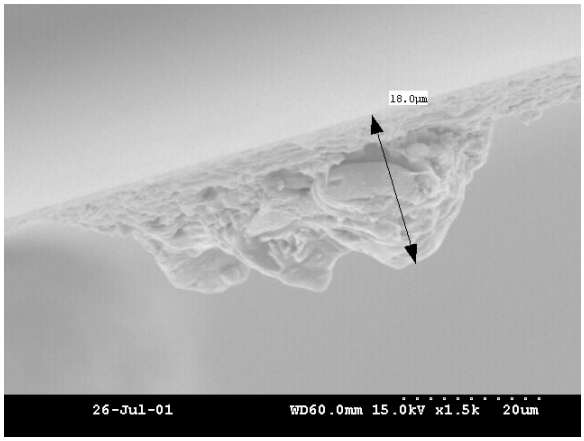
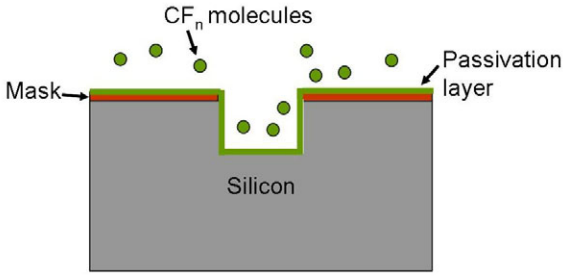


Figure 3.7: SEM image showing the build-up of condensed Si on the back-side of the wafer after laser ablation.

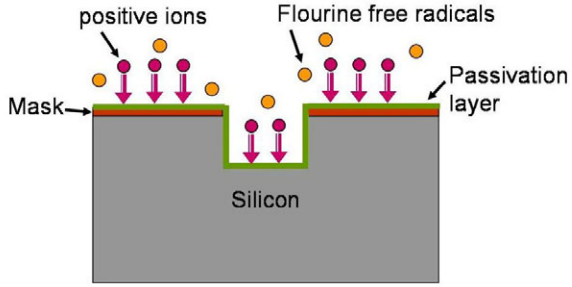
A Surface Technology Systems (STS) ICP was used for TWV etching. It implements an adaptation of the Bosch process called advanced silicon etch (ASE^{TM}) [48, 49]. Like the Bosch process, it consists of two steps – passivate and etch – that are executed repeatedly to yield deep high AR trenches. During the passivation segment, C_4F_8 gas is introduced in the chamber. This deposits a flourocarbon polymer on all exposed surfaces (Figure 3.8 (a)). During the etch step, the C_4F_8 is supplanted with SF_6. Highly directional fluoride ions accelerating towards the sample remove the passivation from the bottom of the features, but not the sidewalls (Figure 3.8 (b)). The remaining part of the etch cycle is simply a short isotropic Si etch due to the free F radicals (Figure 3.8 (c)). For this reason, close observation of features etched using the Bosch process reveal them to have slightly scalloped sidewalls. Vias with aspect-ratios as high as 49 have been reported in literature [50]. Table 3.1 lists the values of various parameters for a typical ASE process, which was recommended for TWV etching.

3.3.1.4 Bosch process optimization

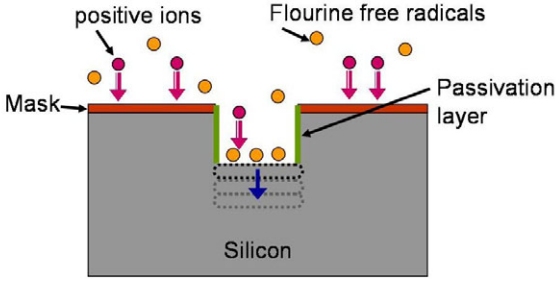
There are a number of Bosch process parameters that must be tweaked to achieve structures having perfectly vertical (90°) and smooth sidewalls. The important parameters include duration of the etching and passivation steps, volumetric gas flow rates, and applied power.



(a) Passivation



(b) Removal of passivation at bottom of features



(c) Short isotropic etch of Si

Figure 3.8: Illustration of the Bosch process.

Table 3.1: Base ASE process conditions recommended for TWV etching in the STS ICP.

	Etch	Passivate
C_4F_8 [sccm]	0	100
SF_6 [sccm]	130	0
O_2 [sccm]	13	0
Time [s]	10	8
Platen Power [W]	13	0
Pressure [mTorr]	0.1	0.1
Coil Power [W]	600	600

They affect not only the form of the final etched structure, such as sidewall roughness and anisotropy, but also etch metrics such as etch rate and etch selectivity (between the masking

layer and Si). The effect of these individual parameters is summarized in Table 3.2 [49].

Table 3.2: Impact of changing Bosch process parameters on etch rate, sidewall profile, and etch selecttivity.

Parameter	Change	Etch Rate	Sidewall Profile	Selectivity
RIE (13.56 MHz) Power	↑	↑	towards re-entrant	↓
	↓	↓	towards positive	↑
Etch Time	↑	↑	towards re-entrant	↓
	↓	↓	towards positive	↑
Pressure	↑	↑	towards re-entrant	–
	↓	↓	towards positive	–
C_4F_8 Flow	↑	↓	–	↑
	↓	↑	–	↓
SF_6 Flow	↑	↑	towards re-entrant	–
	↓	↓	towards positive	–

During fabrication, three major problems were observed for which the process had to be optimized.

1. *Si grass:* Oftentimes, at the conclusion of the Bosch process, it was observed that several high aspect-ratio strands of Si remained unetched and attached to the bottom of the vias. This is a fairly common problem, and the unetched Si strands are called Si grass due to their appearance (Figure 3.9).

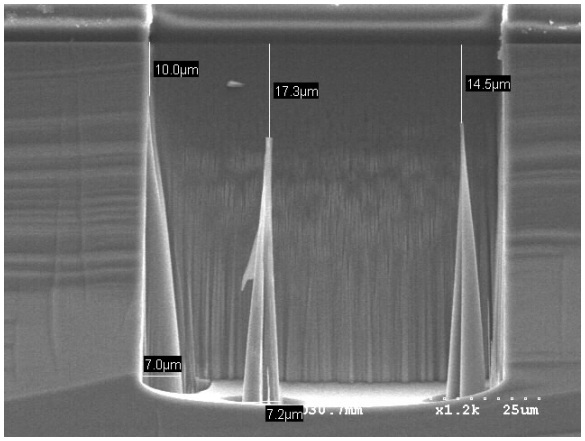


Figure 3.9: Cross-sectional SEM image of a via etched using the Bosch process. The unwanted spikes of Si within the vias are called Si grass.

Si grass typically occurs due to a phenomenon called micromasking. If, during the

etch step, some contaminant particles land on the exposed Si, then they can behave as a micromask; once in place, these particles protect the small areas of Si underneath them. Owing to the anisotropic nature of the Bosch etch, this gives rise to blades of Si grass within the feature. In a multi-user facility, such as the Georgia Tech Microelectronics Research Center (MiRC) cleanroom, contamination control within the plasma tools can be quite tedious.

Insufficiently cured photoresist was also deduced to be a source of contamination. If the photoresist mask is not sufficiently cured, it is possible for photoresist particles to get detached from the surface of the wafer during the first part of the etch cycle and re-sputtered onto the open Si areas that are to be etched. These small photoresist particles would then serve as micromasks.

Once present, Si grass is impossible to remove without affecting the features on the wafer. Slightly increasing the curing time of the photoresist and running O_2-plasma cleaning processes in the ICP were effective in eliminating Si grass. Using SiO_2 as a masking layer would also eliminate possibility of contamination due to photoresist.

2. *Rough sidewalls:* Sidewall roughness was another common observed imperfection. In initial runs, the sidewalls of the vias would either appear to have folds like a drape (Figure 3.10), or they would appear to have vertical striations, almost grassy or fibrous (Figure 3.11).

   While patterning the masking layer, if the lithography and mask-etching steps are not performed in a well controlled manner, they tend to have slightly jagged edges. This uneveness in the masking layer is likely to transfer to the etched vias. After a long etch, this would make the sidewall surfaces look drape-like. Indeed, precise lithography and etching lead to removal of these artifacts.

   It was concluded that excessive passivation polymer adhering to the sidewalls of the via was causing vertical striation-like features to appear on the sidewalls. To negate

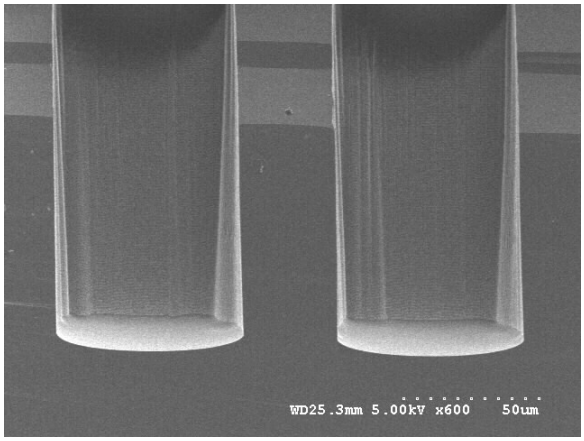


Figure 3.10: SEM image showing drape-like formations on the via sidewalls.

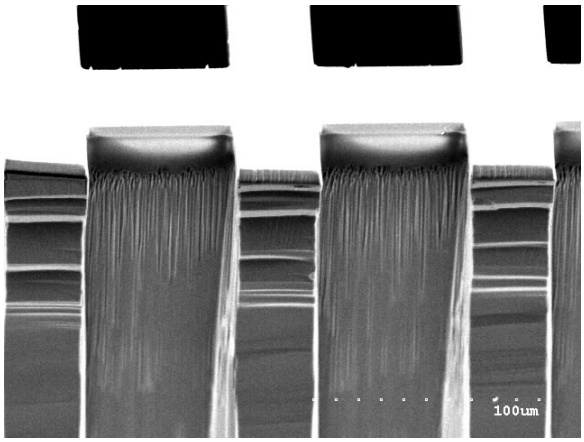


Figure 3.11: Image of Si via with very rough sidewalls.

this, three variations of the base ASE process (Table 3.1) were attempted. In the first, the flow rate C_4F_8 was reduced from 100 standard cubic centimeters per minute (sccm) to 85 sccm. Lower C_4F_8 flow rate causes a smaller amount of passivation on the wafer. In the second variation, 3 watts (W) of power was introduced during the deposition step. The additional bias increases the directionality of the flourocarbon deposition. That is, a lesser amount of polymer is allowed to adhere to the via sidewalls. The final process variant involved reducing the deposition time from 8 seconds (s) to 7 s; shorter deposition time also equates to a smaller amount of polymer deposition. The conditions of these processes are summarized in Table 3.3. Visual inspection

of via cross-sections fabricated by the first two variants revealed that they were not effective (Figures 3.12, 3.13). Lowering the passivation time seemed to improve this defect (Figure 3.14); however, the vias appeared to be slightly bulging in the center. A fourth variation of the standard recipe was created in which all three of the changes described above were introduced simultaneously. As can be seen from the SEM images in Figure 3.15, the improvement in roughness was comparable to that obtained by only reducing the passivation time. In this case, the vias did not have a bulging center. Therefor the process in column IV of Table 3.3 was concluded to be the optimal process for TWV etching.

Table 3.3: Summary of Bosch process variations attempted for etching optimization.

	I		II		III		IV	
	Etch	Pass.	Etch	Pass.	Etch	Pass.	Etch	Pass.
C_4F_8 [sccm]	0	85	0	100	0	100	0	85
SF_6 [sccm]	130	0	130	0	130	0	130	0
O_2 [sccm]	13	0	13	0	13	0	13	0
Time [s]	10	8	10	8	10	7	10	7
Platen Power [W]	13	0	13	3	13	0	13	3
Pressure [mTorr]	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Coil Power [W]	600	600	600	600	600	600	600	600

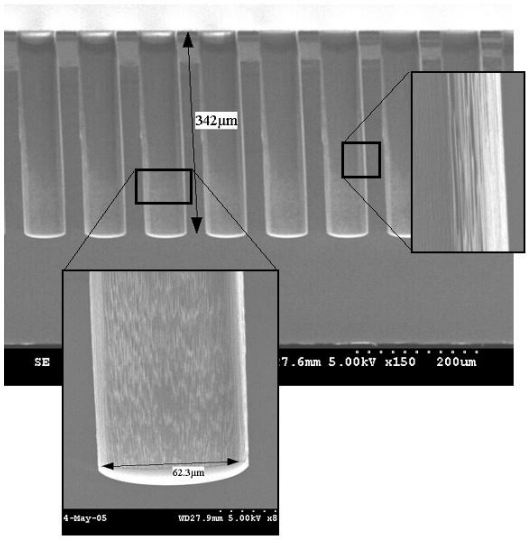


Figure 3.12: Cross-section of via etched using Bosch process with C_4F_8 gas flow lowered to 85 sccm. The sidewalls still appeared to be quite rough.

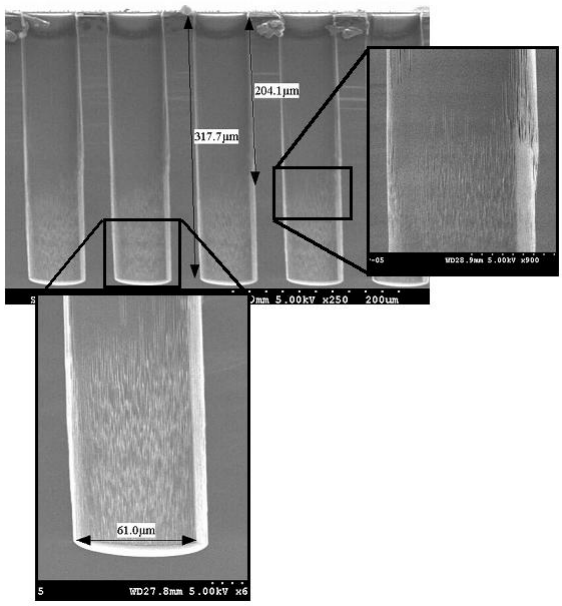


Figure 3.13: Cross-section of via etched using Bosch process with 3 W power added during passivation step. The sidewalls appeared to be quite rough.

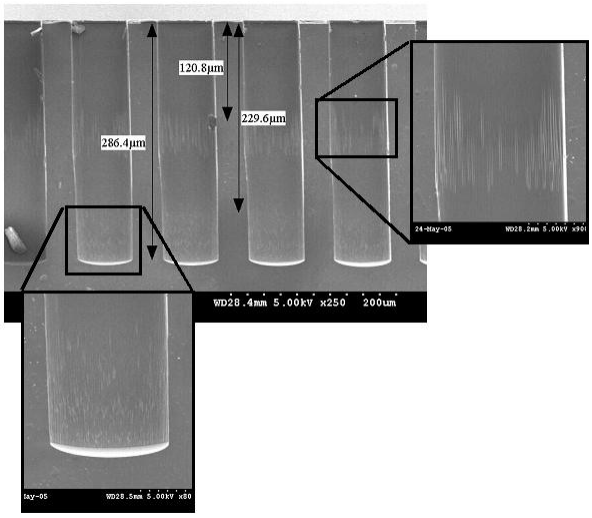


Figure 3.14: Cross-section of via etched using Bosch process with a shortened (7 s) passivation time. While this alteration reduced sidewall roughness, the vias appeared to be slightly bulged at the center.

3. *Notching:* The very bottom of the vias, near the SiO_2 etch-stop layer, was often seen to be wider than the rest of the via, almost as if the process had lost it's anisotropic nature towards the very end (Figure 3.16). This observation has been reported previously

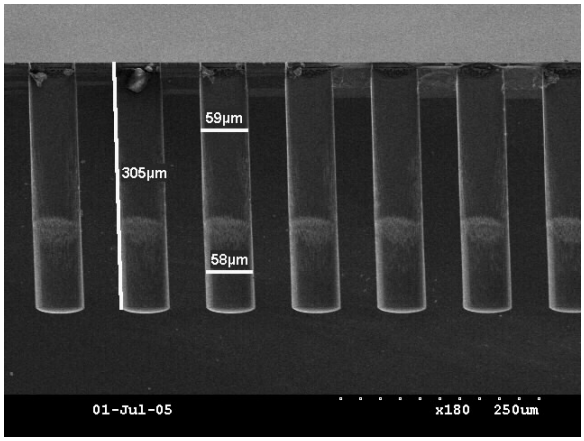


Figure 3.15: Cross-section of via etched using Bosch process with C_4F_8= 85 sccm; passivation power= 3 W; and passivation time= 7 s. The vias had the desired anisotropy as well as low sidewall roughness.

[48], and is termed notching. Charge build-up at the Si/SiO_2 interface causes the rate of lateral etching in this region to be higher than the rate of vertical etching. This results in widening of the features at the interface. Notching was minimized by timing the etch to stop just short of the Si/SiO_2 interface, and then etching further in small increments. While this was implemented successfully, low frequency (380 KHz) plasma processes have been shown to reduce notching and are proposed for use at the very end of a long Bosch process [48].

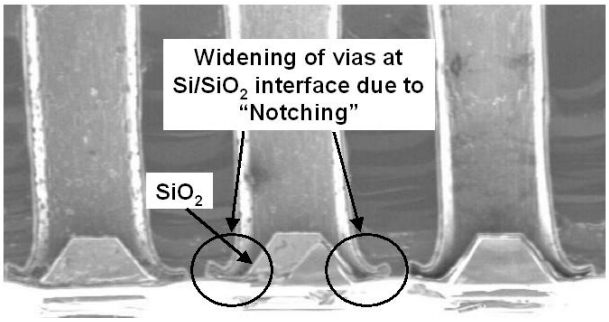


Figure 3.16: Cross-section of TWV where notching at the Si/SiO_2 interface is observed.

3.3.1.5 Via isolation

Contact between the Si substrate and a metal interconnect would result in the formation of a Schottky contact [51]. To avoid this, a dielectric layer is needed to isolate the substrate from the metal in the TWV. Amorphous SiO_2 and Si_3N_4 are excellent choices for use as dielectrics. These can be deposited using plasma-enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD), or thermal oxidation (for SiO_2). For the TWVs, it is desirable to achieve the most conformal deposition possible across the depth of the structure (350–500 μm).

The thickness of films deposited by PECVD processing tends to be maximum at the top-most surface; film thickness decreases with increasing via depth [50, 52]. For TWVs, uniformity of the dielectric can be improved by first depositing material from one side of the wafer followed by the other. In this case, the sidewalls halfway in the via would have the thinnest layer of dielectric. While PECVD films were considered to be a viable alternative for via isolation, it was concluded that the process itself was not optimal for TWV fabrication.

On the other hand, thermal oxidation can be used to grow a very conformal layer of high-quality SiO_2 everywhere on the exposed silicon. It is described by the following chemical reaction (dry oxidation):

$$\mathsf{Si(solid)} + \mathsf{O_2(gas)} \rightarrow \mathsf{SiO_2(solid)} \tag{3.1}$$

Alternatively, water vapor can also be used as the oxidant (wet oxidation):

$$\mathsf{Si(solid)} + \mathsf{H_2O(vapor)} \rightarrow \mathsf{SiO_2(solid)} + \mathsf{2H_2} \tag{3.2}$$

Oxidation processes are typically carried out at high temperatures (950°–1150°C). The kinetics of these chemical reactions are well understood. The Deal-Grove [53] model can be used to calculate the process time (at a certain temperature) to obtain a desired thickness of oxide on the wafer by wet or dry oxidation. Oxide growth rate slows rapidly with

increasing film thickness; hence, the process is generally considered practical only when <2 μm of SiO_2 is desired. Overall, thermal oxidation was a suitable process for depositing a dielectric on the sidewalls of the TWVs. LPCVD of Si_3N_4 was also another option available in the MiRC cleanroom, but was not attempted.

3.3.1.6 Process summary: TWV etching and isolation

Figure 3.17 shows the process flow for TWV fabrication. Fabrication was done on a 400 μm thick, double-side polished, (100) orientation, single crystal silicon (SCS) wafer. Construction of TWVs begins with the deposition of 0.5–1 μm of SiO_2, in an STS PECVD system, on the back-side of the wafer. The oxide layer serves as an etch-stop for the forthcoming via etch. A 10 μm thick layer of NR5-8000 negative photoresist from Futurrex was spun onto the front-side of the wafer, and vias were patterned in the resist using ultraviolet (UV) lithography. Following this, vertical TWVs were etched in Si using the Bosch process in the STS ICP. The Bosch process parameters used for this are listed in column IV of Table 3.3. Circular TWVs of 45–60 μm diameter and square TWVs of 45-65 μm width have been successully etched using this recipe. The etch rate is higher for features with larger dimensions, but have been observed to saturate as feature sizes exceed 100 μm [54]. In this process, the etch rate was calculated to be $\sim$1.40 μm/min for a 52 μm-wide square via, and $\sim$1.8 μm/min for a 64 μm -wide square via. The etch selectivity of Si:NR5-8000, for this process, was measured to be approximately 70:1.

NR5-8000 was subsequently removed by reactive ion etching (RIE) in an oxygen plasma. The substrate was then cleaned in a piranha solution, containing a mixture of sulfuric acid and hydrogen peroxide in a 3:1 ratio at 120°C, for 10 minutes. The wet piranha clean assures that absolutely no resist or organic residue from the Bosch process remains on the substrate. The SiO_2 layer may or may not be removed, depending on the desired final structure. Next, a 1 μm-thick layer of SiO_2 was grown by themal oxidation to serve as an isolation layer. SEM images of a typical sample at various stages of this process are shown in Figure 3.18. This concludes the fabrication of TWVs with a dielectric lining. A variety

of post-process steps can now be performed to achieve the desired type of TWI.

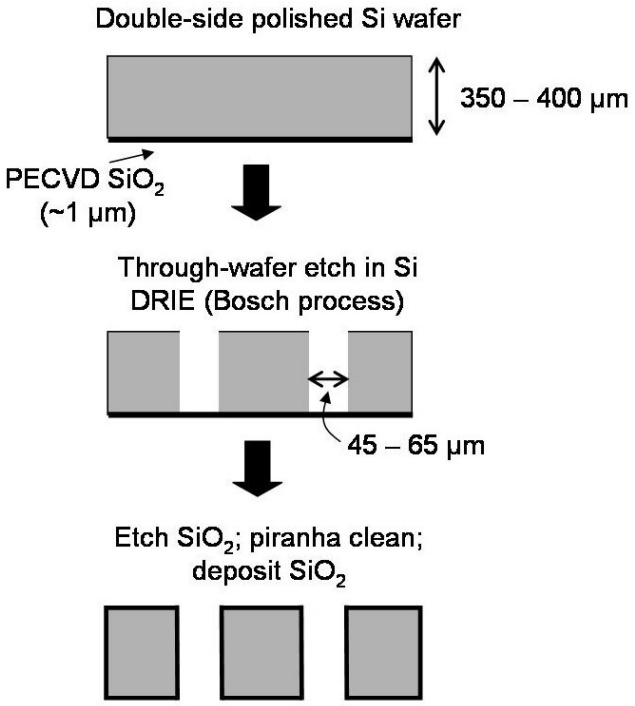
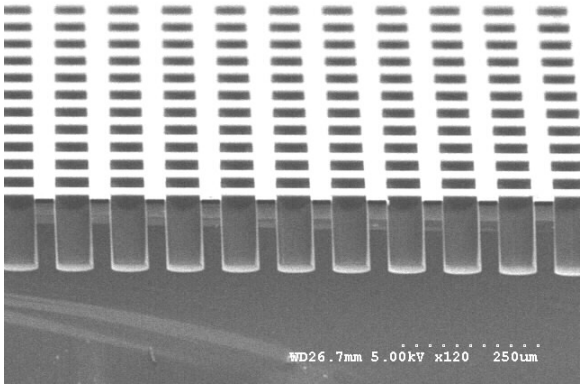
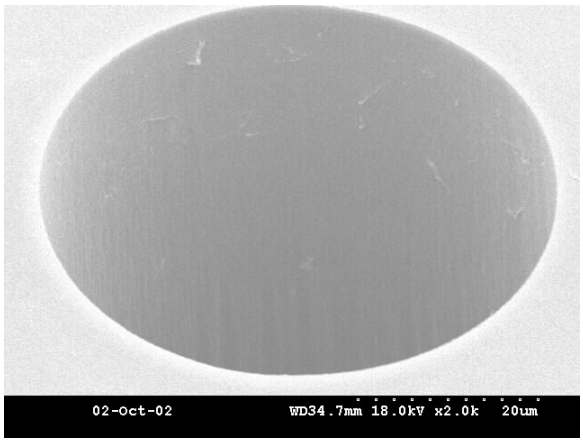


Figure 3.17: Process flow for fabrication of through-wafer vias in Si.



(a)



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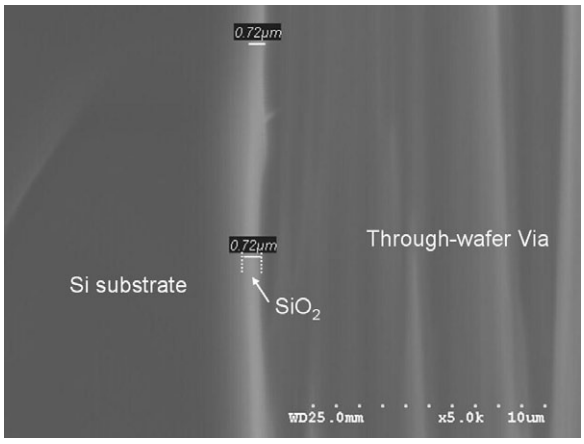


(c)

Figure 3.18: (a) Cross-section image of anisotropic vias in silicon, etched using the Bosch process. (b) Top view of a through-wafer via in silicon. (c) Cross-section of through-wafer via in Si after etching and thermal oxidation.

3.3.2 Conductive Layer Deposition

The isolated TWVs described in the previous section can be made conductive by a number of methods. The choice of process depends on the application for which the TWIs are to be used as well as on the dimensions of the interconnects. In general, the vias can either be lined or filled with a conductive material such as a metal or a doped semiconductor (Figure 3.2). The fabrication processes for these are described next.

3.3.2.1 Metal-clad TWIs

The process for lining the sidewalls of a TWV with a conductive material is shown in Figure 3.19. The sidewalls can be lined with a thin film of metal by sputter-deposition, as illustrated in Figure 3.20. Sputtering tools, fitted with DC magnetron sources, have been shown to be suitable for achieving deposition in high AR vias [55]. However, for TWVs in the probe substrate (45-65 μm wide $\times$ $\sim$400 μm tall, AR= 6-8), DC sputtering was unable to deposit metal all the way to the bottom of the vias. Figure 3.20 illustrates this deficiency in a 65 μm wide $\times$ 375 μm tall via. The same sputtering process yielded good sidewall coverage for a 100 μm wide X 500 μm tall via (Figure 3.21). It was thought that perhaps sputtering from one side of the substrate and then the other – effectively halving the aspect-ratio of the via – would improve coverage. However, this processing trick did not pan out. In the sample shown in Figure 3.22, Cu was first deposited from one side and then the other. For the 375 μm thick wafer, no metal was deposited on the sidewalls about halfway into the via. However, this approach was found to be successful for lower AR vias (Figure 3.21). Lowering the pressure increases the mean free path of the metal particles in the sputtering chamber. This was attempted to possibly induce metal deposition deep in the vias. However, this did not improve the process either. In fact, beyond a certain pressure, plasma ignition and sustenance became quite difficult.

Other methods of metal film deposition include e-beam evaporation, electroless plating, and metal organic CVD. Evaporation is best suited for directional deposition, and would not have been appropriate for deposition on the via sidewalls. Electroless deposition of

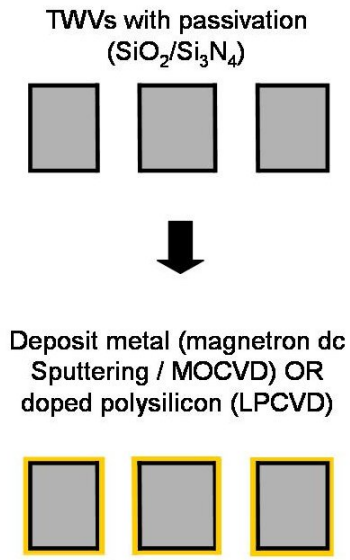


Figure 3.19: Process flow for lining TWVs with a conductive material.

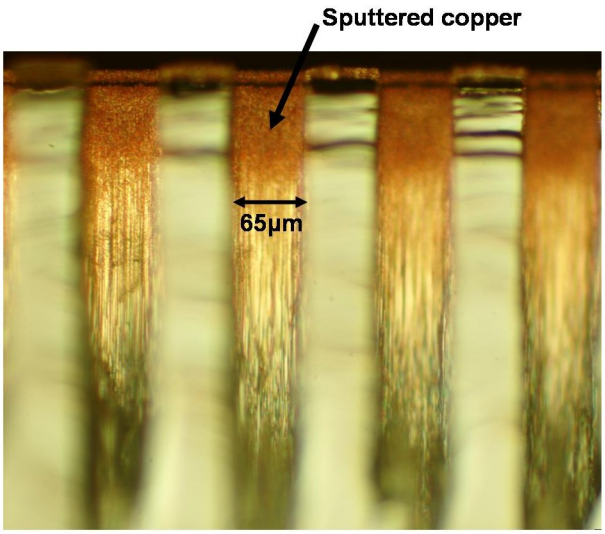


Figure 3.20: Array of 65 μm wide TWVs with sputtered Cu. The deposition was done from the front-side of the wafer.

copper and nickel was unsuccessful owing to the difficulty in activating a dielectric surface. MOCVD was not available within the MiRC cleanroom. There are some opportunities for investigating the use of bias sputtering, a method widely used for sputter cleaning, for improving metal deposition uniformity in high AR vias. Therefore, using the currently available equipment, depositing a continuous thin film of metal on the sidewalls of vias of

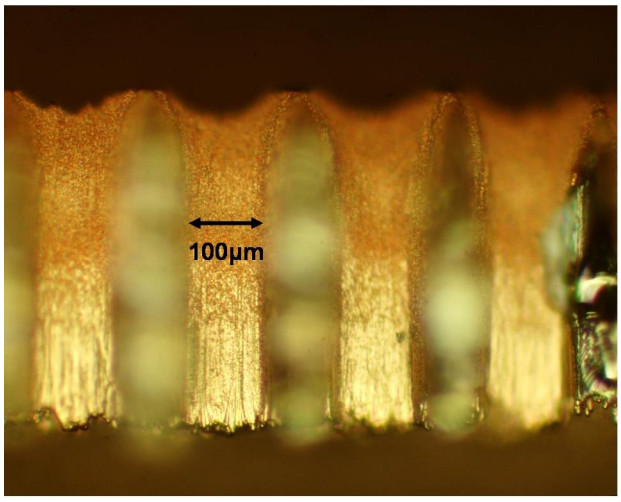


Figure 3.21: Array of 100 μm wide TWVs with sputtered Cu. The deposition was done from the front-side of the wafer.

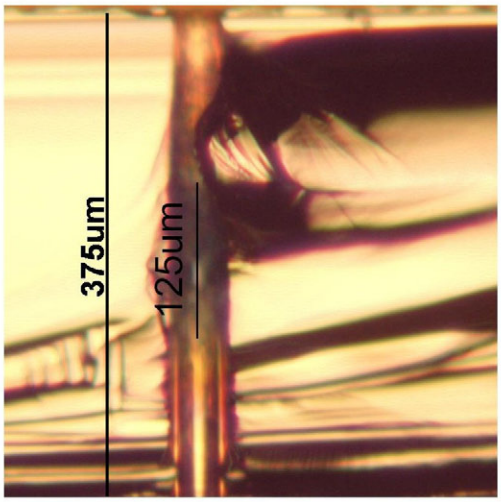


Figure 3.22: Microscope image of a TWV where Cu was first sputtered from the front-side and then the back-side. A stretch of 125 μm in the center of the via remained uncovered by metal.

AR 6-9 proved to be quite a challenging task.

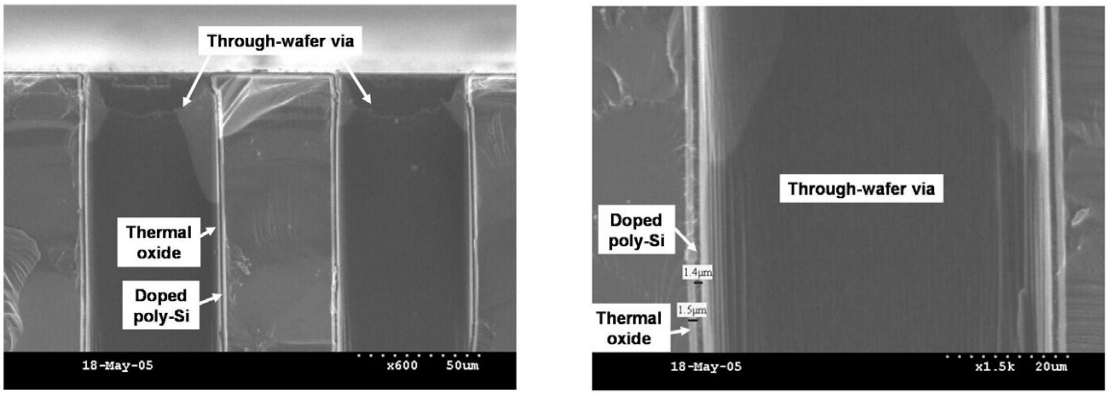
3.3.2.2 Polysilicon-clad TWIs

As evident from older-generation IC technologies, heavily doped polyilicon can be used as an interconnect material. Polysilicon deposition is commonly attained using an LPCVD process, which also means that a conformal and pure layer can be deposited in high AR

vias. It is a high-temperature (580-650°C), low-pressure (0.3-1 Torr) process, and uses silane (SiH_4) gas as the source of Si [52]. The net reaction is described by:

$$\mathsf{SiH_4(vapor) = Si(solid) + 2H_2(gas)} \tag{3.3}$$

The resistivity of LPCVD poly-Si can be reduced by doping (either n-type or p-type) using ion implantation, diffusion doping, or in-situ doping. The probe substrate TWVs were lined with LPCVD poly-Si and then diffusion-doped (n-type, using a phosphorus dopant source). Figure 3.23 shows SEM images of TWVs lined with doped poly-Si.



(a) (b)

Figure 3.23: SEM images of doped polysilicon lining on the sidewalls of a TWV with thermally grown oxide. The LPCVD poly-Si was diffusion doped (n-type) using phosphorus dopant source.

Using a process temperature of 588°C and a process pressure of 250 mTorr, the poly-Si deposition rate was calculated to be 3800 Å/hour. Resistivity of the poly-Si is dependent on the temperature as well as the duration of the doping process. Phosplus TP-470 (n-type) [56] and Boronplus GS-183 (p-type) [57] sources available for use in the MiRC cleanroom's diffusion furnaces were rated to achieve sheet resistivities of <1-7 Ω/square (950-1150°C) and 5-20 Ω/square (1000-1100°C), respectively.

3.3.2.3 Metal-filled TWIs

Electrical TWIs can also be realized by filling the TWVs with a conductive material. A major advantage of filled TWIs over lined ones is that post-TWI processing becomes much

easier – there is no worry of photoresist (or other liquidus materials) flowing into the vias. Copper is an excellent conductor (resistivity = 1.7x10^{-8} Ω-cm), and can be deposited into high AR features using electrodeposition. A process for filling TWVs with electroplated copper is described below.

A typical setup for electrodeposition is illustrated in Figure 3.24; it consists of a power supply, an anode (generally high-purity copper), an electrolyte (a mixture Cu salts), and a cathode (the sample to be plated). Copper is transferred to the sample by an oxidation-reduction process described by:

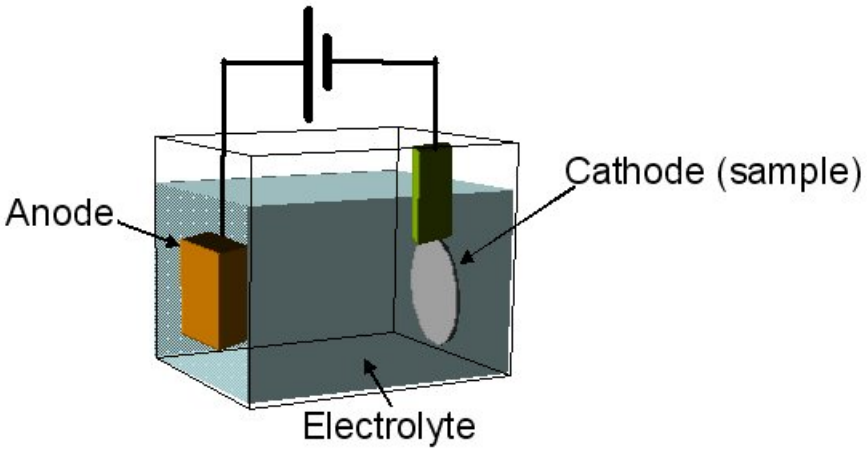


Figure 3.24: Schematic of a typical electroplating setup.

$$\mathsf{Cu} \rightarrow \mathsf{Cu}^{2+} + 2\mathsf{e}^{-}(\mathsf{oxidation} - \mathsf{anode}) \tag{3.4}$$

$$\mathsf{Cu}^{2+} + 2\mathsf{e}^{-} \rightarrow \mathsf{Cu}(\mathsf{reduction} - \mathsf{cathode}) \tag{3.5}$$

Processes for filling TWVs with electroplated copper have been previously discussed in [50, 58]. A similar bottom-up filling approach was adopted in this project. However, the large dimensions and high AR of the TWVs in the probe substrate complicate the electroplating process.

Ideally, if a continuous, conductive seed layer exists everywhere on the substrate, then copper could be plated using a DC current. However, as discussed earlier, it was quite

difficult to deposit such a layer on the sidewalls of a TWV.

A process similar to the one discussed in [50] was attempted. This is illustrated in Figure 3.25. First, a seed layer of Ti/Cu (300 Å/2000 Å) was e-beam evaporated on the back-side of the substrate with TWVs. Next, the sample was placed in a copper electroplating bath. The rate of electroplating is proportional to current density. In a high aspect-ratio via structure, charge tends to build-up at the corners of the via on the surface of the substrate. As a result, the rate of plating at these corners would be greater than that on the surface of the sample. As illustrated in Figure 3.25, electroplated metal would thus tend to *pinch-off* the via. While this is often undesirable during plating of on-chip interconnects, it is advantageous for TWV filling as it creates a continous seed layer on the back-side of the wafer. Additional plating would lead to bottom-up filling of the vias.

Unfortunately, the process did not proceed as described in [50]. The probe substrate had 50 μm-diameter TWVs as compared to vias with 2-10 μm diameter in [50]. As a result, at least 25 μm of copper had to be electroplated on the seed layer before the vias were pinched-off – this was a time-consuming process. Meanwhile, Cu^{2+} ions had access to the seed layer from the front-side of the wafer (through the TWV), Cu electroplated inside the via in an uncontrolled manner. This is shown in the SEM image in Figure 3.26.

To adjust for this, a two-step plating process was adopted. Initially, the side of the wafer away from the seed layer was sealed off with a non-conductive tape. The plating was started and continued until a layer of copper had pinched-off the via openings on the back-side (Figure 3.27). This side was then sealed with the non-conductive tape, and the tape from the front-side was removed. The sample was once again introduced into the plating bath, but now with the front-side facing the anode. Plating was finally stopped when overplated copper was observed everywhere over the vias. Slight overplating was desirable to assure that all vias on the substrate had been completely filled. The tape was removed, and the overplated copper on the front-side was removed by mechanical polishing.

Numerous sources in literature have suggested the use of either a pulse periodic or a

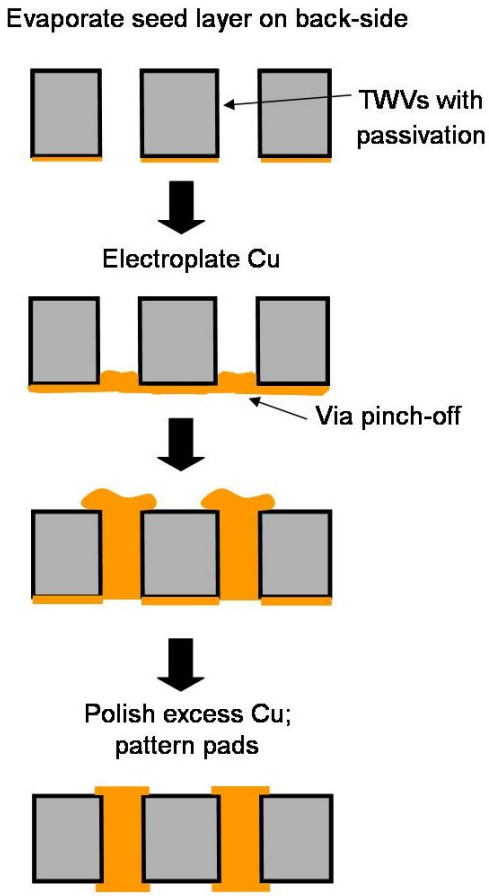


Figure 3.25: Process flow for metal-filled through-wafer interconnects. First, a seed layer of Ti/Cu (300 Å/2000 Å) is evaporated on the wafer back-side. Cu is electroplated using a high-Cu, low-acid content electrolyte. Finally, any excess copper is polished away.

pulse periodic reverse power supply to assist with high aspect-ratio via filling [50, 59]. The primary purpose of such power supplies is to reduce the pinch-off phenomenon at the via edges. The first step of the process described above actually requires pinch-off, and there is no question of pinch-off during the bottom-up filling as no seed layer exists on the front-side of the wafer. Therefore, a standard DC power supply was sufficient. A current density of 2 Amperes/dm^2 was used during the plating. While the process yielded high-quality filled electrical TWIs, the plating took a long time (6-10 hours). Of course, the time would be lesser for shorter and smaller vias.

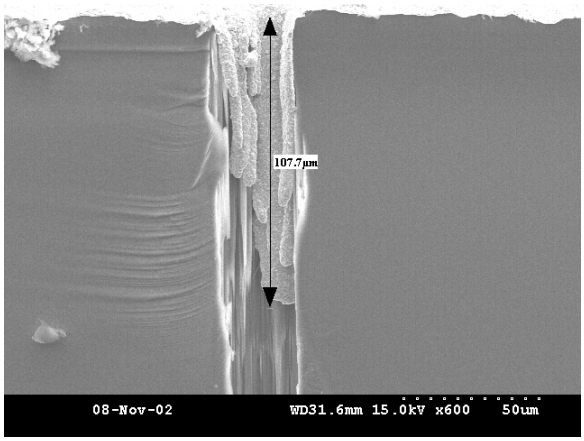


Figure 3.26: SEM image showing electroplating of copper in an uncontrolled manner when the electrolyte was able to access the seed layer from both sides of the TWV.

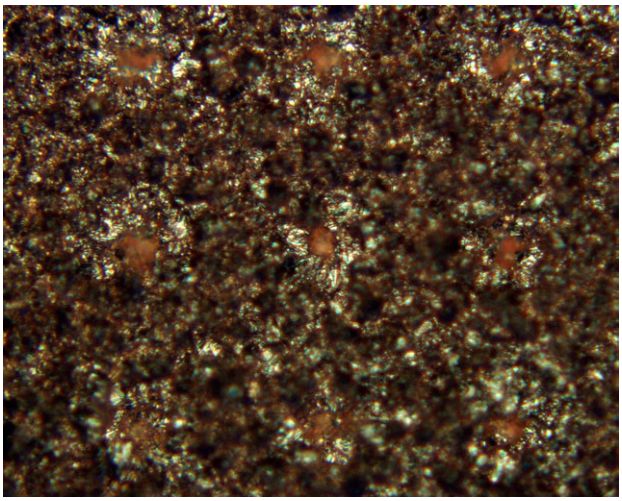
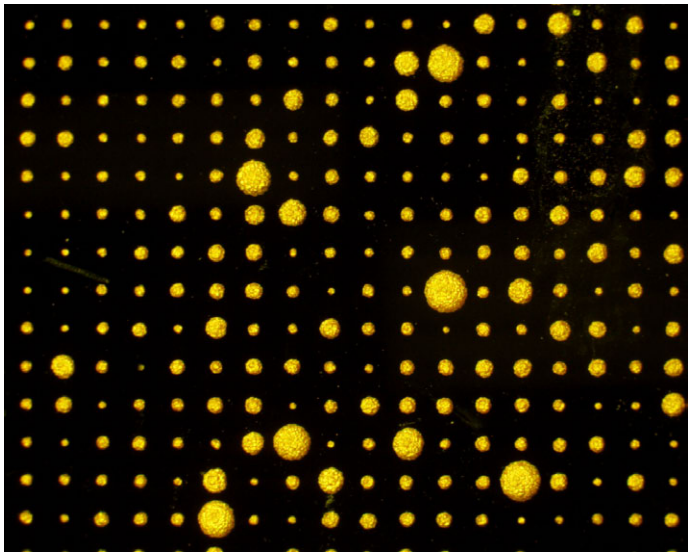


Figure 3.27: Image showing the back-side of the substrate after completion of the first step of the plating process. The vias were completely pinched-off and formed a continuous seed layer for bottom-up via plating.

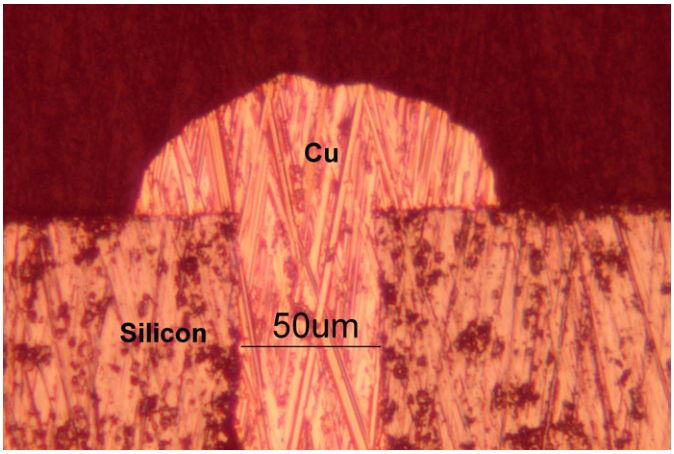
Figures 3.28 and 3.29 show microscope images of copper-filled TWIs successfully fabricated using the above process.

Some additional modifications were also made to improve the wafer-scale uniformity of the electroplating process.

1. A standard Cu plating electrolyte, consisting of copper sulfate ($CuSO_4$) and ∼1-2



(a)



(b)

Figure 3.28: Images of over-plated copper-filled TWVs. Over-plating was desired to assure that all vias on the substrate were completed filled.

Molar of sulfuric acid (H_2SO_4), has a conductivity of ~0.5 S/cm. Lowering the conductivity of the electrolyte is one way of improving the uniformity of electroplating across the wafer. This can be achieved by reducing the sulfuric acid content in the electrolyte. Doing so also increases the solubility of $CuSO_4$, and increases the transport rate of Cu^{2+} ions to the bottom of the TWVs [60], which is an added benefit for bottom-up filling. With this in mind, a high-Cu, low-acid content electrolyte was implemented for TWV filling. Table 3.4 lists the contents of a standard plating bath, and the high-Cu, low-acid bath.

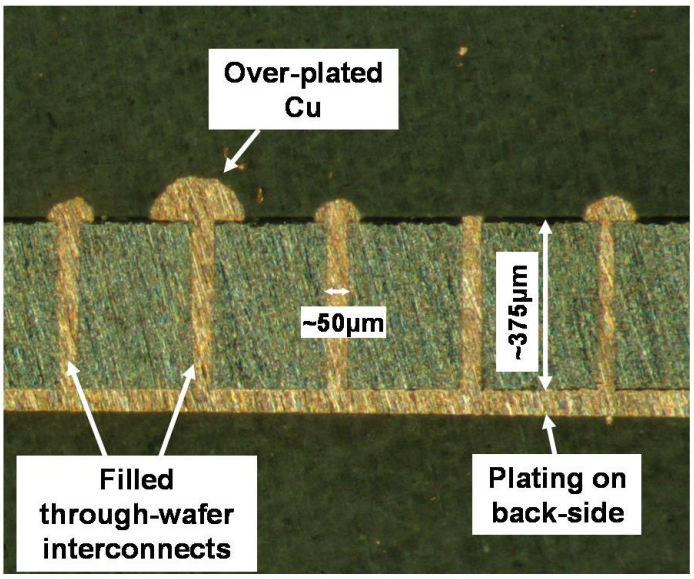


Figure 3.29: Cross-section image of through-wafer vias filled with electroplated copper. The over-plated copper was polished away mechanically.

Table 3.4: Chemical composition of typical and high copper plating electrolytes.

	Typical Plating Bath	High Copper-content Bath
Sulfuric Acid [mL/L]	210	5.5
Copper (II) Sulfate [g/L]	73	65.2
Copper (II) Chloride [g/L]	0.067	0.067

2. Owing to the large number of high aspect-ratio vias being plated in parallel, the physical design of the plating bath should be such as to maximize flow of fresh electrolyte from the anode to the cathode (sample). Figure 3.30 shows a photograph of the plating bath built for this process.

Following via filling, a thin film of metal (Ti/Cu/Ti, 300 Å/1 μm/300 Å) was sputter-deposited on both sides of the substrate and patterned using lithography and (wet) etching. Figure 3.31 shows the cross-section of a via with metal lines on both sides of the substrate. An interconnect daisy chain built in this manner was used for some electrical measurements and reliability testing.

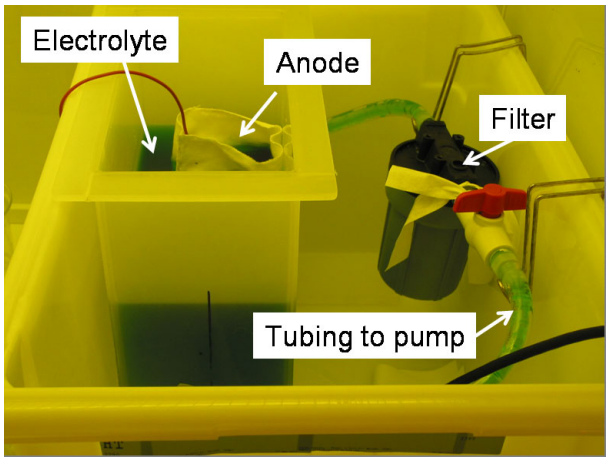
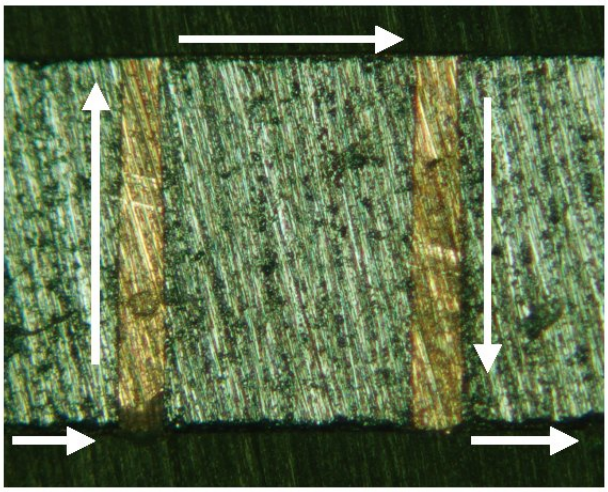
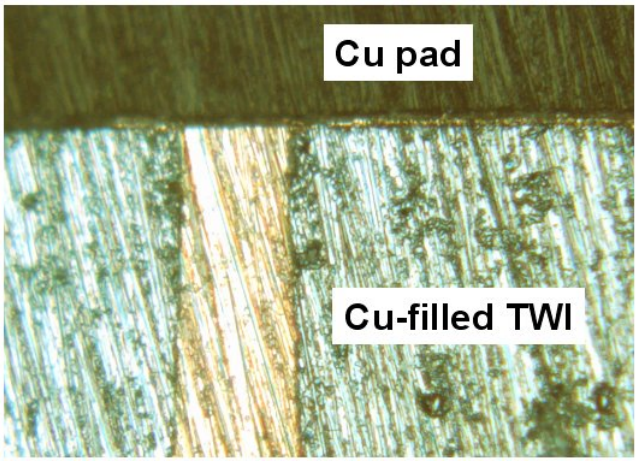


Figure 3.30: Photograph of copper electroplating bath.



(a)



(b)

Figure 3.31: (a) Cross-section image of TWI daisy chain link. (b) Cross-section image of metal pad connected to a Cu-filled TWI.

3.4 Through-Wafer Interconnect Characterization

3.4.1 Electrical Parasitics

In order to estimate the direct current (DC) parasitics of a TWI, it was assumed that the vertical interconnects had a cylindrical geometry and were completely filled with copper, as illustrated in Figure 3.2 (left image). It was also assumed that a dielectric layer exists between the conductive wire and the substrate.

- *Resistance:* The vertical TWI is essentially a cylindrical wire (Figure 3.32).

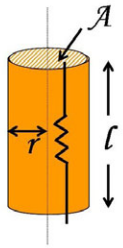


Figure 3.32: To estimate resistance, a metal filled TWI can be modeled as a simple wire of cylindrical (or other) cross-section.

Therefore, resistance (R), in [Ω], can be expressed as:

$$R = \rho \frac{l}{A} \tag{3.6}$$

where ρ= metal resistivity; l= interconnect length; and A= interconnect cross-section area.

Four-point DC resistance measurements were made on the sample with the interconnected TWIs (Figure 3.31) using a Keithley 2700 digital multimeter. While a 4-point resistance measurement is more accurate than a 2-point measurement (as it neglects the series resistance due to the probes and the cables in the measurement setup), it was challenging to fit four probe needles in the small area of the pads of the daisy chain. As a result, there was some error in the measurements due to the experimental setup. Figure 3.33 schematically shows the structures that were measured – for (a),

R_{avg}= 94.34 mΩ; for (b) R_{avg}= 144.46 mΩ; and for (c) R_{avg}= 158.64 mΩ. From these measurements of incremental segments of the daisy chain, the resistance of a single Cu-filled through-wafer interconnect was estimated to be around 18 mΩ.

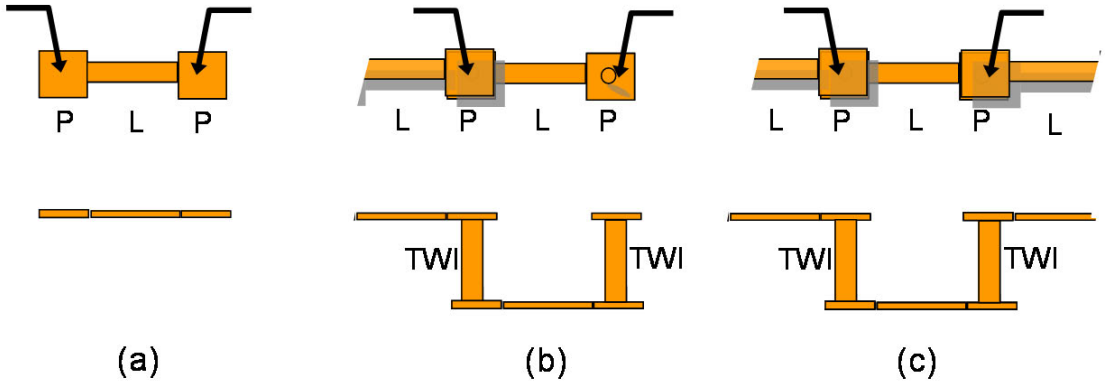


Figure 3.33: Schematic illustration of measured daisy chain segments. Here, P= pad, L= line, TWI= through-wafer interconnect. Values for the 3 illustrated cases were as follows: (a) 1 strap, R_{avg}= 94.34 mΩ; (b) 2 straps, R_{avg}= 144.46 mΩ; and (c) 3 straps, R_{avg}= 158.64 mΩ.

- *Capacitance:* To estimate capacitance (C), a TWI can be modeled as two concentric conductors (interconnect metal and substrate) separated by a dielectric layer – similar to a co-axial wire (Figure 3.34).

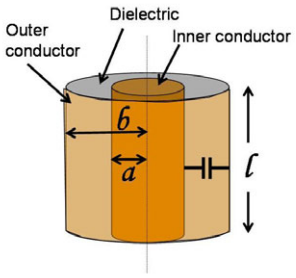


Figure 3.34: To estimate capacitance, a metal filled TWI can be modeled as a simple co-axial cable interconnect.

The capacitance [F] can then be calculated using the following equation:

$$C = \frac{2\pi\epsilon_o\epsilon_r l}{\ln\left(\frac{b}{a}\right)} \tag{3.7}$$

where ϵ_o= permittivity of free space= 8.85×10^{-12} [F/m]; ϵ= relative permittivity of dielectric; l= interconnect length; b= inner radius of outer conductor; and a= radius of inner conductor.

- *Inductance:* The inductance (L), in [H], of a cylindrical wire in free space can be used to obtain an estimate of the inductance of a TWI. The theoretical equation for calculating this is given by [50, 61]:

$$\mathsf{L} = \frac{\mu_o}{2\pi}\left[\mathsf{l}\cdot\ln\left(\frac{\mathsf{l}+\sqrt{\mathsf{l}^2+\mathsf{r}^2}}{\mathsf{r}}\right)+\mathsf{r}-\sqrt{\mathsf{l}^2+\mathsf{r}^2}\right] \tag{3.8}$$

where μ_o= permeability of free space= $4\pi \times 10^{-7}$ [H/m]; l= interconnect length; and r= interconnect cross-section radius.

Table 3.5 lists electrical parasitic values for typical copper-filled TWIs that have been successfully fabricated. In the nominal case (column 1), interconnect length (l)= 400 μm, metal radius (r)= 24 μm, and dielectric thickness= 1 μm. The second and third columns of this table contain values of R, C, and L for similar a TWI structure, but having a smaller width and length, respectively.

Table 3.5: Estimated R, C, L values for copper-filled TWIs of varying dimensions.

	I: l= 400 μm; r= 24 μm	II: l= 400 μm; r= 12 μm	III: l= 200 μm; r= 24 μm
R [mΩ]	3.76	15.03	1.87
C [pF]	2.45	1.25	1.22
L [nH]	0.21	0.26	0.07

3.4.2 Reliability

Reliability is defined as the probability that a component will be operational for the expected period of time [43]. Electronic components experience large amounts of current, fast switching speeds, and therefore, large variations in temperature. This is a cause of concern from the reliability perspective. As it is unreasonable to perform field-like operational

testing of components, accelerated reliability tests have been devised and the associated standards are documented by the JEDEC Solid State Technology Association [62].

A common accelarated test is temperature cycling of the component as described by JEDEC standard JESD22-A105. It was carried out in an air-to-air oven consisting of two chambers, one at 100°C and the other at 0°C. The TWI samples to be cycled were moved from one chamber to another. They remained in each chamber for 10 minutes. Electrical continuity of the daisy chains was measured intermittently (typically at the end of 100 cycle runs) as a test to determine failure.

A Si substrate having only interconnected daisy chains of Cu-filled TWIs (each 400 μm tall $\times$ 50 μm wide) was subjected to thermal cycling. After 400 cycles, about 82% of sampled daisy chains, each having 25 through-wafer interconnects, were electrically continuous.

3.5 Conclusion

Through-wafer interconnects are an efficient way of transferring signals from the probe-side to the redistribution substrate-side of the probe substrate. In this chapter, the design as well as TWI fabrication methods have been discussed. Using these processes, polysilicon-clad, metal-clad, and metal-filled electrical through wafer-interconnects of aspect-ratios ranging from 6 to 8, for a 400 μm wafer, were successfully fabricated.

CHAPTER IV

OPTICAL THROUGH-WAFER INTERCONNECTS

4.1 Introduction

In probe modules intended for testing chips with electrical and optical I/O interconnects, it may be advantageous to transmit optical signals between the DUT and the redistribution substrate. The design, fabrication, and characterization of novel free-space as well as guided-wave optical through-wafer interconnects are described in this chapter. In addition, process integration of guided-wave optical TWIs with mirror-terminated waveguides is also detailed.

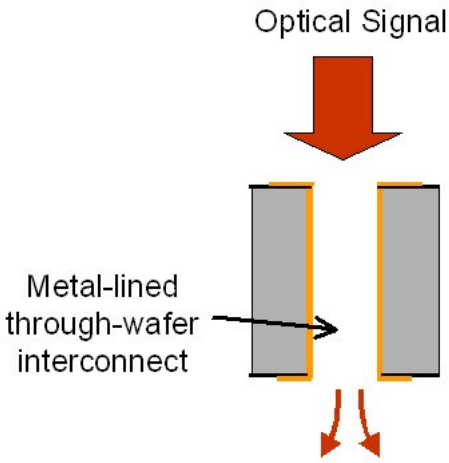
Like their electrical counterparts, optical TWIs would also be an essential element for building heterogeneous 3D microsystems.

4.2 Design

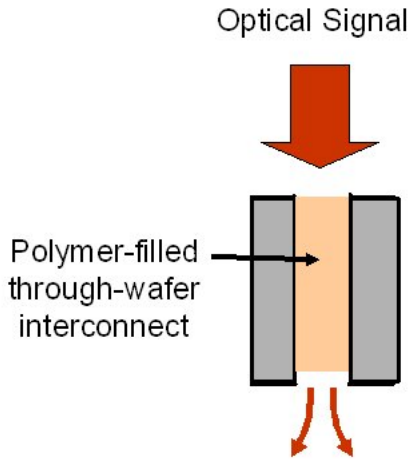
If the substrate material is transparent to the wavelength of light being used, no specific waveguiding structure is required for through-substrate optical transmission. While through-wafer optical interconnections using this phenomenon have been proposed [63–65], this approach limits the selection of substrate materials and useful optical wavelengths of operation. In this work, a waveguiding approach is adopted for optical signal transmission. The through-substrate vias used for electrical signals, and detailed in the previous chapter, are also used for optical signal distribution.

Figure 4.1 (a) shows a metal-lined optical through-substrate interconnect. The through-substrate via is used for exactly what it is – an opening in the substrate. Any light entering from one end will reach the other. If the incident optical signal has a narrow beam width, then, for a short via, the light may not interact with the sidewalls, and would be transported uninterrupted to the other side. This is because the beam may not spread too much over a short distance. On the other hand, if the incident beam is wide and/or the via is tall, then

metal on the sidewalls would behave like a mirror and confine the signal to remain within the via. Unfortunately, this is probably not the most efficient interconnection scheme, as some optical power will always "leak" out at the two ends of the via and would be be absorbed at it's sidewalls.



(a) Lined TWI



(b) Polymer-filled TWI

Figure 4.1: Use of through-substrate vias for optical transmission.

Alternatively, a through-substrate via can also be filled with an optically transparent polymer or dielectric to enable guided-wave optical transmission (Figure 4.1 (b)). Not only do filled vias make subsequent processing easier, but also allow for index-matched optical paths when these optical interconnects are integrated with other passive optical components such as waveguides and lenses. An optical beam incident on the polymer-filled

via will become wider as it traverses the length of the via. If it spreads far enough to interact with the via sidewalls and the index of refraction of the substrate ($n_{substrate}$) is greater than $n_{polymer}$, then the light will refract into the substrate. This can be avoided by depositing a liner on the via sidewalls before filling it with a polymer/dielectric such that $n_{liner} < n_{polymer}$. Now, if the beam does spread enough to interact with the sidewalls, total internal reflection at the polymer-liner interface will help contain and guide the light. Of course, a thin film of reflective material (such as a metal) deposited on the via sidewalls would also help achieve the same (with some of the light absorbed by the metal).

4.3 Fabrication

4.3.1 Lined Through-Wafer Interconnects

Vias lined with metal, polysilicon, or even a dielectric can be used for optical signal transmission. The fabrication of lined optical TWIs is the same as that for lined electrical TWIs, which was discussed in detail in Chapter III. Figures 4.2 and 4.3 show images of fabricated TWIs with a metal and a polysilicon liner, respectively.

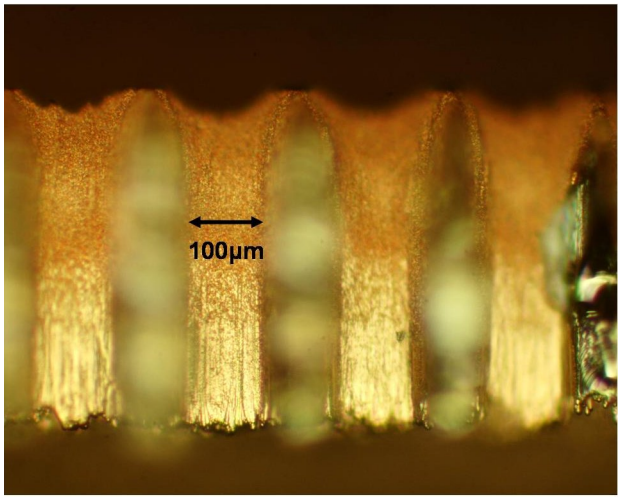


Figure 4.2: Metal-lined through-wafer interconnects for optical signal transmission. Via arrays with lower aspect-ratios can be easily lined with metal using DC sputtering. In the image, the vias are ~100 μm wide and ~400 μm tall

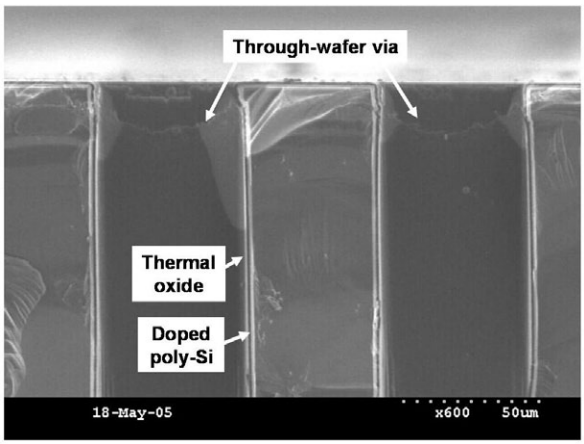


Figure 4.3: Poly-Si-lined through-wafer interconnects for optical signal transmission.

4.3.2 Polymer-filled Through-Wafer Interconnects

The process flow for constructing optical TWIs is not much different from electrical TWIs. It consists of via etching, via filling, and excess polymer removal by polishing (Figure 4.4). Via etching by the Bosch process was discussed in detail earlier and will not be repeated here. For polymer filling, the SiO_2 film that was used as an etch-stop during the Bosch process also doubles as the base of the via. Therefore, it was not etched away after via etching. It will eventually be desirable to have electrical and optical TWIs side-by-side on the same substrate. As a result, the substrate isolation step, achieved by the deposition of a dielectric layer on the via sidewalls, is also included in the fabrication of optical TWIs.

Numerous processes for filling TWVs with polymer have been devised. These are discussed briefly. Of these, the spin-on process was the first one attempted. As this process yielded the desired results, the other processes are left for future work.

4.3.2.1 Spin-on

Perhaps the simplest process for filling the vias with polymer is to spin it on the wafer and let it naturally flow into the vias, aided only by capillary action and gravitational force. The SiO_2 membrane on the back-side serves as the base and prevents the material from falling out. The process is shown in Figure 4.5.

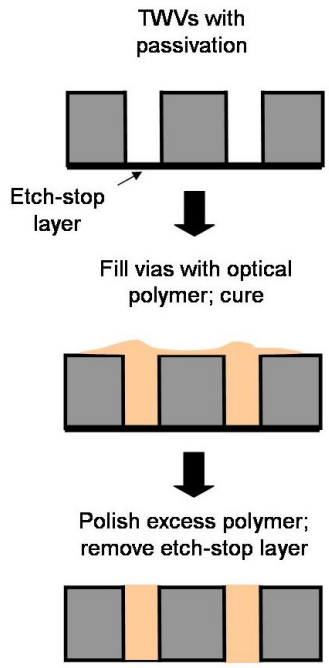


Figure 4.4: Process flow for filling TWVs with polymer. (a) Sample with TWVs, passivation, and etch-stop layer (not etched after DRIE). (b) Fill vias with a low-loss optical polymer. (c) Polish extra polymer, remove etch stop layer.

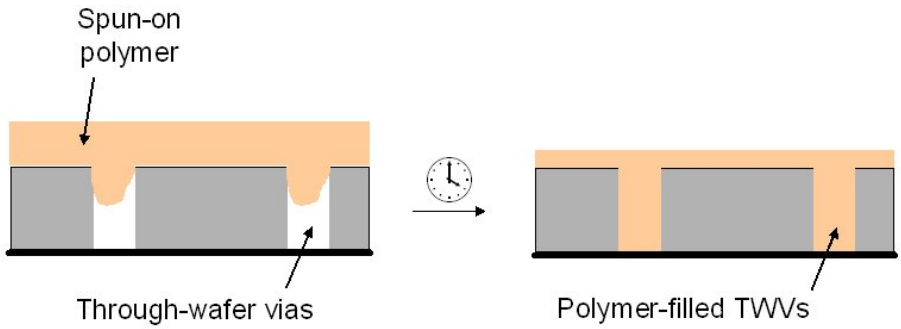


Figure 4.5: Process for filling TWVs by spinning-on polymer and allowing it flow into the vias.

4.3.2.2 Dispense-and-squeegee

This method can be likened to screen printing. The material is first dispensed on the surface of the wafer. A flat squeegee blade is then used to spread the material and force it into the vias. Getting the material to flow into the vias requires a large amount of force and has to

be done at relatively slow pace; while specialty equipment exists for doing this, one was not available for use. The process is illustrated in Figure 4.6.

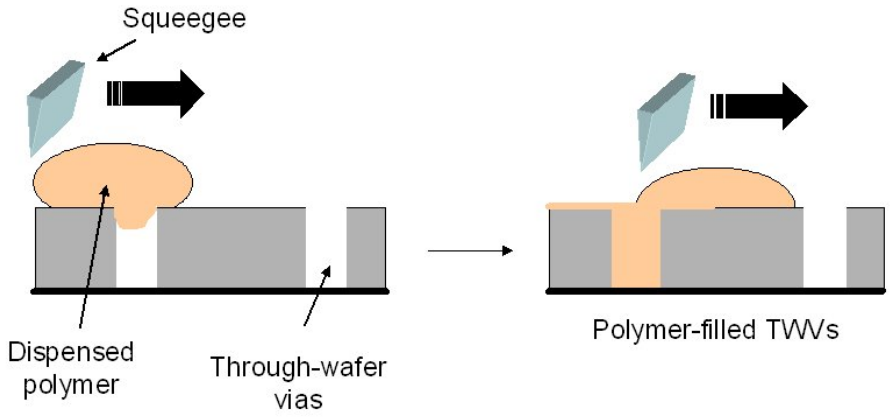


Figure 4.6: Process for filling TWVs by the dispense-and-squeegee method.

4.3.2.3 Polymer reflow

For most polymers, there exists a small temperature window above the glass transition temperature (T_g) but below the decomposition temperature, where it will begin to reflow. So, a unique method for filling the vias is to first fabricate an array of pillar-like structures, made of the polymer, on a separate substrate. These pillars would have the same footprint as a sample of through-wafer vias. The two substrates can then be aligned and attached, with the pillar-like features inserted into the vias. If the temperature of the stacked substrates is increased beyond T_g of the polymer, the polymer will reflow and conform to the geometry of the via. When the temperature is reduced below T_g, the polymer hardens and assumes it's new shape. The process is shown in Figure 4.7.

4.3.2.4 Polymer imprint

Another method for fabricating polymer-filled vias is to first spin-on a thick layer of the polymer material on one wafer, and let it remain in liquidus form. A separate wafer having TWVs but no oxide backing (etch-stop) layer is then pressed against the polymer film with a considerable amount of force. The pressure causes the polymer to flow into the vias. The

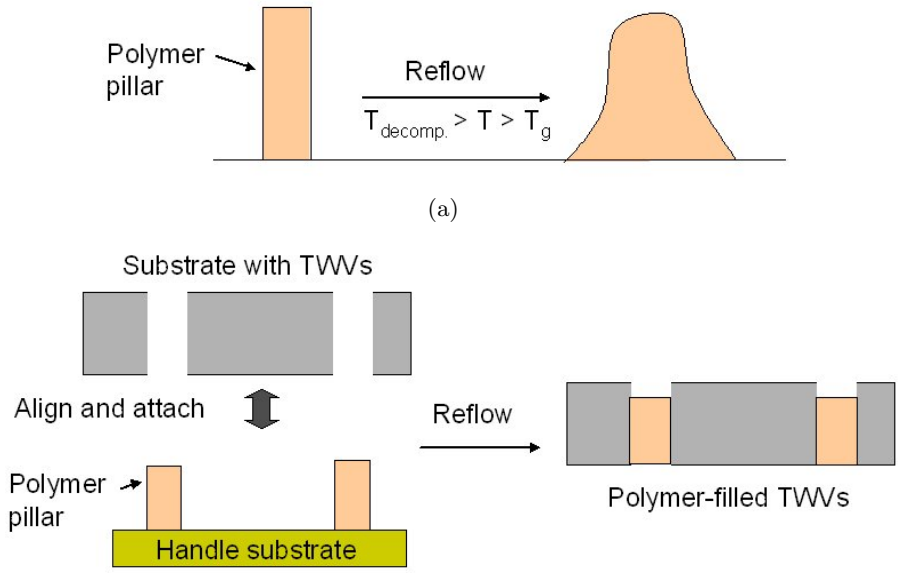


Figure 4.7: Process flow for filling TWVs by reflowing polymer.

stacked wafers can be soft-baked to drive out some of the solvent, and the polymer carrier wafer removed. This leaves behind a wafer with polymer-filled TWIs. The advantages of such a process include that it requires no alignment, and the carrier wafer can be re-used. However, an imprinting system, which can apply a high pressure on the stacked substrates to force the polymer through the vias, would be required. The process is shown in Figure 4.8

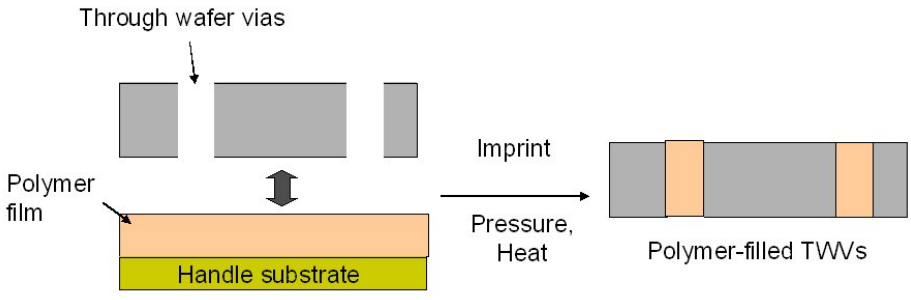


Figure 4.8: Process for filling TWVs by imprinting a thick film of polymer.

4.3.3 Material Selection and Process Summary

Initially, it was thought that a low-viscosity polymer would be best suited for via filling. Enestra optical encapsulant from Promerus, LLC was first used. Enestra is a two-component polymer. Filling experiments were performed using numerous spin speeds and curing conditions. However, the results were not as expected. After the material was spun-on, it was observed that only a small percentage of the vias were filled (Figure 4.9). The material did not seem to flow into the vias easily, but rather preferred to collect on the top surface of the sample around the vias. Discussions with Promerus, LLC revealed that perhaps Enestra had a tendency not to wick on Si or SiO_2. Even when the vias seemed to be filled (from a top view), cross-section images revealed that huge voids existed within.

Low-viscosity polymers, in general, have high solvent content. As a result, during the curing process, much of this solvent was driven out, which lead to shrinkage of the polymer inside the via (Figure 4.10). This is clearly an undesirable result.

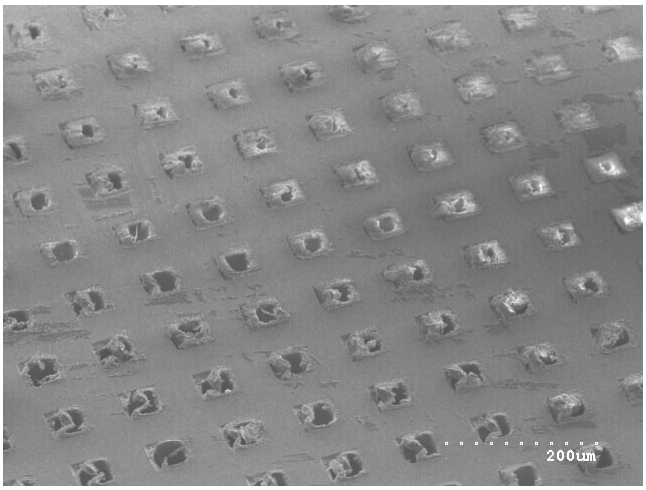


Figure 4.9: SEM image of a sample with TWVs filled with Enestra optical encapsulant. Only a few of the vias (top right) even appeared to be filled with this material.

Another material, Avatrel 2580-20, also from Promerus, LLC was then used. Avatrel is a polynorbornene polymer and is quite viscous; low solvent content reduces the possibility of material shrinkage. Once again, numerous spin and baking conditions were attempted to

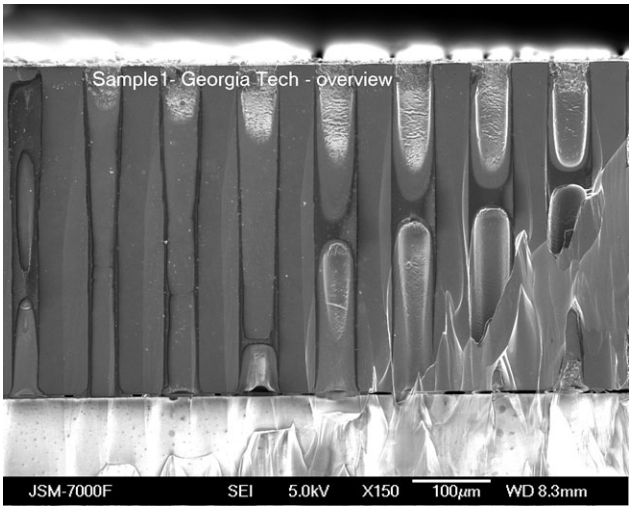


Figure 4.10: Cross-section of TWVs filled with Enestra optical encapsulant. Only some of the vias appeared completely filled. Also, the low-viscosity material shrank while curing, which lead to delamination of the polymer from the via sidewalls.

optimize the process. For the most part, Avatrel appeared to fill the vias uniformly (Figure 4.11). Unfortunately, cross-section images from initial processing iterations showed that the material was not reaching the bottom of the vias. This was overcome by allowing a settling period – additional time for the viscous fluid to reach the bottom – between material spin-on and soft-baking.

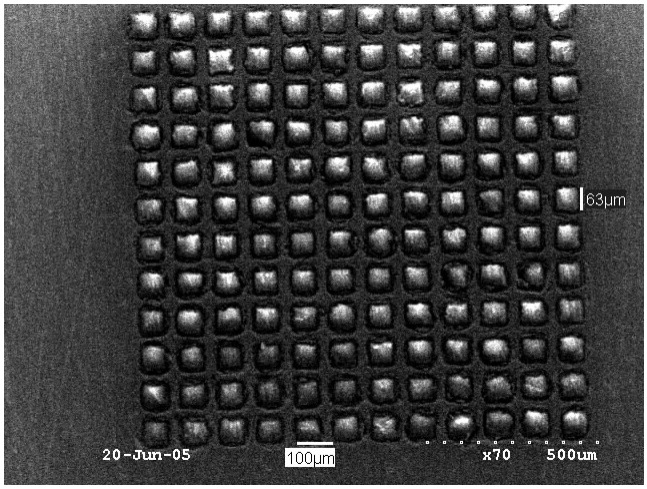


Figure 4.11: SEM image of an array of TWVs filled with Avatrel 2580-20 polymer.

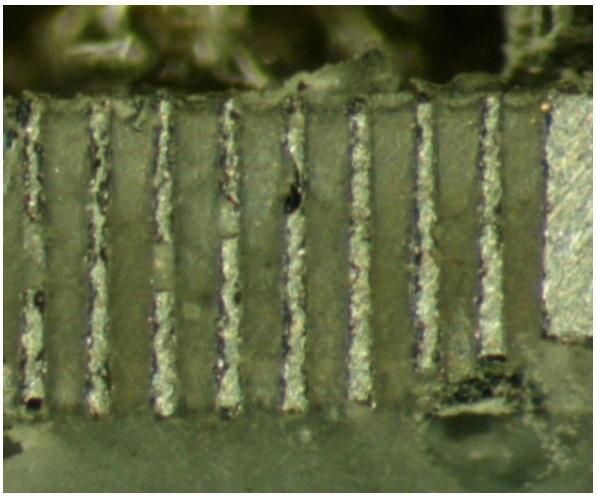
The final process can be summarized as follows:

Following TWV etching, any organic residue on the wafer was removed by a piranha clean. A 1 μm thick film of SiO_2 was then grown thermally to isolate the substrate. Following this, Avatrel 2580-20, an optically transparent polymer, was spun onto the wafer. A two-step spin recipe was used for this – 500 rpm for 10 seconds followed by 1500 rpm for 50 seconds. The wafer was then allowed to sit at room temperature for 10 minutes so that the polymer could flow into the vias. The polymer was soft-baked on a hot-plate; the temperature was ramped from room temperature to 100°C at a rate of 3°C/min, where it remained for 10 minutes. Next, the sample was cured in an oven at 180°C for 90 minutes. Finally, the excess polymer on the wafer was mechanically polished away. Cross-section images of Avatrel-filled through-wafer interconnects are shown in Figure 4.12.

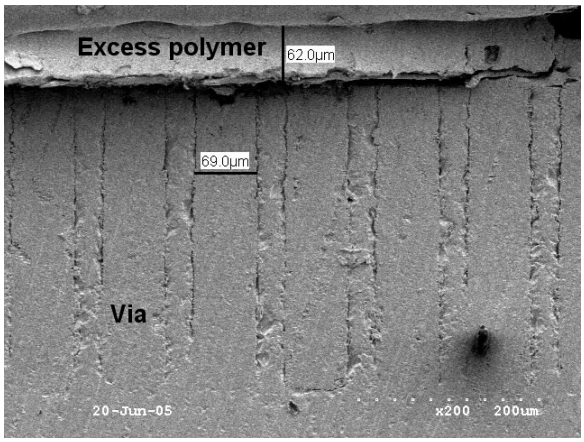
4.3.3.1 Surface smoothness

For optical transmission in a stand-alone TWI, it is desirable that the surface roughness of the interconnect be significantly smaller than the wavelength of light being transmitted. Polishing the excess material over the polymer-filled TWIs was quite challenging as it involved a soft polymer matrix within a hard Si substrate. To avoid *dishing* of the polymer, and to ensure a smooth finish, the polishing was carried out in stages, starting with coarse polishing pads and ending with fine liquid slurries (800 grit → 1200 grit → 4000 grit → 1 μm SiC slurry → 0.3 μm Silicon Carbide (SiC) slurry → 0.05 μm SiC slurry). SEM images of TWVs filled with Avatrel 2580-20 and having very smooth polished surfaces are shown in Figure 4.13. Surface roughness ∼0.5 μm was achieved (Figure 4.14).

Surface roughness may not be a huge problem if this polymer-filled TWI is process-integrated with other optical elements (such as a waveguides and lenses). Surface roughness of the polymer can be reduced by optimizing the polishing process and perhaps using finer slurries, if available. It can be seen from Figure 4.15 that the roughness from one via to another is quite small.



(a)



(b)

Figure 4.12: Cross-section of TWVs completely filled with Avatrel 2580-20 polymer.

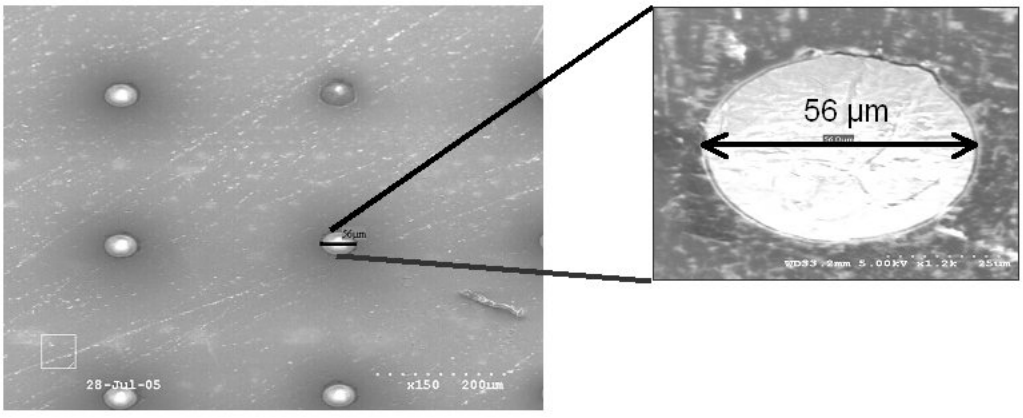
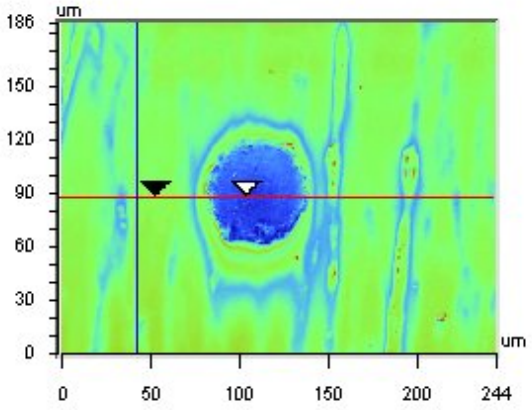


Figure 4.13: Top view of TWVs completely filled with Avatrel 2580-20. The excess polymer was mechanically polished away to yield smooth surfaces.



(a) Profilometer scan of a single TWI

(b) Surface profile of this via in the x-direction

Figure 4.14: Optical profilometer scan of a single TWV filled with Avatrel 2580-20 (a). The surface profile of this image in the x-direction is shown in (b) – a surface roughness of $\sim$0.5 μm was measured.

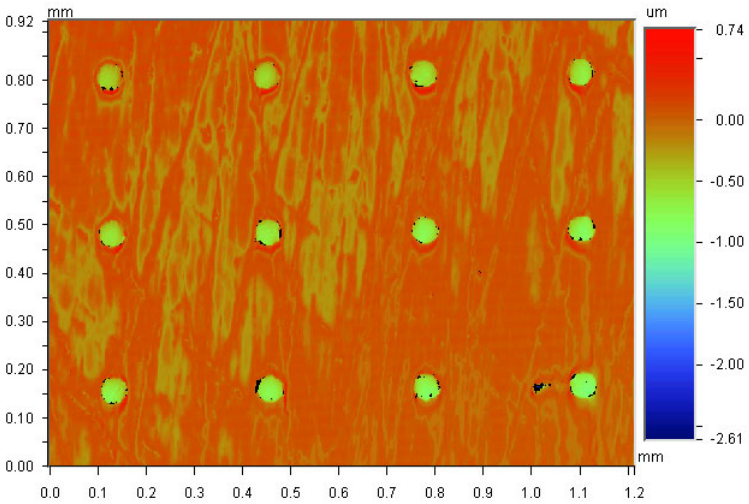


Figure 4.15: Optical profilometer scan showing a typical array of polished, Avatrel-filled TWIs. From this scan, it can be concluded that the polishing process was quite uniform from one via to another.

4.4 Characterization

This section describes the different experiments that were performed to measure (qualitatively and quantitatively) transmission of light in the fabricated free-space and guided-wave optical through-wafer interconnects.

The measurement of optical losses in Avatrel 2580-20 is discussed first. This is followed by sections describing transmission of light in metal-lined TWIs; measurement of optical power transmitted in SiO_2-lined TWIs; and measurement of optical power transmitted in polymer-filled TWIs.

4.4.1 Optical Loss Measurement in Avatrel 2580-20

As Avatrel 2580-20 seemed to be a good choice of material from the processing perspective, a loss coefficient measurement was performed using the image capture method [66]. First, a $\sim$30 μm-thick film of polymer was spun onto a piece of Si. The polymer was soft-baked and cured according to the process described earlier. A single-mode optical fiber, pig-tailed on one end to a laser diode of wavelength 635 nm, was aligned to this slab waveguide. To avoid reflections at the optical fiber-waveguide interface, it was critical to ensure that the end-faces of the fiber and the waveguide were as close to vertical as possible.

Losses in a waveguide can be attributed to absorption, radiation, and scattering. The loss can be expressed in terms of propagation distance using the equation:

$$y = Ae^{-Bx} \tag{4.1}$$

where A= normalization constant, B= loss coefficient, and x= position along the waveguide. The loss coefficient, B, can then be estimated by fitting the scattering loss in the waveguide to this exponential equation.

The scaterring data was obtained by exciting the waveguide with the optical fiber input and taking a bitmap image of the top view (hence, scattered light) of the sample. The image was then fed into MATLAB, and converted into intensity data. The total intensity at any

point (in the direction of propagation) in the slab waveguide was obtained by summing the intensity of all points (across the width of the region of the slab waveguide that was imaged) at that location.

Figure 4.16 shows an image of the light scattered in the 30 μm-thick slab waveguide made of Avatrel 2580-20. The normalized intensity data, obtained from this image, is plotted against the propagation distance in Figure 4.17. A robust bilinear least squares fit was performed on this dataset to obtain values for the normalization constant, and the loss coefficient. Using a nonlinear least squares fit reduces the contribution of point-type defects in the determination of the loss coefficient. The loss coefficient in cm^{-1} can be converted to dB/cm by using the conversion

$$\alpha[\mathrm{dB/cm}] = 10\log_{10}(e)\alpha[\mathrm{cm}^{-1}] \tag{4.2}$$

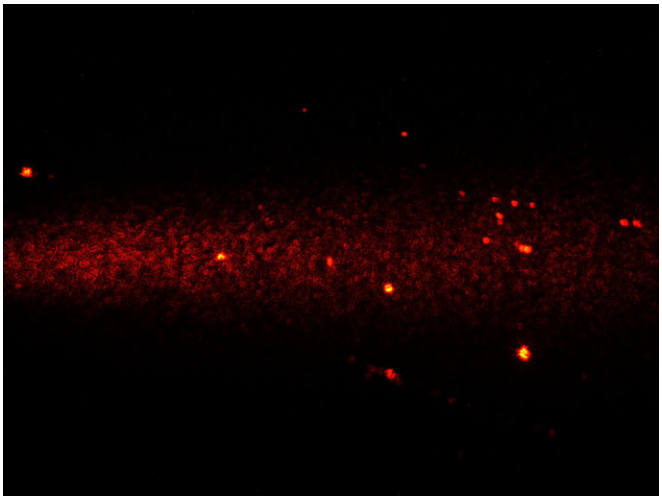


Figure 4.16: Image of scattered light in a 30 μm thick slab waveguide of Avatrel 2580-20 polymer.

Using this curve-fitting method, the loss coefficient of the Avatrel 2580-20 slab waveguide was calculated to be 3.2 dB/cm. Generally, the loss coefficient in a slab waveguide is higher than that of the material loss coefficient since additional loss mechanisms, such as surface roughness and radiation, contribute to slab waveguide loss [67].

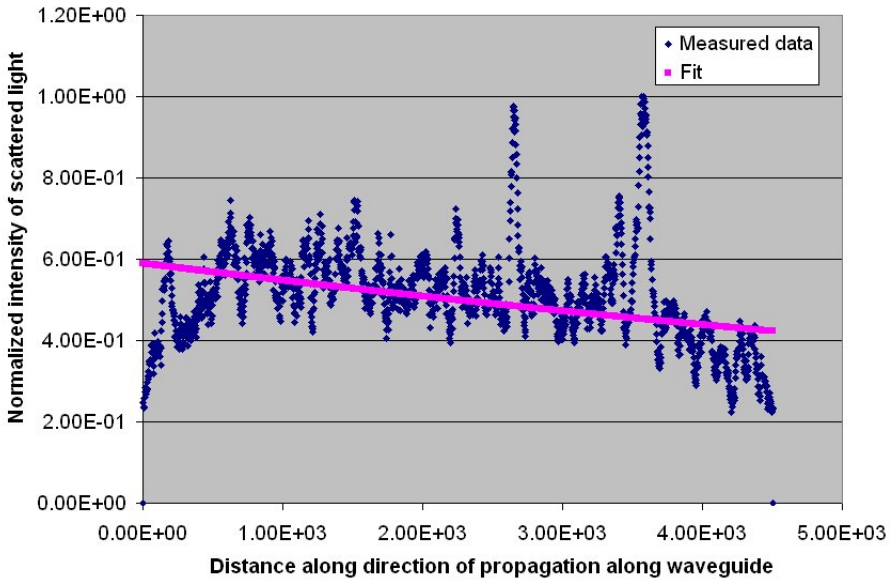
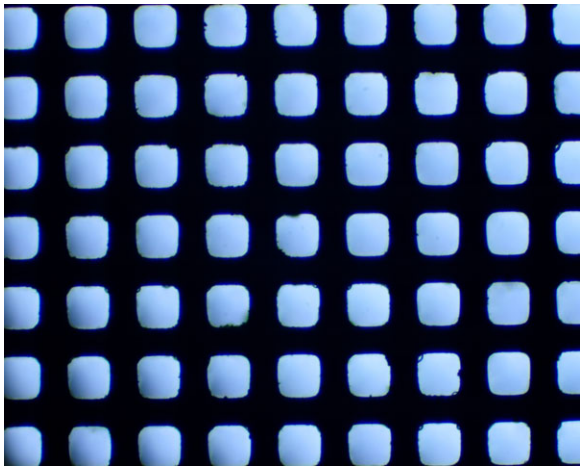


Figure 4.17: Robust bilinear least squares fit to normalized scattered intensity in an Avatrel 2580-20 slab waveguide. The loss coefficient of Avatrel 2580-20 was calculated to be approximately 3.2 dB/cm.

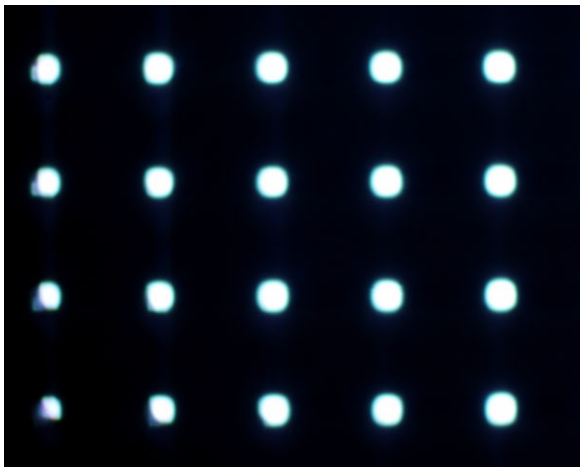
Using this loss coefficient number (α) in Equation 4.1, the power loss in a 400 μm-tall TWI filled with Avatrel 2580-20 polymer was estimated to be about 3% (assuming that light does not interact with the sidewalls of the via).

4.4.2 Optical Transmission in Metal-Lined TWIs

It is plain to understand that when a wafer containing through-wafer vias is illuminated on one side, the light will only transmit to the other side through these openings. Of course, this assumes that the substrate is not transparent to the wavelength of the incident light source. Figure 4.18 shows images of samples with through-wafer vias that were illuminated from the back-side using a broadband (white-light) source. These images demonstrate what is expected intuitively. Optical transmission in a single through-wafer via is discussed next.



(a) Via size= 64 μm $\times$64 μm; Pitch= 100 μm .



(b) Via diameter= 50 μm; Pitch= 325 μm .

Figure 4.18: Microscope images of Si substrates with through-wafer vias. The samples were illuminated from the back-side using a white-light source.

Figure 4.19 shows a schematic of the setup constructed to demonstrate optical transmission in a single TWI. A photograph of the actual testbed is shown in Figure 4.20. One end of the sample was illuminated with a Helium-Neon (He-Ne) laser, of free-space wavelength 632.8 nm; the output, from the other end of the TWIs, was imaged with a charge-coupled device (CCD) camera. The sample being tested consisted of 50 μm diameter vias, at a 325 μm pitch, in a thinned-down ($\sim$200 μm thick) wafer. The He-Ne laser used in this setup emits a beam that is $\sim$640 μm wide, and thus, illuminated multiple TWVs on the test sample. To image only the light exiting a single via, a masking tape, covering all but the one via under examination, was put down on the sample.

At the onset, the camera was focused on the surface of the (back-side) substrate surface, and this was set as the reference (0 μm) point. Images of the light exiting the via at this point and at increasing distances from the substrate surface are shown in Figure 4.21. The alternating dark and light rings represent regions of constructive and destructive modal interference. This is a simple demonstration of optical transmission through the via. Expectedly, the beam diverges with increasing distance from the substrate surface.

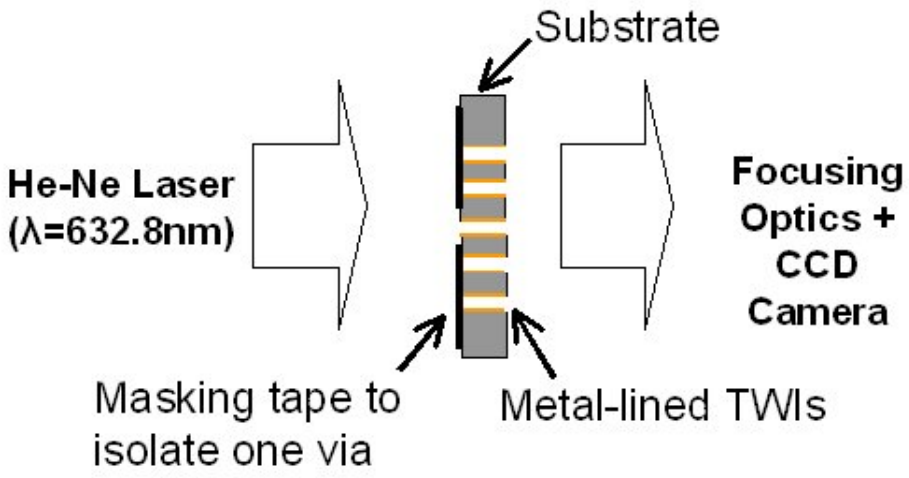


Figure 4.19: Setup for demonstration of optical transmission in lined through-wafer interconnects.

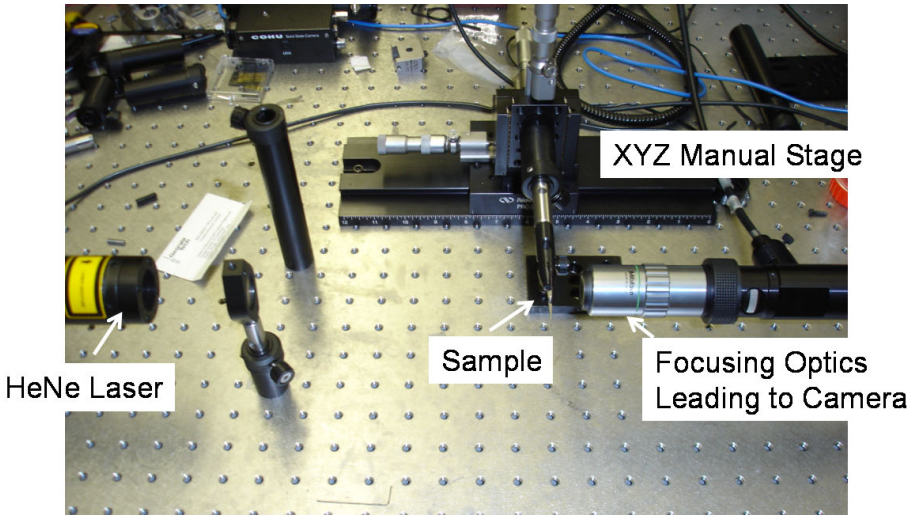
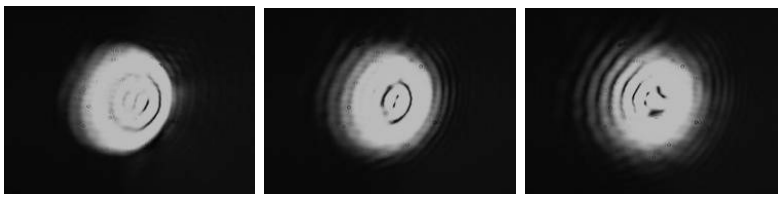
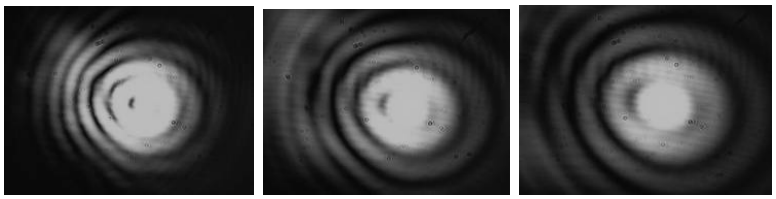


Figure 4.20: Setup for demonstration of optical transmission in through-wafer interconnects.



(a) 0 μm (b) 100 μm (c) 200 μm



(d) 400 μm (e) 600 μm (f) 800 μm

Figure 4.21: Interference patterns, created by optical transmission in through-wafer interconnects, imaged in increasing distances from the substrate.

4.4.3 Optical Power Transmitted in SiO_2-lined TWVs

To add to the aforementioned proof-of-concept demonstrations, a more quantitative measurement was also performed. In this case, the goal was to measure the optical power being transmitted in through-wafer vias in a Si substrate. In addition, measurements were made to ascertain the uniformity of optical power transmitted across an array of such through-wafer vias.

4.4.3.1 Experimental configuration

Figure 4.22 shows a schematic of the measurement setup to measure optical power. A single-mode optical fiber (core diameter= 6 μm) pig-tailed to a laser diode (λ= 635 nm) is positioned directly above the interconnect structure to be characterized. A photodetector placed underneath this sample-under-test is used to measure the transmitted optical power. Photographs of the actual setup are shown in Figures 4.23 and 4.24. This setup was also re-used to make optical power measurements for other interconnect and probe substrate structures, which will be discussed later.

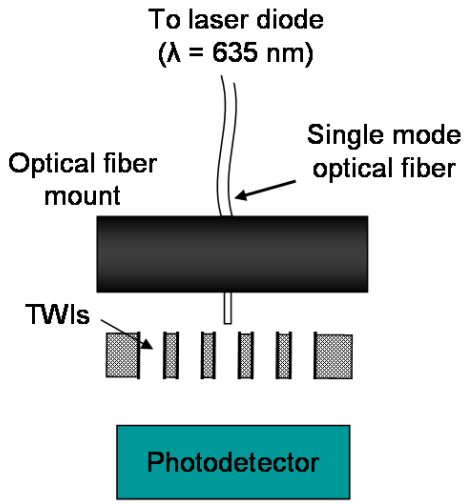


Figure 4.22: Setup for measuring optical power transmitted in a through-wafer interconnect. The optical source is a single-mode optical fiber pig-tailed to a 635 nm laser diode. Owing to the small 6 μm core of the optical fiber, it was possible to accurately position it over individual through-wafer vias.

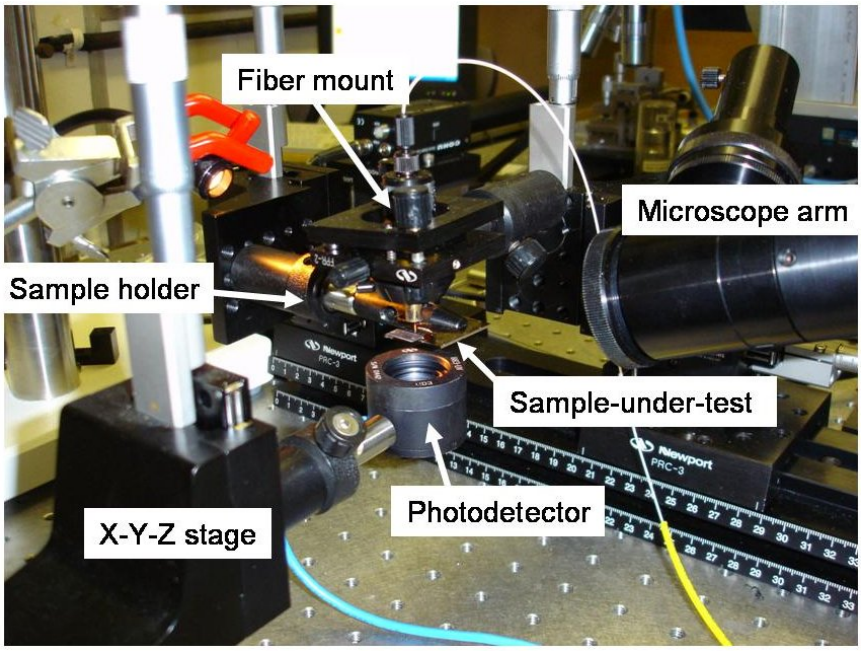


Figure 4.23: Photograph of the experimental configuration for measuring optical power transmitted in vertical interconnect structures.

4.4.3.2 Measurements

The sample-under-test consisted of TWVs in a Si substrate. The vias were ~400 μm-tall $\times$ 50 μm-wide and were fabricated at a 325 μm pitch. The vias were lined with 1 μm of thermally grown SiO_2. The optical power transmitted in a 6×6 array of vias is plotted in Figure 4.25. The power is normalized to the maximum power transmitted in a via in this dataset (a total of 36 points) and is plotted along the y-axis. The x-axis corresponds to the columns in this array. The range of values for each column corresponds to the range of power transmitted in each row of that column. The high, low, and mean values of the normalized optical power are indicated on this chart. For these 36 vias, the mean normalized optical power was 0.913, and the standard deviation was 0.068. From this, it is evident that there is minimal via-to-via variation with respect to the transmitted optical power.

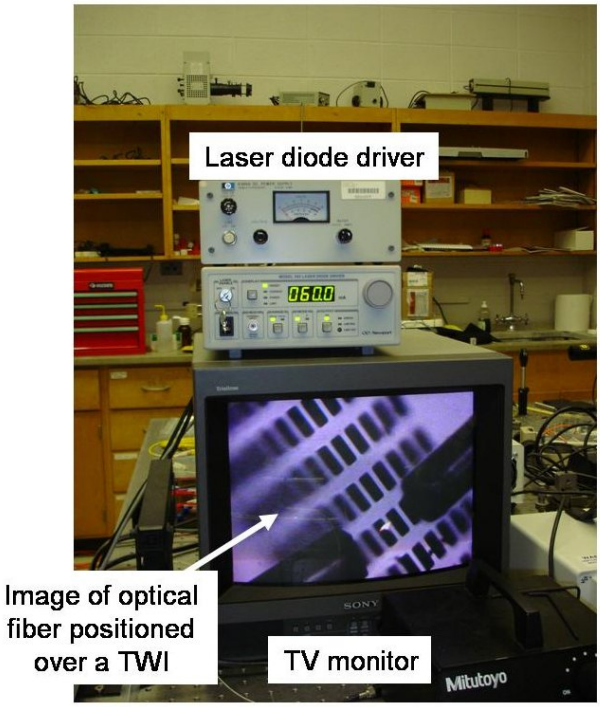


Figure 4.24: Photograph of the laser diode driver and the television monitor used in the optical power measurement setup. The monitor shows the output from a CCD camera, which was used to assist with accurate positioning of the optical fiber directly over a single interconnect structure.

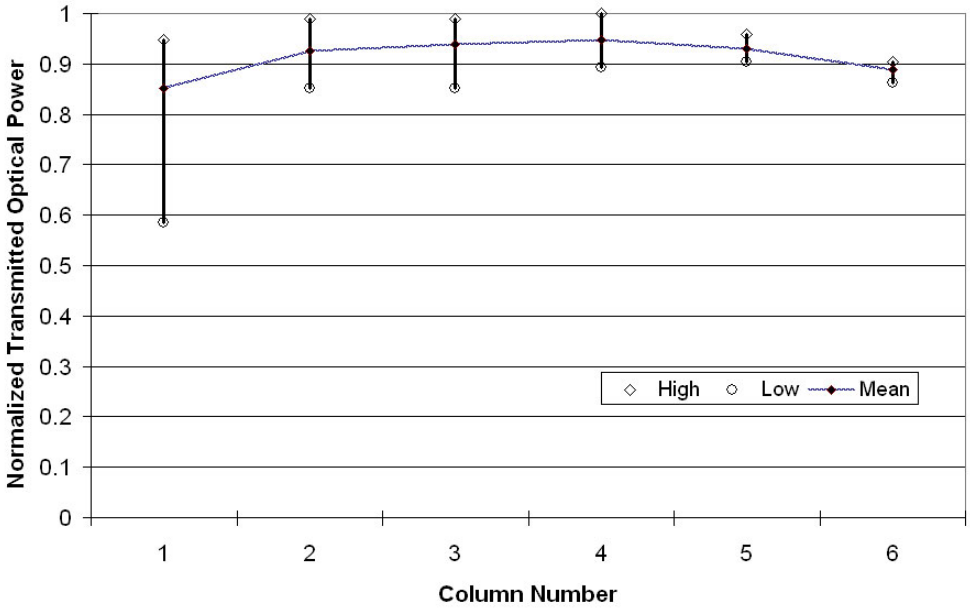


Figure 4.25: Plot of normalized optical power transmitted in a 6×6 array of SiO_2-lined through-wafer vias. The range of values for each column number (x-axis) corresponds to the range of normalized transmitted power measured for six rows in that column.

4.4.4 Optical Transmission in Polymer-Filled TWIs

The qualitative and quantitative measurement of optical transmission in polymer-filled TWIs in detailed in this section.

4.4.4.1 Proof-of-concept demonstration

Transmission through a polymer-filled TWI was demonstrated using the same method as has been described for the metal-lined TWIs. A schematic of this experiment is shown in Figure 4.26. The actual experimental configuration was the same as shown in Figure 4.20. The output from a via as captured by the CCD camera is shown in Figure 4.27.

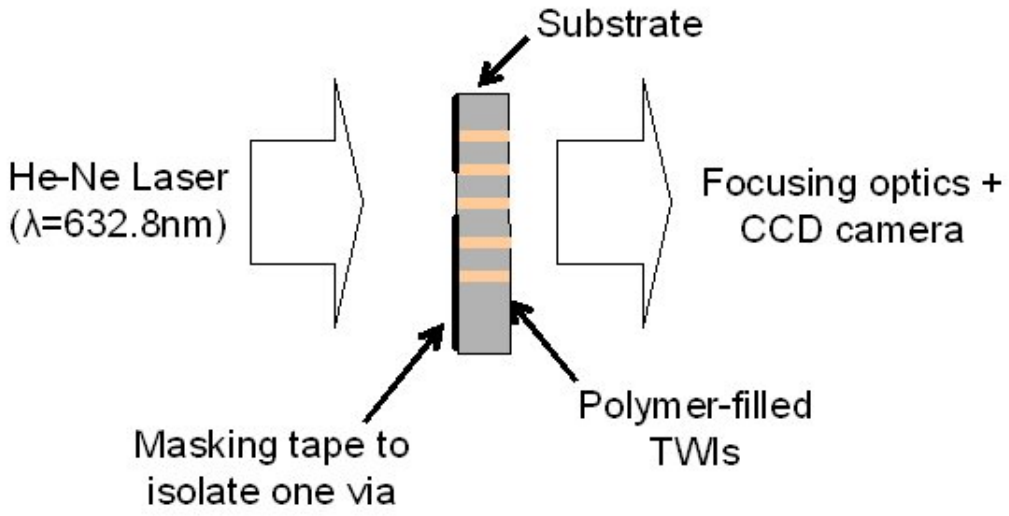


Figure 4.26: Schematic of setup for demonstration of optical transmission in Avatrel-filled through-wafer interconnects.

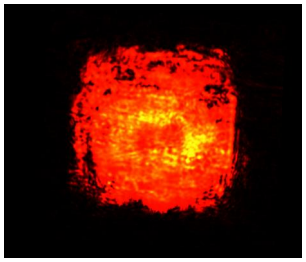


Figure 4.27: Optical output from a TWI filled with Avatrel 2580-20 polymer. The 64×64 μm ^{2} square via was excited with a He-Ne laser of free-space wavelength 632.8 nm.

4.4.4.2 Transmitted optical power

A schematic of the experimental setup for measuring optical power transmitted in polymer-filled TWIs is shown in Figure 4.28. The measurement was made for a 5×5 array of TWIs. The circular vias were 50 μm in diameter, ~400 μm tall, and were fabricated at a 325 μm pitch. 1 μm of SiO_2 was deposited on the via sidewalls before filling it with Avatrel.

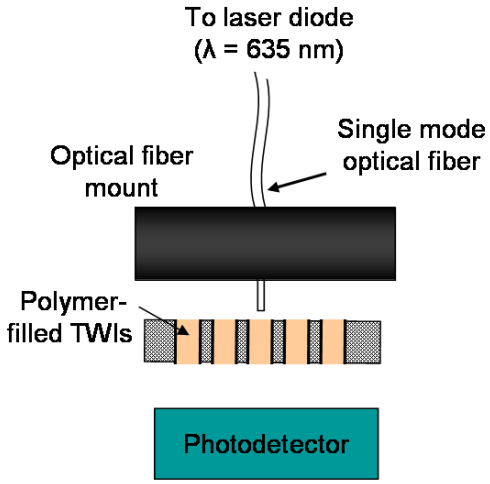


Figure 4.28: Setup for measuring transmitted optical power in a through-wafer interconnects filled with Avatrel 2580-20. The optical source is a single-mode optical fiber pig-tailed to a 635 nm laser diode. Owing to the small 6 μm core of the optical fiber, it was possible to accurately position it over individual through-wafer interconnects.

In order to provide a proper reference, the power measurement was carried out in two steps. First, the optical power transmitted in individual vias, with the SiO_2 lining but without any Avatrel, was measured. Then, these vias were filled with Avatrel 2580-20 following the process described earlier, and the optical power measurement was repeated on the same set of vias measured before the polymer-filling process.

The optical power transmitted in a 5×5 array of polymer-filled TWIs is summarized in the chart shown in Figure 4.29. The x-axis corresponds to the columns of this array. The transmitted optical power is plotted along the y-axis. The power transmitted in each interconnect was normalized to the power transmitted in that interconnect before filling

with Avatrel. The range of values for each column corresponds to the range of power transmitted in the interconnects in that column. The high, low, and mean values of the normalized transmitted optical power are indicated on this chart. In summary, the plotted data represents the percentage of the optical power in an unfilled via that is transmitted when the via is filled with Avatrel 2580-20.

On average, about 13% of the power was transmitted when the vias were filled with polymer. This is much lower than expected (only ∼3% loss was expected). It was concluded that since the surface roughness of the polymer, approximately 500 nm, was on the order of the wavelength of the incident light (λ= 635 nm), a large amount of power was potentially reflected, and thus lost, at the optical fiber-polymer via interface during the measurement. Thus, there is a need for a better polishing process. In addition, a large detector was used in the test setup. Some of the light may have been lost due to scattering from the surface of this large device. Fine-tuning the experimental configuration may provide a more accurate measurement of the transmitted power.

At the same time, when this polymer-filled via is combined with other optical elements to create index-matched optical pathways, such as a waveguide (as will be described later in this chapter), the roughness at the the via-waveguide interface may be a non-issue.

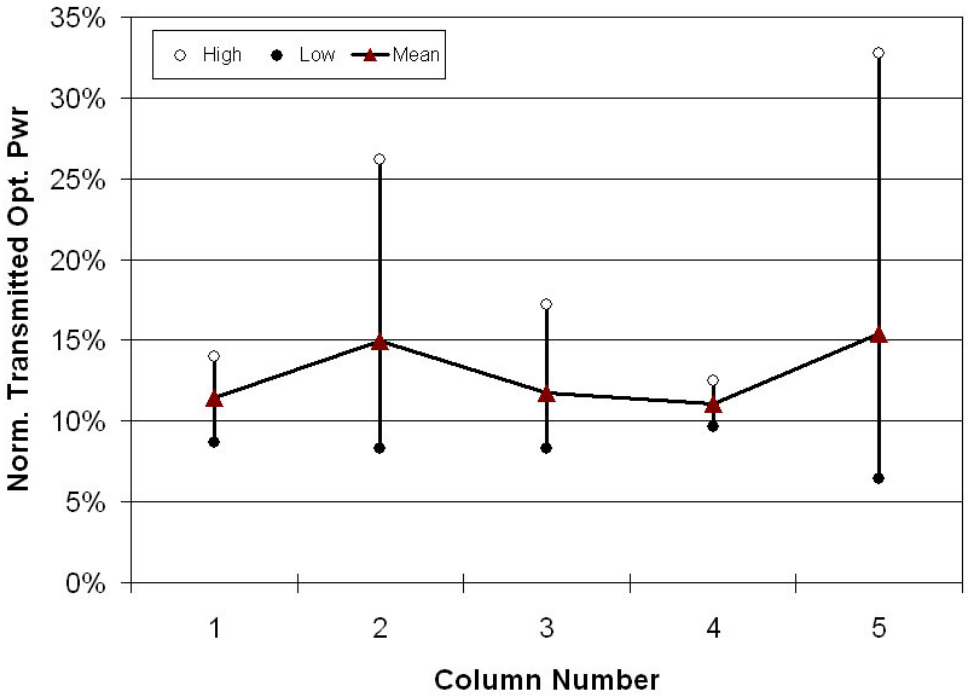


Figure 4.29: Plot of optical power transmitted in a 5×5 array of polymer-filled TWIs as a percentage of the optical power transmitted in those vias before filling with polymer. The graph provides a measure of the amount of power lost owing to filling the vias with Avatrel 2580-20.

4.5 Integration of Polymer-Filled TWIs with Mirror-Terminated Waveguides

While the polymer-filled TWIs have an advantage over their free-space counterparts with respect to subsequent processing, their true benefit becomes apparent when they are combined with other optical elements. This section describes the integration of polymer-filled TWIs with mirror-terminated waveguides. An experiment to demonstrate coupling of light from one side of the substrate to another using this waveguide-mirror-TWI structure is also detailed.

4.5.1 Design

Figure 4.30 illustrates a guided-wave TWI directly above a mirror-terminated waveguide. This combination enables bending an optical signal from the surface-parallel direction (in the waveguide) to the surface-normal direction (in the filled TWI), or vice versa. The filled TWI permits index-matched optical transmission; thus reducing any unwanted back-reflections at the waveguide-via interface.

Lenses, diffractive elements, or optoelectronic devices could also be placed directly above the TWI for index-matched transmission.

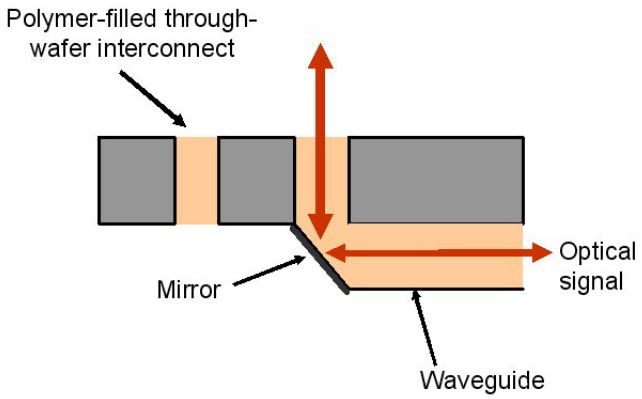


Figure 4.30: Schematic of a polymer-filled TWI coupled to a mirror-terminated waveguide.

4.5.2 Fabrication

Polymer-filled through-wafer interconnects have been process-integrated with 54.7° mirror-terminated waveguides. The process flow is shown in Figure 4.31. While 45° mirrors are considered to be the optimal choice for bending an optical signal from in-plane to the surface-normal direction, the ease of fabrication of 54.7° mirrors made it a good selection for a proof-of-concept demonstration. Also, a 3D guided-wave optical interconnect such as Figure 4.30 is probably more alignment tolerant to mirror angle [68].

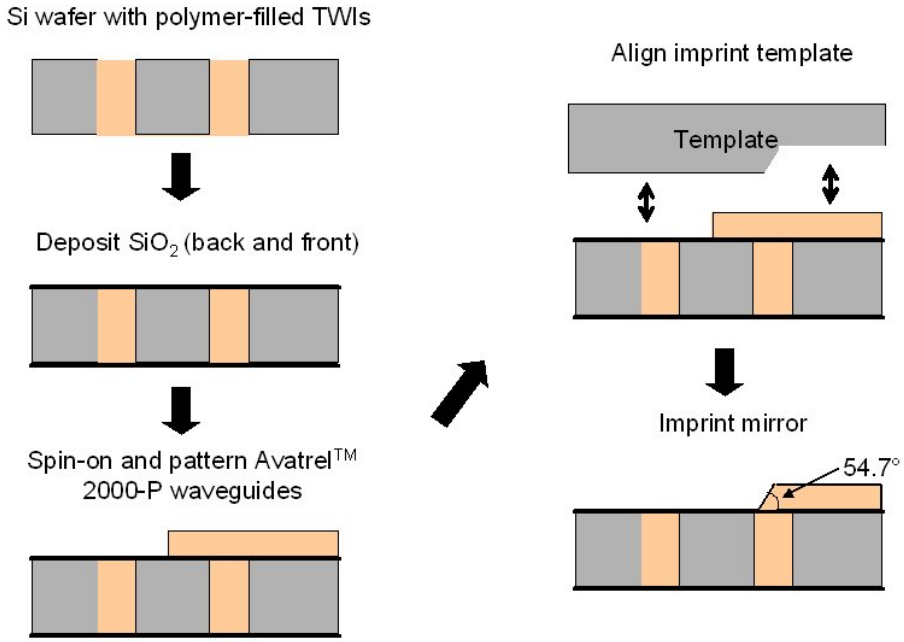


Figure 4.31: Process flow for fabricating mirror-terminated waveguides on a wafer with polymer-filled TWIs.

After fabrication of Avatrel-filled TWIs, a layer of SiO_2 was deposited onto both sides of the wafer. This was done in order to increase adhesion of the waveguides to the substrate. Next, a 10 μm-thick film of Avatrel 2000P, a photodefinable polynorbornene polymer from Promerus, LLC was spun onto the wafer. UV photolithography was used to pattern the Avatrel 2000P into 50 μm wide waveguides. After exposure, the sample was spray developed using Bioact developer, also from Promerus, LLC. The developing step is particularly important; it is crucial to ensure that developer is spread evenly and vigorously across the

entire area of the wafer. Figure 4.32 shows an SEM image of waveguides fabricated over the filled TWIs. The waveguides were deliberately aligned to extend beyond the TWIs to which they are to be coupled. Next, 54.7° mirrors are imprinted onto the waveguides using a nanoimprint lithography tool. The imprinting process also removes the piece of the waveguides extending beyond the vias. This concludes the fabrication of mirror-terminated waveguides coupled to polymer-filled TWIs.

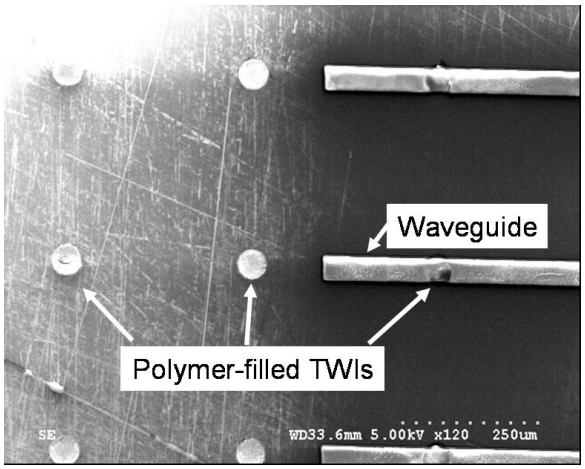


Figure 4.32: SEM image of Avatrel waveguides fabricated over polymer-filled TWIs. The waveguides were purposely patterned to extend beyond the vias by a little bit.

4.5.2.1 Template fabrication and mirror imprinting

Figure 4.33 [69] shows a schematic of nanoimprinting of a thermoplastic resist. The desired pattern is first created on a master template. This pattern is then embossed onto target wafers having a layer of thermoplastic or UV-curable material under high temperature and pressure conditions. Prior to imprinting, the template is coated with a thin film which aids in easy demolding from the imprinted wafer.

The template used for imprinting the waveguides was built on a Si wafer. It consisted of two regions, one higher than another. The drop at the interface between the two regions has an angle of 54.7°. The fabrication of this template began with a bare silicon wafer of (100) orientation. After depositing at least 5000 Å of PECVD SiO_2 on the wafer, a 5 μm layer of NR9-8000 negative resist, from Futurrex, was spun onto the front-side of the

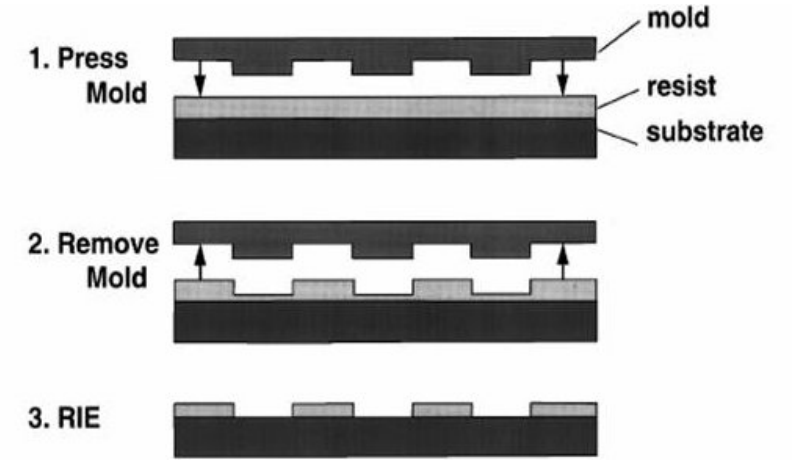


Figure 4.33: Typical process for imprinting a pattern on a thermoplastic material.

wafer, and was patterned using UV lithography. The lithography step was used to mask off half of the wafer; following this, the exposed SiO_2 was etched away using BOE, and the photoresist was removed with Acetone. The next step is to etch the now exposed Si to reveal an angled sidewall between the two regions. The wafer was placed in a beaker containing TMAH at 87-90°C. TMAH etches the (111) crystal plane of Si much faster than the (100) plane, leaving behind trenches with 54.7° sidewalls. The etch rate of Si in TMAH is very temperature-dependent; between 87-90°C, the etch rate was observed to be approximately 0.67 μm/minute. Figure 4.34 shows a schematic of the controlled temperature bath that was used for this process. The exposed Si was etched to a depth of $\sim$15 μm . Finally, a thin film of Ti/Au (300 Å/2000 Å) was sputter-deposited selectively on the trench sidewall (which was to be the mirror facet) and the lower half of the template. Selective metal deposition was achieved by simply placing a glass slide over the regions where no metal was desired.

At the time of this fabrication, the alignment module in the MiRC's nanoimprint lithography tool, from Obducat, was not functional. Therefore, the imprinting was carried out in two steps. First, a flip-chip bonder, from RD Automation, was used to align the template to the sample with waveguides and TWIs. The M10A bonder, shown in Figure 4.35, uses a split-optic vision system and image recognition software to align two substrates. It has

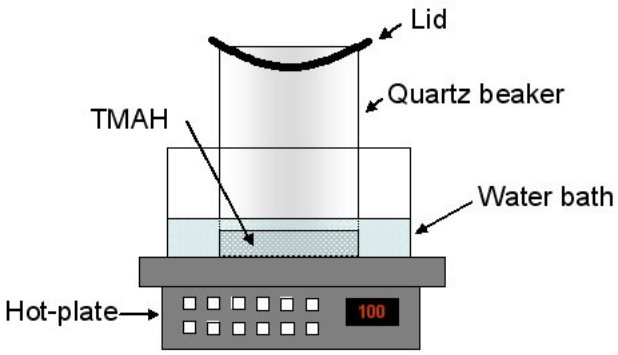


Figure 4.34: Schematic of setup for etching Si in tetramethyl ammonium hydroxide. The water bath was necessary to assure uniform temperature across the TMAH solution.

an alignment accuracy of ± 2 μm. The attachment is typically achieved using a multi-step bonding process wherein the pressure, temperature, and time for each step is user-defined. Figure 4.36 shows an image of the template substrate aligned to the waveguides immediately prior to the attachement in the bonder. For waveguide imprinting, a two-step process was found to work the best – 100 g @ 100°C for 15 s followed by 4,500 g @ 100°C for 90 s. The attached samples were then carefully transported to the nanoimprint tool, where the imprinting process was completed. Imprinting was achieved by applying a pneumatic force (and temperature when needed) on the template that was positioned over the target substrate. In this case, a pressure of 20 bar, and a temperature of 110°C were applied for 30 s.

Ideally, the mirror would reflect any incoming light into the waveguide or the via by total internal reflection (TIR). However, to improve the chances of a successful demonstration in this first-time integration endeavor, the Au-coated template was left attached to the sample with the TWIs and the waveguides. Figure 4.37 shows an SEM image of an imprinted blanket film of Avatrel 2000P. The 54.7° angled sidewall is clearly visible. A sample having mirror-terminated waveguides built using this process is shown in Figure 4.38 – here, the template was demolded to obtain an image.

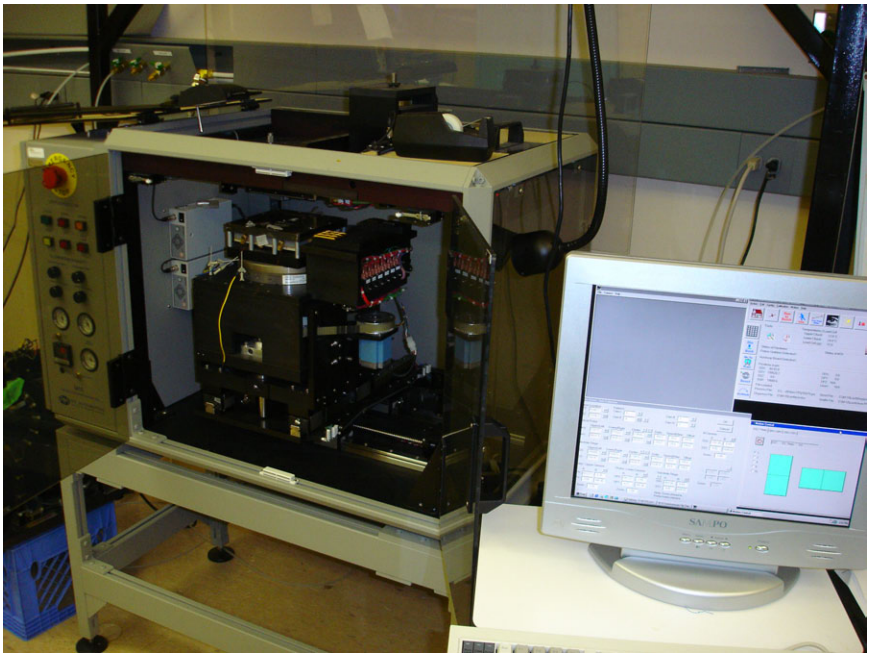


Figure 4.35: Photograph of the RD Automation M10A Flip-Chip Bonder that was used for precision pick and place operations.

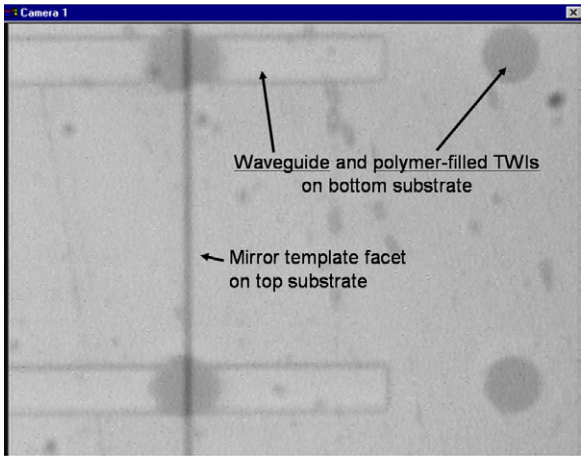


Figure 4.36: Image of mirror template aligned to a substrate having waveguide fabricated over polymer-filled TWIs. The image was captured by the flip-chip bonder's split-optic vision system immediately before attachment.

4.5.3 Waveguide-Mirror-TWI Coupling Demonstration

The setup for testing the coupled waveguide-mirror-TWI structure is shown schematically in Figure 4.39. A single-mode optical fiber, pig-tailed to a 635 nm laser diode, was used

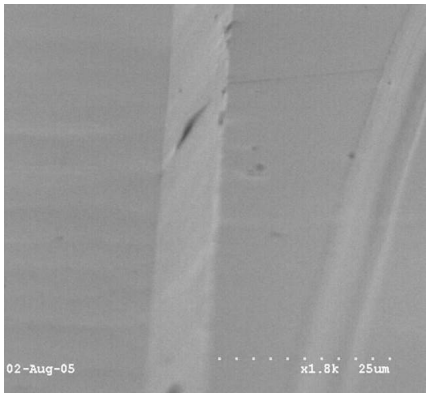


Figure 4.37: Image showing a mirror facet imprinted onto a film of Avatrel 2580-20.

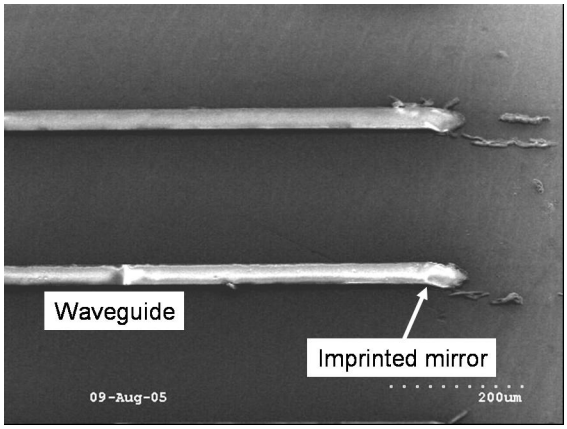


Figure 4.38: SEM image showing the completely fabricated waveguide-mirror-TWI structure.

to excite a waveguide on the backside of the fabricated sample. Once again, it was very important to cleave the test sample such that the cross-section of the waveguides was nearly vertical. This assures maximum coupling of optical power between the fiber and the waveguide. A CCD camera with focusing optics was then used to observe and capture the light being coupled from the optical fiber to the waveguide-mirror-TWI structure. Successful transmission of light from the waveguide and up through the TWI was achieved. Figure 4.40 shows the image captured by the CCD camera.

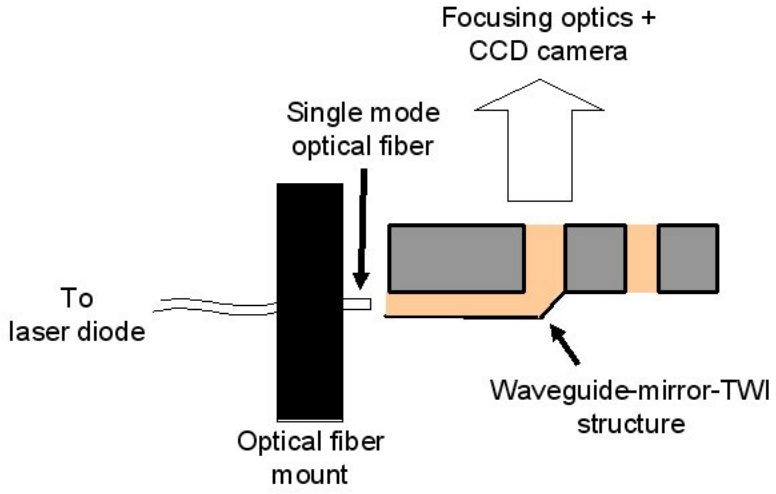


Figure 4.39: Schematic of a experimental setup used to test optical coupling in the waveguide-mirror-TWI structure. Light from a 635nm laser diode was coupled to the waveguide using a single mode optical fiber; the output from the TWI was observed with a CCD camera.

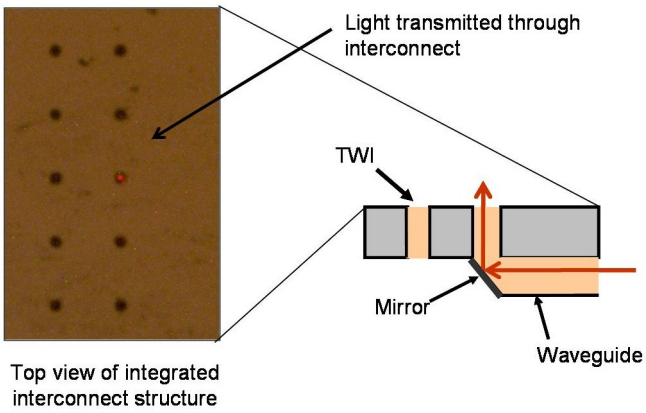


Figure 4.40: Image from CCD camera showing successful optical transmission in the waveguide-mirror-TWI structure.

4.6 Conclusion

Guided-wave through-wafer interconnects designed to transfer optical signals from one side of a wafer to the other have been described in this chapter. Depending on the application and processing requirements, these interconnects can use either air or a polymeric material as the transmitting medium. TWVs filled with Avatrel 2580-20 polymer were also process integrated with mirror-terminated waveguides. This interconnect structure was shown to successfully transmit and bend light from in-plane to out-of-plane. This was a first-time demonstration. Index-matched optical pathways such as this would be very useful not only for probe module applications but also for high-density inter-layer optical transmission in heterogeneous 3D microsystems.

CHAPTER V

COMPLIANT PROBE SUBSTRATE FOR TESTING HIGH PIN-COUNT CHIPS

5.1 Introduction

The physical interface between the device-under-test and automated test equipment has consistently been identified as a challenge for testing in future generations of integrated circuits [1]. High pin-counts, low pitch, high bandwidth, and low cost of fabrication and operation are just some of the key requirements for probe technologies. In addition, to reduce the overall cost of wafer-testing, there is an industry-wide effort to implement parallelism in the process. Equation 5.1 is a simple expression that can be used to estimate the benefits of massively parallel testing:

$$\mathsf{T}_{\mathsf{wafer-test}} = \frac{\mathsf{N}_{\mathsf{die}}}{\mathsf{N}_{\mathsf{probe}}} \left(\mathsf{T}_{\mathsf{align}} + \mathsf{T}_{\mathsf{step}}\right) + \frac{\mathsf{N}_{\mathsf{die}}}{\mathsf{N}_{\mathsf{test}}} \mathsf{T}_{\mathsf{test}} \tag{5.1}$$

where, $T_{wafer-test}$= time to test a wafer, N_{die}= number of chips on a wafer, N_{probe}= number of chips that are contacted at once, N_{test}= number of chips that are tested in parallel, T_{align}= time to align probe card, T_{step}= time to step probe card from one set of chips to another, and T_{test}= time to test a single chip.

Figure 5.1 plots $T_{wafer-test}$ when the various paramaters in Equation 5.1 are varied. It is clear that the worst-case scenario is when a wafer is probed and tested one chip at a time, and the best-case scenario is when all the dice on the wafer are contacted and tested in parallel (wafer-scale).

Traditional ATE units are built on a per-pin architecture, and the total number of available signal pins is therefore limited by the capital investment required; ATEs can cost on the order of several thousand dollars per channel. As a result, parallel testing is most

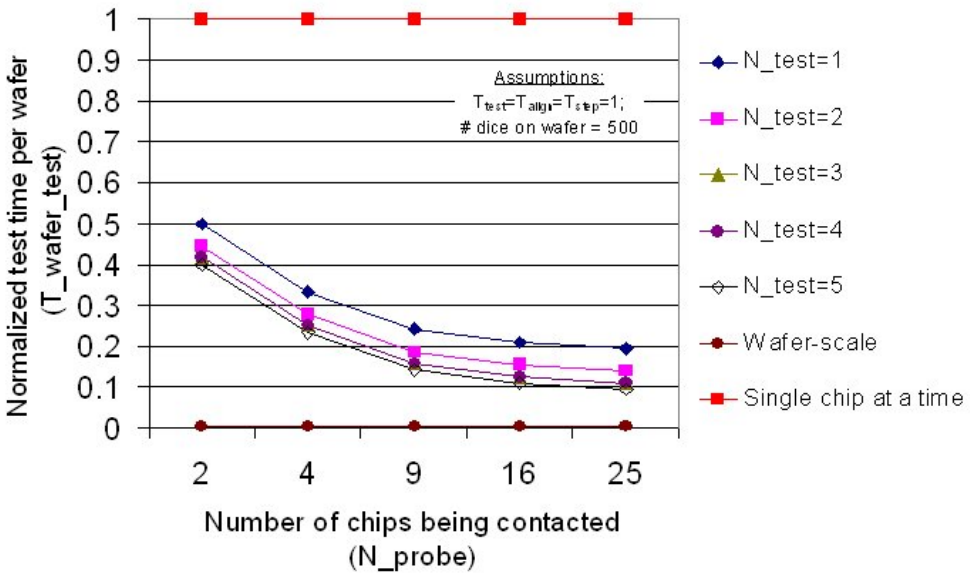


Figure 5.1: Curves depicting variation of normalized test time per wafer as a function of the number of dice being probed and tested in parallel. The alignment time, step time, and test time were assumed to be one.

common in low pin-count products such as commodity memory. If the DUT is a high pin-count device, such as a microprocessor (MPU) or an application-specific IC (ASIC), then some form of reduced pin-count testing needs to be employed to allow parallel testing. Reduced pin-count testing is generally achieved by use of a DFT technique, such as scan and/or BIST. If all chips are designed to be completely self-testable, then only a simple (usually serial) communications bus is necessary to allow the external test equipment to initiate the self test and to capture the final result (pass/fail response or more detailed diagnostic data). One bus, for such purposes, is defined by the IEEE 1149.1 standard (sometimes called *boundary scan*). However, oftentimes, BIST is not able to achieve the required levels of fault coverage, and has to be accompanied by additional testing using *top-off* test vectors. In these cases, the number of ATE signals needed for thorough testing still remains quite high.

While parallelism during testing is desirable to keep costs low, there may be some chips designed for use in high-performance applications (space, military, etc.) where guaranteed fault-free operation takes priority. One way of achieving such high levels of fault detection

would be to use a large number of chip I/Os during testing; doing so increases the controllability and observability of the chip during testing. For example, in a high-performance system-on-a-chip (SOC) design, the large number of I/Os could be used to physically partition the DUT into individual cores. Each core could then be pseudoexhaustively tested, individually or in parallel. Breaking up the DUT into smaller units reduces the volume of test patterns while still maintaining high test fault coverage.

The projected number of probe points per touchdown for different classes of integrated circuits is summarized in Table 5.1 [1].

Table 5.1: Projected trends for multi-DUT testing in different classes of digital integrated circuits.

	2006	2009	2012	2015	2018	2020
Memory						
Signal probe points/touchdown	14,500	17,000	20,000	20,000	20,000	20,000
DUTs in parallel	256	1,024	1,024	2,048	2,048	2,048
Microprocessor						
Signal probe points/touchdown	1,024	1,024	2,000	2,000	6,000	6,000
DUTs in parallel	8	16	32	64	256	512
Application-Specific IC						
Signal probe points/touchdown	1,050	1,500	3,000	3,000	3,000	3,000
DUTs in parallel	8	16	32	64	256	512

Therefore, whether it be for testing a large number of low pin-count/reduced pin-count chips in parallel or a single high pin-count chip, there is a need for high-density probe modules that would be used during wafer-testing. The design, construction, and demonstration of an all-electrical compliant probe substrate are discussed in the following sections.

5.2 Probe Substrate Design

The architecture of the all-electrical probe module is based on the generic probe module illustrated in Figure 2.1; it consists of a probe substrate and a redistribution substrate. The compliant probe substrate is itself comprised of three primary components: (a) compliant probes to contact the I/Os of the DUT, (b) multi-level interconnects for signal redistribution, and (c) through-wafer interconnects for signal transfer between the two sides of the

substrate.

Multi-level interconnects on the probe substrate are optional; signal redistribution could be performed entirely on the redistribution substrate to which the probe substrate is attached. The design and fabrication of multi-level interconnects is therefore not included in this work. It is also assumed that metal-filled through-wafer interconnects, discussed in detail in Chapter III, will be used for transferring signals between the front- and back-sides of the probe substrate.

The probes were batch-fabricated on a silicon substrate, and designed for use in various probe card configurations to provide a reliable, high-speed interface between high pin-count DUTs on the one side and ATE on the other. All probe substrate samples shown here were designed and fabricated to simultaneously contact multiple chips, each having 10^3 I/Os/cm^2. The design is scalable for densities $> 10^4$ I/Os/cm^2. A schematic of this probe substrate is shown in Figure 5.2.

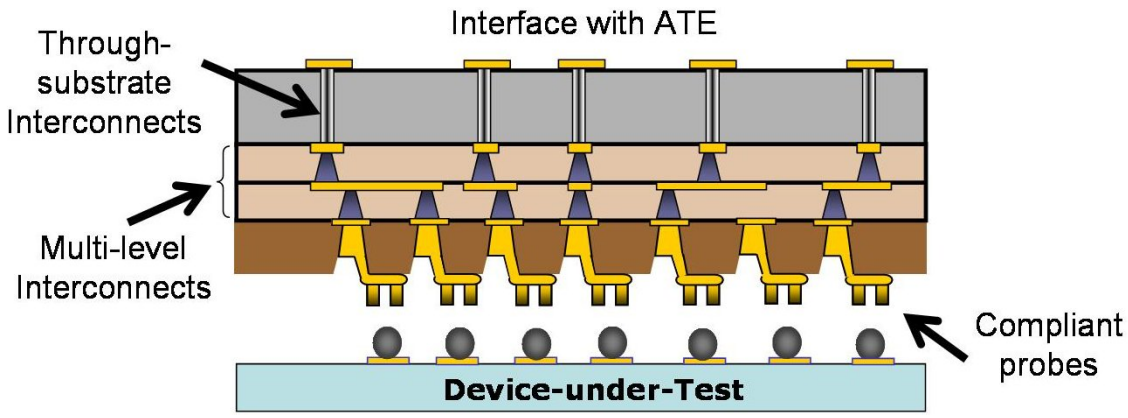
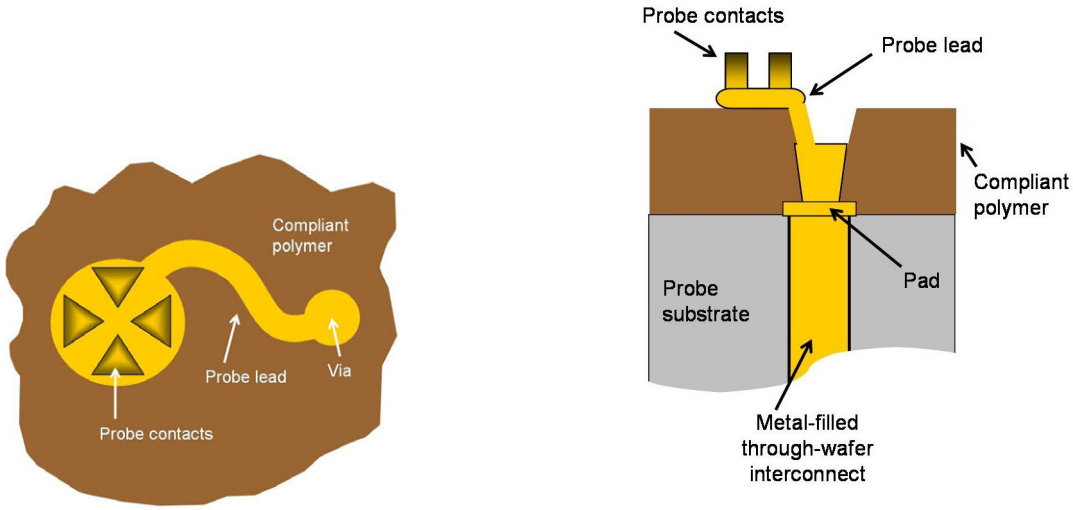


Figure 5.2: Schematic of proposed compliant probe substrate for testing high pin-count chips.

The design of the compliant probes is a modification of the leads from the compliant wafer-level package (CWLP) [70] and Sea-of-Leads I/O interconnects [70]. The probes have out-of-plane (z-direction) compliance, but adhere well to the substrate. Zero in-plane motion is desirable to assure good x-y positional accuracy. Schematics of the probes are shown in Figure 5.3. The structure consists of an S-shaped lead connected to the substrate

through a via on one end. The other end is circular, and has four prism-shaped contacts where the target solder bump would sit (Figure 5.4).



(a) Top view (b) Side view

Figure 5.3: Schematics illustrating the design of the compliant probes.

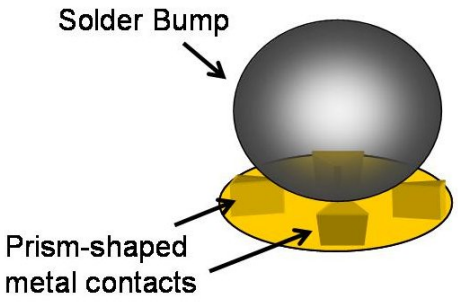


Figure 5.4: Schematic showing contact mechanism of prism-shaped probe tips and a solder bump on the wafer.

Out-of-plane compliance ensures that a stable low-resistance contact can be achieved between the probes and the I/O interconnects on the DUT. When a wafer with compliant I/O interconnects, such as SoL [71], is to be contacted, the probes provide further flexibility for better contact. The probes provide all the requisite compliance when contacting non-compliant I/O interconnects. Vertical compliance is attained by having the leads rest on a

low-modulus polymer. The compliance can be further increased by fabricating embedded air-gaps underneath the leads [71]. The idea is illustrated in Figure 5.6. The amount of compliance is then dependent on the geometry of the air-gaps.

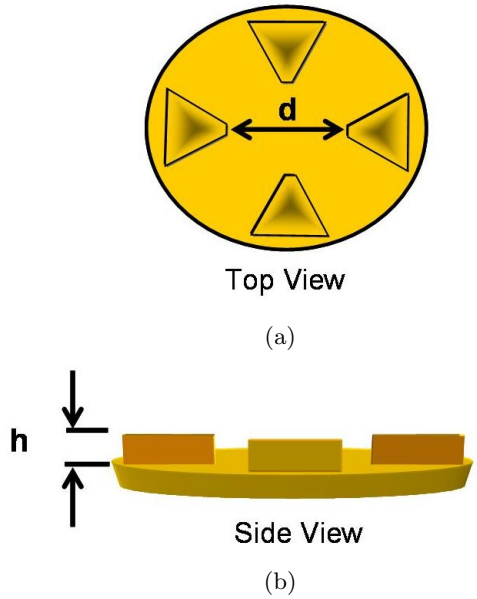


Figure 5.5: Illustration of probe tip design. The separation between the probe tips (a), their height(b), geometry as well as the number of tips can be varied easily to accomodate electrical I/Os of different shapes and sizes.

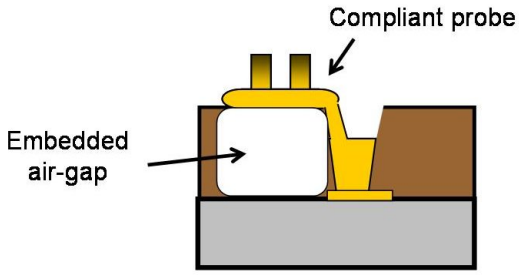


Figure 5.6: Schematic of a compliant lead over an embedded air-gap. The airgap could help increase the out-of-plane compliance.

In the implemented probe structure, the four prism-shaped contact tips were designed to make pressure contact around the edges of the target solder bump (Figure 5.4). This prevents damage to the top side of the solder bump, which is the point of attachment between the chip and a board. The distance between the probe contacts, their height, and

their geometry can be varied to contact electrical I/O interconnects of various shapes, sizes, and materials (Figure 5.5).

The tips ought to be constructed with a hard, non-tarnishing, easy-to-clean, highly-conductive material. Tungsten, tungsten-rhenium, beryllium-copper, gold, paliney 7 (an alloy containing palladium, silver, gold, and platinum), paliney 9 (an alloy containing palladium, silver, gold, platinum, and copper), gold-on-nickel, palladium cobalt, and rhodium are some materials commonly used by probe manufacturers today. The contacts on the fabricated compliant probes were made of electroplated nickel and finished with a thin coating of electroplated gold.

5.3 Fabrication

5.3.1 Process Summary

Like the design, the fabrication of the compliant probes is also based on the CWLP [70]. A schematic of the process flow is shown in Figure 5.7. The fabrication begins on a substrate that already has Cu-filled through-wafer interconnects (as described in Chapter III). A 300 Å/1 μm/300 Å layer of Ti/Cu/Ti was sputter-deposited onto both sides of the substrate. 3.4 μm thick SC 1827 positive photoresist from Shipley Company was spun onto the wafer, and an array of metal pads was defined over the vias by photolithography and wet etching of the metal. The process was repeated to define pads on the back-side of the substrate (Figure 5.7 (a)). Following this, a compliant polymer was spin-coated on the substrate (Figure 5.7(a)). Avatrel 2000P photodefinable polymer (from Promerus, LLC), which has a low tensile modulus of 0.5 GPa and a CTE of 50 ppm, was used. Avatrel 2000P is a polynorbornene polymer. It has a low dielectric constant of 2.6, which helps minimize parasitic capacitance. The polymer film was typically spun-on to a thickness of around 21 μm (500 rpm @ 250 rpm/s for 10 s followed by 2000 rpm @ 500 rpm/s for 40 s; soft-bake= 10:00 min at 100°C (hotplate)), but could be changed by altering the spin-on and baking conditions.

The polymer was cross-linked by exposing it in a UV lithography tool, and then cured

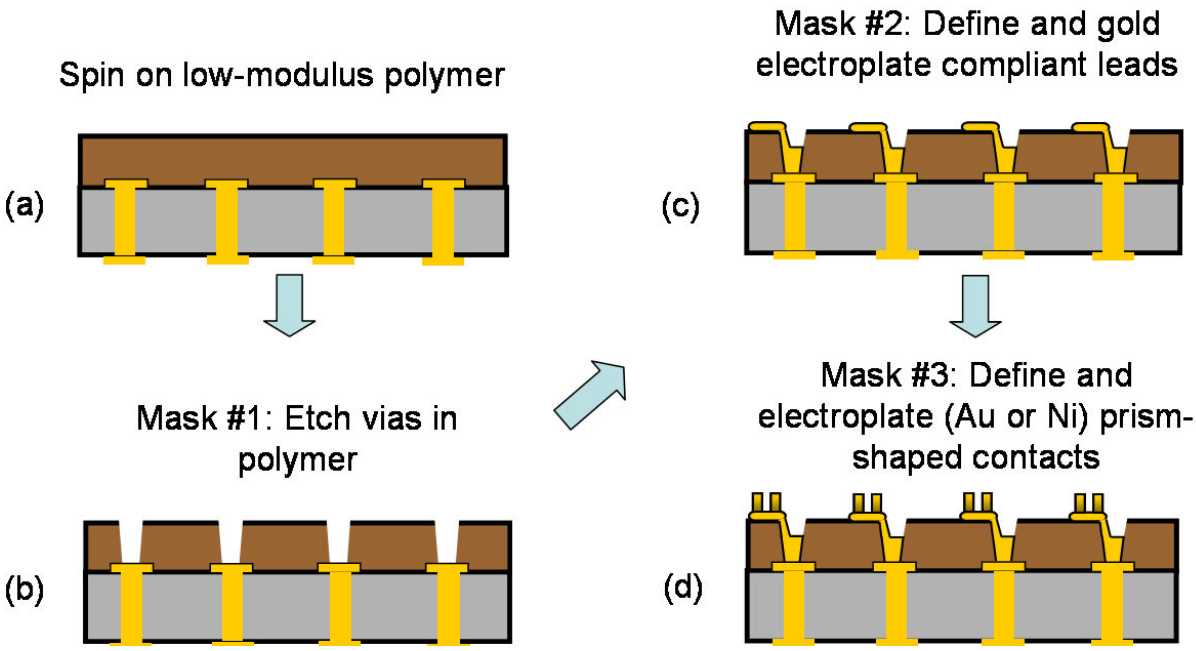


Figure 5.7: Fabrication process flow of compliant probe substrate. (a) On sample with plated through-wafer vias, spin on a compliant polymer (Avatrel). (b) Mask #1: Etch vias to expose the metal pads. (c) Mask #2: Define and electroplate compliant probes. (d) Mask #3: Electroplate probe tips on ends of compliant probes.

in a convection oven or furnace for 4 hours at 200°C. After curing the polymer, a thin layer of aluminum (Al) was sputter-deposited to serve as an etch mask for the polymer. 5 μm thick NR9-8000 negative resist was spun onto the wafer and photolithographically patterned with the first (via) mask; the Al was etched away using a phosphoric-acetic-nitric acid (PAN) etchant at 50°C. After removing the resist by rinsing in Acetone, the exposed polymer was etched away in an RIE (Figure 5.7(b)) using a CHF_3-O_2 plasma. This exposes the metal pads underneath the polymer. The Al etch mask was selectively (with respect to the Ti) removed using Microposit 351 developer (from Shipley Company), and a new layer of Ti/Au/Ti (300 Å/2000 Å/300 Å) was sputter-deposited everywhere. Ti/Au/Ti serves as the seed layer for electroplating the S-shaped leads. The polymer etching process has been previously developed to yield vias with slanted sidewalls [72]. This ensures that the sputtered seed layer will be continous on top of the polymer, along the via sidewalls, and down to the bottom of the vias.

The bottom Ti serves to provide strong adhesion to the polymer beneath. Futurrex NR9-8000, about 10 μm thick, was spun onto the seed layer, and the in-plane compliant leads were monolithically patterned in the photoresist across the entire substrate. Hence, all the leads on the probe substrate can be fabricated in a single step - whether they are to contact a single die, multiple die sites, or an entire wafer. Following the resist developing step, the sample was subjected to a short dry etch in an RIE to *descum* any trace amounts of photoresist remaining within the patterned regions. The top Ti layer was etched away to reveal the sputtered Au. Au leads were then electroplated on the exposed regions to a thickness of about 10 μm (Figure 5.7(c)). A standard potassium aurocyanide-based electrolyte was used for gold plating (Table 5.2 [73]); a plating current density of 20 mA/cm^2 was used. Once electroplating was complete, the photoresist and the seed layer were removed. A new seed layer of Ti/Au/Ti was deposited on the substrate followed by a layer of Futurrex NR9-8000 about 15 μm thick. The thickness of the photoresist depends on the desired contact tip height. A third and final lithography step was used to define the triangular patterns on the edge of each probe lead (Figure 5.7(d)). A short descum etch was done following the resist developing. The top Ti layer was etched away, and the probe tips were formed using electroplating. Once again, all of the contacts across the probe substrate are fabricated in a batch process. As the tips need to be hard, non-tarnishing, and highly conductive, electroplated nickel (Table 5.3 [73]) with a flash of electroplated gold was used. All electroplating steps were done in a setup similar to the schematic shown in Figure 3.24. After plating to the required thickness, the photoresist and the seed layer were removed to yield the complete array of compliant probes.

Table 5.2: Chemical composition of high-speed continuous plating solution used for gold plating.

Chemical	Amount [g/L]
Potassium Gold Cyanide	15-30
Potassium Citrate	90

An SEM image and a 3D optical profilometer scan of a single compliant probe are shown

Table 5.3: Chemical composition of plating solution used for nickel plating.

Chemical	Amount [g/L]
Nickel Sulfate	300
Nickel Chloride	35
Boric Acid	45

in Figures 5.8 and 5.9, respectively. An area-array of plated nickel probe tips is shown in Figure 5.10. As mentioned earlier, probes with contact tips of different shapes and sizes can be fabricated by making only minor changes to the mask design. Figure 5.11 shows an SEM image of an area-array of compliant probes with contacts of different shapes and sizes, fabricated at a 325 μm pitch ($\sim 10^3$ probes/cm^2).

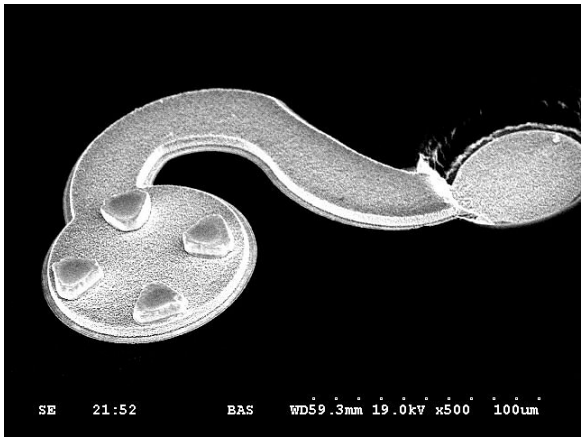


Figure 5.8: SEM image of a single compliant probe consisting of an S-shaped lead and four prism-shaped metal tips. Thousands of probes like this one can be batch-fabricated on the probe substrate.

5.3.2 Probes With Embedded Air-Gaps

Out-of-plane compliance of the probes could be increased by fabricating them atop embedded air-gaps. The idea was illustrated schematically in Figure 5.6. The air-gap is enclosed by a permeable overcoat material. As a result, when the lead is compressed, it displaces a volume of air from the air-gap; the air permeates through the porous overcoat. The pressure in the air-gap is restored when the force on the lead is released.

Compliant leads with embedded air-gaps have been successfully fabricated previously.

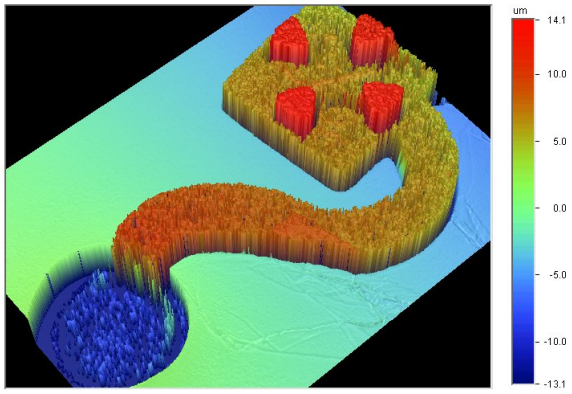


Figure 5.9: 3D rendering of an optical profilometer scan of a single compliant probe.

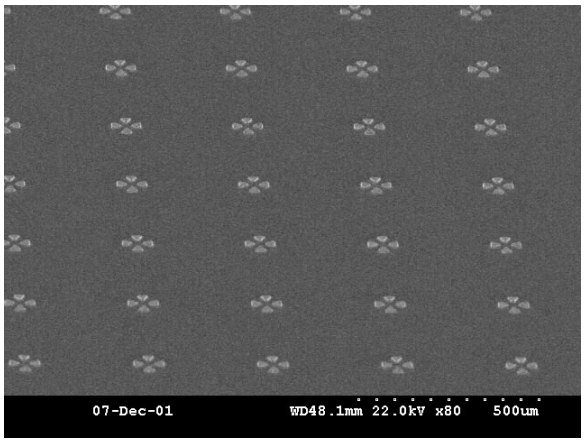


Figure 5.10: SEM image of an area-array of compliant probe tips. Each of these would interface with a solder bump on the DUT.

The details of the process can be found in [71, 74]. Figure 5.12 shows an electroplated compliant gold lead atop an embedded air-gap.

5.4 Compliant Probe Characterization

5.4.1 Contact Resistance (R_{cont})

To minimize signal degradation, it is important that the design of the probes and the materials selected are such as to have the lowest R_{cont} possible. To measure R_{cont}, probes with electroplated Au-on-Ni contacts were fabricated. These were brought in contact with a dummy bumped DUT. Contact between probes and a pair of shorted bumps completed an electrical path, allowing the measurement of contact resistance. A schematic depicting

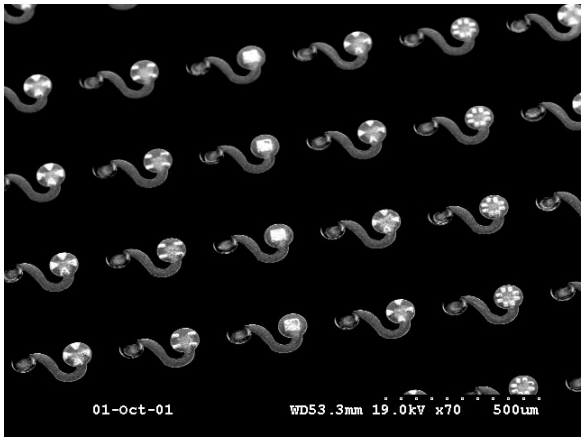


Figure 5.11: SEM image of an array of compliant probes with contact tips of geometries. The shape of the tips was changed simply by altering the design of the mask.

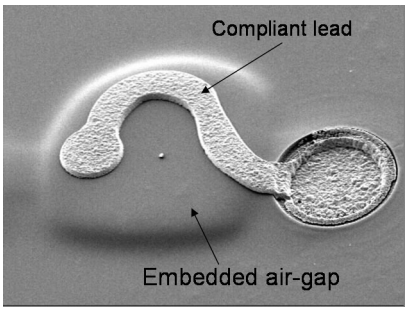


Figure 5.12: SEM image of a compliant lead fabricated over an embedded air-gap. The air-gap would help increase the out-of-plane compliance of the interconnect.

the experiment is shown in Figure 5.13.

5.4.1.1 Fabrication of parts required for measuring R_{cont}

For measuring R_{cont}, a probe substrate sample was built following the process steps detailed in the previous section. The only difference was in the design of the pad layer; here, metal lines were drawn out to connect a few selected probes to peripheral pads on the sample. The pads were made large enough to easily contact test leads from a digital multimeter. Figure 5.14 shows an image of the fabricated compliant probe substrate sample.

A DUT having the same footprint as the compliant probe substrate was fabricated to enable measurement of R_{cont}. This dummy DUT consists of an array of metal bumps on pair-wise shorted metal pads fabricated on a glass slide. The transparent substrate allows

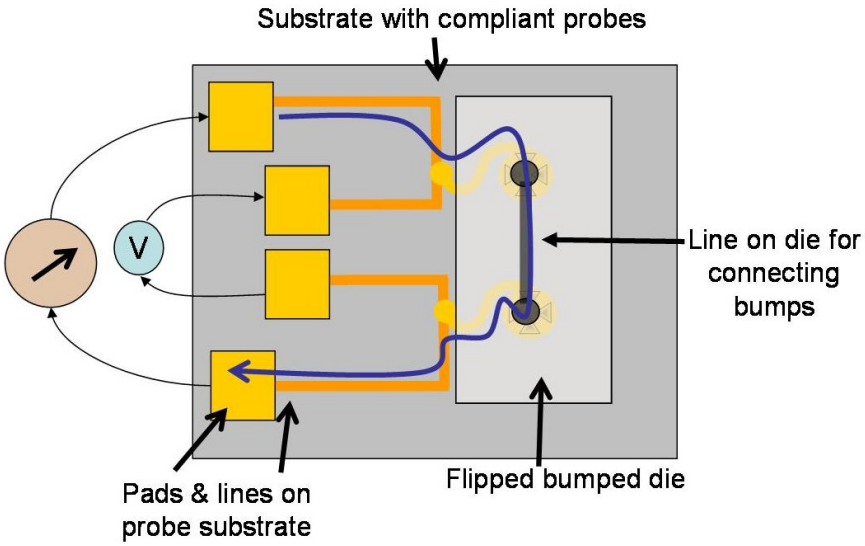


Figure 5.13: Schematic showing method for measuring probe contact resistance.

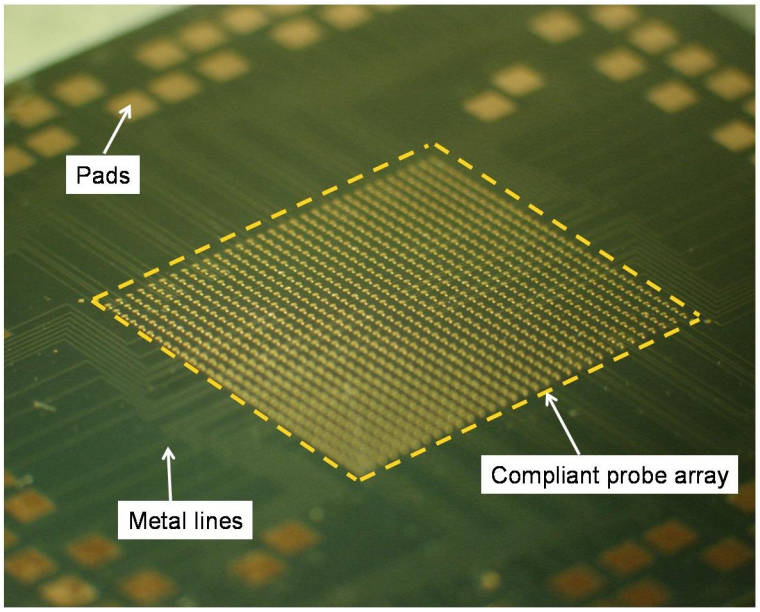


Figure 5.14: Photograph of compliant probe substrate sample used for R_{cont} measurement. Metal lines were fabricated to connect the compliant probes to pads on the periphery of the sample.

for top-down optical alignment (between the DUT and the probe substrate) during the measurement.

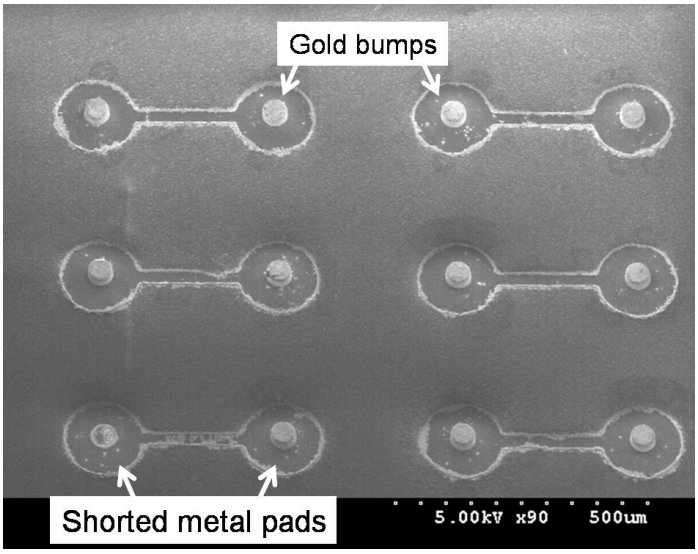
5.4.1.2 DUT fabrication process

After cleaning a glass slide, a layer of Ti/Cu/Ti (300 Å/1 μm/300 Å) was sputter deposited on it. Photolithography and wet etching steps were then used to achieve a pattern of shorted pads on the metal layer. Following this, a layer of Ti/Au/Ti (300 Å/2000 Å/300 Å) was sputter-deposited to act as a seed layer. Next, a $\sim$30 μm-thick layer of NR9-8000 negative resist was spun-on and patterned with a via mask. After developing and a short descum etch, the top layer of Ti was selectively etched in BOE. Gold bumps were electroplated in the via openings to a height of $\sim$25 μm. The resist was then removed by rinsing in Acetone. Figure 5.15 shows images of the fabricated dummy DUT.

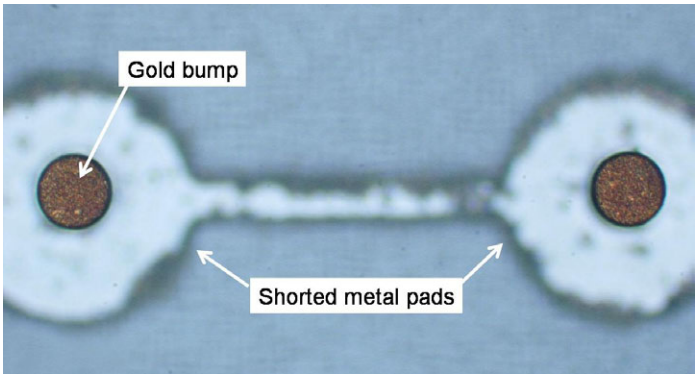
5.4.1.3 R_{cont} measurement procedure

To make a resistance measurement, the DUT must be aligned to and brought in contact with the compliant probes. A Rucker & Kolls probe station was used for this purpose. First, a single bumped die was mounted onto a larger glass substrate using a clear glue. This larger piece of glass was then mounted face-down on the probe station as shown in Figure 5.16. The compliant probe substrate was placed on the wafer chuck, and the two substrates were aligned using the microscope and the in-plane stage motion controls. Once aligned, the vertical separation between the two was reduced until the substrates were in contact. Contact was verified by a simple continuity measurement made with a digital multimeter. Then, a Keithley 2700 series digital multimeter was used to measure four-point resistance for several pairs of compliant probes. The leads attached to the multimeter were connected to the sample by copper wires soldered to the pads on the probe substrate. These are shown in Figure 5.17.

A four-point resistance measurement reading is preferable over a standard two-point one as it neglects the series resistance of the the multimeter connectors and cables; and the pads and traces on the probe substrate. The measured resistance includes the resistance of a pair of compliant probes, a pair of shorted bumps on the dummy DUT, and the contact resistance (for two points of contact) between the two substrates. The interface between



(a)



(b)

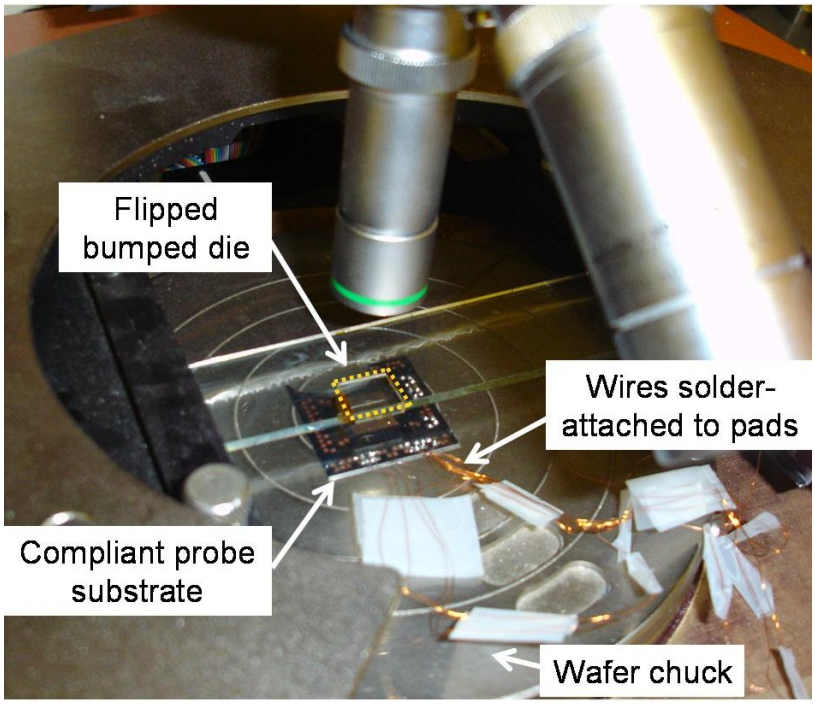
Figure 5.15: (a) SEM image of gold bumps on shorted metal pads. (b) Microscope image of a pair of shorted gold bumps.

the probes and the bumps (i.e. the R_{cont}) is the dominating resistive component in this electrical path. The average R_{cont} per contact was measured to be 0.5 Ω. This compares favorably with R_{cont} data for comparable probe technologies reported in literature [75–86].

5.4.2 Additional Characterization

The compliant lead structure has been characterized to a great extent previously [70–72]. The notable results from these experiments that are also applicable for their use as a compliant probes are summarized below.

(a)

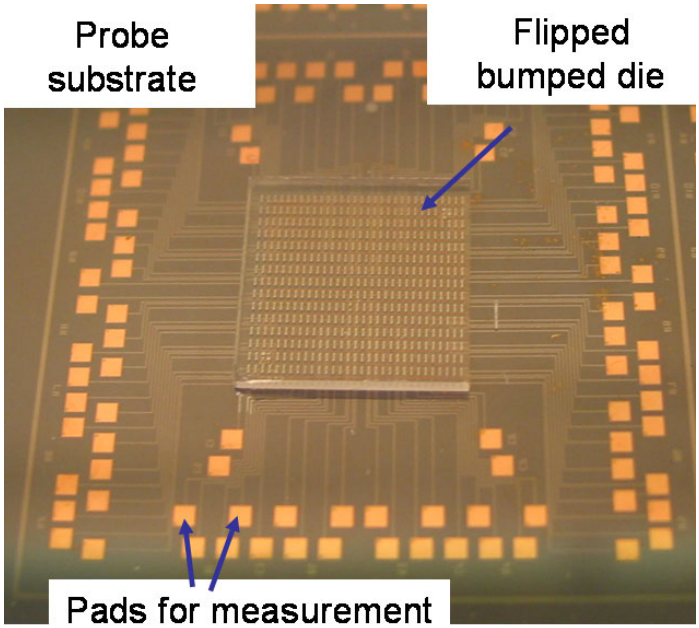


(b)

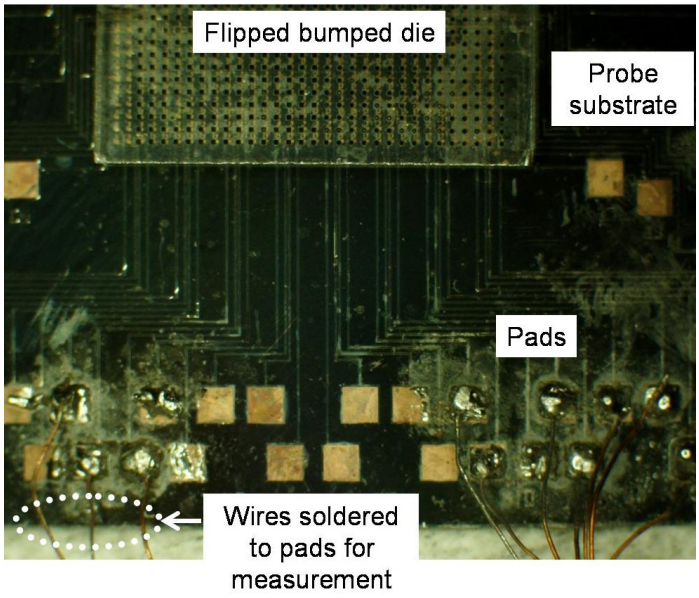
Figure 5.16: (a) Photograph of Rucker and Kolls probe station used for alignment of bumped DUT to the compliant probe substrate. Once aligned, the vertical separation between the two substrates was reduced to bring the two samples in contact. (b) Photograph of samples mounted on probe station for measuring R_{cont}.

5.4.2.1 Electrical measurements

The DC resistance of the probes is estimated to be between 13-37 mΩ for leads of length 185-335 μm, width 20-30 μm, and thickness 10 μm. The variation in DC resistance is



(a)



(b)

Figure 5.17: (a) Photograph of bumped die aligned to a compliant probe substrate sample during R_{cont} measurement. (b) Copper wires solder-attached to the pads were used to connect the leads of the multimeter to the sample.

plotted in Figure 5.18.

Preliminary microwave electrical measurements, reported previously [71], for gold leads approximately 110 μm long, 20 μm wide, and 10 μm thick indicated that the leads exhibited

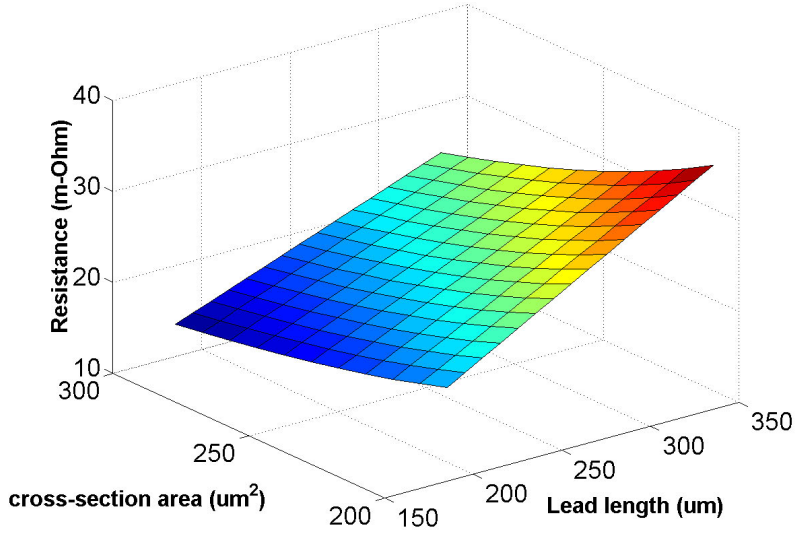


Figure 5.18: Plot of calculated DC resistance as a function of compliant lead geometry.

an almost flat insertion loss from 5 GHz to 40 GHz. A worst-case insertion loss of about 1.2 dB was observed at 40-45 GHz. As microwave measurements performed on leads of similar shape and dimensions have shown excellent performance up to 45 GHz [72], it is expected that the compliant probes will perform well at high frequencies as well.

5.4.2.2 Vertical compliance measurements

The vertical compliance of compliant leads has also been tested previously [71]. Typically, a film of Avatrel, which has a Young's modulus of about 0.5 GPa, was observed to deform elastically till about 10% strain (for an 8 mN applied force). Polymer films with embedded air-gaps had greater vertical compliance. In one instance, as much as 35 μm of displacement was recorded for a 15 mN applied force [87]. These measurements represent the intrinsic compliance of the polymer film and the embedded air-gap structure, respectively.

Fabricating a lead atop either of these reduces the compliance, simply because metals are malleable and exhibit plastic properties. However, the compliance can be adjusted by using thinner metal leads.

5.5 Conclusion

Compliant leads, originally designed for use as chip-to-module interconnections, have been engineered for use as high-density compliant probes. As the probes are constructed using microfabrication techniques, they afford an immense amount of flexibility in the design of the probe tips as well as in the selection of materials. Substrates having compliant probes were fabricated. The leads were made of electroplated gold; the contacts were made of electroplated hard nickel with a thin layer of gold. The average contact resistance between a single probe and gold bump on a DUT was measured to be 0.5 Ω. Probe substrates fitted with these high-density, batch fabricated compliant probes facilitate massively parallel test and are a first step towards achieving full wafer contact and test capabilities.

CHAPTER VI

ELECTRICAL AND OPTICAL COMPLIANT PROBE SUBSTRATE

6.1 Introduction

An attractive entry point for optics in GSI is for chip-to-module communications. This means that optical I/Os will reside alongside conventional electrical I/Os. Various designs for optical I/O interconnections have been proposed in literature. Among these are guided-wave polymer pillar-based I/Os [5], where an optical signal, generated on the chip or off-chip, is transported through a polymer pillar to or from the chip; quasi-free space diffraction grating I/Os [88], where waveguides terminating in diffractive elements, which bend the light in a surface normal direction, are fabricated on the board and the chip; monolithically fabricated optical I/Os [89, 90], where photodetectors and photoemitters are directly fabricated atop the silicon wafer; and hybrid optical I/Os [23, 25, 91], where arrays of vertical cavity surface emitting lasers (VCSELs), photodetectors, or electro-optic multi-quantum well modulators are attached to pads on a chip. Each approach has its pros and cons; the selection of I/O technology is expected to be quite application dependent.

The compliant probe substrate described in the previous chapter has been enhanced to include optical probing capabilities. The optical *probes* discussed in this chapter would be useful for interfacing chips having free-space, quasi-free-space, or guided-wave optical I/O interconnections.

6.2 Design

Figure 6.1 shows a schematic of the probe substrate configuration. The electrical probes are comprised of compliant interconnects capped with metal contacts, and are fabricated

at a 325 μm pitch (approximately 10^3 probes/cm^2). They are compliant in the z-direction (normal to the surface) but maintain x-y (in-plane) positional accuracy. The compliance is desirable to account for any surface non-planarity on the DUT or on the probe substrate itself. Test signals are transferred to the back-side of the probe substrate using plated, through-substrate interconnects. The pads on the back-side interface with the ATE.

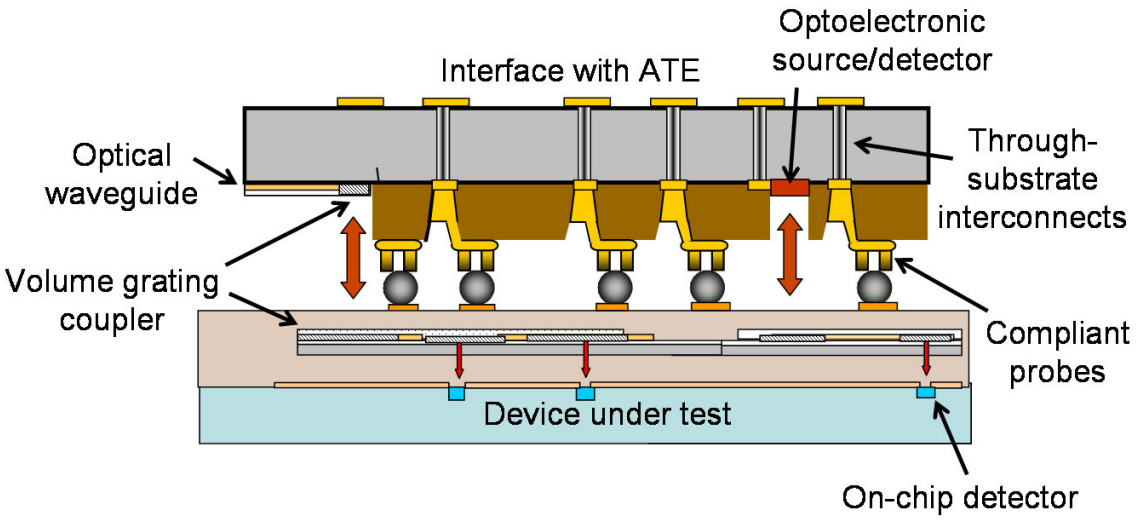


Figure 6.1: Schematic of compliant probe substrate with two-material, grating-in-waveguide optical probes.

6.2.1 Grating-in-Waveguide Optical Probes

The optical *probes* in the configuration shown in Figure 6.1 are comprised of waveguides terminated by volume grating couplers (VGCs) [92, 93].

6.2.1.1 Volume grating couplers

A VGC is a passive diffractive optical device that can couple optical power preferentially from an in-plane waveguide structure to a direction normal to the surface or vice versa. The grating coupler works by having a periodic or quasi-periodic variation of refractive index within the material. In a VGC, the variation of refractive index is created within the bulk (i.e. volume) of the grating material as opposed to a surface-relief grating, where periodic

variations are created by physical removal of the material [94]. Schematics of a surface-relief and a volume grating coupler are shown in Figure 6.2. Here, Λ denotes the grating period, and ϕ is the grating slant angle. The slant in the periodic variation of the refractive index in the VGC is responsible for the preferential coupling (either towards or away from the substrate) [66]. VGCs can also be designed to focus the out-coupled beam. This is advantageous for it's use as an optical probe since the optical power would be concentrated towards the target I/O on the DUT. A focusing coupler is achieved by introducing a chirp in the grating period along the length of the grating such that the grating period decreases with length (Figure 6.3) [92, 94]. As the fabrication of the VGCs does not require any etching (and associated processing), it is simpler to realize than a surface-relief grating.

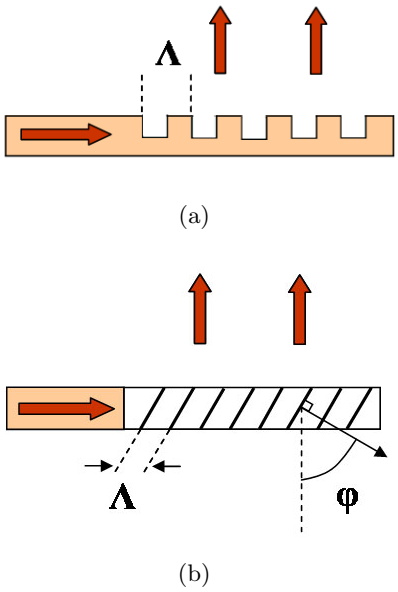


Figure 6.2: Schematic of (a) a non-focusing, preferential-order surface-relief grating coupler, and (b) a non-focusing, preferential-order volume grating coupler.

6.2.1.2 Two-material, grating-in-waveguide optical probes

An optical waveguide fabricated atop a non-focusing, preferential-order volume grating output coupler was selected as the appropriate optical probe structure for a feasible demonstration of the concept (Figure 6.4). The waveguide was made of Avatrel (n_{wg}= 1.5111) and the VGC was realized in Omnidex HRF-600X photopolymer from Dupont (n_g= 1.5161). The

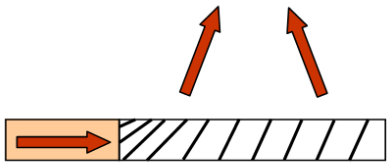


Figure 6.3: Schematic of a focusing, preferential-order volume grating coupler. Designing the grating slant angle to have chirp allows the out-coupled light to be focused to a line at a specific distance from the coupler.

closely matched indices of refraction of the waveguide and grating polymers assures minimal reflection at the physical interface between the two structures. The grating-in-waveguide interconnect sits above a thick layer of SiO_2 (n_{wg}= 1.46), and air (n_{air}= 1) serves as the cover/cladding layer.

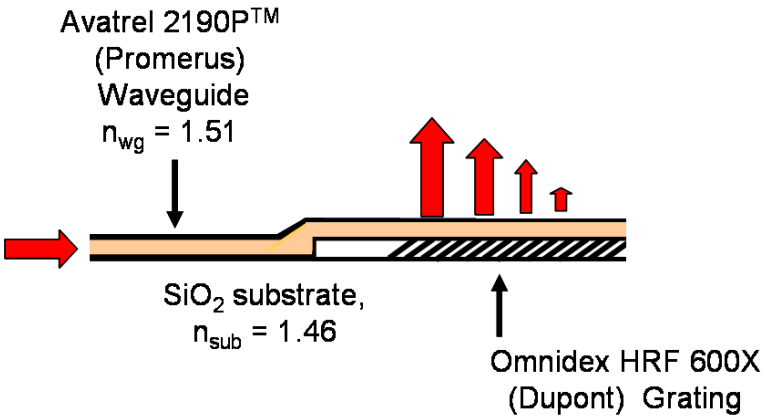


Figure 6.4: Schematic of a grating-in-waveguide output coupler that is to be used an optical probe.

The optical design of grating-in-waveguide interconnects is described in detail in [66]. For an output coupler, the starting point for designing the grating is the out-coupling angle. For surface-normal out-coupling, this angle needs to be close to zero with respect to the waveguide-grating boundary. Then, for the set of materials listed above, and for wavelength λ= 632.8 nm, it was determined the grating ought to have a period Λ= 0.3, and slant angle ϕ= 45.5°. A total of eight optical modes are excited when this diffraction grating is excited

by a transverse electric (TE)-polarized light source of free-space wavelength 632.8 nm. The coupling coefficient, defined as the rate of coupling out of the grating region, is a useful metric to gauge grating performance. The calculated coupling coefficients of the eight excited modes in the designed grating are listed in Table 6.1. The complete grating design procedure as well as efficiency calculations can be found in [66].

Table 6.1: Calculated coupling coefficients for the eight modes that are excited in the volume grating output coupler.

Mode, ν	Coupling coefficient, α [mm^{-1}]
0	20.64
1	20.63
2	1.73
3	0.17
4	0.74
5	0.03
6	0.27
7	0.05

Volume grating couplers, similar to the one used in this probe substrate, have been shown to have high input (80%) [95] and output (95%) [92] coupling efficiencies.

6.2.2 Optical Probing Configurations

Using grating-in-waveguide optical probes, in-plane optical signals are directed normal to the surface, towards the DUT, or vice-versa. Optical sources, mounted either on the probe module or ATE, supply test signals to the DUT via the grating-in-waveguide structures. Similarly placed photodetectors perform an optical-to-electrical conversion of the test response collected from the optical I/Os. Optical fibers coupled to the waveguides would be used to transfer signals to and from optoelectronic test equipment.

Additionally, a probe substrate having waveguides with VGCs on both ends also enables true at-speed testing of any chip with optical inputs and outputs. Tests could be designed such that an optical signal generated on-chip is fed back into an optical input on the chip. Using a signal generated on-chip as a test input removes the need for any external

optoelectronic test equipment and complex signal redistribution schemes. This technique is often referred to as *loopback* testing (Figure 6.5).

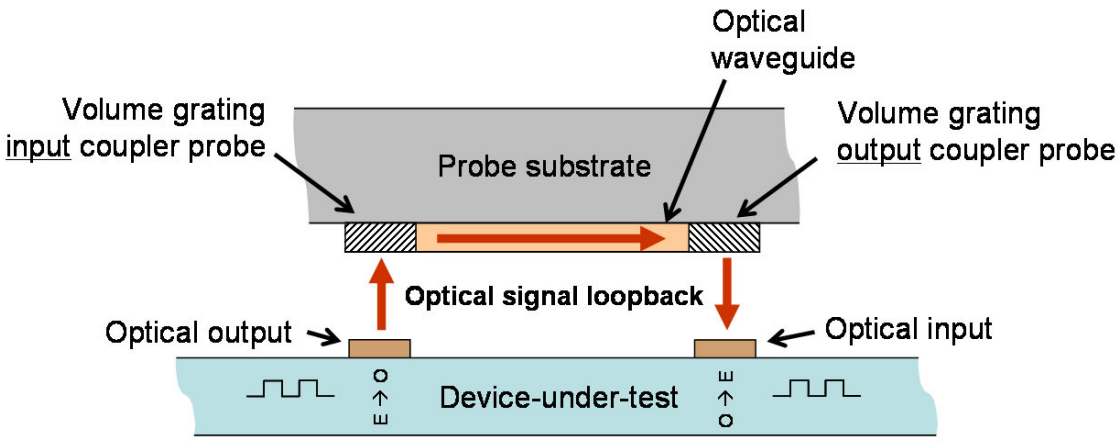


Figure 6.5: Schematic showing optical loopback testing enabled by having an optical waveguide with grating couplers on either end on the probe substrate. Using a signal generated on-chip as a test input for another optical input on the chip enables true at-speed testing.

Photoemitters and photodetectors could be directly integrated onto the probe substrate. Mirror-terminated waveguides are also an alternative to VGC-terminated waveguides. However, in a free-space configuration, reflective couplers lack the ability to maintain the shape of the beam. As a result, unless a photodetector is placed very close to the coupler, it would have to be very large in size to capture a significant amount of the reflected optical power. While these are identified as viable alternatives, they are not covered in this dissertation.

Ultimately, the design and layout of optical components on the probe substrate will be dependent on the intended test plan.

6.3 Prototype Probe Substrate Fabrication

Figure 6.6 depicts the process flow for realizing a prototype probe substrate with compliant electrical probes as well as grating-in-waveguide optical probes. The details of the process are discussed below. The grating-in-waveguide channels were designed to be fabricated between rows of compliant probes. For the prototype, this equates to a pitch of 325 μm or

30 optical-probes/cm^2.

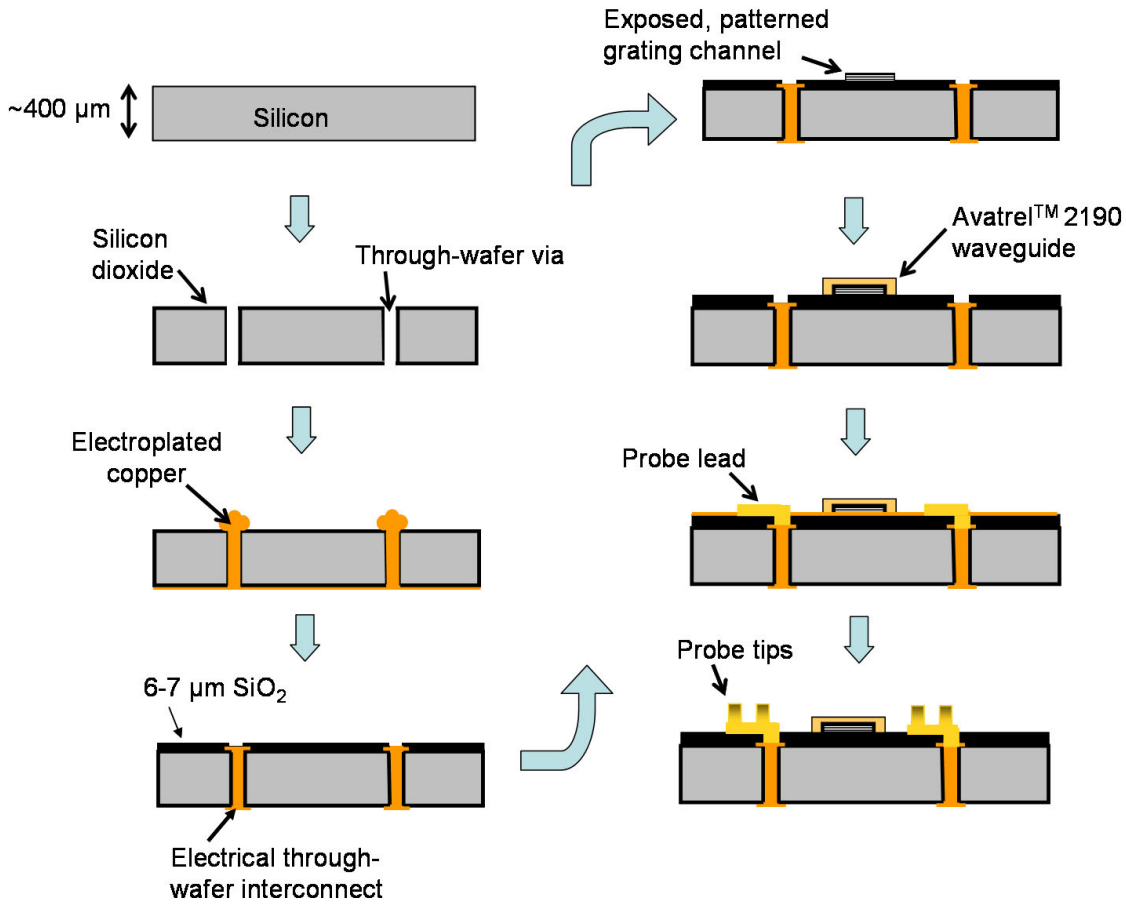


Figure 6.6: Process flow for fabrication of a probe substrate having compliant electrical probes and grating-in-waveguide optical probes. In this prototype, the polymer underneath the compliant leads is replaced with a thick layer of SiO_2 for ease of fabrication.

6.3.1 Plated Through-Wafer Interconnects

The compliant probe substrate was built on a silicon wafer using standard MEMS and IC fabrication techniques. First, TWVs were etched in silicon using the Bosch process. Following this, the vias were passivated with a thin film of thermally-grown SiO_2 ($\sim$1 μm), and filled with electroplated copper to make them conductive. Polishing and etching processes were performed to planarize the overplated copper. Similar to the all-electrical compliant probe substrate, Ti/Cu/Ti (300 Å/1 μm /300Å) was sputtered on both sides of the wafer, and repeated lithography and wet-etching steps were carried out to yield pads

Table 6.2: Process parameters for plasma etching of Dupont Omnidex HRF-600X grating photopolymer.

Parameter	Value
O_2 [sccm]	40
CHF_3 [sccm]	15
Pressure [mTorr]	250
Power [W]	400

on either end of the plated via. The copper-filled TWI process was discussed in detail in Chapter III. Following this, a 6 μm film of SiO_2 was deposited on the substrate using the STS PECVD. The thick SiO_2 passivation layer eases the task of coupling light into the waveguides during the VGC probe characterization.

6.3.2 Grating Channels

The fabrication of the VGC begins with the recording of slab gratings on a 6 μm Omnidex HRF-600X laminate film using the setup shown schematically in Figure 6.7 [93]. The laminate film, as supplied, is covered on both sides with sheets of Mylar. Before exposing the grating, the Mylar sheet on one side was removed. Light from a 363.8 nm argon laser is split into two beams and their interference is recorded on the photopolymer to yield a non-focusing, preferential-order grating. The grating profile, defined through monomer/polymer diffusion, is fixed prior to film cure with an additional 150 mJ/cm^2 uniform one-beam exposure. The exposed grating sheet was laminated face-down on top of the oxide on the sample using a hand roller. Following this, the sample was cured on a hotplate at 150°C for 10 minutes. The remaining Mylar film was then carefully removed using a razor blade, and the curing was completed at 120°C for 90 minutes.

Using gold as a hard-mask, the Omnidex photopolymer was etched in an RIE to reveal raised-strip grating channels. The etch process conditions are listed in Table 6.2. Figure 6.8 shows a microscope image of raised-strip grating channels fabricated alongside plated TWIs on a silicon substrate.

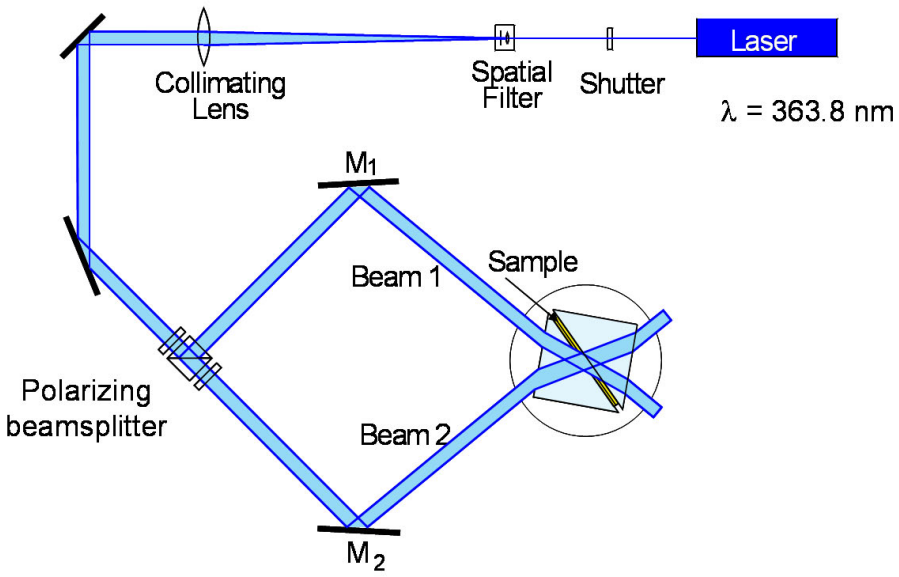


Figure 6.7: Setup for creating volume gratings on a sheet of imageable photopolymer. The grating sheets were recorded separately and then laminated onto the probe substrates.

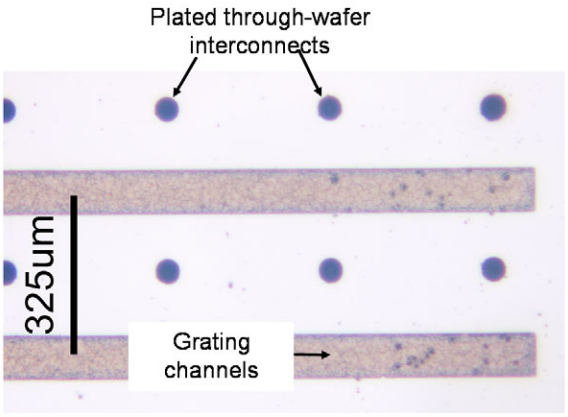


Figure 6.8: Image of raised-strip grating channels fabricated in between rows of copper-filled through-wafer interconnects.

6.3.3 Waveguides

Following grating channel formation, the gold hard-mask was etched away, and a 0.12 μm layer of low-temperature (150°C) PECVD SiO_2 was deposited on the substrate. Low-temperature deposition is essential as higher temperatures would have an adverse effect on the grating photopolymer. The oxide film is also critical for adhesion between the

grating polymer and Avatrel 2190P polymer from Promerus, LLC, which has been shown to be a suitable waveguide material [96]. The propoagation loss of Avatrel 2190 waveguides has been measured to range between 0.78–7.39 dB/cm [66]. Alternatively, SU-8 negative photoresist from Microchem Corp. has been identified as a low-loss waveguide material which would also be compatible with the current fabrication process [97]. A thin layer of AP3000 adhesion promoter from Dow Chemical Company was first spun onto the wafer (3000 rpm @ 1000 rpm/s for 30 s) followed by a 6.8 μm layer of Avatrel^{TM}2190P polymer (200 rpm @ 100 rpm/s for 5 s followed by 500 rpm @ 1000 rpm/s for 40 s). The sample was soft-baked for ten minutes at 100°C in a N_2 purged oven. It was allowed to cool down for ten minutes, and is then photolithographically patterned (300 mJ/cm^2 at 365 nm) into waveguides. The polymer was exposed such as to create waveguides overlaid on the grating channels. On spray developing the sample with Bioact developer (from Promerus), Avatrel waveguides, which completely encapsulate the grating channels, were created. The extra polymer on either side of the grating channels also improves adhesion of the waveguides to the substrate. Avatrel 2190P is usually supplied as a 40-45% solution in mesitylene. For waveguide fabrication, the polymer was diluted to a 25% solution, and was dispensed through a 0.2 μm filter attached to a syringe. Finally, the sample was cured in an N_2 environment at 160°C for 90 minutes. This concludes the two-material, grating-in-waveguide fabrication. Figure 6.9 shows an optical microscope image of the grating-in-waveguide channels fabricated on the probe substrate.

6.3.4 Compliant Probes

The next set of process steps were performed to build-up the compliant probes. First, a thin film of low-temperature oxide (0.12 μm) was deposited on the substrate using the STS PECVD to protect the grating-in-waveguide channels. Lithography and patterning was used to open up vias directly over the plated through-wafer interconnects. The oxide is etched away in BOE. Unfortunately, etching through such a thick layer ($>$ 6 μm) of oxide can take quite some time, and also lead to some amount of undercutting. Dry plasma-assisted

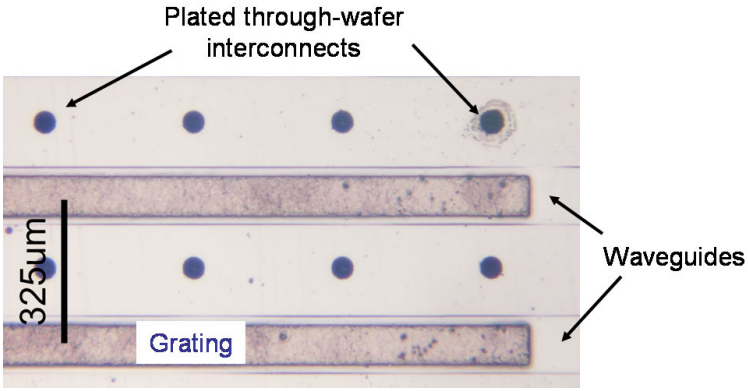


Figure 6.9: Image of two-material, grating-in-waveguide channels fabricated on silicon with plated through-wafer interconnects.

etching could be used if the sample can be maintained at a sufficiently low temperature to prevent polymer deterioration. Once vias were etched down to the metal pads over the TWIs, the photoresist was stripped, and a thin seed layer of Ti/Cu/Ti (300 Å/2000 Å/300 Å) was sputter-deposited on the wafer. The compliant probe leads were then fabricated using photolithography and gold electroplating steps, as described in Chapter V. Figure 6.10 shows an optical microscope image of a prototype probe substrate having grating-in-waveguide optical probes integrated with electroplated probes.

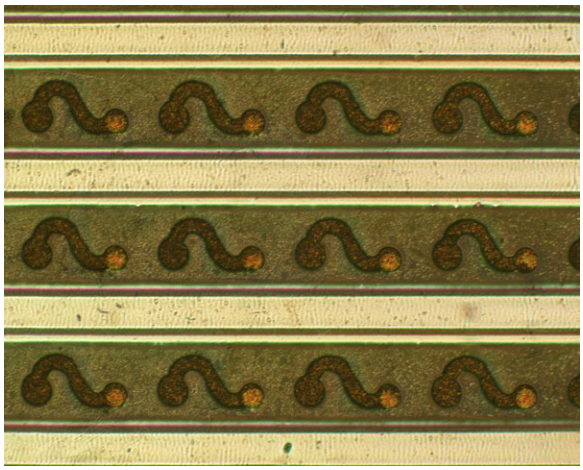


Figure 6.10: Image of compliant leads fabricated alongside grating-in-waveguide optical interconnects.

To somewhat simplify the fabrication of this prototype substrate, the polymer that

would normally exist underneath the leads was substituted with SiO_2. It would be fairly simple to integrate this layer with the appropriate lithography and etch processes.

6.4 Optical Probe Characterization

The grating-in-waveguide out-coupling optical probes are characterized by their coupling coefficient. This output coupling structure was tested using the image capture method. The experimental setup for doing this is illustrated in Figure 6.11; a photograph of the actual test setup is shown in Figure 6.12 [66]. Prior to making the measurement, the sample was carefully cleaved using a diamond-tip scribe. To reduce undesirable reflections at the optical fiber-waveguide interface, it was critical that the waveguide had a near-vertical cross-section.

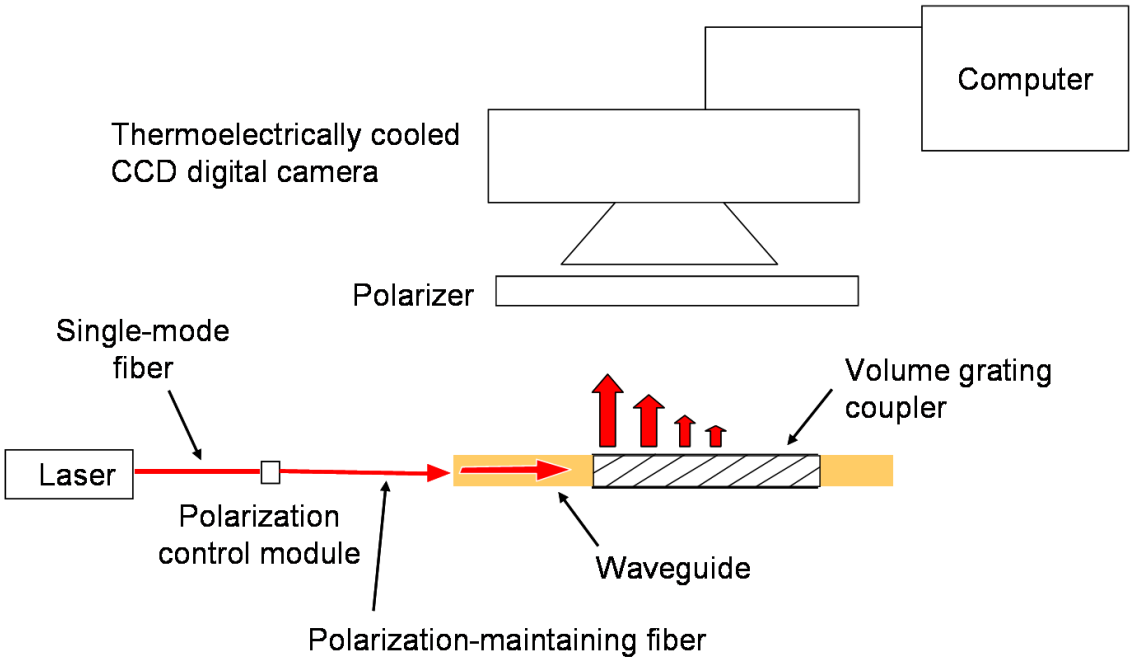


Figure 6.11: Schematic of setup to characterize performance of the grating-in-waveguide output coupler using the image capture method.

The grating-in-waveguide channel was excited using a laser diode source of free-space wavelength 635 nm transmitting through a single-mode optical fiber butt-coupled to a waveguide on the probe substrate. A CCD camera attached to a microscope looking down on the sample was used to capture a bitmap image of photons diffracted and/or scattered

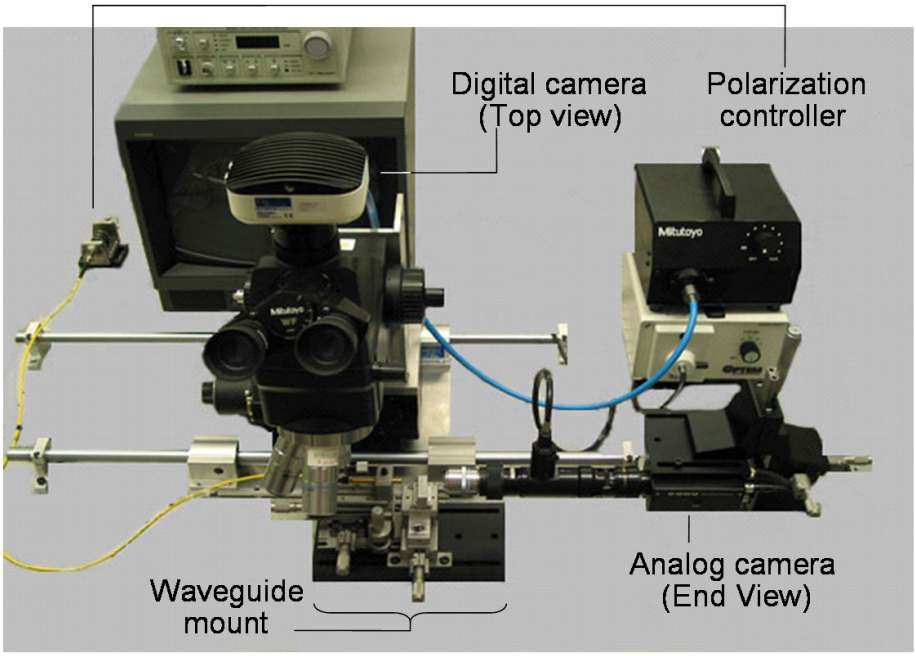


Figure 6.12: Photograph of experimental setup for characterization of the grating-in-waveguide output coupler using the image capture method.

from the grating/waveguide regions. The exposure time was adjusted such that none of the pixels of the CCD were saturated. Figures 6.13, 6.14, and 6.15 show images of the optical fiber coupled to various grating-in-waveguide out-coupling probes. Reflections at the fiber-waveguide interface and the diffracted output from the grating channel are clearly visible.

The captured image, showing out-coupling from a grating-in-waveguide probe, was then fed into MATLAB, and the diffracted output intensity along the length of the grating coupler (columns of the bitmap) was computed by summing the individual pixel intensities for each row in a column (that is, across the width of the coupler). The normalized diffracted output intensity of a typical grating-in-waveguide channel is plotted against distance along the coupler in Figure 6.16. The diffracted output from a non-focusing, preferential-order is expected to be exponential. As a result, a robust linear least squares exponential curve was fit to the measured data, and a typical coupling coefficient, α= 3.95 mm^{-1} was computed.

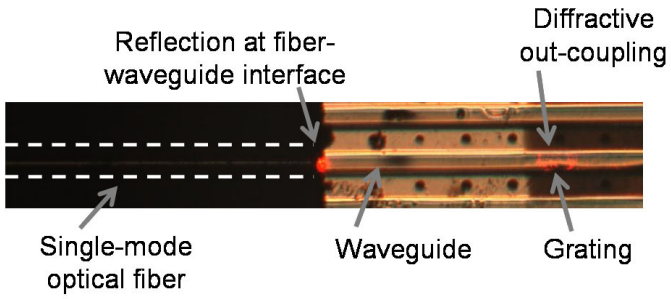


Figure 6.13: Image of optical fiber butt-coupled to a grating-in-waveguide channel with the microscope light turned ON. Reflections at the fiber-waveguide interface as well as the diffracted output from the VGC are apparent. This is a saturated image captured after a long exposure.

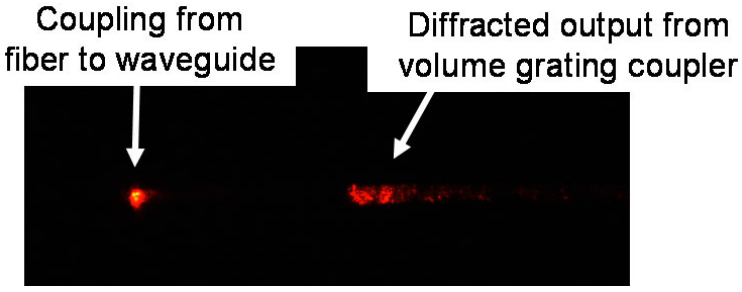


Figure 6.14: Image of diffracted output from a patterned grating-in-waveguide channel with the microscope light turned OFF. This is a saturated image captured after a long exposure.

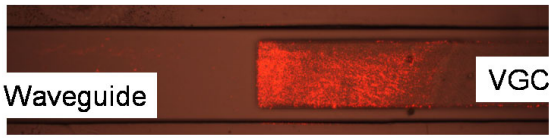


Figure 6.15: Image of surface-normal out-coupling of the optical signal that was input into grating-in-waveguide optical probe. Except for a few specks where light is coupled out due to scattering within the waveguide, out-coupling only occurs in the VGC channel. This is a saturated image captured after a long exposure.

Details of further characterization of similar two-material, grating-in-waveguide output couplers is available in [66, 98]. A peak grating-to-grating coupling efficiency of 31% has been previously reported [66].

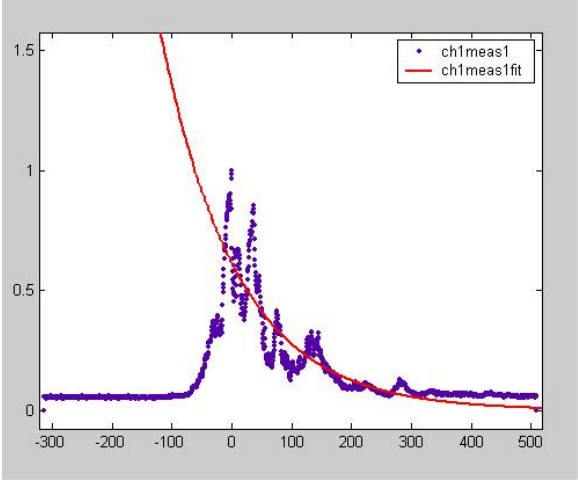


Figure 6.16: Robust linear least squares fit to normalized diffracted intensity of patterned grating channel corresponding to a coupling coefficient α= 3.95 mm^{-1}.

6.5 Conclusion

The compliant probe substrate detailed in Chapter V has been been successfully process-integrated with two-material, grating-in-waveguide optical interconnects to yield a high-density probe substrate with electrical *and* optical probes. The electrical probes, with Au/Ni contacts, have an average contact resistance of approximately 0.5 Ω. The fabricated grating-in-waveguide output couplers have a typical coupling coefficient of 3.95 mm^{-1}. Further process optimization could potentially yield probes with higher coupling coefficients. This is desirable as it equates to out-coupling of larger percentage of optical power in a shorter distance (i.e. smaller coupler regions).

CHAPTER VII

MOEMS-BASED PROBE MODULES FOR TESTING CHIPS WITH POLYMER PILLAR-BASED ELECTRICAL AND OPTICAL I/O INTERCONNECTS

7.1 Introduction

Sea of Polymer Pillars (SoPP) has been proposed as the next generation of chip-level I/O interconnects [99] that would exceed the I/O frequency (> 88 GHz) and current-capacity (> 400 A) requirements projected at the end of the roadmap (in 2020) [1]. This chapter details the design and construction of probe modules for interfacing chips with SoPP-based or SoPP-like I/O interconnects during wafer-testing. The probe module was conceived by drawing from micro-opto-electro-mechanical-systems (MOEMS) design and fabrication principles.

7.1.1 What is SoPP?

Polymer pillars are compliant, high-density ($> 10^5$ I/Os/cm^2), electrical and optical, batch-fabricated, chip-to-module I/O interconnects [5]. Individual pillars can serve as air-clad micro-optical fibers for guided-wave optical transmission, can be metallized for electrical connection, and can even be used for dual-signal (electrical and optical) transmission when partially metallized (here, a conductive film would exist everywhere except on the tip of the pillar). Variations of polymer pillar-based I/Os are illustrated in Figure 7.1.

Optical pillars use air as the cladding layer. This facilitates an index difference (Δn) of 0.51 when the pillars are made of Avatrel ($n_{Avatrel} = 1.51$). As such, the pillars confine light quite well, behaving as cylindrical multi-mode optical waveguides [100]. The high aspect-ratio (as much as 6) pillars and the compliant nature of the polymeric material

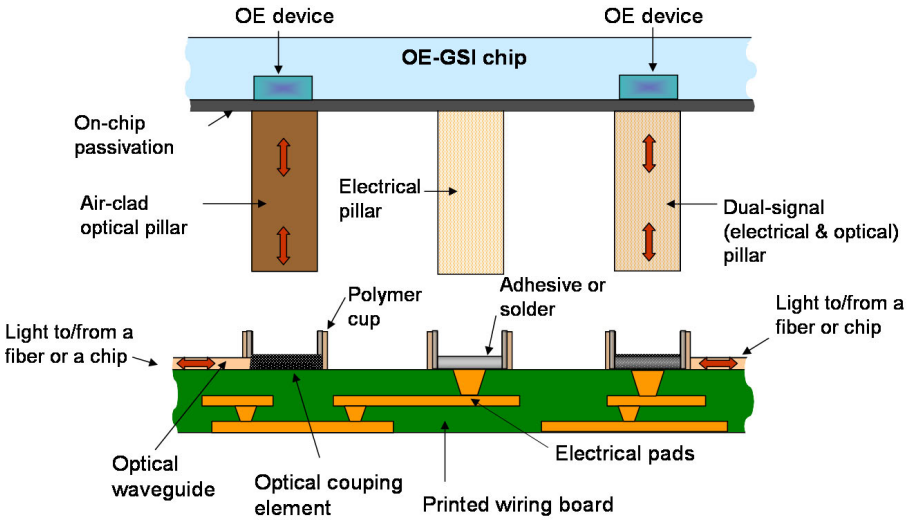


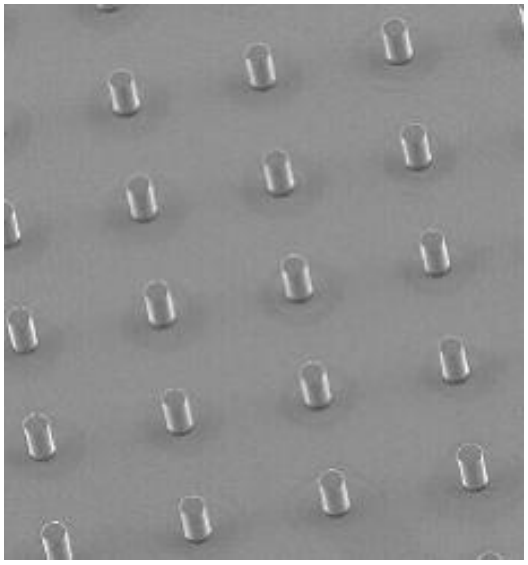
Figure 7.1: Schematic showing different polymer pillar-based I/O interconnections. The same basic pillar-like structure can be used as an air-clad optical I/O or can be slightly modified for use as electrical or dual-signal I/Os.

allow the pillars to bend freely in the event of CTE mismatch between the chip and board during thermal cycling. Such reliable, guided-wave connections between the two substrates eliminates any problems associated with misalignment between optical components on the chip and board. For electrical signals and power distribution, the pillars can be covered with conductive metals, such as copper. Other pillar-like structures that can be simultaneously fabricated include metal (copper) pillars [101] and co-axial pillars [102]. SEM images of arrays of optical and dual-signal SoPP-based I/Os are shown in Figures 7.2 (a) and (b), respectively.

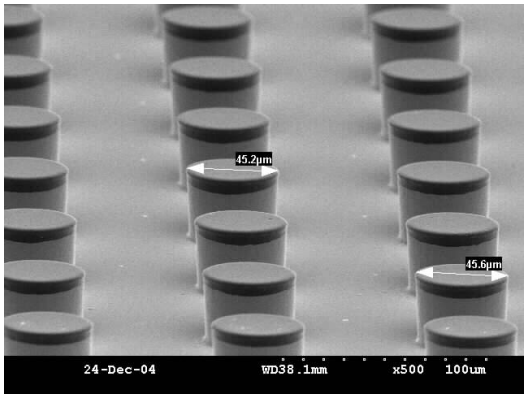
Chips with pillar-based I/Os can be flip-chip attached to a board using solders or adhesives. Pillar-based I/Os are the most intimate combination of electrical and optical input/output (I/O) interconnects for GSI reported in literature.

7.2 Probe Module Design

While the structure of optical I/Os that would be eventually implemented on an OE-GSI chip is yet unknown, optical polymer pillars are an appropriate representation of guided-wave chip-to-board optical interconnects. In addition, electrical pillars are also worthy



(a)



(b)

Figure 7.2: SEM images of (a) optical polymer pillar I/Os and (b) dual-signal polymer pillars I/Os.

representatives of next generation high-density chip-to-board electrical pins. As such, it was judicious to design a probe module, for joint electrical and optical testing, that could interface pillar-based I/Os.

The probe hardware architecture illustrated in Figure 2.1 was once again adopted for designing probe modules for chips with polymer pillar-based I/Os – it consists of a probe substrate and a redistribution substrate (Figure 7.3).

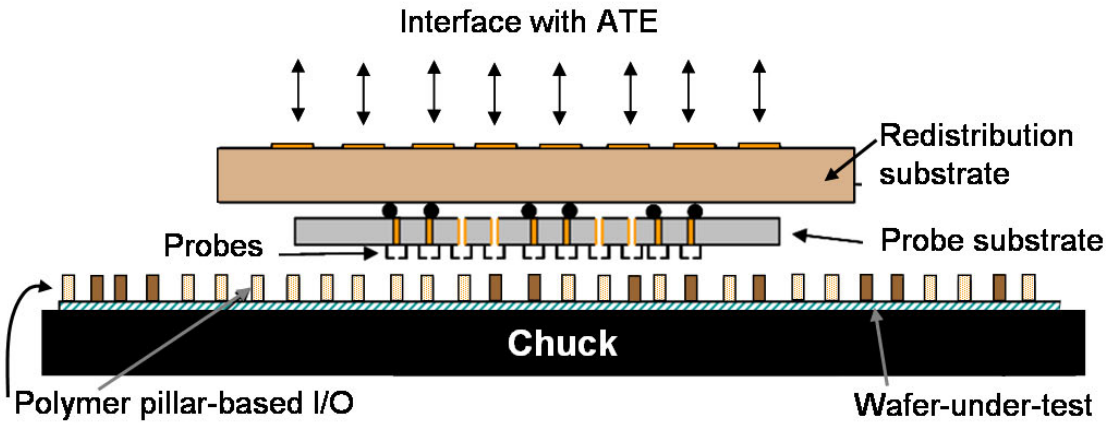


Figure 7.3: Schematic of a generic probe module for testing chips having polymer pillar-based electrical and optical I/Os. It is comprised of a probe substrate and a redistribution substrate.

7.2.1 Probe Module Configurations

Optical I/Os can be probed by a number of methods. The choice of probe depends on the test to be performed, the design of the optical I/O, and the available coupling and redistribution technologies. Figure 7.4 shows a detailed schematic of the possible components on a probe module.

These include:

Active optoelectronic devices: The optical I/Os can be interfaced directly with complementary OE devices. Having an OE device directly above the I/O of the DUT eliminates the need for any optical signal redistribution and allows the redistribution to remain purely electrical.

Passive optical components: Optical components such as a reflective or a diffractive element can also be used to interface with the optical I/Os. When interfacing optical outputs, these elements capture the optical signal and couple it into a waveguide network on the probe module. The function is reversed when interfacing optical inputs.

Waveguide networks: Waveguide networks are necessary on the probe module if passive

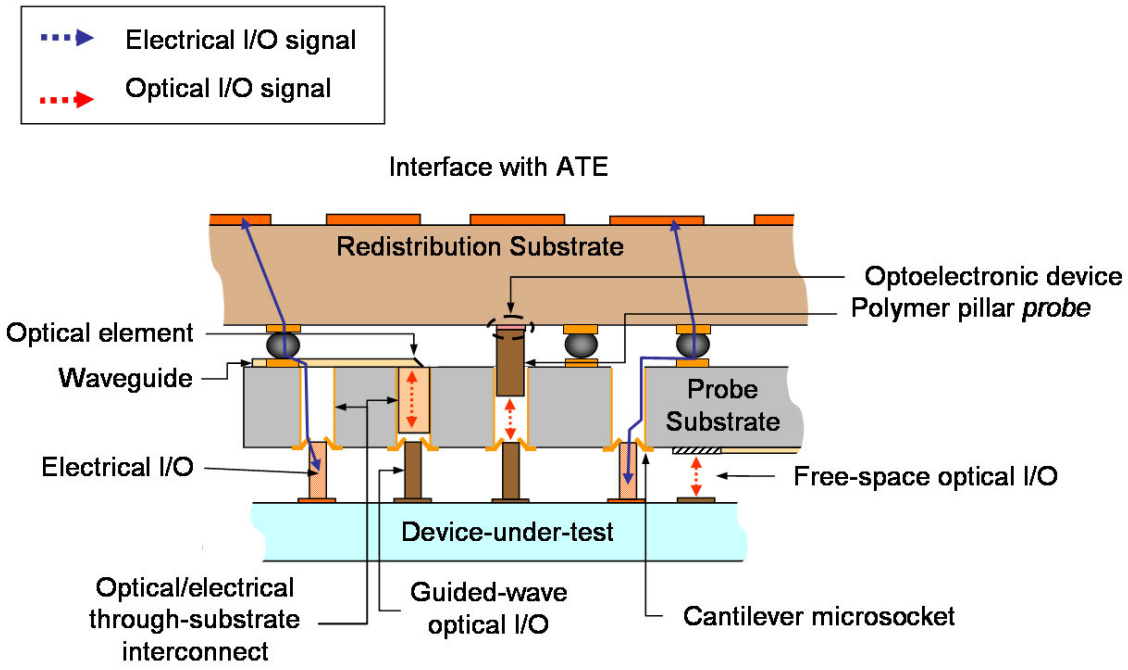


Figure 7.4: Probe module for interfacing chips with electrical and optical polymer pillar-based I/O interconnects. A few different ways of probing the I/Os and redistributing the signals are shown.

optical elements are used for probing optical I/Os. One end of the waveguides would be terminated by the appropriate element (reflective or diffractive). The other end could lead to an active optoelectronic device at the edge of the probe module. Alternatively, waveguides could also be coupled to optical fibers which would then transport the signals to/from the ATE.

Contact probes: Probing optical I/Os does not require contacting them. However, electrical pillars do need to be contacted. The probe module needs to have appropriately designed contact probes.

Through-substrate interconnects: The first level of signal redistribution is to be done on the probe substrate itself. This can be achieved by the use of through-substrate interconnects, as described in Chapters III and IV.

Polymer pillar probes: If a polymer pillar is fabricated atop either the active or passive

optical elements on the probe module, then *probing* of pillar I/Os is reduced to a pillar-to-pillar coupling problem. This is illustrated in Figure 7.5.

Substrate Assembly: The probe substrate could be attached to the redistribution substrate using a standard flip-chip assembly process. Either solder (lead-based or lead-free) or conductive adhesive bumps can be used for this process. This way, if one of the substrates fails, then it can be separated from the other one and replaced with a new part.

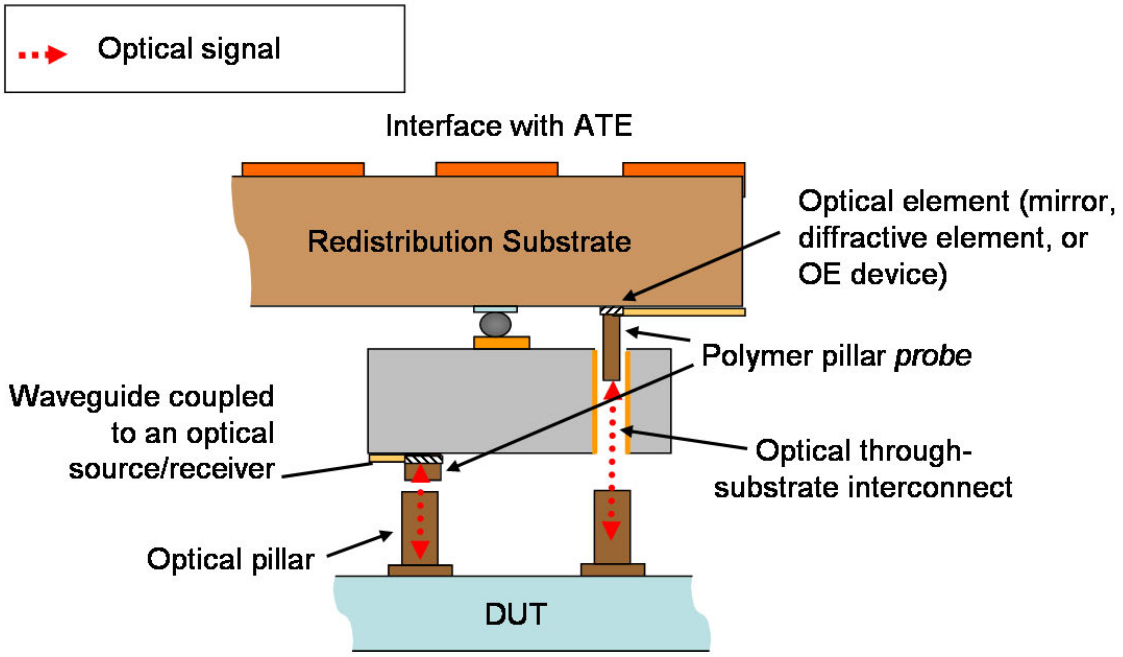


Figure 7.5: Guided-wave optical pillars can be fabricated on the various optical components on the probe substrate. Doing so reduces probing to a pillar-to-pillar coupling problem.

Owing to the lack of knowledge regarding the exact make-up of ATE systems, which would be used for testing chips with electrical and optical I/Os, probe modules having different optical redistribution configurations are proposed. A combination of these configurations can also be used. This flexibility is afforded by the different components discussed above. It is assumed that conventional electrical redistribution techniques will be used to interconnect the electrical probes to the electrical test and power/ground pins on the ATE.

7.2.1.1 *Optical distribution on same side as probes*

The optical equivalent of an electrical wire is a waveguide. Unfortunately, unlike electrical wires, optical waveguides have limited bend radii (i.e. 90° bends would result in a significant loss of optical power), and thus, require more area for routing. If the number of optical I/Os being probed is small, then it is conceivable to have a waveguide distribution network on the probe-side of the substrate (Figure 7.6). The waveguides would be terminated by the appropriate passive optical elements.

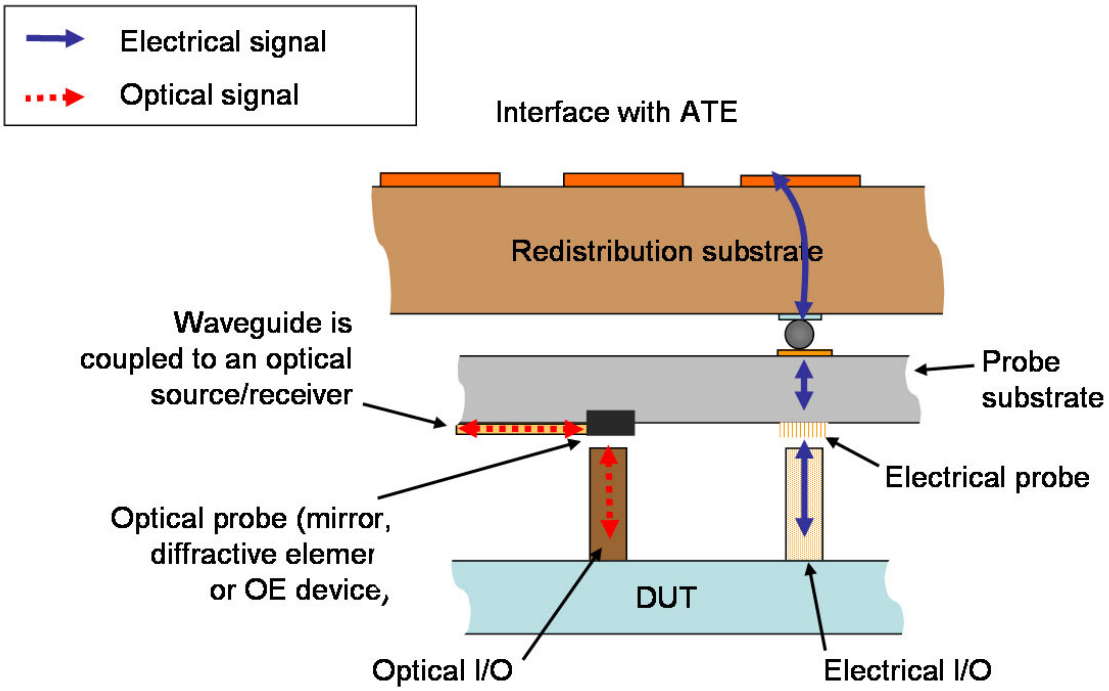


Figure 7.6: Probe module configuration where optical redistribution is implemented on the same side as the probe substrate.

In this configuration, when a signal needs to be directed to the I/O, optical sources located on the probe module or ATE would feed the optical waveguide network. Optical couplers would then bend the light in a surface-normal direction into the probed pillar. Of course, the opposite path is also possible; an optical signal originating from the chip would be captured by the waveguide network on the probe substrate.

7.2.1.2 *Optical distribution on the back-side of the probe substrate*

Processing constraints may not allow the waveguide network to be fabricated on the same side as the probes themselves. If so, the waveguides could be fabricated on the back-side of the probe substrate (Figure 7.7). For a signal originating on-chip, light is transmitted from the I/O to these waveguides by either using a wavelength of light transparent to the substrate material or via a through-substrate interconnect. Conversely, light from a source on the probe module enters the waveguide, is bent and transmitted to the other side of the substrate, and is captured by an optical pillar. Once again, the waveguides would be terminated by surface-normal coupling optical elements.

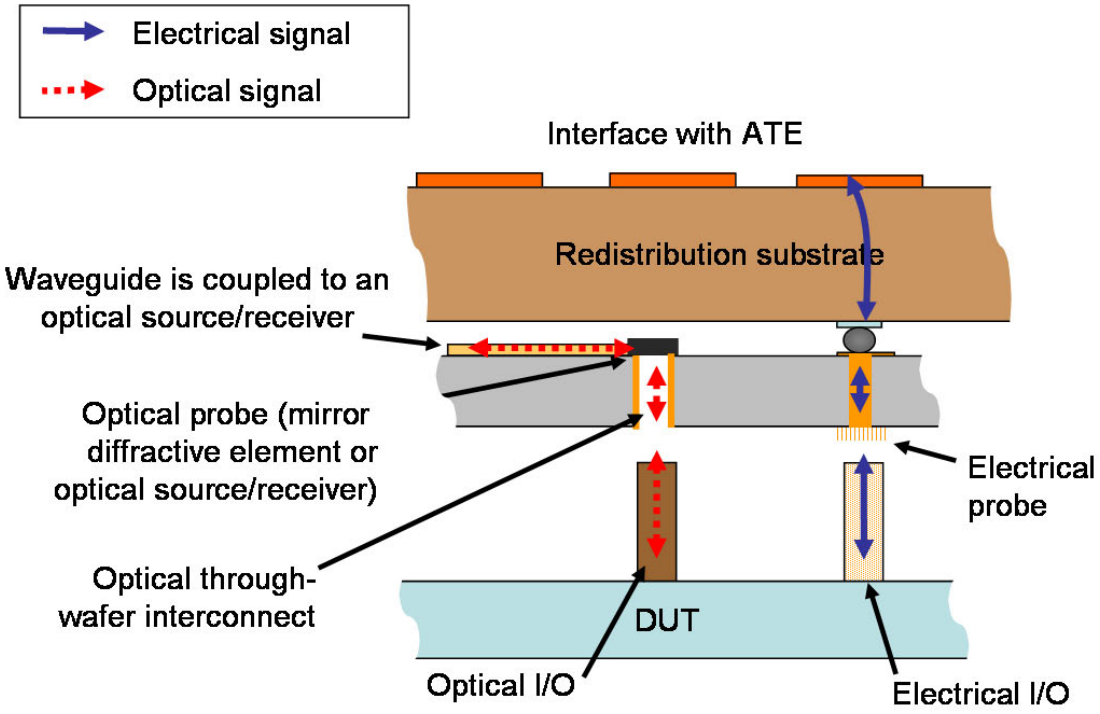


Figure 7.7: Probe module configuration where optical redistribution is implemented on the back-side of the probe substrate.

7.2.1.3 *Optical distribution on redistribution substrate*

A third variation of the probe module is shown in Figure 7.8. It only differs from the previous two cases in that the waveguide network is now fabricated on the redistribution

substrate. This is the first instance where the probing and redistribution functions are split into two physical locations (except for the through-wafer interconnects, which remain on the probe substrate). This division introduces a new feature to the probe module. Oftentimes in manufacturing, probe cards are rendered useless because one or many probes break after repeated use. When this happens, the entire probe card, including the expensive redistribution substrate, has to be discarded. In this embodiment of the probe module, when the probes do fail, the probe substrate could be separated from the redistribution substrate and a new one put in its place. The expensive redistribution substrate, containing electrical and optical interconnect networks can be preserved. The probe substrate then becomes a replaceable part of the probe module – a *probe cartridge*.

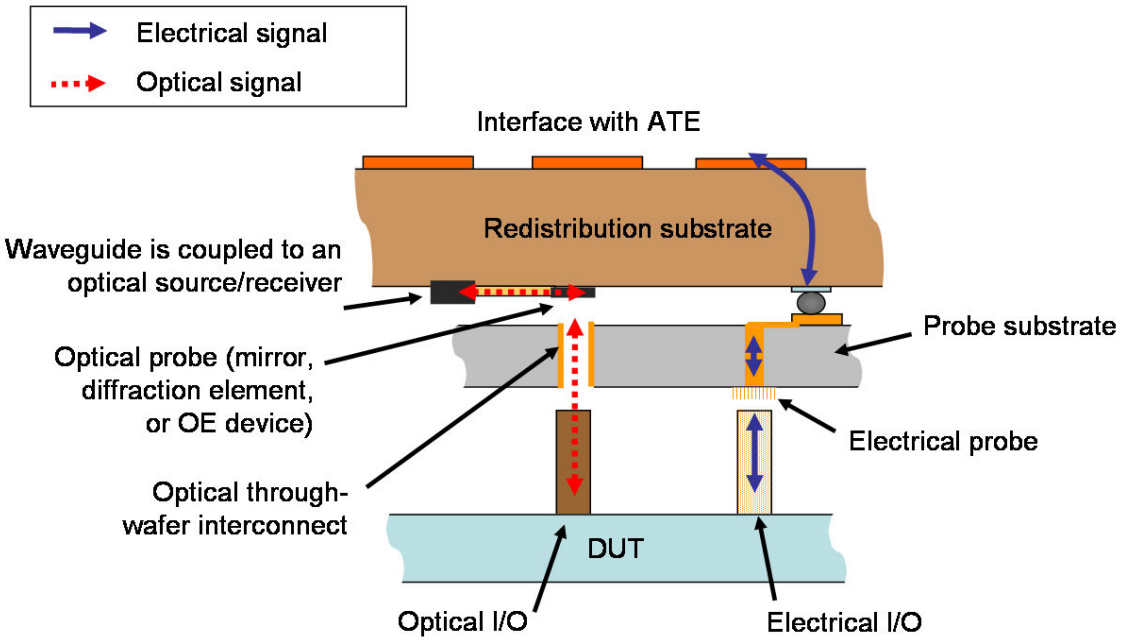


Figure 7.8: Probe module configuration where optical redistribution is implemented on the redistribution substrate. In this scenario, the probing and redistribution functions are implemented on separate substrates. In the event of failure or when the projected lifetime of the probe substrate is reached, this *probe cartridge* can be replaced with a new one.

7.2.1.4 Separate redistribution substrates for electrical and optical signals

The probe module would be truly modular if the optical and electrical distribution were performed on separate substrates. This is shown in Figure 7.9. The electrical signals, transferred to the back-side of the probe substrate, are routed to the periphery, taking care not to block the optical I/Os. The probe substrate is then attached to the electrical redistribution substrate via these peripheral bond pads. The electrical redistribution substrate has an opening at its center. The opening is aligned immediately above the array of through-substrate interconnects on the probe substrate. An optical redistribution substrate, fabricated separately, is attached to the other side of the electrical redistribution substrate. Photoemitters, modulators, and photodetectors as well as passive optical components such as waveguides and couplers populate the optical redistribution substrate. Optical signals originating from the tester are transmitted from the optical redistribution substrate through the probe substrate and into the receiving pillars. Optical signals generated on-chip follow the opposite pathway.

7.3 Prototype Probe Substrate

Each of the configurations described in the previous section is quite complicated. Building one of these would be a mammoth task requiring the integration of a number of different processes such as waveguide fabrication, diffraction grating fabrication, mirror fabrication, and hybrid assembly techniques (for attachment of optoelectronic devices to the probe substrate) to name a few. The goal of this research is not to build any one of these specific probe module configurations *in toto*, but to design and build prototype hardware that would successfully demonstrate repeated probing of a chip having electrical and optical I/O interconnects. Doing *this* would help identify and address the issues related to joint electrical and optical I/O testing at the wafer-level. To this end, a prototype probe substrate was conceived, and is illustrated in Figure 7.10. This bare-bones interposer is comprised of probes to contact the I/Os of the DUT and through-substrate interconnects to transfer

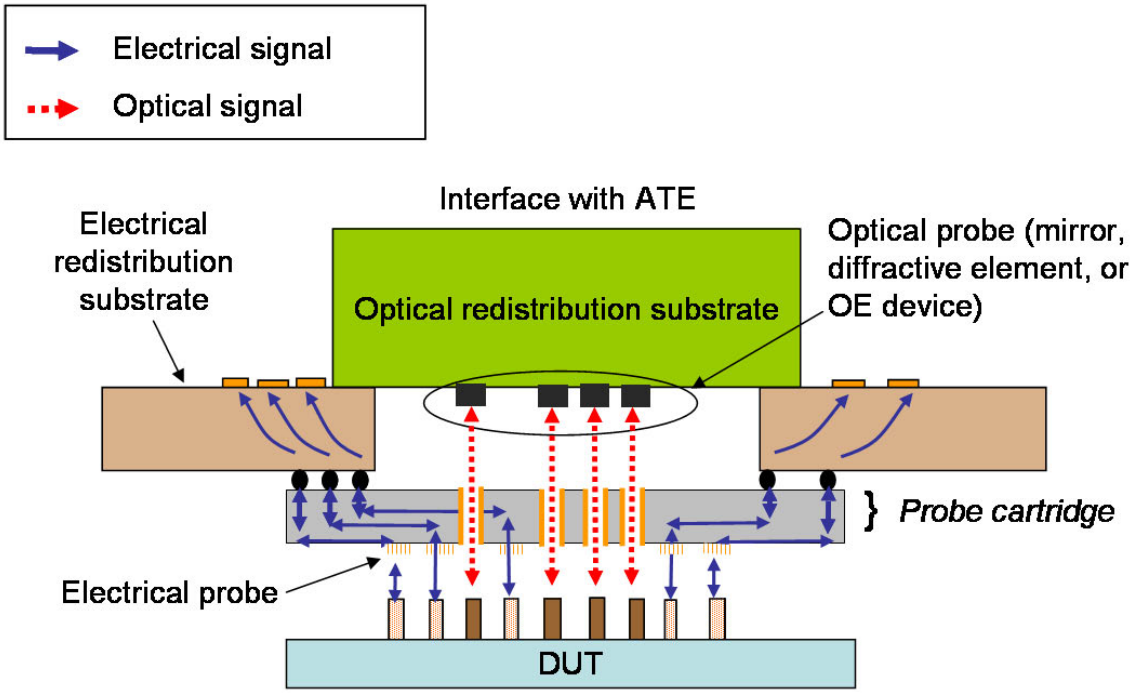


Figure 7.9: Probe module configuration where probing, electrical redistribution, and optical redistribution are implemented on separate substrates. This is a truly modular architecture.

signals to the back-side for connection to the ATE. The design and fabrication of various electrical and optical through-substrate interconnects were described in Chapters III and IV, respectively. The design of probes for contacting pillar-like I/Os is discussed next. This prototype is really at the core of all the different probe module configurations that were described in the previous section.

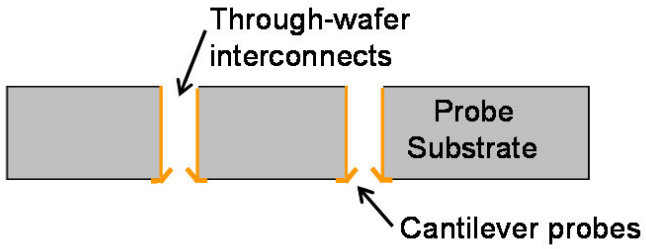


Figure 7.10: Schematic of the bare-bones prototype probe substrate. It is comprised of microsocket probe structures for contacting polymer pillar-based I/O interconnects.

7.3.1 Probe Design

From a probing perspective, contacting polymer pillar-based I/Os presents some unique challenges. Probes used for contacting conventional chip-to-board I/Os, such as solder bumps and die pads, operate by pressing down on the I/O with a predetermined amount of force until good electrical contact is achieved. The applied force can range from a few milligrams to a few grams per contact depending on the type of probe [29–31, 103], the material being contacted, and the age of the probe. Since the basic material in a polymer pillar-based I/O is a soft polymer, applying a large enough force could cause the material to deform permanently leading to creation of pits and defects on the polymer surface. This would certainly have undesirable consequences for optical signal transmission caused, for example, by stray reflections.

A benefit of the high aspect-ratio pillars is that they are mechanically compliant. This compliance assists in keeping the chip attached to the board during thermal cycling. [1]

For example, if a 111 mm^2 chip (CTE_{Si}= 3 ppm/°C) is attached to a typical organic FR-4 printed wiring board (CTE_{PWB}= 17 ppm/°C), then a compliant I/O at the very edge of the die would need to move at least 15 μm for a temperature change (ΔT) of 100°C. As such, the compliant I/O interconnections are designed to achieve at least this required compliance. Unfortunately, during wafer-probing, the I/Os may be forced to deflect beyond this designed range of motion. As a result, under large amounts of lateral strain, pillar-based I/Os could bend or even completely delaminate from the substrate.

Metals are inelastic materials, and exhibit a linear stress-strain relationship only at very low forces. Therefore, when pillars encapsulated with metal are subjected to a vertical or lateral force, they will be prone to some plastic deformation. Polymer pillars (~110 μm tall and ~55 μm wide), both with and without metal, exhibit a vertical displacement-force

[1] The required compliance can be calculated using the equation:

$$\delta = \pm\{(\mathsf{CTE_{PWB}} - \mathsf{CTE_{Si}}) \times \Delta\mathsf{T} \times \sqrt{\mathsf{A_{chip}}}\} \times 10^{-6} \tag{7.1}$$

where CTE_{PWB}= coefficient of thermal expansion of the printed wiring board, CTE_{Si}= coefficient of thermal expansion of the silicon chip, ΔT= change in temperature, and A_{chip}= area of the chip.

ratio between 0.08 – 0.27 μm/mN. The only difference is that in the case of the metallized pillars, the metal begins to deform and wrinkle beyond 10% vertical strain. When a similar set of pillars are subjected to lateral strain, the lateral displacement-force ratios for non-metallized and metallized pillars are 3.01 μm/mN and 1.67 – 2.5 μm/mN, respectively [104]. In conventional flip-chip solder bump interconnects, an additional reflow process step can be used to repair a deformed bump (perhaps damaged during probing) and return it to it's original spherical shape. This is not possible for pillar-based electrical I/Os; therefore, deformed pillars would certainly be a problem during assembly and may result in open connections between the chip and substrate. To avoid these issues, it is *imperative* that the probes be designed to exert minimal force on the polymer pillar I/Os.

The use of SoPP implies the existence of electrical *and* optical I/Os at very high-densities ($> 10^5$ I/Os/cm^2). Even if a small fraction of these are contacted during testing, the electrical and optical signal redistribution requirements on the probe module could be quite challenging.

Conventional contact probes include cantilevers [105] and *buckling-beam* [106] vertical probes (Figure 7.11). The cantilever probes are designed to press down on the chip-level die pad or solder bump I/O. After contact is achieved, the cantilevers are *overdriven* which causes them to slide horizontally across the I/O. This horizontal sliding motion removes any contamination or native interfacial layers. In this way, good contact is achieved [13, 84]. Cantilever probes are mostly used for contacting chips with low I/O counts generally arranged in a peripheral array configuration. On the other hand, buckling-beam probes were invented for contacting area-array I/O interconnects. Buckling-beam probes are essentially springy wires. They are overdriven into the chip I/Os to penetrate any interfacial layers and achieve good contact. The beams *buckle* to absorb any excessive reaction force [13, 106]. From the discussion earlier, it is quite apparent that conventional cantilever and bucking-beam probes would destroy polymer pillar-based I/Os. Even the compliant probes demonstrated in Chapters V and VI would be detrimental to pillar-based interconnects.

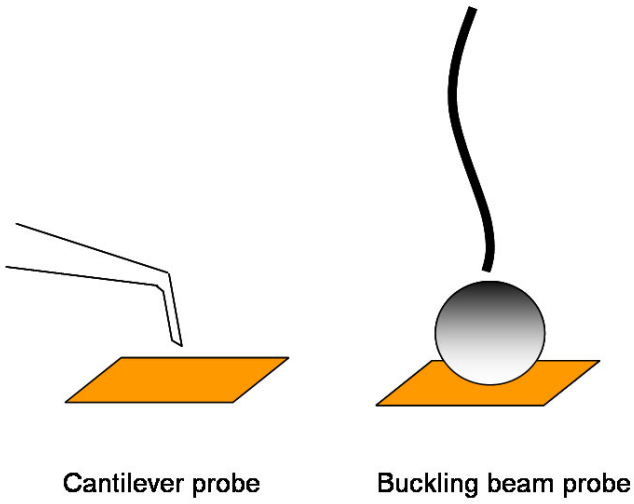


Figure 7.11: Schematics of conventional cantilever and buckling-beam probes.

7.3.2 Contactor Design

As illustrated in Figure 7.1, SoPP is a very versatile I/O interconnect technology. The same pillar-like structure can be used for all-electrical, all-optical, or dual-signal transmission. It would thus be sensible to also design a contact technology to span all pillar-based structures. To ease the process of designing such a universal contact structure, a pillar with metal, only on the sidewalls, was assumed to be the representative target I/O.

The design criteria for the electrical probes are very clear. A low and stable contact resistance is desirable without contacting the pillars from the top or applying too much vertical or imbalanced lateral force. The probes don't necessarily need to contact optical pillars, but some kind of self-aligning mechanism would be helpful to maximize optical coupling to and from the I/O.

With all of the above considerations in mind, each probe on the prototype substrate (Figure 7.10) was designed to resemble a microsocket. It consists of a through-substrate interconnect with inward-facing cantilever probes fabricated at the edge. A cross-sectional illustration of a single probe microsocket is shown in Figure 7.12. During testing, as the pillars are inserted into these sockets, the cantilevers bend to give way, and, in turn, exert

a lateral reaction force on the pillars (Figure 7.13). This force, along with the relative vertical motion between the pillars and the probe substrate creates a vertical sliding contact. Contact between metallized cantilevers and a metal-lined polymer pillar completes an electrical path. For optical I/Os, the cantilevers serve as place-holders that latch on to the sides of a pillar. The aforementioned through-substrate interconnects are used to transfer both electrical and optical signals between the DUT and the redistribution substrate, where multi-level electrical interconnects and optical waveguides with coupling elements could be used to route the signals to the ATE. It is easy to see that this microsocket design leverages the flexibility of the different probe module configurations detailed earlier.

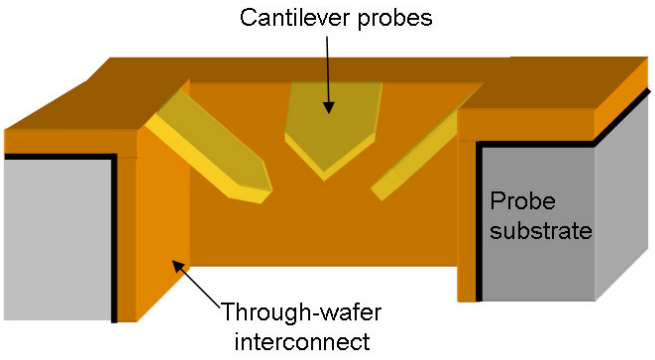


Figure 7.12: Schematic showing cross-sectional view of a single microsocket probe. It consists of cantilever probes over a through-substrate interconnect.

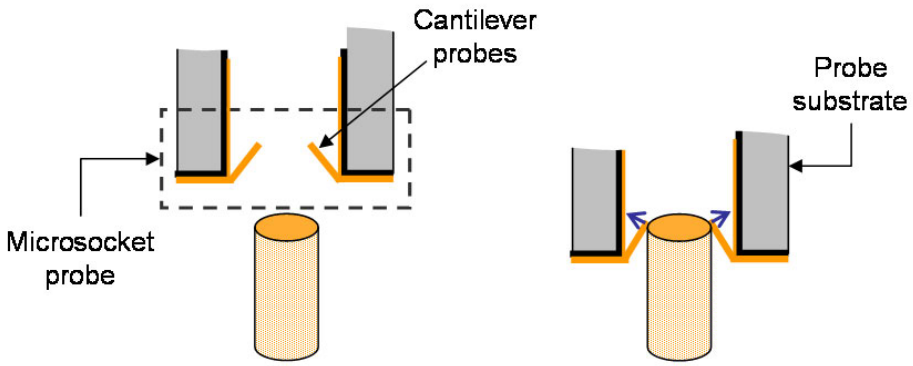


Figure 7.13: Mechanical action of angled cantilever probes during polymer pillar I/O probing.

In Figure 7.12 and 7.13, the cantilevers are intentionally shown to extend downwards at an angle into the through-substrate interconnect. Doing so reduces the amount of flexure stress on the cantilevers. Figure 7.14 (a) shows part of a probe microsocket with a horizontal cantilever probe. The deflection, in [m], of this horizontal cantilever (Figure 7.14 (b)), modeled as a simple beam with one fixed and one free end, can be calculated by the expression [44]:

$$y = \frac{Fx^2}{6EI}(3L - x) \tag{7.2}$$

Here, y= deflection [m], F= applied force [N], x= location of applied force [m], E= Young's modulus [Pa= N/m^2], I= second moment of area [m^4], and L= cantilever length [m]. By re-arranging equation 7.2, the force on the cantilever for a given amount of deflection at the tip (x= L) is given by:

$$F = \frac{3yEI}{L^3} \tag{7.3}$$

The second moment of area, I, of a beam with a rectangular cross-section is given by:

$$I = \frac{1}{12}bh^3 \tag{7.4}$$

where b= beam width, and h= beam height (thickness). Substituting 7.4 into 7.3 gives

$$F = \frac{yEbh^3}{4L^3} \tag{7.5}$$

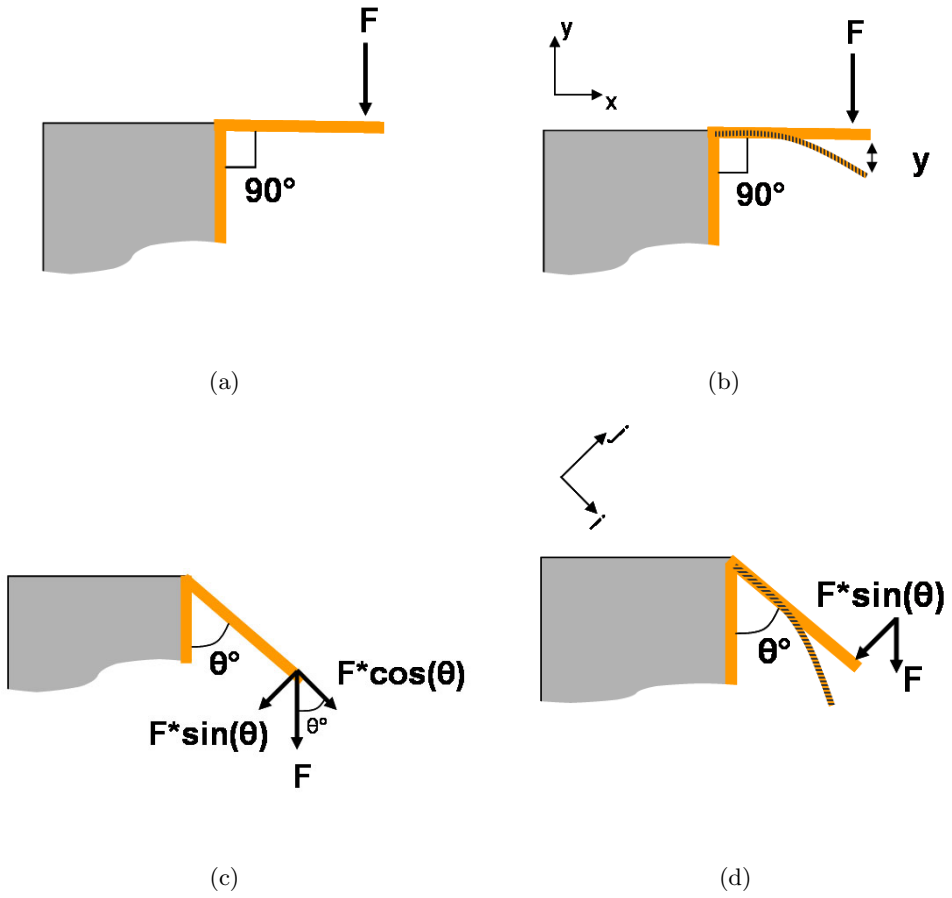
The maximum stress (σ_{max}) in a simple beam of length, L, can be estimated by [44]

$$\sigma_{max} = \frac{6FI}{bh^2} \tag{7.6}$$

Therefore, the maximum stress in a beam, whose tip has undergone a normal (with respect to the stationary beam) deflection, y, is given by the equation:

$$\sigma_{max} = \frac{3}{2}\frac{yEh}{L^2} \tag{7.7}$$

It is interesting to note that σ_{max} is independent of beam width.



(a) (b)

(c) (d)

Figure 7.14: Illustration of (a) a microsocket probe with a horizontal cantilever; (b) bending of a horizontal cantilever; (c) a microsocket probe with an angled cantilever; and (d) bending of an angled cantilever. For an equal tip displacement, angled cantilevers experience a lower maximum stress.

In the case of an angled cantilever, the force component normal to the beam is F.sin(θ) (Figure 7.14 (c)). Thus, for an equal insertion force, F, the force component causing flexure of an angled cantilever is smaller than that for a horizontal cantilever since F $<$ F.sin(θ) (Figure 7.14 (d)). Consequently, for the same amount of deflection, the angled cantilevers are subjected to lower flexure stress, and were therefore selected for the microsocket probes.

In addition, angled cantilevers also enable the vertical sliding contact mechanism with a metallized pillar. For optical pillars, the angled cantilevers behave as guides for self-centering these in the microsockets.

As the microsocket cantilevers will be patterned using photolithography, they can be of virtually any shape and size. A few of these are shown schematically in Figure 7.15. Appropriate processing steps can be selected to yield cantilevers at different angles below the horizontal plane (90-θ in Figure 7.14 (c)).

If the I/Os are also made of a non-tarnishing metal then a pressure contact with a pad on the probe substrate would also suffice to make electrical contact during testing. Figure 7.15 (b) shows a type of pressure contact, where the component on the probe substrate is a metallic receptacle with slanted sidewalls. The slanted sidewalls assist in centering the I/Os in the receptacle. This way, any optical or dual-signal I/Os on the chip would sit directly over a through-substrate interconnect.

Another possible contactor on the probe substrate is shown in Figure 7.15 (c). Here, the cantilevers are made of a soft-compliant material. Essentially, it performs the task of a compliant gripper. When pillar-based I/Os are inserted into these hollow interconnects, the soft sidewalls (cantilevers) compress to facilitate entry of the I/O structure. In doing so, they also press back lightly on the pillars and hold them in place during testing.

Therefore, it is easy to see that there really is an endless number of contact geometries that could be designed to fit within the framework of this MOEMS-based probe module.

7.3.3 Selection of Materials

Material selection for the probes is an integral part of the design process. A cantilever built from a stiff material would not be of much use for probing applications. In general, any material used to build the cantilevers should be highly conductive, non-tarnishing, and must exhibit high fatigue life. Fatigue, a measure of the long-term effect of cyclic loading on a material's performance [107], and stress are among the most common causes of mechanical failure. The cost-performance metric of probe substrates used for wafer-testing dictates that

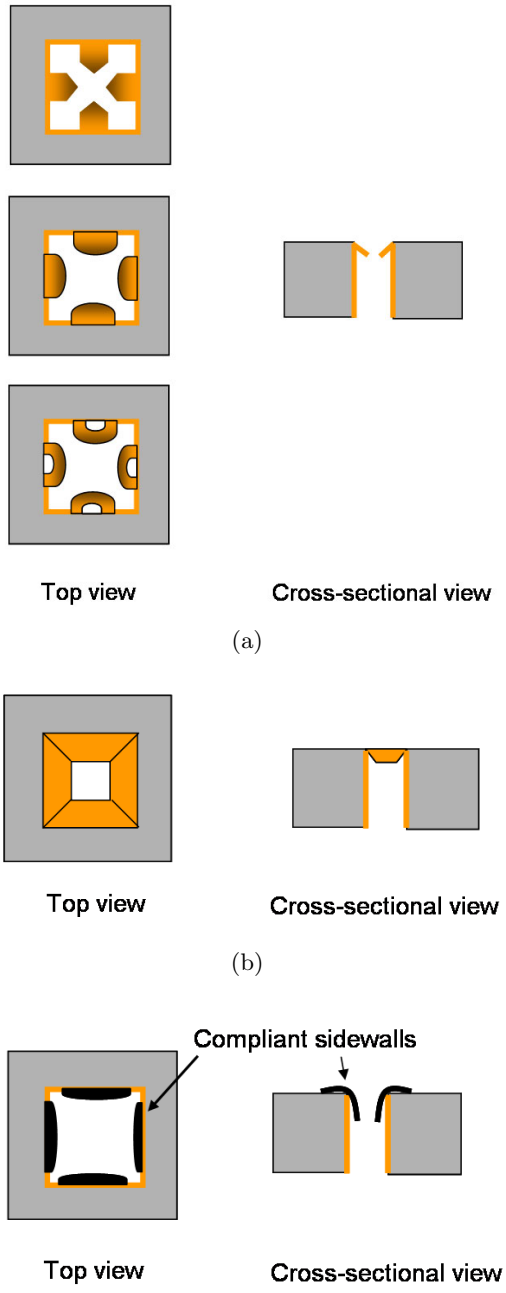


Figure 7.15: Illustration of a few possible microsocket probes. (a) Microsocket having probes of different geometries; (b) Microsocket with a continuous receptacle; and (c) Microsocket with soft compliant sidewalls. The shape and dimensions of the cantilevers can be easily changed by simple modifications during design and fabrication.

the probes ought to withstand hundreds of thousands of touchdowns (mechanical cycles) to the DUT.

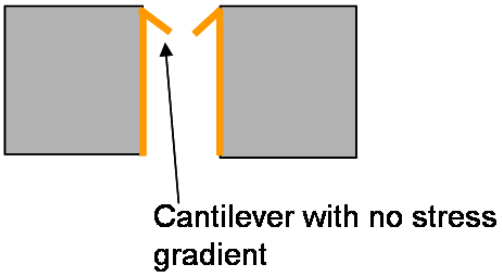
The materials should also be compatible with standard IC and MEMS fabrication processes and temperatures. They should be easy to deposit using methods such as sputtering, evaporation, physical vapor deposition, chemical vapor deposition, electroless plating, electroplating, etc. The list of metals identified in Chapter V as being suitable for the compliant probes are also suitable for microsocket cantilevers (soft gold, nickel, rhodium, beryllium copper, nickel cobalt, palladium cobalt, paliney 7, etc) used to contact electrical I/Os. The mechanical performace of the cantilever probes could be further improved by depositing stressed metal films. The stress in the metal films can be engineered to desired levels by varying the methods and/or conditions of deposition. Specifically, a stress gradient introduced within the metal (along the thickness) during deposition will curl the cantilevers inwards into the through-substrate interconnects (Figure 7.16). This is similar to stressed contactors being built by NanoNexus, Inc [108].

Non-conductive materials having the key mechanical properties listed above could also be used for microsocket cantilevers targeting optical I/Os. Suitable non-conductive materials include Si_3N_4, low-modulus polymers (silicones, polynorbornenes, etc.), and Kapton.

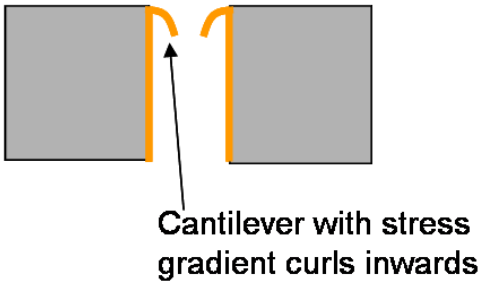
Another option is to build probes using combinations of various materials to achieve the right mix of conductivity, fatigue, low-stress, and compliance. For example, the probes could be formed of a non-conductive material with a low modulus of elasticity, such as polyimide, benzo-cyclo-butene (BCB) or other polymers such as polycarbonates and polynorbonenes. These non-conductive probes could then be metallized with a suitable metal from the list above. However, mixing metallic and plastic materials would make processing harder. In addition, it would also give rise to failure mechanisms owing to physical interactions between neighboring layers.

7.3.4 Prototype Design

A schematic of the prototype probe substrate, built for this work, is shown in Figure 7.10. It was designed to contact an area-array of polymer pillar-based I/Os at a 100 μm pitch. This corresponds to a density of 10^4 probes/cm^2. The ITRS projects a pad pitch of 100



(a)



(b)

Figure 7.16: (a) Schematic showing the cross-section of a cantilever microsocket with no stress gradient in the cantilever material. (b) Schematic showing the cross-section of a cantilever microsocket where a stress gradient has been introduced along the thickness of the cantilever probes. This gradient causes the cantilevers to curl inwards, possibly making them more mechanically reliable than the structure shown in (a).

μm to be reached in 2009, and by the end of the current roadmap, in 2020, area-array pad pitch is predicted to be 70 μm. While the probes on the prototype could be scaled to a 70 μm pitch, a 100 μm pitch was selected as it eased experimentation in research while still demonstrating feasibility for a future technology generation.

The pillars on the DUT were assumed to be 40 μm wide (diameter) with a 60 μm pillar-to-pillar spacing (Figure 7.17). Detailed schematics of the bending cantilevers during pillar insertion into the microsockets are shown in Figures 7.18 and 7.19. The cantilevers extend at a 54.7° angle below the horizontal plane. As a result, the actual length of the arm (l_{cant}) is the projection of the design length (l_{design}). l_{cant} can be calculated using the following expression:

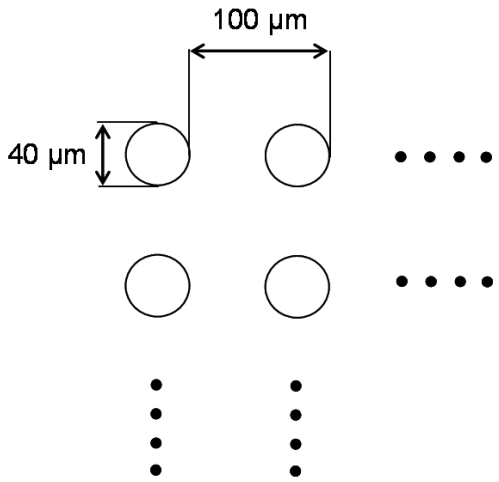


Figure 7.17: Schematic showing the footprint of the target DUT for which the prototype probe substrate is designed. The pillars were assumed to be 40 μm in diameter, and built on a 100 μm pitch.

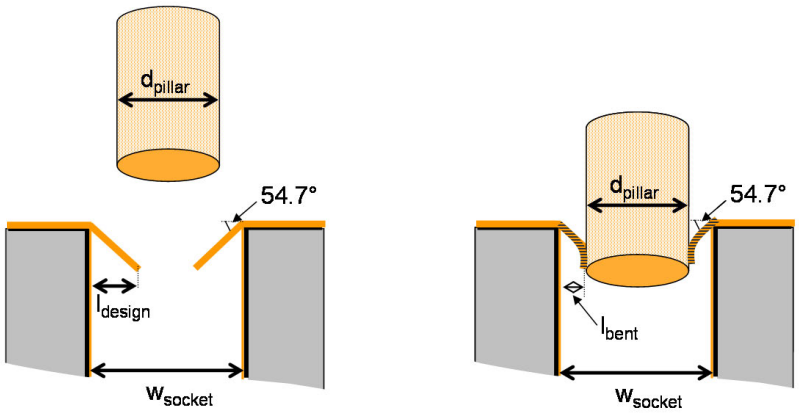


Figure 7.18: Schematic showing bending of the angled cantilevers when a pillar is inserted into a microsocket. The tip of the cantilever is displaced such that l_{design} is reduced to l_{bent}

$$l_{cant} = \frac{l_{design}}{\cos(54.7°)} \approx 1.73 \cdot l_{design} \tag{7.8}$$

Conversely, this equation can also be used to calculate the design length of a feature on a lithography mask that would yield an angled cantilever of length l_{cant}. During fabrication and then characterization, it will be important to know the vertical depth, h_{socket}, of the

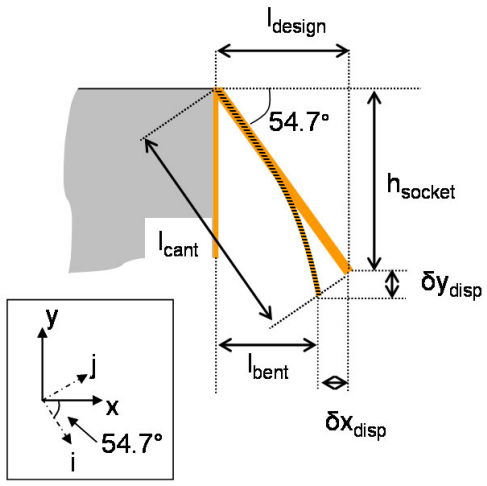


Figure 7.19: Close-up schematic of a single microsocket cantilever. The drawing shows the key parameters used in the design and mechanical analysis of the cantilevers.

microsocket. This can be calculated using the following equation:

$$\mathsf{h_{socket}} = \tan(54.7^{\circ}) \cdot \mathsf{l_{design}} \approx 1.41 \cdot \mathsf{l_{design}} \tag{7.9}$$

As pillars are inserted into the microsockets, each cantilever is displaced to a new location. This is depicted in Figure 7.19. The tip of the cantilever moves closer to the substrate, and l_{design} is reduced to l_{bent}. The difference between these two quantities (in the horizontal plane), labeled as $\delta \mathrm{x}_{disp}$, is a measure of how far the tip of each cantilever moves to accomodate the pillars. Maximum tip displacement of the cantilevers, $\delta \mathrm{x}_{disp,MAX}$, occurs when the center of a microsocket is aligned perfectly with the center of a pillar, and the pillar is completely inserted into the socket. $\delta \mathrm{x}_{disp,MAX}$ can be computed using the expression:

$$\delta \mathsf{x_{disp,MAX}} = \mathsf{l_{design}} - \frac{1}{2}\left(\mathsf{w_{socket}} - \mathsf{d_{pillar}}\right) \tag{7.10}$$

$\delta \mathrm{x}_{disp,MAX}$ for cantilevers of varying design length and due to insertion of pillars of different diameters is tabulated in Table 7.1. In these calculations, w_{socket} was assumed to be 52 μm.

Table 7.1: $\delta x_{disp,MAX}$ for different combinations of values of d_{pillar} and l_{design}. w_{socket} was assumed to be 52 μm.

l_{design} [μm]	$\delta x_{disp,MAX}$		
	d_{pillar}= 20 μm [μm]	d_{pillar}= 30 μm [μm]	d_{pillar}= 40 μm [μm]
10	No contact	No contact	4
15	No contact	4	9
20	4	9	14

7.3.4.1 Design layouts

The mask design for fabrication of the prototype probe substrates was done using Cadence Virtuoso, a computer-aided design (CAD) layout tool. Figure 7.20 shows the cantilever layer of a single microsocket probe. The important design parameters are indicated on this image. To match the footprint of the pillar array (Figure 7.17), the probes were placed in a fully-populated area-array with a probe-to-probe pitch of 100 μm. The width of each microsocket (w_{socket}) was set at 52 μm. Figure 7.21 shows an array of microsockets having the same dimensions. To evaluate the feasibility of fabrication as well as mechanical properties, fifteen such arrays having cantilevers of different dimensions were placed on a single probe substrate die. l_{design} (= {10, 15, 20} μm and corresponding to l_{cant}= {17, 26, 35}) and w_{cant} (= {3, 5, 10, 15, 20}) were varied from array to array but remained the same within each array. Figure 7.22 shows the layout of an entire probe substrate die.

7.3.5 Finite Element Analysis

Finite element models were created using ANSYS [109] to simulate and compare microsocket cantilevers of varying shapes, dimensions, and materials. Figure 7.23 shows an image of the 3D model that was created. Even though the microsocket will have multiple cantilevers, it is likely that during probing they will encounter equal loads (force and displacement). As such, it is sufficient to model a single cantilever. It extends 54.7° below the horizontal plane, and has a pointed tip similar to the design implemented in the CAD layouts. The simulations were repeated for cantilevers of various dimensions. The goal of these simulations was not

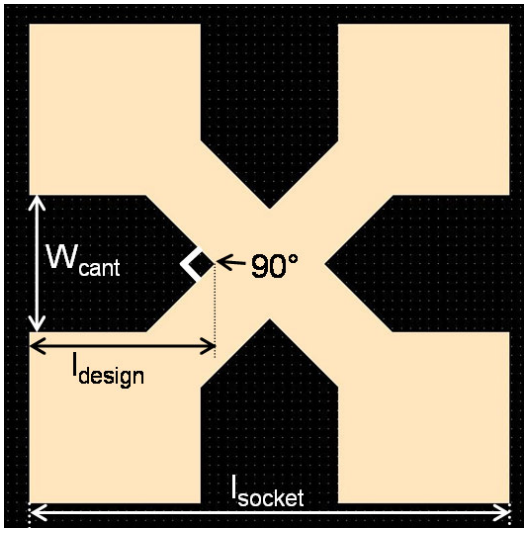


Figure 7.20: Captured image of the physical layout of a single cantilever microsocket. l_{design} and w_{cant} were the key layout parameters. The cantilevers were designed to have a 90° tip. However, this could easily be changed to build cantilevers with rounded tips or any other shape.

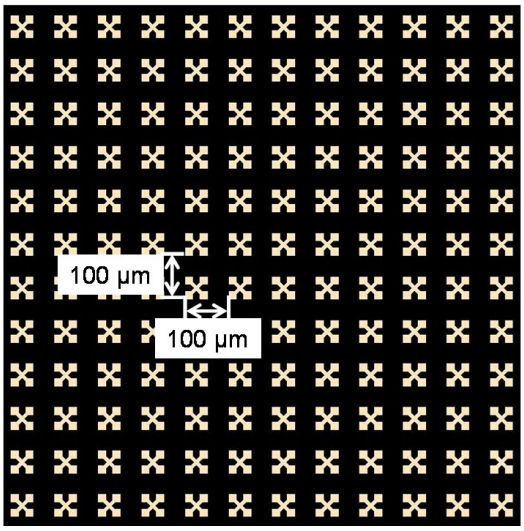


Figure 7.21: Captured image of the physical layout of an array (12x12) of cantilever microsockets. Each microsocket within this array had cantilevers of identical dimensions (15 μm wide $\times$ 20 μm long, in this case). The microsockets were laid out to have a 100 μm pitch, with w_{socket}= 52 μm.

to accurately predict the performance of cantilevers of different dimensions and materials, but rather to observe general trends.

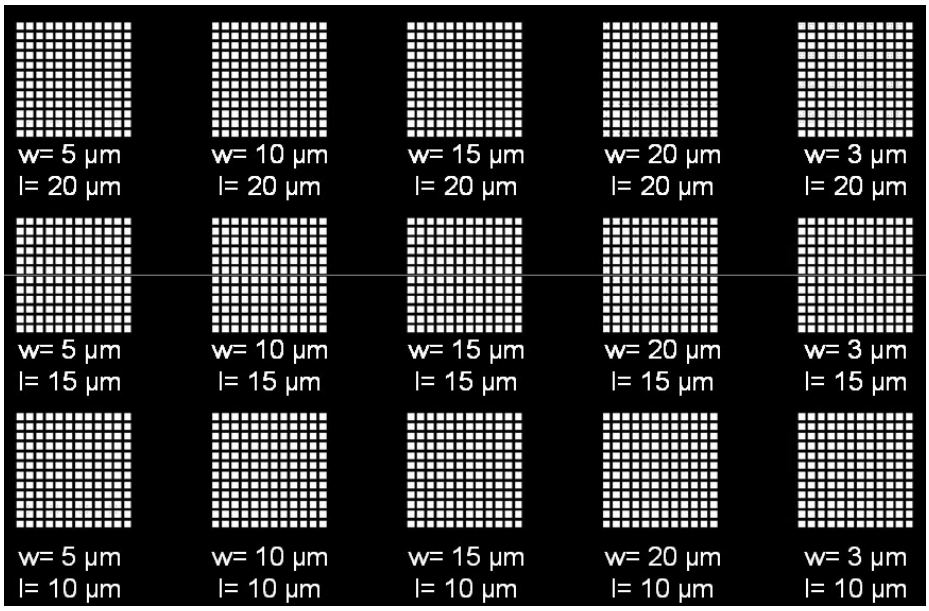


Figure 7.22: Captured image of the physical layout of a single probe substrate die. The design consisted of fifteen separate arrays of microsockets. While the dimensions of the microsocket cantilvers remained the same within a single array, they were varied from array to array.

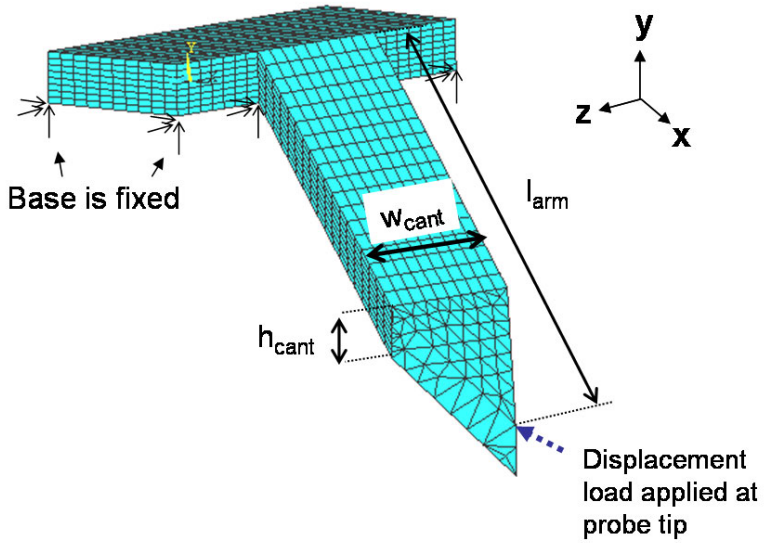


Figure 7.23: Cantilever model created for finite element analysis. During the simulation, the base was fully constrained, and a displacement load was applied at the tip of the cantilever, in the -x direction (inwards, towards the substrate).

Once the model was created, the appropriate boundary conditions were applied to simulate the behavior of the cantilever during pillar insertion. The base, which corresponds to the substrate, was constrained along all degrees of freedom, and a constant horizontal displacement load was applied at the tip of the cantilever (inwards in the -x direction). The applied displacement load was equal to the change in the position of the cantilever along the x axis (δx_{disp}) when contacting a pillar-based I/O.

Figures 7.24 and 7.25 show the deformed shapes of two cantilever designs when a constant displacement load was applied. In the first, the probe was a single-arm cantilever; in the second, the cantilever probe had two load-bearing arms. In both cases, the cantilevers extended out at 54.74° below the substrate surface.

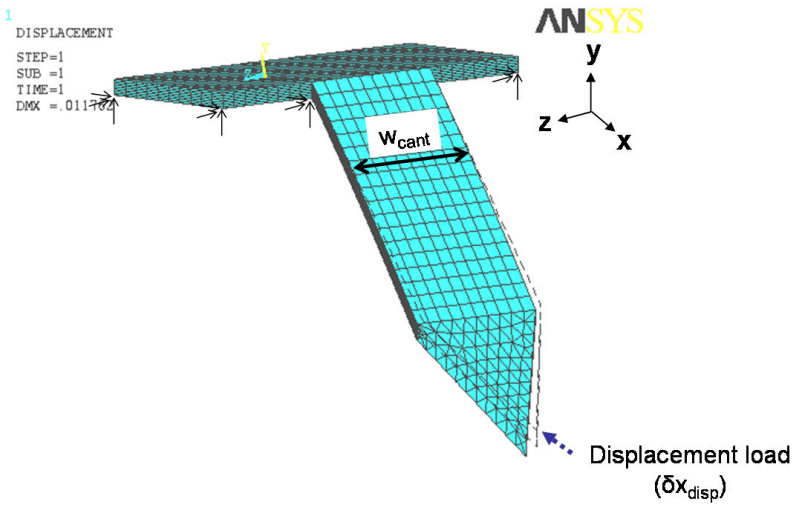


Figure 7.24: Simulated deformed shape of a single-arm angled cantilever of width (w_{cant})= 10 μm, length (l_{cant})= 26 μm, and thickness (h_{cant})= 1 μm when the tip was displaced in the -x direction by δx_{disp}= 9 μm.

The two cantilever designs were simulated in ANSYS. They were assumed to be made of SiO_2 . The width was varied from 3-20 μm and the length from 25-35 μm. While the cantilevers will not be built of only SiO_2, the trends predicted in these simulations are expected to hold for mostly all materials.

Compliance of the cantilevers was calculated by dividing the displacement load by the

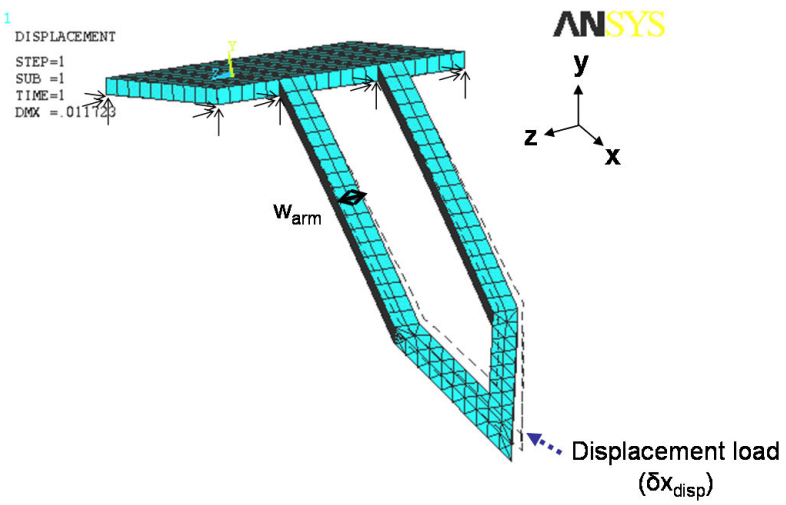


Figure 7.25: Simulated deformed shape of a dual-arm angled cantilever probe of width (w_{cant})= 10 μm, length (l_{cant})= 26 μm, arm width (w_{arm})= 2 μm, and thickness (h_{cant})= 1 μm when the tip was displaced in the -x direction by δx_{disp}= 9 μm.

sum of reaction forces in the x-direction. The simulated stress profiles of the two cantilever designs (Figures 7.24 and 7.25) are illustrated in Figures 7.26 and 7.27. Maximum stress is predicted in regions close to the anchored end of the cantilevers. Average maximum stress was calculated by averaging the stresses on nodes surrounding the node with the maximum stress. Normalized values of compliance and average maximum stress, calculated for single-arm cantilevers of varying sizes, are plotted in Figure 7.28. Compliance increases as probe length is increased or width (w_{prb}) is decreased. However, the average maximum stress in these probes, for all simulated dimensions, did not vary much.

Figure 7.29 shows a plot of normalized compliance and average maximum stress for a dual-arm cantilever, which is 26 μm long and 10 μm wide. It is seen that as w_{arm}, the width of each individual arm, is increased from 1 μm to 4 μm, the compliance decreases, and the average maximum stress remains relatively high. When w_{arm} is 5 μm, which is equivalent to a 10 μm wide single-arm cantilever, the average maximum stress drops sharply. These simulations reveal that, in general, single-arm cantilevers are less compliant and under lower stress than dual-arm cantilevers of equivalent length. The lower stress may be a huge benefit

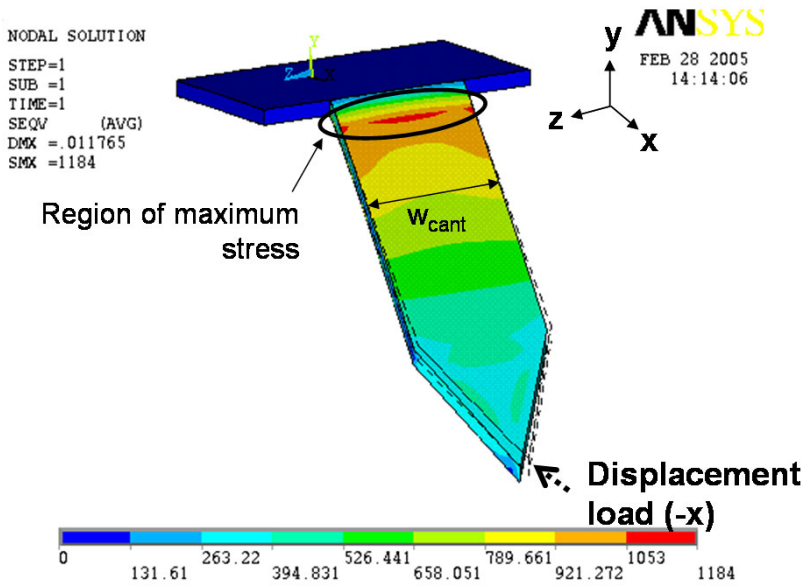


Figure 7.26: Simulated stress profile of a single-arm angled cantilever of width, w_{cant}= 10 μm, length, l_{cant}= 26 μm, and thickness, h_{cant}= 1 μm when a constant displacement load was applied at the tip in -x direction. The region of maximum stress lies close to anchored end of the cantilever.

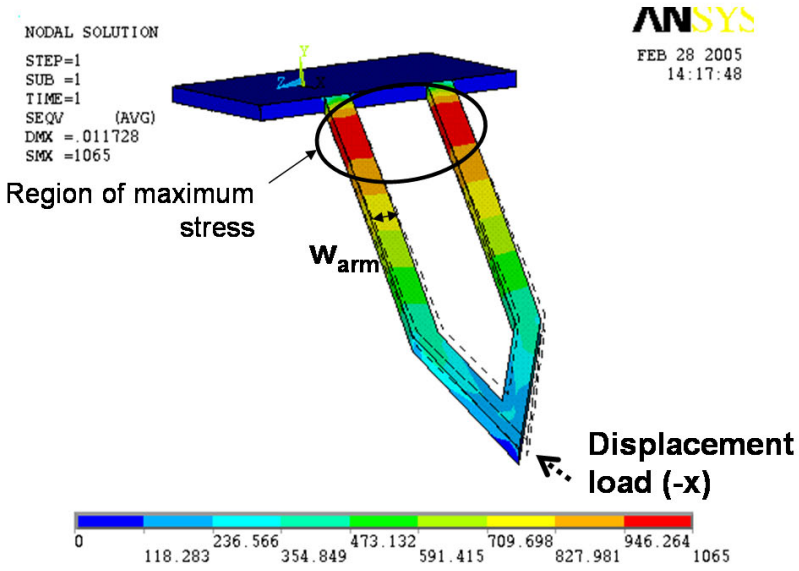


Figure 7.27: Simulated stress profile of a dual-arm angled cantilever of width, w_{cant}= 10 μm, length, l_{cant}= 26 μm, arm width, w_{arm}= 2 μm, and thickness, h_{cant}= 1 μm when a constant displacement load was applied at the tip in the -x direction. The maximum stress appears in both arms near the region close to the anchored end of the cantilever.

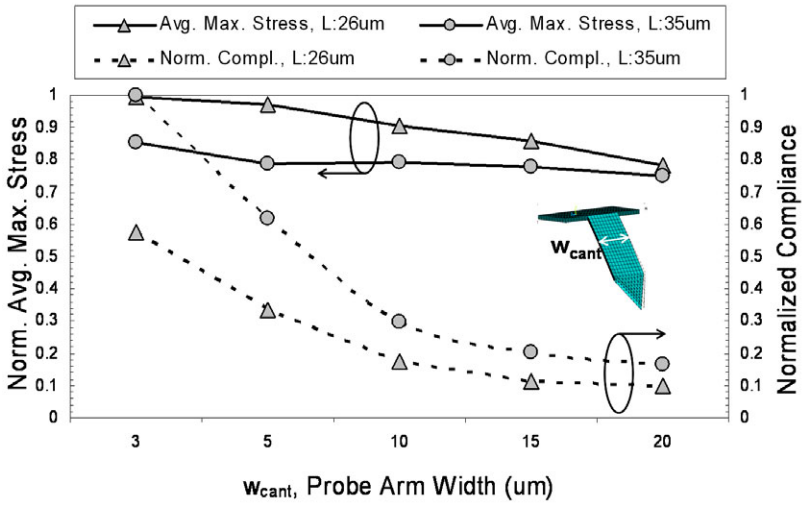


Figure 7.28: Plot of normalized compliance and normalized average maximum stress versus probe width for 1 μm thick SiO_2 single-arm angled cantilever probes. Each curve represents a cantilever of different length as indicated in the legend.

from a probe reliability perspective.

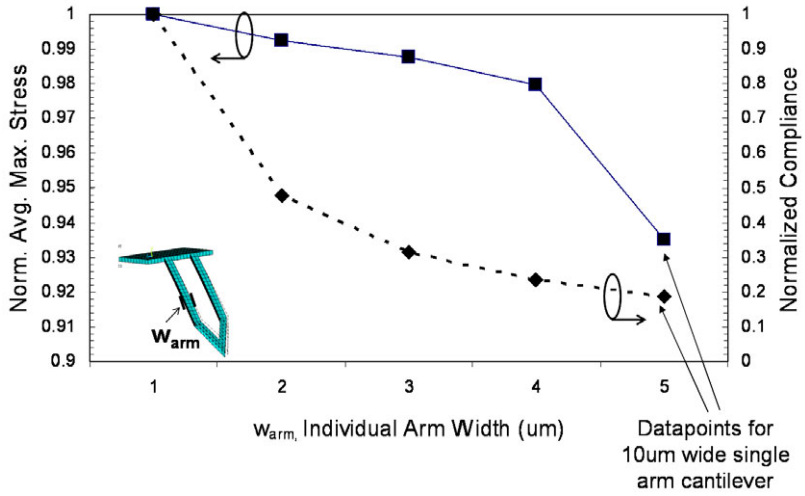


Figure 7.29: Plot of normalized compliance and normalized average maximum stress versus varying individual arm width for a dual-arm angled cantilever probe (total width= 10 μm, length= 26 μm, thickness= 1 μm). At w_{arm}= 5 μm, the dual-arm cantilever is equivalent to a 10 μm wide single-arm cantilever.

The simulations were repeated for single-arm angled cantilevers made of polysilicon, copper, and gold-on-polysilicon. Silicon dioxide and polysilicon display elastic-like properties. As such, they would fracture when the maximum stress in the cantilever exceeds the

ultimate strength of the material. On the other hand, mechanical structures made from metallic materials (i.e. materials displaying plastic-like properties) are typically considered to fail when plastic strain in the structure exceeds 2%.

The normalized compliance of 35 μm long Cu cantilevers of various widths (w_{cant}= 3-20 μm) and thicknesses (h_{cant}= 1-5 μm) is plotted in Figure 7.30. Once again, compliance increases with decreasing thickness and decreasing width. In effect, it can be said that compliance is inversely proportional to the cantilever cross-section area.

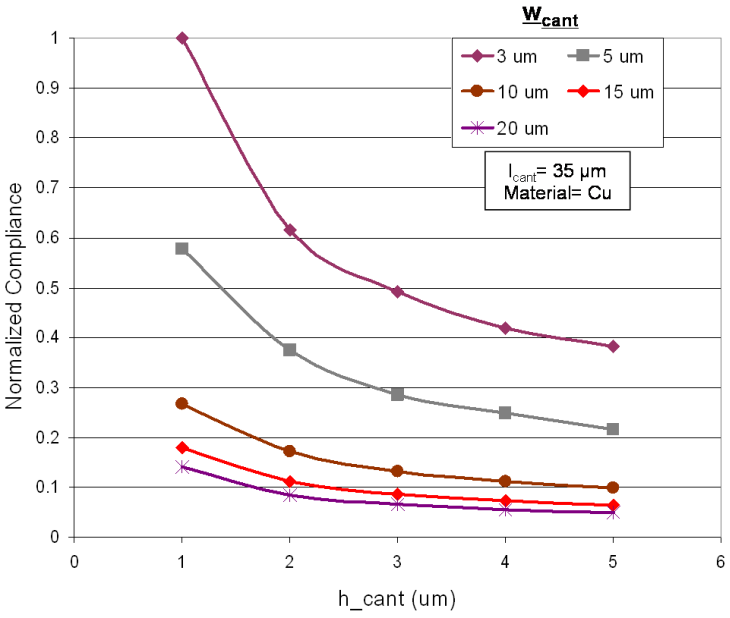


Figure 7.30: Plot of simulated normalized compliance of copper cantilevers versus cantilever thickness. The multiple curves correspond to cantilevers of varying width as indicated in the legend. The length of the cantilever was kept fixed at 35 μm.

Figure 7.31 plots the average maximum stress in gold-on-polysilicon cantilevers (l_{cant}= 35 μm, w_{cant}= 15 μm) of varying thickness. Multiple curves, corresponding to different values of x_{disp} are also shown on this chart. Stress increases as h_{cant} increases. Also, from the multiple curves it is apparent that stress also increases uniformly for an increase in the displacement load.

The normalized compliance of cantilevers with the same dimensions and loading conditions, but made of different materials (silicon dioxide, copper, and gold-on-polysilicon),

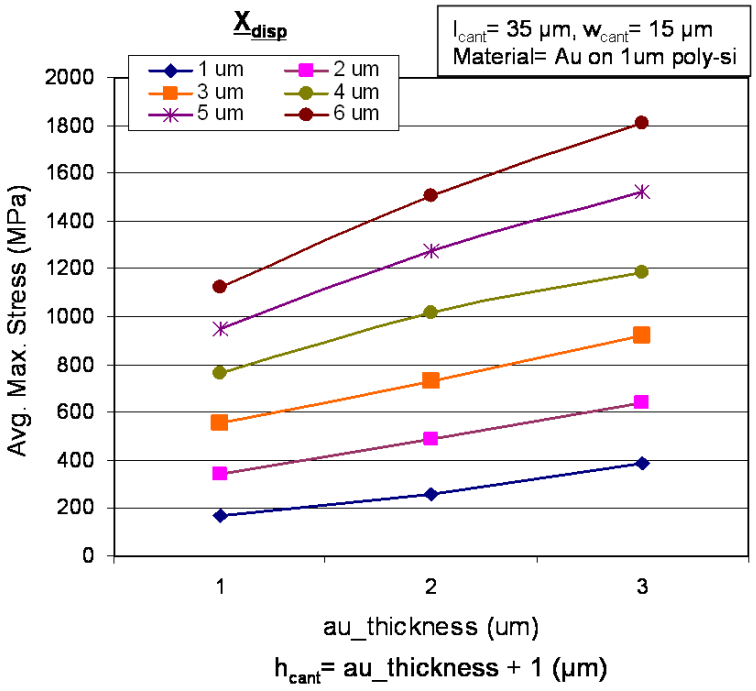


Figure 7.31: Plot of average maximum stress cantilevers versus cantilever thickness. In the simulation, the cantilevers were made of varying thicknesses of gold on 1 μm of polysilicon. The multiple curves correspond to different displacement loads (x_{disp}). The length and width of the cantilever were kept fixed at 35 μm and 15 μm, respectively.

is plotted in Figure 7.32. As expected, the compliance of the SiO_2 probes is much higher (since it exhibits elastic properties) than the metal-based structures. The average maximum stress in these very same cantilevers is plotted in Figure 7.33. Here, the copper cantilever exhibits the lowest stress, whereas the silicon dioxide and gold-on-polysilicon cantilevers are under larger amounts of flexure stress.

Finite element simulations are an effective way of estimating cantilever performance prior to fabrication and testing. These structural simulations could be extended much further to optimize the design as well as the materials that ought to be used. However, this is left for future work.

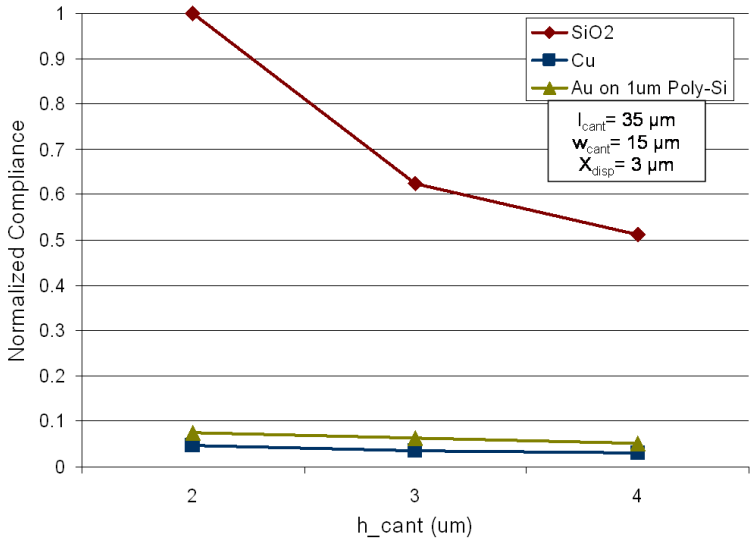


Figure 7.32: Plot comparing compliance of cantilevers made from three different materials – silicon dioxide, copper, and gold-on-polysilicon.

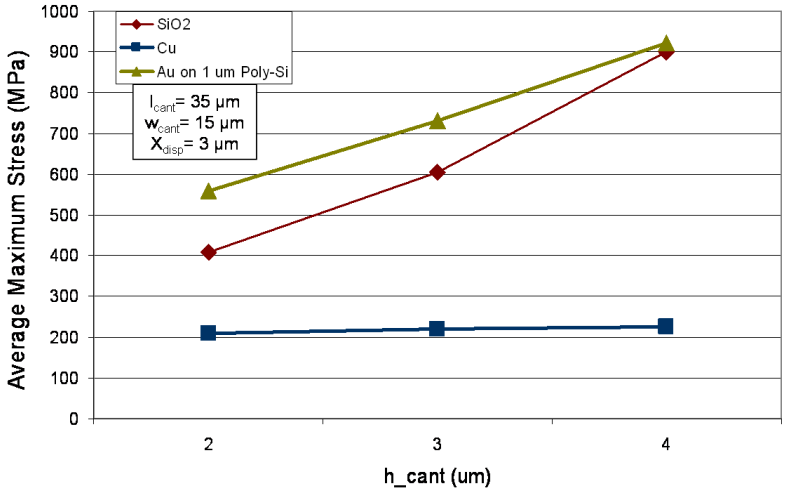


Figure 7.33: Plot comparing average maximum stress in cantilevers made from silicon dioxide, copper, and gold-on-polysilicon. The plotted data is for a displacement load, x_{disp}, of 3 μm applied at the tip of the cantilevers, which were 35 μm long and 15 μm wide.

7.4 Conclusion

The final structure of an optical I/O and the architecture of an OE-GSI chip that would be used in future gigascale chip-based systems is currently still a topic of research. Various probe module configurations for interfacing such chips having polymer pillar-based electrical

and optical I/Os were proposed in this chapter. The pillar-based I/Os are assumed to be representative of high-density electrical and guided-wave optical I/Os in future GSI chips. The design of the probe modules can be customized depending on the purpose of the test and the available test equipment. Specifically, the design of a prototype probe substrate was also discussed. This prototype consists of microsocket probes that are designed to make a vertical sliding contact with the pillar-based I/Os of the DUT. The mechanical performance of the cantilevers can be estimated by using simple static beam equations or by finite element analysis.

A prototype probe substrate with gold-on-polysilicon microsocket cantilever probes was successfully built. Details of the fabrication process as well as the specifics of experiments done to demonstrate successful probing of an area-array of electrical and optical pillar-based I/Os are described in subsequent chapters.

CHAPTER VIII

MOEMS PROBE SUBSTRATE: FABRICATION

8.1 Introduction

The construction of prototype probe substrates, consisting of through-substrate interconnects and angled cantilever probes (Figure 7.10), is described in this chapter. The probe substrates were built on silicon using microfabrication techniques.

The cantilever probes can be built from a variety of materials. Here, the cantilevers were made of a material stack consisting of gold/titanium/doped-polysilicon/SiO_2/doped-polysilicon (variable/30 nm/1 μm/0.5 μm/1 μm). For shorthand, this will be henceforth referred to as gold-on-polysilicon. The Ti layer served as an adhesion layer between Au and poly-Si; the SiO_2 layer, about 0.5 μm thick, was enveloped in the doped-polysilicon. Polysilicon is a popular material used in MEMS. As such, there is a vast amount of know-how on the mechanical properties as well as processing techniques (deposition and etching) for poly-Si . In addition, boron- or phosphorus-doped poly-Si is a conductive material that is compatible with CMOS processing – an important consideration as a number of processing tools in the Georgia Tech MiRC cleanroom needed for micromachining the probe substrates only allow CMOS-compatible (that is, no metals) samples. Gold is a noble metal and does not tarnish. Therefore, using it simplifies electrical-probing characterization. Also, since it was deposited as the very last step in the fabrication process, it does not violate any tool-related requirements.

The fabrication of prototype probe substrates with Au/Ti/poly-Si/SiO_2/poly-Si cantilevers is first described in this chapter followed by a fabrication procedure to build probes of only Au/Ti/poly-Si. Prototypes built using the former method have been characterized, and the details are described in the following chapter.

8.2 Prototype Fabrication Process

The prototype probe substrate was built on a 400 μm thick, double-side polished Si wafer. The probes were fabricated at a 100 μm pitch; varying in length from 15 μm to 35 μm, and in width from 3 μm to 20 μm. The process detailed below describes one way of fabricating the prototype probe substrate. The through-wafer interconnects were lined with doped-poly-Si, and the cantilevers were made of gold-on-polysilicon (Au/Ti/polysilicon/SiO_2/polysilicon). In the process flow that is described first, the polysilicon envelopes a thin film of SiO_2(Figure 8.1). A simplified process flow, depicting only the major process steps, is shown in Figure 8.2. However, in actuality, the entire procedure required more than sixty microfabrication processing steps.

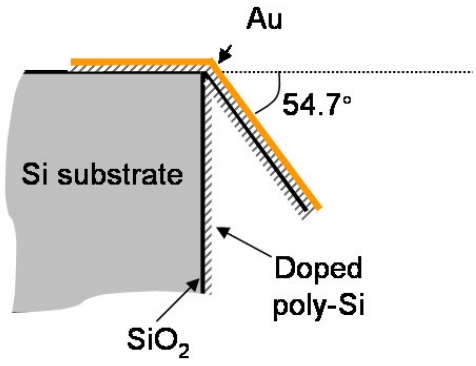


Figure 8.1: Schematic of a single microsocket cantilever that was fabricated. A doped-poly-Si lining on the microsocket through-wafer interconnect makes it conductive. The cantilever was made of a stack of gold-on-polysilicon; the polysilicon encases a thin film of SiO_2.

8.2.1 Si Micromachining

The first step in the process was to clean a (100) oriented, double-side polished Si wafer by rinsing in acetone, methanol, and isopropanol, successively. Any trace amount of native oxide was removed by a brief etch in BOE solution. The wafer was thoroughly rinsed in DI water and dried in nitrogen. A number of tools used for building the probe substrate require the samples to be CMOS-friendly. As a result, the wafer was handled using polyetheretherketone (PEEK) tweezers.

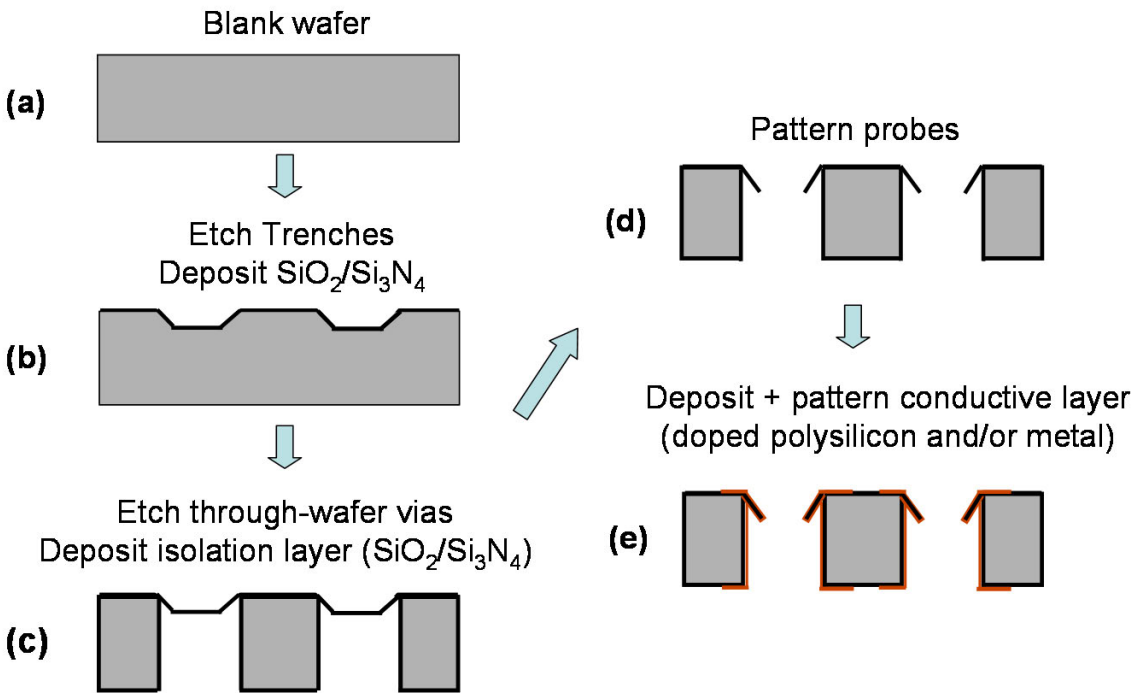


Figure 8.2: Fabrication process for a prototype probe substrate with cantilevers made of gold-on-polysilicon. The major steps in the process included etching trenches which would help define the angled cantilevers (b); etching through-wafer vias from the wafer backside (c); photolithography and etching of the thin-film membrane to yield inward facing cantilevers (d); and deposition and patterning of a conductive film on the sidewalls of the through-wafer vias, and the released cantilevers.

The first set of process steps were used to etch trenches with angled sidewalls in the silicon substrate. 4000Å of Si_3N_4 was deposited on both sides of the wafer using PECVD (see Appendix A). Following this, 5 μm of Futurrex NR9-8000 negative photoresist was spun onto one side of the probe substrate. The resist was photolithography patterned with the first mask to yield an array of square vias 52-64 μm wide. Following a short descum process in the RIE, the nitride in the exposed regions was etched away by plasma etching in the RIE (for processes, see Appendix A). The descum process assures that no trace amounts of undeveloped resist remains in the developed regions. The Plasma Therm RIE in the MiRC cleanroom is a multi-user, general-purpose etcher. The etching of Si_3N_4 was observed to be very sensitive to the RIE chamber conditions. Therefore, a long clean process was typically run prior to Si_3N_4 etching. Visual observation as well as thickness measurements using the

Nanospec film analzyer was used to determine if the nitride was completely etched. The photoresist was removed by rinsing in Acetone.

Anisotropic trenches, ~25 μm deep, were etched in the Si wafer using 25% tetramethyl ammonium hydroxide (TMAH) solution. The wet etch bath shown schematically in Figure 4.34 was used for this purpose. As was described in Chapter III, TMAH etches Si anisotropically along the (111) plane to yield trenches with 54.74° sidewalls (Figure 8.3). The patterned Si_3N_4 serves as an etch mask for this process. The Si_3N_4 was removed by wet etching in a buffered oxide etch (BOE) solution, and 1 μm of PECVD SiO_2 was deposited on the trench-side of the wafer surface (Figure 8.2 (b)). This oxide layer will serve as an etch stop for the forthcoming through-wafer via etch. It is also one of the structural materials used for the cantilever probes. A thinner layer of oxide could be used. A variation of this fabrication process that eliminates the SiO_2 from the cantilever material stack is described later.

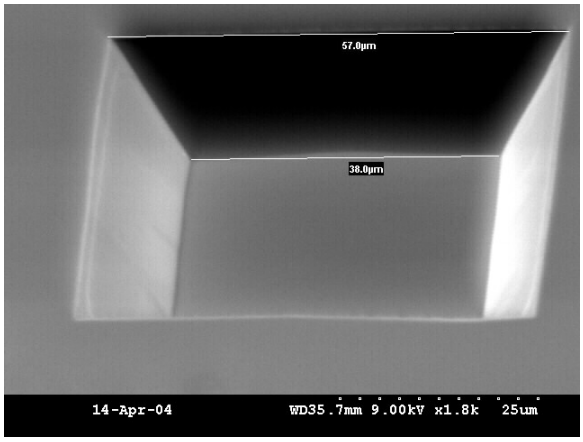


Figure 8.3: SEM image of a single trench etched in Si using TMAH.

The next set of process steps was used to etch through-wafer vias in the Si substrate. The vias were etched from the back-side of the wafer. SiO_2 is very resistant to the Bosch process etch; therefore, the wafer is first dipped in BOE solution very briefly to remove any bit of native oxide that might have formed on the wafer back-side (the side without the trenches). A 10 μm layer of Futurrex NR5-8000 negative photoresist was spun onto the

back-side of the wafer, and vias, aligned to the trenches on the front-side of the wafer, were patterned in the resist. This lithography step required back-side alignment. The EV-620 as well as the MA-6 lithography tools in the MiRC cleanroom both have this capability.

Following photoresist development, the wafer was mounted onto a dummy Si wafer using *cool grease*. [1] The vias were etched in a Si deep reactive ion etcher (DRIE) configured to run the Bosch process. On completion of the DRIE process, a suspended SiO_2 membrane remained over the through-wafer vias (Figure 8.2(c)). Since the bottom of the via was not a planar surface (owing to the trench created in the previous steps), when the bottom of the trench was reached, notching began to occur, and the rate of lateral etching increased. Figure 8.4 shows an SEM image of a TWV where notching led to widening of the via around the trench. Figure 8.5 shows an image of the wider via underneath the trench (the images were taken while looking down on the wafer with the trench-side up).

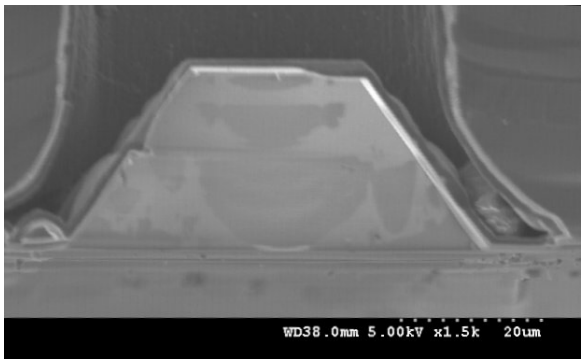


Figure 8.4: SEM image of a TWV above (under) a trench. The non-planar etch stop layer causes notching to begin before the via has been etched all the way through the wafer. As a result, the via is no longer vertical near the trench, but rather has a wider base.

The wider base affects the final cantilever structure in that the cantilever arm is no longer supported by the substrate. To avoid this, once the bottom of the trench is reached, great care ought to be taken to complete the rest of the via etch by running the Bosch

[1] This is necessitated for two reasons. First, in the STS ICP, helium (He) gas impinges on the back-side of the wafer to minimize substrate heating. However, since the trench-side of the wafer faces the bottom during the TWV etch, the leak-up rate of He exceeds the recommended range of values, which is detrimental to the etch process. Second, as the vias are being etched all through the wafer, if the oxide etch stop develops micro-cracks, then the entire wafer could crack.

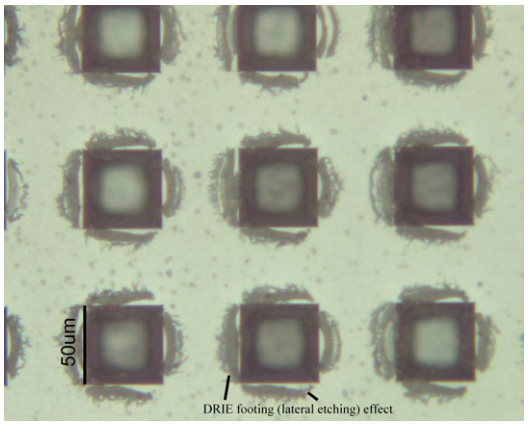


Figure 8.5: Microscope image of a trench and the TWV underneath. Owing to notching, the silicon regions around the trench have been etched away. Like in the center of the trench, there is no silicon remaining underneath these regions, and so they appear dark underneath the white light of the microscope.

process for shorter intervals (therefore, smaller increments of Si are etched). As SiO_2 is a transparent film, holding the substrate up against a light is a quick and easy way of knowing whether the via has etched down to the oxide film in the trench. A low-frequency (380 KHz) Bosch process, as described in [48], may also be useful to avoid notching.

While Acetone or RR4 resist remover (from Futurrex) are recommended for resist stripping, the long DRIE etch renders these methods of resist removal ineffective. Instead, the NR5-8000 was easily removed by dry etching with an oxygen plasma in the RIE. The substrate was then put through a CMOS clean procedure, which included a piranha clean, a DI water rinse, a short BOE dip, another DI water rinse, and spin-rinse drying. This procedure removes the fluorocarbon polymer deposited on the wafer and on the via sidewalls during the Bosch process and any trace amounts of photoresist that may still be there. Next, a thermally grown SiO_2 film was formed everywhere as an isolation layer. The oxide grows everywhere on the exposed silicon, and also on the oxide film on the trench-side of the wafer, albeit at a much slower rate. Understandably, no oxide grows on the suspended SiO_2 membrane itself. LPCVD Si_3N_4 can also be used for the isolation.

8.2.2 Cantilever Definition

The next step in the process was to pattern the SiO_2 membrane in the shape of the cantilevers. This was challenging as it involved transferring a 2D pattern onto the angled sidewalls of a 3D structure. Figure 8.6 shows a schematic of the lithography step.

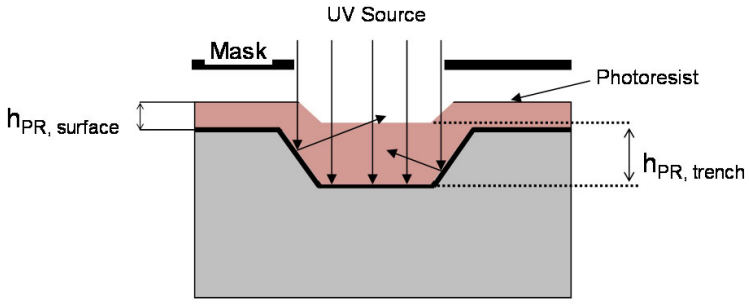


Figure 8.6: Schematic of lithography in a 3D structure. The angled sidewalls tend to reflect the incident UV light. If the resist is too thick, then unwanted regions of the resist will get exposed.

Ideally, it is desirable to have a conformal coating of photoresist with good adhesion to the underlying layer in the trench-shaped membrane. This can be quite hard to achieve using regular spin-on photoresists especially if the trench is deeper than a couple of microns. Spin-on photoresists have a general tendency to fill up the trench as shown in Figure 8.6. If the resist at the center of the trench is too thick, then UV light will reflect off the angled sidewalls and expose, and thus crosslink, the central region, which is highly undesirable. An SEM image of this phenomenon is shown in Figure 8.7.

Conversely, if the resist is spun-on at a higher speed (i.e. to achieve a thinner layer), it will be thinnest at the knee of the trench. This is illustrated in Figures 8.8 and 8.9. Following photolithography, an etching process is used for removing the underlying materials not protected by the photoresist. However, if the resist is not very selective to the etch, then a thin layer at the trench knee would likely fail to provide adequate protection.

Good adhesion between the photoresist and the trench structure was also essential to the process. Figure 8.10 shows an SEM image of cantilevers that were successfully patterned

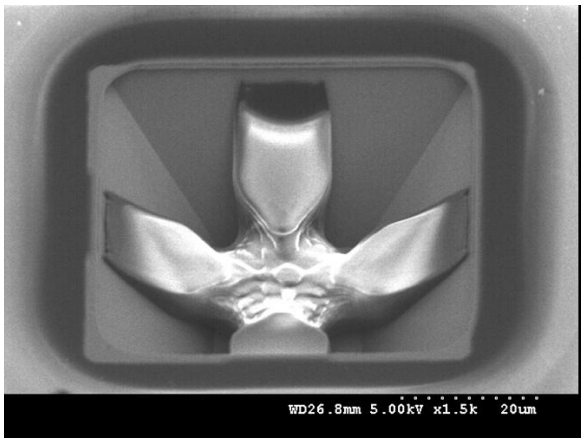


Figure 8.7: SEM image of unsuccessful photolithographic patterning of a 3D structure. It was concluded that reflections off the sidewalls probably converged in the central portion of the resist causing it to be also exposed. As a result, the regions betweeen the cantilevers did not dissolve away in the developer.

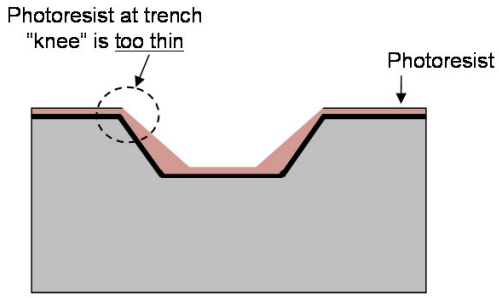


Figure 8.8: Schematic of photoresist profile in a trench when it was spun-on too fast. By doing this, very thin coverage is achieved at the knee of the trench.

but had poor adhesion to the trench sidewalls. The delaminated photoresist would lead to severe undercutting of the underlying material during etching. Therefore, the patterning shown in Figure 8.10 was unacceptable.

Electrophoretic resist, which can be electroplated onto a substrate, has been recommended for photolithographic patterning of 3D structures [110–112]. However, since electrophoretic resist was not available, a set of optimization experiments was carried out to achieve a photoresist application process that not only provided as conformal a layer in

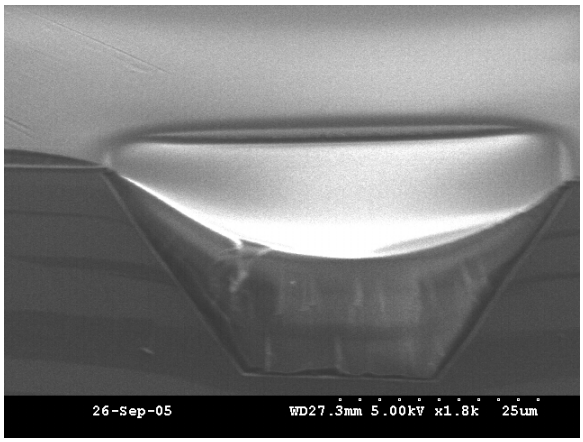


Figure 8.9: SEM image of photoresist profile in a trench when it is spun-on too thin. Very thin coverage is achieved at the knee of the trench.

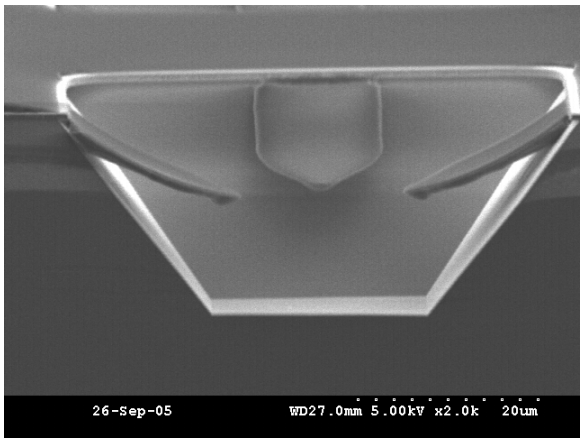
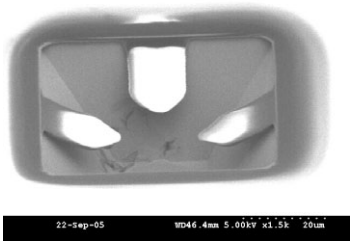


Figure 8.10: SEM image of cantilevers patterned in the photoresist that have lifted-off from the trench sidewalls owing to poor adhesion. Even the photoresist structures have a uniform thickness, the poor adhesion makes this result unacceptable.

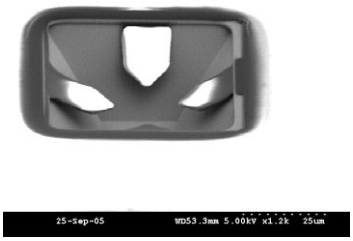
the trench as possible, but also had good adhesion to the trench sidewalls. Both, negative (Futurrex: NR9-8000, NR9-1500P, NR9-1500PY, NR7-1500P) and positive (Shipley: SC1827) photoresists were considered. The spin-speed of the photoresists and the soft-bake parameters (time, temperature, and tool) were the primary variables in this experiment. The details of the different trials in this experiment are summarized in Table 8.1. Figure 8.11 shows SEM images for each of these.

Table 8.1: Summary of process parameters used for evaluation and optimization of spin-on photoresist application inside a trench with angled sidewalls.

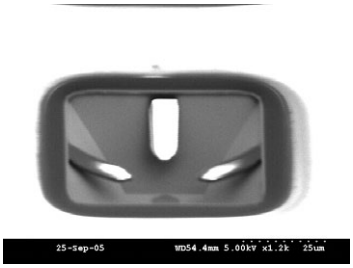
			Soft Bake					
Resist	Samp. #	Spin Rec.	Time	Temp.	Tool	$h_{surface}$	h_{trench}	Observation
		[rpm]/[rpm/s]/[s]	[mm:ss]	[°C]		[μm]	[μm]	
NR9-1500PY	922-2	1000/500/40	1:30	110	Oven (inverted)	4.3	18.41	PA
	923-1	1000/500/40	1:30	110	Oven	4.2	14.87	PA
	923-2	1000/500/40	1:30	100	Hot-plate	3.57	13.88	PA
	927-2	4000/500/40	1:00	150	Hot-plate	1.55	7.55	PA; TaKn
NR9-8000	124-1	5000/1000/50	2:00 2:00	110 130	Hot-plate Hot-plate	5.7	18.1	Not dev.
NR9-1500P	124-1	5000/500/40	1:00	150	Hot-plate	0.8	6.95	Dev.; TaKn
SC1827	926-2	5000/500/40	2:30	110	Oven	3.17	31.19	Memb.
NR7-1500P	927-5	1000/500/40	5:00	110	Oven	3.70	15.94	Not dev.
	927-6	4000/500/40	1:00	150	Hot-plate	1.97	9.87	Dev.; NC
	928-1	**2000/500/40**	**1:30**	**110**	**Oven**	**2.24**	**10.18**	**GA; GD**
PA= Poor adhesion; TaKn= Thin at trench knee; Memb.= Membrane; Dev.= Developed								
NC= Not cleared; GA= Good adhesion; GD= Good definition								



(a) NR9-1500PY: 922-2

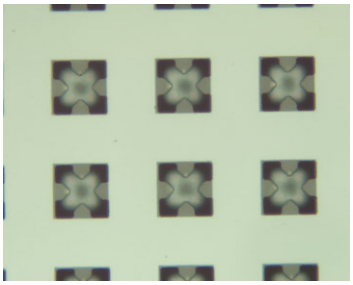


(b) NR9-1500PY: 923-1

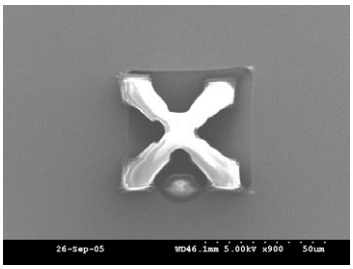


(c) NR9-1500PY: 923-2

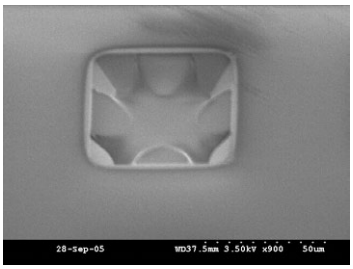
(d) NR9-1500PY: 927-2



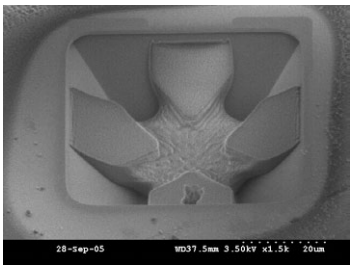
(e) NR9-8000: 124-1



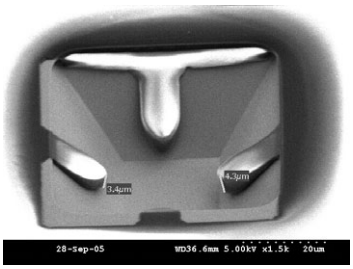
(f) SC1827: 926-2



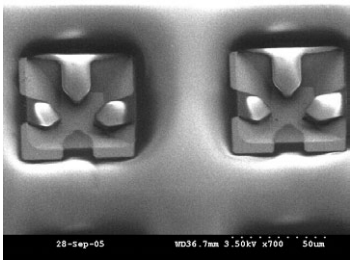
(g) NR7-1500P: 927-5



(h) NR7-1500P: 927-6



(i) NR7-1500P: 928-1



(j) NR7-1500P: 928-1

Figure 8.11: Images showing lithography in a trench. The corresponding process details for each image are summarized in Table 8.1

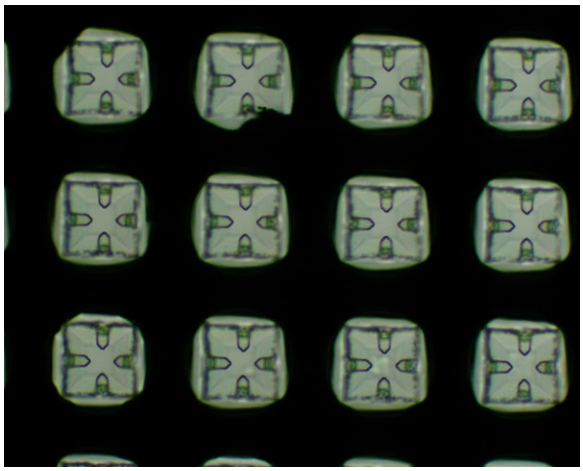
NR9-1500PY is a low-viscosity negative resist, and gave acceptable results *most* of the time. It's biggest problems were adhesion to the trench material and repeatability of the process. Upon further experimentation, NR7-1500P was found to provide the best combination of etch selectivity, adhesion, and resolution (Figures 8.11 – (i) and (j)). Figure 8.12 shows images of cantilevers photolithographically patterned over a membrane. A light source at the bottom of the substrate was used to illuminate this sample. As expected, light only passed through the through-wafer vias. The edges of the via appear slightly jagged and undercut owing to notching.

8.2.3 Membrane Etching and Thin-film Deposition

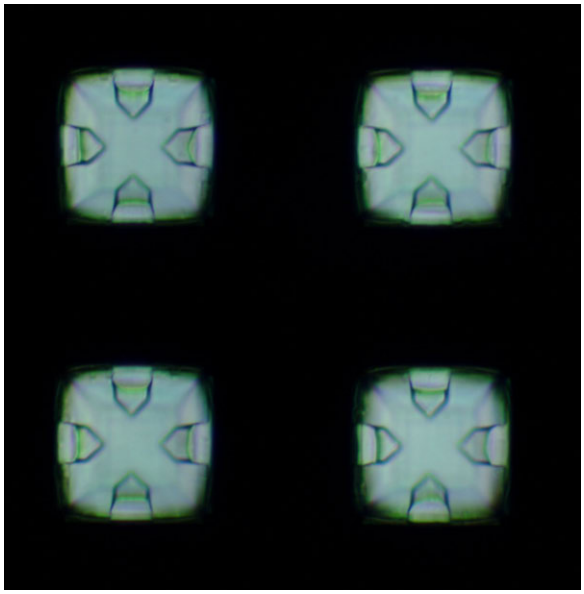
Once the cantilevers were successfully patterned in the (negative) photoresist, the exposed SiO_2 layer underneath was etched away in an ICP-RIE tool (see Appendix A for process). Figure 8.13 shows images of microsocket probes after SiO_2 membrane had been etched away.

The resist was removed by an RIE descum process (Figure 8.2 (d)). At this time, released angled cantilevers remained over the through-wafer vias. The substrate was once again cleaned in a piranha solution, and then made conductive by depositing a thin film ($\sim$1 μm) of LPCVD polysilicon (Figure 8.2 (e)). The polysilicon was diffusion-doped using a phosphorus source (Techneglas TP-470) to make it n-type. The doping was done for 90 minutes at 1050°C. The sample was then annealed for 45 minutes. Using a 4-point probe, the typical resistivity of the polysilicon film was measured to be around 1.3Ω-cm. Successive lithography and etch steps could now be done on both sides of the wafer to isolate the microsockets from each other. This was not imperative for the characterization of the probes that needed to be done at this stage.

This concludes the probe substrate fabrication. Figures 8.14 and 8.15 show images of the fabricated probe substrate. As the cantilevers are defined by photolithographic processes, their geometry can be easily varied by changing the dimensions in the mask. Figure 8.16 shows SEM image of probe microsockets with cantilevers of different sizes.

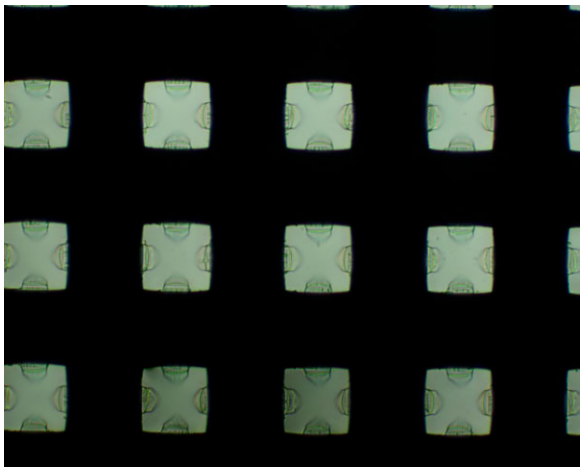


(a)

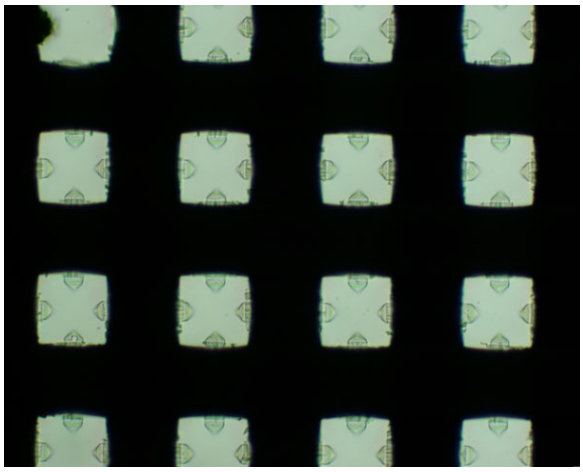


(b)

Figure 8.12: Microscope images of patterned photoresist atop the recessed membrane which sits over through-wafer vias in the silicon substrate. Light, from a source located at the bottom of the substrate, only transmits through etched vias.

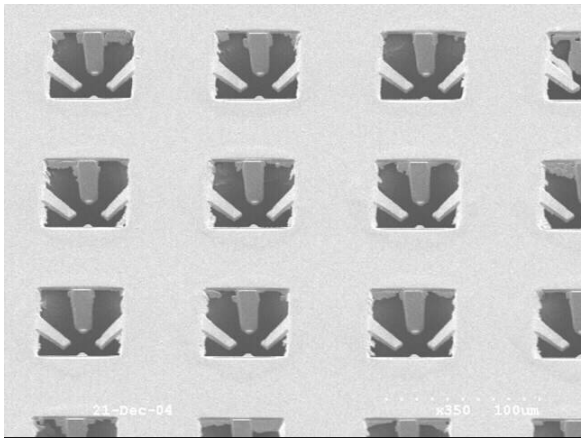


(a)

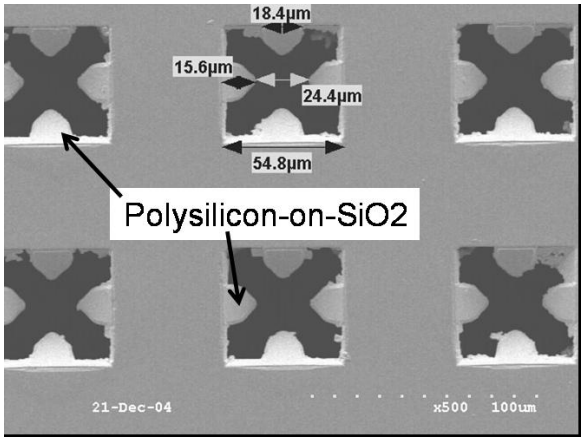


(b)

Figure 8.13: Microscope images of patterned angled cantilevers over through-wafer vias in the probe substrate after SiO_2 etching. These images were taken prior to removal of the photoresist etch mask.



(a)



(b)

Figure 8.14: Doped-polysilicon/SiO_2/doped-polysilicon angled cantilever probes.

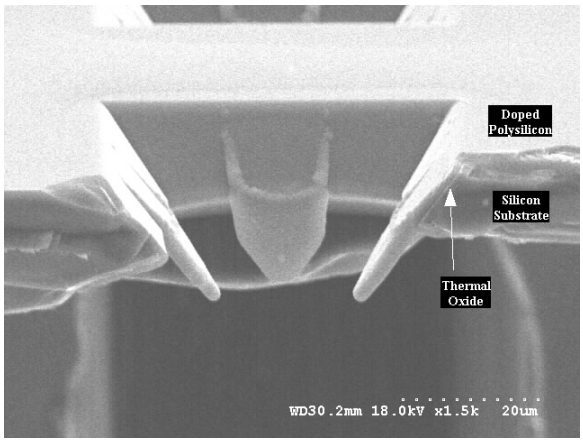
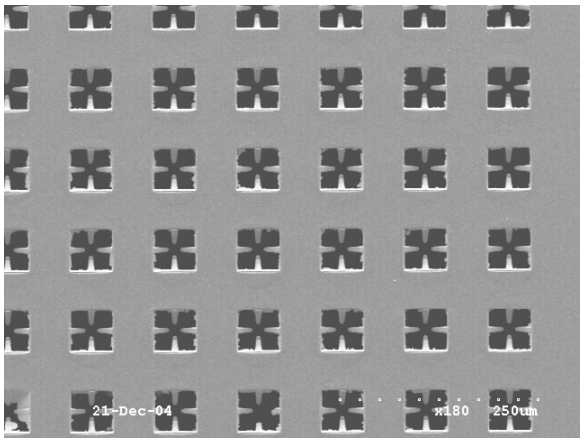
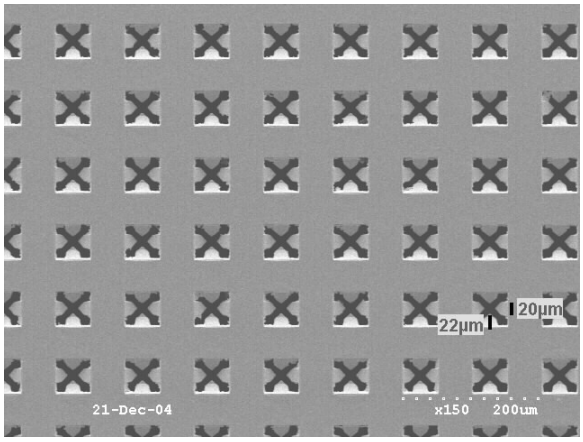


Figure 8.15: SEM image showing cross-sectional view of angled cantilevers over a through-wafer interconnect.



(a) 5μm wide x 20μm long



(b) 20μm wide x 20μm long

Figure 8.16: SEM images of cantilever probes of various dimensions.

8.3 Alternative Fabrication Process

The process for building a microsocket with Au/Ti/doped-polysilicon/SiO_2/doped-polysilicon cantilevers was described in the previous section. The cantilevers in the probe microsocket could also be made with a myriad of other materials – metal-on-polysilicon, Si_3N_4, metal, metal-on-polymer, etc. The fabrication of a probe substrate with only Ti/Au/Ti/doped-polysilicon cantilevers as well as preliminary fabrication results are detailed in this section. Similar to this example, cantilevers made of different materials can be constructed with only slight modifications to the general process illustrated in Figure 8.2.

8.3.1 Metal-on-Polysilicon Cantilevers

Figure 8.17 shows a process flow for building arrays of probe microsockets with Ti/Au/Ti/doped-polysilicon cantilever probes. The subtle difference from the previous method (Figure 8.2) is that there is no longer a thin layer of SiO_2 in the cantilever material stack. Removing the thin layer of SiO_2 may improve the mechanical characteristics of this structure. The fabrication remains similar up until the point of etching through-wafer vias underneath the oxide membranes and isolation of these vias with a thermally grown film of SiO_2 (Figure 8.17 (c)).

Following this, a 1-2 μm-thick layer of LPCVD poly-Si was deposited everywhere on the wafer. The poly-Si was diffusion doped and annealed (Figure 8.17 (d)). Using photolithography, vias were patterned in photoresist directly over the membranes on the trench-side of the wafer. The photoresist was used as an etch mask and the exposed poly-Si (on the membrane-side of the wafer) was etched away in an RIE. Following this, the exposed SiO_2 layer in the trench was also etched away using BOE (Figure 8.17 (e)). Plasma etching could also be used to remove the oxide. The resist was removed by rinsing in Acetone. At this point, any metal of choice could be deposited on the trench-side of the wafer using PVD or evaporation techniques. In this case a film of Ti/Au/Ti (300 Å/1 μm/300 Å) is deposited by DC sputtering. The Ti layer provides improved adhesion to the poly-Si film underneath. Au is a good choice of material simply for it's non-tarnishing nature.

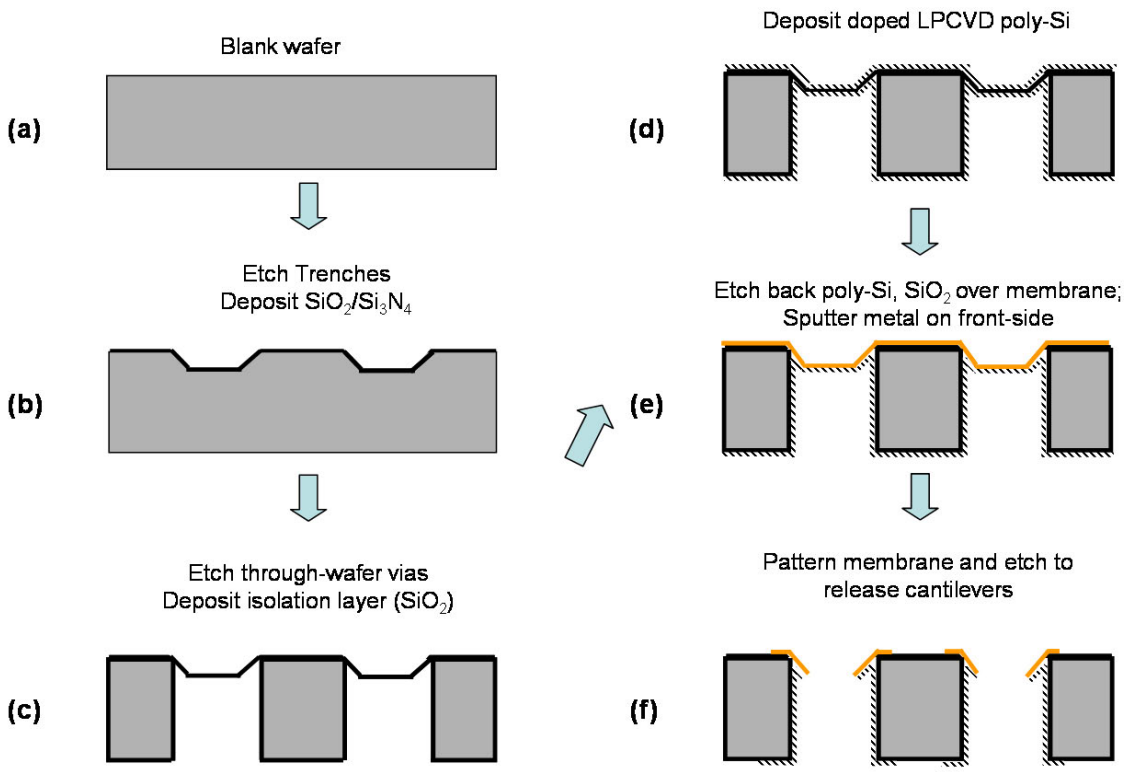


Figure 8.17: Fabrication process for a prototype probe substrate with cantilevers made of Ti/Au/Ti/doped-polysilicon. The final structure attained by this method differs from the one in Figure 8.2 in that there is no longer an oxide layer in the material stack. Only the major process steps shown.

NR7-1500P negative photoresist was then spun onto the wafer to pattern the membrane into angled cantilevers (spin-on: 2000/500/50, soft-bake: 90 s @ 110°C). After resist patterning, the exposed metal stack was removed by wet etching. BOE etches Ti, and an aqueous solution of potassium iodide and iodine ($KI:I_2:H_2O$ – 2:1:10) was used to etch Au. To achieve precise transfer of the pattern to the metal stack, it was important that the patterned photoresist not have negative sloping sidewalls (to prevent undercutting). In addition, further dilution of the metal etchants (to slow down the etching) provided better control over the etch process. After metal etching, the exposed poly-Si was removed by etching in an RIE. Great care was exercised during any subsequent processing steps to avoid destroying the now-released cantilevers. As such, the resist was removed by dipping the sample in Acetone. An additional lithography step could be used to pattern

the back-side of the wafer to isolate the microsockets. This completes fabrication of the Ti/Au/Ti/doped-polysilicon cantilever probe microsockets (Figure 8.17 (f)).

An SEM image of the doped-polysilicon/SiO_2/doped-polysilicon membrane over the through-wafer via is shown in Figure 8.18. A higher magnification SEM image of one side of this membrane is shown in Figure 8.19. Figure 8.20 shows patterned and etched cantilevers made of Ti-Au-Ti-poly-Si. In this image, NR7-1500P photoresist was still present over the etched cantilevers.

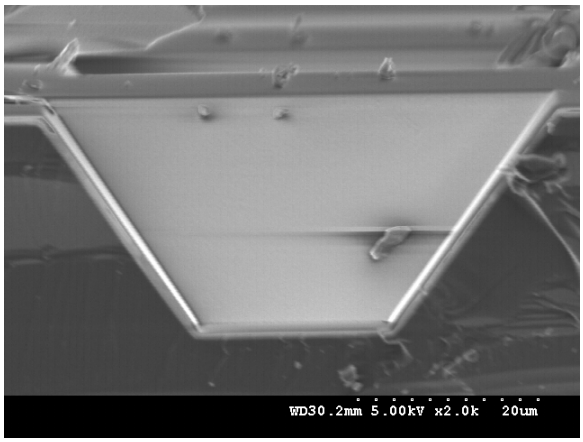


Figure 8.18: Cross-section image of a doped-polysilicon/SiO_2/doped-polysilicon membrane over a through-wafer via.

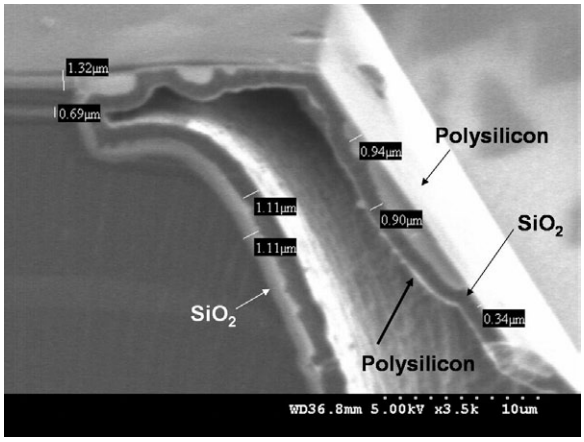


Figure 8.19: High magnification SEM image of one edge of a doped-polysilicon/SiO_2/doped-polysilicon membrane over a through-wafer via.

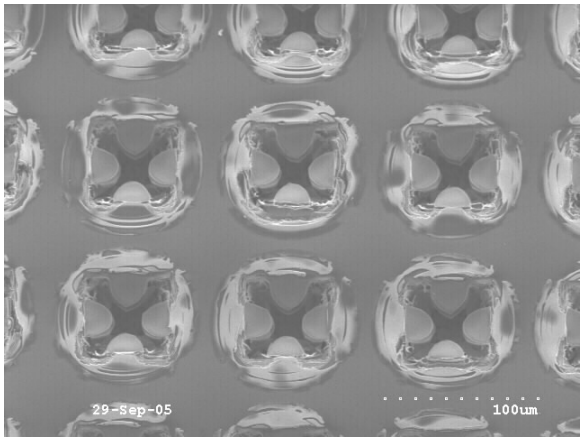


Figure 8.20: Array of patterned and etched microsocket probes made of Ti/Au/Ti/doped-polysilicon. There is still NR7-1500P over the cantilevers.

8.4 Conclusion

Polymer pillars are representative of next-generation chip-to-module interconnect technologies. Specifically, polymer pillars are compliant as well as multi-functional (electrical and guided-wave optical). The combination of these characteristics calls for a new probing technology. The fabrication of a prototype probe substrate was described in this chapter. The probe substrate was micromachined in a silicon wafer using IC and MEMS processing techniques. This allows the probes to have geometries comparable to the I/Os of the DUT. In addition, the probes can also be engineered to have the desired mechanical characteristics. The process flows described in this chapter, for building substrates with cantilevers made of Au/Ti/doped-polysilicon/SiO_2/doped-polysilicon as well as Ti/Au/Ti/doped-polysilicon, can easily be modified to include other suitable materials.

CHAPTER IX

MOEMS PROBE SUBSTRATE: DEMONSTRATION AND CHARACTERIZATION

9.1 Introduction

This chapter describes the various experiments carried out for the demonstration and characterization of the prototype probe substrate described in Chapters VII and VIII. The goal of these experiments was to demonstrate the use of this probe substrate for electrical and optical probing of chips having polymer pillar-based I/O interconnects. In addition, experiments were also performed to evaluate the mechanical robustness of the angled cantilevers in each probe microsocket.

All tests were performed on a prototype probe substrate having microsockets at a 100 μm pitch. The cantilevers were made of poly-Si/SiO_2/poly-Si (1 μm/0.5 μm/1 μm), with the SiO_2 layer encased within the poly-Si. In some cases, the cantilevers were also coated with Au/Ti (variable/30 nm; Ti was the adhesion layer). Henceforth, these will be referred to as gold-on-polysilicon cantilevers. The polysilicon was doped to be n-type, and was deposited (by LPCVD) everywhere on the wafer. A schematic of a single-cantilever is shown in Figure 8.1. A typical area-array of gold-on-polysilicon microsockets on the probe substrate is shown in Figure 9.1.

The dummy device-under-test for these experiments was a substrate with 30 μm-wide $\times$ 40 μm-tall polymer pillars – electrical, optical, or dual-mode.

9.1.1 Fabrication of Dummy Device-Under-Test

Figure 9.2 shows the process flow for fabricating dual-mode polymer pillars on apertures. Minor variations of this procedure were used for building DUTs with optical, electrical, or dual-mode pillars.

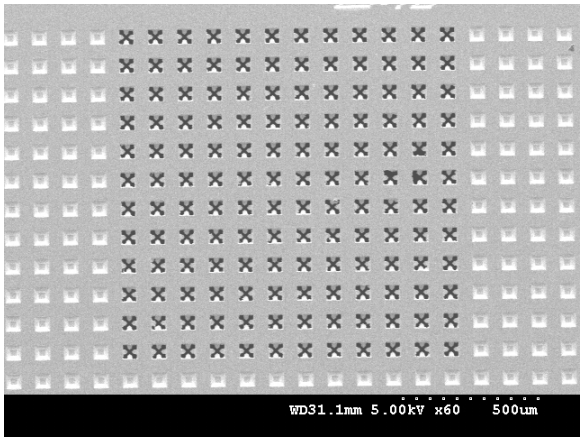


Figure 9.1: SEM image of a typical area array of probe microsockets. All characterization and demonstration was done on similar probe structures. In this particular image, the cantilevers were made of Au/Ti/poly-Si/SiO_2/poly-Si and were approximately 35 μm long $\times$ 15 μm wide.

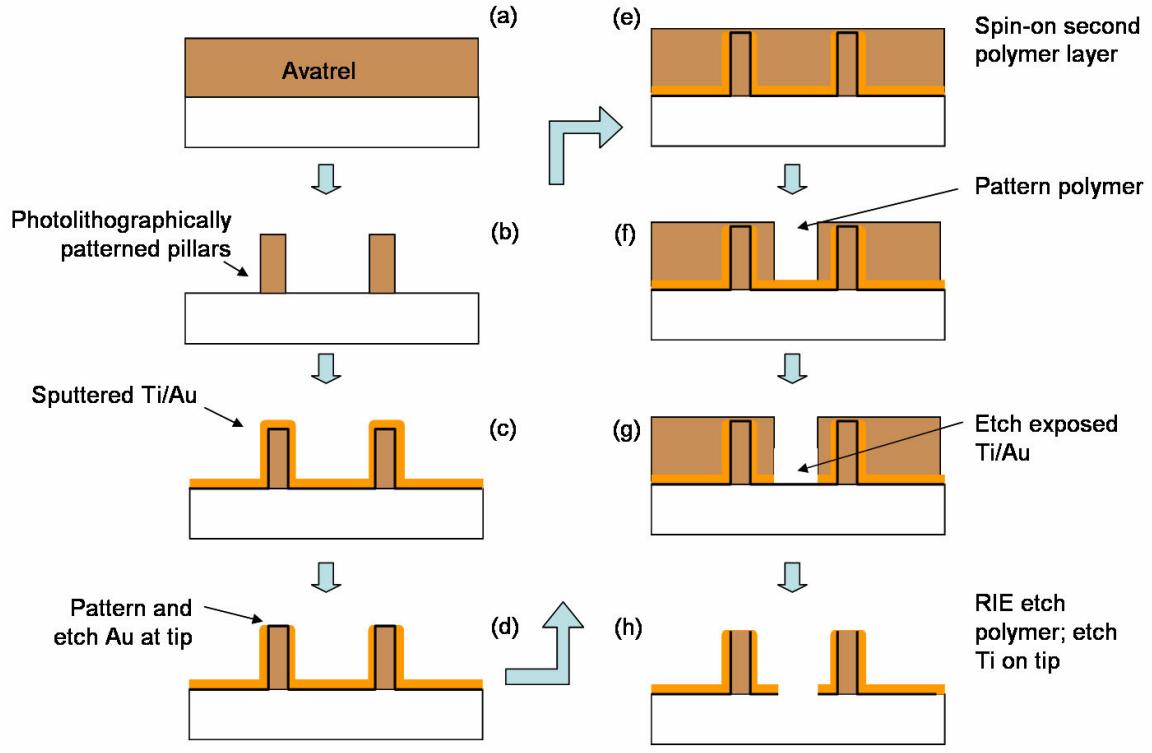


Figure 9.2: Process flow for fabrication of dual-mode polymer pillars. Variations of this process can be used to build DUTs with optical pillars, electrical pillars, dual-mode pillars, or a combination of these.

9.1.1.1 Optical pillars

To enable optical probing measurements, polymer pillars were fabricated on apertures on a glass slide. After cleaning the substrate, Ti/Au/Ti (300Å/3000Å/300Å) was sputter-deposited on the substrate. Using successive photolithography and etching steps, circular openings were etched in the metal corresponding to the locations of the pillars. Following this, ∼0.5 μm of SiO_2 was deposited over the metal (for adhesion), and a thick layer (40 μm) of Avatrel 2000 was spun onto the substrate (800 rpm for 40 s). The polymer was then soft-baked on a hotplate at 100°C for 80 minutes, and photolithographically patterned to yield polymer pillars (dose= 400 mJ at 365 nm; post-exposure bake= 20 minutes in a 100°C oven; develop= Bioact for ∼30 s). The pillars were aligned directly on top of the etched apertures in the metal. Figure 9.3 shows an SEM image of an array of polymer pillars fabricated on apertures on a glass slide.

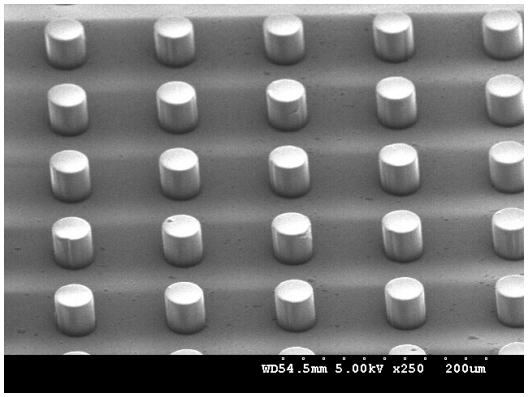


Figure 9.3: SEM image of an array of optical pillars on a dummy DUT used for optical probing characterization.

9.1.1.2 Electrical pillars

Electrical pillars for electrical-probing characterization could be made on a silicon or a glass substrate. First, a film of SiO_2, 0.5-1 μm-thick, was deposited on the wafer by PECVD. Following this, a 40 μm-thick layer of Avatrel polymer was spun onto the wafer, and photolithographically patterned to yield an array of polymer pillars (Figure 9.2 (b)). A layer

of Ti/Au (300 Å/2000 Å) was then sputter-deposited on this sample, and it was covered by a second layer of polymer (Figure 9.2 (e)). A second photolithography step was used to pattern the polymer using the pad or metal-trace layout (Figure 9.4). After developing the polymer, the exposed metal was removed by wet etching (Figure 9.2 (g)). Finally, the polymer cover layer was etched in the RIE tool (Figure 9.2 (h)). As the pillars were covered with a metal film, they remained protected during the etch. An SEM image of a dummy DUT with electrical pillars is shown in Figure 9.5. The pillars are isolated from each other, and connected by metal traces to pads on the periphery of the chip.

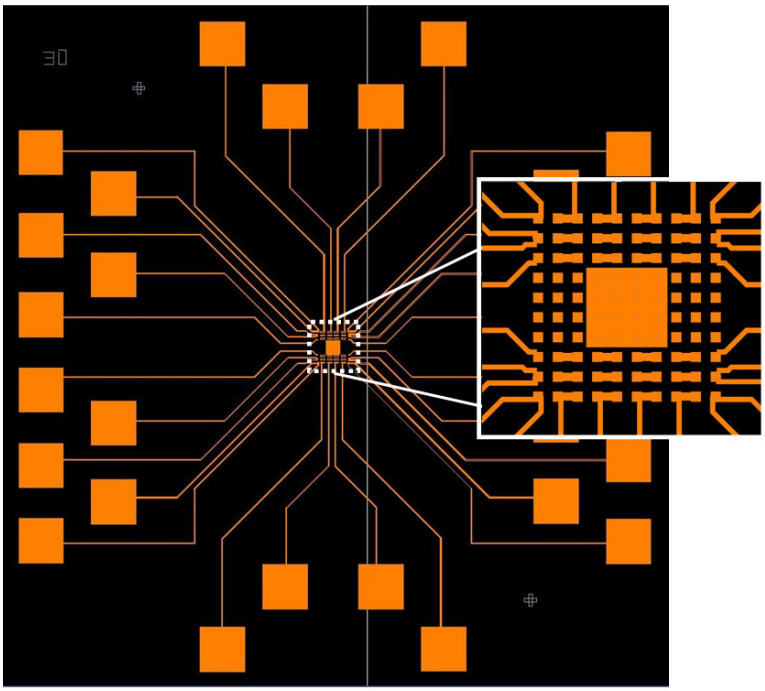


Figure 9.4: Captured image of the physical layout of pads and metal traces on the dummy DUT.

9.1.1.3 Dual-mode pillars

The fabrication process of a DUT with dual-mode pillars is shown in Figure 9.2. It is almost identical to the fabrication of a DUT with only electrical pillars. The only difference is the addition of an intermediate lithography step, which is needed to remove gold from the tips

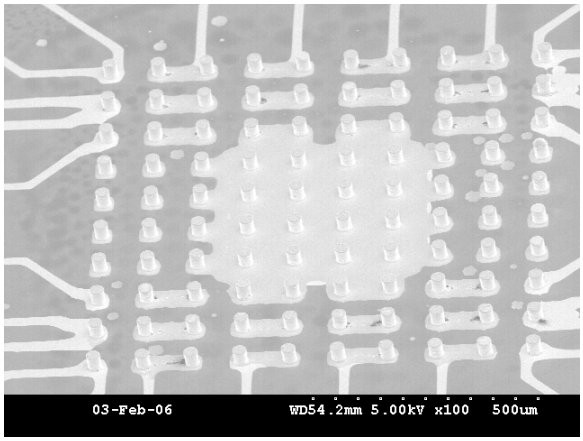


Figure 9.5: SEM of dummy DUT with all-electrical pillars, 30 μm wide $\times$ 39 μm tall.

of the pillars (Figure 9.2 (d)). The thin Ti layer is purposely left on the tip to protect the polymer pillars during subsequent processing. In step (h), this Ti film is etched away in BOE to yield a sample with dual-mode polymer pillars. Figure 7.10 shows an SEM image of a DUT with dual-mode pillars. Once again, metal traces connect the pillars to measurement pads at the periphery of the chip.

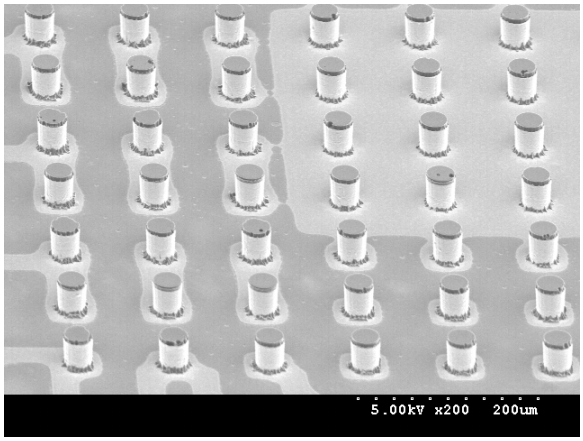


Figure 9.6: SEM image of dual-mode polymer pillars used in probe microsocket characterization. Owing to an aberration during processing, there was no metal on the sidewalls around the very tip of the pillars.

9.2 Probe Substrate-to-Pillar Optical Coupling

For optical probing, the probe substrate ought to be able to transfer optical signals between the test equipment and the DUT. The location of photonic emitters and detectors in the manufacturing test setup will depend on a number of factors such as the type of test to be performed, the architecture of the DUT, the availability of emitters and detectors that can be integrated on the probe substrate, the availability of a passive optical waveguiding and coupling methods, and more. As such, characterization of a true manufacturing-ready probe substrate is not possible at this stage of research. The core components (that is, the probe microsockets) of the prototype are characterized.

9.2.1 Optical Transmission from the Probe Substrate to Polymer Pillars

A simple, yet convincing, demonstration of optical probing using the MOEMS probe substrate can be achieved by coupling light from the optical through-wafer interconnects of the probe microsockets to optical pillars on the DUT. Figure 9.7 shows a schematic of the experimental configuration that was devised for this demonstration. It is similar to the setup used for observation of transmission in optical through-wafer interconnects (Figures 4.19 and 4.20). The only difference for the optical probing experiment is the sample-under-test.

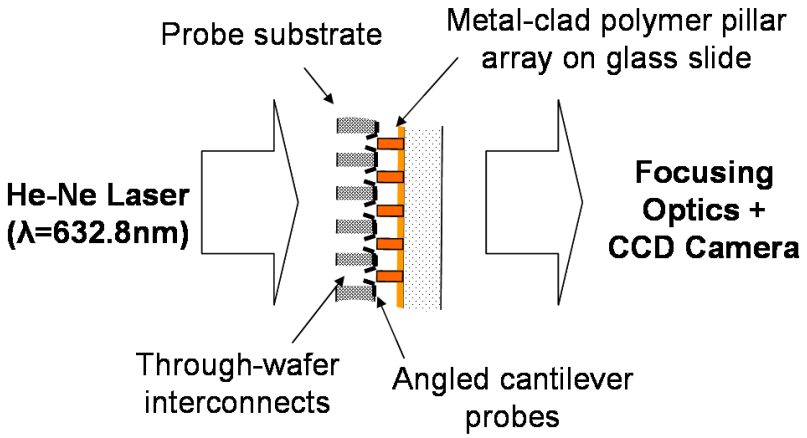


Figure 9.7: Schematic of probe-to-chip optical transmission demonstration setup.

The dummy DUT for this demonstration was a glass slide with pillars fabricated on

apertures – there was metal everywhere on the substrate except on the tips of the pillars. An SEM image of such a sample is shown in Figure 9.8.

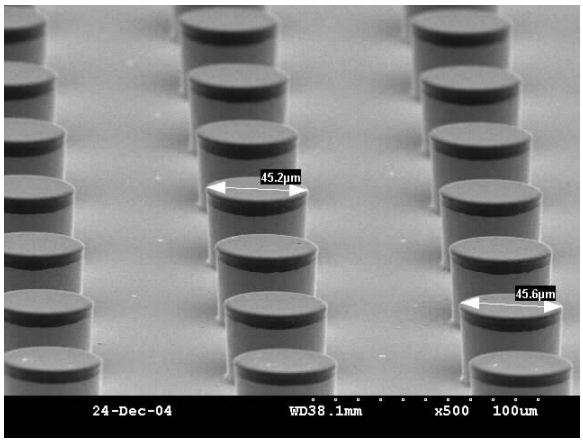


Figure 9.8: SEM image showing an array of polymer pillar I/O interconnects fabricated at a 100 μm pitch. There is metal everywhere except on the tips of the pillars.

First, only the dummy DUT was placed in the experimental setup. As the full-width half-maximum (FWHM) of the laser source is > 600 μm, it illuminated at least a 6×6 array of pillars, which were built on a 100 μm pitch, on the DUT. The sample was oriented with the pillars facing the laser, and the output from the bare-glass (back)-side of the DUT was captured using the CCD camera. Figures 9.9 and 9.10 show images of the output from an array of pillars (viewed from the back-side of the sample) at low- and high-magnifications, respectively. These images are from two different samples.

Similarly, the output (from the cantilever-side) when the back-side of only the probe substrate was illuminated is shown in Figure 9.11.

Following this, the array of polymer pillar I/Os was aligned to and inserted into a matching array of through-wafer interconnects (part of the probe microsockets) on the probe substrate. Ideally, an active alignment system would be best suited for this. As this high-precision capability was not available for use, the alignment and attachment was achieved with a flip-chip pick-and-place process on the M10A flip-chip bonder (Figure 4.35). A three-step bonding process – 25 g, 50 g, 75 g for 15 s each – at room temperature was used for aligning and placing the DUT over the probe microsockets. To avoid shifting of the

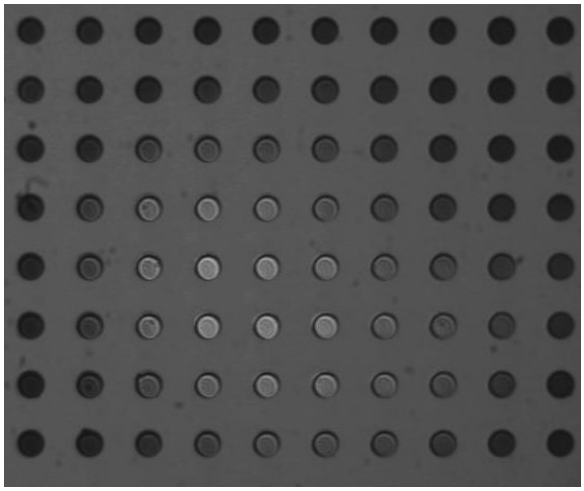


Figure 9.9: Low-magnification image of output from the back-side of a polymer pillar array. As the Gaussian laser beam has an FWHM > 600 μm, it illuminated an array of pillars on the sample. Also, as expected, the intensity of the beam was highest at the center, and tapered off with increasing radial distance.

stacked substrates while transporting them to the measurement setup, the two samples were glued together by dispensing a couple of drops of photoresist at the edge of DUT (owing to capillary action, the photoresist spreads along the region between the two substrates) and raising the temperature of the bonder chuck to drive out the solvent from the photoresist. A photograph of the two stacked substrates is shown in Figure 9.12(a). When this sample was held up to a light, transmission through the aligned attached substrates was clearly visible (Figure 9.12(b)).

Figures 9.13 and 9.14 show low- and high-magnification images of the output from the back-side of the pillar substrate for the attached samples. These correspond to the same set of samples from the images in Figures 9.9 and 9.10, respectively.

Coupling between the through-wafer interconnects and polymer pillars gives rise to an interference pattern which is visible in this image. This pattern has a resemblance to the one observed for optical transmission in only the probe microsocket (Figure 9.11). This is clear evidence of optical transmission from the probe substrate to an array of polymer pillar I/Os, and in a simple manner demonstrates the proposed optical I/O probing scheme.

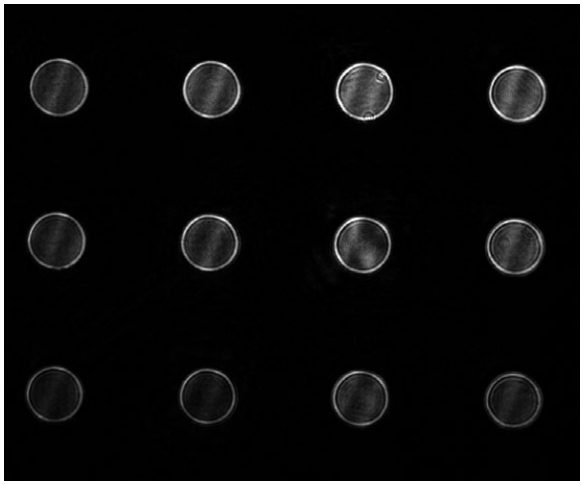


Figure 9.10: Image of output from back-side of a polymer pillar array. Metal everywhere on the front-side except on the tip of the pillars assured that only light incident on the pillars got through to the back-side. Concentric interference patterns, which were typical of polymer pillars, were also visible in this image.

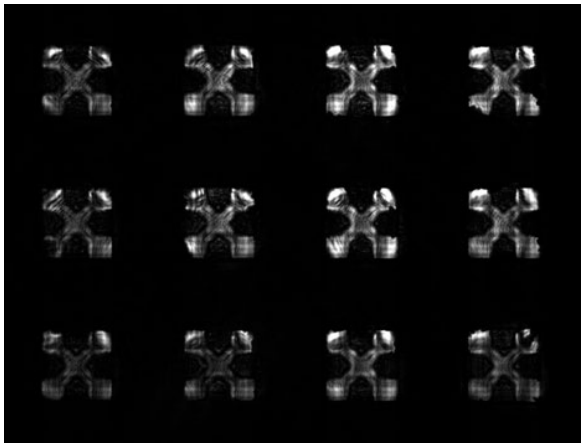
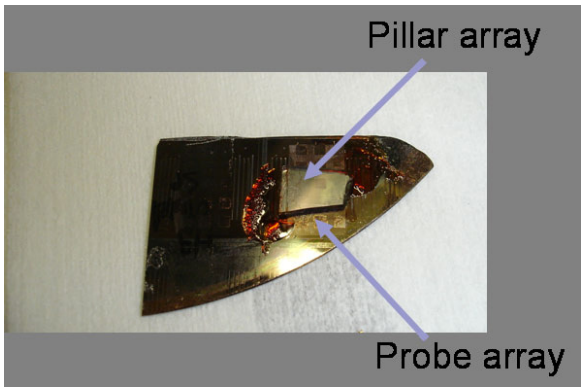
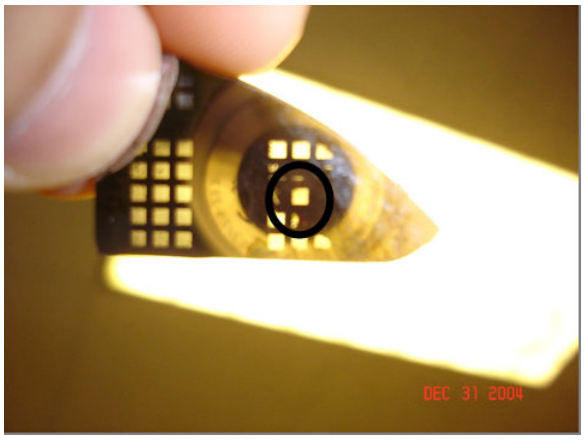


Figure 9.11: Image of output from the probe-side of the MOEMS probe substrate. The angled cantilever probes are clearly visible.



(a)



(b)

Figure 9.12: (a) Photograph of a glass substrate with polymer pillars temporarily attached to the probe substrate for characterization. (b) Transmission of light through the attached substrates quickly confirmed good alignment.

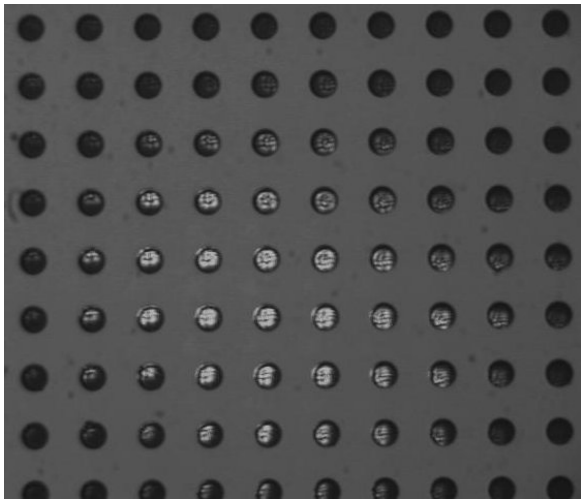


Figure 9.13: Low-magnification image of output from the back-side of a dummy DUT when it was in contact with a MOEMS probe substrate.

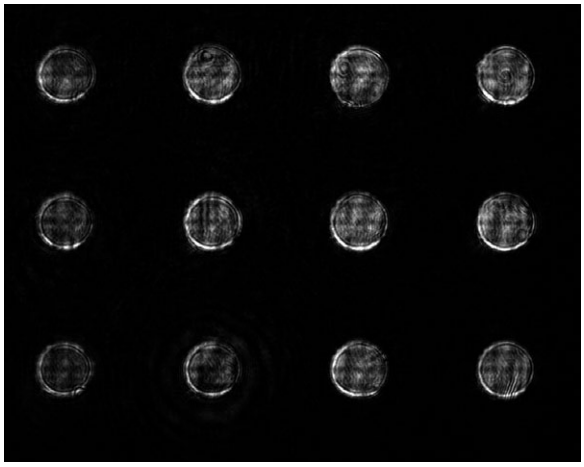


Figure 9.14: Image of output from back-side of a polymer pillar array for the attached samples. Light passes through the through-wafer interconnects, and is successfully coupled into the polymer pillars.

9.2.2 Optical Power Coupling

Figures 9.13 and 9.14 demonstrate optical probing in a qualitative manner. A second set of experiments was carried out to *quantitatively* measure optical coupling between the prototype probe substrate and a DUT with optical pillars. The experimental setup is illustrated in Figure 9.15. It is similar to the configuration described earlier for measuring optical power transmitted in through-wafer interconnects (Figures 4.23 and 4.24). An up-close image of the setup is shown in Figure 9.16. Using a single-mode optical fiber, with a core radius of 6 μm, the incident optical signal could be positioned directly above individual through-wafer interconnects or pillars. For this set of measurements, the DUT consisted of a 10×10 array of optical polymer pillars, 28-30 μm wide × 36-39 μm tall, fabricated at a 100 μm pitch (Figure 9.3) on apertures on a glass slide. These were to be contacted by an array of probes on the probe substrate where the cantilevers were 35 μm long × 15 μm wide and were made of gold-on-polysilicon (1 μm Au).

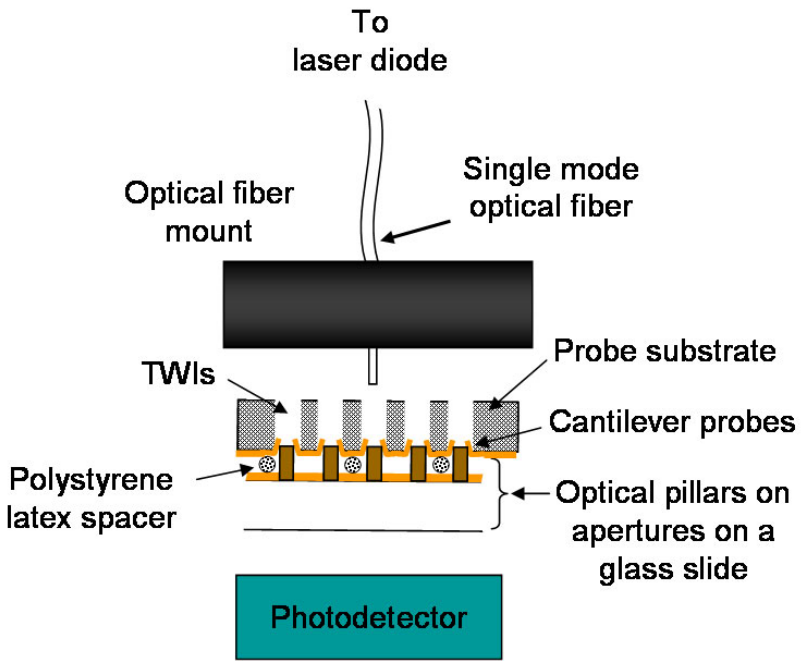


Figure 9.15: Setup for measuring optical power coupled from the prototype probe substrate to an optical pillar on the DUT.

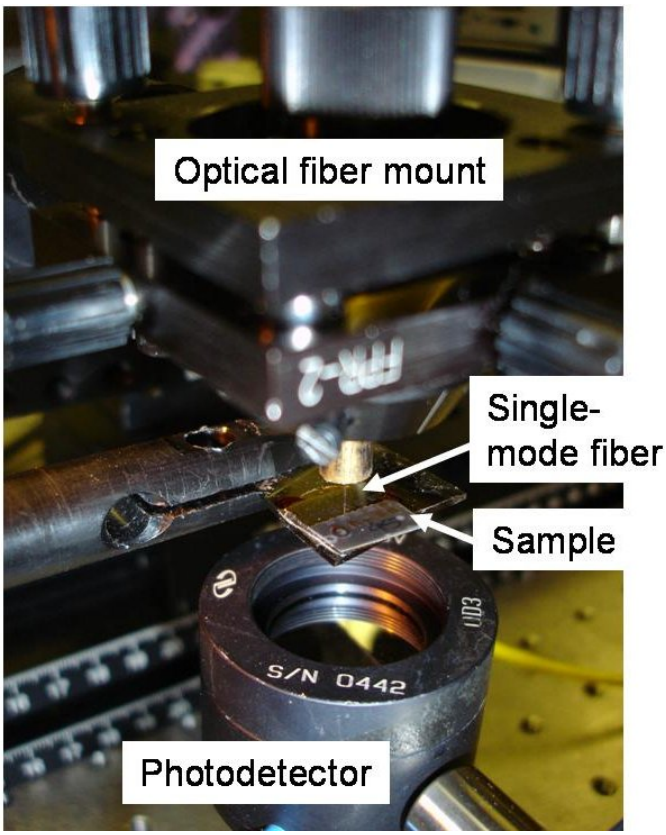


Figure 9.16: Close-up photograph of the optical fiber, a sample-under-test, and the photodetector in the optical power measurement setup.

First, only the probe substrate was placed in the setup, and the optical power transmitted through individual through-wafer interconnects in a 4×4 array was measured. The sample was placed in the setup with the cantilever-side facing away from optical fiber. Following this, an array of pillars on the dummy DUT was aligned to the corresponding array of microsockets using the flip-chip bonder (Figure 9.17). A limitation of using the flip-chip bonder for this experiment is that it continues to press the two substrates together until a specified force is reached; the pillars were essentially jammed into the microsockets. During experimentation, it was observed that this action sometimes caused some cantilevers to break. The microsocket cantilevers were designed for a specific range of motion. Like any other mechanical structure, exceeding this range leads to fracture. To avoid this situation, an aqueous suspension of polystyrene latex spheres of 15 μm diameter was dispensed

onto the DUT around the pillars. When the water evaporated away, a monolayer of solid latex spheres was left around the pillars (Figure 9.18). This way, when the flip-chip bonder brought the two substrates in contact, the pillars were only partially inserted into the microsockets; the polystyrene latex spheres absorbed most of the applied force and served as a uniform spacer between the two substrates. [1] After the bonder had placed the DUT over the probe substrate, the two were glued together with cured photoresist. Figure 9.19 shows a photograph of one such pair of attached samples. A microscope image of this pair is shown in Figure 9.20. In this image, the DUT (with polymer pillars) is at the bottom, and the pillar array is being probed by the microsockets. The inset shows an outline of the pillar as well as the deflected cantilevers in the microsocket.

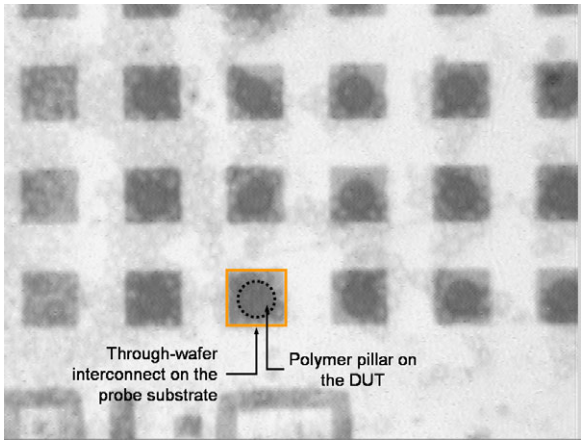


Figure 9.17: Image of probe substrate aligned to an array of polymer pillar I/Os on the dummy DUT. The image was taken using the split-vision camera in the flip-chip bonder prior to attachment.

Optical power measurements were repeated for the same 4×4 array of interconnects on the attached samples, and are summarized in Figure 9.21. Here, the y-axis corresponds to the optical power transmitted through individual probe-to-pillar coupled structures in the 4×4 array. The power for each coupled probe-to-pillar structure is expressed as a percentage of the power transmitted in only the through-wafer interconnects in that pair (measured in

[1] It was also observed that pillars only needed to be partially inserted into the microsockets to achieve good contact. Therefore, the use of a spacer in this experiment was justified.

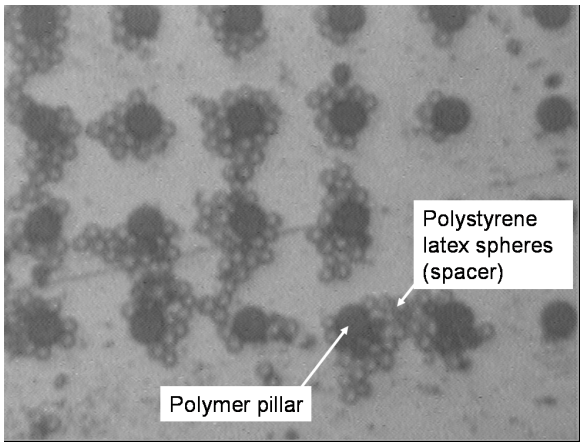


Figure 9.18: Image of polymer pillars and polystyrene latex spheres on the dummy DUT. A monolayer of 15 μm latex spheres served as a spacer and prevented the pillars from crashing into and destroying the probe microsocket cantilevers.

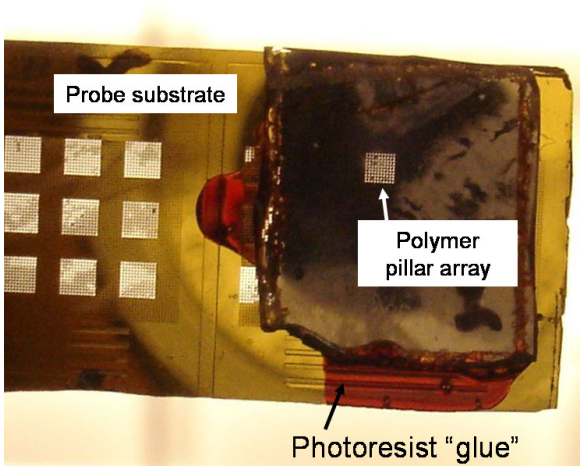


Figure 9.19: Photograph of polymer pillar DUT aligned and temporarily attached to a probe substrate for optical power coupling measurements.

the first half of this experiment). The x-axis corresponds to each column of the measured 4×4 array. The range of values for each column corresponds to the power transmitted in the probe-to-pillar coupled structures in different rows of that column. The high, low, and mean values of this range are clearly marked. This chart essentially quantifies coupling between the probe substrate and the pillars on the DUT.

On average, around 27% optical power was coupled from a through-wafer interconnect to a pillar. The coupling could be increased by sizing the through-wafer interconnects to

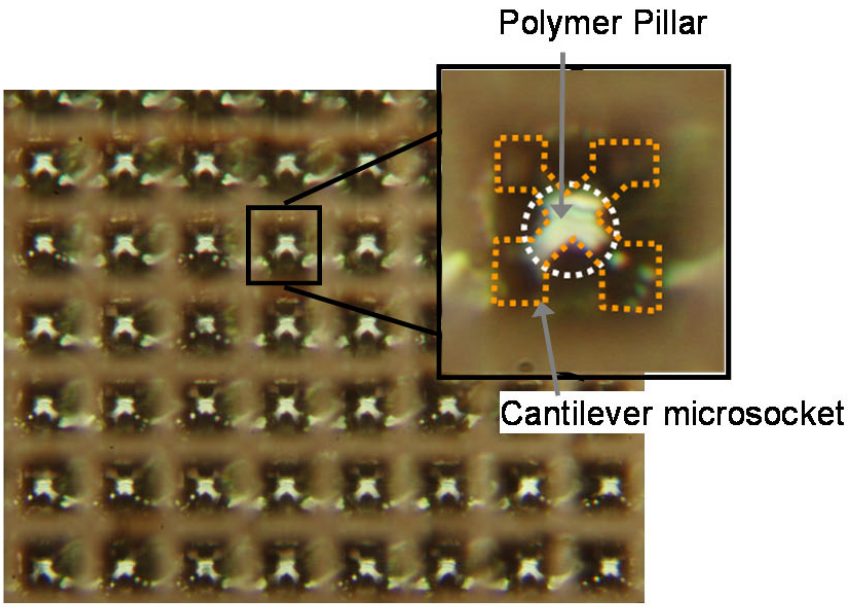


Figure 9.20: Microscope image of cantilever microsockets probing a chip with optical polymer pillar I/Os.

be comparable to the polymer pillar diameter. In this measurement, the through-wafer vias were ∼52 μm wide and the pillars were only 28 μm in diameter.

The coupling measurement did not separate the transmission losses incurred in the pillars and the DUT glass substrate. The raw measured optical power in a set of pillars, the corresponding set of probes, and the attached samples is plotted in Figure 9.22. The power transmitted through individual pillars (and the glass substrate) was measured to be much higher than either the probe substrate or the coupled structures. Therefore, it can be assumed that the losses in the pillars and the glass substrate do not limit this coupling number.

9.2.3 Pillar-to-Pillar Optical Coupling

Fabricating pillars on the probe module, as shown in Figure 7.5, could greatly improve optical coupling between the probe module and the DUT. Doing this reduces probe-to-pillar coupling to a pillar-to-pillar coupling problem. A simple qualitative experiment was done to demonstrate pillar-to-pillar coupling. A schematic of the experimental setup is

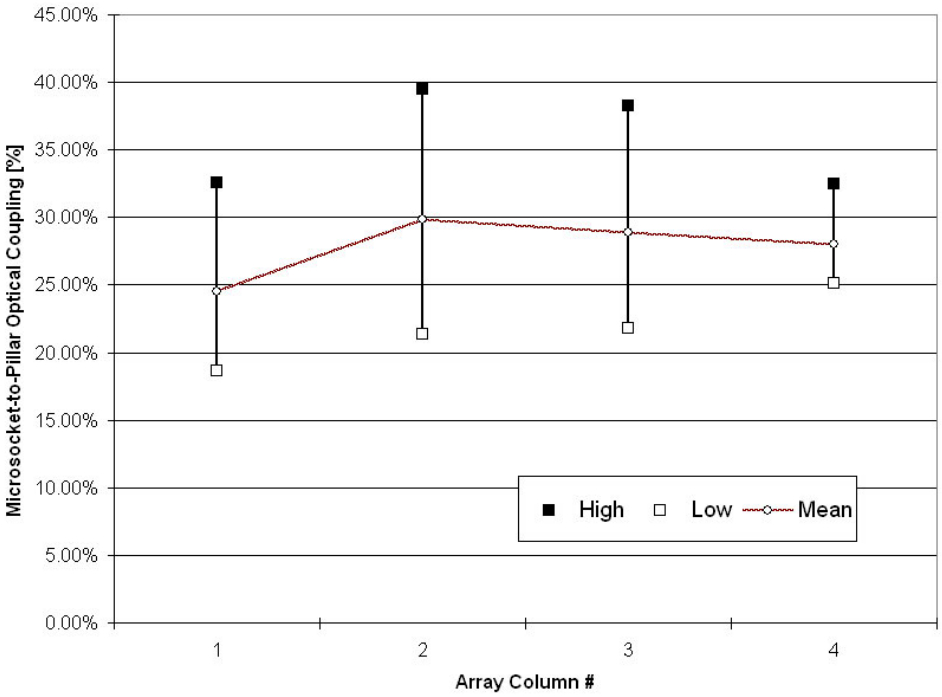


Figure 9.21: Plot showing percentage of optical power coupled between through-wafer interconnects (52 μm wide) on the probe substrate and optical polymer pillar I/Os (28 μm diameter) on a dummy DUT. Data for a 4×4 array of coupled structures is shown. The x-axis corresponds to the columns in this array, and the range of values represent the rows in each column.

shown in Figure 9.23. Two samples with pillars fabricated on apertures on a glass slide were mounted on micropositioners and positioned between a laser and a CCD camera. One sample was kept stationary while the other was actively aligned to the first one. Figure 9.24 shows images of pillar-to-pillar coupling between the two samples. At 0 μm, the camera was focused on the back-side of the pillar substrate closest to it; the additional images were taken as the camera focus was moved further away from the substrate.

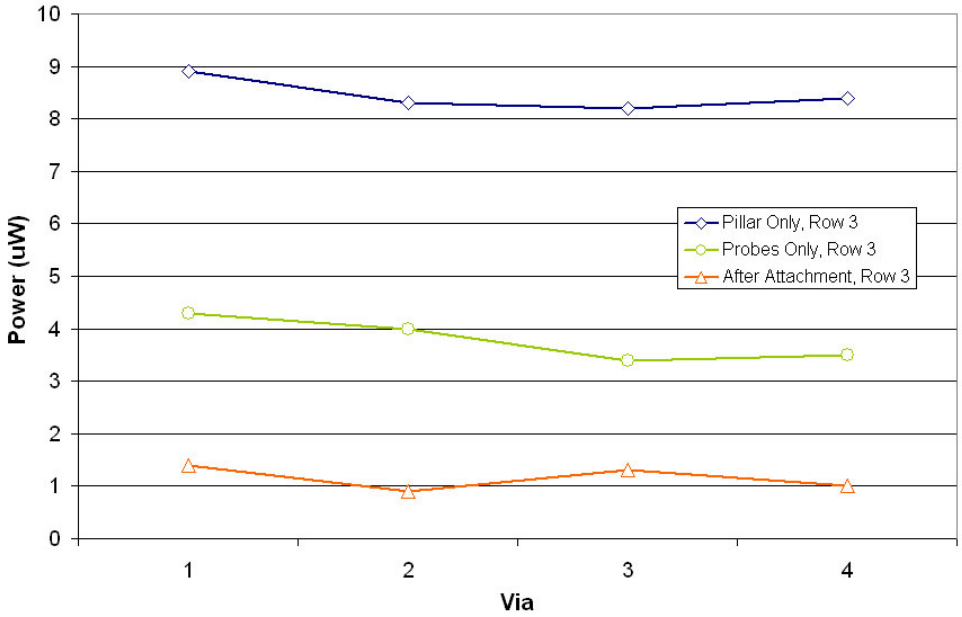


Figure 9.22: Chart graphing optical power transmitted in a set of pillars, a set of corresponding probes, and the attached samples. The source, in all cases, was an optical fiber pig-tailed to a 635 nm laser diode. As the amount of power transmitted in only the pillars was much greater than the power transmitted in only the through-wafer interconnects or the probe-to-pillar coupled structures, the losses in the pillars were assumed to be insignificant when determining optical coupling between the probe substrate and the pillars on the DUT.

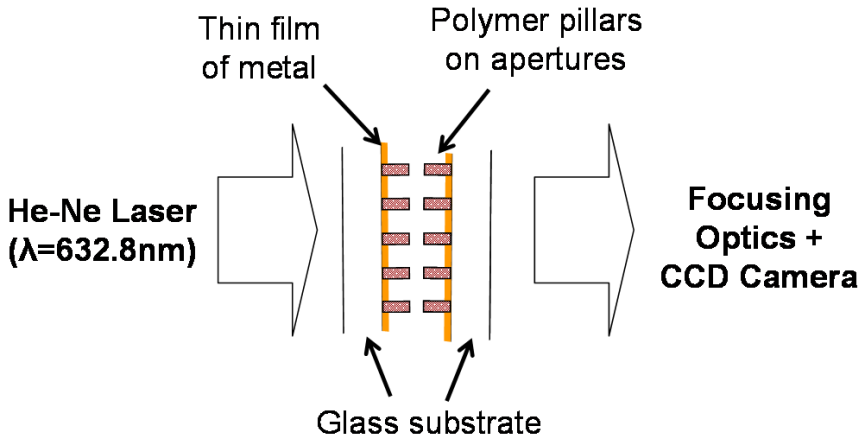
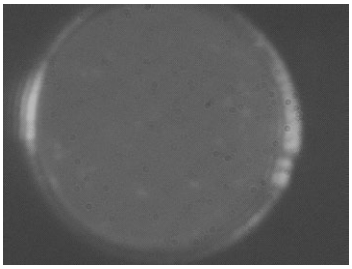
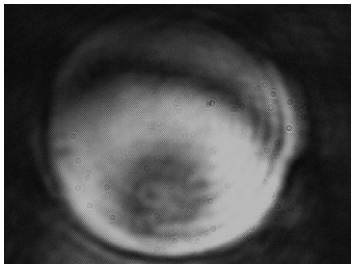


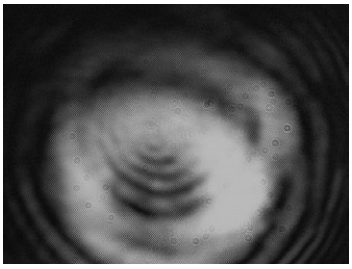
Figure 9.23: Schematic of setup for pillar-to-pillar optical coupling demonstration.



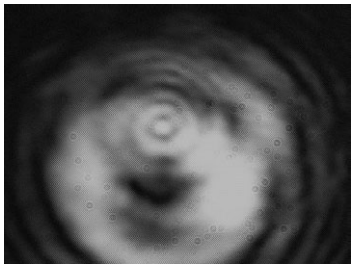
(a) 0 μm , no illumination



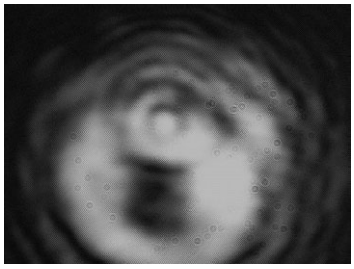
(b) 0 μm



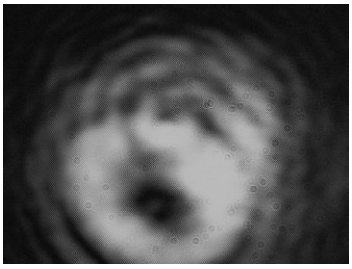
(c) 100 μm



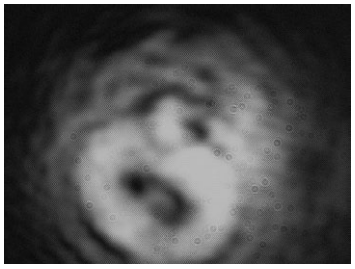
(d) 200 μm



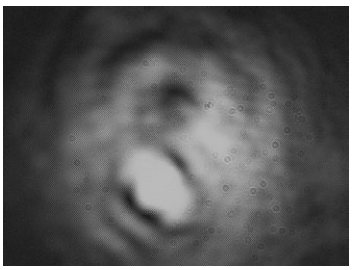
(e) 300 μm



(f) 400 μm



(g) 500 μm



(h) 1000 μm

Figure 9.24: Images of optical coupling from one pillar to another. The images show successive null points as the camera focus is moved further away from the substrate surface. The pillar arrays on the two substrates were approximately 3.45 mm apart, and a slight angular pitch was present between them.

9.3 Probe Microsocket Contact Resistance (R_{cont})

Electrical probing using the MOEMS probe substrate was demonstrated by probing electrical pillars with cantilever microsockets and measuring R_{cont} between the two. The experimental configuration for this measurement is illustrated in Figure 9.25; an electrically-shorted array of probe microsockets is brought in contact with a dummy DUT having electrical polymer pillar I/Os (Figure 9.26). The pillars are electrically isolated from each other; metal lines patterned on the DUT connect the pillars to pads at the periphery of the sample. Contact between the two substrates completes an electrical path, and enables measurement of R_{cont}. A cross-section of the proposed experiment is shown in Figure 9.26.

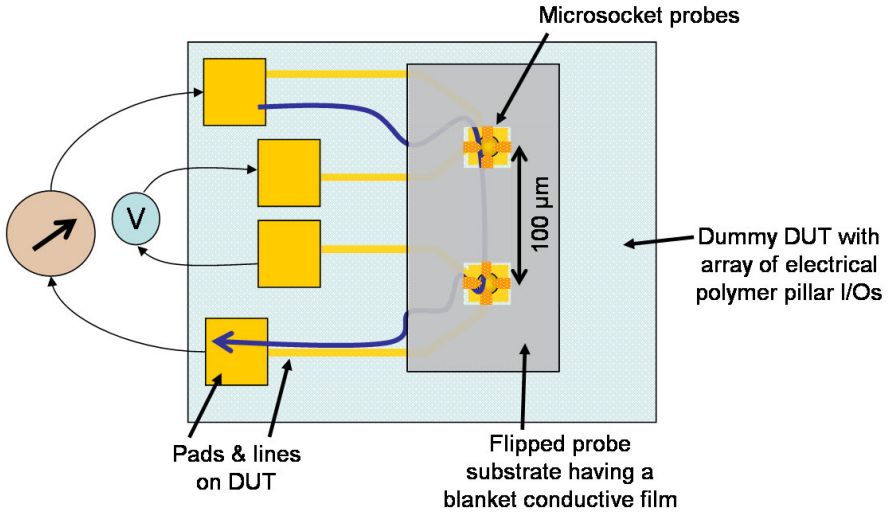


Figure 9.25: Schematic showing method for measuring probe contact resistance.

9.3.1 Probing Electrical Polymer Pillars

During the experiment, the probe substrate (Figure 9.27) was aligned to and brought in contact with the dummy DUT (Figure 9.28) using the flip-chip bonder. The alignment and pick-and-place processes were controlled manually. After alignment (using the bonder's split-vision camera), the probe substrate was slowly stepped towards the DUT until they were in contact. Contact was verified by measuring electrical continuity between the two substrates using a digital multimeter (Figure 9.29). At this time, a 4-point resistance

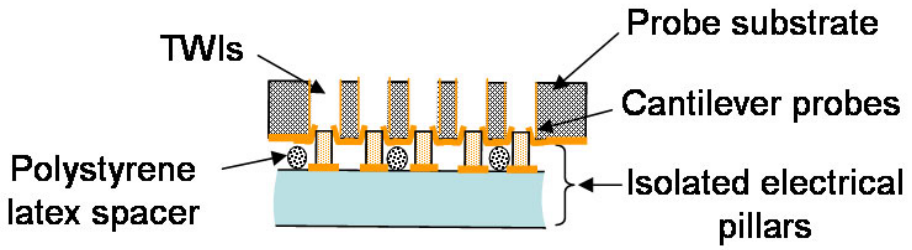


Figure 9.26: Cross-section schematic of a shorted probe substrate in contact with electrically isolated pillars on the DUT. Once again, polystyrene latex spheres were used as physical spacers between the two substrates.

measurement was made. The contact resistance between the microsocket cantilevers and pillars is assumed to be the dominating component in the electrical path; the measured resistance can be assumed to be equal to the probe contact resistance.

R_{cont} was first measured for a microsocket where the gold-on-polysilicon cantilevers were 35 μm long $\times$ 20 μm wide $\times$ 3 μm thick (Figure 9.27); and electrical pillars (30 μm wide $\times$ 39 μm tall) on the DUT coated with Ti/Au (300 Å/2000 Å) (Figure 9.5). Figure 9.30 plots the typical contact resistance (per microsocket-pillar pair) as a function of probe overdrive. Here, 0 μm overdrive refers to the point of first contact between the two substrates. R_{cont} decreases and stabilizes as the probe is overdriven (that is, the pillars are overdriven into the microsockets). Overdriving the pillars into the microsocket increases the contact area; as such, a decrease in the contact resistance is expected. Beyond a certain point (at an overdrive= 11 μm in this measurement), an *open* was observed. At such a large overdrive, there is excessive stress on the cantilevers which could cause them to fracture, resulting in an open circuit condition. Sure enough, it was seen that the cantilevers in this greatly overdriven microsocket had been severed from the substrate.

Overall, the contact resistance of a microsocket was measured to be 0.52 Ω, which is very much in line with the expectations outlined in the ITRS.

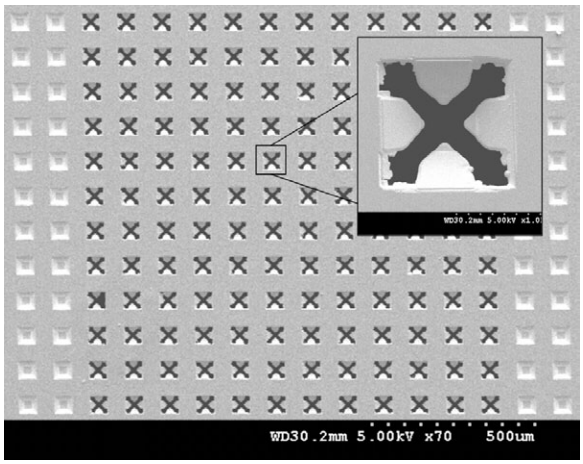


Figure 9.27: SEM image of an array of gold-on-polysilicon probe microsocket with cantilevers that are 35 μm long $\times$ 20 μm wide. The inset shows a single microsocket.

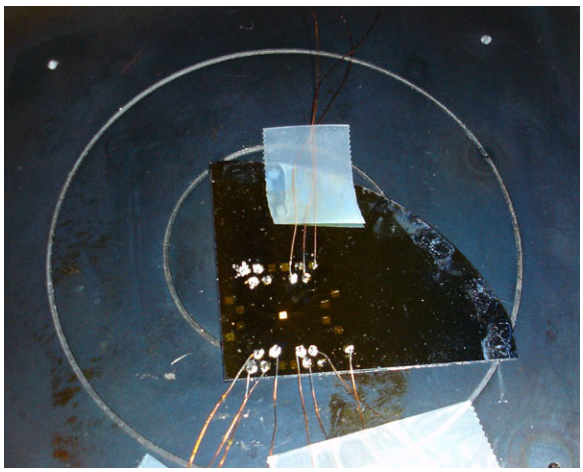


Figure 9.28: Photograph of dummy DUT with an array of electrical pillar I/Os. Solder-attached copper wires were used to connect the pads on the DUT to a multimeter.

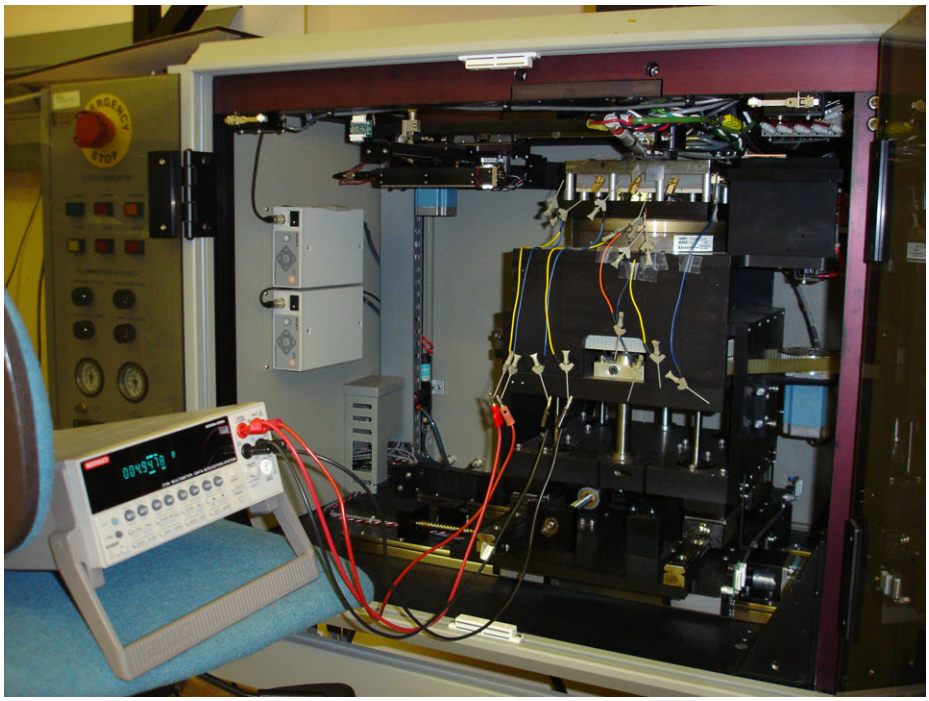


Figure 9.29: Photograph of experimental configuration for measuring probe contact resistance. The probe substrate and the DUT were aligned and brought in contact using the flip-chip bonder. Copper wires solder-attached to measurement pads on the probe substrate were, in turn, connected with cables to a digital multimeter.

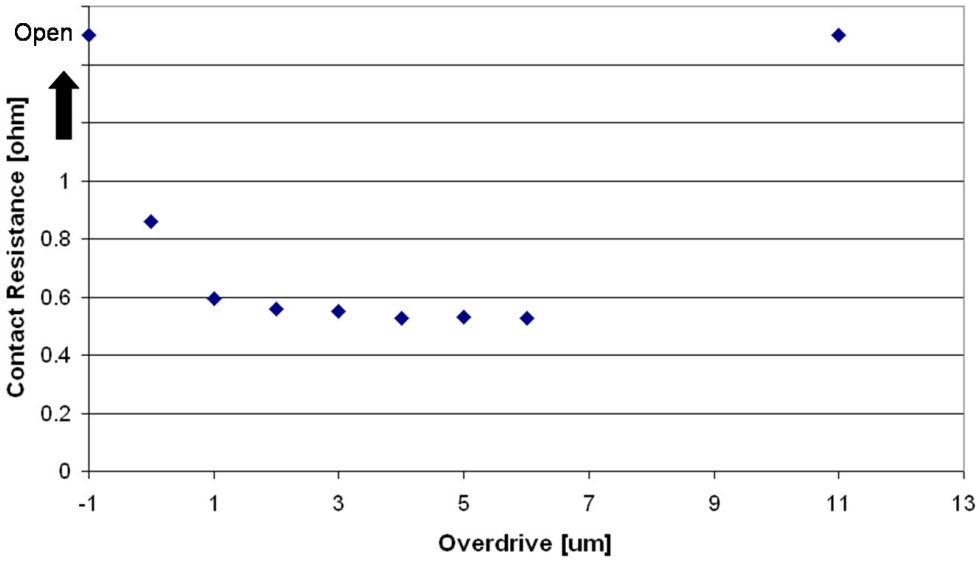


Figure 9.30: Plot of probe contact resistance as a function of vertical overdrive. The cantilevers were made of gold-on-polysilicon (35 μm long $\times$ 20 μm wide $\times$ $\sim$3 μm thick), and the pillars were approximately 30 μm in diameter $\times$ 39 μm tall. 0 μm on the x-axis represents the point of first contact. The contact resistance decreases and stabilizes with increasing vertical motion. Continuing to overdrive the pillar in the socket severs the cantilevers from substrate, resulting in an open.

9.3.2 Probing Dual-Mode Polymer Pillars

The R_{cont} measurement was repeated for a DUT with dual-mode polymer pillars (Figure 9.6). In this sample, metal did not cover the entire sidewall of the pillars – there was a small region around the tip of each pillar that did not have metal on it. R_{cont} as a function of overdrive is plotted in Figure 9.31. The contact resistance for this sample was higher than the previous one simply because poor metal coverage at the pillar tip equates to a very small contact area between the cantilevers and the pillars. Nonetheless, the graph has the same trend as the R_{cont}-overdrive curve for the all-electrical pillars.

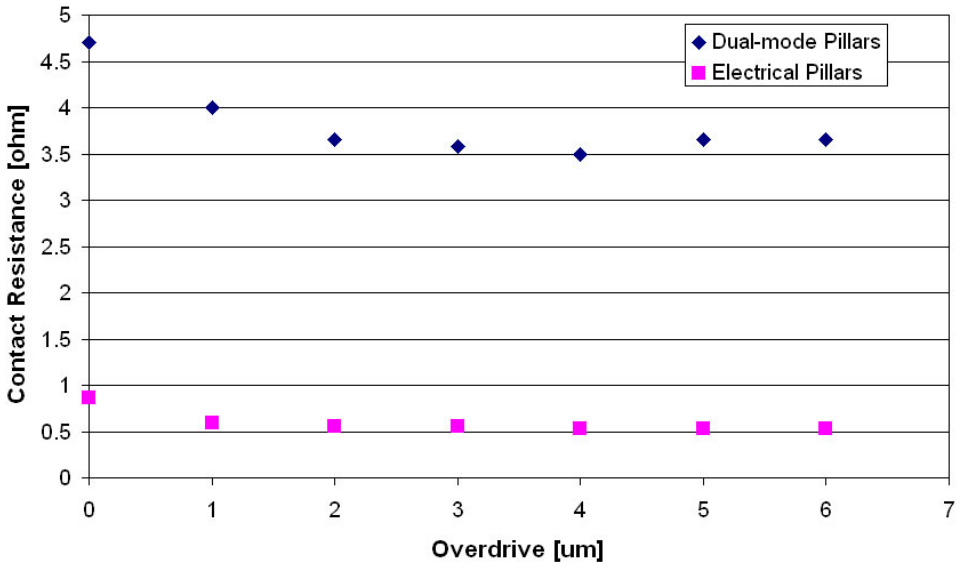


Figure 9.31: Combined plot of contact resistance for probe microsockets as a function of probe overdrive with respect to two different DUTs having: (i) all-electrical pillars, and (ii) dual-mode pillars. The gold-on-silicon microsocket cantilevers were 35 μm long $\times$ 20 μm wide $\times$ 3 μm thick.

9.4 Mechanical Characterization

The application space of the fabricated microsockets – wafer-level testing – requires them to be extremely robust and long-lasting. It is not uncommon to expect probes to have a lifetime on the order of tens of thousands of touchdowns or more. Therefore, mechanical characterization of the fabricated microsockets on the prototype substrates was an important aspect of this research. The mechanical characterization was performed on a probe microsocket where the cantilevers were made of Au/Ti/doped-polysilicon/SiO_2/doped-polysilicon (Variable/300Å /1.

All mechanical characterization was done using the Hysitron Triboindenter at the Georgia Tech MiRC. The Triboindenter is able to continuously monitor nanometer-scale changes in displacement as a function of applied force; the applied load is defined by a user-specified load-function. A diamond flat-punch tip, 30 μm wide $\times$ 45 μm tall, was used to *indent* the microsocket cantilevers. An impression by this tip on a layer of partially-cured photoresist is shown in Figure 9.32.

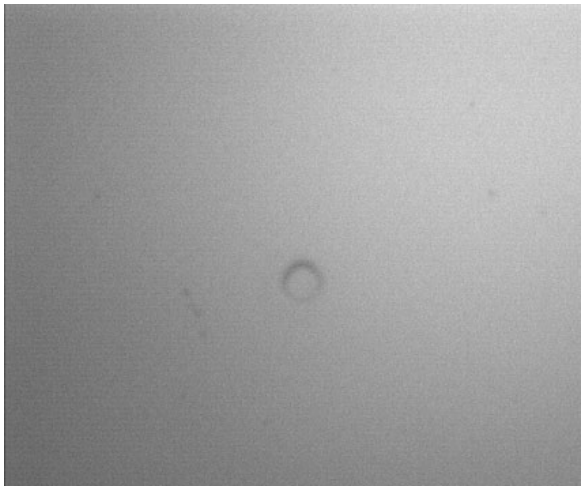


Figure 9.32: Microscope image of an impression of the 30 μm-wide flat-punch tip on photoresist.

While an indenter is typically used for measuring hardness and other mechanical properties of materials, here it was used to simulate probing of a DUT having pillar-based I/Os (Figure 9.33 (a)). As such, the classical interpretation of force-displacement curves does not

fully translate to the data obtained from indenting these MEMS structures. In addition, the interpretation of the measurements are further complicated by: (i) the fact that the tip is not indenting a planar structure; (ii) if the tip is offset from the center of the microsocket, then it will not contact all four cantilevers at the same time (the same issue occurs if the tip is aligned to the center of the microsocket, but any of the cantilevers are slightly higher or lower than the others); and (iii) the cantilevers are made of a heterogeneous stack of materials. These situations are illustrated in Figure 9.33.

A number of indentation experiments were conducted to understand the response of the microsockets to different loading conditions. These included single and repeated indents in the *quasi-static mode*, and repeated indentation in the *dynamic mode*. In the quasi-static mode, the load-function consists of discrete linear segments; a maximum of 50 segments may be applied. On the other hand, in the dynamic mode, a sinusoidally-varying load can be superimposed on the linear segments.

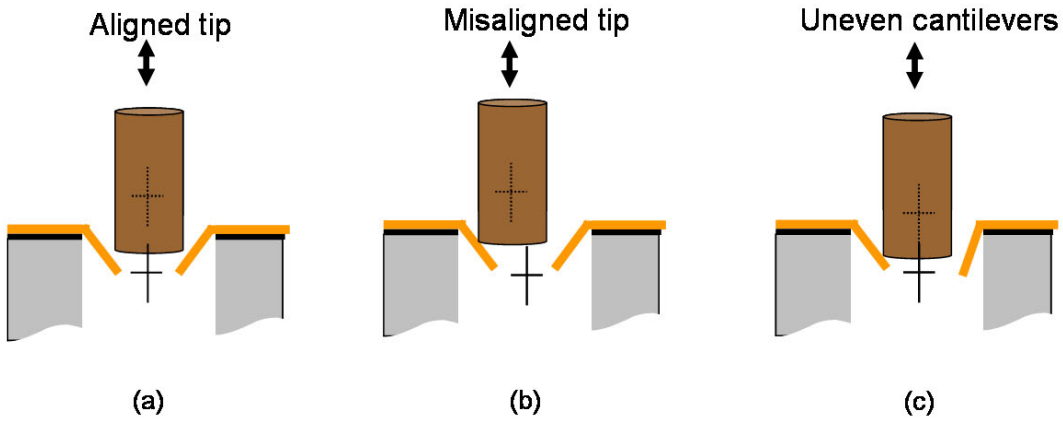


Figure 9.33: Illustrations of different scenarios that may occur when a probe microsocket is indented with the flat-punch tip: (a) Tip is aligned to the center of the microsocket, and makes contact with all cantilevers simultaneously; (b) Alignment offset between the tip and the center of the microsocket causes cantilevers to be indented one at a time; (c) Tip contacts cantilevers individually if the cantilevers are not at the same level for whatever reason.

9.4.1 Single Indents

Figure 9.34 shows the load-displacement curve for a gold-on-polysilicon (1 μm Au) probe microsocket with four 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick cantilevers. It was indented with a simple triangular load function with a peak load of 500 μN. The displacement during loading appears to be linear, but the initial portion of the unloading segment indicates residual plastic deformation (since there is a large drop in the force for a very small change in displacement). However, as the applied load approaches zero, there is a sharp decrease in the displacement.

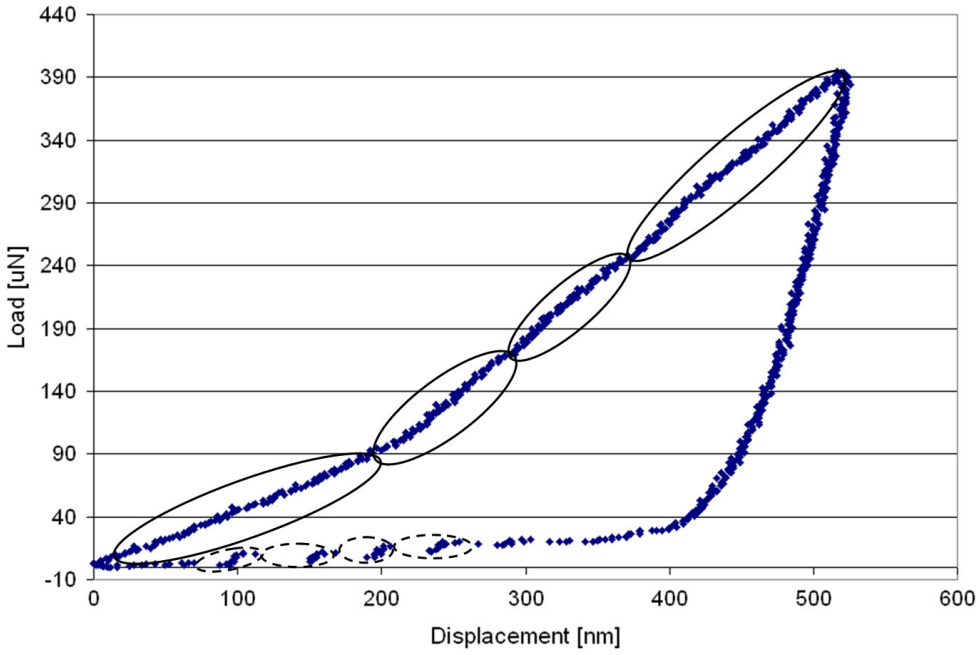


Figure 9.34: Load-displacement curve for a gold-on-polysilicon microsocket. A triangular load function with a peak load of 500 μN was applied on the cantilevers.

This behavior is perhaps indicative of time-delayed stress relaxation in the cantilevers. That is, when the load applied on the cantilevers is initially reduced, there is very little change in the displacement for a large reduction in the applied force, which makes it appear as if the cantilevers have undergone plastic deformation. However, after a short period of time ($\sim$7 s in Figure 9.34), there is a quick change in displacement for almost no change of force. This means that perhaps the microsocket cantilevers snap back to their original

position. Optical profilometer scans of the microsocket probes taken before and after indentation were about the same. This suggests that there was no plastic deformation of the cantilevers.

A closer examination of the loading and unloading segments of this curve reveals four distinct regions (Figure 9.34). For the loading section, the slope of the curve increases slightly at the onset of each of these segments. This non-linear characteristic can be explained if the tip makes contact with the cantilevers one at a time, either due to non-planarity of the tip surface or a slight alignment offset between the tip and the microsocket-center. In either case, the tip initially contacts just one cantilever, which is quite compliant. However, as soon as it contacts a second cantilever, there is increased resistance to the downward motion of the tip, which then displays itself as an increase in the slope of the curve. This is repeated as the tip subsequently contacts the third and fourth cantilevers. Similarly, four distinct artifacts are visible at the very end of the unload segment. As the tip loses contact with each cantilever, there is a sizable drop in the force for a very small change in displacement.

Load-displacement curves for the same microsocket probe (gold-on-polysilicon cantilevers, 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick) for triangular load functions with peak loads of 500 μN, 1000 μN, 1500 μN, and 2000 μN are plotted in Figure 9.35. Plots corresponding to the lower peak loads are almost completely enclosed within the ones for the higher peak loads. This implies that the mechanical response of cantilevers was unchanged for successive indents. Even though the 2000 μN peak-load curve seems to indicate a plastic deformation of around 2100 nm, no actual permanent deformation was observed. Once again, this could be attributed to the occurrence of time-delayed stress relaxation of the cantilevers.

During indentation, as the applied load is increased, the angled cantilevers deflect to make room for the tip. When the deflection is high enough, the tip will slide along the length of the cantilevers. Therefore, at higher loads, the tip would exert the load at a point closer to the free-end of the cantilever, giving rise to a larger moment. Closer inspection of the

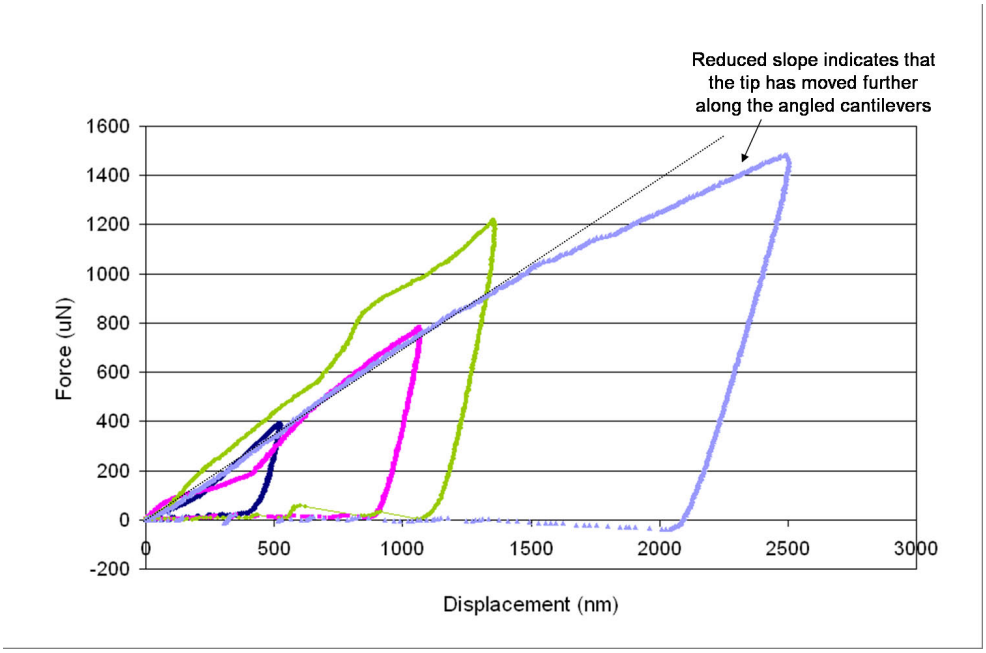


Figure 9.35: Load-displacement curves for gold-on-polysilicon probes indented with triangular load-functions with peak loads of 500 μN, 1000 μN, 1500 μN, and 2000 μN.

2000 μN peak-load plot in Figure 9.35 shows that the slope of the load segment decreases slightly beyond a load of $\sim$1056 μN. In other words, the cantilevers become slightly more compliant. This would be expected if the point of contact between the tip and the cantilevers has shifted closer to the free end of the cantilever.

A load-displacement curve for another probe microsocket with gold-on-polysilicon probes, 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick, is shown (Figure 9.36). The maximum displacement and the shape of the unload segment of this curve is very similar to the 2000 μN peak-load curve shown in Figure 9.35. On the other hand, the shape of the loading segment appears to be quite different and peculiar. This plot exemplifies an indentation scenario where the tip was perhaps offset from the center of the microsocket. Region I of the curve corresponds to the situation where the tip contacts a few (but not all) of the cantilevers. As the load is increased, the tip continues to slide lower into the socket, and as discussed earlier, the slope of the load-displacement curve slightly decreases. However, at some point, the tip contacts the remaining cantilever(s) and the slope of the load-displacement curve rises sharply.

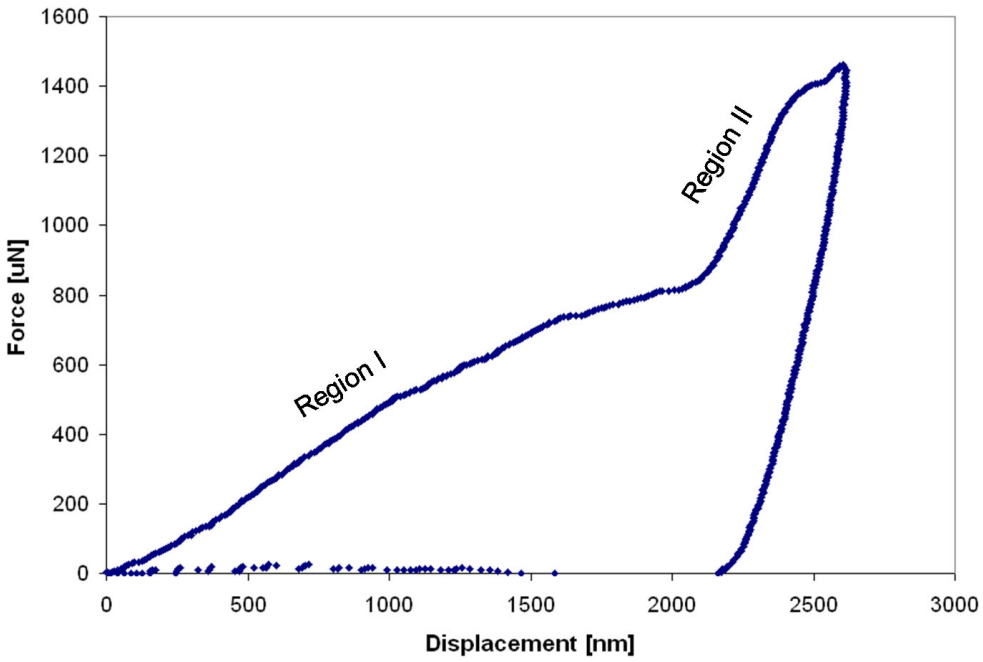


Figure 9.36: Load-displacement curve for a (1 μm Au) gold-on-polysilicon microsocket probe with 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick cantilevers. The initial portion of the loading segment resembles that for other similar microsockets. However, around 2000 μN, The slope of the curve rises sharply.

From intuition it is easy to conclude that the compliance of a cantilever decreases as it gets wider. This was verified with the finite element simulations performed in Chapter VII (Figure 7.30). Figure 9.37 plots the load-displacement curves for two probe microsockets made of gold-on-polysilicon (1 μm Au), and 35 μm long $\times$ 3 μm thick. The only difference was that one was that cantilevers in one were 20 μm wide and the other 15 μm -wide in the other. They were indented with a flat punch tip, following a triangular load function with a 2000 μN peak load. The curve for the 20 μm-wide cantilevers is a little to the left of the one for the 15 μm-wide ones – the (probe microsocket with) wider cantilevers undergoes less displacement for the same applied force.

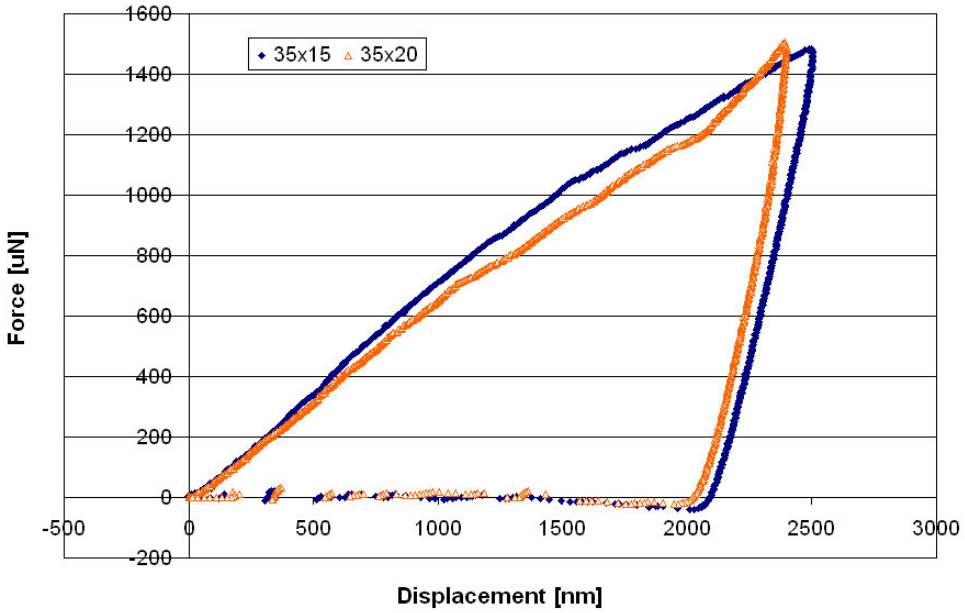


Figure 9.37: Load-displacement curves for probe microsockets with cantilevers 20 μm wide and 15 μm wide. All other dimensions were identical; they were both made of gold-on-polysilicon; and indented with a triangular load-function (peak load= 2000 μN).

9.4.1.1 Broken cantilevers

Figure 9.38 shows a load-displacement curve for a microsocket (gold-on-polysilicon cantilevers, 35 μm long $\times$ 20 μm wide $\times$ 3 μm thick) where a cantilever broke during the indentation. When this happens, the tip slips into the through-wafer via. On the plot, this corresponds to the large increase in diplacement with no change in force. The safeguards built into the indenter software prevent the tip from crashing into the substrate. The cantilevers were loaded with a 4000 μN peak-load triangular load-function. Figure 9.39 shows the load-displacement curve for a subsequent indent on the same microsocket, which now had only three cantilevers. This load displacement curve appears to have the general characteristics that have been observed for microsockets with four cantilevers. This is an interesting result as it shows that the probe microsockets could be used for probing even if one or more of the microsocket cantilvers breaks.

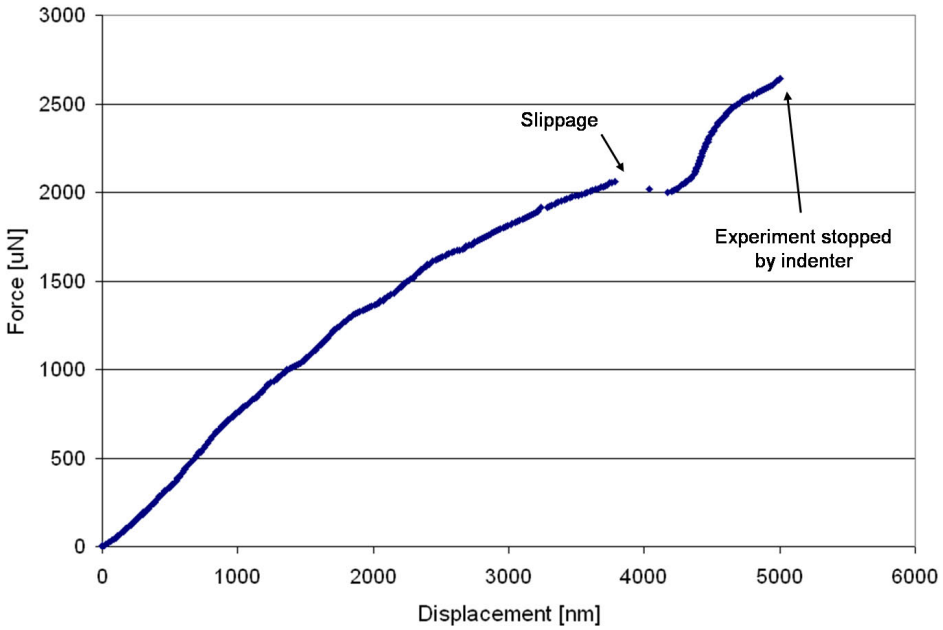


Figure 9.38: Load-displacement curve for a gold-on-polysilicon microsocket with cantilevers that were 35 μm long $\times$ 20 μm wide $\times$ 3 μm thick. In this case, the cantilever broke, which lead to slippage of the tip and then finally the abortion of the experiment to prevent the tip from crashing into the substrate.

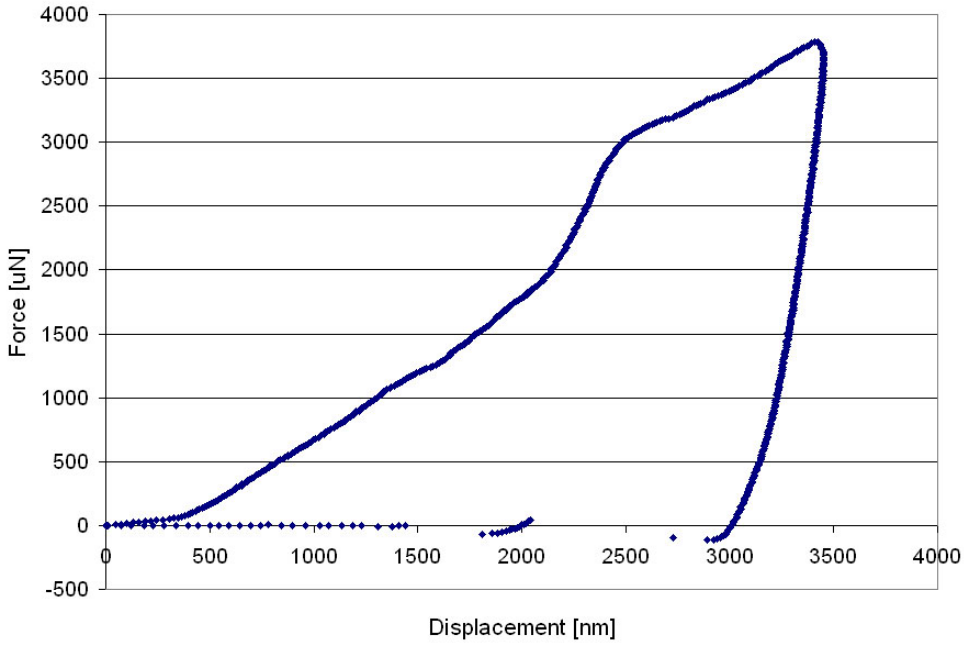


Figure 9.39: Load-displacement curve for an indent immediately following fracture of a single cantilever. Even with only three cantilevers, the microsocket seems to be mechanically functional.

9.4.2 Repeated Indents

This section covers additional indentation measurements that were made to understand the response of the probe microsocket cantilevers to mechanical cycling.

9.4.2.1 Quasi-static mode

Figure 9.40 shows multiple load-displacement curves for a probe microsocket (gold-on-polysilicon cantilevers, 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick) that was repeatedly indented with the same triangular load function in quick succession. The tip breaks contact with the cantilevers between each indent. The right-most curve corresponds to the first indent, and the left-most curve to the fourth indent. The curves, shift from the right to the left, and seem to indicate that the cantilevers are becoming stiffer (the maximum displacement reduces with each successive indent). Another trend clearly visible in the plots is that the slope changes significantly during the loading segment; also, this slope change occurs at smaller displacements in successive experiments. As seen from the single-indent measurements, particularly Figure 9.36, a change in the slope of the load-displacement curve during loading probably occurs when not all cantilevers are contacted at the same time by the tip; as mentioned before this could be due to an alignment offset between the center of the microsocket and the flat-punch tip or difference in height between individual cantilevers.

One hypothesis to explain the shifting of the point at which the slope changes is that the cantilevers being contacted by the tip first are undergoing a small amount of plastic deformation. As a result, with each successive indent, the difference in height between cantilevers is reduced and therefore, the change in slope occurs at a smaller displacement.

Continuing along these lines of measurement, a microsocket (1 μm Au), 35 μm long $\times$ 20 μm wide $\times$ 3 μm thick, was successively indented 20 times in the quasi-static mode. Figure 9.41 shows the load-displacement curves obtained from this experiment. Only curves corresponding to the 1^{st}, 5^{th}, 10^{th}, 15^{th}, and 20^{th} indents are shown. Starting from the plot for the 1^{st} indent, the curves for subsequent indents first shift to the left (the cantilevers have apparently gotten stiffer) before moving to the right. The plot from the 20^{th} indent

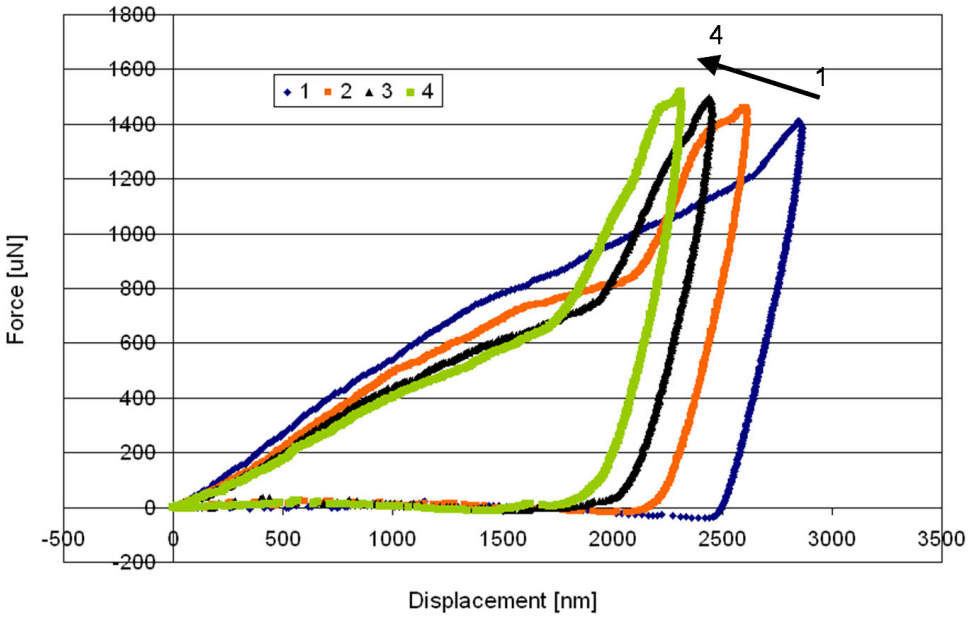


Figure 9.40: Curves showing the load-displacement response of a gold-on-polysilicon (1 μm Au, cantilevers: 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick) microsocket to four successive indents using a triangular load function with peak load= 2000 μN.

falls to the right of the 1^{st} indent; the cantilevers seem to have gotten more compliant.

Multiple loading and unloading steps are often performed in analysis of materials and MEMS structures to understand the reversibility of deformation [113]. Figure 9.42 illustrates a load-function with multiple loading and unloading steps that was used to indent microsocket cantilevers (gold-on-polysilicon, 35 μm long $\times$ 15 μm wide) of varying thicknesses. The hold steps help remove the influence of creep.

Figure 9.43 shows the load-displacement curve for a microsocket with 1 μm Au. During the 1^{st} hold segment, there is a small increase in the tip displacement. This can be attributed to the tip slightly sinking into the metal structure, to creep, or a bit of both. The cyclic loading and unloading cycles are different from the repeated indents discussed earlier as, in this case, the tip never breaks contact with the cantilevers. The general shape of the curve during these multiple load-unload cycles remains the same, only shifting a bit. Figure 9.44 shows SEM images of a microsocket, indented with this load-function, before and after indentation. Visually, these look almost identical. In addition, the distance between the

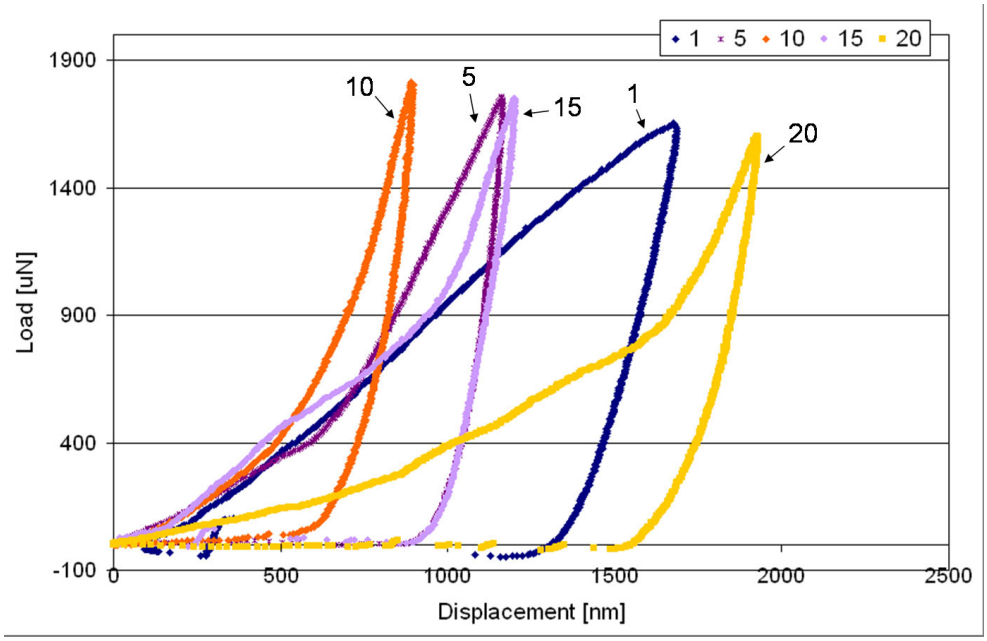


Figure 9.41: Curves showing the load-displacement response of a gold-on-polysilicon (1 μm Au, cantilevers: 35 μm long $\times$ 20 μm wide $\times$ 3 μm thick) microsocket to repeated indentation. The microsockets were indented a total of twenty times with a triangular load function (peak load= 2000 μN). The curves for only the 1^{st}, 5^{th}, 10^{th}, 15^{th}, and 20^{th} indents are shown.

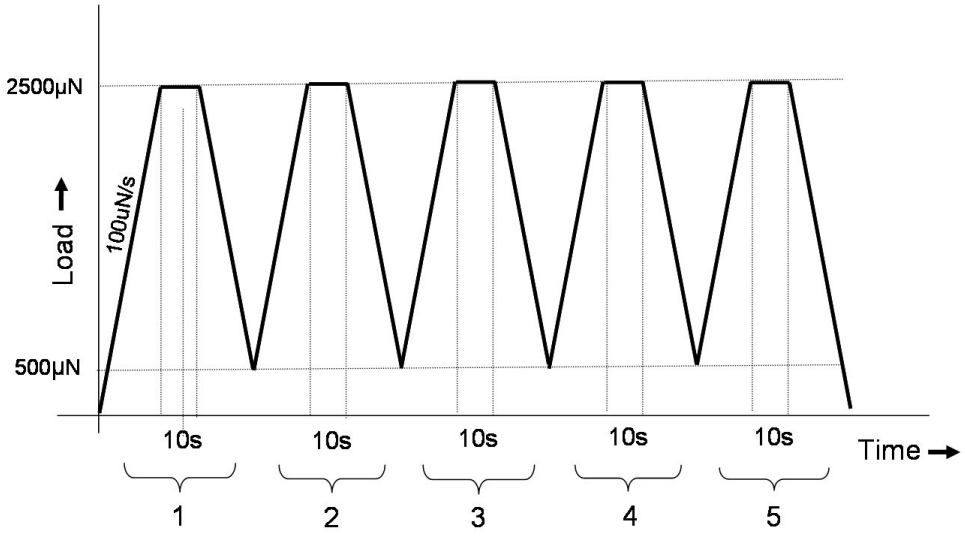


Figure 9.42: Load function with multiple loading and unloading steps that was used to understand the reversibility of deformation of the cantilevers.

substrate surface and the tip of the cantilevers remained about the same before and after indentation (< 0.5 μm). This is and indication that after 5 cycles of loading and unloading, there was almost no plastic deformation.

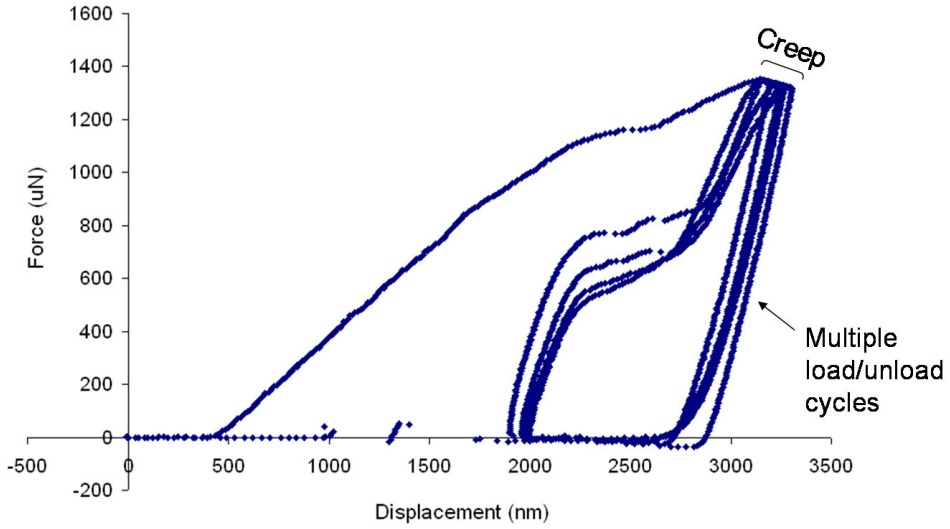
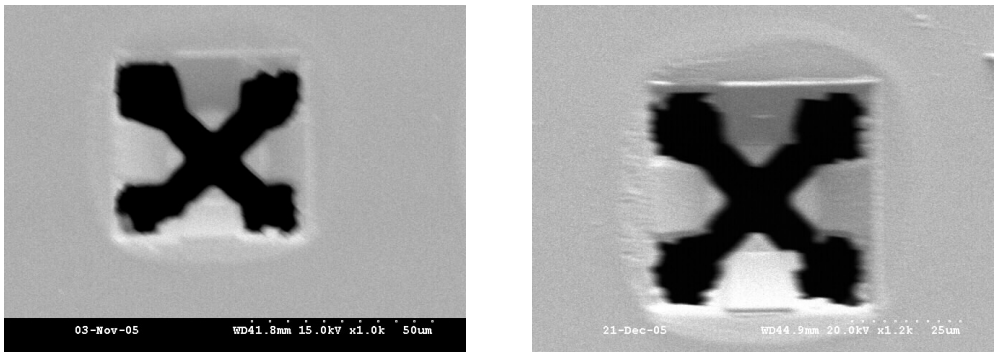


Figure 9.43: Load-displacement curve for a gold-on-polysilicon (1 μm Au) that was indented using the load-function in Figure 9.42. The cantilevers were 35 μm long $\times$ 20 μm wide $\times$ 3 μm thick.



(a) Before indent (b) After indent

Figure 9.44: SEM image of gold-on-polysilicon probe microsocket (1 μm Au) before and after indenting. The images look about the same except for a small cut in the metal in one of the cantilevers in (b).

The load-displacement data for a microsocket with 2 μm Au on polysilicon, having 35 μm long $\times$ 15 μm wide cantilevers, and indented with the load function in Figure 9.42,

is plotted in Figure 9.45. The multiple curves overlap each other quite closely, which is indicative of the ability of the cantilevers to return to their original positions. SEM images taken before and after indentation are shown in Figure 9.46. Once again, the distance between the substrate surface and the tip of the cantilevers remained about the same before and after indentation.

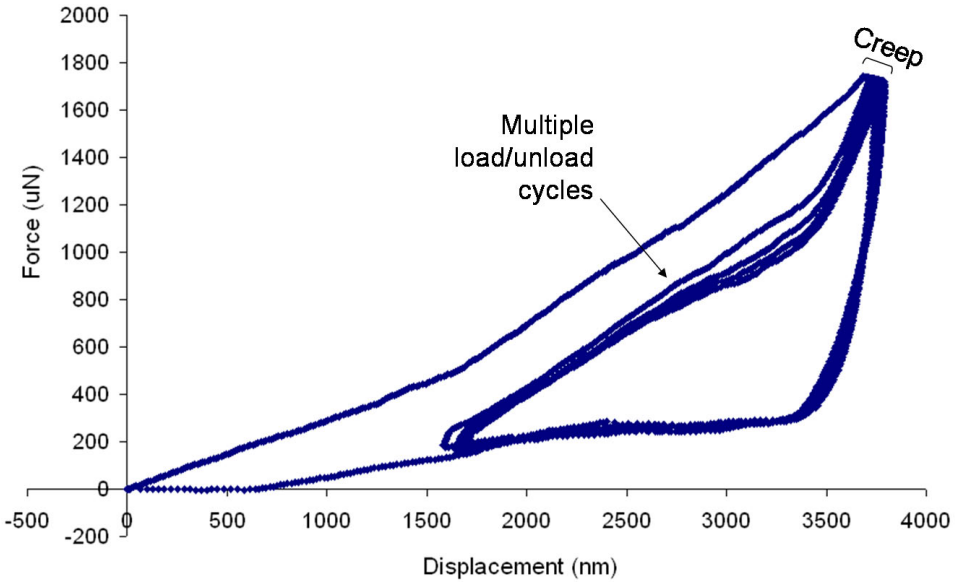
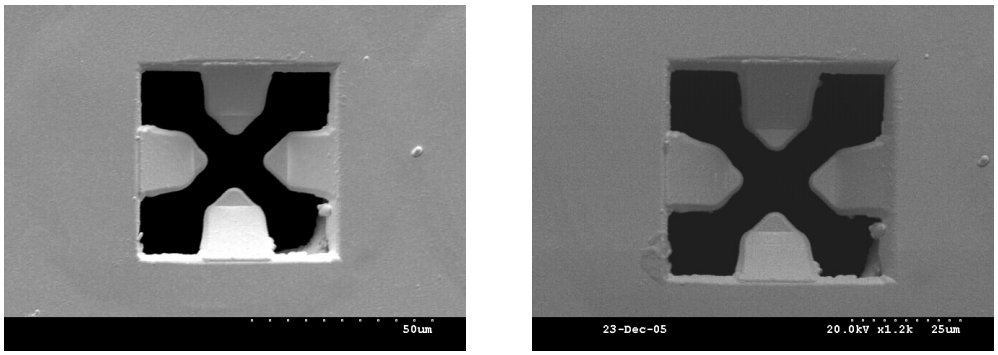


Figure 9.45: Load-displacement curve for a gold-on-polysilicon (2 μm Au) that was indented using the load-function in Figure 9.42. The cantilevers were 35 μm long $\times$ 20 μm wide $\times$ 4 μm thick.



(a) Before indent (b) After indent

Figure 9.46: SEM image of gold-on-polysilicon probe microsocket (2 μm Au) before and after indenting. There is no evidence of plastic deformation in the cantilevers even after multiple indents.

9.4.2.2 Dynamic mode

Repeated indentation in the quasi-static mode is limited by the fact that the load-function can only contain 50 discrete segments. On the other hand, in the dynamic mode, the Triboindenter can be programmed to apply a sinusoidally-varying load with frequencies up to 200 Hz. Performing repeated indentations in this mode enables high-cycle mechanical testing of the probe microsockets. In this testing mode, the Triboindenter performs a *continuous stiffness measurement*. The fatigue life of materials and MEMS structures can be predicted by plotting and analyzing the measured stiffness as a function of number of mechanical cycles. Typically, a drop in the dynamically-measured stiffness represents the onset of fatigue [113].

Figure 9.47 shows the form of a typical dynamic mode load-function that was used for characterizing the probe microsockets. The magnitude of the applied load was selected based on the quasi-static single indent measurements.

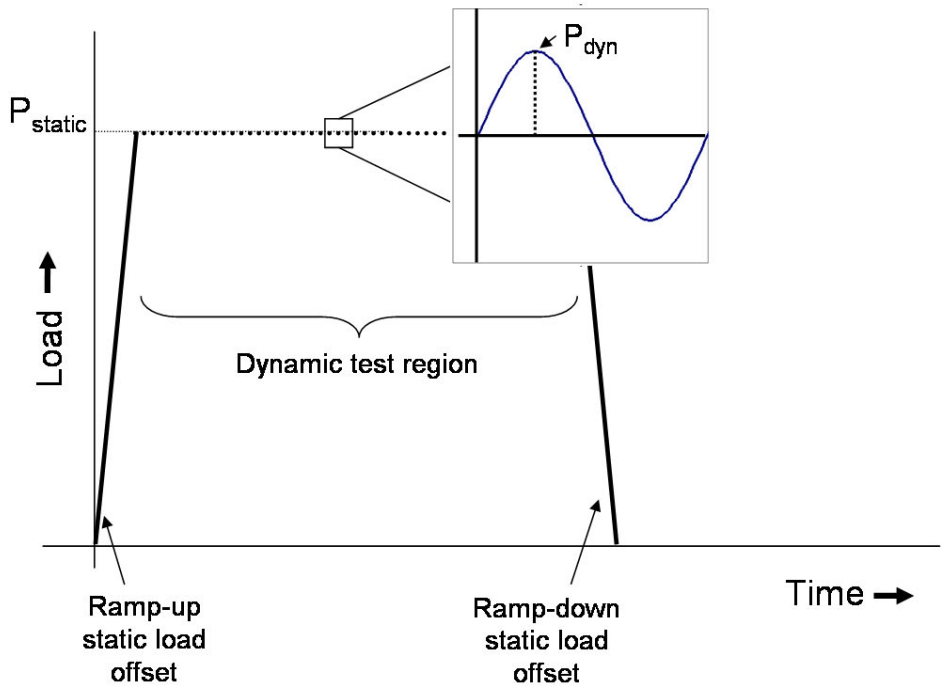


Figure 9.47: Typical load-function used for high-cycle testing of probe microsockets.

Figure 9.48 plots stiffness as a function of number of mechanical cycles for a probe micrsocket with (1 μm) gold-on-polysilicon cantilevers that were 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick. The applied load-function was set up to have P_{static}= 2000 μN, P_{dyn}= 500 μN, and f= 30 Hz. It is important to remember that in this measurement, the tip is constantly in contact with the cantilevers. As such, this experiment is really an extension of the repeated indents done in the quasi-static mode. In this case, the stiffness of the cantilevers increases slightly but levels off after a sizable time period. The number of cycles was calculated from the duration of test. The increasing stiffness can be attributed to some amount of strain hardening in the cantilevers. *As there is no sharp drop in the stiffness, it can be concluded that after 80,850 mechanical cycles, the cantilevers were not mechanically fatigued.* In addition, the absolute change in the stiffness is extremely small (only 0.18 μN/nm in this case).

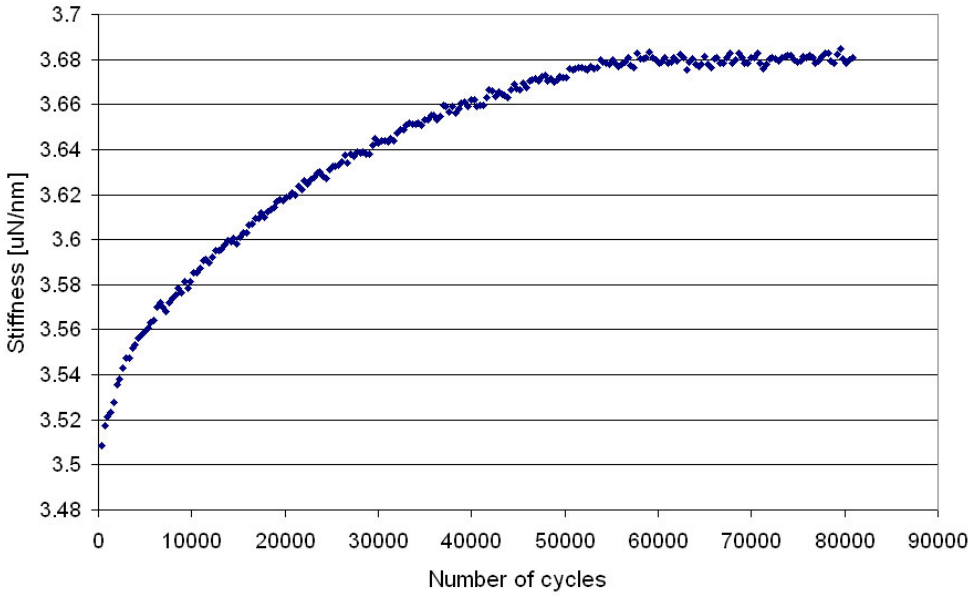


Figure 9.48: Plot of stiffness versus number of mechanical cycles for a gold-on-polysilicon microsocket (1 μm Au, cantilevers: 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick). The measurement was performed in the dynamic mode of the Triboindenter using a load function similar to the one plotted in Figure 9.47 (P_{static}= 2000 μN, P_{dyn}= 500 μN, and f= 30 Hz).

Unfortunately, a quirk in the Triboindenter software did not permit longer tests. To

get around this limitation, the indentation was repeated. Figure 9.49 plots the stiffness and tip displacement as a function of the number of mechanical cycles. This plot is for the same microsocket as Figure 9.48. Only here, a second dataset has been added. As can be seen from the plot, there is a discontinuity between the two sets of data. The stiffness resets to a lower value but then follows the same trend as the first dataset. On the other hand, displacement is a little higher in the second dataset. While part of this discontinuity could be attributed to measurement error in the tool, it could also be that after 80,850 touchdowns, the cantilevers have undergone some plastic deformation. [2] Therefore, when the tip is withdrawn and then re-engaged with the microsocket, the point of contact between the tip and the cantilevers has shifted slightly towards the free-end of the structures. If this is the case, the cantilevers will bend more for the same applied load, and the indenter will record a smaller value for the stiffness.

From indentation experiments, as the cantilevers are mechanically exercised without breaking contact, their stiffness increases. However, if after a large number of such cycles (that is, without breaking contact), the tip is withdrawn and then re-engaged, a lower stiffness is measured.

Figure 9.50 shows a plot of stiffness versus number of cycles for a similar microsocket as the one measured in Figure 9.49, and indented with the same load function (P_{static}= 2000 μN, P_{dyn}= 500 μN, and f= 30 Hz). Here, the stiffness increases initially, but begins to drop after 47,190 cycles. This indicates the onset of mechanical fatigue. This was not a consistent observation in the various probe microsockets that were indented. This failure could be ascribed to a notch or other imperfection in the cantilever material.

Figure 9.51 plots stiffness versus number of mechanical cycles for a probe microsocket with (1 μm) gold-on-polysilicon cantilevers that were 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick. In this measurement, the applied load-function was set up to have P_{static}=

[2] Earlier, it was deduced that there was little to no plastic deformation in the cantilevers. That conclusion was in reference to a small number of indents where the tip was withdrawn and re-applied to the cantilevers each time. The current scenario is different not only because the number of mechanical cycles is significantly larger, but also because the tip is always in contact with the cantilevers.

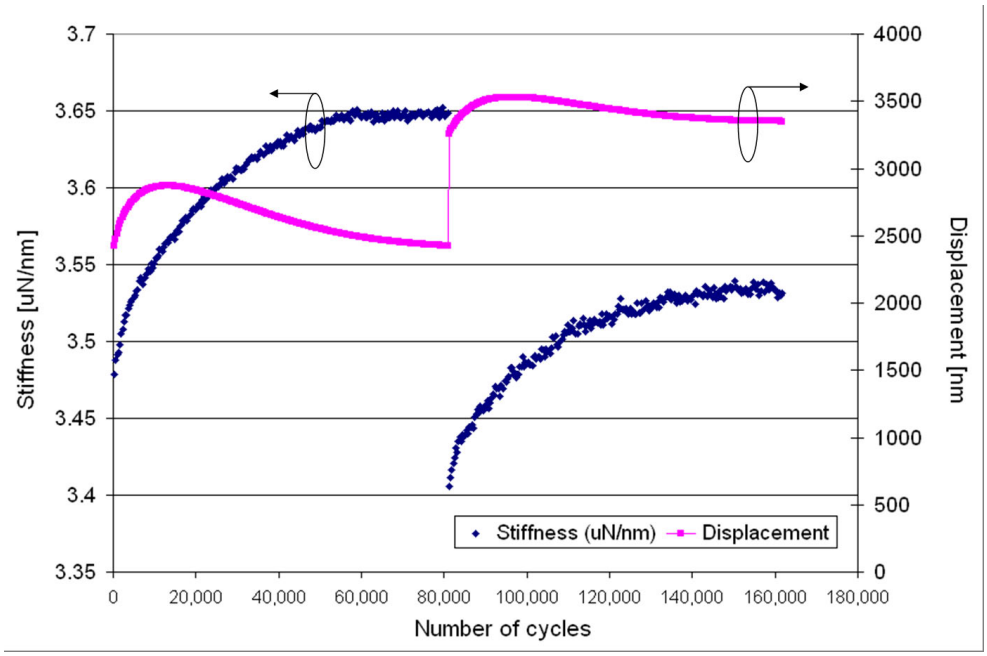


Figure 9.49: Plot of stiffness versus number of mechanical cycles for a gold-on-polysilicon microsocket (1 μm Au, cantilevers: 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick). The measurement was performed in the dynamic mode of the Triboindenter using a load function similar to the one plotted in Figure 9.47 (P_{static}= 2000 μN, P_{dyn}= 500 μN, and f= 30 Hz). The indenter only allowed 80,850 mechanical cycles at a time. As a result, two dynamic indentations were done to gather data over a larger number of cycles.

2500 μN, P_{dyn}= 500 μN, and f= 30 Hz. As seen in previous measurements, even with the increased static load, the stiffness of the cantilever tends to increase over time.

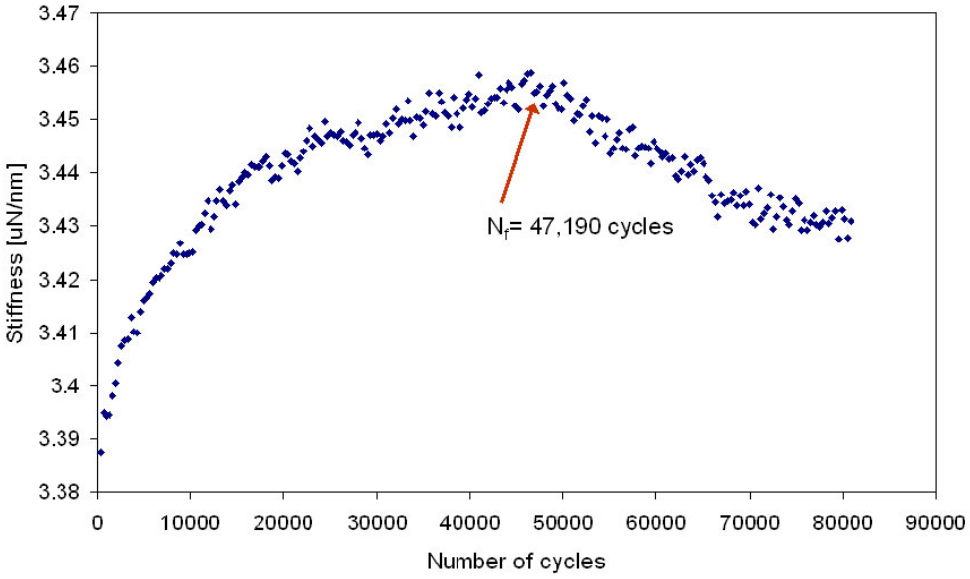


Figure 9.50: Plot of stiffness versus number of mechanical cycles for a gold-on-polysilicon microsocket (1 μm Au, cantilevers: 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick). The measurement was performed in the dynamic mode of the Triboindenter using a load function similar to the one plotted in Figure 9.47 (P_{static}= 2000 μN, P_{dyn}= 500 μN, and f= 30 Hz). At the end of 47,190 cycles, the stiffness drops considerably. Such behavior is indicative of the onset of fatigue in the MEMS cantilever.

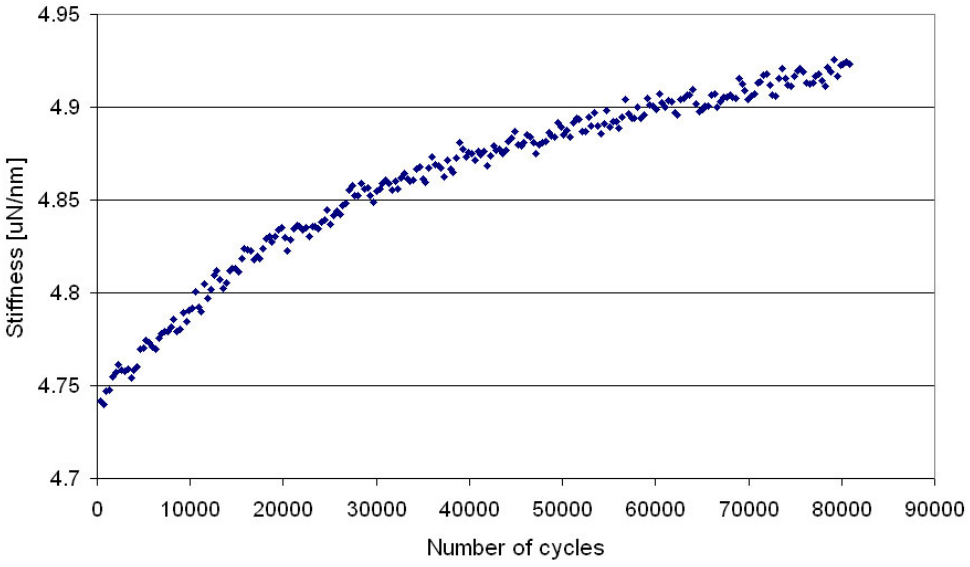


Figure 9.51: Plot of stiffness versus number of mechanical cycles for a gold-on-polysilicon microsocket (1 μm Au, cantilevers: 35 μm long $\times$ 15 μm wide $\times$ 3 μm thick). The measurement was performed in the dynamic mode of the Triboindenter using a load function similar to the one plotted in Figure 9.47 (P_{static}= 2500 μN, P_{dyn}= 500 μN, and f= 30 Hz).

9.5 Conclusion

This chapter has detailed the numerous experiments performed to characterize the electrical, optical, and mechanical properties of the prototype MOEMS probe substrate. The probe substrate was used to successfully couple optical power into the optical pillar I/Os (as much as ∼40%), make low resistance contact with the electrical pillar I/Os (R_{cont}= 0.52 Ω), and survive 160,000 touchdowns without mechanical fatigue. While there is some room for design optimization to improve these results, this is a solid demonstration of a probe substrate which could be used for step-and-repeat wafer-level testing of chips having electrical *and* optical I/O interconnections.

CHAPTER X

CONCLUSIONS AND OPPORTUNITIES FOR FUTURE WORK

10.1 Introduction

The desire to build systems with terabits-per-second bandwidth and low-power operation is driving the semiconductor industry to explore solutions for realizing manufacturable OE-GSI chips. Knowing how to test such chips will be a critical piece of this solution. Prospects for wafer-level testing of chips with electrical *and* optical I/O interconnects have been explored in this work. The salient accomplishments of this research are summarized in the next section. This is followed by a discussion on opportunities for future work.

10.2 Salient Accomplishments

1. **Probe module requirements**: The requirements for a probe module for wafer-level testing of chips with electrical and optical I/O interconnects were derived. These provide the directions from which practical solutions for achieving the same can be realized. The requirements were divided into three levels: (i) at the *contact* level; (ii) at the *substrate* level, and (iii) at the *system* level.

2. **Electrical and optical through-wafer interconnects**: Through-substrate interconnects are an efficient way of transferring signals from one side of a substrate to another. Electrical and optical through-wafer interconnects were successfully built and demonstrated in this research. Through-substrate electrical signal transmission was achieved by lining or filling through-wafer vias with a conductive material (for example, copper or doped polysilicon). Similarly, through-substrate guided-wave optical transmission was achieved by filling through-wafer vias with an optically transparent

polymer (Avatrel 2580-20). The polymer-filled vias were also successfully process integrated with mirror-terminated waveguides. While the electrical and optical through-wafer interconnects were devised for transferring signals from the probes to the redistribution substrate (within the probe modules), they could also be used for interconnecting stacked layers in a heterogeneous 3D microsystem.

3. **Compliant probe substrates for testing high pin-count chips**: Compliant leads, originally designed for use as chip-to-module interconnections, were modified for use as high-density electrical probes (325 μm pitch$\approx 10^3$ probes/cm^2) for contacting DUTs with solder bump I/Os. The contacts of these batch-fabricated electrical probes were made of electroplated gold-on-nickel, and the average R_{cont} was measured to be 0.5 Ω.

4. **Electrical and optical probe substrate**: The compliant probe substrate was upgraded to include optical probes, consisting of two-material, grating-in-waveguide optical interconnects. A typical coupling coefficient of 3.95 mm^{-1} was measured. This was a first-time demonstration of a joint electrical and optical probe substrate for wafer-level testing. Such a probe substrate enables a variety of probe module configurations as well as novel wafer-level test methods (such as optical loopback testing).

5. **High-density MOEMS probe modules for testing chips with polymer pillar-based I/Os**: Numerous probe module configurations for testing chips with electrical and optical I/Os were devised. Finally, MOEMS design and fabrication technology was used to realize (design, build, demonstrate, and characterize) a high-density (100 μm pitch$\approx 10^4$ probes/cm^2) prototype probe substrate for contacting chips with polymer pillar-based electrical and optical I/Os. The probe substrate was used to successfully couple optical power into optical pillars (as much as 40%), make low-resistance contact with electrical pillars (R_{cont}=0.52 Ω), and survive >160,000 mechanical indents.

10.3 Opportunities for Future Work

A tangible outcome of this research, as described in previous chapters, has been the design and fabrication of probe hardware to interface OE-GSI chips during wafer-level testing. While prototypes of this hardware were successfully demonstrated, there is plenty of room for future work. This can be broadly divided into three categories: (i) Joint electrical and optical testing, (ii) Novel interconnects for 3D integration; and (iii) Probe modules for wafer-level electrical and optical testing.

10.3.1 Joint Testing of Chips with Electrical and Optical I/O Interconnects

An important aspect of testing OE-GSI chips is to develop methods for testing optical I/Os that would fit in as a part of the GSI chip's test methodology. The challenges and opportunities for this are discussed herein.

10.3.1.1 OE testing: background

A primary application of OE devices, so far, has been for use in high-speed fiber optic communication networks. These networks are comprised of discretely packaged OE devices interconnected with optical fibers.

Akin to Si ICs, semiconductor OE devices, such as photodetectors and vertical cavity surface emitting lasers (VCSELs), are also built and tested at the wafer-scale [18,20]. However, these are individual devices, and testing them requires no more than a handful of electrical probes and a single optical probe. The purpose of such testing is to characterize the OE device. Tests may include measurement of responsivity, response time, and leakage currents, for photodetectors; and L-I-V (light-current-voltage) characterization, optical spectrum analysis, and optical power measurement, for VCSELs.

Once the OE devices are packaged for use in large-scale fiber optic systems, a different suite of tests is performed on them and on the optical link as a whole. Device testing may include modulation analysis, jitter testing, estimation of extinction ratio, and response time measurements. The quality of the link is assessed by measuring the bit error rate (BER)

and jitter [114].

It is clear from the above discussion that a vast amount of know-how exists for testing OE device-based fiber optic communication systems. *While the fundamentals behind testing such discrete OE devices and fiber optic systems would also hold for testing OE-GSI chips, the problem cannot be simply solved by scaling these optical test strategies down to the chip-level. OE-GSI testing is a different playing field with a different set of constraints.*

10.3.1.2 Why is OE-GSI testing different?

For one, on an OE-GSI chip, measurement of OE device parameters would be confined to characterization testing during initial phases of product development or to in-line testing during high-volume manufacturing. Even a simple measurement of responsivity of an optical input, consisting of an optical I/O, a photodetector, and a receiver circuit, would require at least one optical probe and two electrical probes (for current/voltage sensing). This model may not scale – it may not be feasible to insert two additional electrical I/Os for every optical I/O on the the chip solely for making it testable. An optical DFT method, which would perhaps reduce the total number of I/Os needed for testing the on-chip optical elements is desirable.

In fiber optic links, BER is an all-inclusive metric for link performance. BER is a statistical parameter, and stable measurements are achieved by continually monitoring this metric over a *gating time, t*, which is long enough to record 50-100 errors [114]. For data communication at the chip-level, only a BER better than 10^{-15} (that is, <1 error in 10^{15} bits transmitted) is acceptable [114]. Even if a pseudorandom bit stream is input at 1 Gb/s, measuring 50 errors could take > 13,000 hours (if BER of the link is indeed 10^{-15}). Clearly, this is not feasible. Therefore, only highly reduced-BER testing appears to be feasible at the chip-level. Owing to the short length of chip-to-board optical links, BER may not even be an appropriate test. There is much room for research in this area.

Finally, the difference in physical scale between a fiber optic link and an on-chip optical I/O is another reason that necessitates innovation in test methods. High-speed optical test

equipment can be quite expensive. Therefore, test methods which minimize this overhead will be welcomed by manufacturers. For wafer-probing, a major challenge is to develop probe modules which would allow high-precision, temporary interconnection of a multitude of electrical and optical I/Os, in a chip-size area, to automated test equipment.

10.3.1.3 Challenges

Wafer-testing of chips with electrical and optical I/O interconnects presents numerous challenges. A few of these are summarized below:

1. *Repeatable acceptable optical alignment:* Alignment between optical components is a daunting task even if it is done manually. During wafer-level testing, alignment needs to be achieved rapidly as the probe module is stepped from one chip to another. Misalignment and poor optical coupling between the probe module and the DUT I/Os would be perceived as a missed contact. Therefore, either probers need to be built with tighter alignment tolerances, or some kind of misalignment compensation needs to be built into the probe modules.

2. *Tests for Optical I/Os:* There are numerous tests which can be carried out to ascertain the performance of OE devices, optical couplers, and optical interconnects. Perhaps, a majority of these may be used during the research and development phase of an OE-GSI product chip. However, during production, only rapid high-confidence tests are acceptable. In addition, these tests need to be integrated with the test plan for the entire chip.

3. *Test equipment:* The kind of tests on chips with optical I/Os is closely associated with the equipment that would be needed. Typically, high-precision optical and high-speed test equipment is very expensive. The challenge lies in testing the chip with as low equipment capital costs as possible.

4. *Thermal effects:* A temperature difference between the probe substrate and DUT can cause them to expand at different rates if there is a mismatch in their respective

coefficients of thermal expansion (CTE). This may result in missed contacts between the probes and the DUT I/Os. In addition, thermal variations affect optical signal transmission and devices. To avoid this, systems for joint electrical and optical testing ought to have sound thermal management mechanisms. This may be achieved by smart test scheduling to minimize power dissipation [115], or by physical means such as liquid cooling of the back-side of the wafer-under-test [116].

5. *Optical signal distribution:* The function of an optical input on the chip is to convert the incoming optical signal to a logic-level voltage. Based on the efficiency of the photodetector and transfer characteristics of the receiver circuitry, one can estimate the minimum amount of optical power that must be coupled to the detector to achieve a logic-level voltage swing. The power loss budget of the probe substrate (that is, a sum of all optical distribution elements) can then be estimated as the difference between the optical power output of the source (on the ATE or the probe substrate) and the minimum input required at the optical input to the chip. Failure to remain well within this loss budget would mean that the optical input on the chip does not receive enough power to generate the logic-level swing. This scenario can be equated to a missed contact. Therefore, it is important to pick the optical redistribution elements with enough tolerance to prevent this from happening. Of course, a similar calculation for the reverse optical path can also be done.

10.3.1.4 Radical test methods

This new domain of manufacturing testing of OE-GSI chips is a unique opportunity for test engineers to think outside the box and devise high-confidence yet inexpensive test methods for OE components in a conventional semiconductor testing framework. For example, just two such ideas are described below.

When a conventional probe card is brought in contact with an all-electrical DUT, among the first tests performed is a continuity check to verify that the probes are in contact with the I/Os of the DUT. Continuity tests make use of the electrostatic protection circuits

on the chip [117]. The development of an analogous *contact* test for optical I/Os would be beneficial. This optical contact test could be used to not only verify that the optical components on the probe substrate are achieving good optical coupling with the I/Os of the DUT, but also that the optical I/Os are functioning to specification.

1. Optical time domain reflectometry (OTDR) is a technique commonly used for assessing optical links which have numerous optical interfaces and connectors. An optical signal is fed into a *golden* optical link, which is representative of an actual working link. Owing to discontinuities in the optical link (interfaces and connectors), some amount of the incident light will be back-scattered to the input. The reflected light and the round-trip delay in the calibration link serve as a reference to which other links can be compared. For example, if a large amount of inserted power is back-scattered then it signals a bad optical interface or connector. Therefore, a measurement of this sort can be extrapolated to determine whether a link is performing within specification and if not, then the location of the failure can also be determined.

2. Another contact test for optical outputs on the DUT could employ an image processing element. During the test, electrical signals are input to the DUT so that all the optical outputs begin emitting light. An image capture device, such as a charge coupled array camera, could then be used to take a picture of the sample, and image processing methods could be used to determine not only whether all the outputs did indeed light up, but also whether the output intensity was within expected limits.

10.3.2 Novel Interconnects for 3D Integration

The probe modules designed and built during the course of this dissertation research required stacking multiple substrates. Electrical and optical through-wafer interconnects were fabricated to enable this 3D integration. These vertical interconnects would also be suitable for stacking (multiple) gigascale, optoelectronic, and microfluidic chips to yield a heterogeneous 3D microsystem. Therefore, a natural extension of this work is to optimize the design

and fabrication of these vertical electrical and optical interconnects for 3D integration applications.

10.3.2.1 Electrical through-substrate interconnects

In this work, electrical through-wafer interconnects were built either by lining the sidewalls of a through-wafer via with a conductive thin-film or by completely filling the through-wafer vias with a conductive material. Some suggestions for future work are listed below.

1. Daisy-chains of copper-filled through-wafer interconnects (50 μm diameter $\times$ 400 μm height) were shown to survive 400 thermal cycles. A complete reliability study and failure analysis of these interconnect structures would be quite relevant and useful for optimizing these interconnect structures as well as for making necessary design and material modifications.

2. If a CTE mismatch between the metal filling and the substrate does prove to be a reliability concern, then electrical through-wafer vias could be built by lining the sidewalls with a conductive film of choice and then filling the center of the via with a polymeric material to serve as a buffer (Figure 10.1 (a)). This is along the lines of the metal-lined through-wafer interconnects, filled with a conductive paste, proposed in [118]. In such a case, the thickness of the metal lining, and the choice of dielectric would need to be defined by the acceptable electrical parasitics.

3. Along the same lines, it could be quite beneficial to build co-axial through-substrate interconnects (Figure 10.1 (b)).

4. Finally, if the electrical through-wafer interconnects are placed in a critical path, then, depending on the actual design, it may be beneficial to develop and process integrate compatible thin-film passive electrical elements (such as matching resistors).

Figure 10.1: Possible implementations of electrical through-wafer interconnects: (a) Through-wafer interconnect filled with a CTE-matching buffer material; (b) Co-axial through-wafer interconnect.

10.3.2.2 Optical through-substrate interconnects

Polymer-filled through-wafer interconnects (Chapter IV) have a lot of potential as vertical optical interconnects for heterogeneous 3D microsystems. While a simple spin-on process was used to successfully fill the vias, and some preliminary optical power transmission measurements were made, there is much room for improving these procedures. Polymer-filled through-wafer interconnects can be used as the building block for some novel integrated optics structures. A few areas of future work include:

1. Improving the process flow to reduce roughness after via-filling and polymer-polishing, which may also enhance optical transmission.

2. Simulation and/or modeling of optical transmission in the polymer-filled vias.

3. Improved integration of the polymer-filled vias with mirror-terminated waveguides.

4. Quantification of power transmitted in the waveguide-mirror-TWI structure.

5. Integration of polymer-filled interconnects with other optical elements such as diffraction gratings, lenses, and active optoelectronic devices by nanoimprinting, hybrid attachment, or other post-processing techniques (Figure 10.2).

6. Determination of design rules to ensure that transmitted optical signals do not interact with the via sidewalls, which may lead to undesired reflections.

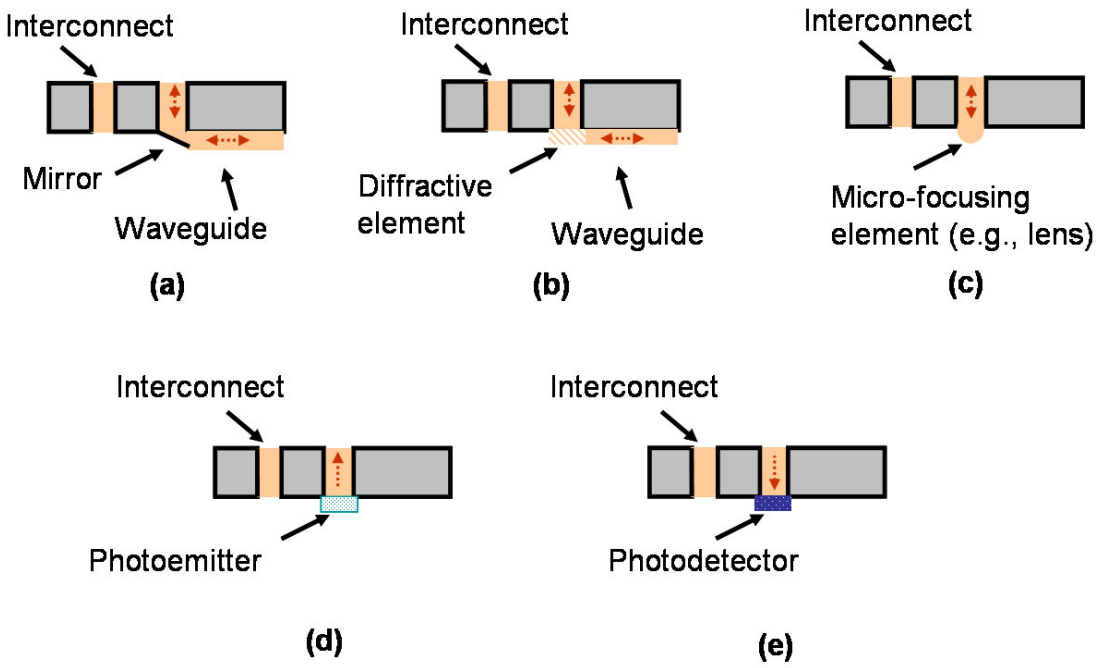


Figure 10.2: Schematic of polymer-filled through-substrate interconnects combined with: (a) a mirror-terminated waveguide, (b) waveguide and a diffractive element, (c) a micro-focusing element, (d) a photoemitter, and (e) a photodetector.

10.3.2.3 3D integration

These interconnect structures, and variations thereof, would find much use in 3D-integrated microsystems such as the one illustrated in Figure 10.3. Some considerations for achieving such a system are listed here.

1. The dimensions of the copper-filled through-wafer interconnects were selected for their use in the probe substrates. For use in 3D ICs, the dimensions of these interconnects would need to be much smaller, so that they do not occupy valuable real-estate on the chips, which could be used for active devices.

2. Electrical through-wafer interconnects could be used in all-electrical 3D ICs or in a heterogeneous 3D stack. In either case, these may co-exist with microfluidic through-wafer interconnects or optical through-wafer interconnects. Process integration of these different interconnect technologies would be an interesting, albeit challenging, task.

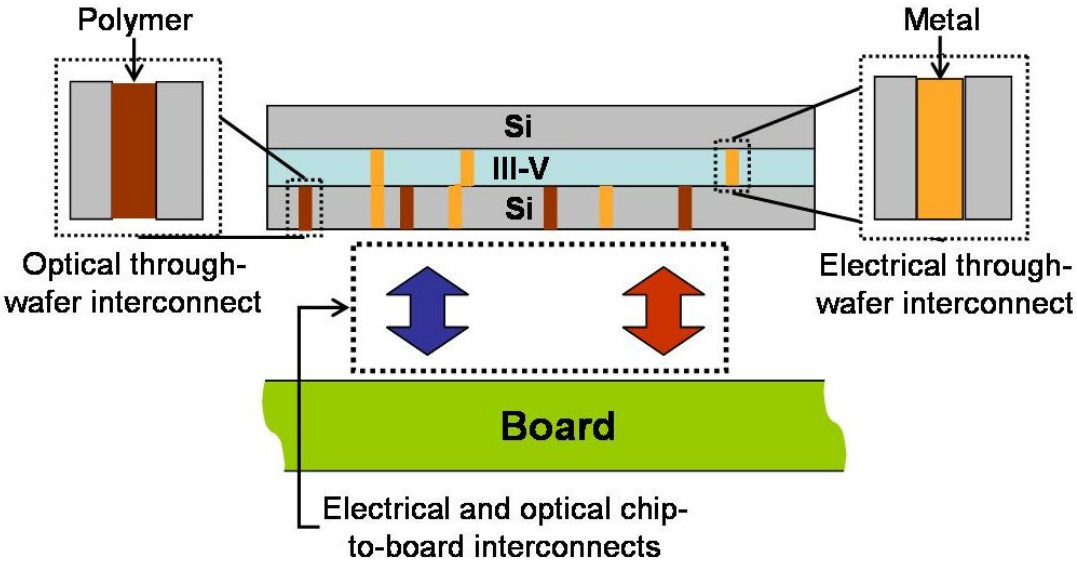


Figure 10.3: Schematic of a heterogeneous 3D microsystem. The different chips in the stack are connected with electrical and optical through-wafer interconnects.

10.3.3 Probe Modules for Electrical and Optical Testing

Prototype probe substrates with electrical and optical probes were described in Chapters V-IX. Their feasibility of operation was verified by simple experimental demonstrations and characterization testing of the individual components. In-depth reliability testing is required before either of these could be used in a manufacturing environment. This would include experimental simulation of actual operation and analysis of probe behavior (electrical, mechanical, and optical) as a function of high-cycle mechanical loading. A result of such testing would help determine how often the probe contacts would need to be cleaned as well as the appropriate cleaning procedure. Consequently, this will assist in the selection of proper materials for the probe contacts.

Additional suggestions for future work specific to the two kinds of probe substrates are summarized in the following sections.

10.3.3.1 Electrical and optical compliant probe substrates

In general, this probing solution is attractive because in some ways it is a shrunk-down version of traditional cantilever probe cards. They are compliant, and can be batch-fabricated at densities projected by the ITRS. Of course, in addition, they also have built-in optical probing capabilities. However, before such probe substrates appear on the foundry test floor, there are some additional questions that need to be investigated.

1. Electrical design and modeling of the interconnect structures (including the probes) on the probe substrate will be needed to ensure that they can be used for high-speed wafer-level testing.

2. From a fabrication perspective, there is a need to enhance the current fabrication procedures to achieve higher probe densities, build different (pointed) contact structures, and use more reliable materials for the contacts.

3. For optical probing, an immediate set of experiments is needed to determine the absolute power coupling efficiency of the grating-in-waveguide probes.

4. It would also be beneficial to investigate the fabrication and process integration of other forms of optical probes; which may include *focused* grating couplers, mirrors, and active optoelectronic devices; on this substrate.

10.3.3.2 MOEMS probe module

This probe module was designed and built to interface chips with very high-density electrical and optical I/Os. Thus far, only a simplified prototype probe substrate containing the core electrical and optical probing components has been fabricated and tested.

1. The mechanical design of the cantilevers in the probe microsockets needs to be optimized to minimize stress during loading, minimize contact resistance, and maximize probe lifetime. This could be achieved by altering the physical design of the cantilevers, by changing the material set (perhaps, even stressed metal cantilevers), or by

adopting a different structure such as microsockets with soft sidewalls. Some of these ideas are illustrated in Figure 7.15.

2. An interesting addition would be to develop appropriate fabrication methods to process integrate components such as optical couplers, waveguides, and active optoelectronic devices.

3. Electrical, optical, and mechanical simulation of these probe modules in a multi-physics environment will provide great insight into defining the limits of their operation. For example, it would be constructive to understand the effect of I/O-to-microsocket misalignment on cantilever compliance, optical coupling, mechanical lifetime, and electrical probing.

10.4 Conclusion

In this thesis, it was assumed that OE-GSI chips would operate with only a single wavelength of light. However, it has been suggested that such chips may employ dense wavelength division multiplexing (DWDM) to maximize bandwidth [119]. In addition, future gigascale chips may contain microfluidic channels and I/Os to maintain a specific temperature of operation [120]. Also, the improvements in interconnect performance enabled by stacking multiple chips [33] as well as the drive to integrate more computing power in a smaller form factor suggests that 3D integration may become more mainstream.

As conventional semiconductor technologies appear to reach their limits [121], it is expected that such novel interconnection and integration technologies will be implemented to extend Moore's Law. From a manufacturing perspective, it is equally important to know how to test these new technologies as it is to know how to build them. As such, wafer-level and microsystem testing promises to be an intriguing and fruitful area of research in the future.

APPENDIX A

PROCESSING RECIPES

A.1 Photolithography

NR9-8000 Negative Photoresist, Futurrex, LLC

i. 5 μm thick

Spin-on	5000 rpm, ramp @ 500 rpm/s, 50 s
Soft bake	2:00 min @ 100°C (hotplate)
	2:00 min @ 130°C (hotplate)
Exposure	110 mJ/cm^2
Post-exposure bake	2:00 min @ 100°C (hotplate)
Develop	00:45-1:00 min in Futurrex RD6 developer with agitation
Rinse	DI water
Nominal Thickness	5.2 μm

ii. 12 μm thick

Spin-on	2000 rpm, ramp @ 500 rpm/s, 40 s
Soft bake	Start at 70°C (hotplate), ramp to 100°C
	10:00 min @ 100°C
Exposure	263 mJ/cm^2
Post-exposure bake	2:00 min @ 100°C (hotplate)
Develop	∼1:00 min in Futurrex RD6 developer with agitation
Rinse	DI water
Nominal Thickness	12.5 μm

NR5-8000 negative photoresist; Futurrex, LLC

i. 10 μm thick

Spin-on	2000 rpm, ramp @ 500 rpm/s, 40 s
Soft bake	8:00 min @ 100°C (hotplate)
Exposure	250 mJ/cm^2
Post-exposure bake	2:00 min @ 100°C (hotplate)
Develop	∼1:00 min in Futurrex RD6 developer with agitation
Rinse	DI water
Nominal Thickness	10 μm

NR7-1500 negative photoresist; Futurrex, LLC

i. In ∼22 μm trench

Spin-on	2000 rpm, ramp @ 500 rpm/s, 40 s
Soft bake	1:30 min @ 110°C (oven)
Exposure	190 mJ/cm^2
Post-exposure bake	1:00 min @ 100°C (hotplate)
Develop	∼0:20 min in Futurrex RD6 developer with agitation
Rinse	DI water

SC 1827 positive photoresist; Shipley Company

i. 3.4 μm thick

Spin-on	1500 rpm, ramp @ 500 rpm/s, 15 s
	3000 rpm, ramp @ 500 rpm/s, 30 s
Soft bake	2:30 min @ 90°C (hotplate)
Exposure	130 mJ/cm^2
Develop	0:45-1:00 min in Microposit 354 developer with agitation
Post-exposure bake	2 min @ 115°C (hotplate)
Rinse	DI water
Nominal Thickness	3.4 μm

25% Avatrel 2190P

i. 6.0 μm thick

Spin-on adhesion promoter AP3000	3000 rpm, 1000 rpm/s, 30s
Spin-on	200 rpm, ramp @ 100 rpm/s, 5 s
	500 rpm, ramp @ 1000 rpm/s, 40 s
Soft bake	10:00 min @ 100°C (N_2 purged oven)
Cool down	10:00 min
Exposure	300 mJ/cm^2
Post-exposure bake	15:00 min @ 115°C (oven)
Cool down	10:00 min
Spray develop	0:20 min in Promerus Bioact developer
Rinse	Isopropanol
Nominal Thickness	∼6.8 μm

A.2 Plasma Etching

Photoresist: descum and strip

i. Plasma Therm RIE

Gases [sccm]	CHF_3= 15, O_2= 40
Pressure [mTorr]	250
Temperature [°C]	
Power [W]	400
Time [min]	descum: 00:15-00:45 strip: variable

Silicon Nitride

i. Plasma Therm RIE

Gases [sccm]	CHF_3= 45, O_2= 5
Pressure [mTorr]	115
Temperature [°C]	30
Power [W]	200
Time [min]	variable

Avatrel 2000P Polymer

i. Plasma Therm RIE

Gases [sccm]	O_2= 45, CHF_3= 5
Pressure [mTorr]	300
Power [W]	300
Time [min]	variable

Polysilicon

i. Plasma Therm RIE

Gases [sccm]	O_2= 7, SF_6= 13, Ar= 7
Pressure [mTorr]	30
Temperature [°C]	40
Power [W]	200
Time [min]	variable

A.3 Dielectric Deposition

Silicon Dioxide

i. Plasma Therm PECVD

Gases [sccm]	SiH_4= 400, N_20= 900
Pressure [mTorr]	900
Power [W]	30
Temperature [°C]	250
Deposition rate [Å/min]	400

ii. STS PECVD

Gases [sccm]	SiH_4= 400, N_20= 1420
Pressure [mTorr]	800
Power @ 13.56 MHz [W]	20
Temperature [°C]	300
Deposition rate [Å/min]	∼475

Silicon Nitride

i. Plasma Therm PECVD

Gases [sccm]	SiH_4= 200, N_2= 900, NH_3= 5
Pressure [mTorr]	900
Power [W]	30
Temperature [°C]	250
Deposition rate [Å/min]	100

ii. STS PECVD

Gases [sccm]	SiH_4= 2000 , N_2= 40
Pressure [mTorr]	900
Power @ 13.56 MHz [W]	20
Temperature [°C]	300
Deposition rate [Å/min]	140

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