Nonhermetic Plastic Packaging of High Voltage Electronic Switches Utilizing a Low-Stress Glob Coating for 95/5Pb/Sn Solder Joints of Flip-Chip Bonded Multichip Module High Voltage Devices

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***Abstract*— AT&T's number five electronic switching system (ESS) is a state-of-the-art electronic switch that uses solid-state gated-diode-crosspoint (GDX) for fast switching of telephone calls. These GDX's operate at 375 V and require exceptional protection and reliability performance of these packages. Ceramic hermetic packages were used for these type of devices. In order to reduce the cost of these GDX's, a new type of flip-chip bonded structure with 95/5 Pb/Sn solder joints GDX's was developed. These flip-chip GDX's were surface-mounted on a conventional ceramic substrate. An thixotropic silicone gel was used as an underfill and overfill glob-coating to provide the ultrahigh reliability performance of these high voltage devices and a silicone elastomer was used to pot the hybrid surface-mounted GDX multi-chip module structure to further enhance the robustness of its structure.**

In this paper, the materials such as the flip-chip solder (95/5 Pb/Sn), silicone gel, and elastomer, and their processes such as flip-chip bumping, reflow, cleaning, encapsulation and reliability testing are described for this robust, high performance and low-cost packages.

***Index Terms*— Elastomers, flip-chip, high voltage devices, MCM, nonhermetic packaging, silicone gels.**

I. Introduction

GATED diode crosspoint (GDX) is the state-of-the-art high voltage switch that operates at 375 V. This solid-state switch is used in AT&T's number five electronic switch system (ESS) that routes phone calls from customer premises to and from the telephone central switching offices. An ultrahigh reliability switch is required for this system. Conventionally, the GDX is packaged in a hermetic leadless ceramic package which is then surface-mounted on a ceramic hybrid IC (HIC) [1]. These GDX HIC's constitute a significant portion of the cost of the number five ESS. In order to cost reduce the number five ESS, an effort was carried out by nonhermetic packaging of this module. The nonhermetic GDX high voltage device was flip-chip bonded by solder bumping GDX devices with a 95/5 (Pb/Sn), then reflowed on a ceramic substrate. Silicone gel was used to glob-coating of the flip-chip GDX devices both as underfill and overfill for reliability protection [2], [3].

The flip-chip solder (95/5 Pb/Sn) bumping process, the reflow, cleaning, encapsulation and reliability testing of the GDX HIC are described as follows.

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II. Experimental

A. Flip Chip Solder (95Pb/5Sn) Bumping Process

To reduce the cost of the 5ESS switch, the expensive hermetic ceramic chip carrier is being replaced by direct flip chip solder bonding of the Si IC's onto the ceramic hybrid IC followed by nonhermetic gel encapsulation. The flip chip bonding process developed for this purpose has to be compatible with all wafer codes used in the HIC, including gated-diode-crosspoint (GDX), linear CMOS, and digital bipolar devices. The process has to satisfy the following criteria:

1) approaching 100% bumping yield (defined as the ratio of the number of good devices after bumping to the number before bumping);
2) passing the specified THB (temperature-humidity-bias) qualification test;
3) transparency to different device codes;
4) robustness in manufacturing.

The solder composition selected for this process is 95%Pb–5%Sn, which has a higher melting point than eutectic solders. This is appropriate for chip level bonding to ensure integrity of joints during subsequent board-level reflows. The solder joint itself is the sole mechanical and electrical interconnection between the Si IC and the ceramic HIC. These different substrate materials, with vastly different coefficients of thermal expansion, will induce stress in the solder joint during thermal cycling. To ensure sufficient thermal-fatigue life in the solder joints, a joint height of 75 μm has been specified. The smallest bump pitch among the wafer codes is on the order of 150 μm. For simplicity, the entire volume of solder is to be deposited on the Si chip. The ceramic HIC will have contacts finished with the appropriate interface metals for wetting and joining to the solder.

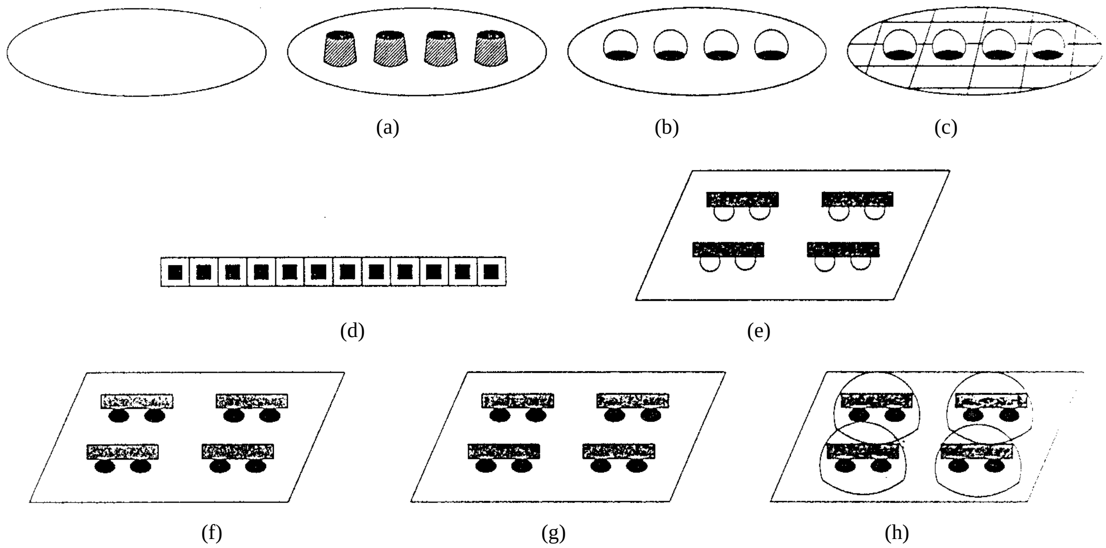

Fig. 1. Flip-chip GDX HIC process flow-chart.

The entire process from a finished Si wafer to solder mounted and encapsulated flip chips on the ceramic HIC is shown in Fig. 1. This section addresses part A: the act of forming solder bumps of appropriate dimensions and properties on individual Si wafers. The best known wafer scale solder bumping process in production is IBM's C4 (controlled collapse chip connection) process [4], which is based on evaporating base metal layers and solder through a metal mask aligned onto a wafer. Electroplating of solder is also in production, although on a smaller scale. Currently, there are many processes for this type of flip-chip interconnection technology [5]–[11].

B. Assembly of Flip Chips onto Ceramic HICs

Bumped Si IC's are flip-chip bonded onto ceramic HIC's for multichip modules which are then assembled into boards for the 5ESS. The landing site for the Si chips consists of a layout of contact pads resembling the layout on the Si chip. The base metals on the ceramic is a multilayer stack of Ti/Pd/Cu/Ni/Au, with layer thicknesses typically higher than those used on Si. The bumped Si chips are first temporarily mounted onto the ceramic module using a procedure known as "tacking." In this process, the ceramic substrate is held on a bottom platen at a temperature about half of the reflow temperature, and a fluxed Si chip is held on a mechanical pick-up tool. Optics are arranged such that the layout of the solder bumps are superimposed on the layout of the contact pads on the ceramic. Alignment is done, and the Si chip is brought into contact with its ceramic mate, with a slight pressure being imposed in the process. With the correct settings of temperature, pressure and tacking time, the solder will soften enough to initiate adhesion with the contact pads. The sticky flux also helps hold the ensemble together. The alignment only has to be accurate to within one pitch of the pads, because of the property of self-alignment, which will be described later. The temporary assembly is then sent through a reflow oven similar to the one described earlier.

During this reflow, which is aided with the applied flux, the solder bump from the Si chip wets the base metal layers on the ceramic HIC and spreads to the extent defined by the base metal pad. The bump shape transforms from a sphere truncated on one side to one truncated to two sides. If the bump is initially misaligned with respect to the bond pad on the ceramic HIC, surface energy forces will bring the chip into alignment such that a near-perfect truncated sphere can be formed. This property is known as self-alignment and is an important benefit of the solder reflow process. It relaxes the tolerance for mechanical alignment of chip to module tremendously.

With the proper reflow parameters, flipped chips will self-align onto their mating substrates and solder joints will approach their equilibrium shape as dictated by the relative dimensions of wettable diameters and joint height. Under these conditions, the solder joints will have an equilibrium density and uniform distribution of porosity. These microvoids have been shown to exist in healthy joints and do not appear to have any effect on the mechanical strength of the joint. On the other hand, a poor reflow process could result in chip misalignment, distorted joint shapes which lead to localized areas of concentrated stress, and macrovoids within the solder. These effects could promote drastically different modes of joint failure and result in much reduced joint strength and fatigue life. The GDX HIC reflow process is described on Fig. 1.

C. Pre-Encapsulation Cleaning of GDX HIC Process

Since flux (Alpha 100) was used in the GDX HIC reflow process, cleaning was required prior to encapsulation to ensure the long-term device reliability. A non-CFC, terpene-based EC-7R (manufactured by Petroferm, Inc.) was used to remove any residue flux contaminant. An automatic semiaquous washing machine (Detrex model) was used in this process. EC-7R was sprayed on the DGX HIC first, then with DI water through a conveyer-belt washer. Results are listed on Table I.

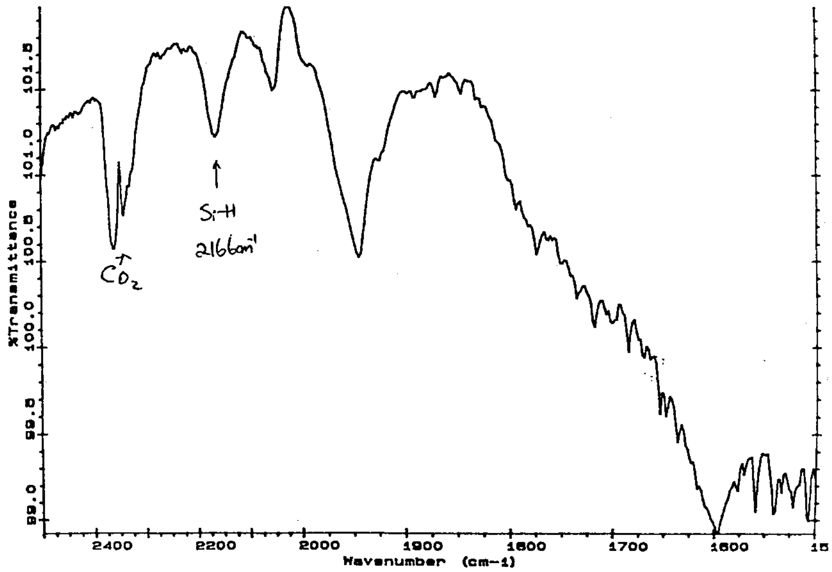

Fig. 2. FT-IR spectra of uncured silicone gel.

TABLE I
CONTACT ANGLES MEASUREMENTS OF EC-7R CLEANED GDX HIC

Sample	θ
As Received (Before cleaning)	46
After EC-7R clean	32
EC-7R plus UV-0_3	0

D. Glob-Coating of Flip-Chip GDX HIC With Silicone Gel

To ensure the high voltage nonhermetic flip-chip GDX HIC and long-term reliability, an ultrahigh purity, low-modulus silicone gel with vinyl and hydride cure siloxane gel was used to glob-coating of the GDX HIC. The thixotropic silicone gel was dispensed (glob) on the GDX devices, vacuum applied at 28 in mercury pressure for 2 min to remove any entrapped bubble and ensure the complete coating of the flip-chip solder joints. The vacuum de-aired silicone gel was then cured at 135 °C for 2 h. FT-IR and microdielectrometry was used to monitor the gel curing to optimize its performance. Results are shown on and Figs. 2–4.

E. Reliability Testing of the Nonhermetic Flip-Chip GDX HIC

Given the stringent reliability requirements of the AT&T number five ESS, the GDX HIC underwent a thorough pre-production qualification to ensure its flip-chip nonhermetic packaging reliability testing. Temperature-humidity bias (85 °C, 85% RH, 600 V) 1000 h was used to accelerate the electrical performance of this new process. Temperature cycling (−40 °C–125 °C) 1000 cycles was used to test the solder joint mechanical reliability and MIL-STD 883C method was also added to ensure the reliability of the process. Results of this testing are shown on Table II.

III. RESULTS AND DISCUSSIONS

A. Flip-Chip Bumping and Reflow of GDX HIC

We have developed a solder bumping process based on solder evaporation, but which uses a resist mask instead of a rigid metal mask. The tedious mechanical alignment of the metal mask scheme, with its associated problems such as mask warpage and tolerance, is now replaced by the well-established and accepted discipline of photolithography. This improvement brings the entire solder bumping operation into closer alignment with the practices of standard IC facility. For the thickness of the solder involved, we have decided to use liftoff, instead of etching, to define the solder bumps. In the conventional understanding of liftoff, the thickness of the liftoff resist mask has to be higher than the thickness of the intended deposit, which, in our case, is on the order of 75 μm. We have chosen dry films (such as Dupont's Riston) for this application. These dry films are laminated onto a clean Si wafer, exposed in a conventional aligner/exposure tool, and developed in either solvent or aqueous based chemicals. The resultant structure is a polymer layer with vias at the interconnection points where bumps are to be formed. The dry film we have chosen behaves as a negative resist, with an important property—the vias have a reentrant profile such that deposits do not cover the sidewall of the via, allowing solvents to enter the via and interact directly with the resist during the liftoff process. Profile control depends on the optimization of exposure and development parameters.

A reliable solder joint can be viewed as consisting of two parts:

1) the solder joint itself which supplies the mechanical strength, the electrical connection, and the appropriate clearance between the two surfaces to be joined;
2) the base metals on the two substrates on either side of the joint which serves as the basis for wetting and adhesion.

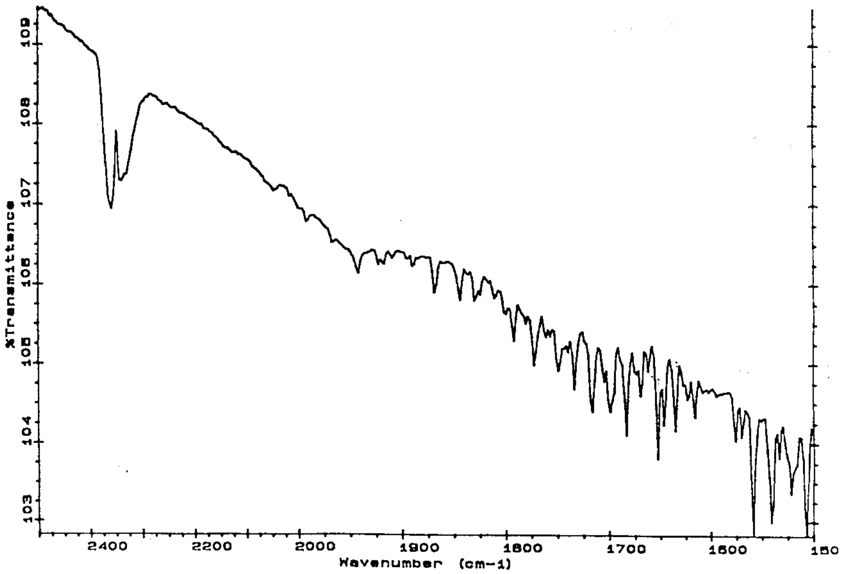

Fig. 3. FT-IR spectra of cured silicone gel.

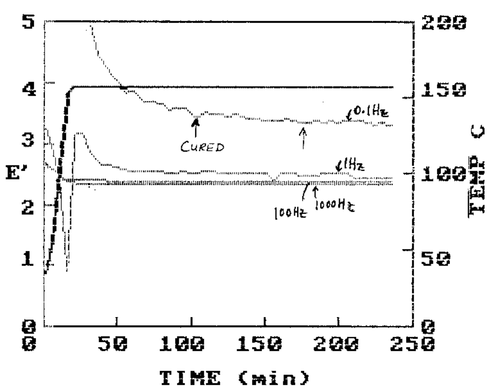

Fig. 4. Microdielectrometry study of silicone gel.

TABLE II
RELIABILITY TESTING OF FLIP-CHIP GDX HIC

Test Method	Results (No. of Failure)
Temperature Cycle (-40°C→125°C)1000 Cycles	0/125
Temperature Humidity Bias (85°C/85%RH/600V d-c)	0/125
High Temperature Storage (125°C for 30 days)	0/125
MIL STD 883C	0/125

The base metals have to have sufficient adhesive strength to both the underlying substrate and to the solder. Since solders typically wet metal films through chemical interactions such as dissolution and intermetallic formation, and the thickness of solder deposits are much larger than the thicknesses of the metal thin films, it is possible that the entire base metal layer is totally consumed during multiple reflows, thus leading to joint delamination. The base metal layers chosen for the Si IC consists of a multilayer stack designed for sustained adhesion through multiple reflows and prolonged temperature and humidity testing. It is based on the Cr/Cu system and includes a co-deposited layer where both metals coexist in a fine-grained structure. The Cu content is intended for interacting with the solder during reflow and Cr, which is inert to solder, serves as a background three-dimensional mesh which interlocks mechanically with the penetrated solder and holds it in place. The fine structure of Cr means that such an adhesion mechanism could be very strong, provided the appropriate layer thickness and material ratio are chosen. The entire stack consists of the following: Cr/CrCu/Cu/Au. The top Au finish provides oxidation protection for the Cu.

All base metal layers are deposited in one pumpdown in a sputtering system. Sputtering is chosen as the deposition method for the base metals because of the uniformity, ease of control and ease of scaling. Just prior to sputtering, the resist-coated wafers are treated with ion-milling, which is integrated with the loadlock of the sputtering system. The ion milling cleans the bottom of the resist via and removes the oxide from the Al bond pads on the Si wafers. The via is typically slightly larger than the Al bond pad so that Al is not exposed at all after the solder bump is formed. This helps eliminate corrosion problems during THB testing.

The wafer then proceeds into another vacuum chamber where solder is being evaporated. For this process, we have chosen inductively-coupled thermal evaporation sources with alloy solder charges. The solder charges have compositions designed to produce a 95Pb/5Sn solid deposit on the wafers. The charges are pre-weighed and evaporated to completion. Because of the much higher vapor pressure of Pb compared to Sn, Pb evaporates first and Sn evaporates last. Thus, the solder deposit formed on the wafer is segregated, with the bulk of the solder being Pb at the bottom, while the top of the solder deposit is mostly pure Sn. This is only an interesting aspect of

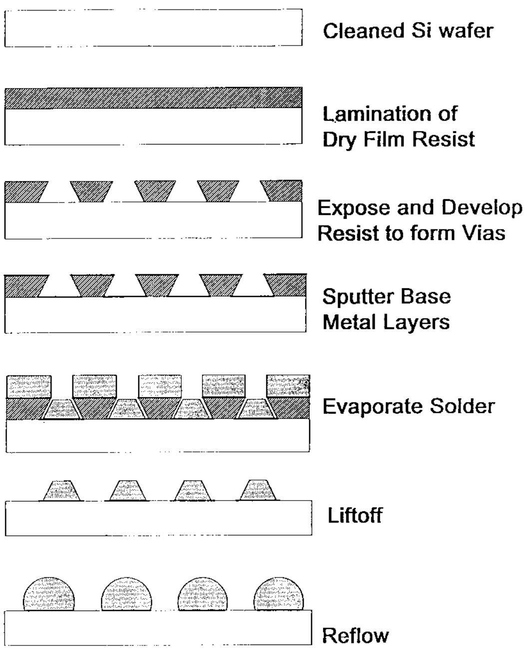

Fig. 5. Formation of flip-chip solder by lift-off process.

the evaporation of the Pb/Sn system, and does not have any implications on subsequent processing.

The solder covered wafers are then immersed in a hot bath of solvents designed to strip the resist, along with the liftoff sheet of solder, without affecting the solder. Most commercial strippers can be used for this purpose, with slight modifications to improve the cleanliness of the liftoff. At this point, the wafer surface will be covered with solder bumps with a slight conical shape, which is a function of the reentrant profile of the resist via. Since a single layer of resist is used for both the sputtering of base metals and for the evaporation of solder, the footprint of the solder matches closely with the footprint of the base metals. This does not always have to be the case. One patterning step can be used for the liftoff of the base metals and another, with a different via diameter, can be used to liftoff the solder. In this case, the second patterning step can be used to produce a via with a much larger diameter, and thus, a solder deposit which is larger in diameter than its wettable base metal area. The advantage of this is that, with an enlarged diameter, a smaller solder deposit height can provide a similar volume of solder (see Fig. 5). During reflow, the solder will withdraw from the unwettable areas and confine itself to within the wettable base, producing a bump similar in characteristics to the one produced by the first instance. The modified scheme is useful for relieving the bottleneck in evaporation, which is typically the step with the lowest throughput in the entire sequence.

The reflow step is used to consolidate the solder bumps from a stack of segregated layers into an alloy, establish wetting between the solder and the base metals, and to transform the bump shapes from truncated cones into truncated spheres. A flux is dispensed onto the wafer surface and the wafer sent through a belt oven, set with a peak temperature slightly higher than the liquidus temperature of 95Pb/5Sn. The flux (Alpha 100) we used is based on organic materials and contains no ionic corrosive agents. Its purpose is to reduce the oxides covering the solder deposits and allow the bumps to settle to their lowest surface energy state. Thus consolidated, the bumped wafers are then cleaned, tested, diced, sorted, and packaged for subsequent assembly onto ceramic HIC's.

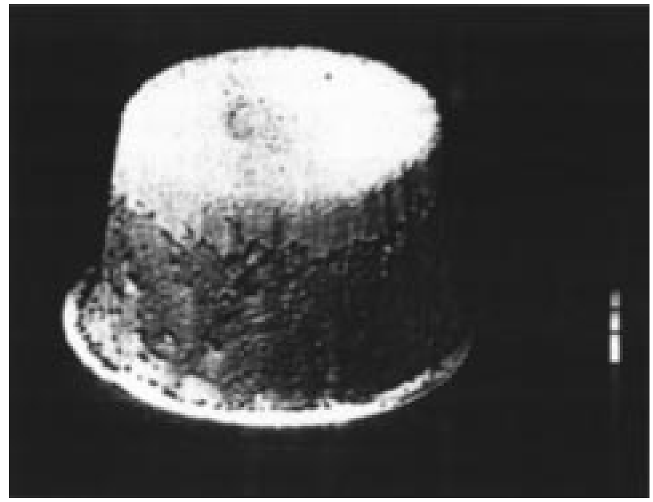

Fig. 6. Solder bump prior to reflow.

The sequence outlined above is shown schematically in Fig. 2.

Micrographs of solder bumps produced using the process described above are shown in Figs. 6 and 7, for pre-reflowed and post-reflowed bumps respectively. The as-deposited bump has the shape of a truncated cone and the reflowed bump, that of a truncated sphere. The bump heights within a wafer lot have a uniformity of about $\pm 7\%$, both before and after reflow. This is an indication that the entire bump shape, not just its height, is extremely uniform. Otherwise, reflow will bring about a wider distribution of bump heights than that obtained after deposition. This uniformity is controlled primarily in the processing of the dry film and in the design of wafer-holding fixtures within the evaporation chamber. The bumping yield, as defined earlier, typically approaches 100% and sometimes even surpasses it. The apparent anomaly has to do with good chips being initially pronounced defective because of errors in testing, usually because of poor contacts. Bumped chips offer better contacts for test probes; thus, nominally "defective" chips can now be pronounced "good," and bumping yield can surpass 100% in principle, and sometimes in practice.

We have initiated an independent isothermal low-cycle fatigue testing of typical joints produced with the standard process. The complete testing scheme and its results are reported elsewhere [11]. The highlights of the test reveal that cylindrically-shaped joints tend to distribute the cycling-induced damage throughout the solder volume and eventual fracture occurs through intergranular cracking, with a strong component of grain boundary sliding. The more natural barrel-shaped joints have areas of reduced cross section at both the top and the bottom of the joint, where the induced stress (and strain) is concentrated. Thus, the damage is not shared uniformly by the rest of the joint; it is localized to parallel fracture planes along these regions of reduced cross section.

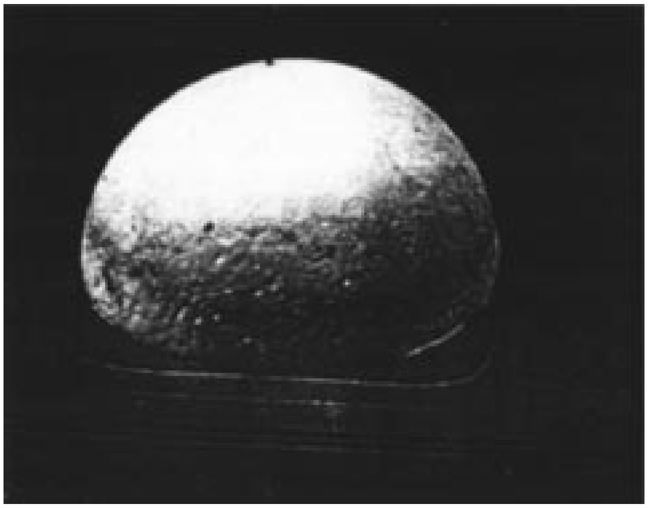

Fig. 7. Solder bump after reflow.

Nevertheless, the barrel-shaped joints have sufficient fatigue life for most intents including this effort. The point here is that a higher fatigue life in solder joints may be obtained through proper design and control of the joint shape.

Test vehicles with flip chip solder joints of all relevant wafer codes have been fabricated with the standard bumping process. A parallel effort is undertaken to optimize the gel composition and the treatment process. Fully assembled and encapsulated test vehicles are subjected to qualification testings which include THB and temperature cycling.

B. Pre-Encapsulation Cleaning of GDX HIC

Since Alpha100, a mild activated flux, was used to reflow the flip-chip GDX onto the ceramic substrate, pre-encapsulation cleaning prior to silicone gel coating is needed for this process to ensure the long-term reliability of the GDX HIC. An EC-7R, a terpene-based orange peel extract, was used to remove the reflux residence and DI water rinse and dry prior to the gel coating [12]. This EC-7R semi-aqueous cleaning solution provides excellent cleaning results. Contact angle and surface analysis shows low angle ($\sim 30°$) and low contaminant after this cleaning process.

C. Glob-Coating of Flip-Chip GDX HIC

A thixotropic silicone gel with silica filler was used to glob-coat the flip-chip GDX HIC. This silicone gel was formulated to have an extremely low modulus (< 1 psi) by intentionally under-crosslinking the polymer network that during temperature cycling and thermal shock testing, no failure was observed. Table II shows the results of these performances. The silica filler also acted as thixotropic agent that controls the flow of the silicone gel. The glob-coating flowed evenly under those solder joints and stop wicking or bleeding excess outside the globed GDX devices. Furthermore, the glob-coating GDX HIC was placed inside an Ultem elastomeric (from GE Plastics Inc.) plastic casing and potted with a silicone for further reliability protection of film IC for a robust GDX HIC structure (see Fig. 8).

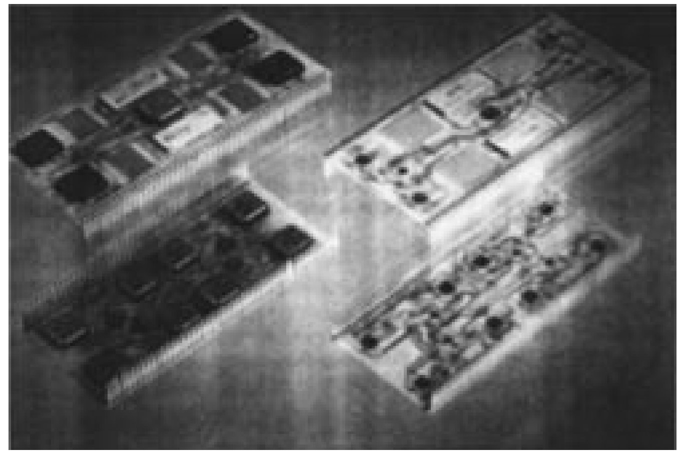

Fig. 8. Nonhermetic flip-chip bonded GDX HIC (on the right) versus hermetic ceramic packaged GDX HIC.

D. Reliability Testing of the Nonhermetic Flip-Chip GDX HIC

To ensure the AT&T number five ESS superior performance, extensive reliability testing were performance to ensure it's reliability. Temperature cycling ($-40° \rightarrow 125$ °C) 1000 cycles was used to ensure the reliability of the flip-chip solder joints. Temperature humidity bias (at 85 °C, 85% RH and 600 V) for 1000 h was used to ensure the anti-corrosion reliability of the modules and MIL STD 883 C with standard salt spray, highly accelerated stress test (HAST) with 121 °C, 2 atm pressure, at 125 °C were used to ensure the module reliability. The gel-coated GDX HIC performance perfectly. Results are shown on Table II.

IV. Conclusion

We have developed a high reliability flip-chip bonded 95/5 Pb/Sn solder joints for the high voltage GDX HIC electronic switch for use in AT&T's number five ESS, and a robust non-hermetic packaging structure which consists of a coating of an ultrasoft silicone gel and an elastomeric silicone. Silicone with its superior electrical property, can nonhermetically protects the high voltage (375 V versus normal 3–5 V device) GDX devices. When proper materials are chosen and processes are carefully monitored and controlled, a reliable flip-chip high voltage device can be manufactured with tremendous cost savings (in excess of tens of millions of dollars per year).

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Dr. Wong received the Best Paper Award in 1981 at the International Society for Hybrids and Microelectronics Annual Meeting, the AT&T Bell Laboratories Distinguished Technical Staff Award in 1987, a 1992 AT&T Bell Laboratories Fellow Award, the IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY (CPMT) Society Outstanding Paper Awards in 1990, 1991, and 1994, respectively, the IEEE-CMPT Society Board of Governors Distinguished Service Award in 1991, the IEEE Technical Activities Board (TAB) Distinguished Service Award in 1994, and the 1995 IEEE CPMT Society's Outstanding Sustained Technical Contributions Award (the highest Society honor). He is a Fellow of AT&T Bell Labs, and a member of Sigma Xi, Phi Lambda Upsilon, National Honorary Chemical Society, and Materials Research Society. He was the Program Chairman of the IEEE 39th Electronic Components and Technology Conference in 1991. He was elected to the Board of Governors of the IEEE-CHMT Society from 1987–1989, served as the IEEE-CPMT Society technical Vice President, 1990 and 1991, President of the IEEE-CPMT Society, 1992 and 1993, and Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, HYBRIDS AND MANUFACTURING TECHNOLOGY, 1995. He currently chairs the IEEE Technical Activities Board, Steering Committee on Design and Manufacturing Engineering, since 1995.

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Mr. Segelken received numerous best paper awards. He is a member of Tau Beta Pi, Pi Tau Sigma, and an ASME Fellow. He has served in numerous executive capacities as a member of the Operating Committee of the Electronic Components and Technology Conference (ECTC), and the 47th General Chair for ECTC and was elected to the Board of Governors of the IEEE-CPMT for two consecutive three-year terms. He served as Guest Editor and Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY.

K. L. Tai, photograph and biography not available at the time of publication.

C. C. Wong, photograph and biography not available at the time of publication.