Next Generation of 100-μm-Pitch Wafer-Level Packaging and Assembly for Systems-on-Package

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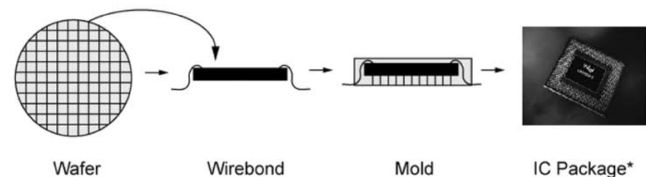
***Abstract*—According to the latest ITRS roadmap, the pitch of area array packages is expected to decrease to 100 μm by 2009. Simultaneously, the electrical performance of these interconnections needs to be improved to support data rates in excess of 10 Gbps, while guaranteeing thermomechanical reliability and lowering the cost. These requirements are challenging, thus, needing innovative interconnection designs and technologies. This paper describes the development of three interconnection schemes for wafer-level packages (WLPs) at 100-μm pitch, involving rigid, compliant, and semicompliant interconnection technologies, extending the state of the art in each. Extensive electrical and mechanical modeling was carried out to optimize the geometry of the interconnections with respect to electrical performance and thermomechanical reliability. It was found that the requirements of electrical performance often conflict with those of thermomechanical reliability and the final "optimum" design is a tradeoff between the two. For the three interconnection schemes proposed, it was found that the electrical requirements can be met fairly well but acceptable mechanical reliability may require organic boards with coefficient of thermal expansion of 10 ppm/K or lower.**

I. Introduction

INFORMATION technology (IT) is more than a trillion dollar industry. It includes hardware, software, services, and applications. Contrary to perception, hardware accounts for more than two-thirds of the IT industry, and the single most important building block of this hardware, of course, is semiconductor devices such as CMOS, GaAs, SiGe, and silicon-on-insulator (SOI) for a variety of computing, communication, consumer, automotive, and other applications. The total worldwide annual market for these devices is approximately \$150 B. These devices, the technology for which is at the threshold of nanoscale (100 nm), are typically fabricated into wafers as big as 300 mm in diameter and are subsequently diced into individual integrated circuits (ICs). They are then packaged, tested, and burnt into individual IC devices, ready to be surface mount bonded onto system level boards. The total number of ICs produced in 2003 was about 375 billion units, each packaged at some cost, typically US\$0.01 per I/O. The total packaging market, which includes IC packaging, as well as systems packaging, is almost as big as the semiconductor market, together accounting for 25% of the IT industry.

The semiconductor industry is racing toward a historic transition—nanochips with less than 100-nm features. The first set of such chips reached production in 2003. Some of these chips have several hundred million transistors which require I/Os in excess of 10 000 and power in excess of 150 W, providing computing speed at terabits per second. These requirements, together with digital and wireless systems around 20 GHz (in 2010), require new approaches to IC and systems packaging in general and IC-to-package interconnections in particular.



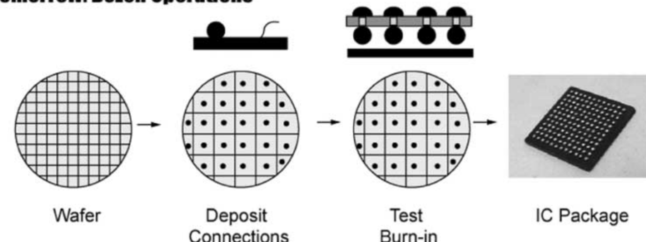


Fig. 1. WLP versus conventional packaging.

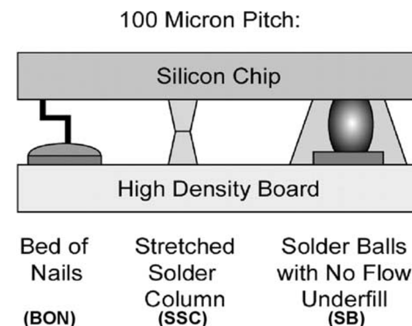


Fig. 2. Proposed 100-μm-pitch interconnections.

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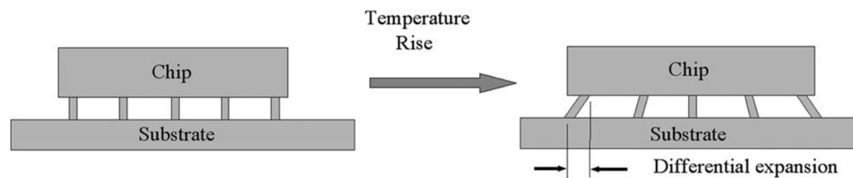


Fig. 3. Flip-chip package.

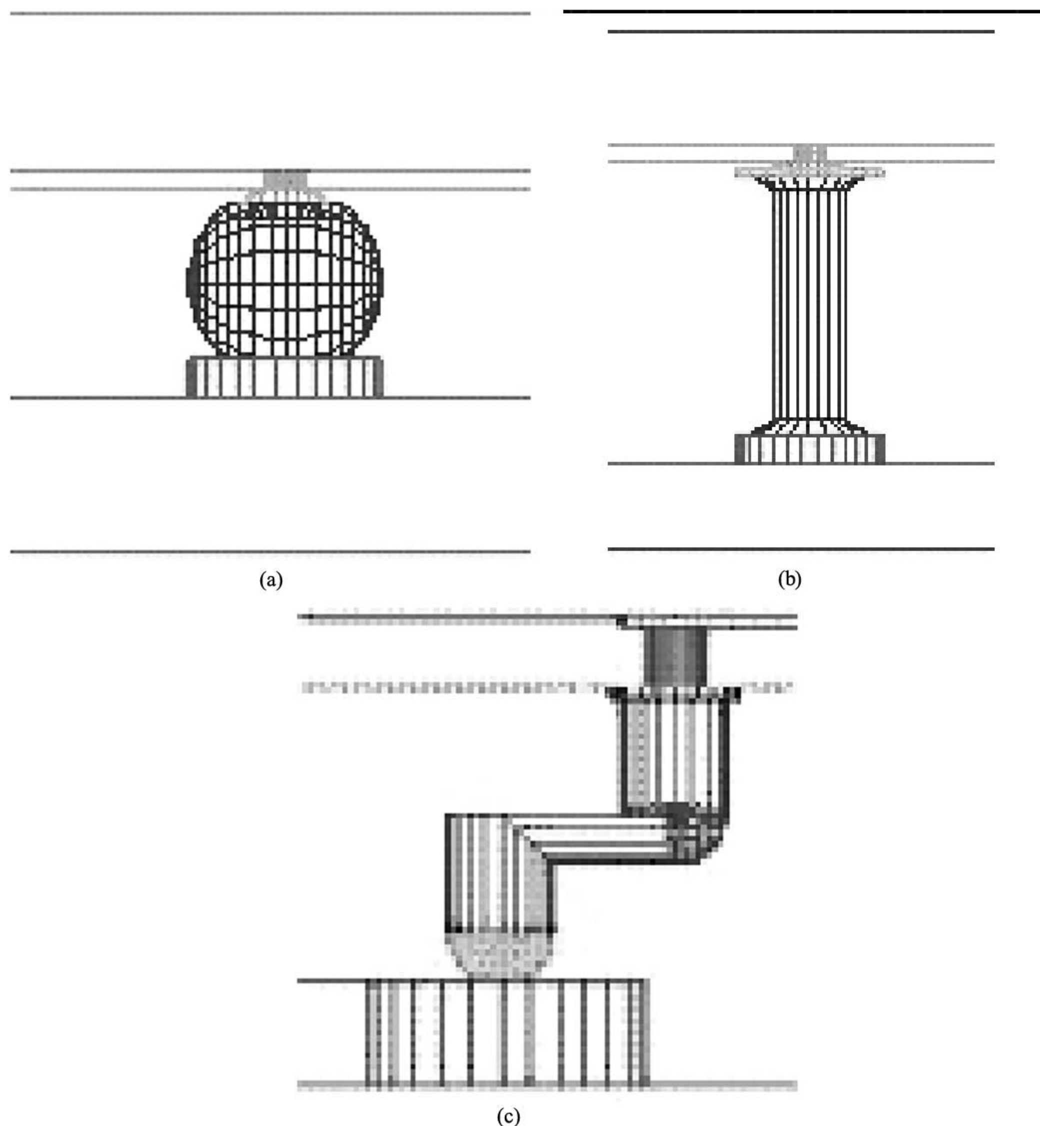


Fig. 4. Three-dimensional models developed for the wafer level interconnections: (a) SB, (b) SSC, and (c) BON.

A. Finer Pitch Need and Technology Barriers

The latest ITRS roadmap clearly states the need for finer pitch area array package and assembly technologies calling for 100-μm pitch by 2009. Simultaneously, the electrical performance of these interconnections need to be improved to support data rates in excess of 10 Gb/s, while guaranteeing thermo-mechanical reliability and lowering cost. These drivers present enormous barriers. The current approach of lead-free solders with underfill present major challenges in both dispensing the underfill and guaranteeing fatigue resistance as the height of solder bumps is lowered. The currently available compliant interconnections, on the other hand, present electrical challenges due to their higher inductance and resistance.

This paper proposes to understand the limits, as well as propose new ways of extending the state of the art of in three IC-to-package interconnection technologies:

1) current solder bumps by extension to stretched-solder column (SSC);
2) current compliant interconnections by extension to lower cost and higher compliancy;
3) current lead-free with organic underfills by extension to improvements in underfill technology.

In 2002, an international collaboration program between the National University of Singapore, the Institute of Microelectronics, Singapore, and the Packaging Research Center, Georgia Institute of Technology, was initiated with a vision is to develop interconnection technologies spanning from 100-μm pitch in the short term to nanoscale in the long term, as wafer level technologies, for the best electrical properties and lowest cost, while guaranteeing mechanical reliability. This paper reviews the progress by this team in the 100-μm-pitch interconnection technologies.

B. What is Wafer Level Packaging?

As illustrated in Fig. 1, a wafer-level package (WLP) is one in which the die and "package" are fabricated and tested on the wafer prior to singulation. This process eliminates many of the packaging processes required using conventional packaging resulting in drastic reduction in manufacturing cost. The benefits of WLP are as follows:

1) smallest IC package size as it is a truly a chip-size package (CSP);
2) lowest cost per I/O because the interconnections are all done at the wafer level in one set of parallel steps;
3) lowest cost of electrical testing, as this is done at the wafer level;
4) lowest burn-in cost, as burn-in is done at the wafer level;
5) enhances electrical performance because of the short interconnections;
6) ease of cooling through the fully exposed back of the die.

In this paper, three basic interconnection technologies for WLPs at 100-μm pitch are pursued, each extending the state of the art (Fig. 2):

1) lead-free solder ball (SB) with underfill, a rigid interconnection;
2) bed of nails (BON), a compliant interconnection;
3) SSC, semicompliant interconnection.

The following are the main electrical and mechanical design parameters considered in this paper:

size of chip: 20 mm × 20 mm;
pitch of interconnections: 100 μm;
number of I/Os: 10 000 per cm^2;
temperature cycling range: -40 to 150 °C;
thermal cycle fatigue life: 1000 cycles (target);
signal frequency: 20 GHz;
interconnection parasitics:
dc resistance: 25 mΩ;
inductance: 50 pH;
capacitance: 10–15 fF.

C. Electromechanical Design of Interconnections

While the primary function of interconnections between chip and substrate (Fig. 3) is to provide electrical connections, mechanical integrity guarantees this electrical connection. At the assembly temperature, the stress in the interconnections is zero. However, during the operation of the chip, the interconnections experience temperature changes which result in differential expansion between chip and substrate due to the difference in the coefficient of thermal expansion (CTE) between the silicon chip

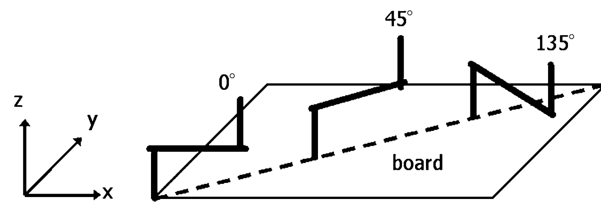
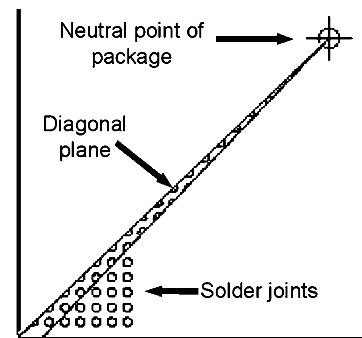
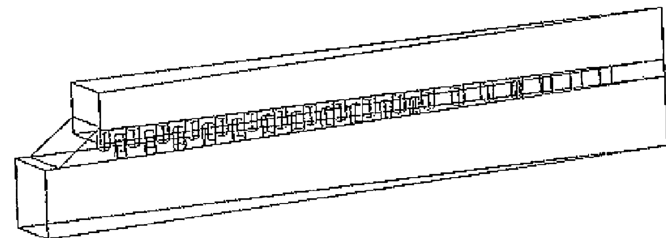


Fig. 5. Schematic illustration of three BON orientations to be investigated.



(a)



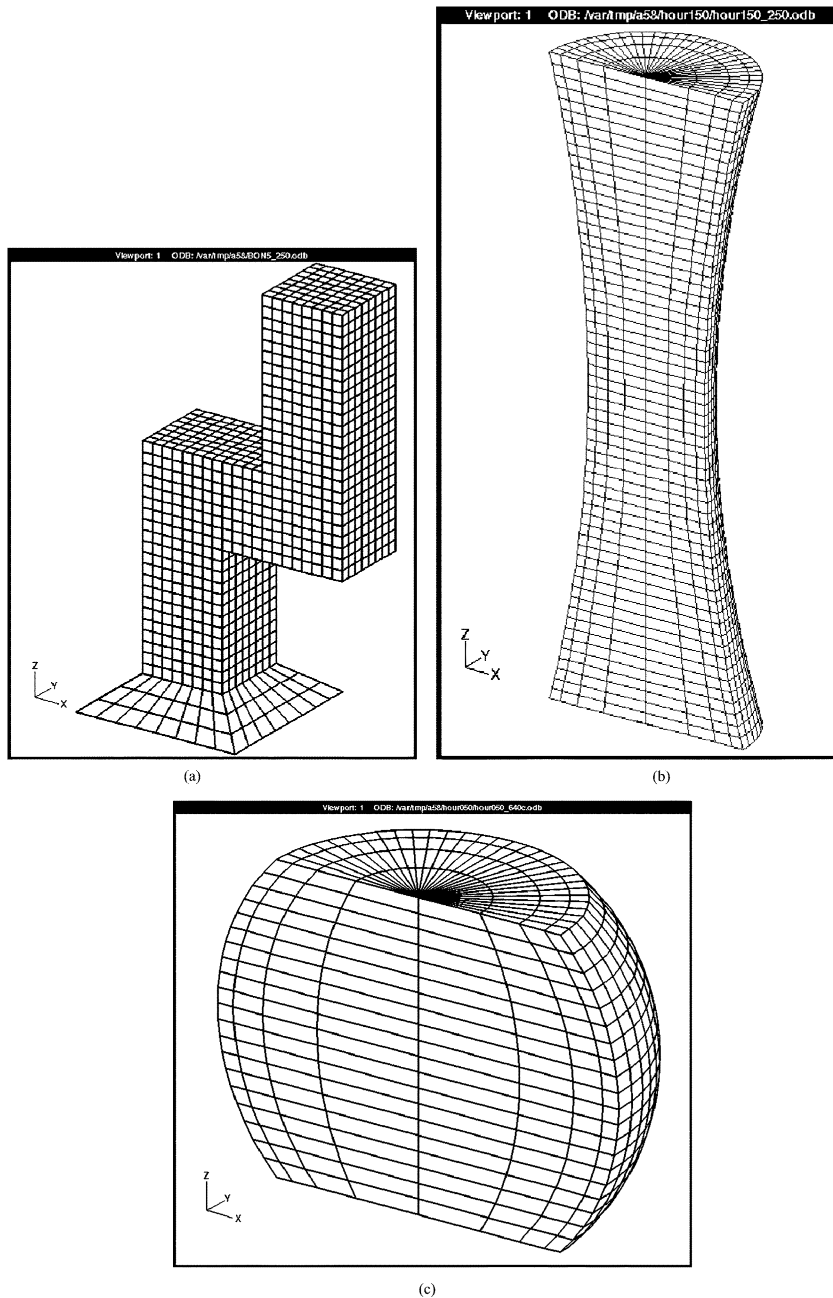
(b)

Fig. 6. (a) Plan view of package. (b) Slim sector model for the package with SB interconnections.

$(\text{CTE} = 3\ \text{ppm/K})$ and the substrate (typically 18 ppm/K for FR4 board material). This is illustrated in Fig. 3. This causes stress to be induced in the interconnections which, if excessive, can result in structural failure which leads eventually to electrical failure of the chip. This is considered the single biggest barrier to fine-pitch interconnections, requiring novel designs.

Two broad classes of interconnections have been proposed in this program, namely, compliant and rigid interconnections. With a compliant interconnection, the mechanical stress in the interconnection for the same CTE mismatch is reduced. However, compliant interconnections are usually accompanied by higher values of electrical resistance and inductance. With a rigid interconnection, on the other hand, electrical resistance and inductance can be lowered but stresses will be increased. Thus, electrical and mechanical design requirements are often conflicting and the final design is a tradeoff between the two.

Thus, before the three types of 100-μm-pitch interconnections were fabricated, extensive electrical and mechanical modeling and simulations were carried out to optimize the geometry of the interconnections. The final dimensions of the interconnections are a tradeoff between the satisfaction of the electrical performance requirements and the mechanical performance requirements. Details of these simulations are given in Sections II–VI. This will be followed by descriptions of fabrication methods and discussion of the results.



(a) (b) (c)

Fig. 7. Micromodels used in fatigue life estimation. (a) BON. (b) SSC. (c) SB.

II. Electrical Modeling of Proposed Interconnection Schemes

The interconnection schemes presented in Section I-C had to fulfill stringent electrical requirements. These requirements were based on the fact that the package using such interconnects had to support high frequency performance applications (e.g., microprocessors, high pin count logic devices, etc.). The ITRS road map [1] stated that in 2005 the high end microprocessor would have a 5-GHz clock frequency, consume 170 W of power and the operating voltage would be 0.9 V. It had been shown [2] that to support the requirements given by the ITRS road map the interconnection of the package had to fulfill some basic electrical properties such as dc resistance $\leq 25\ \mathrm{m}\Omega$, inductance $\leq 50\ \mathrm{pH}$, and capacitance $\leq$10–15 fF. These valued were

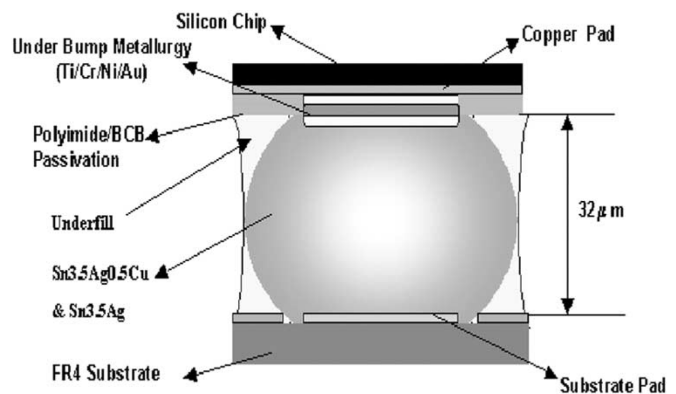


Fig. 8. Solder bump specifications for 100-$\mu\mathrm{m}$ pitch.

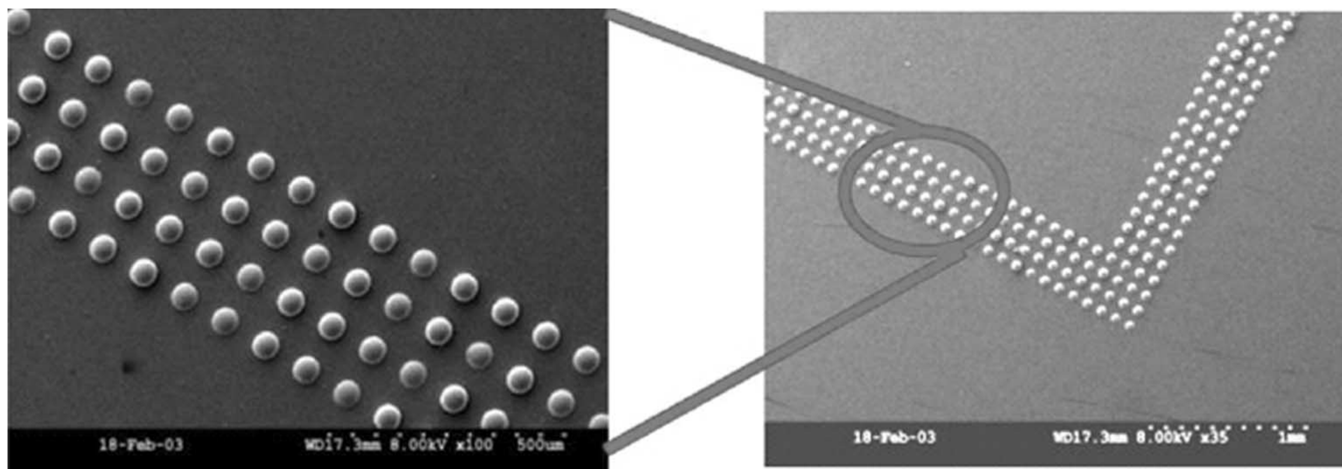


Fig. 9. 100-μm-pitch lead-free solder bumps.

set as targets for the interconnection schemes described in this paper.

The basic electrical characteristics of interconnects under study had been modeled using three-dimensional (3-D) full-wave solver, high-frequency structure simulator (HFSS) [3]. The models developed are shown in Fig. 4. The assumptions made in the 3-D models are that all the dielectric materials in the models are considered to be lossless and the signal traces are considered perfect conductors. With these assumptions, the S-parameters of the models were extracted with the signal lines deembedded and thereafter an impedance parameter extraction was done. An equivalent circuit model for each interconnection was then obtained through a parameter fitting using the circuit simulation software -ADS.

Furthermore, to achieve the targeted values for the resistance, inductance and capacitance an optimization was done. Through geometrical variation (height, width, diameter, etc.) an optimum design for each of the interconnection schemes was obtained. The following table summarizes the geometrical parameters and electrical characteristics of the optimized interconnection schemes.

III. Mechanical Modeling of Proposed Interconnection Schemes

For a 20 mm $\times$ 20 mm package with 100-μm pitch, there would be 40 000 interconnectiions. Even after taking advantage of symmetry, it would be computationally impractical to perform 3-D simulations using adequately-sized elements for all the solder joints. Hence, a macro–micro modeling approach was adopted [5], [6] which used the displacement results from a coarse mesh of the entire structure (i.e., the macromodel) as boundary conditions of a fine mesh of the region of interest (i.e., the micromodel). The response of the region of interest might then be studied using small 3-D solid elements without potentially prohibitive computational requirements.

Two approaches had been taken for the macromodels. In the macromodels of packages with either BON interconnections or SSC interconnections, the interconnections were modeled by equivalent beams [5] while the chip and substrate were modeled as shell elements. An equivalent beam is one which gives approximately the same compliance in the x, y and z directions as the actual interconnection. As the compliance of the BON was not isotropic, the orientation of the BON (illustrated in Fig. 5) is expected to have a significant effect. The equivalent beam model is ideal for this situation, since the beam can easily be rotated without affecting the mesh thus obviating creation of different meshes for different orientations of the BON. However, for packages with underfill, this approach would not be possible. Hence, a second approach was adopted for the macromodel of packages with SB interconnections, where a very slim sector of the package was modeled using 3-D solid elements (Fig. 6) [6]. This was possible since it would be reasonable to assume that as the number of interconnections became very large, the displacement of points on the chip and substrate would tend to be directed radially. This fact had also been confirmed by 3-D finite element analysis of WLPs. The macromodel of a package with SSC interconnections only modeled an eighth of the package, while that of the BON interconnections modeled a quarter. The prerequisite planes of symmetry were assumed. Typical BON, SSC, and SB micromodels, built using 3-D solid elements, are illustrated in Fig. 7.

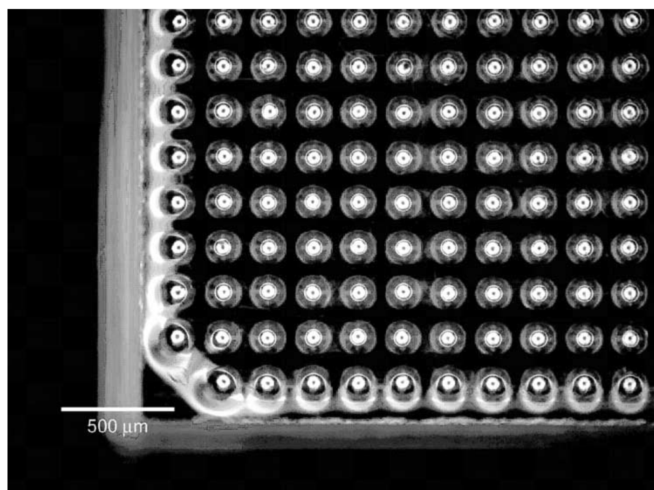


Fig. 10. Underfill coated on the bumped wafer.

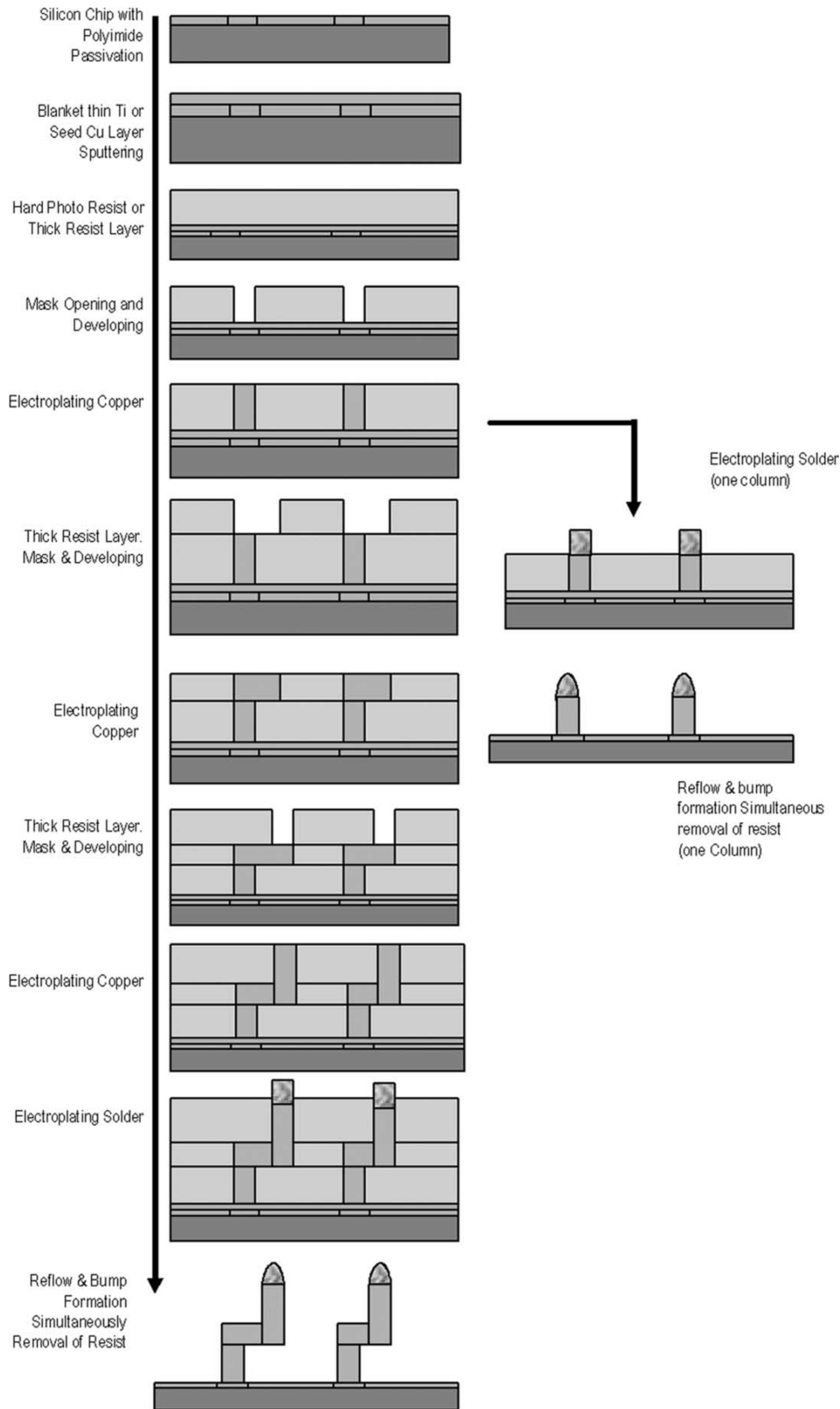


Fig. 11. Process flow of BON interconnections.

The efforts to date had been focused on predicting the fatigue lives of the interconnections with 100-μm pitch. The 20 mm $\times$ 20 mm package with 100 μm pitch was assumed to be fully populated with interconnections. Fatigue life had been estimated under thermal cycling between 150 and -40 °C with the stress-free temperature being 150 °C. To predict the fatigue life of the interconnections, a relatively simple correlation by Solomon [7] based on maximum strain range was

used. Solomon's correlation relate fatigue life N_f to applied maximum plastic shear strain range $\Delta\gamma_p$

$$\Delta\gamma_p N_f^{0.51} = 1.14. \quad (1)$$

$\Delta\gamma_p$ was obtained from a finite element simulation of the temperature cycling process.

IV. Fabrication of Proposed Interconnection Schemes

Lead-Free SB With No-Flow Underfill: The detailed specifications of the solder bump is illustrated in Fig. 8. A 100-μm-pitch lead-free solder (Sn3.5Ag0.7Cu and Sn3.5Ag) bumping process was developed using Harima Chemical's Super Solder process as shown in Fig. 8. An extensive testbed was designed and fabricated to study different pad metallurgies and passivations for the Super Solder bumping process. The results suggest that Ti/Ni/Cr/Au was the optimal under bump metallurgy (UBM) and that polyimide was an ideal wafer passivation. (See Fig. 9.)

A unique wafer level underfill material was developed for this lead-free application. It contains an epoxy resin mix, a phenolic hardener, and a latent catalyst. The curing behavior of the underfill was characterized using a modulated differential scanning calorimeter (DSC). One important requirement for a successful wafer level underfill process was that the underfill should not gel before the solder melted and wetted the substrate. In order to identify the gel point of the underfill, the time to gel was obtained in the isothermal curing experiments performed using the stress rheometer. Compared to the degree of cure (DOC) change in the isothermal curing experiments from the DSC measurement, the DOC at gelation at different curing temperatures was calculated. It was found that the DOC at gelation for the underfill is around 0.85. Therefore, the underfill can be B-stage cured to DOC of 0.7 without pre-gel in the reflow process.

The unique process of the wafer level underfill required the T_g of the B-staged underfill to be around or above room temperature, so that the material would be sufficiently solid to facilitate dicing and prevent further reaction at room temperature storage. The T_g and the DOC of the underfill after B-stage at 130 °C for different times were determined using the DSC.

The assembly of WLP with wafer level underfill was carried out on a 6″ wafer. The underfill was spin-coated on the wafer and B-stage cured at 130 °C for 30 min. Then the wafer was diced into 5 mm $\times$ 5 mm individual chips. Fig. 10 shows the bumped wafer with B-staged underfill after dicing. The B-staged underfill did not show any cracking or delamination after dicing. The thickness of the underfill was about the height of the bumps (i.e., around 50 μm). The chip with wafer level underfill could be considered as a WLP, since no additional underfilling step was needed in the assembly process.

BON Interconnections: The BON interconnection is a novel compliant interconnect, extending beyond compliant interconnects previously reported. Two variations are being pursued: a single layer and a three layer structure. Their geometry and the process flow for fabricating the BON interconnections are illustrated in Fig. 11. Since a higher column height would result in higher compliance, lower stress, and hence, longer fatigue life, interconnections as high as 50 μm were developed.

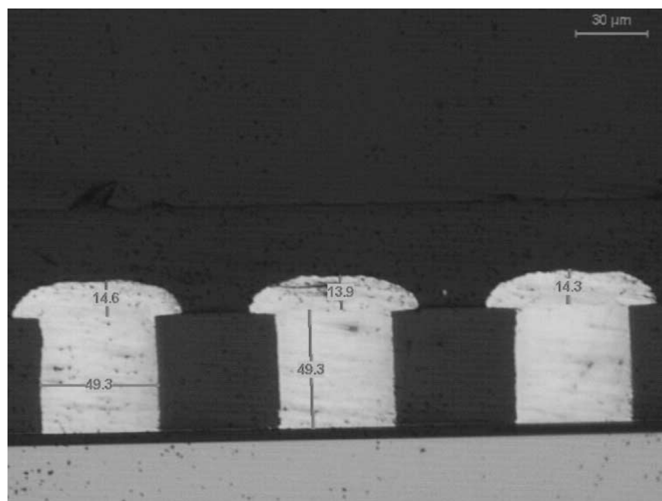


Fig. 12. Optical micrograph of the single layer BON on test die.

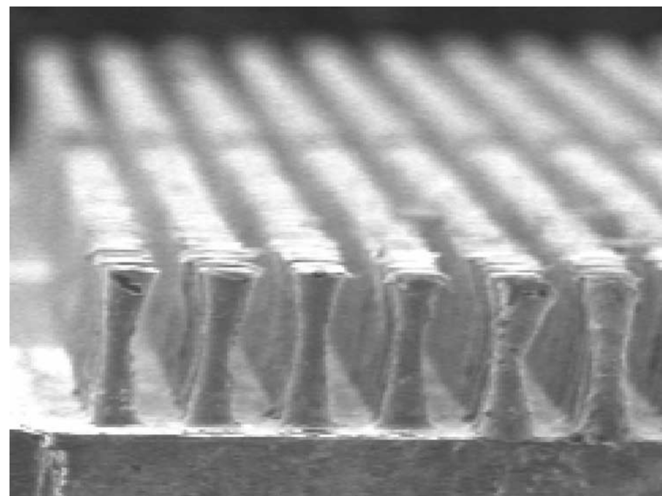


Fig. 13. Array of SSC interconnections.

TABLE I
ELECTRICAL CHARACTERISTICS OF OPTIMIZED INTERCONNECTION SCHEME

Interconnection scheme	DC resistance (mΩ)	Inductance (pH)	Capacitance (fF)
Solder Bump (diameter = 50 µm)	5	32	17
Bed of Nails (diameter = 15 µm, total height = 50 µm)	28	46	18
Stretched solder column (diameter = 30 µm, height = 100 µm)	33	51	21

A single layer BON wafer level interconnection had been successfully fabricated with a nail height of 50 μm. The thick photoresist process with high aspect ratio and good vertical profile was developed after analyzing various commercially available photoresist materials. Copper columns of 50 μm were electroplated, followed by Sn/Pb solder plating to 15 μm thickness. The plating process was optimized for copper nail plating in 12 min and solder plating in 4 min, achieving a coplanarity of

TABLE II
FATIGUE LIFE OF SB JOINT

Cases	Bump Height (μm)	Ball Diameter (μm)	Substrate CTE (ppm/K)	With Underfill	Fatigue Life
Case 1	50	70	5	Yes	2108
Case 2	50	70	10	Yes	1749
Case 3	32	45	10	Yes	1597
Case 4	50	70	5	No	741
Case 5	50	70	10	No	138

TABLE III
FATIGUE LIFE ESTIMATES OF BON USING SOLOMON'S CORRELATION

chip thickness (μm)	250	640	640	640
substrate CTE (ppm/K)	18	18	10	5
orientation = 0º	10	21	60	1575
orientation = 45º	16	41	71	1228
orientation = 135º	200	11	348	4037

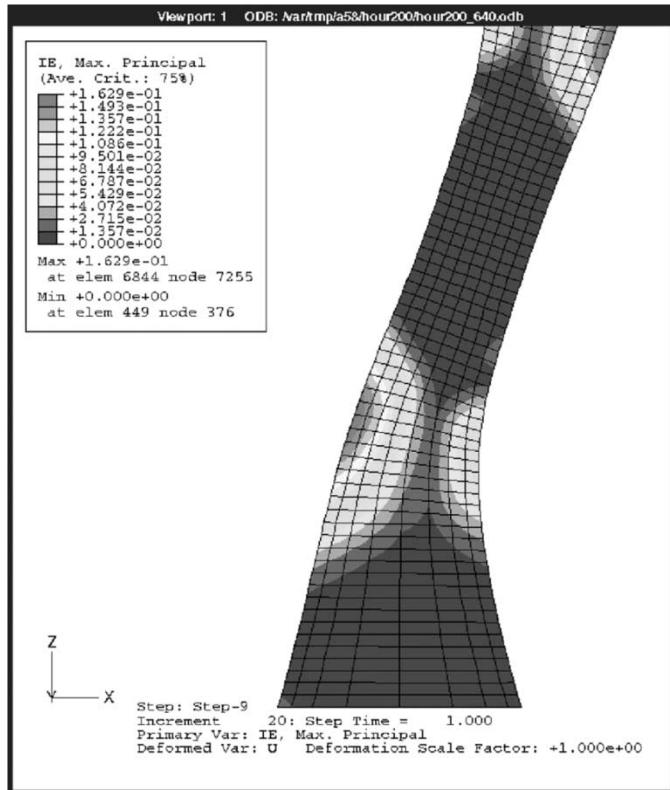


Fig. 14. Typical strain distribution in SSC of high aspect ratio.

$\pm$2-3 μm. For this process optimization study, a 10×10 mm test chip with 3332 I/Os, as shown in Fig. 12, was designed and fabricated.

SSC Interconnections: In terms of mechanical compliance, the SSC interconnection is somewhere between the rigid SB and the compliant BON, and may be regarded as a semicompliant interconnection. In this interconnection design, an amount of high-lead solder is first deposited on all the die-pads on wafers. The solder is then melted, stretched, and cooled to form a unique hourglass shape (Fig. 13) on the entire wafer. Details of the process cannot be given as the process is being patented. To demonstrate the process, a full array of 2000 SSC eutectic solder interconnections on a 10×10 mm test die at 200-μm pitch and die-pad diameter of 100 μm, was developed. This is shown in Fig. 13.

TABLE IV
FATIGUE LIFE ESTIMATES OF SSC INTERCONNECTIONS

Chip thickness (μm)	250	640	640	640
substrate CTE (ppm/K)	18	18	10	5
Height=50 μm	81	-	171	3237
Height=100 μm	97	27	276	3124
Height=150 μm	134	31	518	4405
Height=200 μm	74	38	273	5772

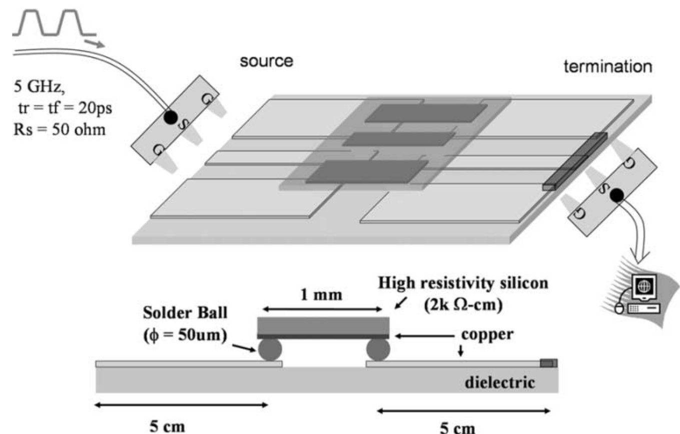


Fig. 15. Test vehicle developed for electrical measurements.

V. RESULTS AND DISCUSSION

A. Thermomechanical Simulations

SB Interconnections: The chip thickness was kept constant at 640 μm while the height and width of the SB were varied. Estimates of the fatigue life based on the finite element simulations using the slim sector model are given in Table II. It can be seen that increasing solder height and decreasing substrate CTE will increase the fatigue life. The use of underfill also increases fatigue life dramatically.

BON Interconnections: The cross section of the BON was fixed at 20 μm square and the pad at 40 μm square. The equivalent beam macro model was employed and it was assumed that

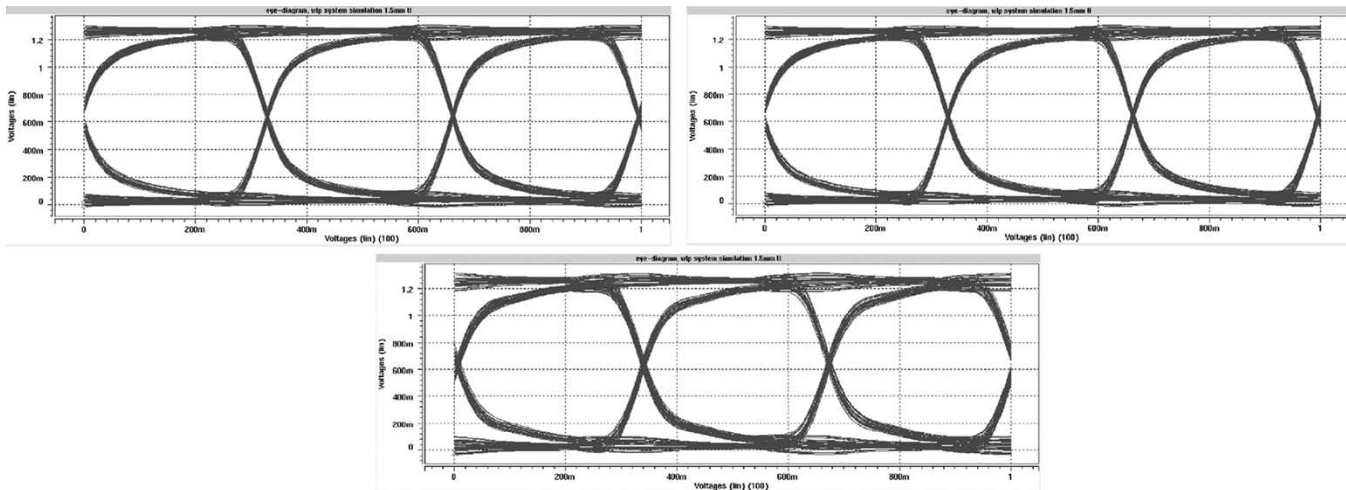


Fig. 16. Eye diagram simulation response for three different interconnection schemes. (a) SB $L = 32$ pH, $C = 17$ fF, $R = 5$ mΩ. (b) BON $L = 46$ pH, $C = 17$ fF, $R = 5$ mΩ. (c) Stretched solder $L = 51$ pH, $C = 21$ fF, $R = 33$ mΩ.

failure of the interconnection occurred at the solder joining the interconnection to the substrate. The results of fatigue life estimates based on the finite element simulations of some BON with various heights and lengths were obtained and those for the "best" BON are given in Table III. As can be seen, a BON oriented at 135° usually has a higher fatigue life than one oriented at 0 or 45°. This is probably due to the fact that the BON is most compliant when oriented at 135° and stiffest at 0°. The effect of chip thickness is not so clear. As expected, smaller values of substrate CTE give longer fatigue lives due to smaller CTE mismatch between chip and substrate. The fatigue lives with a FR4 substrate are very short suggesting that it might not be suitable for use with BON interconnections at 100-μm pitch.

SSC Interconnections: The effect of the height of the SSC was studied. The volume was kept constant at 1.63×10^{-13} m^3 and the pad diameter at 50 μm. The distribution of the maximum principal strain in the SSC of height 200 μm is shown in Fig. 14. A significant finding is that, with the proposed unique shape of the SSC and for high aspect ratios, the location of maximum strain, and hence, the failure site, is shifted away from the usual location at the solder/pad interface toward the center of the interconnection. This can be seen in Fig. 14. This is also confirmed by fatigue experiments conducted on the SSC interconnection which will be described in Section VI.

The results of fatigue life estimates based on the simulations are given in the Table IV. For these simulations, no underfill is considered. As expected, fatigue life increases with height. Reducing either board CTE or chip thickness is beneficial to fatigue life, with board CTE having a greater effect.

B. Electrical Testing

As shown earlier the interconnection schemes had promising electrical parameters, but to demonstrate further their ability to support very high speed signals with minimum deterioration and to provide adequate power supply, a more complex test vehicle and test methodology were needed. The board, the chip, and the interface between them were studied and the electrical performance of the wafer level interconnect schemes were evaluated through the proposed test methodology.

As the ultimate goal of this paper was to demonstrate the ability of the wafer level off-chip interconnections to support speeds and power comparable with that on-chip, this required careful design of the test structure. The test vehicle consisted of coplanar wave guided (CPW) lines on high resistive silicon substrate interfaced with a CPW line on a low dielectric constant and low dielectric loss board [2], [4]. The transition between the chip and the board was completed through the interconnect schemes proposed earlier (BON, SSC, SB), as shown in Fig. 15. Both of the CPW lines had been characterized using time domain reflectometry (TDR) and vector network analyzer (VNA) based measurements.

The synthesized models extracted from the measurement results were used together with the equivalent circuit extracted for the interconnect schemes and a data transmission at 5-GHz speed had been simulated. The methodologies used for model extraction was as described in [2]. The data transmission at 5 GHz was simulated using HSPICE model. A random pulse source with 200 ps period and a rise time of 20 ps was used. The output impedance of the pulse source was 50 Ω and the high-level and low level voltages of the pulse were 2 and 0 V, respectively. The transient signal at the far end termination was simulated from 50 to 100 ns, and converted to the eye diagrams (Fig. 16). All the combinations used for the simulations showed clean and wide open eyes demonstrating that high-speed signal transmission could be achieved off chip through this kind of interconnection. It must be mentioned here that the choice of the board, the design of CPW lines, as well as the design of the chip /interconnect/ board interfaces were very important for the overall system performance.

C. Mechanical Testing

Static tensile tests, as well as mechanical cyclic loading fatigue tests, had been conducted on the SSC interconnection to determine its strength and fatigue life at room temperature [8]. The SSC specimens had base diameters of 100 μm and had been stretched to varying heights (aspect ratios) between two silicon pieces. The experimental setup for the fatigue tests is shown in Fig. 17. The specimen was attached to a specially designed fix-

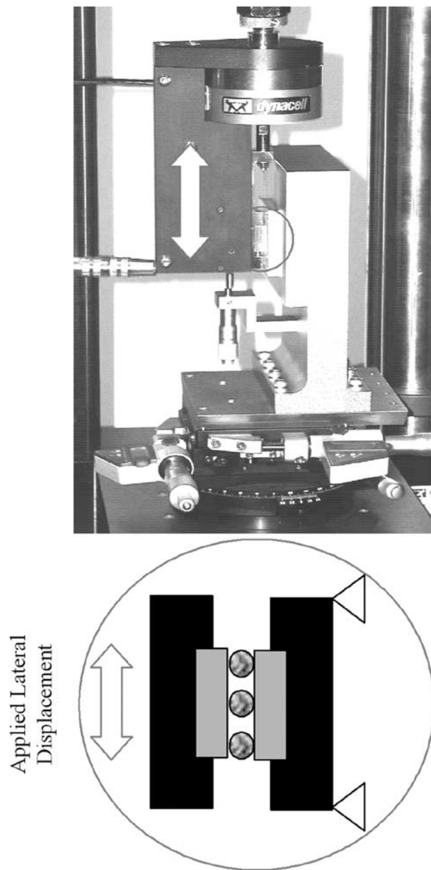
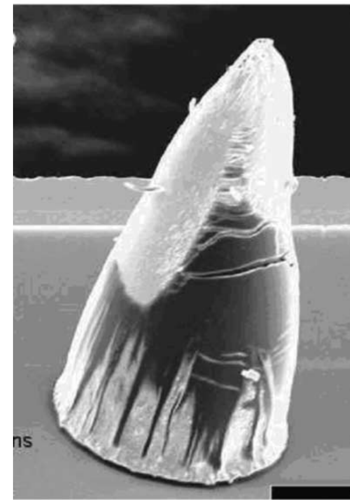


Fig. 17. Experimental setup of mechanical cyclic loading fatigue test.

ture which allowed a sinusoidal cyclic lateral displacement to be applied as shown in Fig. 17.

The experimental test results are given in Table V. In the fatigue tests, specimens were subjected to a cyclic lateral sinusoidal displacement of amplitude of 2.8 μm and frequency 5 Hz. As can be seen from Table V, as the aspect ratio is increased the static strength decreased. This is expected since the solder volume was kept constant and a higher aspect ratio will result in a smaller minimum cross-sectional area of the interconnection and hence, a smaller axial strength. On the other hand, the fatigue life of the interconnections increased with the aspect ratio (height) of the solder column. This is expected as a higher aspect ratio leads to lower shear strains in the interconnection and, hence, a higher fatigue life. Another interesting finding is that at low aspect ratios the site of the fatigue failure is located at the solder/pad interface as is usually the case. However, as the aspect ratio is increased, the failure site moves toward the middle of the interconnection. Fig. 18(a) shows a specimen of aspect ratio 2.2 where the failure occurred at the UBM while Fig. 18(b) shows a specimen of aspect ratio 3.9 where the fatigue failure occurred near the mid-height of the interconnection. This experimental result is consistent with the numerical simulation described earlier (Fig. 14). A significant advantage of shifting the failure location away from the solder/substrate interface to within the bulk material is that fatigue failure should be more consistent and, hence, a more consistent fatigue model should be possible.

(a)



(b)

Fig. 18. Fatigue failure mode for SSC at aspect ratios of (a) 2.2—intermetallic failure at UBM and (b) 3.9—bulk solder failure at midlength.

VI. Evaluation of Proposed Interconnection Schemes

The main objective of the electrical and mechanical simulations described above is to optimize each of the three proposed 100-μm-pitch interconnections and compare them in terms of how well they satisfy the electrical and mechanical requirements. From the aforementioned electrical and mechanical simulations, the best tradeoffs for SB, BON, and SSC interconnections were determined.

A template has been constructed to perform a comparative evaluation of the three proposed interconnections. This is shown in Table VI. As can be seen, all the three interconnections are generally able to meet the electrical requirements. Without underfilling, the SSC has the highest fatigue life followed by the SB and the BON. Assuming Solomon's correlation is correct and without underfilling, all three interconnections are expected to fail to meet a fatigue life of 1000 cycles even with the most advanced organic substrates having a CTE of 10 ppm/K which are commercially available presently. However, with underfilling

TABLE V
MEASURED FATIGUE LIFE AND STATIC STRENGTH OF SSC INTERCONNECTIONS

Aspect ratio	0.9	1.8	2.2	2.8	3.9
Static strength (N)	35	23	17	12	8
Fatigue life (cycles)	600	1,800	2,700	3,600	8,600
Fatigue failure mode	Solder near end	UBM	UBM	UBM	Solder at mid-height

TABLE VI
COMPARISON OF THREE 100 μm PITCH INTERCONNECTION SCHEMES

EVALUATION TEMPLATE	Electrical Requirements			Mechanical Requirements: Fatigue Life without Underfill (cycles) [1000][1]			Mechanical Requirements: Fatigue Life with Underfill (cycles) [1000][1]		
100 µm pitch interconnection scheme	C (fF) [15]	L (pH) [50][1]	R (mΩ) [25][1]	CTE of substrate (ppm/K) 18	10	5	CTE of substrate (ppm/K) 18	10	5
Solder Ball (height 50 µm, diameter 70 µm)	17	32	5	-	417	2223	1320	1749	2108
BON (height 100 µm, length 50 µm)	18	46	28	11	348	4037	-	-	-
SSC (height 150 µm, diameter 50 µm)	21	51	33	31	518	4405	1484	3328	6886

[1] Target values

both SSC and SB can meet mechanical requirements with a substrate CTE of 10 ppm/K. Again, it must be emphasized that the above conclusions are dependent on the accuracy of Solomon's correlation. Also, the solder material currently used in the simulations is eutectic solder. In actual interconnections to be developed eventually, the solder to be used for the SB will be lead-free solder while that used for the SSC will be high-lead solder. Furthermore, the upper limit of the temperature cycling range of 150 °C is more extreme than the usual limit of 125 °C. Reliability tests which are currently being conducted will determine if acceptable fatigue lives will be achieved. However, the simulations do provide a good indication of the relative merits of the three proposed interconnection schemes in terms of mechanical reliability.

VII. CONCLUSION

A Nano Wafer Level Packaging program has been initiated to demonstrate future IC-package interconnections that meet the electrical, mechanical, cost, and pitch requirements. The initial focus, however, has been on 100-μm pitch. Three interconnection designs and technologies at 100 μm pitch such as rigid lead-free SB with no-flow underfill, compliant BON and semi-compliant SSC interconnection have been developed. It was noted that the optimum geometry for electrical requirements often conflict with that for mechanical requirements. Hence, extensive electrical and mechanical simulations have been carried out to optimize their designs in order to satisfy both the electrical and mechanical design parameters. The results indicate that the electrical requirements can be met but for meeting the mechanical requirements, it is necessary to use organic boards with a CTE of 10 ppm/K or lower. Of the three interconnection schemes proposed, the scheme which best meets the electrical requirements is the SB interconnection while the scheme which best meets the mechanical requirements is the SSC.

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