Integrated circuit immunity modelling beyond 1 GHz

Sjoerd Op 'T Land

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Sjoerd OP 'T LAND
ECOLE DOCTORALE : MATISSE
LABORATOIRE : IETR INSA de Rennes - ESEO-EMC

La modélisation de l'immunité des circuits intégrés au-delà de 1 GHz

Thèse soutenue le 20.06.2014
devant le jury composé de :

Frank Leferink
Professeur Université de Twente, Pays-Bas / *président*
Etienne Sicard
Professeur – INSA de Toulouse / *rapporteur*
Geneviève Duchamp
Professeure – Université de Bordeaux 1 / *rapporteur*
Jean-Luc Levant
Expert CEM – Atmel Nantes / *examinateur*
Richard Perdriau
Enseignant Chercheur HDR – ESEO Angers / Co-encadrant de thèse
Mohamed Ramdani
Enseignant Chercheur HDR – ESEO Angers / Co-directeur de thèse
M'hamed Drissi
Professeur – IETR INSA de Rennes / Directeur de thèse

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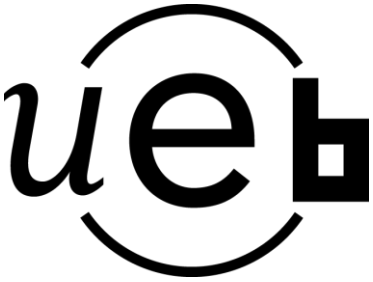
Integrated Circuit Immunity Modelling Beyond 1 GHz



En partenariat avec

[sumus] quasi nanos, gigantium humeris insidentes,
ut possimus plura eis et remotiora videre,
non utique proprii visus acumine, aut eminentia corporis,
sed quia in altum subvenimur et extollimur magnitudine gigantea

[we are] like dwarfs on the shoulders of giants,
so that we can see more than they, and things at a greater distance,
not by virtue of any sharpness of sight on our part, or any physical distinction,
but because we are carried high and raised up by their giant size

[nous sommes] des nains assis sur des épaules de géants,
nous voyons plus de choses et plus lointaines qu'eux,
ce n'est pas à cause de la perspicacité de notre vue, ni de notre grandeur,
c'est parce que nous sommes élevés par eux.

als dwergen [zijn wij], gezeten op de schouders van reuzen,
opdat we méér zien dan zij, en verder,
niet door onze eigen scherpe blik of uitmuntend lichaam,
maar omdat we, hoog opgetild, boven hen uit torenen

Bernard of Chartres (12th century)

Résumé

La compatibilité électromagnétique (CEM) est l'aptitude des produits électroniques à coexister au niveau électromagnétique. Dans la pratique, c'est une tâche très complexe que de concevoir des produits compatibles. L'arme permettant de concevoir des produits bon-du-premier-coup est la modélisation. Cette thèse étudie l'utilité et la faisabilité de la modélisation de l'immunité des circuits intégrés (CI) au-delà de 1 GHz.

Si les pistes des circuits imprimés déterminent l'immunité rayonnée de ces circuits, il serait pertinent de pouvoir prévoir l'efficacité de couplage et de comprendre comment elle découle du routage des pistes. Les solveurs *full-wave* sont lents et ne contribuent pas à la compréhension. En conséquence, un modèle existant (la cellule de Taylor) est modifié de manière à ce que son temps de calcul soit divisé par 100. De plus, ce modèle modifié est capable de fournir une explication de la limite supérieure pour le couplage d'une onde plane, rasante et polarisée verticalement vers une piste de plusieurs segments, électriquement longue et avec des terminaisons arbitraires. Les résultats jusqu'à 20 GHz corrèlent avec des simulations full-wave à une erreur absolue moyenne de 2,6 dB près et avec des mesures en cellule GTEM (Gigahertz Transversale Electromagnétique) à une erreur absolue moyenne de 4,0 dB près.

Si l'immunité conduite des CI est intéressante au-delà de 1 GHz, il faut une méthode de mesure, valable au-delà de 1 GHz. Actuellement, il n'y a pas de méthode normalisée, car la fréquence élevée fausse les observations faites avec la manipulation normalisée. Il est difficile de modéliser et de compenser le comportement de la manipulation normalisée. Par conséquent, une manipulation simplifiée et sa méthode d'extraction correspondante sont proposées, ainsi qu'une démonstration du principe de génération automatique de la carte d'essai utilisée dans la manipulation simplifiée. Pour illustrer la méthode simplifiée, l'immunité conduite d'un régulateur de tension LM7805 est mesurée jusqu'à 4,2 GHz.

À part la tendance générale des fréquences qui montent, il y a peu de preuve concrète qui étaye la pertinence de la modélisation de l'immunité conduite des CI au-delà de 1 GHz. Une simulation *full-wave* suggère que jusqu'à 10 GHz, la plus grande partie de l'énergie rentre dans la puce à travers la piste. Par concaténation des modèles développés ci-dessus, l'immunité rayonnée d'une piste micro-ruban et d'un régulateur de tension LM7805 est prédite. Bien que ce modèle néglige l'immunité rayonnée du CI

lui-même, la prédiction corrèle avec des mesures en cellule GTEM à une erreur absolue de 2,1 dB en moyenne.

Ces expériences suggèrent que la plus grande partie du rayonnement entre dans un circuit imprimé à travers ses pistes, bien au-delà de 1 GHz. Dans ce cas, la modélisation de l'immunité conduite au-delà de 1 GHz serait utile. Par conséquent, l'extension jusqu'à 10 GHz de la méthode de mesure CEI 62132-4 devrait être considérée. De plus, la vitesse et la transparence du modèle de Taylor modifié pour le couplage champ-à-ligne permettent des innovations dans la conception assistée par l'ordinateur. La génération semi-automatique des cartes d'essais dites maigres pourrait faciliter l'extraction des modèles. Certaines questions critiques et importantes demeurent ouvertes.

Mots clefs : EMC, IC, immunité, couplage champ-à-piste, cellule de Taylor, DPI, ICIM-CI, mesure, modélisation, simulation, GHz

Summary

ElectroMagnetic Compatibility (EMC) is the faculty of working devices to co-exist electromagnetically. In practice, it turns out to be very complex to create electromagnetically compatible devices. The weapon to succeed the complex challenge of creating First-Time-Right (FTR) compatible devices is modelling. This thesis investigates whether it makes sense to model the conducted immunity of Integrated Circuits (ICs) beyond 1 GHz and how to do that.

If the Printed Circuit Board (PCB) traces determine a PCB's radiated immunity, it is interesting to predict their coupling efficiency and to understand how that depends on the trace routing. Because full-wave solvers are slow and do not yield understanding, the existing Taylor cell model is modified to yield another 100× speedup and an insightful upper bound, for vertically polarised, grazing-incident plane wave illumination of electrically long, multi-segment traces with arbitrary terminal loads. The results up to 20 GHz match with full-wave simulations to within 2.6 dB average absolute error and with Gigahertz Transverse Electromagnetic-cell (GTEM-cell) measurements to within 4.0 dB average absolute error.

If the conducted immunity of ICs is interesting above 1 GHz, a measurement method is needed that is valid beyond 1 GHz. There is no standardised method yet, because with rising frequency, the common measurement set-up increasingly obscures the IC's immunity. An attempt to model and remove the set-up's impact on the measurement result proved difficult. Therefore, a simplified set-up and extraction method is proposed and a proof-of-concept of the automatic generation of the set-up's PCB is given. The conducted immunity of an LM7805 voltage regulator is measured up to 4.2 GHz to demonstrate the method.

Except for a general trend of rising frequencies, there is only little concrete proof for the relevance of IC immunity modelling beyond 1 GHz. A full-wave simulation suggests that up to 10 GHz, most energy enters the die via the trace. Similarly, the radiated immunity of a microstrip trace and an LM7805 voltage regulator is predicted by concatenating the models developed above. Although this model neglects the radiated immunity of the IC itself, the prediction corresponds with GTEM-cell measurement to within 2.1 dB average absolute error.

These experiments suggest the most radiation enters a PCB via its traces, well beyond 1 GHz, hence it is useful to model the conducted immunity of ICs beyond 1 GHz. There-

fore, the extension of IEC 62132-4 to 10 GHz should be seriously considered. Moreover, the speed and transparency of the modified Taylor model for field-to-trace coupling open up new possibilities for computer-aided design. The semi-automatic generation of lean extraction PCB could facilitate model extraction. There are also critical remaining questions, remaining to be answered.

Keywords: EMC, IC, immunity, field-to-trace coupling, Taylor cell, DPI, ICIM-CI, measurement, modelling, simulation, GHz

Contents

Résumé **i**

Summary **iii**

Contents **v**

Conventions **vii**

1 Introduction **1**
1.1 EMC 1
1.2 Complexity 2
1.3 Industrial need 7
1.4 Research context 9
1.5 This thesis 9

2 Field-to-trace Coupling **13**
2.1 Introduction 13
2.2 State of the Art 14
2.3 Meshed Taylor Model 18
2.4 Modified Taylor Model 33
2.5 Full-wave simulation 54
2.6 Measurement 60
2.7 Conclusions 85

3 IC Conducted Immunity **89**
3.1 Introduction 89
3.2 State of the Art 90
3.3 Modelling passive components 96
3.4 Lean Method 109
3.5 Specialisation: SOIC8 Extraction PCB 120
3.6 Case study: LM7805 131
3.7 Conclusions 140

4 PCB Radiated Immunity **143**
4.1 Introduction 143
4.2 State of the Art 144
4.3 Explorative Simulation 145
4.4 Cascading Trace and IC Models 148
4.5 Conclusions 161

5 Conclusion and Perspectives **163**
5.1 Introduction 163
5.2 Modified Taylor Model for Field-to-trace Coupling 163
5.3 Lean GDPI Method 167
5.4 ICIM-CI Beyond 1 GHz Considered Possible and Useful 169

Bibliography **173**

A Scientific Production **183**

Acknowledgments **185**

Abbreviations **189**

Definitions **195**

Conventions

Units. *Système Internationale* (SI) units, as opposed to Gaussian and imperial units, are employed, unless otherwise noted.

All decibel values, dimensional or dimensionless, are prefixed with their sign, so all excess pluses or minuses are operators [1].

Passivity. The passive sign convention is used as shown in Figure 1.

Responsibility. When reading about the responsibility of anything but a person, this should of course be understood as a metaphor; it facilitates the explanation of cause and effect. In the end, only something with freedom of choice can be accountable. If anyone, these are human beings [2, p. 165ff.].

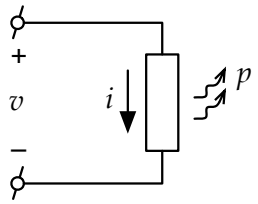


Figure 1: Passive sign convention for voltage and current: a positive product vi means that net power p is dissipated in the element.

Symbols.

B magnetic field in T

H magnetic field in Am^{-1}

E electric field in Vm^{-1}

ε The permittivity ε relates the displacement of charges D in a linear and homogeneous material with the electric field E as follows:

$$D\mathrm{e}^{\mathrm{j}\omega t} \equiv \varepsilon_0 \varepsilon_r E \mathrm{e}^{\mathrm{j}\omega t}, \tag{1}$$

where the relative permittivity ε_r is a second rank tensor in general, which reduces to a scalar for isotropic materials. Conventionally, the real and imaginary parts are denoted as follows:

$$\varepsilon_r = \varepsilon_r' - \mathrm{j}\varepsilon_r''. \tag{2}$$

Under above sign conventions, ε_r' quantifies the energy storage in the material and ε_r'' quantifies the loss.

$\mp$ minus for the near end and plus for the far end

c per unit length (pul) capacitance in Fm^{-1}

l pul inductance in Hm^{-1}

g pul conductanse in Sm^{-1}

r pul resistance in $\Omega\mathrm{m}^{-1}$

ℓ total trace length in m

ℓ_u length of uth trace segment in m

c_0 the speed of light in m/s, supposedly a constant

p position parallel to the (first) trace segment in m

t position transversal to the (first) trace segment in m

n position normal to the (first) trace segment in m

ϕ azimuth

θ elevation

Z_c characteristic impedance

CHAPTER 1

Introduction

Abstract. ElectroMagnetic Compatibility (EMC) is the faculty of working devices to co-exist electromagnetically. In practice, it turns out to be very complex to create electromagnetically compatible devices. The weapon to succeed the complex challenge of creating First-Time-Right (FTR) compatible devices is modelling. In the context of worldwide Gigahertz Direct Power Injection (GDPI) research and the French SEISME project, this thesis investigates whether it makes sense to model the conducted immunity of ICs beyond 1 GHz and how to do that.

1.1 EMC

Problems due to electromagnetic interaction between devices range from funny to lethal. For example, a rusty microwave oven could trigger Mazda, Mitsubishi and Toyoto car alarms. For another example, a New Jersey TV transmitter set off baby monitors at nearby intensive care. Annoyed by the many false alarms, the nurses started to ignore the alarms, killing an estimated 6 babies [3].

For public health and safety, governments require devices to be compliant with EMC standards. For example, the Federal Communications Commission (FCC) essentially requires that 'no harmful interference is caused and that interference must be accepted (...)' by devices on the US market [4]. In Europe, manufacturers are trusted to distinguish and perform relevant EMC testing before labeling their products with a CE-marking.

Manufacturers may also be intrinsically motivated to deliver compatible products. Negatively, the fear for reputation damage pushes internal standards. Positively, manufacturers that strive for excellence will also take EMC into account.

Very often, EMC problems can be understood in terms of this directed graph of electromagnetic energy propagation:

$$\text{aggressor} \longrightarrow \text{coupling path} \longrightarrow \text{victim}. \tag{1.1}$$

For example, the New Jersey TV transmitter could be considered the aggressor, the baby monitor cabling the coupling path and the nurse's control panel the victim.

In this view, the problem could for example be solved by (1) reducing the TV transmitter power, by (2) shielding the cable, by (3) applying an input filter at the control panel or a combination of solutions.

The graph can be simplified by merging the coupling path into the victim:

$$\text{aggressor} \longrightarrow \text{victim}, \tag{1.2}$$

and we can say "the aggressor's *emissions* and the victim's *susceptibility* cause a problem".

In this view, proposed solution (1) is called a reduction of emissions, whereas solution (2) and (3) is called a reduction of susceptibility (or an increase of *immunity*). Notice that there are also cases where the system boundaries are less obvious.

Sometimes the electromagnetic energy is completely guided along the coupling path, for example from an IC power supply pin, along a PCB trace to an analog input pin of another IC. This problem is entirely *conducted*: the conducted emission of the first IC and the conducted susceptibility of the second IC cause a problem.

In all other cases, the coupling path contains free space propagation, for example in the mentioned New Jersey case. The unshielded cable acts as an antenna and converts *radiated* electromagnetic waves to conducted voltage/current waves. This way, the radiated emission of the TV transmitter and the conducted immunity of the control panel cause a problem.

In this paradigm, the EMC of any device can be quantified by its radiated emission and immunity. Devices that have interfaces along which guided electromagnetic energy can leave and enter, also have conducted emission and immunity. The EMC of ICs, for instance, can be quantified on all four aspects, as they have metallic pins.

Notice that the boundary between guided and free space energy is not always clear. For example, the Bulk Current Injection (BCI) method induces (guided) currents by a magnetic field (in free space). Therefore, it has been considered both a conducted and a radiated test method.

1.2 Complexity

Designing a device that is electromagnetically compatible or modifying a device to become so is engineering. That is, solving a problem, given a number of degrees of freedom: the *design parameters* (e.g. resistor value, trace length or circuit topology). These design parameters span the design space D, which contains every possible design. The

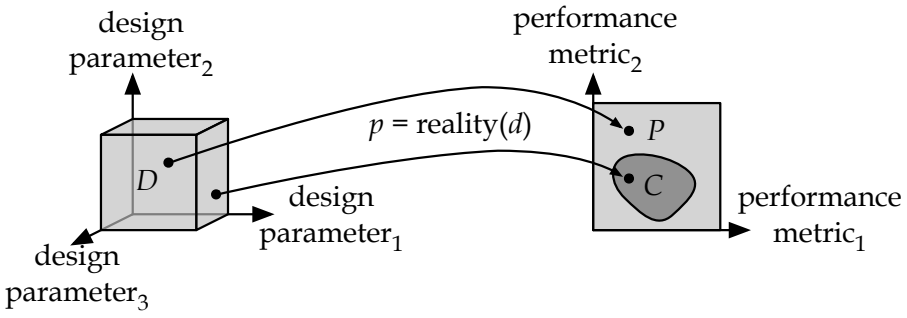


Figure 1.1: Reality maps design space into performance space. One successful design and one unsuccessful design are shown.

problem is solved when the performance of the design complies with the requirements, expressed in terms of performance metrics (e.g. immunity, speed, bandwidth, cost or development time). These performance metrics span the performance space P, of which compliance C is a subspace (e.g. immunity meets or exceeds DO-160F and development time is shorter than one month). Reality determines the performance of each design candidate, reality : $D \rightarrow P$. To successfully design is to find a design d, of which the performance p is compliant with the requirements: any $d \in D$, such that reality$(d) \in C$, as shown in Figure 1.1.

We believe the relevant reality to depend on a small number of deterministic physical laws: those of Newton[1], Maxwell[2] and that of thermodynamics, for example. They can be summed up like so

$$U = (F - ma)^2 + (\nabla \cdot D - \rho)^2 + \ldots + (T\mathrm{d}S - P\mathrm{d}V - \mathrm{d}E)^2 \tag{1.3}$$

and the behaviour of all matter can be described by this universal equation[3]

$$U = 0. \tag{1.4}$$

The next step is to apply the universal equation to the design parameters and to solve for the performance metrics in order to obtain the reality function. Finally, the reality function needs to be inverted to find a compliant design d from a performance $p \in C$.

Except for the proverbial 'spherical cow in vacuum' [5], this is unfortunately never possible. The dimension of design space is generally high and reality is too hard to understand, let alone analytically invertible.

One practical alternative is physical simulation. For a given design d, a (multi-) physics simulator can calculate the performance p. Using trial-and-error, the design

[1] Sir Isaac Newton (1643-1727)
[2] James Clerc Maxwell (1831-1879)
[3] I stole this idea of a useless universal equation from an author that I forgot.

parameters d can be tuned to make the design compliant. The advantage of physical simulation is that it is relatively easy to set-up. The downside is that it is generally time-consuming and it yields little insight. Moreover, the physical simulation of industrial products is often impossible, because the exact constitution of components is secret. Even if these details were available, simulation time would explode: a car of 10^0 m consisting of ICs with 10^{-7} m details would require a hexahedral mesh in the order of $10^{7\times7\times7}$ cells. Even when applying multi-scale meshing techniques to reduce the number of mesh cells, the simulation will remain time-consuming.

Another practical alternative is experimentation. The advantage with respect to simulation is that results may be obtained rather quickly, once the set-up is made. However, creating prototypes, setting up measurements and using rare instruments, like an anechoic chamber, is not free. Similarly to simulation, no fundamental insight is obtained by experimenting with complex systems.

It can be concluded that analysis and simulation of the physical laws, as well as experimentation on complex systems do not yield fundamental insight in the relation between design parameters and performance.

Therefore, simplified views on reality are always applied: *models*. Modeling is design-oriented *approximation*: reality is approximated to become easily invertible. For example, the resistive voltage divider of Figure 1.2 is required to have a voltage transfer $H = 1/3$, when loaded by an unknown load $R_L > 10\,\mathrm{k}\Omega$. The real relation between design parameters (R_1 and R_2) and the performance metric (H) is given by

$$H = \frac{R_1 /\!/ R_L}{R_1 /\!/ R_L + R_2} = \frac{R_1 R_L}{R_1 R_2 + R_1 R_L + R_2 R_L}. \tag{1.5}$$

Suppose that R_L and R_1 (R_2) would be given, it is not obvious to find R_2 (R_1). The equation is true, but one cannot 'see through' it, the relation is *opaque*.[4]

Conversely, when R_1 is chosen much smaller than R_L, the transfer becomes approximately:

$$H \approx \frac{R_1}{R_1 + R_2} \rightarrow \frac{R_2}{R_1} \approx \frac{1}{H} - 1, \tag{1.6}$$

and R_2 follows naturally. Moreover, one sees directly that only the ratio between R_1 and R_2 is fixed by H. Hence, the relation is considered *transparent*.

To summarize, the relation between design parameters and performance metrics can become more transparent by approximation. The price paid is reduction in accuracy and in validity domain (above approximation only holds for $R_1 \ll R_L$).

Note that transparency is subjective: experienced engineers will also see through (1.5). However, even these subjects will consider (1.6) more transparent than (1.5). Therefore, relative transparency is objective.

[4] Dr. Middlebrook calls this an *high-entropy* equation, useless in Design-Oriented Analysis (D-OA).

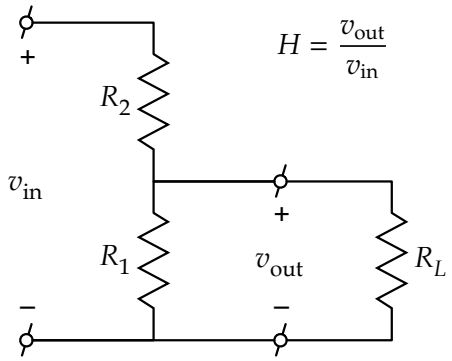


Figure 1.2: Resistive voltage divider with resistive load.

There are general modeling techniques, that are not specific to EMC (although EMC examples will be given).

One modeling technique is *hierarchical segmentation*: a system topology is chosen, for which the system performance is known as function of the performances of its constituants (e.g. a cascade of blocks has a gain that amounts to the product of the gains of the blocks). Next, a successful set of sub-system performances is chosen (e.g. a link budget is distributed). Now, for each sub-system, the requirements are known, and the engineer can try to design them one by one, and simplify again if necessary.

A related technique is the *weak coupling* assumption. That is, although all interactions are really bilateral, only a one-way interaction is taken into account. In the New Jersey example cited on page 1, a TV transmitter induces a cable current, which in turn will re-radiate and be received by the TV transmitter, which will slightly modify its operating point, which will in turn. . . , and so forth. Fortunately, the cable's re-radiation received by the TV transmitter is so weak, that it can be neglected. Only the action of the TV transmitter on the cable needs to be considered to explain the harmful interference. Indeed, when speaking about emission and immunity, weak coupling is implicitly assumed.

Another simplification is to only look at the *worst case*. For example, if decreasing the distance between aggressor and victim makes everything worse, it suffices to prove that there is no harmful interference at the smallest required distance. Instead of having to prove EMC for all distances, we only need to prove it for one particular distance (the worst case). A variant is to consider the *typical case* and base conclusions on a statistic or probabilistic mean.

Intelligent use of phenomenological, descriptive or *black-box models* enables the construction of transparent models. For example, to design a circuit, it might suffice to know the constant ratio between the voltage across the terminals of a resistor and current through it (its resistance). That way, the resistor's material and dimensions do not clutter the circuit model. However, with rising frequency, a parallel capacitance depending on the pad distance becomes necessary to sufficiently model the resistor's

behaviour. Notice that this pad-distance-dependent resistor model is grey-box: it offers one more level of explanation, and then resorts to description again. Models with more than one level of explanation are called *white-box model*. Intelligence is needed to discern whether or not the validity domain of the black-box model matches its application.

There are also modelling techniques specific to electromagnetics or to EMC.

If structures are small with respect to the wavelength of propagating waves, electromagnetic waves can be supposed to propagate infinitely fast. That is, although the field is changing with time (not temporally uniform), fields (hence, voltages and currents) can be considered spatially uniform. Electro- and magnetostatic analysis may be applied to obtain lumped-element capacitances and inductances. This is called the *quasi-static approximation*.

If guided waves need to be considered, and the waveguide is homogeneous, uniform and has an infinitely small cross-section with respect to the wavelength, only the fundamental Transversal ElectroMagnetic (TEM) mode needs to be considered. As few real waveguides are homogeneous, no real waveguide is uniform (that would require infinite length) and all real waveguides have finite cross-section, a Quasi-TEM (QTEM) wave is said to propagate on them.

Finally, emission and susceptibility are often characterised in terms of the *far field magnitude*. In general, an aggressor can generate any spatiotemporal field that satisfies the Maxwell equations. Hence, it needs to be described as $\vec{E}(\vec{r},t)$ or $\vec{H}(\vec{r},t)$. At some distance from the aggressor, however, the field tends to a plane wave with the wave impedance of the vacuum. Assuming susceptibility to be independent of the relative phase of the field's spectral components, it can be described with the magnitude vector of its Fourier transform: $|\vec{E}(\vec{r},\omega)|$. Assuming a linearly polarised wave, the field only decays with the distance $\vec{r}$. Now, the vector $|\vec{E}(\omega)|$ at a rough distance suffices to describe the emissivity of a system. Reciprocally, the susceptibility of a system can be described in terms of a maximum allowed electric field magnitude vector.

Using these and other modelling techniques, the reality function can become invertible: the engineer then knows what knob (design parameter) to turn in which direction to improve performance.

Modelling is an art: if a model is too complicated, it does not yield the wanted insight or it is too expensive to use (tools, training, measurement and simulation time). If a model is too simple, it does not sufficiently describe the reality, so it does not yield the needed insight either. Breedveld calls a model that strikes the right balance for a given problem a competent model. Another way to put it: the Return On Modelling Effort (ROME) should be maximum.

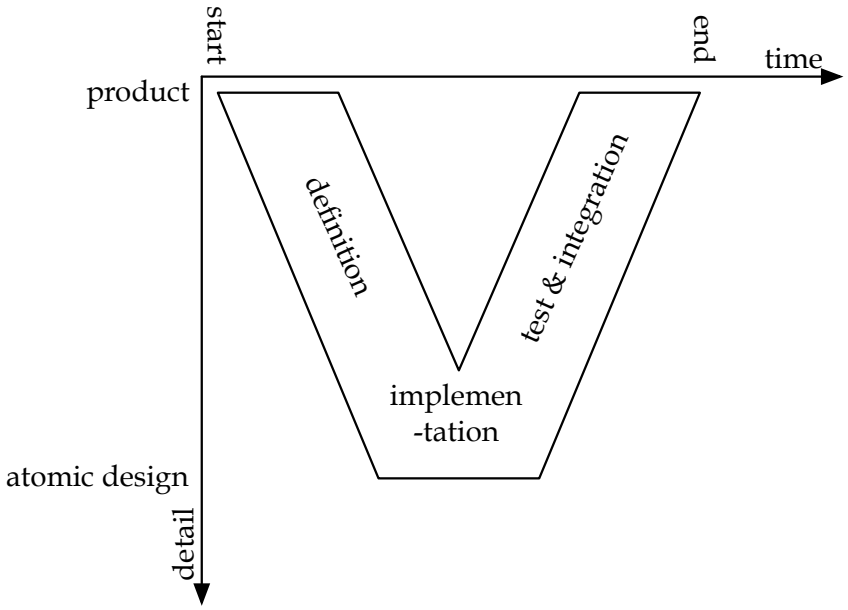


Figure 1.3: V-model for systems engineering.

1.3 Industrial need

For an industrial product, EMC is only one of the performance metrics. Moreover, the total engineering task is distributed over multiple persons. One way of distributing the task is by the hierarchical segmentation mentioned on page 5. A classical way to map this method on time is by means of the V-model sketched in Figure 1.3 [6]. In this paradigm, EMC needs to be taken into account in each phase: definition, implementation and test.

In the definition phase, the product requirements are propagated down the product hierarchy. For example, law may require an electric car to meet the CISPR 12 limits on radiated emissions. Knowing that these emissions will mainly emanate from the electric motor and from the back-to-front cable, requirements can then be imposed on the motor and on the cabling. That way, the cabling designers and motor designers can both be given requirements, with confidence that the combination cable-motor will perform sufficiently when integrated. Generally, more understanding is needed on how subsystem EMC performance 'adds up' to system EMC performance.

In the implementation phase, the subsystem requirements should lead to produceable subsystems. There, the influence of detailed design decisions on subsystem performance is needed. For example, is this filter capacitor needed to pass the BCI test, imposed as subsystem requirement? Or: this IC seems to perform better in DPI, but it is € 0.02 more expensive than another. Does the former IC cost outweigh the risk of not passing the BCI test? Generally and again, more understanding is needed as

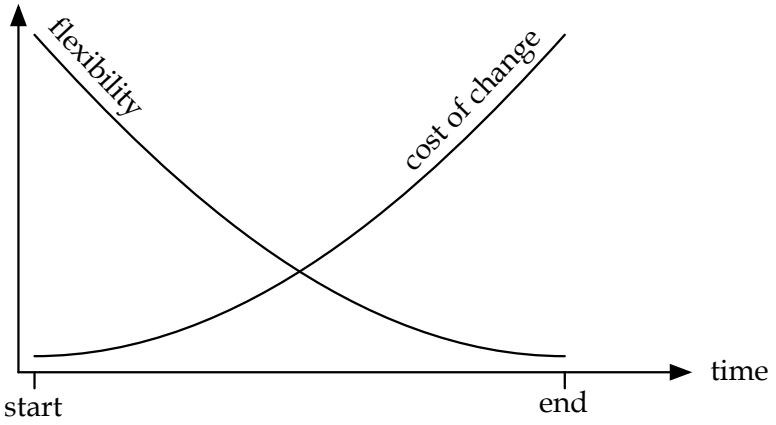


Figure 1.4: Flexibility and consequent cost of change along product design time.

to how component EMC performance 'adds up' to subsystem (PCB, assembly) EMC performance.

In the test and integration phase, the subsystems are assembled, performing the predefined tests at each hierarchical level. For example, after checking that the cable and the motor each do not radiate more than required, the combination battery-cable-motor is tested. If the latter test passes, too, the combination is mounted in an empty chassis to verify that the vehicle does not radiate more than required because of the cable and motor. Finally, the complete car prototype's radiated emissions are measured to make sure that the car is road legal. Standardised tests exist at all detail levels, but the main challenge remains to understand why a test failed in order to remove the root cause.

While the complete, feasible product crystallises along all these phases, there is less and less flexibility in the design. Consequently, the cost of a hypothetical change is high, as illustrated in Figure 1.4. For example, the car radio and Global Positioning System (GPS) receiver are discovered to interfere in a very late integration test. It would have been easy to place them apart early on, but now that the injection molds are already made, the only solution is to shield the GPS receiver stage. Therefore, although few details are available in the early design, the earlier tools can orient the design, the better.

The masterpiece of EMC engineering is to produce a product prototype that is First-Time-Right (FTR). This is currently only a dream, because commonly, multiple product prototypes are needed before reaching compliance.

1.4 Research context

Around the world, thousands of people are trying to advance EMC in various ways: on different hierarchical levels (from vehicle to transistor), with different beneficiaries (from a company to the general public) and with different modelling techniques (as outlined before). The topic, beneficiaries and methodology of this thesis are partly determined by the context in which it was prepared: on the crossroads of the French project SEISME and the worldwide GDPI research, in the ESEO-EMC laboratory.

Simulation de l'Emission et de l'Immunité des Systèmes et des Modules Electroniques (SEISME) or Simulation of Emission and Immunity of Electronic Systems and Modules is a project labeled by Aerospace Valley, performed from 2010 to 2014 for the French Ministry of Defence. It financially federates research to lower the cost of EMC, by enabling virtual prototyping of new and modified electronic systems [7]. Indeed, the modification of systems is a recurring problem in aerospace industry, because of the obsolescence of components occurring before that of long-lived airplanes. For example, replacing just one IC by its successor in an airplane necessitates another qualification of the entire airplane. Instead, it would be a great cost saving to be able to reliably simulate the effect of replacing the IC on the EMC performance of the airplane. To that end, the SEISME project comprises work at all hierarchical levels (IC, PCB, rack and vehicle). This thesis is co-financed by the fifth SEISME work package: 'Modelling Methodology Development for EMC'. As a result, the beneficiary of this thesis is the general public.

Simultaneously, worldwide research on the EMC of ICs is going on. In 2009, Ramdani et al. predicted that measurement methods for conducted immunity of ICs in the $3 - 10\,\mathrm{GHz}$ range would be in industrial use around 2010, and modelling techniques around 2015 [8]. An informal collaboration on the measurement method was led by Etienne Sicard, with participants in France (ESEO, INSA Toulouse), in Spain (*Universitat Polytècnica de Catalunya* (UPC)) and in Taiwan (Bureau of Standards, Metrology & Inspection (BSMI)). Formerly called eXtended DPI (X-DPI), it was later given a more ontological name: Gigahertz Direct Power Injection (GDPI).

The author performed the research in the ESEO-EMC laboratory (formerly GRACE), part of *Institut d'Électronique et de Télécommunications de Rennes* (IETR), Mixed Research Unit (UMR) National Centre for Scientific Research (CNRS) 6164. Since 2000, Ecole Superieure d'Electronique de l'Ouest (ESEO) performs research on EMC in collaboration with industrial partners, as outlined in Figure 1.5. ESEO-EMC has experience in black-, gray- and white-box IC modelling for EMC, but is only autonomous in black-box modelling. For gray- and white-box modelling, close collaboration with semiconductor foundries is needed. This context favoured black-box modelling.

1.5 This thesis

Formulated as falsifiable *main* hypothesis, this thesis states that

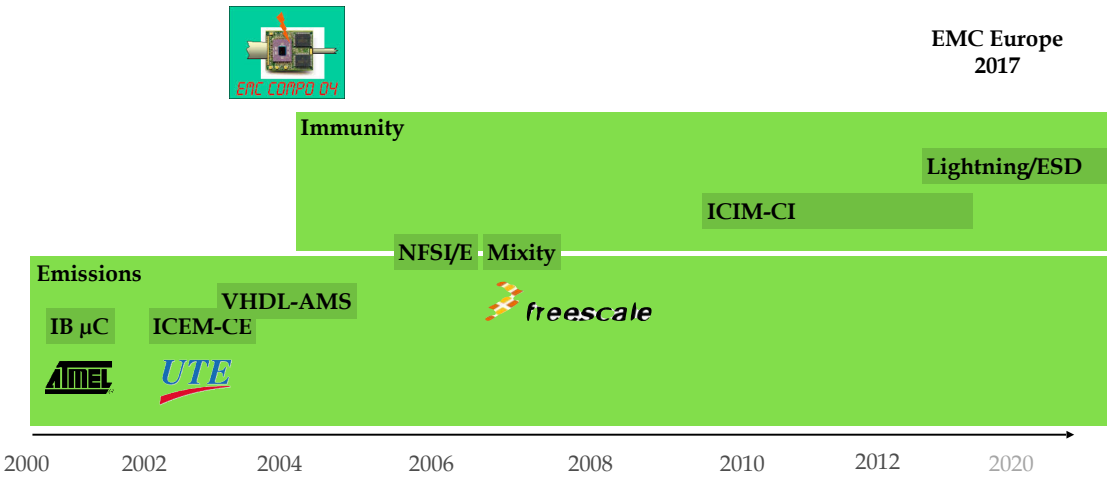


Figure 1.5: Research topics, partnerships and events of ESEO-EMC.

it is useful and possible to model the conducted immunity of ICs beyond 1 GHz.

In Popper's[5] tradition of falsification and the more recent Test Driven Development (TDD), the goal of this thesis is to render the main hypothesis falsifiable by making our underpinning repeatable for anyone with an electronic or microwave background.

Modeling the IC's conducted immunity is *useful* if it is necessary for a competent model of the system's radiated immunity. This thesis will consider the common system of a microstrip PCB trace leading to an IC, as shown in Figure 1.6a. A weakly-coupled model of the system's immunity is given in Figure 1.6b: the incoming radiation illuminates both trace and IC, and electromagnetic energy is also conducted from the trace to the IC. If the IC suffers much more from the radiation picked up by the trace, than from the radiation picked up by the IC itself, the radiated immunity of the IC can be neglected. This is the *dominant-conduction* hypothesis:

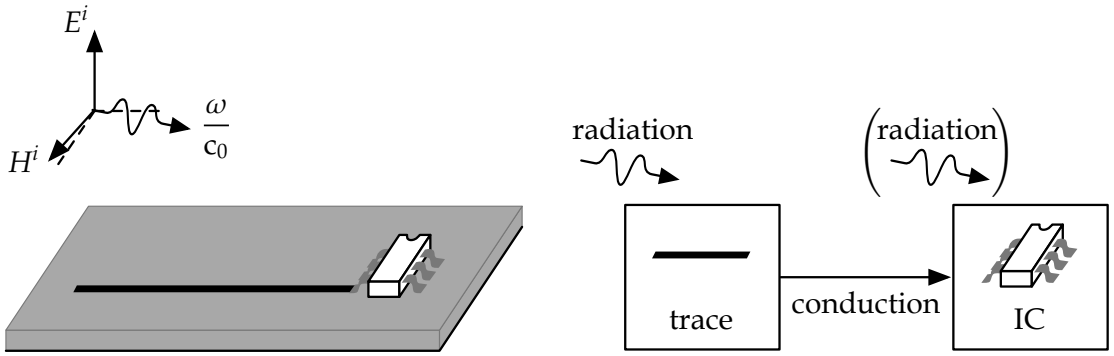
in a typical trace-IC system, the IC is predominantly disturbed by the radiation gathered by the trace and conducted into the IC until above 1 GHz.

If the dominant-conduction hypothesis is true, modeling the conducted immunity of ICs beyond 1 GHz is useful.

Modeling the IC's conducted immunity beyond 1 GHz can be proved *possible* by doing it once.

This thesis is structured as shown in Figure 1.7. In Chapter 2, a model for field-to-trace coupling will be developed that remains transparent for high frequencies. In Chapter 3, a method for black-box-modeling of the conducted immunity of an IC beyond 1 GHz

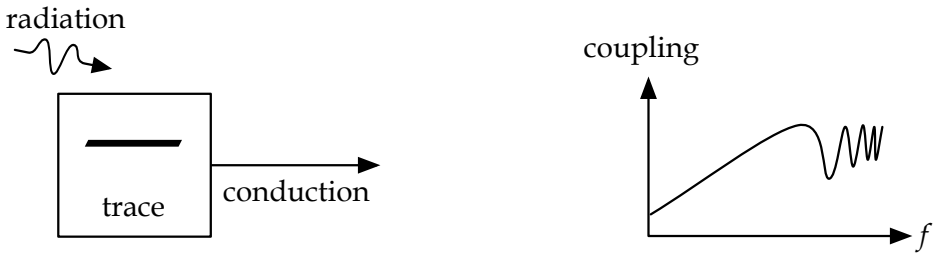
[5]Sir Karl Raimund Popper (1902–1996)



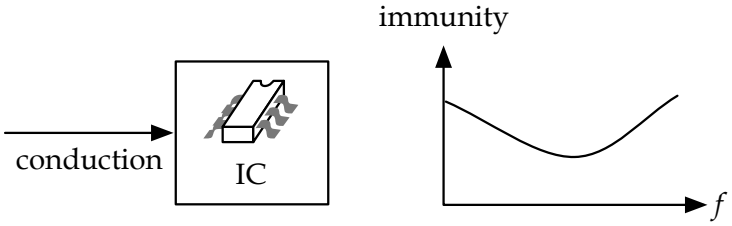
(a) Perspective on the system. (b) Weakly-coupled model of the system.

Figure 1.6: Illumination of the system: a trace connected to an IC.

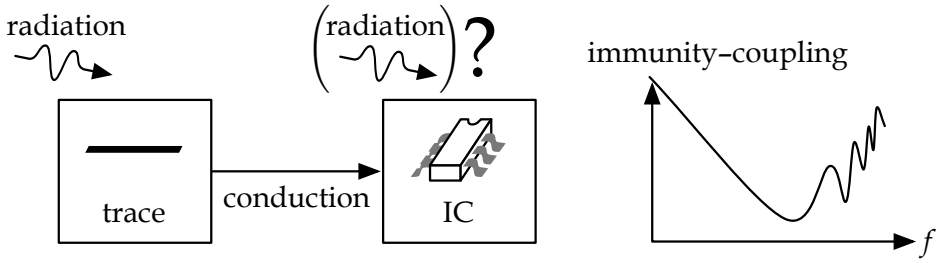
will be developed, which proves that it is *possible*. These two models will then be cascaded and compared to measurement in Chapter 4. If the latter cascade (which neglects the IC's radiated immunity) correlates well with measurement, this underpins the dominant-conduction hypothesis, i.e. that the exercise is *useful*. Overall conclusions and perspectives on future research will be given in Chapter 5. In each chapter, previous work on that topic will be reviewed.



(a) Chapter 2 models and measures field-to-trace coupling.



(b) Chapter 3 models IC conducted immunity from measurement.



(c) Chapter 4 models and measures PCB radiated immunity by concatenating Chapter 2 and 3.

Figure 1.7: Structure of this thesis.

CHAPTER 2

Field-to-trace Coupling

Abstract. If the PCB traces determine a PCB's radiated immunity, it is interesting to predict their coupling efficiency and to understand how that depends on the trace routing. Because full-wave solvers are slow and do not yield understanding, a faster, existing circuit model is employed. This model is modified to yield another 100× speedup and an insightful upper bound, for vertically polarised, grazing-incident plane wave illumination of electrically long, multi-segment traces with arbitrary terminal loads. The results up to 20 GHz match with full-wave simulations to within 2.6 dB average absolute error and with GTEM-cell measurements to within 4.0 dB average absolute error.

2.1 Introduction

How much radiated electromagnetic energy is captured by typical PCB traces? What trace illumination induces the worst case? What are the design parameters that have significant effect on the worst-case coupling?

In practice, radiated electromagnetic energy can arrive in all sort of forms on a PCB trace. It can come from nearby aggressors, like neighbouring traces (*crosstalk*) or cabling. In that case, the full structure of the electric or magnetic field needs to be taken into account. Moreover, as the aggressor is close, the weak-coupling assumption might not hold. On the other hand, the disturbing energy can come from far-away aggressors, like a TV transmitter or Intentional ElectroMagnetic Interference (IEMI). In that case, the far-field and weak-coupling assumptions may be applied, as explained in section 1.2. In the sequel, a far-field, weakly coupled and linearly polarised source will be assumed.

As illustrated in Figure 2.1, typical PCB traces meander with 90° and 45° bends. Width changes and none-chamfered bends occur, introducing impedance discontinuities. On typical 2-layer PCBs, traces can be considered as MicroStrip (MS) lines above

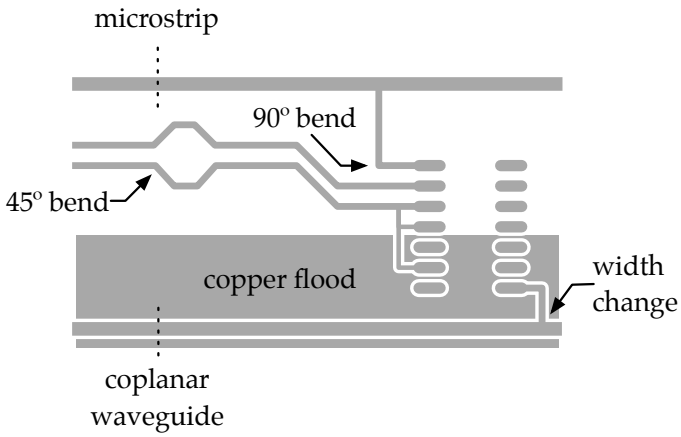


Figure 2.1: Example copper artwork of a typical PCB. Geometrical features that might need modelling are indicated.

a ground plane. On multi-layer PCBs, copper floods to the left and right of a trace make for a CoPlanar Waveguide (CPW) or Grounded CoPlanar Wave-guide (GCPW) if a ground plane is present. In the sequel, meandered MS traces of constant characteristic impedance will be considered, unless mentioned otherwise.

As most circuits are designed to function with node voltages and mesh currents (as opposed to travelling waves), we are interested in trace terminal voltages or currents. Knowing the terminal impedances, the terminal voltage can be converted into the terminal current and vice versa. Because of the author's taste for node analysis, the terminal voltages will be sought, but this really is an arbitrary choice. To simplify, only the case of a trace with exactly two terminals will be considered, unless stated otherwise.

The state of the art will be reviewed in section 2.2. One existing model (Taylor's) will be applied with novel meshing in section 2.3. Although fast, this model is opaque, and therefore, a transparent model will be developed in section 2.4. To challenge both models, full-wave simulations will be performed in section 2.5 and measurements in section 2.6. A concluding overview of the developed models will be given in section 2.7.

2.2 State of the Art

The quest for field-induced voltages at the terminals of general lines is not new. The published models until 2014 will be reviewed, going from physical but opaque to transparent but simplistic.

A versatile solution is to enter the entire aggressor and victim into a full-wave multiphysics solver with circuit co-simulation (e.g. CST Design Studio or COMSOL Mul-

tiphysics), thus including both geometry and electronics. The advantage is that quite many physical effects can be taken into account. Take for example a PCB that heats up, expands, thereby creating a resonating slit in its shielding enclosure, of which the emissions are captured by another PCB's trace and finally rectified to an interfering frequency by an ESD protection network. When all of the geometry and the circuit is precisely entered into the simulation, it is possible to predict this kind of phenomena.

However, it takes a lot of time to precisely enter the geometry and circuit into a simulation. Competent models of electronics are not free, if they are available at all. On top of that, very detailed multi-domain simulations necessitate significant calculation time. In the above example, the simulation must run for a sufficient time to reveal the thermally induced deformation with electromagnetic and then electronic consequences.

Moreover, this method yields little insight. For example, in practice, the aggressor PCB is not always installed in the same position in its enclosure. Does this matter? Did our simulation give the worst case result? Is it worth the extra cost to improve the mechanical fixation of the aggressor in its enclosure? Does it help to reduce the victim trace length? These kind of questions can only be answered by time-consuming parameter sweeps. Even then, sweeping the entire design space is impossible, so *cocktail-effects* (results of a particular mix of causes) might never be detected.

Over and above that, this approach yields very specific results. For example, the EMC of the victim PCB can be demonstrated for one specific aggressor, but in practice there is an infinity of potential aggressors. What can be generally concluded about the victim's immunity? Therefore, the first step towards genericity is splitting aggressor and victim, which requires the weak coupling assumption to hold.

Under the weak coupling assumption, immutable electromagnetic energy impinges on PCB traces and causes induced terminal voltages – and the analysis stops there. A common means to understand the behaviour of PCB traces is transmission line theory: the supposition that there be only a differential transverse electromagnetic mode (TEM).

The common mode is negligible, because the ground planes of modern PCBs suppress it and because the common mode response across the terminals is generally small [9, 10]. A typical microstrip line gradually becomes multimodal above this cut-off frequency [11]:

$$f_{\mathrm{MS,TEM}} = \frac{21.3 \times 10^6}{(w + 2t)\sqrt{\varepsilon_r + 1}} = \frac{21.3 \times 10^6}{(1.0 \times 10^{-3} + 2 \cdot 1.6 \times 10^{-3})\sqrt{4.6 + 1}} = 2.3\,\mathrm{GHz}, \quad (2.1)$$

where trace width w and substrate thickness t represent a relatively large trace on a two-layer FR4 substrate (permittivity $\varepsilon_r = 4.6$), employing *Système Internationale* (SI) units. With PCBs that have an increasing number of layers (decreasing t) and an increasing trace density (decreasing w), this cut-off frequency is only increasing (a $50\,\Omega$ microstrip on a four-layer substrate becomes multimodal from about 8.7 GHz upwards). It can be concluded that, while checking these validity limitations, PCB traces can be considered as transmission lines up to several GHz.

For example, using coupled transmission lines, Mandić predicted the coupling between a Transversal ElectroMagnetic (TEM) cell septum and PCB traces [12] with the Method of Lines (MoL) and a circuit simulator. His model is not transparent, because it uses a circuit simulator. Neither is it intrinsically generic, because the TEM cell geometry is entered in detail, whereas it is supposed to represent a general aggressor. Finally, Mandić' model is not weakly coupled, because it also predicts the effect of the trace on the TEM cell.

There are three weakly coupled transmission line based models [9, 13]: that of Taylor et al. [14], Agrawal et al. [15] and that of Rachidi [16]. They all model a transmission line as a cascade of *cells*. Each cell models a line slice that experiences a uniform field along its length dp. A bifilar (two-wire) transmission line and its one-cell models are depicted in Figure 2.2 for the case of uniform field between both wires (along t). As can be seen, the passive slice of transmission line dp is enriched with one or two distributed sources representing the field induction. In the case of Agrawal's and Rachidi's model, additional sources are needed at both terminals. As the wavelength along the line decreases, the line needs to be considered as a cascade of short enough cells, such that the field is uniform enough along each cell. From two cells upward, the terminal voltage expressions are no longer transparent.

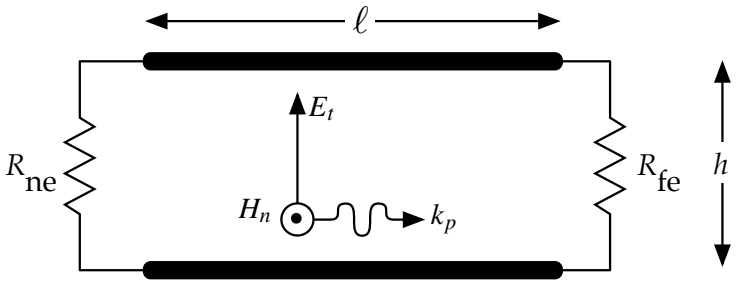
Paul extended Agrawal's model to multi-conductor transmission lines [17, §12.2]. He showed that the coupling distributed on the line can be lumped into a voltage and a current source at only one terminal by means of convolution. Moreover, he elaborated the case of a lossless multi-conductor transmission line in a homogeneous medium, illuminated by a plane wave.

However, in the case of a PCB trace, the medium is non-homogeneous. Bernardi and Cichetti studied the case of arbitrary incident plane wave illumination of a microstrip with arbitrary loads [18]. Unfortunately, their result is opaque and only allows for numerical simulation.[1]

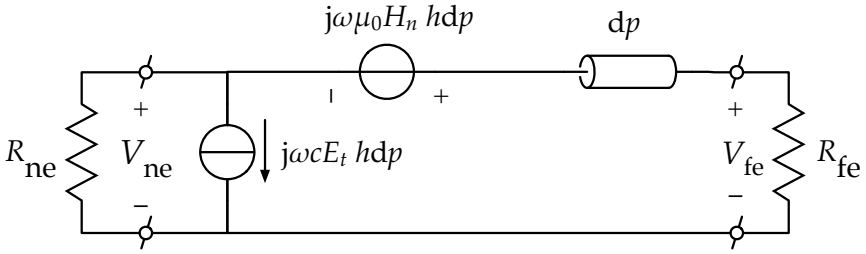
Leone, on the contrary, found transparent expressions for the same case, using Agrawal's model, the Baum-Liu-Tesche (BLT) equation [20] and Snell's law of refraction [19]. He then simplifies by assuming that both loads be matched, which he showed to be a reasonable approximation for moderately mismatched loads. Secondly, the transient excitation should be essentially low-frequency, which is reasonable for Nuclear ElectroMagnetic Pulse (NEMP) testing. From his model, he concludes that end-fire (parallel with the line), vertically-polarised illumination induced the worst case voltage at the near-end terminal.

Indeed, a simple expression for the worst case incidence and trace are useful for testing and design, respectively. Lagos built a numerical algorithm around Leone's model to find the worst case incidence with known load impedances [21]. Although this algorithm could serve to falsify analytical models, it does not prove anything general, nor is it transparent. Magdowski derived analytical expressions from Agrawal's formulation

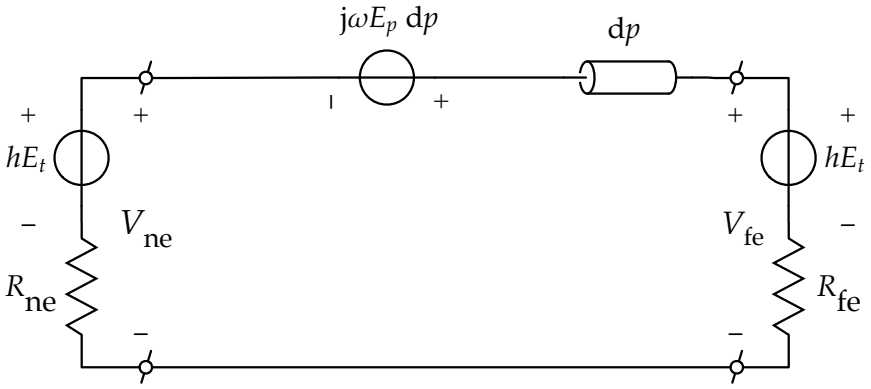
[1] Or, as Leone puts it, "general, but very lengthy equations" [19].



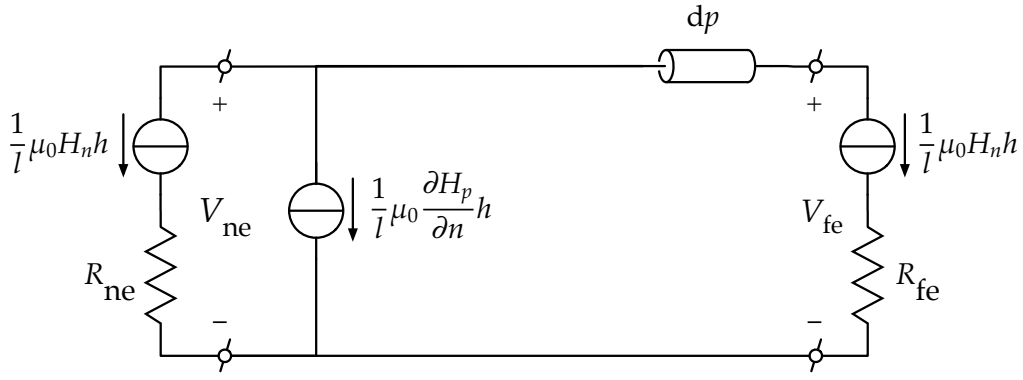
(a) Bifilar line geometry. p, n and t denote the Cartesian coordinates parallel, normal and transversal to the line. The 'ne' and 'fe' indices denote near-end and far-end, respectively.



(b) One-cell electrical model of Taylor et al.



(c) One-cell electrical model of Agrawal et al.



(d) One-cell electrical model of Rachidi.

Figure 2.2: Three equivalent weakly coupled field-to-line coupling models.

for the typical case, that is: for random incidence [22]. However, as it was derived using computer algebra tools, it does not necessarily contribute to the understanding of the coupling mechanism, nor does it simply reveal what trace geometry constitutes the worst case.

A last, extreme simplification is the quasi-static approximation. It lets waves propagate infinitely fast: $c_0 \to \infty$, which is representative for structures that are sufficiently small with respect to the wavelength. With susceptibility tests up to 18 GHz, free-space wavelength descends to 1.7 cm, while PCB traces may be tens of centimetres in length. Therefore, this approximation is too simplistic for high-frequency predictions. However, it may be useful to obtain a low-frequency limit.

To summarise, physical simulation is too costly and yields little insight on field-to-trace coupling. The transmission line approximation seems reasonable and yields insight on field-to-trace coupling (notably through the work of Leone), although not for high frequencies and/or extremely mismatched loads. The quasi-static approximation is too simplistic for practical traces, but yields insight and provides a low-frequency limit.

2.3 Meshed Taylor Model

The most obvious application of Taylor's model for a non-uniform incident field, is to mesh (slice) the line in short enough *cells*, in order for the field to become approximately uniform to each cell.

To demonstrate the Taylor model, a simple microstrip case study will first be drawn up. Then, it will be translated to a bifilar equivalent to match with the Taylor cell of Figure 2.2b. That way, it will be possible to mesh it manually under ADS, which will turn out to be time-consuming and error-prone. Therefore, it will be meshed using Kron's formalism, first on paper and then automatically. Finally, frequency-adaptive meshing will be tried out, which is novel for 1D circuit simulation.

Case study

A rather simple case study will now be defined to evaluate the various models by simulation and measurement. However, more realistic PCB traces should be kept in mind when concluding on their performance.

Microstrips, i.e. traces above a ground plane are widely used. Moreover, with respect to CPWs and striplines, they are good antennas and therefore prone to create immunity problems. Hence, a microstrip will be taken as case study.

Operational and harmonic frequencies of electronics keep rising, so the wavelengths keep falling. For example, the Wireless Home Digital Interface (WHDI) uses a 5 GHz

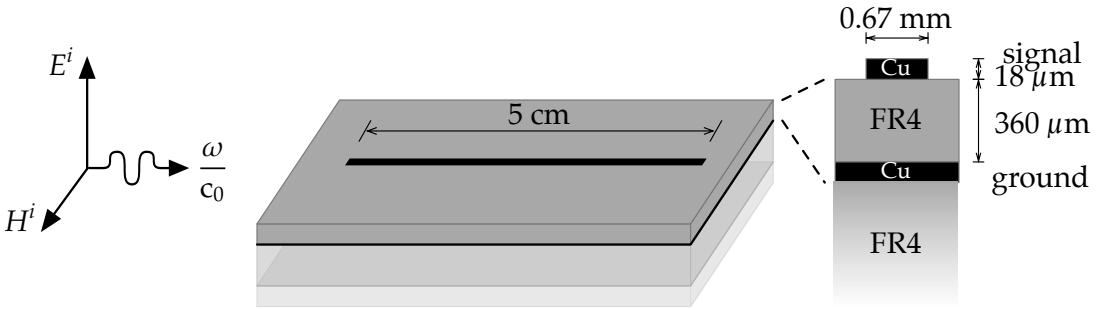


Figure 2.3: Microstrip of 5 cm length, illuminated by a grazing-incident, vertically polarised, end-fire excitation.

carrier, or a 3 cm wavelength in typical substrate. Back-up radars may use ultra-wideband signals up to 24 GHz, or down to 1.25 cm. PCBs still have sizes in that order of magnitude, so long-line effects can be expected. Therefore, a 5 cm trace, illuminated with a frequency up to 20 GHz is chosen.

In practice, traces are never characteristically terminated, because the terminating ICs and passives have frequency dependent impedances. Neither are real-world traces uniform, because of width changes and unmitered (unchamfered) bends. Existing microwave theory could be employed to incorporate these non-idealities in simulation, whereas we would like to focus on modelling of field-to-trace coupling. Therefore, a uniform trace that is characteristically terminated will be studied. To facilitate measurement, the characteristic impedance is chosen to be 50 Ω. A common substrate is chosen: FR4, which has a relative permittivity ε_r of about 4.6 . For an outer layer microstrip on a typical four-layer stack-up, the substrate is 360 μm thick [23]. Typical traces are mostly covered by solder mask, hence only consist of unplated 18 μm copper [23].

Finally, an illumination must be chosen. For low frequencies, the worst case (end-fire excitation) is grazing-incident [19]. Moreover, Gigahertz Transverse ElectroMagnetic (GTEM) cell measurements emulate a grazing-incident plane wave, by integrating a PCB in the waveguide wall. Finally, grazing-incident illumination will turn out to be easy to analyse. Therefore, a grazing incident, vertically polarised plane wave illumination is chosen. This case study is summarised in Figure 2.3. The remainder of this thesis will be restricted to grazing incidence, which is a considerable limitation.

The field strength E^i will be chosen to be representative of that generated by a standard GTEM cell, in order to allow for comparison with measurement. Because of linearity, this choice induces no loss of generality.

Bifilar Microstrip Equivalent

The essential difference between a bifilar line and a microstrip is the presence of a ground plane and a substrate.

The ground plane doubles the field strength E^i. This can be understood from the case of a Hertzian dipole, placed just above the *np*-plane, infinitely far from the origin, in an otherwise empty universe, such that the field E_t is 1 V/m at the origin. If a ground plane is now placed at the *np*-plane, there will be no field anymore under the *np*-plane and the field above it will have doubled. In the special case of a GTEM-cell, this free space field $2E^i$ equals 23.7 V/m for 1 V at the GTEM input. That way, the induced voltages can be numerically interpreted as voltage transfers. More details about the GTEM-cell's electromagnetic field and the measurement set-up will be given in section 2.6.

As for the dielectric substrate, the plane wave just above it is imposed. Since the field in the substrate must follow with a constant phase lag, the wavenumber k in the dielectric is equal to that in free space. Moreover, the material is not magnetic, hence the magnetic field H in the substrate is $2H^i$. Considering the substrate as part of an infinitely broad parallel-plate voltage divider, the electric field E in the substrate turns out to be $2E^i/\varepsilon_r$.

In summary, the bifilar-equivalent grazing-incident illumination of a microstrip causes the following plane wave in the substrate:

$$H = 2H^i \tag{2.2}$$

$$E = 2E^i/\varepsilon_r \tag{2.3}$$

$$k = \frac{\omega}{c_0}\,, \tag{2.4}$$

as illustrated in Figure 2.4.

Manual meshing

Now that the bifilar equivalent of the illuminated microstrip is known, the field-induced terminal voltages can be predicted using discrete Taylor's cell and a circuit simulator. Recall that a discrete Taylor's cell consists of a slice of passive transmission line Δp, enriched with sources representing the effect of an incident electromagnetic field (cf. Figure 2.2b).

The slice of passive transmission line Δp can be modeled with a telegrapher's cell, which lumps the distributed or per unit length (pul) resistance, conductance, inductance and capacitance into discrete elements $r\Delta p$, $g\Delta p$, $l\Delta p$ and $c\Delta p$, respectively. The copper and dielectric losses are represented by the dissipative elements $r\Delta p$ and $g\Delta p$, respectively. A line can be modeled as lossless or lossy by omitting or including these dissipative elements. For example, a lossless model of a line of length ℓ meshed in three cells is depicted in Figure 2.5.

Practically, the 50-mm case study was entered in Agilent's Advanced Design System (ADS). To that end, a mesh size should be decided upon. As the case study goes up to 20 GHz, the free-space wavelength descends to 15 mm. Supposing a velocity factor of 2/3, the wavelength in substrate thus descends to 10 mm. Without further

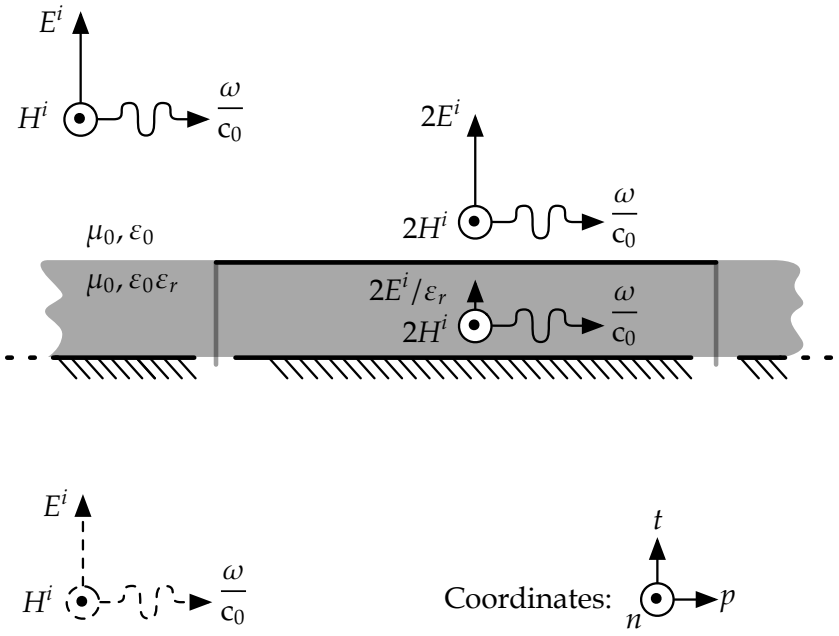


Figure 2.4: The far-away plane wave source (top left) is reflected by the microstrip's ground plane (image source at the bottom left). This results in the fields shown at the right.

understanding of a problem, the line should be meshed to a small fraction of the wavelength. To be safe, $\lambda/20$ was chosen, or 0.5 mm. To avoid placing 100 ADS cells, a `10mm_line` cell is defined, that contains 20 0.5-mm Taylor cells. The 50-mm line is then modeled by placing 5 `10mm_line` cells, as shown in Figure 2.6.

In order to simulate the passive, 50-mm microstrip, values need to be entered for c, l, g and r. To that end, ADS LineCalc was used, which is based on the models of Hammerstad and Jensen [24], Wheeler [25] and Kirschning and Jansen [26]. From the case study definition, the length $\ell = 50\,\text{mm}$, the characteristic impedance $Z_c = 50\,\Omega$, the substrate height $h = 360\,\mu\text{m}$, the copper thickness $t = 18\,\mu\text{m}$, copper conductivity $\sigma = 5.96 \times 10^{-7}\,\text{S/m}$ and the relative permittivity $\varepsilon_r = 4.6$ were entered. A typical loss tangent of $\tan\delta = 0.025$ at 1 GHz [27, Table 3.3] and a typical copper roughness for outer layer copper of $1.6\,\mu\text{m}_{\text{rms}}$ [28] were supposed. LineCalc calculated the width w of this line to be 0.67 mm and the effective permittivity $\varepsilon_{r,\text{eff}} = 3.34$ and produced an `MSUB` two-port, allowing to simulate the microstrip behaviour.

From LineCalc's effective permittivity, the pul capacitance c was calculated:

$$Z_c = \frac{1}{cv} = \frac{\sqrt{\varepsilon_{r,\text{eff}}}}{cc_0} \Longrightarrow c = \frac{\sqrt{\varepsilon_{r,\text{eff}}}}{Z_c c_0} = \frac{\sqrt{3.34}}{50 \cdot 3 \times 10^8} \approx 122\,\text{pF/m}, \tag{2.5}$$

where v is the phase speed in substrate. From this result the pul inductance l was

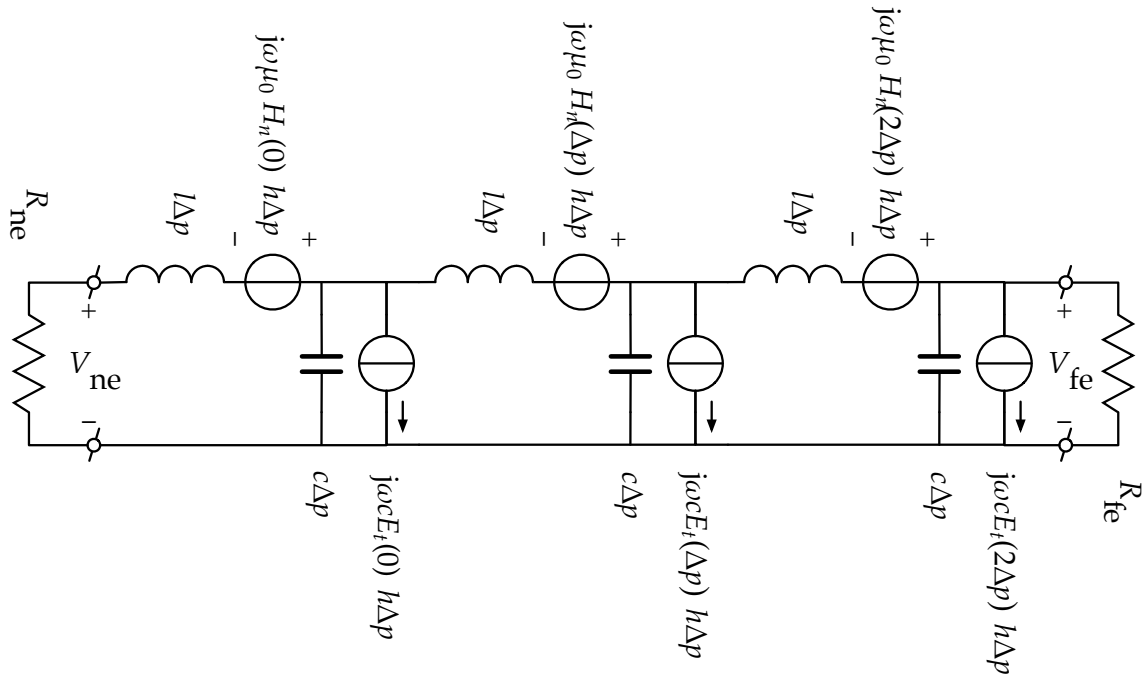


Figure 2.5: Transmission line meshed in three cells ($\Delta p = \frac{1}{3}\ell$). The passive transmission line is modeled as lossless, with l and c being the per-unit-length inductance and capacitance, respectively.

calculated:

$$Z_c = \sqrt{\frac{l}{c}} \Longrightarrow l = Z_c^2 \cdot c = 50^2 \cdot 122 \times 10^{-12} \approx 305\,\text{nH/m}. \tag{2.6}$$

According to the simplest model, the pul conductance g is linearly dependent on frequency, supposing a frequency-independent loss tangent $\tan\delta$ [27]:

$$g = \omega c \tan\delta, \tag{2.7}$$

which is plotted in Figure 2.7a. Finally, the pul resistivity r is simply the resistance of the effective cross-section A_{eff}:

$$r = \frac{1}{\sigma A_{\text{eff}}}, \tag{2.8}$$

where the effective cross-section is the apparent trace cross-section for low frequencies, but limited by the skin depth δ_s for increasing frequency [10]:

$$A_{\text{eff}} = \min\left(wt, 2\delta_s\left(w+t\right)\right) \tag{2.9}$$

$$\delta_s = \frac{1}{\sqrt{\pi f \mu_0 \sigma}}. \tag{2.10}$$

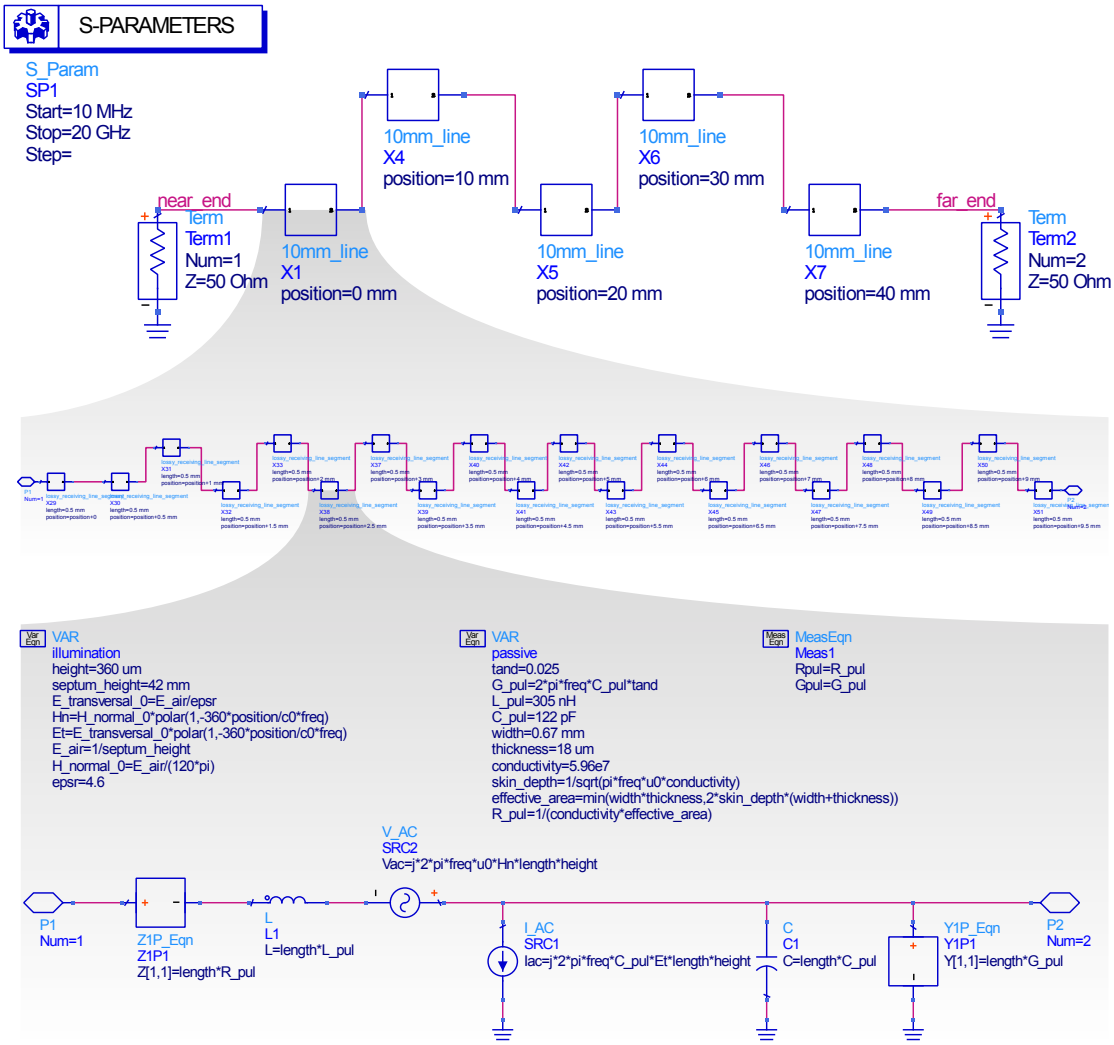


Figure 2.6: Implementation of the meshed transmission line under ADS as a chain of parametrised cells. The 50-mm line is meshed into 100 cells of 0.5 mm.

The resulting r is plotted in Figure 2.7b. Notice how these c, l, g and r pul parameters are implemented in the `passive VAR` block in the ADS cell at the bottom of Figure 2.6.

In order to gauge the accuracy of this simple *clgr* model, the S-parameter simulation of Figure 2.6 was run and compared to the S-parameters of ADS behavioural `MSUB` model. The either-end return loss $-S_{11}$ and $-S_{22}$ of the *clgr* model (not plotted) was very high for low frequencies and never descended under 20 dB up to 20 GHz, which indicates good matching. The transfer phase $\angle S_{21}$ of the *clgr* and the `MSUB` model correspond to within 2° (not plotted). The line's transfer magnitude $|S_{21}|$ according to the *clgr* and the `MSUB` correspond very well, as can be seen in Figure 2.7c.

Now that the passive *clgr* elements are checked to constitute a competent model of a passive transmission line, the active elements representing the field-to-trace coupling can be added: voltage and current sources representing magnetic and electric induction, respectively.

Contrary to the *clgr* elements, their values depend on the relative position to the plane wave origin. To that end, each cell takes a `position` parameter and calculates the local field accordingly. This is done in the ADS cell at the bottom of Figure 2.6, in the `VAR illumination` block of equations.

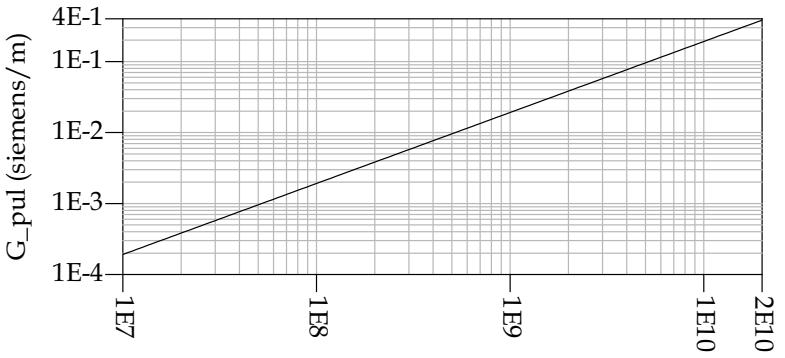
Now, an AC simulation can be run. In contrast to the S-parameter simulation, the distributed sources will be activated and thus simulate the effect of the illumination defined in the case study. The simulation was run for the far end, with and without the *rg* elements modeling the line's losses. The results are presented in Figure 2.8.

The *plateau* and null frequencies look like resonances, but this transmission line is not in resonance: both ends are characteristically terminated. Therefore, the relation between the 'resonance' frequencies and the geometrical dimensions is not simple. An attempt to explain the phenomenon will be made in section 2.4.

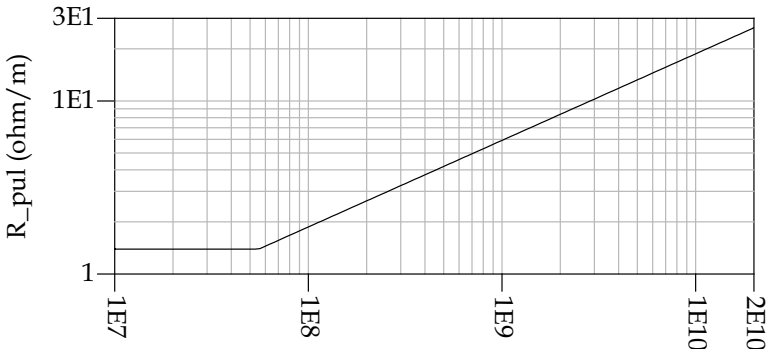
As can be seen from Figure 2.8b, the lossless model slightly overestimates the coupling when the coupling is high, as could be expected. The lossless model underestimates the coupling, however, when it's low. Because EMC problems are most likely to occur when the coupling is high, the lossless model could here safely have been used for design purposes. Therefore and unless otherwise noted, lossless models will be studied in the sequel of this thesis.

It be noted that either-end loads are matched to the trace in this case study, which never occurs in industrial practice. Intuitively, it may be expected that a lossless model also overestimates the field-to-trace coupling in a mismatched case. If that is the case, this lossless model may safely be used in an industrial case. It can also be expected that the bigger the mismatch, the larger the error induced by using a lossless model.[2] A large, pessimistic error will result in expensive over-designing. At any rate, as can be seen above, a lossless model sometimes underestimates coupling, so the lossless model

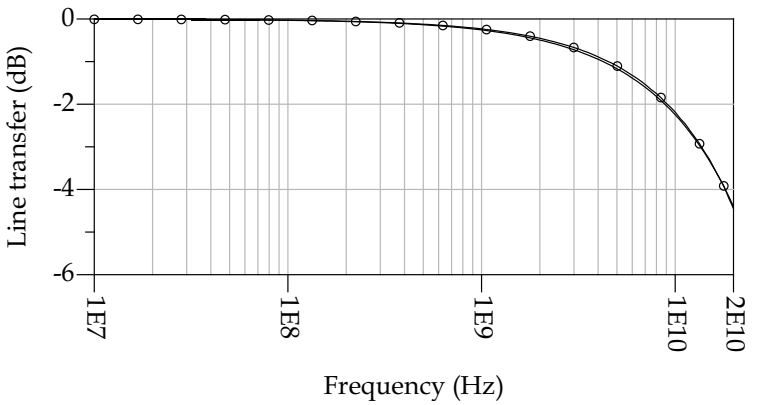
[2]Consider the case of a lossless trace either-end terminated in an open circuit. A lossless model will then predict infinite terminal voltages, although in reality they will be finite because of the trace's losses.



(a) The $\omega c \tan\delta$ dielectric conductance (notice the unitary slope).

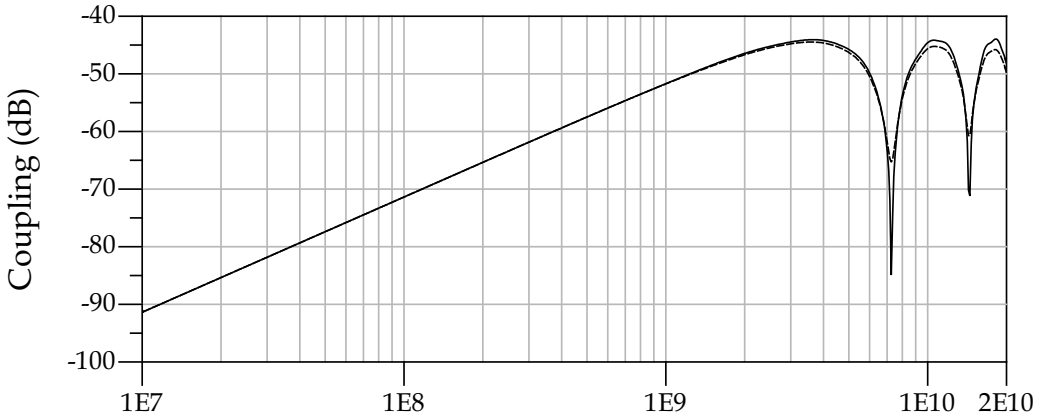


(b) The copper resistance, dominated by the $\propto \sqrt{f}$ skin loss above 55 MHz.

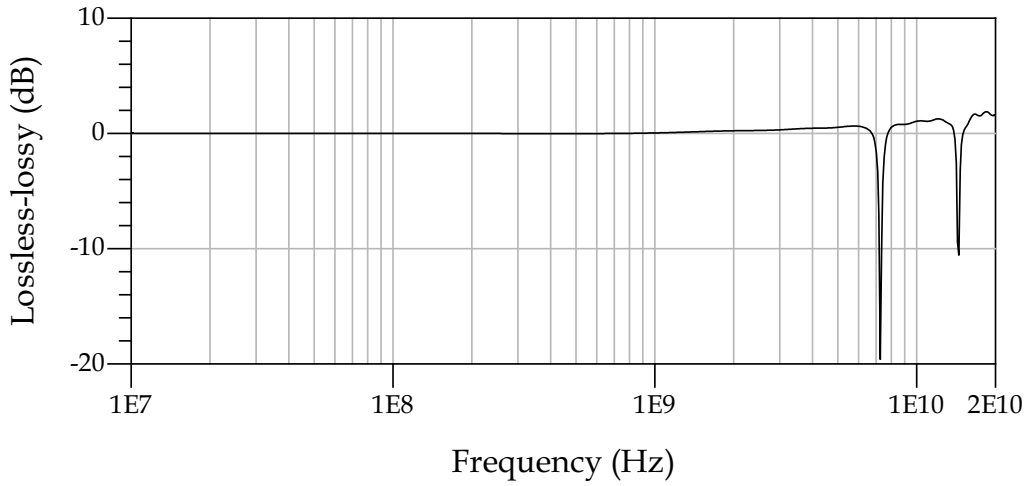


(c) Comparison of the *rg* loss model (curve with ∘ markers) with ADS' `MSUB` model (plain curve) for the 5-cm case study microstrip.

Figure 2.7: Modeling of the frequency dependent transmission line losses by *g* and *r*.



(a) Voltage transfer of GTEM input to the microstrip's far end, simulated with (dashed) and without (solid) the *rg* loss elements.



(b) Difference between the lossless and the lossy simulation.

Figure 2.8: Relevance of taking into account the losses for field-to-trace coupling.

must be used with care and intuition must be checked in general.

Using the lossless model, the near-end and far-end induced voltages of Figure 2.9 were predicted. These values will serve as a reference to compare other models to. It is interesting to note that either terminal voltage has a high-pass envelope.

However, it is a rather laborious task to manually mesh a trace. For the straight trace defined as case study, it was rather straightforward, but for a more realistically-shaped trace, it is more difficult and error-prone. Moreover, it is not easy to change the meshing resolution, which causes over-meshing and wasted time or under-meshing and the risk to miss important details in industrial practice. Therefore, manually meshing a trace

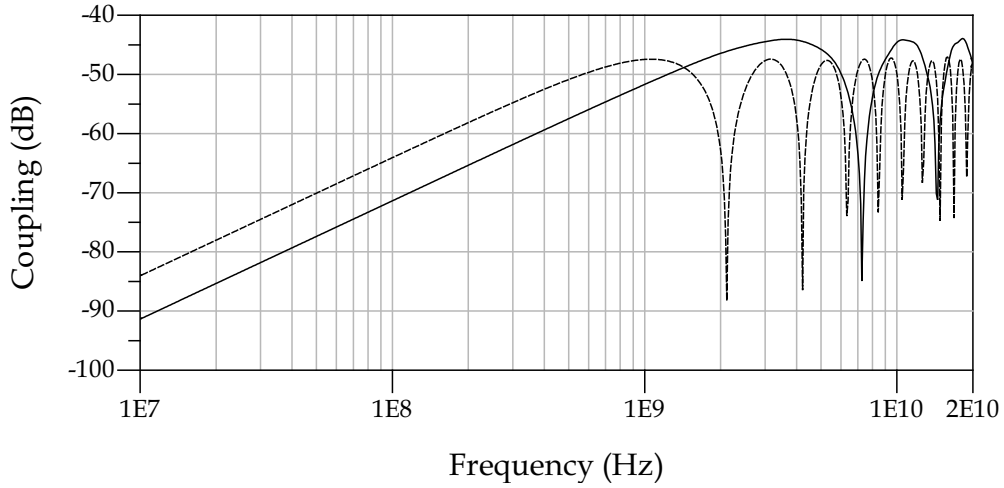


Figure 2.9: ADS simulation result for voltage transfer of the GTEM input to the near-end (dashed trace) and far-end (solid trace) of a 5-cm lossless microstrip trace.

and entering the meshes as discrete elements in a standard circuit simulator does not seem a promising direction for practical use.

Meshing under Kron's formalism

To facilitate meshing of realistically-shaped traces and to promote experimentation with the meshing resolution, the meshing will be automated. As it is not straightforward to implement this inside existing circuit simulators with a Graphical User Interface (GUI), like ADS or OrCAD, it will be done in a custom circuit simulator.

First, this problem will be analyzed in terms of Gabriel Kron's formalism [29], because of its promise to handle complex electromagnetic systems [30]. Next, the analysis will be translated into a computer programme. Finally, the result will be compared to the result from manual meshing under ADS.

Generally, solving a problem in Kron's formalism consists of eight steps: stating the problem, drawing the associated graph, defining the topological base, entering the sources, transforming, solving in mesh space, deducing the differences of potentials and deducing other required quantities [31].

The problem was already stated in Figure 2.5 and now need to be converted to a graph. In this graph, *nodes* (or junctions) and *meshes* (or loops) need to be identified. Meshes consist of at least two *branches* (or vertices) that each connect two nodes. Simplified Kirchhoff branches will now be used, which generally consist of an impedance Z and a voltage source e as defined in Figure 2.10. One possible graph is depicted in Figure 2.11.

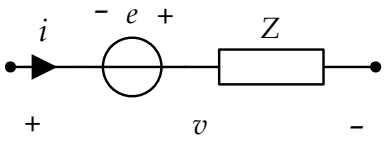


Figure 2.10: Simplified Kirchhoff branch. The difference of potential v across the branch and the current i through the branch are defined such, that when iv is positive, net power is dissipated in the branch (passive sign convention).

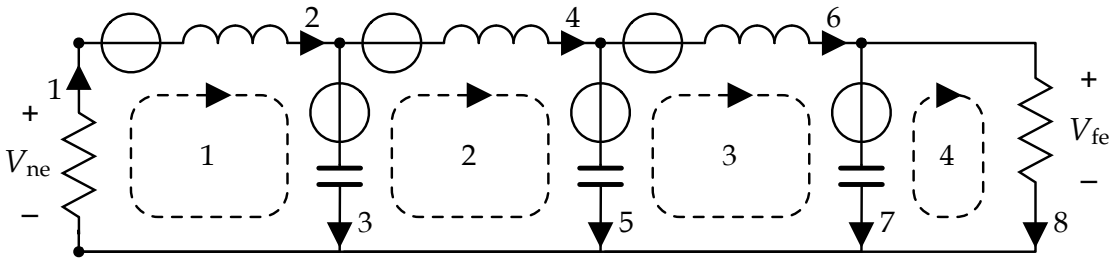


Figure 2.11: Graph representation of a three-cell transmission line model. Please verify that there are 4 meshes (dashed loops, numbered), 8 branches (with arrows, numbered) and 5 nodes (dots, not numbered).

Let i, v and e be column vectors in the *branch space*, that is: containing the currents and voltages of every branch. The (arbitrary) branch numbers of Figure 2.11 define which vector component represents which voltage and current: it is the definition of a *topological base*. Kirchoff's mesh rule and Ohm's law then hold as in $e + v = Zi$. In this case, the impedance matrix Z only has entries on its main diagonal:

$$Z = \begin{bmatrix} R_{\mathrm{ne}} & & & & & & & \\ & \mathrm{j}\omega l\Delta p & & & & & & \\ & & \frac{1}{\mathrm{j}\omega c\Delta p} & & & & & \\ & & & \mathrm{j}\omega l\Delta p & & & & \\ & & & & \frac{1}{\mathrm{j}\omega c\Delta p} & & & \\ & & & & & \mathrm{j}\omega l\Delta p & & \\ & & & & & & \frac{1}{\mathrm{j}\omega c\Delta p} & \\ & & & & & & & R_{\mathrm{fe}} \end{bmatrix} \tag{2.11}$$

To incorporate the current sources in the simplified Kirchhoff branch, their Thévenin equivalents E_th are used. The source vector e stemming from the illumination electro-

magnetic field thus becomes:

$$e = \begin{bmatrix} 0 & 0 \\ H_n(0) & 0 \\ 0 & E_t(0) \\ H_n(\Delta p) & 0 \\ 0 & E_t(\Delta p) \\ H_n(2\Delta p) & 0 \\ 0 & E_t(2\Delta p) \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \mathrm{j}\omega\mu_0\, h\Delta p \\ h \end{bmatrix}. \tag{2.12}$$

To solve for the mesh currents, the equations need to be transformed to another topological base: that of the *mesh space*. Simultaneously and inevitably, the branches are connected together. This is done by means of the *connectivity* matrix L, which links the branches (rows) with the meshes (columns). In this case,

$$L = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 1 \end{bmatrix}. \tag{2.13}$$

Note that a minus sign signifies a branch going against the mesh direction. Tensors in mesh space will be denoted with a hat, e.g.:

$$\hat{e} = L^{-1}e \qquad i = L\hat{\imath} \qquad \hat{Z} = L^{-1}ZL \qquad \hat{v} = L^{-1}v \equiv \mathbf{0},$$

where the last vector (voltage around every mesh) is zero according to Kirchhoff's mesh law. The connectivity matrix L is Hadamard-like, of which the inverse can be found by its transpose [31]. Kirchoff's mesh rule and Ohm's law can be transformed to mesh space as follows:

$$\cancel{L^{-1}v} + L^{-1}e = L^{-1}Zi = L^{-1}ZL\,\hat{\imath} \tag{2.14}$$

$$\hat{e} = \hat{Z}\,\hat{\imath}. \tag{2.15}$$

Notice that by transforming to the lower-dimensional mesh space, the branches were connected together.

To solve the system, the pseudoinverse (denoted $^+$) can be used:

$$\hat{\imath} = \hat{Z}^{+}\hat{e}, \tag{2.16}$$

because the sources e and impedances Z are given, and the mesh currents $\hat{\imath}$ are sought.

The quantities of interest are the near-end and far-end voltages, which can now be found by means of the terminal impedances:

$$V_{\text{ne}} = -\hat{\imath}_1 R_{\text{ne}} \tag{2.17}$$

$$V_{\text{fe}} = \hat{\imath}_8 R_{\text{fe}}. \tag{2.18}$$

As the frequency-domain response is sought, these expressions need to be evaluated as function of the frequency ω.

In order to automatically mesh a microstrip and solve for its terminal voltages, the above analysis need to be generalised for an arbitrary number of cells and implemented as a computer programme.

To promote reproducible computational research [32], a free-to-use programming language is preferred. Python was selected, because it is, like its predecessor ABC, a programming language for intelligent computer users, which need not be computer programmers [33]. The `numpy` and `matplotlib` packages provide sufficient means for matrix algebra and visualisation of results, respectively.

It is rather straightforward to generalize (2.11) and (2.12), and functions were written that generate these for an arbitrary number of cells. To generalise (2.13), the cases of 2 and 3 cells were manually elaborated and first formulated as a unit test [34]. Next, an implementation satisfying both unit tests was written.

To evaluate (2.16), `numpy`'s Moore-Penrose pseudoinverse was called upon, which uses Singular Value Decomposition (SVD). All code was then incorporated in the `field2line` framework, written for this thesis and allowing for easy comparison of different field-to-trace coupling models and measurements [35].

To be sure to over-mesh the structure, a meshing resolution of 50 cells per free-space-wavelength for the highest frequency of interest was chosen: 167 cells in total for the 5-cm case-study. With 661 logarithmically-spaced frequency points from 10 MHz to 20 GHz, the calculation took 54 s on an Intel 2.53 GHz Core 2 Duo processor. The far-end result is plotted and compared with the formerly obtained ADS result in Figure 2.12. The log frequency-weighted average difference between manual ADS meshing and automatic Kron meshing is -0.03 dB, the average absolute difference being 0.1 dB.

Frequency-adaptive Meshing

In order to accelerate the calculation, the Kron-based simulation was profiled. About half of the total execution time was found to be spent on the pseudoinverse of (2.16). This and other matrix manipulations depend heavily on the size of the matrix, which is drawn up for every frequency point. As the required number of cells is much lower for low frequencies, it makes sense to mesh the line for each frequency in the required number of cells. Note that the speedup will be most pronounced for a logarithmic frequency sampling. This was done with 50 cells per free-space-wavelength for each

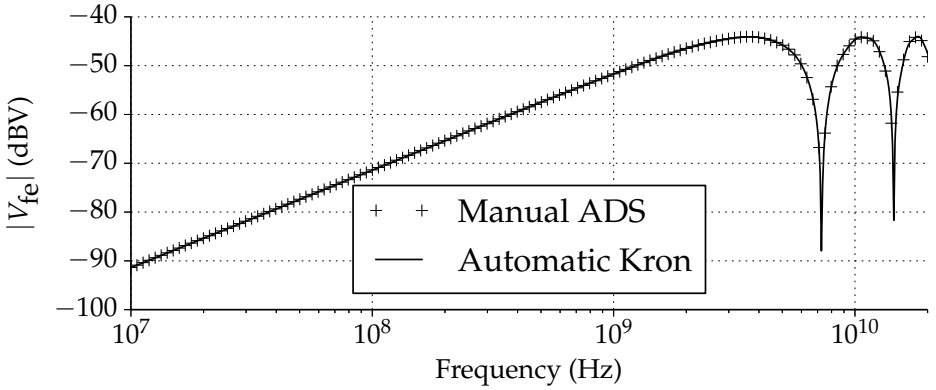


Figure 2.12: Comparison between manually meshed (ADS) and automatically meshed (Kron) simulation of the far-end induced voltage.

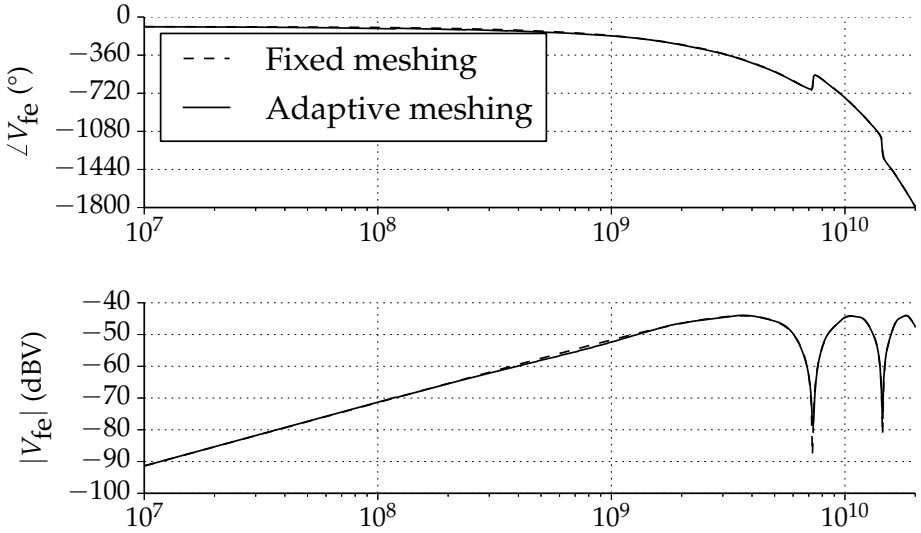
frequency, reducing the execution time to 4 s on the same platform. Fixed and frequency-adaptive meshing are compared in Figure 2.13. An average difference between fixed and adaptive meshing of −0.1 dB and an average absolute difference of 0.2 dB were obtained.

Now that the simulation runs rather quickly, the sensitivity to the meshing resolution can be easily studied. The number of cells per wavelength of the frequency adaptive simulation was swept from 1 to 50, and the error was calculated with respect to the simulation result for a fixed meshing of 50 cells per wavelength. The result is plotted in Figure 2.14. As can be seen, both error metrics become very reasonable (below ±1 dB) from 20 cells per wavelength upward, at least in this case study.

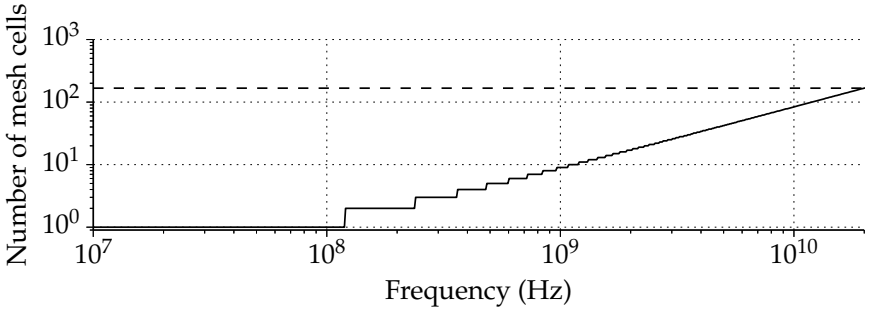
Conclusion

The simple case study of the far-end induced voltage on a 5-cm, characteristically terminated microstrip, illuminated by a vertically polarised plane wave, was studied by meshing the trace into many Taylor cells. This was first done manually, using ADS, carefully taking into account dielectric and copper losses. This led to the conclusion that the trace losses could be neglected to obtain only slightly pessimistic results. Then, the meshing was automated under Kron's formalism, yielding the same results as under ADS. The latter implementation also allowed for frequency-adaptive meshing, which achieved a speedup of an order of magnitude. In this case study, 20 cells per wavelength sufficed to obtain precise results.

Note that the automatic meshing could easily have been applied to multi-segment, arbitrarily-shaped traces with arbitrary loads. In spite of that and for simplicity, it was not done.



(a) Simulation result in amplitude and phase.



(b) Number of cells used for the simulation.

Figure 2.13: Comparison of fixed and frequency-adaptive automatic meshing in Kron-based simulation.

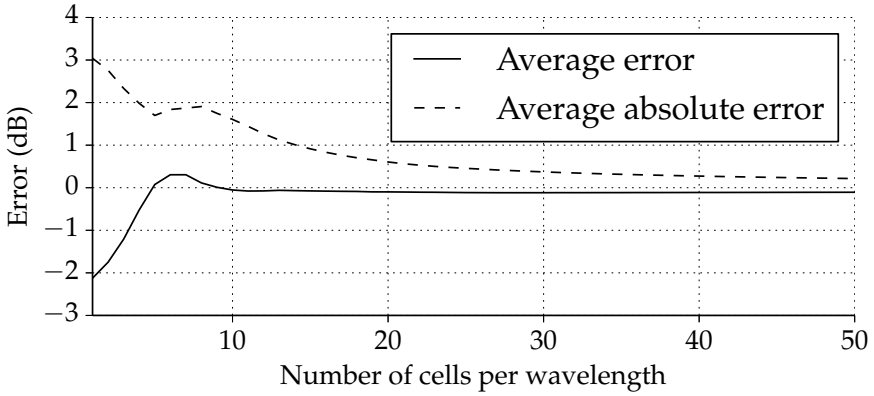


Figure 2.14: Sensitivity of adaptively-meshed simulation to the meshing resolution. A non-adaptively-meshed simulation with 50 cells per wavelength served as reference to calculate the error metrics.

2.4 Modified Taylor Model

As shown in the previous section, the coupling of an incident wave to a PCB trace can be predicted by meshing the trace in electrically short Taylor cells, and solving the resulting circuit. Although the solution is found relatively quickly (4 s for a 5-cm microstrip), it does not yield insight. Indeed, the underlying model is completely opaque: imagine the system of equations of a two-cell mesh. Little understanding is obtained, and important engineering questions remain unanswered, like "What design parameters have significant impact on the field-to-trace coupling?" or "What is the worst-case illumination (to test devices)?"

To answer these important questions, a transparent model will be constructed bottom-up. In each step, the model will be generalised, while keeping transparency by determining the worst case. The starting point is a single Taylor cell, valid for grazing-incident, vertically polarised plane wave incident on a single electrically short trace segment with matched loads. Then, the model will be generalised to an electrically long trace segment. Next, the model will be extended to multiple segments. Finally, the model will be generalised to comprise arbitrary loads. To conclude, this modified Taylor cell will be compared to above meshed Taylor simulations in terms of speed and insight.

Short Trace

The starting point for the generalisation is one electrically short microstrip segment, illuminated by a vertically polarised, grazing-incident plane wave.

Electrically short means very small with respect to the exciting wavelength. Conversely, the exciting wavelength is very large with respect to the trace length, so the phase shift of the incident field along the line tends to zero and the field can be con-

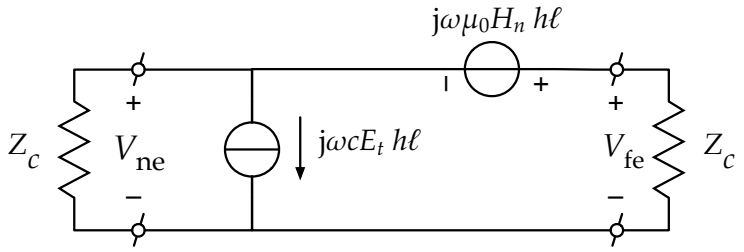


Figure 2.15: An electrically short bifilar transmission line with characteristic loads modeled as a single Taylor cell.

sidered spatially uniform. Consequently, the line can be lumped as a single Taylor cell $\Delta p = \ell$. Because the line is electrically short, the phase lag $\beta\ell$ is negligible so the passive line segment ℓ can be neglected. The resulting model of a short line with characteristic loads ($R_{\text{ne}} = R_{\text{fe}} = Z_c$) is shown in Figure 2.15. The low-frequency either-end terminal voltages can be found by inspection [10]:

$$V_{\text{LF}} = -\frac{1}{2}\text{j}\omega\, cE_t Z_c\, h\ell \mp \frac{1}{2}\text{j}\omega\, \mu_0 H_n\, h\ell, \tag{2.19}$$

where c is the pul capacitance of the line. Unless otherwise noted, the near-end and far-end results are presented simultaneously throughout this thesis; $\mp$ means minus for the near end and plus for the far end.

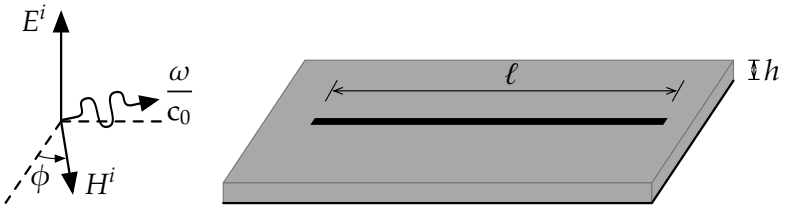
To evaluate this expression for grazing incidence, the substrate fields E_t and H_n first need to be determined. Let the incidence azimuth ϕ be defined as in Figure 2.16a. Similarly to the end-fire case developed on p. 19, the incident field doubles in the substrate, the electric field is diminished by the permittivity and the phase speed remains unchanged, as shown in Figure 2.16b.

Using the constitutive relations

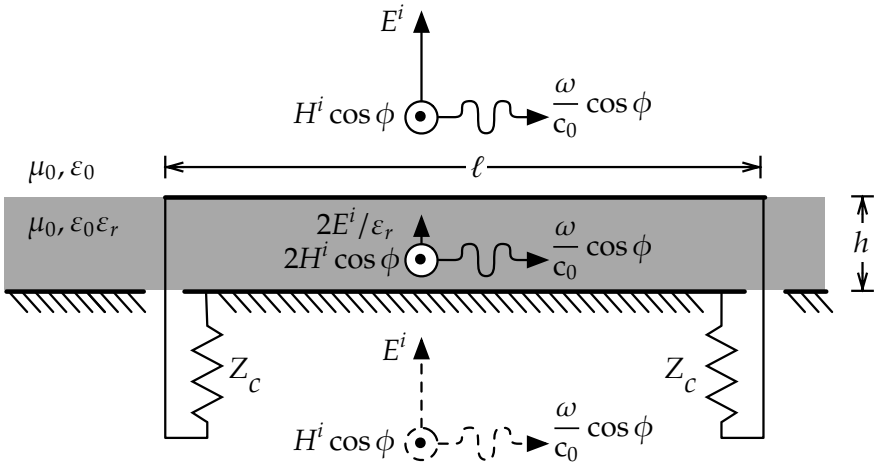
$$Z_c = \frac{1}{cv_{\text{line}}} = \frac{\sqrt{\varepsilon_{r,\text{eff}}}}{c\ \text{c}_0}; \quad E^i = H^i\sqrt{\frac{\mu_0}{\varepsilon_0}}; \quad \text{c}_0 = \frac{1}{\sqrt{\mu_0\varepsilon_0}},$$

the low-frequency terminal voltage under grazing incidence can now be expressed in terms of E^i and ϕ:

$$\begin{aligned} V_{\text{LF}} &= \frac{1}{2}\text{j}\omega\left(-Z_c c\frac{2E^i}{\varepsilon_r} \mp \mu_0 2H^i\cos(\phi)\right)h\ell \\ &= \text{j}\omega E^i\left(-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\text{c}_0\varepsilon_r} \mp \sqrt{\mu_0\varepsilon_0}\cos(\phi)\right)h\ell \\ &= \text{j}k^i E^i\left(-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r} \mp \cos(\phi)\right)h\ell, \end{aligned} \tag{2.20}$$



(a) Perspective on the grazing incident wave: the incident electric field is perpendicular to the substrate and the wave vector makes an angle ϕ with the transmission line axis.



(b) Cross section of the transmission line. The incident and reflected plane wave sources produce the shown substrate field.

Figure 2.16: Approximation of the substrate field strength for grazing incidence.

where the effective permittivity $\varepsilon_{r,\text{eff}}$ is the field-weighted average permittivity that the microstrip mode encounters: consequently, it is somewhere between the ε_r of the substrate and unity of the air.

By inspecting (2.20), the influence of the different design parameters can be gauged. The induced voltage is linearly dependent of the loop surface $h\ell$, of which the trace length ℓ is easy to change in a late design stage, whereas the substrate thickness h is harder to change. The substrate's permittivity ε_r is only of little influence, as it occurs both in denominator and (indirectly) in the enumerator.

The worst case illumination can also be found by inspection: the highest near-end (far-end) induced voltage magnitude occurs for $\phi = 0$ ($\phi = \pi$), that is, at the end where the incident wave is coming *from*. Note that this result is consistent with [19].

Long Trace

The next generalisation towards real-life traces is to include electrically *long* traces.

First, a thought experiment will be performed to intuitively understand the long line effect. Alternatively, analytic reasoning will be used to quantify this long line effect, which will result in a single modified Taylor cell, which is also valid for high frequencies. This will be numerically checked against the meshed simulation results obtained above. Finally, the single modified Taylor cell will be used to obtain a transparent worst case.

Consider the illumination of Figure 2.16a; now that the trace is generally long with respect to the wavelength, the field becomes of a function of the position p along the line:

$$E^i(p) = E^i(0) \cdot i(p), \tag{2.21}$$

where i denotes the *normalised amplitude* of the illuminating field, which is just a phase lag:

$$i(p) = \mathrm{e}^{-\mathrm{j}k_p p}; \quad k_p = \frac{\omega}{\mathrm{c}_0} \cos\phi. \tag{2.22}$$

The near-end (far-end) induced voltage can be thought of as the effect of a traveling wave on the line: the backward (forward) *eigenwave* [36]. Its normalised amplitude w is also a phase lag:

$$w(p) = \mathrm{e}^{\pm\mathrm{j}\beta p}; \quad \beta = \frac{\omega}{v}\,, \tag{2.23}$$

where v is the phase speed of a wave on the transmission line.

Now imagine the illumination and the forward eigenwave at such a low frequency, that a single Taylor cell is a competent model because the error it introduces is negligible. Along Figure 2.17(a-d), we will imagine what happens for rising frequency and consequently, what the error introduced by a single Taylor cell would be.

Figure 2.17a shows the case for low frequencies, where the incident field remains uniform along the line and the guided wave propagates quasi-instantly on the line, so modeling the line as one Taylor cell is legitimate.

As shown in Figure 2.17b, with increasing frequency, the wavelength decreases. When the wavelength gets in the order of the line length, a propagating wave appears, both in free space and in the transmission line. Yet, this does not immediately invalidate the model. Indeed, the field is no longer uniform along the line, but the forward eigenwave of the line and the free space plane wave travel in the same direction. That means that, for every line slice, the free space wave and the eigenwave still have approximately the same phase. Therefore, it is still legitimate to model the line as one cell.

As frequency increases further, like in Figure 2.17c, the phase difference between the forward eigenwave and the incident plane wave becomes significant; in the example shown, the phase *difference* goes from 0 at $p = 0$ to π at $p = \ell$. On average, both waves are still cross-correlated, but less so than for low frequencies.

In the extreme case of Figure 2.17d, the phase difference goes all the way from 0 at $p = 0$ to 2π at $p = \ell$. On average, the two waves are no longer cross-correlated and

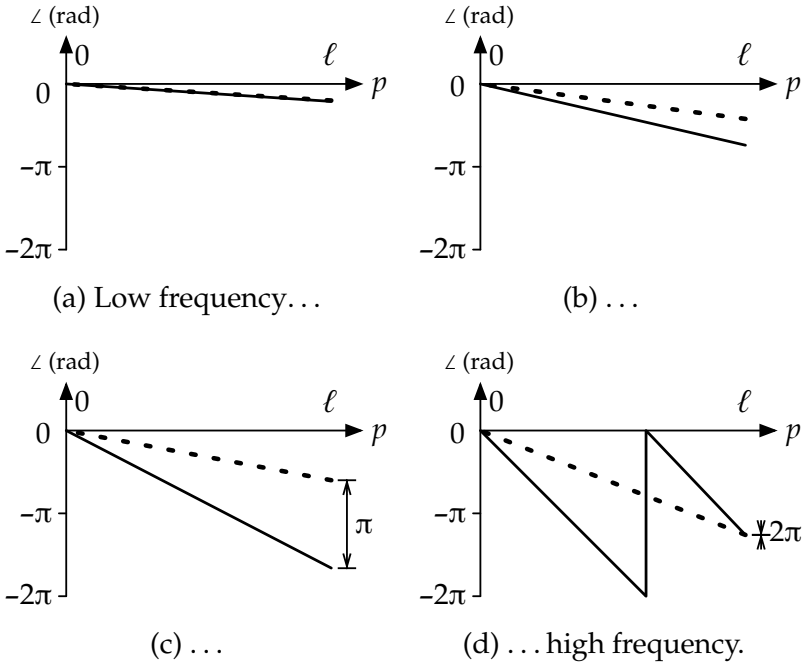


Figure 2.17: Phase along the transmission line of the line's eigenwave $\angle w$ (solid line) and illuminating plane wave $\angle i$ (dashed line), for increasing frequency.

coupling is not expected any longer. For even higher frequencies (not depicted), there will be some net correlation again, but never as much as for low frequencies.

To summarize, a single Taylor cell correctly predicts coupling for low frequencies. However, it overestimates the coupling at increasing frequencies, because the decreasing length-average similitude of the illuminating- and the eigenwave. Put differently, the high-frequency solution should equal the low-frequency solution of (2.20), corrected by some unitless measure K of similitude. This K should be unity for low frequencies, in order not to modify the low frequency coupling. K should amount to zero when the phase difference along the line goes all the way from 0 to 2π.

Armed with this intuitive expectation, an analytical approach can be safely taken. Now that the field is not generally uniform anymore, the integral over infinitely many cells dp along the line's length must be taken. Now that the propagation delay on the line is not negligible anymore, the passive lossless transmission line must be taken into account as well. This integral corresponds to a sliding cell dp with transmission lines at its left and its right with lengths p and $\ell - p$ respectively, as shown in Figure 2.18.

Both sources of the infinitesimal cell directly see a characteristic load, so (2.20) gives the backward- and forward traveling voltages. The near-end voltage contribution of

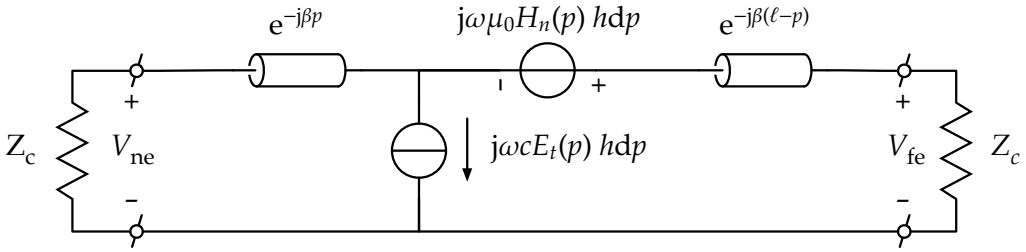


Figure 2.18: Modelling an electrically long, lossless bifilar transmission line with characteristic loads as the continuous integral of infinitesimal cells of length dp.

the infinitesimal cell is then delayed by the left half p of the lossless transmission line:

$$\begin{aligned} \mathrm{d}V_{\mathrm{ne}} &= \left(-\frac{1}{2}Z_c\, \mathrm{j}\omega c E_t(p)\, h\mathrm{d}p \; - \frac{1}{2}\, \mathrm{j}\omega\mu_0 H_n(p)\, h\mathrm{d}p\right)\mathrm{e}^{-\mathrm{j}\beta p} \\ &= \mathrm{j}k^i E^i(0)\left(-\frac{\sqrt{\varepsilon_{r,\mathrm{eff}}}}{\varepsilon_r} - \cos(\phi)\right)\mathrm{e}^{-\mathrm{j}k_p p}\mathrm{e}^{-\mathrm{j}\beta p}\, h\mathrm{d}p \end{aligned} \tag{2.24}$$

$$V_{\mathrm{ne}} = \mathrm{j}k^i E^i(0)\left(-\frac{\sqrt{\varepsilon_{r,\mathrm{eff}}}}{\varepsilon_r} - \cos(\phi)\right) h \int_0^\ell \mathrm{e}^{-\mathrm{j}k_p p}\mathrm{e}^{-\mathrm{j}\beta p}\, \mathrm{d}p. \tag{2.25}$$

Similarly, the far-end voltage contribution is delayed by the right half $(\ell - p)$ of the transmission line:

$$V_{\mathrm{fe}} = \mathrm{j}k^i E^i(0)\left(-\frac{\sqrt{\varepsilon_{r,\mathrm{eff}}}}{\varepsilon_r} + \cos(\phi)\right) h \int_0^\ell \mathrm{e}^{-\mathrm{j}k_p p}\mathrm{e}^{+\mathrm{j}\beta p}\, \mathrm{d}p\, \mathrm{e}^{-\mathrm{j}\beta\ell}. \tag{2.26}$$

Let us now try to interpret the result as an equivalent circuit in order to develop intuition. By slightly rewriting (2.25) and (2.26), we can recognise the low-frequency induced voltage of (2.20), multiplied by a factor K:

$$V_{\mathrm{ne}} = \underbrace{\mathrm{j}k^i E^i(0)\left(-\frac{\sqrt{\varepsilon_{r,\mathrm{eff}}}}{\varepsilon_r} - \cos(\phi)\right) h\ell}_{V_{\mathrm{LF,ne}}}\; \underbrace{\frac{1}{\ell}\int_0^\ell \mathrm{e}^{-\mathrm{j}k_p p}\mathrm{e}^{-\mathrm{j}\beta p}\, \mathrm{d}p}_{K_{\mathrm{ne}}} \tag{2.27}$$

$$V_{\mathrm{fe}} = \underbrace{\mathrm{j}k^i E^i(0)\left(-\frac{\sqrt{\varepsilon_{r,\mathrm{eff}}}}{\varepsilon_r} + \cos(\phi)\right) h\ell}_{V_{\mathrm{LF,fe}}}\; \underbrace{\frac{1}{\ell}\int_0^\ell \mathrm{e}^{-\mathrm{j}k_p p}\mathrm{e}^{+\mathrm{j}\beta p}\, \mathrm{d}p}_{K_{\mathrm{fe}}}\; \underbrace{\mathrm{e}^{-\mathrm{j}\beta\ell}}_{\text{delay}}, \tag{2.28}$$

where K is the length-averaged cross-correlation between the illumination- and eigenwave amplitudes:

$$K = \frac{1}{\ell}\int_0^\ell i(p)\cdot w^*(p)\, \mathrm{d}p = \frac{1}{\ell}\int_0^\ell \mathrm{e}^{-\mathrm{j}k_p p}\mathrm{e}^{\mp\mathrm{j}\beta p}\, \mathrm{d}p = \frac{1}{\mathrm{j}(-k_p \mp \beta)\ell}\left(\mathrm{e}^{\mathrm{j}(-k_p \mp \beta)\ell} - 1\right), \tag{2.29}$$

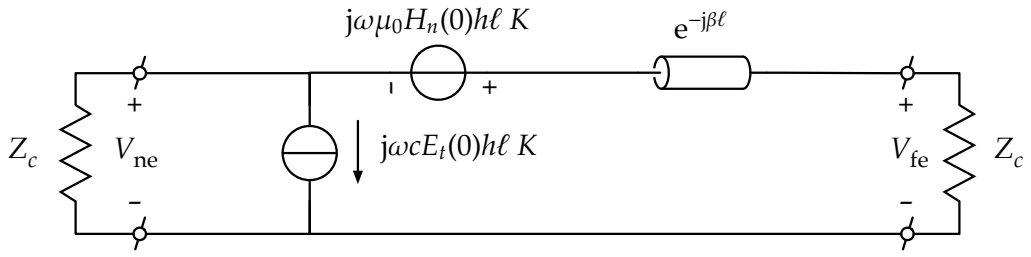


Figure 2.19: The modified Taylor cell; the correction factor K takes into account the long line effect.

which indeed is a measure for similitude. This result is visualised in Figure 2.19: a single Taylor-like cell, also valid for high frequencies. One passive transmission line of length ℓ accounts for the delay of (2.28). Note that for calculating the near-end or the far-end induced voltage, K_{ne} or K_{fe} need to be used, respectively.

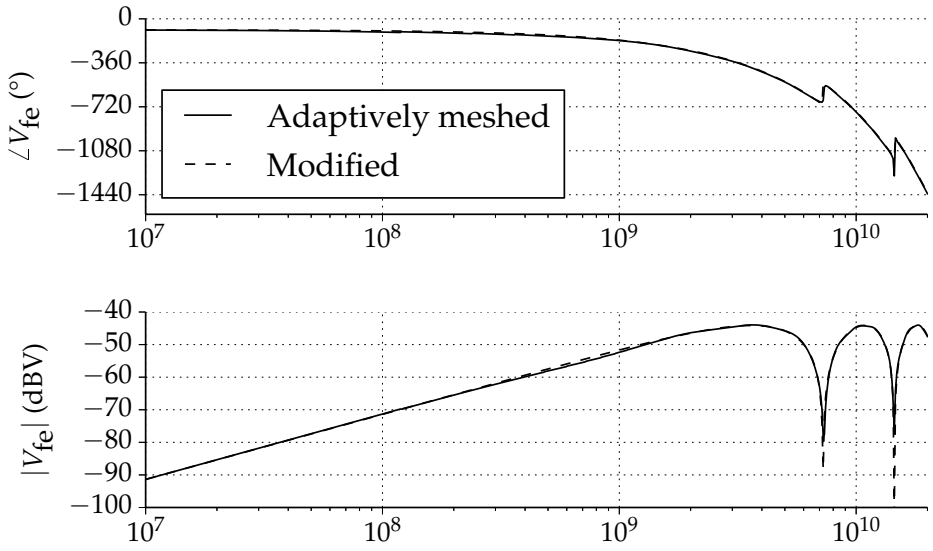
To better understand the meaning of K, consider the non-physical case where the excitation wave travels with the same phase speed along the line as a wave on the line: $k_p \equiv \beta$. With Figure 2.17 in mind, it can be intuitively understood that both waves are similar for any frequency or wavelength. Analytically, this can be shown by calculating the far-end correlation K_{fe} for a wave number difference $-k_p + \beta$ tending to zero and a finite line length ℓ:

$$\begin{aligned} K_{\text{fe}} &= \lim_{-k_p+\beta\to 0} \frac{1}{\mathrm{j}(-k_p+\beta)\ell}\left(\mathrm{e}^{\mathrm{j}(-k_p+\beta)\ell} - 1\right) \\ &= \lim_{-k_p+\beta\to 0} \frac{\cancel{\cos\left((-k_p+\beta)\ell\right)} + \mathrm{j}\sin\left((-k_p+\beta)\ell\right) - \cancel{1}}{\mathrm{j}(-k_p+\beta)\ell} = 1. \end{aligned} \tag{2.30}$$

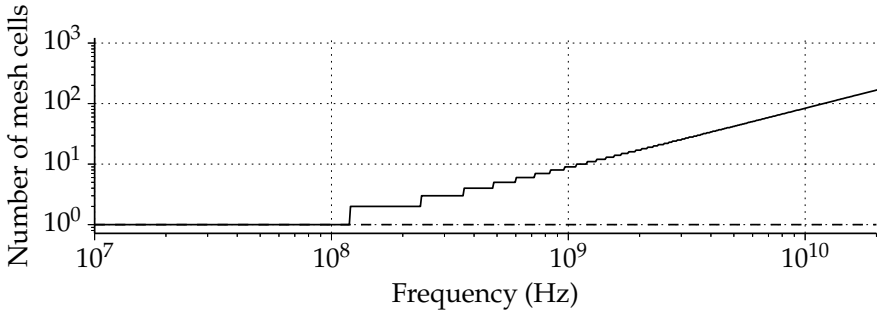
Apparently, the non-uniformity of the excitation field does not suffice to invalidate a single-cell Taylor model. It is rather the discrepancy between β and k_p that makes K deviate from unity.

To gauge the correctness of (2.28) and the numerical speed-up of having only a single (modified) cell, the modified Taylor cell was implemented in the `field2line` framework mentioned before. This allowed for easy comparison between the simulation results of different models.

For example, the modified Taylor cell has an average error of -0.1 dB and a 0.2 dB average absolute error with respect to the first, manual ADS simulation (not shown). For another example, the modified Taylor cell was compared to the adaptively meshed Taylor cell in Figure 2.20. Phase comparisons proved a useful tool in debugging the implementation. As can be seen, the modified and the meshed Taylor cell correlate rather well; $+0.1$ dB average error, 0.3 dB average absolute error.



(a) Simulation result in amplitude and phase.



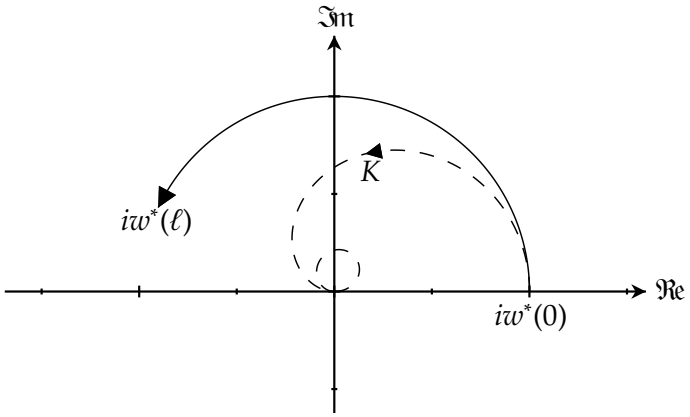
(b) Number of cells used for the simulation.

Figure 2.20: Comparison of modified Taylor with frequency-adaptive meshing (cf. Figure 2.13).

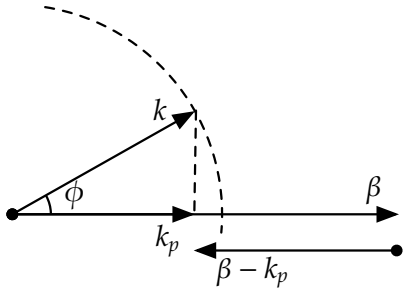
The simulation with the single modified Taylor cell took 0.4 s, which is about another order of magnitude speedup with respect to the adaptively meshed Taylor cell.

Does the worst-case conclusion for an electrically short line also hold for an electrically long line? Looking at (2.28), it can be seen that the line delay only introduces a phase shift, so it can be ignored when reasoning about voltage magnitude. Both near-end and far-end voltage magnitudes are the product of the low-frequency terminal voltage V_{LF} and the correction factor K. If the worst-case $|K|$ coincides with the worst-case $|V_{\text{LF}}|$, the worst-case product is the product of worst cases. Let us explore this hypothesis by finding the worst-case $|K|$.

Let us interpret K geometrically on the complex plane. Recall that the integrand $i\omega^*(p)$ yields the similarity of the excitation plane wave and the line's eigenwave at any



(a) On the complex plane: K is the centre of gravity of the arc $iw^*(p)$. The trajectory of K is dashed for $0 \leq iw^*(\ell) \leq 4\pi$.



(b) In Carthesian space: wave vector alignment with the transmission line.

Figure 2.21: Geometric interpretations of K's constituents.

position p on the transmission line. At the beginning of the line, both waves have the same phase. As i and w are normalised amplitudes, the integrand amounts to one. Due to the different propagation speeds of the excitation wave and the line's eigenwave, the phase difference grows along the line. The arc described by the integrand in the case of a forward propagating wave is shown in Figure 2.21.

The integral divided by its length yields the arc's centre of gravity K. By inspecting Figure 2.21a, it can be seen that $|K| \leq 1$. Moreover, the greater the phase difference at the end of the line, the longer the arc, the smaller $|K|$. Conversely, the smaller the phase difference at the end of the line, the greater $|K|$. The phase difference at the end of the line is $(\beta - k_p)\ell$. Hence, for a given ℓ, the worst case occurs when k_p and β are closest.

To see when β and k_p are closest, picture the line's wavenumber β as a vector pointing in the line direction. The excitation wave vector parallel to the line k_p then is the

projection of k on the first vector. Moreover, as the excitation wave always propagates faster than a wave on the line, k is always shorter than β, as is the case in Figure 2.21b. By inspection, it can be concluded that $\beta - k_p$ is minimal when the excitation wave vector k is parallel with the line. Therefore, $|K_{\text{fe}}|$ is maximum when exciting from the near-end side, parallel to the line: end-fire excitation. Analogously, $|K_{\text{ne}}|$ is maximum when exiting from the far-end side, parallel to the line. Put differently, $|K|$ is maximum at the end where the incident wave is going *to*.

So, both for $|K|$ and $|V_{\text{LF}}|$, the worst case occurs for end-fire excitation, but not from the same end, unfortunately. Indeed, Leone's case study suggests that the worst-case end be frequency dependent [19]. All the same, the upper bound mentioned before can be evaluated:

$$\max|V| \leq \max|V_{\text{LF}}| \cdot \max|K| = \max|V_{\text{LF}}|, \tag{2.31}$$

which is true but not very useful, because $|V_{\text{LF}}|$ increases without bound as function of frequency.

Therefore, the product $V_{\text{LF}}K$ will be first evaluated for a given E^i, h, ℓ, ε_r and $\varepsilon_{r,\text{eff}}$, and then the worst-case ϕ will be sought.

$$K = \frac{1}{\mathrm{j}(-k^i\cos(\phi) \mp \beta)\ell}\left(\mathrm{e}^{\mathrm{j}(-k^i\cos(\phi)\mp\beta)\ell} - 1\right), \tag{2.32}$$

$$|V| = |V_{\text{LF}}||K| = E^i h \left|\frac{-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r} \mp \cos(\phi)}{-\cos(\phi) \mp \sqrt{\varepsilon_{r,\text{eff}}}}\right| \left|\mathrm{e}^{\mathrm{j}\omega\left(-\cos(\phi)\mp\sqrt{\varepsilon_{r,\text{eff}}}\right)\frac{\ell}{c_0}} - 1\right|. \tag{2.33}$$

The rightmost term determines the worst case frequency, then amounting to 2. The rest is frequency- and length- (!) independent.

Knowing that $\sqrt{\varepsilon_{r,\text{eff}}} > 1$ and for given E^i, h, ε_r and $\varepsilon_{r,\text{eff}}$,

$$\max_{\omega\ell}|V| = 2E^i h \frac{\left|-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r} \mp \cos(\phi)\right|}{\sqrt{\varepsilon_{r,\text{eff}}} \pm \cos(\phi)}. \tag{2.34}$$

In order to find the maximum with respect to ϕ, we would like to differentiate and equate to zero to find the critical points. However, for ϕ where the enumerator sign flips over, the fraction is not differentiable. Fortunately, these ϕ constitute the minima, whereas we search the maxima. We may ignore the absolute operator because critical points stay critical under the absolute operator:

$$\frac{\partial}{\partial\phi}\max_{\omega\ell}|V| = 2E^i h \frac{\mp\sqrt{\varepsilon_{r,\text{eff}}}\left(1 - \frac{1}{\varepsilon_r}\right)\sin(\phi)}{\left(\sqrt{\varepsilon_{r,\text{eff}}} \pm \cos(\phi)\right)^2}. \tag{2.35}$$

The denominator is never zero, so the derivative only equals zero for $\phi = 0, \pi$: we only need to consider end-fire illumination.

Let us compare $\phi = 0$ (left hand side) and $\phi = \pi$ (right hand side) for the near-end case of (2.34) (recall that $\sqrt{\varepsilon_{r,\text{eff}}} < \varepsilon_{r,\text{eff}} < \varepsilon_r$):

$$\cancel{2E^i h}\frac{1+\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}}{\sqrt{\varepsilon_{r,\text{eff}}}+1} \lessgtr \cancel{2E^i h}\frac{1-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}}{\sqrt{\varepsilon_{r,\text{eff}}}-1} \tag{2.36}$$

$$\left(1+\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}\right)\left(\sqrt{\varepsilon_{r,\text{eff}}}-1\right) \lessgtr \left(1-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}\right)\left(\sqrt{\varepsilon_{r,\text{eff}}}+1\right) \tag{2.37}$$

$$\cancel{\sqrt{\varepsilon_{r,\text{eff}}}}+\frac{\varepsilon_{r,\text{eff}}}{\varepsilon_r}-1-\cancel{\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}} \lessgtr \cancel{\sqrt{\varepsilon_{r,\text{eff}}}}+1-\frac{\varepsilon_{r,\text{eff}}}{\varepsilon_r}-\cancel{\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}}, \tag{2.38}$$

so, $\phi = \pi$ constitutes the worst case for the near-end. Conversely, $\phi = 0$ constitutes the worst case for the far-end.

By plugging these worst-case ϕ into (2.34), we conclude:

$$\max_{\omega\ell,\phi}|V| = 2E^i h\frac{1-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}}{\sqrt{\varepsilon_{r,\text{eff}}}-1}, \tag{2.39}$$

which is the high-frequency, worst-case, either-end induced voltage in a characteristically terminated microstrip illuminated under grazing incidence.

Now that the high-frequency worst case of (2.39) and the low-frequency worst case of (2.20) are found, they can be joined to obtain a broadband worst case:

$$\max|V| = E^i h \cdot \min\left\{\underbrace{\frac{\omega}{c_0}\ell\left(1+\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}\right)}_{\text{low-frequency}}, \underbrace{2\frac{1-\frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}}{\sqrt{\varepsilon_{r,\text{eff}}}-1}}_{\text{high-frequency}}\right\}, \tag{2.40}$$

(magnetic, electric)

that is, the envelope formed by the low-frequency near-end voltage for $\phi = 0$ and the high-frequency voltage for $\phi = \pi$, as illustrated in Figure 2.22 and Figure 2.23.

This broadband worst case envelope can be physically interpreted as follows: for low frequencies, the worst case occurs when the magnetic and the electric contributions add up constructively. The wavelength is great with respect to the line length, so the line does not feel the difference between a forward or a backward travelling wave: $K_{\text{fe}} = K_{\text{ne}} = 1$. For high frequencies, the worst case occurs when the illuminating wave is aligned with the wave propagating towards the terminal. The magnetic and electric contributions cancel somewhat, but the alignment ($K \to 1$) has a bigger effect.

Multiple Segments

To study multi-segment traces a simple case study was drawn up. To facilitate for analytical and numerical debugging, a small number of segments was chosen: three.

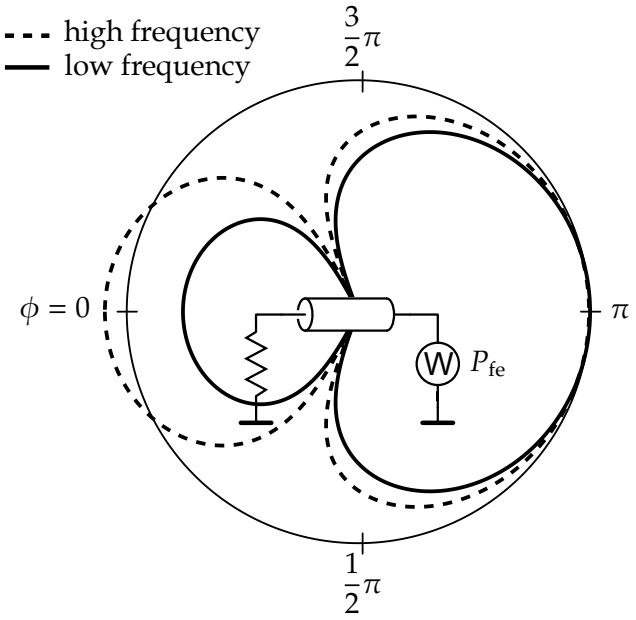


Figure 2.22: Qualitative antenna pattern of the far end. The radial axis has no particular unit: the low-frequency gain of (2.20) is linear in ω, the high-frequency gain of (2.34) is normalised to coincide with the low-frequency gain at $\phi = \pi$. Notice the broadband null at $\cos(\phi) = \mp\frac{\sqrt{\varepsilon_{r,\mathrm{eff}}}}{\varepsilon_r}$.

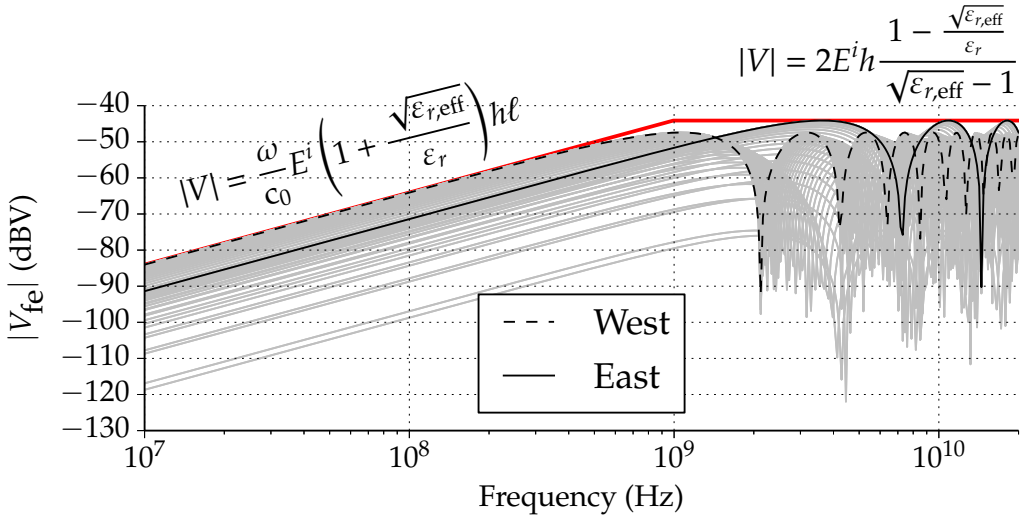


Figure 2.23: Coupling to one end of a rotated trace: the eastern orientation ($\phi = 0$, actual far-end coupling) and western orientation ($\phi = \pi$, rather near-end coupling) are highlighted. The orientation of the trace was swept from 0 to 2π in 100 steps. The broadband envelope of (2.40) is plotted in red.

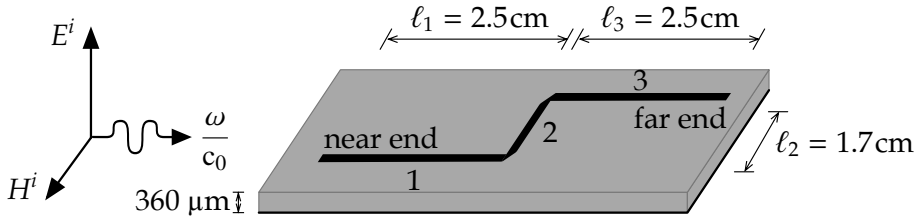


Figure 2.24: Case study on three-segment trace with mitred bends.

The lengths were chosen to have the trace significantly differ from one straight segment, as can be seen in Figure 2.24. Similarly to the above analyses, the terminal voltages under end-fire illumination will be sought.

To simplify the analysis, the transitions between the segments will be considered negligible. That way, the entire trace will behave like a uniform transmission line, like it did in the analysis of a single microstrip segment. In practice, this will require optimally mitred bends, because straight corners introduce excess capacitance [37].

The coupling to multiple straight line segments can be found by superposition, because the segments are matched. In the three-segment case study, the contributions of the straight line segments ℓ_1, ℓ_2 and ℓ_3 must be summed:

$$V_{\text{ne}} = \left(K^1_{\text{ne}} V^1_{\text{LF,ne}} + K^2_{\text{ne}} V^2_{\text{LF,ne}} + K^3_{\text{ne}} V^3_{\text{LF,ne}}\right) \tag{2.41}$$

$$V_{\text{fe}} = \left(K^1_{\text{fe}} V^1_{\text{LF,fe}} + K^2_{\text{fe}} V^2_{\text{LF,fe}} + K^3_{\text{fe}} V^3_{\text{LF,fe}}\right) \mathrm{e}^{-\mathrm{j}\beta\ell} \tag{2.42}$$

where K^u_{fe} is the far-end correction factor of the uth line segment. $V^u_{\text{LF,fe}}$ ($V^u_{\text{LF,ne}}$) denotes the low-frequency far-end (near-end) voltage of the uth segment according to (2.19). ℓ is a shorthand for the line's total length $\ell_1 + \ell_2 + \ell_3$. In general:

$$V_{\text{ne}} = \sum_{u=1}^{n} K^u_{\text{ne}} V^u_{\text{LF,ne}} \tag{2.43}$$

$$V_{\text{fe}} = \sum_{u=1}^{n} K^u_{\text{fe}} V^u_{\text{LF,fe}} \mathrm{e}^{-\mathrm{j}\beta\ell}, \tag{2.44}$$

where n denotes the number of segments. The correction factors K^u are found by integrating iw^* along the particular segment. Now that the segment is no longer necessarily parallel with p anymore, let s denote the path length along the entire trace. For example,

$$K^2 = \frac{1}{\ell_2} \int_{\ell_1}^{\ell_1+\ell_2} i(s) w^*(s)\, \mathrm{d}s = \frac{1}{\ell_2} \int_{\ell_1}^{\ell_1+\ell_2} \mathrm{e}^{-\mathrm{j}k_p \ell_1} \mathrm{e}^{\mp \mathrm{j}\beta s}\, \mathrm{d}s, \tag{2.45}$$

because the incident field is uniform along segment 2. In general, it can be shown that

$$K^u = \frac{1}{\mathrm{j}(-k_s \mp \beta)\ell_u} \left(\mathrm{e}^{\mathrm{j}(-k_p p_{\text{end}} \mp \beta s_{\text{end}})} - \mathrm{e}^{\mathrm{j}(-k_p p_{\text{begin}} \mp \beta s_{\text{begin}})}\right), \tag{2.46}$$

where k_s is the incident wave vector along the line segment and k_p is the incident wave number. The distance from the field origin at the beginning (end) of the segment is denoted by p_{begin} (p_{end}). The path length along the trace at the beginning (end) of the segment is denoted by s_{begin} (s_{end}).

Likewise, for the low-frequency contributions V^u_{LF}, the field orientation with respect to the line segment must be taken into account. For example,

$$V^2_{\text{LF}} = -\text{j}\omega c \frac{E^i}{\varepsilon_r} Z_c h \ell_2 = -\text{j}\frac{\omega}{\text{c}_0} E^i h \ell_2 \frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}, \tag{2.47}$$

because the incident magnetic field is parallel to line segment 2, hence it does not contribute to the terminal voltage.

In order to find a transparent worst case for multi-segment traces, recall the single-segment worst case of (2.40). The multi-segment induced voltage is the sum of the segment's contributions. There is no simple (transparent) way to know whether the contributions add up constructively or destructively. Therefore, a loose upper bound on the sum of the contributions is the sum of the upper bound of the contributions:

$$\max|V| = E^i h \cdot \min\left\{ \frac{\omega}{\text{c}_0}\ell\left(1 + \frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}\right), 2n\, \frac{1 - \frac{\sqrt{\varepsilon_{r,\text{eff}}}}{\varepsilon_r}}{\sqrt{\varepsilon_{r,\text{eff}}} - 1} \right\}, \tag{2.48}$$

where ℓ is the total path length of the multi-segment trace and n denotes the number of segments. This upper bound is calculated for the case study and compared to an azimuthal sweep ($\phi \in [0, 2\pi)$) of (2.44) in Figure 2.25.

Notice that even for low frequencies, no curve actually touches the upper bound (contrary to Figure 2.23). This can be understood by recognising that the low-frequency upper bound holds for a straight trace of the same total length ℓ. Only for this straight trace, the electric and magnetic contribution entirely add up at the near end. For any trace deviating from a straight trace, with the same length, the contributions will not add up to that maximum.

Notice also that the high frequencies, the asymptote is rather tight: 2.6 dB higher than the sweep maximum in this particular case study. However, imagine considering a straight trace as many short traces in series. Contrary to the low frequency asymptote, the high frequency asymptote will grow without bound, while the trace remains the same. Therefore, there must also be cases where the high frequency upper bound is not at all tight.

Arbitrary Loads

Basic transmission line theory will now be applied to obtain the either-end induced voltages for arbitrary (generally mismatched) loads.

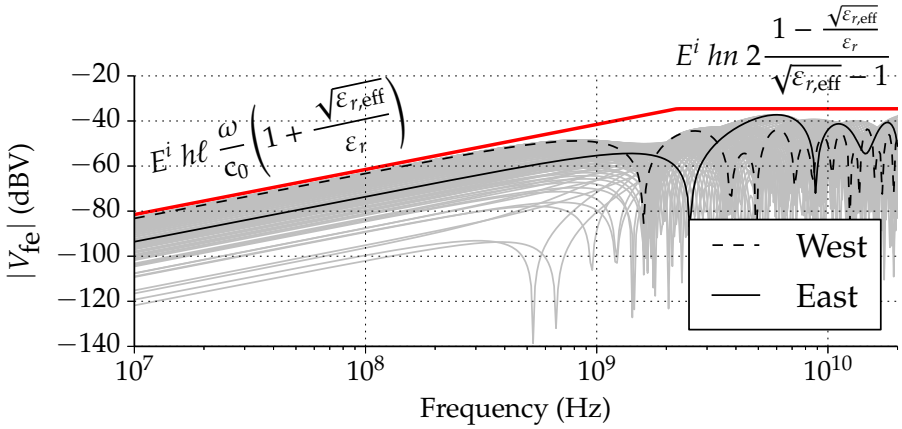


Figure 2.25: Coupling to one end of a rotated, multi-segment ($n = 3$) trace: the eastern orientation (actual far-end coupling) and western orientation (rather near-end coupling) are highlighted. The orientation of the trace was swept from 0 to 2π in 100 steps. The broadband envelope of (2.48) is plotted in red.

From the foregoing, the terminal voltages V_{ne} and V_{fe} on characteristic loads are known, which can be considered voltage waves coming out of a transmission line of characteristic impedance Z_c. These voltage waves will then generally be reflected by the either-end terminal impedances Z_{ee} according to their voltage reflection coefficients:

$$\Gamma_{\mathrm{ee}} = \frac{Z_{\mathrm{ee}} - Z_c}{Z_{\mathrm{ee}} + Z_c}. \tag{2.49}$$

As illustrated in Figure 2.26, the far-end induced voltage wave V_{fe} will be reflected by the far-end terminal impedance, then delayed by the transmission line. Together with the near-end induced voltage V_{ne}, it can be considered a voltage wave $V_{\mathrm{inc,ne}}$ incident on the near-end terminal impedance:

$$V_{\mathrm{inc,ne}} = V_{\mathrm{ne}} + \Gamma_{\mathrm{fe}} V_{\mathrm{fe}} \mathrm{e}^{-\mathrm{j}\beta\ell}. \tag{2.50}$$

If the near-end would be characteristically terminated ($Z_{\mathrm{ne}} = Z_c$), this is exactly the final near-end voltage [38].

In general, however, a near-end reflection will occur:

$$V_{\mathrm{refl,ne}} = \Gamma_{\mathrm{ne}} V_{\mathrm{inc,ne}} = \frac{Z_{\mathrm{ne}} - Z_c}{Z_{\mathrm{ne}} + Z_c} V_{\mathrm{inc,ne}}, \tag{2.51}$$

that is, the near-end reflected wave *would* induce a voltage $V_{\mathrm{refl,ne}}$ on a characteristic load. With this knowledge, the reflected wave can also be represented as an equivalent near-end voltage source as shown in Figure 2.27a:

$$V_{\mathrm{refl,ne,equiv}} = V_{\mathrm{refl,ne}} \frac{Z_c + Z_{\mathrm{ne}}}{Z_c} = V_{\mathrm{inc,ne}} \frac{Z_{\mathrm{ne}} - Z_c}{\cancel{Z_{\mathrm{ne}} + Z_c}} \frac{\cancel{Z_c + Z_{\mathrm{ne}}}}{Z_c} \tag{2.52}$$

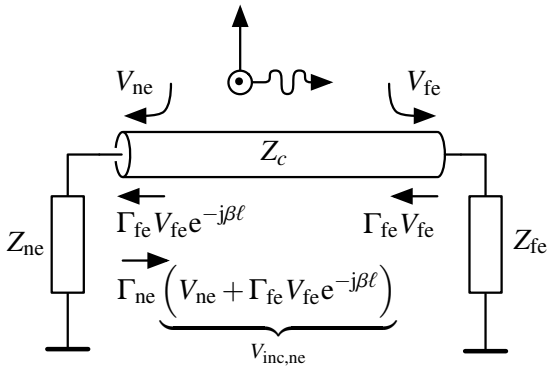


Figure 2.26: From top to bottom: the either-end induced voltage waves, the far-end reflection and the near-end reflection.

To avoid having to consider infinite reflections going up and down the line, the far-end terminal impedance is translated to the near end:

$$\Gamma_{\mathrm{fe@ne}} = \mathrm{e}^{-2\mathrm{j}\beta\ell} \Gamma_{\mathrm{fe}} \tag{2.53}$$

$$Z_{\mathrm{fe@ne}} = Z_c \frac{\Gamma_{\mathrm{fe@ne}} + 1}{\Gamma_{\mathrm{fe@ne}} - 1}, \tag{2.54}$$

where '@ne' denotes 'as seen at the near end'. Now, the final near-end reflected voltage can be calculated using the voltage divider of Figure 2.27b:

$$V_{\mathrm{refl,ne,final}} = V_{\mathrm{refl,ne,equiv}} \frac{Z_{\mathrm{fe@ne}}}{Z_{\mathrm{ne}} + Z_{\mathrm{fe@ne}}}. \tag{2.55}$$

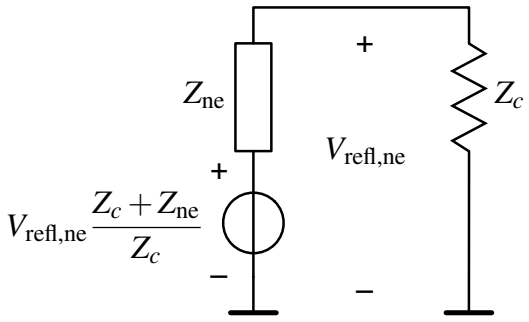
The total near-end voltage is the sum of the incident and the final reflected voltage:

$$\begin{aligned} V_{\mathrm{ne,final}} &= V_{\mathrm{inc,ne}} + V_{\mathrm{refl,ne,final}} \\ &= \left(V_{\mathrm{ne}} + \Gamma_{\mathrm{fe}} V_{\mathrm{fe}} \mathrm{e}^{-\mathrm{j}\beta\ell} \right) \left(1 + \frac{Z_c - Z_{\mathrm{ne}}}{Z_c} \frac{Z_{\mathrm{fe@ne}}}{Z_{\mathrm{ne}} + Z_{\mathrm{fe@ne}}} \right), \end{aligned} \tag{2.56}$$

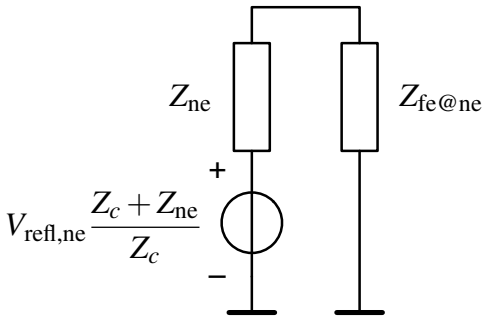
which also holds, *mutatis mutandis*, for the total far-end voltage. Note that this solution is, albeit lengthy, closed-form.

The conclusion of (2.56), especially when expanded, is very opaque. In order to gain insight, a design-oriented worst case will now be sought.

Particularly, an EMC-aware PCB designer will try to achieve sufficient immunity, having some influence on routing and terminal impedances. Sufficient immunity equals worst-case (maximum) voltages at the trace terminals, depending on the immunity of the connected components. Routing influence may consist in reducing trace length or changing trace width within the practical possibilities. Terminal impedances may also be tuned, by introducing frequency-dependent parallel or series impedances.



(a) First step: find the near-end voltage source equivalent to the reflected voltage wave, using a characteristic load.



(b) Second step: find the final near-end reflected voltage, using the actual far-end terminal impedance, translated to the near end.

Figure 2.27: Calculating the final effect of the near-end reflection.

Especially for low-frequency circuits (e.g. a logical output and a logical input), both terminal impedances are expected to be rather mismatched (i.e. some Ω connected to some kΩ). Furthermore, the engineer will be interested in the worst-case voltage magnitude over angle of incidence and frequency.

To deal with the complexity of (2.56), its terms and factors will be separately inspected to find an upper bound to them. The sum and product of these upper bounds will then also constitute an upper bound.

Although the near- and far-end voltages V_{ne} and V_{fe} will never simultaneously amount to the upper bound of (2.48), it is safe to assume so. Moreover, the phasor $\mathrm{e}^{-\mathrm{j}\beta\ell}$ rotates with frequency, so for some frequencies, the near- and far-end induced voltages will add up in phase. Therefore, the first factor of (2.56) can be safely approximated like so:

$$\max\left|V_{\text{ne}} + \Gamma_{\text{fe}} V_{\text{fe}} \mathrm{e}^{-\mathrm{j}\beta\ell}\right| \leq \max|V_{\text{ee}}|\left(1 + \rho_{\text{fe}}\right), \tag{2.57}$$

where ρ_{fe} is the magnitude of the far-end reflection coefficient Γ_{fe}. This reasoning step

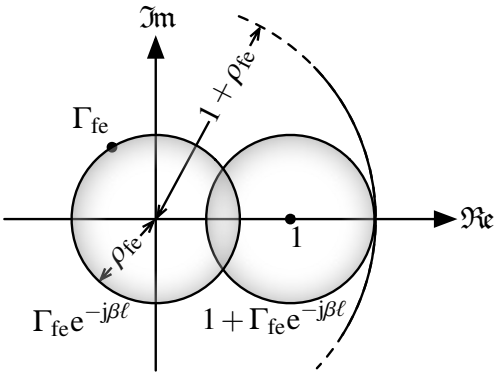
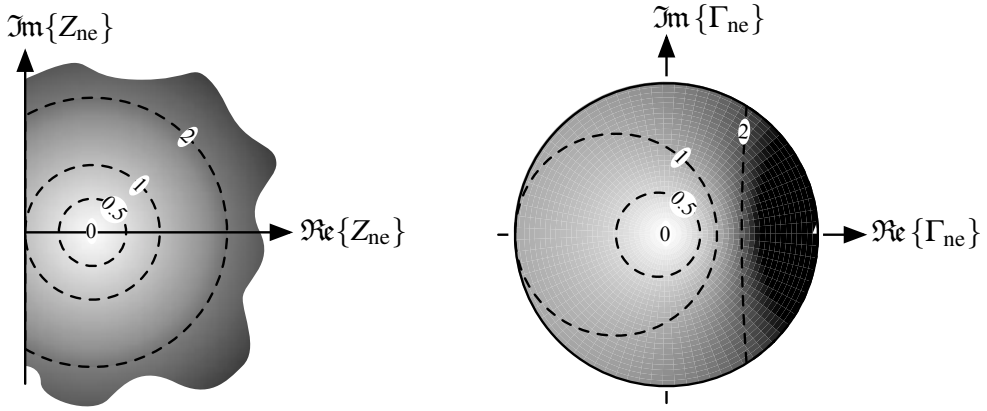


Figure 2.28: Geometric construction of (2.57), normalized by $\max|V_{ee}|$.



(a) On the infinite impedance plane. (b) On the Smith chart.

Figure 2.29: Color map of the near-end impedance dependency.

is illustrated in Figure 2.28; notice that $\Gamma_{fe@ne}$ describes a circle.

In the second factor of (2.56), the absolute value of the next interesting term of (2.56) is:

$$\left|\frac{Z_c - Z_{ne}}{Z_c}\right| = \left|\frac{Z_{ne}}{Z_c} - 1\right|, \tag{2.58}$$

as illustrated in Figure 2.29. However, no obvious design-oriented approximation could be made.

The remaining opaque factor is:

$$\frac{Z_{fe@ne}}{Z_{ne} + Z_{fe@ne}}. \tag{2.59}$$

Let us therefore find its maximum magnitude while $e^{-j\beta\ell}$ describes the unit circle (i.e. the product $\beta\ell$ takes all possible values). To that end, the fraction will be rearranged to obtain a difference, which has an obvious geometric interpretation on the complex plane: a distance.

$$\begin{aligned}\max_{\beta\ell}\left|\frac{Z_{\text{fe@ne}}}{Z_{\text{fe@ne}}+Z_{\text{ne}}}\right| &= \max_{\beta\ell}\frac{1}{\left|1+\frac{Z_{\text{ne}}}{Z_{\text{fe@ne}}}\right|}\\ &= \frac{1}{|Z_{\text{ne}}|\min_{\beta\ell}\left|\frac{1}{Z_{\text{ne}}}+\frac{1}{Z_{\text{fe@ne}}}\right|} = \frac{1}{|Z_{\text{ne}}|\min_{\beta\ell}\left|-\frac{1}{Z_{\text{ne}}}-\frac{1}{Z_{\text{fe@ne}}}\right|}.\end{aligned} \tag{2.60}$$

Put geometrically: the worst case occurs when the mirrored near-end admittance $-Y_{\text{ne}}$ and the far-end admittance seen at the near end $Y_{\text{fe@ne}}$ are closest. Now what does $Y_{\text{fe@ne}}$ look like, on the complex admittance plane?

Recall that admittance and reflection coefficient are related by:

$$Y = \frac{1}{Z_c}\frac{1-\Gamma}{1+\Gamma} \tag{2.61}$$

which is a Möbius transformation, so generalized circles in Γ correspond with generalized circles in Y. Therefore, $Y_{\text{fe@ne}}$ must be a circle. Moreover, this transformation is mirror symmetric about the real axis. As the $\Gamma_{\text{fe@ne}}$ itself is mirror symmetric about the real axis, its transform $Y_{\text{fe@ne}}$ must be mirror symmetric about the real axis too. Hence, the transform $Y_{\text{fe@ne}}$ must be a circle with a real centre.

Now it suffices to find two transformed points to entirely define the transformed circle. Let us take the rightmost and the leftmost value of $\Gamma_{\text{fe@ne}}$, that is $\pm\rho_{\text{fe}}$. Their admittance counterparts are

$$Y_{\text{fe@ne}} = \frac{1}{Z_c}\frac{1\mp\rho_{\text{fe}}}{1\pm\rho_{\text{fe}}}. \tag{2.62}$$

As these points lie on a circle with a real centre, the centre and radius can be found by taking half the sum and half the difference:

$$Y_{\text{fe@ne,radius}} = \frac{1}{2}\frac{1}{Z_c}\left(\frac{1+\rho_{\text{fe}}}{1-\rho_{\text{fe}}}-\frac{1-\rho_{\text{fe}}}{1+\rho_{\text{fe}}}\right) = \frac{1}{Z_c}\frac{2\rho_{\text{fe}}}{1-\rho_{\text{fe}}^2} \tag{2.63}$$

$$Y_{\text{fe@ne,centre}} = \frac{1}{2}\frac{1}{Z_c}\left(\frac{1+\rho_{\text{fe}}}{1-\rho_{\text{fe}}}+\frac{1-\rho_{\text{fe}}}{1+\rho_{\text{fe}}}\right) = \frac{1}{Z_c}\frac{1+\rho_{\text{fe}}^2}{1-\rho_{\text{fe}}^2} \tag{2.64}$$

The sought minimum is constructed in Figure 2.30: $Y_{\text{fe@ne}}$ describes a circle and $-1/Z_{\text{ne}}$ always lies in the left half plane. The minimum distance between a circle and a point is the distance from the circle's centre to the point minus the circle's radius. For a rather mismatched far-end load (a circle close to the imaginary axis), a reasonable approximation can be found by inspection of Figure 2.30:

$$\min_{\beta\ell}\left|-\frac{1}{Z_{\text{ne}}}-\frac{1}{Z_{\text{fe@ne}}}\right| \geq \mathfrak{Re}\left\{\frac{1}{Z_{\text{ne}}}\right\}. \tag{2.65}$$

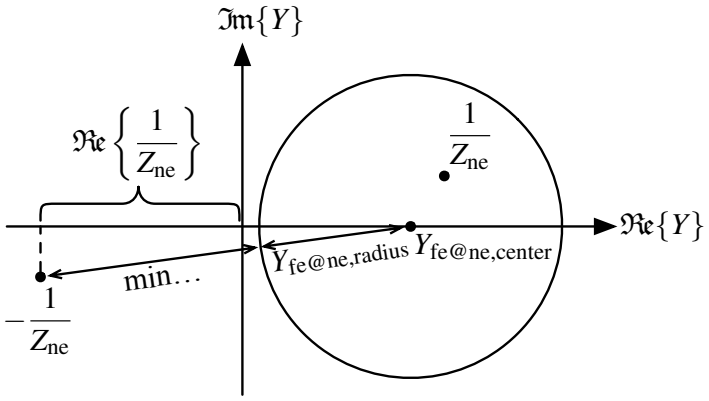


Figure 2.30: Geometric construction of (2.65). Y_{ne} accidentally lies inside the $Y_{\text{fe@ne}}$ circle.

Note that this approximation is also true for rather matched far-end loads, but it will result in a looser upper bound. Other approximations are possible, but for the sake of transparency and in view of the typical application, this candidate was retained.

Plugging this result into (2.60) yields

$$\max_{\beta\ell}\left|\frac{Z_{\text{fe@ne}}}{Z_{\text{fe@ne}}+Z_{\text{ne}}}\right| \leq \frac{1}{|Z_{\text{ne}}|\frac{1}{\Re\mathfrak{e}\{Z_{\text{ne}}\}}} = \frac{1}{\cancel{|Z_{\text{ne}}|}\frac{\Re\mathfrak{e}\{Z_{\text{ne}}\}}{\cancel{|Z_{\text{ne}}|^2}}} = \frac{1}{\cos\angle Z_{\text{ne}}}, \tag{2.66}$$

which is barely transparent.

Plugging the worst case terms and factors found above in (2.56), this upper bound is obtained:

$$V_{\text{ne,final}} \leq \max|V_{\text{ee}}|\,(1+\rho_{\text{fe}})\left(1+\left|\frac{Z_{\text{ne}}}{Z_c}-1\right|\frac{1}{\cos\angle Z_{\text{ne}}}\right), \tag{2.67}$$

mutatis mutandis for the far end.

Note that this upper bound is particularly pessimistic for rather matched far-end loads. Tighter upper bounds exist and were found, but turned out to be opaque.

One obvious design-oriented conclusion may be drawn from this result: matching helps. This can be seen from (2.67), because the smaller ρ_{fe} and the closer Z_{ne} to Z_c, the smaller the upper bound. Note that this matching can be achieved by changing the terminal impedances or by changing the line's characteristic impedance (by tuning the trace width, typically). The last factor shows that a purely capacitive (inductive) near-end load is particularly bad, and adding a small resistance in series (parallel) may dramatically reduce resonances.

To demonstrate the applicability, the upper bound of (2.67) is calculated for the three-segment trace with typical mismatched loads. It is compared with the azimuthally swept solution of (2.56) in Figure 2.31. Notice that for some frequencies, neither the eastern nor the western orientation constitute the worst case.

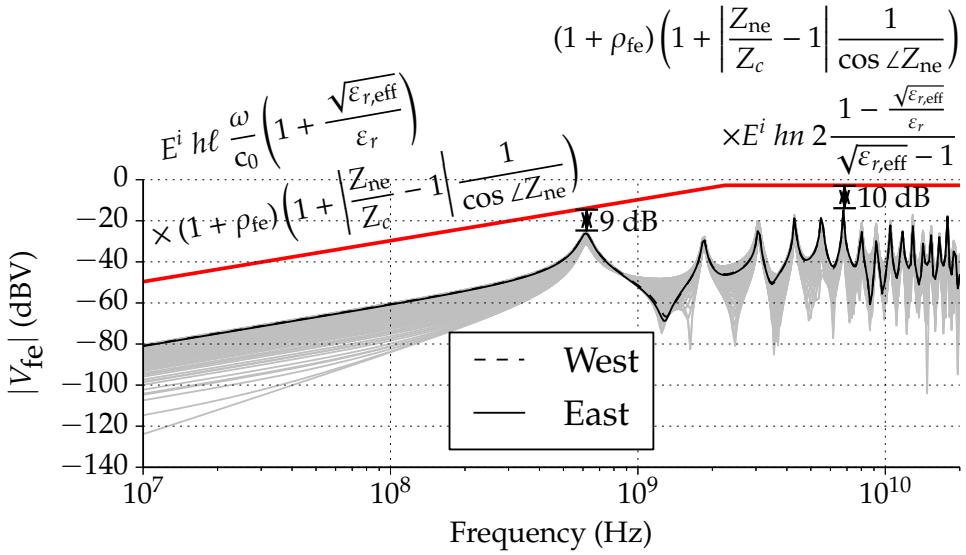


Figure 2.31: Coupling to one end of a rotated, multi-segment trace with mismatched loads: 1 Ω at the near end, 1 kΩ at the far end. The eastern orientation (actual far-end coupling) and western orientation (rather near-end coupling) are highlighted. The orientation of the trace was swept from 0 to 2π in 100 steps. The broadband envelope of (2.67) is plotted in red.

Conclusion

A lightweight model for field-to-trace coupling was constructed by generalising step-by-step. The model consists of a single Taylor cell, corrected for high frequencies with the cross-correlation K between the incident- and eigenwaves. By superposition of one such cell for each segment, the model also applies to multi-segment traces. By another correction factor, the effect of either-end mismatched loads can be taken into account. The model thus predicts the coupling of a grazing incident, vertically polarised plane wave to a multi-segment, uniform microstrip trace with arbitrary terminal loads.

Because the model is closed-form, it outperforms the meshed solution. For instance, it executes ten times as fast as the adaptively meshed model of section 2.3, while correlating to within 0.3 dB average absolute error.

The transparent formulation of Figure 2.31 also has practical design implications. For example, matching the trace impedance and its terminal impedances reduces resonance peaks. The substrate permittivity has only little influence on the coupling. For low frequencies, the coupling is proportional to the total trace length and the substrate thickness. For high frequencies, the coupling is loosely proportional to the number of trace segments, but not to the trace length.

The are also practical (pre-compliance) testing implications. For example, the worst-

case induced voltage on a straight microstrip trace occurs at the near end for low frequencies and the far end for high frequencies. The trace also has a blind azimuthal spot at $\cos(\phi) = \mp\sqrt{\varepsilon_{r,\text{eff}}}/\varepsilon_r$.

The modified Taylor model has a limited validity domain, in comparison with industrial electronics. Therefore, industry-related research should indicate to what extent its limitations form a problem. If so, the model might need improvement.

For instance, no trace width (i.e. impedance) changes or branches can be modelled.

Furthermore, the mismatched loads were supposed to have a frequency-constant complex impedance. This is not the case for IC terminals or passive loads.

Moreover, trace losses were not taken into account. Especially with very reflective terminal loads, this may seriously overestimate the induced voltages. The above analysis should be repeated with a complex β to represent losses, to transparently represent them in the upper bound.

Finally, the presented upper bound is not very tight. A practical case should reveal whether or not this induces costly overengineering. Moreover, as we only started to enjoy Möbius transformations, stricter yet transparent upper bounds may have been overlooked.

2.5 Full-wave simulation

The Taylor cell applied in section 2.3 and simplified in section 2.4 is based on some unchecked assumptions. Firstly, a meandered trace is modelled as a TEM transmission line: uniform, homogeneous and monomodal. Secondly, the substrate field is supposed to be a fraction of the illumination (cf. Figure 2.4). Finally, the bifilar line model is applied to a microstrip trace. Do these modelling decisions significantly degrade its predictions?

To check these assumptions, two case studies will be simulated with a full-wave solver. The case studies are designed to be comparable both with the modified Taylor cell and with measurements. The full-wave solver allows for a perfect illumination of a perfectly-defined geometry and known lossless dielectric with lumped-element loads, without applying the idealisations mentioned above. Comparing its results with those of the modified Taylor cell will therefore gauge the impact of the assumptions.

First, the case studies will be drawn up. These will be entered and then simulated under CST Studio. The simulation results will then be compared to the corresponding predictions of the modified Taylor cell. Consequently, conclusions will be drawn on the validity of the Taylor model's assumptions.

Case Study

The three-segment microstrip studied before is chosen again, for simplicity's sake. In measurement, the PCB will need coaxial connectors to give access to both trace terminals. The entire path from connector to connector needs to be matched to the VNA characteristic impedance of 50 Ω. At the near end, a short calibration standard is connected, inevitably including an electrical delay τ_d, as shown in Figure 2.32. For the far end, two different configurations will be considered.

The first configuration called 'matched', the far end of the trace sees a 50 Ω load. In measurement, this simply corresponds to connecting the VNA to the far-end SMA connector. In this case, the induced near-end voltage will be reflected once by the short circuit and there will be no more transmission line reflections after that.

Therefore, a second configuration called 'probed' is defined. To have a mismatched load at both ends, but still be able to measure with a VNA, a 220 Ω probe resistance is installed in series with the trace at the far end. When the VNA is connected, the trace will see a far-end load of 270 Ω. The actual far-end voltage will be sampled by the 50/270 resistive divider. To be precise, the 220 Ω resistor used in measurement, was measured and found to have a 44 fF parasitic parallel capacitance. This will need to be taken into account both in simulation and using the modified Taylor model.

Simulation Set-up

The trace was entered in CST Microwave Studio as an infinitely-thin, Perfect Electrical Conductor (PEC). The ground plane was a 75×75 mm PEC beneath the trace. The substrate was a lossless dielectric layer with $\varepsilon_r = 4.6$, covering the ground plane. The trace was terminated in 50 Ω discrete face ports. The geometry was meshed using a

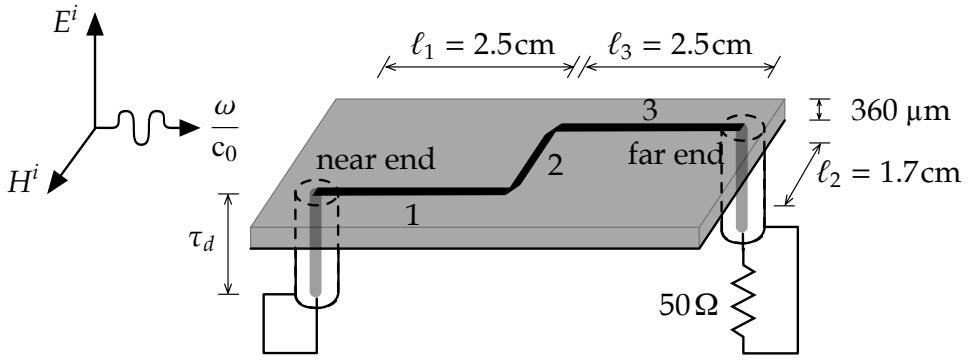


Figure 2.32: Perspective on the case study PCB: a three-segment, 50 Ω microstrip trace over a ground plane, illuminated by a horizontally polarised plane wave. The near end's coaxial connector is shorted, the far end's connector is terminated in a characteristic load (the VNA's input).

hexahedral $\lambda/20$ mesh for 20 GHz, except near the microstrip: one mesh cell across the dielectric thickness and at least two mesh cells across the trace width. The Perfect Boundary Approximation (PBA) compensates for the staircase meshing of the mitered trace corners.

All boundary conditions were set to 'open and add space': that is, $\lambda/8$ extra space was added, terminated by 4 Perfectly Matched Layers (PMLs). This geometry was then illuminated with a vertically polarised plane wave excitation, as illustrated in Figure 2.33a. The plane wave electric field strength was $1/d$, where d is the average GTEM-cell septum distance 42.2 mm.

In order to take the terminal impedances into account, a geometry-circuit co-simulation was chosen, also because of its scaleability to many and non-linear loads. Hence, the above-mentioned geometry with plane wave excitation was entered as one schematic block in the co-simulation. At the near end, a lossless transmission line was connected, representing the coaxial connection with a 80-ps delay τ_d up to the short standard, followed by a perfect short circuit.

At the far end, for the 'matched' configuration, a perfect load was connected, monitored by a voltage probe. As the structure is illuminated with the field caused by 1 V at the septum, the output voltage in volts predicts the measurable S_{21} transfer from septum to far end. The resulting schematic is depicted in Figure 2.33b.

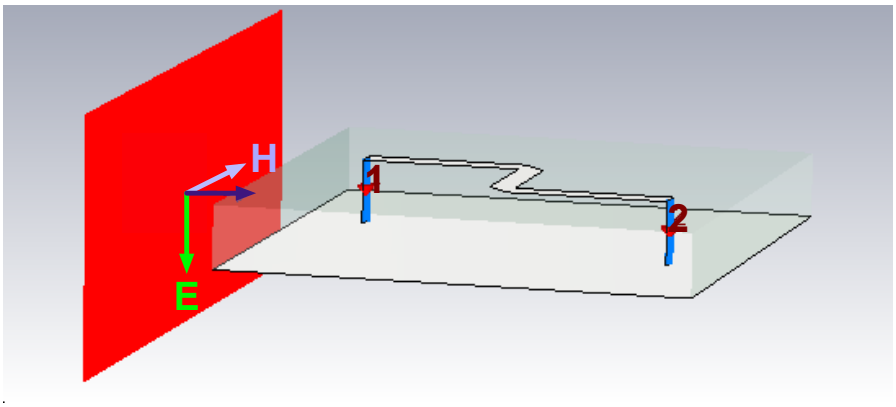
For the 'probed' configuration, the same co-simulation schematic was used, but with the series probe resistance inserted, as shown in Figure 2.33c. Because this probe resistance will consume 2.5 mm trace length, the third segment ℓ_3 was modified to 22.5 mm.

Results

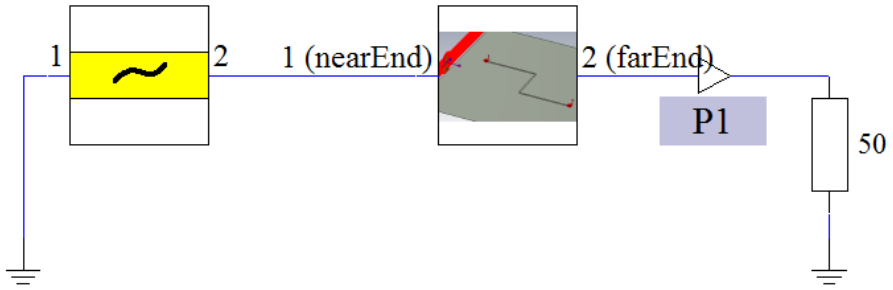
The inherent causality of co-simulation requires a time-domain solver and a Finite Integration Technique (FIT)-based solver [39] was chosen. The 'matched' co-simulation was run with a −80 dB accuracy criterion. In order to allow for phase comparison, the phase reference of the plane wave was moved from the simulation boundary to the near end. The result is compared with the modified Taylor prediction in Figure 2.34.

The log-frequency average difference between simulation and the extended Taylor prediction, a measure for bias, was −0.36 dB over the 50 MHz to 20 GHz range. The average absolute error was 0.94 dB. The comparison was repeated with different meshing resolutions and accuracy criteria, as shown in Table 2.1. With the lowest accuracy settings, the required simulation time is reasonable: 35 s on a 2×2.5 GHz Intel® E5 with 16 GB RAM and an NVIDIA® Tesla™ 20 Graphics Processing Unit (GPU). As can be seen, increasing the accuracy criterion has little influence, but decreasing the mesh size has. Moreover, the more precise the simulation, the lower the average absolute error.

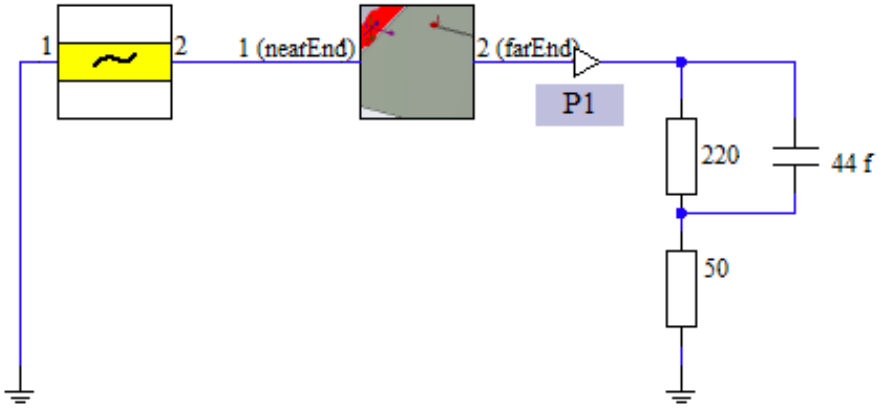
Then the simulation was run for the 'probed' configuration. The simulation seemed to converge (decreasing residual energy), but started diverging again. This problem may be caused by the long-lasting reflections going up and down on the lossless line



(a) Geometry (figure not to scale, in order to see the substrate) as entered into CST Microwave Studio. The dielectric substrate is shown translucent. Note the polarisation of the incident plane wave from the left.



(b) Co-simulation schematic as entered into CST Design Studio for the 'matched' configuration. The first block is a lossless transmission line defined by its delay τ_d, the second block is the geometry with excitation of Figure 2.33a.



(c) Co-simulation schematic as entered into CST Design Studio for the 'probed' configuration, identical to Figure 2.33b, except for the far-end termination.

Figure 2.33: Overview of the CST Studio full-wave simulation.

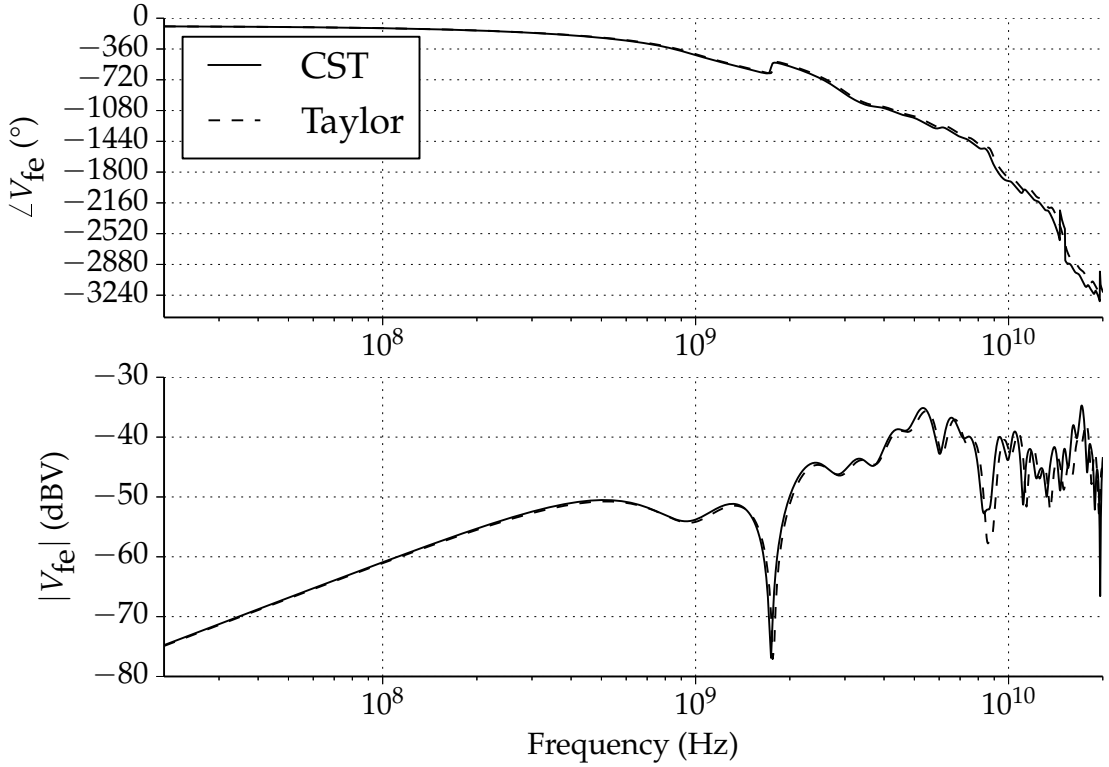
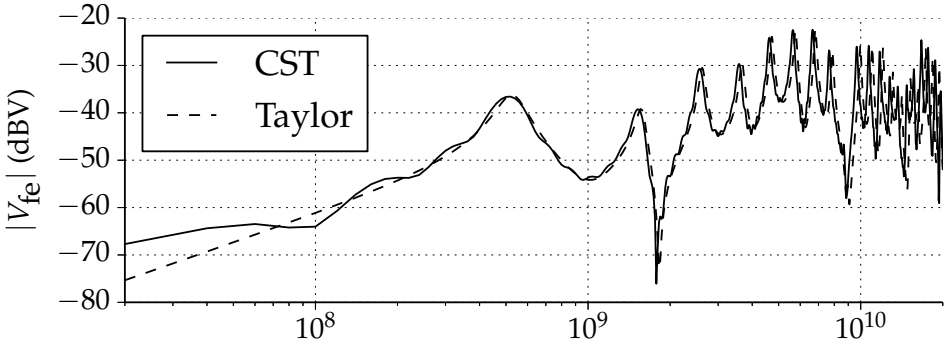


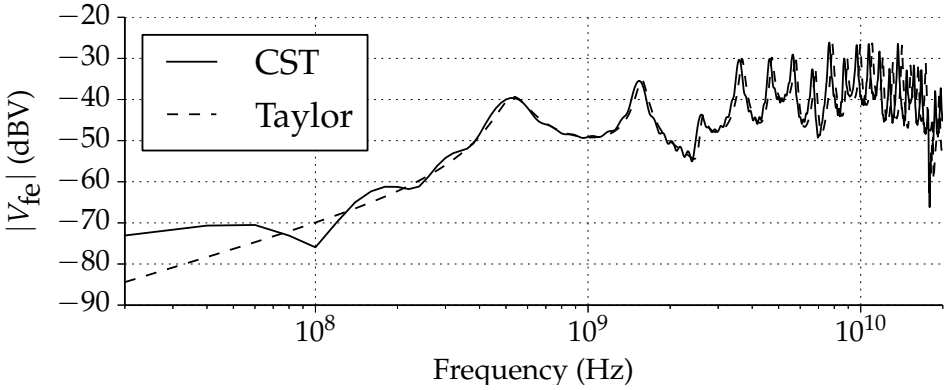
Figure 2.34: Field-to-trace coupling of the meandered trace as simulated ($\lambda/20$, −80 dB) and calculated with the extended Taylor model. The near-end is terminated in a delayed short circuit.

Table 2.1: Sensitivity of CST results for meshing and stop criterion on 'shorted' configuration. Averages are log-frequency weighted from 50 MHz to 20 GHz.

simulation		error Taylor–CST	
meshing	accuracy criterion	average	average absolute ↓
$\lambda/10$	−60 dB	−0.78 dB	1.42 dB
$\lambda/10$	−80 dB	−0.81 dB	1.39 dB
$\lambda/20$	−60 dB	−0.36 dB	0.94 dB
$\lambda/20$	−80 dB	−0.36 dB	0.94 dB



(a) End-fire plane wave incidence from the shorted terminal side.



(b) Broadside incidence from the probed terminal side.

Figure 2.35: Comparison between full-wave simulation and modified Taylor results for a three-segment trace, shorted on one end and equipped with a 220 Ω probe at the other side.

and a numerical imprecision. At any rate, it never reached the accuracy criterion. To work around this problem, the criterion was set to −55 dB. Therefore, the simulation stopped relatively early, which could cause the low-frequency simulation results to be inaccurate. The result is plotted in Figure 2.35a.

To further challenge the validity of the Taylor model, the simulation was repeated by illuminating the geometry from all four cardinal directions. For example, the broadside illumination from the probed terminal side is depicted in Figure 2.35b. The comparison with the model was performed for all four directions as tabulated in Table 2.2. The average absolute error over all this campaign was 2.51 dB.

As can be visually appreciated from Figure 2.35, this is mainly due to a broadband frequency shift; it seems that the CST resonances occur slightly earlier, which corresponds with an additional trace length of about 1 mm. This might be due to the non-zero length of the discrete face ports, which is not accounted for in the modified Taylor model. This hypothesis was not further investigated, however.

Table 2.2: Error of the CST 'probed' simulation under the four cardinal incidence directions.

	error Taylor–CST	
incidence	average	average absolute
end-fire from short side	−0.29 dB	2.58 dB
end-fire from probe side	−0.32 dB	2.37 dB
broadside from short side	−0.38 dB	2.55 dB
broadside from probe side	−0.29 dB	2.55 dB
average	−0.32 dB	2.51 dB

Conclusions

The correlation between full-wave CST simulations and the modified Taylor model was studied on a tree-segment microstrip. It was first configured with a short at the near end and a match at the far end, yielding 0.9 dB average absolute error. Moreover, increasing the full-wave precision decreased the error. Although no extensive sensitivity study was conducted, this suggests that the model is rather truthful. In second configuration with a short and a mismatched resistive load, a 1.5 dB average absolute error was obtained, averaged over the four cardinal azimuthal orientations.

Recall that CST does not rely on a transmission line model of the trace, a simple substrate field formulation nor on the bifilar equivalent of the microstrip. Yet, above low errors and the good visual agreement are observed. Hence, these assumptions may be considered acceptable.

2.6 Measurement

Both the modified Taylor model of section 2.4 and the full-wave simulations of section 2.5 are based on idealisations of reality. For instance, real substrates are lossy and dispersive. Moreover, the illumination performed with a GTEM cell may not exactly be a single plane wave. A field-to-trace coupling set-up will contain non-ideal waveguide transitions that might not be negligible. Finally, spatially extensive discrete components will be used, which might not be competently modelled by lumped elements.

What is the effect of these various idealisations? What non-idealities need to be taken into account to competently model field-to-trace coupling? What accuracy can be attained in the prediction of field-to-trace coupling? Does the transparent upper bound derived from the modified Taylor model work in practice?

To answer these questions, the field-to-trace coupling of a simple case will first be predicted and measured. To try and improve accuracy, the frequency-dependent substrate

permittivity will be measured and taken into account. In another improvement attempt, the non-ideality of the GTEM cell will be characterised, modelled and taken into account. Then, field-to-trace coupling will be measured of increasingly complex cases: a three-segment trace with characteristic and non-characteristic loads, as well as a seven-segment trace. Finally and to the extent that the results correlate, the idealisations will be considered valid.

Single-Segment Microstrip

The simplest case study thus far consisted of an end-fire illuminated, single-segment 5 cm microstrip trace with characteristic loads.

As illumination, the GTEM cell was chosen as the plane wave source. The GTEM cell can be considered a characteristically terminated 50 Ω waveguide with a coaxial input connector. The centre conductor is a strip, called the *septum*. At the top and bottom centre, this mode emulates a vertically polarised plane wave. Commonly, the bottom 'usable volume' is employed for testing equipment. In this thesis, the top field is employed, because the used Schaeffner 250A-SAE GTEM cell has a 10×10 cm top opening for illuminating PCBs. The air field between the PCB and the septum can be approximated by dividing the septum voltage V_{septum} by the septum distance d [40]. The septum distance d was measured to be 42.2 mm on average under the 10×10 cm PCB aperture, so for 1 V on the septum, the air field amounts to

$$2E^i = \frac{V_{\text{septum}}}{d} = \frac{1}{42.2 \times 10^{-3}} \approx 23.7\,\text{V/m}. \tag{2.68}$$

To measure the broadband transfer from the GTEM cell input to any trace terminal, a VNA is employed as shown in Figure 2.36. Port 1 of the VNA is connected to the GTEM cell input, port 2 is connected to the terminal of interest of the illuminated trace. If the trace is matched to the VNA characteristic impedance, the measured S_{21} parameter equals the voltage transfer between GTEM septum and a 50 Ω trace terminal. Put differently, the terminal voltage caused by 1 V at the septum in dBV will numerically equal the S_{21} parameter in dB.

To keep the entire path matched, the PCB needs to provide coaxial connectors to give access to both trace terminals. In order to fabricate the case study with small and known mechanical uncertainties, the PCB was made in a four-layer industrial FR4 process, traces matched to 50 Ω and connector-to-board transitions optimised, as can be seen in Figure 2.37. To limit the influence of the screws, M2 nylon screws were used. The PCB's ground contact was matched to the shape of the GTEM-cell aperture to smooth the transition from the ground plane to the GTEM-cell wall. The resulting PCB is shown in Figure 2.38. In order to express the layout as an objective function of fabrication and experiment constraints, it was described in code, using the library that will be developed on page 123ff.

The measurement result was first predicted using the modified Taylor model. The substrate's relative permittivity ε_r was taken to be 4.6. Using ADS LineCalc, the filling

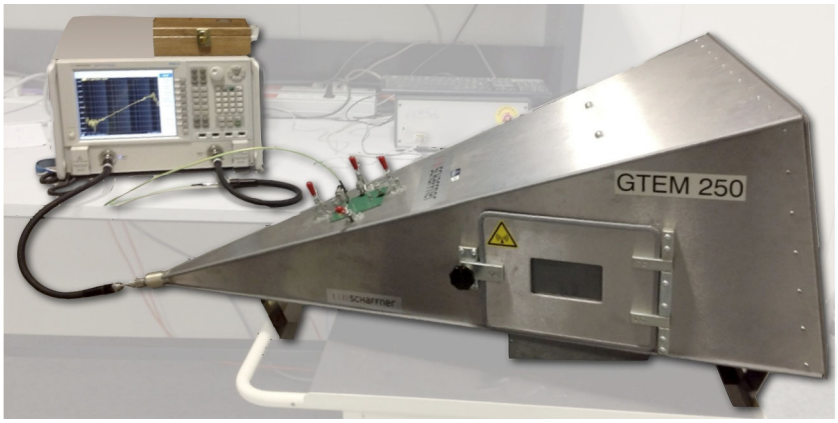
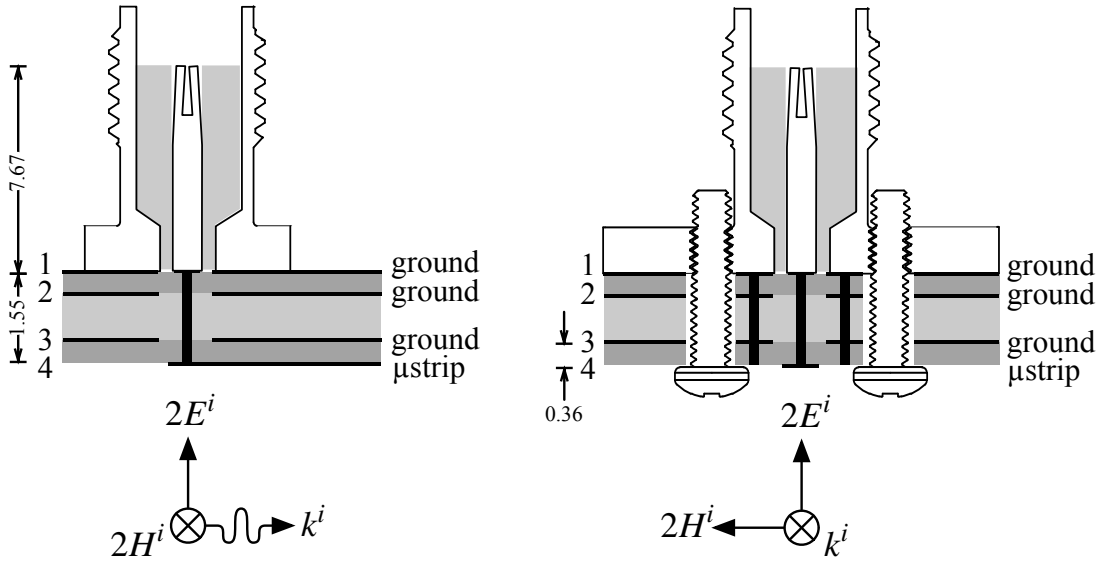


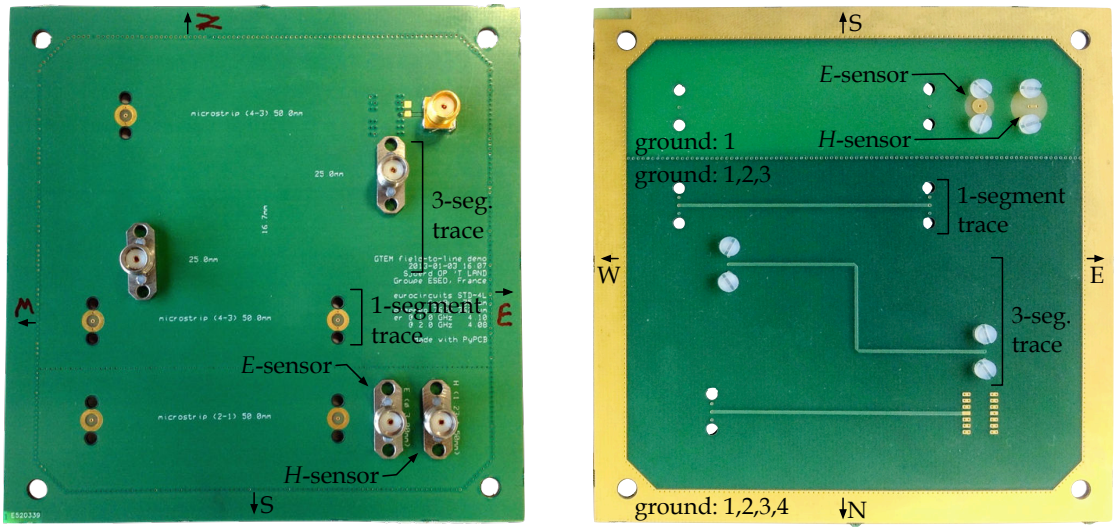
Figure 2.36: Measurement set-up overview with the relevant parts highlighted: VNA and GTEM cell with the 10×10 cm PCB mounted.



(a) Lateral cross-section.

(b) Frontal cross-section.

Figure 2.37: SMA-to-microstrip transition: a Molex SD-73251-185 SMA jack, screwed onto a footprint, optimised using CST to minimize reflections (drawing not to scale, dimensions in mm).



(a) Top side (layer 1). (b) Bottom side (layer 4).

Figure 2.38: GTEM 10×10 cm PCB.

factor of the microstrip was calculated to be 0.67 on average over the frequency range of interest. With this approximation, the microstrip's effective relative permittivity $\varepsilon_{r,\text{eff}}$ was calculated to be 3.4. The substrate thickness was taken to be 362 μm. The incident field strength of (2.68) was entered and the model was run.

The coupling to the single-segment was then measured with an Agilent N5247A VNA. First a calibration was performed to the 3.5 mm reference plane, that would then connect to the GTEM cell input and the SMA connector on the PCB outside. The frequency was logarithmically swept from 20 MHz to 20 GHz. The measurement is compared to the modified Taylor model prediction in Figure 2.39.

As a measure for systematic bias, the log-frequency average error Taylor – measurement was calculated: −2.1 dB. The average absolute error was 2.27 dB. To get a more robust metric of the accuracy, the measurement was repeated by turning the PCB in all four cardinal directions. Over all four measurements, the average error was −1.81 dB and the average absolute error was 2.63 dB.

Permittivity Modelling

In a first attempt to improve the prediction, the substrate's permittivity was taken into account. Because the supplier guarantees nothing with regard to the substrate permittivity, we would like to measure it ourselves. From the industrial perspective, a measurement method is sought that requires few measurement-specific investments. However, typical EMC laboratory equipment like a VNA will be supposed available. From the modified Taylor model, the permittivity is known to have medium influence

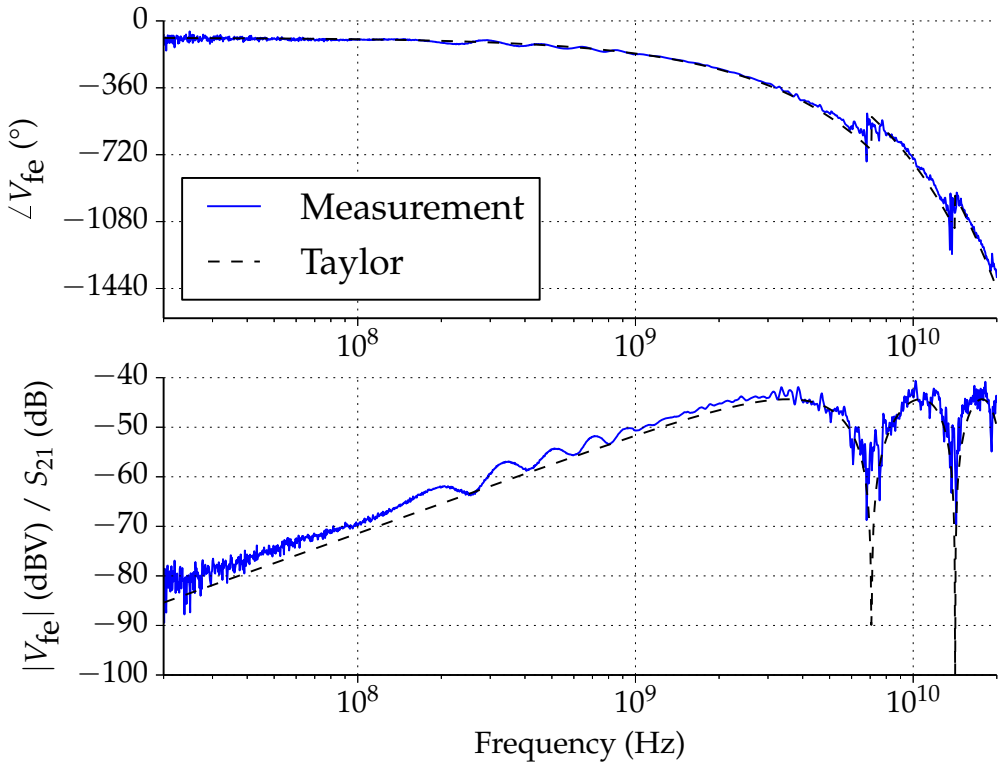


Figure 2.39: Measured and predicted field-to-trace coupling for a 5 cm microstrip segment.

on the field-to-trace coupling. Therefore, a moderate measurement accuracy of 10% is targeted.

Our case study is the Eurocircuits 4-layer standard stack-up used for the field-to-trace measurement, shown in Figure 2.40. The prepreg (core) consists of 2 (probably 4) sheets of Technolam NP-155F [41]. The prepreg and core are both composite materials consisting of fibre glass fabric ($\varepsilon_r \sim 5$) in epoxy resin ($\varepsilon_r \approx 3.2$) [42]. The fabric consists of straight warp yarns in length direction, with weft yarns going up and down in the cross- (transversal) direction. We do not know if this PCB was rotated during panelisation, that is, x and y might be swapped. Most probably, the laminate sheets are rectangular, so the warp yarns in all sheets will be parallel.

First, a short overview of existing permittivity measurement methods will be given. From these methods, a practical method will be chosen and compared to reference measurement performed by a research acquaintance.

A complete overview of all existing measurement methods is outside the scope of this

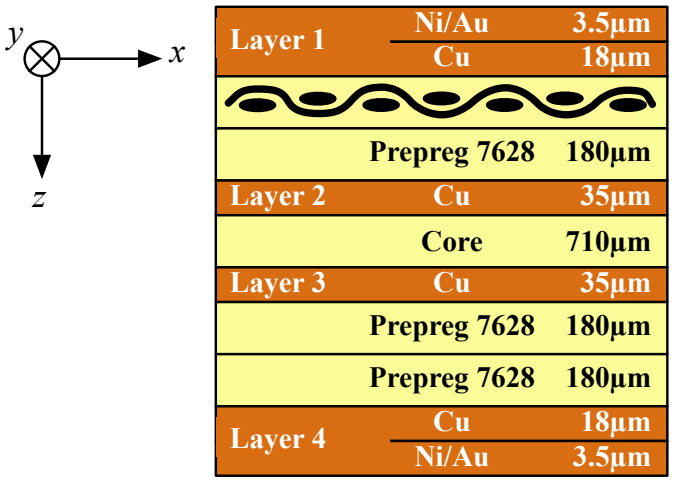


Figure 2.40: Eurocircuits standard 4-layer stackup with material directions: weft- or x-direction, warp- or y-direction, and depth- or z-direction.

thesis. Moreover, as these measurement methods are inventions, there is no overview of all *possible* measurement methods. Furtunately, some classifications can be made and general properties can be attributed to these classes.

All measurement methods can be classified as resonant or non-resonant. Resonant methods work for a finite number of frequencies and accurately measure even small losses (ε_r''). Non-resonant methods are broadband and only measure high losses accurately. [43]

Examples of resonant methods are the resonant cavity, the Fabry-Perot resonator, the open (or Courtney) resonator, Full Sheet Resonance (FSR) [44], planar resonators pressed against or between samples [45]. Examples of non-resonant methods are the coaxial probe, the parallel-plate set-up, transmission line (planar [46], coaxial or rectangular [47, 48]) and free-space measurement. These methods all require a *fixture*: something that couples guided waves to a known geometry containing the Material Under Test (MUT). A recurring problem is the presence of air gaps between fixture and MUT [49, 43].

The choice of a measurement technique depends on the frequency range of interest, the expected values of real permittivity and loss, the required measurement accuracy, the temperature range to be characterized, the size and shape of the material and the necessity of non-destructive or non-contacting measurements.

We choose a planar ring resonator [50, 51, 52, 53] to evaluate the possibility to measure accurately without special (i.e. expensive) fixtures. It is a destructive method: the ring is etched on the substrate, which cannot be reused afterwards. It is a resonant method, so only a few frequency samples of the permittivity will be available.

To evaluate this rather experimental method, a reference measurement is needed.

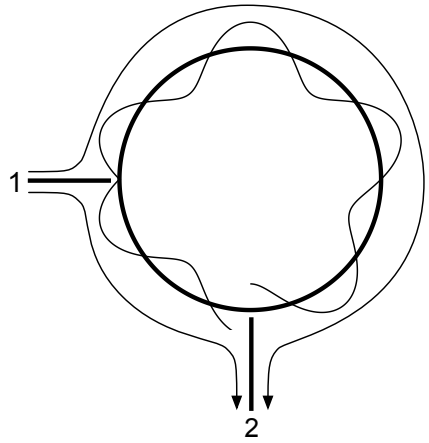


Figure 2.41: Microstrip ring resonator excited with $5\lambda = 2\pi r$. The clockwise- and counterclockwise wave amplitudes are superimposed on the artwork.

As the Rectangular Dielectric WaveGuide (RDWG) is an established method, mastered by our research acquaintance Olga Tereshchenko at the University of Twente [48], it was chosen as the reference measurement. It is a destructive, banded method: samples of different sizes need to be cut out for insertion in waveguides of different bandwidths.

The planar ring resonator is illustrated in Figure 2.41. It consists of a microstrip ring, which supports a clockwise- and a counterclockwise propagating wave. Two microstrip feeds, spaced 90° apart, are capacitively coupled to the ring. Imagine that power coming from port 1 equally splits into a clockwise- and a counterclockwise propagating wave. If the circumference $2\pi r$ equals an odd multiple of the wavelength λ (like in the figure), both waves interfere destructively at the feed point of port 2, therefore S_{21} is minimum. If the circumference equals an even multiple of the wavelength, there is constructive interference, hence S_{21} is maximum.

By measuring the resonance frequencies (the local maxima of S_{21}) the phase velocity v and the real effective permittivity $\varepsilon_{r,\text{eff}}$ can be calculated:

$$v = \lambda f = \frac{2\pi r}{k} f \quad k = 2, 4, 6, \ldots \tag{2.69}$$

$$\varepsilon_{r,\text{eff}} = \left(\frac{c_0}{v}\right)^2, \tag{2.70}$$

where k is the harmonic index and r is the effective radius of the ring. From this $\varepsilon_{r,\text{eff}}$ and the trace cross-sectional geometry, the real substrate permittivity ε_r' can then be calculated using a microstrip model.

Note that the imaginary permittivity can also be measured using this method, by measuring the quality factor Q, which represents the total resonator loss. However, to be accurate, radiation and conductor losses must also be known and subtracted to isolate

the dielectric loss [54]. Furthermore, there is no simple analytical relation between few geometrical parameters, observed Q and the imaginary permittivity; all geometrical parameters play a role and thereby complicate the metrological analysis.

A typical approach is to simulate a completely known ring resonator without MUT, either by means of closed-form relations [52] or by a finite-element solver [55]. Then the complex permittivity of a hypothetical MUT is varied and some interpolant is fitted to the results. Finally, the measurements are mapped back to the complex permittivity by the inverse interpolant. For simplicity, and because the modified Taylor model does not take losses into account anyway, this will not be done.
This method for measuring the permittivity has several metrological advantages. First and foremost, the microstrip is infinite along its propagation direction, so the uniformity criterion of transmission line is fully met. Put differently, there are no fringing fields at the ends that need to be taken into account.

Secondly, only few quantities need to be known precisely (cf. (2.69)). If the ring is sufficiently large with respect to the trace width ($r/w > 7$), which is our case, the wave travels the centreline of the annular ring [56]. Therefore, even under- or overetching of the PCB will not affect r, only photolithographical scaling errors, which are generally known and small. Trace width has almost no influence on the filling factor (FF) which relates ε_r and $\varepsilon_{r,\mathrm{eff}}$. The uncertainty of the resonance frequency f, when measured with a VNA is also known and small.

Thirdly, the orientation of the microstrip turns along the ring's circumference with respect to the FR4 fabric orientation. As a result, the average ε_r is found and the alignment with the fabric is non-critical. Notice that the field is mostly perpendicular to the substrate, so we find $\varepsilon_{r,zz}$, which is the interesting tensor component for field-to-trace coupling under grazing incidence.

Lastly, under certain conditions, the feed construction is non-critical. As long as the feeds are short with respect to the ring circumference, resonance modes in the feeds only appear beyond the interesting bandwidth of the resonator. As long as the coupling gap g is sufficiently large with respect to the trace width w ($g > 0.4w$, [53]), the resonance frequencies of the ring can be considered untouched by the feeds. As long as the feed is reasonably matched to the VNA, the ring resonances will dominate the S_{21} readout and there is no need for de-embedding.

Two resonator rings were put on the test panel of Figure 2.42 with 1.91 cm and 8.38 cm respective diameters, targeting overlapping resonance frequencies on a reasonable PCB surface. The microstrip was placed on outer layer 1, with a ground plane on layer 2 (cf. Figure 2.40). Surface mount SMA connectors were soldered onto the resonator feeds using reflow soldering. No solder mask was present on the substrate samples as well as on the rings. Consequently, the rings have a gold finish.

The S_{21} parameter of both rings was measured using an Agilent N5247A network analyser, after calibration up to the SMA connectors. As the coupling is very weak, a 10 Hz intermediate frequency (IF) bandwidth was used to lower the noise floor. A 200 ps electrical delay was subtracted to flatten the phase response somewhat. The

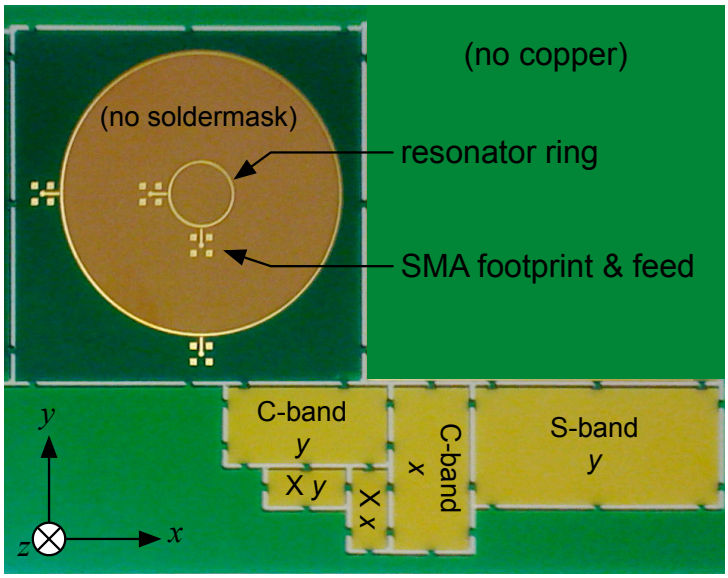


Figure 2.42: Panel containing both the resonator rings and substrate samples for the RDWG measurement method.

result is shown in Figure 2.43. The frequency was swept from 10 MHz to 12 GHz on the large ring, from 2 GHz to 26 GHz on the small ring, both with 801 points.

The resonances were manually identified and the frequency (on the 801-point scale) of the local maxima are tabulated in Table 2.3 for both rings. Notice that from the 12th harmonic upward, another mechanism seems to obscure the ring resonances. On the small ring, a similar effect appeared after the 4th harmonic, but left the 6th and 8th distinguishable. The QTEM cut-off frequency of this particular microstrip is [11]:

$$f_{\text{MS,TEM}} \approx \frac{21.3 \times 10^6}{(w + 2h)\sqrt{\varepsilon_r + 1}} \approx 6.4\,\text{GHz}, \tag{2.71}$$

so resonances above that frequency should be interpreted with caution.

Using ADS LineCalc, we reverse-calculated the substrate ε_r' for a measured $\varepsilon_{r,\text{eff}}$ at a given frequency. The resulting permittivities are added to Table 2.3 as the $\varepsilon_{r,zz}$ column.

The reference RDWG method consists of measuring the scattering parameters of an rectangular waveguide with and without the MUT sample, cf. Figure 2.44. A software algorithm then solves for the complex permittivity ε_r.

We fabricated samples for the available rectangular waveguide sections. As can be seen in Figure 2.44a, the wave only 'feels' the vertical component of the permittivity tensor $\varepsilon_{r,yy}$, mainly in the middle of the sample. To also measure the horizontal component $\varepsilon_{r,xx}$, we fabricated rotated samples from the same substrate. Notice, because of the field profile, that air gaps at the left and right end of the sample hardly impact the measurement result.

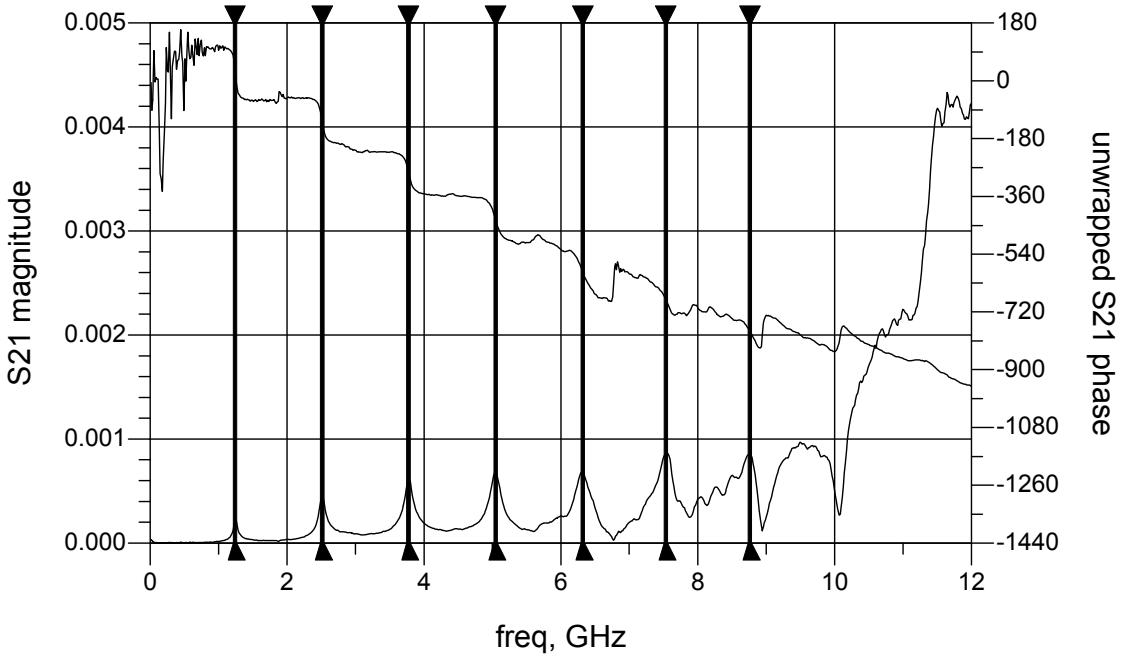
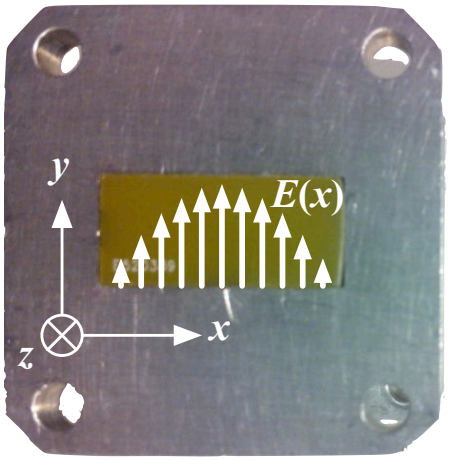


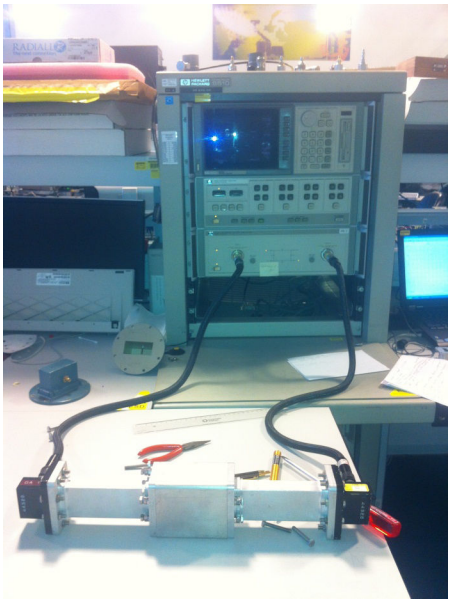
Figure 2.43: Measured S_{21} parameter of the large resonator ring, with resonance peaks indicated. An electrical delay was subtracted to make the 180° phase jumps manifest.

Table 2.3: Observed resonances using the two microstrip ring resonators.

observation		interpretation			
diametre	frequency ↓	harmonic	speed (m/s)	$\varepsilon_{r,\text{eff}}$	$\varepsilon'_{r,zz}$
83.82 mm	1.24 GHz	2	1.63×10^8	3.38	4.61
83.82 mm	2.51 GHz	4	1.65×10^8	3.28	4.45
83.82 mm	3.77 GHz	6	1.66×10^8	3.28	4.44
83.82 mm	5.05 GHz	8	1.66×10^8	3.26	4.40
19.15 mm	5.51 GHz	2	1.66×10^8	3.27	4.41
83.82 mm	6.32 GHz	10	1.66×10^8	3.25	4.37
83.82 mm	7.53 GHz	12	1.65×10^8	3.29	4.42
19.15 mm	11.09 GHz	4	1.67×10^8	3.23	4.30
19.15 mm	17.24 GHz	6	1.73×10^8	3.01	3.93
19.15 mm	22.82 GHz	8	1.72×10^8	3.05	3.93



(a) Photo of MUT sample in waveguide, with superimposed *E*-field profile.



(b) Set-up overview photo.

Figure 2.44: The RDWG measurement.

Table 2.4: Material property calculation algorithms available in the Agilent 85071E software programme

	Method	Calculates	Best for...	Particularities
1.	Nicolson- Ross	ε_r & μ_r	magnetic, short or lossy MUTs	Fast, but has discontinuities.
2.	Reflection/ Transmission Epsilon Precision Model	ε_r ($\mu_r \equiv 1$)	non-magnetic materials, long, low-loss MUTs	Accurate, no discontinuities.
3.	Transmission Epsilon Fast Model	ε_r ($\mu_r \equiv 1$)	non-magnetic materials, long, low-loss MUTs	Similar to precision but faster and better for lossy MUTs.

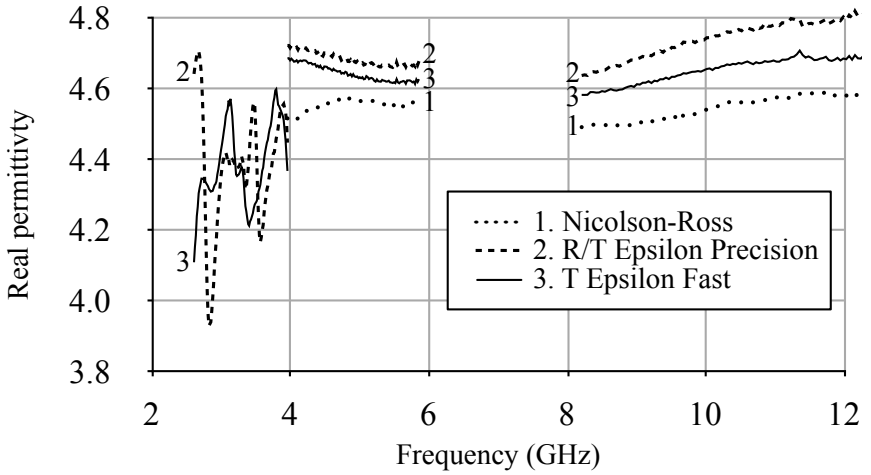
Next, Tereshchenko measured the *S*-parameters with an HP 8510C VNA at 21° and 30% relative humidity. She repeated the measurement for all three bands, using rotated samples if available: 5 measurements in total (cf. Figure 2.44b).

Finally, the complex permittivity needed to be extracted from this measurement data. Three algorithms in the Agilent 85071E software are available as outlined in Table 2.4. As the Flame Retardant 4 (FR4) samples are non-magnetic, short, and have medium loss, Table 2.4 shows that none of the three available methods is an obvious match. Therefore, Tereshenko tried all three, and chose model 2, because it gave physically plausible results for all bands (cf. Figure 2.45) and because of its robustness against positioning errors.

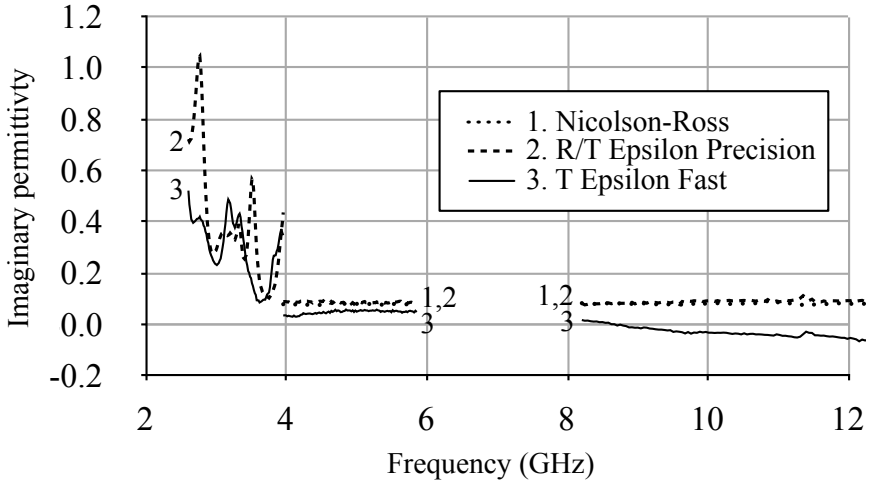
To summarise, the real permittivity perpendicular to the substrate ($\varepsilon'_{r,zz}$) of the prepreg between layer 1 and 2 was measured using a microstrip ring resonator. For reference, the complex permittivity in the plane of the substrate ($\varepsilon_{r,xx}$ and $\varepsilon_{r,yy}$) of the entire stackup was measured by Tereshchenko using the RDWG method. The results are compared in Figure 2.46.

The obtained values vary with frequency between 4.3 and 4.8. Supposing material isotropy ($\varepsilon \equiv \varepsilon_{xx} \equiv \varepsilon_{yy} \equiv \varepsilon_{zz}$) and homogeneity between the layers, the permittivities measured with both methods should be equal. Under that condition only, the difference between permittivities obtained with both methods equals the relative measurement error between the two methods. In the X-band, both methods correspond to within 12%, which is slightly worse than our objective. In the C-band, both methods correspond to within 5%, which was our initial objective.

To take the dispersive real permittivity of the used substrate into account, this measurement can be used. Instead of plugging a constant scalar $\varepsilon_r = 4.6$ into the modified Taylor model, a frequency-dependent vector needs to be entered. Lacking a physical model, a frequency-linear interpolation of the samples of Table 2.3 was entered.



(a) The real part of the permittivity.



(b) The imaginary part of the permittivity, representing the losses.

Figure 2.45: The complex permittivity of the y-direction samples, calculated with the different methods.

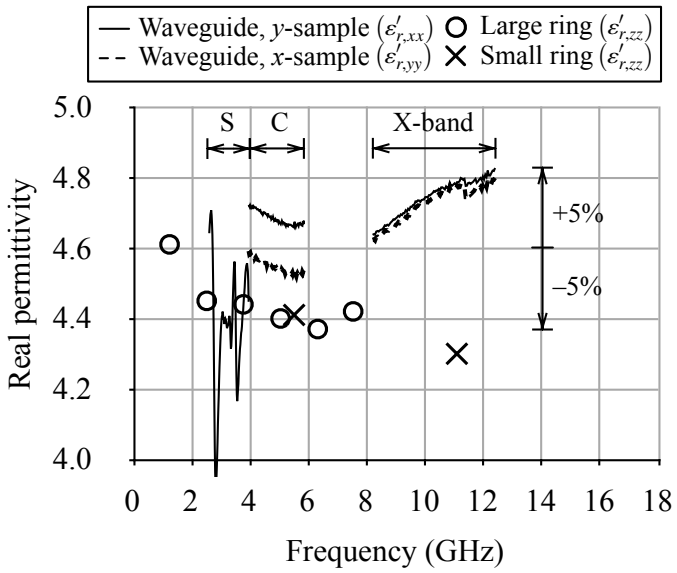


Figure 2.46: Comparison of permittivity measured using waveguide and resonator methods.

The field-to-trace coupling was calculated again and is compared with measurement in Figure 2.47. The average error over all cardinal directions was −1.52 dB average and 2.79 dB average absolute.

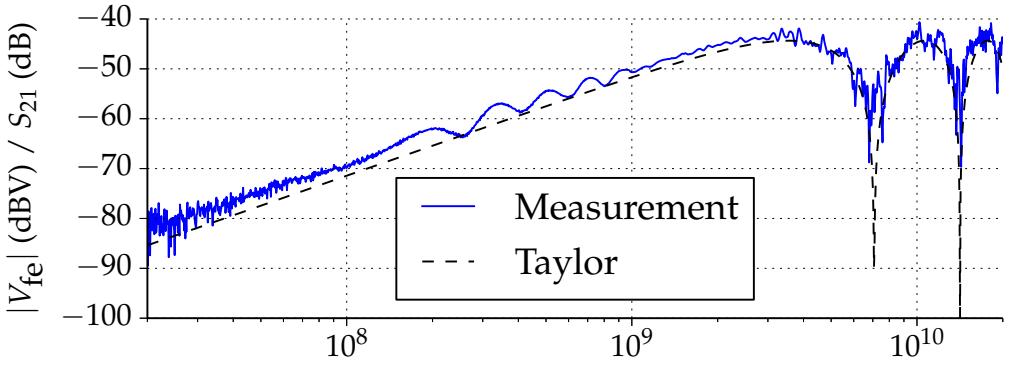
In this example, the systematic bias was improved with 0.29 dB by taking into account the measured permittivity. However, the average absolute error worsened by 0.16 dB. Moreover, as can be seen from Figure 2.47, the prediction clearly worsened beyond 3 GHz. This may be explained by the Quasi-TEM (QTEM) assumption breaking down differently in the planar resonator and in the illuminated trace. Because measuring and taking into account the substrate permittivity takes considerable effort, without yielding clear improvement, the simple model of $\varepsilon_r = 4.6$ will be used from here on out.

GTEM Cell Modelling

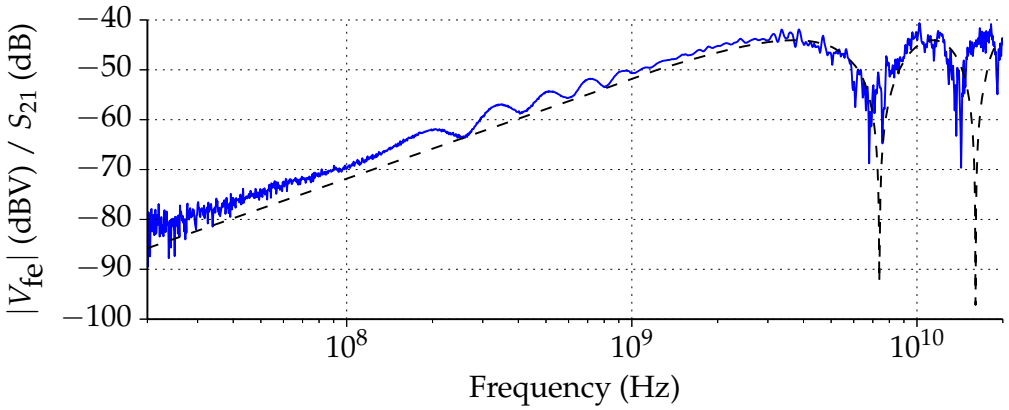
In another attempt to improve the predictions, the GTEM cell's illumination is critically examined.

Ideally, the GTEM cell emulates a vertically polarised plane wave, as will be explained. This model will be challenged by field-strength sensors and a Voltage Standing Wave Ratio (VSWR) measurement. Consequently, a first-order model describing the cell's non-ideality will be proposed.

A GTEM cell can be considered a rectangular, paraxial, tapered 50 Ω waveguide. The narrow end of the taper is equipped with a coaxial connector and the wide end is terminated in a hybrid resistive/absorber 50 Ω load, as shown in Figure 2.48a. As the



(a) Typical values: $\varepsilon_r = 4.6$ and $\varepsilon_{r,\text{eff}} = 3.4$, yielding −1.81 dB average error and 2.63 dB average absolute error over all cardinal directions. (Repetition of Figure 2.39.)

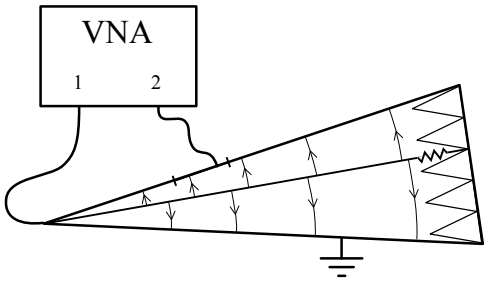


(b) As measured with the ring resonator, yielding −1.52 dB average error and 2.79 dB average absolute error over all cardinal directions.

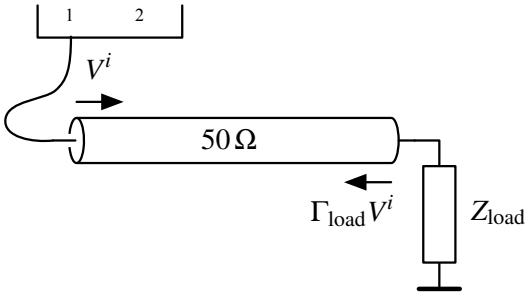
Figure 2.47: Measurement and prediction of the field-to-trace coupling using different substrate permittivity models.

medium is homogeneous (air) and the line is approximately uniform (taper, matching), the fundamental mode is TEM, as shown in Figure 2.49. By placing a PCB, the ground plane of the PCB becomes part of the metallic wall. This seemingly infinite ground plane corresponds well with the earlier analysis of the substrate field strength, summarised in Figure 2.4.

To get a rough idea of the field uniformity under the 10×10 cm opening of the GTEM cell, the field uniformity was measured. To do so, *E*-field and *H*-field sensors were integrated in one corner of the PCB (cf. Figure 2.38). The *H*-field sensor consists of two vias and a trace that form a loop tangential to the septum, as short as technologically possible for the field to be uniform in the loop (1.23 mm), as high as technologically possible to increase its surface (1.50 mm). To measure the *E*-field, a disk of 3 mm diameter was



(a) Lateral cross section.



(b) First-order model of the GTEM cell, including the absorber reflections.

Figure 2.48: Modelling the measurement set-up to illuminate PCBs.

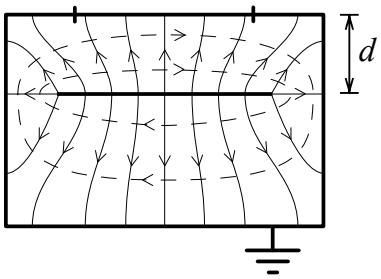


Figure 2.49: Frontal cross section and the fundamental mode: solid electrical field lines and dashed magnetic field lines.

used, in order to stay under $\lambda/10$ at 10 GHz and to have sufficient coupling surface to measure strong enough a signal.

The transfer from GTEM cell septum to the *E*-field sensor was measured at four different PCB orientations by rotating the PCB. Up to 5 GHz, the log-frequency averaged difference between the maximum and minimum transfer was 1.4 dB, and 5.8 dB between 5-20 GHz. As far as the *H*-field sensor is concerned, it only has two valid positions. The average difference in transfer between both positions was 1.5 dB up to 5 GHz, and 3.9 dB between 5-20 GHz. In absolute terms, a CST simulation of the *H*-field sensor yielded on average 1 dB more than the measured transfer up to 10 GHz, after which the discrepancy went up to 5 dB.

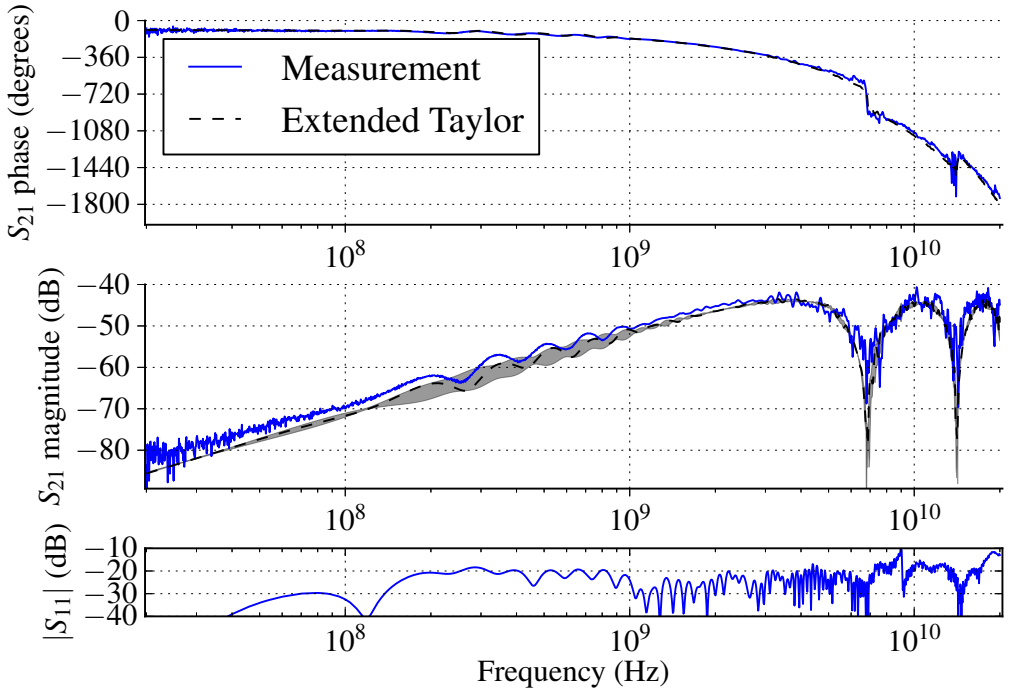
These numbers suggest that the field non-uniformity is in the order of a few dB. However, the shape of its non-uniformity is not known, so the predictions cannot be adjusted accordingly. A simple model for the field non-uniformity is therefore needed.

Recall the conception of a GTEM cell as a perfect waveguide. If it actually were, an incoming voltage wave V^i would travel along the septum once and be perfectly absorbed at the wide end. As a consequence, the S_{11} observed at the GTEM cell input should be $-\infty$ dB, or rather the noise floor of the VNA. However, it is not: the manufacturer promises -19 dB maximum and we even measured incidental excesses up to -10 dB in the DC-18 GHz range.

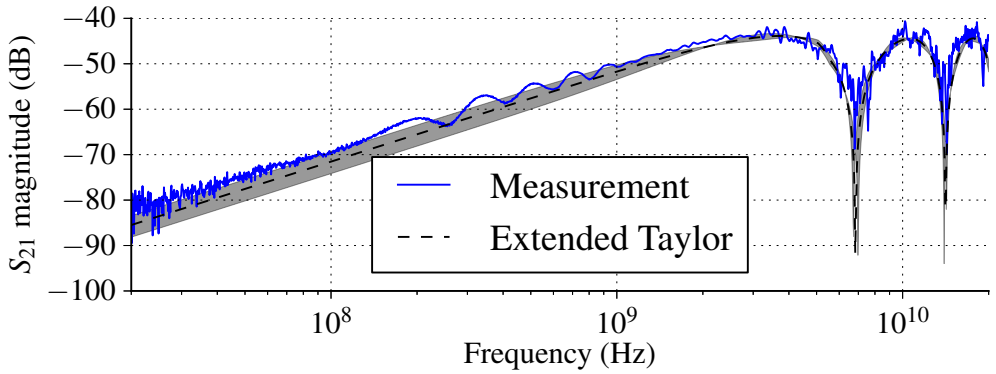
A first-order model to explain this observation is to suppose the GTEM waveguide to be perfectly matched and lossless, but the wide-end load to be slightly mismatched, as illustrated in Figure 2.48b. In this model, there will be the incident wave E^i and *one* reflected wave $\Gamma_{\text{load}}E^i$, where Γ_{load} is the electric field reflection coefficient of the load. The value of Γ_{load} can be easily extracted from an S_{11} measurement, the reference plane should just be phase offset from the GTEM input to the centre of the illuminated trace.

Using this model, the GTEM-field-to-trace coupling can be predicted more accurately. First, the induced voltage by the forward-going wave E^i that illuminates the trace should be calculated. Then, the induced voltage by the backward-going wave $\Gamma_{\text{load}}E^i$ that illuminates the trace should be added. This prediction was tested on the same simple case of a 5-cm microstrip. The S_{11} parameter of the GTEM cell was first measured, phase-shifted by 53 cm, the equivalent distance from the GTEM-cell input to the middle of the trace. The resulting prediction (dashed) is compared with measurement (blue) in Figure 2.50a. The average error is now -1.75 dB (was -1.81 dB) and the average absolute error is now 2.60 dB (was 2.63 dB). More importantly, a striking similitude is visually observed in the 0.1–2 GHz range.

If the position of the trace is not well-known with respect to the GTEM cell input, the phase of Γ_{load} must be considered unknown. In that case, the voltage induced by the backward-going wave may add to or subtract from the voltage induced by the forward-going wave. That way, the gray uncertainty band in Figure 2.50a could be calculated, only based on $|S_{11}|$. Without measuring anything, the manufacturer-given



(a) Model using the measured S_{11} (dashed curve) or $|S_{11}|$ (gray band).



(b) Model using the manufacturer-specified VSWR ≤ 1.25 (or $|S_{11}| < -19\,\text{dB}$).

Figure 2.50: Measurement and modeling of the coupling to the far end of a 5 cm, characteristically terminated microstrip, taking into account the first reflection of the illuminating GTEM cell.

maximum voltage standing wave ratio (VSWR) 1.25 ($|S_{11}| = -19\,\text{dB}$) can be used to obtain the uncertainty band of Figure 2.50b. These uncertainty bands do not improve the accuracy, but inform about the measurement uncertainty that is inherent to the set-up.

To summarise, measuring the S_{11} parameter of the GTEM cell and taking it into account is relatively easy. The prediction of the field-to-trace coupling improved by 0.1 dB on (absolute) average. The striking resemblance in the 0.1–2 GHz range suggests that the hybrid load reflections actually cause the oscillations. Even if only the scalar VSWR is known, the measurement uncertainty due to absorber reflections can be quantified. For these reasons, the GTEM model will be taken into account from here on out.

Beyond 2 GHz, another non-ideality seems to take over, which might be explained as multi-moding. Notice also that the systematic bias remains about −2 dB. Because this is observed in measurement, but not in full-wave simulation with plane wave illumination, we hypothesize that this is due to a yet unidentified non-ideality of the GTEM cell.

More Complex Cases

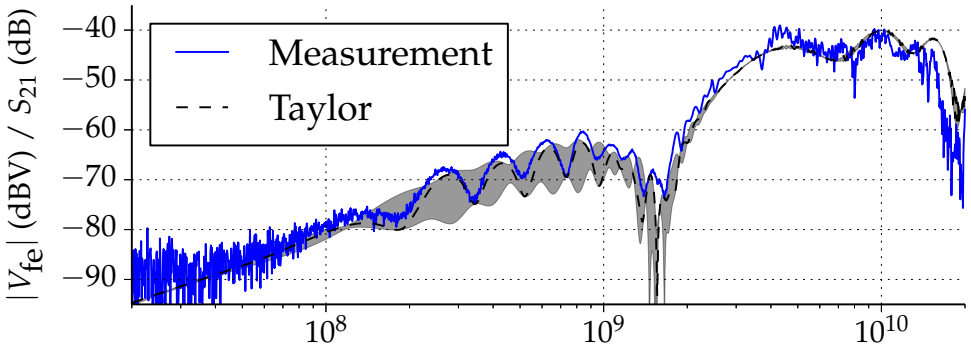
To further challenge the modified Taylor model, measurements will now be performed on more complex traces and non-characteristic loads. For each case, a comparison will be made with the deterministic prediction and the transparent upper bound of the modified Taylor model.

The first complex case is the three-segment trace with characteristic loads of Figure 2.24. Similarly to the first measurement, the trace is a 50 Ω microstrip with mitred bends, as can be seen in Figure 2.38.

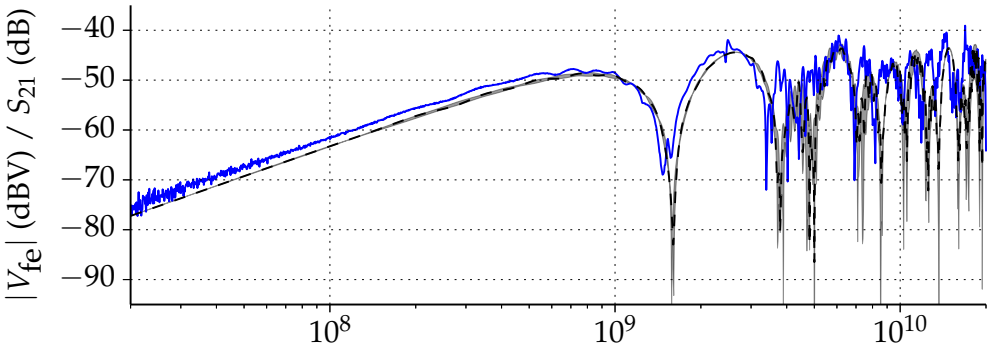
The S_{21} parameter was measured to one end of the trace, while terminating the other end in 50 Ω. The square PCB was rotated in order to illuminate the trace from all four cardinal directions. Judging from the frequency-average error, the best- and worst matching directions are compared to the modified Taylor model in Figure 2.51a and 2.51b, respectively. Averaged over all four directions, an average error of −1.53 dB is found, and an average absolute error of 2.85 dB.

The measurements are also compared to the transparent upper bound in Figure 2.51c. The upper bound seems to envelope all measurements, as expected. However, even the western illuminated trace should be about 2 dB below the low-frequency asymptote, as predicted in Figure 2.25 and by full-wave simulations not incorporated in this thesis. It seems that the GTEM field strength is about 2 dB higher than predicted by V_{septum}/d, for a yet unknown reason. Despite that, the upper bound is rather tight, even when taking into account this error.

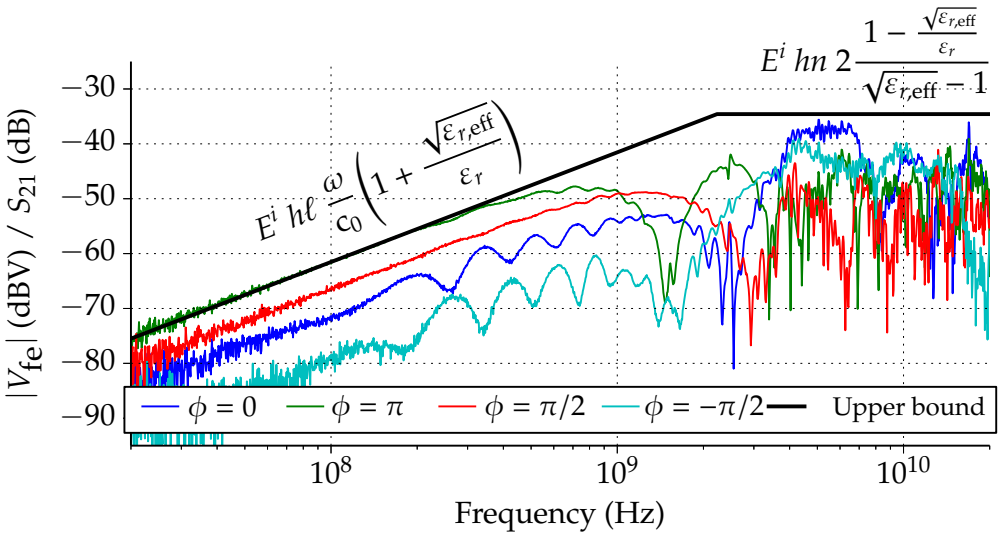
Next, the same trace is shorted at the near end by an Agilent 85052D-60006 short circuit. From the near end of the illuminated trace to the short circuit, the signal traverses the PCB, the SMA connector and the short standard. The PCB has a thickness t of 1.55 mm. Modeling this path as a homogeneous waveguide, the delay $\sqrt{\varepsilon_r} \cdot t/\mathrm{c}_0$ should approximate 11.1 ps. The SMA connector has a Teflon dielectric ($\varepsilon_r = 2.1$) of 7.67 mm from board to reference plane. Similarly, this should account for 37.1 ps. The short



(a) Best matching direction: north (broadside from far-end side). The average Taylor–measurement error is −1.19 dB, the average absolute error is 2.85 dB.

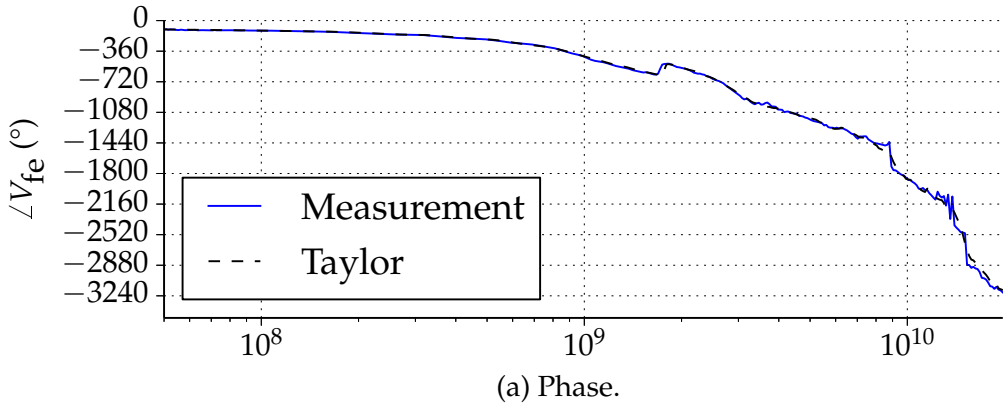


(b) Worst matching direction: west (endfire from the near-end side). The average Taylor–measurement error is −2.00 dB, the average absolute error is 3.14 dB.

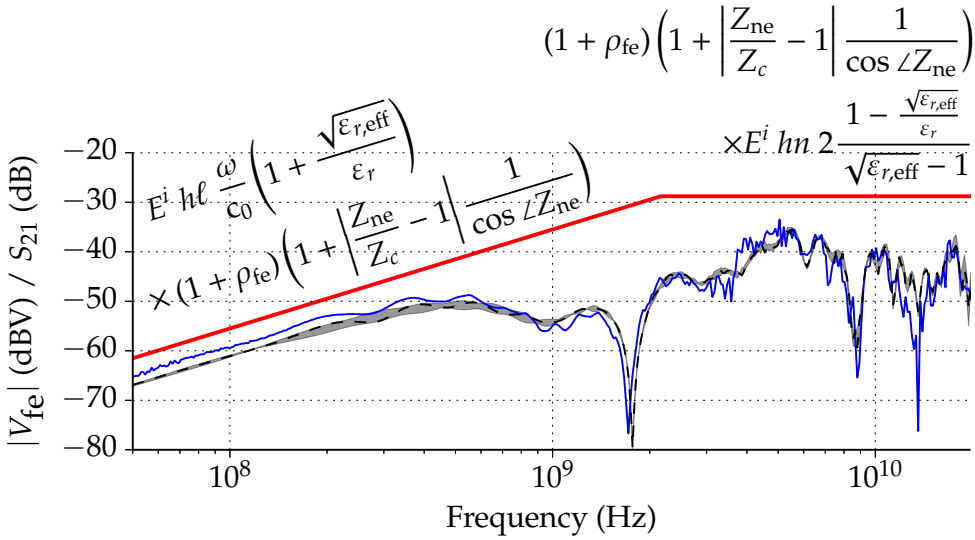


(c) All directions, as compared to the upper bound of (2.48).

Figure 2.51: Measurement versus modified Taylor prediction of the coupling to a three-segment ($n = 3$) microstrip with characteristic loads.



(a) Phase.



(b) Magnitude and upper bound.

Figure 2.52: Measurement versus modified Taylor prediction of the coupling to a three-segment microstrip, shorted at the near end, matched at the far end. Port 1 is the GTEM cell input, port 2 is the trace's far end.

standard is specified to have a 31.78 ps delay, totaling to a delay of 79.95 ps. The near-end load is thus modeled by a short circuit with a lossless, 79.95-ps delay. The far end of the illuminated trace is directly connected to the VNA like in the former experiment.

The measurement was performed and compared against the extended Taylor model. The average difference with the modified Taylor model was −0.22 dB with an average absolute error of 2.13 dB.

To consider either-end reflections, a far-end mismatch allowing for measurements was needed. For that purpose, the trace was cut open at the far end and a 0603 surface

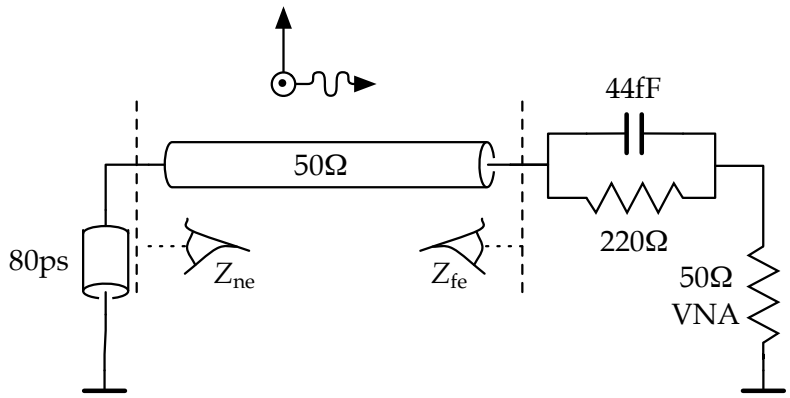


Figure 2.53: Model of the near-end short standard and the far-end resistive probe, leading to the VNA input.

mount 220 Ω resistor was soldered in series. This modification shortened the third line segment ℓ_3 to 22.5 mm. Just before, this resistor was measured up to 20 GHz with the low-budget fixture that will be described in section 3.3. The measured impedance could be satisfactorily modelled by a 44 fF parasitic capacitance. As the VNA, connector and transition are matched to 50 Ω, they can be modeled as a simple 50 Ω load. The resulting model of the terminal loads is shown in Figure 2.53.

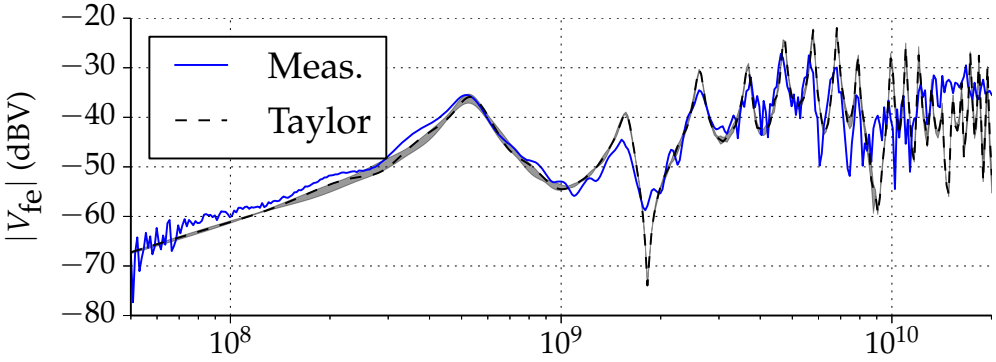
The measurement was then performed and the S_{21} readout of the VNA was divided by the voltage transfer of the resistive voltage divider to estimate the actual far-end voltage. The Taylor–measurement error, averaged over all four cardinal directions and over log-frequency is −1.75 dB, the average absolute error is 4.02 dB. The directions with the best and the worst average error are shown in Figure 2.54a and 2.54b, respectively.

The rather high error might be explained by the fact that the 220 Ω probe resistor is illuminated itself, too. With rather reflective loads, many reflections travel up and down the line, making its losses less negligible. These two non-idealities are neither taken into account by the full-wave simulation nor by the extended Taylor model. Therefore, they might explain the discrepanciy between measurement and the modified Taylor model.

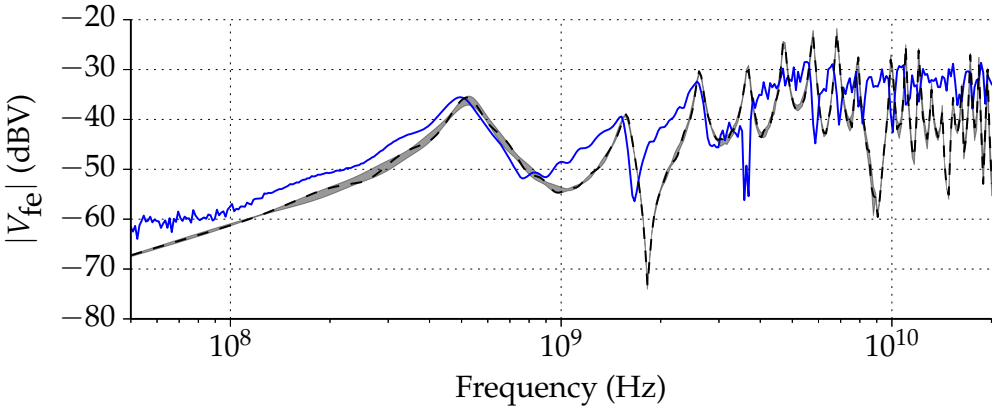
As demonstrated in Figure 2.54c, the coupling remains under the transparent upper bound for all cardinal directions. For this particular trace and these four directions of illumination, the proposed upper bound is 7 dB too pessimistic for the low frequency asymptote, and 13 dB too pessimistic for the high frequency asymptote.

To assess the validity of the modified Taylor model for traces with more complex routing, another trace is needed. Our research acquaintance Tvrtko Mandić provided us with measurements that he performed on such a trace.

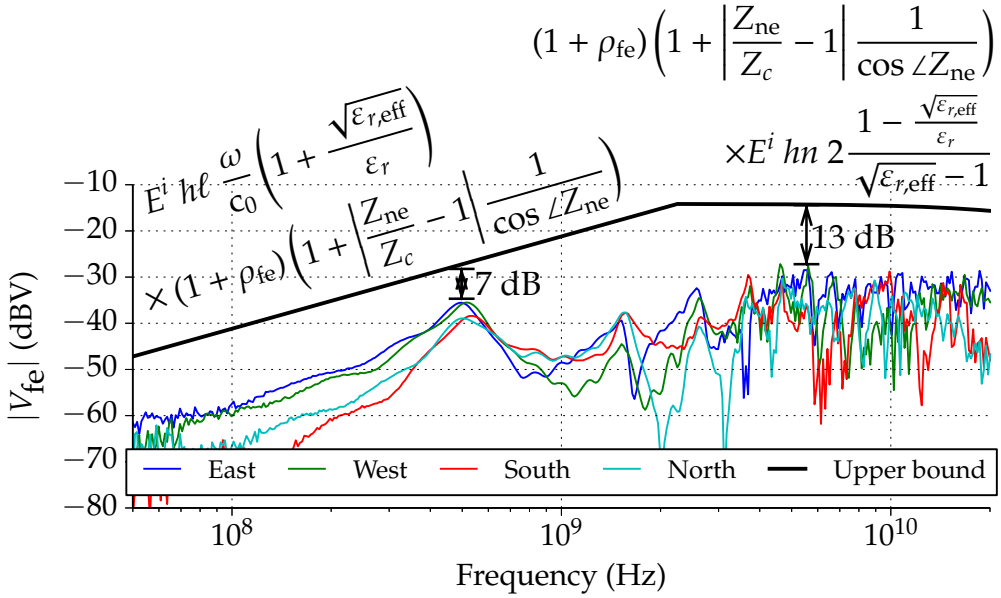
Mandić realised a 50 Ω microstrip trace on a 1-mm FR4 substrate ($\varepsilon_r = 4.5$), hence of 1.75 width ($\varepsilon_{r,\mathrm{eff}} = 3.6$). His trace consisted of 7 segments of 14.5, 10.75, 19.5, 21.75, 6,



(a) Best correlation: west (endfire illumination from the far-end side). The average Taylor–measurement error was −0.86 dB, the average absolute error 3.08 dB.



(b) Worst correlation: east (endfire illumination from the near-end side). The average Taylor–measurement error was −3.58 dB, the average, absolute error 5.51 dB.



(c) All directions, compared to the transparent upper bound of (2.67). The high-frequency limit is not flat, because of the parasitic capacitance in the near-end load.

Figure 2.54: Induced voltage in the near end of the multi-segment trace, as measured (port 1 on the GTEM cell input, port 2 is the trace's far end equipped with a series resistive probe, the near end being shorted using a calibration standard).

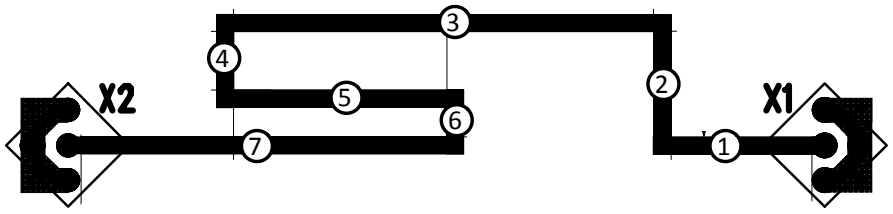


Figure 2.55: Mandić's 7-segment microstrip trace.

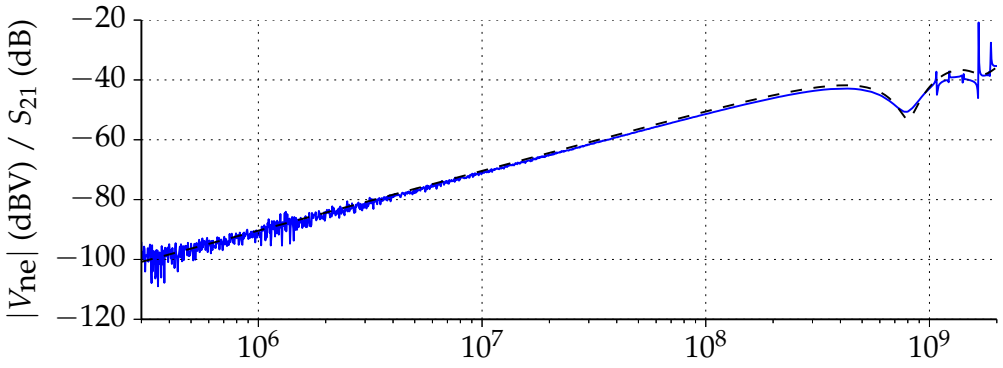
3 and 14 mm length, as enumerated in Figure 2.55. The 90° bends are not mitred. The trace is fabricated on a 10×10 cm PCB. The trace terminals are equipped with 3-pin through-hole SMA connectors.

The field-to-trace coupling was measured by Mandić using a TEM cell. Analogously to a GTEM cell, the TEM cell is a rectangular, coaxial 50 Ω waveguide. A top opening of 10×10 cm allows illuminating PCBs with an air field $2E^i$ of V_{septum}/d. The septum distance d is constant over the opening: 45 mm. The TEM cell has coaxial input and output connectors. Similarly to the GTEM measurements, the coupling measurements are performed by connecting one port of the VNA to the TEM cell input, and the other port to one end of the transmission line. The second TEM cell port, as well as the second transmission line port are terminated in 50 Ω.

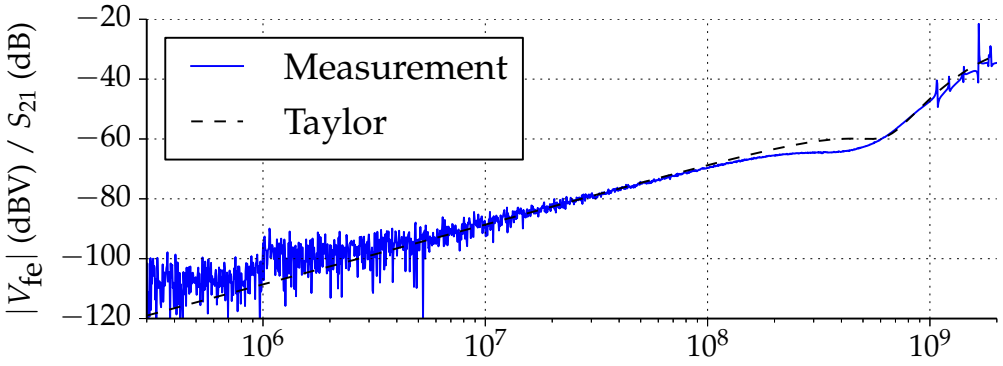
The result is compared to the modified Taylor model for the near-end and the far-end coupling in Figure 2.56a and 2.56b, respectively. Mandić showed that the sharp peaks measured above 1 GHz are due to TEM cell resonances [57]. The log-frequency averaged Taylor–measurement error over both terminal voltages is −0.05 dB and the average absolute error is 2.07 dB.

It be noted that there is little systematic bias, both numerically and visually. This corroborates with the hypothesis that the 2 dB systematic offset observed in GTEM measurements is really due to a non-ideality of the GTEM cell. Moreover, the low average absolute error suggest that even these seven traces with mutual interactions can be competently modelled by the modified Taylor model.

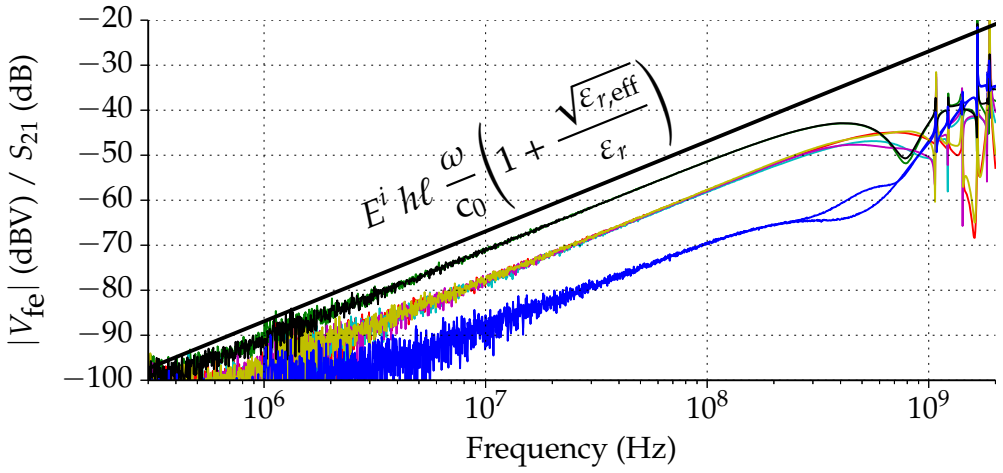
To assess the validity of the upper bound, the far-end and near-end coupling was measured in all four cardinal directions. Because of the high number of segments n, the high-frequency upper bound is out of sight, as can be seen in Figure 2.56c. Nonetheless, the low-frequency upper bound is respected and about 4 dB too pessimistic.



(a) Near-end coupling (0.73 dB average error, 1.15 dB average absolute error).



(b) Far-end coupling (−0.83 dB average error, 2.98 dB average absolute error).



(c) All ends, all directions and the worst-case asymptote.

Figure 2.56: Comparison between measurement and both models.

Conclusions

The field-to-trace coupling of increasingly complex cases was measured and compared with the modified Taylor prediction, as summarised in Table 2.5. The coupling to a single 5 cm trace was measured and predicted by supposing an ideal plane wave illumination and a constant substrate permittivity $\varepsilon_r = 4.6$.

Using a microstrip resonator, the substrate permittivity was then measured and taken into account. The prediction did not unambiguously improve and above 10 GHz, it visually deteriorated. This might be explained by the gradual breakdown of the QTEM assumption at these frequencies. Because of the considerable effort without clear improvement, this permittivity model was not retained.

In another attempt to explain the discrepancy between measurement and prediction, the first reflection of the GTEM cell hybrid load was measured and taken into account. This yielded a slight numerical, but a clear visual improvement of the predictions. Moreover, it yields a quick indicator of the measurement uncertainty due to this GTEM cell non-ideality. Because of this improvement at the price of a simple measurement, this GTEM cell reflection model was retained.

Then, with the same GTEM cell, the coupling to a three-segment trace with matched and unmatched loads was measured and predicted. The average Taylor–measurement error over all GTEM cell measured cases is −1.3 dB, which indicates a systematic negative bias. The average absolute error was 2.9 dB, although that might not be that good an accuracy metric; often, the match is better appreciated visually.

Lastly, measurements performed by Mandić on a seven-segment trace in a TEM cell up to 2 GHz were predicted. The small error suggests that the modified Taylor model also holds for traces with closely-spaced segments with mutual interactions. Although the TEM cell was supposed ideal, almost no systematic bias was observed: −0.05 dB. Therefore, the systematic bias observed in the precedent GTEM cell measurements is probably due to a non-ideality that is proper to the GTEM cell.

The transparent upper bound was not exceeded throughout these measurements. The tightness of the upper bound varied: margins ranging from 0 dB to 13 dB were observed.

2.7 Conclusions

The coupling of incident electromagnetic waves to PCB traces was found to be studied by many authors, yet with few transparent results. Only Leone derived a transparent low-frequency upper bound for the coupling of an arbitrary-incident, arbitrarily polarised plane wave to a single microstrip trace segment with moderately mismatched terminal loads.

To explore the problem and obtain a reference, a 5 cm microstrip segment was manually meshed into $\lambda/20$ Taylor cells. A comparison of the coupling to a line with matched loads suggested that neglecting the microstrip losses only introduce a slight,

Table 2.5: Measurement and modelling of non-idealities in section 2.6.

measurement	modelled non-ideality	error average	error avg. abs.	error visual
1-segment	–	−1.81 dB	2.63 dB	
	permittivity	−1.52 dB	2.79 dB	problems > 10 GHz
	GTEM refl.	−1.75 dB	2.60 dB	good match oscillations
3-segment	GTEM refl.	−1.53 dB	2.85 dB	
3-segm. shorted	GTEM refl.	−0.22 dB	2.13 dB	
3-segm. probed	GTEM refl.	−1.75 dB	4.02 dB	
7-segment	–	−0.05 dB	2.07 dB	

pessimistic error. Therefore, and to simplify, trace losses are neglected from there on out. To promote experimentation and to enable practical application, the meshing was successfully automated and the terminal voltages were predicted using Kron's formalism. By frequency-adaptive meshing of the trace, an order of a magnitude speedup was achieved. A sensitivity study suggest that meshing finer than $\lambda/20$ is a waste of time. All the same, these numerical solutions do not provide understanding.

Therefore, the single Taylor cell was modified to remain valid for high frequencies, at least for grazing-incident, vertically polarised plane wave incident on a microstrip trace segment with matched loads. This modified Taylor cell consists of Taylor's cell, which predicts the low-frequency coupling, and the cross-correlation K between the incident wave and the line's eigenwave. More importantly than another order of a magnitude speedup, this model yields understanding. From the modified Taylor cell, it can be understood that for low frequencies, the electric and magnetic coupling add up constructively at the trace's near end under end-fire illumination. Consistent with Leone, the latter illumination constitutes the worst case. In this case, trace length and substrate thickness are the design parameters that proportionally determine the low-frequency coupling. For high frequencies, the worst case occurs at the far end, because the incident- and the eigenwave are aligned, yielding a maximum K. In that case, only the substrate thickness determines the worst-case coupling, and not the trace length.

By superposing one modified Taylor cell per segment, the coupling to multi-segment traces can be predicted. By applying transmission line theory, predictions for arbitrary loads can be calculated analytically. The worst case was also studied as function of the terminal loads and a loose upper bound was found. Not surprisingly, the better both terminal impedances are matched to the trace, the smaller the either-end voltages are. It be noted that the trace impedance may also be tuned for given terminal impedances.

Full-wave simulation of the case studies used above correspond very well to the predictions obtained with the modified Taylor cell. Apparently, the transmission line

assumption inherent to the (modified) Taylor cell holds, even for segmented traces. Also, the approximation of the substrate field seems to work.

In comparison with GTEM cell measurements, it turned out redundant to measure and take into account the substrate permittivity. It was useful, however, to take into account the first GTEM cell's reflection. Even then, about 1.3 dB more coupling is observed with the GTEM cell than with the modified Taylor cell or with full-wave simulation. Therefore, it is supposedly due to a non-ideality of the GTEM cell that is not taken into account by either model. Averaged over the different case studies, an average absolute error of 2.7 dB was found. The transparent upper bound found from the modified Taylor model was respected.

With the obtained transparent model, EMC-aware PCB designers can make informed design decisions. For example, for a weak analog signal, the maximum trace length and substrate thickness can be calculated early in the design process, just from the field strength that the PCB must be compliant with. For another example, the designer knows that at high frequencies, it may be a waste of time to shorten the trace to improve the PCB radiated immunity. As a last example, the trace width of a sensitive signal may be tuned to be in between both terminal impedances in order to reduce EMC risks. The latter is a 'free' EMI countermeasure. Because the modified Taylor model is closed-form, field-to-trace coupling of a given trace can be predicted in the order of tens of milliseconds.

The transparent models are also of use for testing. For example, in pre-compliance testing of a prototype with a sensitive trace, the engineer can immediately perform end-fire illumination at either end, instead of having to rotate the Device Under Test (DUT).

In future research, the illumination should be generalised to arbitrarily-polarised, arbitrarily-incident plane waves, because in reality, perturbing electromagnetic fields are unknown. Considering the worst case and taking loose upper bounds may help to keep the expressions transparent.

CHAPTER 3

IC Conducted Immunity

Abstract. If the conducted immunity of ICs is interesting above 1 GHz, a measurement method is needed that is valid beyond 1 GHz. There is no standardised method yet, because with rising frequency, the common measurement set-up increasingly obscures the IC's immunity. An attempt to model and remove the set-up's impact on the measurement result proved difficult. Therefore, a simplified set-up and extraction method is proposed and a proof-of-concept of the automatic generation of the set-up's PCB is given. The conducted immunity of an LM7805 voltage regulator is measured up to 4.2 GHz to demonstrate the method.

3.1 Introduction

What is the conducted immunity of ICs beyond 1 GHz? How to obtain models for IC conducted immunity that are valid beyond 1 GHz? Can this be done efficiently in an industrial context?

Because of the prototyping cost and delay, PCB designers strive for First-Time-Right (FTR) EMC compliance. PCB-level designers decide on placing and routing of ICs and various electronic and electromechanical components. The designer understands the routed traces that connect the components, so the transparent model for field-to-trace-coupling developed in Chapter 2 might be of use to them. The ICs, however, are black boxes to the PCB designer, which just fulfil certain functions. Therefore, opaque models of the involved ICs suffice for PCB-level design and simulation.

If conduction remains the dominant perturbation mechanism beyond 1 GHz, models are needed that are descriptive of the conducted immunity of ICs beyond 1 GHz. To underpin this thesis' main hypothesis (cf. p. 9), a *possible* technique should be demonstrated to obtain these models. The modelling technique should be applicable in an industrial context, valid for a wide range of ICs and produce models that allow for

PCB-level simulations.

To that end, the existing models and modelling techniques for conducted IC immunity will be reviewed in section 3.2, to conclude that no standardised method beyond 1 GHz currently exists. A first attempt to extend the current state of the art in black-box modelling beyond 1 GHz consists in modelling the passive components used in its measurement technique beyond 1 GHz, as will be documented in section 3.3. It will turn out that its passive components are not always needed, and that there are other effects that need to be taken into account. Therefore, a 'lean extraction PCB' approach will be elaborated from the ground up in section 3.4. This approach will be applied to general SOIC8-packaged ICs by semi-automatically generating an extraction board in section 3.5. Using this board, one IC will be modelled in section 3.6: the LM7805 voltage regulator. Conclusions will be drawn in section 3.7.

3.2 State of the Art

With the keywords of the goal mentioned above in mind, published IC conducted immunity models were inspected with the following questions:

1 'wide range of ICs': What range of ICs are modelled? From a single transistor to an A/D-converter, a CPU or a television SoC?
2 'black box': What kind of model is used and why?
3 'modelling technique': What measurement and simulation techniques are used to obtain these models?
4 'competent models': What prediction is accurate enough? Should the output of the model be boolean (pass/fail) or continuous (DC offset voltage, RF disturbance propagation)?
5 'beyond 1 GHz bandwidth': What bandwidth is modelled for and why?

The results are enumerated in Table 3.1. If the publication mentions the initial modelling goal (to aid the IC, PCB- or equipment designer), it is marked in the table.

As for the range of modelled components, the least complex component was found to be a single transistor, ranging up to A/D converters and the I/O buffers of a microcontroller. In view of the complexity of contemporary SoCs, this range is rather modest. Few examples were found of the integration of these models in a greater whole.

Often, authors do not document their choice for a black, white or grey box. However, the modelling goal is briefly mentioned in most publications. Not surprisingly, the modelling goal correlates with the modelling depth (black-, white- or grey box). That is, research targeting IC designers creates white-box models, which explain the integrated circuit's susceptibility root cause. Research targeting PCB or equipment designers, on

Table 3.1: Literature study results for IC conducted immunity models.

publication		modelant		model			
year	ref.	component	bandwidth	goal ↓	colour	output	technique
2010	[58]	current mirror	0–10 GHz	IC	white	voltage	simulation
2010	[58]	LIN driver	0.05–12 MHz	IC	white	pass/fail	simulation
2010	[58]	ring oscillator	1–7.7 GHz	IC	white	jitter	simulation
2010	[58]	4-bit adder	40MHz	IC	white	pass/fail	simulation
2009	[59]	ADC	1 kHz–1 GHz	IC	white	pass/fail	simulation, ICIM-CI
2002	[60]	op-amp	0–1 GHz	IC?	white	voltage	analysis-measurement
2002	[61]	CMOS op-amp	0–2 GHz	IC?	white	voltage	analysis-measurement
2010	[62]	ADC	0.1–10 MHz	IC?	grey	pass/fail	DPI
2009	[63]	μC with ADC	0–0.6 GHz	IC/PCB	grey	EFT shape	VNA
2007	[64]	μC input buffer	0.01–2 GHz	IC/PCB	grey	pass/fail	sim., measurement, DPI
2010	[65]	op-amp	5–100 MHz	PCB	grey	voltage	analysis, DDPI, VNA
2010	[66]	FlexRay tranceiver	1–200 MHz	PCB	grey	pass/fail	DPI, BCI
2013	[67]	74LS inverter	0–1 GHz	?	grey	pass/fail	DPI, VNA, ICIM-CI
2013	[68]	EEPROM memories	1 MHz–1 GHz	PCB?	black	pass/fail	DPI, VNA, ICIM-CI
2009	[69]	various	1 MHz–1 GHz	PCB	black	pass/fail	DPI, VNA, ICIM-CI
2008	[70]	CMOS inverter	0.05–1 GHz	PCB	black	voltage	DPI, NNs
1978	[71]	74xx, opamp, 7805	0.01–10 GHz	equipment	black	p/f, voltage	DPI
2000	[72]	"	"	"	"	"	
2013	[73]	LDO	1–18 GHz	PCB?	black	pass/fail	DPI

the other hand, do not need or want to understand the inner workings of the IC, but just predict how it will contribute to the susceptibility of the PCB or equipment.

One clear industrial advantage of black-box models is the protection of IP. That is, detailed knowledge of an IC's internals allows counterfeiting. A descriptive behavioural model, on the contrary, would allow IC manufacturers to publish the immunity of their products without disclosing precious know-how.

Loeckx showed another motivation for black-box modelling [58]. Even though he had all information about the IC and of accurate interconnect models, he was barely able to predict the DPI behaviour, because of the computationally complex simulation. Although he found a hierarchical method to generate fast behavioural models, this is indicative of the difficulty in creating white-box models.

For these reasons, black-box models seem most practical for the needs of the industrial PCB designer.

The modelling techniques employed are mathematical analysis, circuit-level simulation and measurement. These correspond roughly to white-, grey- and black-box resulting models. Not all authors go all the way from analysis, simulation or measurement to a formalised immunity model. Actually, the only formalised black-box IC immunity model is called Integrated Circuit Immunity Model for Conducted Immunity (ICIM-CI) and is currently in the process of standardisation as IEC 62433-4 [74]. This standard and its data exchange format Conducted Immunity Markup Language (CIML) should promote exchange of immunity models, as illustrated in Figure 3.1. The model predicts functional failure of an IC under CW disturbances entering the IC pins. To do so, the model consists of a Passive Distribution Network (PDN) and an Immunity Behaviour (IB) part as schematised in Figure 3.2.

In the standardisation discussions at time of writing, the PDN is a linear multiport, of which every port represents a ground-referenced IC pin. Using the PDN, the reflected and transmitted power can be calculated, given a forward power. At some forward power, all IC pins start to exhibit considerable non-linear behaviour (like all physical systems do), chiefly due to ESD protection diodes. This challenges the model validity of a linear PDN. However, as long as failure always occurs at power levels where the IC still can be considered linear, the linear PDN is a competent model. 'Can be considered' means that the model yields system level immunity predictions that are accurate enough. Depending on the definition of 'failure' and 'accurate enough', this *linearity hypothesis* on which the ICIM-CI model depends, may be valid or invalid.

The IB commonly consists of a look-up table for every port that yields a transmitted power threshold as function of the disturbance frequency. If the transmitted power through any port exceeds the threshold, the IC is predicted to fail altogether. Other immunity behaviours are envisaged in IEC 62132-4 as well, where a scalar performance metric (like DC offset or jitter) is returned. An ICIM-CI model is a black box itself, but it may be extracted from (white-box) integrated circuit simulations. The PDN can be completely described with S-parameters, which can be measured using a VNA. The

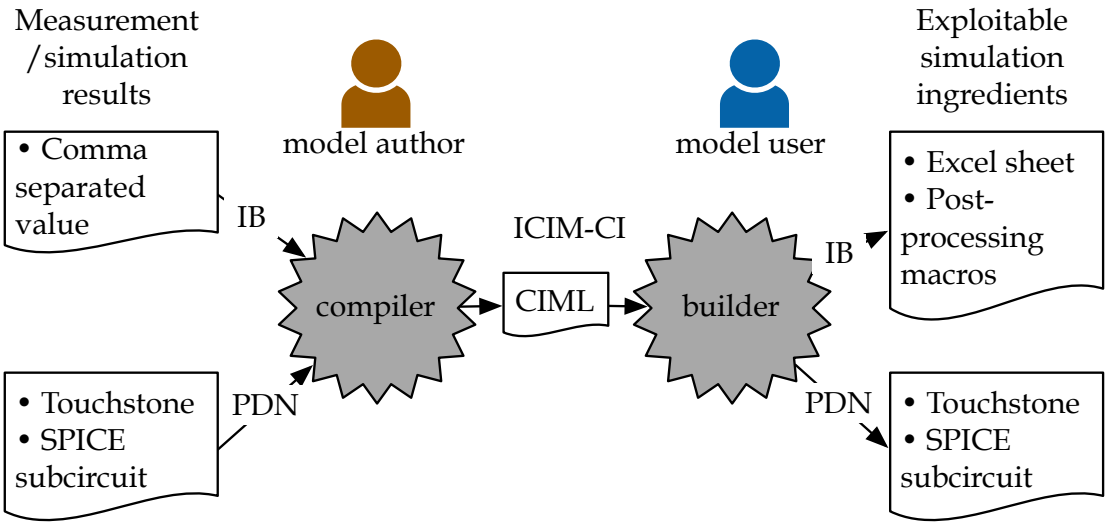


Figure 3.1: Schematic use case of a single-file ICIM-CI standard.

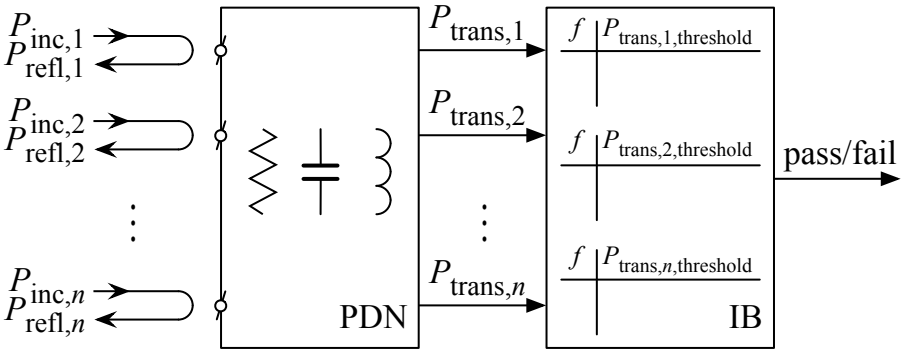


Figure 3.2: Symbolic representation of the ICIM-CI of IEC 62433-4. In this case, the IB just returns a boolean pass/fail signal, based on transmitted power threshold lookup tables.

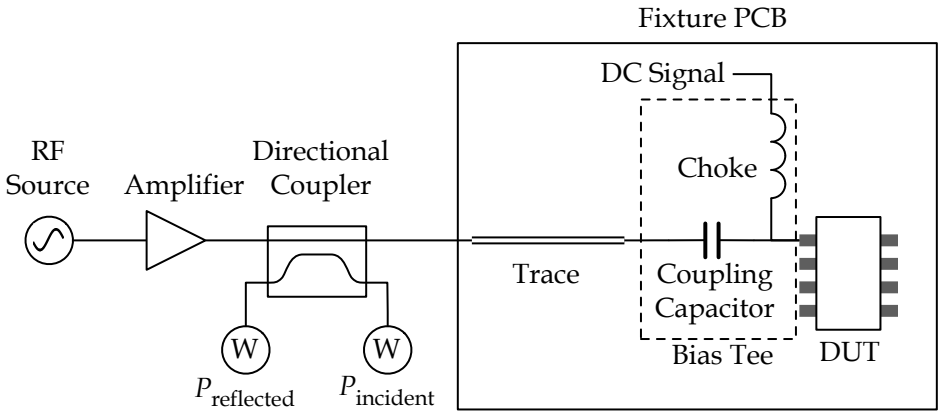


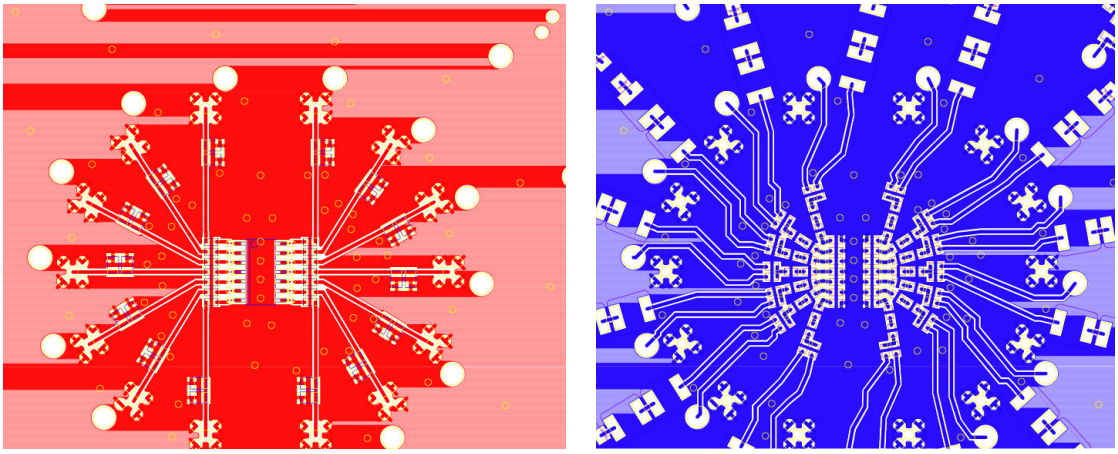
Figure 3.3: RF injection path of the DPI set-up proposed in IEC 62132-4.

difficulty lies in moving the reference plane to the IC pins.

The IB's transmitted power threshold can be extracted from measurement using the DPI set-up described in IEC 62132-4. Its goal is to characterise the susceptibility of an IC to conducted disturbances, while reducing the influence of the particular test set-up on the measurement results. The set-up proposed by IEC 62132-4 [75] is shown in Figure 3.3: it consists of a PCB with the Device Under Test (DUT) and some peripherals, and a directional coupler that allows for measuring the incident and reflected power. That is, for every frequency, the forward power is increased until the IC fails according. The definition of failure needs to be given elsewhere, and a suitable technique for observing failure needs to be applied. At the point of failure, the difference $P_{\text{fwd}} - P_{\text{refl}} = P_{\text{trans}}$ is taken to be the power really dissipated by the IC.

The most difficult part is injecting a known RF disturbance power into the IC pin under test. Mathematically, the differential power measurement yields the net power leaving the directional coupler output. Although it is not common terminology in DPI, this is the transmitted power at the reference plane of the coupler output. Recall that the ICIM-CI reference plane should lie at the Pin Under Test (PUT) boundary. Therefore, recording the differential power measurement as the IB is legitimate to the extent that the cabling and on-PCB loss is negligible. For that reason, the standard requires the insertion loss not to exceed 3 dB [75, §7.4]. That way, the coupler output and PUT reference planes are numerically close.

The great advantage of this approach is that it is simple: one can design a PCB with all necessary periphery, measure incident and reflected power when the DUT fails and register the difference as being $P_{\text{trans,threshold}}$. However, two critical remarks on the accuracy of the method can be made. First of all, when the PUT is very reflective, $P_{\text{fwd}} \approx P_{\text{refl}}$ and the wattmetre errors dominate the P_{trans} reading [71, p. 112]. In practical cases, in the $1 - 3$ GHz range, the difference between the true and the measured P_{trans} can go down to -10 dB [76].



(a) Component- and RF perturbation side. (b) Peripheral- and functional side.

Figure 3.4: Generic SOIC14 extraction PCB as developed at Valeo's (image courtesy Frédéric Lafon).

Therefore, an improvement upon both inaccuracies was proposed earlier by Lafon [69]. The measurement set-up can be the same as in Figure 3.3, in this proposal, however, only the forward power P_{fwd} at failure will be recorded. To obtain the transmitted power P_{trans}, all of the set-up is modelled in SPICE, then simulated with the recorded forward power $P_{\text{fwd,threshold}}$, and the transmitted power $P_{\text{trans,threshold}}$ is calculated. Put differently, the reference plane is moved from generator output to DUT pin by simulation.

Practically, the used extraction PCB is generic for a particular package (SOIC14, in the example of Figure 3.4), and has almost the same and well-known layout for each pin. The layout allows to solder bias tees and other peripheral circuitry for every pin. Passive components that make up the bias tees are separately measured, modelled and entered in the simulation. The DUT is modelled by measuring its *S*-parameters with a VNA, after calibrating using a custom Short-Open-Load (SOL) calibration PCB that moves the reference plane up to the DUT pins for the *S*-parameter measurement. Finally the *S*-parameters are converted to a SPICE model with IdEM [77].

The bandwidth of most models is limited to 2 GHz. There are exceptions: Chang et al. measured at 18 GHz, but they do not explicitly define the RF reference plane [73]. Judging from their extraction PCB layout, the reference plane not very representative. Similarly, the McDonnell Company measured up to 10 GHz at the SMA reference plane of connectorised bias tees, relying on striplines and Zero Insertion Force (ZIF) sockets to have negligible insertion loss, it seems [71]. Lafon measures up to 3 GHz and remarks that with rising frequency, the mutual inductance of DPI capacitors becomes non-negligible and needs to be modeled [27].

Maybe it is for these practical difficulties that there is no standardised measurement method beyond 1 GHz; IEC 62132-4 is defined up to 1 GHz. The different attempts, however, show a popular trend towards higher frequencies [8].

To summarise, since the 1980's, people have tried to construct some more or less standardised descriptive models of conducted IC immunity up to 10 GHz. Depending on the modelling goal (e.g. predict system immunity or improve IC immunity) the models were more or less explanatory (e.g. black-box or white-box). The most standardised model to date is ICIM-CI, which can be extracted by VNA and DPI measurements on ICs. The DPI exhibits accuracy problems for rising frequency, something for which Lafon proposed an alternative. However, this alternative still requires careful modelling of the set-up. In general, authors and committees are unclear about the definition of reference planes. For these and other reasons, we consider there is no standardised black-box modeling technique beyond 1 GHz.

3.3 Modelling passive components

The hardware set-up prescribed in IEC 62132-4 comprises on-PCB decoupling networks, that is, DC-blocks and bias tees [75]. We would like to assess the feasibility of a similar set-up for frequencies beyond 1 GHz. These decoupling networks consist of discrete components like capacitors, inductors and resistors and PCB traces. Models of traces are readily available and can be simulated with tools like ADS. Discrete component models can be bought from specialists like Modelithics, Inc., and sometimes they are supplied by the component manufacturer.

In the latter case, however, it is not always clear whether and how the models include the PCB layout [78] and how element values vary as result of production tolerances [79]. To verify the manufacturer's models, we would like to model the components ourselves by means of measurement. Commercial SMD test fixtures like Agilent's 16196 allow measuring SMDs up to 3 GHz, for about 5 k€ [80]. Furthermore, one needs an impedance analyser that can measure up to 3 GHz.

Attempting to find a cheaper solution, while gaining experience with PCB design for 10 GHz, we decided to design a test fixture ourselves. This attempt to find a cheap and simple solution also suggests to use standard measurement equipment. That is, instead of a somewhat special impedance analyser, we would like to use a network analyser, which is present in virtually any EMC laboratory. Nonetheless, the analyser's frequency range should encompass at least the resonance frequency of the DUT. We use the HP 8720C VNA at hand, which has a frequency range of 50 MHz–20.05 GHz.

Therefore, a typical case study that is useful for the DPI set-up will be defined. For that case, a measurement fixture will be designed. The case study will then be measured with the fixture, yielding raw impedance data. Different ways of compensating these data for

Table 3.2: Frequency-dependent behaviour of AVX 1 pF U-series NP0 chip capacitors, copied and extrapolated from [81].

package		behaviour	
JEDEC	metric	resonance	ESR @ resonance
0402	1.0×0.5 mm	8.3 GHz	0.15 Ω
0603	1.6×0.8 mm	7.9 GHz	0.2 Ω
0805	2.0×1.25 mm	7.2 GHz	0.3 Ω
1210	3.2×2.5 mm	6.3 GHz	0.2 Ω

the fixture influence will then be compared. Consequently, a preferred compensation method will be concluded upon, as well as the fixture performance.

Case Study

To assess the test fixture, we chose a capacitor that is candidate for Gigahertz Direct Power Injection (GDPI) set-ups: a 1 pF microwave capacitor from AVX. This capacitor is available in JEDEC 0402, 0603, 0805 and 1210 packages. We chose the 0603, trying to strike the balance between a high resonance frequency and the mechanical reproducibility of the measurements. The 0603-packaged capacitor allegedly resonates at 8 GHz with an Equivalent Series Resistance (ESR) of 0.2 Ω at resonance (cf. Table 3.2). No tolerance nor reference planes are specified, however.

Design

The two-terminal (one-port) DUT needs to be connected somehow to a two-port VNA. Hence, there is essentially only one measurement configuration when using one VNA port, cf. Figure 3.5a. With two ports, there are essentially two possible configurations,[1] shunt and series, cf. Figure 3.5b-c. From symmetry, we deduce that $S_{11} = S_{22}$ and $S_{21} = S_{12}$, so there are two interesting S-parameters per configuration. This gives us five quantities that can be measured with a VNA: the (one-port) reflection coefficient, the series S_{11}, the series S_{21}, the shunt S_{11} and the shunt S_{21}. Due to the measurement principle of the VNA, the impedance thus measured is more or less precise. The 10% uncertainty of impedance magnitude is shown in Figure 3.6.

The most interesting impedance region of measurement will be around the resonance. One frequency decade under its nominal resonant frequency of 8 GHz, the

[1] In bond graph terminology, one can prove that there are only two junctions that do not dissipate nor store energy: the 0-junction and the 1-junction. The former corresponds with a parallel circuit, the latter with a series circuit.

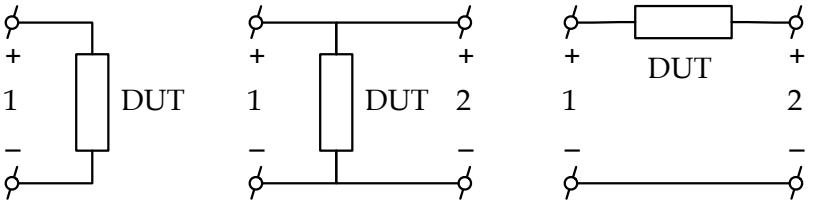


Figure 3.5: All possible ways to connect a DUT to one and two ports: (a) reflection, (b) shunt and (c) series.

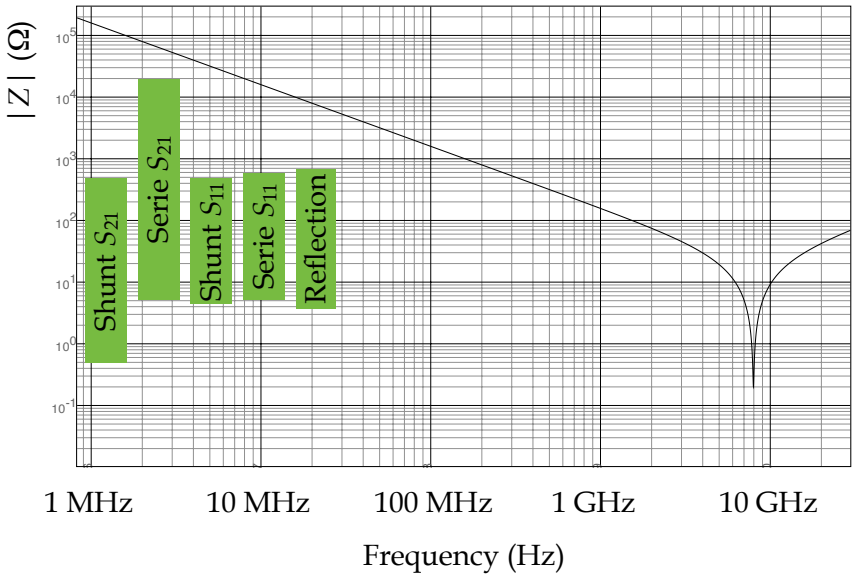


Figure 3.6: Theoretical impedance magnitude of the nominal AVX U-series 10 pF capacitor. The impedance intervals of 10% uncertainty are given for a best-of-class VNA [82].

impedance of 1 pF is as high as 199 jΩ. At resonance, the impedance is the nominal ESR of 0.2 Ω. This 200 mΩ–200 Ω range pleads for a S_{21} shunt configuration. However, for ease of measurement and calibration, we would like to try the 'reflection' configuration, which should allow us to at least estimate the equivalent C and L of the DUT. We accept beforehand that we will not be able to accurately measure the ESR.

The fixture should allow for a reproducible and compact connection between the connector and the DUT up to about 10 GHz. For robustness, an SMA connector was selected.

Commonly, board-edge end-launch SMA connectors are used for experimental setups, their advantage over thru-hole connectors being a straight waveguide transition without stubs. For example, the Emerson Johnson® 26.5 GHz end-launch SMA con-

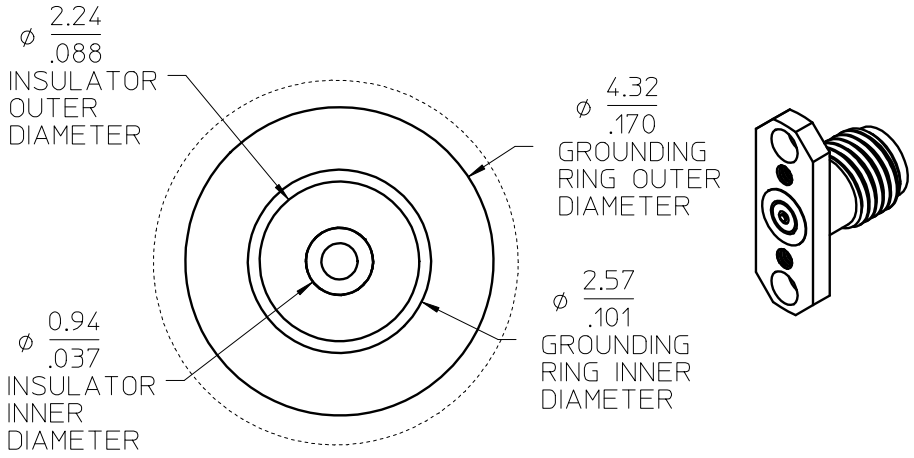


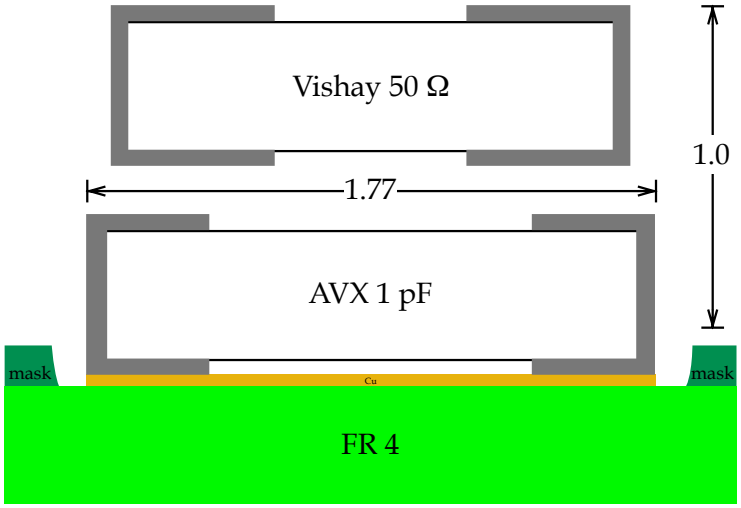
Figure 3.7: Bottom and perspective view of the Molex SD-73251-185 27 GHz SMA connector. Dimensions are in mm/inch. [84]

nector [83], which is slid on the PCB edge and soldered to a microstrip or Grounded CoPlanar Wave-guide (GCPW) waveguide. A disadvantage of this connector may be, that the DUT will be mounted at about 6 mm from the board edge, to allow the ground lugs of the connector to be properly soldered and not generate too much parasitic capacitance. Furthermore, the connector is dimensioned for GCPWs on high-frequency substrates, which makes the necessary PCB more expensive and difficult to order.

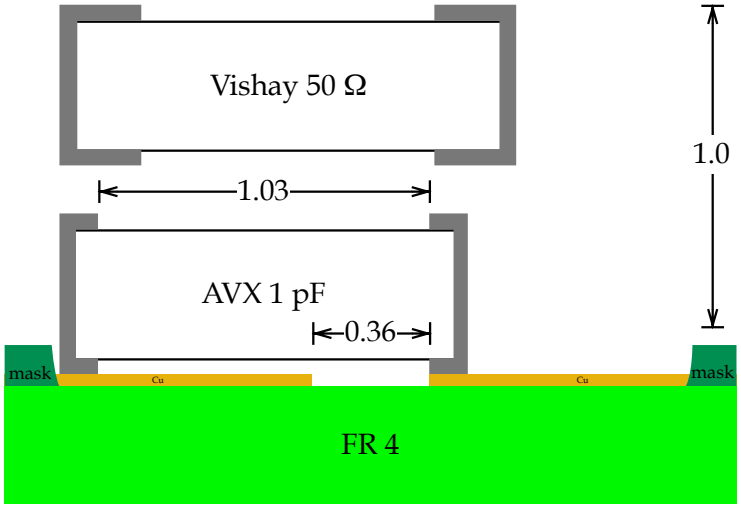
Therefore, Molex Incorporated advised us to use their SD-73251-185 SMA connector (cf. Figure 3.7). This 27 GHz SMA connector is screwed onto the PCB, instead of soldered [84]. A ring of 'bolt' vias and one central via emulate a coaxial connection through the board. Allegedly, low insertion losses can be achieved with well-designed transitions [85]. As the wave only traverses the thickness of the lossy board (1.5 mm, typically), an Flame Retardant 4 (FR4) substrate might suffice. If so, the board becomes cheaper and easier to order with respect to an RF substrate.

On the other side of the board, the DUT will be clamped between the central via and the bolt vias, thus creating a non-coaxial fixture [86], i.e. the fixture is not point-symmetric around the connector's axis. Like in commercial fixtures, the DUT will not be soldered, but contacted using a spring. This avoids measuring the unknown parasitics introduced by the solder joint. Furthermore, a PCB will wear by repeated soldering and desoldering. To increase life time, gold plated pads are used. The total assembly is illustrated in Figure 3.9.

The DUT footprint was chosen such, that the case study capacitor and a precision 50 Ω resistor [87] fit. The rectangular soldermask gap on top of the PCB helps the



(a) Choice of total path length. Longest capacitor and resistor, according to their specified production tolerances, with the largest wraparound electrodes.

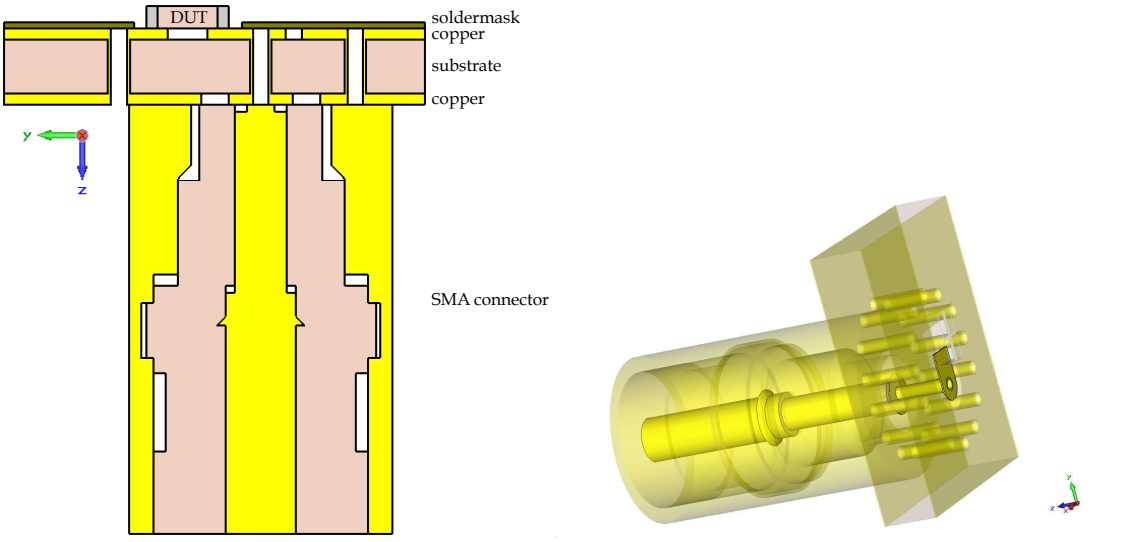


(b) Choice of gap width. Shortest capacitor and resistor, according to their specified production tolerances, with the smallest wraparound electrodes.

Figure 3.8: Lengthwise design of the DUT footprint. All dimensions in mm.

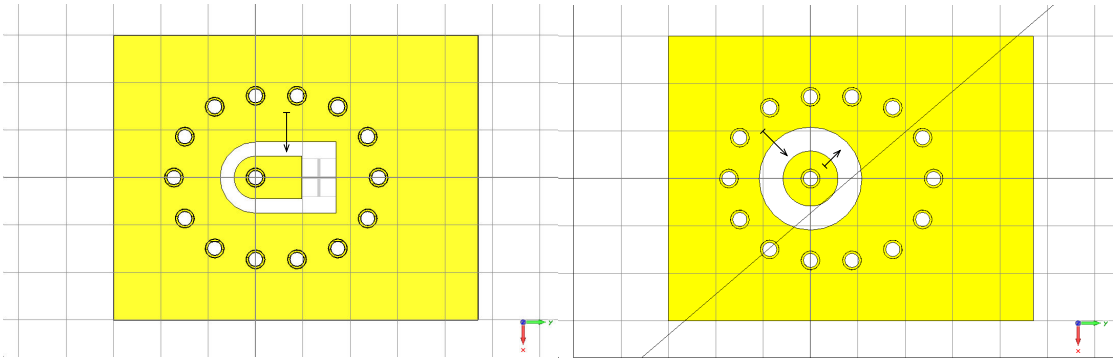
operator to align the DUT. By taking the minima and maxima of both DUT mechanical tolerances, the footprint was designed, as illustrated in Figure 3.8.

To optimise the transition from SMA connector to footprint, the Molex-supplied 3D model of the SMA connector was entered into CST. A small PCB was on put on top, based on the SMA's nominal footprint [84], Molex' example design [85] (8 bolt vias of 12 mil) and the standard Eurocircuits 2-layer build-up [23]. For the SMD, we used the



(a) Cross section, not to scale. (b) Central conductor and pads are highlighted.

Figure 3.9: Overview of the fixture.



(a) DUT side of the PCB. (b) SMA side of the PCB.

Figure 3.10: Optimised PCB layout of the fixture (grid size 1 mm). The arrows indicate the degrees of freedom.

footprint designed above.

The performance was evaluated by the fixture's S-parameters. That is, an ideal fixture only introduces an electrical delay and no losses: $|S_{11}| = -\infty$ dB and $|S_{21}| = 0$ dB. The remaining degrees of freedom in PCB layout were the outer and inner diameter of the ground contact and the ground plane clearance of the SMD footprint. These three design parameters were swept within the limitations of manufacturability in order to obtain a low and smooth S_{11} and a high and smooth S_{21}. The resulting layout is presented in Figure 3.10.

After this optimisation, two other uncertain parameters were identified: DUT placement and substrate permittivity. The sensitivity for DUT placement was studied by translating and rotating the nominal DUT within the solder mask gap. The effect of the substrate permittivity was studied by sweeping the permittivity ε_r between 3.9 and 4.9 for the nominal DUT placement. As can be seen in Figure 3.11, the fixture performance remains rather stable.

The fixture was fabricated in the standard 2-layer Eurocircuits process. The PCB was cleaned with 70% IPA and the SMA connector was screwed-on hand-tight, in lack of a 0.09 Nm torque limited screwdriver. A stainless-steel bow with a nylon M3 screw was mounted to keep the DUT in place. Two white LEDs were added to mitigate the shadow cast by the bow. Using a jeweler's magnifying glass, the alignment can now be properly inspected.

The SMA connector was connected to the first port of an HP 8720C VNA (50 MHz–20 GHz) with a semi-rigid SMA 90° bend. The resulting set-up is depicted in Figure 3.12.

Compensation

Raw measurements taken with this fixture now need to be compensated for the fixture's presence. Three compensation methods will now be explained and applied.

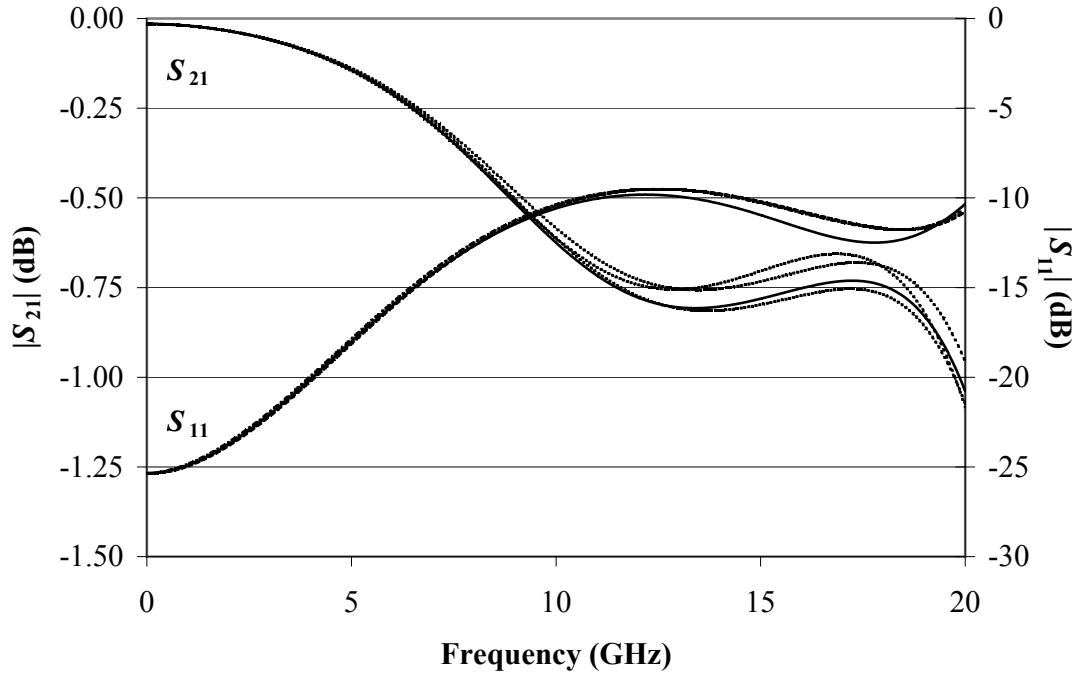
The simplest compensation consists in subtracting an electrical delay from the measurement results.

That is, the fixture is considered a lossless, characteristic transmission line ($Z_0 = 50\,\Omega$), just described by a propagation delay τ_d. To apply this compensation, we proceed as follows. First, a SOL calibration with an Agilent 85052D 3.5 mm calibration kit is performed on the VNA to shift the reference plane to the end of the SMA elbow. The S_{11} parameter of the fixture without DUT is then measured and an open stub is fitted to the result.

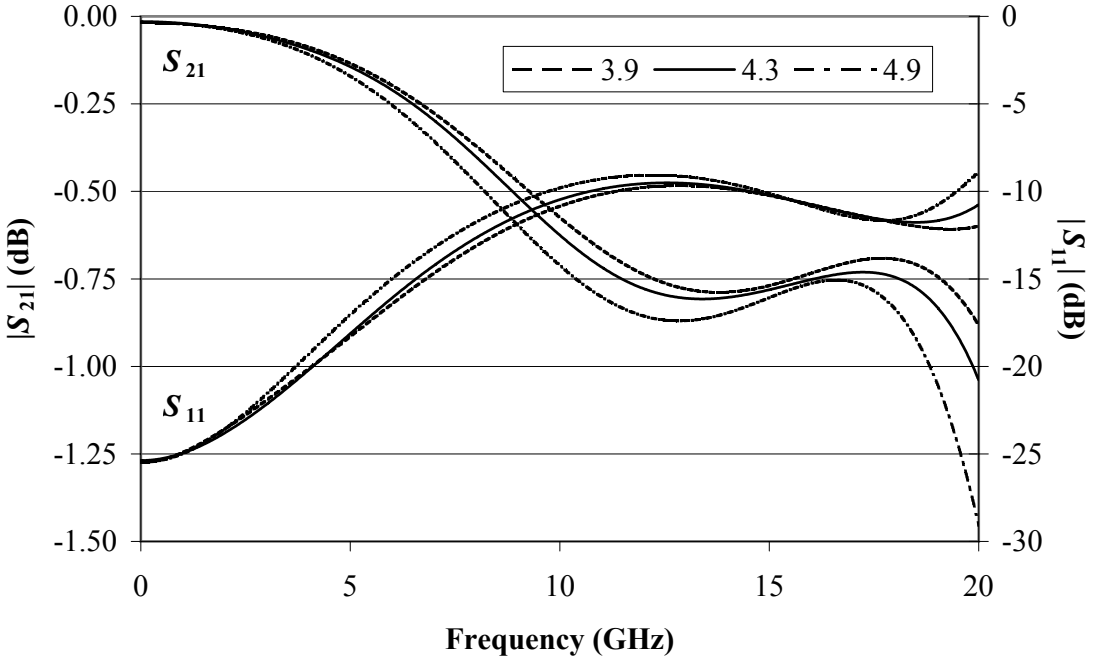
The Agilent 85052D 3.5 mm calibration kit is valid up to 26.5 GHz [88], but the fixture-without-DUT will be capacitive. Therefore, we manually fitted the τ_d more to the low than to the high frequencies and obtained 53 ps, as can be seen in Figure 3.13.

A slightly more advanced compensation consist in using the CST-simulated S-parameters of the fixture to de-embed the DUT from the fixture.

Apply this compensation, the VNA was again calibrated up to the SMA reference plane. We then de-embed the DUT from the fixture in Agilent's Advanced Design System (ADS), as shown in Figure 3.14. However, the compensated 1 pF case study thus obtained stays capacitive until 20.05 GHz, as if the compensated fixture is too short. When we de-embed an 'open' measurement in the same way, we need to add 8 ps electrical delay to obtain $\angle S_{11} = 0° \pm 4°$ up to 8 GHz.



(a) Sensitivity to DUT placement offset. Solid curve shows the response at the nominal DUT position. Non-solid curves show the response for $\Delta x = +0.1\,\text{mm}$, $\Delta y = \pm 0.2\,\text{mm}$ and $\Delta\theta = +10°$.



(b) Sensitivity to substrate permittivity.

Figure 3.11: Sensitivity study in simulation of the fixture's *S*-parameters. The linear frequency scale reveals GHz issues. The solid line consequently represents the nominal case.

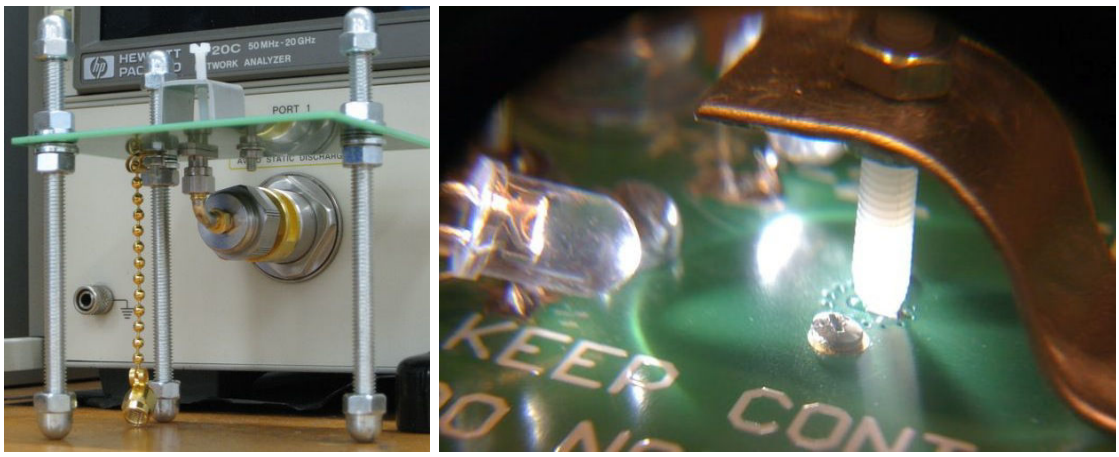


Figure 3.12: Measurement set-up. (a) Overview: PCB with HP 8720C VNA. (b) Detail: spring-loaded nylon bolt keeps the DUT in place.

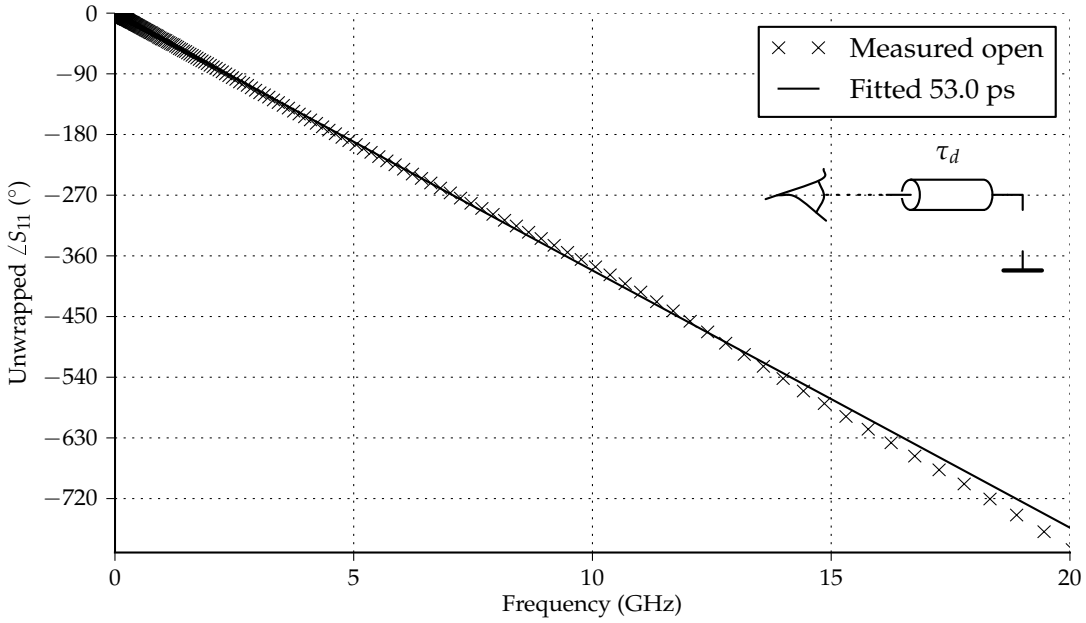


Figure 3.13: Open measurement with fitted stub

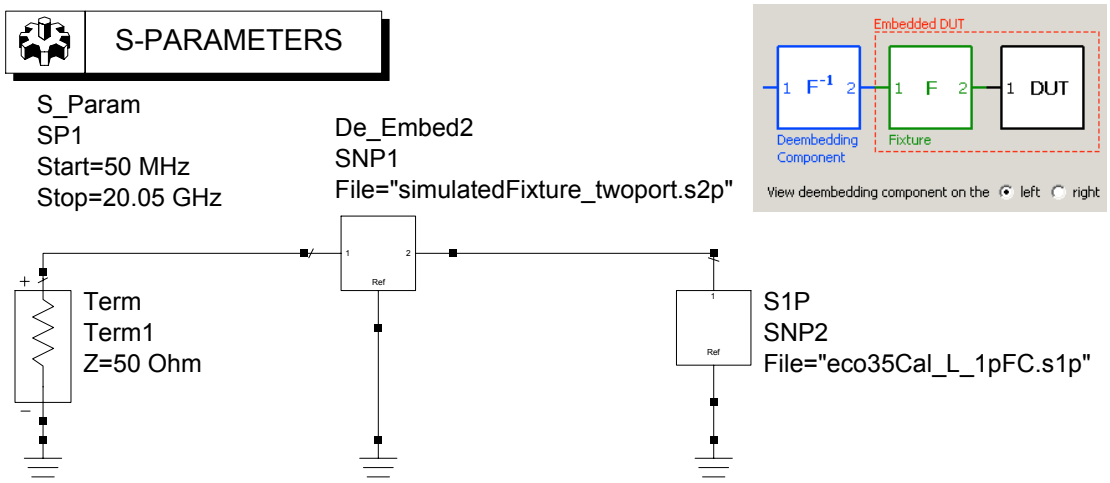


Figure 3.14: The de-embedding network under ADS.

Without understanding this 8 ps or 1.6 mm (at $2/3c$) shortcoming of the CST simulation, we will use the de-embedding anyhow in the comparison, and systematically add 8 ps.

Finally, a SOL calibration can be used, based on standard measurements and their short- open- and load ideals.

As short standard, we measure a polished $1.52 \times 0.75 \times 0.5$ mm brick of 750‰ Au to mimic the nominal size of the 0603 load used. Because of the gold contacts, its main imperfection is supposed to be its non-zero inductance. The ideal model should therefore at least model this inductance.

Inductance is the capability of electric current flowing in a closed loop to generate a magnetic flux. Regarding this capability as linear, inductance is measured in $\mathrm{H} \equiv \mathrm{WbA}$. The value of this self-inductance thus depends on our choice of the subspace over which we integrate the magnetic flux density caused by 1 A of current. It is not obvious over what subspace to integrate the self-inductance of our short-circuit. Furthermore, the current density will not be uniform over our brick volume, and not even over its faces, due to the combination of the skin effect and Joule[2] heating. In gold, the crossover frequency where the equivalent radius 0.25 mm is twice the skin depth equals 0.36 MHz [10]. Therefore, the current density in the brick will be considered zero, as will be the magnetic flux density.

Rosa calculates the self-inductance of a bar with a rectangular cross-section by integrating the magnetic flux density between the planes touching the bar's end faces

[2]After James Prescott Joule (1818–1889).

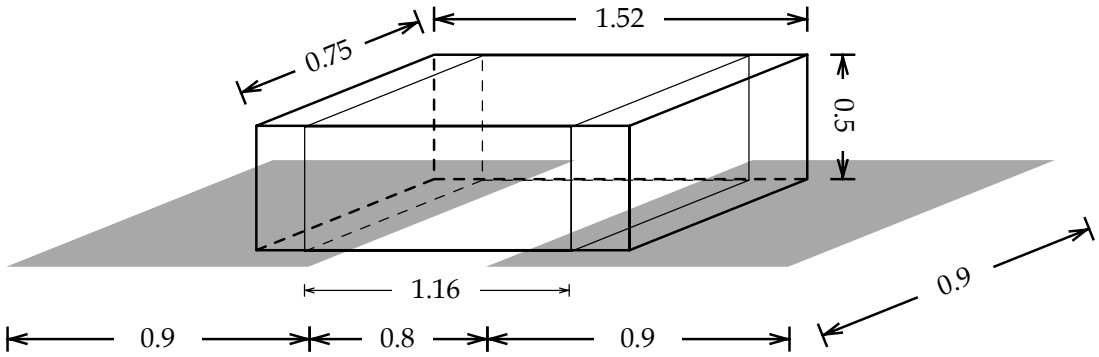


Figure 3.15: Rectangular bar model of the golden brick. The bar is a little shorter to incorporate the current that will enter the brick halfway the brick-pad overlap.

[89]. He seems to suppose a uniform current distribution [90] and finds:

$$L_{\text{tot}} \approx \frac{\mu_0}{2\pi}\ell\left[\ln\left(\frac{2\ell}{w+h}\right)+\frac{1}{2}+0.2235\frac{w+h}{\ell}\right], \tag{3.1}$$

where ℓ, w and h are the length, width and height of the bar, respectively. To get rid of the internal inductance, we subtract the radius independent, 0.05-nHmm^{-1} internal inductance of a round wire [10]:

$$L_{\text{ext}} \approx \frac{\mu_0}{2\pi}\ell\left[\ln\left(\frac{2\ell}{w+h}\right)+\frac{1}{2}+0.2235\frac{w+h}{\ell}-\frac{\mu}{4}\right]. \tag{3.2}$$

We assume that the current effectively enters the brick halfway the pad-brick overlap, cf. Figure 3.15. The brick will therefore have an effective length of $0.8+(1.52-0.8)/2 = 1.16$ mm. We plug the values into (3.2) and obtain:

$$L_{\text{ext}} \approx \frac{4\pi\times10^{-7}}{2\pi}1.16\times10^{-3}\left[\ln\left(\frac{2\cdot1.16}{0.76+0.5}\right)+\frac{1}{2}+0.2235\frac{0.76+0.5}{1.16}-\frac{1}{4}\right]\approx 0.26\,\text{nH}. \tag{3.3}$$

As for the open circuit, it should approximate a DUT of infinite impedance ($\infty\,\Omega$), so we just do not place any DUT. This way, only dust or grease in the 0.8 mm gap between the patches could provide an ohmic path. Normally, this will be in the order of MΩs.

Of course there will be stray capacitance between the conductor pad and the ground plane around. Insofar as this stray capacitance will also be there with a DUT in place, this is good, because the open circuit calibration will allow the VNA to compensate the stray capacitance. The stray capacitance at the place of the DUT however, will be replaced by the DUT, so it should not be compensated. Therefore, it should be considered part of the standard.

Let us estimate the stray capacitance through the air that will be replaced by the DUT. We suppose all charge will be on the surface of the contacts, which will be particularly

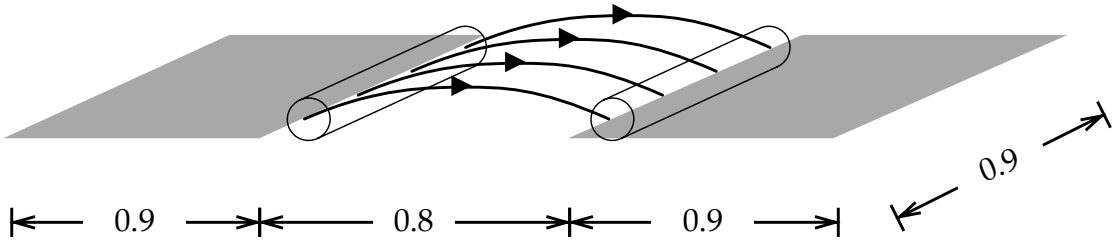


Figure 3.16: Approximation of stray capacitance in the air above the contacts by means of parallel round wires (drawing not to scale nor in correct perspective).

adequate for high frequencies, due to the skin effect. The charge on the inner rims of the contacts will generate an electric field through the substrate ($\varepsilon_r = 4.3$) and a smaller electric field through the air above. To estimate the capacitance in the air above the contacts, we take half the capacitance created by two parallel round wires suspended in air, both with a diameter equal to the contact thickness (35 μm), cf. Figure 3.16. Based on the per-unit-length capacitance of two parallel wires according to [10], we find:

$$C = \frac{\ell}{2} \cdot \frac{\pi\varepsilon}{\ln(s/r)} = \frac{0.8 \times 10^{-3}}{2} \cdot \frac{\pi 8.85 \times 10^{-12}}{\ln(0.8 \times 10^{-3} / 0.175 \times 10^{-3})} = 7.32\,\text{fF}, \tag{3.4}$$

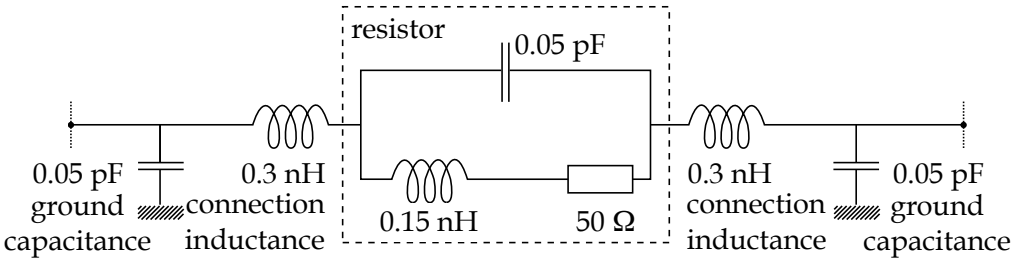
where ℓ and r are the length and diameter of the two wires, respectively, s is the separation between the two and ε is the permittivity of the medium.

As load standard, we measure a Vishay 50 Ω thin-film microwave resistor in a wrap-around 0603 package (reference CH0603-50RJNT). Allegedly, these resistors remain resistive up to 50 GHz [87]. Vishay's lumped-element model of a correctly mounted resistor in this package is depicted in Figure 3.17.

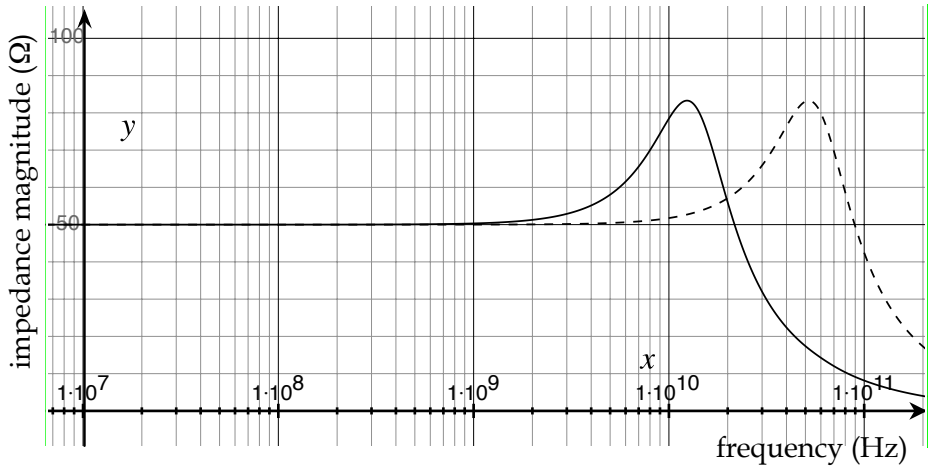
The lumped-element ideal models for the three standards were entered in ADS and plotted in Figure 3.18. To compensate a measurement, offline calibration was needed, because the used VNA does not allow entering the *LCRLC* load ideal.

The AVX 1 pF case study capacitor was measured and compensated using the three aforementioned methods. Recall that the nominal resonance frequency of this capacitor is 8 GHz. The results are plotted in Figure 3.19.

Looking at the impedance magnitude in Figure 3.19a, and assuming that the capacitor behaves as an *RLC*-series until 20 GHz, the impedance magnitude compensated both by an electrical delay and the SOL calibration look plausible up to about 12 GHz. Above that frequency, probably, either an *RLC*-series model is inadequate, or the calibration is wrong, or both. The CST-based compensated impedance magnitude deviates from the other compensations from 4 GHz and upwards, so we do not trust this compensation method. Furthermore, the 8 ps shortage of the CST model is not explained, which challenges the correctness of the compensation. We therefore discard the CST-de-embedded results.



(a) Lumped element model [79]. The elements in the dashed rectangle represent the resistor, while the other elements represent the parasitics of the PCB pads after and before the transition to a characteristic transmission line.



(b) Calculated impedance magnitude of the resistor itself (dashed) and the resistor including connection and ground parasitics (solid).

Figure 3.17: Model of the Vishay CH0603-50RJNT resistor.

Looking at the impedance phase in Figure 3.19b, we note that an *RLC*-series model predicts a neat transition of the impedance phase from $-90°$ to $+90°$ at the resonance frequency. The resonance frequency, judging from the phase plot, is 6.9 GHz according to the SOL calibration or 6.5 GHz according to the electrical delay compensation.

Conclusions

We designed, realised and tested a solderless test fixture on FR4 substrate that allows measuring the impedance of 0603 SMD components using an appropriate VNA. The fixture was optimised for measurements around 50 Ω, which allows to measure the resonant frequency of typical DPI coupling capacitors, but prohibits measuring the ESR very precisely.

The fixture was tested by measuring an microwave capacitor of 1 pF nominal value.

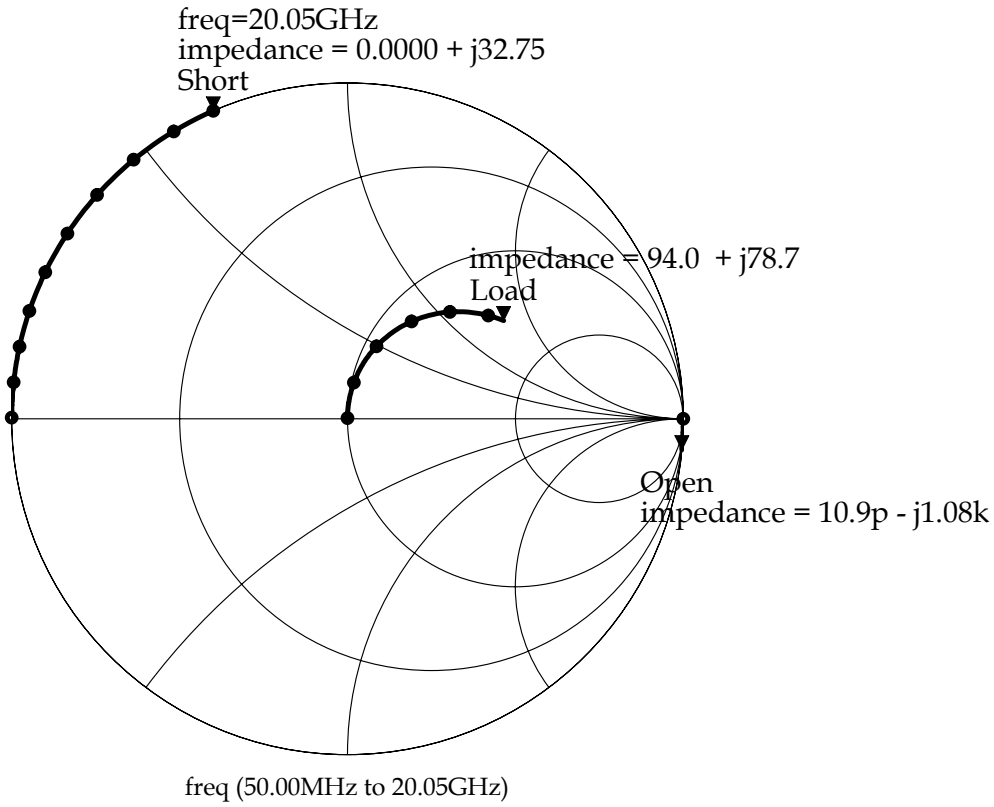


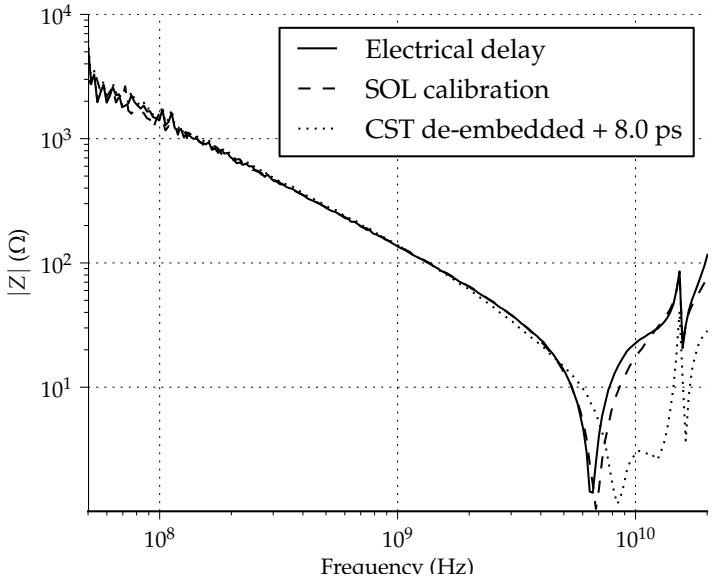
Figure 3.18: S_{11} parameter of the lumped element-models of the three standards. Complex impedances at 20.05 GHz are shown at the end of each curve.

We compared three different methods to compensate the fixture: subtracting an electrical delay, an SOL calibration and de-embedding using a CST simulation of the fixture. The former two methods seem to work well up to 12 GHz and give similar results. The latter method has a yet unexplained problem and does not look trustworthy above 4 GHz.

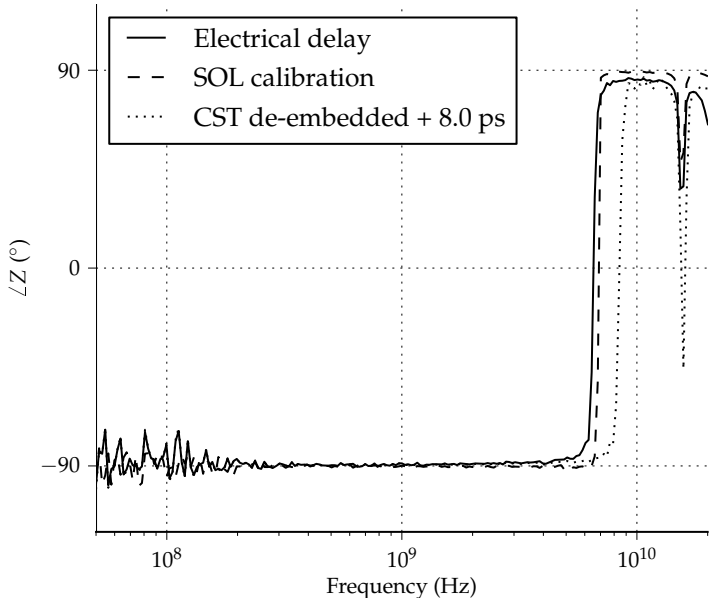
Using the fixture requires operator skills to manually align the SMD correctly. Furthermore, no metrological rigour was exercised to be able to define the measurement accuracy, so measurements taken with this fixture should be used as indication.

3.4 Lean Method

Recall Lafon's modelling method, which consists in moving the DPI reference plane to the PUTs by simulating the extraction PCB [69]. Now that the behaviour of SMD passives can be characterised well beyond 1 GHz, an extraction PCB can be better modelled. Lafon showed that de-embedding DPI measurements this way improves



(a) Impedance magnitude.



(b) Impedance phase

Figure 3.19: Measurement results of a 1 pF AVX capacitor, compensated using three different compensation techniques (electrical delay, SOL calibration and de-embedding using CST simulation results).

accuracy by about 10 dB [76]. Furthermore, his generic extraction PCB allows for changing peripheral passives while experimenting. Of course, the PCB model used for de-embedding must be changed accordingly. For instance, competent models of the used passives must be available.

This modelling obligation is also a disadvantage. For example, neighbouring bias tee capacitors have a mutual inductance that cannot be neglected from 1 GHz upwards [27]. Also, the complex, dispersive permittivity of the PCB substrate must be known to incorporate the dielectric losses. The conductor losses are mainly determined by the skin effect, and with rising frequency, the skin thickness approaches the surface roughness. Therefore, the surface roughness becomes important to correctly model the conductor losses. Furthermore, it is hard to route a generic extraction PCB that has exactly the same layout for each pin, while still providing footprints to solder peripheral circuitry. Particularly, the fan-out of the traces will quickly impose corners that have different angles for each pin, as can be seen in Figure 3.4. With rising frequency, these routing differences have increasing influence and complicate the competent modelling of the extraction PCB.

Recognising that above problems arise from a dense and integrated extraction PCB, one may ask: is it really necessary to place all periphery that close to the DUT? Therefore, the idea of a 'lean' (minimalist) extraction PCB, which modularises and decouples the periphery will be investigated. To that end, the question will first be asked what the essential requirements on an ICIM-CI extraction set-up are. Then, a case will be studied using these requirements, to find that a lean PCB is possible. Consequently, an extraction method suitable for high frequencies, using a lean extraction PCB will be developed.

ICIM-CI Measurement Requirements

For the extraction of an ICIM-CI from measurements, the DUT's PDN and IB must be quantified. To measure the PDN, the DUT's RF impedances must be measured at the PUT reference plane, while its electronics are in a representative operating point. To measure the IB, the DUT failure must be measured, while it is performing a typical or worst-case task under a known RF perturbation at its PUTs.

For both purposes, the DUT must be put at the same time in a functional and a perturbation environment. The functional environment must be representative of the typical application of the DUT and allow for failure monitoring. The perturbation environment must allow to inject a sufficient, well-known amount of RF perturbation in the DUT's pins [91].

The particular functional environment will, of course, depend on the DUT's function.

Generally speaking, ICs need one or more stable voltage supplies. That is, a DC voltage on one or more pins with respect to the ground. Depending on the IC's operating frequency, this voltage supply must present a more or less broadband low impedance.

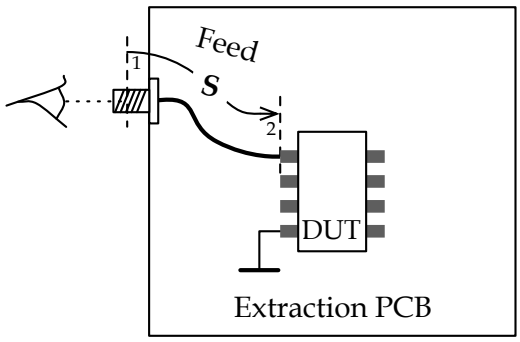


Figure 3.20: Definition of feed (described by its *S*-parameters). The connector- and PUT reference planes are dashed and correspond to respective port 1 and 2 of the *S*-parameters.

In standardised test set-ups, this requirement is often fulfilled with LISNs and/or bias tees.

Analog ICs will need supply and monitoring of analog signals with impedances typical of the application. For DC or low-frequency applications, this can be realised with programmable voltage or current supplies meters, connected through bias tees to the PUTs.

Logic ICs will need toggling input signals, representative of the application, while monitoring the (quality) of the output data. Typically, arbitrary waveform generators and oscilloscopes with mask testing are used to that end.

For applications where the functional signals overlap the perturbation signals, advanced multiplexing techniques are needed [70, 67].

The RF environment may be quite generic, for its purpose is to deliver a known RF perturbation power to the PUTs. If the RF forward power, incident on the extraction PCB's connectors is known, still PCB losses and crosstalk may misreport the actual power incident on the DUT's pins.

To limit the distortion caused by losses, IEC 62132-4 requires the extraction PCB losses to be smaller than 3 dB [75, ¶7.4]. This can be checked by installing a connector at the PUT reference plane and measuring the insertion loss of the *feed*, as defined in Figure 3.20.

IEC 62132-4 imposes no requirements on crosstalk. However, when power is leaked to a neighbouring pin, one will observe the joint susceptibility of the PUT and its neighbouring pin. This leakage is called far-end crosstalk: the forward propagating power leaked from one feed to forward propagating power in a neighbouring feed. In reality, there is always some crosstalk, so the question is: what crosstalk is acceptable?

Let us assume that the immunity of an entire IC is the minimum of the individual immunities of its pins; we thereby neglect complex interactions between multiple dis-

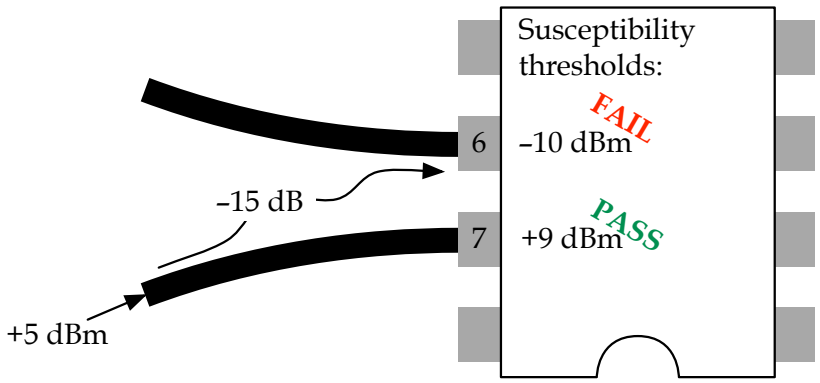


Figure 3.21: Thought experiment: an ATA6662 with its "true", unknowable, susceptibility thresholds. The crosstalk between feeds obscures the susceptible pin.

turbing signals. Under this assumption, the worst acceptable crosstalk is the largest possible difference between the immunity of any two neighbouring pins.

For example, supposing all pins to be matched to the feeds: the immunity level of pin 6 of a ATA6662 LIN transceiver at 10 MHz reportedly was −10 dBm of transmitted power, while the neighbouring pin 7 has an immunity level of +9 dBm of transmitted power [92], as illustrated in Figure 3.21. Suppose that the extraction PCB has −15 dB of far-end crosstalk between the traces of pin 6 and pin 7. When injecting on pin 7, one will observe an immunity level of +5 dBm, caused by the susceptibility of pin 6, instead of +9 dBm, proper to pin 7. To unambiguously characterise the immunity of the pins of this IC, an extraction PCB with better than −20 dB far-end crosstalk would be preferable.

Lacking more available immunity data of neighbouring pins, a far-end crosstalk better than −20 dB is targeted. More important than having little crosstalk, though, is to *know* the crosstalk; this way one is warned for misinterpretations of DPI measurements.

To summarise, a lean extraction PCB consists of connectorised traces leading to the DUT's pins with less than 3 dB loss and less than −20 dB crosstalk, well beyond 1 GHz.

Case Study: Lean extraction PCB for LM7805

The lean extraction PCB by itself meets the perturbation requirements stated above. However, the functional requirements must also be met in the extraction set-up.

To study the suitability of a lean extraction PCB, above requirements will therefore be elaborated for the simple case of an LM7805, a 5-V linear voltage regulator. For instance, it has one input and one output and requires no peripheral components. Only the voltage regulator's input will be studied in this case study. Although this case study is simple with respect to industrial cases, it will reveal the possibilities and limitations

of a lean extraction PCB.

To specify the functional environment for the LM7805, data sheets from its various manufacturers were consulted. Most data sheets specify the nominal performance of the LM7805 voltage regulator for an input voltage V_{in} of 10 V, a load current of 40 mA, an input filter capacitor C_{in} of 330 nF and an output filter capacitor of C_{out} of 100 nF. Some data sheets mention that the capacitors need to be of the solid tantalum type [93]. These functional environment specifications are summarised in Figure 3.22a.

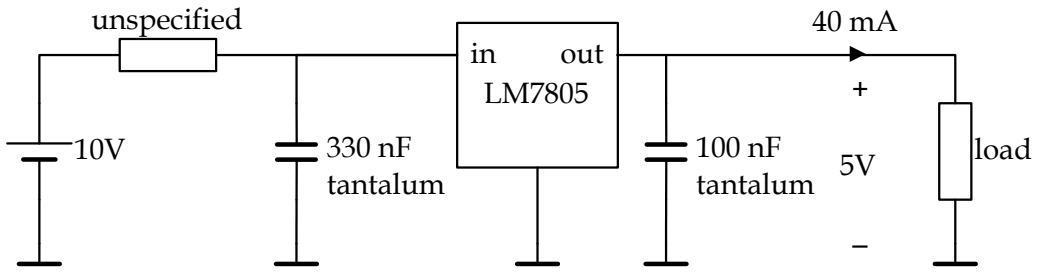
Often, only non-quantitative placement requirements are given, like: "the capacitors need to be placed as close as possible to the LM7805". Because we are going to challenge precisely this requirement, we need to guess the essential quantitative requirement behind the statement. The specification of tantalum capacitors [93] corresponds to an equivalent series inductance (ESL) in the order of 2 nH [94], hence to resonance frequencies of tens of MHz. Furthermore, the ESR of these solid tantalum capacitors is in the order of ohms [94].

The input filter capacitor supposedly serves to feed the regulator by low enough an impedance magnitude, so we require $|Z_{\text{supply}}| < 5\,\Omega$ (the ESR) up to 6 MHz (the expected resonance frequency of the input filter capacitor). The output filter capacitor, however, may be an essential part of the regulator's feedback loop, so we require $\Im\mathfrak{m}\{Z_{\text{load}}\} < 1/(\omega 100 \times 10^{-9})$ up to 11 MHz (the expected resonance frequency of the output filter capacitor). In order to draw the typical load current, $\Re\mathfrak{e}\{Z_{\text{load}}\} \approx 125\,\Omega$. We suppose the regulator correctly regulates the output voltage up to about this frequency. Let us call therefore call $0 - 10$ MHz the functional frequency range of the regulator.

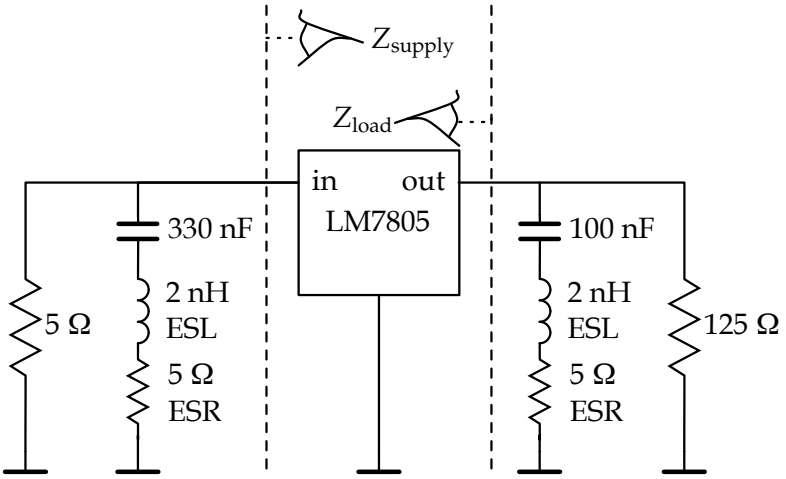
Although most data sheets guarantee an output voltage deviation of 250 mVDC, an output voltage offset in excess of $\pm 100\,\mu$VDC in a 1 kΩ load will be considered a failure. This extremely severe criterion was chosen in order to observe susceptibility with the available radiated field strength in the 20 MHz-4.2 GHz range, as we will see in Chapter 4.

To gauge the compatibility of these functional requirements and the lean extraction PCB, the impedance of the source and load networks specified above were entered into an ADS simulation (cf. Figure 3.22b). To represent the feeds of the lean extraction PCB, 5 cm of 50 Ω coplanar grounded waveguide was added in series (cf. Figure 3.22c). The resulting impedance shift can be appreciated in Figure 3.23. The 70 mΩ increase in series resistance is barely visible. Only above resonance of the capacitors, the impedance rises with frequency and then, transmission line resonances appear. In this case, the impedance shift due to the added feeds is negligible in the functional frequency range, so the requirements stated above are met.

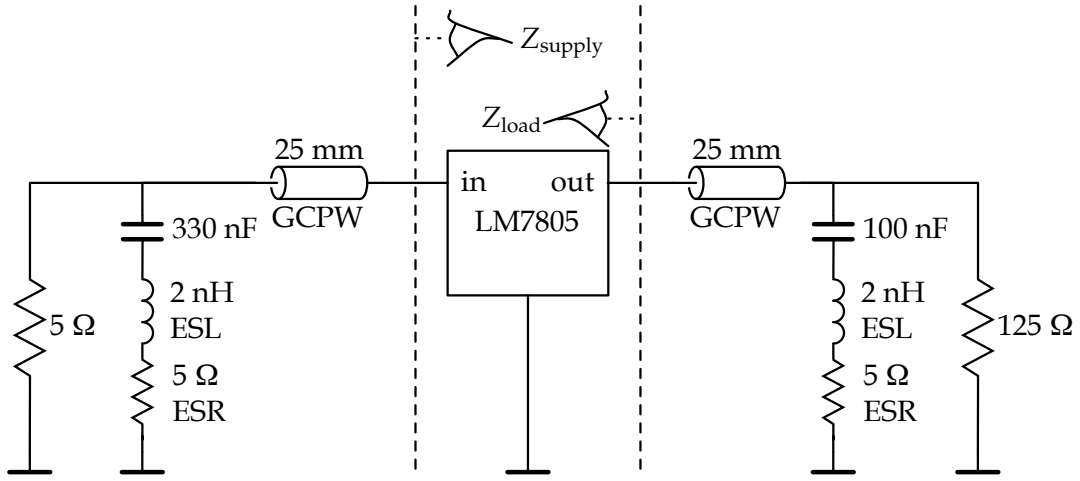
This principle is expected to hold true in general, at least for ICs with moderate functional frequency ranges (up to tens of MHz). Therefore, a lean extraction PCB with off-board source and load networks is considered valid for ICIM-CI extraction.



(a) Specification from datasheet.



(b) Circuit for the simulation of the specified supply and load impedances, as seen by the LM7805.



(c) Circuit for the simulation of the impact of trace insertion.

Figure 3.22: Analysis of the functional environment of the LM7805.

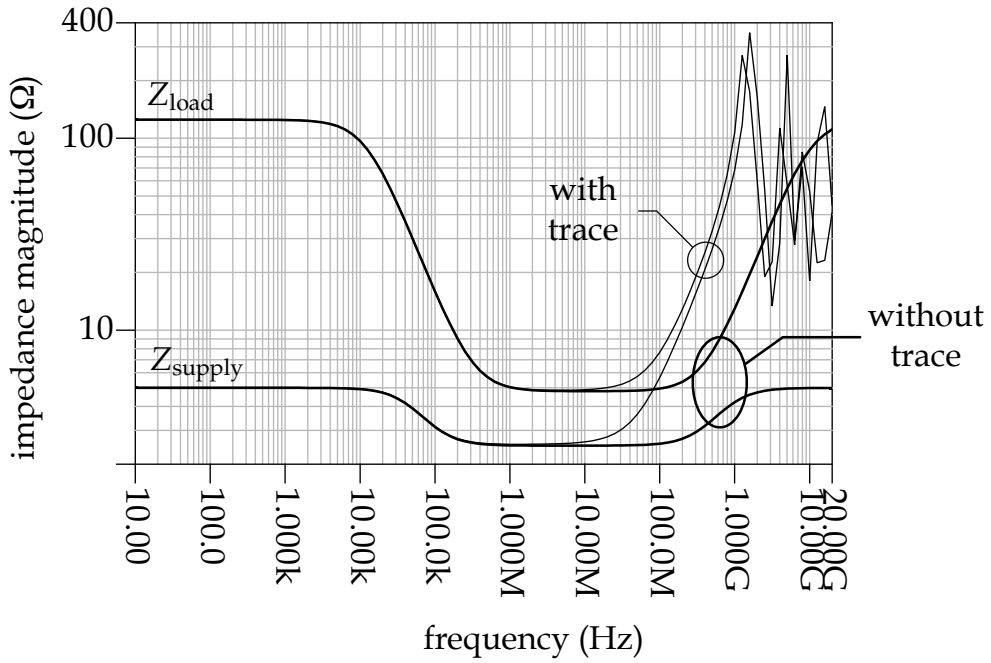


Figure 3.23: Impedance of specified source and load (thick curves) and the same impedances in series with 5 cm of 50 Ω trace (thin curves).

Lean ICIM-CI Method

With peripheral circuitry placed off-board, the lean extraction PCB only fans out the DUT pins to connectors. Hence, the peripheral circuitry necessary for a functional environment must be connectorised as *peripheral modules*, like a bias tee, a filter capacitor, a load emulator or a DC block. Refer to Figure 3.24 to see how a DUT, mounted on an extraction PCB may connect to its peripheral modules. The peripheral modules may be custom PCBs for a particular DUT, or Commercial Off-The-Shelf (COTS) modules, which may be reused between DPI set-ups.

With a lean extraction PCB and the necessary peripheral modules in hand, how to practically extract an ICIM-CI from measurement? How to easily move the reference plane of PDN and IB to the IC pins?

For the extraction of the PDN, Lafon already employed a calibration kit. That is, he reproduced the feed several times, with known impedances instead of the PUT. For instance, his calibration kit was fabricated in the same PCB panel as the extraction PCB, in order to have the same permittivity and substrate thickness. The feed was reproduced with open, short, load, thru or line standards to allow a Short-Open-Load-Thru (SOLT) or Thru-Reflect-Line (TRL) calibration. Any VNA can calibrate on these standards in order to translate the *S*-parameters measured at the extraction PCB's connector plane

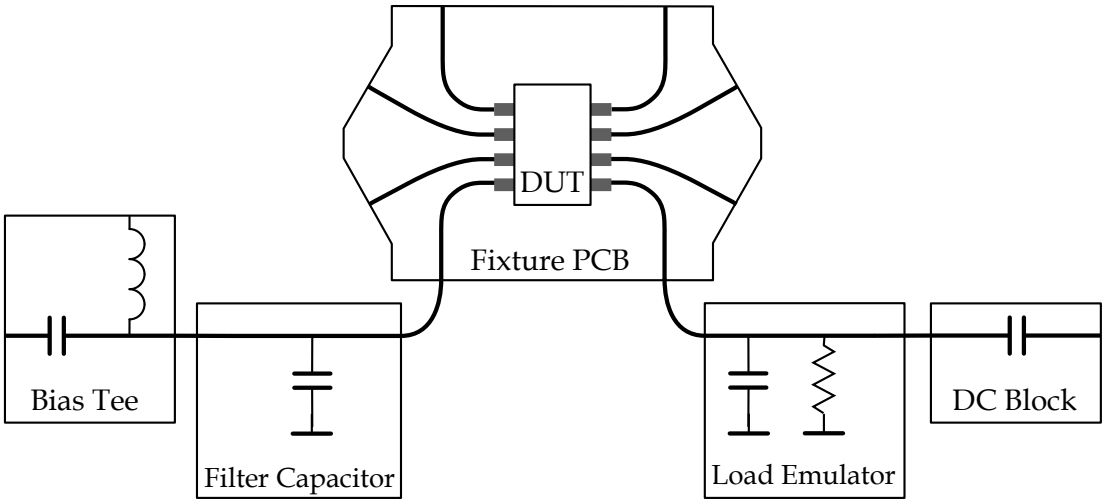


Figure 3.24: DUT on extraction PCB with example periphery. Signal generator and directional coupler not shown.

to the PUT plane.

However, he also needed to faithfully reproduce relevant on-board peripherals on the calibration kit. For example, the on-board capacitor or even the bias tee had to be reproduced. Because this bias tee consists of SMDs, it is critical that the soldering is consistent between standards and feed, particularly for rising frequencies. Moreover, if the bias tee was modified on the extraction board, it should equally be modified on the calibration kit.

With the lean extraction PCB and peripheral modules, on the contrary, the same calibration kit can be used for any peripheral module. That is, to measure the impedance of a PUT, the calibration can be performed on the calibration kit, *seen through* the peripheral module. That way, the reference plane is moved from the input of the peripheral module to the PUT, rather than from the extraction PCB connector plane to the PUT.

A practical advantage is that the peripheral circuitry need not be reproduced. Even a sloppily-soldered peripheral module will be compensated for, because the identical module is used during calibration and measurement. The only thing that remains critical is the similitude of the feeds on calibration kit and the extraction PCB. Because less soldering is involved, this becomes easier with the lean extraction PCB.

As for the extraction of the IB, this is also a matter of reference planes. That is, the standardised DPI, the transmitted threshold power at the output of the directional coupler is measured. The standard requires that the insertion loss of feed is less than 3 dB. If the cable between directional coupler and extraction PCB has negligible loss, too, the standard implicitly considers the error negligible.

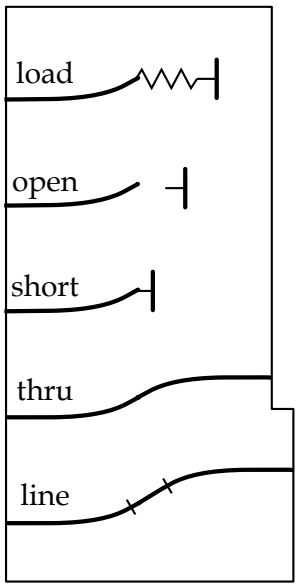


Figure 3.25: A calibration kit, allowing to move the reference plane from the extraction PCB connector plane to the PUT plane.

Alternatively, Lafon proposes to record the generator's forward power [69]. By careful modelling of the entire following RF chain (amplifier, cabling, on-board bias tee), the transmitted power at the PUT reference plane is calculated by circuit simulation.

Using the lean extraction PCB, the reference plane of the DPI result can be moved to the PUT as illustrated in Figure 3.26. The first step is to calibrate the VNA to a suitable coaxial reference plane. The second step is to measure and save the S-parameters of the calibration standards on the calibration kit, as seen through the peripheral modules. In the case of a reflection-only (SOL) calibration, only the reflection parameter of each standard is measured. Let the injection path be described by $\mathbf{S}$ (port 1 is the connector, port 2 is the PUT reference plane) and the reflection coefficient of the standard by Γ. The measured apparent reflection coefficient $\hat{\Gamma}$ is then:

$$\hat{\Gamma} = S_{11} + \frac{S_{21}S_{12}\Gamma}{1 - S_{22}\Gamma} \ , \tag{3.5}$$

of which the verification with a flow graph and Mason's rule is left as an exercise to the teacher. From the three measured reflection coefficients $\hat{\Gamma}$ of the open, short and load standards $\Gamma = \{+1, -1, 0\}$, one can numerically solve for three unknowns, typically the directivity S_{11}, the source match S_{22} and the reflection tracking product $S_{21}S_{12}$ [95]. As the injection path is passive and behaves linearly for all reasonable voltages, we know them to be reciprocal: $S_{21} = S_{12}$. Except for a π-phase ambiguity, the insertion loss can therefore be determined from the reflection tracking product: $|S_{21}| = \left|\sqrt{S_{21}S_{12}}\right|$[3] These

[3]Because of measurement errors and numerical imprecision, the square root will have a small imaginary

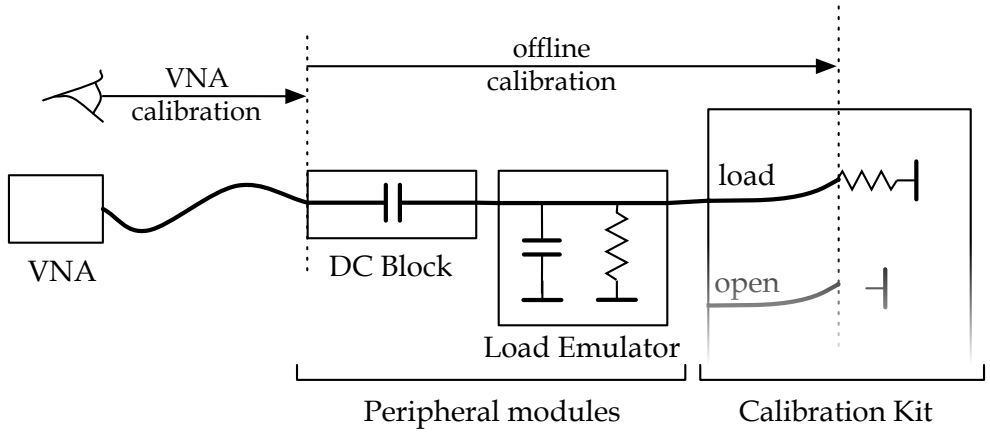


Figure 3.26: Translation of the reference plane from the peripheral modules' input to the PUT by two-step calibration.

calculations typically need to be performed as an offline calibration, on a PC.

Alternatively, the peripheral modules can be omitted during the two-step calibration. That way, the offline calibration yields a model of the feed only (connector and trace). Because the peripheral modules are equipped with connectors, their *S*-parameters can be measured separately. By concatenating both models on a PC, a model of the entire injection path can be obtained.

By subtracting the insertion loss $|S_{21}|$ of the injection path, the DPI measurement result can be moved from the peripheral module's input to the PUT. That is, to the extent that the source match of the injection path is negligible, the insertion loss can simply be subtracted from the DPI result. For example, if the DUT first fails with $+25$ dBm forward power at the input of the peripheral module, and the insertion loss of the injection path is 2 dB, that means a $+23$-dBm forward power threshold at the PUT. If the source match is not negligible, the forward power at the PUT can be analytically calculated using the PUT's reflection coefficient (not elaborated in this thesis).

To summarise, a lean extraction PCB only consists of connectors and traces leading to the DUT. This requires functional peripheral circuitry to be placed on connectorised peripheral modules. By calibrating a VNA first to the input of the peripheral modules and then to the PUT using a calibration kit, the insertion loss of the entire injection path can be calculated. Using this insertion loss, the DPI result can be corrected to obtain the threshold power at the PUT. The same calibration can be used to measure the PDN using a VNA.

The advantage of this approach with respect to Lafon's method is that the peripheral circuitry no longer needs to be modelled. Even unknown, bought or self-built peripheral

part. Either the absolute or the real value could be used to estimate $|S_{21}|$.

circuitry can just be measured. In case of doubt, or in order to improve the set-up, each module can be separately verified against analytical equations or SPICE simulations. Furthermore, if the same peripheral modules are used during PDN and IB measurement, the model becomes more consistent.

The disadvantage may be the necessity of software to perform offline calibration. Also, lab personnel needs to understand the two-step calibration procedure. More fundamentally, placing the peripheral circuitry on connectorised modules modifies their impedance as seen by the DUT. ICs stringent impedance masks, for example because of a high working frequency, may require shorter traces than practically feasible.

3.5 Specialisation: SOIC8 Extraction PCB

To study the feasibility of a lean extraction PCB without specialising too much, a generic SOIC8 extraction PCB is designed. SOIC8 was chosen in collaboration with Bureau of Standards, Metrology & Inspection (BSMI) because it is a common IC package, and widely used in the automotive industry because of its reliability.

Recall the goal of the lean extraction PCB: to connectorise the IC pins and provide a well-known perturbation injection path. From an industrial point of view, the solution should be economical in fabrication and in use. Moreover, the ease of extension to other packages should be known.

The design of a generic SOIC8 lean extraction PCB will first be underpinned. This design will prove impractical to draw with ordinary PCB design tools, so a library to programmatically generate PCB layouts will be developed. The generic extraction PCB will then be generated using this library and fabricated in an industrial process. To gauge the quality of this perturbation environment, the loss and crosstalk of the PCB will then be measured. Finally, conclusions will be drawn and practical recommendations for future revisions will be given, as well as perspectives because of the automatic layout generation.

PCB Design

The generic lean extraction PCB should allow for DPIs on any SOIC8-packaged IC. Because the PUT can be any pin, access should be provided to all pins. To avoid wasting precious centimetre-wave power, the feeds should have low loss and low crosstalk. For the feeds to be practically well-known, the feeds need to be electrically equivalent. That way, the feed calibration only needs to be performed once, and can then be applied for all PUTs.

Secondarily, to promote experimentation, we would like the fixture to be low-cost. To freely compare many DUTs, we choose not to solder but to clamp the DUT.

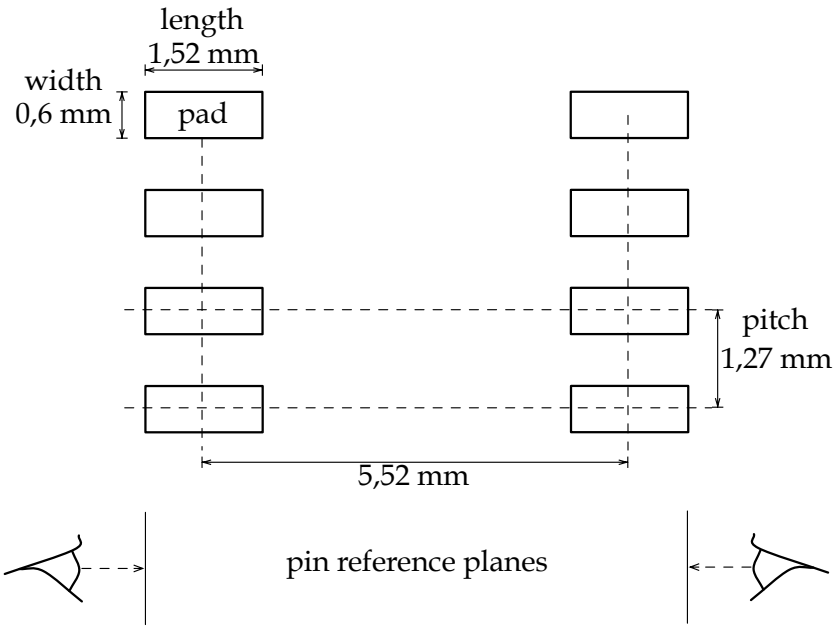


Figure 3.27: Definition of the SOIC8 footprint for GDPI purposes, as agreed upon with BSMI.

Recommended footprints for the SOIC8 package vary and also depend on the industrial soldering technique used. Recommended pad widths vary between 0.56 mm and 0.72 mm. We chose to take a typical maximum pin width 0.5 mm and add 0.1 mm to facilitate DUT placement, without introducing too much coupling uncertainty. The pad length is rather tight with respect to different recommendations: 1.52 mm. The resulting footprint agreed upon with BSMI is shown in Figure 3.27.

To avoid losing power on a trace-pad discontinuity, we decide to use a waveguide with the same width as the pad. To keep the fixture low-cost, we choose a standard Eurocircuits 4-layer FR4 stack-up [23]. To distribute a ground reference with low impedance, we opt for a ground plane. As the trace will end up on the outer layer, we have the choice between a microstrip and a GCPW. A 0.6 mm microstrip on outer layer 1 with inner layer 2 as a ground plane was calculated to have a characteristic impedance of 56.7 Ω, using ADS LineCalc and supposing a permittivity $\varepsilon_r = 4.1$ (the manufacturer specification we had at the time). If we want the GCPW to continue until the IC pads, there needs to be a trace of ground in between the pads, which has a minimum width of 0.15 mm in standard Eurocircuits technology. This implies a maximum lateral gap of 0.26 mm, which corresponds to a 49.8 Ω GCPW, when using layer 2 as a ground plane. For this particular trace width and substrate thickness, the characteristic impedance of a GCPW approaches 50 Ω the closest.

Another advantage of a GCPW is that it has less capacitive crosstalk between neighbouring traces; the ground in between serves as a shield. Furthermore, budget board-

edge SMA connectors are available that launch a GCPW wave with a SWR (standing wave ratio) below 1.5 for 18 – 26.5 GHz [83]. For these reasons, we chose to use a GCPW.

One extraction PCB and a calibration kit are estimated to fit on a 10×5 cm panel. With the stack-up mentioned above, a 50 cm^2 PCB costs about € 80. An SOLT calibration kit requires 5 connectors, and a fully equipped extraction PCB 7 more connectors, supposing one ground pin. With connectors ranging from € 0.50 to € 50, the connector is relatively important for the total cost.

Trying to strike the right balance between quality and price, a conventional board edge connector from Emerson was selected. From their example recommendations, it seems 0.21 mm ground lug clearance is needed at the left and right of a GCPW, including both lateral gaps. For the GCPW designed above, a good distance between ground lugs would thus be

$$w + 2g + 2 \cdot a = (0.6 + 2 \cdot 0.26 + 2 \cdot 0.21) \times 10^{-3} = 1.54\,\text{mm}, \tag{3.6}$$

where w denotes the trace width, g the bilateral gap, a the clearance between the ground plane and the ground lugs.

In the Johnson connector series for this board thickness, a ground lug distance of 1.27 mm and 1.70 mm is available. For safety, the latter of the two was chosen: the Emerson 142-0771-831, € 7.33 at Digi-key.

For a generic PCB all IC pins need feeds to connectors. In this case of SOIC8, there are four pins at both sides, with a 1.27 mm pitch. The Johnson connectors practically need 1 cm of board edge. Consequently, the traces from the pads to the connectors have to fan out. However, to keep losses low and to limit the distortion of peripheral impedance, the feeds must be kept short. Therefore, an efficient fan-out taper is needed. The optimum taper is a circle segment, so we use arc-shaped traces. To keep the feeds electrically equivalent, the effective length of the arcs must be equal. As an empirical rule, the effective length of a microstrip arc is $w\theta/2$ shorter than its centreline length, where w is the trace width and θ is the arc's angle [37].

However, when using arcs of equivalent length, while fanning out, the bend radii will be different and the trace ends will not generally line up. Because the connectors at the trace ends need to be mounted on the PCB edge, the PCB will not be rectangular.

To render the feeds knowable, a calibration kit is needed that faithfully reproduces the feeds with short, open, load, thru and line standards. The load was chosen to be a 50 GHz 0402 flip-chip 50 Ω resistor: the Vishay CH0402-50RGFPT [87], in order to match the trace width. Line standards are effective for a phase shift between 20° and 160°, and are provided for 1 – 8 GHz (9.98 mm) and 2.5 – 20 GHz (4.04 mm). A thru standard is provided for all bend radii, to be able to check that the feeds are indeed electrically equivalent.

PyPCB

Drawing bent traces is possible in some layout tools, such as Altium or ADS, but drawing the corresponding non-rectangular board outline and placing equidistant stitching vias can only be done manually. This laborious task is error-prone and needs to be done over if any elementary parameter changes (trace length, trace radius) or when an extraction PCB for another package would need to be designed.

More fundamentally, (PCB) design is a many-dimensional puzzle. Solving this puzzle consists in the iterative propagation of the requirements. The advantage of classical PCB design tools is that the designer can interactively solve this puzzle. However, the propagation of requirements takes place in the head of the designer, implicitly. Consequently, when any of the requirements changes or constraints are added, the designer has to propagate the new requirements, which is error-prone. For example, connector J1 should be flush with the PCB border, then connected by a 50 Ω trace to connector J2, that should be flush with the opposing PCB border. When changing the PCB outline, he must manually move the connectors to remain flush with the PCB border.

This way of working is annoying while playing around with design alternatives, and error-prone for a multitude of more complex design constraints. To make PCB design more enjoyable and less error-prone, it would be great to have a language to express the design constraints. An automat could then propagate these constraints to find a solution that meets all requirements.

Knowing the immense complexity of modern-day PCBs, it would be too ambitious to create this automat for any PCB. However, a solution that works for the layout of an SOIC8-generic lean extraction PCB seems reasonable. This solution could then become the starting point of a community-driven generalisation. Because of the (open) community perspective and the rapidity of development, Python was chosen as interpreter. To express the final goal, the project was titled PyPCB.

The design flow then becomes as illustrated in Figure 3.28. PyPCB would translate the explicit design in industrially feasible layout description. Using existing tools, these layouts can then be previewed. Once satisfactory, the layout description can be sent out for fabrication.

To allow for this flow, unit tests were defined on simple layout elements and then implemented. This Test Driven Development (TDD) was facilitated by the `nose` testing framework.

Firstly, the `geometry.py` allows describing planar geometry. On top of axioms like `Location`, `Angle` and `Segment`, basic geometric concepts are built, like `Square` (subclass of `Rectangle`), `Arc` and `Circle`. From these, PCB-oriented planar geometries are modelled with classes like `Pad`, `Trace` and `MiteredBend`. Using these, multi-layer entities are described, such as `Via`, `CoplanarTrace` (subclass of `Trace`) and `Sma`.

It turned out useful to introduce the notion of an `Arrow`, that is, a `Direction` vector with a `Location` origin. The concept was inspired by the planar ports that ADS uses to

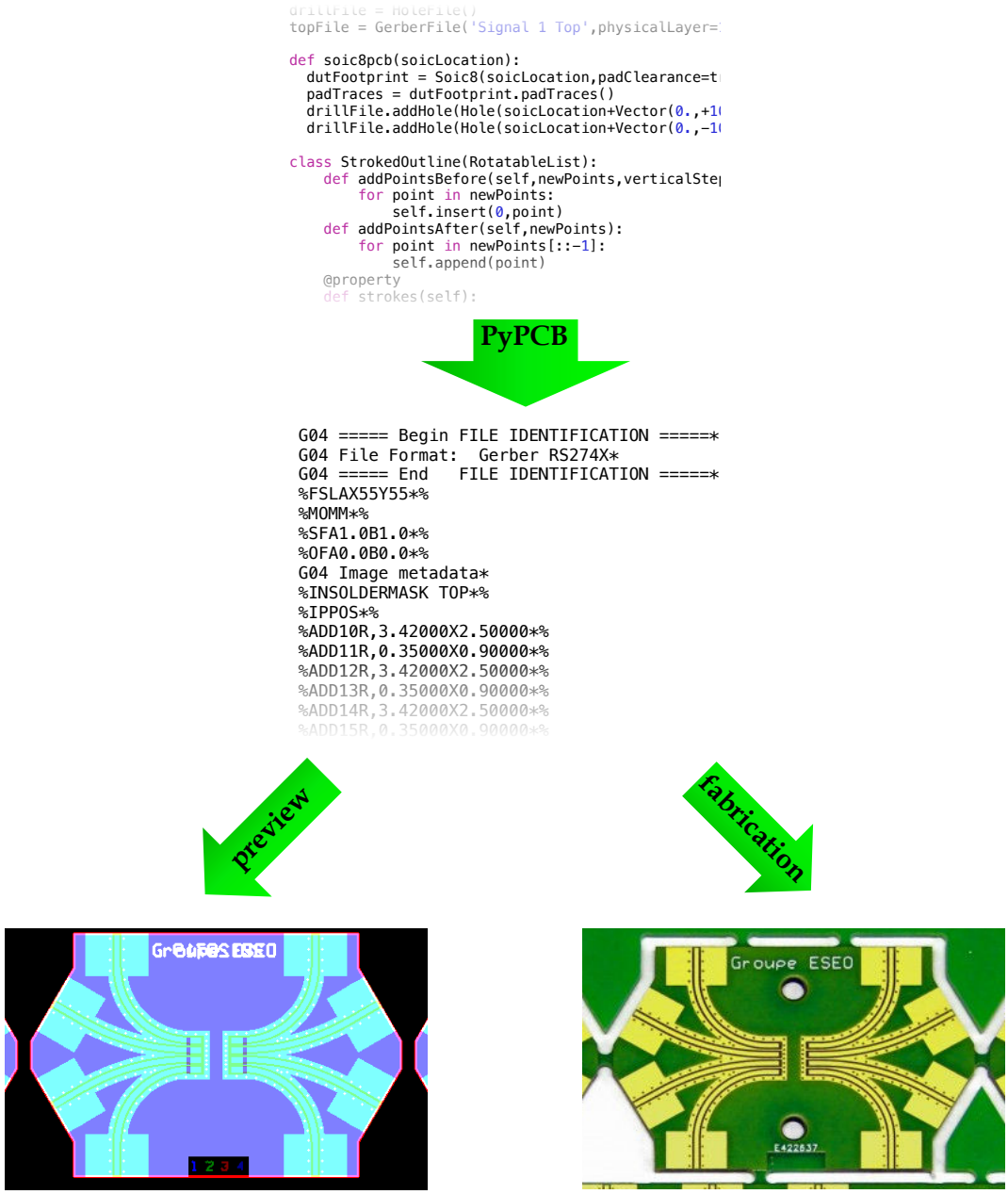


Figure 3.28: PyPCB design flow: from essential code, Gerber and Excellon files are generated, that can be visualised and fabricated.

automatically layout microwave circuits. Indeed, these `Arrow`s often bear the meaning of a reference plane (or line, strictly speaking).

`DrawGroup`s allow to hierarchically construct a layout. For example, top-aligning of two groups `drawGroupA` left of `drawGroupB`, can be done like so:

```
drawGroupA.topRight = drawGroupB.topLeft
```

Using `stroketext.py`, text can be drawn using the stroke font courteously provided by Altium Limited.

The description of stackups and their fabrication constraints is done in `stack.py`. For example, `EuroCircuits6C` (sub-subclass of `Classification` contains knowledge about the minimum via stitching pitch. That way, `CoplanarTrace` can remain agnostic of technology constraints. If one day another manufacturer is chosen, their classification can be entered and the stitching via pitch of GCPWs will automatically change.

A `Stack` consists of inner and outer `Face`s (commonly called layers), as well as cross-layer information like cutting contours, plated- and non-plated holes. The faces consist of one or more `GerberFile`s defined in `rs274x.py`. The holes are ultimately described in an `Excellon` object, as defined in `excellon.py`. The entire `Stack` can be shipped out as a ZIP archive that is conform with the Eurocircuits specifications.

The entire PyPCB module consists of 2473 Single Line Of Code (SLOC), of which 607 SLOC of tests. For example, a Sierpiński carpet was generated using PyPCB. A Sierpiński carpet is a fractal that also has applications in antenna design [96]. The following code was used:

```
from pypcb import *
copper =  GerberFile('Sierpinski')

def sierpinski(centre=Location(0,0),width=10.,recursions=1):
    for x in [-1,0,1]:
        for y in [-1,0,1]:
            if not(x == 0 and y == 0):
                subcentre = Location(x,y)*width/3+centre
                if recursions == 0:
                    Square(subcentre,width/3).draw(copper[0])
                else:
                    sierpinski(subcentre,width/3,recursions-1)

sierpinski(recursions=3)
copper.writeOut()
```

The resulting `Sierpinski.gbr` can be visualised using a free Gerber viewer like Penta-Logix' ViewMate. The result is shown in Figure 3.29.

Using PyPCB, the extraction PCB designed above was explicitly described. That is, an SOIC8 footprint is defined as the starting point. Based on the `Arrow`s of its pads, GCPWs of the same equivalent length but with different bend radii were constructed. Vias that

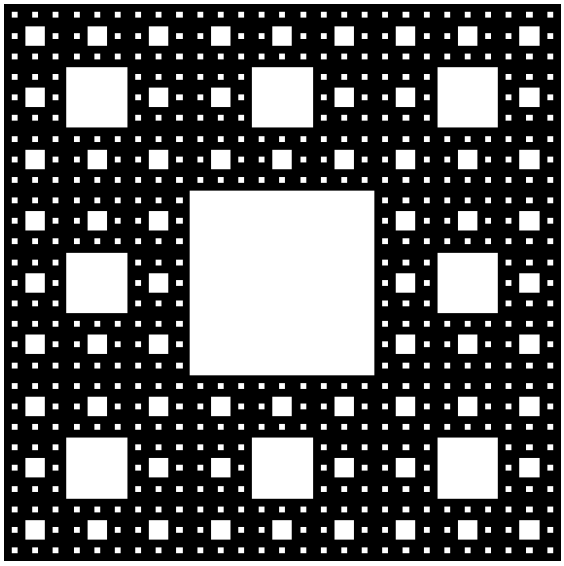


Figure 3.29: Sierpiński carpet as generated with PyPCB.

were too close to manufacture, were automatically merged. At the end of these traces, an SMA footprint was placed. The cutting contour of the board was then constructed by linking the SMA footprint edges. The bend radii and the trace length were tweaked manually to avoid overlap of the SMA footprints.

The calibration kit was defined by repeating the identical feed. For the line and thru standards, the identical feeds were followed by a straight trace segment, and then by another identical feed. The straight trace segments automatically wrote their actual length in the silkscreen. Next, the SOL standards were placed. Finally, the cutting contour was constructed by linking the SMA footprint edges together using orthogonal segments. The total panel was constructed by putting three extraction PCBs above the calibration kit.

The code was run and the resulting archive of Gerber and Excellon files was sent to Eurocircuits. The fabrication result is shown in Figure 3.30.

The Python module PyPCB was developed to generate PCB layouts based on explicit design decisions. That is, layout elements need to be geometrically constructed instead of drawn at fixed coordinates. The code was used to generate the layout for the lean extraction PCB and the corresponding calibration kit.

To propagate the design constraints, lazy evaluation was tried. That is, while creating the objects, only relative coordinates between objects were stored. Only at the end of the programme, all coordinates were evaluated to become absolute in a single coordinate system. This proved too difficult to implement, so absolute coordinates are evaluated from the beginning. Aligning entities then immediately move objects in this

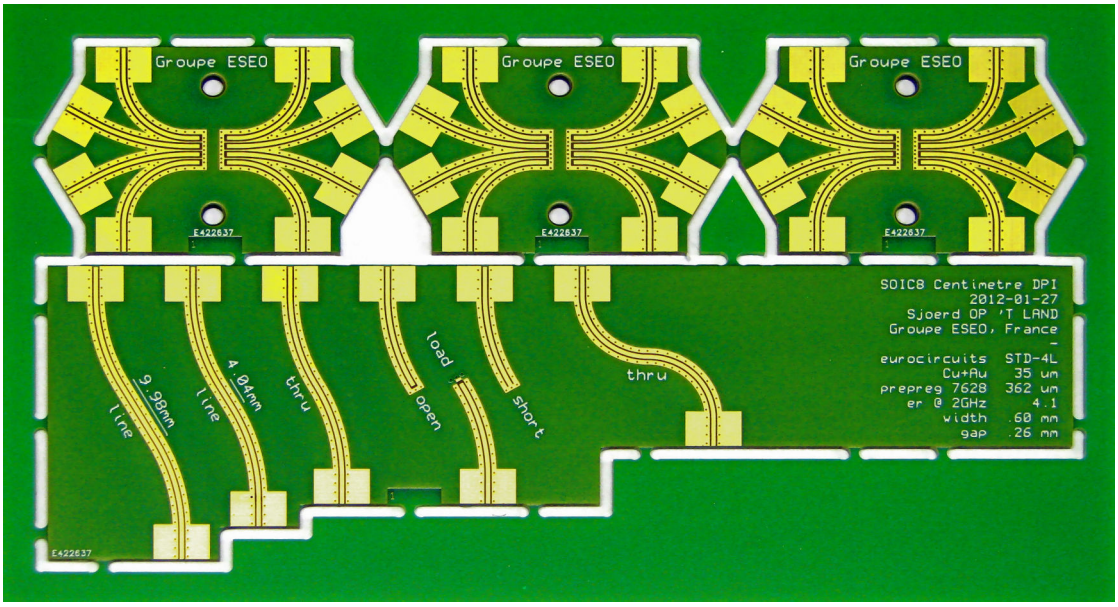


Figure 3.30: Fabricated lean extraction PCB panel, consisting of one calibration kit and three extraction PCBs.

absolute coordinate system.

PyPCB might be improved by SymPy, a Python library for symbolic mathematics. Firstly, storing symbolic coordinates could turn out to be an elegant way to propagate design constraints. Secondly, the SymPy's `geometry` module might essentially replace our `geometry.py`. Because of SymPy's maturity, more elegant ways of expressing geometric constructions may become possible.

A more revolutionary turn would be to continue programming PCB design, but to stop coding. That is, the designer should be empowered to construct his design using a Graphical User Interface (GUI). For example: dragging J1 flush to the PCB contour would store 'J1 flush to the PCB contour' instead of 'J1 at location $(112.4, 65.5)$ mm'. This idea came from Bret Victor, who already presented a mature proof-of-concept [97].

Quality Check

The quality of the generic extraction PCB as perturbation environment will now be gauged from loss and crosstalk measurements and simulation.

As a first indicator of the feed loss, the calibration kit was equipped with SMA connectors [83] and the S_{21} parameter of the thru standards on the calibration loss was measured. The result is plotted in Figure 3.31 as the solid curve. The large bend radius thru S_{21} amounts -3.7 dB at 20 GHz. Because the thru standard consists of two end-to-end connected feeds, this suggests a feed insertion loss of 1.85 dB at 20 GHz.

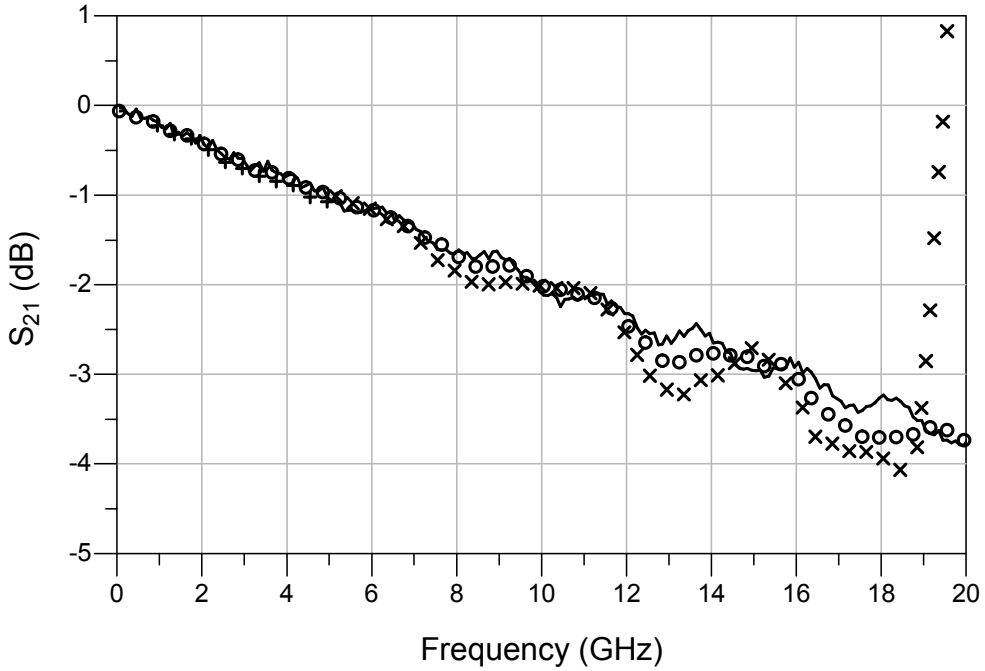


Figure 3.31: Measurement of the S_{21} parameter of the large radius thru (solid line). Circuit simulation of thru by connecting two feed models back-to-back, where the feed models are obtained by measuring SOLT ($\circ$), TRL 1 – 8 GHz ($+$) and TRL 2.5 – 20 GHz ($\times$) and performing offline calibration.

To check the electrical equivalence of the small and large bend radii, the S_{21} of the small radius thru was measured too (not plotted). The difference with the large bend radius is maximally ±0.3 dB and $+3$ ps from the large radius thru. At a phase speed of $c_0/2$, this corresponds with a 1 mm effective length difference per feed. The 0.2-mm Eurocircuits milling uncertainty does not suffice to explain this difference. The empirical rule used to compensate the centreline length of the feeds might not have held for these GCPWs.

To characterise the feed in another way, we measure the short, open, load, thru and line standards, and extract a feed model by offline calibration (cf. section 3.4). We then cascade two feed models back-to-back in ADS and simulate the end-to-end transfer; if the feed model is good, this transfer should correspond to the measured thru transfer above. The simulation results are added to Figure 3.31. The feed model based on SOLT measurements results in a transfer that deviates maximally ±0.5 dB over all 0.05 – 20 GHz frequency range. Similarly, models are extracted from TRL standards for the short and the long line. Around 19 GHz, the short line phase shift surpasses 150°, and the resulting prediction starts to deviate heavily. Apparently, line standards should not be used beyond about 150°, whereas we designed for up to 160°.

In order to understand the ±0.5-dB deviations between prediction and measure-

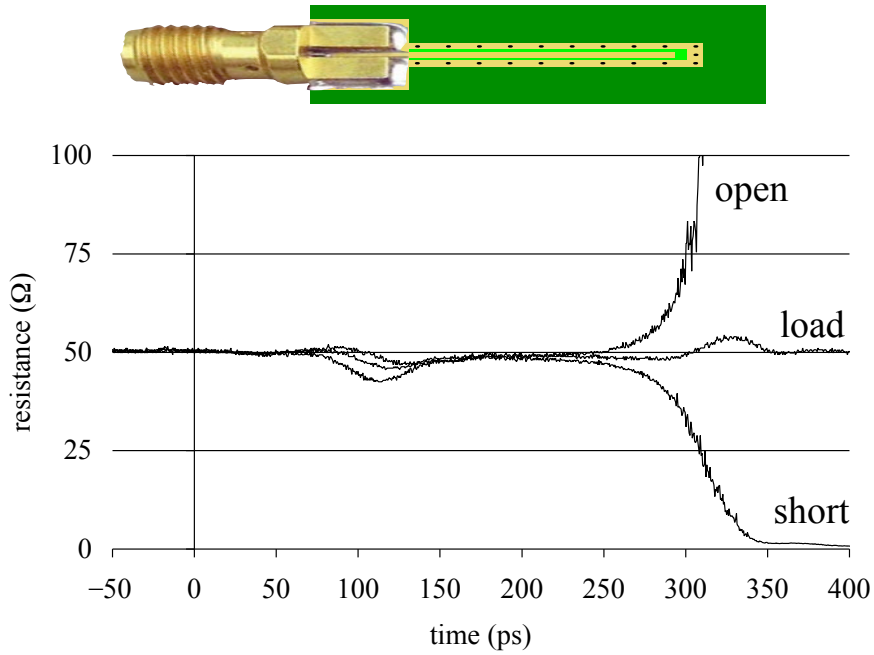


Figure 3.32: Time domain reflectometry of the short, open and load standards (rise time of 35 ps). The image of the open standard is warped according to ADS LineCalc delay data, $t = 0$ ps corresponds with the SMA reference plane.

ment, we check the step response of the SOL standards with a Time Domain Reflectometre (TDR). As we know the propagation velocity, we can map the round-trip-time to a physical position along the line, which is done in Figure 3.32. It can be noticed that the standards differ about 5 Ω just after the board edge at 70 ps. Supposedly, the soldering and/or the connector alignment is not consistent from standard to standard.

The DUT-side crosstalk cannot be measured physically, because there is no room for two SMA connectors next to each other at the place of the DUT. Therefore, we asked our research acquaintance Ignacio Gil of the *Universitat Polytècnica de Catalunya* (UPC) to perform an electromagnetic simulation of the PCB with Agilent Momentum. According to the simulation results, the layout exhibits a worst-case crosstalk of −19 dB at 14 GHz between neighbouring large radius and small radius feeds.

To appreciate the reliability of the simulation, the following measurement was devised. The extraction PCB was cut in half and the IC pads were shorted with copper tape at the PUT reference plane. The transfer from one SMA connector to the neighbouring connector was measured. The same set-up was simulated, by shorting the ports of the simulated neighbouring traces. The simulation results are compared to measurement in Figure 3.33. On average, the simulation is 5 dB too optimistic. This suggests that the real PUT crosstalk of the extraction PCB is also higher than simulated, towards −14 dB.

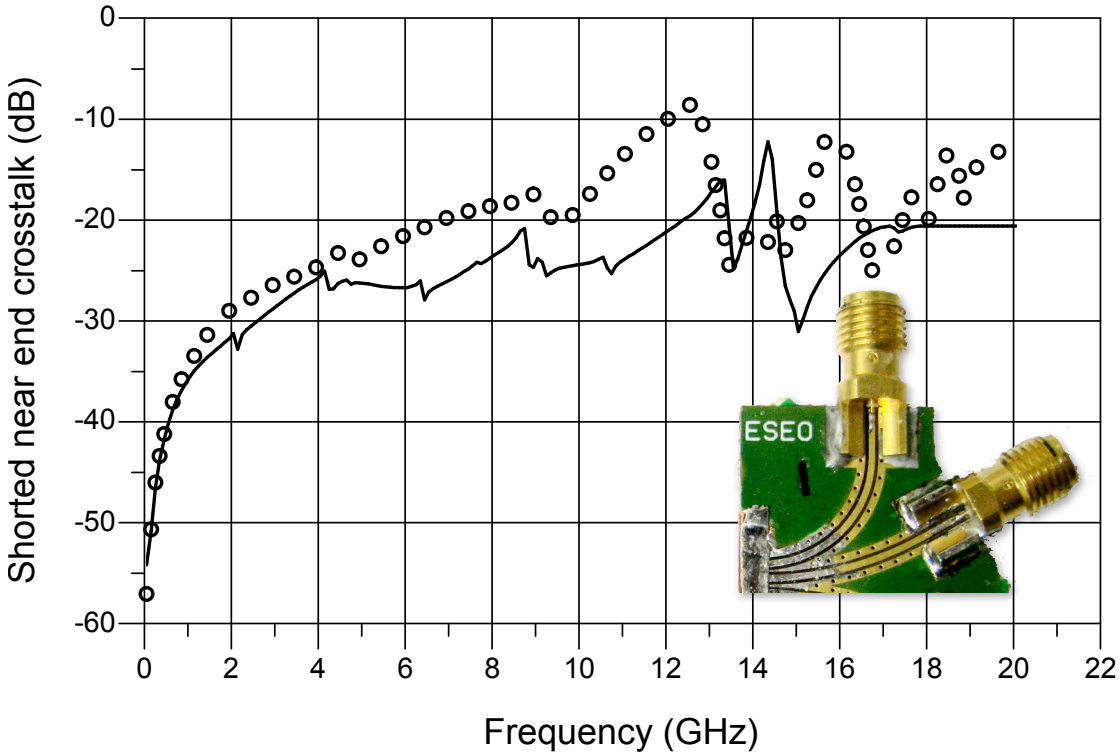


Figure 3.33: Measurement (○) and Agilent Momentum electromagnetic simulation (solid line) of the SMA-end crosstalk between a neighbouring large radius and small radius feed, with all PUT-ends shorted to ground.

To summarise, the extraction PCB has a feed loss of 1.9 dB at 20 GHz. In light of the 3 dB requirement formulated in IEC 62132-4, this is perfectly acceptable. The ±0.5-dB reproducibility of the feed seems to be limited by the consistency of the connector-PCB alignment and soldering. The worst case far-end crosstalk between neighbouring traces is estimated to be about −14 dB. With respect to the −20 dB requirement derived in section 3.4, this is marginal. However, the crosstalk is more or less known, so DPI measurements can be intelligently interpreted.

The extraction PCB could mainly be improved on the reproducibility of the connector mounting. Soldering angled connectors under pressure proved difficult, so a future fan-out should end in straight angles. As revealed by TDR-measurements that are difficult to reproduce, the centre conductor is subject to mechanical play, causing invisible solder cracks. Soldering with a more elastic silver solution might prove more robust to mechanical stress. A solder mask dash could limit excess solder flowing down the trace. Only if these measures do not improve reliability, more expensive connectors should be tried.

Conclusions

To prove the feasibility of a lean extraction PCB, a generic PCB for SOIC8-packaged ICs was developed. To employ bent GCPWs, it proved useful to develop the PyPCB library to programmatically generate PCB layouts. Measurements and simulations on the resulting calibration kit show that the feeds have acceptable loss up to 20 GHz.

The extraction PCB is fitted with budget SMA connectors on a standard FR4 substrate to reduce fabrication cost: depending on the number of feeds fitted with SMA connectors, one extraction PCB and calibration kit cost around € 200. Moreover, the spring-loaded extraction PCB does not require soldering the DUT, thereby reducing utilisation cost.

One important aspect remaining to be understood, is the perturbation mode incident upon the PUTs because of the trace fan-out. Firstly, the GCPW conducts three modes: a microstrip mode, a coplanar common mode and a coplanar differential mode.

Secondly, the calibration standards represent a single GCPW feed, but at the DUT, many traces come together and there is no place for stitching vias along some 8 mm. Therefore, the mode may radically change nearby the DUT, without this effect appearing on calibration traces. A future study could be performed on a thru standard without stitching vias, and with nearby neighbouring traces: the lean extraction PCB without DUT footprint. If the mode conversion proves problematic, a generic extraction PCB might be invalid for high frequencies. In that case, extraction PCBs need to be designed for each specific DUT or even PUT.

Apart from that, the PyPCB library may prove very interesting for generalising the method to other ICs and -packages. Although the library still requires manual tweaking of layouts, the automatic generation of an extraction PCB based on a pinout should be feasible. For example, a graphical application could allow users to choose a package, indicate the pins that need to be injected on, as well as power and ground pins, and pins for which no feed is needed. The application then optimises the layout for that particular case, creates the corresponding calibration kit, and sends the order to Eurocircuits.

3.6 Case study: LM7805

Now that a generic extraction PCB is available, the lean extraction method developed in section 3.4 can be applied to a real DUT. The same case study that was used to prove the validity of the lean extraction method will be used: in particular, a National Semiconductor LM78L05ACM.

Knowing that the ICIM-CI model will be used in a radiated PCB immunity test in Chapter 4 directs the model validity domain as follows. Because of the significant field-to-trace attenuation, little power will be available at the PUT to provoke failure. Therefore, amplifiers will be needed in order to observe susceptibility, which in our

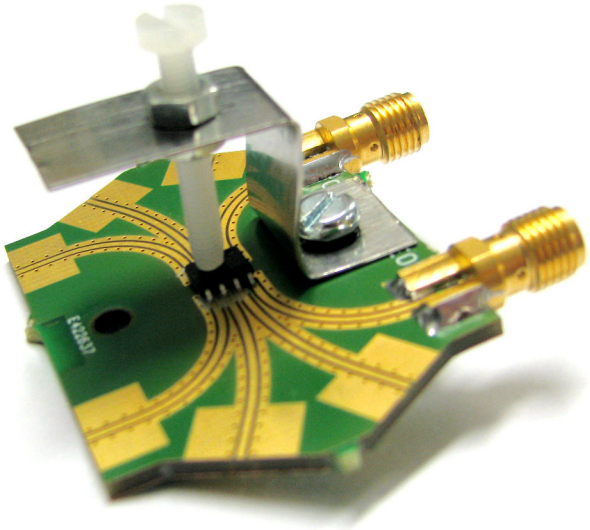


Figure 3.34: LM7805 on generic SOIC8 extraction PCB.

laboratory dictated the upper frequency bound: 4.2 GHz. Another trick to observe susceptibility, is to define a very stringent functional criterion.

Recall that the ICIM-CI model consists of a PDN and an IB. The PDN will first be extracted from VNA measurements. Next, the IB will be extracted from DPI measurements, corrected using the feed model.

PDN Extraction by VNA Measurement

To obtain the PDN, the *S*-parameters were measured using an Agilent 8753E VNA. To that end, the LM7805 was put on the generic SOIC8 extraction PCB. All unused and ground pins of the IC (2 up and until 7) were shorted to ground using a CircuitWorks 2200MTP conductive coating dispenser. The input (pin 8) and the output (pin 1) of the extraction PCB were equipped with SMA connectors, as shown in Figure 3.34.

To get the LM7805 IC into its operating point, 10 V was applied to the input through the VNA's bias tee. To check the solderless connections at DC, the output voltage was verified to be 5 V through the VNA's other bias tee. The measurement set-up is schematised in Figure 3.35.

To move the reference plane to the IC pins, the two-step calibration developed in section 3.4 was employed. First, the reference plane was moved to the extraction PCB's SMA connectors. That is, 3.5-mm standards from the Agilent 85052D 3.5 mm economy calibration kit were connected instead of the extraction PCB. Then, the VNA's built-in calibration with the corresponding ideal definitions was run.

Next, the short- open- and load standards on the extraction PCB calibration kit were measured and saved to a PC. Using `scikit-rf`, an offline calibration was performed,

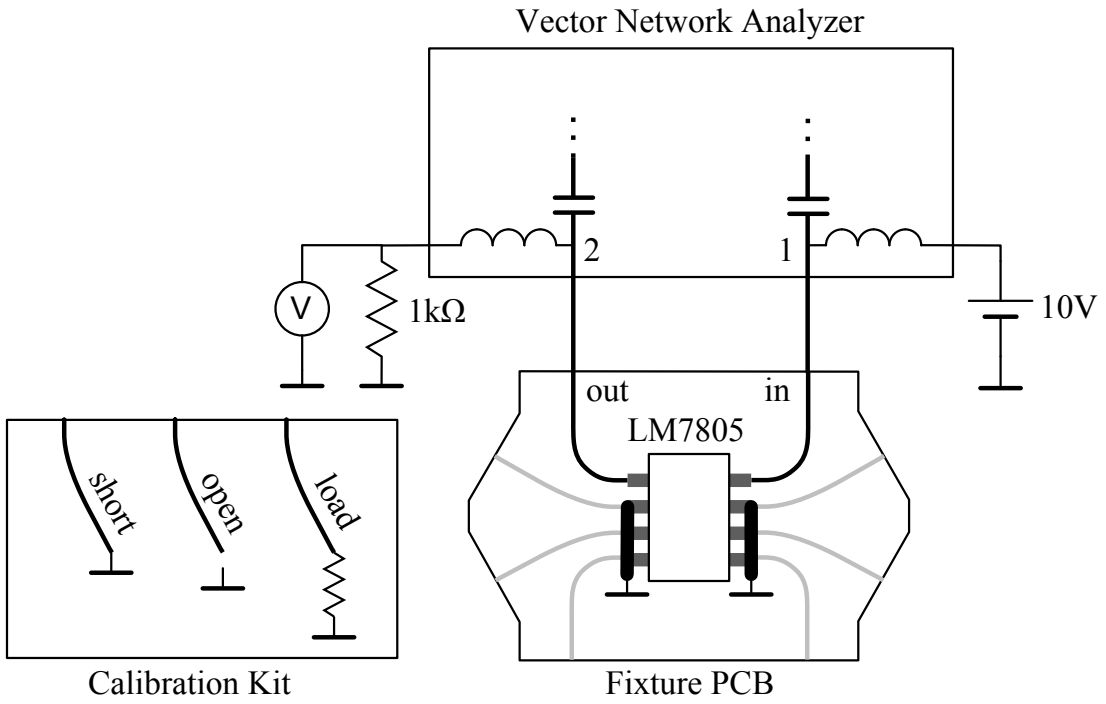
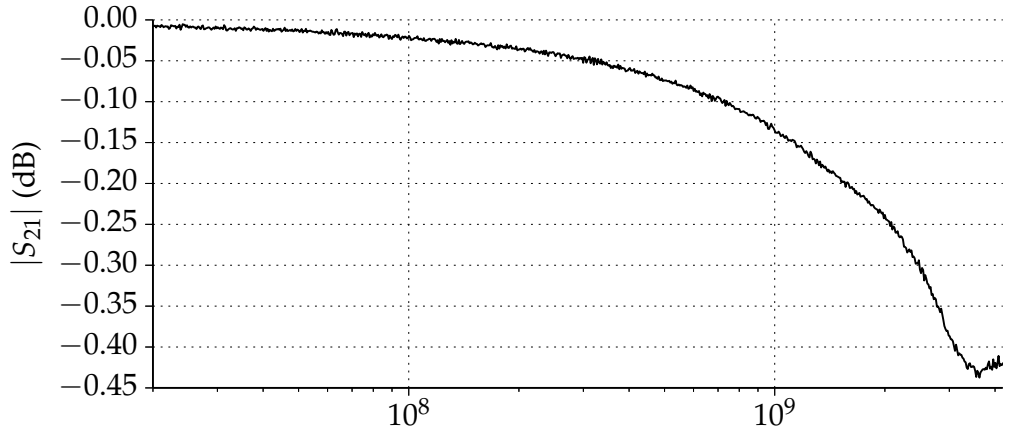


Figure 3.35: Measurement set-up for PDN extraction of the LM7805 IC.

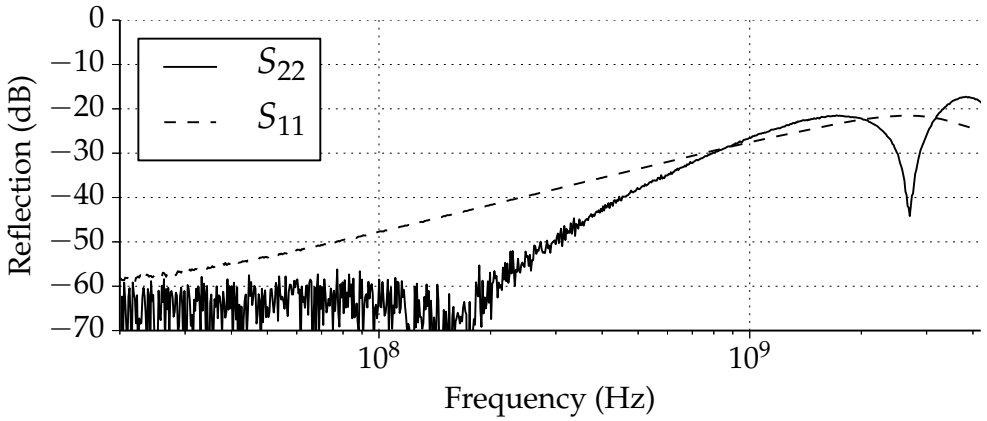
assuming ideal standards (i.e. reflection coefficients -1, $+1$ and 0, respectively). This calibration thus moves the reference plane from the SMA connector to the PUT. The calculated calibration coefficients can be visualised using `scikit-rf` and are plotted in Figure 3.36.

Finally, the LM7805 input impedance is measured at the SMA reference plane, using the extraction PCB. The measurement is saved and compensated on the PC, using calibration coefficients obtained above. The resulting impedance at the PUT reference plane is plotted in Figure 3.37. The oscillations in the $120 - 210$ MHz range are present both on the SMA and the PUT reference planes. This phenomenon may be explained by the marginal stability of the LM7805 without external capacitors. The VNA's stimulus may lead the active LM7805 to ring, leading to false reflection readings. Indeed, turning off the 10 V power supply removes the ringing (measurement not plotted). However, the impedance profile also changes shape by turning off the power supply. Therefore, and because the impedance profile of Figure 3.37b only exhibits small oscillations, the 10-V powered measurements are used for the remainder of this thesis.

Although a *CRL*-like behaviour can be recognized in the impedance profile, we have chosen not to fit a grey-box model to the data, because it does not help falsifying the main hypothesis. Instead, it would degrade the realism of the descriptive, black-box model.

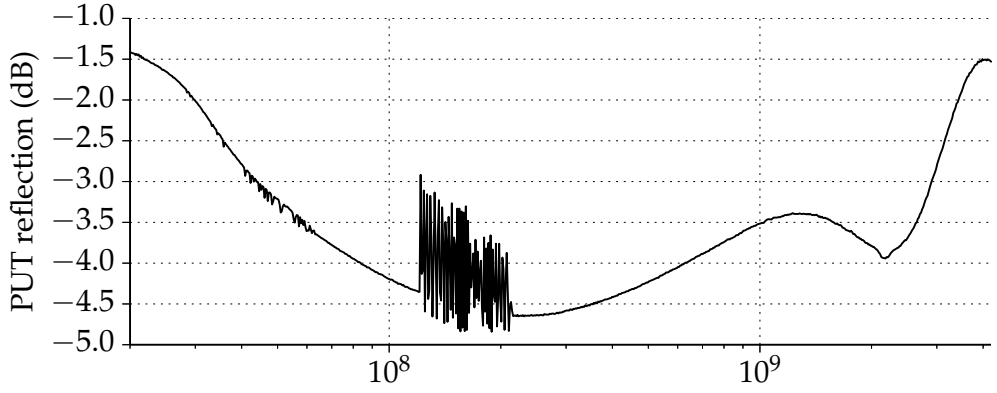


(a) Feed loss $\sqrt{S_{12}S_{21}}$, estimated from the reflection tracking product.

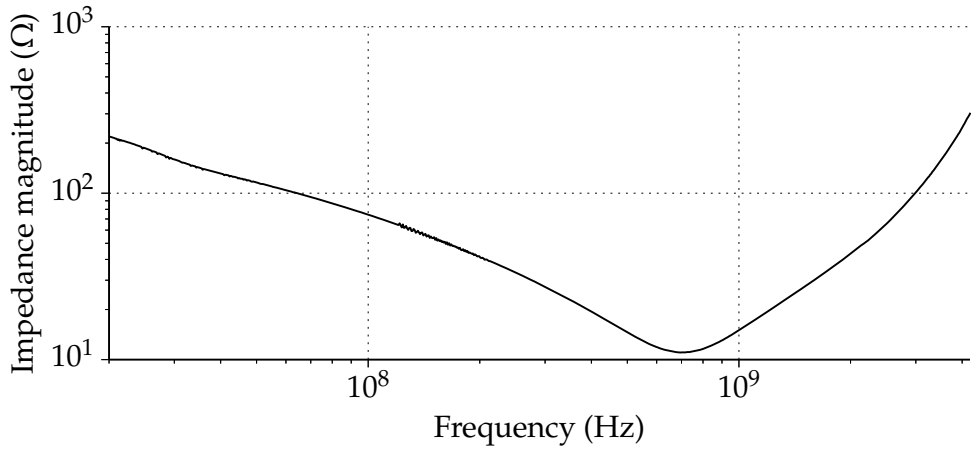


(b) Either-end feed reflection, equal to the source match (S_{22}) and the directivity (S_{11}).

Figure 3.36: Calibration coefficients describing the feed between SMA reference plane (port 1) and PUT (port 2).



(a) In terms of the reflection coefficient Γ_{PUT}



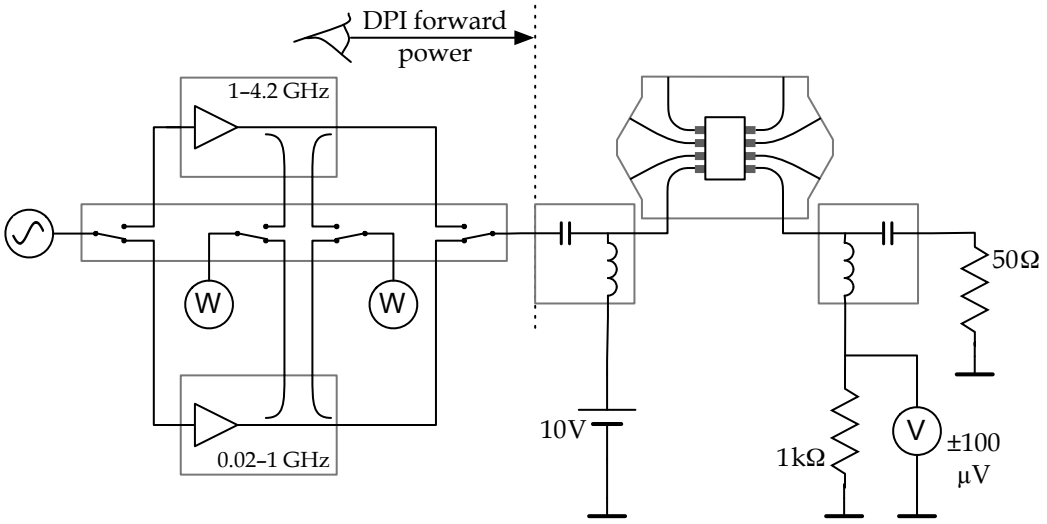
(b) In terms of the impedance Z_{PUT}

Figure 3.37: Linear port behaviour of the LM7805 input (operating point $V_{\mathrm{in}} = 10\,\mathrm{V}$), at the PUT reference plane.

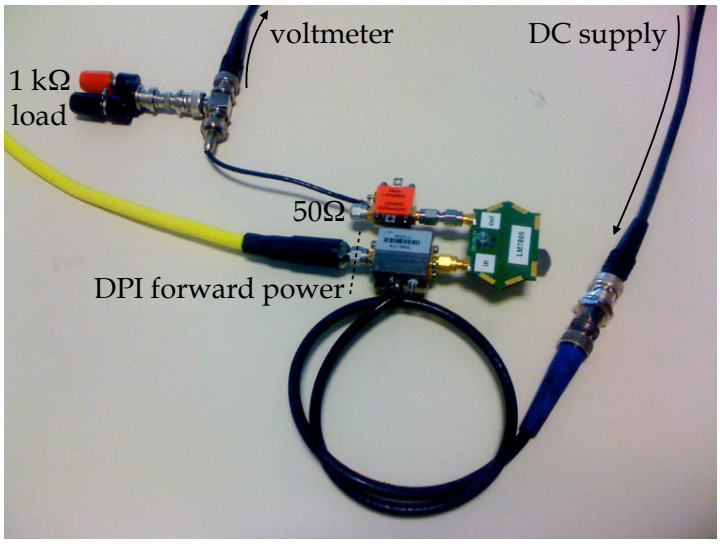
IB Extraction by DPI Measurement

The DPI set-up of Figure 3.38 was made, consisting of a functional and perturbation environment.

Functionally, the voltage regulator IC was powered with 10 V from an Agilent N6700B power supply via the Picosecond 5545 input bias tee. This bias tee was then connected to the extraction PCB, leading to the DUT input. The DUT output voltage was connected to an Agilent 4411A voltmeter via a Mini-Circuits ZX85-12G-S+ bias tee. To decrease the settling time of the output voltage and to put the LM7805 in typical working conditions, it was DC-loaded with 1 kΩ. In order to observe a high susceptibility, the functional criterion was defined less than two orders of magnitude higher than the voltmeter noise



(a) Schematic.



(b) Photo.

Figure 3.38: DPI set-up with lean extraction PCB. The dashed line indicates the initial reference plane of the forward power measurement.

floor: ±100 μVDC output offset. Because of this severe criterion, the non-disturbed voltage drift during the DPI measurement could not be neglected. Therefore, before every frequency-power point, the RF disturbance was turned off, the nominal output voltage was measured again and the voltmeter thresholds were recalculated.

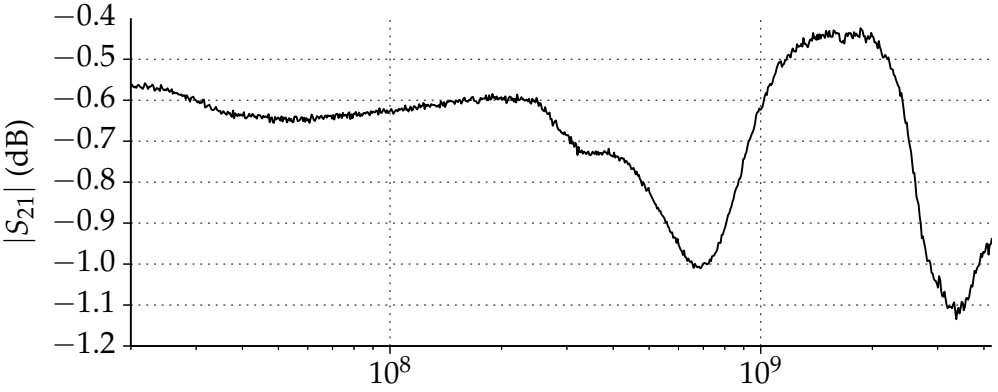
As for the perturbation, two different RF amplifiers were used to obtain the necessary power: the Prâna AP32-DT120 for the $20 - 1000$ MHz range and the Milmega AS0104-3030 for the $1 - 4.2$ GHz range. The amplifiers were routed through an Agilent L4490A switching platform to the DUT input bias tee, which has a 20 GHz bandwidth. The DUT output bias tee has a 12 GHz bandwidth and is loaded with a 6-GHz 50-Ω load.

The DPI measurement was performed as follows. For each frequency in the logarithmic range from 20 MHz to 4.2 GHz, the failure threshold RF power was sought. To speed up the DPI measurement, successive approximation is used: failure is sought by stepping up the generator power in steps of 5, 1, 0.5 and 0.25 dB [62]. After each refinement, the power was lowered to encounter failure while stepping *up*, in order to avoid hysteresis uncertainty. This way, the forward power threshold at the IC pin was measured with 0.25 dB resolution.

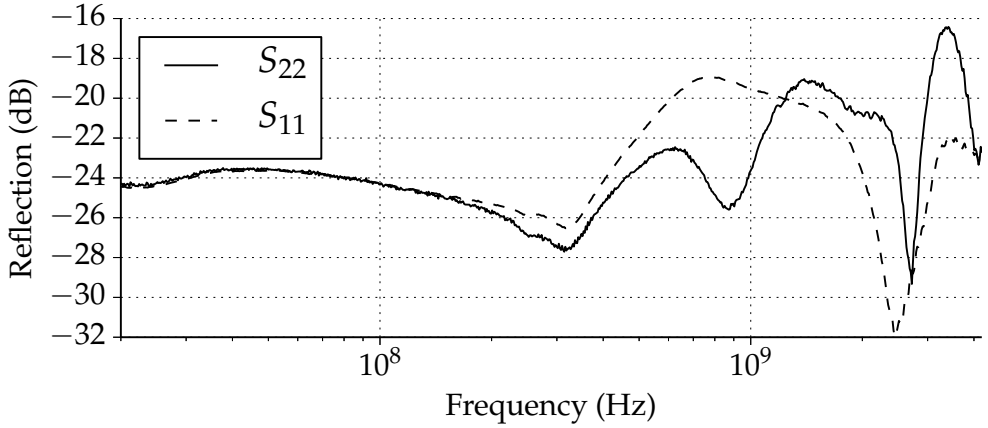
Once the failure was reached, an image of the forward power was obtained from the amplifier's integrated directional couplers. The latter were connected to an Agilent E4419B wattmeter through the L4490A switching platform. To deduce the exact power incident on the input bias tee's RF input, the directional couplers were calibrated on the bias tee input reference plane (the dashed line in Figure 3.38). That is, one probe of the wattmeter was connected through a Mini-circuits BW-N30W50+ 30 dB precision attenuator to the cable, that otherwise led to the input bias tee. The other probe of the wattmeter was connected as usual, measuring the forward power image from the direction couplers. At constant generator power, the frequency was swept and readings of both wattmeters were registered. The attenuation of the precision attenuator was first measured with a VNA and then added to the reading of the first wattmeter probe to obtain the real forward power at the bias tee. Then the difference with the second wattmeter probe was recorded as correction.

To move the reference plane from the bias tee input to the PUT, a model of the injection path between the two reference planes was made. The bias tee S-parameters were measured with the VNA between its input and output SMA reference planes. Then, the feed network of Figure 3.36 was appended using `scikit-rf`. The S-parameters of the resulting network are plotted in Figure 3.39. As can be seen, the PUT-side mismatch is relatively small: S_{22} remains below -18 dB for most frequencies. Therefore, only the injection path loss needs to be taken into account. That is, the injection path $|S_{21}|$ was added to the recorded forward power threshold. This way, the forward threshold power $P_{\text{fwd,th}}$ at the PUT was obtained.

Finally, the transmitted power threshold $P_{\text{trans,th}}$ can be calculated from the forward

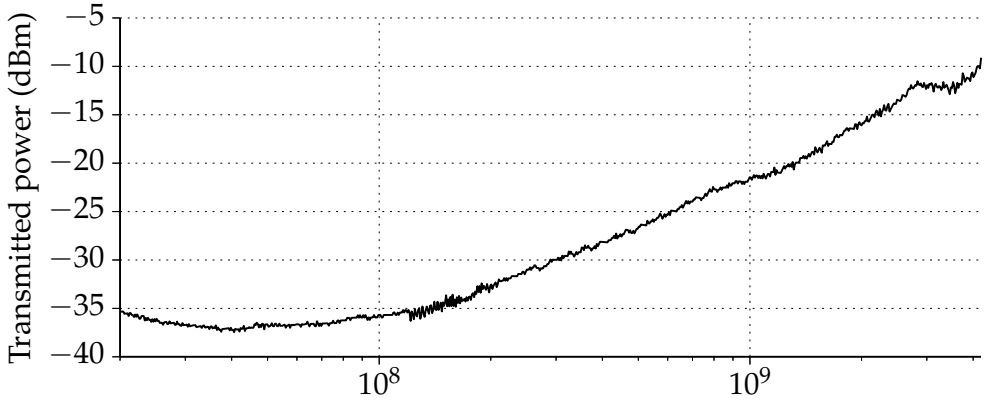


(a) Injection path loss.

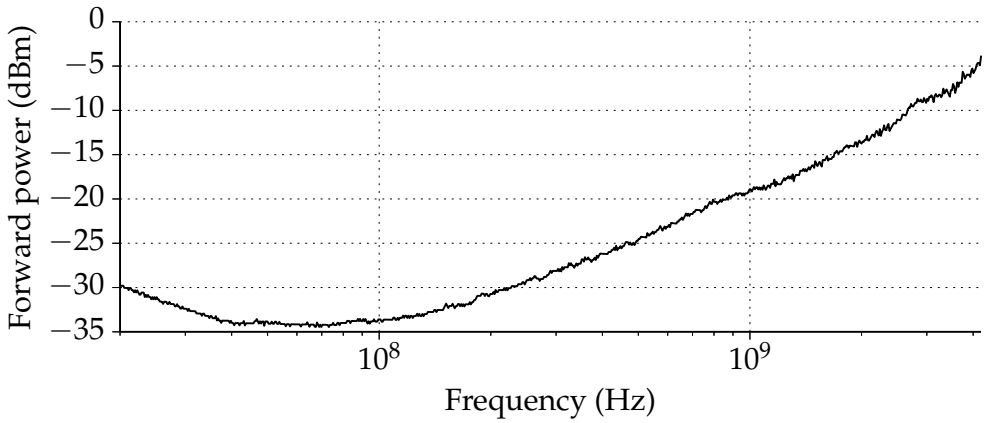


(b) Either-end injection path reflections.

Figure 3.39: Model of the injection path between the input bias tee's RF input (port 1) and PUT (port 2).



(a) In terms of the transmitted power to the PUT.



(b) In terms of the forward power at the PUT.

Figure 3.40: CW immunity of a LM7805 voltage regulator input for a ±100 μVDC output criterion.

power threshold and the PUT reflection coefficient Γ, which was measured above:

$$P_{\text{trans,th}} = P_{\text{fwd,th}} \cdot \left(1 - |S_{11}|^2\right). \tag{3.7}$$

Both thresholds are plotted in Figure 3.40.

Conclusions

An ICIM-CI of the National Semiconductor LM78L05ACM voltage regulator was extracted from measurements according to the lean method of section 3.4. That is, a two-step calibration allowed to measure the PUT impedance and to characterise the feed (connector and trace leading to the PUT). The latter model is then combined with the measured *S*-parameters of a bias tee used during DPI, to correctly move the forward

power threshold reference plane to the PUT, too. Finally, the two models are used to calculate the transmitted power threshold. No significant difficulties were encountered in the extraction process.

To explore the validity domain of the conducted immunity model thus created, the input voltage and complex load could be swept. Aiming to manage IC obsolescence, it would be useful to create ICIM-CIs of equivalent ICs from different suppliers and study the model differences and similitudes.

3.7 Conclusions

In an industrial context, it makes sense to extract ICIM-CI models from measurement. The common IEC 62132-4 DPI test to measure IC immunity is only standardised up to 1 GHz. With increasing frequency, DPI yields uncertain transmitted power thresholds. Therefore, Lafon already proposed an alternative method to determine the transmitted power, by careful modelling and simulation of the used extraction PCB.

Following this approach, a fixture was created to measure and model the SMD passive components that constitute extraction PCBs up to about 12 GHz. Still, the correct modelling of extraction PCBs was foreseen to remain time-consuming and error-prone. Therefore, an alternative method was proposed around a lean extraction PCB, designed to be easy to model. The peripheral circuitry consequently needs to be implemented off-board, on peripheral modules with coaxial connectors. The *S*-parameters of the entire injection path (peripheral modules and the feed on the extraction PCB) can then be found by measuring SOLT standards through eventual peripheral modules. If the injection path has a good source match, only its insertion loss needs to be taken into account. The forward threshold power at the PUT can then be found by subtracting this insertion loss from the threshold found by DPI at the input of the peripheral modules.

To demonstrate this approach, a lean extraction PCB was designed, generic for SOIC8-packaged ICs. In order not to put the peripheral circuitry (on the peripheral modules) too far away, the on-board feeds needed to be short. This suggested bent GCPWs, which is not easy to draw with conventional PCB Computer Aided Design (CAD) tools. Therefore, the PyPCB library was developed, which allows to programmatically generate complex layouts by explicitly propagating constraints. Moreover, this library opens the way for industrialising the method to other packages. Using this library, the PCB layout was described and then generated. The PCB fabricated in a standard FR4 process and equipped with budget SMA connectors. Its feeds exhibited an insertion loss of 1.9 dB at 20 GHz. The worst case far-end crosstalk between neighbouring traces was estimated to be about −14 dB. The reproducibility of the feed was ±0.3 dB, probably because of the inconsistency of the connector-PCB soldering.

Specialising even further, the conducted immunity of a very simple, analog IC was modelled: the LM7805 linear voltage regulator.

Perspectives

The design of the lean extraction PCB necessitated a clear definition of the model boundaries. A two-dimensional definition of reference *lines* was agreed upon with BSMI (cf. Figure 3.27).

However, as the common name suggests, reference *planes* should be defined, thus enclosing the DUT, substrate and ground plane. Indeed, the implicit choice of a substrate and feed waveguides may impact the ICIM-CI. For example, the GCPW guides the superposition of a microstrip and coplanar modes. With increasing frequency, the immunity to incident electromagnetic power may depend on the mode. Further research should indicate whether this is an important issue. Consequently, IEC 62433-4 and IEC 62132-4 will probably need amendment.

Using the findings of this thesis, the IEC 62132-4 standard could already be improved as follows.

The standard states in section 4.1 that "it has been observed that many ICs are most susceptible to the disturbances at quite high reflections," while McDonnel already showed that high reflections cause high measurement uncertainty of the transmitted power [71]. Therefore, Lafon's alternative method of deducing the transmitted power should at least permitted by the standard and might even be required [76]. The offline calibration method proposed in this chapter could also be added as informative appendix. At any rate, it would be a smart step forward to require DPI test reports to state the measurement uncertainty.

The standard is ambiguous as to the physical placement of the bias tee or blocking capacitor in the injection path. For example, section 7.2 states "[Are] placed directly on the testboard: (...) the connection from the end of the transmission line (RF injection port) via the DC block to the DUT [and] DC biasing networks connected to the pin under test." Section 7.3 requires the DC blocking capacitor to be electrically close to the PUT: "The end of the transmission line to the pin of the DUT should be as short as possible. A trace length equal to 1/20 of the shortest wavelength applied is a reasonable target. Shorter trace lengths are advantageous." The formulation is somewhat unclear, but Figure 4 suggest that the output of the blocking capacitor should be close to the PUT. No proof is given as to why that would be 'advantageous'. On the other hand, section 7.5 remarks: "The DC biasing network may also be connected to the injection path offside the printed circuit board."

The latter seems most reasonable: the operator might find it practical to integrate bias tees on the extraction PCB, but he might also consider the modelling difficulty as we did in this chapter. Therefore, the choice should be left to the operator. However, this freedom should consistently be propagated throughout the standard. For example, when presenting the schematics with on-board DC blocks, it should be mentioned that

this is one possible way of implementing bias tees. For another example, section 7.2 should be less categoric about what components should go on the extraction PCB and what may be placed off-board.

On the construction of the bias-tee, the enigmatic remark of section 7.5 "To minimise the effect of mismatching in both cases, the connection from the high impedance decoupling DC-biasing network to the injection path shall be shorter than $\lambda/20$ of the highest frequency in the test (e.g. less than 15 mm for 1 GHz)." could be clarified like so: "As the high frequency impedance of the inductance of the biasing network is high, the trace between the inductance and the matched injection path forms a stub. To keep the effect of this stub negligible, it shall be shorter than $\lambda/20$ of the highest frequency in the test (e.g. less than 15 mm for 1 GHz)." An illustration of placement and construction of a bias tee could clarify what dimensions are critical and what dimensions are not. More in general, clear definitions of components and reference planes could make the standard more comprehensible.

To characterise the set-up, section 7.4 requires the attenuation between the coaxial injection port and the PUT reference plane to be measured less than 3 dB. As the transmitted power is measured at the output of the directional coupler, the systematic error could be reduced by including the cabling and eventual off-board bias tees in this measurement. Moreover, the higher the frequency is, the harder it is to solder a connector to the PUT reference plane. Therefore, section 7.4 might also allow offline calibration of the feed, leading to its calculated $|S_{21}|$.

Finally, section 4.2 mentions 'test selectivity' as an important goal of the DPI. It would be good to elaborate this requirement as an upper bound to the far-end crosstalk, for example −10 dB. To measure the far-end crosstalk, the method used in section 3.5 of this thesis could be proposed. At any rate, the test report should comment on the difference between the immunity of neighbouring pins and state whether the PCB's crosstalk could play a role in the observations.

CHAPTER 4

PCB Radiated Immunity

Abstract. Except for a general trend of rising frequencies, there is only little concrete proof for the relevance of IC conducted immunity modelling beyond 1 GHz. Therefore, the cascade of a Grounded CoPlanar Wave-guide (GCPW) trace and an SOIC8 lead frame is studied with full-wave simulation, to find out that up to 10 GHz, most energy enters the die via the trace. Similarly, the immunity of a microstrip trace and an LM7805 voltage regulator is predicted up to 4.2 GHz by concatenating the models developed in the former chapters. Although this model neglects the radiated immunity of the IC itself, the prediction corresponds with GTEM-cell measurement to within 2.1 dB average error. These experiments suggest the dominant-conduction hypothesis to hold true well beyond 1 GHz.

4.1 Introduction

Now that modeling IC conducted immunity beyond 1 GHz proved possible, is it also *useful*? That is, in a realistic system that contains the IC, do perturbations predominantly perturb the IC by conduction or rather by radiation? How does this depend on frequency?

The little literature that directly or indirectly treats the question will be reviewed in section 4.2. For little is published on the matter, a qualitative exploration by full-wave simulation will be performed in section 4.3. Alternatively, the radiated immunity of a simple PCB will be predicted in section 4.4, while neglecting the radiated immunity of the IC. If nonetheless, this prediction correlates well with measurement, this suggests dominant conduction. Conclusions will be drawn in section 4.5.

4.2 State of the Art

Little explicit conclusions are published on the dominant coupling mechanism of real-life perturbations into ICs. Lagos and Fiori explain why they believe the dominant-conduction hypothesis to hold up to several GHz: "radiated EM fields also couple with the wiring interconnects (leadframe and bonding wires) of integrated circuits, but induced voltages are usually negligible as long as package interconnects are significantly shorter than the interference minimum wavelength. Given that the maximum size of mass-production IC packages is usually smaller than a few centimeters, the disturbance collected by the package interconnects can be neglected up to several gigahertz, hence (. . .) the direct coupling of external EM fields to IC interconnects (at package and chip level) will be neglected." [21] With similar reasoning, Lafon et al. state that the direct coupling to the IC can be neglected up to at least 4 GHz [76].

There is some indirect proof, however, for dominant conduction beyond 1 GHz.

Ramdani et al. describe and explain industrial trends in the EMC of ICs. Because of the steady miniaturisation, ICs can be sped up, which in turn increases power consumption. To counter the latter effect, the supply voltage is steadily lowered, which inherently lowers the noise margin for digital circuitry, hence lowering IC immunity. Simultaneously, the potential aggressors increase because of the spectacular digitalisation of our society. Also within products, the threat of aggressors increases because of the accelerating communication buses and switching noise on supply rails. Consequently, IC customers push for increasing immunity. This might explain their expected extension of the frequency range of conducted immunity modelling and measurement techniques [8].

Indeed, the publication of research on DPI extension up to 2 GHz in 2012 [91] and up to 18 GHz in 2013 [73], implies that IC conducted immunity beyond 1 GHz is industrially interesting. For example, the latter authors show a +20-dBm forward power threshold observed around 17 GHz on an Low DropOut voltage regulator (LDO). Maurice and Pigneret reports the conducted susceptibility threshold of a simple digital circuit to be $+20$ dBm of transmitted power in the $2 - 4$ GHz band [98]. The current mirror studied by Loeckx starts to offset around 5 GHz with less than $+10$ dBm forward power [58]. McConaghy shows increased conducted susceptibility of a 1990 logic circuit above 10 GHz [99]. However, none of the authors prove that these conducted perturbations could correspond with real-life situations.

Reciprocally, the absence of standards on IC radiated immunity models is also interesting. The IEC 62433-4 Integrated Circuit Immunity Model for Conducted Immunity (ICIM-CI) was recently approved as New Proposal (NP). No such proposal for IC radiated immunity was made yet. This could be partially due to little actual, industrial importance.

Finally, the IC interconnects are sometimes believed to strongly attenuate incoming perturbations above some GHz. However, Chun, Pham, Laskar, and Hutchison

measured the −3-dB bandwidth of SOIC8-packaged thru-lines to be 12 GHz [100]. The pseudo-physical model does not include inductive coupling between neighbouring bondwires and as such, it cannot be trusted to predict the physical path of the power: maybe the power is not really conducted to the die, but capacitively coupled to all pins at the same time, for example. Nonetheless, this measurement is an indication that significant power can couple on and off the die, well beyond 1 GHz.

On the other hand, there is also indirect evidence for dominant radiation beyond 1 GHz.

For example, the bondwire plus leadframe inductance of wire-bonded packaging is in the order of some nH. For flip-chip packages, the 'lead' inductance is lower, but still in the same order of magnitude [101]. 2 nH, for instance, equals 251 jΩ at 20 GHz. In other words, the die starts to electrically float. Put differently, with rising frequency, it becomes harder for conducted functional signals and perturbations to arrive at the die. This might explain the popularity of Antenna on Chip (AoC) solutions for 60 GHz [102], but also Antenna in Package (AiP) for 2.4 GHz [103]. This suggests significant direct coupling of (functional) radiation to chip-size structures.

Although there are no standardised IC radiated immunity models, there are various measurement methods, like the IEC 62132-6 Local Injection Horn Antenna (LIHA), up to 10 GHz, the IEC 62132-9 Near Field Scan of Immunity (NFSI) and the IEC 62132-8 IC stripline, up to 6 GHz. This suggests that IC radiated immunity is an interesting quantity.

Perdriau, Maurice, Dubois, Ramdani, and Sicard estimate the radiated immunity threshold of a particular digital circuit to be as low as −5 dBm transmitted power at 20 GHz [104].

In summary, there is no hard proof for nor against the real-life relevance of IC conducted immunity measurement beyond 1 GHz. However, below a certain frequency, radiated perturbations can be expected to mainly couple to the trace and then be conducted to the die. Above a certain frequency, perturbations can be expected to be mainly coupled directly to the die. In between these frequencies, there must be a conducted-radiated transition frequency, which will depend on the trace and IC geometry and materials.

Therefore, the question is: what is the conducted-radiated transition frequency?

4.3 Explorative Simulation

To quickly get a qualitative idea about the dominant coupling mechanism as function of frequency, a full-wave solver was employed as follows. The conducted-radiated transition frequency will be determined for a modern trace-IC configuration that has a low expected transition frequency. That way, if even that configuration exhibits a transition frequency above 1 GHz, all other modern cases may be expected to have a transition frequency above 1 GHz.

In modern electronics, traces with or without ground planes are applied, with coplanar ground planes and/or ground planes beneath the trace. From all these configurations, a Grounded CoPlanar Wave-guide (GCPW) is expected to be the worst antenna because of the nearby ground planes. Consequently, little radiated perturbation will be captured with respect to the IC, hence a low transition frequency.

As for the IC, the bigger the package, the more coupling can be expected. This pleads for packages with a big lead frame, like a 40-pin Dual Inline Package (DIP). However, mainstream electronics are moving towards smaller Surface Mount Technology (SMT) packages like Quad Flat package No leads (QFN) and Ball Grid Array (BGA). To strike a realistic balance, popular in automotive because of its reliability, an SOIC package was chosen.

The trace was modelled under CST as a 0.6 mm, 50 Ω coplanar trace. Again, to minimise the antenna efficiency of the trace, it was terminated in a discrete characteristic (50 Ω) load at the near end.

To obtain a realistic IC model, the SOIC8 package of a National LM7805 was opened (Figure 4.1a) and conscientiously reproduced under CST (Figure 4.1b). The lead frame was modelled as Perfect Electrical Conductor (PEC). A bondwire was though up, and a 50 Ω discrete port was installed between the end of the bondwire and the IC's internal ground plane. The package was modelled as epoxy resin. The structure was illuminated by a 1 V/m endfire plane wave. The power arriving on the die was monitored.

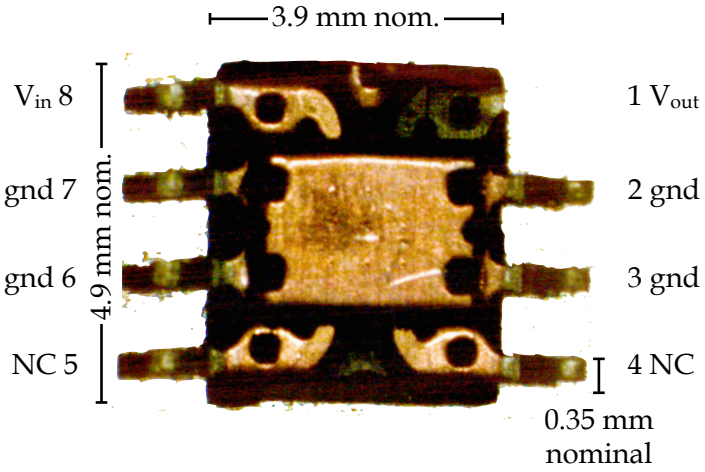
By a parametric sweep of the trace length, the coupling via the trace could be qualitatively identified.

Not to our surprise, a longer trace caused more coupling at low frequencies (Figure 4.2). At about 20 GHz, the trace length does not seem to change the coupling anymore, which suggests that all power couples directly to the package and the bondwire. For particular lengths and frequencies, destructive interference seems to occur. The transition frequency seems to be between 10 GHz and 19 GHz, but clearly above 1 GHz.

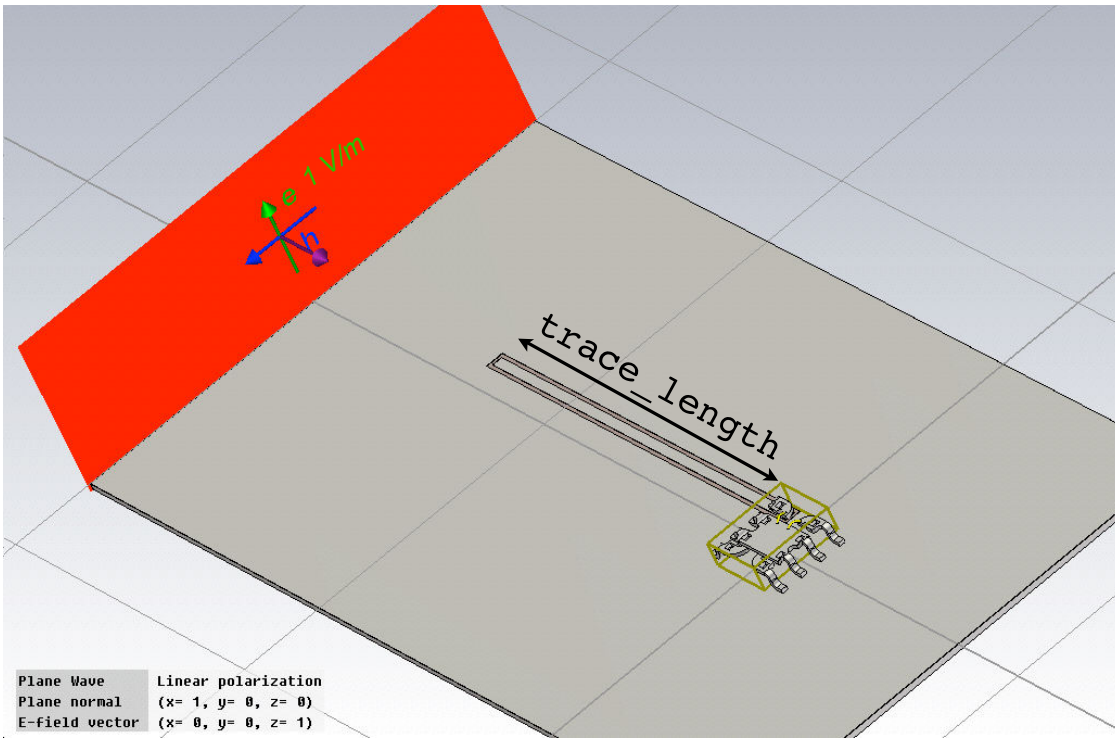
It be noted that side fire illumination could have coupled much less to the trace, and thus have revealed a much lower transition frequency. However, as all incidence angles may occur in practice, it can still be concluded that for some angles, conduction is dominant. At least for these cases conducted immunity IC models are required.

To summarise, a qualitative study of the dominant coupling mechanism was performed on a modern trace and IC. Despite the GCPW, the lossy substrate and the matched load, the coupling seems to be predominantly conducted, at least up to 10 GHz.

However, we have no analytical reference to validate the simulation against and we have no insight in the influence of all geometric parameters. Therefore, more proof is needed.



(a) Macroscopic photo of a mechanically opened National Semiconductor LM78L05ACM voltage regulator. Nominal dimensions are taken from the product data sheet.



(b) Simulation of reproduced leadframe, GCPW and plane wave as entered under CST.

Figure 4.1: Simulation set-up to study the contribution of PCB trace, package and bondwire to the field-to-die coupling.

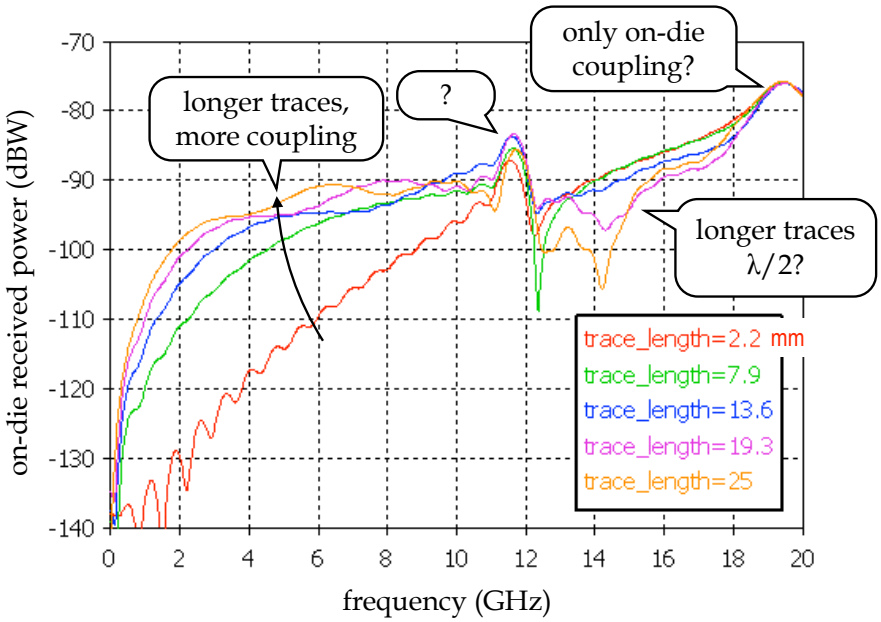


Figure 4.2: Simulation result: on-die received power as function of frequency and trace length for 1 V/m far-field illumination.

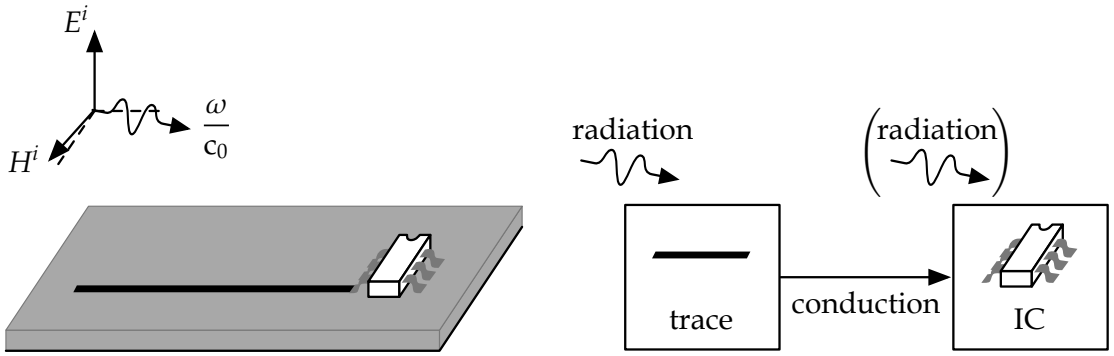
4.4 Cascading Trace and IC Models

The dominant coupling mechanism will now be studied using the overarching approach of this thesis, as follows. The radiated immunity of the cascade of a trace and an IC will be predicted by cascading the models developed in Chapter 2 and 3. That way, the radiated immunity of the IC is neglected, as illustrated in Figure 4.3b. Next, this prediction will be compared to measurement, where both trace and IC are exposed to the radiated perturbation. To the extent that the prediction corresponds well with the measurement, the radiated immunity of the IC is negligible.

To allow for measurement, a demonstrator PCB with the LM7805 voltage regulator will first be developed. Knowing the demonstrator, two measurement configurations will be decided upon. For each configuration, the field-to-trace coupling will then be calculated. By slightly adapting the IC conducted immunity, as measured in Chapter 3, the radiated immunity of the whole will be predicted for both configurations. Finally, these predictions will be compared to measurements.

Demonstrator Design

As must conducted immunity tests, any radiated immunity test must provide a perturbation and a functional environment. The perturbation environment allows for a well-defined supply of radiated perturbation. The functional environment puts the



(a) Perspective on the system. (b) Weakly-coupled model of the system.

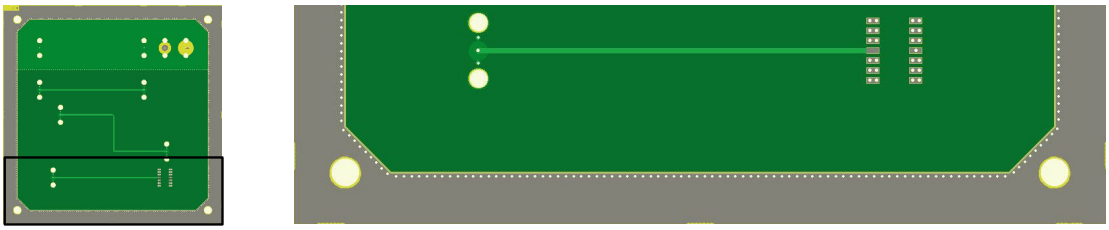
Figure 4.3: Illumination of the system: a trace connected to an IC (repetition of Figure 1.6).

Device Under Test (DUT) in a typical or worst case application and allows for failure surveillance. In this particular case, the demonstrator geometry was chosen such, that the field-to-trace coupling model and the ICIM-CI developed in this thesis could model the entire demonstrator.

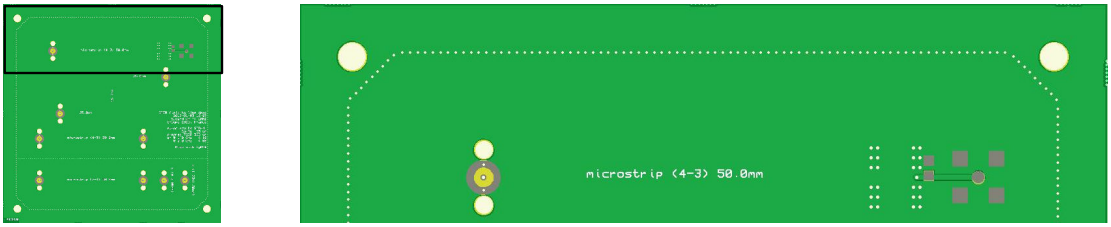
As for the perturbation environment, the trace could be any multi-segment microstrip, given the model developed in Chapter 2. However, at the time of fabricating the demonstrator, the modified Taylor cell was not yet proven by measurement. Therefore, to reduce the number of uncertainties, a single microstrip segment of 5 cm was chosen. Similarly to the field-to-trace measurements, the trace was put on a 10×10 cm PCB for illumination in a Gigahertz Transverse ElectroMagnetic (GTEM) cell.

The IC was chosen to be the LM7805 linear voltage regulator, of which the input's immunity was modelled in section 3.6. The footprint was chosen to be similar to that used on the extraction PCB. Also, the substrate was chosen to be the same as on the extraction PCB: 360 μm Flame Retardant 4 (FR4). However, to challenge the independence of the model to the waveguide design, another ground plane was defined. The trace leading to the regulator's input is a microstrip, so no coplanar ground is used in the demonstrator. Also, no ground plane is put on the outer PCB layer, just beneath the IC package, contrary to the extraction PCB. To provide a low-impedance ground, all ground pads were equipped with two in-pad vias.

As for the functional environment, the regulator should be supplied with a DC supply voltage. Therefore, the other end of the illuminated trace is equipped with a precision Molex SMA connector, allowing to connect a bias tee for DC supply. As the connectorised bias tee can be measured with a VNA, the RF charge impedance can also be well-known. Because the ICIM-CI describes the immunity of the IC input, the trace leads to the IC input. To monitor failure, the regulator output DC voltage should be measured. To avoid coupling of the radiated perturbation to the IC's output, which is not modelled, an in-pad via directly brings the signal to the outside of the GTEM cell. It



(a) Bottom side (illuminated by the GTEM cell).



(b) Top side (outside of the GTEM cell).

Figure 4.4: Eurocircuit pre-production visualisation of the trace-IC demonstrator. Dark grey signifies gold-plated outside copper.

might prove necessary to supply an output capacitor for stability, so a suitable footprint was provided. The trace being at the outside of the GTEM cell, a precision Molex SMA can no longer be used, so a budget SMD SMA connector was used. Similarly, a bias tee with a 50 Ω load can be applied to correspond with the model extraction environment. The DC output of the bias tee allows for monitoring of the voltage offset.

The resulting demonstrator PCB is shown in Figure 4.4. The footprint of the precision Molex SMA connector was optimised using CST to provide a good transition from microstrip to coax. A cross-section of the PCB is shown in Figure 4.5. Notice how the models for field-to-trace coupling and IC immunity describe touching regions. Notice also that the microstrip-to-SMA transition, the SMA connector and the input bias tee are not modelled by either model. Therefore, they should be represented as the charge impedance connected to the left end of the field-to-trace coupling model.

Measurement Configurations

Given this demonstrator PCB, equipped with an LM7805 voltage regulator, there are two remaining degrees of freedom. Firstly, the RF charge impedance connected to the input bias tee. Because this charge is connected to the RF SMA connector of the input bias tee, it is easy to experiment with this variable. Secondly, the 10×10 cm (square) PCB can be easily rotated by quarters of a turn.

To start with a simple case, the PCB is placed such, that the trace is end-fire illuminated with the IC at the far end, as shown in Figure 4.6a. As this configuration was shown before to induce the worst case terminal voltage for high frequencies, the highest

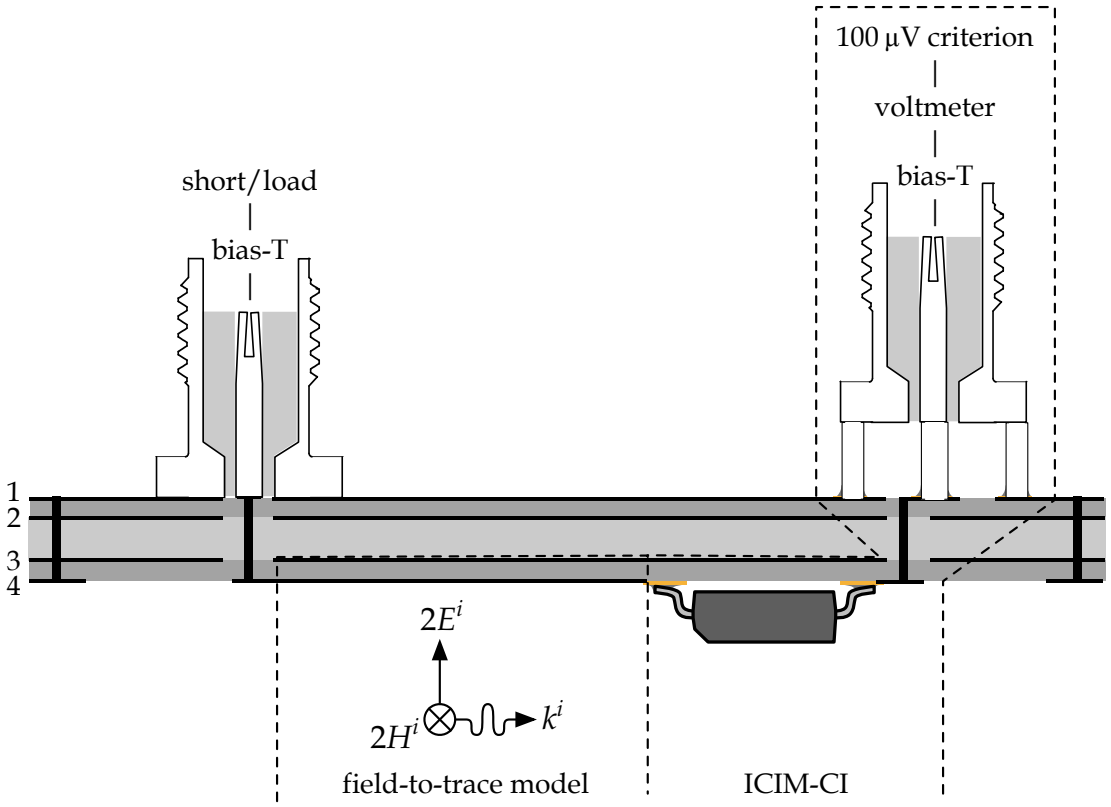
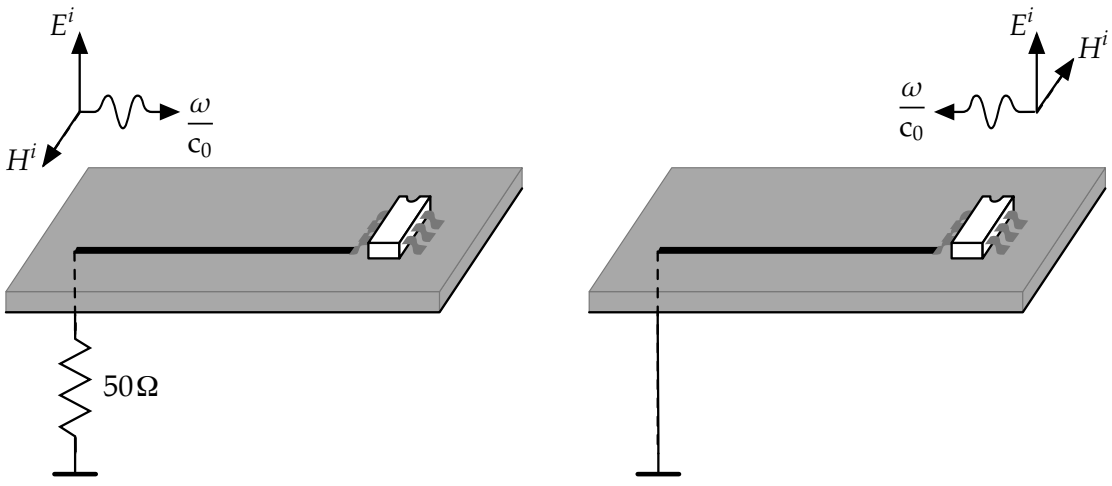


Figure 4.5: Longitudinal cross-section of the trace-IC demonstrator (not to scale). Model boundaries are dashed.



(a) 'Matched' (b) 'Shorted'

Figure 4.6: Measurement configurations.

susceptibility can be expected. To exclude modelling problems with the near-end charge impedance, the bias-tee was terminated in a broadband 50 Ω load. This configuration (near end: 50 Ω charge, far end: LM7805 Pin Under Test (PUT)) will be referred to as 'matched'.

To challenge the modelling of a non-characteristic charge impedance, a short calibration standard is connected to the input bias tee, as shown in Figure 4.6b. Because reflections are now expected, the lower high-frequency coupling to the near end may still suffice to observe susceptibility. Therefore, the card is rotated by 180°; the trace is still end-fire illuminated, but the IC is now located at the near end. This configuration (near end: LM7805 PUT, far end: short standard) will be referred to as 'shorted'.

Field-to-trace Coupling Calculation

Using the field-to-trace coupling model developed in Chapter 2, the trace terminal voltage induced by a given field on given terminal impedances can be calculated.

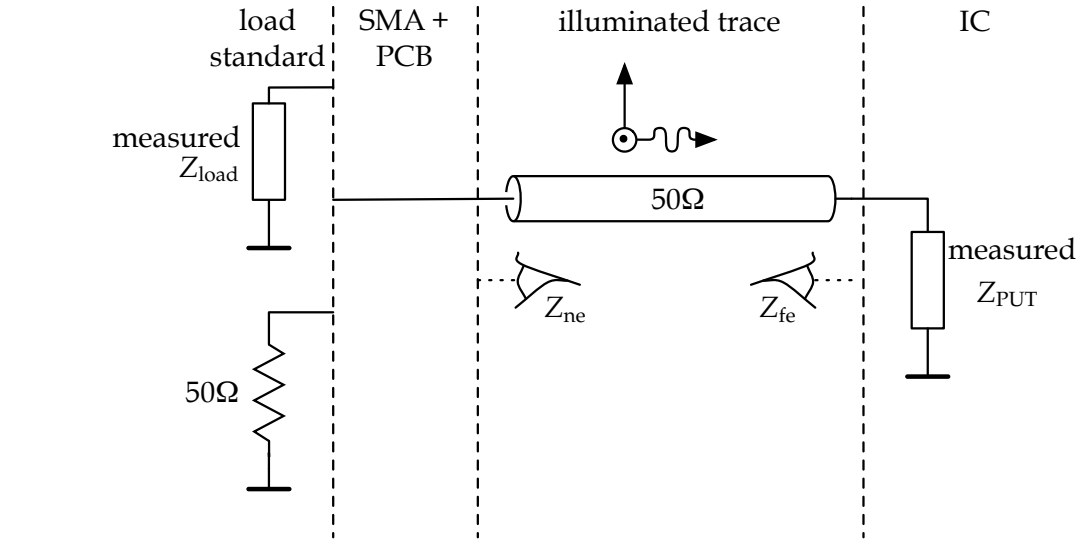
The trace is well-known: a 5 cm, end-fire illuminated microstrip on a 360 μm FR4 substrate. The field will be the field strength, that would be generated by 1 V on the GTEM cell septum.

To determine the terminal impedances as seen by the illuminated trace, the geometry of Figure 4.5 must be carefully inspected. At the right side (at the PUT), the field-to-trace model is flush with the ICIM-CI. That is, the right-end impedance coincides with the reference plane of the Passive Distribution Network (PDN) extracted from measurement in section 3.6. Therefore, the ICIM-CI's S_{11} only needs to be converted to Z_{11}.

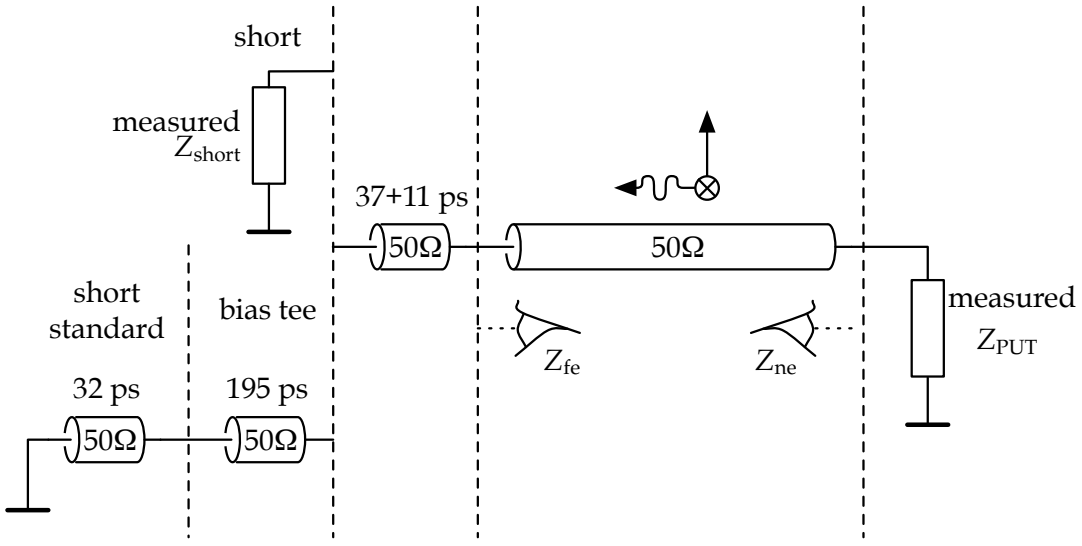
At the left side, however, the trace is connected to an SMA connector through a microstrip-to-coaxial transition. As both were designed to resemble a 50 Ω waveguide, they may be modelled as electrical delays. As calculated in Chapter 2, the connector has a 37 ps delay and the transition about 11 ps. To exclude non-idealities of the used 50 Ω standard or the short, the impedance of both will be measured with a VNA through the bias tee. The resulting model is shown in Figure 4.7. Both charges are measured at the bias tee's 'RF+DC' output with a VNA, then retarded by $37 + 11$ ps. The resulting impedances are plotted in Figure 4.8.

Alternatively, simplified charge models can be used. For the matched configuration, if the standard is perfect and the bias tee a 50 Ω waveguide, the simplified model shown at the top of Figure 4.7 may be used. As can be seen from Figure 4.8a, this seems a reasonable approximation. For the shorted configuration, the nominal delays of the short standard and the bias tee can be used to retard a perfect short circuit.

Again, the `field2line` framework developed in Chapter 2 was used to numerically calculate the induced voltage V_{PUT} at the IC's PUT.

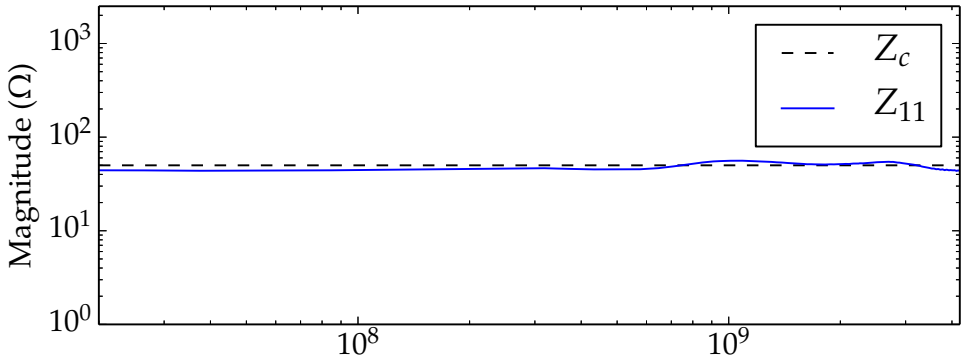


(a) 'Matched'

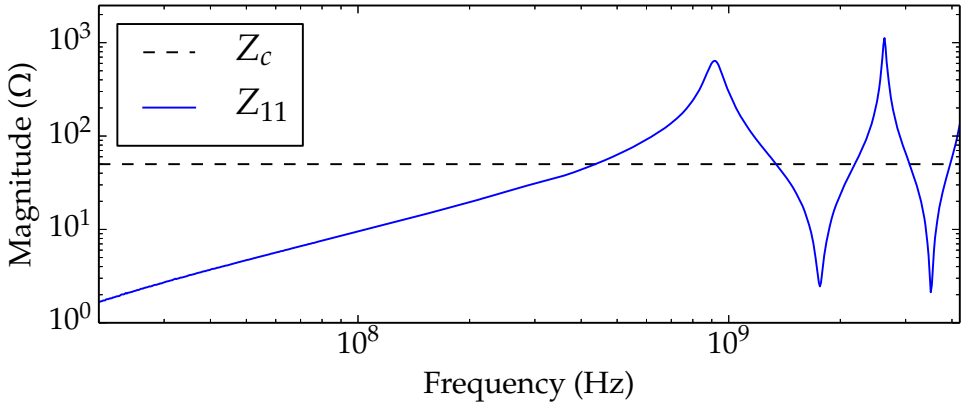


(b) 'Shorted'

Figure 4.7: Model of the illuminated trace leading to the PUT of the IC. At the left, the impedance of any charge measured at its SMA reference plane can be used. Alternatively, simplified models of the load and short standards can be used.

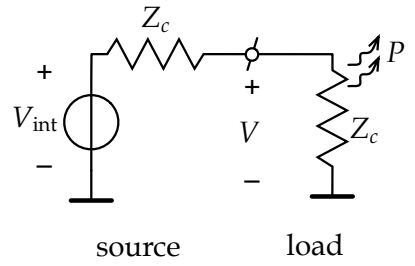


(a) Measured impedance of the Picosecond 5545 bias tee 'AC+DC' port (the 'AC' port was connected to the other port of the VNA), delayed by $37 + 11$ ps.



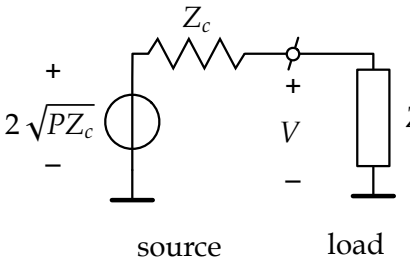
(b) Measured Agilent 85052D-60006 male short, seen through the Picosecond 5545 bias tee, delayed by $37 + 11$ ps.

Figure 4.8: Charge impedances Z_{charge}, which will be entered at one end into the illuminated trace model.



$$P = \frac{V^2}{R} = \frac{\left(\frac{1}{2}V_{\text{int}}\right)^2}{Z_c}$$
$$V_{\text{int}} = 2\sqrt{PZ_c}$$

(a) First step: find the internal source voltage for a given forward power using a matched load.



$$V = 2\sqrt{PZ_c}\frac{Z_{\text{PUT}}}{Z_{\text{PUT}} + Z_c}$$

(b) Second step: use this internal voltage to find the load voltage for an arbitrary load.

Figure 4.9: Conversion of forward power to voltage.

Radiated Immunity Calculation

To calculate the forward power immunity threshold at the GTEM cell input, the above models will now be concatenated.

The first step is to interface the field-to-trace model and the ICIM-CI. The former yields a voltage V_{PUT} (for 1 V at the septum), while the latter yields a threshold net power transmitted to the PUT. The choice was made to adapt the ICIM-CI, by converting the transmitted power threshold to a threshold voltage (cf. Figure 4.9):

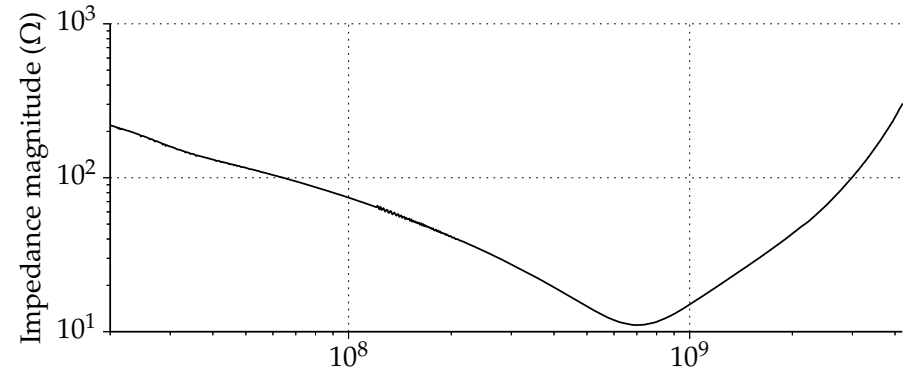
$$V_{\text{th}} = 2\sqrt{P_{\text{fwd,th}}Z_c}\frac{Z_{\text{PUT}}}{Z_{\text{PUT}} + Z_c}\,, \tag{4.1}$$

where $P_{\text{fwd,th}}$ is the forward threshold power at the PUT reference plane, as observed in DPI, Z_c is the characteristic impedance of the DPI set-up and Z_{PUT} is the IC's impedance as measured with a VNA. This calculation is graphically performed in Figure 4.10.

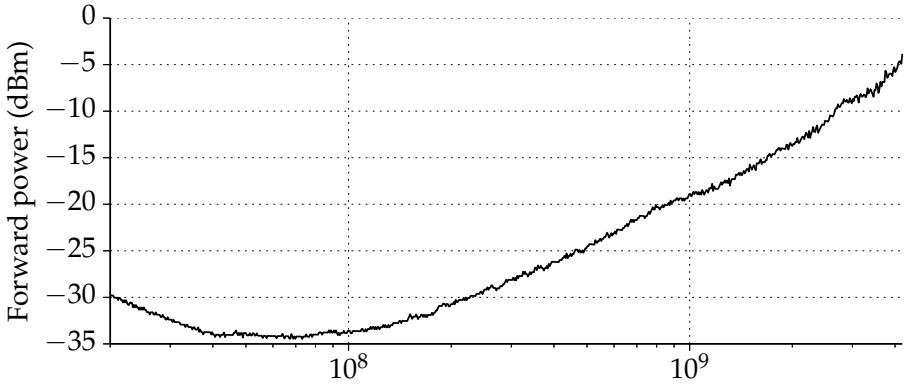
The next step is to calculate the septum threshold voltage:

$$V_{\text{th,septum}} = \frac{V_{\text{th}}}{H}, \tag{4.2}$$

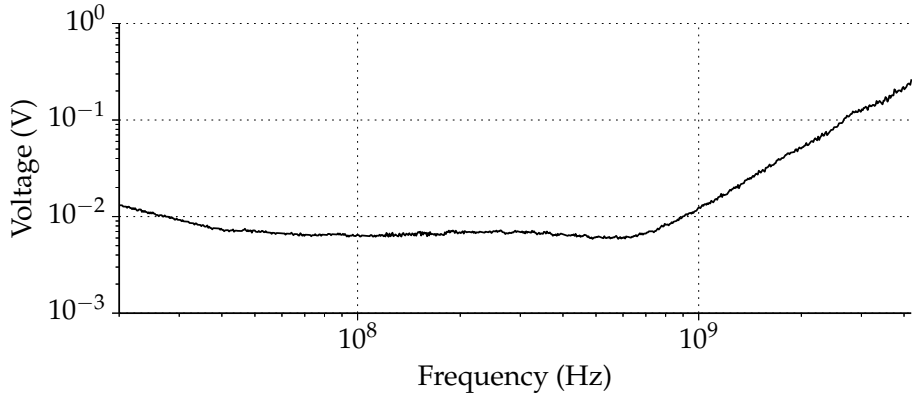
where H is the voltage transfer from septum to PUT, as given by the field-to-trace coupling model. It be noted that H may be a random variable, because of the phase



(a) IC impedance Z_{PUT} as measured with the VNA for $V_{\text{in}} = 10\,\text{V}$ on the SOIC8 extraction PCB, calibrated using the calibration kit (repetition of Figure 3.37b).



(b) IC immunity measured with DPI (100 μVDC criterion), corrected for the SOIC8 extraction PCB using the calibration kit (repetition of Figure 3.40b).



(c) IC immunity in terms of threshold voltage.

Figure 4.10: Calculation of the IC immunity in terms of threshold voltage, calculated according to (4.1).

uncertainty of the GTEM cell reflection. Consequently, $V_{\text{th,septum}}$ may be stochastic, too. This calculation is performed graphically in Figure 4.11.

Finally, this septum threshold must be converted to a forward threshold power incident on the GTEM cell input:

$$P_{\text{fwd,GTEM,th}} = \frac{V_{\text{th,septum}}^2}{Z_{\text{c,GTEM}}} = \frac{(V_{\text{th}}/H)^2}{50.0}. \tag{4.3}$$

This calculation graphically simply corresponds to a vertical shift and scale on a logarithmic axis.

Comparison with Measurement

Now that a quantitative prediction is calculated, the measurement can be performed. The measurement set-up and procedure will be described and the measurement results will be compared to the prediction.

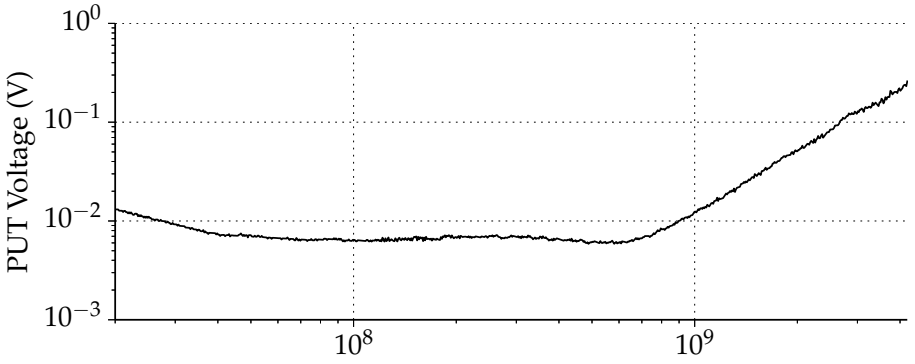
The demonstrator PCB was fabricated and assembled as can be seen in Figure 4.12a. Then, the PCB was placed on the GTEM cell opening as shown in Figure 4.12b. Similarly to the DPI measurement conditions, the voltage regulator IC was powered with an Agilent N6700B power supply via the Picosecond 5545 input bias tee. The output voltage was coupled out via a Mini-Circuits ZX85-12G-S+ bias tee, loaded with 1 kΩ and then connected to an Agilent 4411A voltmeter. The RF perturbation coming from various amplifiers was connected to the GTEM cell input. In the 'matched' configuration, the 'RF' terminal of both bias tees was terminated in 50 Ω. For the 'shorted' configuration, an Agilent 85052D-60006 short standard was connected the 'RF' terminal of the input bias tee.

The radiated immunity in the GTEM cell was measured similarly to the DPI. That is, with successive approximation and a final 0.25 dB forward power resolution. Because of the subtle failure criterion of ±100 μVDC, the output voltage drift made the measurement time-variant. To counter this effect, the nominal output voltage had to be measured again before each point, like during DPI.

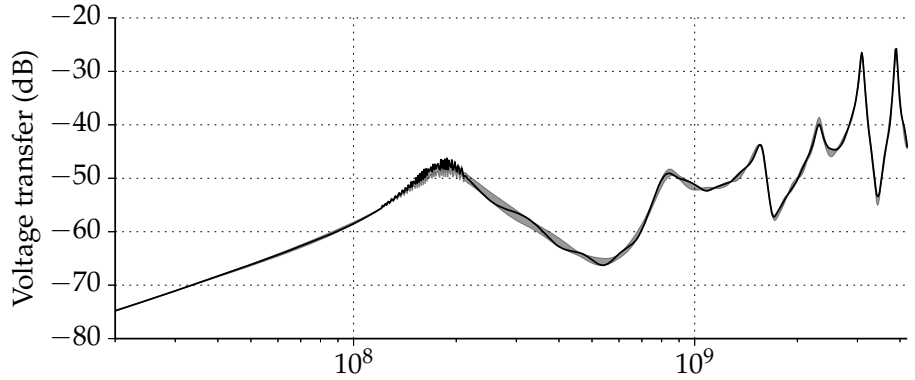
Again, similarly to the DPI measurement, the Prâna and the Milmega amplifiers were used to cover the 20 MHz to 4.2 GHz frequency range. The forward power at the directional couplers was compensated with a calibration to obtain the forward power at the input of the GTEM cell.

The immunity measurement result is compared with the prediction for both configurations in Figure 4.13.

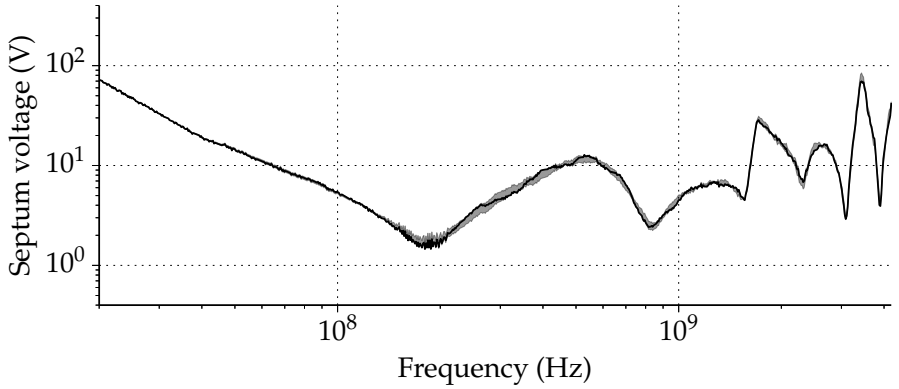
The peak in the measurement at 290 MHz occurred intermittently, both in DPI and GTEM measurements. Probably, the voltage regulator without external output capacitor is marginally stable around this frequency, and the disturbance may excite



(a) PUT failure threshold (repetition of Figure 4.10c)

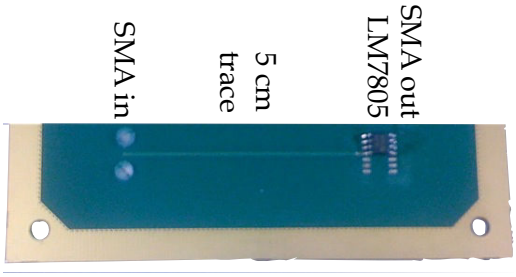


(b) Voltage transfer from GTEM septum to PUT.

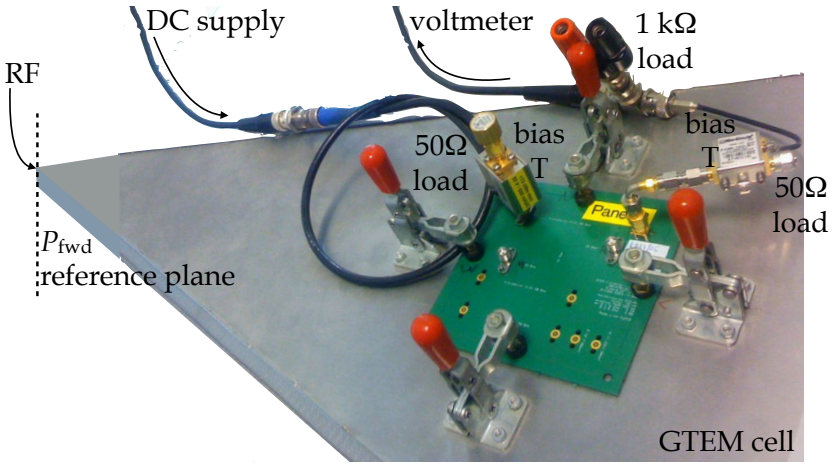


(c) Consequent septum failure threshold.

Figure 4.11: Calculation of the radiated immunity for the shorted configuration (difference on above scales).



(a) Illuminated side of the demonstrator PCB, consisting of trace and IC.



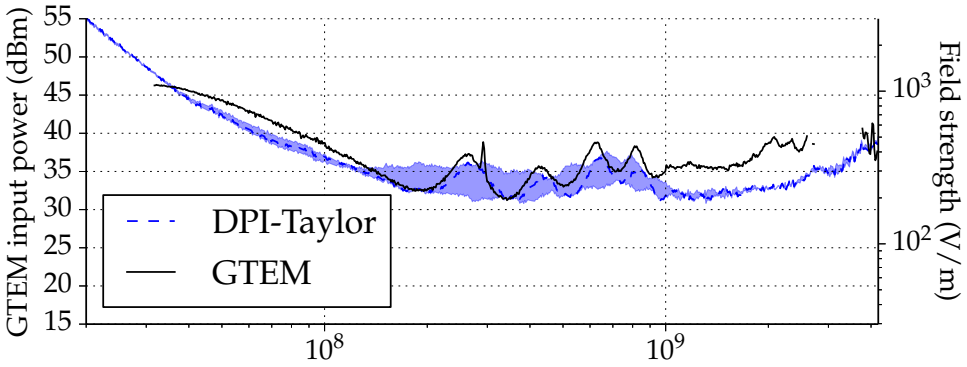
(b) Demonstrator PCB placed on the GTEM cell and connected to peripherals.

Figure 4.12: Measurement of the radiated immunity of the demonstrator PCB in the 'matched' configuration.

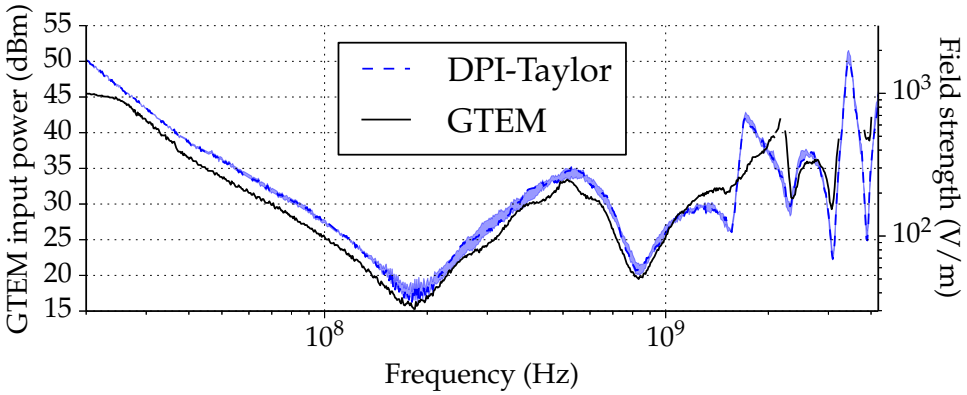
this oscillation. Notice also how the GTEM measurement flattens around the alleged +46 dBm (40 W) at low frequencies. The Prâna amplifier used in this range has an output 3 dB compression point at 25 W, so significant harmonic distortion can be expected. As can be seen from the prediction, higher harmonics encounter lower immunity, so the observed failure could be caused by harmonics. This might explain the low-frequency flattening.

The comparison with prediction was repeated for simplified charge models, to investigate the importance of accurate charge models. Instead of the VNA-measured impedance, the idealised models of Figure 4.7 were used. To check the method, an oversimplified charge model was applied in the 'shorted' case: a 0 Ω without a 32 + 195 ps delay. This charge model is expected to predict resonances that are significantly frequency-shifted.

The results are numerically compared in Table 4.1. Notice that the averages are calculated along the log-sampled frequency range from 20 MHz to 4.2 GHz, wherever failure could be observed.



(a) 'Matched' configuration (near end: matched load, far end: LM7805 input).



(b) 'Shorted' configuration (near end: LM7805 input, far end: short standard).

Figure 4.13: Prediction and measurement of the radiated immunity of a 5 cm trace and an LM7805 voltage regulator. The shaded area represents the uncertainty introduced by the reflection phase of the GTEM absorbers. Gaps in the black curve signify that no susceptibility could be observed with the available RF power.

For the 'matched' configuration, the average absolute error is 2.01 dB (as plotted in Figure 4.13a). Using the ideal charge model improves this number slightly, but the visual match is about as good (not plotted).

For the 'shorted' configuration, the average absolute error is 2.19 dB (as plotted in Figure 4.13b). This number only slightly deteriorates when using the idealised charge model of a delayed short. When using a simple short, the curve visually deteriorates (not plotted), as can be seen from the increased average absolute error 4.36 dB.

In summary, the radiated immunity of a trace and an IC can be predicted to within 2.1 dB average absolute error by correctly concatenating the modified Taylor model and the ICIM-CI. On average, using a measured charge model is not necessary, at least up

Table 4.1: PCB immunity prediction – measurement error as function of terminal model quality.

		error			
config.	charge model	average	avg. abs.	maximum	minimum
matched	delayed meas.	−1.91 dB	2.01 dB	+2.30 dB	−6.80 dB
	(delayed) 50 Ω	−1.53 dB	1.87 dB	+2.79 dB	−6.70 dB
shorted	delayed meas.	+1.14 dB	2.19 dB	+7.68 dB	−14.29 dB
	delayed 0 Ω	+0.97 dB	2.22 dB	+4.71 dB	−17.73 dB
	0 Ω	+1.12 dB	4.36 dB	+14.40 dB	−13.75 dB

to 4.2 GHz.

4.5 Conclusions

Because of the small size of IC leadframe and bonding wires with respect to the wavelength, the direct coupling of radiated interference with IC is generally supposed to be negligible up to several GHz. On the other hand, Antenna in Package (AiP) solutions for 2.4 GHz suggest the contrary. In order to understand the coupling mechanism and, consequently, the relevance of IC immunity tests beyond 1 GHz, two experiments were conducted.

Firstly, a full-wave simulation was performed on a trace and a SOIC8 interconnect. The coupling of an incident plane wave to the die was found to be dependent on the trace length up to 10 GHz. This experiment suggests that the dominant coupling mechanism for a modern IC is conducted, well beyond 1 GHz.

Secondly, the field-to-trace model and the ICIM-CI obtained in Chapter 2 and 3 are concatenated, to predict the radiated immunity of the whole up to 4.2 GHz. Although this model does not take the direct radiated immunity of the IC into account, it corresponds with measurement to within 2.1 dB average absolute error. In another way, this experiment suggests that the perturbation predominantly perturbs the IC by conduction, well beyond 1 GHz.

Both experiments were conducted on modern packages, while electronics are continuously expected to shrink, hence reduce direct coupling. Therefore, the dominant-conduction conclusion may be expected to remain valid over time and for increasing frequencies. Consequently, IC immunity modelling beyond 1 GHz seems useful.

In this particular concatenation of systems at the hierarchical PCB level, the radiated perturbation seems to mainly couple to the trace and then be conducted to the IC. This subsystem generally is comprised in a much larger system, for example in a rack, in a

shielded enclosure, connected with cable bundles in a vehicle. It would be interesting to prove that the dominant-conduction hypothesis also holds true in that case. A topological approach like the Power Balance technique developed by Junqua et al. could be a good starting point [105].

CHAPTER 5

Conclusion and Perspectives

Abstract. From the observations described in this thesis, it can be concluded that it is useful and possible to model the conducted immunity of ICs beyond 1 GHz. Therefore, the extension of IEC 62132-4 to 10 GHz should be seriously considered. Moreover, the speed and transparency of the model for field-to-trace coupling open up new possibilities for computer-aided design. The semi-automatic generation of lean extraction PCBs could facilitate model extraction. There are also critical remaining questions, remaining to be answered.

5.1 Introduction

What have we seen throughout this thesis? How could all of this be put into practice today? What can not yet be concluded? Where should we, therefore, go tomorrow?

The first building block of this thesis is the transparent model for field-to-trace coupling; section 5.2 will review the results and draw up a research agenda for this model alone. The second building block is the lean Gigahertz Direct Power Injection (GDPI) method, comprising semi-automatic PCB layout generation, which will be reviewed and of which the future possibilities will be sketched in section 5.3. Finally, section 5.4 will conclude upon the thesis' main hypothesis.

5.2 Modified Taylor Model for Field-to-trace Coupling

Literature offered little understanding on how PCB traces determine the coupling of incident RF radiation to conducted voltages or currents. That is, models allowing for numerical simulation existed, notably the weakly coupled Taylor cell or its equivalents. When applying this model to electrically short, bifilar lines in vacuum, the effect of

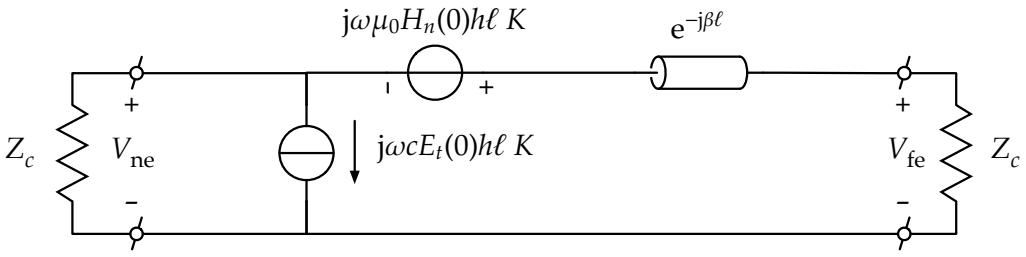


Figure 5.1: The modified Taylor cell; the correction factor K takes into account the long line effect. (Repetition of Figure 2.19.)

line dimensions and orientation can be understood [10]. However, when applying this models to PCB traces, the result becomes hard to understand because of the substrate. Only Leone gave a transparent worst case for a single microstrip segment with moderately mismatched loads, for low frequencies. Nonetheless, for high frequencies, the trace becomes electrically long, meshing is required and understanding is lost.

Yet, to acquire a numeric reference, a meshed model was implemented for the case of a grazing incident, vertically polarised plane wave on a single microstrip with arbitrary loads. The Taylor-telegrapher's cell was applied under Kron's formalism. By frequency-adaptive meshing of the trace, a 10× speedup was achieved. Of course, no profound understanding was obtained.

Therefore, the single Taylor cell was modified to remain valid for high frequencies. Thereby, meshing is no longer needed and understanding could be hoped for. The modification is a correction factor K, which quantifies the similitude between the illumination and the trace's eigenwave, which would spontaneously propagate on the line:

$$K = \frac{1}{\ell} \int_0^\ell i(p) \cdot w^*(p) \, \mathrm{d}p, \tag{5.1}$$

where i and w are the normalised amplitude phasors of the illumination and the eigenwave, ℓ is the trace length and p is the coordinate along the trace segment. Indeed, this is the length-averaged cross-correlation between illumination and eigenwave. The resulting modified Taylor cell is repeated in Figure 5.1. Note that for calculating the near-end or the far-end induced voltage, the backward- or the forward-going eigenwave needs to be used. By superposition and basic transmission line theory, the model was extended to hold for vertically polarised, grazing-incident plane wave illumination of uniform multi-segment traces with arbitrary loads. Because of the single cell, closed-form solution, another 10× speedup was achieved.

Predictions from this model were compared to full-wave simulation, yielding very good correlation. Because the full-wave solver does not rely on transmission line theory or our approximation of the substrate field, both approximations seem legitimate.

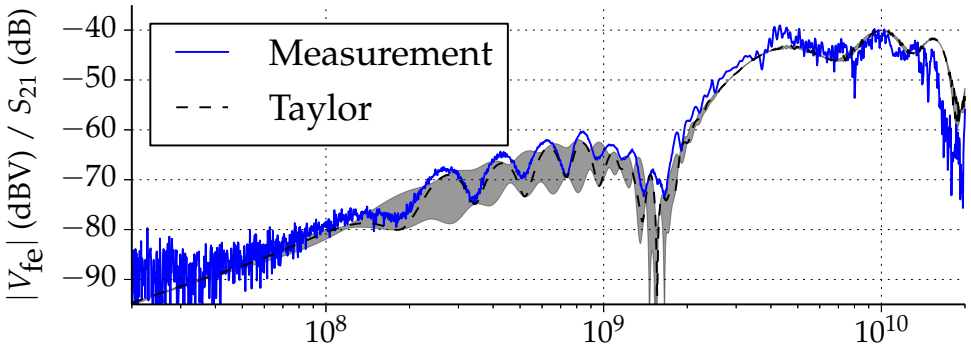


Figure 5.2: Prediction and measurement of coupling to a three-segment microstrip with characteristic loads. Without taking into account GTEM cell reflections, the prediction would be midway the grey zone. (Repetition of Figure 2.51a.)

The modified Taylor predictions were also compared to Gigahertz Transverse ElectroMagnetic (GTEM) cell measurements, taking into account substrate permittivity and GTEM cell reflections.

To take into account the frequency-dependent real substrate permittivity, a planar resonator was employed to measure the used substrate. In comparison to Rectangular Dielectric WaveGuide (RDWG) measurements on the same substrate, this method seemed to work. However, taking into account the measured permittivity did not yield significant improvement of the field-to-line coupling prediction up to 3 GHz, and worsened it above. Because of this low Return On Modelling Effort (ROME), the permittivity measurements were not used anymore and a simple $\varepsilon_r = 4.6$ was retained.

To take into account the non-ideality of the GTEM cell hybrid load, the S_{11} of the GTEM cell was measured and translated to the position of the illuminated trace. The forward wave and its first reflection by the hybrid load was then fed to the modified Taylor model. As can be seen in the striking example of Figure 5.2, this predicts the oscillations in the $0.1 - 2$ GHz range. Because of the good ROME, this correction was retained.

Based on this model formulation, the transparent upper bound shown in Figure 5.3 could be found. Several practical consequences could be drawn from this formulation. Not surprisingly, matching helps. Practically, this can be done by adding passive components at the trace terminals, or just by adjusting the trace width, which is 'free'. Furthermore, decreasing the substrate thickness h (not so easy) or the trace length ℓ (easier) helps for low frequencies. At high frequencies, shortening the trace does not help, although the crossover frequency between 'low' and 'high' frequencies increases. Finally, changing the substrate permittivity ε_r does not significantly decrease coupling at any frequency, because $\varepsilon_{r,\text{eff}}$ will change accordingly.

For a single microstrip segment with matched loads, this worst case occurs for end-fire excitation at the near-end side for low frequencies and at the far-end side for high

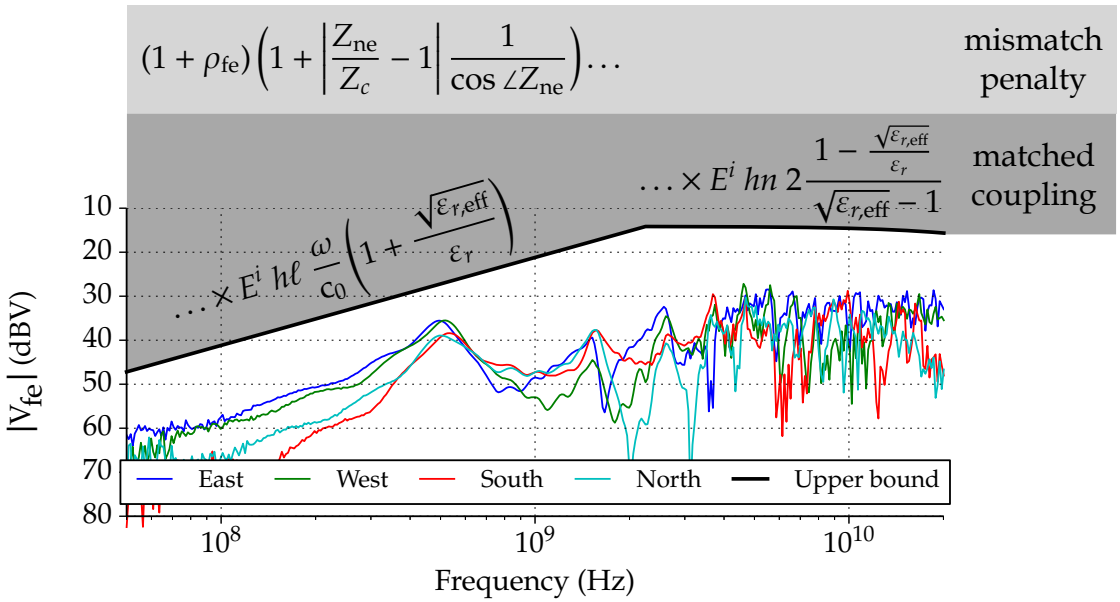


Figure 5.3: Upper bound versus measurement of an either-end mismatched ($0-270\,\Omega$), three-segment trace, after Figure 2.54c.

frequencies. Consequently, it is most interesting to illuminate a sensitive trace from either end in pre-compliance testing.

The upper bound was not proven for arbitrarily-polarised, arbitrarily-incident plane waves. As any electromagnetic fields can perturb a PCB in real life, the analysis should be extended to all polarisations and all angles of incidence. Considering the worst case and taking loose upper bounds may help to keep the expressions transparent.

A deterministic approach was taken in this thesis to allow for understanding, debugging and selection of test scenarios. However, as perturbing fields are random in real life, it might be useful to take a stochastic approach [22]. The challenge will remain to keep the solution transparent.

The +1.3-dB systematic bias of the GTEM measurements with respect to the Taylor model predictions remains enigmatic. Full-wave simulation of the GTEM cell for the top opening might yield new insights.

Throughout the modelling process, errors were mainly quantified by the average absolute error in dB. However, the match was often better appreciated visually. Therefore, techniques like Feature Selective Validation (FSV) should rather be applied [106].

Finally, the presented upper bound is rather loose. For one case study, the upper bound was as much as 13 dB too high in the high-frequency range. This might be due to the pessimistic assumptions behind the upper bound: there are no trace losses and all segments will interfere constructively for some frequency. Moreover, rather

rough approximations were used in the consideration of arbitrary terminal impedances. Therefore, a sensitive trace from industrial reality should be studied to see how loose the upper bound is in practice. If it turns out to be too pessimistic and that it would cause costly over-engineering, the assumptions and approximations should be revisited.

5.3 Lean GDPI Method

Now that the conducted perturbation induced by an incident electromagnetic field beyond 1 GHz is known, the conducted immunity of ICs is also interesting beyond 1 GHz. The IEC 62433-4 Integrated Circuit Immunity Model for Conducted Immunity (ICIM-CI) is a mature model to describe IC's immunity, which consists of a Passive Distribution Network (PDN) and an Immunity Behaviour (IB) part. From the PCB designer's perspective, it is generally impossible to obtain such models from IC manufacturers, so a method is needed to extract these models from measurement.

The IEC 62132-4 DPI already allows for extracting the IB and is standardised up to 1 GHz. The transmitted power threshold is deduced from a directional coupler power reading. The reference plane of this measurement is at the output of the directional coupler, instead of at the Pin Under Test (PUT). Moreover, the directional coupler power measurement has a high uncertainty. To solve both problems, Lafon proposed the following method. First, the PDN is measured at the PUT reference plane by calibrating the VNA with a calibration kit that mimics the DPI feed. Then, the entire DPI set-up is carefully modelled, including peripheral circuitry present during DPI. That way, the transfer from forward power at the generator to transmitted power to the PUT can be simulated. The DPI is then performed and corrected using this transfer.

A practical problem of this method is the required modelling of the peripheral circuitry on the DPI extraction PCB. With increasing frequency, this becomes increasingly difficult.

Therefore, this thesis proposed to move the peripheral circuitry away from the PCB, to obtain a *lean* extraction PCB. A lean extraction PCB only consists of feeds (i.e. connectors and traces) leading to PUTs. The extraction PCB thereby becomes easier to design and to characterise beyond 1 GHz. Necessary peripherals can be placed on connectorised peripheral modules. That way, they can be characterised by VNA measurements.

The feeds can also be characterised by VNA measurement, in two steps. That is, the VNA is calibrated to the connector reference plane. Standards on feed calibration kit are then measured and transferred to a PC. There, a second calibration is performed to obtain the correction factors that describe the feed.

These black-box models of the measurement set-up can then be used to move the reference plane of both VNA and DPI measurements to the PUT.

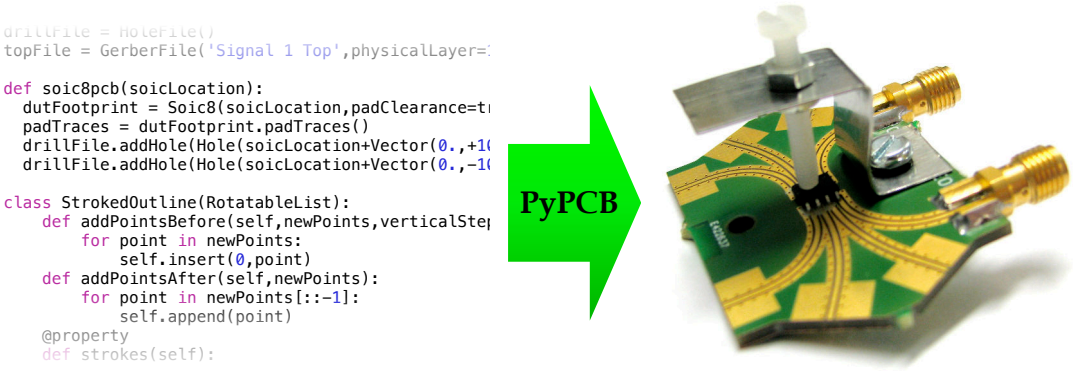


Figure 5.4: The lean extraction PCB is code-generated with PyPCB, after Figure 3.28.

To demonstrate this method, a generic SOIC8 lean extraction PCB was developed. In view of the industrialisation of the method, the PCB design was partly automated. That is, the PyPCB module was developed to generate the PCB layout in code.

The feed loss of the resulting fixture was measured to be 0.1 dB/GHz and the worst-case crosstalk was estimated at −14 dB. The fixture was then used to extract the ICIM-CI of an LM7805 voltage regulator up to 4.2 GHz.

Based on this proposition, the IEC 62132-4 DPI could be improved by requiring a documented measurement uncertainty. This in turn, would logically allow Lafon's transmitted power deduction method. The placement of peripheral circuitry is actually overconstrained and ambiguous, which should be solved. The lean extraction proposed in this thesis could be informatively added as one possible method. Also, a requirement to the crosstalk between feeds might be added.

The tooling for model extraction could also be improved. For example, by creating measurement software that records observations together with the measurement uncertainty. This software should then propagate the uncertainty through all calculations leading to an ICIM-CI, for example with the Python `uncertainties` package.

Many questions remain, however. For example, how does this method extrapolate to ICs that require more and closer-by peripherals? Could the method also be applied to ICs with more compact packages? Can PyPCB be used in an industrial context to generate extraction PCBs for complex ICs?

More fundamentally, the physical meaning of the DPI results beyond should be investigated. For example, when multi-modal waveguides like the Grounded CoPlanar Wave-guide (GCPW) are used, what does a transmitted power threshold mean? Is the power distribution over modes important? If so, IEC 62433-4 should also define the reference planes of its waveguide ports.

A good check to gauge the objectivity of the standard would be to let two parties

independently extract models from the same Device Under Test (DUT) and compare the resulting ICIM-CI.

5.4 ICIM-CI Beyond 1 GHz Considered Possible and Useful

There is general consensus that below 1 GHz, real-life radiated perturbations mainly couple to cabling and PCB traces. It also seems intuitive that for rising frequencies, the wavelength approaches the size of the IC and direct coupling becomes important. At some frequency, the radiated immunity of the IC is even expected to become dominant.

However, there is little experimental data to determine the conducted-radiated transition frequency. No theoretical deduction of this transition frequency from trace and package geometry was found either.

Therefore, the modified Taylor model for field-to-trace coupling and an ICIM-CI model were concatenated to predict the radiated immunity of a 5 cm PCB trace and an SOIC8-packaged voltage regulator IC. This experiment connects the building blocks of this thesis, as illustrated in Figure 5.5.

Although the radiated immunity of the IC itself was thus neglected, good correlation between measurement and prediction was observed up to 4.2 GHz. Therefore, this observation did not falsify the dominant-conduction hypothesis. Moreover, because packages shrink and have decreasing parasitic inductance, the dominant-conduction hypothesis can be expected to hold true in the future. For the present, modeling the conducted immunity of ICs beyond 1 GHz will therefore be considered *useful*.

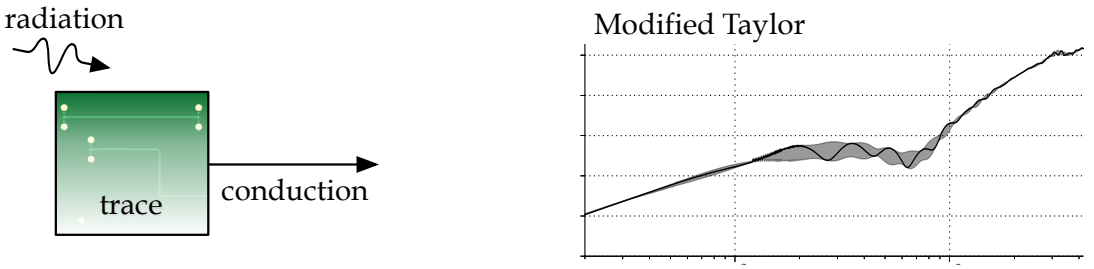
As this thesis also showed that it is *possible* to model the conducted immunity of ICs beyond 1 GHz, the main hypothesis

it is useful and possible to model the conducted immunity of ICs beyond 1 GHz

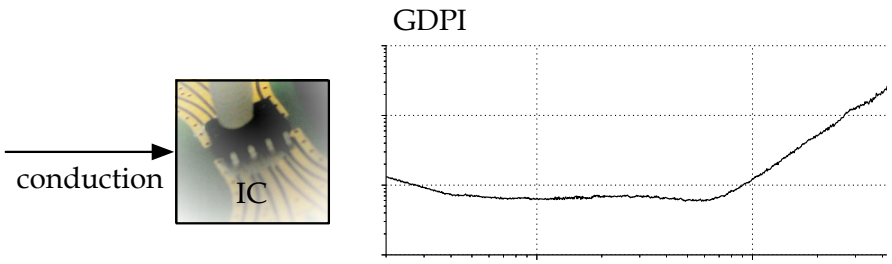
was not falsified.

Supposing that conduction indeed remains the dominant interference mechanism for integrated circuits above 1 GHz, GDPI measurements are useful. IEC 62132-4, ¶ 4.1 currently reads: "For a frequency range below 1 GHz, this leadframe, as well as the structures on-chip, are not regarded as efficient antennas for the reception of unwanted RF energy." Based on this thesis' observations, 'below 1 GHz' may safely be changed to 'up to several GHz', at least in some cases. Moreover, the standard should be amended as described in section 3.7 to prescribe and propose measurement set-ups that are valid beyond 1 GHz.

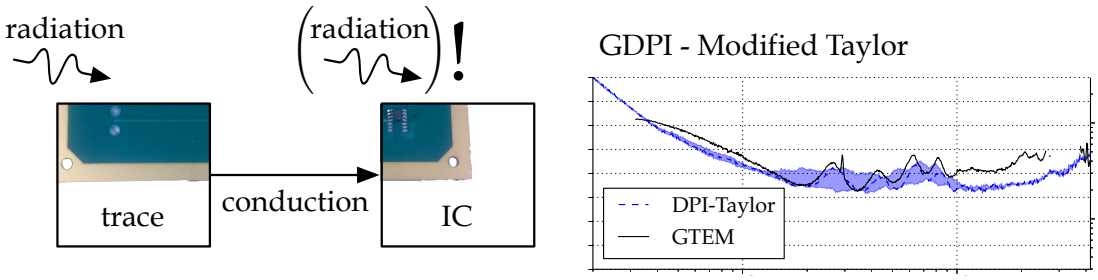
In this thesis, it turned out practical to express the immunity threshold of an IC in terms of voltage, instead of transmitted power. This might be an argument to favor the voltage formulation, permitted in the last IEC 62433-4 Conducted Immunity Markup Language (CIML) proposal.



(a) Chapter 2 modeled and measured field-to-trace coupling.



(b) Chapter 3 modeled IC conducted immunity from measurement.



(c) Chapter 4 modeled PCB radiated immunity by subtracting (a) from (b), and checked with GTEM measurements.

Figure 5.5: Structured results of this thesis, after Figure 1.7.

Finally, the speed of the closed-form immunity prediction of trace and IC should be made accessible to PCB designers. That way, they can estimate PCB immunity quickly and early in the design process.

For example, a designer could click on a PCB trace or net and be almost immediately provided with immunity curves. An entire PCB could also be analysed and based on ICIM-CI models of the ICs, sensitive traces could be marked in red. A wizard could then be provided to optimise the trace width to match the terminal impedances at the most problematic frequency.

If the modified Taylor model turns out to be reciprocal, it can be used to quickly predict emissions. For example, PCB design tools could quickly estimate the far-field emissions of a PCB by chaining Integrated Circuit Emission Model for Conducted Emission (ICEM-CE) and a trace-to-field coupling model together.

The main conclusion might be challenged by studying a borderline geometry: for example a 2-cm trace, leading to a large package that contains 2-cm leads. Will the majority of the radiated energy still couple to the trace? And how does the answer on that question depend on the frequency?

Another critical question that should be asked is: are there real IC susceptibility issues beyond 1 GHz? For instance, we needed the ridiculous functional criterion of 100 μVDC to be able to observe 'susceptibility' of the LM7805 voltage regulator. In Sketoe's 1999 DPI campaign, no susceptibility could be observed anymore beyond 2 GHz, contrary to 1978 ICs. Maybe present-day ICs have become robust enough and no immunity modelling (radiated nor conducted) is needed anymore.

Again, the verdict should come from real-life examples. An industrial EMC problem caused by Continuous Wave (CW) perturbation beyond 1 GHz should be analysed to see whether it can be understood as rooted in an IC. If so, this thesis' modelling method should be applied to try and falsify the main hypothesis.

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APPENDIX A

Scientific Production

This PhD-thesis is related to earlier and future publications, as follows:

1 The measurement and simulation on the seven-segment trace on p. 81ff. were taken from Sjoerd T. Op 't Land, Tvrtko Mandić, Mohamed Ramdani, Adrijan Barić, Richard Perdriau, and Bart Nauwelaers. "Comparison of field-to-line coupling models: Coupled transmission lines model versus single-cell corrected Taylor model." In: *Electromagnetic Compatibility (EMC EUROPE), 2013 International Symposium on*. Sept. 2013, pp. 276–281. The Method of Lines (MoL) approach presented in the article was not incorporated in this thesis, as it is original work of Tvrtko Mandić.

2 The measurement of PCB substrate permittivity presented on p. 63ff. is a slight adaptation of Sjoerd T. Op 't Land, Olga V. Tereshchenko, Mohamed Ramdani, Frank B.J. Leferink, and Richard Perdriau. "Printed Circuit Board Permittivity Measurement Using Waveguide and Resonator Rings." In: *Proceedings of EMC'14 Tokyo*. The article contains a justification for metrological requirements on permittivity measurements, which is not included in this thesis.

3 The analytical derivation of the modified Taylor model presented in section 2.4 appeared earlier in Sjoerd T. Op 't Land, Mohamed Ramdani, Richard Perdriau, Marco Leone, and M'hamed Drissi. "Simple, Taylor-based worst-case model for field-to-line coupling." In: *JPIER* 140 (June 2013), pp. 297–311. DOI: 10.2528/PIER13041207.

4 The intuitive explanation of the modified Taylor model first appeared in Sjoerd T. Op 't Land, Richard Perdriau, Mohamed Ramdani, Olivier Maurice, and M'hamed Drissi. "Kron Simulation of Field-to-line Coupling using a Meshed and a Modified Taylor Cell." In: *Electromagnetic Compatibility of Integrated Circuits (EMC Compo 2013), Proceedings of the 9th International Workshop on*. Nara, Japan, Dec. 2013.

5 The measurement on a one-side non-characteristic load presented on p. 78ff. will appear shortly in Sjoerd T. Op 't Land, Mohamed Ramdani, Richard Perdriau,

Yannis Braux, and M'hamed Drissi. "Using a Modified Taylor Cell to Validate Simulation and Measurement of Field-to-Shorted-Trace Coupling." In: *IEEE Transactions on Electromagnetic Compatibility* 56.4 (870 2014), p. 864. ISSN: 0018-9375. DOI: 10.1109/TEMC.2014.2313231.

6 The extension of the modified Taylor model to arbitrary either-end loads presented on p. 46ff. and the GTEM cell modelling on p. 73ff. should appear in Sjoerd T. Op 't Land, Mohamed Ramdani, Richard Perdriau, Jean Sudolski, M'hamed Drissi, and Frank B.J. Leferink. "Field-to-Long-Segmented-Trace Coupling with Arbitrary Loads and a Transparent Upper Bound Using a Single Modified Taylor Cell." In: *IEEE Transactions on Electromagnetic Compatibility* (). In preparation.

7 The design of an extraction PCB for SMD passives presented in section 3.3 appeared earlier in Sjoerd T. Op 't Land, Richard Perdriau, and Mohamed Ramdani. "Low-cost 0603 SMD Impedance Measurement Fixture." In: *Mediterranean Telecommunication Journal* 3.1 (Feb. 2013). Presented earlier on Congrès Mediterranéen des Télécommunications et Exposition, 22 to 24 March 2012, Fez, Marocco, pp. 40–43.

8 The design of a lean extraction method and PCB presented in Chapter 3 appeared earlier in Sjoerd T. Op 't Land, Richard Perdriau, and Mohamed Ramdani. "Design of a 20 GHz DPI method for SOIC8." In: *Electromagnetic Compatibility (EMC EUROPE), 2012 International Symposium on*. Sept. 2012, pp. 1–6. DOI: 10.1109/EMCEurope.2012.6396691.

9 The merger of the modified Taylor field-to-line coupling and a conducted immunity IC model presented in Chapter 4 should appear in Sjoerd T. Op 't Land, Mohamed Ramdani, Richard Perdriau, and M'hamed Drissi. "Modeling the far-field radiated immunity of integrated circuits using conducted immunity and field-to-line coupling." In: *IEEE Transactions on Electromagnetic Compatibility* (). In preparation.

10 A proof of concept for the measurement of non-linear behaviour of ICs was not incorporated in this thesis, but published as Sjoerd T. Op 't Land, Richard Perdriau, Mohamed Ramdani, and Frédéric Lafon. "Towards nonlinearity measurement and simulation using common EMC equipment." In: *Electromagnetic Compatibility of Integrated Circuits (EMC Compo), 2011 8th Workshop on*. Nov. 2011, pp. 125–130.

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Abbreviations

AC Alternating Current, often used informally to indicate variations on the DC operating point, or any frequency > 0 Hz.

ADC Analog to Digital Converter

ADS Agilent's Advanced Design System

AiP Antenna in Package

AoC Antenna on Chip

BCI Bulk Current Injection

BGA Ball Grid Array

BLT Baum-Liu-Tesche

BSMI Bureau of Standards, Metrology & Inspection, Taiwan

CAD Computer Aided Design

CE *Communauté Européenne*, European Community

CIML Conducted Immunity Markup Language

CISPR *Comité International Spécial des Perturbations Radioélectriques*, International Special Committee for Radio Electric Disturbances

CMOS Complementary Metal Oxide Semiconductor, the ubiquitous IC technology.

CNRS National Centre for Scientific Research, *Centre National de la Recherche Scientifique*

COTS Commercial Off-The-Shelf

CPW CoPlanar Waveguide

CPU Central Processing Unit

CST Computer Simulation Technology AG, develops and markets high performance software for the simulation of electromagnetic fields in all frequency bands.

CW Continuous Wave

DC Direct Current, often used informally to indicate 0 Hz.

DDPI Differential DPI

DIP Dual Inline Package

DPI Direct Power Injection, an immunity test method defined in IEC 62132-4. [75]

DUT Device Under Test

EFT Electrical Fast Transient

EMC ElectroMagnetic Compatibility

EMI ElectroMagnetic Interference

ESD ElectroStatic Discharge

ESR Equivalent Series Resistance

ESEO Ecole Superieure d'Electronique de l'Ouest

FCC Federal Communications Commission

FIT Finite Integration Technique

FR4 Flame Retardant 4, a class of common, low-cost PCB substrates.

FSV Feature Selective Validation

FTR First-Time-Right, *bon du premier coup*

GCPW Grounded CoPlanar Wave-guide

GDPI Gigahertz Direct Power Injection

GPS Global Positioning System

GPU Graphics Processing Unit

GRACE *Groupe de Recherche en Architecture des Composants Electroniques*, Research Group on Electronic Component Architecture

GTEM Gigahertz Transverse ElectroMagnetic, a broadband test mode of IEC 62132-2. [40]

GUI Graphical User Interface

HDR *Habilitation à Diriger des Recherches*

IB Immunity Behaviour

ICEM-CE Integrated Circuit Emission Model for Conducted Emission

ICIM-CI Integrated Circuit Immunity Model for Conducted Immunity

IC Integrated Circuit

IEMI Intentional ElectroMagnetic Interference, interference intended to hinder an enemy.

IETR *Institut d'Électronique et de Télécommunications de Rennes*, Rennes Institute for Electronics and Telecommunications

INSA *Institut National de Sciences Appliquées*, National Institute of Applied Sciences

IPA IsoPropyl Alcohol

IP Intellectual Property

JEDEC Joint Electron Devices Engineering Council, the former name of the JEDEC Solid State Technology Association

LDO Low DropOut voltage regulator

LED Light Emitting Diode

LIHA Local Injection Horn Antenna

LIN Local Interconnect Network, a digital bus for automotive communication.

LISN Line Impedance Stabilisation Network, a device that, when placed in series with a power supply, guarantees a broadband, known, source impedance (often 50 Ω).

MoL Method of Lines

MS MicroStrip

NEMP Nuclear ElectroMagnetic Pulse

NFSI Near Field Scan of Immunity

NN Neural Network

NP New Proposal

PBA Perfect Boundary Approximation

PC Personal Computer

PCB Printed Circuit Board

PDN Passive Distribution Network

PEC Perfect Electrical Conductor

PML Perfectly Matched Layer

pul per unit length

PUT Pin Under Test

QFN Quad Flat package No leads

QTEM Quasi-TEM

RAM Random Access Memory

RDWG Rectangular Dielectric WaveGuide

RF Radio Frequency

ROME Return On Modelling Effort

s.c.J. *sub conditione Jacobi*, under James' condition.

SEISME *Simulation de l'Emission et de l'Immunité des Systèmes et des Modules Electroniques*, Simulation of Emissions and Immunity of Electronic Systems and Modules

SI *Système Internationale*, International System of units

SLOC Single Line Of Code

SMA SubMiniature version A, a screw-type coaxial connector for DC-18 GHz.

SMD Surface Mount Devices are mounted at the surface of a PCB, as opposed to through-hole components. SMD is the modern device form of choice, because of compactness and speed of assembly. Through-hole components may be used for mechanical strength or if heat considerations oblige so.

SMT Surface Mount Technology, see SMD

SoC System on a Chip

SOIC Small Outline IC, an SMD IC package with leads on two opposite sides.

SOL Short-Open-Load

SOLT Short-Open-Load-Thru

SPICE Simulation Program with Integrated Circuit Emphasis, a general-purpose open source analog electronic circuit simulator.

SVD Singular Value Decomposition

TDD Test Driven Development

TDR Time Domain Reflectometre

TEM Transversal ElectroMagnetic, a mode that has neither electric nor magnetic fieldlines tangential to the propagation direction.

TRL Thru-Reflect-Line

UMR Mixed Research Unit, *Unité Mixte de Recherche*

UPC *Universitat Polytècnica de Catalunya*, Polytechnical University of Catalonia

US United States

VNA Vector Network Analyser

VSWR Voltage Standing Wave Ratio

WHDI Wireless Home Digital Interface

XML eXtended Markup Language

X-DPI eXtended DPI

ZIF Zero Insertion Force

Definitions

Below, the definitions as used in this report are enumerated.

jitter Deviation of a time reference $\hat{t}$ with respect to the real time t.

phase shift Signal $a = \cos(\omega t + \alpha)$ is said to have a phase shift $\phi_{ab} = \alpha - \beta$ with respect to signal $b = \cos(\omega t + \beta)$.
(A positive phase shift is called lead, a negative phase shift lag.)

emulation System X is said to emulate another system Y when the behaviour of X mimics the behaviour of Y by means of a mechanism analogous to the mechanism of Y.

simulation System X is said to simulate another system Y when the behaviour of X mimics the behaviour of Y by means of a (mathematical) model of the behaviour of Y.

modelling Process of defining a model.

model Simplified view on physical reality.
(A model of a system can often be thought separated in a structure (e.g. circuit topology) on the one hand, and parameters (e.g. element values) on the other hand.)

transparent Revealing the injection from design parameters to performance.

opaque Opposite of transparent.

functional criterion Requirement on behaviour.
(Examples: "v_{out} deviates less than ±100 ns and ±1 V from v_{out} without disturbance")

element Part of a model.
(Example: a capacitance.)

electrical criterion Requirement on (a function of) one ore more electrical quantities.
(Examples: "the voltage at node '+' with respect to the ground is larger than 100 mV_{pp}", or "the power transmitted to port '–' is less than 1 mW".)

emission The caused electromagnetic field.

susceptibility The sensitivity of a function to an electromagnetic field.

immunity Inverse susceptibility.

conducted Completely guiding the electromagnetic energy.

radiated Not conducted.

device System with a (subjective) function.

must This word, or the terms *required* or *shall*, mean that the definition is an absolute requirement of the specification. [115]

must not This phrase, or the phrase *shall not*, mean that the definition is an absolute prohibition of the specification. [115]

should This word, or the adjective *recommmended*, mean that there may exist valid reasons in particular circumstances to ignore a particular item, but the full implications must be understood and carefully weighed before choosing a different course. [115]

should not This phrase, or the phrase *not recommended* mean that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behavior described with this label. [115]

may This word, or the adjective *optional*, mean that an item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because the vendor feels that it enhances the product while another vendor may omit the same item. An implementation which does not include a particular option *must* be prepared to interoperate with another implementation which does include the option, though perhaps with reduced functionality. In the same vein an implementation which does include a particular option *must* be prepared to interoperate with another implementation which does not include the option (except, of course, for the feature the option provides.) [115]

competent model Model, exactly extensive enough to answer a certain question.

black-box model Model that only describes behaviour.

grey-box model Model that offers one layer of explanation, before employing black-box models.

white-box model Model that offers two or more layers of explanation, before employing black-box models.

component Part of a system.
(For example: a capacitor.)

system Physical whole.

reproducibility The inverse amount of systematic errors. [46]
That is, when we are measuring the exact same quantity, we should observe the same value. All variation is thus caused by the measurement method and we call them systematic

repeatability The inverse amount of manufacturing variability. [46]
For example, when we are measuring the same attribute of different instances of the same type (e.g. substrates or ICs), we would like to observe the same value. All observed variation is the effect of finite repeatability and finite reproducibility.

INSA de RENNES
Service des Formations

AVIS DU JURY SUR LA REPRODUCTION DE LA THESE SOUTENUE

Titre de la thèse:
Modélisation de l'immunité des circuits intégrés mixtes dans la bande 1GHz-10GHz

Nom Prénom de l'auteur : OP'T LAND SIEUWERD TEUNIS

Membres du jury :
- Monsieur LEFERINK Frank
- Monsieur DRISSI M'HAMED
- Monsieur LEVANT Jean-Luc
- Monsieur SICARD Etienne
- Monsieur PERDRIAU Richard
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F. LEFERINK

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M'hamed DRISSI

Résumé

La compatibilité électromagnétique (CEM) est l'aptitude des produits électroniques à coexister au niveau électromagnétique. Dans la pratique, c'est une tâche très complexe que de concevoir des produits compatibles. L'arme permettant de concevoir des produits bon-du-premier-coup est la modélisation. Cette thèse étudie l'utilité et la faisabilité de la modélisation de l'immunité des circuits intégrés (CI) au-delà de 1 GHz.

Si les pistes des circuits imprimés déterminent l'immunité rayonnée de ces circuits, il serait pertinent de pouvoir prévoir l'efficacité de couplage et de comprendre comment elle découle du routage des pistes. Les solveurs *full-wave* sont lents et ne contribuent pas à la compréhension. En conséquence, un modèle existant (la cellule de Taylor) est modifié de manière à ce que son temps de calcul soit divisé par 100. De plus, ce modèle modifié est capable de fournir une explication de la limite supérieure pour le couplage d'une onde plane, rasante et polarisée verticalement vers une piste de plusieurs segments, électriquement longue et avec des terminaisons arbitraires. Les résultats jusqu'à 20 GHz corrèlent avec des simulations *full-wave* à une erreur absolue moyenne de 2,6 dB près et avec des mesures en cellule GTEM (Gigahertz Transversale Electromagnétique) à une erreur absolue moyenne de 4,0 dB près.

Si l'immunité conduite des CI est intéressante au-delà de 1 GHz, il faut une méthode de mesure, valable au-delà de 1 GHz. Actuellement, il n'y a pas de méthode normalisée, car la fréquence élevée fausse les observations faites avec la manipulation normalisée. Il est difficile de modéliser et de compenser le comportement de la manipulation normalisée. Par conséquent, une manipulation simplifiée et sa méthode d'extraction correspondante sont proposées, ainsi qu'une démonstration du principe de génération automatique de la carte d'essai utilisée dans la manipulation simplifiée. Pour illustrer la méthode simplifiée, l'immunité conduite d'un régulateur de tension LM7805 est mesurée jusqu'à 4,2 GHz.

À part la tendance générale des fréquences qui montent, il y a peu de preuve concrète qui étaye la pertinence de la modélisation de l'immunité conduite des CI au-delà de 1 GHz. Une simulation full-wave suggère que jusqu'à 10 GHz, la plus grande partie de l'énergie rentre dans la puce à travers la piste. Par concaténation des modèles développés ci-dessus, l'immunité rayonnée d'une piste micro-ruban et d'un régulateur de tension LM7805 est prédite. Bien que ce modèle néglige l'immunité rayonnée du CI lui-même, la prédiction corrèle avec des mesures en cellule GTEM à une erreur absolue de 2,1 dB en moyenne.

Ces expériences suggèrent que la plus grande partie du rayonnement entre dans un circuit imprimé à travers ses pistes, bien au-delà de 1 GHz. Dans ce cas, la modélisation de l'immunité conduite au-delà de 1 GHz serait utile. Par conséquent, l'extension jusqu'à 10 GHz de la méthode de mesure CEI 62132-4 devrait être considérée. De plus, la vitesse et la transparence du modèle de Taylor modifié pour le couplage champ-à-ligne permettent des innovations dans la conception assistée par l'ordinateur. La génération semi-automatique des cartes d'essais dites maigres pourrait faciliter l'extraction des modèles. Certaines questions critiques et importantes demeurent ouvertes.

Mots clefs : EMC, IC, immunité, couplage champ-à-piste, cellule de Taylor, DPI, ICIM-CI, mesure, modélisation, simulation, GHz

Abstract

Electromagnetic Compatibility (EMC) is the faculty of working devices to co-exist electromagnetically. In practice, it turns out to be very complex to create electromagnetically compatible devices. The weapon to succeed the complex challenge of creating First-Time-Right (FTR) compatible devices is modelling. This thesis investigates whether it makes sense to model the conducted immunity of Integrated Circuits (ICs) beyond 1 GHz and how to do that.

If the Printed Circuit Board (PCB) traces determine a PCB's radiated immunity, it is interesting to predict their coupling efficiency and to understand how that depends on the trace routing. Because full-wave solvers are slow and do not yield understanding, the existing Taylor cell model is modified to yield another 100 times speedup and an insightful upper bound, for vertically polarised, grazing-incident plane wave illumination of electrically long, multi-segment traces with arbitrary terminal loads. The results up to 20 GHz match with full-wave simulations to within 2.6 dB average absolute error and with Gigahertz Transverse Electromagnetic-cell (GTEM-cell) measurements to within 4.0 dB average absolute error.

If the conducted immunity of ICs is interesting above 1 GHz, a measurement method is needed that is valid beyond 1 GHz. There is no standardised method yet, because with rising frequency, the common measurement set-up increasingly obscures the IC's immunity. An attempt to model and remove the set-up's impact on the measurement result proved difficult. Therefore, a simplified set-up and extraction method is proposed and a proof-of-concept of the automatic generation of the set-up's PCB is given. The conducted immunity of an LM7805 voltage regulator is measured up to 4.2 GHz to demonstrate the method.

Except for a general trend of rising frequencies, there is only little concrete proof for the relevance of IC immunity modelling beyond 1 GHz. A full-wave simulation suggests that up to 10 GHz, most energy enters the die via the trace. Similarly, the radiated immunity of a microstrip trace and an LM7805 voltage regulator is predicted by concatenating the models developed above. Although this model neglects the radiated immunity of the IC itself, the prediction corresponds with GTEM-cell measurement to within 2.1 dB average absolute error.

These experiments suggest the most radiation enters a PCB via its traces, well beyond 1 GHz, hence it is useful to model the conducted immunity of IC beyond 1 GHz. Therefore, the extension of IEC 62132-4 to 10 GHz should be seriously considered. Moreover, the speed and transparency of the modified Taylor model for field-to-trace coupling open up new possibilities for computer-aided design. The semi-automatic generation of lean extraction PCB could facilitate model extraction. There are also critical remaining questions, remaining to be answered.

Keywords: EMC, IC, immunity, field-to-trace coupling, Taylor cell, DPI, ICIM-CI, measurement, modeling, simulation, GHz

N° d'ordre : 14ISAR 19 / D14 - 19
Institut National des Sciences Appliquées de Rennes
20, Avenue des Buttes de Coëmes • CS 70839 • F-35708 Rennes Cedex
Tel : 02 23 23 82 00 - Fax : 02 23 23 83 96