Conception et réalisation d'amplificateur de puissance MMIC large-bande haut rendement en technologie GaN

Victor Dupuy

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université de BORDEAUX

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L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DE SCIENCES PHYSIQUES ET DE L'INGÉNIEUR

SPÉCIALITÉ ÉLECTRONIQUE

Par Victor, DUPUY

Conception et réalisation d'amplificateur de puissance MMIC large-bande haut rendement en technologie GaN

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Abstract

Titre : Conception et ralisation d'amplificateur de puissance MMIC large-bande haut rendement en technologie GaN

Résumé : Ces travaux de thése se concentrent sur la conception d'amplificateur de puissance MMIC large-bande haut rendement en technologie GaN pour des applications militaires de type radar et guerre électronique. Les objectifs principaux sont de proposer des structures innovantes de combinaison de puissance notamment pour réduire la taille des amplificateurs actuels tout en essayant d'améliorer leur rendement dans le même temps. Pour cela, une partie importante de ces travaux consiste au développement de combineurs de puissance ultra compactes et faibles pertes. Une fois ces combineurs réalisés et mesurés, ils sont intégrés dans des amplificateurs de puissance afin de prouver leur fonctionalité et les avantages qu'ils apportent.

Différents types d'amplificateur tant au niveau de l'architecture que des performances sont réalisés au cours de ces travaux.

Mots clés: GaN, MMIC, amplificateur de haute puissance, combinaison de puissance, haut-rendement

Title : Design and realizations of wideband and high efficiency GaN MMIC high power amplifiers

Abstract : This work focus on the design of wideband and high efficiency GaN MMIC high power amplifiers for military applications such as radar and electronic warfare. The main objectives consist in finding innovative power combining structures in order to decrease the overall size of amplifiers and increasing their efficiency at the same time. For these matters, an important part of this work consisted in the design and realization of

ultra compact and low loss power combiners. Once the combiners realized and measured, they are integrated into power amplifiers to prove their functionality and the advantages they bring.

Several kind of amplifiers have been realized whether regrind their architecture or their performances.

Keywords GaN, MMIC, high power amplifier, power combining, high efficiency

Contents

List of Figures v

List of Tables xi

1 Introduction 1

2 Bibliography and Context 3

2.1 Military applications . . . 3
2.2 GaN devices and technologies . . . 7
2.2.1 Silicon and wide bandgap devices . . . 7
2.3 The HEMT GaN : a transistor dedicated to power applications . . . 8
2.3.1 Transistor Basics . . . 8
2.3.2 The GaN HEMT . . . 10
2.3.2.1 History and principle . . . 10
2.3.2.2 Physical structure . . . 11
2.3.2.3 Electrical characteristics . . . 12
2.3.2.4 Figures of merit . . . 16
2.4 Power Amplifier Design . . . 17
2.4.1 Definitions . . . 17
2.4.1.1 Power . . . 17
2.4.1.2 Gain . . . 19
2.4.1.3 Efficiency . . . 20
2.4.1.4 Linearity . . . 21
2.4.2 Power Amplifier Basics . . . 22
2.4.2.1 Power Amplifier Classes . . . 27
2.4.3 Amplifiers Topologies . . . 31

2.4.3.1 Single-ended topologies . . . 32
2.4.3.2 Balanced / Differential topologies . . . 33
2.4.4 Wideband amplifiers . . . 37
2.4.4.1 Reactively matched amplifiers . . . 38
2.4.4.2 Feedback amplifiers . . . 39
2.4.4.3 Traveling wave amplifiers . . . 40
2.5 State of art . . . 42
2.5.1 X-band . . . 42
2.5.2 Wideband : C-band to Ku-band amplifiers . . . 46
2.6 Thesis contribution . . . 51

3 Power Combining **53**
3.1 Theory on combiners for power amplifiers . . . 54
3.1.1 Current combiners . . . 55
3.1.2 Transformers . . . 58
3.1.3 Couplers . . . 64
3.2 Vertical coupling and elements stacking . . . 69
3.2.1 Mechanical aspects . . . 70
3.2.2 Electrical aspects . . . 74
3.3 Realizations . . . 79
3.3.1 Stacked Balun . . . 79
3.3.1.1 C to X-band balun . . . 79
3.3.1.2 X to Ku band balun . . . 94

4 Wideband High Power Amplifiers **99**
4.1 C to X-band high power amplifier . . . 99
4.1.1 Specifications . . . 99
4.1.2 Output power stage . . . 100
4.1.3 Input stage : active balun . . . 118
4.1.4 Overall HPA Architecture . . . 126
4.2 X to Ku-band traveling wave amplifier . . . 131
4.2.1 Specifications . . . 131
4.2.2 Design methodology . . . 132
4.2.3 25 Ohms / 25 Ohms single TWA . . . 133

4.2.4 50 Ohms / 50 Ohms differential TWA 140
4.3 Confidential power amplifier design 144

5 Conclusion and Perspectives 145

6 List of Publications 147

References 149

List of Figures

2.1 Example of a 300W hybrid S-band power amplifier module 4
2.2 Example of a X-band full MMIC HPA 5
2.3 Example of C-band to Ku-band three stages MMIC HPA 5
2.4 Example of a full module based on MMIC's 6
2.5 Heterojunction bipolar transistor 9
2.6 Field effect transistor 10
2.7 AlGaN/GaN HEMT cut view 11
2.8 HEMT small signal electrical model 13
2.9 Output static characteristic of an HEMT transistor 15
2.10 Power coming in and out an Amplifier 18
2.11 1dB input and output compression point 22
2.12 Scattering Parameters principle 23
2.13 Example of S-parameters plots (linear and Smith chart) 25
2.14 Stable amplifier vs. unstable amplifier 26
2.15 Sinusoidal amplifier classes 28
2.16 Amplifier classes vs. bias point 29
2.17 Non Sinusoidal amplifier classes 31
2.18 Common-source power amplifier 32
2.19 Cascode power amplifier 34
2.20 Current combined power amplifier 35
2.21 Balanced (pseudo-differential) power amplifier 36
2.22 Differential power amplifier 37
2.23 Reactively matched amplifier 39
2.24 Feedback amplifier 40

2.25 Traveling wave amplifier 41
2.26 Compact two stages current combined GaN HPA 43
2.27 Compact two stages current combined GaN HPA 44
2.28 A 14W GaN HPA realized withUMS GH25 process 45
2.29 C-Ku band 20W reactively matched GaN amplifier 47
2.30 14W 2-18 GHz GaN Non-uniform Distributed Power Amplifier 48
2.31 Decade bandwidth 2 to 20GHz GaN differential distributed power amplifier 49

3.1 A 2-way Wilkinson combiner 56
3.2 A 2-way lumped Wilkinson combiner 56
3.3 A 19GHz, 3 stages 16 way Wilkinson combiner from the German Space Agency 57
3.4 HPA output stage using a transformed Wilkinson combiner 58
3.5 Transformer representation 58
3.6 Transformer in 2-ports configuration 60
3.7 Stacked transformer (left) and planar transformer (right) 63
3.8 Power amplifiers combined with baluns 64
3.9 Typical coupler representation and ports name 65
3.10 Example of an HPA using couplers for power splitting/combining . . . 68
3.11 Representation of a Lange coupler and port denomination 69
3.12 Lange coupler on alumina substrate 69
3.13 Simplified MMIC layers stack 71
3.14 Two lines crossing thanks to an air-bridge 71
3.15 Airbridge used as a stacked layer 72
3.16 Openings in pillars for oxide removal 73
3.17 Example of a possible shape realizable, top view 74
3.18 Illustration of vertical (left) and planar (right) coupling 75
3.19 Simulated testbench to compare planar and vertical coupling 76
3.20 Comparaison of energy transfer between planar and vertical coupling . . 77
3.21 Comparaison of coupling factor between planar and vertical coupling . . 78
3.22 Comparaison of mutual inductance between planar and vertical coupling 79
3.23 Detailed representation of a balun 80
3.24 Optimal impedances for a balun with a transformation ratio of one . . 81

3.25 Elementary HPA combined with baluns . . . 82
3.26 Elementary balun shapes : rectangular (left) and circular (right) . . . 83
3.27 Rectangle balun and principal dimensions . . . 83
3.28 Balun configuration for geometry tuning . . . 84
3.29 Balun response vs. geometry . . . 85
3.30 Conventional and Marchand balun arhcitecture . . . 86
3.31 Transmission parameters for a conventional and a Marchand balun . . . 87
3.32 Using winding midpoint as DC feed . . . 87
3.33 Transmission parameters for a balun with DC block capacitor and without 88
3.34 Transmission parameters for the rectangle balun . . . 89
3.35 Phase difference for the rectangle balun . . . 90
3.36 Shaping a balun to reduce its size . . . 91
3.37 Realized C to X band balun . . . 92
3.38 Ports configuration for EM simulation and measurement . . . 92
3.39 Transmission comparison for EM simulation and measurement . . . 93
3.40 Phase difference comparison for EM simulation and measurement . . . 94
3.41 Impedances comparison for EM simulation and measurement (2Ghz to 12GHz) . . . 95
3.42 Capacitor added in parallel to the differential winding to reduce size and increase bandwidth . . . 96
3.43 X to Ku-band balun with inside capacitors . . . 97
3.44 X to Ku-band balun transmission parameters . . . 97
3.45 X to Ku-band balun phase difference between differential paths . . . 98

4.1 Proposed designed flow for HPA design . . . 101
4.2 Common source topology used to characterize transistors . . . 102
4.3 I_{ds} vs. V_{ds} for various V_{gs} for an 8*125μm device . . . 103
4.4 I_{ds} vs. V_{gs} for V_{ds} =25V for an 8*125μm device . . . 104
4.5 Load pull simulation results for an 8*125μm device at 8GHz . . . 105
4.6 Comparison between different gate widths for an 8 fingers transistor at 10GHz . . . 106
4.7 Non linear simulation results for an 8*125μm device at 10GHz . . . 107
4.8 8*125μm device characteristics vs. frequency . . . 108

4.9 8*125μm device selected optimal impedances in Smith chart 109
4.10 Selected architecture for the output stage 110
4.11 Simulated small signal gain of the output stage standalone chip 111
4.12 Simulated output power and PAE vs. frequency for P_in=29dBm for output stage standalone chip 111
4.13 Simulated output power, PAE and gain vs. frequency for P_{in}=29dBm for output stage with a matched input 112
4.14 Rollet factor from DC to 20GHz 113
4.15 Example of a Bilbao stability analysis 114
4.16 Bilbao stability analysis : DC to 10 GHz, pertubator at gate 114
4.17 Bilbao stability analysis : 10 to 20 GHz, pertubator at drain 115
4.18 Bilbao stability analysis : 5 to 10 GHz, pertubator at output 115
4.19 Picture of the output stage standalone chip 116
4.20 Die reported on an aluminum substrate 116
4.21 Small signal measurements for the output stage 117
4.22 Non linear measurements for the output stage at 4GHz, 5GHz and 6GHz: Gain (top left), output power (top right) and PAE (bottom left) 118
4.23 Non linear measurement and simulation results comparison 118
4.24 Differential pair used as an active balun 120
4.25 Input and outputs matching 121
4.26 Phase difference between the differential outputs 122
4.27 Output power vs. frequency for each output path at P_{in}=20dBm 123
4.28 Output voltage waveforms at 3.8GHz 123
4.29 Output power vs. input power at 3.8GHz 124
4.30 Active balun layout view 125
4.31 Architecture proposed for the overall HPA 126
4.32 Full HPA small signal gain 127
4.33 Full HPA output power vs. frequency for P_{in}=22dBm 128
4.34 Full HPA gain vs. frequency for P_{in}=22dBm 128
4.35 Full HPA PAE vs. frequency for P_{in}=22dBm 129
4.36 Full HPA performances 130
4.37 Differential TWA design methodology 132
4.38 Schematical representation of a TWA 134

4.39 Common source cell 135
4.40 Optimal number of cells vs. maximal frequency of operation 135
4.41 Low pass filters introduced by cells connection 136
4.42 Power gain vs. frequency for various number of cells 136
4.43 Number of cells optimization in function of gain, output power and bandwidth 137
4.44 Selected architecture for the single TWA 138
4.45 Small signal simulation for the single TWA 139
4.46 Large signal simulation results for the single TWA at P_{in}=30dBm . . . 139
4.47 Output power and PAE for various drain voltage 140
4.48 Differential TWA representation 140
4.49 Small signal simulation results the differential TWA 141
4.50 Large signal simulation results for the single TWA at P_{in}=33dBm . . . 142
4.51 TWA partial layout 143
4.52 GaN TWA state of art 144

LIST OF FIGURES

List of Tables

2.1 **Frequency bands and military applications** 4
2.2 **Material Properties** 8
2.3 **Amplifiers classes summary** 32
2.4 **Wideband amplifiers comparison** 38
2.5 **Wideband amplifiers comparison** 42
2.6 **X-band high power amplifiers state of art** 46
2.7 **Wideband high power amplifiers state of art** 49

3.1 **Coupling factor vs. insertion loss** 67
3.2 **Ports configuration for insertion loss simulation** 76
3.3 **Ports configuration for coupling factor extraction** 77
3.4 **Quarter wave length upon frequency in GaN material** 81
3.5 **Balun sizes for geometry optimizaton** 84
3.6 **Comparison between theoretical and simulated electrical length (rectangular balun)** 85
3.7 **X to Ku-band balun performances** 98

4.1 **C to X band HPA specifications** 100
4.2 **X to K_u band HPA specifications** 131
4.3 **Differential TWA performances** 142

1

Introduction

In every day life, we are surrounded by wireless communicating devices everywhere. In the past decades, we have witnessed a tremendous growth in the overall wireless communications market. Together with this growth, major improvements and research progresses have made it possible for wireless devices to achieve impressive performances. For example, thanks to the 4G/LTE standard a customer can surf the web walking on the street on his mobile phone as fast as he would at home on his computer with a DSL internet connection. Achievements of this kind are now made possible by the improvements made in terms of radio-frequencies transmitters? and emitters? architectures and integrated circuits technologies too.

Historically, it all starts in in 1864 when James Clerk Maxwell proposed a theory that predicates the behavior of electromagnetic waves and their interactions with the matter, even though Hans Christian Orsted was the first person making a link between electricity and magnetism back in 1820. Then from the second half of the 19th century till the 1930's various kind of wireless communications appear such as telegraph, hertzian links or transatlantic links. However, next major improvements happened during World War II where techniques and devices such as radio jamming, encrypted communications, walkie-talkies and of course radars took birth. Since then, military applications and needs kept increasing and thus offering means and goals to research in terms of wireless communications.

The aim of this thesis is to develop innovative High Power Amplifiers (HPA) for military wireless communication systems. The Power Amplifier (PA) is the key component of any wireless (and even wired) transmitter. Indeed the main performances such

as the range of action, the lifetime, the link speed and the quality of transmission are directly related to the PA performances. Basically, when designing an HPA dedicated to be implement in a transmitter of any kind , the following criteria are fundamentals :

- **Output power**: range of action
- **Bandwidth**: data rate
- **Efficiency**: life time and power management
- **Size**: ease of integration
- **Linearity**: quality of the link

The radars and electronic warfare applications targeted in this work do not demand strong requirements in terms of amplifiers linearity. Indeed while amplifier linearity is critical for most communication applications, they are strongly relaxed in these particular electronic warfare and radars applications. On the contrary highly non linear behavior is preferred most of time. On the contrary output power, bandwidth, efficiency and size are critical. Apparition of wide band gap devices about ten years ago has permitted to achieve output powers and efficiencies not even imaginable with any Silicon based technology. For example output power over 100Watts at 1GHz and over 20W at 10GHz have been reported with efficiencies around 50%.

In this work we focus on the design of wideband HPAs with high efficiency and small size.

In chapter 3, a presentation of the main military applications is made, then the basics and principles of power amplifier design are depicted. This chapter ends with a state of art of High power amplifiers.

Chapter 42 focuses on power combiners, it starts with theory on combiners before detailing the innovative power combiners realized and measured.

Finally, chapter 5 presents two different power amplifiers realized in this work, one working from C to X band and the other one from X to K_u band, they are both using the combiners introduced in the previous chapter.

2

Bibliography and Context

2.1 Military applications

Even though it is not considered as a mass market as mobile phones or civilian wireless communications for example, the amount of funds and manpower involved to develop new solutions for military communications have reached a very high level. Indeed, it is a strategic matter for many countries to be at the state of art in terms of military applications and systems. It is a well known fact that a lot of innovations and new technologies have come from the military side. Constraints in terms of performances, reliability and robustness dictated by the harsh environment the systems have to deal with, result most of the time in systems and circuits that define a new state of the art.

Most of the applications are located in the DC to 40GHz frequency range. Table 2.1 summarizes these applications as a function of the frequency bands. From HF band to L band, the circuits are discrete most of the time. Due to the wavelengths corresponding to these frequencies, it would not be neither realistic nor viable to implement systems in any kind of integrated circuits. In fact, size of chips would be so large that among other things the cost of fabrication would not be affordable. Circuits working in S-band can be either integrated or discrete. Power levels of more than 1000W are often targeted for S-band radars for example and these levels can not be achieved in a chip so lots of discrete components are still out there to meet this kind of specifications.

However, a solution into combining multiple MMICs on a printed board or module is more and more used, this is know as the hybrid approach. Fig 2.1 is an example of 300W

Name	Frequency (GHz)	Application
HF	0.003 - 0.03	OTH surveillance
VHF	0.03 - 0.3	Long-range surveillance
UHF	0.3 - 1	Long-range surveillance
L-band	1 - 2	Long-range surveillance
S-band	2 - 4	Moderate-range surveillance
C-band	4 - 8	Long-range tracking
X-band	8 - 12	Short-range tracking
Ku-band	12 -18	High-resolution mapping
K-band	18 - 27	Police/traffic radar
Ka-band	27 - 40	Police/high-resolution mapping

Table 2.1: Frequency bands and military applications

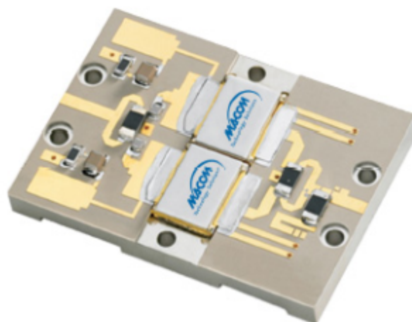

Figure 2.1: Example of a 300W hybrid S-band power amplifier module -

power amplifier module operating from 2.7GHz to 2.9GHz developed by MACOM. It illustrates the principle : two MMICs (white blocks on the picture) are combined through a printed board to increase output power. To make thermal management better a metal base is attached to the bottom of the board, then the power dissipation area is larger than it would be in a single chip so heat is evacuated faster. This results in the module operating at lower ambient temperature which leads into improved performances and increased lifetime.

For C-band and beyond, full-MMICs solutions are very often the solution of choice for two main reasons. Firstly, required output powers are not as high as for S-band applications, they are in the 5W to 50W and this kind of power levels can be achieved in a single MMIC chip. Secondly, printed boards have significant loss at 4GHz and

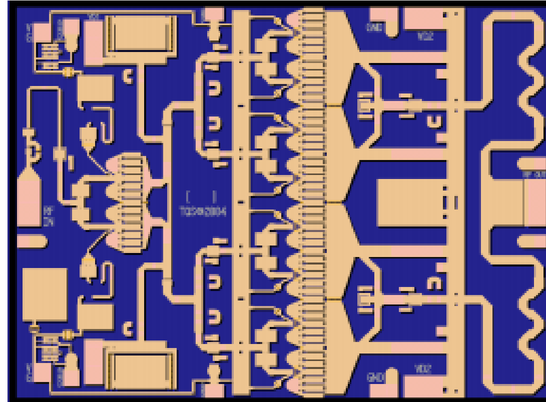

Figure 2.2: Example of a X-band full MMIC HPA -

over, so in terms of performances and efficiency it is best for the RF signal to stay inside the chip as much as possible, that is why fully integrated circuits are preferred for C-band and over. Fig 2.2 is an example of an X-band HPA GaAs full MMIC from Triquint, it delivers 38dBm from 9GHz to 10GHz and occupies an area of 9.2mm^2. It is a two stages high power amplifier using current combiners as splitter and combiner.

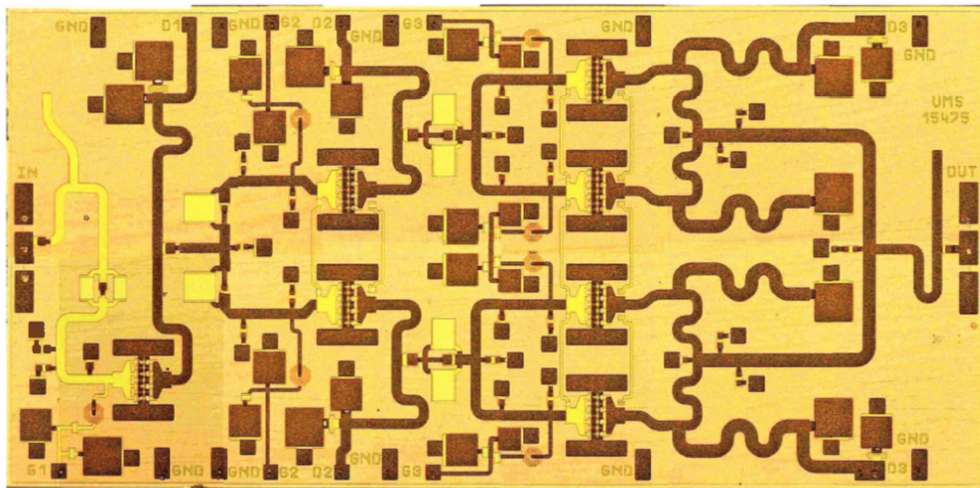

Figure 2.3: Example of C-band to Ku-band three stages MMIC HPA -

Another example of a full MMIC is presented in Fig 2.3. It is a GaN HPA operating from 6GHz to 18GHz delivering more than 6 W of output power with an efficiency going from 13% to 25% upon frequency. The die size is of 19.8mm^2 for this three stages amplifier. It has been implemented in the soon to be released UMS GH25 GaN process.

For most applications, MMICs are not meant to be used as standalone components but are dedicated to be integrated into systems to achieve complex functions. The idea is to integrate several MMICs together with low cost silicon ICs and even dies from other technologies sometimes to realize very specific functions. An example of a T/R module from THALES SA dedicated to X-band radar applications is shown in Fig 2.4. The core chip composed of variable gain amplifiers, delay blocks and phase shifters is fully integrated in a Silicon chip, so is the logic control for the overall module. The HPA for the TX path and the LNA for the RX path are both GaN MMICs while the antenna switch can either be a MEMS switch, a circulator or probably a GaN switch in the next future. All of these components are implemented in a single board and encapsulated to make a full T/R module dedicated to X-band radar applications.

Due to the power levels required, the bandwidth requirements and the robustness needed to comply with military applications, it is obvious that a low cost silicon technology like CMOS bulk for example is not going to be a good candidate. SiGe (Silicon Germanium based technologies) have shown drastic progress in terms of delivered power over the past few years but they have not quite reach high enough numbers in terms of power and efficiency yet. Moreover SiGe technologies suffer from their difficulties to evacuate heat. Wide bandgap based technologies have been the material of choice for many years in the military domain. Indeed, most of the chips dedicated to military applications are made in GaAs such as radar core chip and T/R module. However, recently a great interest has be shown for GaN devices who have the same advantages

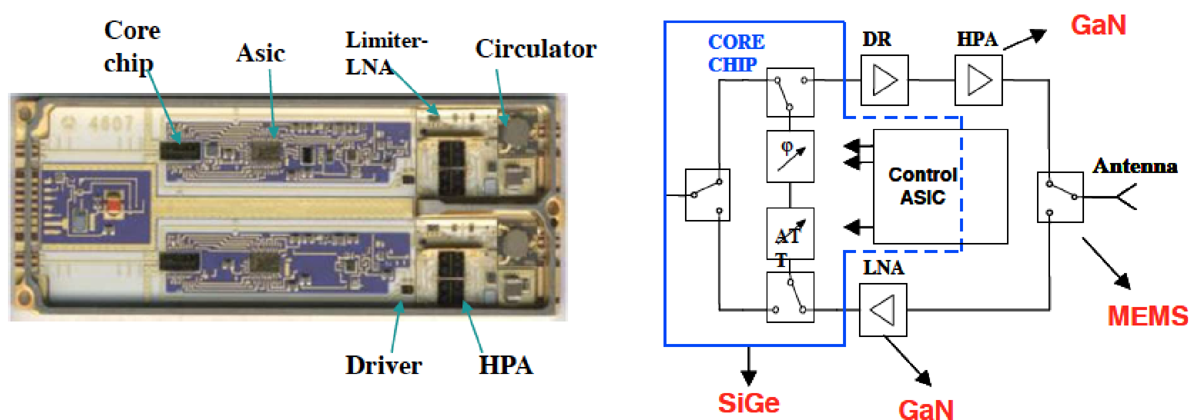

Figure 2.4: Example of a full module based on MMIC's -

as GaAs ones compared to Silicon based devices but with a much higher power density and thermal conductivity.

2.2 GaN devices and technologies

2.2.1 Silicon and wide bandgap devices

The following parameters are a relevant background to compare each material advantages and disadvantages :

- **Bandgap**: defined as the energy level difference between the lower and the upper side of the valence band of a material. It corresponds to the amount of energy needed by an electron to climb from the valence band to the conduction band. It determines the maximal temperature of operation of the device. Moreover, the higher the bandgap is, the less sensible to radiations the component is going to be.

- **Breakdown field**: defined as the maximum voltage a device can handle (with regards to its size) a device can handle before deterioration. High breakdown voltage is directly to high output power because the component can be biased at an high DC value and important voltage swings can be applied to it.

- **Electron mobility**: an high electron mobility will result in less resistive losses and thus better performances in terms of gain.

- **Thermal conductivity**: defines the ability of a component to dissipate heat. High thermal conductivity results in a device operating at a lower temperature and thus having better performances. This number strongly affects the device efficiency.

In Table 2.2, these key parameters are compared for Si, GaAs and GaN material. Looking at the numbers, it appears that GaN as a bandgap three times bigger than Si and a breakdown voltage ten times bigger. Consequently, a GaN based device would be able to handle voltage swings ten times higher than Si and then obviously generate much more power. More power means more DC power consumption and thus more heat too, but thanks to its high bandgap value GaN material will operate at a lower

temperature than a Si device so self heating is not going to be an issue. Silicon-Carbide (SiC) looks like a good candidate in terms of bandgap and breakdown field but it suffers from a low electron mobility. However, we will see in the following that its very high thermal conductivity makes it suitable for high temperatures operations.

Property	**Si**	**GaAs**	**GaN**	**4H-SiC**
Bandgap (eV)	1.1	1.43	3.4	3.26
Breakdown field (V/μm)	30	40	300	200$<$ 300
Electron mobility (cm$^2/s$)	1500	8500	1500 (2DEG)	700
Thermal conductivity (W/cmK)	1.3	0.55	>1.5	<3.8
Dielectric constant (Er)	11.7	12.9	9	9.7

Table 2.2: Material Properties

2.3 The HEMT GaN : a transistor dedicated to power applications

2.3.1 Transistor Basics

Historically the transistor was first invented at the Bell Laboratories in December 1947 by John Bardeen, Walter Houser Brattain and William Bradford Shockley, they received a nobel prize in 1956 for this discovery. Initially they tried to realize a field effect transistor (FET) as the one described by Julius Edgar Lilienfeld back in 1925 but they ended up discovering the phenomenon of current amplification which latter resulted in the heterojunction bipolar transistor (HBT). A transistor is a semi-conductor device with three terminals. It can either perform an amplifying function or a switch one (OFF or ON state). There are two different kinds of transistors, each having several variants. The first one is the HBT (Fig 2.5) which terminals are named, base, emitter and collector. Its behavior is mainly dictated by the current on its base, indeed current can flow between the collector and the emitter when the current applied on the base is high enough.The main parameter for this kind of transistor is its current gain β defined by : $I_c = \beta . I_b$. HBT transistors behave very well in terms of noise at low frequencies and can achieve very high oscillating frequencies too. Moreover they can achieve very interesting power densities which make them suitable for many different applications.

On the down side, HBTs suffer from self heating effects as their current increase with temperature so techniques such has emitter degeneration have to be used.

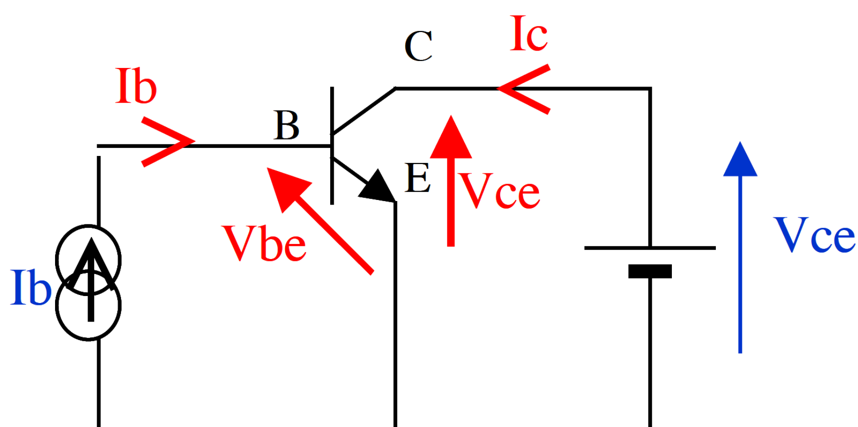

Figure 2.5: Heterojunction bipolar transistor -

The other kind of transistor is the FET (Fig 2.6), its terminals are called gate, drain and source. The amount of current flowing from the drain to the source is dependent on the source voltage. The most relevant parameter for this type of transistor is its transconductance gm defined by : gm $=I_d/V_{gs}$. Due to its intrinsic characteristics, this kind of transistor is well suited to perform as a switch, in fact a low value on its gate would result in the transistor to behave as an open circuit (OFF state) while a high value on its gate would make it behave as a short circuit (ON state). If the switching speed is high enough, then this transistor can perform various digital functions such as logic gates or processors for example, that is the case of CMOS transistors which are the devices of choice when talking about very large scale integration at low cost.

FET based transistors can also be of great interest for high power applications such as the MESFET (Metal semi-conductor FET) for example or more recently the high electron mobility transistor (HEMT). HEMT transistors have been the transistors used to make all of the designs presented in this thesis, so a special and detailed focus on them is made in the following part.

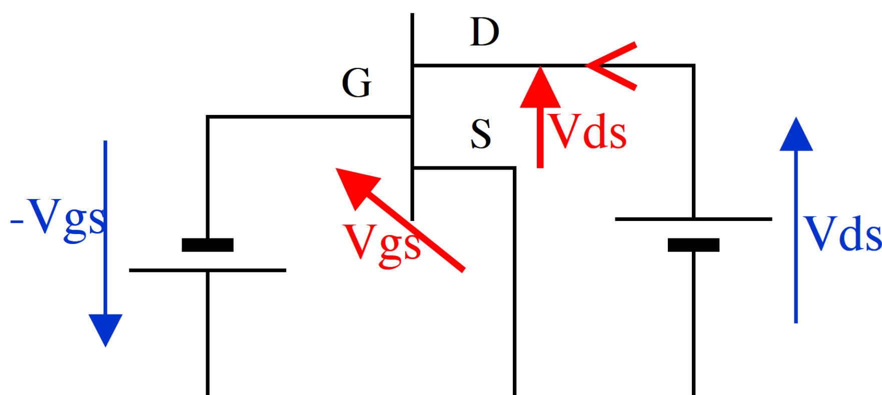

Figure 2.6: Field effect transistor -

2.3.2 The GaN HEMT

2.3.2.1 History and principle

HEMT (High Electron Mobility Transistor) appeared in the 80's and have been introduced as unique microwave devices with the smallest noise characteristic existing worldwide. The HEMT is seen as major evolution of the MESFET transistor and has replaced it in many cases since the 90's. Since then, it never stopped developing and can now be found in lots of electronic devices among which cellular phones or cars for example.

Even though it appears to behave as any FET transistor because the current flowing from drain to source is depending on the voltage applied to the gate, the mechanisms involved are quite different. Indeed it is made of an heterojunction and a junction between two material with different forbidden energy gaps. From this heterojunction, the creation of a very thin undoped canal with a low resistivity appears which results in very high electron mobility. This layer called the two-dimensional electron gas is the consequence of both spontaneous and piezoelectric polarization. So the fundamental transistor effect is here obtained with the modulation of this two-dimension gas by the gate voltage while in a MESFET transistor the gate voltage dictates the width of the conduction canal between drain and source.

2.3.2.2 Physical structure

Fig 2.7 represents the section view of an AlGaN/GaN HEMT transistor similar to the ones used in this work. It represents the layers involved in the realization of such a transistor. This picture is not technology specific but intends to describe the general architecture of any AlGaN/GaN HEMT.

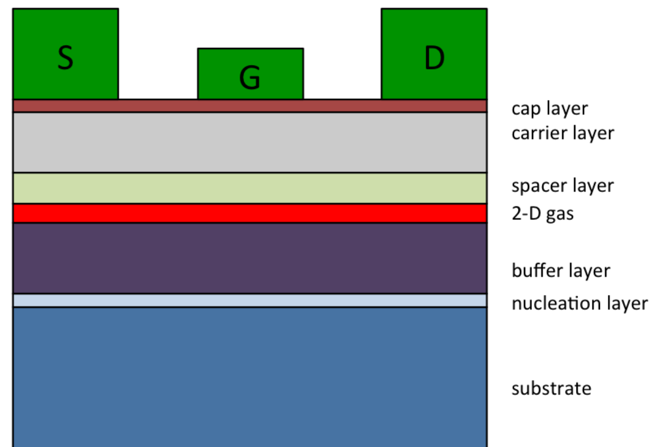

Figure 2.7: AlGaN/GaN HEMT cut view -

An HEMT transistor is composed of a substrate, a material with a large forbidden energy gap and another material with a smaller energy gap. As said earlier, it is the junction between these two materials that lead to the 2-D electron gas creation. An other important phenomenon is the presence of a Schottky junction between the gate metal layer and the substrate.

Here is a description of the layers presented in Fig 2.7 :

- **Substrate**: Due to their difficulty to manufacture and their high cost, GaN substrates are almost never used. 4H-SiC is a popular choice due to its good ability to dissipate heat and because it has the same crystalline network as GaN so they match easily. Diamond and Sapphire are best in terms of power dissipation but their cost prevent them to be used for mass market.
- **Nucleation layer**: Made of AlN, this layer prevents interfacial charges to happen for GaN on the SiC substrate.
- **Buffer layer**: This layer is made in a low forbidden energy gap material, GaN in our case. The 2-D gas appears in the upper side of this layer.
- **Spacer layer**: This layer is made of a larger forbidden energy gap material, AlGaN in this case. This non intentionally doped layer is only a few nanometers thick and permits to reduce the electrons-carriers interactions between the 2-D gas and the doped layer. The thicker this layer is, the fastest the electrons mobility is and the smallest the charger density is, and vice versa of course.
- **Carrier layer**: Made of large gap material such as doped AlGaN, this layer is a few nanometers thick and its aluminum concentration is around 20 to 30%.
- **Cap layer**: This is the upper layer and its goal is to produce good ohmic contacts for both drain and source.

2.3.2.3 Electrical characteristics

To design circuits with HEMT transistor, an electrical model is needed to perform simulations with CAD(Computer Aided Design) tools. Most of the time the small signal model is implemented with lumped elements such as the one presented in Fig 2.8. Basically, the transistor behavior is modeled by a voltage controlled current source.

These elements can be classified whether as intrinsic elements or extrinsic ones. Intrinsic elements are those inside the transistor which actually perform the transistor functions while extrinsic elements are the outside parasites such as the accesses. Both categories elements are listed and detailed in the following:

Let start with the intrinsic elements:

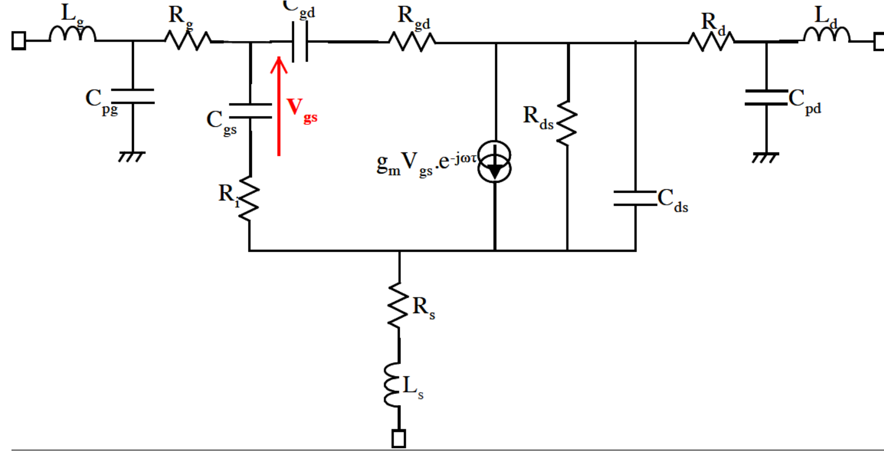

Figure 2.8: HEMT small signal electrical model -

- **Current source**: This is the main element describing the transistor effect. This current source is voltage controlled that models the phenomenon of gain inside the transistor. It is defined by :

$$I_{ds} = g_m v_{gs} e^{-} j^{\omega\tau}$$

(2.1)

τ models the delay due to the electrons transit time in the channel. The transconductance g_m is the fundamental transistor characteristic and represents the current variation modulated by the gate voltage, it is defined as :

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{v_{ds}=v_{ds0}}$$

(2.2)

- **Output conductances**: It represents the current variation modulated by the drain voltage.It is a representation of the channel resistance (g_d=R_{ds}) and is defined as :

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{v_{gs}=v_{gs0}}$$

(2.3)

- **gate capacitances**: The gate-source and gate-drain capacitances respectively C_{gs} and C_{ds} and illustrate the charge accumulation in the depopulated area located under the gate. C_{gs} models the variation of this charge accumulation modulated by the gate-source tension for a constant gate-drain tension and C_{ds} models this same variation modulated by the gate-drain tension for constant gate-source tension :

$$C_{gs} = \left.\frac{\partial Q_g}{\partial V_{gs}}\right|_{v_{gd}=v_{gd0}}$$

$$C_{gd} = \left.\frac{\partial Q_g}{\partial V_{gd}}\right|_{v_{gs}d=v_{gs0}}$$

(2.5)

- **Drain-source capacitance**: C_{ds} decries the capacitive coupling between the drain and source accesses.
- **Resistances**: R_i and R_{gd} model the fact that the channel is distributed. R_i is defined as the input resistance and permits to model the transistor input impedance while R_{gd} models the component feedback between input and output but is often neglected.

And now the extrinsic elements:

  - **Source resistance**: R_s models the resistive apsect of the ohmic contact between the source electrode and the active area of the channel.
  - **Drain resistance**: R_d models the resistive apsect of the ohmic contact between the drain electrode and the active area of the channel.
  - **Gate resistance**: R_g represents the losses due to distributed effect along the gate electrode
  - **Gate access capacitances**: C_{pg} and C_{pd} are the capacitances induced by the gate and drain accesses related to the substrate.

The most common and the easiest way to quantify an HEMT transistor behavior is through its I_{ds} versus both V_{ds} and V_{gs} charactherisitic. This plot is called the output static characteristic of the transistor. An example is presented in Fig 2.9. The drain source-current (I_{ds}) is plotted versus the drain-source voltage (V_{ds}) for various gate-source tensions (V_{gs}).

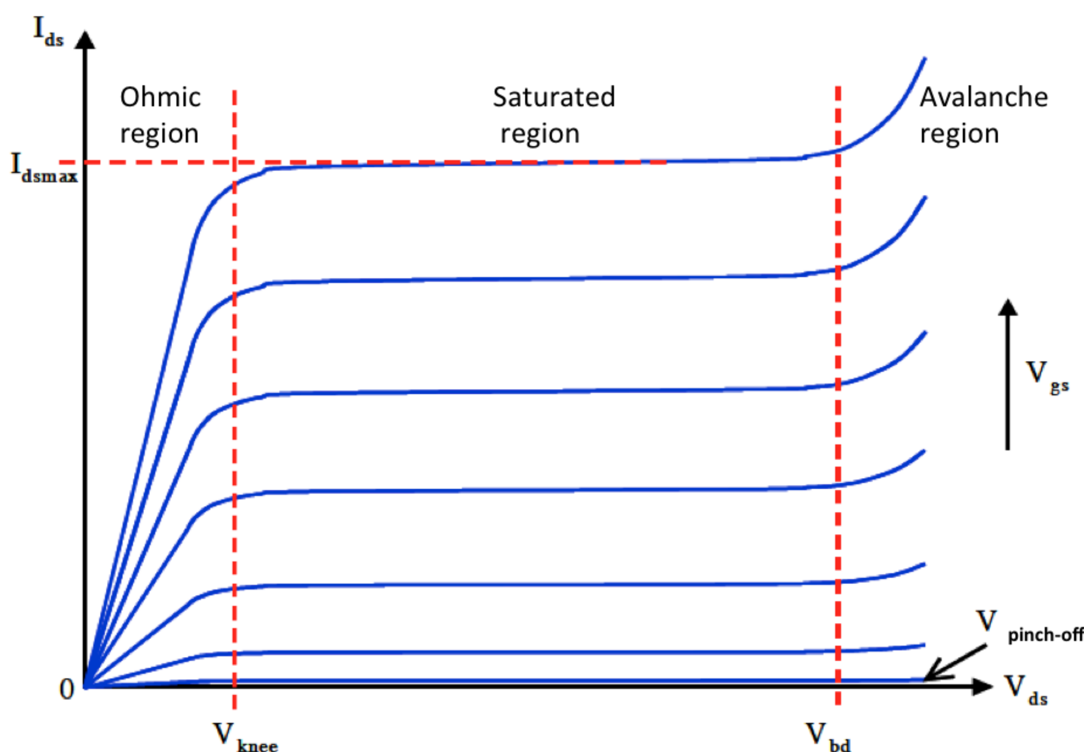

Figure 2.9: Output static characteristic of an HEMT transistor -

Four different regions or working modes can be discerned:

- **Blocked region**: Either or both V_{gs} and V_{ds} have values to low to activate the device so no current is flowing from drain to source. In this mode, the transistor ideally behave as an open circuit but in practical due to the parasitic elements it is approximated by a capacitance that grows with the transistor size. The transistor remains blocked while V_{gs} is lower than the transistor threshold voltage known as V_{th}.

- **Ohmic region**: I_{ds} increases linearly with V_{gs} and V_{ds}. In fact, with a V_{ds} increase the electrons mobility increases in the channel and the I_{ds} get

larger. This region is called the ohmic one because the transistor behaves as resistor, indeed the current is proportional to a voltage. This region is limited by the point (V_{knee}, I_{dsmax}).

To ensure being in this mode of operation the following conditions have to be fulfilled :

$$v_{gs} = >v_{th} \; and \; v_{ds}<(v_{gs} - v_{th})$$

(2.6)

- **saturated region**: In this region reached at v_{ds}=v_{knee}, the electron mobility limit has been attained so the drain-source current for a specific v_{gs} value can not increase any more even if v_{ds} keeps being increased. I_{ds} is at its saturated value (I_{dSmax}) hence the name of the region. The transistor ideally behaves as a current source because its current value is not affected by the voltage between drain and source. To ensure being in the saturated region, these conditions have to be respected:

$$v_{gs} = >v_{th} \; and \; v_{ds}>(v_{gs} - v_{th})$$

(2.7)

- **avalanche region**: When the field in the channel reaches its critical value, an avalanche phenomenon occurs. Electrons and holes are liberated more and more till a strong and fast increase of the drain-source current. This phenomenon is irreversible and results in the device destruction. This phenomenon happens when v_{ds} reaches the transistor breakdown value known as V_{bd}.

2.3.2.4 Figures of merit

To judge of a transistor performances and capacities three figures of merit have been defined, two of them are frequency related and the third one is noise related:

- **cut off frequency**: f_t is the frequency at which the transistor current gain in short circuit is equal to the unity:

$$f_t = \frac{g_m}{2.\pi(c_{gs} + c_{gd})}$$

(2.8)

- **maximal oscillating frequency**: f_{max} is the frequency at which the matched transistor transductic gain is equal to the unity. If the assumption that $(R_i C_{gd} \omega)^2 << 1$ is made then :

$$f_{max} = \frac{g_m}{4.\pi C_{gs}} (\frac{1}{R_i.C_{gd}})^{\frac{1}{2}} = \frac{f_t}{(4.R_i.C_{gd})^{\frac{1}{2}}}$$

(2.9)

- **noise factor**: NF determines the noise generated by a device and is defined as :

$$NF = 2.\pi.C_{gs}(\frac{R_g + R_i}{C_{gm}})^{\frac{1}{2}}$$

2.4 Power Amplifier Design

2.4.1 Definitions

Let's start with a few definitions related to power amplifiers, they will be classified under the following categories : power, gain, efficiency and linearity.

2.4.1.1 Power

Fig 2.10 is an illustration of the input and output power paths in a generic amplifier. V_{sin} is assumed to be an RF source delivering a signal at a frequency f_0.

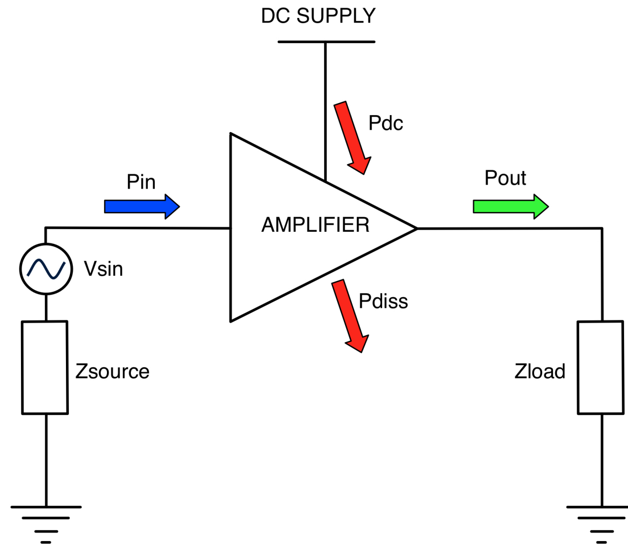

Figure 2.10: Power coming in and out an Amplifier -

According to physical law of conservation of energy, the total amount of energy getting in a physical device has to be strictly equal to the total amount of energy getting out this same device, then :

$$P_{in} + P_{dc} = P_{out} + P_{diss}$$

(2.11)

For a periodic signal of period T=1/f_0, the RF input power (P_{in}) and the RF output power (P_{out}) can be obtained with the following formula:

$$P = \frac{1}{T}\int_0^T v(t).i(t)\,\mathrm{d}t$$

(2.12)

In the case of sinusoidal waves, the medium output power is defined by :

$$P_{out} = \mathbb{R}[\frac{1}{2}V_{out}.\overline{I_{out}}]$$

(2.13)

It is a common thing to model the output impedance by a purely resistive load R_L, in this case the output power can be expressed as:

$$P_{out} = \frac{{V_{out}}^2}{2.Z_{load}}$$

(2.14)

From Eq 2.14, we can notice that the output power is proportional to the square of the output voltage and that it decreases when the output load increases. We will comeback to this latter when talking about the advantages of wide bandgap devices for high output power applications. The amount of power delivered by the power supply is defined by :

$$P_{dc} = \frac{V_{dd}}{I_{dd}}$$

(2.15)

The amount of power which is not going out through the output load is dissipated through heat (P_{diss}). Low efficiencies amplifiers dissipate a lot of power through heat instead of delivering power the load. The official unit to express a power quantity is the Watt, however it is common to express it in dBm too. The conversion from one to an other is done with :

$$P[dBm] = 10log(1000.P[W])$$

(2.16)

2.4.1.2 Gain

When considering radio-frequencies circuits, the power gain is most of the time the one considered rather than the voltage gain. The traditional definition for the power gain is the transductic gain G_T that can be expressed by:

$$G_T = \frac{P_{out}}{P_{avail}}$$

(2.17)

where P_{out} stands for the output power delivered to the load and P_{avail} stands for the power available at the amplifier input. P_{avail} is equal to P_{in} defined earlier if and only if the source and the amplifier input are perfectly matched to each other, otherwise there are losses and P_{avail} is lower than P_{in}.

$$G_T[dB] = P_{out}[dBm] - P_{in}[dBm]$$

(2.18)

The power gain is maximal for low level input power, that is to say when all the devices making the amplifier are working in linear mode and not in saturation. The gain at saturation or the gain under compression are critical values too when considering an RF power amplifier. This gain is lower than the linear transductic gain (G_T) but is the one that matters when the amplifier is under conditions to deliver maximal power to the load (input power high enough) .

2.4.1.3 Efficiency

Efficiency is a critical criteria to judge the quality of a power amplifier. Indeed, it quantifies the ability to deliver power to a load while dissipating as less as possible through it. It specially matters in systems that are battery powered in order to increase lifetime or in embedded systems where heat dissipation can be an issue. There are, two main definitions to characterize an amplifier efficiency. The first one is called energetic efficiency and is defined as :

$$\eta = \frac{P_{out}}{P_{dc}}$$

(2.19)

This definition assumes that a power amplifier is actually a device that converts a DC energy into a RF energy. Thus, η is a number which quantifies the quality of the energy conversion. A value of 1 for η would mean that all the DC energy is converted into RF one, however due to the actives

devices parasitics and to the passive devices losses, this value can never be reached. A much more useful definition for power amplifiers is the Power Added Efficiency (PAE) which is expressed by:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \eta(1 - \frac{1}{G_T})$$

(2.20)

The advantage of this definition is to combine both the energetic efficiency and the amplifier gain. In fact, high PAE are achieved with high gain (P_{out}-P_{in}) and low DC consumption.

2.4.1.4 Linearity

An amplifier is considered to be linear as long as the output signal follow a linear evolution compared to the input signal. This can be traduced by the fact that the amplifier keeps the same gain even if the input power is increasing. If it were the case, amplifiers could achieve an infinite output power, of course it does not work like that. Every amplifier has an output power limit and whatever is the input power the output power will never go beyond this limit. This limit is called the saturated output power. What actually happens is that when increasing the input power, the gain will start to slowly decrease and thus the amplifier will not have a linear behavior anymore. The amplifier is said to work in compression when its gain starts decreasing from its small signal value. The input and output power values for with the gain has decreased by 1dB are values used to characterize an amplifier. From this, we can define the three following parameters:

* **P_{sat}**: Saturated output power. The maximal output power that can be reached by an amplifier regardless its input power.
* **ICP1**: Input compression point at 1dB. It is defined as the input power value for which the small-signal gain as decreased by 1dB.
* **OCP1**: Output compression point at 1dB. It is defined as the output power value for which the small-signal gain as decreased by 1dB.

If ICP1 and OCP1 are expressed in dBm and if G_T is expressed in dB then:

$$OCP1 = ICP1 + G_T - 1$$

(2.21)

Fig 2.11 is a graphical representation of the compression phenomenon. The left plots represents the output power versus the input power and we can notice that the evolution stops being linear at some point and the output power ultimately stops increasing at all to reach its saturated value. On the right plot, we can see that the gain decreases slowly while the input power increases till it reaches the 1dB compression point and then it drastically drops all the way down.

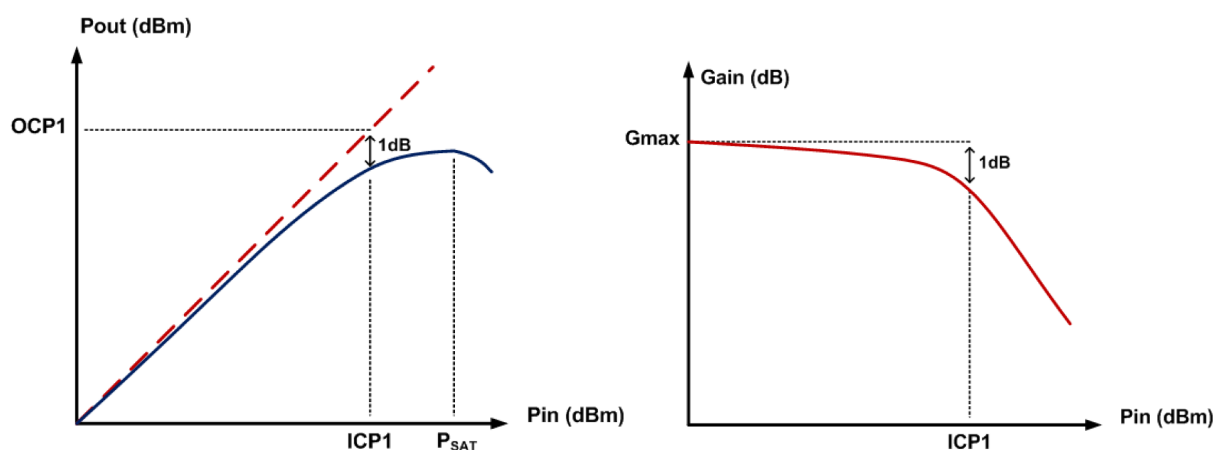

Figure 2.11: 1dB input and output compression point -

2.4.2 Power Amplifier Basics

The study of a PA can either be done in linear mode of operation or large signal (non-linear) one. There are several parameters for each case which determine the performances of a PA. Most of the time, PA design is a combination of both linear and large signal behavior because most applications require specifications for each. A PA is considered to work in linear mode of operation whenever its input signal is small enough that it will not put

any active devices in saturation. One way to describe the linear behavior of a system is the use of scattering parameters (S-parameters). This approach is very popular especially for PA working at RF frequencies and beyond. It has the advantages to give many informations over a single analysis (whether it is simulation or measurement). Indeed, information such as input and output matching, gain and stability can be extracted directly from an S-parameter analysis. The principle of such an analysis is illustrated in Fig 2.12 for a 2 ports device. The amplifier is considered as a black box with a main input (in_1) on the left side and a main output (out_2) on the right side, an alternate output (out_1) and an alternate input (in_2) are also present to model reflection phenomenons.

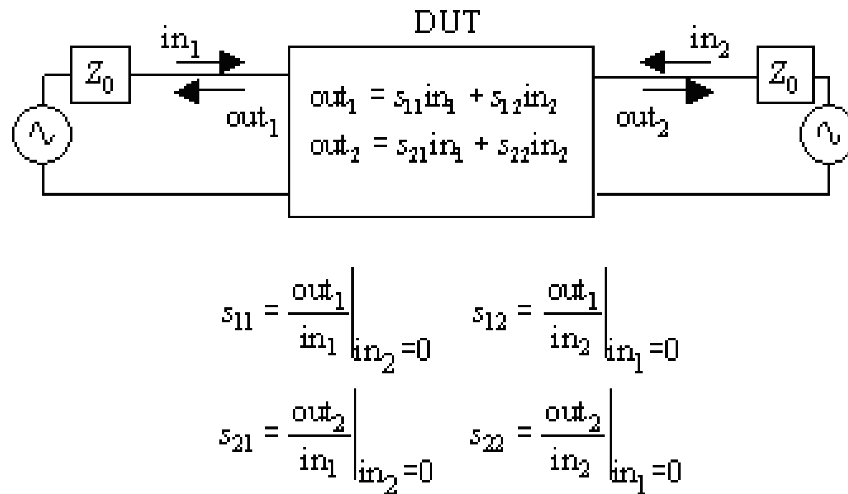

Figure 2.12: Scattering Parameters principle -

The analysis technique consists in exciting alternatively each input and quantifying the amount of signal that is transmitted through the device and the amount reflected back to the excited input. Performing this analysis at each input results in the obtention of a scattering matrix composed of the following four parameters:

* **S_{11}**: Input reflection coefficient. Amount of the signal when excited through in_1 that does not go through the device but that is reflected back to the source through out_1. This parameter gives information on

the input matching, an ideal PA would have S_{11} equal to 0, meaning that the signal applied through in1 fully carries through the amplifier and none is sent back to the source.

* **S_{22}**: Input reflection coefficient. Amount of the signal when excited through in_2 that does not go through the device but that is reflected back to the source through out_2. This parameter gives information on the output matching, an ideal PA would have S_{22} equal to 0.
* **S_{21}**: Transmission coefficient. Amount of the signal when excited through in_1 that goes through the device and that is outputted through out_2. Also known as the device gain, it gives information on how much the device amplifies the input signal, the greater S_{21} is, the more gain an amplifier has.
* **S_{12}**: Isolation coefficient. Amount of the signal when excited through in_2 that goes through the device and that is outputted through out_1. This parameter gives information on the device stability, an ideally stable amplifier would have S_{12} equal to 0, meaning that any signal sent through out_2 can not go all the way back to in_1.

Most of the time, S_{21} and S_{12} parameters are expressed in dB and plotted versus frequency over a linear scale. A value of 0dB corresponds of a magnitude of 1, for example a device S_{21} equal to 0dB will output an exact copy of the input signal in terms of shape and amplitude. If S_{21} is negative in dB then the output signal will have a lower amplitude than the input one and if S_{21} is positive, then the amplitude of the output signal is going to be greater than the the input one and in this case we can talk about signal amplification. The reflection coefficients S_{11} and S_{22} can be expressed in dB versus frequency too but then it only gives information about the magnitude. It is commonly admitted for a power amplifier that S_{11} and S_{22} have to be lower than -10dB to ensure proper matching, it corresponds to no more than 10% of the signal being reflected to the source (or the load). To obtain informations about both magnitude and phase, reflections parameters can be plotted on a Smith Chart too. This visualization method is oftener used for impedance matching and to design matching networks.

An example of S-parameters plot is presented in Fig 2.13 for both a linear representation and a Smith Chart representation.

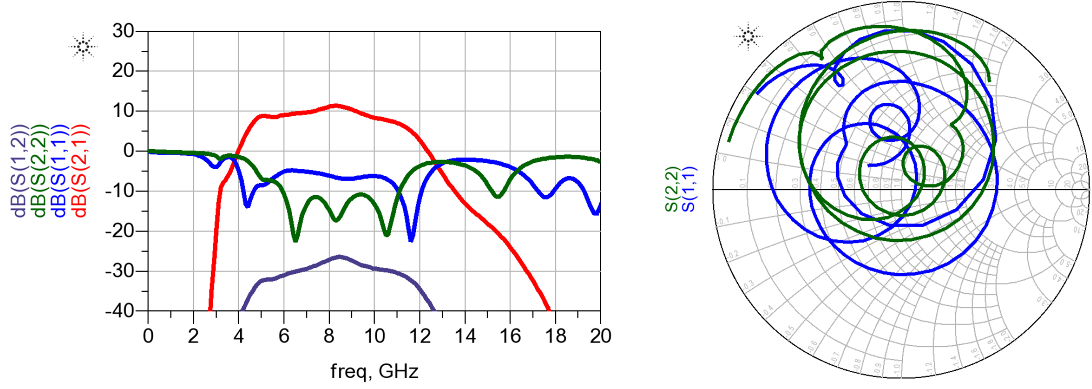

Figure 2.13: Example of S-parameters plots (linear and Smith chart) -

From an S-parameters analysis, information on linear stability can be extracted too. For any amplifier, stability is critical criterion to ensure. Indeed, an unstable amplifier is very likely to oscillate and thus not to behave as expected. To avoid this behavior, the amplifier must be unconditionally stable for every frequencies, unconditionally meaning for every impedances within the smith chart. A criteria to ensure unconditional stability has been proposed by John Rollet, it is called the Rollet's stability factor, but it is commonly called K-factor.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2}{2|S_{21}S_{12}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

(2.22)

This factor is calculated from S-parameters and is defined by Eq 2.22. Unconditional stability is theoretically ensured while K-factor remains over the unity. However, the K-factor is only relevant for a one stage amplifier. Indeed for a two (or more) stages amplifier, a value of k over one is not enough to ensure stability. It is preferable to consider the Rollet's stability factor as an informative parameter better than anything else. Let say that an amplifier with a K-factor under one is unstable for sure and that an amplifier with K-factor greater than one as a chance to be stable. In Fig 2.14,

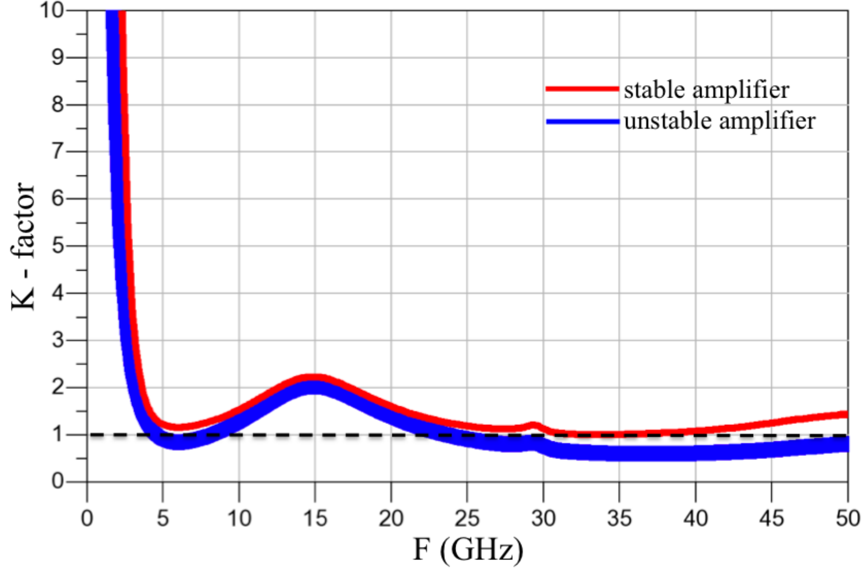

Figure 2.14: Stable amplifier vs. unstable amplifier -

the example of a stable amplifier and an unstable one is illustrated. The red plot corresponds to stable one where K remains over one from DC to 50GHz while the blue plot goes under one multiple times which correspond to an unstable and potentially oscillating amplifier.

Besides the Rollet factor, an other criteria know as the μ-factor can be used as a proof of unconditional stability. The μ-factor is defined in Eq 2.23, unconditional stability is ensured if μ is greater than one. This formula applies for any two port devices wether it is single or multi stage, so a more valuable information can be extracted from the μ-factor than from the k-factor. In practical, it is mandatory to check both factors and ensure they are greater than one.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \overline{S_{11}}\Delta| + |S_{12}S_{21}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

(2.23)

2.4.2.1 Power Amplifier Classes

Power Amplifiers are commonly designated by their classes. The class of operation an amplifier refers to both its bias point and to output voltage and current waveform shapes. Depending on the class, the amplifier will exhibits better performances either in terms of linearity or in terms of efficiency, the choice being mainly commanded by the application targeted. Amplifier classes can be separated into two main categories : sinusoidal classes and non-sinusoidal ones. It is important to notice than GaN based technologies do not offer complimentary transistors (as p-mos in cmos technologies for example), thus topologies and classes are limited.

Class A, B and C are known as the sinusoidal ones because the output voltage wave as a sinus shape, here is a description for each of these classes:

* **Class A**: The amplifier is biased at a DC value equal to half the saturation current, meaning that it conducts at all time for both the positive and the negative half of the input wave. It is the best class in terms of linearity but the worst in terms of efficiency as transistors never switch of and thus always draw current even when there is no input signal.
* **Class B**: The amplifier is biased at a DC value precisely equals to the transistor threshold voltage, thus there is conduction only half of the time when the input signal is positive and the transistor remains off when the input is signal is negative. The efficiency is better than for class A amplifiers but the linearity is degraded. A push-pull configuration can be used to improve linearity, where a n-type transistor will take care of the positive half of the signal and an p-type one handles the negative side.
* **Class C**: The amplifier is biased at DC value lower than the threshold voltage so conduction happens only when the input signal is high enough, current is drawn less than half of the time. The efficiency is increased compared to a class B amplifier but the linearity is even more decreased.

Fig 2.15 is the representation of the output waveforms (both current and voltage) for the A, B and C classes. Voltage and current are both normalized, a value of one corresponding to quiescent voltage and current. We can notice that current is drawn at all time for class A, half of the time for class B and less than half of the time for class C.

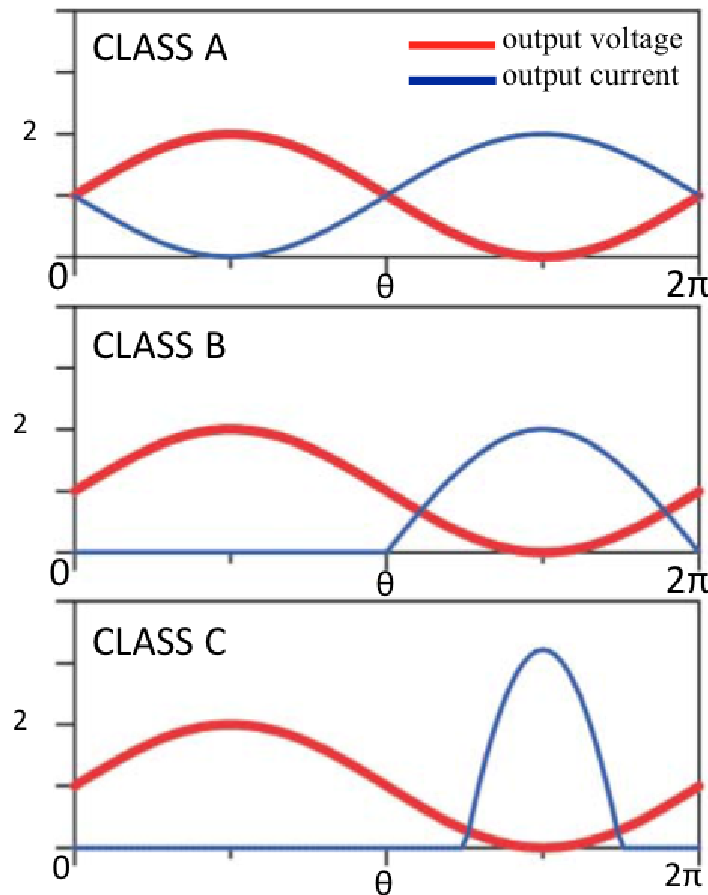

Figure 2.15: Sinusoidal amplifier classes -

It is possible bias the amplifier at a point located somewhere between class A and class B, this is a called deep AB class. It consists in biasing transistors at 10 to 20 % of their saturated drain current, it has the advantage of drastically improving the efficiency when compared to class A operation and have an interesting behavior in terms of output power. Of course, linearity is strongly degraded but this is not a problem for applications

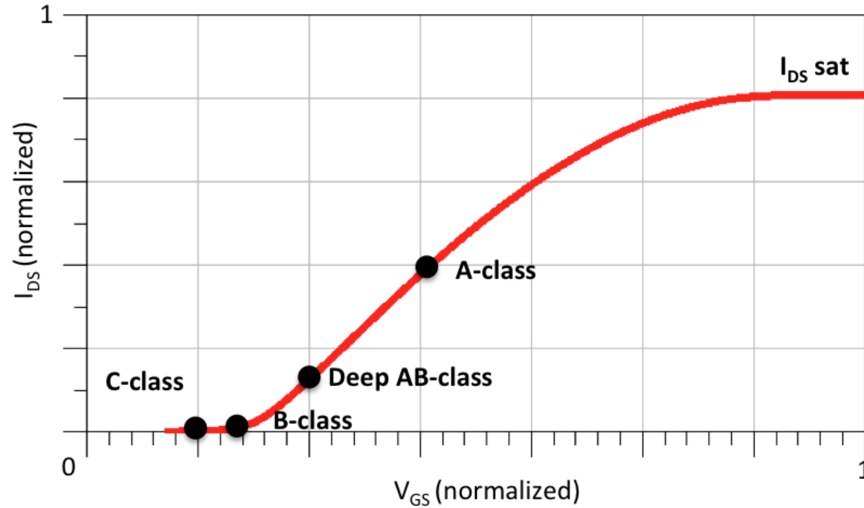

Figure 2.16: Amplifier classes vs. bias point -

such as military one where linearity is not required. Most of the amplifiers realized in this thesis have been biased in deep AB class at 10% of their saturated drain current.

In Fig 2.16, classes of representation are placed on a $I_{DS}(V_{gs})$ plot. As expected, class A corresponds to a quiescent current equal to half of I_{Dsat}, class B is set exactly at the threshold voltage and deep AB class is somewhere in the 10 to 20% of I_{Dsat} region.

The non sinusoidal classes are based on making the active device work as a switch, that is to say being either in off-state or in saturated mode of operation. Ideally, in this kind of behavior either the current or the voltage is equal to zero, so the efficiency is maximal. However, transistors are not perfect, in fact they have parasitic impedances and capacitances so there is a non negligible amount of time where current and voltages are both non equal to zero. Moreover, these non sinusoidal classes often use impedance harmonic tuning for wave forming matters, which make them non suitable for wideband applications. The more common classes, D, E and F are depicted in the following :

* **Class D**: Class-D amplifiers use two or more transistors (in push-pull like configuration) as switches to generate a square drain-voltage

waveform. A series-tuned output filter passes only the fundamental-frequency component to the load. Current is drawn only through the transistor that is on, resulting in a 100% theoretical efficiency for an ideal amplifier. However parasitics detailed before and non-zero switching time of transistors quite decrease this theoretical value.

* **Class E**: Class E employs a single transistor operated as a switch. The drain voltage waveform is the result of the sum of the DC and RF currents charging the drain-shunt capacitance. In optimum class E, the drain voltage drops to zero and has zero slope just as the transistor turns on.

* **Class F**: Class F boosts both efficiency and output by using harmonic resonators in the output network to shape the drain waveforms. The voltage waveform includes one or more odd harmonics and approximates a square wave, while the current includes even harmonics and approximates a half sine wave.

As for the sinusoidal classes, a normalized representation of the output waveforms is represented in Fig 2.17 for each of the D, E and F classes. It can be noticed that there is no overlapping between voltage and current waves.

Over the past years, new classes have been introduced but they more an improvement of already existing classes than whole new classes. For example, a class S amplifier is actually a class D amplifier which converts analog signals into digital pulses thanks to a delta-sigma modulator. An other one is class J, which actually consists in biasing the amplifier in deep AB class and presenting specific impedances to the harmonics in order to improve efficiency. Table 2.3 summarizes for all the classes depicted earlier the conduction angle (equivalent to time the transistor conducts over a period) and the theoretical efficiency for and ideal amplifier. To conclude, when linearity is critical class A should be privileged at the cost of efficiency. Non sinusoidal classes are of great interest to achieve very high efficiencies but their linearity is very poor and the harmonic impedance tuning techniques deployed prevent them to be implemented on wideband amplifiers. Thus,

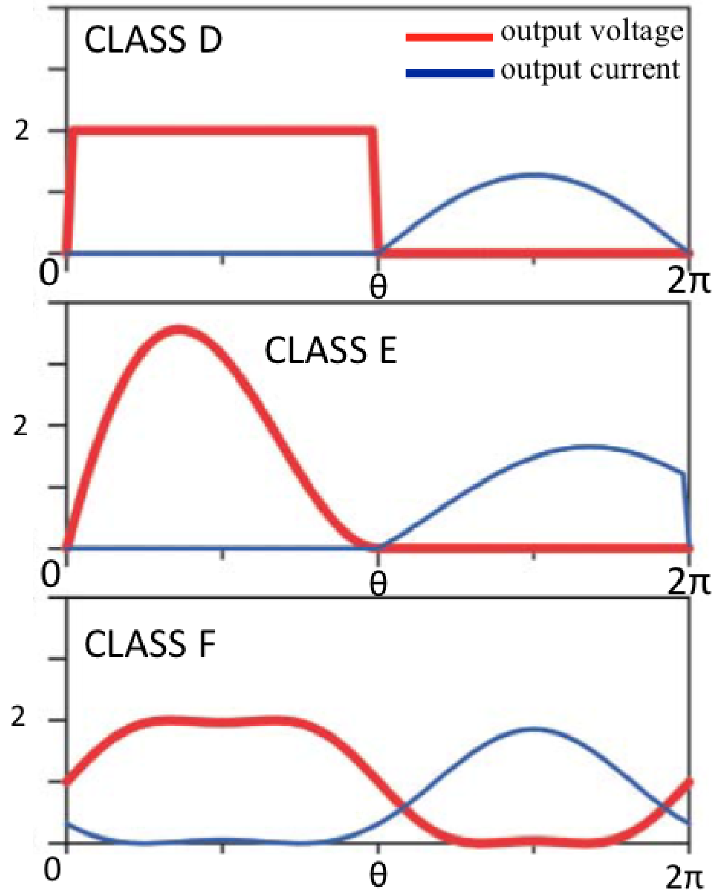

Figure 2.17: Non Sinusoidal amplifier classes -

the AB class appears to be a good compromise between efficiency, power and wideband capabilities.

2.4.3 Amplifiers Topologies

Even though, there is an important amount of topologies from the most basic one to very exotic and unusual approaches, power amplifiers architectures can be classified in two main categories : single ended or balanced/differential. To increase performances such as gain or output power, it is common to cascade or parallelize several elementary cells. In the following a description of each approach is given together with some examples to illustrate them.

Class	Conduction Angle	Maximal Theoritical Efficiency
A	360°	50%
AB	180°to 360°	50% to 78.5%
B	180°	78.5%
C	<180°	100%
D and over	ON/OFF switching	100%

Table 2.3: Amplifiers classes summary

2.4.3.1 Single-ended topologies

The single-ended approach basically consists in having one input and one output without any combining devices. The most simple structure is based on a single transistor and is called common-source architecture (Fig 2.18). The transistor gate acts as the RF input, the drain is the RF output and the source is grounded hence the common-source determination. Matching networks are placed at the gate and the drain for the amplifier to work at the desired frequency.

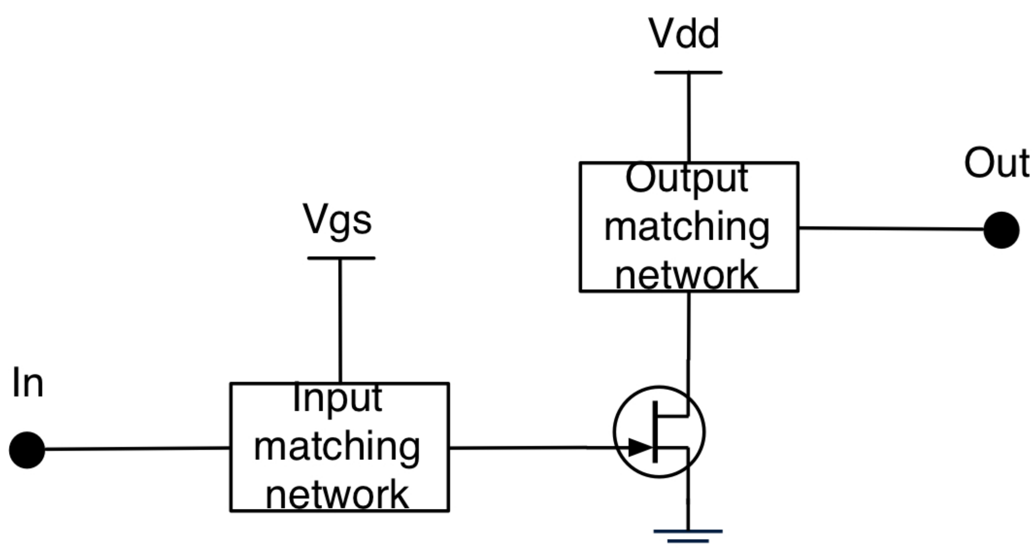

Figure 2.18: Common-source power amplifier -

This topology is pretty simple to implement and offers good performances in

terms of gain and frequency, however it suffers from a poor isolation making it though to optimize and easily unstable specially at low frequencies where the transistor has an important intrinsic gain. However, this low frequency stability issue can be fixed by placing an high pass filter on the transistor gate in order to decrease gain at low frequencies while not modifying at higher frequencies. Other variants based on a single transistor exist like the common-gate (gate grounded) or the common-drain (drain grounded) but they do not perform as well as the common source method so they are not used very much as power amplifier elementary cells.

To improve the isolation and the power ability of a common source amplifier, an interesting approach is the cascode one (Fig 2.18). It consists in inserting a common-gate transistor on top of a common-source one. Indeed, the input and the output are now separated by two transistors instead of one which makes the isolation much higher. Moreover, by having two transistors in cascade, the supply voltage can be increased by a factor of two which results in a drastic increase regarding the output power.

However, cascode amplifiers can be though to stabilize, even impossible under certain conditions. An other issue is the connection between common-source drain and the common-gate source. Indeed, physically this connection is a transmission line which acts as low pass filter together with both transistors parasitic capacitances and this results in a decreased maximal frequency of operation.

2.4.3.2 Balanced / Differential topologies

Balanced and differential topologies consist in combining or parallelizing several single-ended elementary cells such as common-source or cascades ones. The main advantage is the increase in terms of output power(two cells parallelized would deliver the amount of power as a single cell) with no costs on the gain but the main drawback is the need for splitters and combiners to make the cells work together. Combiners have losses that would affect the overall performances and they can fulfill a large die area which affects the cost of the overall amplifier.

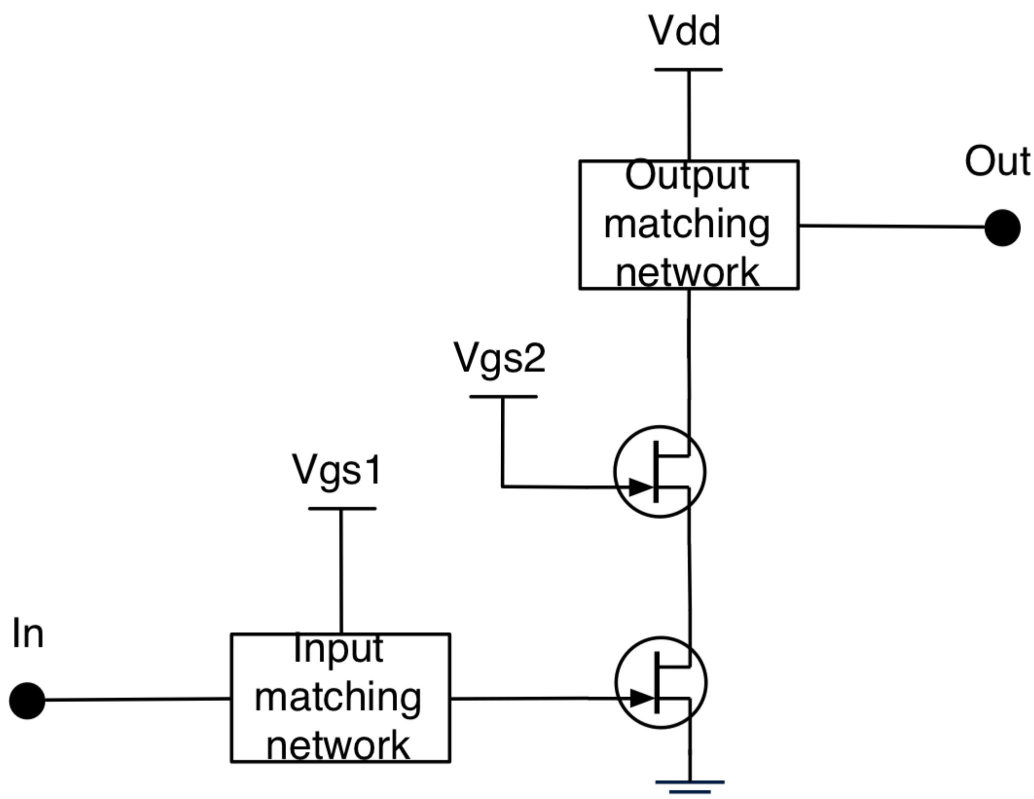

Figure 2.19: Cascode power amplifier -

The easiest way to implement such an amplifier is the current combining approach Fig 2.20). Two elementary identical cells are parallelized and combined in phase. This combination can be easily done with a current splitter/combiner such has a wilkinson one, which is only composed of transmission lines and a resistor to ensure isolation between the two paths.

This approach benefits from the wilkinson combiner advantages which are the ease of design and the low loss abilities, so very good results in terms of output power and efficiency are usually obtained. However, these kind of combiners are based on transmission lines whom length need to be equal to $\lambda/4$ of the working frequency . This results in very large size combiners and limited bandwidths. Even though, the combiner can be improved in terms of bandwidth by adding parallel elements to it at specific places,

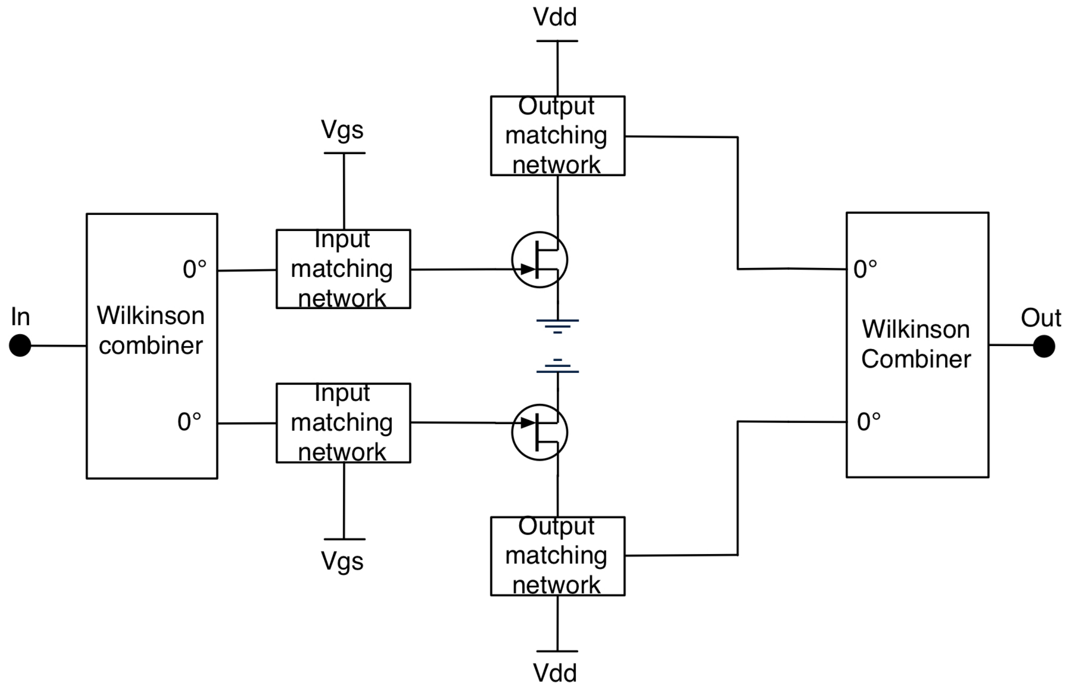

Figure 2.20: Current combined power amplifier -

its size remains a critical issue. Moreover, an exact symmetry has to be respected in between the different paths or the cells are going to be imbalanced which would result in poor performances in the best case and the amplifier destruction in the worst case.

An other approach consist in using 3-dB couplers (Fig 2.21) to split and combine power between the elementary cells. With this topology a phase difference of 90°is generated by the coupler between the two paths, so it is mandatory to use the same kind of coupler for splitting and combining to make sure to recombine the cells in phase at the output.

With a coupler approach, bandwidths of more than an octave can be achieved without many troubles and thus with losses small enough to ensure reasonable performances in term of output power and efficiency for the overall amplifier. However, couplers are quite large to implement even though slitghly smaller than current combiners like wilkinson ones.

The two topologies presented are known as balanced or pseudo-differential

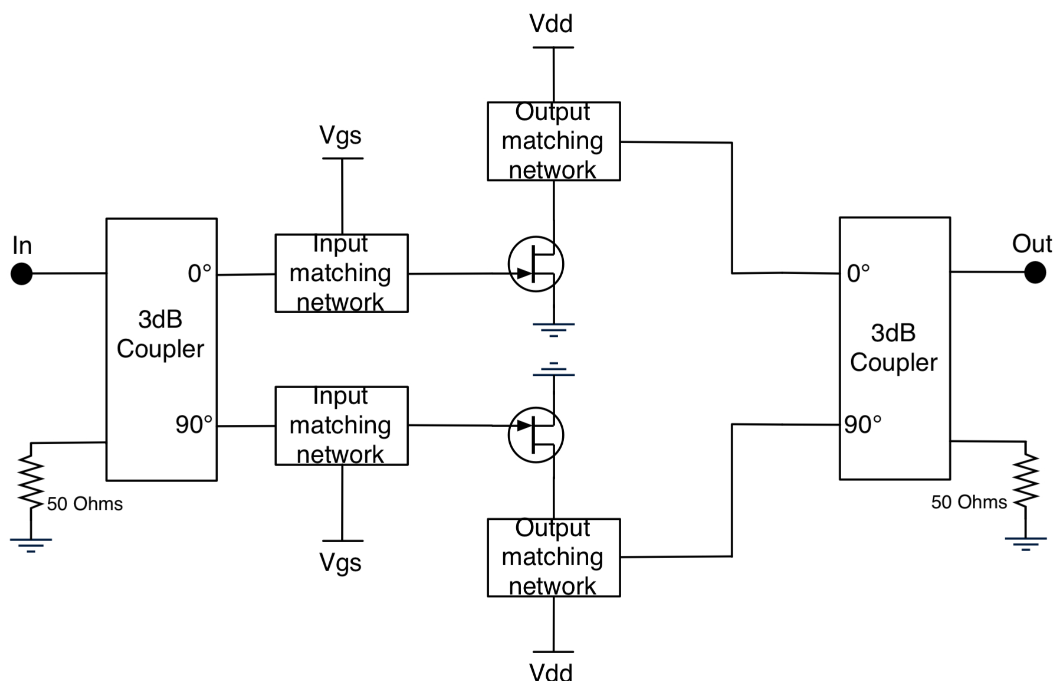

Figure 2.21: Balanced (pseudo-differential) power amplifier -

techniques, there advantages have been exposed but they suffer from some limitations that can be resolved with a fully differential topology (Fig 2.22). In this approach, baluns (balanced/unbalanced) transformers are used to perform power splitting and combining functions. A balun is made of two inductors close to each other (side by side or one on top of the other) and the transfer of energy is made through electrical and magnetical coupling. From a single source it generates two outputs in phase opposition (180°) between the paths.

Baluns happen to be much smaller than any other kind of combiners. Moreover, matching networks can be included within the balun by adding capacitors in parallel to the balun and by optimizing the balun impedance transformation ration. An other advantage, is that the balun middle point can be used to bias (input balun) and supply (output balun) the power cells. All of that results in a drastic size reduction of the overall amplifier, indeed not only baluns are small but they can perform multiple tasks too. Large

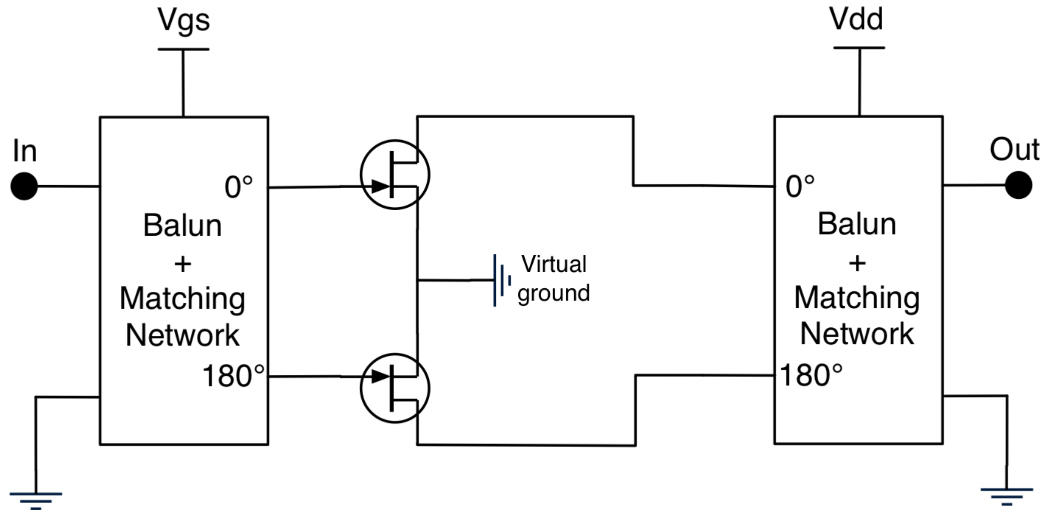

Figure 2.22: Differential power amplifier -

bandwidths can be achieved with baluns (sometimes equal to a decade) making it a very good candidate for wideband applications. The fully differential approach leads to generation of a virtual ground, this helps a lots in terms of symmetry and parasitic rejection too. On the down side, baluns can be very complicated to design and optimize. Indeed, time consuming electromagnetic simulations are mandatory to design a balun. Regarding losses, baluns do not perform as well as current combiners and couplers but they still allow to achieve decent performances.

Table 2.4 is a summary of the advantages and disadvantages of each topology presented. From the basic but very efficient single-ended common-source amplifier with to quite complex fully differential balun based amplifier with enhanced performances and reduced size, the critical choice of topology will have to be made depending on the performances to achieve and on the time and cost that can be spend to realize the amplifier.

2.4.4 Wideband amplifiers

In nowadays, more and more applications require wideband systems and thus wideband power amplifiers. In civilian applications, this need can

Topology	Bandwidth	Performances	Ease of design	Size
Common source	+++	+	+++	+++
Cascode	++	++	++	+++
Wilkinson combined	+	+++	++	+
Coupler combined	++	+++	++	+
Balun combined	+++	++	+	+++

Table 2.4: Wideband amplifiers comparison

come from high speed transfer datas such as optical fibers for example. Military applications have not miss this trend and require wideband emitters and receivers too for radar or electronic warfare matters. An amplifier is considered to be wideband if works a bandwidth greater than an octave. If F_{min} is the minimal working frequency of the amplifier and F_{max} its maximal one, then the condition : $F_{max} \geq 2.F_{min}$ has to be fulfilled so the amplifier can be called a wideband one. The main issue is to obtain constant performances all over the bandwidth of interest. Indeed, active devices have much more gain at low frequencies than at higher ones and their optimal impedance change a lot with frequency. That is why, it is necessary to use some dedicated techniques to flatten the response all over the frequency range of interest. In the following, the most common techniques to do so are presented.

2.4.4.1 Reactively matched amplifiers

The principle of a reactively matched amplifier (Fig 2.23) consists in introducing resistors connected to the ground in parallel of both the gate (R_{in}) and the drain (R_{out}) access of the transistor. This resistors allow to control the gain in lower frequencies and thus to obtain a flat gain all over the bandwidth. Inductors in series are added in between resistors and ground (L_{in} and L_{out}) in order to bypass resistors at higher frequencies and thus make their effect negligible. As power supplies are equivalent to ground from an RF point of view, these elements can be included in the biasing network (R_{in}, L_{in}) and the supply network (R_{out}, L_{out}).

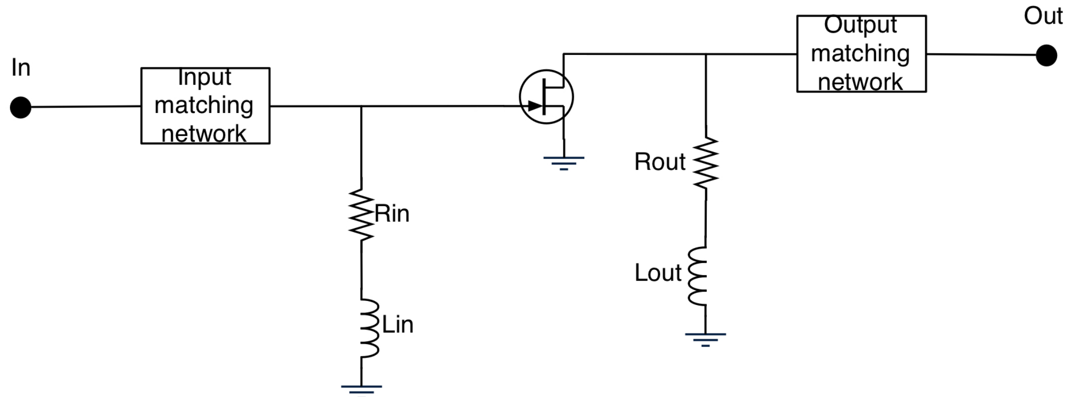

Figure 2.23: Reactively matched amplifier -

This kind of topology of topology require high gm active devices to exhibit good performances. However, these devices have important input and output capacitances which complicate the realization of matching networks, and that implies more loss in these networks. Moreover, this topology does not produce highf gain and even if it is possible to cascade several stages to increase it, a strong attention has to be made to the overall stability. To conclude, a reactively matched amplifier is pretty simple to design but its bandwidth will not be able to exceed much than an octave and the gain flatness will not be very good.

2.4.4.2 Feedback amplifiers

The feedback amplifier topology (Fig 2.24) consists in placing a resistive (R_{fb}) network between the input and the output of the active device. A capacitor (C_{fb}) and an inductor (L_{fb}) are also present in this serial network respectively to cut the DC component and to bypass the feedback at high frequencies. This kind of feedback permits to control the gain at lower frequencies and thus to flatten it over a wide frequency band.

As for the reactively matched topology, the feedback one require high gm transistors and thus high input and output capacitances, which results in harder matching networks to design. By cascading several feedback ampli-

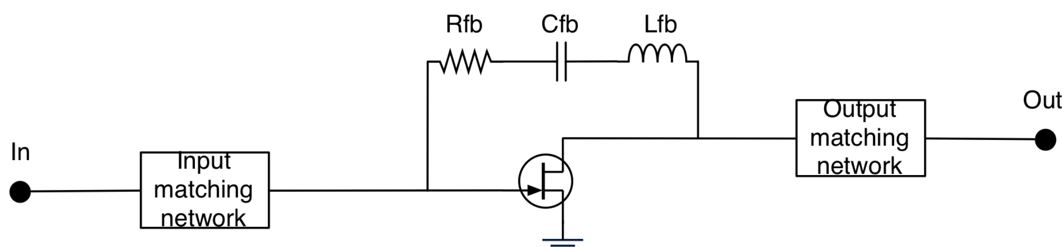

Figure 2.24: Feedback amplifier -

fiers and optimizing them each, it is possible to achieve a very flat gain over up to two octaves. In fact each stage can compensate the gain ripple of each other when designed properly. On the down side, stability is critical issue whenever a loop in between the input and the output is created. In fact, if the feedback signal comes back in phase with the input signal and with some gain, then the Barkhausen condition is fulfilled and the system is going to enter in self oscillation.

2.4.4.3 Traveling wave amplifiers

The principle of a traveling wave amplifier (TWA) is nothing like the architectures presented before. Instead of trying to compensate or remove the input and output capacitances of active networks, the approach consists in using them to transmit or carry the signal from the input to the output. A TWA can be considered as two lines (an input one and an output one) actively coupled by cells distributed over these two lines. Fig 2.25 is representation of a conventional TWA. The input line is made of the Lg/2 and Lg elements while the output one is made of Ld/2 and Ld elements. Cells 1 to N are the active coupling elements, most of the time they are either based on common source transistors or cascode structures. The combination of the parasitic elements of the active cells together with the line segments permit to realize bandpass transmission lines over a very wide frequency band.

The more cells there are, the higher the gain of the amplifier is going to be and the smaller the bandwidth is going to be. In fact the more cells there

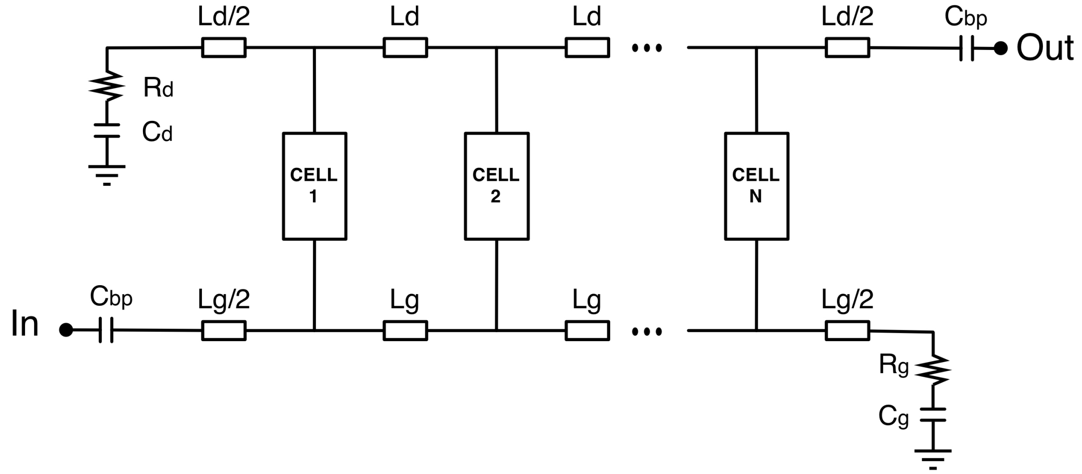

Figure 2.25: Traveling wave amplifier -

are, the more line segments are needed to connect each line and the more parasitics there are from the cells which results in lower frequency cut off for the access lines and thus for the overall TWA. Moreover, parallelizing to many cells is useless because at the some point more losses are introduced by the access lines than the gain increase with each added cell. TWA have typically behave well in terms of stability due to their quite low gain and the good isolation obtained thanks to transmission lines. On the down side, TWAs take a large area when implemented as MMICs compared to reactively matched or feedback structures. Indeed, the number of cells is typically quite important (around 10) and the transmission lines have important length.

Very good gain flatness over a wide frequency range can be achieved with TWAs thanks to resistive load placed at the end of each line to match the lines impedance. Even though, it is a very though topology to optimize and it has a limited gain, the traveling wave approach is definitely the one of choice when bandwidths over a decade are targeted. While TWA have traditionally been used to optimize gain flatness and bandwidth, a methodology to maximize output power and efficiency is introduced in (1).

Table 2.5 summarizes advantages and disadvantages of each wideband struc-

tures presented in this chapter. When large bandwidths are required and when die area is not an issue, the TWA approach appears to be the one of choice while reactively matched and feedback structures should be privileged when bandwidth around one or two octave with die size constraints are targeted.

Topology	**Bandwidth**	**Gain**	**Gain flatness**	**Stability**	**Size**
Reactively matched	+	++	+	++	+++
Feedback	+	++	++	+	+++
TWA	+++	+	+++	+++	+

Table 2.5: Wideband amplifiers comparison

2.5 State of art

GaN MMIC is still an emerging and recent technology. Even though founders propose lots of stand-alone (whether packaged or not) transistors to realize hybrid amplifiers, access to fully integrated process with both active and passive components remains quite restricted because most of technologies are still under development or in qualification phase up to now. However, several very interesting integrated realization have been reported in the literature. In this part, only fully integrated HPA realizations dedicated to military applications are presented, which implies high output power and wideband characteristics (basically from C-band to Ku-band) with a special focus on X-band amplifiers. While GaN based circuits are the ones that draw the main attention in here, some outstanding results in GaAs and SiGe will be depicted too.

2.5.1 X-band

In the following the most interesting architectures and the HPA with the best performances are listed and depicted:

A compact two stages current combined GaN HPA: This amplifier (Fig 2.26) (2) is based on a classical architecture. Indeed, it is a two

stages amplifiers based on common-source topologies. The first stage is made of two transistors while the output power stage is made of four. The power combination is made with current based combiners which have the advantage of exhibiting very low losses so great results can be achieved in terms of both output power and efficiency at the cost of die size, these kind of combiners taking a large area on the chip. This circuit was realized with 0.25μm AIGaN/GaN HEMT from Fujitsu. From 9GHz to 12 GHz it exhibits a small signal of 24dB, an output power between 39.5dBm (8.9W) and 41.7dBm (14.8W). In the same frequency range, the efficiency goes from 38.6% to 51.1%. The possibility to apply a voltage supply up to 45V on this technology permit to achieve these kind of performances. The overall die size is equal to 7.2 mm^2

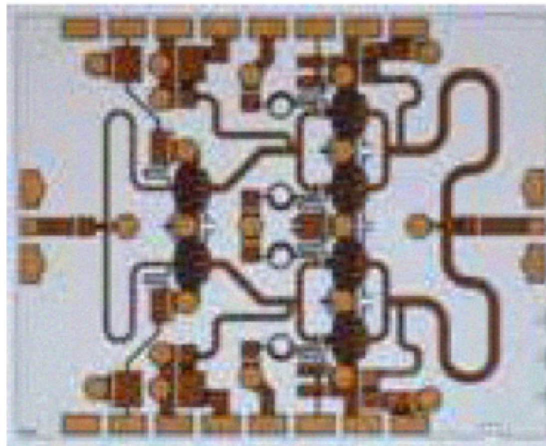

Figure 2.26: Compact two stages current combined GaN HPA -

. Although it is only a two-stages amplifier so it suffers from a quite low gain at high input power values, the performances of this HPA and its size make it very suitable for X-band military applications.

A 50W current combined GaN HPA: This realization (Fig 2.27) (3) has been done with the goal to maximize output power. Indeed, even if it is based on the same architecture as the previous circuit (two-stages amplifiers with common-source transistors) and current combiners, its gate width development of 8mm just for the power stage clearly means that it has been designed to maximize the output power. This circuit was realized

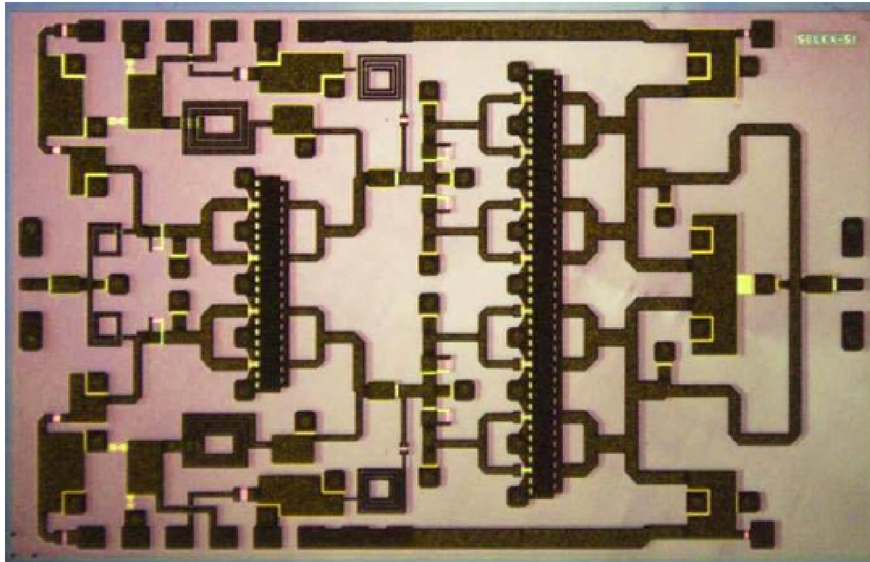

Figure 2.27: Compact two stages current combined GaN HPA -

with a 0.5μm from Selex Sistemi Integrati and occupies an area of 16mm^2, which way larger than the previous example but which makes sense when looking at the gate development.

This HPA exhibits more than 25W of output power with an associated gain greeter than 15dB and a PAE over 35% in the 8Ghz-10.5GHz frequency band under a power supply of 20V which represents normal operation. If the voltage supply is increased to 35V, the amplifier delivers more than 50W in the same frequency band with a peak output power of 58W around 9GHz. The associated gain is between 18dB and 20dB while the PAE is greater than 27%.

A 14W GaN HPA realized withUMS GH25 process: Even though based on the same topology as the previous example, this amplifier (Fig 2.28) (4) is of great interest because implemented in the same technology (UMS GH25) as the circuits realized in this thesis so it makes a very good comparison point for the work to be detailed later in this manuscript. A special attention has been made in this design in order to get the intrinsic parameters of active devices in order to match it as well as possible.

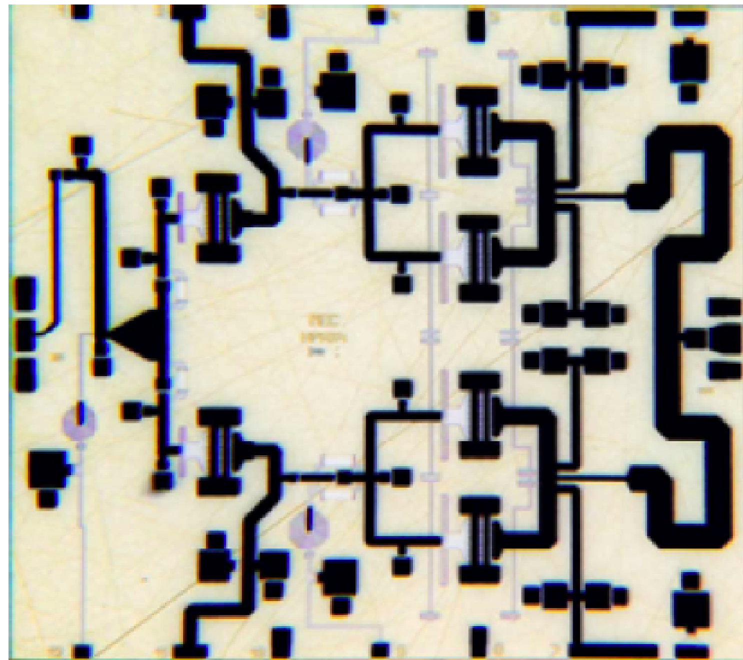

Figure 2.28: A 14W GaN HPA realized withUMS GH25 process -

With a total gate width development of 4mm for the output power stage, this amplifier is able to deliver 14W of output power from 8.8GHz to 10.4GHz with an efficiency between 38 and 44% in the band. The small signal gain is around 25dB and the overall die size is 18mm^2. Compared to the other circuits, this one is never supplied with more than 26V, making it behave well in terms of reliability and longevity.

These three amplifiers are used under pulsed operation mode with different pulse conditions (pulse width and duty cycle), this helps increasing performances because active devices do not heat as much as in continuous wave

operation mode and thus their performances are not degraded at all.

In X-band, where output power and efficiency are the key specifications, the current combining approach is chosen in nearly all realizations that can be found in the literature.

Ref	Freq (GHz)	Output power (W)	Linear Gain (dB)	PAE (%)	Supply Voltage (V)	Size mm^2
(2)	9-12	12	24	45	45	7.2
(3)	8-10.5	25	15	41	20	16
(4)	8.8-10.4	14	24	38	26	18
(5)	8.8-11.5	14	18	31	30	12
(6)	8.5-10.5	27	18	30	35	18

Table 2.6: X-band high power amplifiers state of art

Table 2.6 summarizes the best results achieved in X-band for GaN MMIC high power amplifiers over the past few years. Much more power can be obtained (more than 100W) with hybrid solutions but this not the interest of this work. Indeed, such an amount of power and thus heat can not be dissipated in a small size MMIC chip. That's why up to know it is not realistic to imagine fully integrated solutions that can deliver more than 50W in X-band.

2.5.2 Wideband : C-band to Ku-band amplifiers

The frequency range of interest when talking about wideband amplifiers for military applications is mainly from C-band to Ku-band. Several architectures allow to reach this kind of bandwidths, each having their advantages and disadvantages. For example, traveling wave amplifiers are the best in terms bandwidth capability but they can neither deliver as much output power or achieve as good efficiencies as current combined amplifiers and moreover TWAs typically occupies a larger die area. In the following, a few relevant designs that can be found in the literature are depicted:

A C-Ku band 20W reactively matched GaN amplifier: This solution (Fig 2.29) (7) is based on reactively matched topology as for the X-band

designs which permits to deliver an higher output power (20W) all over the band but this is at the cost of gain flatness. With this approach the key component which is going to determine the performances in terms of bandwidth and efficiency is definitely the output power combiner. This one is classical current combiner.

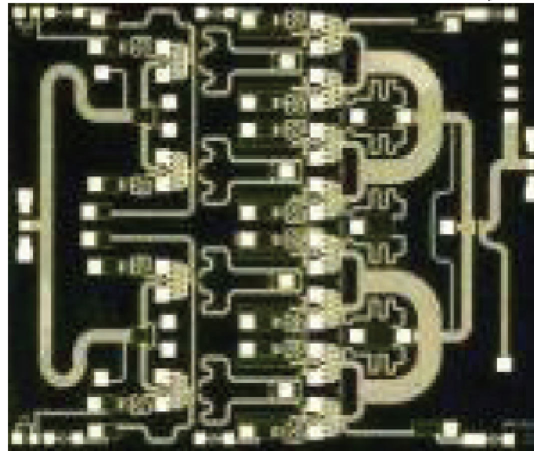

Figure 2.29: C-Ku band 20W reactively matched GaN amplifier -

To achieve a relative bandwidth over 100%, capacitors are added in parallel to the combiner at specific locations to create resonances and thus increase bandwidth. Shorted stubs are present too in parallel to the output line to compensate for parasitic capacitances and help match the output to 50Ω. This amplifier realized with a Mitsubishi GaN process occupies an area of 20mm^2, it delivers an average of 20W from 6 to 18GHz with an average efficiency of 15%. This amplifier was clearly designed to maximize output power and not efficiency but the power density achieved (1W/mm^2) is a quite high value for a wideband amplifier.

A 14W 2-18 GHz GaN Non-uniform Distributed Power Amplifier: A distributed architecture from Triquint is presented here (Fig 2.30) (8). This is clearly the solution of choice to achieve greater bandwidths together with flat response in terms of both gain and output power. Indeed there is no other structure that can compete with the distributed one in terms of bandwidth. On the down side, these amplifiers typically exhibit less gain than reactively matched ones and are tougher to design and optimize too.

To increase output power performances, a non uniform topology was picked, it means that the output transmission is getting wider as getting closer to the RF output. This is done to compensate and match the impedance decrease that happens when getting closer the output. The last transistors have a gate width greater than the first one to help improving output power too.

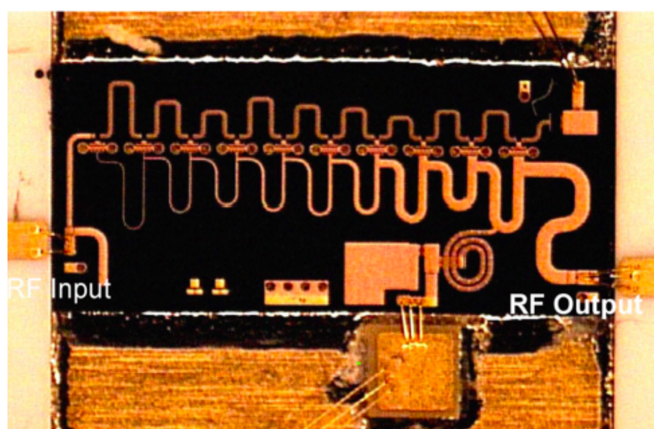

Figure 2.30: 14W 2-18 GHz GaN Non-uniform Distributed Power Amplifier -

In the 2GHz to 18GHz frequency band, this realization exhibits an average of 14W with an average efficiency of 28% under a 35V bias voltage. These are very impressive values over such a bandwidth, especially with a gain flatness lower than 2dB. A peak output power of 18W can be achieved if increasing the bias voltage up to 40V, but it results in bandwidth and efficiency decrease.

A decade bandwidth 2 to 20GHz GaN differential distributed power amplifier: This is an example of an other wideband distributed amplifier (Fig 2.31) (9). The specificity of this design was the choice of a low size transistor (gate width = 200μm) for the unit power cell in order to achieve high frequencies operation. However the small gate width reduces the power capabilities of the amplifier. So to compensate for that, a differential architecture was used. It consists in the parallelization of two unitary distributed amplifiers, which are combined using a wideband current combiner, the output power is increase by 3dB minus the combiner

losses.

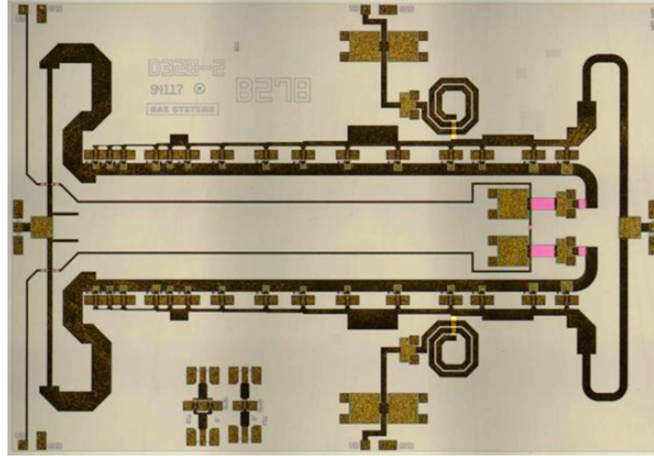

Figure 2.31: Decade bandwidth 2 to 20GHz GaN differential distributed power amplifier -

Even though this structure is quite area consuming (die size is 38.2mm^2), it exhibits very interesting performances. Indeed form 2 to 20GHz, this amplifiers averages 16W of output power together with 26% of PAE. It works under a 30V supply voltage and its small signal gain is 12dB in average. By combining both the advantages of both a distributed structure and a differential one, this design is definitively a reference for wideband HPA not only in terms of performances but for its architecture too.

In Table 2.7, the best results in terms of wideband HPA are summarizes. Distributed topology is picked most of the time but some good results can be achieved too with a more classical reactively matched amplifier.

Ref	Freq (GHz)	Output power (W)	Linear Gain (dB)	PAE (%)	Supply Voltage (V)	Size mm^2
(7)	6-18	20	16	15	35	19.2
(8)	2-18	14	NA	28	35	NA
(9)	2-20	16	12	26	30	38,25
(10)	6-18	9	18	31	40	18.7
(11)	6-18	9	20	20	25	18

Table 2.7: Wideband high power amplifiers state of art

Even though access to GaN integrated technologies remains quite limited because it is a very recent and thus still under development, quite a few realizations of high power amplifiers GaN MMICs can be found in the literature as exposed earlier whether talking about X-band circuits or wideband ones. A great amount of work has been done to maximize the output power and achieve very high efficiencies, for example 25W of output power with more than 40% of PAE have been reached in X-band on an MMIC, results far from imaginable before GaN outbreak. On the downside, these circuits with very high performances are quite big in terms of die area. Indeed, wide gate width development is needed to achieve high power which makes active devices bigger and more importantly low loss combiners are required to achieve high efficiencies. And these combiners can be very large, sometimes about half the size of the overall amplifier.

2.6 Thesis contribution

In this thesis, a special focus was made on the development of both small size and compact power combiners in order to reduce die size area without efficiency degradation. The main idea consists in transferring techniques and architecture used by Silicon designers to GaN MMIC, especially the fact of stacking elements which is often done in Silicon but does not appear possible in GaN at first sight. Indeed, there is only one metal layer available to designers in GaN and obviously two layers are required to stack elements. Once this difficulty overcome, stacked combiners such as baluns and couplers can be realized. Chapter 2 depicts the realization and the design methodology to implement these combiners and in Chapter 3, high power amplifiers based on these kind of combiners are presented.

Another aspect explored in this work is the reconfigurability and multi-modes topic. In fact, some military applications can take advantage from a multimodes high power amplifier. The reconfigurability can be envisaged both in terms of delivered power and bandwidth. For example, it can be interesting to realize a wideband medium power amplifier for electronic warfare purposes that can be in reconfigured into an high power X-band HPA for radar matters. Not only it is about amplifier design but some higher level system aspects are taken in consideration in such a circuit.

3

Power Combining

In the previous chapter, the major impact of power combiners in an HPA performances has been pointed out. Indeed due their strategic placement at the output of power stages, their losses directly reflect on the amplifier output power and efficiency. Moreover, the size of a classical power combiner is quite important (basically the largest block of the entire amplifier), so when looking for more compacts amplifiers, size reduction of the power combiner is definitely the best way to go. The ultimate objective is then to design a low loss and compact combiner at the same time, but of course these two objectives are contradictory. At least, they are contradictory when considering classical structures such as the Wilkinson based current combiner for example which exhibits very low losses but which occupies a very large area.

An innovative way to implement power combiners is presented in this chapter, it is based on the principle of stacking elements vertically instead of putting them side by side and playing with their geometry to reduce their size as much as possible. This chapter starts with some theoretical considerations on the main power combiners that can be found in the literature and goes on by depicting the stacking principle developed in this thesis before concluding with some combiner realizations.

3.1 Theory on combiners for power amplifiers

A classical combiner only performs a symmetrical power summation. Indeed it has multiple inputs and one output and ideally the power obtained on the output terminal is the sum of the power received at each input port. The most basic combiners would only behave correctly if the power injected at each input is the exact same, otherwise asymmetries are going to appear and the power summation is not going to be what it was supposed to be. Moreover, Even though, there are a drastic amount of different combiners, they can all be classified in two main families which are the current based combiners and the voltage based ones, some others being a combination of booths. They all present advantages and disadvantages. For example current combiners exhibit very low insertion loss so they are the component of choices when targeting high efficiency amplifiers but this at the cost of die area because these combiners take a large space to be implemented. In the following , each kind of combiner is depicted from a theoretical point of view and some examples are presented.

To evaluate the characteristics and the performances of the different combiner kinds, the following parameters have to be taken into consideration:

* **Bandwidth**: Defines the frequency range over which the device acts as a combiner. It can be specified in terms of insertion loss and/or phase difference between the paths. While the 3dB attenuation is a convention to determine amplifiers bandwidth, it makes more sense to take a 1dB limit for combiners because they are totally useless when having such important losses.
* **Insertion loss**: The amount of signal lost through the combiner when the power summation is performed. For example, if summing two signals with an energy of 20dBm each through a combiner with 1dB insertion loss then the power available at the output would be equal to 22dBm.

* **Isolation**: The amount of undesired power that goes from one input to another input instead of going to the output. A value of -20dB is often considered as a minimum for a combiner to perform well.
* **Mismatch**: Characterizes both the differences between the input terminals in terms of insertion loss and relative phase to the output. To guarantee an optimal behavior of the overall amplifier, both mismatch should be minimized as much as possible or asymmetries would appear resulting in efficiency loss and active devices self heating.
* **Transformation ratio**: Some kinds of combiners can have a different characteristic impedance at the input and the output side. For example, a transformation ratio of 2 means that the input impedance (ate each terminal) is the double than the output one.

With these basics consideration in mind, each kind of combiner can now be detailed more precisely.

3.1.1 Current combiners

Current summation based combiners are probably the most classical architecture and the most straight forward to design.The first combiner of this kind was introduced in 1960 by Ernest Wilkinson in (12), it is usually called a Wilkinson combiner (or splitter). An ideal Wilkinson combiner combines two (or more) signals with an equal phase into one signal in opposition of phase with the inputs ones. It uses two quarter-wavelength transformers to match the split ports to the common port, as shown in Fig 3.1 .

A lossless reciprocal passive three-port junction cannot be matched at all ports simultaneously so a resistor is introduced to match the ports and to improve the isolation of the output ports. Theoretically the resistor does not dissipate any power since ports 2 and 3 are in phase and thus the is no voltage difference between these two ports at nay time, so the Wilkinson power combiner is lossless, but in practice there are some low losses. As it based on quarter wavelength transmission lines, the size of the combiner is directly related to its center frequency and it can get very massive at

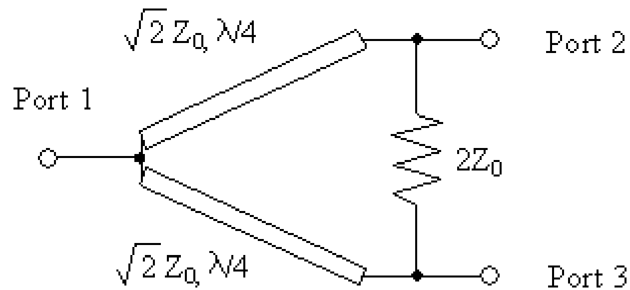

Figure 3.1: A 2-way Wilkinson combiner -

low frequencies. To resolve this issue, it is possible to implement such a combiner with lumped components instead of transmission lines. Indeed, a pi-network made of a serial inductor and two parallel capacitors can behave exactly the same a transmission line. An example of a lumped Wilkinson combiner is presented in Fig 3.2.

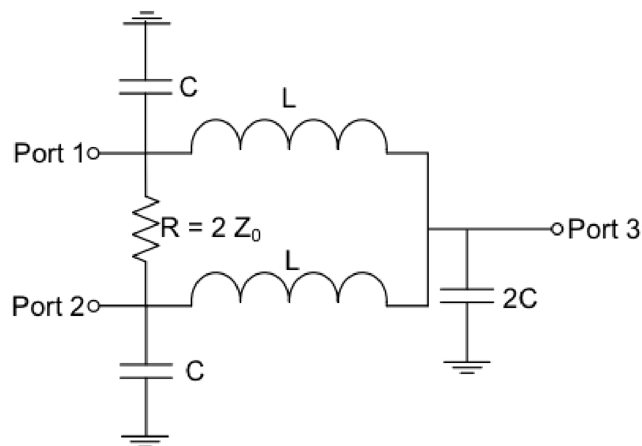

Figure 3.2: A 2-way lumped Wilkinson combiner -

Wilkinson combiners can be implemented as well in single side printed circuit boards as in integrated circuits. They can theoretically have as many inputs as wanted by duplicating the initial structure, they can also be thrown of balance so more power is taken from some inputs than other. This obtained by modifying the transmission lines geometries and changing the resistor value. Conventional Wilkinson combiners do not excel in terms

of bandwidth but by implementing a multi-stages combiner it is possible to achieve over decade bandwidths. A multi-stages Wilkinson combiner is basically obtained by cascading several unitary combiners, an example of 3 stages 16 ways combiner working at 19GHz from the German Space Agency is presented in Fig 3.3. On the downside, this extra bandwidth is obtained at the cost of insertion loss which increase at each time a stage is added. Indeed, the signal as to go through each transmission line stage and thus losses increase.

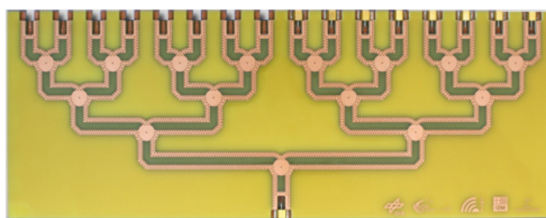

Figure 3.3: A 19GHz, 3 stages 16 way Wilkinson combiner from the German Space Agency -

Wilkinson combiners perform great in terms of insertion loss (losses around 0.1dB are easily achieved in X-band) and are pretty easy to design but they suffer from their very important size and their quite limited bandwidth. When designing combiners for power amplifiers, an other aspect to take into consideration is impedance matching, the goal being to match the power amplifier output to the overall output which is typically 50Ohms. A derivative of a traditional Wilkinson combiner is often used to do so. It consists in adding parallel capacitors and/or stubs at specific locations on the wilkinson combiner transmission lines to obtain the desired impedance at both ends of the combiner.

Fig 3.4 is an example from UMS of and high power amplifier output stage using a modified 2 stages Wilkinson combiner as a power combiner. The shape of the Wilkinson combiner is easy to spot on the picture and parallel capacitors and stubs can be seen too. Moreover one of the stub can be used to feed the power supply to the active devices.

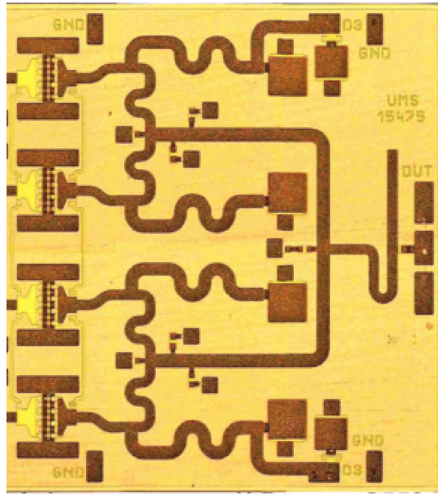

Figure 3.4: HPA output stage using a transformed Wilkinson combiner -

3.1.2 Transformers

A transformer is constituted by the combination of two magnetically coupled inductors, one being called the primary and the other one the secondary. Such coupling results from the fact that a portion of the magnetic flux generated by a time-varying primary current also crosses the secondary inductor. This coupling is expressed in terms of a mutual inductance. Inductances are defined as the ratio between magnetic flux and electric current.

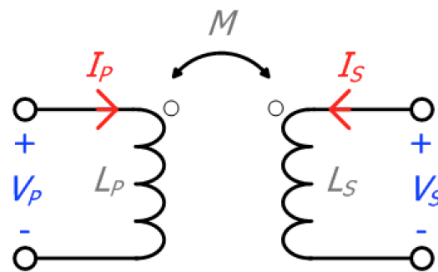

Figure 3.5: Transformer representation -

Considering Fig 3.5 where primary and secondary are represented, if a current is applied to the primary, and the secondary terminals is left open, so i_s=0. Then the primary voltage will not be affected by the secondary and will only depend on its self inductance L_P and the time variation rate of

the current flowing through the primary, as described in Eq 3.1:

$$v_p = L_p.\frac{di_p}{dt}$$

(3.1)

Moreover, this primary current variation will induce a voltage in the secondary, which will be proportional to the mutual inductance M as expressed in Eq 3.2:

$$v_s = M.\frac{di_p}{dt}$$

(3.2)

Now, if current is applied to both windings simultaneously and considering the fact that the mutual inductance phenomenon is symmetrical in both directions then the voltage-current relations for each winding can be expressed by Eq 3.3 and Eq 3.4:

$$v_p = L_p.\frac{di_p}{dt} + M.\frac{di_s}{dt}$$

(3.3)

$$v_s = L_s.\frac{di_s}{dt} + M.\frac{di_p}{dt}$$

(3.4)If considering a sinusoidal excitation, the voltage current relations can be expressed in complex notation such as in Eq 3.5 Eq 3.6:

$$V_p = j\omega L_p.I_p + j\omega M.I_s$$

(3.5)

$$V_s = j\omega L_s.I_s + j\omega M.I_p$$

(3.6)

When considering ideal lossless transformers together with the fact that the primary and the secondary have identical electrical powers, we can deduce

from the above relations that transformers have a constant impedance ratio. This ratio is often linked to the inductance value of each winding as described in Eq 3.7:

$$N = \frac{V_p}{V_s} = \sqrt{\frac{L_p}{L_s}}$$

(3.7)

In practical, it means that a load connected to the secondary would be seen in the primary side as the same load multiplied by N^2. There is a tremendous advantage resulting from this property, indeed as mentioned earlier, the ultimate objective is to use a device that can perform the power combination and the impedance matching at the same time. By playing with the impedance transformation ratio of the transformer this becomes possible.

Transformers are way harder to design than current combiners depicted in the previous section. Not only, they are various topologies possible but they are some key parameters to size properly too. One way to extract these parameters is by considering the transformer as 2-ports device instead of a 4-ports one, this done by grounding one terminal on both the primary and the secondary winding as show in Fig 3.6.

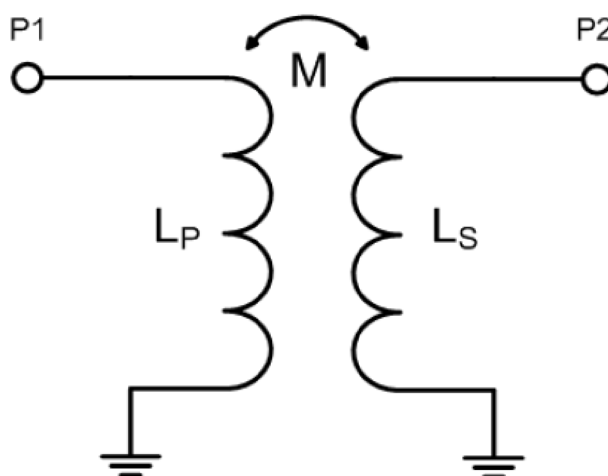

Figure 3.6: Transformer in 2-ports configuration -

The parameters extracted from this 2-ports configuration are frequency dependent for most of them, they are obtained from Z-parameters which can be obtained after a mathematical transformation from an S-parameters analysis. First thing to look is obviously the inductance value of each winding, they are defined by Eq 3.8 and Eq 3.9 for the primary and the secondary:

$$L_p = \frac{\Im(Z_{11})}{\omega}$$

(3.8)

$$L_s = \frac{\Im(Z_{22})}{\omega}$$

(3.9)

The inductance ratio n_L is defined as :

$$n_L = \frac{L_s}{L_p}$$

(3.10)

The mutual inductance M relates the fact that a current change in one winding will directly generate a voltage change in the other winding, it is defined by:

$$M = \frac{\Im(Z_{21})}{\omega}$$

(3.11)

The coupling strength between the windings is expressed by the coupling factor k. A value of 0 refers to an absence of coupling while a value of 1 represents a perfect coupling, meaning a full transfer of energy from one winding to the other. This factor is defined by:

$$k = \frac{M}{\sqrt{L_p.L_s}}$$

(3.12)

There are a number of different definitions usually employed to evaluate the quality-factor of inductors. Its fundamental definition relates to the ratio between stored and dissipated energies by the passive component in an oscillation cycle. An integrated inductor stores magnetic energy by nature, but also presents parasitic capacitances which will be responsible for some electric energy storage. Therefore, since an inductive behavior is sought in an integrated transformer, the stored energy which is considered is the difference between the peak magnetic and electric energies. Then this quality factor can be expressed as the ratio between imaginary and real parts of the corresponding impedances, as expressed in Eq 3.13 and Eq 3.14 respectively for the primary and the secondary:

$$Q_p = \frac{\Im(Z_{11})}{\Re(Z_{11})}$$

(3.13)

$$Q_s = \frac{\Im(Z_{22})}{\Re(Z_{22})}$$

(3.14)

Another fundamental property of transformers is its insertion loss, especially for power combiner application. However, these losses are highly dependent on the impedances presented to each terminal of the transformer. Most of the time, the balun would be designed to be matched to the optimal impedances of the amplifiers to be combined so it does not make sense to evaluate the losses on 50Ohms. The equation 3.15 is a computation of the minimal insertion loss as if the balun were seeing its optimal impedances, this is most valuable way to compare several transformers in terms of loss.

$$IL_m = \frac{1}{1 + 2.(x - \sqrt{x^2 + x})}$$

with

$$x = \frac{\Re(Z_{11}).\Re(Z_{22}) - [\Re(Z_{12})]^2}{[\Im(Z_{12})]^2 + [\Re(Z_{12})]^2}$$

(3.15)

After these general considerations on transformer theory, let's now focus on the specifies for use as power combiners. When used as a power combiner or splitter, an inductance based transformer is often called a balun which stands for balanced/unbalanced. Fig 3.7 is an example of differential amplifier using baluns for both power splitting and combining. On the input, the signal is injected in one terminal of the primary winding while the second terminal can either be grounded or left open (Marchand configuration). The Marchand approach is detailed in (13). This results in the secondary in two signals (on at each terminal) in opposition of phase with the same power level (half of the power inputed in the primary for each, considering the transformer lossless). Then, the signal is amplified in each amplifier and is combined back through an other balun which works inversely than the first one. Indeed it receives two signals in opposition of phase and combine them in a single signal with a power level equal to the sum of the inputed signals. To work properly, the two signals inputed to the output balun should have the same power level, which means that the two amplifiers have to be the same and work in similar conditions.

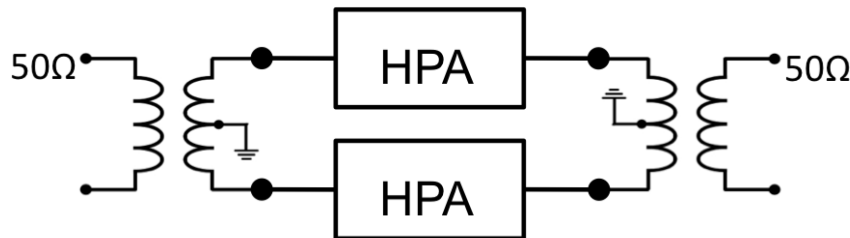

Figure 3.7: Stacked transformer (left) and planar transformer (right) -

There are two main topologies to implement such baluns in integrated circuits, either planar or stacked. On a planar approach, both windings are located in the same metal layer and one is imbricated into the other and the coupling surface corresponds to the sides of the windings that face each other. When considering the vertical approach, one winding is stacked on the top of the one, so they are implemented in different layers, layers close to each other to increase the coupling. The coupling is obtained through

the surfaces of the windings that face each other. In practical, the energy transferred through vertical coupling is greater than through horizontal one, simply because the surface face to face is greater than when the windings are side by side. In Fig 3.8, a comparison between the stacked topology and the vertical one is presented. Moroever, by stacking the windings and thus using the vertical dimension, the planar occupation of the balun can be reduced, which results in a more compact design.

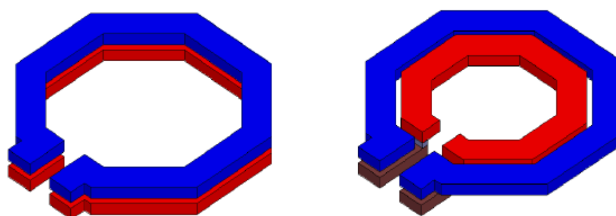

Figure 3.8: Power amplifiers combined with baluns -

While, it is a common thing to implement stacked baluns in silicon based technologies ((14)) because they offer multiple metal layers to designers, it has not been done yet in an MMIC process. Indeed, a classical MMIC process has a single metal routing layer so it is not possible to stack elements on top of each other. However, in the following of this chapter, a solution to the issue is proposed.

3.1.3 Couplers

The last principal family of devices that can be used as power combiners depicted in this chapter are couplers. While current based combiners perform the combination with keeping all signals in phase and balun transformers perform this task by putting signals in opposition of phase, couplers basically perform combination with signal in quadrature (that is to say 90°difference between signals) or in opposition of phase. Couplers are typically four ports devices and are based on the principle that when two lines are close enough to each other, energy transfer happens from one line to the other one, this transfer phenomenon is called the coupling effect.

They can be implemented as easily in integrated circuits or in printed circuit boards. A coupler can be represented as shown in Fig 3.9 with the according terminals name.

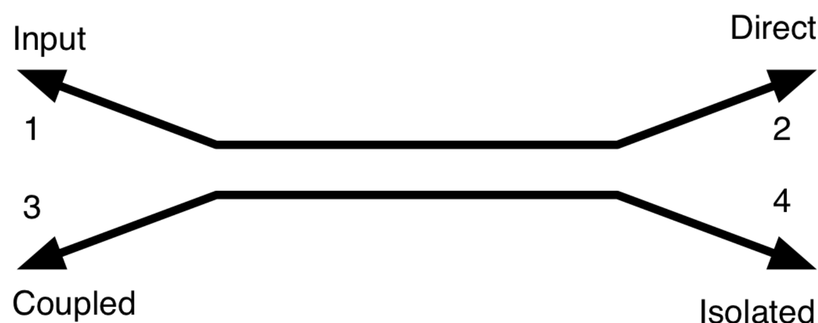

Figure 3.9: Typical coupler representation and ports name -

When a signal is injected into the input port (port 1), most of it is redirected to the direct port (number 2) and a fraction of it goes to the coupled port (number 3) thanks to the coupled effect, to ensure this behavior it is mandatory that the isolated port (number 4) is terminated by a load with an impedance equal to the overall device characteristic impedance, so no power at all flows through that port. At first coupler were introduced for measurement matters. Indeed, the coupler was inserted into a system between its ports 1 and 2 and a very small fraction of the signal was coupled through port 3 where a measurement device was connected to estimate the power level actually injected into the overall system. For example, a 20 dB coupler was transmitting to port 3, a signal 20 dB lower than what injected into port 1, so only 1% of the power was deviated from its original path and 99% were actually transmitted into the system. Only thing left to do, was to multiply by 99 the amount measured at port 3 to know the amount injected into port 2.

Three fundamental parameters permit to characterize properly a coupler. The first one is the coupling factor C, it relates the amount of power coming from the input port that goes to the coupled port instead of the direct output. It is simply expressed as the ratio of power coming in port 1 (P_1)

divided by the amount of power coming out of port 3 (P_3) as shown in equation 3.16:

$$C(dB) = 10log\frac{P_1}{P_3} = -20log|S_{13}|$$

(3.16)

If the coupler was ideal and lossless, no power at all would be flowing through the isolated port number 4. Of course, this is not the case in practical and a small amount of power is going through this isolated port. That amount is known as the isolation I and is expressed in equation 3.17.

$$I(dB) = 10log\frac{P_1}{P_4} = -20log|S_{14}|$$

(3.17)

Last fundamental parameter is the directivity D, it expresses the coupler ability to transfer power from the input port to the coupled port while rejecting the power coming from the through port that comes from reflections on this port. D can be expressed as follow:

$$D(dB) = 10log\frac{P_3}{P_4} = -20log\frac{|S_{31}|}{|S_{14}|}$$

(3.18)

WIth simple mathematics, these three parameters can be linked as shown in equation 3.19:

$$I(dB) = C(dB) + D(dB)$$

(3.19)

There is one more parameter to take into account when considering couplers, which is insertion loss between then input port and the direct port. Theoretically, for the case of an ideal coupler, these losses all come from the coupling effect and the fact the some of the input power is deviated through the coupled port. However, with real couplers some other effects such as

conductor or dielectric loss and unsuitable matching contribute to the insertion loss too. These insertion loss can be expressed as in equation 3.20:

$$IL(dB) = 10log\frac{P_2}{P_1} = -20log(S_{21})$$

(3.20)

As said previously, if neglecting parasitic losses, the insertion loss are directly related to coupling. Indeed a high coupling factor would result in low insertion loss because only a few amount of power is redirected to the coupled port and most of it is flowing through the direct port. Table 3.1 presents the insertion loss for various coupling values.

Coupling (dB)	**Insertion loss (dB)**
3	3
6	1.25
10	0.458
20	0.0436
30	0.00435

Table 3.1: Coupling factor vs. insertion loss

When used as a measurement tool, an high coupling value would be chosen as mentioned earlier. On the contrary, for our application of interest (power combining) a coupling value of 3dB should be picked.

Indeed, for 3dB coupling, the insertion loss are equal to 3dB too, meaning that the same amount of power is coming out the direct port and the isolated one, thus a symmetrical power divider (or combiner) with signals in quadrature is obtained. By using one coupler as a power splitter and one other as a power combiner, a differential HPA can be implemented as it is done in (10). This example is illustrated in Fig 3.10 which is a picture of the realized HPA which in fact is the combination of differential amplifiers combined with couplers.

A particular kind of couplers are of great interest for power combiners matters due to their low loss and bandwidth abilities, they are called Lange

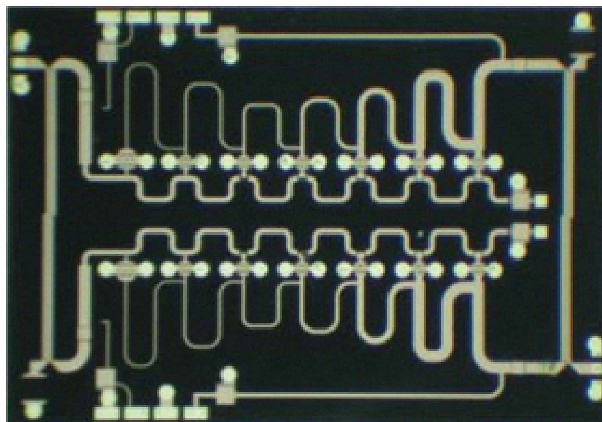

Figure 3.10: Example of an HPA using couplers for power splitting/combining -

couplers, due to the name of their inventor. As shown in Fig 3.11, a Lange coupler has the same ports as a traditional one. The one represented here is called a four-strips coupler because it is made of four main transmission lines, but some other variants such as six or eight strips are commonly found too. The different strips are connected together at specific points by wirebonding (or upper metal levels for IC realizations) in order to increase coupling and ensure DC continuity.

The conductor length L is set by the desired center frequency of operation, basically this length is equal to a quarter wavelength of the central frequency. The width and spacing parameters (W, S) should be tuned to obtain the desired coupling ratio and the impedances at each terminal. Even though, pretty accurate models are available in CAD softwares, electromagnetic simulations are mandatory to design a valuable Lange coupler. Fig 3.12 is an example of a Lange couple realized on alumin substrate and working around 2GHz.

On the following, we will focus on the combiners realizes in the frame of this work, which are baluns and Lange couplers. These two topologies have been picked in order to achieve size reduction of the devices and low insertion loss. Based on existing architectures, a new way of implementation for MMIC is proposed and detailed in the next sections.

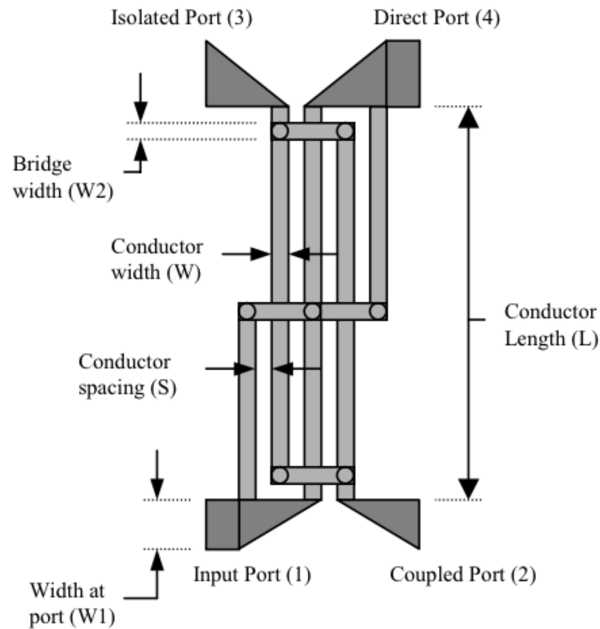

Figure 3.11: Representation of a Lange coupler and port denomination -

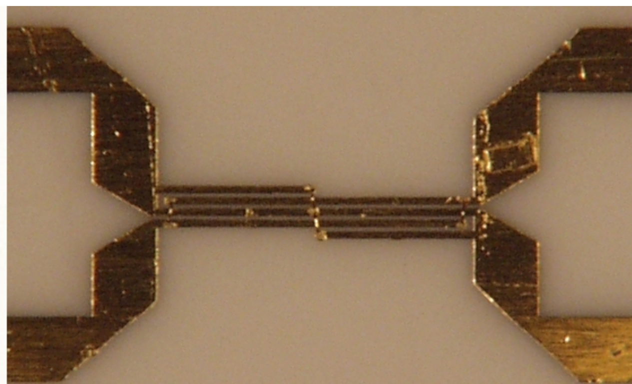

Figure 3.12: Lange coupler on alumina substrate -

3.2 Vertical coupling and elements stacking

While stacked structures are often used for combiners in silicon based designs, they do not exist in MMIC based technologies. Indeed, a classical MMIC process offers only one metal layer for routing and it is pretty obvious that to stack elements of any kind two layers at least are required.Two main advantages directly result from the fact of implementing stacked structures,

one being the size reduction and the other one the insertion loss reduction. Size reduction implicitly comes from the fact that instead of placing components on a two-dimensions environment, some are placed on top of each other using the verticality and thus the planar area is reduced and the integration is increased. Moreover, the stacked approach results in the creation of vertical coupling between the two elements being stacked, and this vertically coupling is typically higher when compared to the planar coupling. Higher coupling factor results in a greater amount of energy transferred and thus lower insertion losses in the overall structure.

In the following, an innovative approach to make possible the realization of stacked structures is presented from both a mechanical and an electrical point of view.

3.2.1 Mechanical aspects

Even though GaN or GaAs based integrated technologies are very promising for the next future and open the door to some realizations not possible in any silicon based technologies, they suffer from the fact that they typically offer one metal routing layer for design. This aspect is critical not only because it drastically increase the size of circuits but also because it prevents from implementing stacked structures. However, to make possible the design of circuits in such a process, air-bridges have been introduced. In fact, thank to them it is possible to punctually go over a line implemented in the regular metal layer, so it is possible to cross two lines without any connections between them.

For confidentiality matters as the technology from UMS used to realize all of the work achieved in this thesis has not be publicly released yet, no information at all about geometries, physical properties and physical dimensions would be provided in the following. Anyway, the principles and techniques presented here are not technologically dependent and could be applied to any MMIC process.

A simplified MMIC layers stack is presented in Fig 3.13. The default metal routing layer is located at the bottom, on top of it is an oxide that can be

removed to make physical and electrical contact with layers above. On the contrary to make capacitor this oxide would be kept and the metal layer and pillar layer would act as electrodes.

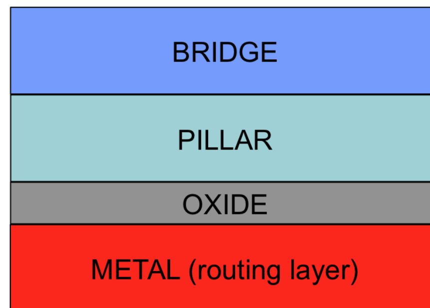

Figure 3.13: Simplified MMIC layers stack -

In Fig 3.14, an example of two lines crossing thanks to an air bridge is presented. As it can be seen on the picture, the principle is pretty easy. Indeed, one metal line punctually stops to go up to the air-bridge, then cross over the other line before going back down to the metal layer. The air-bridge represented in blue is both supported and connected to the metal layer by the help of pillars. As shown in the layers stack previously, the oxide has to be removed between the metal and the pillar to ensure continuity.

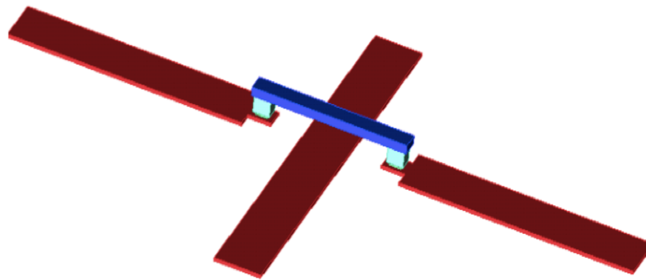

Figure 3.14: Two lines crossing thanks to an air-bridge -

The air-bridge length is constrained to a maximum to ensure it is not going to collapse on the metal layer it is going over. This limitation implies that the line going under the bridge is going to be limited in width, indeed its width has to be smaller than the air-bridge maximal length. Moreover, a small coupling effect would appear between the bridge and the metal layer.

Even though this effect is quite weak because the air-brige and the metal are separated by an air gap of a few μm, it should be considered when high power signals are going through the air-brdige or the line under it.

On a conventional use as just described, air-bridges are meant only to be punctual and used for line crossing. However, an other use of them can be foreseen with the aim to implement a second metal layer on top of the existing one. Indeed, if the pillar is not only punctual anymore but is deployed all over the default metal layer then stacking becomes possible. An idea of this kind has been patented in (15) but to our knowledge, there are no proof of realization in the available literature.

The principle proposed here is illustrated in Fig 3.15. It is based on the fact the layer dedicated to host air-bridges is actually made of metal material, so it is a good candidate to act as a metal layer.

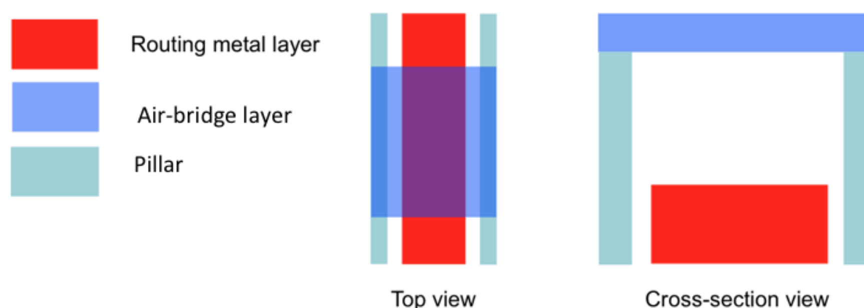

Figure 3.15: Airbridge used as a stacked layer -

As shown in the top view, the air-bridge is deployed all over the metal layer, it results in the superposition of two metal material which is what we require to implement stacked structures. There are no physical contact between the metal and the air-bridge to ensure each layer is electrically independent and would transfer energy to each other only by coupling effects. However, the oxide layer is removed so there is only free air between the two layers. Pillars distributed on the side of the metal layer to support the air-bridge layer. To make that realizable, the air-bridge layer has to overflow on each side (left and right) of the metal layer so pillars can be placed on the sides without making contact with the metal layer. Due to

process realizations constraints, the pillars can not be continuous all along the air-bridges, indeed openings have to be made regularly into the pillars line to make the oxide removal possible. Fig 3.16 represents the position of openings made in pillars from both a top and a side view. A compromise has to be made to ensure there are enough openings area to clean the oxide properly and that there is enough pillars area to support the air-bridge and prevent it from sinking.

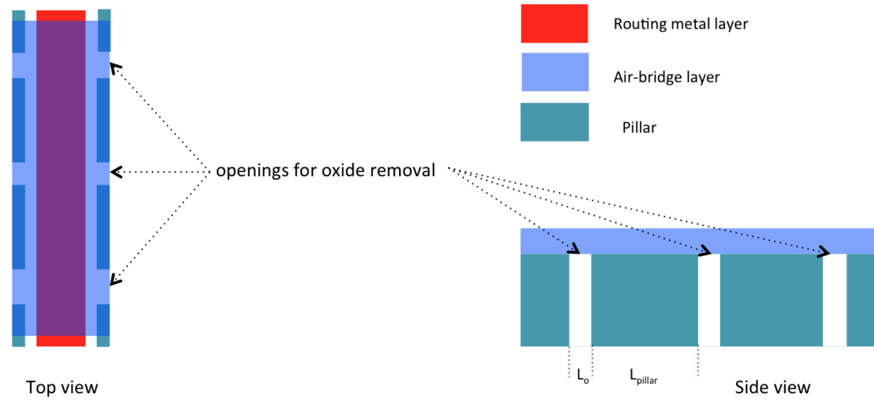

Figure 3.16: Openings in pillars for oxide removal -

Even though, as mentioned earlier no exact values can be given, according to UMS foundry a good compromise is to remove between 15% and 25% of any pillar segment and that should be done at regulars intervals as shown in Fig 3.16 and thus the following criteria:

$$5.6L_o \geq L_{pillar} \geq 3L_o$$

(3.21)

Designers have the freedom to tune values inside this range by performing EM simulations while guaranteeing both robustness to the structure and clean oxide removal. Besides that, the overall length of the air-bridge and the structure does not have any limits. On the contrary, the width of the air-bridge is still constrained (same constraint as the one related to a punctual air-bridge length explained earlier). This constraint is a limiting factor for both the air-bridge layer and the metal layer because that last one has to fit

within the pillars supporting the air-bridge layer. Restricting the maximal width directly results in limiting the overall current that can flow within the structure. These limitations in terms of width and current are proper to each founder and even to each technology but they should carefully be followed to ensure maximal reliability and robustness.

If these two constraints are fulfilled (openings in pillars and maximal width), then pretty much any shape can be realized, it is not mandatory to design only straight lines. Fig 3.17 describes the possibility to make shapes such as a U-turn for example, top view and 3D bottom view are presented for more clarity.

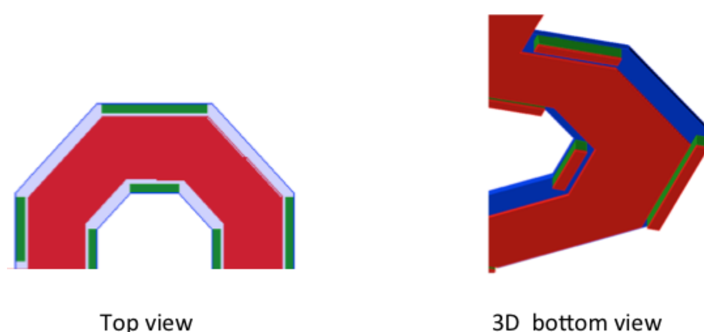

Figure 3.17: Example of a possible shape realizable, top view -

In this section, the possibility of implementing a stacked structure in an MMIC process has been exposed by creating a second layer with the helps of conventional air-bridges, in the following section a focus on the electrical properties and advantages that this kind of structures bring is going to be detailed.

3.2.2 Electrical aspects

Coupling between two elements whether they are transmission lines or other elements, is introduced by their proximity to each other and is directly related to the area that two elements have facing. This coupling can be either unwanted as cross talking in printed circuit boards for example or it can be voluntary to perform energy transfer as in couplers or balun transformers.

Not only stacked structures are very interesting in terms size reduction and compactness but they also open the door to the vertical coupling instead of only planar coupling. The difference between vertical and planar coupling is illustrated in Fig 3.18 for two transmission lines. While planar coupling happens through the thickness of the lines, vertical one occurs through their width, and typically the width of a line is way greater than its thickness.

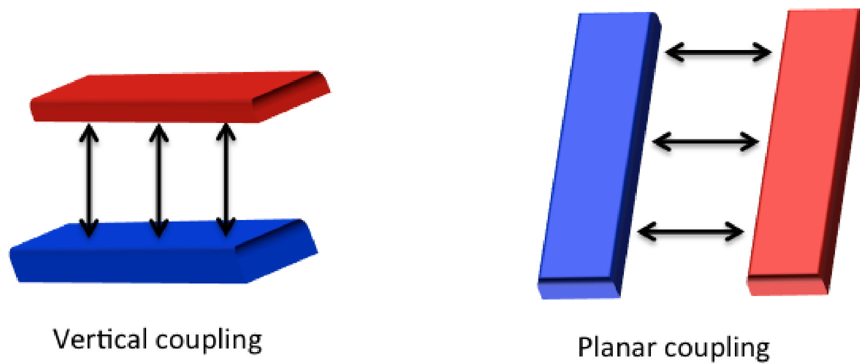

Figure 3.18: Illustration of vertical (left) and planar (right) coupling -

Indeed, the thickness of a metal line in a conventional MMIC process is of a few μm while the width of a 50Ω line is around 100μm at 10GHz. So it appears obvious, that for lines of the same length, the coupling area when lines are stacked is going to be greater than when the lines are side by side. To verify this assumption, EM simulations have been performed to compare both couplings. The test bench is pretty basic, it consists in the planar case of two identical lines side by side and in the stacked of these two same lines on top of each other.

This test bench is illustrated in Fig 3.19. Each line has a length of 1mm and a width of 20μm, the spacing between the lines in both case (planar and vertical) is equal to 5μm, so a fair comparison between both approaches can be performed. For this test, the Marchand approach has been picked because the transformers presented in the following sections are based on Marchand principle. It means that in a line, one terminal is the input and the other terminal is left open while in the second line each terminal is considered as an output. To make a correlation with Fig 3.19, Table 3.2

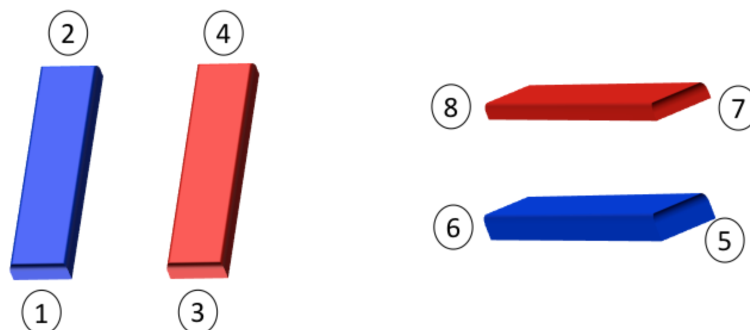

Figure 3.19: Simulated testbench to compare planar and vertical coupling -

presents ports correspondence:

Port	Planar case	Vertical case
Input	1	5
Open	2	6
Outputs	3,4	7,8

Table 3.2: Ports configuration for insertion loss simulation

Each input and output port are 50Ω. Simulation results for both case are presented in Fig 3.20.

It consists in a S-parameters simulation of the EM simulated structures. The simulation goes from DC to 50GHz, for both case the minimal loss (or the most energy transferred) is located around 25GHz. It appears that the vertical coupling is clearly more efficient than the planar one. Indeed, at 25GHz the loss for each path in the vertical case are 3.1dB and 5.1dB when they are 3.8dB and 8.4dB for the planar structure. These figures clearly confirm the fact the vertical coupling is more efficient simply because the coupling area is greater than in the planar case. Not only, it is more efficient, it has a more wideband behavior too. Indeed, it should be noticed that the loss do not vary much (less than 0.5dB) in the vertical approach while there are more variations and strong cut-off in the planar case at 10GHz and over 40GHz. On the contrary, there is a cut-off at 5GHz for the vertical structure but no upper limit until 50GHz at least.

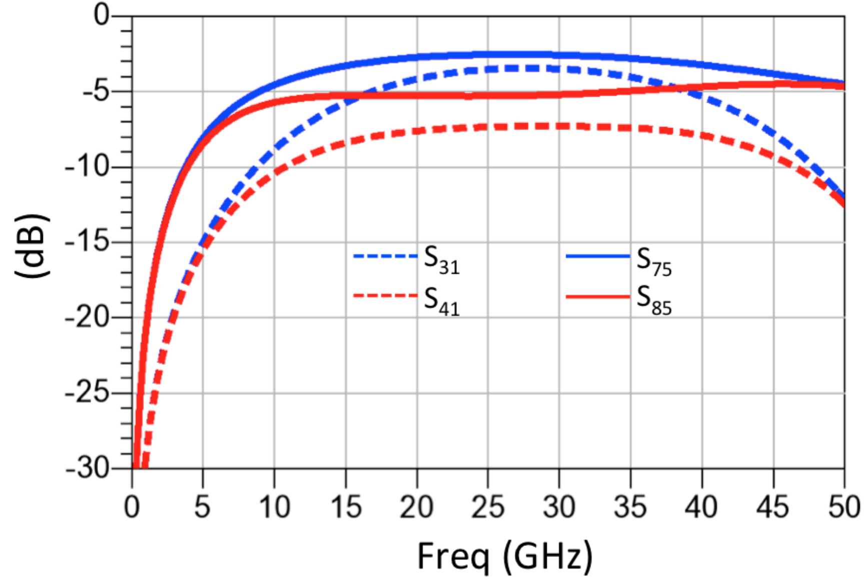

Figure 3.20: Comparaison of energy transfer between planar and vertical coupling -

The coupling factor k as defined in Eq 3.12 can also be extracted from this EM simulation. For this matter, the ports configuration is quite different though. Indeed, the equation that defines k applies only if each line has one terminal connected to a 50 Ohms load and the other one is grounded. So, still based on Fig 3.19, the ports configuration is now as described in Table 3.3:

Port	Planar case	Vertical case
50 Ohms	1,2	5,6
Ground	3,4	7,8

Table 3.3: Ports configuration for coupling factor extraction

The simulations results for both the planar (Kplanar) and the vertical (Kvertical) are plotted in Fig 3.21 from DC to 25GHz. Once again, results are in favor of the vertical approach. Indeed, the highest coupling factor corresponds to a maximal energy transfer and the vertical coupling factor is greater than the planar one by a constant margin of 0.2 all over the tested frequency range.

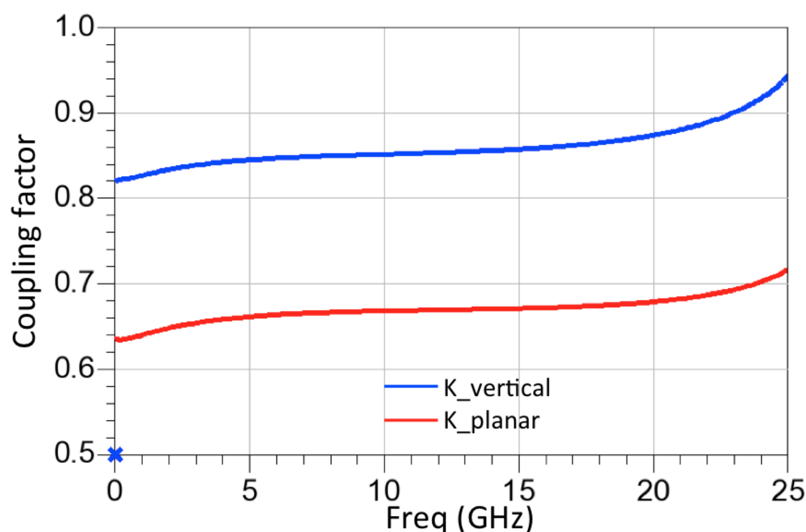

Figure 3.21: Comparaison of coupling factor between planar and vertical coupling -

From the same ports configuration and simulation it possible to evaluate the mutual inductance M (as defined by Eq 3.11) too. Plots of the mutual inductance for the two cases are reported in Fig 3.22. Once again, the vertical structure gives better performances which was predictable because the mutual inductance is just a different way to represent the energy transfer between two nearby devices. s

Looking at the plots, it appears that the vertical mutual inductance has a value greater than the planar one by 0.2nH in average, for example at 20GHz, the vertical mutual inductance is equal 1nH while the planar one is equal to 0.82nH.

Over all the simulations performed on a similar test bench for both the planar and the vertical structure, it appears that the vertical approach has better abilities to transfer power thanks to an increased coupling area, moreover its frequency behavior is wider than the planar topology. In the two previous sections, the feasibility and the advantages of stacked structures for power transfer matters have been depicted and confirmed by simulations results. In the next section, the realization of both balun transformers and couplers based on this stacked principle are detailed.

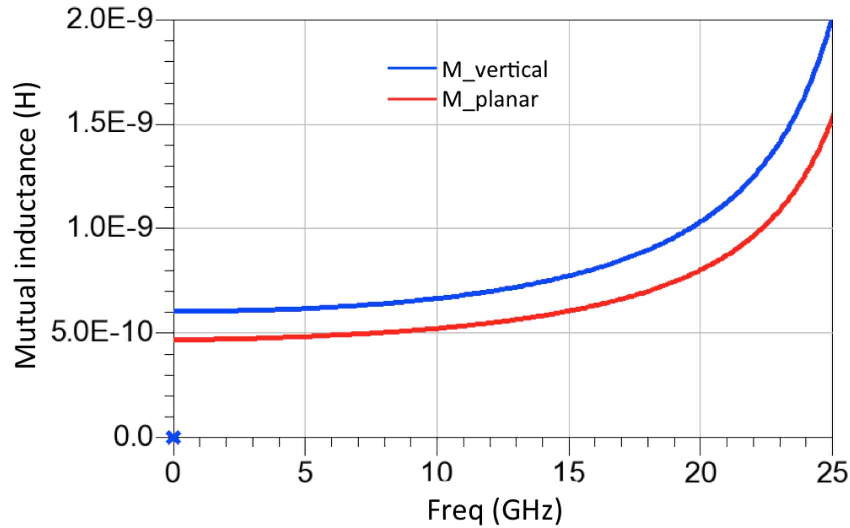

Figure 3.22: Comparaison of mutual inductance between planar and vertical coupling -

3.3 Realizations

From now on, only vertical topologies are going to be considered. Based on the principles mentioned on the previous section, two baluns transformers and a Lange coupler implemented with stacked air-bridges approach are going to be detailed.

3.3.1 Stacked Balun

Firstly, a C to Xband balun is going to be depicted all the way from design to measurements and then an improved topology to increase the bandwidth and reduce loss in the X to K$_u$-band.

3.3.1.1 C to X-band balun

Balun transformers are made of two elements (windings) and energy transfer happens thanks to coupling between them as detailed in the beginning of this chapter. When designing a balun, first thing to take into account is its frequency of operation because the windings size are made of quarter

wave length elements. Indeed as shown in Fig 3.23, each winding can be decomposed into two elements each corresponding to a quarter wave length. These elements can be wires, inductors or metal lines in the case of integrated circuits. Terminals 5 and 6 are the windings midpoints respectively for the primary and the secondary.These midpoints are not necessarily used in every case, but we will see in the following that they are very useful to spread DC feed. For the example of the primary, one element corresponding to a quarter wave length should be introduced between terminals 1 and 5 and an other between terminals 2 and 5, so basically a winding is the serial combination of two elements. Moreover, this winding midpoint can be used to spread biasing to devices connected to the winding.

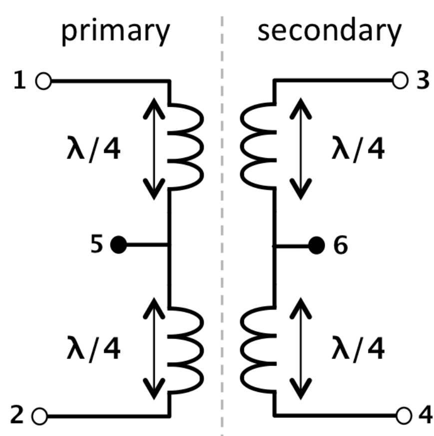

Figure 3.23: Detailed representation of a balun -

In order to size a winding, it is mandatory to first calculate the wavelength λ in the material of interest (GaN in our case). This can be done thanks to the equation 3.22 where ϵ_r is the electrical permittivity of the material concerned and F the frequency of operation and c the light velocity in the air.

$$\lambda = \frac{c}{F.\sqrt{\epsilon_r}}$$

(3.22)

Table 3.4 take a census of the quarter wave lengths for several frequency in the GaN material used to design the baluns (ϵ_r=10.2). It goes from 5.85mm at 4GHz up to 1.3mm at 18GHz. These values basically give the dimensions of the main elements that make up a balun. For optimal performances when targeting wideband baluns, the central frequency of the bandwidth should be used to size elements.

Frequency (GHz)	Quarter wavelength (mm)
4	5.85
8	2.93
10	2.34
12	1.95
18	1.3

Table 3.4: Quarter wave length upon frequency in GaN material

In early design steps and in order to evaluate broadband capabilities, balun should be designed with no transformation ratio. Indeed as detailed in (16), the larger bandwidths are always achieved when the transformation ratio is equal to one.

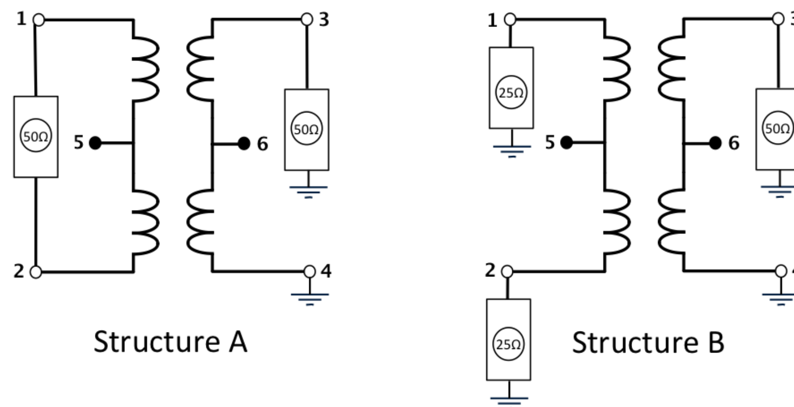

Figure 3.24: Optimal impedances for a balun with a transformation ratio of one -

By taking the example with a characteristic impedance of 50 Ohms, two configurations can be used with a transformation ratio of one, they are

both presented in Fig 3.24. For each configuration, in the secondary pin 3 is connected to a 50 Ohms load and pin 4 is grounded. On the primary there is two cases. In the first one (structure A) a 50 Ohms load is connected in between pin 1 and 2 while in the second approach (structure B), each pin (1 and 2) are connected to 25 Ohms load. These configurations keep the impedance ratio to one and thus they are optimal impedances in order to maximize the energy transfer between the primary and the secondary. . While the differential approach is more suitable to connect a differential mixer as in (17) for example, in the case of power combining, the second approach is often preferred in order to connect one autonomous power cell to each terminal of the primary as shown in Fig 3.25.

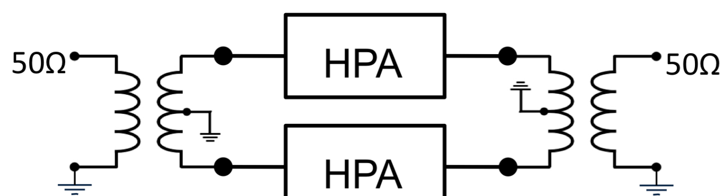

Figure 3.25: Elementary HPA combined with baluns -

With all of these considerations in mind and the stacking topology presented in section 3.2, it is now possible to move on to balun designs. Due to the innovative and exotic approach used to stack windings, it is not possible to model the coupling and mutual inductance phenomenon at schematic level. That is why there is no choice but to perform time consuming EM simulations of each structure to be tested. The simulator used is MOMENTUM from Agilent (now Keysight) both in its 2009 and 2012 versions.

To start with, a shape has to be picked for the balun, initially simple and wide shapes should be privileged not to introduce parasitic effects. Rectangular or circular shapes such as in Fig 3.26 are good candidates at this stage. A rectangular shape is selected to start with.

Following the procedure depicted in section 3.2, the primary winding is going to be implemented in the default metal layer and the secondary in the upper customized air-bridge layer. The rectangular shaped selected is

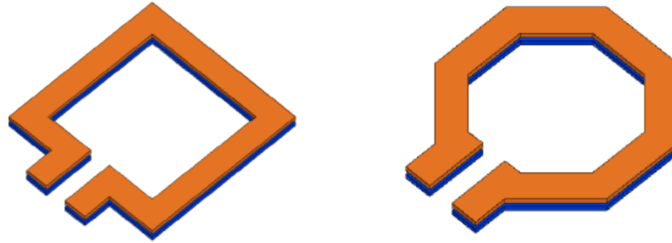

Figure 3.26: Elementary balun shapes : rectangular (left) and circular (right) -

illustrated in Fig 3.27, the angles have been curved to minimize propagation discontinuities on turns.

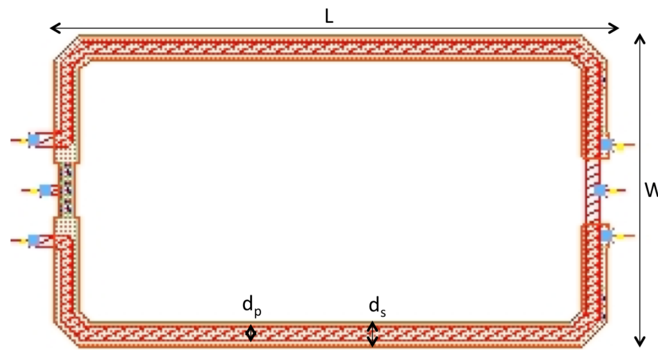

Figure 3.27: Rectangle balun and principal dimensions -

Four parameters are highlighted, they are the one to be tuned to optimize the balun performances :

* **L**: balun outside length
* **W**: balun outside width
* $\mathbf{d}_p$: primary width
* $\mathbf{d}_s$: secondary width

Firstly, d_p and d_s will be kept constant and L and W only are going to be tune to change the size of each half winding. Indeed, even if theoretically these half windings should have a length equal to a quarter wave length, we will see that in practical it differs quite a bit. A configuration similar to Fig 3.28 is used to characterize the balun overall size.

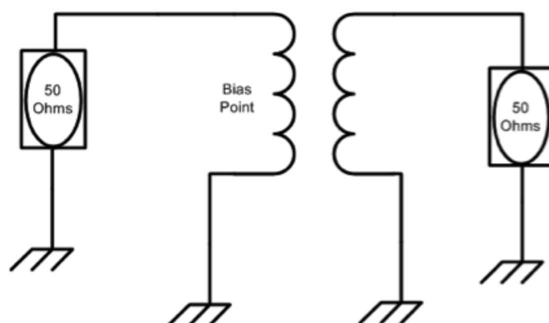

Figure 3.28: Balun configuration for geometry tuning -

Different sizes of W and L are simulated through Momentum to determine the optimal size, sizes are announced in Table 3.5. In addition of W and L, the electrical wavelength of an half-winding is also calculated to make comparison with the theoretical quarter wavelength.

This length that should theoretically be equal to a quarter wavelength of the central frequency as mentionnned previously is in this configuration equal to W/2 + L +W/2 = W + L.

Balun	W (mm)	L (mm)	Electrical length (mm)
Balun α	0.8	1	1.8
Balun β	1	1.4	2.4
Balun γ	1.2	2.2	3.4

Table 3.5: Balun sizes for geometry optimizaton

Once the EM simulations performed, the transmission parameter is plotted for the 3 baluns. It consists in performing an S-parameters analysis and plotting S_{21} if 2 is output port and 1 the input one while referring to Fig 3.28. The simulation results are plotted in Fig 3.29 for the balun sizes. As predicted by theory, the shortest the half winding electrical length is, the highest the balun central frequency is located. Indeed, the smallest balun which case α is centered around 22GHz, the medium balun case β is around 15GHz while the larger one case γ is around 9GHz.

However, when related to central frequency, the electrical length observed is quite different from what it should according theory and equation 3.22. In-

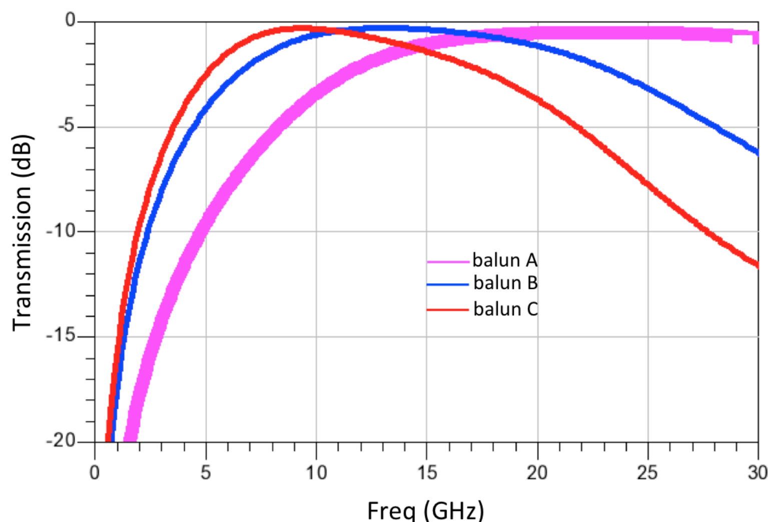

Figure 3.29: Balun response vs. geometry -

deed, in practical a larger overall value is required. For comparison matters, Table 3.6 presents the theoretical electrical length and the experimental one from simulations for various frequency points (EL stands for the electrical length of an half winding). One explication to this difference comes from the fact that each there is a turn, the electrical length is reduced as if waves were taking short cuts on turns. This is due to coupling effects when lines get close to each other on turns.

Frequency (GHz)	Theoritical EL (mm)	Simulated EL (mm)
9	2.6	3.4
15	1.56	2.4
22	1.07	1.8

Table 3.6: Comparison between theoretical and simulated electrical length (rectangular balun)

As the objective is to implement a balun working from C to X-band, the balun case γ appears to be the best candidate. Based on this geometry, next step is to select the most efficient architecture to perform the differential to single conversion. Not only minimal loss are targeted, but even before that, symmetry between the two paths is crucial aspect for power

combining applications. Indeed, it is mandatory that each path has the same frequency response and the same loss versus frequency. Two architectures are compared as shown in Fig 3.30. The conventional architecture consists in connecting each port of the primary to a load and one port of the secondary to a load too while grounding the last terminal. On the contrary on the Marchand approach, the three first terminals are connected in the same way but the last one is left open.

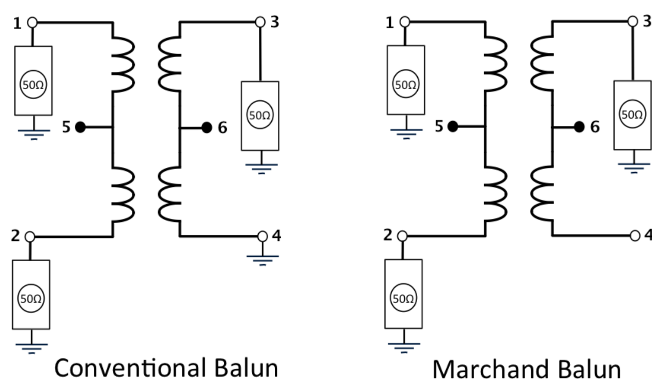

Figure 3.30: Conventional and Marchand balun arhcitecture -

As shown in schematics, each terminal is connected to a 50 Ohms load without taking into account for the transformation ratio. Indeed, the objective for now is to compare the two structures in similar conditions and moreover when performing measurements of the realized balun, there would be no choice but to connect it to 50 Ohms loads.

Both configurations are simulated and plotted in Fig 3.31. Ports numbering is done according to Fig 3.30, which means that for both cases, port 3 is the output while 1 and 2 are the differential inputs. S_{31} and S_{32} are plotted for each configuration from DC to 20GHz.

The Marchand topology exhibits better performances and behavior. Indeed, not only in terms of symmetry but also with regards to bandwidth the Marchand approach performs better. For example the magnitude imbalance does not exceed 1dB from 5 to 16 GHz while for the conventional case there is an average of 2dB difference and goes up to almost 3dB from 3 to 14GHz.

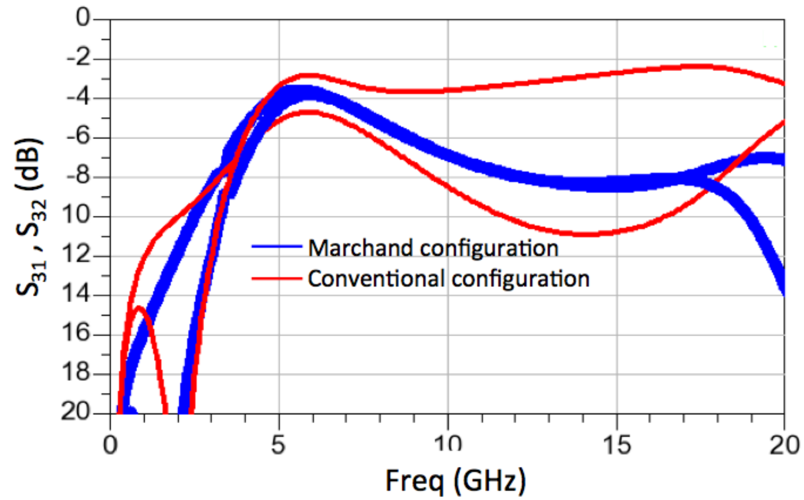

Figure 3.31: Transmission parameters for a conventional and a Marchand balun -

From now on, the Marchand like approach is the only one that would be used.

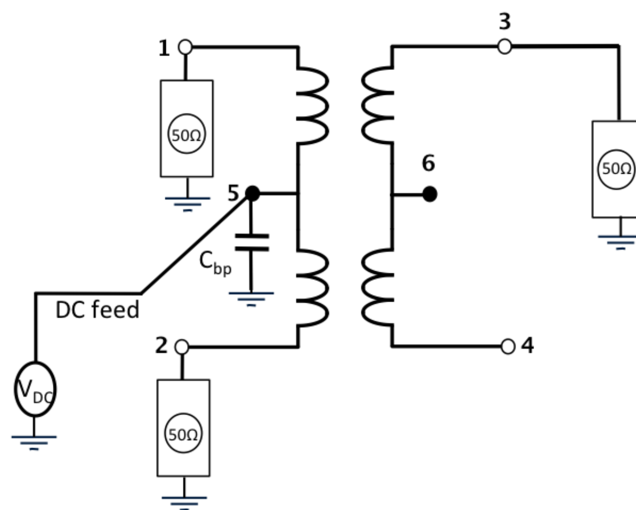

Figure 3.32: Using winding midpoint as DC feed -

When using balun as a power combiner or splitter, an interesting aspect can be used. Indeed, it is possible to use the windings midpoint to provide DC feed to each terminal of the concerned winding. Thanks to that it i

possible to supply DC power to the power cells connected to the balun. In practical, drain voltage can be provided by the output balun used as a power combiner and the gate voltage by the input one used as a splitter. Fig 3.32 is a schematic representation of such an architecture. When using this feed approach, it is important to make sure that the RF signal is going to be blocked and not leaking through that DC feed because this would result in increase insertion loss for the balun and even worst risk of oscillations as an RF component would be injected into the DC supply. To make sure this does not happen, it is mandatory that the winding midpoint is as close as possible to a perfect ground from an RF point of view, which means either an actual ground or a DC voltage. Two criteria have to be fulfilled to ensure this condition: first, a transmission line with a length close to a quarter wave length of the balun central frequency has to be inserted between the midpoint and the DC feed and secondly, large bypass capacitors have to be placed as close as possible to the balun midpoint. These two conditions should ensure good RF rejection and no perturbations in the balun behavior.

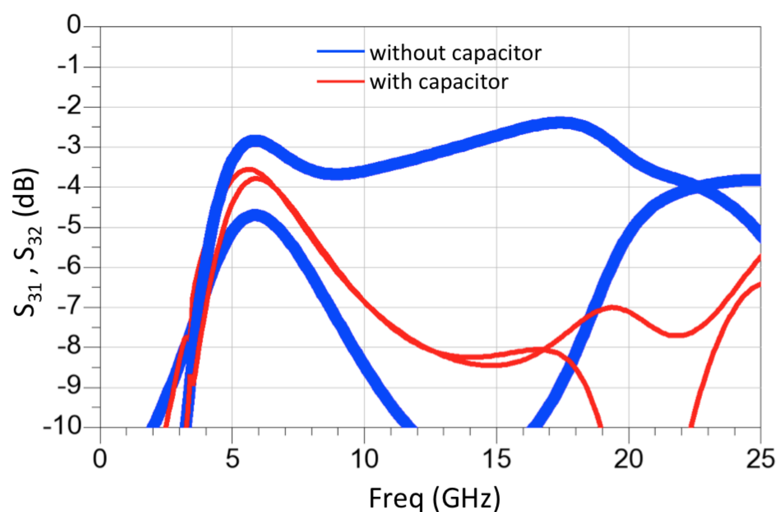

Figure 3.33: Transmission parameters for a balun with DC block capacitor and without -

Fig 3.33 presents is a plot of S_{31} and S_{32} for the Marchand balun with its midpoint connected to a DC feed, blue traces are without the bypass capacitor while the red ones are with a 10 pF capacitor connected in parallel

to the winding midpoint has shown in Fig 3.32. Once again, the impact of the decoupling capacitor is drastic. Indeed without capacitor, the response is extremely attenuated in one of the two paths to more than 5dB compared to the other path from 4 to 12 GHz. On the contrary, with the capacitor the response is much improved and the symmetry is great from 4 to more than 15GHz. A value of 10 pF was used, because it is the largest that can be implemented and the highest the value is, the best RF ground it provides. In the following, this capacitor is always going to be present whenever midpoint is used as DC bias.

With all of these considerations in mind, it is now possible to evaluate the performances as a balun transformer of our device. As a reminder, the balun selected has a rectangular shape with overall length and width of 2.2mm and 1.2 mm respectively. It used in Marchand configuration with a DC feed connected to the primary winding.

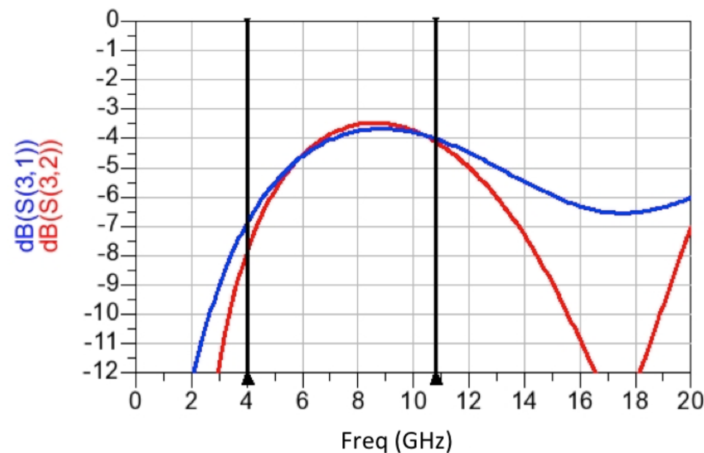

Figure 3.34: Transmission parameters for the rectangle balun -

The transmission parameters and the phase difference between the differential path compared the output are respectively plotted in Fig 3.34 and Fig 3.35. In terms of magnitude a very good symmetry is noticed between the two paths, from 4 to 11GHz the magnitude imbalances averages 0.15dB and does never exceed 0.6dB. In terms of loss, a minimal value of 0.6dB is achieved at 9GHz and the 3dB bandwidth goes from 4.5GHz to 11GHz.

Concerning losses, 3dB have to be removed from the values that can be read on the plots due to the differential to single conversion. Regarding the phase difference between the paths, the optimal value of 180°is obtained around 7GHz and it linear decreases from 176°at 4GHz to 185°at 11GHz, which corresponds to a relative error lower than 2.8%, a value more than acceptable to perform power combining.

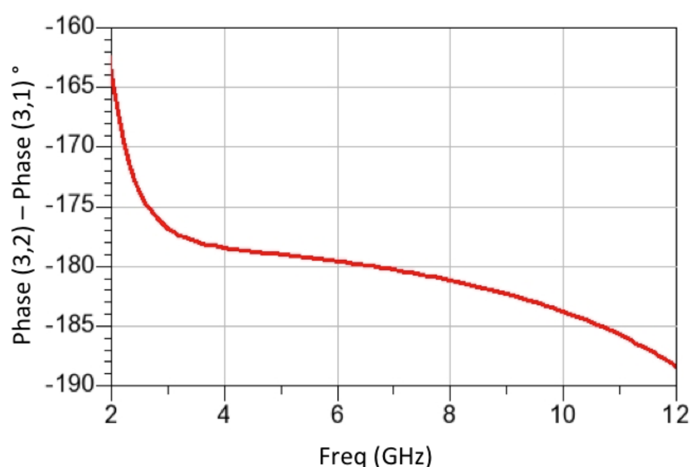

Figure 3.35: Phase difference for the rectangle balun -

This rectangular shape appears to be working properly (both in terms of loss, phase difference and imbalance) to work as a power combiner, however its size is quite massive (2.64mm^2). To solve this issue and shrink its size as much as possible, the balun shape should be optimized. Indeed, in the rectangular structure, there is a big empty space within the balun. So it is decided to give a wave and circular shape to each half winding to decrease its size. As shown in Fig 3.36, with this technique, the overall size is reduced from 2.64mm^2 to 1.44mm^2, while keeping the same electrical length for the half windings so in theory the same bandwidth and central frequency.

As the waves shapes get quite close to each other, the overall coupling should be increased because not only vertical coupling but planar coupling is happening too with this configuration. The same simulations as for the rectangular baluns are performed to ensure that shaping did not change the

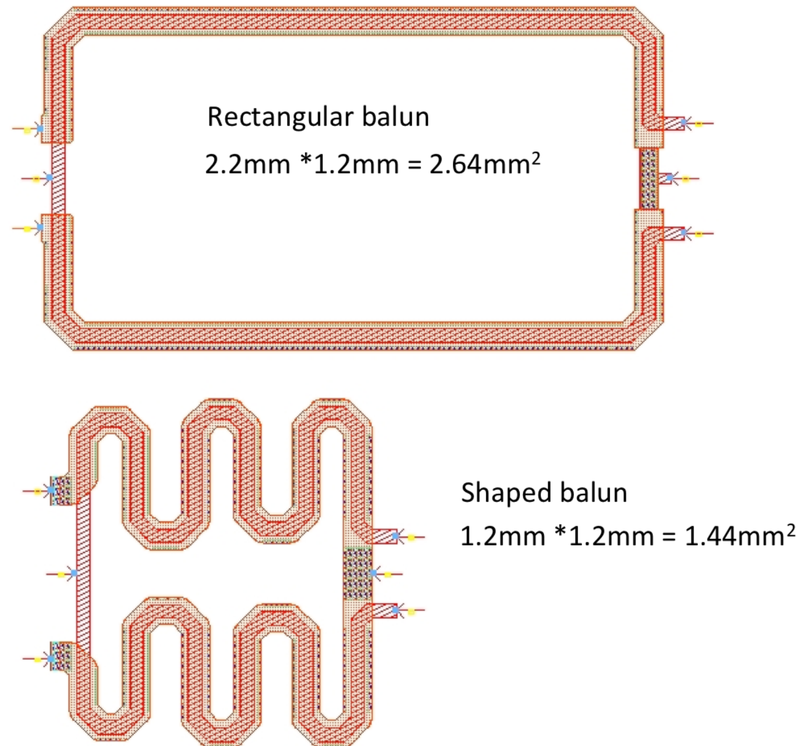

Figure 3.36: Shaping a balun to reduce its size -

performances. The results are quite impressive because the plots exhibit the exact same behavior.

This shaped balun has been realized with the UMS GaN integrated process GH25. A picture of the realized balun is presented in Fig 3.37, its length and its width are both equal to 1.2mm resulting in overall an area of $1.44mm^2$. As mentioned before, the DC bias has been included to the primary winding and a bypass capacitor is connected as close as possible to the midpoint. The capacitor has been located inside the balun to reduce size even more. For measurement matters, the primary winding is connected to a differential RF pad, but during measurements each input would act independently and in opposition of phase.

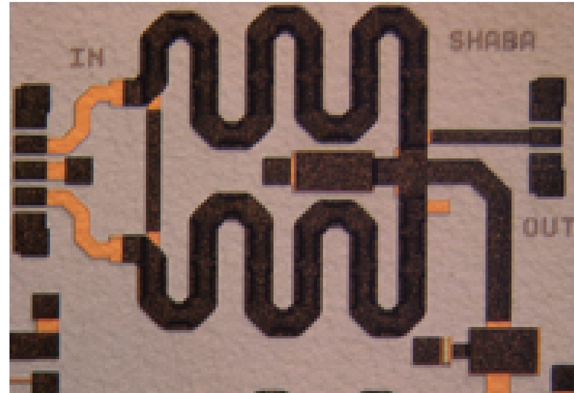

Figure 3.37: Realized C to X band balun -

Last step is to make a comparison between the EM simulations and measurements. Measurements are performed under probes with a VNA (vectorial network analyzer) to extract S-parameters. Then, by inputting these measurements back into Agilent ADS simulator, a fair comparison can be made between simulations and measurements. To be even more precise, connections to RF pads have been added to EM simulations. Ports configuration and numbering used in the following plots is the one depicted in Fig 3.38. Terminals 3 and 6 are the outputs respectively for EM simulation and measurement, while 1,2 and 4,5 are the differential inputs. As mentioned earlier, each connected port is 50 Ohms both for simulation and measurement.

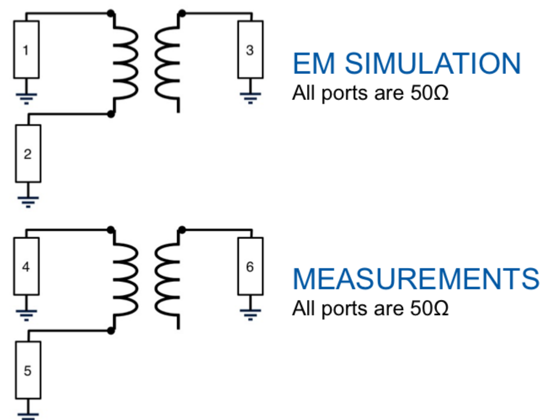

Figure 3.38: Ports configuration for EM simulation and measurement -

Fig 3.39 presents the transmission parameters. Measurements are plotted in red and simulation results in black, the link between the paths are made with either the plain curves or circled one. A quasi ideal agreement is observed from 3GHz to 11GHz, indeed the difference between measurement and simulation do not exceed 0.3 dB for the worst case and averages under 0.1 dB in this frequency range. After 11Ghz, there is a divergence in results but this happens in the region where the device does not act as a balun anymore which certainly explains these differences. A minimal value of insertion loss of 0.6dB is obtained at 5.6GHz and the 1dB bandwidth goes from 5 to 7GHz. This 1dB bandwidth is quite small in this case, because 50 Ohms impedances are presented to the balun when they should of 25Ohms to respect the transformation ration. However, the aim was to compare simulations and measurements to make sure the design methodology was accurate and reliable. In the next chapter, where baluns would be used to combine power cells, optimal impedances would be presented to them.

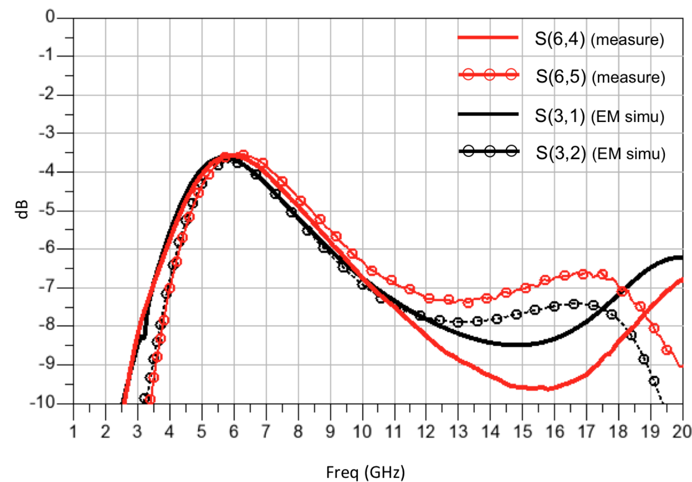

Figure 3.39: Transmission comparison for EM simulation and measurement -

Fig 3.40 is a comparison of the phase difference between the differential paths. Measurement plot is in red while simulated one is in dash black. Once again the correlation between the two is pretty strong, indeed the difference goes from 0.1°at 3GHz to 3°at 11GHz.

Last thing to compare to ensure, that the balun was properly modeled with

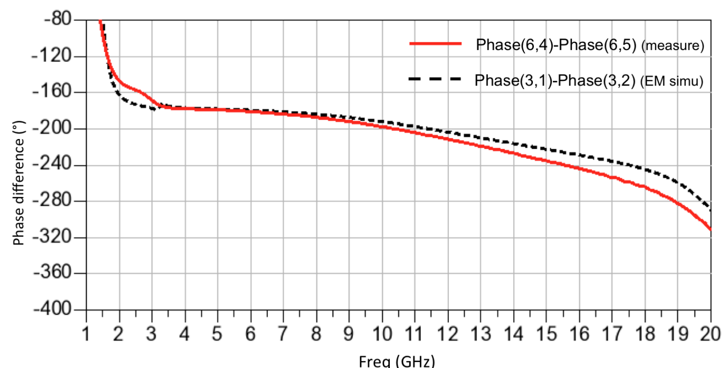

Figure 3.40: Phase difference comparison for EM simulation and measurement -

the EM simulator is the reflection coefficient for each port, the results are presented under Smith chart format in Fig 3.41. Even though, it is more difficult to give a numbered comparison when looking at Smith charts, the correlation looks very good. Indeed, for each port, both plots have the same shape and follow each other quite well.

With this realization, not only the concept of vertically stacked balun in an MMIC process with the help of a customized air-bridge layer has proven to be functional and quite efficient regarding its performances and its overall size but a good correlation between simulation and measurement is reported too proving the good modeling made in EM simulations. This modeling aspect is mandatory in order to realize others baluns with even better performances as detailed in the next section.

3.3.1.2 X to Ku band balun

Based on the methodology detailed in the previous section, a second balun has been designed to achieve wider bandwidth and lower losses. Now that the concept has been validated with measurements of a first balun, it is possible to be more aggressive and take more risks to get better performances out of stacked balun. The balun designed in this section is meant to work in X and K_u-band that is to say from 8GHz to 18GHz. The structure is similar

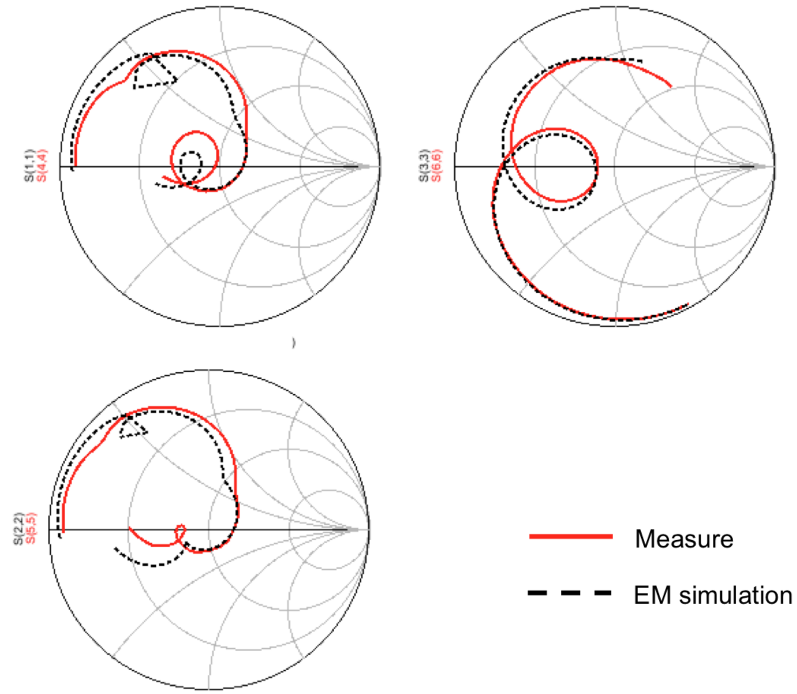

Figure 3.41: Impedances comparison for EM simulation and measurement (2Ghz to 12GHz) -

to the one used for the C to X-band balun, the lengths of the elements has to be decreased though because the central frequency is now around 13GHz.

Moreover, to reduce even more the size and increase the bandwidth at the same time, a capacitor based solution is used. This solution which is detailed in (18) consists in adding one or several capacitors in parallel of the two differential terminals. This capacitive loading virtually increases the electrical length of each half winding so they can be physically shorter and moreover it creates resonances which result in a bandwidth increase. Fig 3.42 illustrates the location of the capacitors. The simulation presented in the following, will be done under the configuration from Fig 3.42, that is to stay Marchand like configuration as before, 50Ω load to the output bur this time 25Ω load to the input terminals because this balun has not been neither realized or measured so there is no need to perform the comparison on 50Ω load.

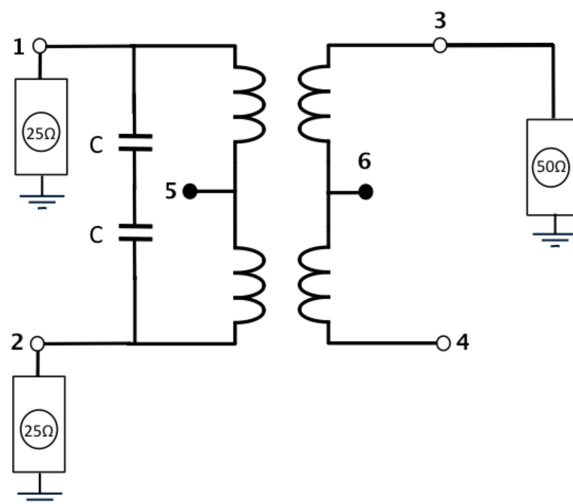

Figure 3.42: Capacitor added in parallel to the differential winding to reduce size and increase bandwidth -

Always with the objective in mind to reduce overall size, the capacitors have actually been placed within the balun instead of on the terminals, so the power cells when using the balun as a power combiner can be connected as close as possible to the balun which is a good thing both in terms of size and insertion loss. The EM simulated balun is shown in Fig 3.43. Its length is equal to 0.62 mm and its width to 0.6mm, resulting in an area of 0.38 mm^2. After optimization, the optimal case selected was to introduce two capacitors of 0.2pF each.

Fig 3.44 presents the transmission parameters for this improved balun that is to say S_{31} and S_{32}. It exhibits minimal loss of 1dB at 10 GHz and goes from 1.4dB at 8GHz to 1.8dB at 18GHz with a magnitude imbalance lower than 0.15dB all over the band. Not only, this balun exhibits better performances in terms of bandwidth and intrinsic loss, it also much more symmetrical than the previous one.

Looking at the phase difference between the differential paths presented in Fig 3.45, a similar analysis can be made. Indeed, the phase difference fluctuates from 180.1°to 181.2°from 10 to 18GHz, resulting in phase error lower than 0.6%.

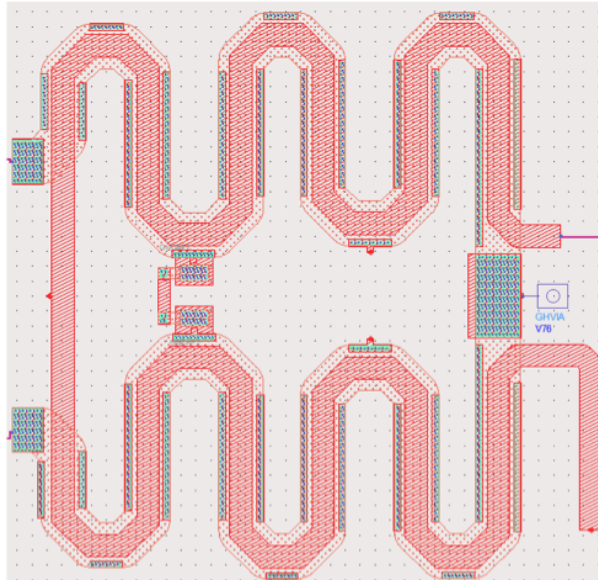

Figure 3.43: X to Ku-band balun with inside capacitors -

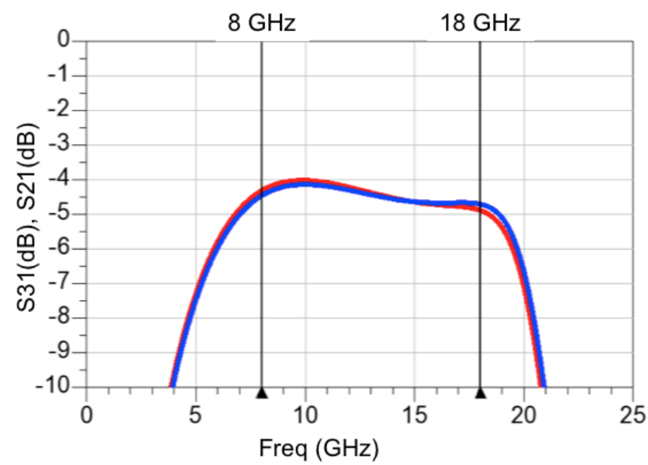

Figure 3.44: X to Ku-band balun transmission parameters -

The performances of this improved balun are summarized in Table 3.7

Throughout this section, a new way to implement stacked baluns in an MMIC process with a single default metal layer has been depicted and proved to be functional with measurement results. Each of the baluns detailed in this section will be each use in the next chapter as power combiners (and even splitter) for the realization of two different high power amplifiers.

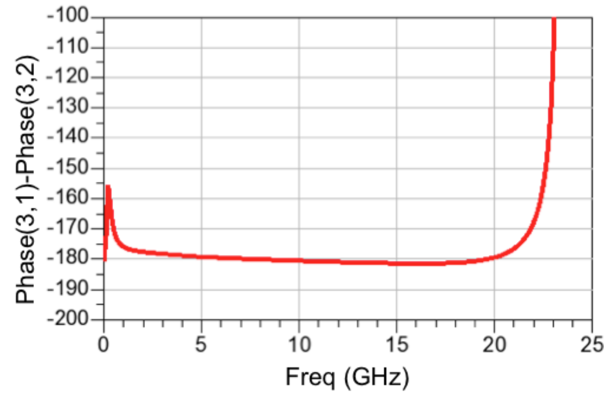

Figure 3.45: X to Ku-band balun phase difference between differential paths -

Frequency (GHz)	Insertion loss (dB)	Imbalance (dB)	Phase (°)
8	1.4	0.15	180.1
10	1	0.12	180.6
18	1.8	0.2	181.2

Table 3.7: X to Ku-band balun performances

Thanks to their compact sizes and low insertion loss, they will definitively contribute into the successful realization of compact and efficient HPAs.

4

Wideband High Power Amplifiers

This chapter focuses on the design and realizations of HPA (High Power Amplifiers). All of the circuits presented here rely and use the power combiners presented in the previous chapter. Two different amplifiers are presented here. The first one is a compact 2 stages C to X band HPA and the second one is a differential TWA (Traveling wave Amplifier) working fro 8 to 18GHz. They have both been designed with the objective to make them as compact as possible. Indeed, the objective is not to compete with the state of art in terms of output power because lots of work has been already done with this aim as detailed in the state of art presented in chapter 2. The philosophy here, is to take advantage of the stacked structures presented in chapter 3 to reduce size of power combiners while keeping high efficiency and large frequency bandwidths.

4.1 C to X-band high power amplifier

4.1.1 Specifications

This first HPA has been realized in the frame of the SIMCLAIRS (Studies for Integrated Multifunction Compact Lightweight Airborne Radars and Systems) program , a consortium lad by the EDA (European Defence Agency)

including leading companies in the domain of MMIC design for airborne and military applications such as THALES SA, SELEX and SAAB. One of the topics addressed in this program was the design of wideband and high efficiency high power amplifiers. The applications targeted are X-band military radars and electronic warfare. To this extent, some specifications have been extracted, there are summarized in Table 4.1.

Bandwidth (GHz)	2.7 - 10.8
P_{sat} (dBm)	35 in [2.7GHz - 9.8GHz] 38 in [9.8GHz - 10.8GHz]
PAE (%)	>30 in [2.7GHz - 9.8GHz] >40 in [9.8GHz - 10.8GHz]
Conditions	CW @ 80°C
Die size (mm^2)	15 to 20
Technology	GaN GH25 (UMS)

Table 4.1: C to X band HPA specifications

Even though these objectives appear quite reasonable in terms of output power, the efficiency criteria seems much more difficult to achieve. Moreover, inside a single chip a dual behavior is expected in terms of output power and PAE. Indeed, 35 dBm and 30% PAE are required in most of the frequency range but 38 dBm and 40% PAE are expected in the last gigahertz of the band located within the X-band. As it is often done, the output power stage is going to be designed first before moving on to the input stage, each stage is detailed in following sections.

4.1.2 Output power stage

The output stage is critical both in terms of output power and efficiency. Indeed, the power capabilities of the overall HPA are limited by the output power of this stage. Moreover, it is the stage that would draw the biggest amount of current so it would have the largest impact on PAE. That is why, a specific design flow has to be followed to size the active elements properly and ensure best results. The design flow adopted is depicted in Fig 4.1.

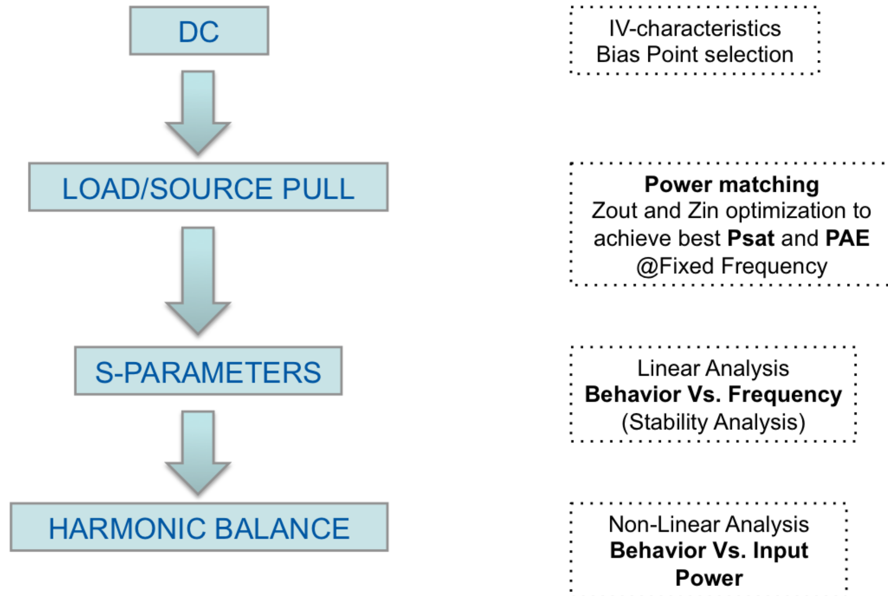

Figure 4.1: Proposed designed flow for HPA design -

It is mandatory to start with a DC analysis in order to size the transistors gate development for them to deliver the required output power and bias them at their optimal point of operation. Once that step completed, source/load pull simulation can be performed to find optimal impedances in terms of output power and efficiency, keeping in mind that a tradeoff has to be made because optimal impedances for PAE and output power are not the same. Moreover, when working over a wide frequency range, these source/load pull simulations have to be performed for several frequency points because the optimum change with frequency. Next, a linear analysis will be run to check stability and behavior versus frequency, the linear gain can be adjusted at this stage too. Finally, harmonic balance simulations for several frequency points will give indications on the compression point and the available output power and achievable efficiencies.

Common source architecture is going to be the base structure of the HPA thanks to its behavior in terms of linear gain and ability to deliver power. Cascode architecture could be considered too, but it is not needed in our case, indeed GaN transistors can handle such high voltage(breakdown around

100V) swings that they are able to create enough powers when used as standalone cells. So, the schematic used to perform most of the following simulations is the one introduced in Fig 4.2. Both DC feed and bias have not been represented for ease of reading and clarity but they are provided directly through drain and gate with a an ideal serial inductor with an high value (1μH).

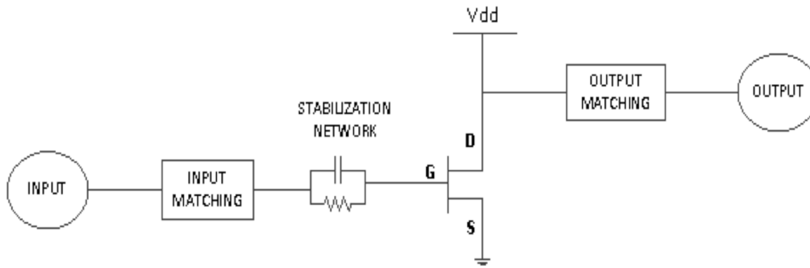

Figure 4.2: Common source topology used to characterize transistors -

Several transistors are available on the UMS GH25 design kit. When focusing on those dedicated to power applications, there are options for number of fingers and finger widths. Devices from 2 to 8 fingers with elementary finger width from 75μm to 150 μm by increment of 25μm can be used. Best efficiencies can be achieved with smaller devices while output power increase with the transistor size, so once again a tradeoff has to be made. According UMS recommendations, static drain voltage should not exceed 25V and bias current should be around 100mA by mm of gate width development in order to guarantee optimal reliability and lifetime.

Using the schematic presented in Fig 4.2, both gate and drain voltage are swept to perform DC characterization of active devices. Firstly, drain current (I_{DS}) is plotted versus V_{DS} for various V_{GS}. The network of curves obtained from this simulation is plotted in Fig 4.3 for the case of an 8*125μm transistor. It can be noticed that if the gate voltage is under -3V then the transistor is blocked and no current flows from drain to source, the pinch-off voltage is exactly of -2.95V. To fulfill UMS recommendations, with a drain supply of 25V, the gate bias should not exceed -2V, indeed in these conditions the drain current is equal to 100mA for that transistor which overall

gate development is equal to 1mm.

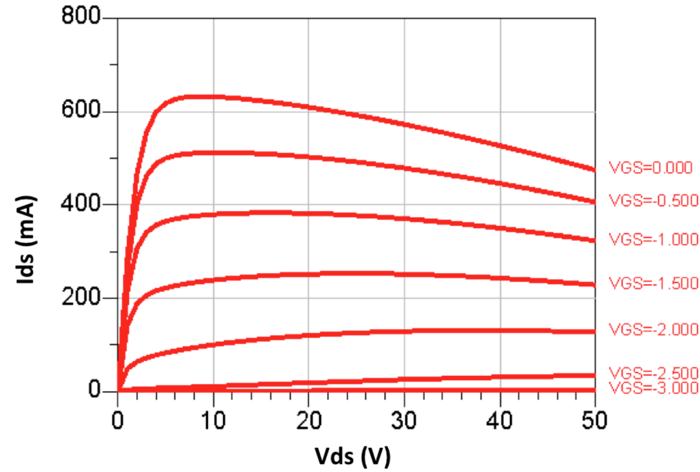

Figure 4.3: I_{ds} vs. V_{ds} for various V_{gs} for an 8*125μm device -

It is important to notice that for gate voltage greater than -1.5V, the current does not behave as predicted in the saturated region. Instead of staying constant when V_{DS} increases, I_{DS} starts do decrease, this phenomenon is due to the thermal effects that are being take into account in the transistor model. In fact, when a certain amount of current is flowing through the transistor, it starts heating and then the current density decreases which results in a smaller I_{DS}. This thermal effects can be deactivated in the transistor model, but in this case they should be kept on as this circuit is meant to work under CW conditions so the active devices will actually heat up. It is only in the case of pulse operation mode, that active devices have time to cool down in between two pulses and thus current is not decreasing.

Next DC analysis, consists in plotting the drain current versus the gate voltage at a fixed drain voltage, plot is presented in Fig 4.4 for an 8*125μm device with V_{DS} set to 25V. This plot confirms that the pinch-off is slightly greater than -3V, we also get information on the saturated current which is around 800mA for this particular device.

This $I_D(V_{GS})$ characteristic is very useful to choose the transistor class of operation. For example, the transistor is in class A when the bias current is equal to the half of the saturated current (400mA in this case) and class

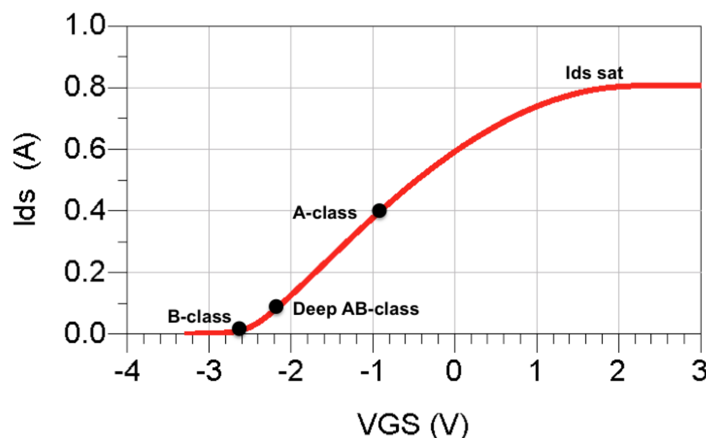

Figure 4.4: I_{ds} vs. V_{gs} for V_{ds} =25V for an 8*125μm device -

B corresponds to a gate voltage equal to the pinch-off value. Following the 100mA/mm rule, results in the device working in deep AB class which is optimal in terms of efficiency as detailed in chapter 2. Whatever the transistor size chosen in the following, the gate voltage would be between -2.2V and -2V to ensure a drain current around 10 to 15% of the saturated current, this would guarantee both deep AB class and reliability requirements. So from this DC analysis and for every transistor size, the bias point would be set to:

* **V_{DS}**: 25V
* **V_{GS}**: from -2.2V to -2V
* **I_{DS}**: from 80 mA/mm to 100mA/mm

Once the bias point selected, next step is to perform load and source pull analysis both to determine the transistors optimal impedances and to evaluate performances in terms of output power and PAE. This analysis consists in sweeping the impedances presented to both the input and the output of the transistor alternatively. Indeed, as the transistor isolation is not infinite, a change in load impedance in one side would have repercussions on the other side. One way to perform this simulation is to set a fixed load on the input side and sweeping loads on the output. After that, it is the output

load that is fixed and the input one sweep. Forming this routine back and forth should end up in the optimal impedances not changing anymore after a few iterations (generally 3 or 4 is enough). Commonly, the impedances are swept in phase at constant magnitude and thus for various magnitude values, this results in circles if plotted in a Smith Chart. Simulation results are often plotted in Smith Chart too for ease of read, the results obtained are circles of constant output power and circles of constant efficiency, in fact they could be circles of constant "any parameters" designers might want to optimize. An example of a Load pull simulation results is presented in Fig 4.5 for an 8*125μm device at 8GHz.

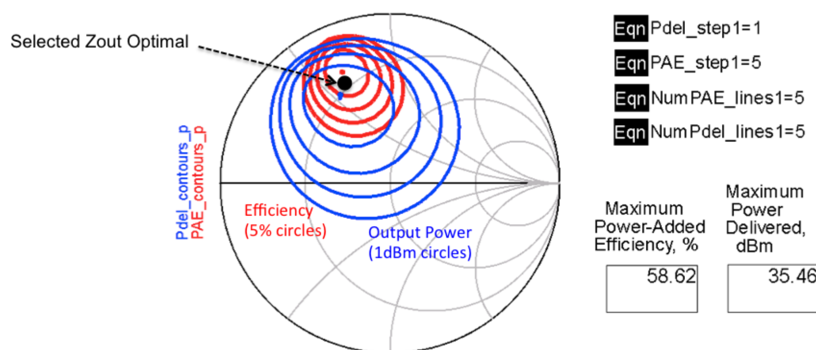

Figure 4.5: Load pull simulation results for an 8*125μm device at 8GHz -

Output power (blue circles) and efficiency (red circles) have been plotted. In this example, the maximal output power is equal to 35.5dBm and the maximal efficiency is 58.6%. However, these two maximum are obtained for different impedances so they can not be achieved together, a trade off has to be made. Power contours are 1dB and efficiency ones are 5% which means that when staying inside the same circle the output power won't change by more than 1dB (or the PAE by more than 5%). As shown in this plot, the optimal impedance is picked somewhere in between the two optimums. As the optimal impedances are frequency dependent, these source/load pull analysis have to be performed for several frequency point when working over a wide frequency range. In this analysis, the input power considered is the one delivered by the generator and the one that actually goes inside

the device. Indeed, these two power levels differ because the devices are not matched and thus some energy is reflected back to the input generator.

These three analysis are enough to select the best transistor size according to the overall HPA specifications. Considering the output power required (35 to 38dBm), only 8 fingers devices are considered, the others being to small to produce that kind of output power, or at least it would require to put to many of them in parallel to obtain the desired values. So, in order to select the best size to achieve both output power and efficiency criteria, all of the simulations presented before are performed for each 8 gates transistor available, results are presented under a chart form for ease of read in Fig 4.6. Simulations are performed at 10GHz for now, because it is in the region where higher power and efficiency are targeted. These results highly rely on the impedances chosen during the source/load pull steps, in this case they have been chosen to obtain a maximal PAE, which explains the non linear variations in maximal gain for example.

N (fingers)	8	**8**	8	8
W (µm)	150	**125**	100	75
Wtot (mm)	1,2	**1**	0,8	0,6
Vds (V)	30	**30**	30	30
Vgs (V)	-2,2	**-2,2**	-2,2	-2,2
Ids (mA)	99	**82**	66	49
J (mA/mm)	82,50	**82,00**	82,50	81,67
OCP1 (dBm)	27,74	**26,80**	25,50	24,80
Psat (dBm)	36,75	**35,94**	35,15	33,75
PAE max (%)	54,82	**55,00**	55,56	57,30
Gain Max (dB)	15,75	**16,50**	15,58	14,33
Gain @PAE Max (dB)	10,10	**11,18**	9,50	9,03
Zin (Ohm)	4,22 +j*3,2	**5,0 +j*3,1**	9,1 +j*1,25	19,8 +j*11,7
Zout (Ohm)	9,8 +j*30,1	**12,2 +j*36,3**	16,1 +j*44,6	20,7 +j*62,0

Figure 4.6: Comparison between different gate widths for an 8 fingers transistor at 10GHz -

Each device has been biased with the same current density (J in the chart) for the comparison to be fair. As expected, the smallest transistor has best efficiency and the biggest one has the highest output power. Moreover,

the optimal impedances (both input and output) decrease when the device size increase and it is important to keep in mind that the farther you go from 50Ω, the more losses the matching network is going to introduce. Based on these considerations, the 8*125μm device appears to be the best compromise in this case. However, it is not able to deliver more 35,9dBm which certainly enough to match the large bandwidth specifications of the HPA to be designed (35dBm) but not the reduced bandwidth and high power mode (38dBm), so they will be no choice but to combine at least two of these devices with a power combiner to obtain the required output power. This selected device can achieve 55% PAE in best case, but taking in consideration loss introduced by combiners and matching networks that would degrade the efficiency, it should possible to achieve the efficiency specifications for the HPA.

Before going into power combining steps, the power response of the device needs to be evaluated. This is done with a non linear simulation as an Harmonic Balance one for example. The device is biased as mentioned in DC characterization and has optimal impedances. The analysis consists in sweeping the input power, to evaluate the transistor behavior under compression and high input power. Output power, PAE and associated gain are plotted versus input power in Fig 4.7 for the 8*125μm device at 10GHz.

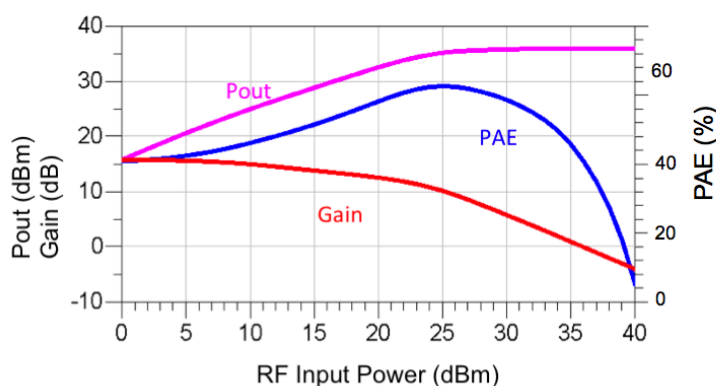

Figure 4.7: Non linear simulation results for an 8*125μm device at 10GHz -

The weak compression distinctive feature of GaN devices is clearly highlighted. Indeed, the maximal efficiency is obtained for a gain decrease

of 5.5dB compared to the small signal gain. Moreover, the PAE max is obtained slightly before output power saturation. For an input power of 25dBm, the output power is equal to 35dBm together with a PAE of 49% and an associated gain of 10dB. To obtain maximal performances, this power transistor should be driven by a driver stage that delivers around 25dBm to achieve maximal efficiency. This simulation has been performed for several frequency points over the bandwidth of interest, results are presented on a chart in Fig 4.8.

Frequency (GHz)	3	6	8	10	12
N (fingers)	8	8	8	8	8
W (µm)	125	125	125	125	125
Wtot (mm)	1	1	1	1	1
Vds (V)	25	25	25	25	25
Vgs (V)	-2,2	-2,2	-2,2	-2,2	-2,2
Ids (mA)	78	78	78	78	78
J (mA/mm)	78,00	78,00	78,00	78,00	78,00
OCP1 (dBm)	26,44	26,10	25,70	25,65	25,70
Psat (dBm)	35,30	35,30	35,80	35,92	36,00
PAE max (%)	63,16	59,80	58,70	56,45	53,94
Gain Max (dB)	16,44	15,30	15,60	15,80	15,10
Gain @PAE Max (dB)	9,80	8,75	9,90	10,11	9,20
Zin (Ohm)	36,25 +j*39,33	24,36 +j*20,6	14,08 +j*6,39	6,51 +j*3,45	2,5 +j*3,58
Zout (Ohm)	48,75 +j*60,39	24,3 +j*46,9	19,22 +j*37,8	14,38 +j*32,2	10,16 +j*27,54

Figure 4.8: 8*125μm device characteristics vs. frequency -

As the intrinsic gain of transistors is higher in low frequencies, they exhibit better performances in terms of output power and efficiency. Moreover, it is important to notice the strong dependancies of optimal impedances in function of frequency, for example the output optimal impedance goes from 49Ω +j*60Ω at 3 GHz to 10Ω +j*27Ω at 12 GHz.

This frequency dependence is crutial parameter to take into account, indeed the matching networks would have to follow these impedances variations to ensure optimal performances all over the bandwidth. To give an idea of the requirements for the matching networks, the optimal selected output impedances have been plotted on a Smith Chart versus frequency in Fig 4.9.

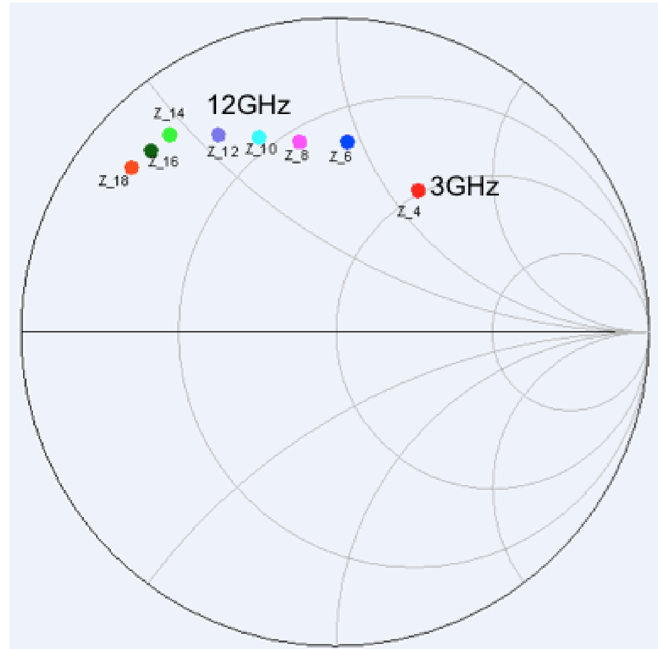

Figure 4.9: 8*125μm device selected optimal impedances in Smith chart -

Based on these results, it is mandatory to combine two active devices to meet the specifications in terms of power and PAE. The proposed architecture consists in combining two devices with the C to X-band balun realized and presented in section 3.3, this would allow to end up with a single output matched to 50Ω. As far as the input is concerned, it would be left differential at this stage because a driver stage implemented next would provide a differential signal. The architecture proposed is presented in Fig 4.10.

The supply voltage would be fed to the power devices through the balun midpoint by taking the precautions exposed in chapter 3 (bypass capacitor and quarter wavelength DC feed line). Even though, the balun combiner was characterized with 50Ω in the previous chapter, it was in fact designed to be as close as possible to the active devices optimal impedances and following them frequency wise. Inductive matching networks are introduced in between transistors and the balun to compensate for the transistors capacitances, they are implemented by transmission lines (TL) instead of inductors because inductors could not carry the amount of current delivered by each power cell. To prevent from low frequency self oscillations, an high pass RC

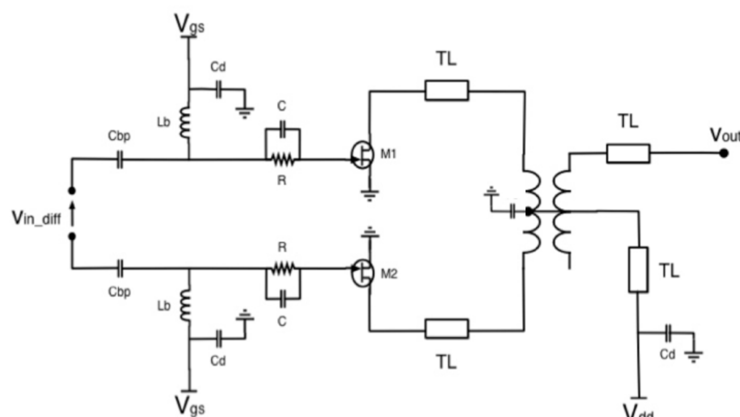

Figure 4.10: Selected architecture for the output stage -

network is placed on each device gate in order to cut the low frequency gain of the devices. The bias voltage is fed directly to the gates through choke inductors (L_b) and bypass capacitors (C_d) to ensure proper RF rejection. The DC power consumption of this overall output stage is equal to 160mA @25V.

This stage has been realized has a standalone one with differential input and single output instead of being connected directly to a driver. Indeed, it was mandatory to be able to measure it by itself specially to make sure of the balun combiner behavior, this power stage and the standalone balun have been realized at the same time, so no measurements of the balun were available before the amplifier design. The input has voluntary not been matched in order to be connected to the driver stage in the future. In fact it did not make sense to match to 50Ω as it it meant to be connected to a stage which is not 50Ω either.

The simulated small signal gain is presented in Fig 4.11 while non linear simulations results are presented in in Fig 4.12. The small signal gain reaches a maximum of 2.5dB at 4.2Ghz and remains over 10dB from 2.8GHz to 6.3GHz, then it is constantly decrease to 5.5dB at 10.8GHz. This decrease comes from the fact that the input is not matched and this issue will be fixed when considering the overall HPA with its driver stage.

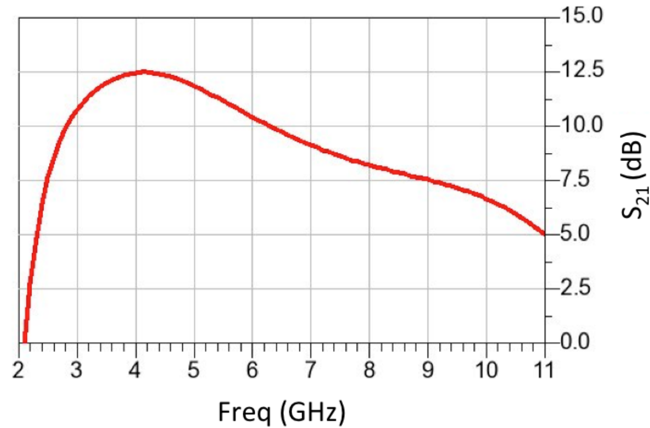

Figure 4.11: Simulated small signal gain of the output stage standalone chip -

The same analysis can be made when looking at non linear simulation results, best results are achieved between 4 and 6GHz. Indeed, 36.dBm of output power together with 52% PAE are achieved at 5GHz and they drop down to 33.5dBm and 27% at 10 GHz. The optimal input impedances between 4 and 6GHz are quite close to 50Ω, that is why this stage performs well on these frequency range when it is left unmatched.

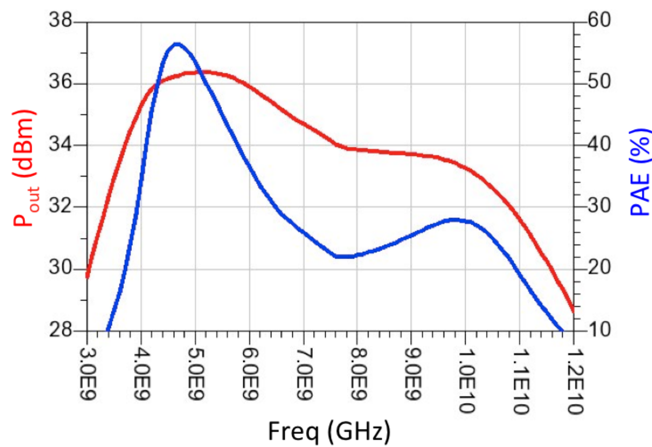

Figure 4.12: Simulated output power and PAE vs. frequency for P_in=29dBm for output stage standalone chip -

Before going into measurement results, a last simulation was performed by matching the differential input to evaluate the broadband performances of

the structure. Matching was done by adding an open stub at the input of each differential path. Results of this simulation are presented in Fig 4.13.

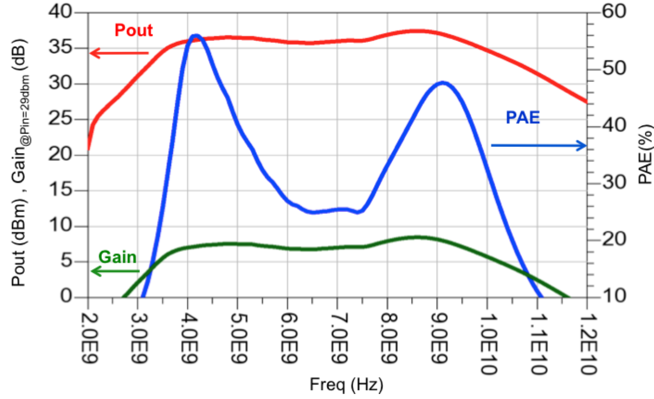

Figure 4.13: Simulated output power, PAE and gain vs. frequency for P_{in}=29dBm for output stage with a matched input -

Even though, there are some fluctuations in the efficiency behavior (from 52% at 4GHz down to 25% at 7GHz and back up to 45% at 9.5GHz), the output power stays over 35dBm from 3.5GHz till 10GHz. So, this prove the ability of such a structure to perform over a wide frequency range.

As far as linearity is concerned, both linear and non-linear studies have to be performed. Linear analysis is performed by computing the rollet factor (K-factor). To ensure stability, this factor has to remain over the unity for any frequencies. As detailed in chapter 2, this criterion is only valid for a single stage component. In fact, in the case of a multi stages amplifier, oscillations happening in a stage could be hidden by other stages as this calculation only relies on S-parameters results. So, it is not possible to claim that a multi stage amplifier is stable only by referring to the K-factor, however if K goes under the unity, then the amplifier is probably unstable. So the K-factor is a necessary but not sufficient data. The K-factor is plotted for the output power stage in Fig 4.14. We can notice that from DC to 20GHz, it remains over one, so the amplifier does not exhibit any instability behavior.

However, a deeper analysis has to be performed to ensure unconditional stability not only because the Rollet factor is not sufficient but also because stability has to be ensured for non linear mode of operation. A traditional

Figure 4.14: Rollet factor from DC to 20GHz -

way to do so is to inject short current pulses at each terminal of the amplifier (both RF and DC terminals) and to observe over a transient analysis that the amplifier gets back to a stable state once the current pulse is gone. Unfortunately, the models used in this work to design amplifiers do not come with temporal modeling , so no information could be obtained from the current pulse injection solution.

To perform the stability analysis, an harmonic mixing solution is then used. It consists in injecting a perturbation at some specific nodes (gate and drain of each transistor) and run a simulation in harmonic mixer mode. Then, the simulation results have to computed with a mathematical tool, to extract a transfer function for the device under test. From this transfer function, poles and zeros can be identified and a sufficient condition for unconditional stability is to make sure that there are no conjugate poles with a positive real part. This stability analysis is know as the Bilbao one. Fig 4.15, is an example of poles extraction after a Bilbao analysis. This example corresponds to a stable case. Indeed even though, some conjugate poles appear, they are all with negative real part (there are on the right side of the vertical line, line which separates negative real part (on the left) and positive ones (on the right)). If conjugated poles had appear within the red circle, then the device would be unstable.

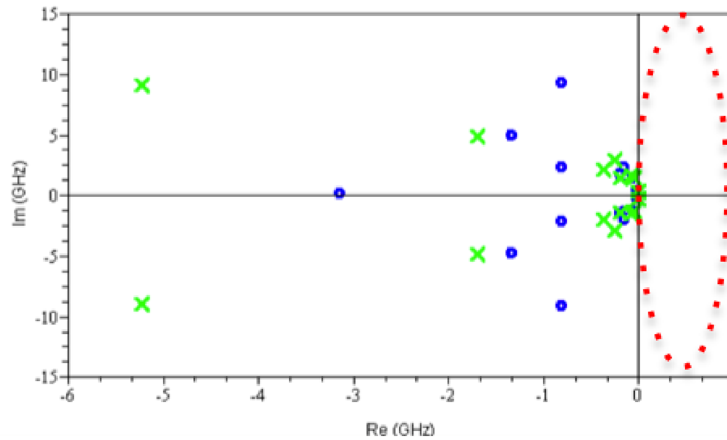

Figure 4.15: Example of a Bilbao stability analysis -

In the output power stage described in this part, the Bilbao analysis has been performed from DC to 20GHz by steps of 5 or 10 GHz in order to ensure faster and more accurate simulations. The analysis was performed at each gate and drain transistor and the main output. The results proved unconditional stability in every case computed, meaning that no conjugated poles with positive real parts were found. Some examples of these simulation results are presented in Fig 4.16, Fig 4.17 and Fig 4.18.

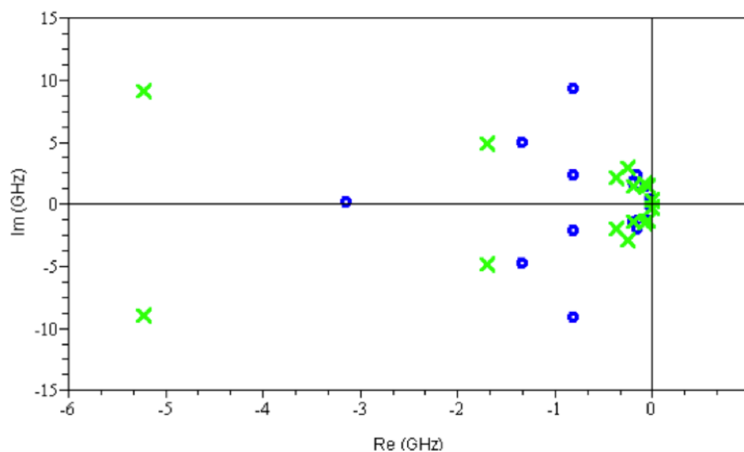

Figure 4.16: Bilbao stability analysis : DC to 10 GHz, pertubator at gate -

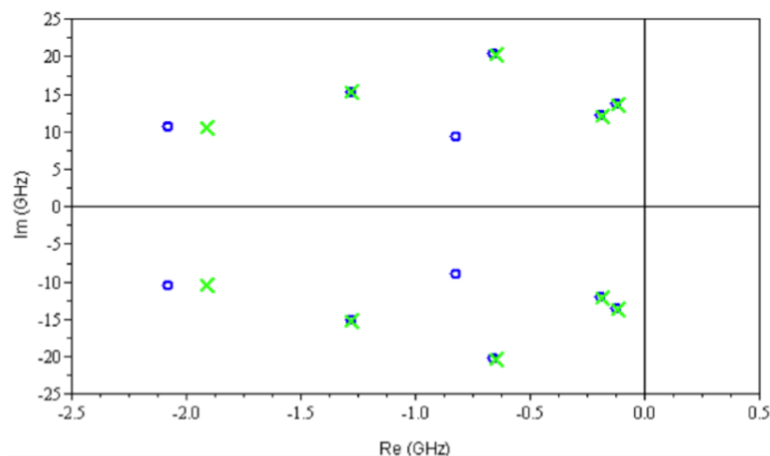

Figure 4.17: Bilbao stability analysis : 10 to 20 GHz, pertubator at drain -

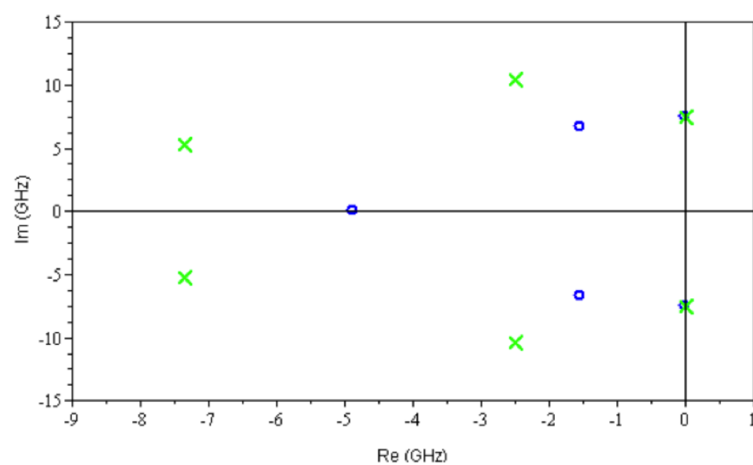

Figure 4.18: Bilbao stability analysis : 5 to 10 GHz, pertubator at output -

The realized standalone output stage is presented in Fig 4.19, its length and width are equal to 3.3mm and 1.9mm for an area of 6.27mm^2, pads included.

To perform measurements, the chip was reported on a FR4 printed circuit board. DC connections were made to the boards with wirebondings in order to add decoupling capacitors on the board to ensure stability, but RF measurements have been done under probes for better accuracy. As shown in Fig 4.20, an aluminum base was placed under the printed board to improve cooling of the die, actually an opening was made in the board for

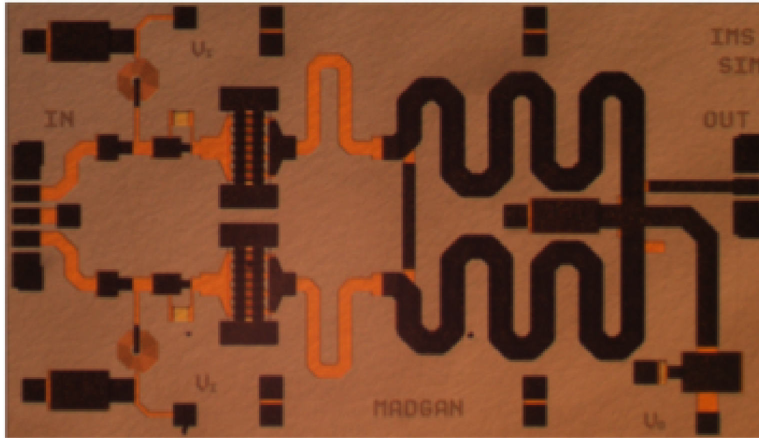

Figure 4.19: Picture of the output stage standalone chip -

the aluminum base to be glued directly to the die with a thermal conductive glue. Thanks to that, no external cooling devices were required at any time during measurements even under high input power.

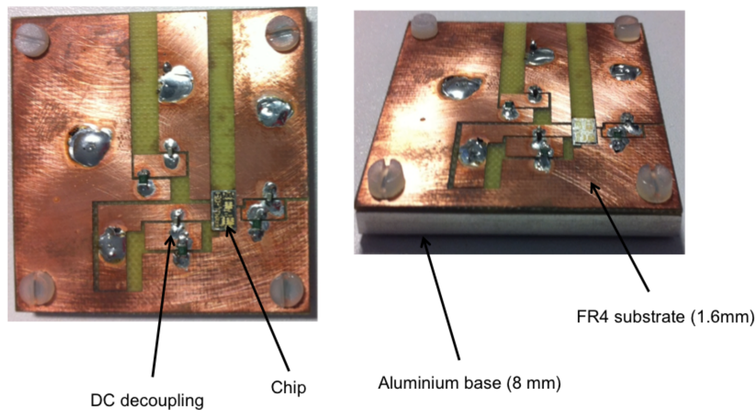

Figure 4.20: Die reported on an aluminum substrate -

Small signal measurements are plotted in Fig 4.21, the results are similar as what was observers in simulation, that is to say an optimal gain between 4 and 6GHz and thus a constant decrease till 10GHz due to the unmatched input. The gain is typically 0.5dB to 1dB lower than what expected in simulations but the behavior and shapes are similar. The results are consigned in Fig **??**.

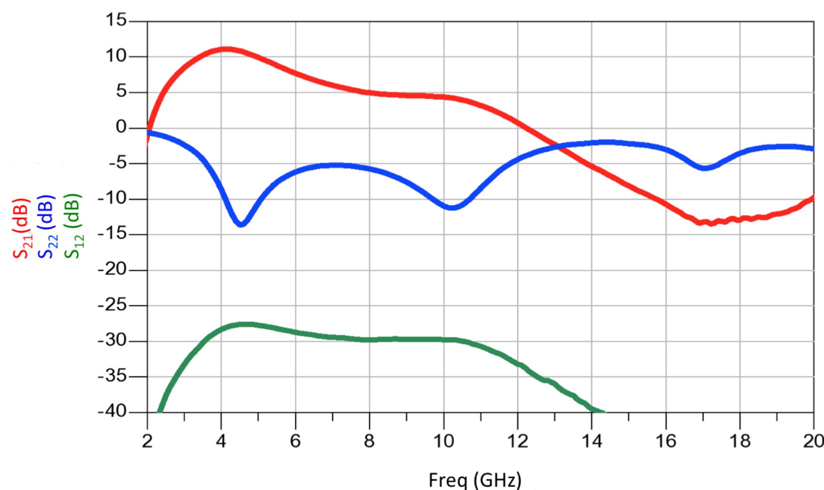

Figure 4.21: Small signal measurements for the output stage -

Then, non linear power measurements are performed for various frequency points. This setup measurement needs to be calibrated in terms of loss and compression for each frequency point, that is why it is not possible to perform a frequency sweep but only discrete points. 3 frequency points have been chosen (4GHz, 5Ghz and 6GHz) to evaluate the power behavior of this output stage. It did not make sense to perform this measurements at higher frequencies with the input unmatched. For more clarity, gain versus input power is plotted on the same graph for each frequency, something for the output power and PAE. Results are presented in Fig 4.22.

The lack of a measurement driver that can deliver enough power explains the non familiar shape of output powers and PAE plots, indeed to achieve saturation 29dBm of input power were required while our source could deliver only 27dBm. Anyway, 37dBm of output power and 47% PAE were measured at 4GHz, results in agreement with simulations.

To confirm this agreement, Fig 4.23 offers a comparison between simulations and measurements. Indeed, besides the small gain decrease (less than 0.5dB) the results match simulation pretty well and prove one more time that the balun has been well modeled and allows to achieve high PAE close to 50%. Next step is to connect this output stage to a driver and evaluate the performances of the overall HPA.

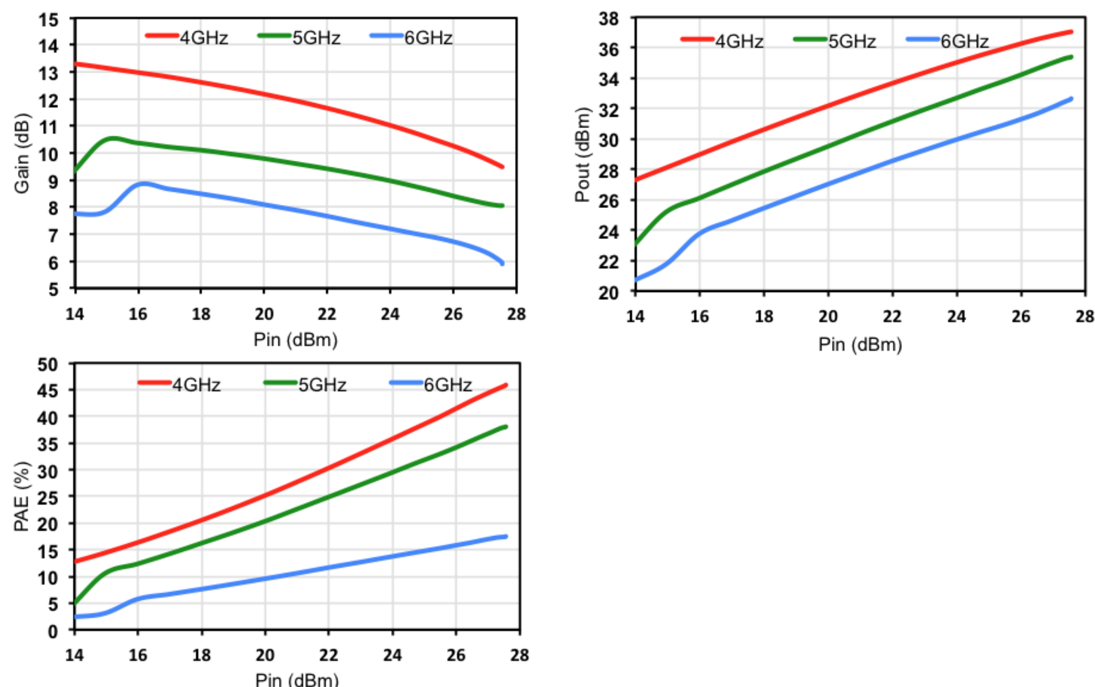

Figure 4.22: Non linear measurements for the output stage at 4GHz, 5GHz and 6GHz: Gain (top left), output power (top right) and PAE (bottom left) -

		4GHz	5GHz	6GHz
P_{out}(dBm)	sim	36.6	35.3	33.5
	meas	37	35.2	33.5
PAE(%)	sim	52	37	21
	meas	47	38	17.5
Gain(dB)	sim	8.7	8.3	6.4
	meas	9.2	7.4	6.2

Figure 4.23: Non linear measurement and simulation results comparison -

4.1.3 Input stage : active balun

In order to drive properly the output stage, an input stage delivering 26dBm to each differential path is required. That stage has to perform the single to differential conversion too. The classical way to do so, would be to use a passive balun (same as one used in the output but in splitter mode instead of combiner) and then implement the driver with common source

cells. However, in order to reduce size and increase efficiency, the goal here is to perform both tasks at once. This principle is called the active balun, meaning a balun with gain instead of insertion loss. When talking about differential amplifiers, the classical differential pair comes to mind even though such a circuit has two inputs and two outputs when we need one input only and two outputs. In the literature, various examples of a differential pair with two inputs and single output can be found such as in (19) and in (20). However, one input and differential outputs are far less common. So, in order perform the single to differential conversion with gain instead of losses, a differential pair in referenced mode will be used. Indeed one input will receive the RF signal and the second input will be grounded from the RF point of view, both sides will have the same DC bias point. Outputs will be in opposition of phase and thus generate the differential signal. The circuit topology is presented in Fig 4.24. For the same matters as the output stage, tho active balun was not matched to 50Ω in its outputs in order to be connected later directly to the output stage, that is why the results presented here do not cover the bandwidth all the way up to 10.8GHz as expected but they will once all connected together in the overall HPA.

By inputting the signal to only one input, dissymmetry in terms of both gain and phases will appear in the outputs. The design challenge is thus to decrease them as much as possible with compensation techniques. The circuit is based on transistors M2 and M3, which form the differential pair core. Theses transistors are HEMT GaN with a size of 8*125m each, they are biased with a DC current of 145 mA each. M1 is a device of 8*150m which biases the differential pair. The wideband input matching network is formed by the parallel elements C1 and L1 and by the serial capacitor C2 that acts as bypass capacitor too. Inductors L3 and L4 are chock inductors for each differential output but although contribute to the output matching networks. In the same way, capacitors C4 and C5 are used both for output matching and for bypass purpose. V_e is the single input on the gate of M2, while V_{s+} and Vs_- are the two differential outputs respectively taken on M2 and M3 drains. As mentioned earlier, the fact to input the signal

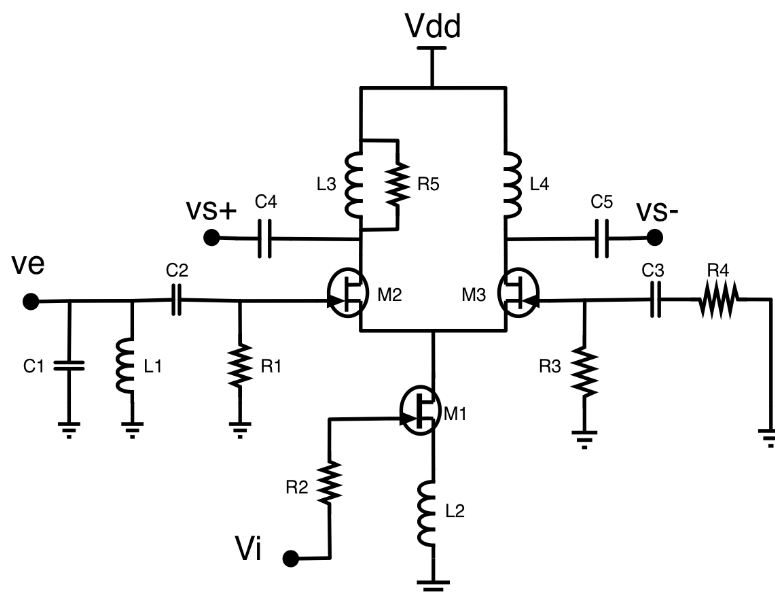

Figure 4.24: Differential pair used as an active balun -

on one side of the differential pair only is going to generate dissymetries in terms of gain and phase in between the two outputs. To compensate these dissymetries resistors R4 and R5 are introduced respectively in series on M3 gate and in parallel with choke inductor L3. These resistors aim at modifying the quality factor of C3 and L3, in order to decrease dissymetries in between the outputs.

As far as biasing is concerned, an effort was made to decrease the numbers of different voltage values. The fact that GaN HEMT transistors require negative Vgs values to function properly must be taken into consideration. Vi is the voltage applied to M1 gate; it controls the DC current level. Vi is chosen to bias M2 and M3 at the desired current value (145mA for each transistor) and to be able to impose a null voltage to M2 and M3 gates, that is to say to ground them from a DC point of view. A value of -1.8V for Vi allows to achieve these requirements, it leads in a static drain voltage of 2.7V for the transistor M1. This means that both sources of M2 and M3 have their DC voltage set to this same value of 2.7V. Then when we connect M2 and M3 gates to the ground, it results in a V_{gs} DC voltage of

-2.7V for both M2 and M3. Setting VDD to 25V, currents Ids2 and Ids3 are equal and are set with the help of the single voltage reference Vi. The value of 145mA for Ids2 and Ids3 was determined to be the best compromise between gain and power delivered to the output.

Both linear and non-linear simulations are performed to optimize this circuit performances,both as driver amplifier and as a balun. For the amplifier side, input and output matchings, alongside power delivered have to be plotted, while for the balun gain imbalance and phase difference between the outputs are two highly important criteria. Linear and non-linear simulation results are presented in two different parts in this section.

S-parameters simulation is performed to ensure proper input and output matching along with linear stability. The convention that S_{11} correspond to the input Ve and that S_{22} and S_{33} respectively correspond to the outputs Vs+ and Vs- is taken in the following. S_{11} remains under -10dB in the [2.5GHz - 6GHz] band as shown in Fig 4.25. This demonstrates that matching network formed by C1, L1 and C2 has wideband capabilities. In the output side, a difference between S_{22} and S_{33} is observed. Even if both curves have the same shape, S_{22} remains at a much lower value than S_{33} for every frequency over 3GHz.

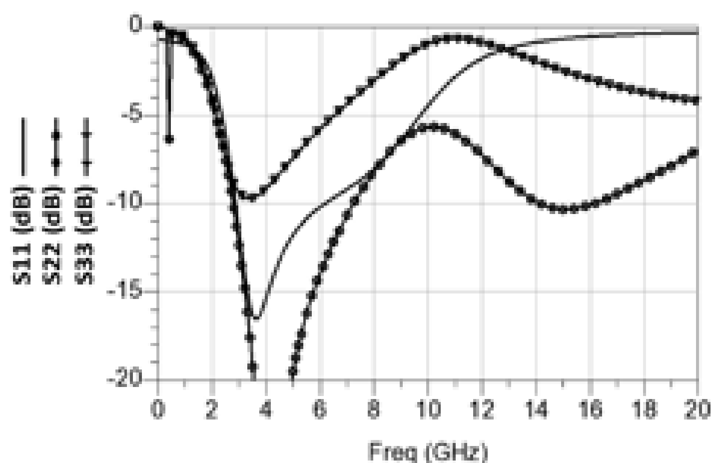

Figure 4.25: Input and outputs matching -

This difference can be explained by the fact that an effort has been made

to equalize the two outputs in terms of power behavior more than in terms of linear mode of operation. In other words, the matching performed is a power matching and not one to the conjugate as it is normally done to improve small signal gain. Fig 4.26 is a plot of the phase difference between the outputs Vs+ and Vs-. In the frequency band of interest, the phase difference goes from 189@2.5GHz to 175@6GHz. This leads to a maximal error of 5.5% compared to 180°.

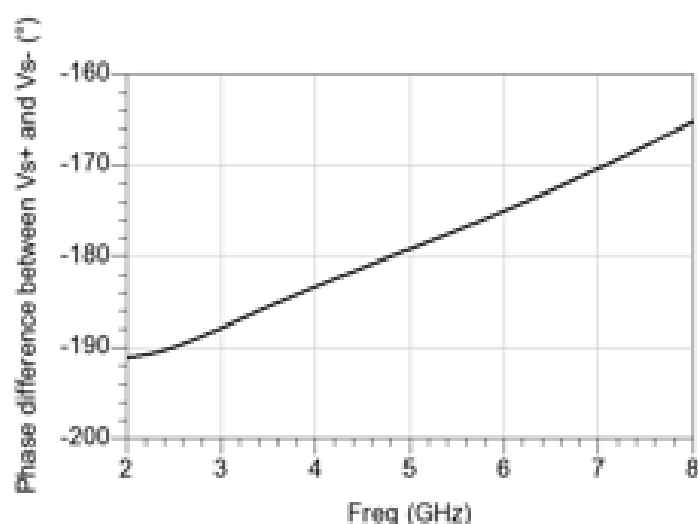

Figure 4.26: Phase difference between the differential outputs -

To evaluate power performances and non-linear behavior, harmonic balance simulations are performed. Both wideband and high power aspects have to be considered here. That is why, firstly a frequency sweep with a fixed input power level has to be performed and then a power sweep at a fixed frequency in the middle of the frequency band is simulated. Fig 4.27 represents the output power delivered to each of the differential output for frequencies from 2GHz to 8GHz with an input power level constant at 20dBm. In the [2.4GHz-6GHz] frequency band, each output delivers more than 25dBm with a peak of 27.4dBm@3.8GHz. The power imbalance in between the two outputs varies from 0dB to 0.4dB in the [2.4GHz-6GHz] frequency band.

Both output voltage waveforms are plotted in Fig 4.28, two periods are represented, which gives access to both amplitude and phase information.

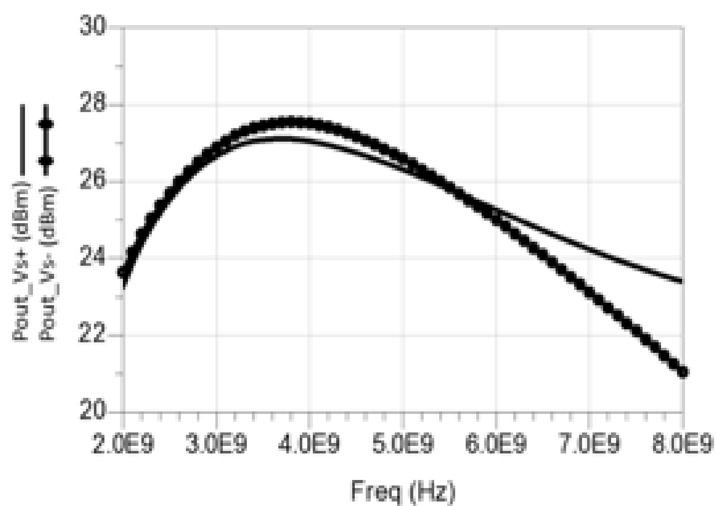

Figure 4.27: Output power vs. frequency for each output path at P$_{in}$=20dBm -

First thing to notice is that differential outputs are out of phase. To be accurate the maximal time difference experienced between when one output reaches is the maximal value and the other one is minimal value is of 3.2ps. Considering the fact that a frequency of 3.8GHz corresponds to a period of 263ps, this time difference represents a phase mismatch of 4.4°.

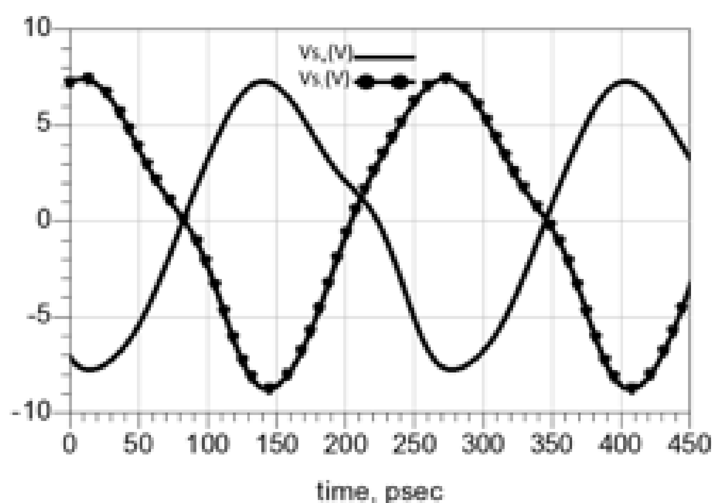

Figure 4.28: Output voltage waveforms at 3.8GHz -

In terms of amplitude, one output has an excursion of 15V when the second

one reaches 16.1V. This corresponds to 6.8% of relative error in between the outputs. Fig 4.29 is a power sweep performed at 3.8GHz, a frequency where best performances are achieved. Both outputs (Vs+ and Vs-) are represented versus input power. An output power of respectively 29.1dBm and 29.6dBm for both outputs is observed for an input of 25dBm, this results in a differential output power (sum of the output power delivered to each path) of 32.4dBm and thus in a differential gain of 7.4dB. These values confirm the great interest of this circuit topology that realizes the single to differential conversion and has power gain at the same time making it very reliable to act as a driver amplifier for a differential power stage.

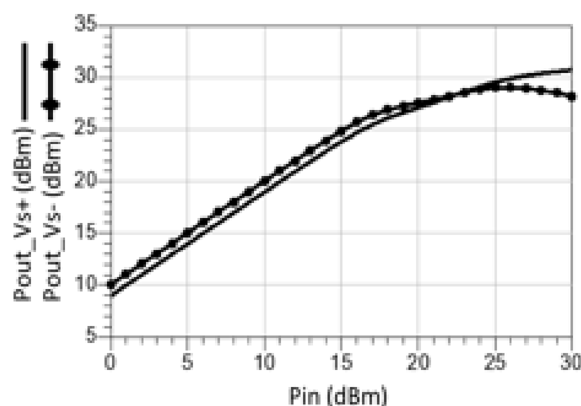

Figure 4.29: Output power vs. input power at 3.8GHz -

Taking a look at mismatch between the two power paths in Fig 4.29, a very good correlation is obtained for an input power between 18dBm and 25dBm with a power imbalance lower than 0.2dB. From 0dBm to 17dBm of input power, an almost constant imbalance of 0.9dB is observed while power paths diverge for an input power of 25dBm. Due to the strong changes in the transistor behavior, which goes from linear to highly non-linear through the power sweep, the compensation technique presented earlier has been designed to be the most efficient for an input power around 20dBm, which is proven by values enounced earlier.

Unfortunately due to an issue during the circuit fabrication, some resistors went missing so open circuits were present instead of them, making impossi-

ble this circuit to be measured to confirm the simulations results. However, the layout of this design is presented in Fig 4.30, its length and width are 2.5mm and 1.4mm for an overall area of 3.5mm^2.

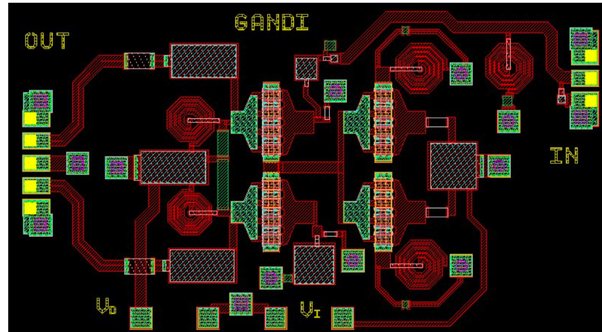

Figure 4.30: Active balun layout view -

With these two stages designed and characterized, simulations of the full HPA can now be performed to evaluate overall performances and try to match the specifications expressed at the beginning of this section.

4.1.4 Overall HPA Architecture

Both the input active balun and the output power stages have been designed separately as described in the previous sections but from the very beginning they have been meant to be connected to each other. With the issue explained about the active balun realization, this combination will not be possible for measurements but it can still be done by simulation. The proposed architecture is presented in Fig 4.31.

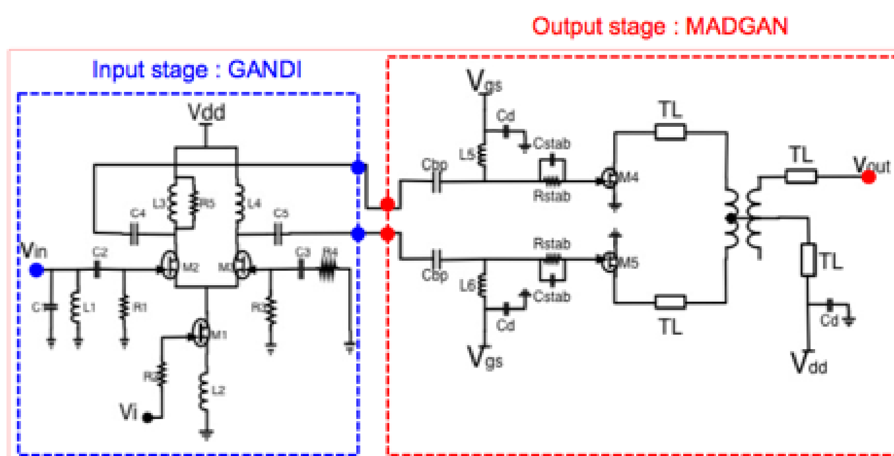

Figure 4.31: Architecture proposed for the overall HPA -

As shown in the previous section, the active balun delivers two signals in opposition of phase to drive the power cells which are then combined out of phase in the stacked balun to result in a single output where both power paths are summed.

It results in an HPA with single input and single output both matched to 50Ω. The interstage matching was not any troubles because both stages have been designing to match each other in order to optimize power transfer from the driver to the output stage. The choice of implementing in the same circuit the driver and the single to differential conversion permits to drastically reduce the overall size. Moreover, the use of the stacked balun as an output power combiner helps reducing size too while keeping the efficiency to a very acceptable value. Even though, layout of the overall HPA has

not been realized because no tapeouts was foreseen for it, based on the size of the two individuals blocks the overall size of the HPA should be around $12mm^2$ including both RF and DC pads. The overall DC consumption is equal 305mA under 25V.

The small signal gain is presented in Fig 4.34, it stays 22.5dB from 3.5GHz to 10.5GHz and reaches a maximum of 28.1dB at 4.5GHz. The overall bandwidth specified [2.GHz - 10.8GHz] is not exactly respected due to the stacked balun combiner cut-off frequencies but he wideband behavior claimed in the previous sections is demonstrated by this plot. The pick of gain appears in low side of the frequency range while it was specified that the output power should increase in the last part of the range. Non linear results will exhibit that the output power actually increase at the end of the band, indeed the HPA has been optimized to work best under compression and not in its small signal behavior and the optimal impedances differ for these two cases. That's why in small signal the gain is higher around 5GHz instead of 10GHz as it would be in the high input power mode.

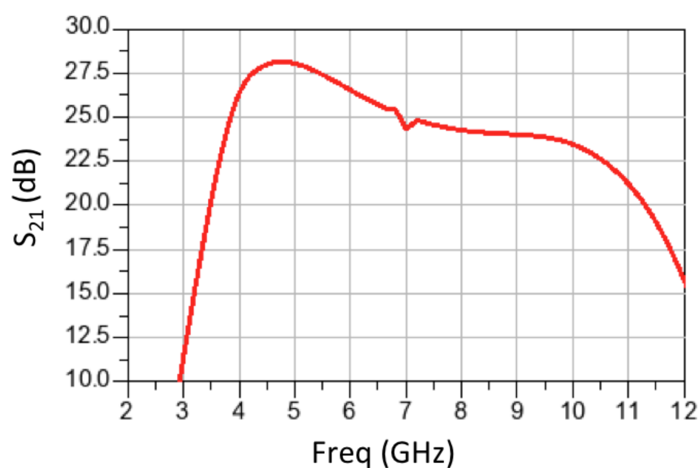

Figure 4.32: Full HPA small signal gain -

Non linear simulations performed with an input power of 22dBm permit to evaluate the output power, efficiency and associated gain performances of the HPA versus frequency. Output power is plotted in Fig 4.33, a maximum of 38.2dBm is reached at 10GHz at it stays over 35dBm from 4GHz to

10.8GHz as specified. The output power ripple is about 1.2dB all over the band. This ripple was way greater (around 3.5dB) in small signal behavior, but thanks to compression phenomenon not only the gain is reduced but so is the ripple when in high input power mode. Indeed, the associated gain for an input power of 22dBm is presented in Fig 4.34. It reaches a maximum of 16dB at 10.5GHz and does not go under 15 dB from 4 to 10.8 GHz, the ripple being lower than 1dB all over the band.

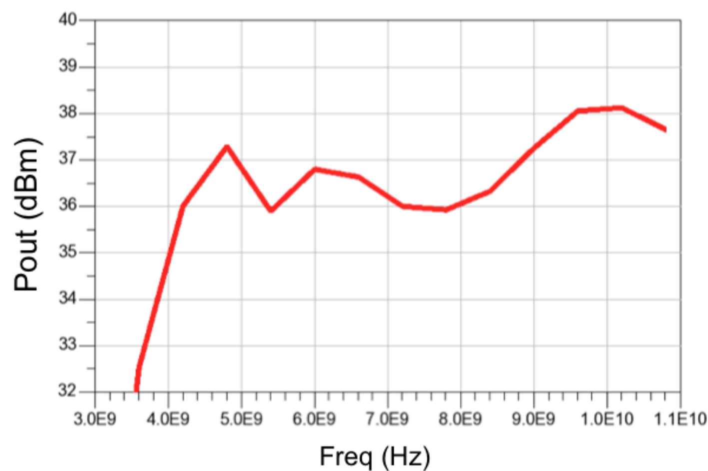

Figure 4.33: Full HPA output power vs. frequency for P_{in}=22dBm -

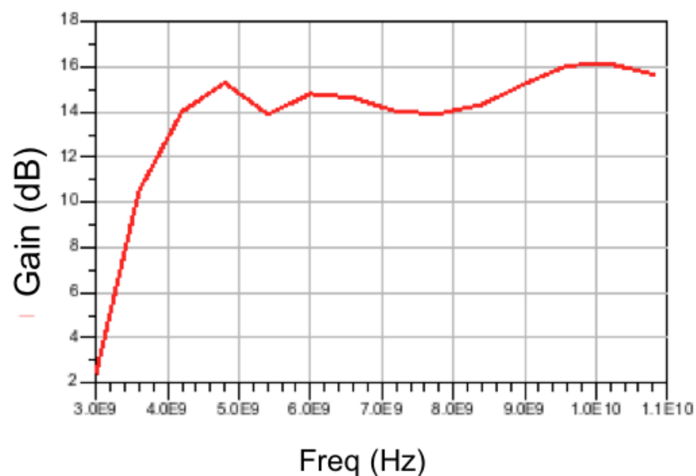

Figure 4.34: Full HPA gain vs. frequency for P_{in}=22dBm -

Last parameter to plot is the PAE for the overall HPA with an input power

of 22dBm too as shown in Fig 4.35. A maximum of 32% is obtained at 10.5GHz and from to 10.5GHz it averages 26% and the worst case reached at 7.5GHz is equal to 18%. The fact that the PAE fluctuates more than the other parameters is explained by the fact that efficiency is very sensitive to impedances mismatch, thus it is very difficult to maintain a flat PAE when working over wide frequency ranges. Moreover, the second and third harmonics impedances have a large impact on PAE behavior has detailed in (21), so this becomes even tougher to manage when working with a frequency range so wide that the 2nd harmonic of the beginning of the band actually corresponds to the first harmonic in the end of the band.

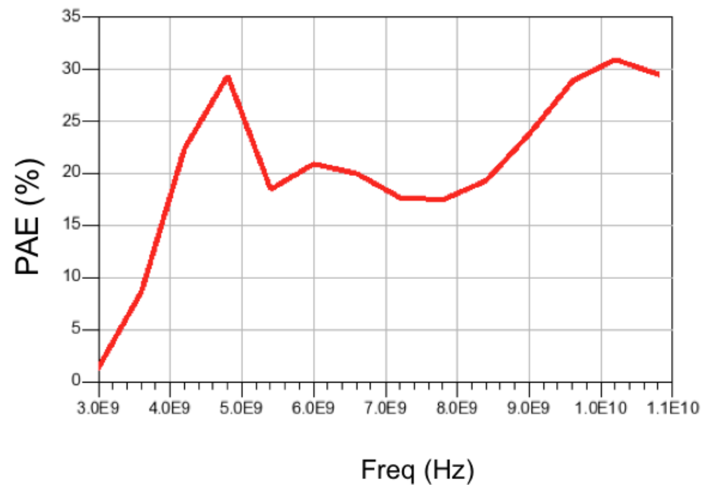

Figure 4.35: Full HPA PAE vs. frequency for P$_{in}$=22dBm -

Fig 4.36 reminds the performances of this full HPA both for linear and non linear behavior. As expected in the specifications, there is an increase in terms of output power and efficiency in the end of the frequency range. The output power condition is achieved expect in the very first part of the band (from 2.8GHz to 3.5GHz) but the PAE does not quite match the specifications but still remains at very convenable values when comparing to the state of art presented at the end of chapter 2. Moreover, based on estimations this HPA would fit within an area of 12mm^2 making it very compact, which proves the benefits of both the stacked structure and the active balun.

Freq (GHz)	**4 – 9.8**	**9.8 – 10.8**
Linear Gain (dB)	25 ±1.3	22.8 ±1
$Gain_{@Pin=22dBm}$ (dB)	14.8 ±1.2	15.8 ±0.2
Output $Power_{@Pin=22dBm}$ (dBm)	37±1.2	38 ±0.2
$PAE_{@Pin=22dBm}$ (%)	24 ±6	31 ±1

Figure 4.36: Full HPA performances -

4.2 X to Ku-band traveling wave amplifier

4.2.1 Specifications

For this second realization, our goals was to design a wideband amplifier going as high in frequency as the UMS GH25 allows to. As a reminder, the f_t of the active devices is around 25GHz, so trying to cover a range going all the way up to the end of K_u band (18GHz) seems quite challenging but plausible with a proper design methodology. This HPA design is part of a bigger system patented by THALES SA that can not be discussed here for confidentiality matters. Anyway, the specifications for the HPA are presented in Table 4.2.

Bandwidth (GHz)	8 - 18
Linear gain (dB)	12
P_{sat} (dBm)	38
PAE (%)	>20
Conditions	CW @ 80°C
Die size (mm^2)	20
Technology	GaN GH25 (UMS)

Table 4.2: X to K_u band HPA specifications

The objective in terms of bandwidth is to cover both X and K_u band from end to beginning (8GHz to 18GHz) with an output power greater than 38dBm at any time. The specification in PAE can appear quite relaxed (greater than 20%) but it is still going to be a challenge in the end of the frequency range when the active devices intrinsic gain is getting quite small. Moreover, a special attention has to be made to keep the PAE frequency response as flat possible.

According to discussions made on chapter 2, the traveling wave amplifier approach (TWA) seems to be a very good candidate both to achieve extra large bandwidth and flat response. However, TWA are not the best architecture in terms of gain and ability to deliver power, so the solution proposed

consists in parallelizing two standalone TWA to increase the output power as detailed in the following sections.

4.2.2 Design methodology

To cover both bandwidths and output power specifications, a single TWA is not going to be enough so it is decided two combine two elementary TWA to sum their power up in order to obtain 38dBm of output power from X to Ku band. Indeed as detailed in the previous HPA realization, unitary cells can highly deliver more than 35dm. By doing so, the constraint on output power is relaxed for the standalone TWA and thus bandwidths and efficiency requirements can be achieved more easily. A good candidate to act both as power combiner and splitter is the X to Ku band stacked balun presented in section 3.3. As mentioned in this section, baluns can achieve best bandwidth performances when their transformation ratio is equal to one, which means that if the single side of the balun is loaded by 50Ω, it would work best with each of his differential outputs loaded by 25Ω. Base on these considerations, the design methodology proposed in Fig 4.37 should lead to interesting results.

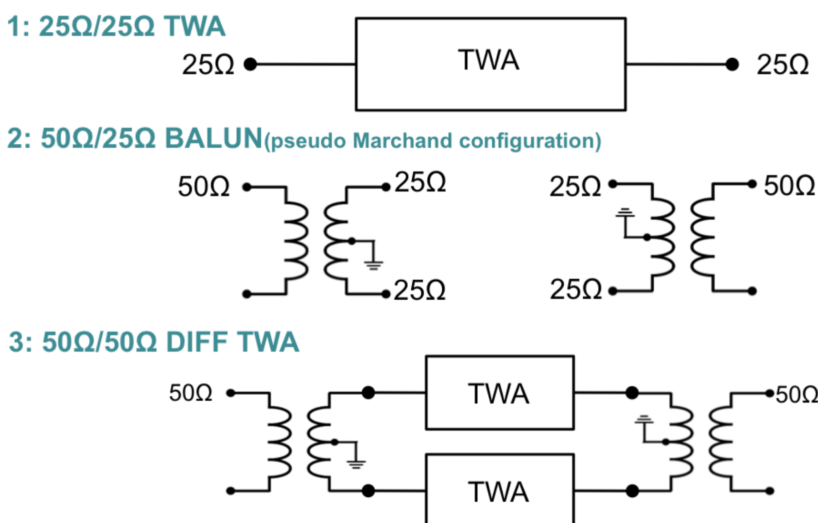

Figure 4.37: Differential TWA design methodology -

Each step of this approach is detailed in the following:

* **25Ω/25Ω TWA**: design of the elementary standalone TWA matched to 25Ω both in its input and output.
* **50Ω/25Ω balun**: design of the balun for use as power splitter and combiner. This step was already done in section 3.2, the same can be used for combining and splitting functions.
* **50Ω/50Ω differentialWA**: combination of the two elementary TWAs thanks to the stacked balun to double output power and still have an overall chip with single input and single output.

Not only it is advantageous to design the TWA with 25Ω terminations for combination matters as explained previously, but it is also good in terms of the elementary TWA performances. indeed in this frequency range, optimal impedances for the active devices in terms of efficiency and output power are way lower than 50Ω so the matching process is going to be either and with less loss at 25Ω than it would be at 50Ω.

In the next section, the design of the elementary TWA is detailed and the optimizations performed are explained.

4.2.3 25 Ohms / 25 Ohms single TWA

As detailed in chapter 2, a TWA can be seen as two lines (an input one and an output one) actively coupled by active cells, which results in an amplification of the signal going through the input line, the amplified signal being obtained at the end of the output line. TWAs are known to be the best architecture to achieve large bandwidths with a very flat gain. However, when gain flatness is not crucial for the application, improvements can be made to the structure to maximize output power and efficiency instead, these improvements are being discussed in this section. A classical TWA is presented from a schematic point of view in Fig 4.38.

In a conventional TWA (or uniform TWA), all cells are the same, all input transmission lines in between cells (Lg1..L_{gn}) have same width and length, same thing applies for output lines (L_{d1}..L_{dn}) and both input and output lines should be terminated by a resistor with a value of 25Ω in our case

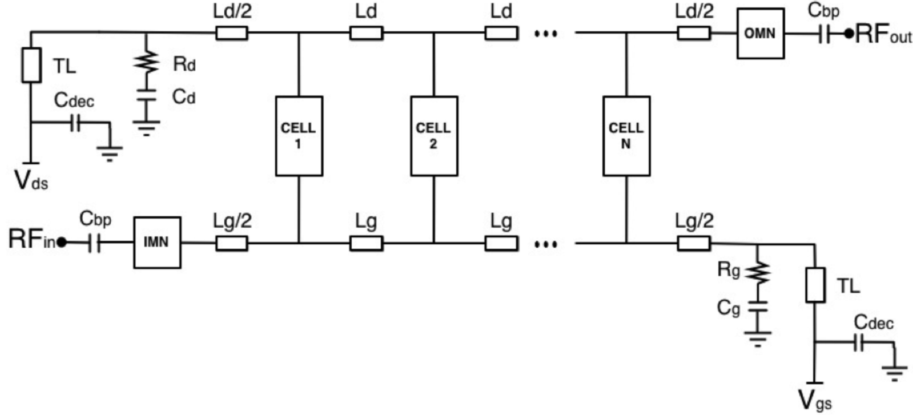

Figure 4.38: Schematical representation of a TWA -

(would be 50Ω for a conventional TWA). If these conditions are met then the amplifier is optimized in terms of small-signal gain and gain flatness as detailed in (22). However, as described in (23) when trying to optimize the TWA in terms of output power and PAE, non-uniform topologies should be concerned. This approach consists in increasing transistor sizes in cells close to the output and changing size of transmission lines in order for each cell to see its optimal impedance in terms of output power and PAE.

An efficient way to perform the design, is to start with an uniform architecture in a first time in order to optimize the number of cells and the topology of the cells too. Even though, cascode structures are often used with low breakdown voltage devices, in the case of GaN a simple common source cell is enough such as Fig 4.39. R_{stab} and C_{stab} act as an high pass filter to reduce the low frequency gain and prevent from instability.

Number of cells and total gate width development would strongly affect the frequency response and the gain of the TWA. Basically, a large number of cells results in high gain but small bandwidth and vice versa. This phenomenon is well illustrated in Fig 4.40 that can be found in (24). This phenomenon is due to the fact that each time one cell is added a low pass LC networked (formed by the connection line and the input capacitance of the active device) is introduced. All of these low pass networks adds up and

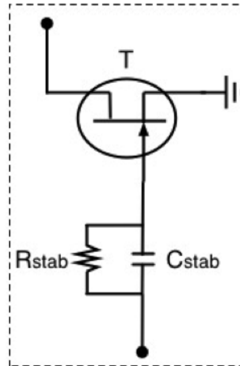

Figure 4.39: Common source cell -

at some point the global cut-off frequency of the overall access line limits the amplifier bandwidth.

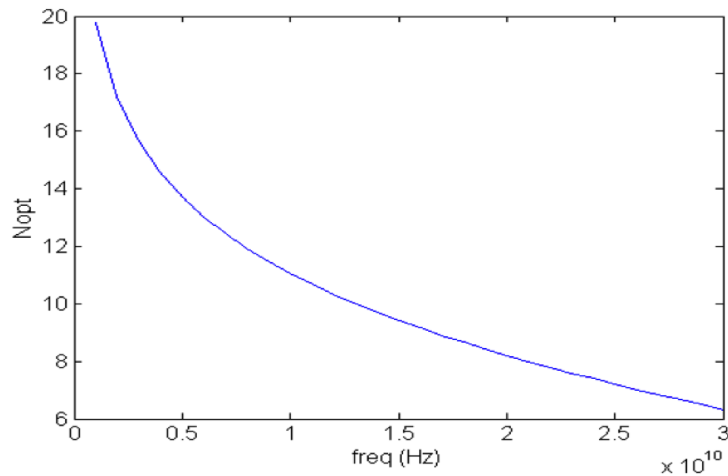

Figure 4.40: Optimal number of cells vs. maximal frequency of operation -

Fig 4.41 illustrates the low pass filters introduced each time a new cell is added. On the input side the low pass filter is created by the couple (L_g,C_{gs}) while on the output side it comes from L_d,C_{ds})

Another interesting graph to look at is Fig 4.42, that can also be found in (24). It makes a link between gain, number of cells and bandwidth. As in the previous plot, it appears that increasing the number cells ends to bandwidth reduction. On the contrary, it has the advantage to increase the

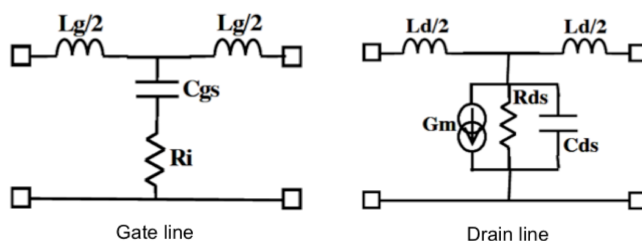

Figure 4.41: Low pass filters introduced by cells connection -

gain within the bandwidth. A special has to be made when choosing the number of cells with regards to the frequency range and the gain targeted, a tradeoff would have to be made either way.

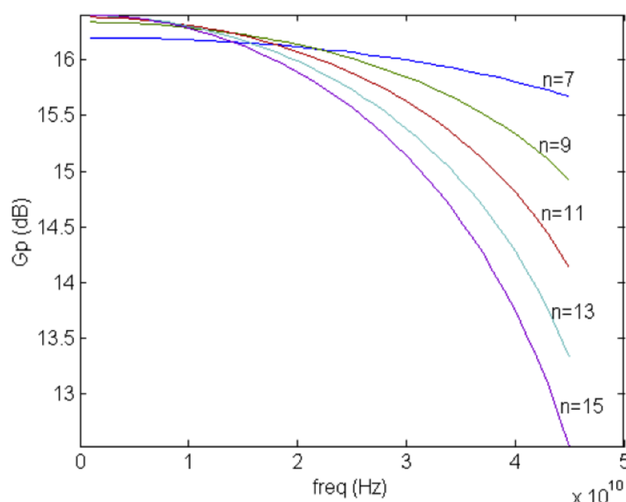

Figure 4.42: Power gain vs. frequency for various number of cells -

To confirm these theoretical principles, simulations are performed based on the schematic introduced in Fig 4.38. To start with, the unitary comm source cell is implemented with a 4*100μm device. All cells are biased at 20V and 120mA/mm. Bot small signal gain and output power are plotted in Fig 4.43 for 5,8 and 11 cells.

The small signal gain is in average 2dB higher from 4 to 18GHz with 11 cells instead of 5 but with 11 cells this gain start to decrease at 17GHz. However, this cutoff phenomenon does not happen when looking at the output power plots. Indeed, there is always a difference in frequency cutoff between small

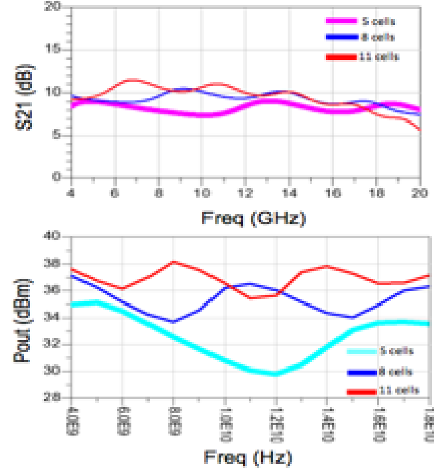

Figure 4.43: Number of cells optimization in function of gain, output power and bandwidth -

and large signal behavior due to the compression phenomenon. So, 11 cells seems to be the maximum number of cells possible to reach the upper frequency limit of 18GHz.

In a conventional architecture (Fig 4.38), each transmission line is terminated by a resistor (R_g and R_d) with a value equal to the characteristic impedance of the transmission line in order to ensure constant phase speeds in the line for proper recombination and thus flat gain all over the frequency range. However, with the objective in mind to maximize the overall output power, it appears obvious to remove the output line termination resistor (R_d) so no power is dissipated through it and all of the power is going through the main output. This would results in more gain ripple but once again what matters here is the output power. More information on that specific topic can be found in (9)

Instead of using similar cells and transmission lines all over the TWA, it is possible to increase the transistor size of the last cells to increase output power and change the geometry of the lines too. Indeed, by increasing transistor sizes, more current can flow through them and so they can deliver more power to the output load. Moreover,the optimal impedance of the structure decreases when getting closer to the output termination, so the

last transmission lines should have their width increase to counterbalance this phenomenon.

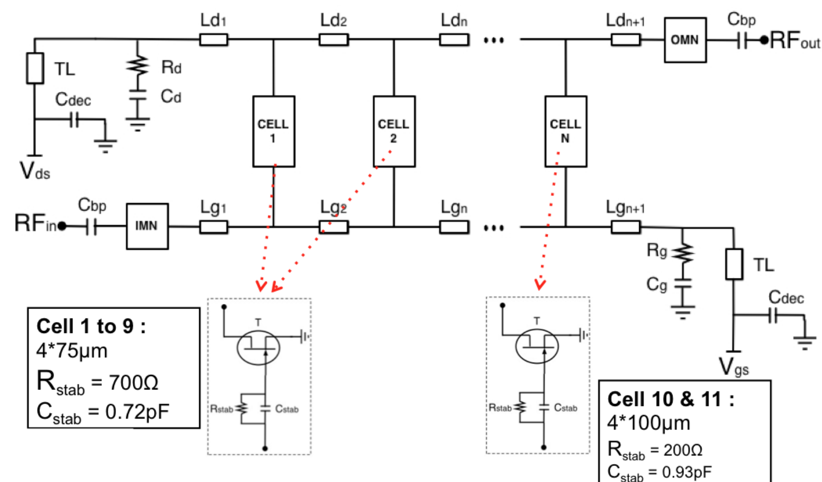

Figure 4.44: Selected architecture for the single TWA -

Based on all of these previous discussions, the choice of a non uniform architecture with eleven cells is made without a drain termination resistor. Cells 1 to 9 are made of 4*75μm devices while cells 10 and 11 are made with 4*100μm transistors. Each segment of line has been optimized with the help of Agilent ADS simulator and parametric analysis. Referring to Fig 4.38, IMN and OMN are matching networks to get the input and output impedances as close as possible to 25Ω. The selected architecture is presented in Fig 4.44.

Small signal simulation results for this single architecture are presented in Fig 4.45. The gain averages 13.2dB from 8 to 18GHz with a gain ripple of 0.7dB. The output reflection coefficient S_{22} remains under -13dB all over the range while the input one S_{11} is only under -5dB.

Non linear simulations resulted are presented in Fig 4.46 versus frequency for an input power of 30dBm. In average the output power and the PAE are respectively equal to 37.3dBm and 18.8% with maximal values of 38dBm and 24% respectively at 11GHz and 14.8GHz.

So the elementary 25Ω / 25Ω TWA is designed and characterized in order

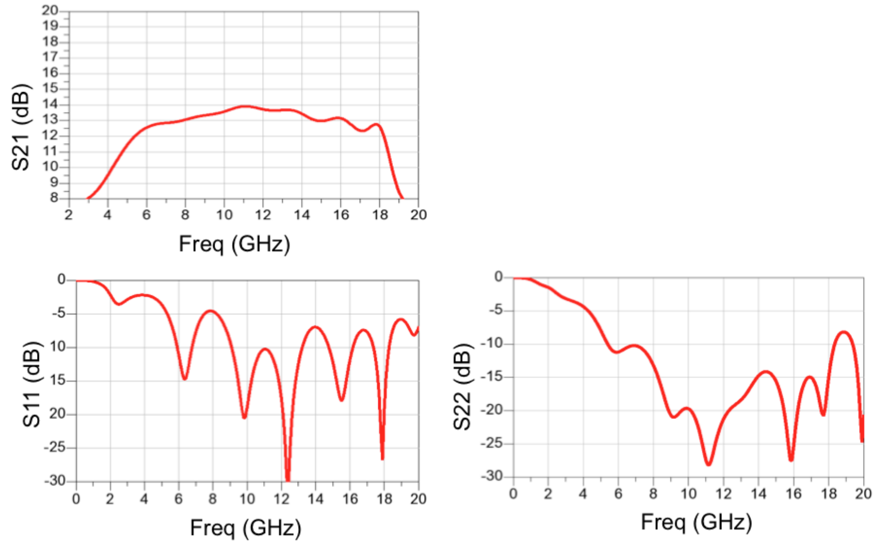

Figure 4.45: Small signal simulation for the single TWA -

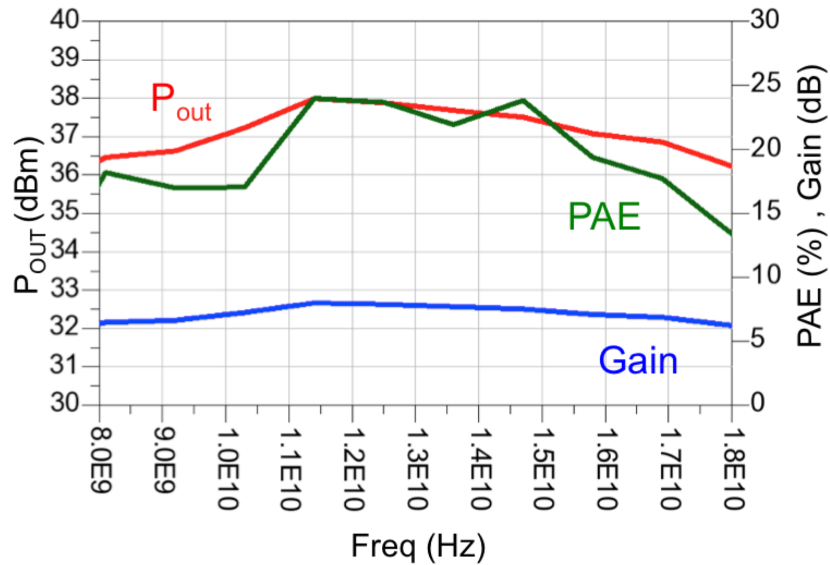

Figure 4.46: Large signal simulation results for the single TWA at P_{in}=30dBm -

to be used as building block for the overall amplifier. However, a last simulation result is presented in this section, it consists in sweeping the drain voltage and see its effect on output power and PAE. Results are presented in Fig 4.47. Increasing the drain voltage results in an increased output power

but a reduced PAE, so it is decided to keep the drain voltage at 20V as the PAE obtained is already lower than the one specified while the output power should easily achieve what was targeted after power combination.

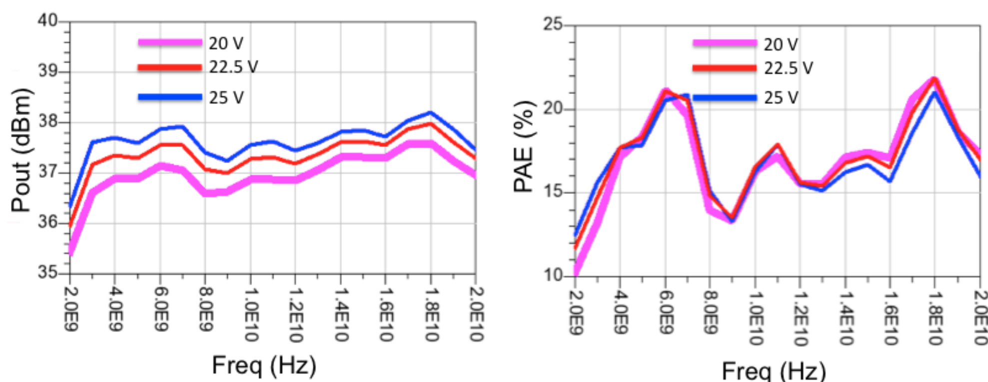

Figure 4.47: Output power and PAE for various drain voltage -

4.2.4 50 Ohms / 50 Ohms differential TWA

With the two main building blocks already designed, that is to say power combiners and splitters and the single 25Ω TWA, this last step only consists in connecting the elements together and perform simulations to ensure proper behavior and that the targeted specifications are met. The implementation is done as shown in Fig 4.48. It is important to note that as opposes in the previous HPA designed, this time the balun mid points were not used to feed supply and bias to the elementary TWAs. Indeed, for proper operation, it is mandatory that the TWA are biased and supplied through the transmission lines ends.

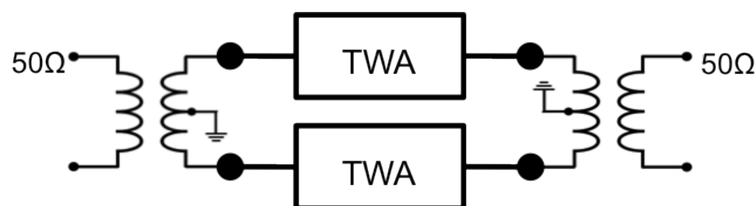

Figure 4.48: Differential TWA representation -

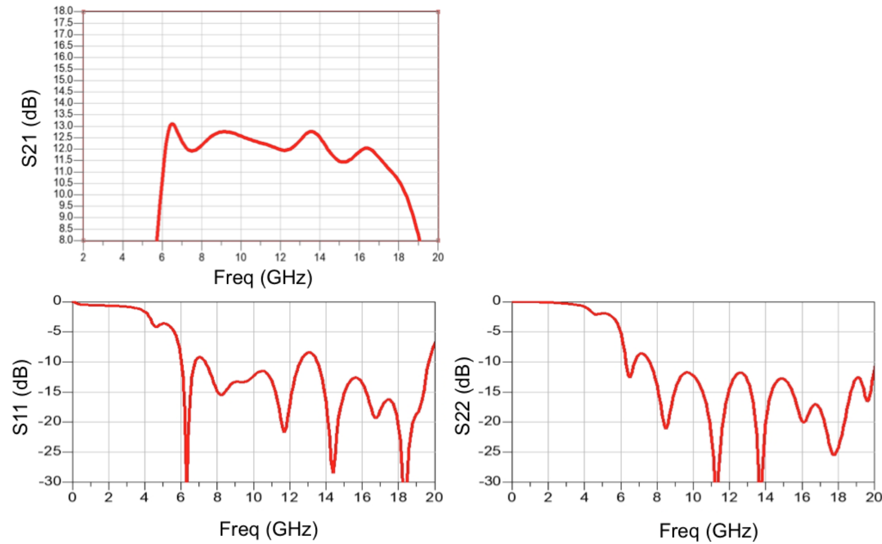

Figure 4.49: Small signal simulation results the differential TWA -

Small signal simulation results for the overall differential TWA are presented in Fig 4.49. Small signal gain is over 12.2 dB from 8GHz to 18GHz and reaches a peak value of 14.1dB at 13GHz. Gain ripple is close to 2dB, as explained before circuit has been optimized in terms of power and not gain flatness and this not a big issue because the gain is going to be flatten when under compression with an high level input signal. Both input and output reflection coefficients have a wideband behavior and acceptable values, indeed S_{11} remains under -8dB from 8 to 18GHz while S_{22} is under -12 dB. Even more , the small signal gain is still over 12dB down to 6GHz so the bandwidth is extended when considering small signal only.

Fig 4.50 presents the non linear simulation results. For an input power of 33dBm, the output power averages 39.7dBm all over the band and reaches a maximum of 40.4dBm at 11GHz. The PAE is 18.5% in average and reaches a peak value of 22%. The associated gain is around 6.6dB in average with a ripple of 0.7dB. Once again, we can notice the difference of 5.5dB between the linear again and the gain at PAE max, a phenomenon typical of GaN based devices.

All of the results are summarized in Table 4.49. All of the specifications

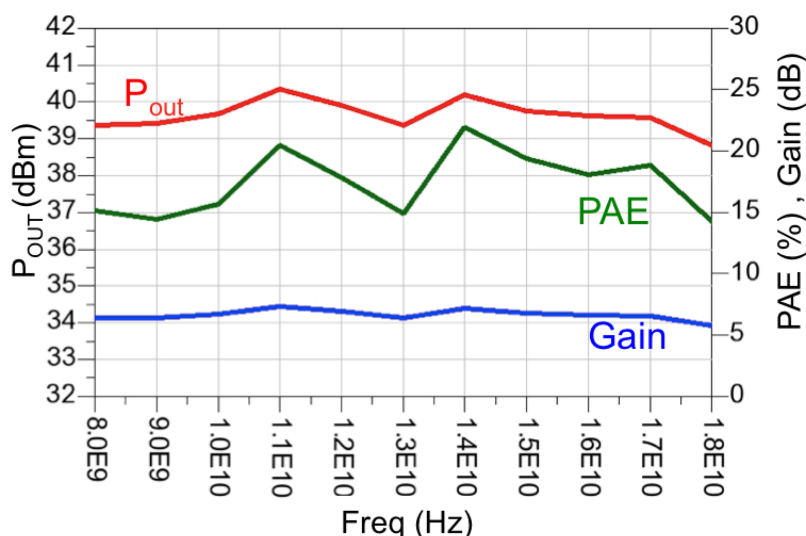

Figure 4.50: Large signal simulation results for the single TWA at P_{in}=33dBm -

exposed in the beginning of this section are achieved besides PAE which slightly lower than what was expected (18.5% in average instead of 20%), but the output power delivered and the compact size somehow compensate for this lack.

Bandwidth (GHz)	8 - 18
Linear gain (dB)	11.7 - 13.1
P_{sat} (dBm)	39 - 40.3
PAE (%)	15 -22
Die size (mm^2)	15

Table 4.3: Differential TWA performances

Even though it could not be completed to the end due to lack of time and need to work on other projects and as no tapeout could have been scheduled for this realization, the layout of this differential TWA was realized to estimate its overall size. The layout is presented in Fig 4.51, only thing missing is some of the output drain lines between the cells.However, both combiners and splitters have been implemented and EM simulated as same as the input lines. A special attention was made with the input lines EM

simulations as the lines of the two elementary TWA get close to each other, it was necessary to make sure coupling between these two lines will not affect the amplifier behavior. The overall estimated dimensions are 6mm in length and 2.5mm in width resulting in an area of 15mm^2 including DC and RF pads.

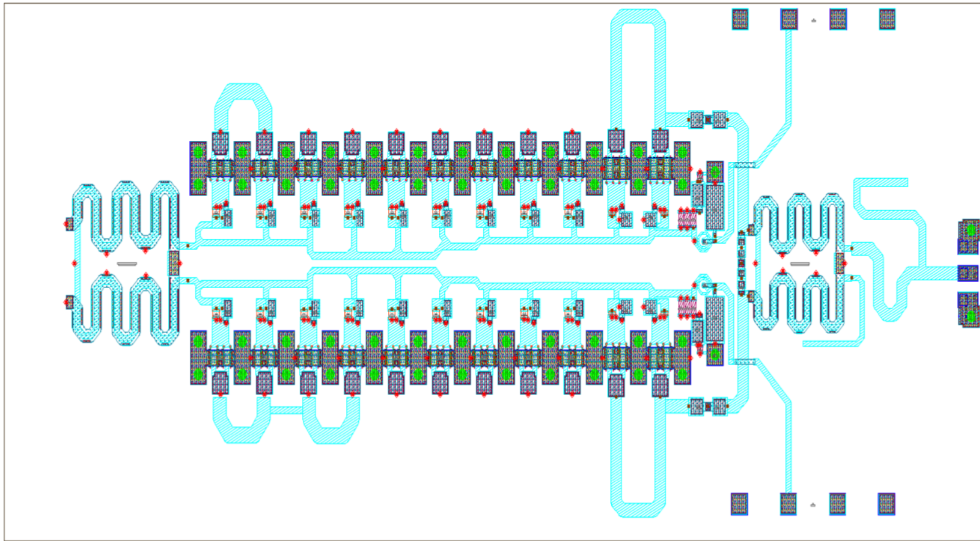

Figure 4.51: TWA partial layout -

Fig 4.52 compares this realization with circuits reported in the literature. In terms of output power, our realization is definitively not the best one, indeed some have reported output power greater than 20W ((9)) but at the cost of a very large size (38.25mm^2). Our objective was to end up with a compact solution instead of the most powerful one, and this can be considered as a success because this realization is only 15mm^2.

Based on this architecture, it can be said that they are a great approach to achieve very large bandwidths. With proper optimization, they can easily compete with other structures in terms of output power and power density in this case thanks to the area gained by using the stacked balun transformers. On the down side, they are certainly can be overcome in terms of efficiency by more classical structures, so they should be used only when bandwidth is main criteria.

REF	Techno	Freq (GHz)	Vdc (V)	Idc (A)	Pout (dBm)	G (dB)	PAE (%)	Architecture	Surface (mm^2)
[KOM11]	AlGaN/GaN HEMT 0.20µm	2 -20	30	NA	Max@OCP3 :43,3 Average@OCP3 : 42	Max : 11,1 Average : 9,7	Max : 35,7 Average : 26	Balanced Non Uniform Distributed	38,25
[REE10]	AlGaN/GaN HEMT 0.25µm	2 -20	35	NA	Max @4GHz : 41,5 > 40	12	Min : 24 Average : 28	Non Uniform Distributed	NA
[CAM08]	AlGaN/GaN FET-DFP 0.25µm	1,5 - 17	35	NA	Max@5GHz : 41 > 39	> 10	Max : 38 > 20	Non Uniform Distributed	15,3
[MAS10]	AlGaN/GaN HEMT 0.25µm	6 - 18	40	NA	Max : 41	10,4	18	Balanced Non Uniform Distributed Lange Coupler	18,72
[MEH07]	AlGaN/GaN HEMT 0.15µm	3 - 18	10	0,28	Max : 34 Average : 33,1	10,4	15	Balanced Distributed Lange Coupler	20,6
[KOB09]	AlGaN/GaN HEMT 0.20µm	DC -20	30	0,4	Max : 34 @OCP1: 32,5	>12,5	10 -15	Distributed Cascode	4,8
[MEY05]	AlGaN/GaN HEMT 0.15µm	4 - 18	NA	NA	@OCP3: 33	9	@ OCP1: 16	Distributed Cascode	46
This Work	AlGaN/GaN HEMT 0.25µm	8 -18	20	0.44	Max : 39.9 Average : 38.9	Max :12.4 Average : 11.7	Max :20.5 Average : 15.5	Differential Common source	Estimated : 15

Figure 4.52: GaN TWA state of art -

4.3 Confidential power amplifier design

During this PhD work, an other power amplifier was developed. In fact, more than a power amplifier it is the combination of two power amplifiers working in separated frequency bands and with different power levels. Unfortunately for confidentiality matters and THALES SA interests, no information at all can be released to the public whether about the performances of this circuit or its architecture. This work was about 10 months long and resulted in chip which is currently under fabrication. Moreover, a patent has been written and submitted, but at this time it is still pending which why no information can revealed yet. Only thing that can be said, is that the vertically stacked approach presented in previous chapters was used to realize this very particular and innovative design.

5

Conclusion and Perspectives

The main objective of this work was to develop innovative solutions to contribute to the size reduction of wideband GaN MMIC HPAs without degrading their efficiency. To this extent, the idea was to import techniques from silicon designs that have proven to be efficient. That's why the stacked topology was developed to implement compact baluns and couplers. Not only an innovative approach was described but it was proven to work with a realization and measurements. Something valuable to do in the future would be to develop an electrical model for the stacked baluns and couplers. Indeed, instead of having to perform every simulations with an EM engine, it would time saving to be able to do them at schematic level. Thanks to that more structures could be tested and improved in order to make the combiners more efficient. An other aspect that should be explored, is to use the stacked baluns to combine more than two power cells. Indeed, it would be interesting to develop a DAT (distributed active transformer) to combine four or eight cells. This approach has given very good results in silicon design in terms of die size and efficiency, so it is definitely something to look at in MMICs.

In this PhD, three amplifiers have been realized:

* **C to X band high power amplifier**: This amplifier based on common source cells, is using the developed stacked balun as power com-

biners. It exhibits more than 35dBm from 4 to 11GHz with a peak of 38.2dBm and 48%PAE, in average the PAE is 25%.

* **X to K_u band TWA**: TheTWA architecture was used in this design to maximize the bandwidth. From 8 to 18GHz, this amplifier exhibits 39dBm and 19% PAE in average. To increase output power, two elementary TWAs have been combined with the help of the second balun developed in this work.
* **confidential HPA**: As mentioned earlier, no information can be given at this time for confidentiality reasons

Amplifiers realized in this work were obviously dedicated to military applications considering the frequency ranges targeted and the power levels at stake. However,the fact that in this work we developed solutions in order to make MMICs chips smaller than what they are at the moment should be of great interest for civilians and everyday applications that start looking into GaN based devices. Indeed, the only chance to see GaN devices become an important player in the IC world would be at the cost of drastic die size reductions compared to actual MMICs.

GaN based technologies are quite limited in maximal frequency of operation for now. In fact, in our case it was not possible to design circuits working over 18 or 20 GHz. Development of new technologies with thinner gate widths in the next few years will permit to target applications up to 40GHz very soon. This will make reachable an all lot of new applications and moreover stacked combiners would be very small at these frequencies which is great in terms of die size reduction but the would also be more difficult to design due to all the parasitics effects happening when working in millimeter wave ranges such as skin effect for example.

Last thing that could be done, is to develop the use of stacked baluns and couplers for other applications than power combining. For example, baluns are needed in mixers and VCOs, so it would be interesting if these kinds of circuits can benefit from the die size reduction offered by the stacked approach too.

6

List of Publications

* **V. Dupuy, E. Kerherve, N. Deltimple, N. Demriel, Y. Mancuso**

  Very high efficiency SiGe and GaN High Power Amplifiers for tile modules

  International Microwave Symposium, Tampa, Florida, June 2014

* **V. Dupuy, N. Deltimple, B. Mallet-Guy, P. Garrec, Y. Mancuso, E. Kerherve**

  A 2.4GHz to 6GHz Active Balun in Gan Technology

  IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Abu Dhabi, UAE, December 8-11, 2013

* **V. Dupuy, N. Deltimple, E. Kerherve, J-P. Plaze, P. Dume, B. Mallet-Guy, Y. Mancuso**

  A 39.7 dBm and 18.5% PAE compact X to Ku band GaN Travelling Wave Amplifier

  IEEE MWSCAS, College Station, Texas, USA, August 3-6, 2014

* **V. Dupuy, N. Deltimple, J-P. Plaze, P. Garrec, Y. Mancuso, M. Dematos, S. Aloui, E. Kerherve**

  A Compact Wideband High Power Amplifier in GaN Technology with 47% peak PAE

  IEEE International Wireless Symposium (IWS), Xi?an, China, March 24-26, 2014

* **N. Deltimple, V. Dupuy, E. Kerherve, P. Garrec, Y. Mancuso, J-P. Plaze, B. Mallet-Guy, C. Auric**

  A Compact Fully Integrated GaN High Power Amplifier for C-X Band Applications

  IEEE RADAR 2014, Lille, France, October 13-17, 2014

* **V. Dupuy, N. Deltimple, Y. Mancuso, C. Auric E. Kerherve**

  Balun actif bande S/C en technologie GaN

  18emes Journes Nationales Microondes (JNM?13), Paris, France, June 14-17, 2013

* **J. Prades, A. Ghiotto, T. Taris, N. Regimbal, J. Pham, V. Dupuy, E. Kerherve**

  A microwave switchable low noise power amplifier for an active backscatter tag

  Microwave and Optical Technology Letters

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