Study of Schottky Barrier MOSFETs on SOI, SiGeOI and GeOI Substrates

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UNIVERSITE DE GRENOBLE
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T H E S E

pour obtenir le grade de

DOCTEUR DE L'Université de Grenoble
délivré par l'Institut polytechnique de Grenoble

Spécialité : *« Micro et Nano Electronique »*

préparée au Laboratoire des Dispositifs Innovants (CEA-Leti)

dans le cadre de **l'Ecole Doctorale**

*« **Electronique, Electrotechnique, Automatique & Traitement du Signal** »*

présentée et soutenue publiquement

par

Louis HUTIN

le 07 octobre 2010

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JURY

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“Science is the acceptance of what works and the rejection of what does not. That needs more courage than we might think.”

Jacob Bronowski

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Introduction Générale

Depuis sa première démonstration expérimentale par Kahng et Attala il y a un demi-siècle, le transistor à effet de champ à canal Silicium est devenu et s'est maintenu comme le moteur principal de l'industrie du semi-conducteur. Bien que son architecture et sont principe de fonctionnement soient restés essentiellement inchangés à ce jour, ses dimensions physiques n'ont cessé de décroître, suivant la loi de Moore.

Cette loi est principalement ressentie par le grand public sous diverses variantes telles que "mon prochain ordinateur portable sera plus rapide", "mon prochain téléphone portable sera plus compact et aura plus de fonctionnalités", qui peuvent toutes se conclure par "et je l'achèterai au même prix dans deux ans".

En fait, la première formulation de cette loi par Gordon Moore lui-même est qu'en augmentant la complexité d'un circuit pour une surface de puce donnée, en d'autres termes la densité d'intégration d' "environ un facteur deux par an" (à travers la mise en place des avancées technologiques réalisées pendant ce temps) permettrait de minimiser le coût de fabrication par transistor. De plus, les règles de "scaling" établies par Bob Dennard *et al.* ont montré la voie vers la diminution de la taille des composants, tout en maintenant la structure de la brique de base transistor, et en obtenant de surcroît un gain en performances mesuré en fréquence d'horloge.

Cette synergie entre considérations économiques et avancées technologiques a été décrite comme "l'horloge de Moore", un mécanisme autorégulé pour lequel le ressort technique (minimisation du produit puissance×temps de propagation) se synchronise avec le pendule commercial de la réduction du coût par bit. C'est par le biais de cette horloge que la loi de Moore est devenue une prophétie auto-réalisée durant les années dorénavant connues sous le nom d'ère du « happy scaling », ayant perduré jusqu'aux années 2000. Depuis lors, le mécanisme s'est effondré, puisque la réduction de la taille des composants n'a plus suffi à garantir les bonus cumulés d'une meilleure performance et d'un coût de fabrication réduit.

Oublions temporairement les contraintes de réduction de coût pour nous focaliser sur les qualités nécessaires pour faire d'un MOSFET (Metal Oxide Semiconductor Field Effect Transistor) un interrupteur plus efficace. Une façon basique de voir le problème est de chercher à minimiser l'énergie de commutation à l'état bloqué et à l'état passant. Celle-ci vaut $0.5 \times C_G \times V_{DD}^2$, où C_G est la capacité de grille du MOSFET, et V_{DD} sa tension d'alimentation. Au premier ordre, les lois du "happy scaling" impliquaient une réduction combinée de V_{DD} et de la longueur de grille L_G (et donc de C_G).

Le principal obstacle à la réduction de V_{DD} résulte du fait que les MOSFETs sont des dispositifs thermiques, avec une limite de pente sous le seuil idéale fixée à $(kT/q) \times \ln(10)$,

c'est à dire 60 mV par décade de courant à 300 K. Si l'on désire fixer le courant à l'état bloqué I_{OFF}, alors la réduction de V_{DD} a pour conséquences une plus faible surtension de grille (V_{DD}-V_T), et un courant à l'état passant I_{ON} plus faible. Inversement, si l'on désire fixer I_{ON} malgré un V_{DD} réduit, cela implique d'abaisser la tension de seuil V_T et ainsi augmenter I_{OFF}.

Pourtant, diminuer V_{DD} est une nécessité puisque cela permet de réduire la densité de puissance dans les circuits intégrés. Une densité de puissance trop élevée mène à un échauffement qui dégrade à la fois le courant passant (en dégradant la mobilité des porteurs) et le courant à l'état bloqué (en augmentant les fuites dues aux porteurs thermalisés).

Par le passé, réduire L_G contrebalançait efficacement les effets de la réduction de la tension d'alimentation (la résistance de canal était réduite, et I_{ON} s'en trouvait augmenté). Malheureusement, ce n'est plus suffisant puisqu'avec la réduction de la longueur du canal, les résistances parasites externes deviennent prépondérantes dans la limitation d'I_{ON}. De plus, des MOSFETs avec L_G~30-35nm étant d'ores et déjà en production industrielle à grande échelle, on ne peut pas s'attendre à ce que la réduction de L_G se poursuive indéfiniment.

Trois solutions en rupture avec le "classique" MOSFET à Source et Drain dopés et canal Si de 1960 peuvent être proposées pour résoudre ce problème:

1. Réduire les résistances parasites externes qui limitent I_{ON} dans les dispositifs à canaux courts (Source et Drain surélevés dans le cas SOI, accès siliciurés, voire Source et Drain complètement métalliques…)
2. Augmenter la vitesse des porteurs dans le canal pour réduire la résistance de canal (stresseurs, Germanium, semi-conducteurs III-V, graphène…)
3. Abaisser la pente sous le seuil pour relâcher les contraintes en termes de compromise of I_{ON}/I_{OFF} (I-MOS, TFETs, transistors Nano Electro-mécaniques à grille suspendue…)

Le but de cette thèse n'est pas de combiner des éléments des points 1, 2, et 3. Tout en restant relativement ambitieux, l'objectif se limite aux points 1 et 2: Source/Drain métalliques et canal Germanium. De plus, les analyses présentées dans ce manuscrit seront effectuées principalement dans le cadre de l'intégration sur substrats sur isolant (SOI, SiGeOI, GeOI). Ce choix est déterminé par plusieurs facteurs:

- La préservation de l'intégrité électrostatique dans les dispositifs à canaux courts, les nœuds technologiques visés étant "sub-22nm"
- La limitation des fuites de jonction qui dégradent les caractéristiques des MOSFETs sur Germanium (du fait de la faible bande interdite du Ge)
- La limitation des fuites de jonction qui dégradent les caractéristiques des MOSFETs à barrière Schottky (du fait de leur fonctionnement ambipolaire)

De plus, l'intégration de MOSFETs sur SOI est actuellement une pierre angulaire de la technologie développée au CEA-Leti.

L'essentiel de ce manuscrit est rédigé en anglais (chapitres I à V). Le lecteur francophone pressé pourra se rapporter au résumé en français ainsi qu'à la conclusion générale (pp. 243-282). Les références citées dans ces derniers sont explicitées dans les chapitres en anglais correspondants.

Symbols, acronyms

Symbol	Meaning	Units
A	Area	m^{-2}
A^*	Effective Richardson constant for thermionic emission	$A.cm^{-2}.K^{-2}$
A_n^*	Effective Richardson constant for thermionic emission for electrons	$A.cm^{-2}.K^{-2}$
A_p^*	Effective Richardson constant for thermionic emission for holes	$A.cm^{-2}.K^{-2}$
A^{**}	Effective reduced Richardson constant for thermionic emission	$A.cm^{-2}.K^{-2}$
A_n^{**}	Effective reduced Richardson constant for thermionic emission for electrons	$A.cm^{-2}.K^{-2}$
A_p^{**}	Effective reduced Richardson constant for thermionic emission for holes	$A.cm^{-2}.K^{-2}$
B	Magnetic field	T
C	Capacitance	F
C_{ox}	Gate oxide capacitance	$\mu F.cm^{-2}$
d (Chap.III)	Barrier thickness under which the transmission probability is 1	nm
D_{it}	Interface states density	$eV^{-1}.cm^{-2}$
D_{itm}	Metal interface traps density	$eV^{-1}.cm^{-2}$
D_{its}	Semiconductor interface traps density	$eV^{-1}.cm^{-2}$
D_{it}^{bottom}	Interface states density at the bottom interface (Si or Ge/BOX)	$eV^{-1}.cm^{-2}$
D_{it}^{top}	Interface states density at the top interface (Si or Ge/Gate stack)	$eV^{-1}.cm^{-2}$
D_n	Diffusion coefficient for electrons	$cm^2.s^{-1}$
D_p	Diffusion coefficient for holes	$cm^2.s^{-1}$
D_0	Pre-exponential factor in the Arrhenius law of diffusivity versus temperature	-
E	Energy	J
E_a	Activation energy	J
E_c	Kinetic energy	J
E_C	Conduction band energy	J
E_{cnl}	Charge neutrality level energy	J
E_{eff}	Effective transverse electric field	$V.cm^{-1}$
E_F	Semiconductor Fermi-level energy	J
$E_{F,degen}$	Semiconductor Fermi-level energy in the degenerate case	J
$E_{F,non\text{-}degen}$	Semiconductor Fermi-level energy in the non-degenerate case	J
$E_{F,0}$	Semiconductor Fermi-level energy at T=0K	J
E_{Fm}	Metal Fermi-level energy	J
E_{Fn}	n-type semiconductor quasi-Fermi-level energy	J
E_{Fp}	p-type semiconductor quasi-Fermi-level energy	J
E_g	Energy bandgap	J / often in eV
E_g^{xx}	Energy bandgap of material "xx" (E_g^{Si}, E_g^{SiGe}, E_g^{Ge} etc.)	J / often in eV
E_s	Energy corresponding to the top of the barrier in the Fowler theory	J
E_{sat}	Saturation electric field, ratio of v_{sat} to μ_{eff}	$V.cm^{-1}$
E_V	Valence band energy	J

E_0	Vacuum energy level	J
E_{00}	Characteristic energy for Field Emission	J
f_M	Occupation probability in the metal	-
f_p	Probability of emission over the Schottky Barrier	-
f_q	Ratio of total interfacial current flows with and without accounting for the distortion of the electron distribution due to quantum mechanical transmission	-
f_S	Occupation probability in the semiconductor	-
F_{mag}	Lorentz force	N
G	Conductance	G
h	Planck constant	J.s
ħ	Reduced Planck constant	J.s
I	Current	A
I_B	Bulk current, most of the time normalized by the channel width	$\mu A.\mu m^{-1}$
I_d, I_D	Drain current, most of the time normalized by the channel width	$\mu A.\mu m^{-1}$
I_{Dsat}	Drain current in saturation regime	$\mu A.\mu m^{-1}$
I_{Dsat0}	Drain current in saturation regime corresponding to $R_S=0\Omega$	$\mu A.\mu m^{-1}$
I_F	Current in forward bias	A
I_G	Gate current, most of the time normalized by the channel width	$\mu A.\mu m^{-1}$
I_{lin}	ON-State current, most of the time normalized by the channel width, in linear regime (low V_{DS})	$\mu A.\mu m^{-1}$
I_{OFF}	OFF-State current, most of the time normalized by the channel width	$\mu A.\mu m^{-1}$
I_{ON}	ON-State current, most of the time normalized by the channel width	$\mu A.\mu m^{-1}$
I_{OFFr}	OFF-State current, relative to the threshold voltage	$\mu A.\mu m^{-1}$
I_{ONr}	ON-State current, relative to the threshold voltage	$\mu A.\mu m^{-1}$
I_R	Current in reverse bias	A
I_S	Source current, most of the time normalized by the channel width	$\mu A.\mu m^{-1}$
J	Current density	$A.\mu m^{-2}$
J_D	Reverse saturation current density, diffusion theory	$A.\mu m^{-2}$
J_F	Current density in forward bias	$A.\mu m^{-2}$
J_{FE}	Reverse saturation current density in field emission dominant regime By extension, current density of field-emitted carriers	$A.\mu m^{-2}$
$J_{m\rightarrow s}$	Current density, flux directed from metal to semiconductor	$A.\mu m^{-2}$
J_n	Electrons current density	$A.\mu m^{-2}$
J_{n0}	Reverse saturation electrons current density	$A.\mu m^{-2}$
$J_{s\rightarrow m}$	Current density, flux directed from semiconductor to metal	$A.\mu m^{-2}$
J_p	Holes current density	$A.\mu m^{-2}$
J_{p0}	Reverse saturation holes current density	$A.\mu m^{-2}$
J_{TE}	Reverse saturation current density, thermionic emission theory By extension, current density associated to thermionically emitted carriers	$A.\mu m^{-2}$
J_{TED}	Reverse saturation current density, thermionic emission diffusion theory	$A.\mu m^{-2}$
J_{TFE}	Reverse saturation current density in thermionic field emission dominant regime By extension, current density of thermally excited, field-emitted carriers	$A.\mu m^{-2}$
J_{tun}	Tunnel current density $J_{tun}=J_{FE}+J_{TFE}$	$A.\mu m^{-2}$
J_0	Reverse saturation current density	$A.\mu m^{-2}$
k, k_B	Boltzmann constant	$J.K^{-1}$

k	Wavevector	-
L (Chap.II)	Length of the quasi-neutral region	nm
L_c	Contact length	µm
L_D	Debye length	nm
L_{eff}	Effective channel length	µm
L_g, L_G	Gate length	µm
$L_{overlap}$	Distance over which Gate and Source, or Gate and Drain overlap	nm
L_{relax}	Distance of lateral strain relaxation	nm
$L_{underlap}$	Distance between Gate and Source edges, or Gate and Drain edges	nm
m^*	Majority carriers effective mass	kg
m_C	Density of states effective mass in the conduction band	kg
m_{hh}	Heavy holes effective mass	kg
m_l	Longitudinal electrons effective mass	kg
m_{lh}	Light holes effective mass	kg
m_{so}	Split-off holes effective mass	kg
m_t	Transverse electrons effective mass	kg
m_T^*	Majority carriers tunneling effective mass	kg
m_{Thh}^*	Heavy holes tunneling effective mass	kg
m_{Tlh}^*	Light holes tunneling effective mass	kg
m_V	Density of states effective mass in the valence band	kg
m_0	Mass of an electron at rest	kg
n	Carriers concentration, electrons	cm^{-3}
n_i	Intrinsic carriers concentration	cm^{-3}
n_i^{xx}	Intrinsic carriers concentration in material "xx" (n_i^{Si}, n_i^{SiGe}, n_i^{Ge} etc.)	cm^{-3}
n_m	Electrons concentration at the maximum of potential energy x_m	cm^{-3}
n_0	Fictional electrons concentration in the case $E_{Fn}(x_m)=E_{Fm}$	cm^{-3}
N_a, N_A	Acceptor impurities concentration	$at.cm^{-3}$
N_A^-	Ionized acceptor impurities concentration	$at.cm^{-3}$
N_{act}	Electrical dopant activation level	$at.cm^{-3}$
N_C	Density of states in the conduction band	cm^{-3}
N_{ch}	Channel doping	$at.cm^{-3}$
N_d, N_D	Donor impurities concentration	$at.cm^{-3}$
N_D^+	Ionized donor impurities concentration	$at.cm^{-3}$
N_t	Bulk traps density	cm^{-3}
N_V	Density of states in the valence band	cm^{-3}
q	Elementary charge	C
Q_{dep}	Depletion charge	C
Q_f	Fixed charges near the Gate interface	C
R	Current response per absorbed photon in the Fowler theory	A/W
R_{ac}	Accumulation resistance	Ω
R_{access}	Access resistance, cf. R_{SD}	Ω
$R_{channel}$	Channel resistance	Ω
R_{co}	Contact resistance	Ω
R_D	Drain-end series resistance	Ω / Ω.µm

R_H	Hall coefficient	$cm^3.C^{-1}$
R_S	Source-end series resistance	Ω / Ω.µm
R_{sh}	Sheet resistance	$Ω / Ω.sq^{-1}$
R_{SD}	Source and Drain series resistance	Ω / Ω.µm
R_{Si}	Resistance of a Silicon rod	Ω
R_{sp}	Spreading resistance	Ω
S (Chap.II)	Slope parameter	-
S (Chap.III), S_{wi} (Chap.IV)	Subthreshold swing	mV/dec
T	Temperature	K
T_{dep}	Depletion depth	nm
T_{xx}	Film thickness of material "xx" (T_{Si}, T_{SiGe}, T_{Ge} etc.)	nm
T_M	Temperature below which TFE conduction at zero bias becomes FE	K
T_{ox}	Gate oxide thickness or equivalent oxide thickness	nm
TR	Transmission probability across a potential barrier	-
U_p	Total potential energy	J
v_D	Effective diffusion velocity	$cm.s^{-1}$
v_R	Thermionic recombination velocity	$cm.s^{-1}$
v_{sat}	Saturation carrier velocity	$cm.s^{-1}$
v_{th}	Therman velocity	$cm.s^{-1}$
V	Voltage	V
V_B	Built-in voltage	V
V_{bg}, V_{BG}	Back-Gate Voltage	V
V_{dd}, V_{DD}	Supply voltage	V
V_{DS}	Drain to Source voltage	V
$V_{f\text{-}max}$	Transition voltage from FE to TFE for degenerate semiconductors	V
V_F	Forward bias	V
V_{fb}, V_{FB}	Flat-band Voltage	V
V_{GD}	Gate to Drain Voltage	V
V_g, V_{GS}	Gate to Source Voltage	V
V_H	Hall Voltage	V
V_R	Reverse bias	V
V_T (Chap.II)	Thermal voltage	V
V_T (Chap.III)	Threshold voltage	V
V_T^*	Threshold voltage in saturation regime	V
V_{th} (Chap.IV)	Threshold voltage	V
$V_{th,n}$	Threshold voltage of nFETs	V
$V_{th,p}$	Threshold voltage of pFETs	V
W	Channel width	µm
W_{acc}	Accumulation region width	nm
W_c	Contact width	µm
W_{dep}	Depletion region width	nm
W_{depF}	Depletion region width, forward bias	nm
W_{depR}	Depletion region width, reverse bias	nm

W_{design}	Top view channel width	µm
W_{eff}	Effective channel width	µm
W_{SCR}	Space Charge Region width	nm
x_m	Distance from the metal/semiconductor interface of the extremum of potential energy	nm
x_1	Distance from the metal/semiconductor interface of the first turning point	nm
x_2	Distance from the metal/semiconductor interface of the second turning point	nm
δ (Chap.II)	Interfacial layer thickness	Å
Δ (Chap.II)	Potential drop across the interfacial layer (thickness δ)	V
ΔG_X	Gibbs energy variation for the formation of the defect X	J
ΔH_X	Enthalpy variation for the formation of the defect X	J
ΔS_X	Entropy variation for the formation of the defect X	J
$\Delta\Phi$, $\Delta\Phi_b$	Image force barrier lowering	eV
$\Delta\Phi_{bn}$	Image force barrier lowering for electrons	eV
$\Delta\Phi_{bp}$	Image force barrier lowering for holes	eV
$\Delta\Phi_F$	Image force barrier lowering, forward bias	eV
Γ	Point in the E-**k** dispersion relationship where **k**=**0**	-
ζ	Effective barrier in the tunnel MIS diode theory	eV
ε_{Ge}	Relative permittivity of Germanium	$F.m^{-1}$
ε_i	Permittivity of interfacial layer	$F.m^{-1}$
ε_{ox}	Permittivity of the gate oxide	$F.m^{-1}$
ε_s	Permittivity of semiconductor	$F.m^{-1}$
ε_{Si}	Relative permittivity of Silicon	$F.m^{-1}$
ε_0	Permittivity of vacuum	$F.m^{-1}$
E (Chap.II)	Electric field	$V.cm^{-1}$
E_m	Maximal value of the electric field (value at $x=x_m$)	$V.cm^{-1}$
η (Chap.II)	Ideality factor	-
η (Chap.III)	Fitting parameter in Poisson equation	-
λ (Chap.II)	Mean free path	nm
λ (Chap.III)	A characteristic length scale on which potential variations are screened	nm
µ	Carrier mobility	$cm^2.V^{-1}.s^{-1}$
μ_e, μ_n	Electron mobility	$cm^2.V^{-1}.s^{-1}$
μ_{eff}	Effective mobility	$cm^2.V^{-1}.s^{-1}$
μ_h, μ_p	Hole mobility	$cm^2.V^{-1}.s^{-1}$
μ_0	Low-field mobility	$cm^2.V^{-1}.s^{-1}$
ν	Photon frequency	Hz
ν_0	Photon frequency such that $h\nu_0=q\Phi_b$	Hz
Φ_0	Charge neutrality level (relative to the Valence Band)	eV
Φ_b	Schottky Barrier Height	eV
Φ_{bn}	Effective Schottky Barrier Height for electrons	eV
Φ_{bn0}	Intrinsic Schottky Barrier Height for electrons	eV
Φ_{bp}	Effective Schottky Barrier Height for holes	eV
Φ_{bp0}	Intrinsic Schottky Barrier Height for holes	eV

Φ_m	Metal Workfunction (relative to vacuum energy level E_0)	eV
Φ_n	Position of the Fermi-level relative to E_C (n-type)	eV
Φ_p	Position of the Fermi-level relative to E_V (p-type)	eV
ρ	Density of charges per volume unit	$C.m^{-3}$
ρ_c	Specific contact resistivity	$\Omega.cm^2$
ρ_c^{hh}	Specific contact resistivity associated to heavy holes conduction	$\Omega.cm^2$
ρ_c^{lh}	Specific contact resistivity associatted to light holes conduction	$\Omega.cm^2$
ρ_{sd}	Resistivity of a doped semiconductor layer	Ω/sq
σ	Conductivity	$S.cm^{-1}$
σ_n	Capture cross-section of electrons	cm^2
σ_p	Capture cross-section of holes	cm^2
ψ_{acc}	Potential in the accumulation region	eV
ψ_{bi}, Ψ_{bi}	Built-in potential	eV
ψ_{dep}	Potential in the depletion region	eV
Ψ_g	Gate potential	V
ψ_{im}	Potential associated to the image force	eV
Ψ_s	Surface potential	V
τ_n	Minority carrier lifetime for electrons	s
τ_p	Minority carrier lifetime for holes	s
χ	Semiconductor electron affinity	eV

Acronyms	**Meaning**
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ALCVD	Atomic Layer Chemical Vapor Deposition
ASIC	Application-Specific Integrated Circuit
BG	Back Gate
BJT	Bipolar Junction Transistor
BOX	Buried Oxide
BTBT, BBT	Band-To-Band Tunneling
CB	Conduction Band
CBKR	Cross-Bridge Kelvin Resistor
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
DB	Dangling Bond
DC	Dual Channel
DCOI	Dual Channel On Insulator
DFEH	Dark-Field Electron Holography
DG	Double Gate
DIBL	Drain-Induced Barrier Lowering
DSCOI	Dual Strained Channel On Insulator
DSS	Dopant-Segregated Source and Drain
DUV	Deep Ultra Violet (Lithography)
E-beam	Electron Beam (Lithography)
EDS, EDX	Energy Dispersive X-Ray Spectroscopy
EELS	Electron Energy Loss Spectroscopy
EOT	Equivalent Oxide Thickness
FDSOI	Fully Depleted Silicon on Insulator
FE	Field Emission
FG	Front Gate
GAA	Gate-All-Around
GeOI, GOI	Germanium On Insulator
GIDL	Gate-Induced Drain Leakage
GND	Ground
HDD	Highly Doped Drain
HF	Hydrofluoric acid
High-k, High-κ	Material with a high dielectric constant (compared to SiO_2)
HPO	High Pressure Oxidation

IBS	Implantation before silicidation
II	Ion Implantation
IL	InterLayer
I-MOS	Impact Ionization Metal Oxide Semiconductor (Field-Effect Transistor)
ITM	Implantation Through Metal
ITRS	International Technology Roadmap for Semiconductors
ITS	Implantation Through Silicide
LDD	Lowly Doped Drain
LOA	Low temperature Oxygen Anneal
LOL	Laughing Out Loud
LTA	Laser Thermal Anneal
MESFET	Metal Semiconductor Field-Effect Transistor
MIGS	Metal-Induced Gap States
MIS	Metal-Insulator-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPU	Microprocessing Unit
NBED, NBD	Nano Beam Electron Diffraction
NBTI	Negative Bias Temperature Instability (of $V_{th,p}$)
NEGF	Non-Equilibrium Green's Function
nFET	Metal-Oxide-Semiconductor Field-Effect Transistor with an n-type conduction channel
NIL	Nitride InterLayer
OIL	Oxide InterLayer
PAI	Preamorphization-Assisted Implantation
PBTI	Positive Bias Temperature Instability (of $V_{th,n}$)
PECVD	Plasma Enhanced Chemical Vapor Deposition
pFET	Field-Effect Transistor with a p-type conduction channel
PVD	Physical Vapor Deposition
RMS	Root Mean Square
RNM	Read Noise Margin
RO	Ring Oscillator
RTA	Rapid Thermal Anneal
SBFET	Schottky Barrier Field Effect Transistor
SBH	Schottky Barrier Height
SC	Semiconductor
SCE	Short Channel Effects
SCR	Space Charge Region
S/D	Source and Drain

SEM	Scanning Electron Microscopy
SG	Single Gate
SGOI	Silicon Germanium On Insulator
SIMS	Secondary Ion Mass Spectroscopy
SNM	Static Noise Margin
SOI	Silicon On Insulator
SOLES	Silicon On Lattice Engineered Substrates
SPER	Solid-Phase Epitaxial Regrowth
SPM	Sulfuric Peroxyde Mixture
(“x”T-)SRAM	Static Random Access Memory with “x” Transistors
SRH	Shockley-Read-Hall recombination
SRP	Spreading Resistance Probe
SSL	Solid Solubility Limit
STEM	Scanning Transmission Electron Microscopy
TAT	Trap-Assisted Tunneling
TCAD	Technology Computer Aided Design
TDD	Threading Dislocations Density
TE-D	Thermionic Emission – Diffusion theory
TEM	Transmission Electron Microscopy
TFE	Thermionic Field Emission
TFET	Tunnel Field-Effect Transistor
TLM	Transmission Line Model
UTB	Ultra Thin Body
UTBOX	Ultra Thin Buried Oxide
VB	Valence Band
VdP	Van der Pauw structures
WKB	Wentzel-Kramers-Brillouin approximation
XSTEM	Cross-Sectional Scanning Transmission Electron Microscopy
XTEM	Cross-Sectional Transmission Electron Microscopy
α–	Amorphous
c-	Crystalline **or** Compressively-strained
s-	Strained
t-	Tensily strained

Chapter I. Introduction

I.1. Context

Since its invention half a century ago [*Kahng'60*], the Si-based Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) has become and maintained itself as the driving force for the semiconductor industry. Although the architecture and working principle of the MOSFET has essentially remained the same, its physical dimensions have been constantly reduced following Moore's Law [*Moore'65*].

This law is mostly experienced in the daily life under several variations such as "my next laptop will run faster" or "my next cell phone will be more compact and have more functions" which all could end up with "and I will purchase it to the same price two years from now".

Actually, the first formulation by Gordon Moore himself in the original paper simply states that increasing the circuit complexity for a given chip area, in other words the integration density, by "a rate of roughly a factor of two per year" (through the implementation of technological advances) would minimize the manufacturing cost per transistor. Additionally, the set of scaling rules established by Bob Dennard *et al.* [*Dennard'74*] showed the way towards the downscaling of component size while maintaining the structure of the basic transistor building block, and achieving a gain in performance measured in clock frequency.

This synergy between economical considerations and technological achievements was described in [*Declerck'05*] as "Moore's clock", a self-regulating mechanism in which the technological spring of power×delay product improvement was perfectly synchronized with the commercial pendulum of cost/bit reduction. This is how Moore's law became a self-fulfilling prophecy during what has been called the "happy scaling era", which lasted up to the early 2000's. Since then, Moore's clock has been falling apart as the downsizing of the components no longer guaranteed the combined bonuses of higher performance and lower cost.

For now, let us forget about the cost-reduction aspects and focus on what it takes to make a MOSFET into a more efficient switch. One basic way to look at this problem is seeking to minimize the energy to switch the transistor on and off. This energy is equal to $0.5 \times C_G \times V_{DD}^2$, where C_G is the gate capacitance of the MOSFET, and V_{DD} is the power supply voltage. Basically, the "happy scaling" rules implied a combination of lowering V_{DD} and reducing the gate length L_G (and therefore C_G).

The main limitation in scaling V_{DD} stems from the fact that MOSFET are thermal devices, with an ideal subthreshold swing limit set to $(kT/q) \times \ln(10)$, *ie* 60 mV/decade at 300 K. If the OFF-State current I_{OFF} has to remain the same, then reducing V_{DD} results in a smaller gate overdrive (V_{DD}-V_T), and a lower ON-State current I_{ON}. If, reciprocally, I_{ON} should

remain the same at reduced V_{DD}, it implies lowering the threshold voltage V_T and therefore increasing I_{OFF} (Figure I-1).

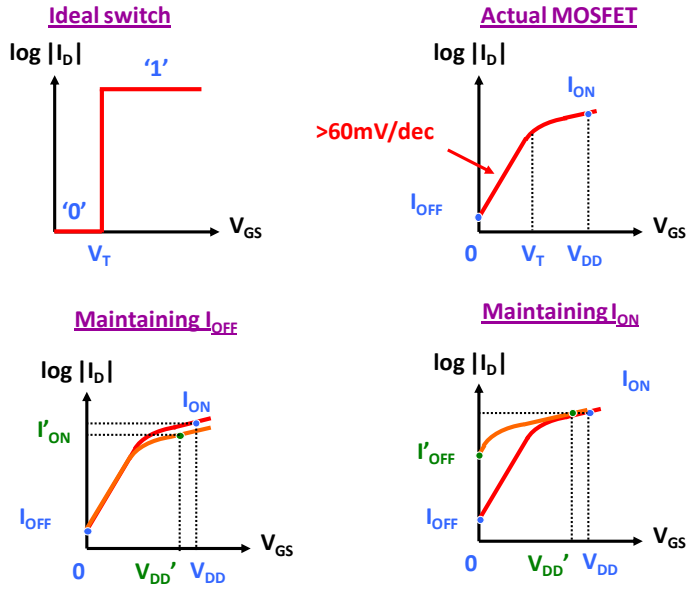

Figure I-1: Illustration by schematic I_D-V_{GS} MOSFET characteristic curves of the issues related to scaling V_{DD} in terms of ON/OFF trade-off, given the subthreshold swing limitation of 60mV/dec.

Yet, lowering V_{DD} is fundamental as it enables to reduce the power density in integrated circuits. A too large power density means heat, which degrades both the ON-State performance (mobility degradation) and the OFF-State characteristics (increased thermal leakage).

In the past, downscaling L_G has proven successful in counteracting the effect of V_{DD} lowering, as it primarily resulted in reducing the channel resistance, therefore increasing I_{ON}. Unfortunately, this is no longer sufficient since along with aggressive scaling, I_{ON} became mostly limited by extrinsic series resistance. Besides, MOSFETs with L_G~30-35nm being already in large scale industrial production to this day [*Packan'09*], we cannot expect the dimensions scaling to continue forever.

Three solutions in rupture with the plain old Silicon-based conventional MOSFET of 1960 can be proposed to solve this conundrum:

1. Reducing the extrinsic parasitic resistance limiting I_{ON} at short gate lengths (Raised S/D in the SOI case, silicided access, or completely metallic Source and Drain…)
2. Boosting the carrier velocity to drastically reduce the channel resistance (channel stressors, Germanium, III-V semiconductors, graphene…)
3. Lowering the subthreshold swing to relax the constraints in terms of I_{ON}/I_{OFF} trade-off (I-MOS, TFETs, Nano Electro-mechanical relays…)

The goal of this thesis is not to combine 1, 2, and 3. It is however, ambitiously enough, to combine 1 and 2: metallic S/D **and** Germanium channel.

I.2. Schottky-Barrier transistors

The idea behind the use of metal S/D is that no matter how highly the Source and Drain regions are doped, they will never be as conductive as if they were made of metal. On the other hand, one could object that no matter how low the metal/semiconductor Schottky barrier can be, it will be hard to fare better than the "no barrier" case of doped p/n diodes where carriers can freely diffuse on each side of the junction. This basically calls for a careful examination of the trade-off between sheet resistivity reduction in the access region and injection efficiency at the Source/Channel junction.

This injection efficiency can be evaluated through the parameter of metal/semiconductor contact resistivity. The smaller the Schottky barrier is, the lower the contact resistivity will be. If the barrier cannot be "intrinsically" small enough to lead to comparable performance with respect to conventional p/n junctions MOSFETs, a common way to increase the interfacial current density is to make it thinner to facilitate carrier transmission through it. This solution typically involves the formation of a thin, highly doped layer at the interface. Another trade-off then appears, as some of the advantages of an architecture featuring an undoped channel and atomically abrupt junctions (*eg* in terms of Short Channel Effects management, variability…) could be lost in the process.

The intrinsic barrier height properties depend on the metal, but also on the semiconductor. There are reasons to think that contacts on Germanium could lead to smaller barrier heights, contact resistivities, and therefore higher injection efficiency than on Silicon, mainly due to the smaller bandgap in Ge.

I.3. Transistors on GeOI

Regardless of what has been developed in the previous paragraph, the main motivation for using Germanium as a channel material is simply that carriers drift faster in this semiconductor compared to Silicon. Germanium is in fact a high mobility semiconductor, but has been abandoned in the early 1960's for MOSFET fabrication due to the chemical instability and water solubility of its native oxide.

The introduction of high-k as gate dielectrics in the last decade has provoked a renewal of interest in Ge-based devices and their expected superior transport properties. On

the other hand, the development of the Ge technology and has accumulated a handicap of roughly 40 years with respect to Si, which makes practical implementations challenging.
For instance, it seemed not so long ago that the realization of highly-doped, shallow junctions by n-type doping was a major obstacle for Ge nFETs fabrication, and therefore for Ge CMOS integration. If some progress has been made regarding electrical activation of n-type dopants in Ge, the high diffusivities of As and P above 550°C remain a challenge. Then again, there are good reasons to think that metallic Source and Drain would provide both lower access resistivity as well as ultimately abrupt junctions.

I.4. Ge and metallic Source and Drain, a mutually profitable association?

In the quest for minimizing the contact resistivity of metal/semiconductor junctions in Schottky-Barrier MOSFETs, first order observations suggest looking into SBFET integration on Germanium. Reciprocally, from the point of view of Ge CMOS realization, first order observations on the need to achieve high junction abruptness and low sheet resistivity suggest looking into SBFETs.

Yet, these remain first order observations. The goal of this thesis will be primarily to provide, separately, an in-depth analysis of the pros and the cons for Schottky-Barrier MOSFETs (Chapter II and Chapter III), and Germanium-based devices (Chapter IV). In particular, these analyses will be carried out in the framework of integration on "On-Insulator" substrates (SOI, SiGeOI, GeOI). This choice can be justified by several factors:

- The preservation of the electrostatic integrity of short-channel devices, as the sub-22nm technological nodes are targeted
- The limitation of junction leakage plaguing the characteristics of low bandgap Ge-channel devices
- The limitation of junction leakage degrading the characteristics of ambipolar SBFETs

Moreover, the integration of MOSFETs on SOI substrates is currently a cornerstone of the technology developed in Leti. Finally, we will see if their various qualities can combine when merging these architectures into SBFETs on GeOI substrates.

Chapter I. - References

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Chapter II. **Metal/Semiconductor contacts**

The aim of this chapter is to identify the specifications that would make a Schottky junction suitable for CMOS logic applications, in particular in terms of contact resistivity. First, we will introduce the physics of Metal/Semiconductor contacts, from the formation of the Schottky potential barrier to the expression of the interfacial current densities. Subsequently, we will review the most commonly used experimental techniques for characterization of Schottky junctions, and the hypotheses on which they rely. We will then evoke the trade-off between the use of simplified expressions and the actual intricate nature of the contributions from the various current transport processes in some cases. These cases are often the most relevant for CMOS applications. A One-Dimensional analysis of a Metal/Si diode will provide further qualitative and quantitative understanding regarding the respective impacts of parameters such as barrier height, doping, bias and temperature on its electrical behavior.

II.1. Theory of the Schottky junction

II.1.1. Formation of a Schottky Barrier

In this section, the more intuitive case of an n-type semiconductor and electron currents will be considered for illustration.

II.1.1.a. « Perfect contact » limit case

When a metal is connected to an n-type semiconductor, electrons tend to naturally flow from the semiconductor into the metal as the Fermi levels tend to align. The energies of an electron at rest being no longer the same on each side, an electric field builds up between the two surfaces. A negative charge appears on the surface of the metal, counterbalanced by a positive charge on the semiconductor surface, resulting from the depletion of electrons no longer compensating for the presence of ionized donor impurities.

The concentration of these ionized donors being inferior by several orders of magnitude to that of electrons in the metal, the Space Charge Region (positive charge in our case) extends over a non-negligible width in which then bands are bent upwards. Contact is obtained by approaching both interfaces until the distance that separates them becomes zero. The height of the barrier then results from the bands bending on the semiconductor side.

Following this simple picture, one can immediately deduce that the barrier height for electrons (Φ_b) is solely determined by the metal workfunction (Φ_m) and the semiconductor electron affinity (χ) according to:

$$\Phi_b = \Phi_m - \chi$$

(eq. II-1)

This is the so-called Schottky relationship, describing the “perfect contact” limit case (Figure II-1).

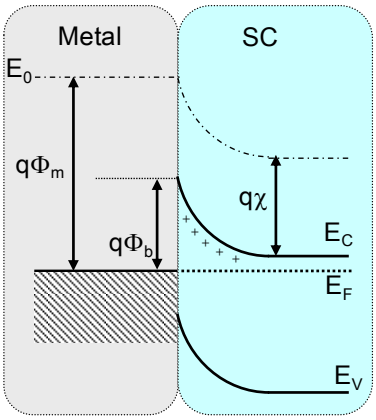

Figure II-1: Simplified band diagram of a metal/n-type semiconductor contact, defining the Schottky Barrier Height (Φ_b) in the perfect contact limit case.

II.1.1.b. Imperfect interfaces

Yet in practice, the Schottky Barrier Height (noted SBH in the following) in a given semiconductor (*e.g.* Si, or Ge) is seldom if ever fully determined by the metallization. This is a consequence of the importance of the interface states (see section II.1.1.b.i for a discussion on their origin). This distribution of states within the forbidden band-gap can be characterized by a charge neutrality level Φ_0 (also noted E_{cnl}). The surface is neutral if the surface states are occupied up to this energy level. Above this level, the surface states are called acceptor-like (neutral if unoccupied, negatively charged if occupied). Below, they are called donor-like (neutral if occupied by electrons, positively charged if unoccupied).

If Φ_0 is superior to the Fermi-level, a global positive charge is induced by the interface states, which implies a narrowing of the Space Charge Region (SCR). This positive charge then contributes to counterbalance the negative charge at the metal surface, which implies that the contribution from the ionized donors in this compensation is diminished. Hence, the band bending is reduced, and therefore the SBH is lowered. This mechanically results in bringing Φ_0 and E_F closer to each other. Reciprocally $\Phi_0<E_F$ results in a negative surface charge, the SCR broadens and the SBH increases, reducing the shift between Φ_0 and E_F.

Thus, an interface states-induced negative feedback loop tends to reduce the gap between E_F and Φ_0. Intuitively, the higher the interface states density, the higher the gain in the loop. The charge neutrality level then "pins" the Fermi-level in the semiconductor, so that the SBH becomes virtually independent on metallization in the most extreme cases. This phenomenon is referred to in the literature as "Fermi-level pinning".

Furthermore, an interfacial layer (*e.g.* native oxide) of thickness $\delta\neq0$ almost always separates both surfaces. If δ is thin enough (a few Å), electrons can easily tunnel through it so that its impact on transport can be neglected. Nevertheless, the presence of this layer can modify the electrostatics of the contact by causing a potential drop. For the following, we can improve our description of the Schottky contact to Figure II-2.

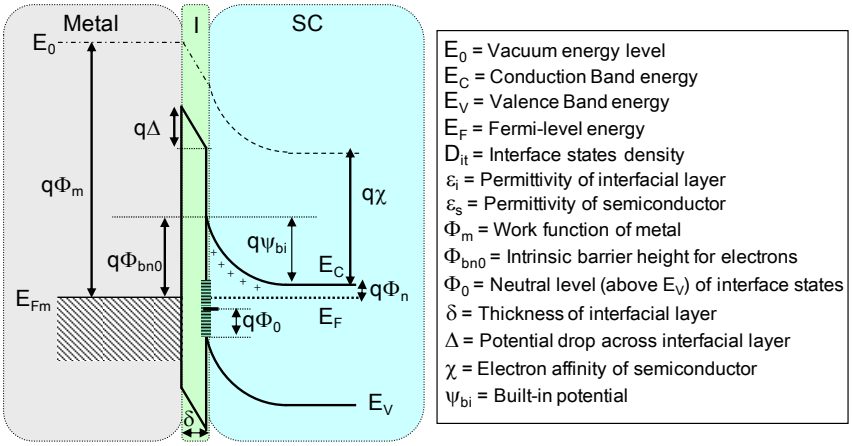

Figure II-2: Simplified band diagram of a metal/n-type semiconductor contact taking into account an insulating (I) interfacial layer and interface states, with definition of some characteristic parameters.

II.1.1.b.i. Origin of the interface states

There has been a debate in the late seventies and early eighties regarding the origin of the interface states causing the pinning phenomenon. Rowe *et al.* [*Rowe'75*] have studied the relative importance of « intrinsic » states present at the surface of the semiconductor before metal deposition (finite number of discrete states induced by dangling bonds, broken bonds, surface disorder), and « extrinsic states » induced by the atoms of deposited metal.

These extrinsic states are commonly referred to as MIGS, for Metal-Induced Gap States. They originate from the disruption of crystalline periodicity at the interface: the wavefunctions of the electrons in the metal "tail" over a few Å past the interface with the semiconductor, following an exponential decay. The typical penetration lengths are of 3Å in Si and 4Å in Ge [*Sze'07*], as the decay length increases with decreasing semiconductor bandgap. This "tail" is expressed by a combination of Bloch states of the bulk semiconductor (Conduction Band States, Valence Band states) with complex wave vector, and results in a continuum of states located within the bandgap. The states in the upper half of the bandgap are primarily derived from Conduction Band states and are of acceptor type, whereas those in the lower half are primarily derived from Valence Band States and of donor type.

In [*Rowe'75*], it was observed in particular that on Ge(111) and Ge(100), the influence of intrinsic states disappeared during metal deposition and the extrinsic states associated to the adatoms were found to be dominant. However, in the case of Ge(110), the influence of the intrinsic surface states seemed unchanged after metallization implying that surface states were playing a predominant role in the Fermi-level pinning. Subsequent studies [*Spicer'79*],[*Spicer'80*],[*Allen'82*] focused on the role of surface states associated to defects in the semiconductor.

It was later argued by Tersoff [*Tersoff'84*] that these considerations were mostly valid for monolayer metal coverages, but inappropriate for bulk interfaces (*ie* with a thick metal

layer), and a parameter-free model for Fermi-level pinning by MIGS was proposed. Its core is that the branching point E_B, energy at which the MIGS cross over from Valence to Conduction Band character, is the actual charge neutrality level Φ_0 and is a property of the bulk of the semiconductor (not of its surface). In bulk interfaces, the MIGS screen any surface defect-induced dipole located within the decay length, and are orders of magnitude more significant in the pinning process. The decay length of MIGS varies according to the surface orientation, which explains the orientation dependence of pinning on ideal epitaxial interfaces [*Tung'84*], a feature that the surface defects model failed to explain. The consistence of these views has also been confirmed recently by experimental observations on Metal/Ge contacts obtained by deposition or germanidation [*Dimoulas'06*], [*Nishimura'07*].

II.1.1.c. Fermi-level pinning

II.1.1.c.i. D_{it} and slope parameter

The sum of the charges in the interfacial layer and in the depletion region of the semiconductor is equal to the opposite of the charge at the surface of the metal. Gauss's law thus allows expressing the potential across the interfacial layer. Let N_d be the donor impurities concentration in the semiconductor and E_g the energy bandgap. The following equation is obtained:

$$\Phi_m - \chi - \Phi_{bn0} = \sqrt{\frac{2q\varepsilon_s N_d \delta^2}{\varepsilon_i^{\,2}}\left(\Phi_{bn0} - \Phi_n - \frac{kT}{q}\right)} - \frac{qD_{it}\delta}{\varepsilon_i}\left(E_g - q\Phi_0 - q\Phi_{bn0}\right)$$

(eq. II-2)

We can introduce the quantities $c_1 = \frac{2q\varepsilon_s N_D \delta^2}{\varepsilon_i^2}$ and $c_2 = \frac{\varepsilon_i}{\varepsilon_i + q^2 \delta D_{it}}$.

If we assume a transparent interfacial barrier, $\varepsilon_i = \varepsilon_0$ and c_1 can be neglected. The SBH can then be expressed as a linear function of the workfunction:

$$\Phi_{bn0} = c_2\left(\Phi_m - \chi\right) + \left(1 - c_2\right)\left(\frac{E_g}{q} - \Phi_0\right) \equiv c_2\Phi_m + c_3$$

(eq. II-3)

With varying Φ_m, the experimental extraction of c_2 and c_3 can lead to Φ_0 and D_{it}.

From (eq. II-3) arise two limit cases:
If $D_{it} \to \infty$ then $c_2 \to 0$ and $q\Phi_{bn0} = E_g - q\Phi_0$ (**total Fermi-level pinning** to the charge neutrality level, also known as Bardeen's strong pinning limit case [*Bardeen'47*])
If $D_{it} \to 0$ then $c_2 \to 1$ and $q\Phi_{bn0} = q\Phi_m - \chi$ (**no pinning**, the Schottky-Mott law applies [*Mott'38*], [*Schottky'40*])

The quantity c_2 is frequently referred to as the « slope parameter » S [*Mönch'87*],[*Dimoulas'06*],[*Ikeda'06*], defined as $S=d\Phi_{bn0}/d\Phi_m$. It basically translates into the controllability of the SBH by the choice of the metal on a scale from 0 to 1, for a given semiconductor. As a rule of thumb, S can be evaluated as [*Mönch'99*]:

$$S \approx \frac{1}{1+0.1(\varepsilon_s - 1)^2}$$

(eq. II-4)

- In Silicon, Φ_0 is said to be typically located around 1/3 of the bandgap above the top edge of the valence band (≈0.37eV), and S≈0.27 [*Sze'07*]. This means that the formed SBH are generally more favorable to holes conduction than to electrons conduction, and that they are relatively independent on the metallization.
- Studies on Germanium samples reported Φ_0 located at 0.18eV above the valence band according to [*Yeo'02*], 0.09eV according to [*Dimoulas'06*]. S has been evaluated to 0.02 [*Mönch'87*], <0.04 [*Ikeda'06*], 0.05±0.01 [*Dimoulas'06*]. These values are considerably lower than in Si and testify to even more pronounced trends (Figure II-3).

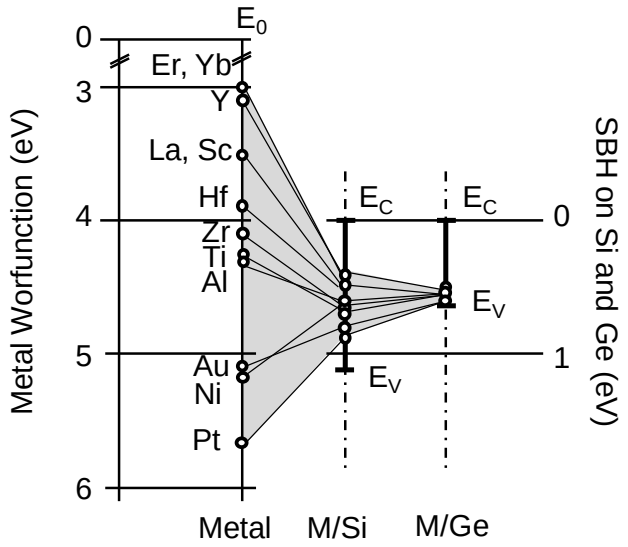

Figure II-3: Illustration of the influence of Fermi-level pinning on the SBH for electrons in Si and Ge (data: [Nishimura'07])

II.1.1.c.ii. Complementarity

To our knowledge, the overwhelming majority of the SBH extraction studies on type IV semiconductors have been realized on n-type Ge and Si. It may be legitimate to wonder whether or not the predominance of the interface states should be the same on p-doped samples. According to Smith and Rhoderick, it is the case in Silicon [*Smith'71*]. Our

experimental data on n- and p-Ge also hint towards this conclusion [*Hutin'09*]. It seems generally accepted that the surface properties do not depend *a priori* on the type of doping [*Sze'07*].

In this case, we can formulate the hypothesis of complementarity. We can assume that the intrinsic SBH for holes (Φ_{bp0}, independent of the doping level and determined only by the Fermi-level pinning) on a p-doped substrate would be the energy bandgap minus the value of the SBH for electrons (Φ_{bn0}) measured on an n-doped substrate and vice versa.

$$\Phi_{bn0} + \Phi_{bp0} = E_g$$

(eq. II-5)

II.1.1.c.iii. Depinning and dipole-induced modulation

In Si and Ge, the MIGS penetrate only within a few Å past the interface [*Louie'75*]. If an insulating layer (*ie* material with a wide bandgap) is introduced between metal and semiconductor, even the smallest thicknesses should be enough to fully absorb the MIGS. Furthermore, a passivation mechanism occurs, reducing the interface states density related to the dangling and broken bonds. As both MIGS and surface states densities are diminished, the pinning factor decreases, hence the term of "depinning layer".

Experimentally, this trend has recently been demonstrated [*Lieten'08*], [*Nishimura'08*],[*Zhou'08*] to produce ohmic contacts on n-type Germanium insulating interfacial layers (resp. Ge_3N_4, GeO_x and Al_2O_3) with thicknesses ranging from 0.6 to 2nm. The depinning layer should not be too thick, as it reduces the current density at low field by introducing an additional barrier for tunneling.

Even further control on the SBH has been shown by Coss *et al.* [*Coss'09*] with the introduction of a high-κ/oxide dipole between the metal and the semiconductor. A double layer (~1 nm high-κ / ~1nm SiO_2) results not only in depinning the Fermi-level (reduction of the S factor), but also in shifting of the charge neutrality level Φ_0 through the creation of a dipole at the oxide/high-κ dielectric interface. For example in this work, dipole magnitudes of +0.57eV and -0.35eV have been observed for respectively AlO_x/SiO_2 and LaO_x/SiO_2 interfacial bilayers. The magnitude depends on the high-κ thickness and saturates at roughly 10Å. This ultimately results in tuning the SBH to <0.1eV and <0.2eV from the conduction band (resp. valence band) edge of Silicon.

II.1.1.d. The Schottky effect, or image force

II.1.1.d.i. Origin and consequences

The Schottky effect, or image force, is another factor to consider which strays from the ideal case expression of the SBH (eq. II-1). It results in a reduction of the barrier height induced by a force exerted on the carriers in presence of an electric field.

In vacuum, when an electron is located at a distance x away from a metal, it causes plasma oscillations in surface of the metal, which can be described by the induction of a positive charge. The resulting attraction force between the electron and the metal surface is equivalent to that which would be induced by a positive charge of equal absolute value, located in –x with respect to the metal surface. This attraction force, the image force, is given by:

$$F(x) = \frac{-q^2}{16\pi\varepsilon_0 x^2}$$

(eq. II-6)

hence the work exerted on the electron:

$$\int_{-\infty}^{x} F(x')dx' = \frac{-q^2}{16\pi\varepsilon_0 x}$$

(eq. II-7)

In presence of an electric field E, the total potential energy U_p as a function of x is given by the sum:

$$U_p(x) = \frac{-q^2}{16\pi\varepsilon_0 x} \pm q|\mathrm{E}|x$$

(eq. II-8)

(– sign if along –x, + sign if along +x). A maximum is reached when the derivative equals 0 at:

$$x_m = \sqrt{\frac{q}{16\pi\varepsilon_0|\mathrm{E}|}}$$

(eq. II-9)

hence a variation of potential induced by the image force ΔΦ:

$$\Delta\Phi = \sqrt{\frac{q|\mathrm{E}|}{4\pi\varepsilon_0}} = 2|\mathrm{E}|x_m$$

(eq. II-10)

This yields the typical barrier shape pictured below Figure II-4.

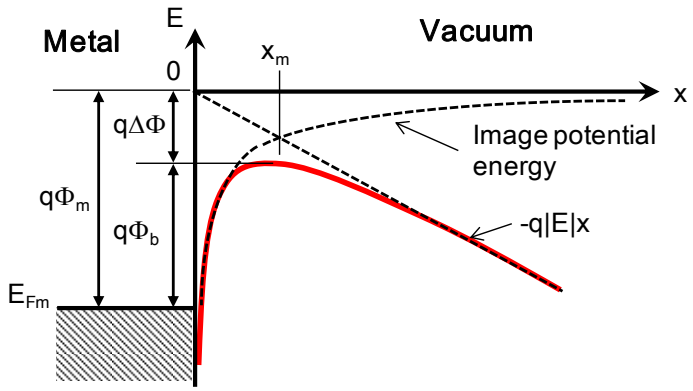

Figure II-4: Total potential energy of an electron in vacuum at a distance x from a metal, Submitted to an electric field E, and taking into account the image force.

By analogy to a metal/semiconductor system, the barrier lowering becomes $\Delta\Phi = \sqrt{qE/4\pi\varepsilon_s}$ with a non-zero electric field owing to the junction built-in potential. Typical values in Si will be discussed in details later on (sections II.3.1. and II.3.5.). Suffice it to say for now that even when $\Delta\Phi$ has a low value (*e.g.* a few tens of meV), the impact of image force can be significant in terms of transport above and across the barrier. We can note that in Ge (ε_s=16.2ε_0 vs. ε_s=11.9ε_0 in Si), the barrier lowering might be lower in absolute value, but relatively more important with respect to the size of the energy bandgap (0.66eV vs. 1.12eV in Si).

In practice, the field does depend on distance in a Schottky junction, but we can use the total depletion approximation and consider the maximal value of the electric field (at the surface) $E_m = \sqrt{2qN|\Psi_s|/\varepsilon_s}$. Ψ_s is the surface potential. In the case of a reverse bias V_R, and for an n-type semiconductor $|\Psi_s| = \Phi_{bn0} - \Phi_n + V_R$, yielding :

$$\Delta\Phi = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}} = \left[\frac{q^3 N|\Psi_s|}{8\pi^2\varepsilon_s^3}\right]^{1/4}$$

(eq. II-11)

The effective SBH is thus Φ_{bn0} to which the bias and doping-dependent barrier lowering induced by the image force is subtracted:

$$\Phi_{bn} = \Phi_{bn0} - \Delta\Phi$$

(eq. II-12)

This is illustrated below in Figure II-5:

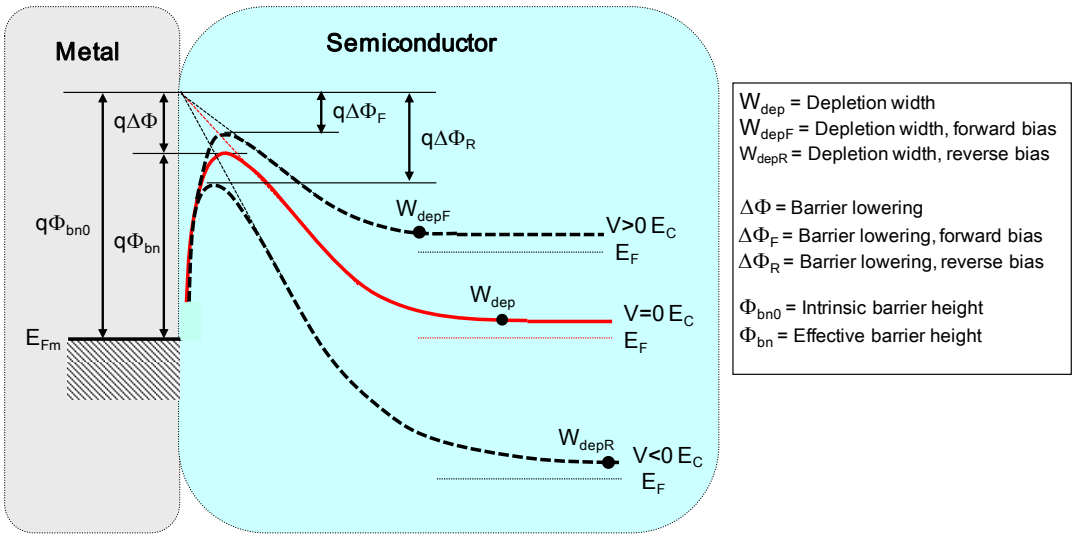

Figure II-5: Bias dependence of the image force-induced barrier lowering, intrinsic and effective SBH.

The value of the permittivity ε_s in (eq. II-11) can be slightly inferior to the static permittivity of the semiconductor. If during the emission process, the transit time between the interface and the maximum of potential energy of the barrier (at x_m) is smaller than the dielectric relaxation time, the semiconductor is not « fully » polarized and one can expect a lower effective permittivity. According to [*Sze'07*], however, the static permittivity approximation is very acceptable in both Si and Ge.

II.1.1.e. Summary

The potential barrier for carriers which builds up when a metal and a semiconductor are in contact is not fully defined by the electron affinity of the semiconductor and the metal workfunction.

In practice, the Fermi-level of the semiconductor is pinned to the interface states charge neutrality level, as strongly as the interface states density is important. In particular in Ge, the controllability of the Schottky Barrier Height by the metal workfunction is reduced to around 5%. The intrinsic barrier heights are to our knowledge always favorable to hole conduction.

In addition, the image force has a field-dependent lowering effect on the barrier and changes its shape. For high doping levels and strong bias conditions, its electrostatic effect is not negligible. In general, its impact on charges tunneling through the barrier and therefore on total current density is expected to be substantial.

In the next section, the main theories for interfacial current calculation in Schottky junctions will be presented.

II.1.2. **Interfacial current transport**

Unlike in p/n junctions, conduction across Schottky junctions relies mostly on majority carriers. If we chose the case of a metallic contact on an n-type semiconductor under forward bias, there are five main transport mechanisms (cf. Figure II-6):

1. Electrons emitted from the semiconductor in the metal above the barrier, often referred to as TE for Thermionic Emission.
2. Electrons tunneling through the barrier, often referred to as FE for Field Emission.
3. Recombination within the Space Charge Region (like in p/n junctions)
4. Diffusion of electrons in the depletion region
5. Diffusion of holes from the metal in the semiconductor (process equivalent to recombination in a neutral region)

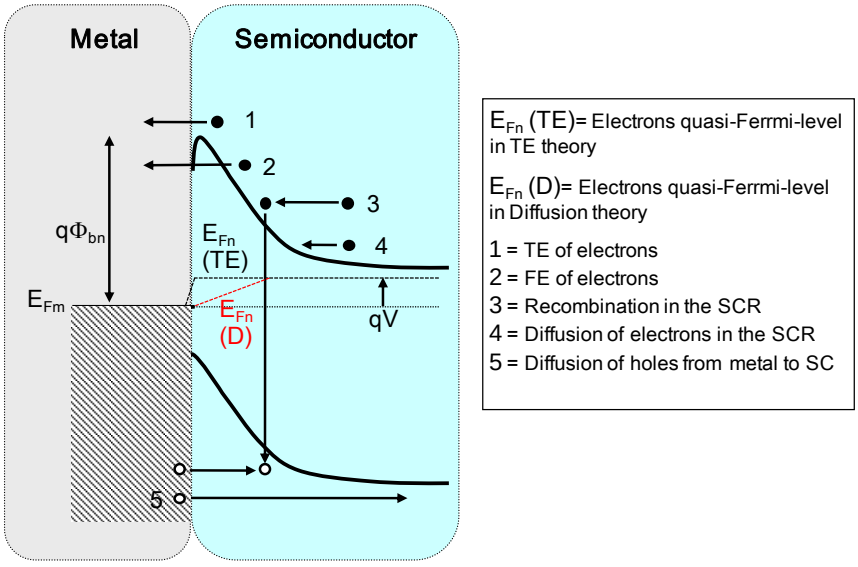

Figure II-6: Illustration of the main transport processes across a forward biased metal/n-type semiconductor junction. The quasi-Fermi level is represented in the cases of TE theory (II.1.2.a.) and diffusion theory (II.1.2.b.)

II.1.2.a. Thermionic Emission (TE) Theory

The thermionic emission model was developed by Bethe in 1942 [*Bethe'42*], and is generally applied to high mobility semiconductors (Si, Ge, GaAs etc.). In the case of low mobility semiconductors, the theory of diffusion (cf. next section) is more adequate.

The TE theory relies on the following assumptions:

- The SBH is much larger than kT (=26 meV @ 300K)
- The thermal equilibrium is established at the plane determining emission

- The existence of a net current flow does not affect the equilibrium so that one can superimpose two current fluxes: one from metal to semiconductor, the other from semiconductor to metal, each with a different quasi-Fermi level. If TE is the limiting process, E_{Fn} is constant throughout the depletion region (cf.Figure II-6).

The shape of the barrier does not matter as according to these hypotheses, the current fluxes depend on its height only. The current density from semiconductor to metal can be obtained by integrating the concentration of electrons having sufficient energies to be emitted above the barrier (between E_{Fn} $+q\Phi_{bn}$-qV and ∞).

$$J_{s\to m} = A^* T^2 \exp\left(-\frac{q\Phi_{bn}}{kT}\right)\exp\left(\frac{qV}{kT}\right)$$

(eq. II-13)

A* is the effective Richardson constant for thermionic emission, neglecting the interactions with optical phonons as well as quantum reflection on the barrier (cf. II.1.2.c.iii). In these conditions, it is defined by:

$$A^* = \frac{4\pi q m^* k^2}{h^3}$$

(eq. II-14)

m* is the majority carriers effective mass (calculation detailed in II.2.6.), and h the Planck constant. The Richardson constant appears when calculating the supply function N(W,E)dWdE (number of electrons with energy within the range E to E+dE whose normal component lies in the range W to W+dW), incident upon the interface plane per area per time) [*Young'59*]. It arises as an energy-independent factor in front of the Fermi-Dirac statistics carrier distribution.

The flux from metal to semiconductor is defined as the opposite of $J_{s\to m}$ in the conditions of thermal equilibrium (V=0).

$$J_{m\to s} = -A^* T^2 \exp\left(-\frac{q\Phi_{bn}}{kT}\right)$$

(eq. II-15)

Hence a total current density ($J_{s\to m}$ + $J_{m\to s}$):

$$J_n = \left[A^* T^2 \exp\left(-\frac{q\Phi_{bn}}{kT}\right)\right]\cdot\left[\exp\left(\frac{qV}{kT}\right)-1\right] = J_{TE}\left[\exp\left(\frac{qV}{kT}\right)-1\right]$$

(eq. II-16)

II.1.2.b. Diffusion Theory

The diffusion theory was initiated by Walter Schottky in 1938 [*Schottky'38*]. It relies on the following hypotheses:

- The SBH is much larger than kT
- The effect of electron collisions in the depletion region (*ie* diffusion) is accounted for
- The carrier concentrations at x=0 and x=W_{dep} are unchanged by the current flow (they conserve their equilibrium values)
- The semiconductor is non-degenerate

The current density equation (here in the case of an n-type semiconductor) is derived from the classical drift-diffusion model. We assume that the energy of the electrons in the conduction band is entirely kinetic (assimilation of the kinetic energy E_c to the potential energy corresponding to the bottom of the conduction band E_C).

$$J_n = q\left(n\mu_n \mathrm{E} + D_n \frac{dn}{dx} \right) = qD_n \left(\frac{n}{kT} \frac{dE_c}{dx} + \frac{dn}{dx} \right)$$

(eq. II-17)

The energy is then integrated over the depletion region between x=0 and x=W_{dep}. This finally yields:

$$J_n = \frac{qN_C D_n \left[\exp\left(\frac{qV}{kT} \right) - 1 \right]}{\int_0^{W_{dep}} \exp\left[\frac{E_c(x)}{kT} \right] dx}$$

(eq. II-18)

The barrier height dependence arises from the potential distribution:

$$E_c(x) = E_C(x) = q\Phi_{bn} - \frac{q^2 N_d}{\varepsilon_s} (W_{dep} x - \frac{x^2}{2})$$

(eq. II-19)

with

$$W_{dep} = \sqrt{\frac{2\varepsilon_s}{qN_d} (\Psi_{bi} - V - \frac{kT}{q})}$$

(eq. II-20)

where Ψ_{bi} is the built-in potential, cf. Figure II-2.

We can note that this theory does not take the image force into account, as (eq. II-19) is derived assuming a maximal electric field in x=0.

$$J_n \approx q\mu_n N_C \mathrm{E}_m \exp\left(-\frac{q\Phi_{bn}}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right] = J_D\left[\exp\left(\frac{qV}{kT}\right)-1\right]$$

(eq. II-21)

The expression in (eq. II-21) is relatively similar to that of the TE theory. However, the reverse saturation current J_D is bias-dependent (cf. E_m) and has a reduced temperature dependence.

According to Rhoderick [*Rhoderick'70*], the analysis of experimental data shows that the diffusion theory is a bad approximation for high mobility semiconductors such as Ge. The TE model seems more adequate, but can be further improved by incorporating some of the elements of the elements above.

II.1.2.c. Thermionic Emission Diffusion (TE-D) Theory

The approach proposed by Crowell and Sze [*Crowell'66-a*] aims at unifying the two previous ones. It is assumed that the barrier is high enough for the charges density between x=0 and $x=W_{dep}$ to be essentially that of the ionized donors (approximation of total depletion). As in the TE theory, a superimposition of two opposite fluxes is considered, but the quasi-Fermi level is not constant in the SCR (cf. diffusion theory). Furthermore, the maximum of potential energy for the electrons is located in $x=x_m$ (cf. (eq. II-9)) instead of x=0, as the image is accounted for.

II.1.2.c.i. Thermionic recombination velocity

The TE-D theory is based on the boundary condition of a thermionic recombination velocity v_R at the metal-semiconductor interface. If the barrier section between x=0 and $x=x_m$ acts as a drain for electrons, the current flow can be described in terms of an effective recombination velocity at the potential energy maximum x_m. Let n_m be the electron concentration at x_m when the current circulates, the total current density is of the form:

$$J = q(n_m - n_0)v_R$$

(eq. II-22)

where n_0 is a « fictional » concentration corresponding to the case $E_{Fn}(x_m)=E_{Fm}$ (cf. E_{Fn} (D) in Figure II-6, as if it was possible to reach equilibrium without changing the position or value of the maximum of E_C):

$$n_0 = N_c \exp\left(-\frac{q\Phi_{bn}}{kT}\right)$$

(eq. II-23)

The (eq. II-22) thus features a bias-dependent term (qn_mv_R) describing the flux from semiconductor to metal, and another bias-independent negative term ($-qn_0v_R$) representing the flux from metal to semiconductor.

II.1.2.c.ii. Effective diffusion velocity

Solving (eq. II-22), an effective diffusion velocity v_D is introduced. It is associated to the transport of electrons from W_{dep} to x_m, for determining n_m:

$$v_D \equiv D_n \exp\left(\frac{q\Phi_{bn}}{kT}\right) \Big/ \int_{x_m}^{W_{dep}} \exp\left(\frac{E_C}{kT}\right) dx$$

(eq. II-24)

The final current density is:

$$J(V) = \frac{qN_C v_R}{1+(v_R/v_D)} \exp\left(-\frac{q\Phi_{bn}}{kT}\right) \cdot \left[\exp\left(\frac{qV}{kT}\right) - 1\right] = J_{TED}\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

(eq. II-25)

- The predominance of the TE or the diffusion regime varies according to the relative values of v_R and v_D.
- The assumption of total depletion enables to approximate v_D by $\mu_n E_m$ [*Rhoderick'88*].
- If the electrons distribution is Maxwellian for $x \geq x_m$ and if the electrons circulating from metal to semiconductor are entirely determined by the current density qn_0v_R, then the semiconductor behaves as a thermionic emitter and v_R is the thermal velocity A^*T^2/qN_C; (eq. II-25) can be rewritten as:

$$J(V) = \frac{A^*T^2}{1+(v_R/v_D)} \exp\left(-\frac{q\Phi_{bn}}{kT}\right) \cdot \left[\exp\left(\frac{qV}{kT}\right) - 1\right] = J_{TED}\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

(eq. II-26)

- If $v_D >> v_R$ (case of high mobility semiconductors), then (eq. II-26) is limited by v_R and $J_{TED} \approx J_{TE}$. The criterion $\mu E_m >> v_R$ is more rigorous than the one introduced by Bethe [*Bethe'42*] ($E_m > kT/q\lambda$ with λ the mean free path).
- If $v_R >> v_D$ (case of low mobility semiconductors), then (eq. II-26) is limited by v_D and $J_{TED} \approx J_D$.

II.1.2.c.iii. Interactions with optical phonons, quantum tunneling and reflection

In this paragraph, we shall evoke the way optical phonon backscattering and the transmission through the barrier are handled in the TE-D theory.

In most of the cases, there is a non negligible probability for an electron to interact with optical phonons in the vicinity of the potential energy maximum, and to be back-scattered [*Crowell'65*],[*Kao'80*]. A first approximation of the emission probability over the barrier could be:

$$f_p = \exp(-x_m / \lambda)$$

(eq. II-27)

Moreover, the distribution of electrons withstands a distortion due to the fact that electrons can either tunnel through or be reflected by the barrier [*Crowell'66-b*],[*Chang'70*]. The ratio of the total current flows with and without accounting for these effects is noted f_q. These modifications can be implemented by introducing the effective reduced Richardson constant A^{**}:

$$A^{**} = \frac{f_p f_q A^*}{1 + (f_p f_q v_R / v_D)}$$

(eq. II-28)

The final expression is then similar to that of the TE theory, replacing A^* with A^{**}:

$$J(V) = A^{**} T^2 \exp\left(-\frac{q\Phi_{bn}}{kT}\right) \cdot \left[\exp\left(\frac{qV}{kT}\right) - 1\right] = J_{TED}\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

(eq. II-29)

In practice yet, the implementation of field-dependent A^{**} is not easy. It can differ from A^* by as much as 50% in Si [*Andrews'70*] according to doping, temperature and bias. The next section will deal with a more direct approach to Field-Emission current.

II.1.2.d. Field-Effect Emission (FE)

The previously introduced approaches, including the synthetic Thermionic Emission – Diffusion theory are essentially designed for moderately doped semiconductors in forward bias where TE is the predominant transport process.

In numerous cases however, and especially under reverse bias (a case of prime importance for us, as the Source is reverse-biased for carriers injection in a Schottky MOSFET, as we will see in the next Chapter), a tunneling component appears which is no longer negligible, and which requires a deeper analysis than the introduction of a variable effective reduced Richardson "constant".

II.1.2.d.i. Ideality factor

The field-effect current density circulating from the semiconductor towards the metal is proportional to the transmission coefficient multiplied by the occupation probability in the semiconductor, and the vacancy probability in the metal.

$$J_{s\to m} = \frac{A^{**}T^2}{kT}\int_{E_{Fm}}^{q\Phi_{bn}} f_S TR(E)(1-f_M)dE$$

(eq. II-30)

The probabilities are swapped to obtain the flux in the opposite direction:

$$J_{m\to s} = \frac{A^{**}T^2}{kT}\int_{E_{Fm}}^{q\Phi_{bn}} f_M TR(E)(1-f_S)dE$$

(eq. II-31)

These calculations are not immediate, and it can be practical to introduce an experimentally determined ideality factor η.

$$J = J_0\left[\exp\left(\frac{qV}{\eta kT}\right)-1\right]$$

(eq. II-32)

J_0 is the reverse saturation current density, and can be extracted by an extrapolation at V=0V of a J-V characteristic curve. In the « ideal » case of pure thermionic emission, $J_0=J_{TE}$ and η=1. With increasing semiconductor doping (typically $N_d>10^{17}cm^{-3}$) and/or decreasing temperature, both J_0 and η increase.

This approach is used in a large majority of publications, for cases with low semiconductor doping. Thus, J_0 is roughly constant (and function of the SBH as is J_{TE}), η is somewhat close to 1 and is an indicator of the quality of the Φ_b extraction. The closer it is to unity, the more reliable the SBH extraction using J_{TE}.

Nonetheless, the interpretations allowed by this model remain very qualitative. If η is far from 1, the only useful conclusion would be that the current cannot be considered as purely thermionic and that the extracted Φ_b value is therefore "somewhat" incorrect.

II.1.2.d.ii. A simplified analytical approach

Without having to actually compute the integrals (eq. II-30) and (eq. II-31) (which will be carried out in II.3.3.), we will now review a more in-depth analysis comprehending Field-effect current proposed by Padovani and Stratton [*Padovani'66*]. The first step is to consider three co-existing transport regimes, one of which dominates over the others at zero bias according to doping, temperature and bias conditions.

- Thermionic emission (TE regime)
- Field emission (FE regime) concerning the charges of energy equal to or below the Fermi level tunneling through the potential barrier
- Thermionic Field Emission (TFE regime), concerning the carriers transmitted at energies for which the barrier is thinner, having received a thermal energy kT

It is probably one of the most comprehensive simplified description of interfacial current, along with the model of Crowell and Rideout [*Crowell'69-a*] which describes the continuous variation from one regime to the other, unfortunately without accounting for the image force. The Figure II-7 below illustrates this decomposition into three regimes in the case of an n-type degenerate semiconductor.

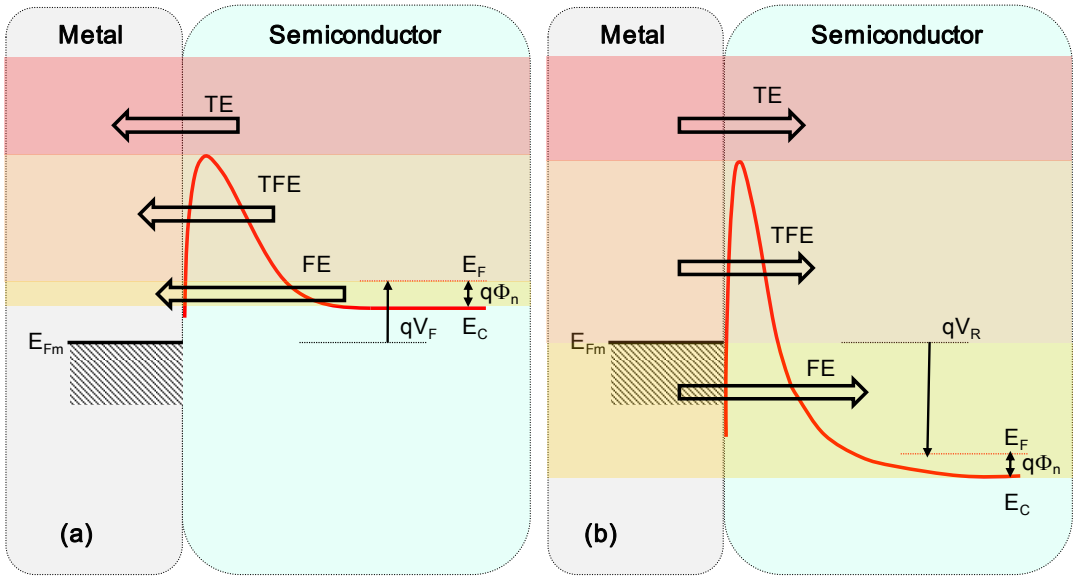

Figure II-7: Decomposition of the electron interfacial current into three regimes for a metallic contact on a degenerate n-type semiconductor under (a) forward bias and (b) reverse bias.

A rough criterion allows discriminating the dominant current transport mechanism. Let E_{00} be the energy defined as follows:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_d}{m_T^* \varepsilon_s}}$$

(eq. II-33)

This energy is characteristic of a material for given doping conditions, and is linked to the Wentzel-Kramers-Brillouin (WKB) expression of the transmission coefficient for carriers with zero energy. m_T* the tunneling effective mass of the majority carriers (not to be confused with the effective mass for calculation of the Richardson constant (eq. II-14), cf.II.2.6.b.), and N_d is the ionized donors concentration.

- If $E_{00} << kT$, the TE regime is most likely dominant.
- If $E_{00} >> kT$, the FE regime is dominant.
- If $E_{00} \approx kT$, the TFE regime should be dominant.

<u>Under forward bias V_F:</u>

The FE current density can be expressed as:

$$J_{FE} = \frac{A^{**}T\pi \exp\left[-q\left(\Phi_{bn} - V_F\right)/E_{00}\right]}{c_1 k \sin(c_1 \pi k T)}\left[1 - \exp\left(-c_1 q V_F\right)\right]$$

(eq. II-34)

with

$$c_1 \equiv \frac{1}{2E_{00}} \log\left[\frac{4\left(\Phi_{bn} - V_F\right)}{-\Phi_n}\right]$$

(eq. II-35)

Φ_n is a negative potential in the case of a degenerate semiconductor. We can note that the temperature dependence is no longer featured in the exponential term. The low temperature dependence with respect to thermionic emission is indeed characteristic of tunnel conduction.

The current density in TFE regime can be expressed as follows:

$$J_{TFE} = \frac{A^{**}T\sqrt{\pi E_{00} q\left(\Phi_{bn} - \Phi_n - V_F\right)}}{k\cosh(E_{00}/kT)} \exp\left[-\frac{q\Phi_n}{kT} - \frac{q\left(\Phi_{bn} - \Phi_n\right)}{E_0}\right] \exp\left(\frac{qV_F}{E_0}\right)$$

(eq. II-36)

with

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right)$$

(eq. II-37)

Under reverse bias V_R:

The FE current density is given by:

$$J_{FE} = A^{**}\left(\frac{E_{00}}{k}\right)^2 \left(\frac{\Phi_{bn} + V_R}{\Phi_{bn}}\right) \exp\left(-\frac{2q\Phi_{bn}^{3/2}}{3E_{00}\sqrt{\Phi_{bn} + V_R}}\right)$$

(eq. II-38)

And finally the TFE current density is:

$$J_{TFE} = \frac{A^{**}T}{k}\sqrt{\pi E_{00} q\left[V_R + \frac{\Phi_{bn}}{\cosh^2\left(E_{00}/kT\right)}\right]} \exp\left(-\frac{q\Phi_{bn}}{E_0}\right) \exp\left(\frac{qV_R}{\varepsilon'}\right)$$

(eq. II-39)

with

$$\varepsilon' = \frac{E_{00}}{E_{00}/kT - \tanh(E_{00}/kT)}$$

(eq. II-40)

These expressions may seem complex, but are relatively easy to use once the various parameters have been defined. In particular, they can be used to derive the specific contact resistivity in the case of ohmic contacts (cf. II.2.5.).

Important remarks:

Some more refined discriminating criteria than the comparison between kT and E_{00} exist in order to identify the dominant current transport process at zero bias. Those are discussed in [*Crowell'69-a*] for various transitions, and whether the semiconductor is degenerate or not (cf. II.2.6.b.ii).

The forward bias equations do not connect at zero bias with the reverse bias cases. As a matter of fact, the reverse bias expressions do not go through zero for V=0. This weakness of Padovani and Stratton's theory [*Padovani'66*] is pointed out in the Appendix of [*Crowell'69-a*] and is attributed to a mistake in algebraic calculations. The expressions for forward biases seem more reliable.

The notion of effective barrier height resulting from image force lowering is included in the current density expressions. However, writing $\Delta\Phi$ as a function of the forward bias yields (according to (eq. II-11)):

$$\Delta\Phi = \left[\frac{q^3 N_d \left(\Phi_{bn0} - \Phi_n - V_F \right)}{8\pi^2 \varepsilon_s^3} \right]^{1/4}$$

(eq. II-41)

(the lowering decreases with increasing V). The quantity between brackets becomes negative for typically a few hundreds of mV (when the semiconductor goes from depletion to accumulation), and $\Delta\Phi$ becomes imaginary. Thus, this model is unfortunately applicable at low values of V_F only.

From the two previous observations follows that it is not really recommended to rely on (eq. II-34) and (eq. II-38) (in FE regime) or (eq. II-36) and (eq. II-39) (in TFE regime) to try and re-create a J-V diode characteristic curve. The principal interest will be to derive from the current density expression a specific contact resistivity as a function of the SBH (cf. II.2.5.).

II.1.2.e. Minority carriers injection

We have so far only considered the current owing to the transport of majority carriers. We will now briefly evoke the contribution of the minority carriers (*ie* holes in the case of an n-type semiconductor) to the total current. At low bias, this contribution is negligible because the diffusion of minority carriers is lower by orders of magnitude than the TE or FE

conduction of majority carriers. But when the electric field increases, the drift of minority carriers can be considered.

Let J_{n0} be the pre-exponential term of the majority carrier current (J_{TE}, J_D, J_{TED}, J_{TFE}, J_{FE}…) and L the length of the quasi-neutral region, the injection ratio is given by:

$$\frac{J_p}{J_p + J_n} = \frac{\mu_p n_i^2 J_n}{\mu_n N_d^2 J_{n0}} + \frac{qD_p n_i^2}{N_D L J_{n0}}$$

(eq. II-42)

The second term is bias-independent and corresponds to the ratio at low field. The first term corresponds to the minority carriers drift and can significantly increase at high current densities. According to [*Sze'07*], in the case of a Au/n-Si barrier with ($N_d=10^{15}cm^{-3}$), this ratio yields 5×10^{-4} at $J_{n0}=5\times10^{-7}A.cm^{-2}$ (low bias), and increases to 5% at $J_{n0}=350A.cm^{-2}$.

II.1.2.f. Interfacial layer – Tunnel Effect MIS diode

It can occur that an interfacial insulating layer (1-3nm thick) is formed (voluntarily or not) before metal deposition, creating a tunneling MIS (Metal Insulator Semiconductor) junction. The characteristics of this type of structure with respect to a metal/semiconductor contact:

- A reduced current especially at low field
- A lower barrier (due to the potential drop in the interfacial layer)
- A higher ideality factor
- Possibly Fermi-level depinning as the interface states density can be modified

Andrews and Koch [*Andrews'71*] propose the following approximation of the current density:

$$J = A^* T^2 \exp(-\sqrt{\zeta}\delta)\exp\left(-\frac{q\Phi_b}{kT}\right)\left[\exp\left(\frac{qV}{\eta kT}\right)-1\right]$$

(eq. II-43)

ζ (in eV) and δ (in Å) are respectively the effective barrier and the interfacial layer thickness. It is basically (eq. II-32) (TE regime) modulated by a tunneling probability $\exp(-\sqrt{\zeta}\delta)$ reducing the current density.

The ideality factor η becomes [*Andrews'71*]:

$$\eta = 1 + \left(\frac{\delta}{\varepsilon_i}\right)\frac{\left(\varepsilon_s / W_{dep}\right) + qD_{its}}{1 + \left(\delta / \varepsilon_i\right)qD_{itm}}$$

(eq. II-44)

where D_{its} and D_{itm} are respectively the semiconductor and metal interface trap densities at equilibrium.

Finally, we can observe that the MIS tunnel diode reduces the emission of majority carriers without influencing the diffusion of minority carriers, enhancing the injection ratio at low field (eq. II-42).

II.1.2.g. Summary

The theory of diffusion [*Schottky'38*] has been incorporated in the « classical » Thermionic Emission model [*Bethe'42*] through the use of the effective reduced Richardson constant A^{**}. Yet, the latter and its dependence on the electric field remain difficult to evaluate. It is reasonable for high mobility semiconductor (such as Ge) to conserve the pure thermionic approach, as the effective diffusion velocity of majority carriers in the Space Charge Region is large with respect to the thermionic recombination velocity. The use of the (simpler to calculate) effective Richardson constant A^{*} can be justified.

However, these models and their variations are mostly suitable to predict the behavior of the junction junctions with large barriers, low doping, and in forward regime (carriers circulating from semiconductor in the metal). The case in which we are interested in for the targeted applications is:

- Low barriers for injection efficiency
- Possibly high doping to further decrease the barrier height
- Reverse bias conditions as in Schottky MOSFETs operation, the carriers are injected from the metallic Source into the semiconductor channel

In these cases, the assumption of a reverse saturation current depending only on the barrier height, and neglecting the barrier shape conditioning Field Emission across the barrier is no longer acceptable.

Taking into account the Field Emission component is not immediate, as one has to integrate the probabilities of occupancy and vacancy on each side of the junction, times the transmission coefficient. At least two simplified modelling approaches can be used.

The first one, using an ideality factor η to evaluate the extent of which the characteristics stray from the pure TE case in forward regime, remains very qualitative.
The second one [*Padovani'66*], [*Crowell'69-a*] with simplified current density expressions adapted to the cases of Thermionic Field Emission (TFE) and Field-Emission (FE) seems more advanced. In spite of imperfections casting doubt on the relevance of a comparison between the model and experimental J-V characteristics (mostly reliable for small values of forward biases), its advantage is the possibility of deriving specific contact resistivities for ohmic or quasi-ohmic contacts on degenerate semiconductors.

All of these models describe the current of majority carriers, assuming that no interfacial layer separates the metal from the semiconductor. At high field, the drift of minority carriers might have to be considered for lightly doped semiconductors. At low field,

the presence of an insulating layer (1-3nm thick) is likely to modify the Fermi-level pinning as well as the majority carriers current density.

The next section will provide a link with experimental characterization of the electrical metal/semiconductor contact properties.

II.2. Experimental characterization methods

II.2.1. **Method based on I-V characteristics**

For lightly doped semiconductors and large barriers, according to (eq. II-29) (TE-D theory), the current density in **forward bias** can be expressed as follows:

$$J_F = A^{**}T^2 \exp\left(-\frac{q\Phi_{bn0}}{kT}\right)\exp\left(\frac{q\Delta\Phi}{kT}\right)\exp\left(\frac{qV}{kT}\right) = J_0 \exp\left(\frac{qV}{kT}\right)$$

(eq. II-45)

As previously seen (II.1.2.d.i), a tunneling current component might exist and have to be accounted for through the introduction of an ideality factor (eq. II-32):

$$J_F = J_0 \exp\left(\frac{qV}{\eta kT}\right)$$

(eq. II-46)

From the measured characteristics, J_0 is obtained by an extrapolation of the forward current to V=0 (Figure II-8). The ideality factor is then (as $\Delta\Phi$ and A^{**} depend on V):

$$\eta \equiv \frac{q}{kT}\frac{1}{\frac{d(\ln J)}{dV}} = \left[1 + \frac{d\Delta\Phi}{dV} + \frac{kT}{q}\frac{d(\ln A^{**})}{dV}\right]^{-1}$$

(eq. II-47)

Experimentally, η is obtained by the slope of the linear interpolation at low forward bias (Figure II-8). If it is close to unity, then with a good approximation:

$$\Phi_{bn} = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_0}\right)$$

(eq. II-48)

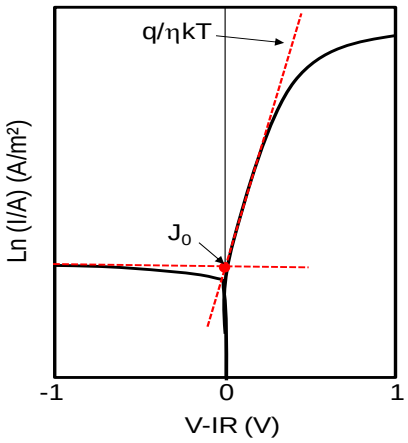

Figure II-8: Principle of SBH extraction from a diode current-voltage characteristic curve. If η is equal to 1, the SBH Φ_{bn} can be derived from J_0 with (eq. II-48).

If it is not, then the extraction is inaccurate. In addition, this technique requires the knowledge of the electrically active contact area (to obtain J), eliminating the effect of series resistance so as to consider the true bias dependence, and accurately evaluating A^{**}.

II.2.2. **Activation energy method**

The advantage of the activation energy approach over the previous one is that the knowledge of the diode area and of the Richardson constant do not influence the value of the extracted SBH. From (eq. II-29) we derive, for a given forward bias V_F and junction area A:

$$\ln\left(\frac{I_F}{T^2}\right) = \ln\left(AA^{**}\right) - \frac{q\left(\Phi_{bn} - V_F\right)}{kT}$$

(eq. II-49)

where $q(\Phi_{bn}-V_F)$ is homogenous to an activation energy E_a. For a reasonable range of temperatures around 300K, A^{**} and Φ_{bn} can be considered constant. Thus, at a fixed V_F, plotting $\ln(I_F/T^2)$ versus 1/T (Arrhenius plot, or Richardson plot) yields AA^{**} (y-intercept), and Φ_{bn} (slope).

However, if the transport is not purely thermionic, the current density no longer follows an Arrhenius law, the linear fitting becomes approximate and the extraction inaccurate.

II.2.3. **Method based on C-V characteristics**

The C-V method is relatively simple to implement, and consists in plotting $1/C^2$ as a function of the bias applied to the contact (C being the metal/semiconductor capacitance). The intercept with the x-axis V_B is linked to the built-in potential Ψ_{bi}. The slope gives information on the carrier concentration, useful to determine Φ_n. The following relationship is then used [*Goodman'63*]:

$$\Phi_{bn} = V_B + \frac{kT}{q} + \Phi_n = \Psi_{bi} + \Phi_n$$

(eq. II-50)

Unfortunately, the technique is restricted to large barrier heights (much larger than kT/q), and to non-degenerate semiconductors.

II.2.4. **Photoelectric measurement**

The photoelectric measurement is a direct method to evaluate the barrier height [*Crowell'62*]. It consists in illuminating a sample by a monochromatic light with an energy lying between the barrier height and the size of the bandgap (in order to enable emission above the barrier without provoking band-to-band recombination) $q\Phi_{bn}<h\nu<E_g$. The semiconductor is transparent at these wavelengths, but the metal layer should be thin enough to permit the illumination of the interface (Figure II-9).

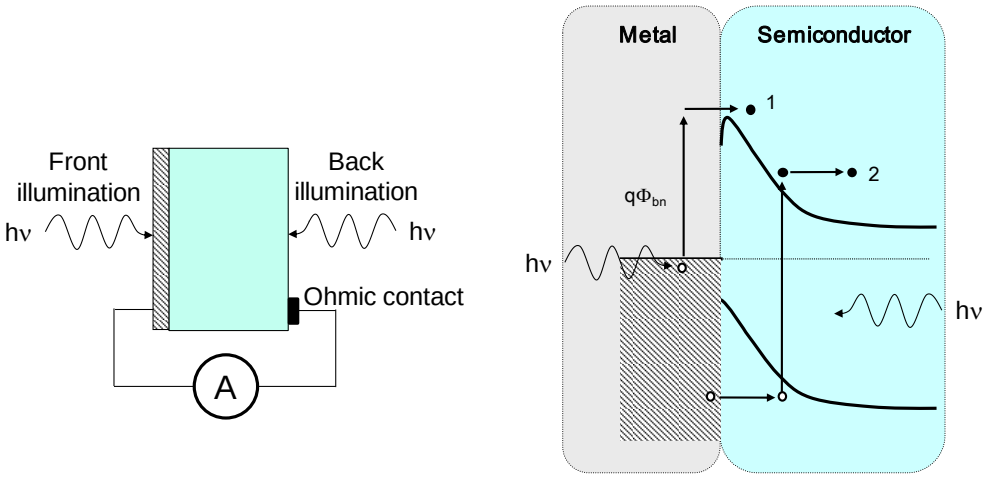

Figure II-9: Experimental settings of the photoelectric measurement, and simplified band diagram showing (1) emission above the barrier (2) band-to-band recombination (to be avoided, if $h\nu>E_g$).

The current response R per absorbed photon is given as a function of the energy hν by the Fowler theory [*Fowler'31*]:

$$R \propto \frac{T^2}{\sqrt{E_s - h\nu}} \left\{ \frac{x^2}{2} + \frac{\pi^2}{6} - \left[\exp(-x) - \frac{\exp(-2x)}{4} - \frac{\exp(-3x)}{9} - ... \right] \right\}$$

(eq. II-51)

for $x \geq 0$. E_s is the sum of $h\nu_0$ (equal to the barrier height $q\Phi_{bn}$) and of the Fermi level (relative to the bottom of the conduction band), and $x=h(\nu-\nu_0)/kT$. Under the conditions $E_s >> h\nu$ and $x>3$, (eq. II-51) can be reduced to:

$$R \propto (h\nu - h\nu_0)^2$$

(eq. II-52)

Plotting the photo-response R versus the photon energy $h\nu$, the intercept with the x-axis gives the Schottky Barrier Height.

A limitation to this method could be the necessity of realizing an ohmic contact on the semiconductor for current measurement (cf. Figure II-9). Additionally, the barrier to be characterized has to be larger than that of this "ohmic" contact.

II.2.5. **Cases of ohmic and quasi-ohmic contacts**

A metal-semiconductor ohmic contact is defined by having a negligible junction resistance with respect to the total resistance of the device to which it belongs. Sometimes however, this condition is fulfilled for junction with non-linear current-voltage characteristics (steeper slope under forward bias than in high reverse bias conditions). In this case, we can talk about quasi-ohmic contacts.

The specific contact resistivity is a macroscopic parameter defined as the reciprocal of the derivative of the current density with respect to the voltage. When the voltage tends toward zero, it is an important figure of merit of the quality of the ohmic contact.

$$\rho_c = \left(\frac{dJ}{dV} \right)^{-1}_{V=0}$$

(eq. II-53)

Thus, it is possible to derive the current densities expressions of Padovani and Stratton [*Padovani'66*], and this way to obtain the relationship between contact resistivity and barrier height:

- In TE dominant regime (eq. II-16):

$$\rho_c = \frac{k}{A^{**}Tq} \exp\left(\frac{q\Phi_{bn}}{kT} \right)$$

(eq. II-54)

- In TFE dominant regime (eq. II-36):

$$\rho_c = \frac{k\sqrt{E_{00}}\cosh(E_{00}/kT)\coth(E_{00}/kT)}{A^{**}Tq\sqrt{\pi q\left(\Phi_{bn}-\Phi_n\right)}}\exp\left[\frac{q\left(\Phi_{bn}-\Phi_n\right)}{E_{00}\coth(E_{00}/kT)}+\frac{q\Phi_n}{kT}\right]$$

(eq. II-55)

- In FE dominant regime (eq. II-34):

$$\rho_c = \frac{k\sin(\pi c_1 kT)}{A^{**}\pi qT}\exp\left(\frac{q\Phi_{bn}}{E_{00}}\right)$$

(eq. II-56)

The quantity c_1 is that of (eq. II-35).

This specific contact resistivity ρ_c can be linked to the contact resistance R_{co} measured on an I-V characteristic curve by Berger's TLM model [*Berger'72*]. If W_c is the contact width (dimension perpendicular to the direction of transport), L_c its length, and ρ_{sd} the resistivity of the doped semiconductor layer:

$$R_{co} = \frac{\sqrt{\rho_c\rho_{sd}}}{W_c}\coth\left(L_c\sqrt{\frac{\rho_{sd}}{\rho_c}}\right)$$

(eq. II-57)

The above equation takes into account the non-uniformity of current density across contacts of large dimensions. The simpler relationship according to which the resistance is obtained by multiplying the resistivity with the contact area is only the short-contact limit case.

II.2.6. **Practical examples for low and thin Schottky barriers**

II.2.6.a. Low barriers on moderately doped Si

Two fundamental experimental issues when characterizing a metal/moderately-doped semiconductor diode are:

- How to collect the current without blurring the information by the introduction of another Schottky contact (*eg* metallic probe on the moderately doped semiconductor)
- How to eliminate the resistive contribution of the moderately doped semiconductor on the current-voltage characteristics, especially if it is larger than the contact resistance (case of low barriers)

The experimental setup and modelling presented in [*Dubois'04*] addresses both these limitations for low-barrier Schottky contacts on Si. First of all, two identical back-to-back Schottky diodes are fabricated, so as to obtain a symmetrical circuit (Figure II-10).

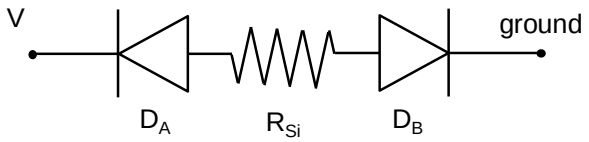

Figure II-10: Equivalent circuit corresponding to two back-to-back Schottky diodes separated by the Si series resistance [Dubois'04].

In the case where the potential drop across the Silicon series resistance is negligible, the current is limited by D_B is reverse operation for positive values of V, and the identical D_A reverse regime for negative values of V.

Second, when the substrate is doped up to a few 10^{15}at.cm^{-3}, and if the Schottky barrier is intrinsically low, extraction methods based on current-voltage characteristics or activation energy become inaccurate, as the resistance observed mostly owes to R_{Si}. Nonetheless, one can effectively reduce the R_{Si} relative contribution by lowering the temperature. In this work [*Dubois'04*], $R_{Si}(T)$ could be modeled as follows:

$$R_{Si}(T) = R_{Si}(300) \cdot \left(\frac{T}{300} \right)^{\alpha}$$

(eq. II-58)

with α=1.5 and $R_{Si}(300)$=98Ω.

Thus, the extraction takes place in **reverse regime** and at **low temperature**, for which the **tunneling component can be significant**. The approach chosen for extraction in this work was that of Crowell and Rideout [*Crowell'69-a*], which presents the advantage of describing continuously the transition from pure field-emission to pure thermionic emission. Furthermore, the influence of barrier lowering which this model lacks has been taken into account. Fitting with Arrhenius plots lead to the following conclusions:

- The implementation of Barrier lowering greatly enhances the agreement with the bias dependence at low temperature of experimental data.
- Achieving a perfect reproduction of both the temperature and bias dependence considering only TE or TFE is difficult, especially at low temperature. Nevertheless, it is possible to extract a barrier height with a satisfactory accuracy.
- The TE current density expression (+barrier lowering) provides a better modelling than the TFE one, overestimating the current level. Therefore TE seems accurate enough to model low barriers on moderately doped semiconductors.

II.2.6.b. Barriers on highly doped Ge

This paragraph shows a practical implementation of the method described in II.2.5. , applied to the case of SBH extraction on highly-doped p- and n-type (001)Ge [*Hutin'09*] (previous work on contacts on highly-doped Si: [*Varahramyan'96*])[1]. The samples in this work were made out of 200mm GeOI wafers obtained by Smart Cut™ process with Ge(001) epitaxially grown on Si(001) donor wafers. The active areas, defined by mesa etching, were implanted with BF_2 (respectively As). Concerning the electrically active dopant concentrations, the knowledge of the implanted impurity depth profile (by Secondary Ion Mass Spectroscopy or Monte Carlo simulation in similar conditions) combined with local sheet resistance and ellipsometric Ge thickness measurements yielded $N_a=3.5\times10^{19}$ at.cm^{-3} (respectively $N_d=3\times10^{18}$ at.cm^{-3}). Cross-Bridge Kelvin Resistor (CBKR) structures of various contact side lengths L_c were patterned for contact resistance R_{co} measurements (Figure II-11).

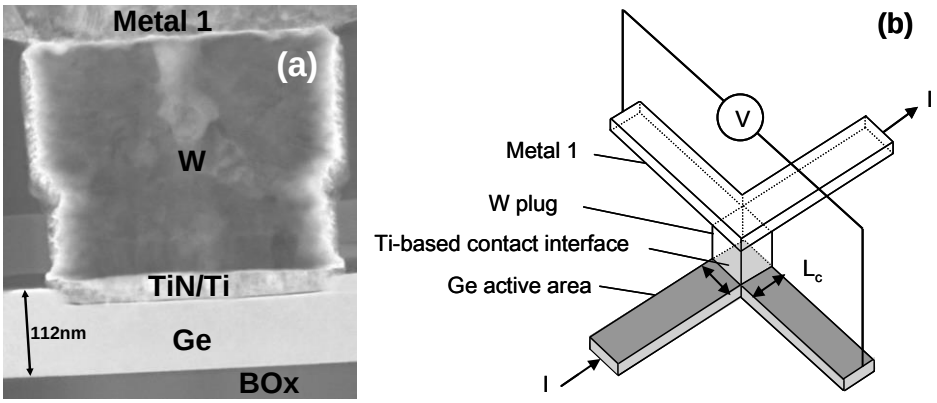

Figure II-11: (a) Cross-Sectional Scanning Transmission Electron Microscopy (XSTEM) picture of a contact stack on GeOI. Ti is deposited on the contact bottom and sidewalls as a precursor for TiN, which prevents W diffusion (picture by F. Aussenac). (b) Cross-Bridge Kelvin Resistor (CBKR) structure for contact resistance (R_{co}) measurement.

With known R_{co}, ρ_{sd} and contact dimensions, the best fitting values for specific contact resistivity (eq. II-57) were $\rho_c=3.1\times10^{-8}$ Ω.cm^2 on p-doped Ge and $\rho_c=1.6\times10^{-5}$ Ω.cm^2 on n-doped Ge (Figure II-12). As a reference point, a maximum contact resistivity of $\rho_c=4\times10^{-8}$ Ω.cm^2 is expected for Fully Depleted SOI by year 2015, according to the 2009 edition of ITRS [*ITRS'09*]. The difference of several orders of magnitude between the contact resistivities of p-doped and n-doped samples is typical of metal/Germanium contacts with a strong pinning close to the valence band (Figure II-3).

[1] The results shown in this section derive from a simplified modeling of the interfacial current, relying on the assumption of a single dominant current transport process. For a further detailed and quantitatively more accurate analysis, please refer to section II.3.4.

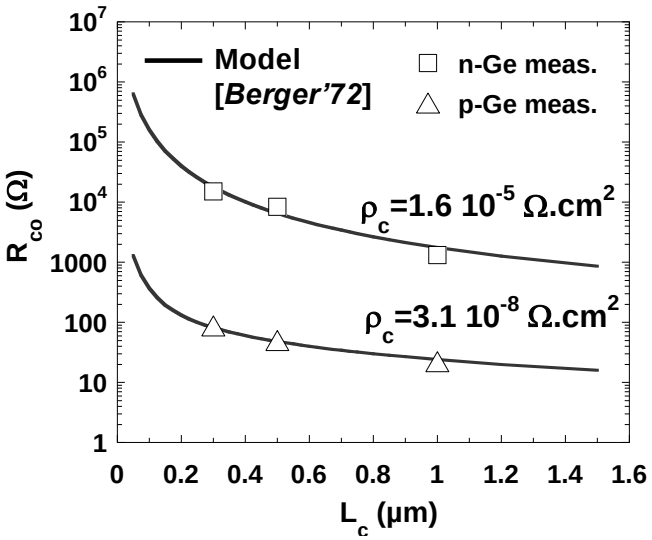

Figure II-12: Measured R_{co} on CBKR structures for various L_c on p- and n-doped GeOI. The extraction of ρ_c is performed by fitting with Berger's model [Berger'72].

The first step before identifying the dominant current transport process at zero bias, and therefore the correct expression linking ρ_c to the SBH is to properly evaluate the needed parameters, in the case of transport along <100> in Ge.

II.2.6.b.i. Determining the parameters

First of all, the calculation of the effective Richardson constant requires the knowledge of an effective mass for thermionic emission (eq. II-14). For one given constant energy ellipsoidal surface in the reciprocal space: if l, m and n are the direction cosines of the current density relative to the principal axes of the ellipsoid; m_x, m_y and m_z the corresponding components of the effective mass tensor, then the contribution m_i* to m* is [*Crowell'69-b*]:

$$m_i^* = \left(l^2 m_y m_z + m^2 m_z m_x + n^2 m_x m_y\right)^{1/2} \quad ; \quad m^* = \sum_i m_i^*$$

(eq. II-59)

In Ge, there are eight ellipsoids of minimal energy for the conduction band located on the <111> direction of the reciprocal space. As each of them is centered on the boundary of the first Brillouin zone, four equivalent ellipsoids (eight half ellipsoids) should be considered. In these samples, the conduction occurs perpendicularly to the (100) surface. Hence, Table II-1 reports m* values obtained by projection on the <100> direction ($m_x=m_l$; $l^2=1/3$; $m_y=m_t$; $m^2=2/3$; $m_z=m_t$; $n^2=0$).

Regarding the valence band energy maxima, we considered in this study the parabolic bands approximation near **k**=**0** (Γ) for light and heavy holes. This implies isotropic effective

masses ($m_x=m_y=m_z$), constant energy spheres centered on Γ ($l^2=1$; $m^2=n^2=0$) and a simplified result: $m^*=m_{lh}+m_{hh}$.

On the other hand, the tunneling effective mass in the direction of emission m_T^* is given for electrons by [*Crowell'69-b*]:

$$\frac{1}{m_T^*}=\frac{l^2}{m_x}+\frac{m^2}{m_y}+\frac{n^2}{m_z}$$

(eq. II-60)

For holes, (eq. II-60) gives $m_{Thh}^*=m_{hh}$ and $m_{Tlh}^*=m_{lh}$. With the coexistence of two non equivalent spheres of constant energy for light and heavy holes, we chose to consider separately the current components due to each type of carrier, and summed them in the end ($J_{tot}=J_{lh}+J_{hh}$). Note that **this is not equivalent to summing the effective masses** (cf. square root term in (eq. II-33) and nonlinear dependence on E_{00} in the current density expressions (eq. II-34) and (eq. II-36)). This requires additionally the knowledge of the light (respectively heavy) holes over total holes concentration ratio p_l/p (respectively p_h/p), in order to properly weigh the equations involving Φ_p and N_a (in particular $\Delta\Phi_{bp}$ (eq. II-11) and E_{00} (eq. II-33)). Assuming a three dimensional holes gas, the density of states in the valence band is proportional to the effective mass to the power 3/2:

$$\frac{p_l}{p}=\frac{m_{lh}^{3/2}}{m_{hh}^{3/2}+m_{lh}^{3/2}} \quad ; \quad \frac{p_h}{p}=\frac{m_{hh}^{3/2}}{m_{hh}^{3/2}+m_{lh}^{3/2}}$$

(eq. II-61)

Concerning the Richardson constant, numerical applications at 300K for our doping conditions showed $v_R>>v_D$ (cf. (eq. II-14) and (eq. II-28)). We hence used the approximation $A^{**}\approx A^*$ for calculations.

Parameters	**n-Ge<100>**	**p-Ge (isotropic)**
Longitudinal effective mass m_l (kg)	1.59 m_0	-
Transverse effective mass m_t (kg)	0.082 m_0	-
Light holes effective mass m_{lh} (kg)	-	0.043 m_0
Heavy holes effective mass m_{hh} (kg)	-	0.3 m_0
Density of states in the conduction band N_C at 300K (cm^{-3})	1.04×10^{19}	
Density of states in the valence band N_V at 300K (cm^{-3})	2.24×10^{17} (light holes) 4.12×10^{18} (heavy holes)	
Effective mass for the Richardson constant m* (kg)	1.19 m_0	0.343 m_0
Effective Richardson constant A* ($A.cm^{-2}.K^{-2}$)	143	40.86
Tunneling effective mass m_T* (kg)	0.12 m_0	0.043 m_0 (light holes) 0.3 m_0 (heavy holes)
Heavy holes ratio p_{hh}/p at zero bias	0.95	
Light holes ratio p_{lh}/p at zero bias	0.05	
Permittivity ε_s ($F.m^{-1}$)	16.2 ε_0	

Table II-1 : Germanium parameters used for calculations at T=300K.
m_0 is the electron rest mass (kg), and ε_0 the vacuum permittivity ($F.m^{-1}$).

II.2.6.b.ii. Determining the dominant current transport process

As seen in II.1.2.d.ii, TE, TFE and FE regime are predominant when respectively: $kT/E_{00}>>1$, $kT/E_{00}\sim1$, and $kT/E_{00}<<1$ (criterion for a first order evaluation). At 300K in Ge, the conditions on doping for $E_{00}=kT$ would be roughly $N_d=3.5\times10^{18}$ at.cm^{-3} or $N_a=10^{19}$ at.cm^{-3}. Having for p- and n-type samples E_{00} energies close or superior to kT, TFE and FE dominant regimes will be considered in the following.

A refined analysis based on a more accurate criterion reveals that the dominant transport process is TFE for the n-doped samples and FE for the p-doped samples. The TFE to FE transition for degenerate semiconductors was examined by Crowell and Rideout [*Crowell'69-a*]. The forward bias $V_{f\text{-}max}$ approximated by

$$V_{f-\max} \approx \Phi_{bn,p} + \Phi_{n,p}\sinh^2\left(E_{00}/kT\right) - \left(kT/q\right)\cosh^2\left(E_{00}/kT\right)$$

(eq. II-62)

gives a value below which the current is TFE-dominated. Theoretical $V_{f\text{-}max}$ has proven positive for the contacts on n-type Ge, and reached 0 on p-type (for any $\Phi_{bp}\leq0.67$eV, which is

the Ge bandgap). In this case, (eq. II-62) turns into a condition over a temperature T_M below which TFE conduction at zero bias becomes FE:

$$\sinh^2\left(E_{00}/kT_M\right)=\frac{\Phi_{bn,p}-kT_M/q}{kT_M/q-\Phi_{n,p}}$$

(eq. II-63)

II.2.6.b.iii. SBH extraction

Eventually, the contact resistivity expressions to be used for SBH extraction are that of TFE for n-type contacts (eq. II-55), and FE for p-type contacts (eq. II-56). As a result of the distinction between light holes and heavy holes currents, the contact resistivity associated to light holes ρ_c^{lh}, and to heavy holes ρ_c^{hh} were calculated separately. The total contact resistivity is that of ρ_c^{lh} and ρ_c^{hh} in parallel:

$$\rho_c=\frac{\rho_c^{lh}\cdot\rho_c^{hh}}{\rho_c^{lh}+\rho_c^{hh}}$$

(eq. II-64)

The extracted intrinsic Schottky Barrier Height values were then respectively Φ_{bp0}=0.28eV and Φ_{bn0}=0.39eV (Figure II-13)[2].

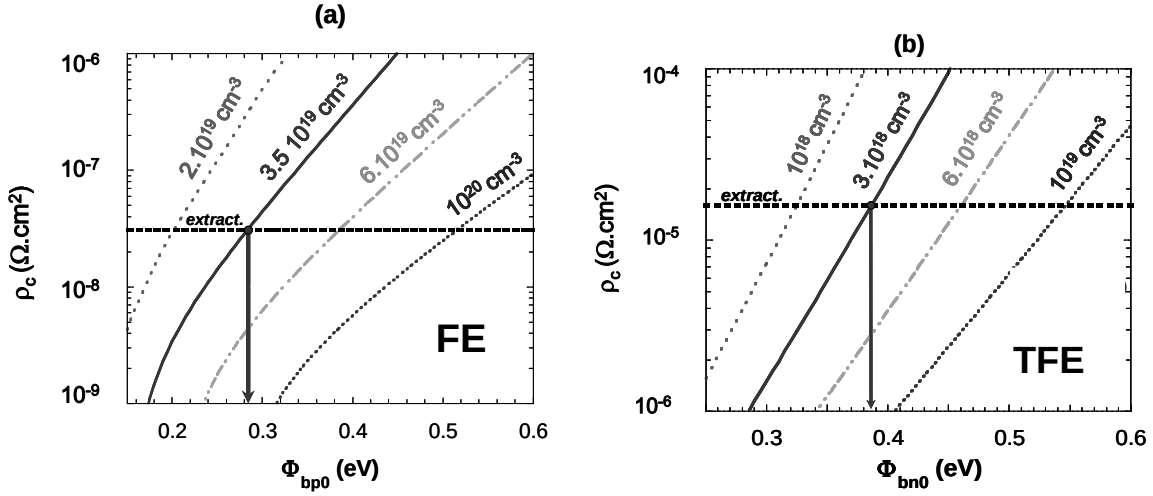

Figure II-13: (a) Analytical curves plotting $\rho_c(\Phi_{bp0})$ for FE mode in p-Ge for various N_a doping levels. Φ_{bp0} is determined by intercept between the extracted ρ_c and N_a values.
(b) Analytical curves plotting $\rho_c(\Phi_{bn0})$ for TFE mode in n-Ge for various N_d doping levels. Φ_{bn0} is determined by intercept between the extracted ρ_c and N_d values.

[2] See also Figure II-38 in section II.3.4.c. for the same sets of curves in the general case (TE, TFE, FE considered simultaneously).

The complementarity hypothesis (cf. II.1.1.c.ii) is indeed verified for the characterized contacts, as $\Phi_{bp0}+\Phi_{bn0} = 0.67eV \approx E_g^{Ge}$. Nevertheless, the effective SBH values Φ_{bp} and Φ_{bn} are lower, due to the image force induced barrier lowering (eq. II-11).
The impact of surface doping on the effective barrier is shown on Figure II-14, displaying Φ_{bp}=0.15eV and Φ_{bn}=0.32eV.

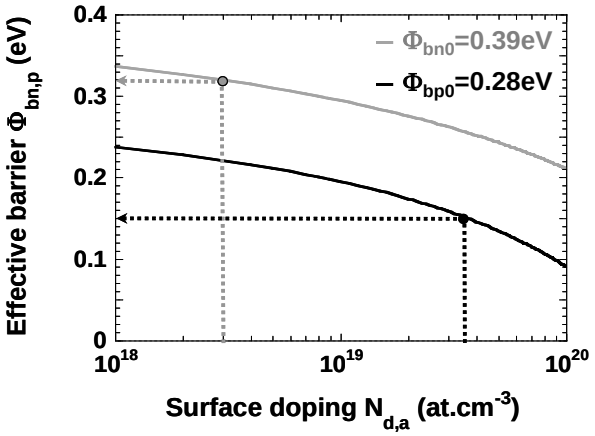

Figure II-14: Impact of surface doping on barrier lowering due to image force for the extracted SBH.

II.2.6.b.iv. Depinning action of an interfacial layer

Although only Ti was purposely deposited on the Ge surface, the extracted SBH do not match previously reported values for Ti/n-Ge contacts under TE dominant regime (weakly doped substrates, $\Phi_{bn}\approx\Phi_{bn0}\approx$0.57eV [*Han'98*],[*Dimoulas'06*], leading to $\Phi_{bp}\approx\Phi_{bp0}\approx$0.1eV). Han *et al.* [*Han'05*] report a formation of a TiGe layer at temperatures as low as 300°C. However, in spite of the thermal budget of our metallization process (450°C for several minutes), an Energy Dispersive X-Ray (EDX) analysis of the contact interface revealed that no TiGe layer was formed (Figure II-15 a)), suggesting that a passivation mechanism had occurred. We indeed observed a 2nm thick interfacial layer between Ge and Ti using Cross-sectional Transmission Electron Microscopy (Figure II-15 b)).

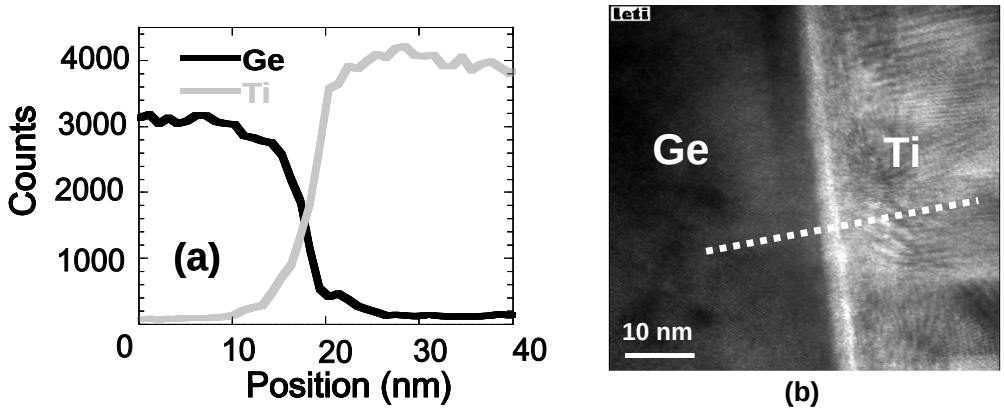

Figure II-15: (a) EDX analysis corresponding to the Ti/Ge interface, showing the absence of TiGe (point-to-point resolution: 1nm). (b) XSTEM image of the contact (picture: F. Aussenac). A 2nm thick interface is visible on the picture. The dotted line is the scanning line of the EDX analysis.

The composition of the interfacial layer was characterized using Electron Energy Loss Spectroscopy (EELS). The absence of an oxygen peak (Figure II-16) in the usual range of energy loss values indicates that the buffer oxide etch prior to metal deposition has been effective. The spectrum in the interface region suggests that the layer consists in non-stoichiometric titanium carbide (TiC_x). The presence of carbon could be a result of processing steps related to contact definition and etching.

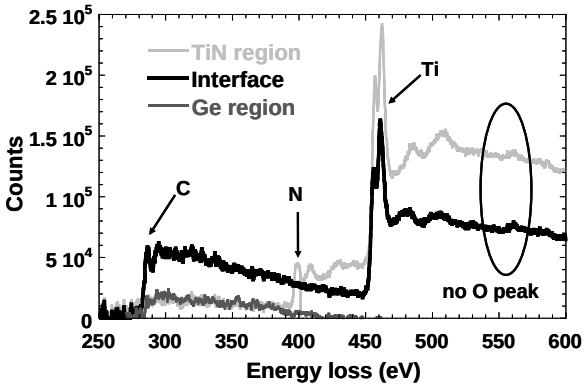

Figure II-16: EELS analyses in the vicinity of the Ti/Ge contact interface. The spectra associated with the TiN and Ge regions are represented for referential purposes.

In order to eliminate the influence of the contact etching steps, the same metallization process has been carried out on Ge blanket wafers (after dopant ionic implantation and annealing in the same conditions). This time, the EDX analysis of the interface (Figure II-17 a)) revealed the presence of a ~10nm thick TiGe intermediate layer, also visible on the STEM picture (Figure II-17 b)), in agreement with conclusions from [*Han'05*].

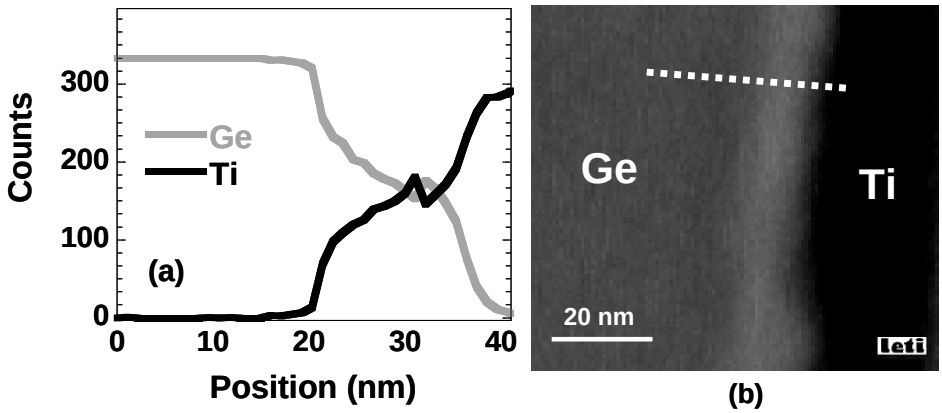

Figure II-17: (a) EDX analysis corresponding to the Ti/Ge interface on blanket wafers, showing the presence of TiGe (point-to-point resolution: 1nm). (b) XSTEM image of the interface (picture: F. Aussenac); the dotted line is the scanning line of the EDX analysis.

Thus, we conclude that the 2nm thick interfacial titanium carbide layer observed on our patterned samples after contact etching blocked the formation of TiGe. Furthermore, it is also the likely cause of the discrepancy with SBH values previously reported for Ti/Ge contacts, slightly reducing the dissymmetry between Φ_{bp0} and Φ_{bn0} through Fermi-level depinning. Finally, the surface doping further reduces both Schottky barriers through image force lowering (Figure II-18).

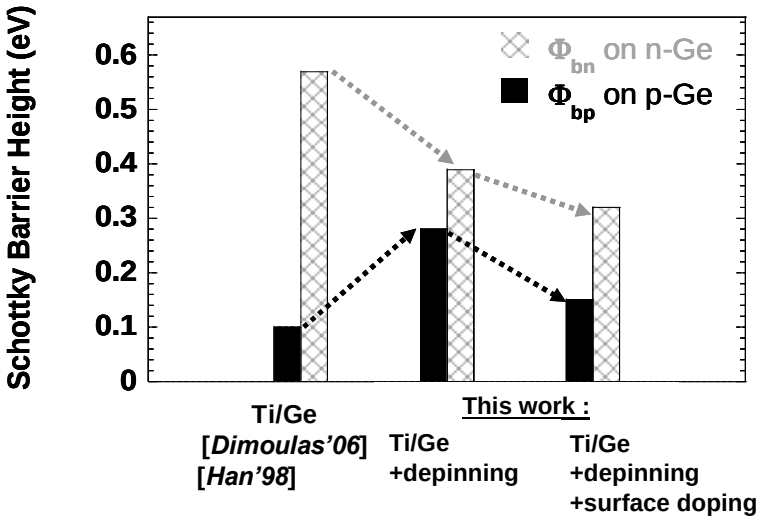

Figure II-18: Synthetic diagram showing the Schottky Barrier Heights for electrons on n-Ge and for holes on p-Ge for Ti-based contacts on Ge. Ti/Ge SBH for electrons are reported in [Dimoulas'06] and [Han'98], the barrier for holes were deduced by E_g^{Ge}-Φ_{bn}.

II.2.7. **Summary**

The accurate characterization of a Schottky Barrier Height is not a simple problem, especially when straying from the "easy" case of 100% thermionic emission over a large barrier in non-degenerate semiconductors (cf. C-V, photoemission techniques) and a current density following an Arrhenius law (cf. I-V, activation energy techniques).

For MOSFET applications with a highly efficient source injection in reverse bias, the most relevant configurations are those of small barriers and/or in degenerate semiconductors. The cases of study described in paragraph II.2.6. show that the intricate height and doping-dependent contributions of TE, TFE and FE regimes are not always easy to untangle, and their relative importance can sometimes be counterintuitive.

Moreover, even if all the parameters required for taking into account the tunneling component are very carefully determined; it is not guaranteed that using the approximate current density expression corresponding to one allegedly dominant current transport process (and disregarding the others) would always provide an accurate SBH evaluation.

II.3. Analytical One-Dimensional Modelling

So far, we reviewed simplified models which presented the advantage of not having to integrate the product of occupancy, vacancy and transmission probabilities in energy.

In this part, we will focus on the analytical 1-D modelling of a metal/p-Si diode. Without resorting to the simplified expressions, we will calculate the respective contributions of thermionic and tunneling current for various doping, temperature, SBH and bias conditions. This aims at providing a more refined understanding of the processes and dependences at stake in the emission of majority carriers at the Source of a Schottky MOSFET.

As seen in II.1.1.c. , the Fermi-level is mostly pinned (in Si and Ge) close to the valence band. The most "natural" application is therefore p-MOSFET, and the case studied in the following will be that of holes injection on p-type Si. The first step is to recreate the 1-D band diagram of a Metal/p-Si Schottky junction.

II.3.1. **One-Dimensional band diagrams**

II.3.1.a. Fermi-level

In the non-degenerate case, the Fermi-level (relative to the Valence Band) is obtained by:

$$E_{F,non-dgen}(N_A,T) = \frac{k\cdot T}{q}\cdot \ln\left(\frac{N_A}{N_V(T)}\right) + 2^{-3/2}\cdot\frac{N_A}{N_V(T)}$$

(eq. II-65)

with N_A the ionized acceptors concentration, and N_V the density of states in the Valence Band:

$$N_V(T) = 2\cdot\left(\frac{2\cdot\pi\cdot m_V\cdot k_B\cdot T}{h^2}\right)^{3/2}$$

(eq. II-66)

where m_V is the density of states effective mass in the valence band. In the degenerate case,

$$E_{F,dgen}(N_A,T) = E_{F,0}(N_A)\cdot\left[1-\frac{\pi^2}{12}\cdot\left(\frac{k\cdot T}{q\cdot E_{F,0}(N_A)}\right)^2\right]$$

(eq. II-67)

with $E_{F,0}$ the Fermi-level at 0K :

$$E_{F,0}(N_A) = \left(3\cdot\pi^2\cdot N_A\right)^{2/3}\cdot\frac{\hbar^2}{2\cdot q\cdot m_T^*}$$

(eq. II-68)

At low doping levels (eq. II-65) prevails. When E_F from this expression reaches 0, (eq. II-67) should be used, as shown below Figure II-19:

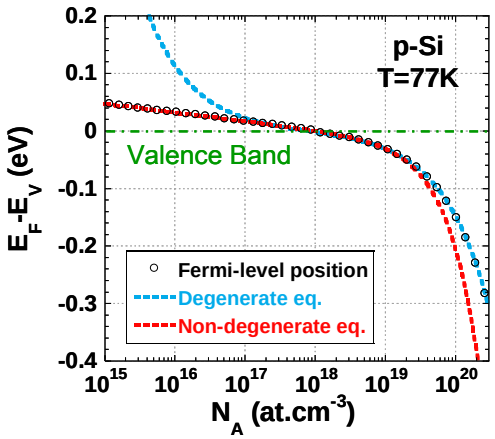

Figure II-19: E_F-E_V in p-type Si at T=77K, as a function of p-type doping level.

Figure II-20 below shows the evolution of E_F defined as above with temperature, for various N_A concentrations in Si.

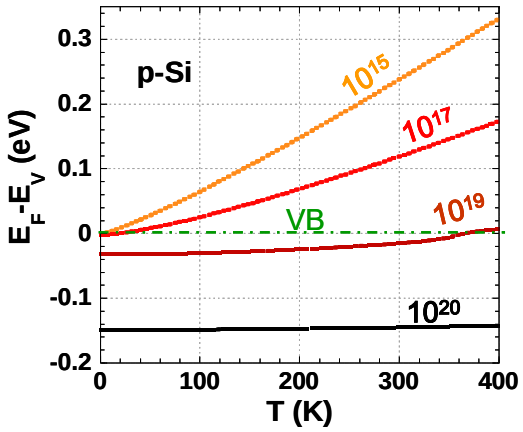

Figure II-20: E_F-E_V in p-Si versus temperature, for various N_A (at.cm^{-3}).

II.3.1.b. Accumulation and depletion

The temperature and doping-dependent difference E_F-E_V at equilibrium gives Φ_p in the neutral region of a Schottky junction, hence the built-in potential:

$$\psi_{bi}(\Phi_{bp0}, N_A, T) = \Phi_{bp0} - \Phi_p(N_A, T)$$

(eq. II-69)

Φ_{bp0} is the intrinsic Schottky barrier height *ie* the position of the valence band at the maximum of potential energy relative to the metal workfunction (which is aligned with the equilibrium Fermi-level), without taking into account the image potential (maximum located at the interface), as seen on Figure II-21.

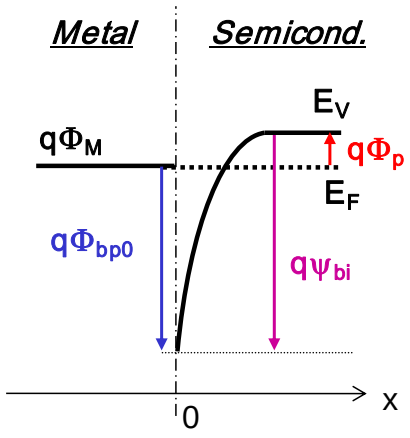

Figure II-21: Band diagram of a Schottky junction at zero bias with an intrinsic barrier height of Φ_{b0}, a degenerate semiconductor and resulting positive ψ_{bi}: presence of a depletion region.

In the following, V is defined as the bias applied on the semiconductor (equivalent to –V applied on the metal electrode).

- If $\Psi_{bi} > V$

The semiconductor is in depletion at the interface, and the depletion layer width is:

$$W_{dep}(\Phi_{bp0}, N_A, T, V) = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot \left[\psi_{bi}(\Phi_{bp0}, N_A, T) - V\right]}{q \cdot N_A}}$$

(eq. II-70)

- If $\Psi_{bi} < V$

The semiconductor is in accumulation at the interface, and the accumulation layer width is:

$$W_{acc}(\Phi_{bp0}, N_A, T, V) = \sqrt{2} \cdot L_D(N_A, T) \cdot \left[\exp\left(\frac{\left|\psi_{bi}(\Phi_{bp0}, N_A, T) - V\right|}{2 \cdot V_T(T)} \right) - 1 \right]$$

(eq. II-71)

with L_D the Debye length and V_T the thermal voltage:

$$L_D(N_A, T) = \sqrt{\frac{\varepsilon_{Si} \cdot k \cdot T}{q^2 \cdot N_A}}$$

(eq. II-72)

$$V_T(T) = \frac{k \cdot T}{q}$$

(eq. II-73)

Figure II-22 gives an idea of the order of magnitude of the Space Charge Region (SCR) width, and its nature according to doping level and applied bias.

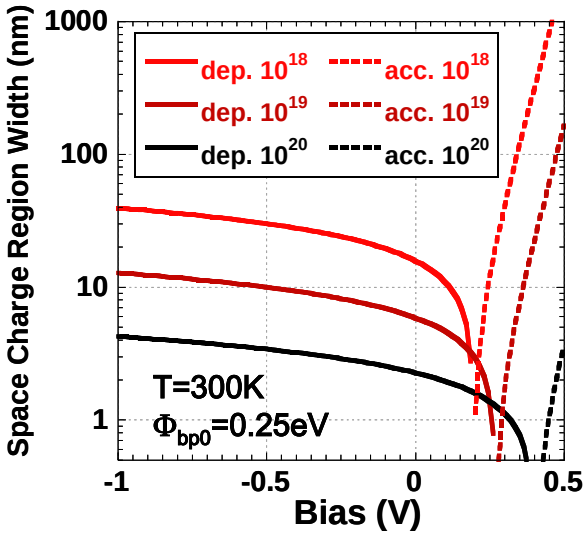

Figure II-22: Space Charge Region width and nature (depletion or accumulation) versus bias on the semiconductor for various doping levels N_A (at.cm^{-3}).

Of course, the thinner the depletion region, the easier it will be for charges to tunnel from the metal through the barrier.

Still without taking into account the image potential, the potential in the SCR can be expressed as below:

- In depletion:

$$\psi_{dep}(\Phi_{bp0}, N_A, T, V, x) = -\Phi_{bp0} + \frac{q \cdot N_A}{\varepsilon_{Si}} \cdot \left(W_{dep}(\Phi_{bp0}, N_A, T, V) \cdot x - \frac{x^2}{2} \right)$$

(eq. II-74)

- In accumulation:

$$\psi_{acc}(\Phi_{bp0}, N_A, T, V, x) = -\Phi_{bp0} - 2 \cdot V_T(T) \cdot \ln\left(1 + \frac{x}{L_D(N_A, T) \cdot \sqrt{2}} \right)$$

(eq. II-75)

To one of these the image potential should be added. In its classical formulation (see alternate modelling in II.3.5.) it is, for holes on the VB side:

$$\psi_{im}(x) = \frac{q}{16 \cdot \pi \cdot \varepsilon_{Si} \cdot x}$$

(eq. II-76)

The Conduction Band potential is deduced by changing the sign of ψ_{im} and adding the energy of the bandgap.

In Si, with T in Kelvin and E_g in eV:

$$E_g(T) = 1.169 - \frac{4.9 \cdot 10^{-4} \cdot T^2}{T + 655}$$

(eq. II-77)

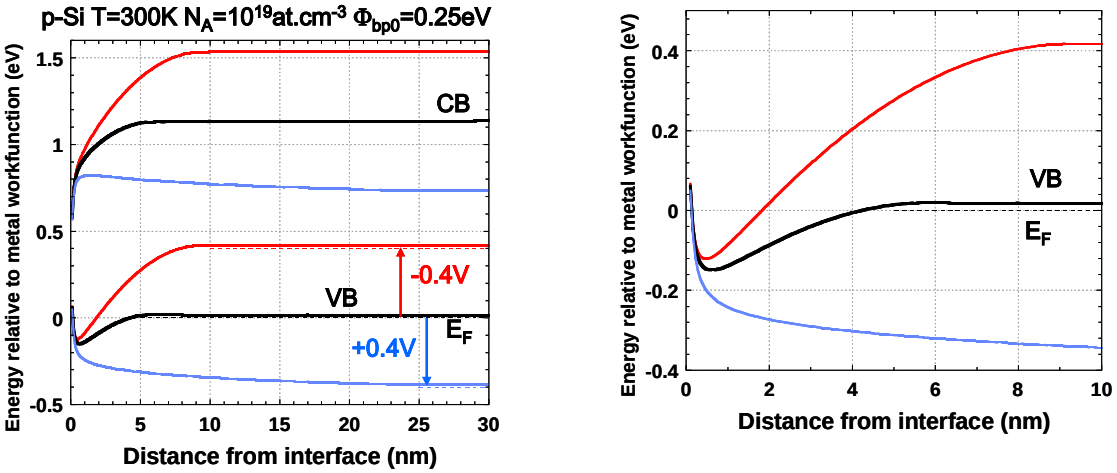

Figure II-23: 1-D band diagrams (p-Si, T=300K, $N_A=10^{19}at.cm^{-3}$, $\Phi_{bp0}=0.25eV$) at equilibrium, under forward (+0.4V) and reverse (-0.4V) bias. On the right, closer view of the barrier shape on the Valence Band side.

II.3.2. **Maximum of potential energy, turning points**

The value of the maximum of potential energy (which is actually here a minimum, as we consider the Valence Band) has to be known, as it defines the energy above which thermionic emission occurs. We can consider that in accumulation, the current flows almost exclusively from Si to metal, and is diffusion-limited. In depletion, the maximum of potential energy corresponds to the apparent barrier height, and its position is useful to determine the so-called turning points x_1 and x_2 for each energy (tunneling occurs between x_1 and x_2, cf. Figure II-24).

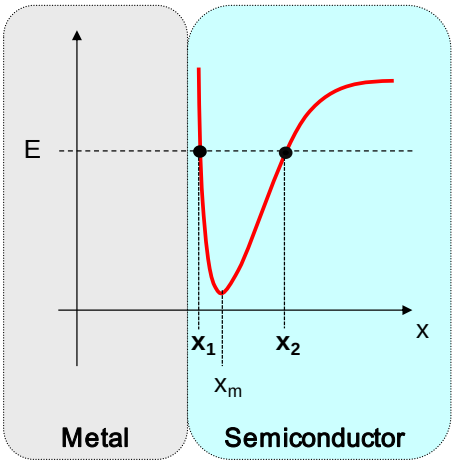

Figure II-24: Position of the turning points $x_1<x_m$ and $x_2>x_m$ associated to the energy E and for a given barrier shape.

Except in exceptional cases for which the depletion region width is so thin (<1nm) that it overlaps the zone of influence of the image potential, x_m is easy to determine, as:

$$\left(\frac{d(\psi_{dep}(\Phi_{bp0},N_A,T,V,x)+\psi_{im}(x))}{dx}\right)_{x=x_m}=0$$

(eq. II-78)

The turning points are defined as follows:

$$x_1(\Phi_{bp0},N_A,T,V,E)=x\in\left]0;x_m\right]/\psi_{dep}+\psi_{im}=\frac{E}{q}$$

(eq. II-79)

$$x_2(\Phi_{bp0},N_A,T,V,E)=x\in\left[x_m;W_{dep}\right]/\psi_{dep}+\psi_{im}=\frac{E}{q}$$

(eq. II-80)

It is interesting to see how the distance between the turning points as a function of energy evolve with varying doping, barrier, bias and temperature. It provides an insight on the potential contribution of tunneling current.

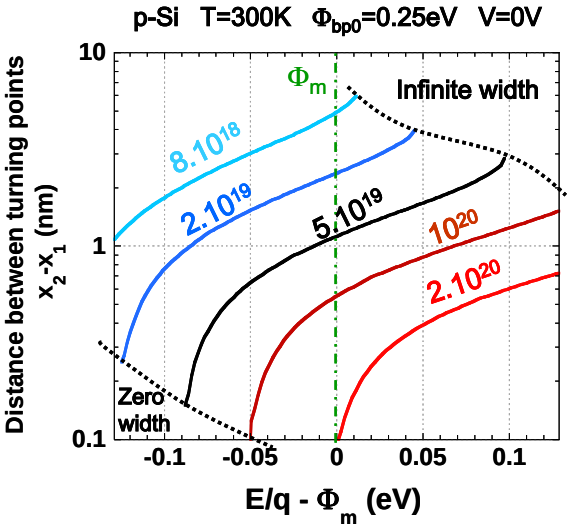

Figure II-25: Distance between the turning points as a function of the energy relative to the metal Fermi-level, for various acceptor concentrations N_A ($at.cm^{-3}$) in p-type Si.

By increasing the doping level, tunneling becomes easier due to a reduced distance between turning points (thinner barrier). On the top right extremity of each curve: holes of superior energy cannot tunnel (x_2 is no longer defined at these energies). On the bottom left extremity: carriers below this energy are beyond the valence band potential energy maximum (zero turning point), they are thermionically emitted.

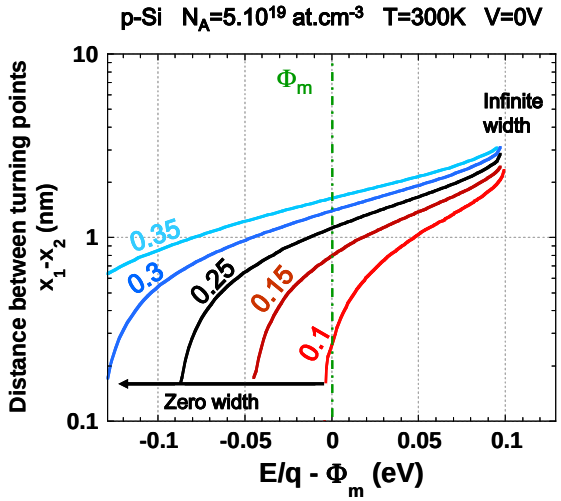

Figure II-26: Distance between the turning points as a function of the energy relative to the metal Fermi-level, for various intrinsic barrier heights for holes Φ_{bp0} (eV).

Increasing the SBH reduces the tunneling current by increasing the barrier width at a given energy. On the other hand, it is relevant to note that the total conduction owing to tunneling becomes predominant as the occurrence of thermionic emission (bottom left) is "delayed".

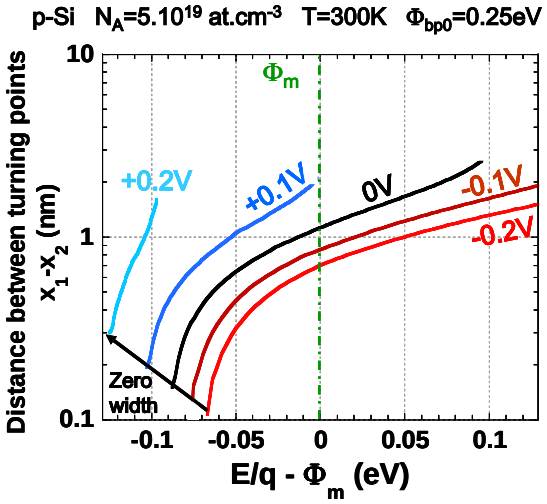

Figure II-27: Distance between the turning points as a function of the energy relative to the metal Fermi-level, for various applied (forward, blue and reverse, red) biases.

Positive biases (semiconductor side) flatten and broaden the barrier shape; negative biases elongate and sharpen it, increasing the tunneling current.

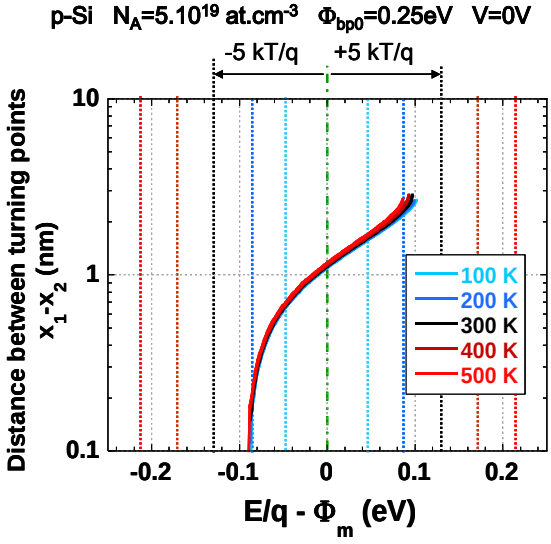

Figure II-28: Distance between the turning points as a function of the energy relative to the metal Fermi-level, for various temperatures.

With temperature, the barrier shape does not change much. But if we consider that conduction mostly originate from carriers of energies within ±5kT/q around the Fermi level, the proportion of tunneling current is more important at low temperatures.

II.3.3. **Interfacial majority carriers current density**

If the metal electrode is the potential reference, the Fermi-Dirac carriers distributions f_S and f_M (resp. in the semiconductor and in the metal) are:

$$f_S(T,V,E) = \frac{1}{1+\exp\left(\frac{E+q\cdot V}{k\cdot T}\right)}$$

(eq. II-81)

$$f_M(T,E) = \frac{1}{1+\exp\left(\frac{E}{k\cdot T}\right)}$$

(eq. II-82)

As we consider holes, the probability of occupancy becomes that of vacancy and vice-versa. This does not change anything in the absolute value of the current densities, when the fluxes are superimposed in the integral.

The energy of the Valence Band being $q(\psi_{dep}+\psi_{im})$, the transmission probability in energy in the Wentzel-Kramers-Brillouin (WKB) approximation is given by:

$$TR\left(\Phi_{bp0}, N_A, T, V, E\right) = \frac{\exp\left(-2\int_{x1}^{x2}\sqrt{\frac{2\cdot\left|q\cdot\left(\psi_{dep}+\psi_{im}\right)-E\right|\cdot m_T^*}{\hbar^2}}\cdot dx\right)}{1+\frac{1}{4}\cdot\exp\left(-2\int_{x1}^{x2}\sqrt{\frac{2\cdot\left|q\cdot\left(\psi_{dep}+\psi_{im}\right)-E\right|\cdot m_T^*}{\hbar^2}}\cdot dx\right)}$$

(eq. II-83)

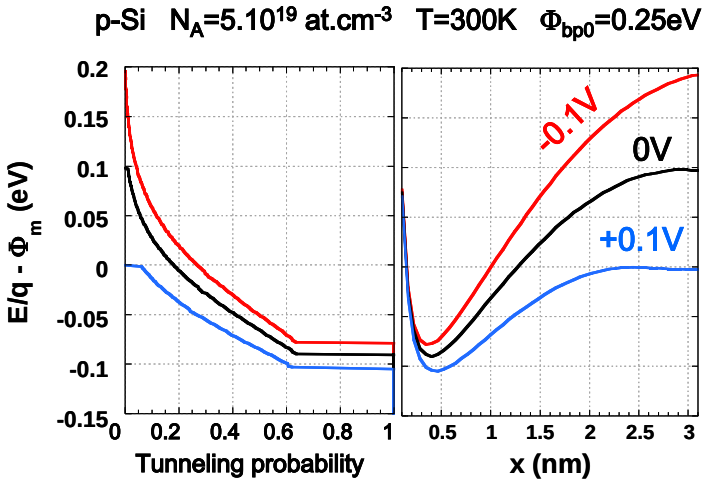

Figure II-29: WKB quantum tunneling probability and corresponding barrier shape at equilibrium, under reverse (red) and forward (blue) bias.

II.3.3.a. Thermionic Current

Thermionic and Field-effect currents are computed with the same integral, using only different bounds. For thermionic current, the considered energies are comprised between the potential energy optimum and infinity.

$$J_{TE}\left(\Phi_{bp0}, N_A, T, V\right) = \frac{A_p^* \cdot T}{k} \cdot \int_{-\infty}^{q\cdot\left(\psi_{dep}(x_m)+\psi_{im}(x_m)\right)} TR(\Phi_{bp0}, N_A, T, V, E) \cdot \left(f_M(T,E) - f_S(T,V,E)\right) \cdot dE$$

(eq. II-84)

TR equals 1, and in practice, one can replace -∞ by the energy at x_m minus 20 kT (or any energy at which f_S can be considered equal to zero).

II.3.3.b. Field Emission Current in depletion

II.3.3.b.i. FE current

FE current corresponds to carriers of energy comprised between the upper edge of the Valence Band in the neutral region, and (cf. Figure II-30):

- In reverse bias (V<0, current from metal to SC): the metal Fermi-level

$$J_{FE}\left(\Phi_{bp0}, N_A, T, V<0\right) = \frac{A_p^* \cdot T}{k} \cdot \int_{0}^{q\cdot\left(\psi_{dep}(W_{dep})+\psi_{im}(W_{dep})\right)} TR(\Phi_{bp0}, N_A, T, V, E) \cdot \left(f_M(T,E) - f_S(T,V,E)\right) \cdot dE$$

(eq. II-85)

- In forward bias (V>0, current from SC to metal): the semiconductor Fermi-level (energy –qV if $q.\Phi_m$ is the potential reference) <u>only if the semiconductor is degenerate</u> (else, no FE current)

$$J_{FE}\left(\Phi_{bp0}, N_A, T, V>0\right) = \frac{A_p^* \cdot T}{k} \cdot \int_{E_F}^{q\cdot\left(\psi_{dep}(W_{dep})+\psi_{im}(W_{dep})\right)} TR(\Phi_{bp0}, N_A, T, V, E) \cdot \left(f_M(T,E) - f_S(T,V,E)\right) \cdot dE$$

(eq. II-86)

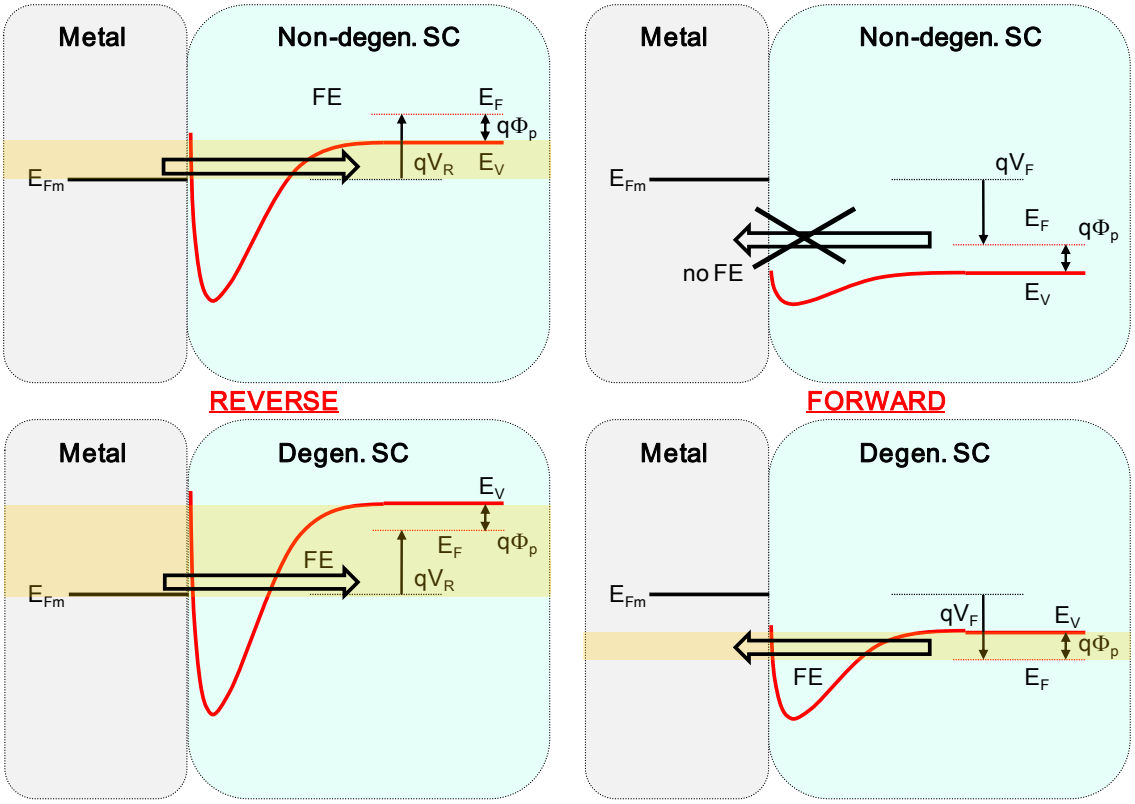

Figure II-30: Illustration of the bounds to consider in the cases of reverse and forward biases applied to non-degenerate and degenerate semiconductors for FE current density calculation.

II.3.3.b.ii. TFE current

TFE current takes place at energies located between the optimum of potential energy and (cf. Figure II-31):

- In reverse bias: the metal Fermi-level or the top edge of the valence band in the neutral region (can be inferior to $q\Phi_m$ if the semiconductor is non-degenerate and $V_R<\Phi_p$)

$$J_{TFE}\left(\Phi_{bp0}, N_A, T, V<0\right)=\frac{A_p^*\cdot T}{k}\cdot\int_{q\cdot\left(\psi_{dep}(x_m)+\psi_{im}(x_m)\right)}^{\min\left(0;q\cdot\left[\psi_{dep}(W_{dep})+\psi_{im}(W_{dep})\right]\right)} TR(\Phi_{bp0}, N_A, T, V, E)\cdot\left(f_M(T,E)-f_S(T,V,E)\right)\cdot dE$$

(eq. II-87)

- In forward bias: the top edge of the valence band in the neutral region (if the semiconductor is non-degenerate) or the Fermi-level of the semiconductor (if it is degenerate)

$$J_{TFE}\left(\Phi_{bp0}, N_A, T, V>0\right)=\frac{A_p^*\cdot T}{k}\cdot\int_{q\cdot\left(\psi_{dep}(x_m)+\psi_{im}(x_m)\right)}^{\min\left(-qV;q\cdot\left[\psi_{dep}(W_{dep})+\psi_{im}(W_{dep})\right]\right)} TR(\Phi_{bp0}, N_A, T, V, E)\cdot\left(f_M(T,E)-f_S(T,V,E)\right)\cdot dE$$

(eq. II-88)

The total tunneling current is finally given in each case by $J_{FE}+J_{TFE}$.

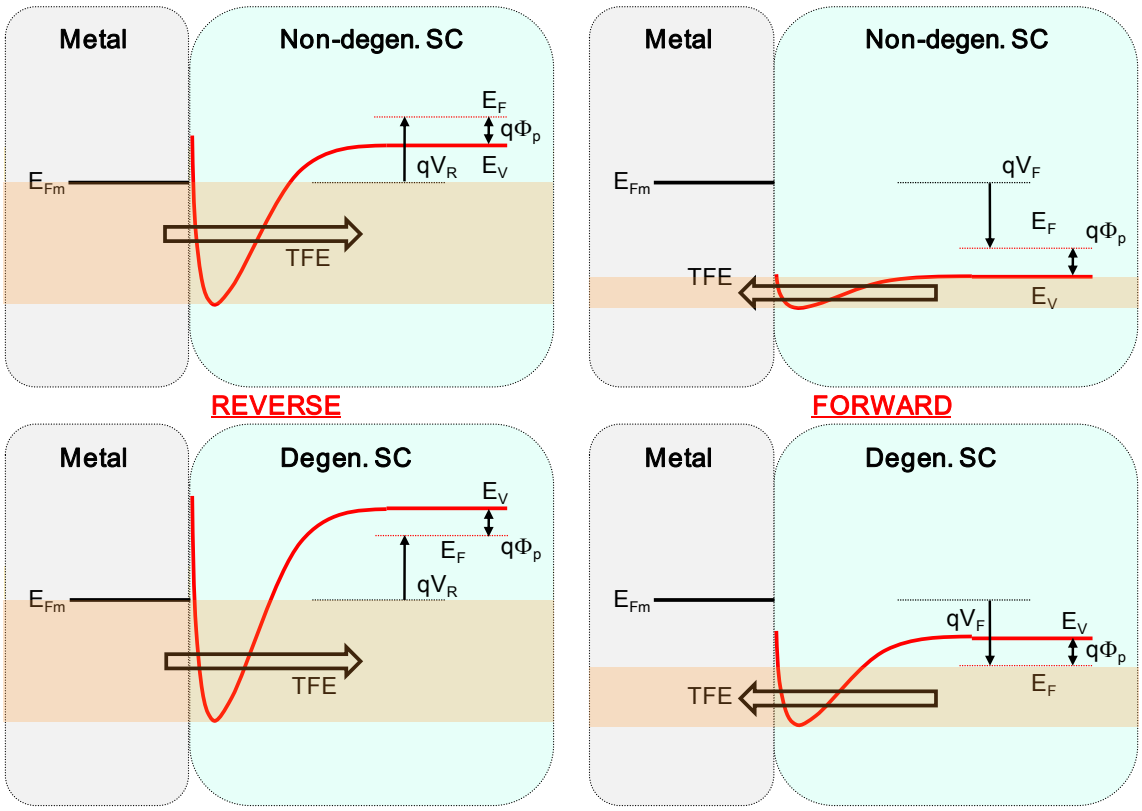

Figure II-31: Illustration of the bounds to consider in the cases of reverse and forward biases applied to non-degenerate and degenerate semiconductors for TFE current density calculation.

II.3.4. **Dependences**

II.3.4.a. Majority carriers current density

Observing the majority carriers current density obtained as a function of the bias applied on the semiconductor provides a good qualitative understanding of the factors bringing the characteristics closer to an ohmic behavior. The reference case in the following graphs (black cuve) is that of a contact on p-Si with a doping level of 5.10^{19} at.cm^{-3} and an intrinsic SBH of Φ_{bp0}=0.25eV, at 300K. Due to the modelling, a slight discontinuity is generally observed near the flat-band voltage, where the injection becomes limited by the diffusion speed of carriers in the accumulation region. The proportion of tunneling current density $J_{tun}/(J_{TE}+J_{tun})$ is also observed. Below is the dependence on doping.

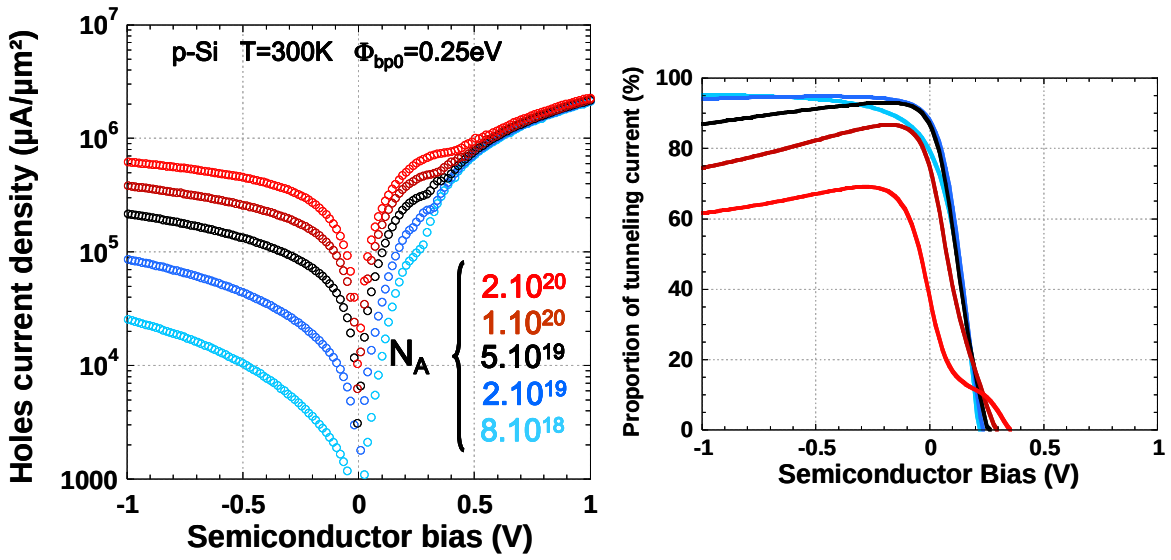

Figure II-32: Holes current density versus applied bias on the semiconductor for various acceptor concentrations, and corresponding fraction of tunneling current.

We can see on Figure II-32 that:

- **The doping level in the semiconductor primarily increases both the current density in reverse bias, and the forward current density at low field** (for V values lower than V_{fb}). There is almost a decade of current density at V=-1V between the case of a 2.10^{19} at.cm^{-3} acceptor concentration and that of a 2.10^{20} at.cm^{-3} concentration.
- For an intrinsic **barrier for holes of 0.25eV** (which would correspond to a PtSi/Si contact, and is among the lowest reported on Si considering Fermi-level pinning), and a **considerably high doping level** (2.10^{20} at.cm^{-3}), the **J-V characteristic curve is still dissymmetric**.
- The assumption that **the tunneling current is more important in highly-doped semiconductors is not necessarily true**, especially in reverse bias. The tunneling current density itself is probably higher than in moderately doped Semiconductors (thinner SCR), but the thermionic current also increases due to an increased barrier lowering influence of the image force. Indeed, in (eq. II-74) and (eq. II-76): for a given x, ψ_{dep} loses significance when W_{dep} decreases, whereas ψ_{im} remains the same.
- We can see the proof that the **simplified criterion for evaluating the dominant current transport process at zero bias** (cf. II.1.2.d.ii) **does not work when the semiconductor is degenerate**. According to (eq. II-33), E_{00} is as large as the dopant concentration is high, and increasing the doping should always lead towards a predominance of FE current. Yet, we see here a **40% proportion of tunneling current at zero bias for an acceptor concentration of 2.10^{20} at.cm^{-3}** (high E_{00} energy), **leaving 60% to TE current** which is the actual dominant transport process.

Acknowledging this, a question remains on this approach considering one process at a time: **how accurate can the SBH extraction be, when disregarding 40% of the current density?**

After these considerations on the uncertainties related to SBH extraction on degenerate semiconductors, we can observe what a SBH variation of a few tens of meV changes on the characteristics.

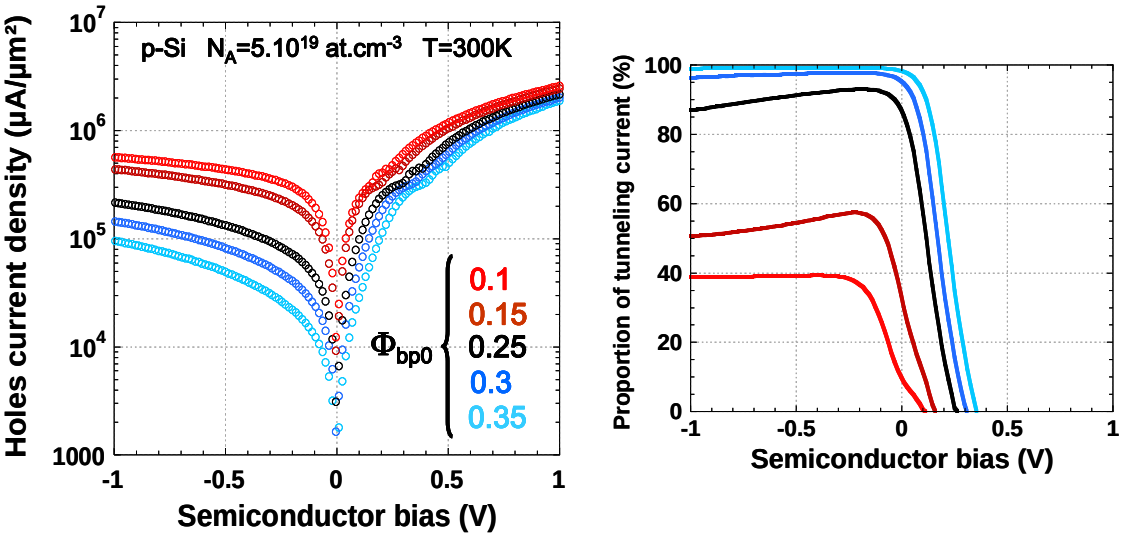

Figure II-33: Holes current density versus applied bias on the semiconductor for various intrinsic SBH for holes, and corresponding fraction of tunneling current.

- A lower barrier increases both the reverse and forward current densities.
- At low forward bias, the ideality factor is closer to 1 when the barrier height decreases (for a given doping level), as TE current increases (from ~5% to ~90% at zero bias between respectively Φ_{bp0}=0.35eV and Φ_{bp0}=0.1eV).
- The current density for a 1V reverse bias is roughly doubled in this case for a 10meV SBH decrease.

Finally, we can observe the temperature dependence of the characteristics:

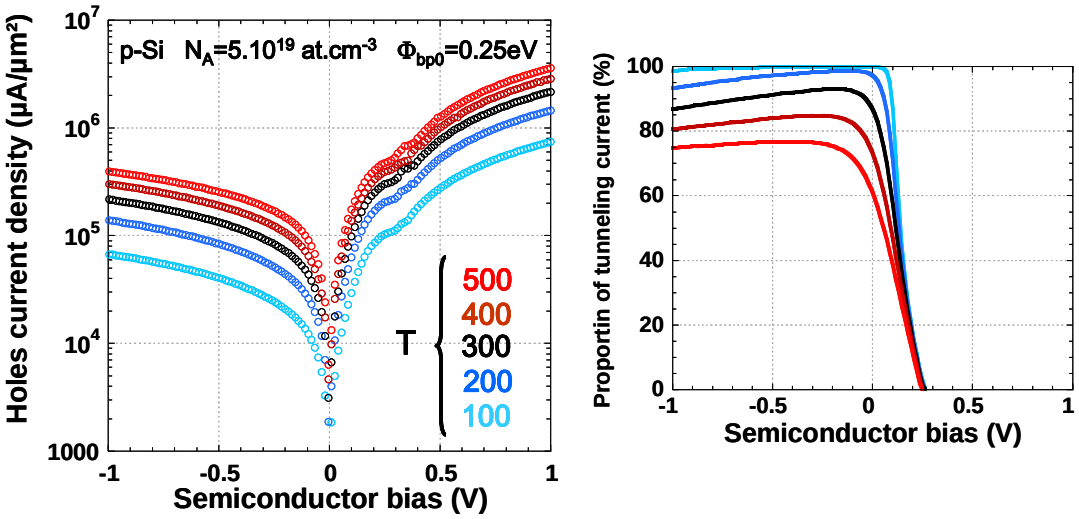

Figure II-34: Holes current density versus applied bias on the semiconductor for various temperatures, and corresponding fraction of tunneling current.

Higher temperatures increase the overall current and decrease the ideality factor by increasing the fraction of thermionic current, as expected according to Figure II-28.

II.3.4.b. Ohmic behavior and contact resistivity

An ohmic contact, *ie* a completely linear J-V characteristic would be the ideal case, maximizing the current density in reverse bias (and thus the injection at the Source in a MOSFET). However, this cannot happen unless the charges coming from the metal do not meet any barrier (0% tunneling current), in which case their probability of transmission would be lowered to less than unity. **At 300K, this actually requires a negative effective Schottky Barrier Height**, in order to compensate for the temperature-dependent spreading of the carriers distribution around the metal Fermi-level.

In practice, the contact resistivity evolves with the applied bias, as does the proportion of tunneling current. If its dynamic value at zero bias (eq. II-53) is an important "standardized" figure of merit, a more relevant definition for MOSFETs applications would be its (static) value $(J/V)^{-1}$ at $V=V_{op}$, with V_{op} the potential drop across the Metal/Semiconductor contact of interest when the supply voltage $V_{dd}=V_{GS}=V_{DS}$ is applied. Since at the ON-State the Source-side junction is under reverse bias and the Drain-side junction is under forward bias, any non-linear and non-symmetrical current-voltage characteristics will lead to different values for $V_{op,S}$ and $V_{op,D}$. Solving the voltage sharing between two contact diodes and the channel resistance that they are flanking is a famously self-consistent problem; which means the effective contact resistivity depends on the transistor performance at a given supply voltage. As a rule of thumb, evaluating the dynamic value at V=0V is as accurate as the contact features a low resistivity.

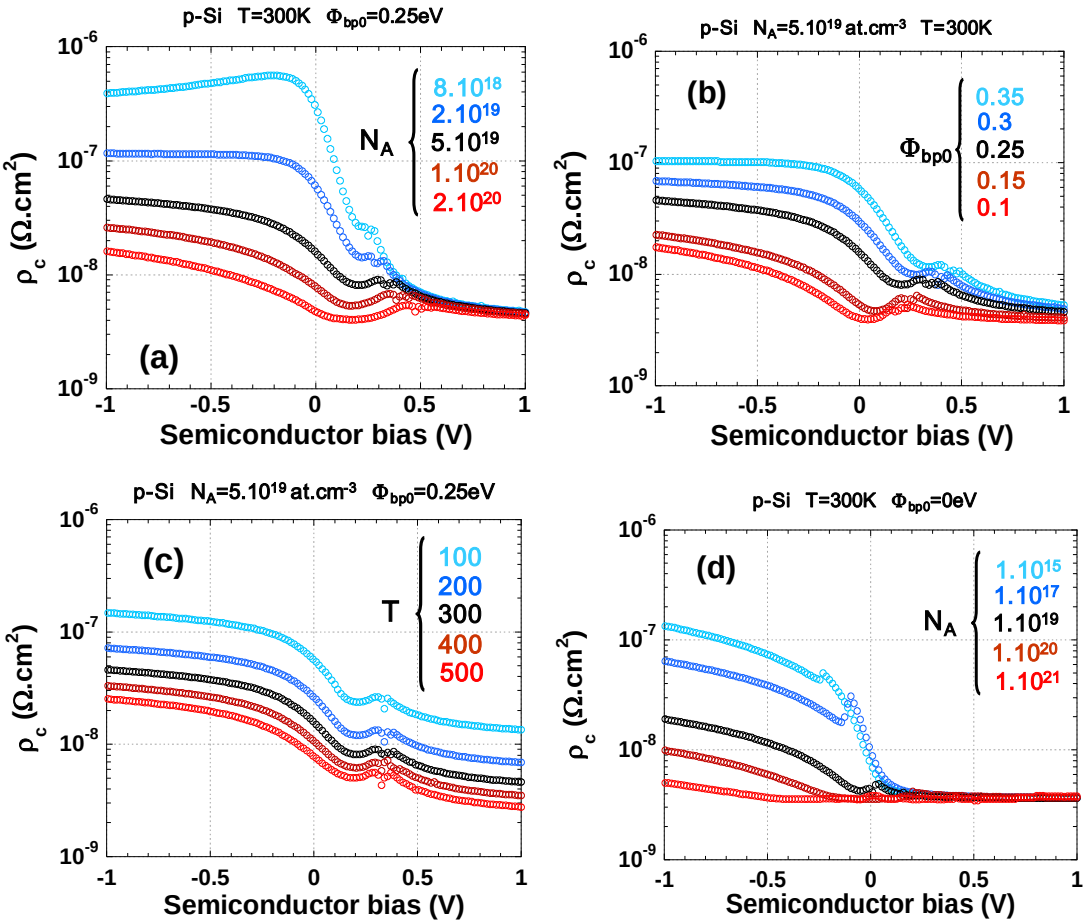

Figure II-35: Contact resistivity defined as V/J as a function of the bias applied on Si for various (a) acceptor concentrations in Si (b) intrinsic SBH (c) temperatures. The case (d) shows the influence of doping for a contact with intrinsic SBH equal to 0eV (effective SBH can become <0 at high N_A).

In the perspective of "conventional" MOSFETs with doped Source and Drain and silicided access, these ρ_c values can be related to the latest ITRS specifications for integration on Fully Depleted SOI (Table II-2).

Year of production	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*
Contact maximum resistivity for FDSOI MPU/ASIC ($\Omega.cm^2$)	**4.10^{-8}**	**2.10^{-8}**	**10^{-8}**	**8.10^{-9}**	**7.10^{-9}**	**6.10^{-9}**	**5.10^{-9}**

	Manufacturable solution exist, and are being optimized
	Manufacturable solutions are known
	Manufacturable solutions are NOT known

Table II-2: ITRS 2009 specifications for maximum contact resistivity for FDSOI MPU/ASIC.

II.3.4.c. Case of metal/Ge contacts

Let us see now what happens when considering the parameters for Schottky contacts on Ge (contact interface on the (100) plane), as seen previously in Table II-1, paragraph II.2.6.b.i.

We already have some qualitative elements of answer regarding the electrical contact properties:

1. In Ge, the **effective masses for holes are lighter**, which results in:
   - **larger transmission probabilities** for a given barrier width, *ie* facilitated tunneling (cf. (eq. II-83)
   - but a **lower Richardson constant A^*** ((eq. II-14 and (eq. II-59), implying a typically smaller thermionic current.

2. The **dielectric constant is larger** than in Si, resulting in:
   - **smaller image force-induced barrier lowering** than in Si (cf. (eq. II-11). Therefore for a given intrinsic barrier height, there will be less TE current than for Si.
   - **larger depletion regions** (cf. (eq. II-70). The barriers will tend to be wider as in Si for the same doping, temperature, SBH conditions.

3. The **Fermi-level pinning is stronger and Φ_0 closer to the VB edge** than in Si:
   - **Typically, lower intrinsic barriers for holes** are observed in Ge (*eg.* PtGe/Ge contact: Φ_{bp0}=0.06eV, vs. PtSi/Si: Φ_{bp0}=0.25eV)

4. The **hole mobility is larger in Ge**:
   - If we refer to paragraph II.1.2.c.iii, and in particular to (eq. II-28), this implies that f_p and v_D are larger in Ge. The larger transmission probabilities (cf. above) imply that f_q is also larger in Ge. Regarding v_R the thermionic recombination velocity, it should be roughly the same as in Si, as a smaller A^* is divided by a smaller N_V (by a factor ~1/2 in both cases). As a result, **A^{**} should generally be closer to A^* in Ge than it is in Si**, which could counterbalance the fact that $A^*_{Si}>A^*_{Ge}$. This trend, however, is not taken into account in the present model, as we chose to use A^* for the sake of simplicity. However, one has to keep it in mind before taking the following ρ_c values for granted, as J varies linearly with the Richardson constant, and A^{**} can lie somewhere between A^* and $A^*/2$ in Si [*Andrews'70*].

The counterpart of Figure II-35 for contacts on p-Ge is shown below in Figure II-36.

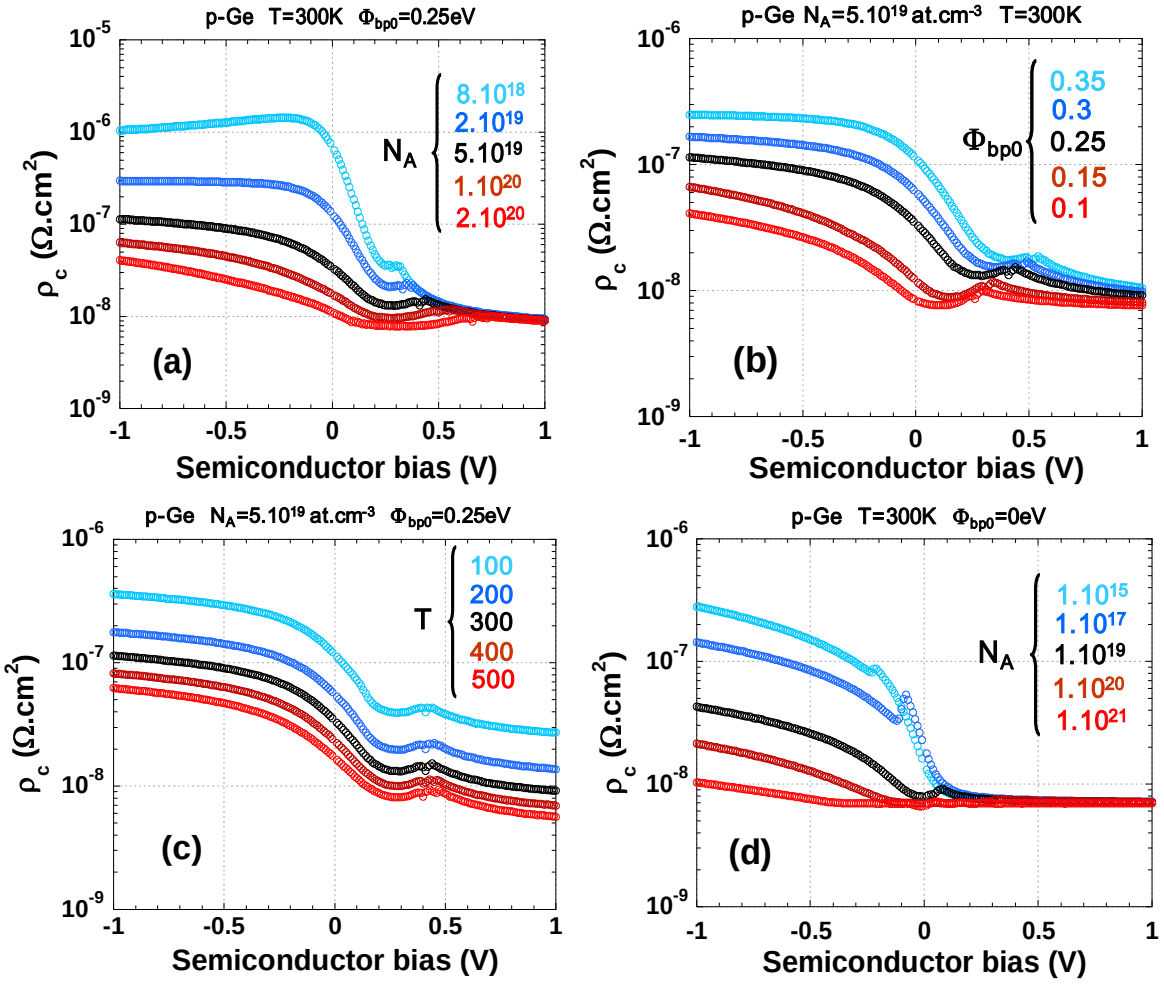

Figure II-36: Contact resistivity defined as V/J as a function of the bias applied on Ge for various (a) acceptor concentrations in Ge (b) intrinsic SBH (c) temperatures. The case (d) shows the influence of doping for a contact with intrinsic SBH equal to 0eV (effective SBH can become <0 at high N_A).

We can see that the trends and orders of magnitude are essentially the same. Quantitatively, the specific contact resistivities are higher in Ge for the same set of parameters, which mostly owes to a lower Richardson constant (cf. remark on A^{**} above) and a lesser portion of TE current due to a weaker impact of the image force.

Nevertheless, for a given metal, the intrinsic SBH on Ge are lower than on Si, which counterbalances this slight disadvantage (Figure II-37).

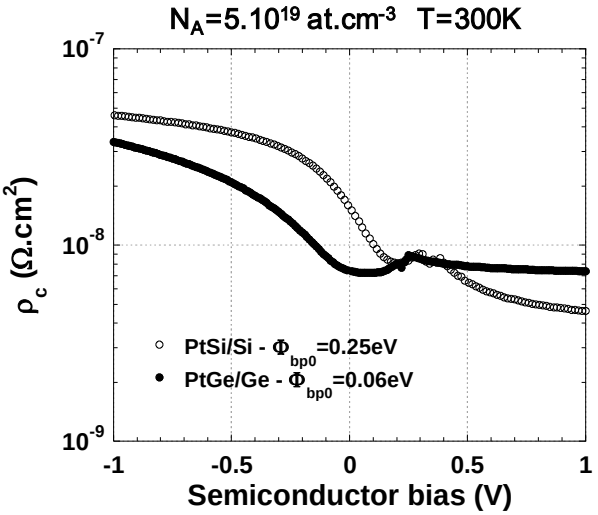

Figure II-37: Contact resistivity defined as V/J as a function of the bias applied on the semiconductor at 300K and for a doping level $N_A=5.10^{19}at.cm^{-3}$. The open circles correspond to a contact on p-Si with intrinsic SBH equal to 0.25eV (eg. PtSi/Si). Closed circles correspond to a contact on Ge with intrinsic SBH equal to 0.06eV (eg. PtGe/Ge).

It is also important to note that the quantitative results in this section do not match exactly those showed in II.2.6.b. In particular, Figure II-13 suggests that a contact resistivity of 10^{-9} Ω.cm^2 can be easily achieved, *eg* with an intrinsic SBH of 0.24eV and $N_A=6.10^{19}$ at.cm^{-3}, whereas the 1-D analytical modelling shows a saturation minimum at 7.10^{-9} Ω.cm^2 in the far forward regime even for a zero-barrier contact (pure TE regime).

And yet, this saturation value of 7.10^{-9} Ω.cm^2 is completely in agreement with (eq. II-54), which gives ρ_c in TE regime. This stresses the limits of using the simplified expressions from [*Padovani'66*], which can yield values of contact resistivity in FE regime lower than those corresponding to straightforward thermionic emission over a 0eV barrier. It is indeed physically inconsistent to predict an increased current density while introducing a tunneling barrier with a transmission probability lower than unity.

Most probably, this error results from the discriminating criteria for identifying the dominant transport regime. As we can see on Figure II-32, FE does not become systematically dominant at zero bias with increasing doping (not if the barrier is low), as opposed to what the criteria based on E_{00} (eq. II-33) suggest.

The set of curves showing the contact resistivity as a function of intrinsic SBH for various doping levels is re-plotted in Figure II-38 considering all the current transport mechanisms (TE, TFE, FE) at once.

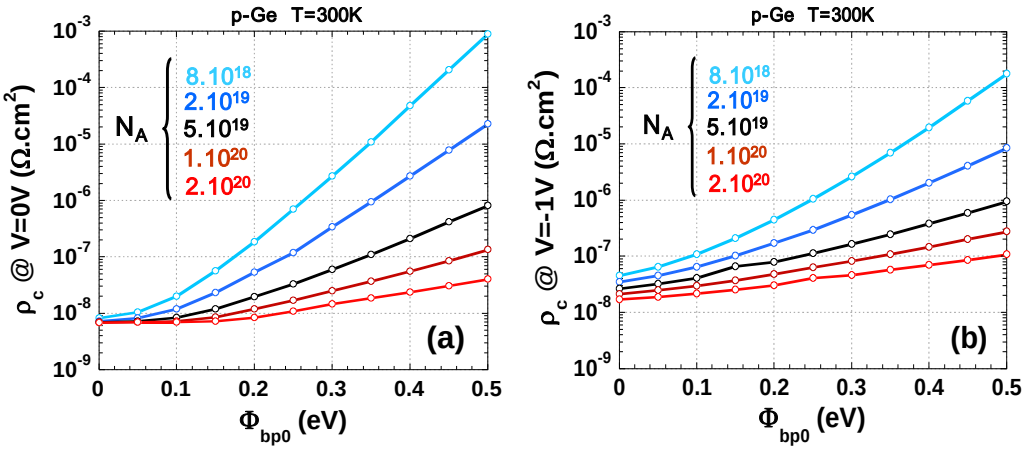

Figure II-38: Specific contact resistivity vs. intrinsic SBH for holes and for various doping levels calculated (a) at V=0V (for direct comparison with Figure II-13) and (b) at V=-1V.

II.3.4.d. Summary

We have seen in this part that the dependence of the electrical properties of a metal/semiconductor interface on doping, SBH, temperature and bias are very intricate.
Qualitatively, the contact resistivity is very dependent when the SBH is high, much less for low SBH where TE dominates. Evaluating the dominant current transport process at zero bias by solely examining the characteristic energy E_{00} is insufficient for high doping levels. Furthermore, the simplification consisting in considering only one dominant transport regime, disregarding the other two can be fairly rough. The ohmicity of the contact is limited by the tunneling probability in reverse bias conditions.

Quantitatively, the value of the minimum contact resistance achievable is strongly linked to the Richardson constant, which is not so easy to accurately evaluate (cf. A^{**} in (eq. II-28). The comparison of the electrical properties for contacts on p-Ge and p-Si is not strongly conclusive, but the typical orders of magnitude for $\rho_c(\Phi_{bp0},N_A,T,V)$ are the same.

II.3.5. **Self-consistent, non-divergent modelling of the image force**

II.3.5.a. Issues related to the classical formulation

So far, we modeled the image force lowering by deriving Coulomb's law, which results in a "1/x" diverging potential energy. This modelling is suitable for a macroscopic approach, but might seem improper given the characteristic distances at stake. More pragmatically, this divergence is a major inconvenience for TCAD simulation. The solutions implemented *e.g.* in Synopsis and Silvaco TCAD softwares so as to account for barrier lowering while still defining a boundary condition for the potential at the interface can seem a bit rough. Basically, the optimum of potential energy is shifted to the interface with the metal, resulting in a triangular potential barrier with the correct height, but an altered width (Figure II-39).

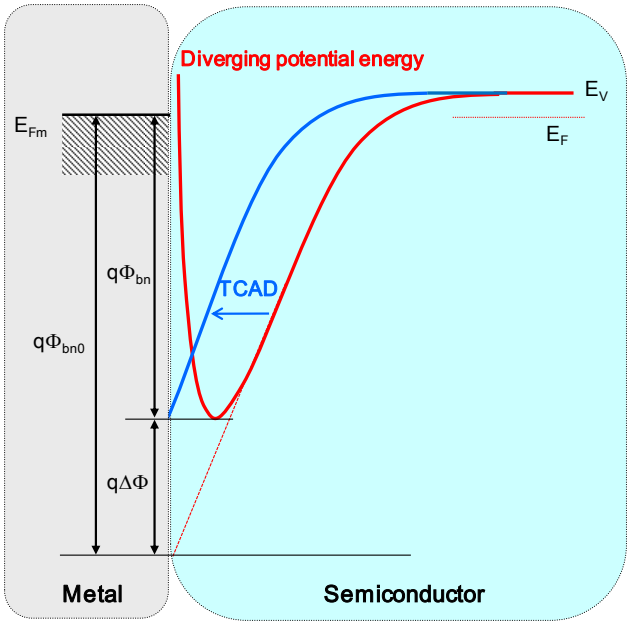

Figure II-39: Modelling of the image force-induced barrier lowering using the classical formulation, and subsequent potential barrier profile as implemented in some major TCAD simulators.

One can easily visualize that this approximation introduces additional uncertainties in terms of both transport (the transmission coefficient is computed for a barrier a few Å thinner) and electrostatics (position of W_{dep} shifted by x_m). A way of getting rid of the divergence problem can be found in a quantum-mechanical approach to image potential modelling.

II.3.5.b. Self-consistent expression of the image force potential

The work of Hartstein and Weinberg [*Hartstein'78*] raises the following questions: "*What would be an appropriate generalization of the image force in quantum mechanics? What is the proper formulation of the image force problem when the tunneling electron cannot be considered to be a point particle in the barrier region?*". Indeed, the classical image potential as formulated in (eq. II-8) implicitly assumes that the electron can be treated as a point charge, even in a tunneling situation for which it would be localized in the barrier.
Quantum mechanically, an external charge is given by image the probability of finding an electron at **r'** multiplied by the electron charge $q|\psi(\mathbf{r'},t)|^2$. The metallic surface charge distributes itself in response to this charge distribution, and can be expressed as an image charge distribution $-q|\psi(-\mathbf{r'},t)|^2$. The image force potential at position **r** is the response of a test charge q at position **r** to the image charge distribution, and can be expressed as:

$$\Psi_{im} = -\int_{-\infty}^{0} \frac{q^2 \left|\psi(-r',t)\right|^2}{2 \cdot \varepsilon(r-r')} dr' = -\int_{-\infty}^{0} \frac{q^2 \left|\psi(r',t)\right|^2}{2 \cdot \varepsilon(r+r')} dr'$$

(eq. II-89)

1. For electrons of energies well above the barrier, we can consider that the charge is localized. In the classical limit of a point charge the wavepacket reduces to a delta function $\psi(\mathbf{r})=\delta(\mathbf{r}-\mathbf{r_0})$ where $\mathbf{r_0}$ is the position of the electron, and the classical image force is predicted.
2. For electrons below the top of the barrier, at energies for which the transmission coefficient is smaller than unity, the wavepacket on the semiconductor side of the interface can still be considered as a superposition of plane waves, but its charge distribution is given by $TRq|\psi(\mathbf{r})|^2$, with TR the wavepacket transmission probability of the interface.

Therefore, the image force term will be modified by the transmission probability of the interface. This phenomenon being known, and because the solving of the wavefunction integral is a difficult problem, a relatively user-friendly generalization of the image force potential is provided in [*Hartstein'79*]. It still implies that the wavefunction of the incident electrons can be described as a δ function even in the barrier region, but the weighing of the potential by TR remains from the analysis above.

$$\Psi_{im}(E,x) = -TR(E)\frac{q^2}{16\pi\varepsilon_s x}$$

(eq. II-90)

- As TR weighs ψ_{im} and ψ_{im} increases TR by modifying the barrier shape, both have to be calculated self-consistently.
- The barrier shape is "perceived" differently by electrons of different energies.
- For electrons of energies for which TR cannot be larger than 0 (*eg.* energies beyond that of the conduction or valence band at W_{dep}), the image force lowering is not visible, which means that the turning point x_1 is located at the interface. This way, **the potential divergence issue is solved**.
- To each energy corresponds a barrier shape, but it is possible to re-construct an effective barrier by evaluating the turning points x_1 and x_2 at each energy. Figure II-40 below shows the calculated effective barrier shapes corresponding to the first three iterations on a metal/p-Si contact. The initialization case correspond to Ψ_{dep} only (no image force), on the basis of which the transmission coefficient is calculated for weighing the energy-dependent Ψ_{im}, yielding the total potential of iteration 1 and so forth.

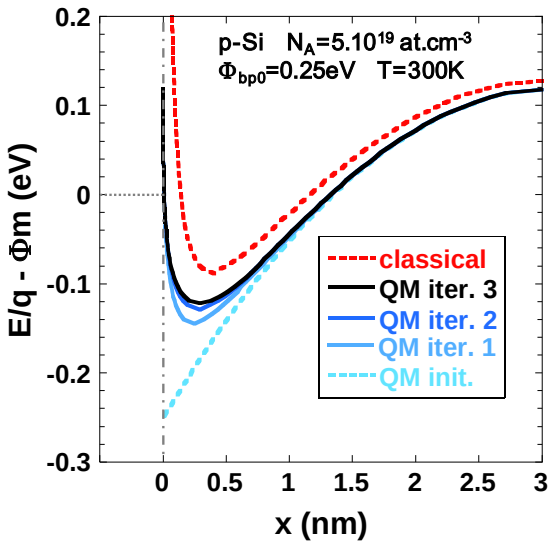

Figure II-40: Valence Band profile for a metal/p-Si contact considering the classical expression of image force potential, and reconstructed effective barriers for three iterations of the self-consistent modelling based on weighing by the transmission probability at each energy.

The results of this approach seem to converge towards a somehow intermediate solution, showing that the classical formulation of the image force potential leads to an overestimation the barrier lowering, an underestimation of the barrier thickness, and therefore an overestimation of both tunneling and thermionic current.

It should be noted, however, that the iterative approach can be significantly long in terms of computation time. It is nevertheless probably the most adequate for predictive quantitative evaluations. In addition, it is compatible with TCAD simulation as the boundary condition $x_1=0$ at $E=q.\Psi_{dep}(W_{dep})+q.\Psi_{im}(W_{dep})$ prevents the potential from diverging.

II.4. Conclusion

In this chapter, we have reviewed the mechanisms conditioning the formation of the potential barrier arising at the metal/semiconductor interface. Its effective value does not depend only on the metal workfunction and position of the Fermi-level in the semiconductor. It is modulated by Metal-Induced Gap States and surface states through the phenomenon of Fermi-level pinning. In addition, the image force changes the height and shape of the barrier.
If the barrier is large, the interfacial current can easily be modeled by the Thermionic Emission - Diffusion theory. The contribution of majority carriers' diffusion in the Space Charge Region is not especially relevant for high mobility semiconductors like Si and Ge.
For highly doped interfaces or at low temperatures, however, the Field Emission process cannot be ignored. Simplified expressions provide means to evaluate its contribution without having to compute the integrals in energy weighed by the transmission probability. One is based on the ideality factor η, indicating to which extent the experimental results stray from the TE theory. This method is limited in terms of quantitative interpretations. The other method is more sophisticated, but is based on the assumption that one of the transport mechanisms (Thermionic Emission, Thermionic Field Emission, or Field Emission) dominates and should be the only one to be considered.

Experimental characterization techniques derive from these models. Most of them are easy to use (I-V, activation energy, C-V, photoemission), but much more efficient and accurate when the barrier is large. Other approaches are more suitable for the cases of small barriers or contacts on degenerately doped semiconductors. But they depend on an increased number of parameters (more sources of uncertainty), and are limited by the consideration of a single dominant interfacial current transport process.

We have then studied in further details the impact of SBH, doping, temperature and bias conditions on the nature of the interfacial current, through 1-Dimensional analytical modelling of Schottky contacts, computing the energy integrals and simultaneously accounting for the three transport mechanisms. Qualitatively, this enabled us to correct some assumptions generally made on the predominance of tunneling-based current at high doping levels. Additionally, the predominance of a particular transport process is not necessarily obvious, and assuming so can lead to quantitative errors.

We also could see to which extent the accurate evaluation of the contact resistivity relies on a proper definition of the parameters (*eg* Richardson constants, effective masses), as well as on an accurate modelling of the potential profile. In particular, the classical modelling of the image force can still be improved in a non-divergent, self-consistent way in agreement with quantum-mechanical principles. But this can lead to fairly long calculation times, for reaching a level of accuracy that we do not necessarily need for the purposes of the present study.

Quantitative prediction of the electrical behavior of a Schottky junction is far less straightforward than it might seem at first glance. Nevertheless, in order to conclude on the requirements for a Schottky contact suitable for CMOS logic applications, we can sum up by making the following remark. The contact resistivity in reverse bias (majority carriers circulating from metal to semiconductor) reaches its minimum value when the barrier vanishes **and** the Fermi-level in the semiconductor is beyond the VB (or CB) edge so as to maximize the number of available states for conduction (cf. contact resistivity of zero-barrier contacts on lightly-doped Si or Ge on Figure II-35 and Figure II-36). In MOSFETs, the "pure Schottky" approach (no interfacial doping) is interesting for the control of Short Channel effects. Yet, according to our 1-D case, even if the intrinsic SBH could be lowered to a value of 0eV (which in practice would require Fermi-level depinning), the contact resistivity on an undoped semiconductor could be superior by roughly one order of magnitude with respect to that of a contact on degenerately doped Si or Ge (see the cases $N_A=10^{15}$ at.cm^{-3} vs. $N_A=10^{20}$ at.cm^{-3}). This trend is even more pronounced for larger SBH values (see Figure II-38 at zero bias: a difference of 2 orders of magnitude at $\Phi_{bp0}=0.4$eV between the cases $N_A=8.10^{18}$ at.cm^{-3} vs. $N_A=10^{20}$ at.cm^{-3}). Yet, we should keep in mind these values are based on the assumption that the distance between the two electrodes is superior to the SCR width. In practice, if the distance between Source and Gate is less than W_{dep}, the barrier might become thinner and ρ_c lower.

In spite of the advantages that an atomically sharp junction on an undoped semiconductor could bring in terms of electrostatic control, a high interfacial doping seems unavoidable to optimize the carriers' injection efficiency/parasitic resistance. An intermediate solution would be to achieve the highest doping level possible, while controlling the junction abruptness. The difference of such an approach with respect to traditional p/n junction MOSFETs with silicided access would then become quite subtle.

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Chapter III. **The Schottky-Barrier MOSFET on SOI substrate**

In this chapter, based on the previously presented knowledge on metal/semiconductor contact properties, we will review the principles of operation of the Schottky MOSFET. After having defined the technological requirements to maintain its competitiveness relatively to conventional MOSFETs with doped Source and Drain on SOI, we will evoke the various challenges in terms of device integration, so as to provide elements of answer regarding the future perspectives of this architecture.

III.1. Introduction

III.1.1. History of the Schottky-Barrier MOSFET

A short history of the Schottky-Barrier MOSFET (SB-FET) is provided in a thorough review by Larson and Snyder [*Larson'06*]. The idea of completely replacing doped S/Ds with metal was first proposed in 1966 by Yoshio Nishi, who submitted a patent issued in 1970 [*Nishi'70*]. The first paper on the topic was published in 1968 by Lepselter and Sze [*Lepselter'68*], featuring a bulk pFET with PtSi S/D. Yet, the poor performance of the presented device (one order of magnitude lesser drive current than on conventional MOSFETs at the time) led to a decade of inactivity on the matter.

Ten years later, Koenecke showed the strong dependence of drive current on the distance between gate edge and S/D electrodes edges [*Koenecke'81*]. This started a renewal of interest for Schottky MOSFETs, with publications treating of:

- The benefits of an interfacial doping layer to increase the drive current [*Koenecke'82*], [*Oh'84*], [*Swirhun'85*]
- A first demonstration of a Schottky nFET [*Mochizuki'84*]
- Asymmetric devices with metal Source and doped Si Drain [*Tsui'89*], [*Kimura'94*].

It was also shown that the use of Schottky Barrier MOSFETs (SBFET) could eliminate parasitic bipolar effects [*Sugino'82*], [*Sugino'83*], [*Swirhun'85*], by demonstrating a latchup-immune CMOS structure featuring a conventional nFET and a p-SBFET.

Since 1994, the SBFET has been investigated in the light of its advantages for device scaling [*Tucker'94-a*], [*Tucker'94-b*], [*Snyder'96*], resulting in significant advances in state-of-the-art process technology.

III.1.2. Reasons to chose Metal S/D over p/n junctions

We shall recapitulate in this paragraph the basic reasons which motivated the study of Schottky junction transistors as an alternative to conventional p/n junctions MOSFETs for aggressive nodes. We will then summarize and see the extent at which these various advantages are relevant and can be combined in practice in the SOI case.

III.1.2.a. Series resistance reduction

With scaling, the extrinsic parasitic resistances become increasingly detrimental to the ON-state properties of conventional MOSFETs. The commonly admitted model for describing the drain current in saturated regime I_{Dsat} for long-channel devices has long been the following:

$$I_{Dsat} = \frac{1}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot \mu_{eff} \cdot C_{ox} \cdot (V_{GS} - V_T)^2$$

(eq. III-1)

where W_{eff}, L_{eff}, μ_{eff} are respectively the effective channel width, channel length and mobility in the channel; C_{ox} is the gate capacitance (oxide permittivity ε_{ox} over oxide thickness or equivalent oxide thickness T_{ox}); V_T is the threshold voltage. This is inadequate for short-channel devices, due to the effects of velocity saturation, V_T roll-off, mobility degradation at high transverse effective field, and Source and Drain Series resistance.

In [*Chen'96-a*], an approximation is proposed to express $I_{Dsat}(R_S)$ as a function of I_{Dsat0}: the saturation current corresponding to R_S=0Ω. Note that R_S corresponds to the series resistance for the Source end only.

$$I_{Dsat}(R_S) = I_{Dsat0}\left(1 - \frac{2 \cdot I_{Dsat0} \cdot R_S}{V_{GS} - V_T} + \frac{I_{Dsat0} \cdot R_S}{V_{GS} - V_T + E_{sat} \cdot L_{eff}}\right)$$

(eq. III-2)

where E_{sat} is the ratio of v_{sat} the saturation velocity to μ_{eff}. It is obvious from this expression that the saturation drain current at high V_{GS} can decrease significantly with increasing series resistance.

Ng and Lynch [*Ng'86*] proposed a model for R_S decomposition in conventional MOSFETs pictured below.

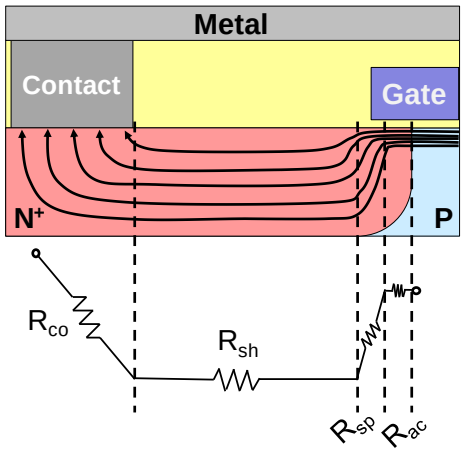

Figure III-1: Parasitic series resistance representation on a cross-sectional view of a conventional nMOSFET (source side), and sketching of the current lines.

R_{co} is the contact resistance, R_{sh} the sheet resistance in the doped region. R_{sp}, called spreading resistance, corresponds to the current lines crowding near the channel. R_{ac} is the resistance in the overlapping Gate/Source region where the current mainly remains near the surface. In this model, the (R_{ac}+R_{sp}) quantity is related to the doping gradient near the junction. Qualitatively, it decreases with increasing lateral doping profile abruptness.

Using fully metallic S/D obviously results in decreasing R_{sh}, due to the lowering of the resistivity in the region between gate and contact. The junction being *a priori* atomically abrupt, we can imagine that R_{ac}+R_{sp} are significantly lowered. R_{co} near the contact plug becomes negligible (metal/metal contact), but another R_{co} component appears near the channel edge, directly conditioning carrier injection at the Source (Figure III-2).

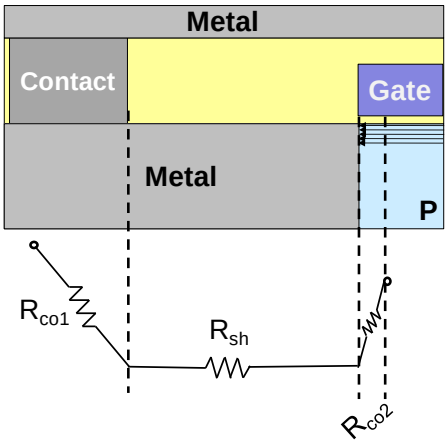

Figure III-2: Parasitic series resistance representation on a cross-sectional view of a SB-FET (source side), and sketching of the current lines.

According to this first order analysis, whether the SB-FET architecture represents an asset in terms of series resistance reduction with respect to the conventional MOSFET boils down to the optimization of the R_{co2} component. We have seen in the previous chapter that the contact resistivity of usual metal/alloys on lowly doped semiconductors was not necessarily low, even for a 0eV Schottky Barrier Height. The lowering of R_{co1}, R_{sh}, R_{ac} and R_{sp} should not be overshadowed by a high R_{co2} located exactly at the channel edge.

In the SOI case, calculations and design considerations were made so as to determine for which contact resistivity values a full silicidation of the Silicon film (body thickness ~10nm) would be advantageous in terms of total access resistance [*Su'94*], [*Dubois'02*], [*Poiroux'09*]. As it turns out, fully metallic Source and Drain would eventually degrade the total R_S unless the specific contact resistivitiy ρ_c of the Metal/Si contact is lower than 10^{-8} $\Omega.cm^2$. This value seems difficult, if not impossible to reach with regards to the usual range of Schottky Barrier Heights on undoped semiconductors.

III.1.2.b. Low temperature processing

The electrical activation of impurities in the S/D regions requires annealing steps at high temperature (typically 1050°C in Si). In addition to the energy consumption used during the fabrication process, this is an issue in terms of thermal stability of the other components of the transistor. For instance, in MOSFET structures with high-κ and metal gate, a SiO_2 capping layer is often used for Si/high-κ interface passivation purposes. A high thermal budget for S/D activation can result in EOT increase [*Batude'09-a*]. Furthermore, in the event of a sequential 3D integration scheme [*Batude'09-b*], the fabrication process of the upper stage should not degrade the performance of the bottom stage transistors. For these reasons, a low temperature processing for junction formation is always welcome, and silicidation typically occurs for temperatures in the range of 400-500°C. We will see later in this chapter (paragraph III.3.3.) that even in the event that dopant activation is required to enhance the Schottky MOSFETs performance, it is possible to achieve it with little to no increase of the thermal budget.

III.1.2.c. Immunity to Short Channel Effects and variability

A major issue in ultimately scaled transistors realization is the effect of random dopant fluctuation on threshold voltage variability [*Weber'08*]. This is mainly related to the differences in Short Channel Effects (SCE) control from one device to another.

As *a priori*, no dopants are involved in Schottky junctions formation, Schottky MOSFETs might seem interesting from this point of view. Atomically sharp, undoped Schottky junction would provide immunity to Drain Induced Barrier Lowering and electrical gate length reduction due to the lateral gradient of highly doped p/n junctions.

In practice though, non negligible variability issues have been reported on SOI Schottky MOSFETs, related the control of the Schottky Barrier Height, itself linked to the formation of the silicide (interface quality, lateral penetration depth) [*Feste'08*]. In addition; the introduction of dopant segregation layers at the Source and Drain would lower the variability associated to inhomogeneous Φ_b, but bring us back to the case of conventional MOSFETs with doped S/D.

III.1.2.d. Latch-up and parasitic bipolar effects

Latch-up can occur in bulk CMOS architectures if no specific design precautions (*eg* guard rings) are taken. If we consider an inverter (Figure III-3) with an n-well implant, a pair of parasitic bipolar transistors arises as a byproduct of this configuration.

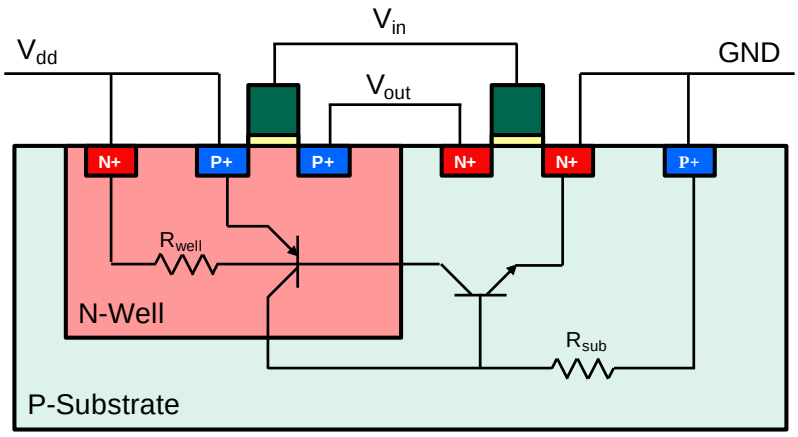

Figure III-3: Cross-sectional schematic of a Bulk CMOS inverter with the parasitic bipolar transitors arising from this configuration (vertical PNP and lateral NPN, the base of each being connected to the collector of the other).

The collector of each parasitic bipolar transistor is connected to the base of the other, forming a positive feedback structure. A path of low resistance is created between V_{dd} and GND when both BJT conduct. If the product of the gains of the two transistors in the feedback loop is greater than unity, latchup occurs and can result at the minimum in circuit malfunction (worst case: device destruction). This can be avoided by reducing the well and substrate resistances, for instance implementing guard rings with frequent contacts to the rings in the periphery of the n-well.

This circuit latch-up is eliminated using Silicon-On-Insulator substrates, where the n-well implant region is limited by the interface with the Buried Oxide. However, in a Partially-Depleted SOI configuration, lateral parasitic bipolar transistor remain (*eg* between Source and Drain), and are responsible for single-transistor latch at high drain biases [*Chen'88*]. Holes can be generated at the Drain, which forward bias the body-to-Source p/n junction, raising the potential of the floating body, reducing the threshold voltage and increasing the Drain current (kink effect). This floating-body effect can result in an abrupt increase of the circuit power and loss of functionality at the typical operating voltages.

Latch-up and single-transistor latch are highly sensitive to the bipolar emitter efficiency of the MOSFET Source. A rectifying Schottky junction is generally a poor minority-carrier injector. As a matter of fact, the common-emitter gain of a Schottky junction has been shown to be three to six orders of magnitude lower than that of a conventional Source junction [*Sugino'83*]. Therefore, the use of Schottky Source and Drain leads to a natural immunity to latch-up and single-transistor latch regardless of substrate type and doping level, V_{dd} and layout.

III.1.2.e. Relevance of these advantages in the SOI case

Table III-1 below summarizes the advantages evoked above, and the conditions under which they remain relevant and can be combined in the framework of integration on SOI substrates.

Advantages	**Reasons**	**Remarks**
Series resistance reduction	Low sheet resistivity of the metal	Advantage conserved on thin SOI only if $\rho_c<10^{-8}$ $\Omega.cm^2$ **Interfacial doping seems inevitable**
Low temperature processing	Low temperatures for silicidation	If interfacial doping required, **low temperature activation is still possible with dopant-segregation techniques**
SCE, variability	No SCE, no variability associated to SCE	There should be **no doping**, and process-induced **variability due to inhomogeneous Φ_b remains**
Parasitic bipolar effects	Low bipolar emitter efficiency of Schottky Junctions	Latch-up: **only relevant on bulk** substrates Single transistor latch: **true if no interfacial doping**, and only relevant on Partially Depleted SOI substrates

Table III-1: Summary of the previously evoked advantages of Schottky MOSFETs, and remarks on their validity in the case of device integration on SOI substrates.

The fact that there is no known metal which could provide an intrinsic SBH low enough to satisfy the conditions on ρ_c highlights the necessity of implementing interfacial doping. Therefore, on SOI substrates, the only remaining advantages of the Schottky approach with respect to, for instance, conventional MOSFETs with partially silicided S/D, are low temperature processing and (possibly) series resistance reduction. In the following, we will review in further details the electrical behavior of Schottky-Barrier devices.

III.2. DC characteristics of Schottky MOSFETs

This section aims at reviewing the basic principles of operation in a Schottky MOSFET, and at identifying the mechanisms that distinguishing them from the processes occurring in conventional MOSFETs with doped Source and Drain. This will lead to a proper interpretation of the experimentally obtained characteristics and set the basis for defining paths towards process integration optimization.

III.2.1. ON-State and OFF-State

III.2.1.a. Basic principles

Let us consider the examples of a conventional pMOSFET (with doped p-type Source and Drain), and that of a Schottky MOSFET with a low barrier for holes (*eg* Pt or Ni-based Source and Drain). The OFF-State bias conditions are defined as V_{GS}=0V and V_{DS}=V_{dd}<0V. The ON-State conditions are V_{GS}=V_{DS}=V_{dd}<0V.

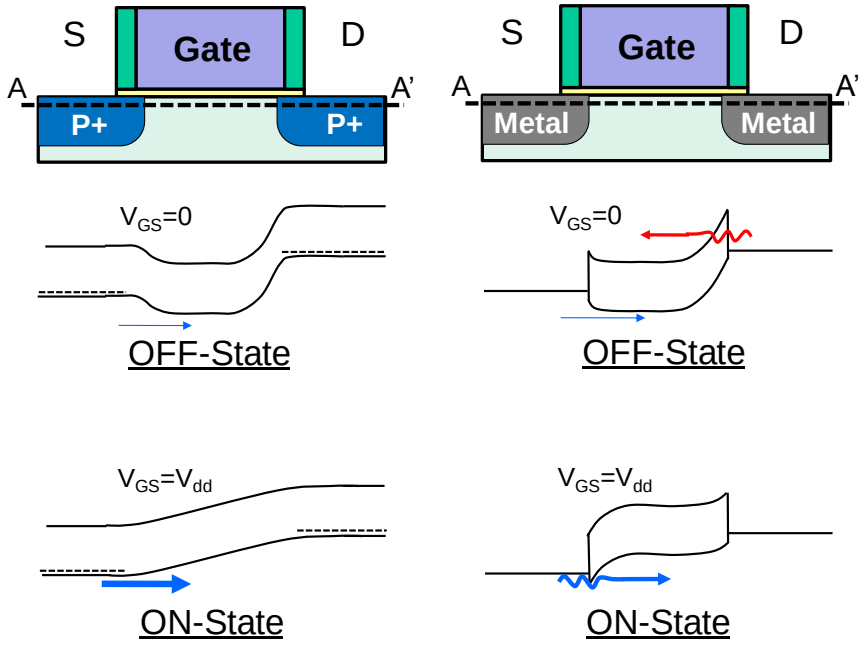

Figure III-4: OFF-State and ON-State simplified longitudinal band diagrams in a conventional pFET (left) and in a Schottky Barrier MOSFET with a low barrier for holes (right).

Case of the conventional MOSFET

At OFF-State, holes on the Source side face a smooth potential barrier arising from the built-in potential (Ψ_{bi}) corresponding to the Fermi-level difference within the Source and within the (*a priori* undoped) channel. The leakage current is determined by holes diffusing through the Space Charge Region. On the Drain side, the concentration of electrons is as negligible as the concentration of ionized acceptor impurities is high. There is no significant flow of electrons drifting from Drain to Source, except for direct Band-to-Band Tunneling (which may typically occur if $V_{GD}+\Psi_{bi}>E_g/q$). We can assume for the sake of simplicity that there is no Drain-related leakage current.

At ON-State, within the inversion layer, the potential barrier is removed and holes can freely drift from the Source towards the Drain.

Case of the Schottky MOSFET

At OFF-State, holes on the Source side face an abrupt potential barrier arising from the mechanisms described in details in the previous Chapter (mostly Fermi-level pinning and doping level at the semiconductor interface). For guaranteeing good ON-State operation characteristics, this barrier is chosen to be low. The lower the barrier, the easier it can be overcome by thermally excited carriers, which would result in leakage current arising from holes circulating from Source to Drain. **Additionally**, unlike in conventional MOSFETs, the metallic Drain acts as a reservoir of electrons which can most of the time tunnel through a barrier rendered thin by the Gate-to-Drain bias (electrons flowing from Drain to Source). This ambipolar behavior is characteristic of Schottky MOSFETs, but highly undesirable in that it may dramatically increase the OFF-State current.

At ON-State, the Source-to-Channel junction is reverse-biased, facilitating thermionic emission (by image force lowering) and enabling tunneling on the Source side. Meanwhile, it becomes impossible for electrons from the Drain to tunnel into the channel.

In the light of this first-order analysis, the addition of p-type interfacial doping layers results in two advantages, as depicted on Figure III-5 below.

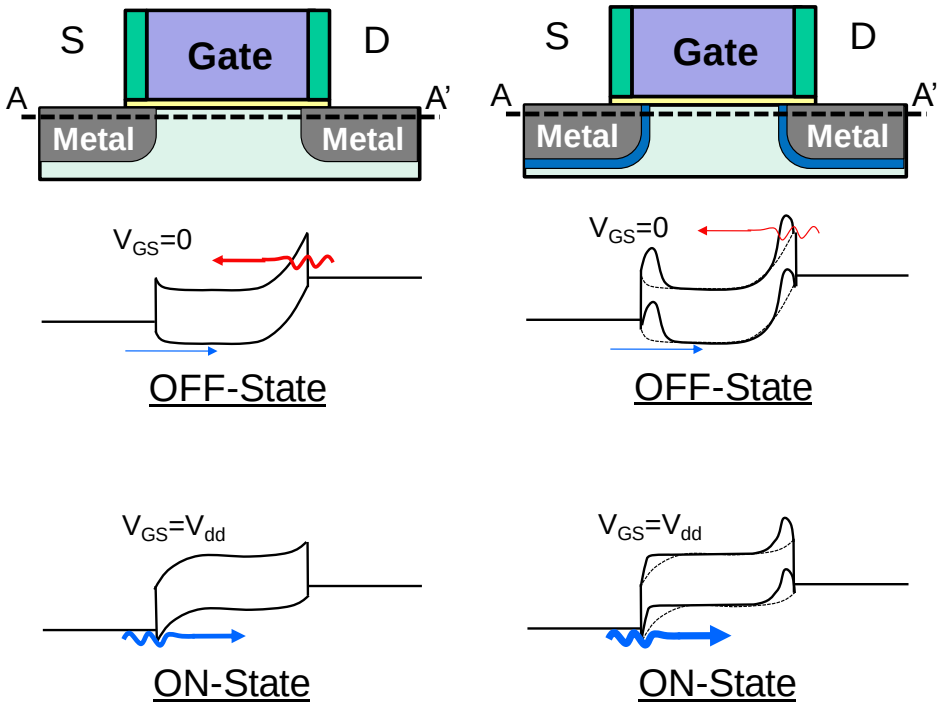

Figure III-5: OFF-State and ON-State simplified longitudinal band diagrams in a Schottky Barrier MOSFET without interfacial doping (left) and in the same structure with interfacial p-type doping (right). The superimposed dashed lines on the right part are reminiscent of the bands configuration in the undoped case (left).

On the one hand, the interfacial doping increases the ON-State current by thinning (and lowering) the barrier at the reverse-biased Source, as expected. On the other hand, it also enlarges the barrier on the Drain side at OFF-State, decreasing the Drain-to-Source electrons-induced leakage current.

Prior to quantitatively conclude on the Barrier heights and widths required to achieve ohmicity during injection, **it is very important to mention a fundamental difference** between the cases studied in the previous Chapter and the electrostatic configuration in a MOSFET. Previously, we treated the bias applied to the semiconductor as a boundary condition at infinity so that the Space Charge Region of the Schottky junction could build up to its full extent. In a Schottky MOSFET, if the underlap between Source and Gate is inferior to the SCR width, the built-in potential of the Schottky junction is screened by the Gate bias so that the resulting current density is **not equivalent** to what a One-Dimensional profile with a V_G bias applied on the semiconductor at infinity would yield. This principle is schematically shown on Figure III-6.

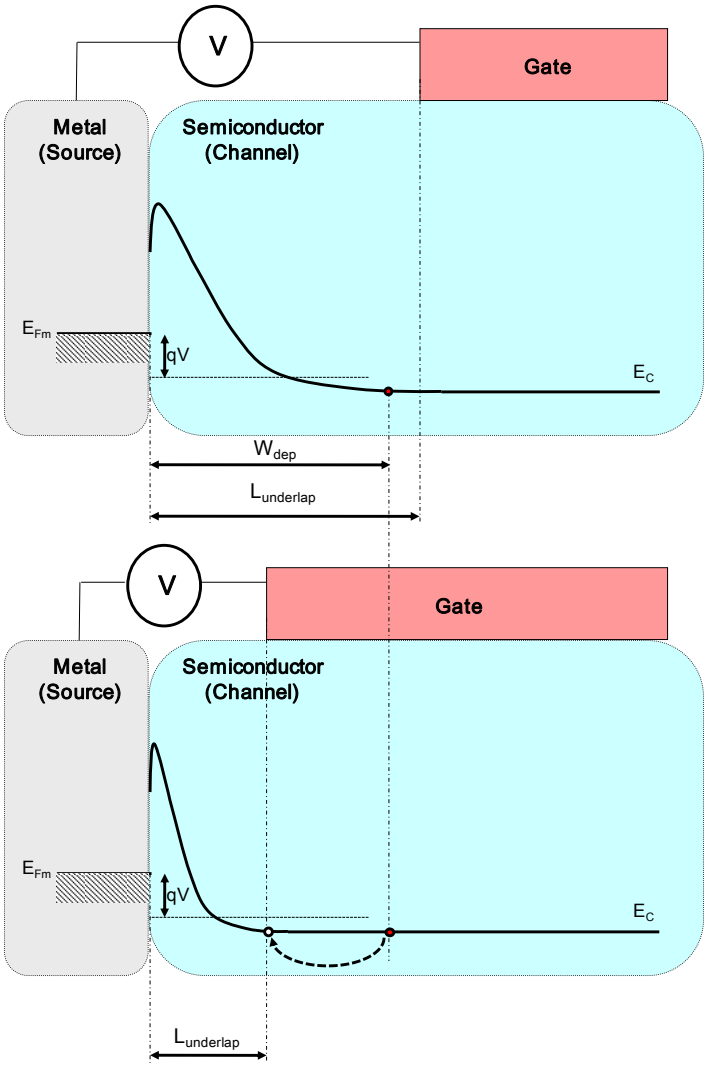

Figure III-6: Schematic description of the One-Dimensional surface potential associated to the Conduction Band of the Source-Channel Schottky junction in the cases where $L_{underlap}>W_{dep}$ (top) and $L_{underlap}<W_{dep}$ (bottom, screening of the Schottky junction built-in potential by the Gate bias).

As a consequence, the horizontal distance between Gate edge and Source/Drain edges is an important parameter to consider for OFF-State, ON-State and subthreshold characteristics.

III.2.1.b. Schottky nFET or pFET?

Whether a Schottky-Barrier MOSFET behaves as a pFET or an nFET is determined by both the choice of the metal and the doping conditions. But the importance of the SBH should not be underestimated, and it might take more than a "simple" n-type extensions implant before metal deposition to turn a PtSi S/D MOSFET (*ie* with a strong preference for holes injection) into an nFET, as illustrated by Figure III-7.

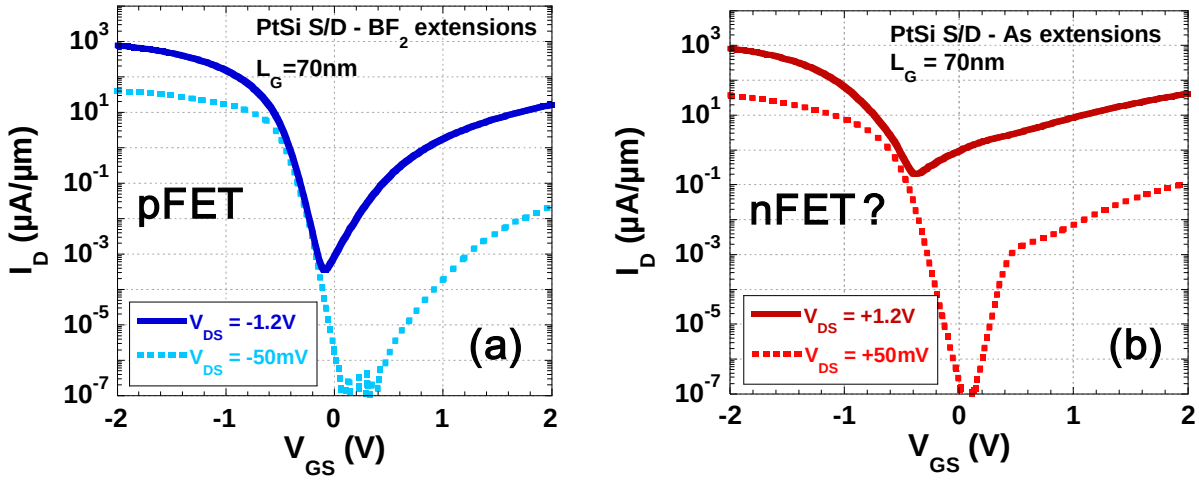

Figure III-7: Measured I_D-V_{GS} characteristics of (left) a PtSi S/D MOSFET with p-type BF_2 extensions and (right) a PtSi S/D MOSFET with n-type As extensions implanted and annealed before metal deposition.

This is of course, only for illustration purposes, and much more convincing results have been obtained for fabricating nFETs with PtSi S/D using more advanced dopant segregation techniques (see paragraph III.3.4.b.). But it gives a strong visual idea on how essentially ambipolar Schottky MOSFETs can be distinguished from conventional FETs with a surface silicidation.

III.2.1.c. Ambipolarity analysis

The following data were included in a study on Single and Double Gate planar MOSFETs on FDSOI with metallic Source and Drain [*Hutin'09*]. In particular, Figure III-8 below reports measured and simulated (using Silvaco Atlas TCAD tools) I_D-V_{DS} characteristics of a Single-Gate Schottky MOSFET with PtSi Source and Drain and p-type

interfacial doping. Morphologically, the structure is that of a Double-Gate MOSFET with a disconnected Bottom Gate acting as a ground plane and the Gate dielectric acting as Buried Oxide, hence the appellation SG UTBOx (Single Gate Ultra Thin Buried Oxide). As the Schottky barrier for holes is supposedly significantly lower than that for electrons, such a device (although ambipolar) can be designated as a pMOSFET.

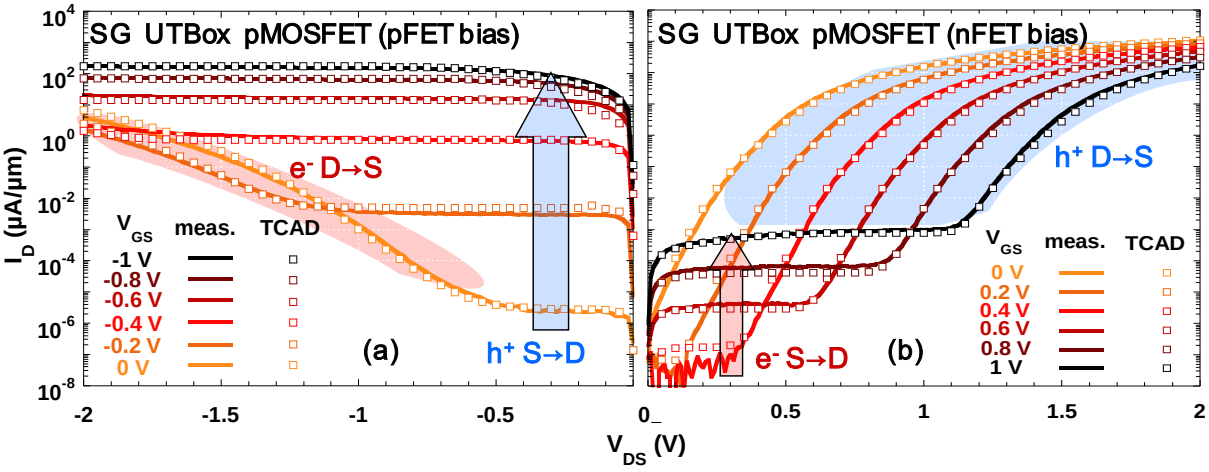

Figure III-8: Measured (lines) and simulated (squares) I_D-V_{DS} characteristics of a Single-Gate MOSFET with PtSi S/D and BF_2 extensions (L_g=70nm) under (a) pFET bias: V_{GS}<0; V_{DS}<0 and (b) nFET bias: V_{GS}>0; V_{DS}>0.

It is indeed immediately visible on these characteristics that in spite of interfacial doping, the device remains essentially a Schottky MOSFET. In fact, a transistor effect is visible both under pFET and nFET bias, and in the latter case for V_{GS} values lower than that of the Si bandgap energy (direct Band-to-Band Tunneling discarded). As confirmed by the TCAD simulation, these regions of the curves forming a plateau correspond respectively to (a) holes and (b) electrons current flowing from Source to Drain.

Reciprocally, the regions of the curves under the colored areas are relevant to the study of OFF-State in Schottky devices. On Figure III-8 a), the corresponding process is a flow of electrons emitted at the Drain, as explained in Figure III-9.

Figure III-9: Schematic cross-sectional band diagrams in the channel direction under pFET bias at a given negative V_{DS} bias x with V_{GS}=0V (left) and at V_{DS}=x-0.2V; V_{GS}=-0.2V (right). The dashed lines on the right are reminiscent of the bands configuration on the left.

At V_{GS}=0V, applying increasingly negative V_{DS} biases results in increasing electrons tunneling from Drain to Source. V_{DS} has *a priori* no influence on holes injection on the Source side. As V_{GS} is set to -0.2V, holes injection is facilitated at the Source (corresponding to the higher plateau on Figure III-8 a) and electron tunneling at the Drain is impeded, until the same band configuration as in the previous case is obtained, *ie* V_{DS}=x-0.2V. This explains the -0.2V shift to the left of the part of the curve corresponding to Drain to Source electrons circulation.
Similarly on Figure III-8 b), the region under the colored area corresponds to a flow of holes emitted at the Drain, as explained by Figure III-10.

Figure III-10: Schematic cross-sectional band diagrams in the channel direction under nFET bias at a given positive V_{DS} bias x with V_{GS}=0V (left) and at V_{DS}=x+0.6V; V_{GS}=0.6V (right). The dashed lines on the right are reminiscent of the bands configuration on the left.

At V_{GS}=0V, applying increasingly positive V_{DS} biases results in increasing holes tunneling from Drain to Source. As V_{GS} is set to 0.6V, previously non-existent electrons injection is enabled at the Source (cf. plateau on Figure III-8 b)) and hole tunneling at the Drain is impeded, until the same band configuration as in the previous case is obtained, *ie* V_{DS}=x+0.6V, hence the shift of the part of the curves under the blue area.

Figure III-11 below shows the I_D-V_{DS} characteristics under "pFET bias" and "nFET bias" of the devices shown on Figure III-7 (paragraph III.2.1.b.). We can qualitatively observe how substituting As extensions to BF_2 extensions raises the plateaus corresponding to Source to Drain (resp. Drain to Source) electron conduction under nFET bias (resp. pFET bias). Nevertheless, the pFET transistor effect remains the strongest; hence the aspect of the I_D-V_{GS} curves on Figure III-7.

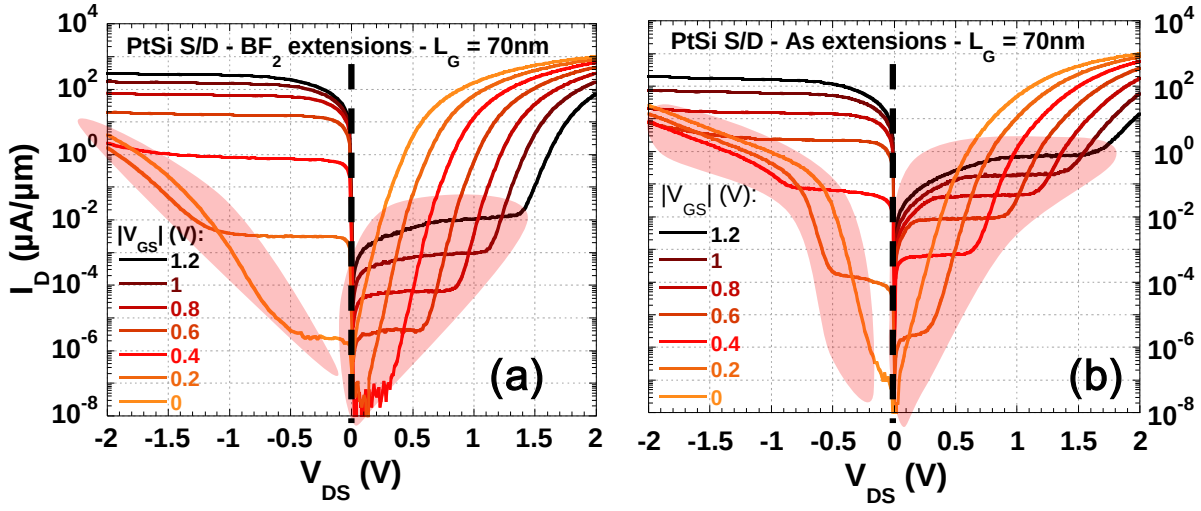

Figure III-11: Measured I_D-V_{DS} characteristics of Single-Gate MOSFETs (L_g=70nm) with PtSi S/D, (a) BF_2 extensions and (b) As extensions under pFET bias and nFET bias. The red areas highlight the plateaus associated to electrons injection.

Also, it is worth noting on Figure III-8 from the perspective of OFF-State current reduction is that even in this case with the technological implementation of interfacial doping layers at the Source and Drain contacts, the ambipolar behavior of the Schottky MOSFET is still responsible for 2.5 decades of leakage current at V_{DS}=-1V (cf. Figure III-8 a) at V_{GS}=0V).

III.2.1.d. Influence of doping abruptness

For a given device geometry, the two parameters that can be changed are the interfacial doping level, and the lateral doping abruptness. Let us first consider a given peak activation level at the interface of N_A=5.10^{19} at.cm^{-3}, which is the value used for fitting the experimental measurements with TCAD simulation. The electrically active doping profile which fitted the best the I_D-V_{GS} and I_D-V_{DS} characteristics was a Gaussian distribution with a lateral abruptness of roughly 3nm/dec, which is consistent with what can be obtained by flash-annealed (1050°C, 1s) Boron extensions in Si. Figure III-12 shows the change in Conduction Band profile in the vicinity of the Drain while keeping the same peak activation level and decreasing the abruptness to 5nm/dec.

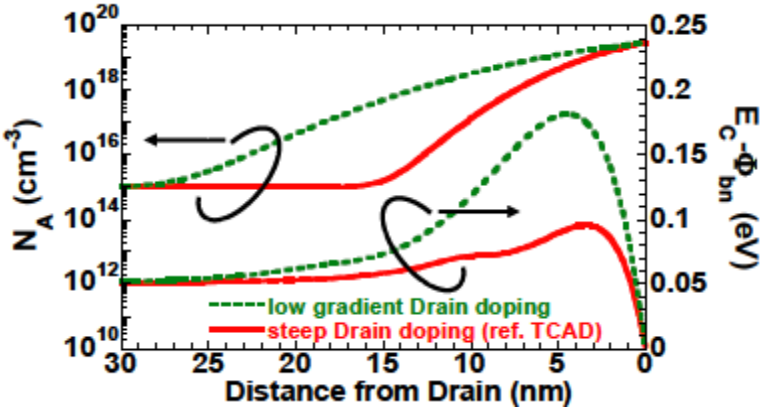

Figure III-12: Simulated impact of the Drain side doping lateral abruptness on the local potential barrier profile for electrons.

The reference (solid lines) "steep Drain" doping and CB profiles show a competition between the Space Charge regions of the channel-to-extensions p^+/p junction (channel doping $N_A=10^{15}$ at.cm^{-3}), and that of the Schottky junction. The interfacial doping layer is spatially too confined for the bump in the CB to build up to its fullest extent. This effect is not an asset, as the higher the bump, the higher the barrier for electrons and the lesser the leakage current. It seems to be alleviated by relaxing the lateral abruptness to lower gradients, increasing the effective SBH for electrons at a given peak active concentration.

Indeed, Figure III-13 shows that decreasing the Drain doping lateral abruptness from 3nm/dec to 5nm/dec at $N_{A,max}=5.10^{19}$ at.cm^{-3} results in a one decade improvement of the OFF-State current at V_{DS}=-1V.

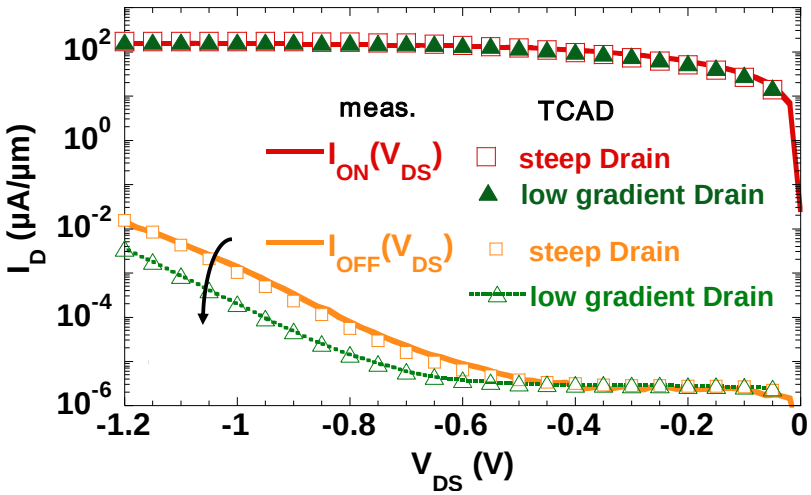

Figure III-13: Effect of lowering the Drain doping gradient on the D to S electrons current ruling I_{OFF} (V_{GS}=0V) at high V_{DS}, with simulated characteristics corresponding to the cases exposed in Figure III-12. I_{ON} (at V_{GS}=-1V) is not impacted, as the Source side doping profile was left unchanged (symmetrical to the "reference" Drain profile).

One can also notice that changing the Drain doping profile leaves I_{ON} invariant. Conversely, modifying the Source doping profile will affect I_{ON} as a deeper well in the

valence band improves hole injection, while leaving I_{OFF} unchanged. Eventually, as shown on Figure III-14 below, extremely steep profiles may yield lower I_{ON}/I_{OFF} ratios.

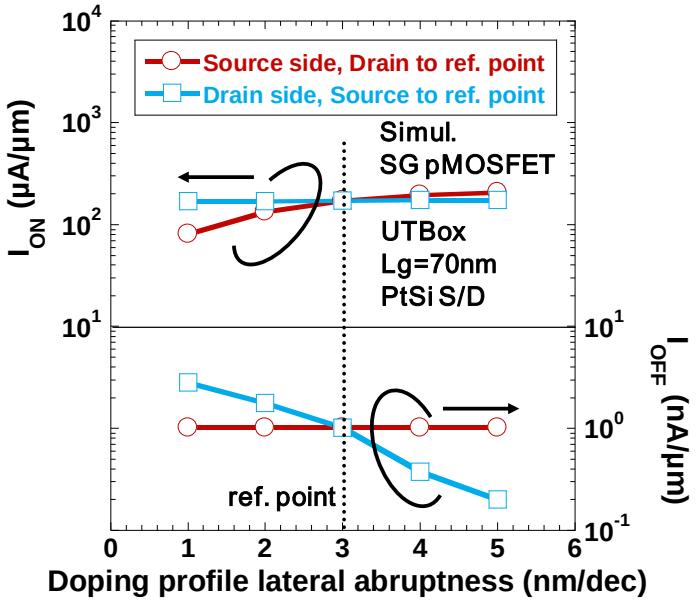

Figure III-14: Simulated influence of the Source side (circles) or Drain side (squares) doping abruptness on I_{ON} and I_{OFF}, while the other end is fixed at reference point (3nm/dec).

III.2.2. **Subthreshold regime in the Fully-Depleted SOI case**

The OFF-State of Schottky MOSFETs may also be limited by their sub-threshold characteristics. An approximate expression of the subthreshold swing in undoped Schottky MOSFETs on Silicon-On-Insulator (SOI) has been proposed by Knoch *et al.* [*Knoch'06*] in the case where there is no underlap between Source and Gate.

Intuitively enough, the subthreshold swing is closely related to the evolution with Gate bias of the transmission probability through the Schottky Barrier on the Source side. If the contact is ohmic (cf. flat $\rho_c(V)$ under reverse bias in previous chapter), the injection should be primarily limited by the expansion of the inversion layer with increasing Gate bias, and the theoretical limit of 60mV/dec can be reached in an electrostatically well tempered device. Reciprocally, a large barrier and a non-ohmic contact would result in drive current limitation at low V_{GS} which would necessarily impact the subthreshold characteristics.

III.2.2.a. Dependence on SOI thickness

The surface potential is determined in by a One-Dimensional model based on a modified Poisson equation [*Banna'95*] used together with the nonequilibrium Green's function (NEGF) formalism to self-consistently determine the charge in and current through the Schottky MOSFET [*Knoch'02*]. If the buried oxide thickness is large, the modified Poisson equation for the surface potential $\Psi_s(x)$ can be expressed as follows:

$$\frac{d^2\Psi_s(x)}{dx^2} - \frac{\Psi_s(x) - \Psi_g + \Psi_{bi}(x)}{\lambda^2} = \frac{q^2 \cdot \rho(x) \cdot \eta}{\varepsilon_s}$$

(eq. III-3)

where Ψ_g is the Gate potential, Ψ_{bi} the built-in potential of the Schottky junction, η a fitting parameter describing the non-uniformity of the lateral field across the SOI thickness (typically 1 in Ultra-Thin Body SOI MOSFETs). ρ includes the density of mobile charges as well as a constant charge background due to doping, and λ is defined as the characteristic length scale on which potential variations are screened:

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\eta \cdot \varepsilon_{ox}} \cdot T_{Si} \cdot T_{ox}}$$

(eq. III-4)

It has been shown [*Zhang'07*] that (eq. III-3) describes well the electrostatics of Fully-Depleted SOI Schottky MOSFETs for $T_{Si}/\lambda \leq 1.5$.

Let us consider the OFF-State case, where the density of mobile charges is small and we can assume ρ is constant (cf. background charge due to doping). In this situation, a simple analytical solution can be derived for (eq. III-3), showing an exponential screening of the Schottky Barrier (*ie* Ψ_{bi}) on the length scale λ. The smaller λ, the more efficiently the lateral Space Charge Region of the Schottky junction is screened, *ie* modulated by the Gate. In the subthreshold regime, it means that the reverse biasing of the source will be more efficient, as the barrier at a given depth will become thinner for lower values of V_{GS}, increasing the tunneling probability hence the current density. In conclusion, just like in conventional MOSFETs, the subthreshold swing is reduced by scaling both T_{ox} and T_{Si}.

III.2.2.b. Dependence on channel or interfacial doping

The modelling presented in [*Knoch'06*] to derive a simple expression of the subthreshold swing relies on a set of strong assumptions, but is qualitatively useful. The following hypotheses are made for the sake of simplicity:

- In the OFF-State ρ=0, as the density of mobile charges is negligible, and the substrate is supposed undoped
- V_{DS} is large and the effective barrier is larger than kT

- The transmission probability across the Source Barrier is supposed equal to 0 when the barrier width is larger than a distance d, and equal to 1 when it is thinner than d, as pictured on Figure III-15 below

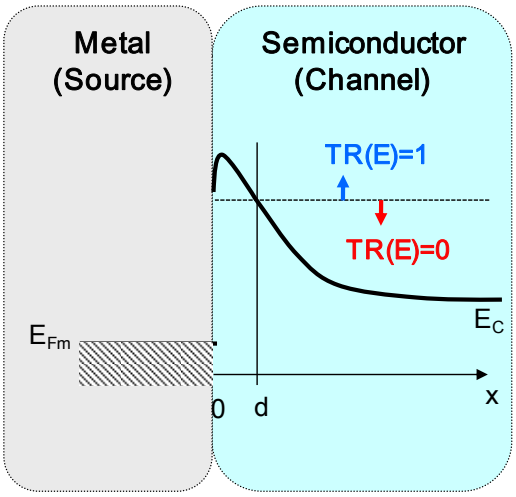

Figure III-15: Principle of the simplification used to establish the derive an expression for subthreshold swing in FDSOI Schottky MOSFETs [Knoch'06]. The transmission probability at a given energy is considered to be 1 if the barrier width at this energy is lower than a distance d, and 0 if it is larger.

The subthreshold swing S is derived from the expression of the drain current I_D as follows:

$$S = \frac{k \cdot T}{q} \cdot \ln(10) \cdot \frac{1}{1 - \exp\left(-\frac{d}{\lambda}\right)}$$

(eq. III-5)

Because in general λ>d, this result can be expanded:

$$S = \frac{k \cdot T}{q} \cdot \ln(10) \cdot \left(\frac{1}{2} + \frac{\lambda}{d}\right)$$

(eq. III-6)

According to [*Knoch'06*], if d is defined as the distance for which TR drops to e^{-2}, then it is typically comprised between 3 and 4nm and shows a weak dependence on the Schottky Barrier Height. As a result, (eq. III-6) the authors conclude that S can be considered as independent on substrate doping in the Fully-Depleted case.

This conclusion, however, is relevant as long as the barrier is strongly modulated by the Gate, *ie* in the case where there is no underlap between Gate and Source. There is no dependence on substrate doping in (eq. III-6) because the built-in potential $\Psi_{bi}(x)$ has little to no influence on the surface potential $\Psi_s(x)$ in (eq. III-3). This would obviously no longer be

the case within a hypothetical underlap region ((eq. III-3) no longer stands) as qualitatively explained below.

What really influences the current density at low V_{GS} is not so much d itself than the corresponding energy, above which TR(E) can be considered equal to one. For instance if we assume a significantly high substrate doping, a $L_{underlap}$ of about 10nm should enable the Schottky SCR to significantly expand before being submitted to the screening from the Gate potential. Thus, as shown on Figure III-16, the energy at x=d is lower in the highly doped channel configuration, leading to improved carrier injection in subthreshold regime.

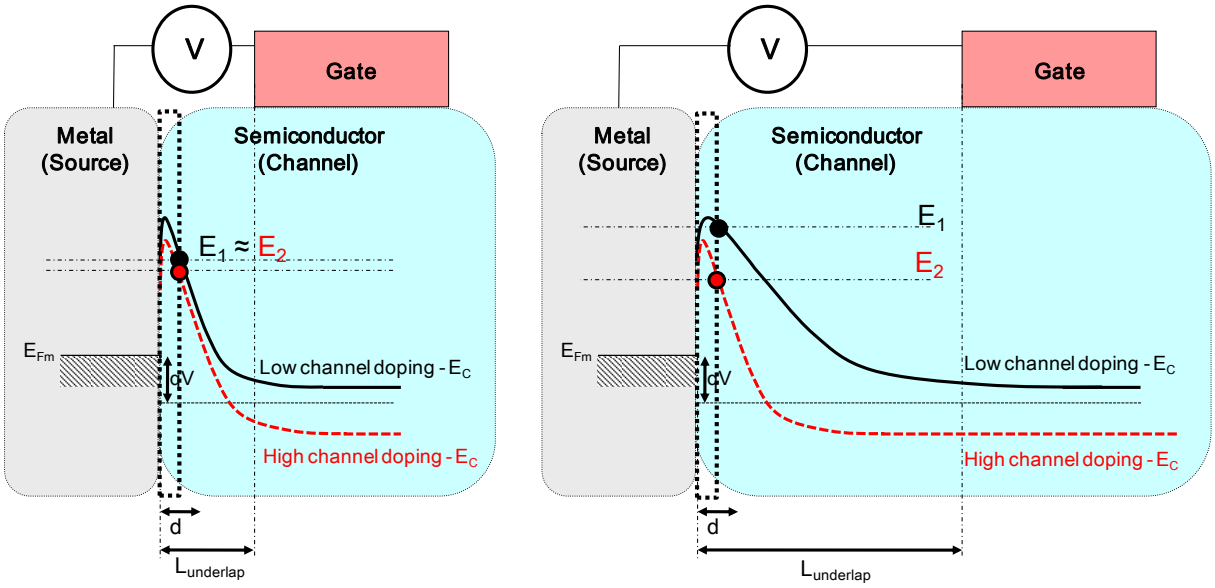

Figure III-16: Schematic band diagrams showing the increasing influence of channel (or interfacial) doping on the transmission probability while increasing the distance between Source and Gate edge.

The subthreshold swing S is improved by decreasing the SOI thickness. If the Gate and Source are underlapped, S depends on channel or interfacial doping. This dependence may vanish when reducing or eliminating the underlap.

III.3. Device integration

Two integration schemes will be presented in this section. The first consists in a damascene approach, in which cavities corresponding to the Source and Drain areas are filled with metal, silicidation is performed, and the gate is liberated with Chemical-Mechanical Polishing (CMP) steps. This approach can be advantageous in that it enables the integration of virtually any type of S/D metal without having to deal with the specific chemistry of selective removal of the unreacted metal with respect to the silicided areas. The definition of cavities,

however, can add significant process complexity. The second scheme is a more conventional self-aligned process with selective removal of the unreacted metal after silicidation annealing. As we will quantitatively evoke the performance of the resulting devices, the benefits of thin interfacial doped areas in the vicinity of the silicide/Si interfaces will be once again highlighted. Thus, a paragraph will be dedicated to the various techniques of dopant segregation.

Finally, we will compare the options for fabricating Metal S/D nFETs for Schottky CMOS. In particular, we will discuss the challenges related to adopting a Dual S/D Metal solution (*ie* with rare earth conduction band-edge silicides with a strong preference for electon injection for nFETs), and confront it to a simpler Single Metal scheme with separately optimized dopant-segregation conditions.

III.3.1. **Damascene Source and Drain**

III.3.1.a. Single Gate

The Single Gate, damascene process described in [*Poiroux'09*] is a variation of the standard FDSOI process [*Andrieu'06*] used in Leti. The Silicon in the Source/Drain regions is etched after spacers formation, and cavities are formed by reverse active area lithography. An additional tilted extension implant might be performed before metal deposition, in this case 6nm of Platinum. After silicidation (at 450°C to limit the lateral penetration of the silicide under the spacers), a W/TiN/Ti stack is deposited to fill the cavities. TiN acts as a diffusion barrier for fluorine (cf. subsequent conformal tungsten CVD deposition with a WF_6 precursor), and studies showed much reduced contact resistivities using a TiN/Ti stack, possibly due to a smoother interface than in the "TiN only" case. The metal stack is finally planarized so as to liberate the Gate electrode (Figure III-17).

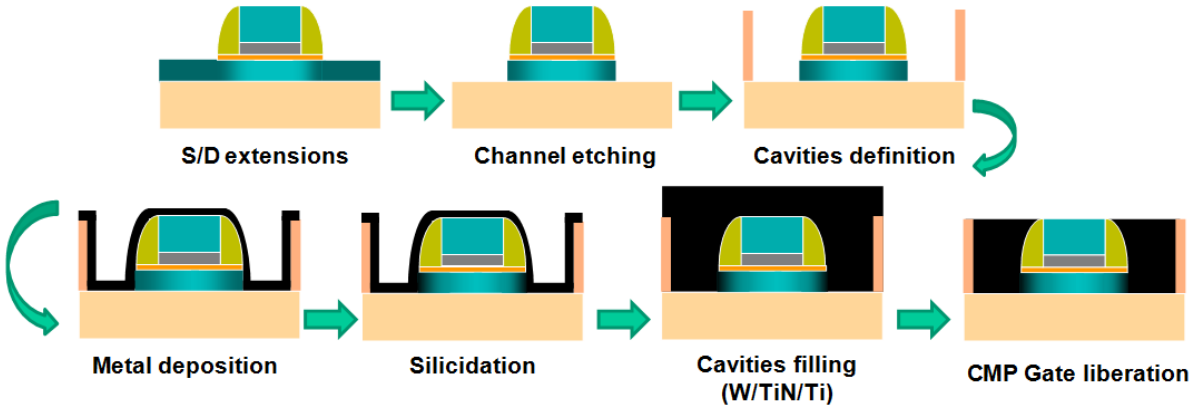

Figure III-17: Schematic process flow of the damascene integration scheme for metallic Source and Drain MOSFETs on SOI.

The mean value of the measured contact resistivity using this doping and metallization process was of 6×10^{-9} $\Omega.cm^2$, in line with the requirements for access resistance optimization

on metal S/D FDSOI MOSFETs [*Su'94*], [*Poiroux'09*]. The fabricated pFETs exhibit good performance (I_{ON}=345 µA/µm, I_{OFF}=30nA/µm, L_G=50nm, V_{DS}=-1V).

III.3.1.b. Double Gate

This metal S/D integration scheme was taken one step further in [*Vinet'09*] by combining it with the realization of Double Gate MOSFETs by molecular bonding.

The starting material being SOI wafers, the process starts by depositing the Back Gate stack (3nm ALCVD HfO_2, 5nm PVD TiN, 50nm *in situ* doped poly SiGe). After the deposition and the planarization of an oxide encapsulation layer, the wafers are bonded onto oxidized bulk Si substrates. The Si channel is then etched and the Front Gate (FG) stack is formed on top. Figure III-18 summarizes the following steps.

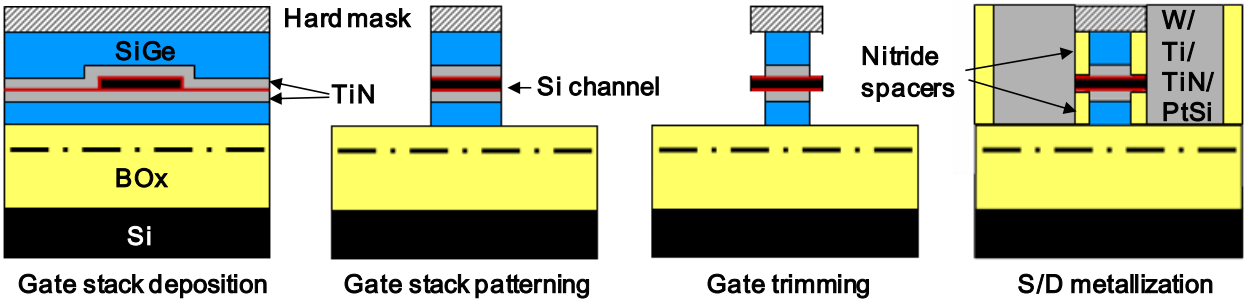

Figure III-18: Simplified process flow of the self-aligned Double Gate Metal S/D MOSFETs fabrication [Vinet'09], [Hutin'09].

The whole stack (channel and gates) is patterned down to the Buried Oxide, using HBr/O_2 chemistry for the SiGe gates and Si channel, and BCl_3 for HfO_2. Both SiGe gate lengths are defined thanks to a selective isotropic plasma etching (CF_4/O_2, leaving the channel and hard mask unchanged), and TiN is removed using an HCl/H_2O_2 solution. Extensions are then implanted, and nitride spacers patterned, followed by the damascene approach described in the previous paragraph. An X-TEM view of the final device is shown on Figure III-19 below.

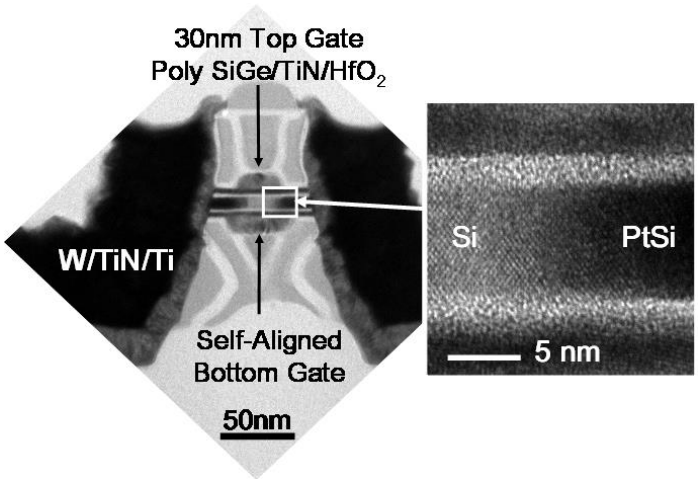

Figure III-19: Cross-sectional Transmission Electron Microscopy pictures of (left) a device with 30nm gate length and (right) the PtSi/Si interface (pictures: D. Lafond).

This process is self-aligned, and the BG and FG lengths are close to each other, being defined by the same isotropic etching. The total resistance $R_{channel}+R_{access}$ was measured for various L_g at high V_{GS}, and was found to saturate close to 400Ω.µm ($R_S \approx R_D \approx 200$Ω.µm, in line with state-of-the-art technologies [*Yako'08*]).

III.3.1.c. Performance and scalability assessment

The structures presented in [*Poiroux'09*] and [*Vinet'09*] were compared and analyzed in [*Hutin'09*]. The simplified process flow and different configurations are recapitulated Figure III-20.

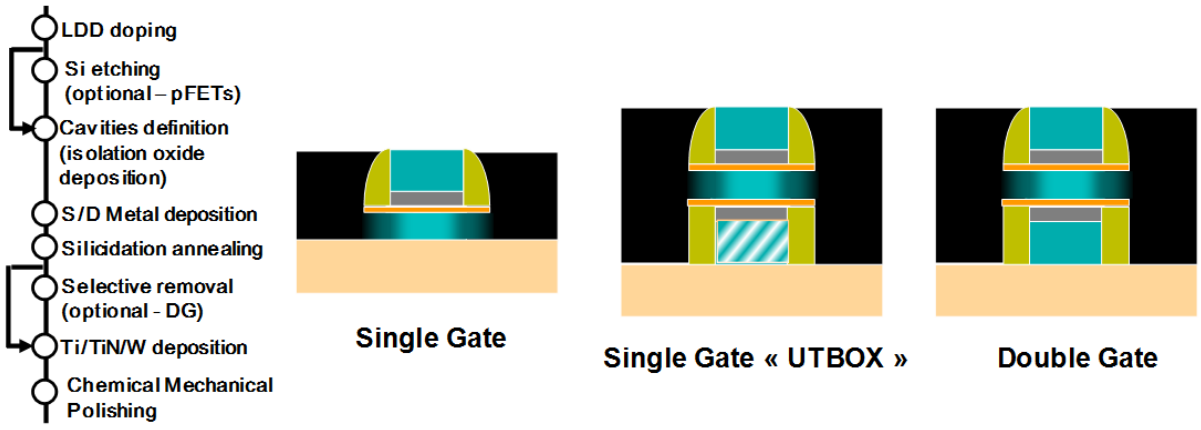

Figure III-20: Simplified process flow of S/D metallization, and schematic representations of the various MOSFET structures fabricated. Single Gate (SG), Single Gate with a disconnected bottom gate acting as an Ultra Thin Buried Oxide (SG UTBox), and Double Gate (DG), all featuring interfacial p-type doping.

Prior to studying their performance, it was shown that the carrier injection in these devices was still conditioned by the metal/Si junction (cf. paragraph III.2.1.c.) - although improved by interfacial doping (cf. III.2.1.d.) -, which distinguish them from conventional MOSFETs with silicided S/D. This is also visible on Single Gate pFETs I_D-V_{GS} characteristics Figure III-21, where the change of metallization (NiSi versus PtSi) affects not only the ON-state, but also the OFF-state current. Additionally, an increase in dose and activation thermal budget of the BF_2 extensions further results in higher ON-state and lower OFF-state ("reduced doping": LDD implant and 1050°C spike anneal – "high doping": LDD implant and spike anneal followed by spacers definition, HDD implant and a second spike anneal). Furthermore, C-V curves and extracted effective mobility on long-channel SG pMOSFETs (split CV method) show no transport degradation due to the process (1.4nm EOT, no observable D_{it} peak at low frequency, good mobility for a PVD TiN/HfO_2 gate stack).

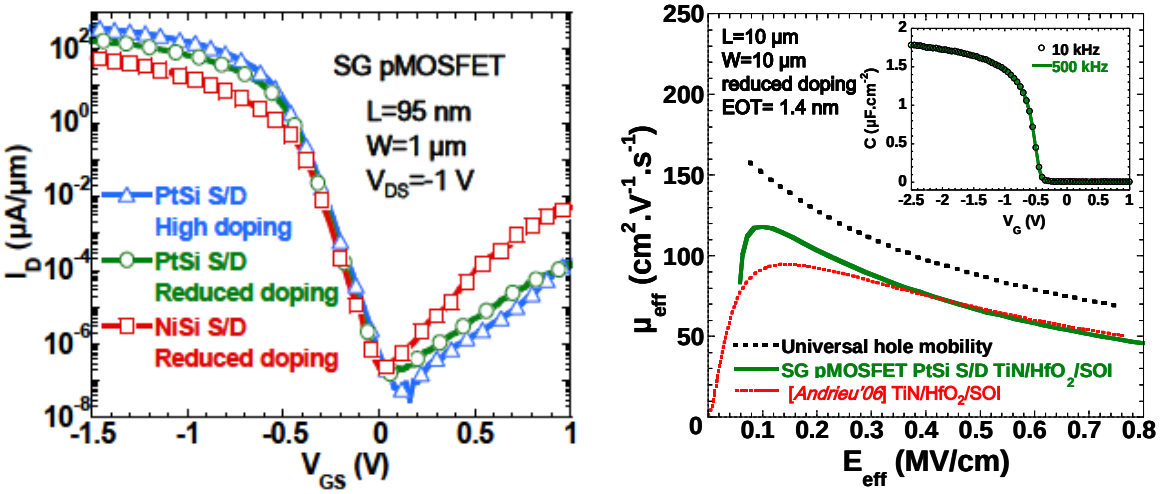

Figure III-21: Left: Drain current vs. Gate to Source voltage (I_D-V_{GS}) characteristics of SG pMOSFETs showing the sensitivity to both S/D metallization (Pt or Ni) and doping conditions at the Metal/Si interface ("high" or "reduced" dose and thermal budget). Right: Effective mobility μ_{eff} in the channel versus transverse effective field E_{eff} extracted on a SG pMOSFET (split C-V method). Gate capacitance vs. Gate voltage curves are shown in the inset (measured at 10kHz and 500kHz).

The study of short channel effects (Figure III-22) shows that in spite of better I_{ON}/I_{OFF} ratios, SG pMOSFETs with high dose and thermal budget doping conditions present degraded SCE due to electrical gate length reduction, hence a trade-off between performance optimization and scalability. The diffusion of dopants in the channel can be optimized by dopant segregation techniques (reviewed later in paragraph III.3.3.). However, we have seen earlier (paragraph III.2.1.d.) that excessively steep interfacial doping profiles could prove counterproductive in terms of performance, as they might result in "atrophied" potential wells (Source side, favoring injection current) or bumps (Drain side, impeding leakage current). The lateral extent of S/D extensions should be carefully optimized [*Vega'08*].

Another solution lies in improving the electrostatic integrity of the device through UTBOX or Double Gate geometry, which display a regain of SCE control. The I_D-V_{GS} curves of DG pFETs with PtSi S/D are also shown for L_G down to 20nm on Figure III-22.

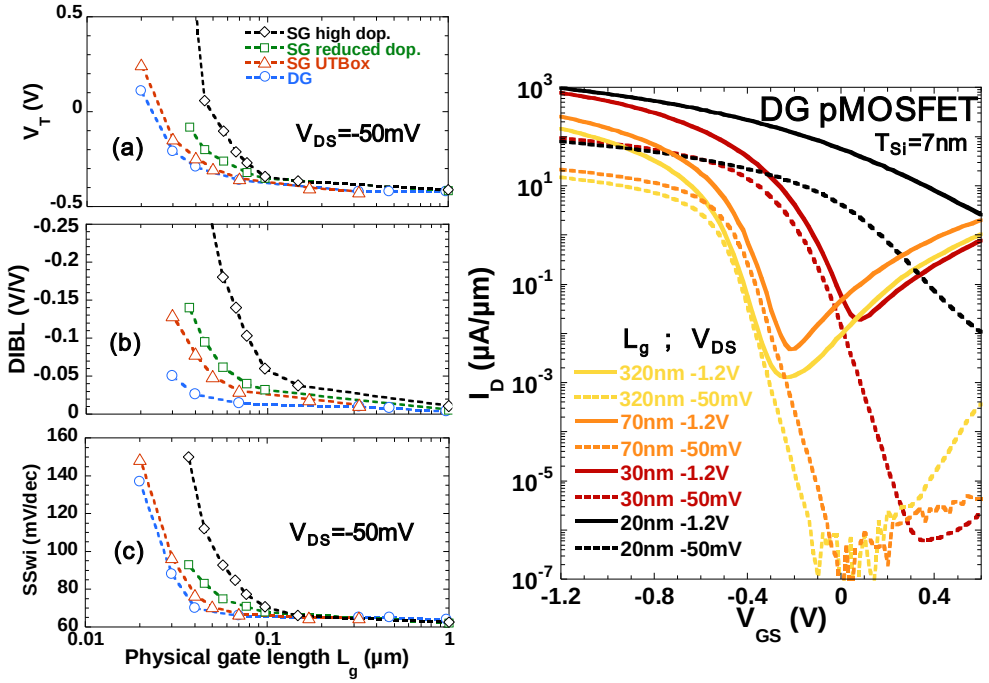

Figure III-22: Left: ***(a)*** *Threshold voltage,* ***(b)*** *DIBL and* ***(c)*** *Subthreshold swing as a function of L_g on the different fabricated structures (all pMOSFET with PtSi S/D) Right: I_D-V_{GS} characteristics of DG pMOSFETs (PtSi S/D) for various L_g and V_{DS}. Currents are normalized by top view W.*

Eventually, although a performance comparison between devices with different equivalent oxide thicknesses and in different bias conditions is not straightforward, our realizations of Schottky pFETs with PtSi S/D and interfacial doping in a damascene integration scheme exhibit state-of-the-art I_{ON}-I_{OFF} trade-offs (Figure III-23) in addition to well-controled Short Channel Effects for Double Gate devices.

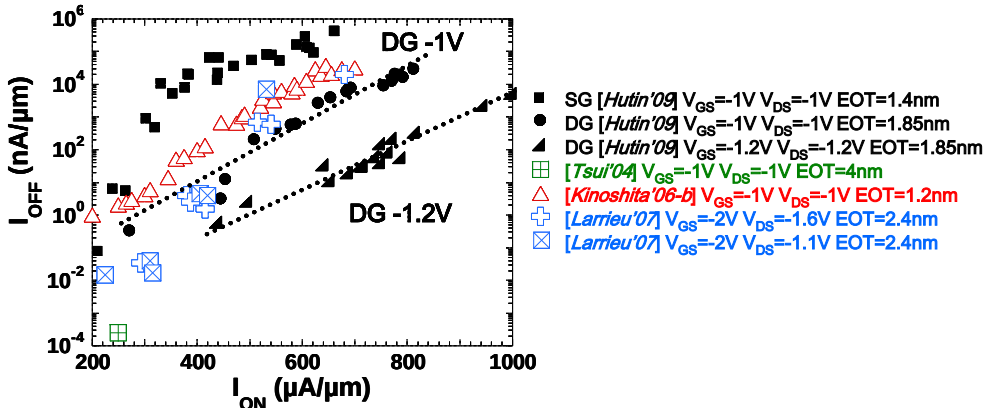

Figure III-23: I_{OFF}-I_{ON} benchmark of Schottky pMOSFETs with Dopant Segregated Source and Drain and unstrained Si channel (I_{OFF} measured at V_{GS}=0V).

III.3.2. **Self-Aligned silicidation followed by selective etching**

The previously described damascene approach is particularly adapted for implementing metallic S/D within the vertical Double Gate transistors process described in [*Vinet'09*] and Figure III-18. Nevertheless, the definition of cavities adds process complexity which can be avoided for planar Single Gate devices. In this case, a more "mainstream" approach for self-aligned S/D silicidation (first proposed for conventional submicronic MOSFETs in [*Shibata'81*]) adapted to Schottky MOSFETs consists in three steps (Figure III-24):

1. Metal deposition
2. Silicidation annealing
3. Selective removal of the unreacted metal

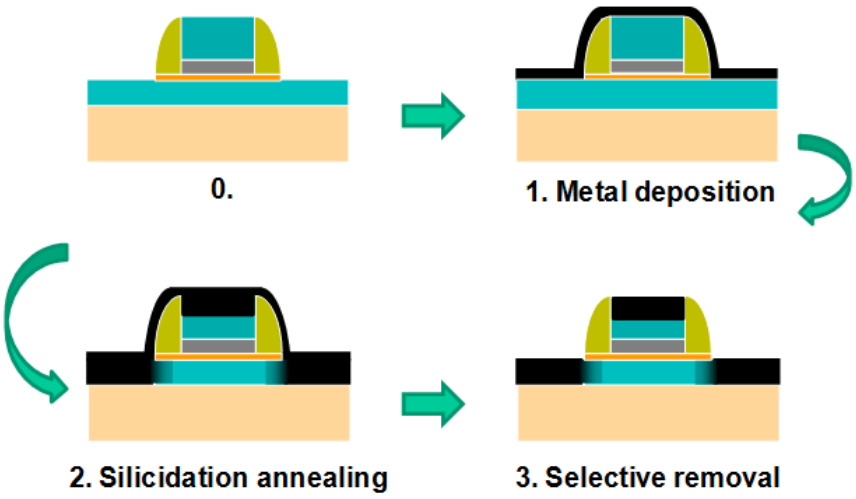

Figure III-24: Schematic process flow of a self-aligned S/D silicidation followed by selective removal of the unreacted metal on SOI.

The third step aims at isolating the Source, Gate and Drain and should be selective with respect to the silicide formed in step 2. We have seen in the previous chapter that Platinum was a choice candidate for achieving an efficient carrier injection in Schottky-Barrier pFETs. However, due to its noble metal properties, Pt is difficult to etch and known to be exclusively soluble in aqua regia solutions ($HCl/HNO_3/H_2O$). Although extensively investigated for various dilution and temperature conditions [*Zhang'06*], aqua regia etching presents some drawbacks. First, the volatility of the byproducts created during the reaction between concentrated HCl and concentrated HNO_3 results in a loss of potency of the solution over time [*Breil'09*]. Second, a superficial oxidation of the PtSi silicide is required to achieve selectivity with respect to Pt [*Rand'74*], [*Van Dal'06*]. As the oxidization reaction consumes Si, this process is not suitable for transistor fabrication on thin SOI substrates [*Dubois'08*]. Thus, the transformation of the chemically stable Pt layer into a more reactive phase of Pt_xGe_y was proposed [*Breil'07*], [*Breil'08*] as an alternative solution to aqua regia etching. The

process consists in depositing a layer of Germanium on top of the Platinum, followed by a germanidation annealing (300°C < T < 600°C), and etching of the PtGe in a Sulfuric Peroxide Mixture (SPM). It was shown that the barrier height at the PtSi/Si interface was not affected by this process.

It should be noted that the implementation of NiSi silicides instead of PtSi, in addition to be less expensive to process, would also provide an easier technological solution due to the high etch selectivity between NiSi and unreacted Ni [*Vega'10*]. However, the workfunction of this silicide is closer to midgap (Φ_{bp0}≈0.5eV), which makes it a good candidate for a single-S/D-metal integration scheme, but requires more efforts in interfacial doping techniques to achieve the same performance as PtSi-based Schottky pFETs.

III.3.3. **Dopant segregation techniques**

The necessity of reducing the intrinsically ambipolar behavior of Schottky MOSFETs through a highly doped interfacial layer in order to reach better I_{ON}/I_{OFF} ratios has been highlighted in previous sections. So as not to jeopardize one of the most important advantages of Schottky MOSFETs, *ie* scalability, the doping profile has to remain particularly abrupt, especially for a planar Single Gate device geometry.

III.3.3.a. Principle

The dopant segregation techniques consist in taking advantage of the dopants pile-up at the metal/Si interface (first described in [*Thornton'81*]) to limit the thermal budget of the activation annealing, and therefore their diffusion into the channel.
If we refer to Figure III-24, the dopant implantation can occur either:

- between steps 0 and 1: Implantation before silicidation (IBS) [*Swirhun'85*], [*Kinoshita'04*], [*Kinoshita'05*], [*Kinoshita'06-a&b*], [*Kaneko'06*], [*Huang'08*], [*Qiu'08*], [*Urban'09*], [*Larrieu'09*], [*Urban'10*]
- between steps 1 and 2: Implantation through metal (ITM) [*Horiuchi'86*], [*Nagasawa'87*], [*Tsui'91*], [*Dubois'08*]
- between steps 2 and 3: Implantation through silicide (ITS) followed by a drive-in anneal to bring the dopants towards the silicide interface [*Tsui'91*], [*Chen'92*], [*Chen'96-b*], [*Dubois'08*], [*Zhang'08*], [*Qiu'08*], [*Larrieu'09*], [*Khater'10*], [*Vega'10-a&b*], [*Zhang'10*]

A disadvantage of the IBS technique is that the thermal budget of the silicidation annealing is typically insufficient to heal the implant-induced damages within the Si film. In

the case of ITM and ITS, dopants are confined within the silicide or metal layer without generation of defects [*Dubois'08*].

While the silicidation process occurs through a re-arrangement of bonds between Si and the metal, the impurities are pushed towards the silicide/Si interface ("snow-plough" effect) due to their relatively low solid solubility in the silicide. The low silicidation temperatures (~450°C-600°C) are such that little diffusion of the dopants occurs in Si. This crowding of impurities in the vicinity of the interface eventually results in the incorporation of most of them into substitutional sites, therefore yielding a very high electrical activation within a narrow region.

This interpretation is consistent with an improved injection through enhanced tunneling across the Schottky Barrier. However, it is also speculated that this favorable change in electrical characteristics might be due to the formation of metal-dopant or silicide-dopant clusters (as observed in [*Maex'89*]) modifying the workfunction of the metal.

The ITS approach seems to be the most efficient, with Boron atoms sharply segregating at a PtSi/Si interface with a peak concentration of 2×10^{20} at.cm^{-3} after a drive-in anneal in N_2 at 500°C during 5min [*Dubois'08*], yielding a SBH lower than 0.082eV. Similarly, record contact resistivity values (ρ_c = 6~7×10^{-9} Ω.cm^2) have been achieved on both n^+ and p^+ dopant-segregated NiPtSi/Si contacts (drive-in anneal at 550°C, 30s) [*Zhang'10*], ultimately resulting in state-of-the-art Schottky CMOS performance [*Khater'10*] (nFETs: I_{ON}=734 µA/µm @ L_G=30nm – pFETs: I_{ON}=532 µA/µm @ L_G=30nm).

ITM has proven so far to be a less efficient technique (Φ_{bp}=0.13eV in [*Dubois'08*]), likely due to a loss of dopant dose during the silicidation reaction, which is believed to push the impurities towards the top surface.

III.3.3.b. Silicide thermal stability and ITS dopant segregation

It was shown in [*Qiu'08*] that dopant-segregated junctions formed by ITS present sharper profiles at PtSi/Si interfaces than at NiSi/Si interfaces. The role of excess vacancies and point defects appearing during silicide formation as an additional cause of dopant diffusion had been previously highlighted [*Wittmer'84*], [*Chen'92*]. It was therefore speculated that this is due to the difference in thermal stability of PtSi versus NiSi [*Kittl'08*]. In fact, Ni atoms tend to be rejected from the silicide and diffuse within the silicon when NiSi is annealed over extended periods of time at sub-agglomeration temperatures [*Tsuchiaki'04*]. In the hypothesis that the metal atoms diffuse interstitially, their large size would generate a sufficient amount of stress to break Si-Si bonds and give rise to vacancies, thus enhancing dopant diffusion, especially if these metal atoms form clusters. Recent experimental data in [*Vega'10-a*] tend to confirm these considerations.

To increase the silicide thermal stability while conserving the process integration and low cost advantages of NiSi, NiPt silicides with a low Pt content have been recently investigated [*Huang'08*], [*Marukame'08*], [*Sonehara'08*], [*Zhang'10*], [*Khater'10*]. However, this approach is limited by the fact that NiPtSi is constituted of NiSi and PtSi grains. On FDSOI devices and FinFETs where the channel thickness or width might be close to the average grain size in the silicide, the abruptness of the dopant-segregated junction ultimately boils down to whether a NiSi or a PtSi grain is adjacent to the channel, and a new source of variability arises.

Alternately, Fluorine or Nitrogen post-silicide ionic implantations (F-PSII and N-PSII) have been reported to increase NiSi thermal stability by effectively controlling Ni diffusion [*Tsuchiaki'05*], [*Tsuchiaki'08*], [*Imbert'08*], [*Loh'09*], [*Batude'09-a*], [*Vega'10-a*]. N-PSII tends to promote the formation of a $NiSi_2$ phase [*Loh'09*], whereas F-PSII leaves the silicide unchanged. Successful tuning of the dopant-segregation junction depth by F-PSII has been demonstrated in [*Vega'10-a*] on NiSi silicides, through the limitation of the Ni atoms rejection process.

III.3.4. **Metallic S/D for nFETs**

As metal/Si contacts are *a priori* (cf. Fermi-level pinning, previous Chapter) favorable to hole injection, the overwhelming majority of studies in the literature report on pFET fabrication. In an effort to develop Schottky CMOS, two approaches compete for fabricating nFETs with metallic Source and Drain.

The first one consists in integrating rare earth (conduction) band-edge silicides with low intrinsic Schottky barriers for electrons Φ_{bn0}. This is a Dual S/D Metal approach, as the silicides for pFET and nFET fabrication are considered separately. The second approach proposes a simpler process, using a single metal (preferably close to midgap) and relying on the effective barrier lowering by dopant segregation (n-type for nFETs, p-type for pFETs).

III.3.4.a. Dual S/D Metal for Schottky CMOS

As rare earth elements are known to provide the lowest Schottky Barriers for electrons (due to Fermi-level pinning relatively close to the conduction band), it appears natural to try and integrate silicides such as ErSi or YbSi for high-performance Schottky nFETs. However, as the associated intrinsic barrier heights are of the order of 0.28eV [*Dubois'08*], further barrier modulation through *e.g.* interfacial doping seems inevitable. Moreover, these materials present in practice several serious drawbacks such as the formation of pinholes and pyramidal defects [*Tsai'04*], [*Tan'06*], [*Breil'09*] (degrading the sheet resistance and possibly the contact resistance with upper metal layers), their high reactivity with the oxygen (present in spacers,

isolation oxide or buried oxide), and their bad thermal stability (significant Si out-diffusion can be observed above 500°C [*Breil'09*]).

These constraints impose a low thermal budget and, on SOI, a partial etch of the Si film prior to metal deposition is preferable. Functional nFETs with As-doped extensions, ErSi and YbSi S/D were demonstrated down to L_g=45nm in [*Hutin'09*] using the damascene S/D process described in paragraph III.3.1. The TEM pictures Figure III-25 show that the resulting structure is not optimized (thick spacers and gate dielectric, no penetration of the silicide below the spacers), but the corresponding Oxygen elemental mapping obtained by Electron Energy Loss Spectroscopy (EELS) shows no undesirable oxidation of the silicide at the YbSi/Si interface.

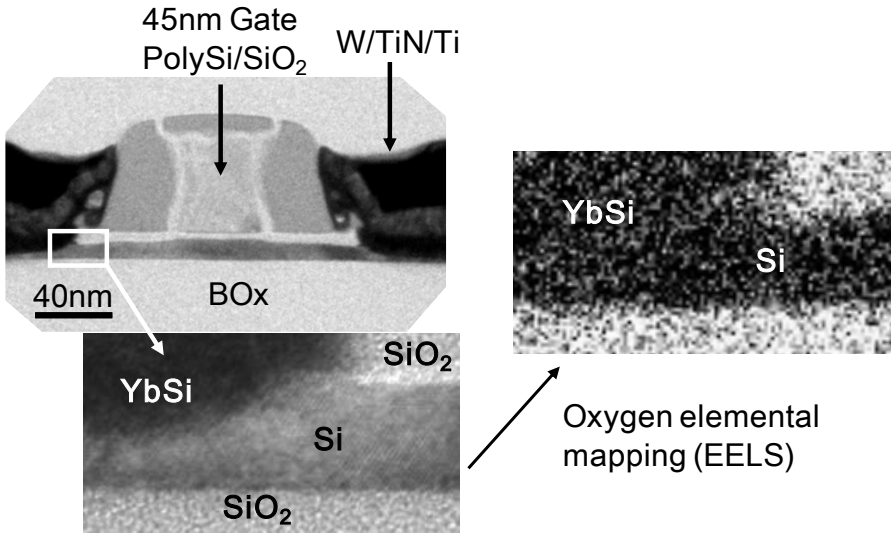

Figure III-25: X-TEM micrograph of a 45nm long Single Gate nMOSFET with YbSi S/D and (IBS) dopant segregated Source and Drain, with zoom on the Channel/Source interface, and corresponding EELS Oxygen elemental mapping. (pictures: D. Lafond)

The I_D-V_{GS} characteristics (Figure III-26) show a similar behavior between ErSi and YbSi S/D, and clearly different features for the NiSi S/D devices. The latter seem to express an ambipolar Schottky operation, with a mediocre injection of electrons and relatively high injection of holes in OFF-State. It is tempting to conclude that ErSi and YbSi S/D devices display much more "nFET-like" curves owing to a lower Φ_{bn}, and higher Φ_{bp}. However, the distance between the edge of the rare earth silicides and the gate edge seems too large for the injection to be primarily controlled by the silicide/Si junction (as opposed to the n^+/p junction between extensions and channel).

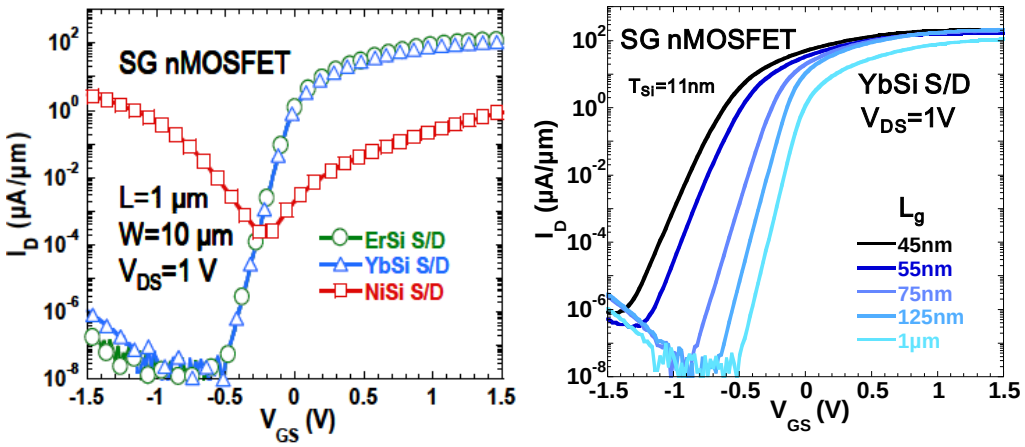

Figure III-26: Left: I_D-V_{GS} characteristics of SG nFETs with various S/D metallizations (Er, Yb and Ni). YbSi and ErSi S/D devices show extremely reduced leakage current as low as 10 fA/µm at V_{DS}=1V. Negative V_T are attributed to the Poly-Si gate - Right: I_D-V_{GS} characteristics of YbSi S/D SG nMOSFETs at high V_{DS} for various gate lengths down to 45nm.

As explained in III.2.1.c. , the analysis of the I_D-V_{DS} curves under "pFET bias" and "nFET bias" enables to observe (or not) the characteristic ambipolar behavior of Schottky MOSFETs (Figure III-27).

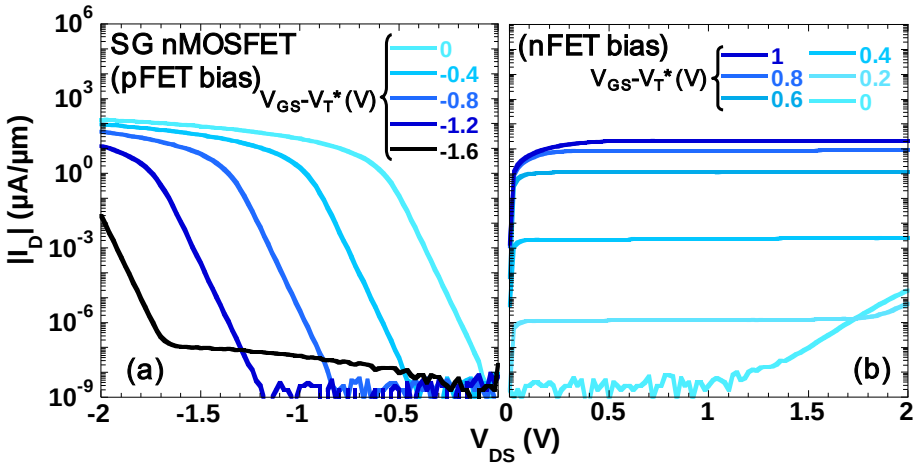

Figure III-27: Measured I_D-V_{DS} characteristics of a Single-Gate MOSFET with YbSi S/D and Arsenic extensions (L_g=1µm) under (a) pFET bias: V_{GS}<0; V_{DS}<0 and (b) nFET bias: V_{GS}>0; V_{DS}>0. V_T^* is the threshold voltage in saturation regime.

Plateaus apparently similar to those on Figure III-8 are visible. However, they appear for $|V_{GS}-V_T^*| > E_g^{Si}/q$ on Figure III-27 a), and for $V_{DS} > E_g^{Si}/q$ on Figure III-27 b). In short, they are not a manifestation of ambipolar conduction, but due to direct band-to-band tunneling of electrons, respectively at the Source and at the Drain, as schematically explained on Figure III-28.

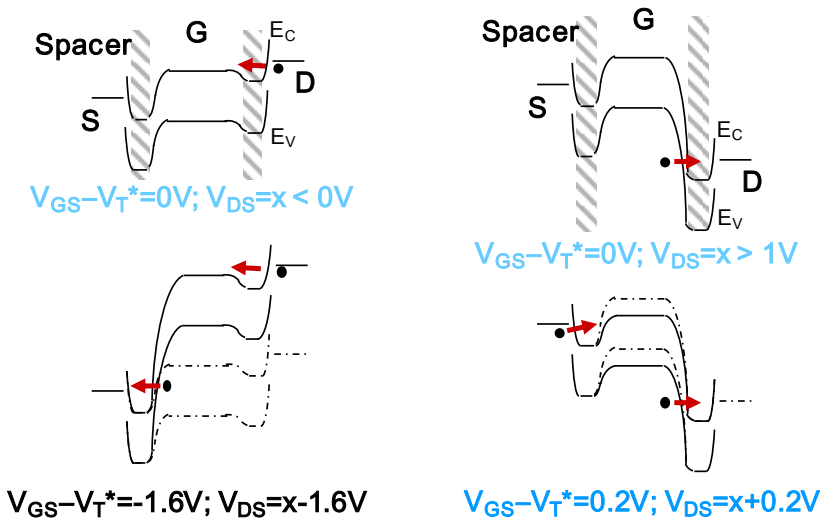

Figure III-28: Schematic cross-sectional band diagrams in the channel direction under pFET bias (left) and nFET bias (right) for qualitative analysis of the current plateaus Figure III-27.

Whereas it is probable that the nickel silicide did diffuse sufficiently under the spacers (as suggested by the strongly ambipolar I_D-V_{GS} Figure III-26), the distance between the YbSi/Si contact and the channel is indeed too large for the ON- and OFF-state to be determined by anything else than the n^+/p junctions. Compared to conventional nFETs of equivalent gate lengths, the ON-state current is very low, ironically due to high series resistance (cf. large spacers, limited silicide diffusion, possibly mediocre interface with the W/TiN/Ti stack etc.). Yet, surprisingly, the performance of these nFETs compares very well with other exotic metal S/D nFETs with n-type extensions presented in the literature (Figure III-29).

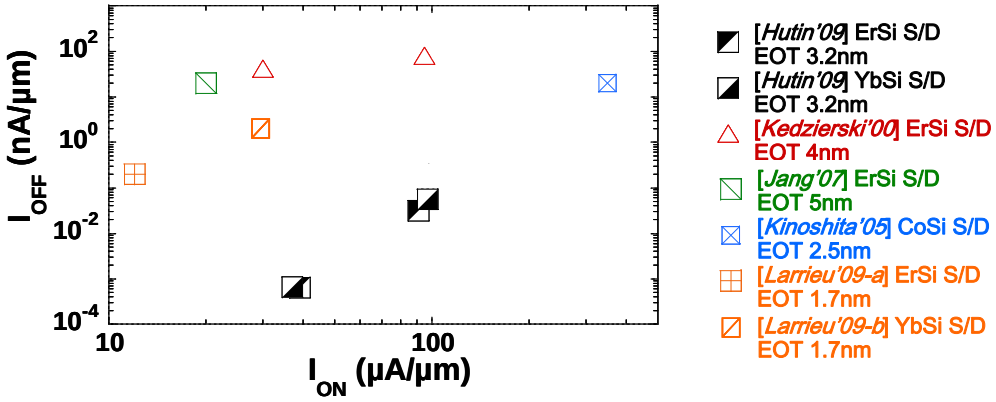

Figure III-29: I_{OFF}-I_{ON} benchmark of unstrained channel SG nFETs with metal S/D. I_{ON} was extracted at V_{DS}=1V and $V_{GS}=V_T + 2V_{DS}/3$; and I_{OFF} at $V_{GS}=V_T - V_{DS}/3$ [Chau'05]; $I_D(V_T)=10^{-7}\times W/L_g$ (A/µm).

The competitiveness of a Dual S/D metal approach is still far from obvious. In addition to increasing the process complexity, the performances of nFETs with rare earth silicide S/D are hardly convincing. Other easier to process, cheaper materials (Pt, Ni, Co…)

are available with relatively higher intrinsic Schottky barriers Φ_{bn}, which could nevertheless be compensated for by implementing a strongly efficient interfacial n-type doping.

III.3.4.b. Single S/D Metal for Schottky CMOS

Since the integration of conduction band-edge silicides proves complicated and not so rewarding, efforts have been made lately to optimize n-type dopant segregation on silicides *a priori* more favorable to holes injection: PtSi+IBS [*Dubois'08*]; F-PSII+NiSi+ITS [*Vega'10-a&b*]; NiPtSi+ITS [*Zhang'10*], [*Khater'10*]. This also enables to consider a single silicidation step for both nFETs and pFETs and considerably simplifies CMOS fabrication.
The SBH for electrons are indeed reported to be drastically reduced by As segregation: 0.15eV [Dubois'08] (extraction on Arrhenius plots), 0.12eV [*Vega'10-b*] (Φ_{bp} extraction from C-V measurements, Φ_{bn} deduced by complementarity), and even 0.06eV [*Zhang'10*] (same method as the latter).

In particular, Single-silicide, NiPtSi S/D CMOS has been most recently demonstrated on 10nm thick SOI in [*Khater'10*] using B segregation for pFETs and As segregation for nFETs down to L_g=20nm. The threshold voltages are fairly symmetrical, and so are the On-State currents at $|V_{GS}|$=1V: 560µA/µm for nFETs and 490µA/µm for pFETs at L_g=30nm. In spite of perfectible SCE control (DIBL ~150mV/V at L_g=30nm, which is relatively high for this film thickness and a supposedly limited diffusion of dopants), these results are the most advanced to date in the perspective of Single S/D Metal integration for Schottky CMOS.

III.4. Conclusion

Replacing doped junctions by metal/semiconductor junctions in the Source and Drain of MOSFETs was originally considered for various reasons evoked at the beginning of this chapter. When it comes to device integration on Silicon On Insulator for CMOS logic applications, the only relevant advantages are basically low temperature processing and series resistance reduction.

Concerning the latter, the conclusion is not as obvious as it might first seem. By bringing the metal/semiconductor contact at the entrance of the channel, in an *a priori* undoped region, the whole advantage of using a layer with lesser sheet resistivity in the S/D areas could be overshadowed due to a tenfold increase (or more) of the contact resistivity component. As a rule of thumb, the contact resistivity should be kept below a maximum of 10^{-8} Ω.cm^2, which cannot occur naturally in metal-to-undoped Si contacts.

Should interfacial doping be the solution (through narrowing the Schottky Barrier and increasing tunneling current), then such ρ_c values have been experimentally linked to

interfacial dopant concentrations of at least a few 10^{20} at.cm^{-3}. Therefore, to remain a credible in terms of series resistance reduction, a Schottky-Barrier MOSFET should feature highly-doped extensions with the same activation level as in conventional doped S/D MOSFETs.
Furthermore, a first-order analysis of the operation of a Schottky-Barrier MOSFET shows that for the usual range of biasing conditions (V_{dd}~1V), interfacial doping is required not only to improve carrier injection in the On-State, but also to limit leakage current in the Off-State. It can be also necessary to avoid a degradation of the subthreshold swing which would typically occur otherwise in underlapped geometries.

According to these points, the picture of a "good" Schottky MOSFET on SOI strongly resembles that of a conventional MOSFET on SOI with silicided access regions. And ultimately, their performance should be very close as the main structural difference lies in the thickness of the metal layer.

The true specificity of Dopant-Segregated Source and Drain (DSS) Schottky MOSFETs is the dopants activation mechanism, occurring at low temperature. In addition to being an advantage in itself, it could provide the opportunity to reduce dopants diffusion in the channel and therefore improve the Short Channel Effects. However, this potential improvement over RTP-activated junctions has not been demonstrated yet. Furthermore, extremely abrupt lateral doping profiles might degrade the injection at the metal/semiconductor interface.

The development of the fully-metallic Source and Drain technological modules does not look like an absolute necessity for improving the performance and scalability of planar, symmetrical single gate devices on FDSOI. Yet, it can be of prime importance in the elaboration of different architectures, such as the vertical Double Gate transistor presented in III.3.1.b.

Moreover, the constraints arising from SBH modulation through interfacial doping, and in particular the activation level needed, could be alleviated on lower-bandgap semiconductors such as Germanium or Silicon-Germanium alloys. This is nevertheless a whole different world which will be treated in the next chapter.

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Chapter IV. Ge-based substrates and devices

In this chapter, after a brief historical review of the rise, fall and rebirth of Ge-based transistors, we will introduce the basic electrical properties of "Sister Germanium" compared to "Brother Silicon" (as formulated in [*Vanhellemont'07*]). We will then present the different ways to prepare Ge-based substrates for device fabrication, after which the newly re-activated subject of Ge and GeOI CMOS will be treated in details. As some questions will be raised on the sustainability of pure Ge technology for advanced nodes, the somewhat "intermediate" SiGe approach will be evaluated. Finally, as it represents the point of convergence of all of the chapters, the state-of-the-art of Schottky Ge MOSFETs will be introduced, and compared with the results obtained in the frame of this thesis.

IV.1. Introduction

IV.1.1. Early history of (Ge) electronics

IV.1.1.a. The first transistors

Shortly after the Second World War, AT&T's research and development arm, Bell Labs, formed a Solid State Physics group led by William Shockley with the purpose of finding an alternative to glass vacuum tube amplifiers for telecommunication relays. Vacuum tubes were bulky, unreliable and consumed too much power. The principle of the point-contact transistor was developed, and Shockley had been working on the theory of such a device without succeeding in building a working model. His first prototype of a semiconductor amplifier consisted in a small cylinder coated thinly with silicon, mounted close to a small metal plate (field-effect transistor). Following John Bardeen's observations that surface states were largely responsible for the failed experiments, the initial prototype was altered by adding a point contact (Figure IV-1) between the metal and the semiconductor, itself surrounded by an electrolyte solution (provoking charge migration at the surface of the semiconductor, therefore enhancing the operation). Yet, the observed amplifications remained very weak.

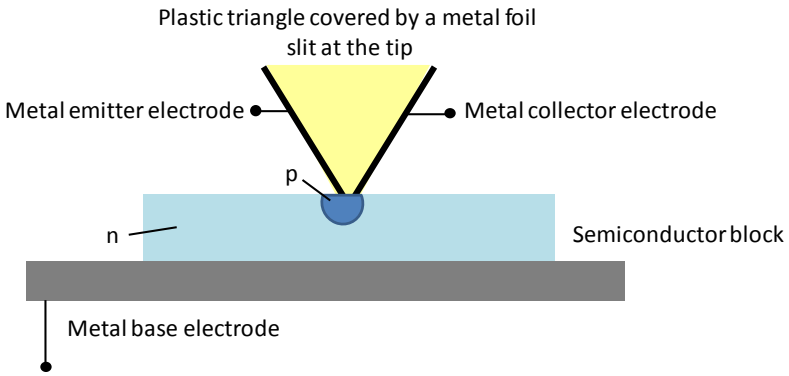


Figure IV-1: Schematic sketch of an early point-contact transistor. A small positive bias on the emitter results in holes injection at the semiconductor surface, therefore creating a p-type surface layer, and a p-n junction between base and collector. A small change of current across the first contact (emitter) results in a greater change of current across the second (collector), hence the amplification effect.

Replacing Silicon with Germanium, the amplification was increased by about 300 times. This is how on December 23, 1947, Bardeen and Brattain – working without Shockley – created the first operating transistor amplifier (Figure IV-2), made of Germanium [*Bardeen'48-a&b*].

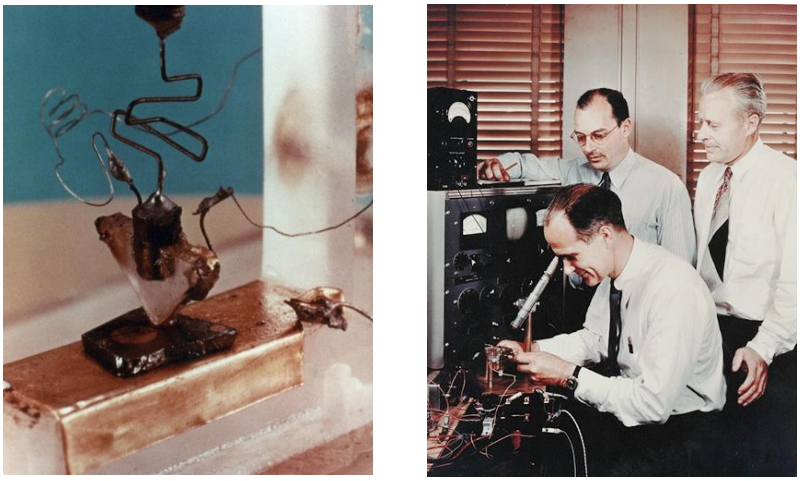


Figure IV-2: (left) the first Germanium point-contact transistor amplifier demonstrated in December 1947 by (right) John Bardeen and Walter Brattain with support from William Shockley from Bell Labs.

We can note at this point that the Fermi-level pinning close to the valence band at the Ge surface (described in Chapter II, and evoked later in section IV.3.2.b.) played a decisive role in the history of transistors. Indeed, it both results in an easily achievable p-type inversion, as well as a facilitated injection of holes from metal to Germanium.

Yet, Shockley was annoyed to have been left out of the discovery. As he considered that the person who had the original idea was the sole inventor and should be the only name on the transistor patent, he filed a patent on his own (without Bardeen or Brattain) based on his concept of field-effect amplifier. However, Bell Labs' attorneys soon discovered that the field-effect principle had been anticipated and patented in 1930 (patent first filed in Canada in 1925) by Julius Lilienfeld [*Lilienfeld'25*]. Thus, the ideas of Shockley were dismissed, and Bell decided to file solely on Bardeen and Brattain's point-contact structure [*Bardeen'48-b*], which was undeniably different.

Besides the struggle for recognition, Shockley was also dissatisfied with the design of the point-contact resistor (which he judged fragile and difficult to manufacture). He worked on the description of what he called then the "sandwich" transistor (consisting of an n/p/n or a p/n/p Germanium sandwich), with a first proof-of-concept demonstration on April 7, 1949. This resulted in his invention of the junction transistor, presented two years later [*Shockley'51*], which quickly supplanted the early point-contact transistor of Bardeen and Brattain. Five years later in 1956, Shockley, Bardeen and Brattain would share the Nobel Prize in Physics as the co-inventors of the transistor.

The first transistorized consumer product in the US was a hearing aid in 1952: the Sonotone 1010 (Figure IV-3). It featured two vacuum tubes and one npn junction transistor made by Germanium Products Corporation. The first all-transistor hearing aid was introduced in 1953 by the Maico Company and by 1954, 97% of all hearing aids used only Ge transistors.

The first commercialized transistor radio was the Regency TR-1 in 1954, including 4 Germanium transistors supplied by Texas Instruments. In August 1955, Sony began to sell its TR-55, containing 5 Ge transistors placed on a printed circuit board.

1952
Sonotone 1010
1 Ge transistor

1954
I.D.E.A. Regency
4 Ge transistors

1955
Sony TR-55
5 Ge transistors

Figure IV-3: The first marketed transistorized products in the early 1950's contained Germanium transistors.

IV.1.1.b. The first integrated circuits and the reign of Silicon

In 1958, Jack Kilby, an engineer at Texas Instruments, was working on the resolution of the circuit design problem called the "tyranny of numbers". This problem emerged at the time from the multiplication of interconnected discrete components soldered by hand on printed circuit boards (PCB), which were themselves wired to other PCB modules, thus generating major reliability problems.

Kilby theorized that all common electronic components (transistors, resistors, capacitors, etc.) could be co-integrated on a single Germanium block. The same year, in September, he demonstrated for the first time an operating integrated circuit, on monolithic Ge. He subsequently filed a patent on February 6, 1959 [*Kilby'59*] (Figure IV-4). This patent would only be issued in 1964.

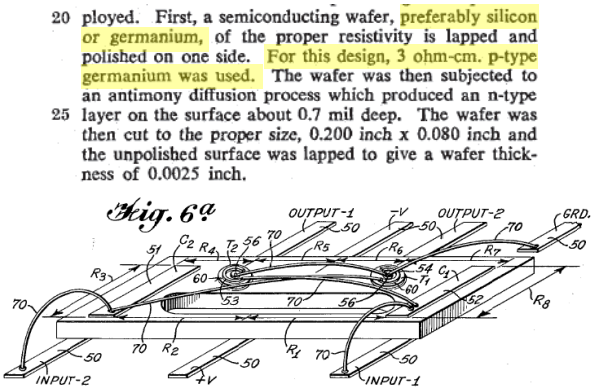

ployed. First, a semiconducting wafer, preferably silicon or germanium, of the proper resistivity is lapped and polished on one side. For this design, 3 ohm-cm. p-type germanium was used. The wafer was then subjected to an antimony diffusion process which produced an n-type layer on the surface about 0.7 mil deep. The wafer was then cut to the proper size, 0.200 inch x 0.080 inch and the unpolished surface was lapped to give a wafer thickness of 0.0025 inch.

Fig. 6a

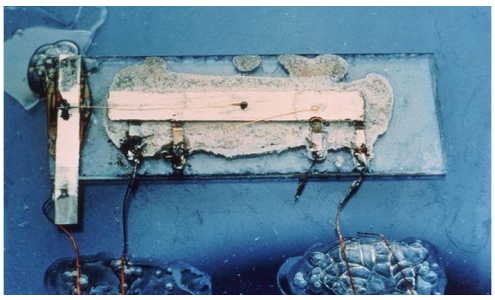
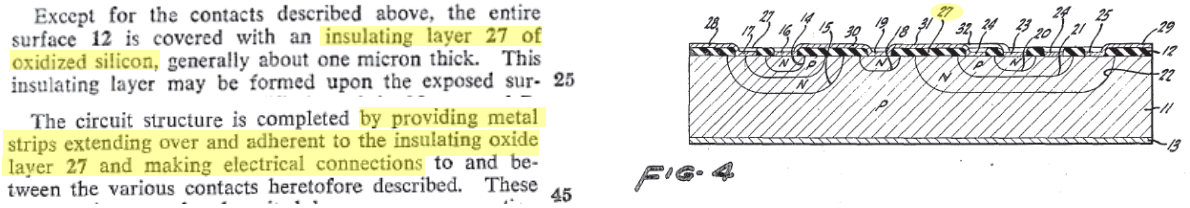


Figure IV-4: (left) Excerpt of the patent [Kilby'59] describing the first functional IC (right), on Germanium.

We can note on Figure IV-4 that the components were then connected by soldered wires, as Kilby could not solve the problem of co-integrating and isolating leads with the same process. This is precisely the point on which Robert Noyce's design, from Fairchild Semiconductor, was superior. Fairchild Semiconductor is a company co-founded in 1957 by the so-called "Traitorous Eight" who had left the Shockley Semiconductor Laboratory. Among them, Robert Noyce and Gordon Moore would later found Intel. In June 1959 (only a couple of months after Kilby), Noyce filed a patent entitled "Semiconductor Device-and-Lead Structure" [*Noyce'59*], which was issued in 1961. His structure was Silicon-based, proposed connections by thin-film metal strips separated from the active semiconductor areas by an insulating oxide (Figure IV-5).



Except for the contacts described above, the entire surface 12 is covered with an insulating layer 27 of oxidized silicon, generally about one micron thick. This insulating layer may be formed upon the exposed sur-

The circuit structure is completed by providing metal strips extending over and adherent to the insulating oxide layer 27 and making electrical connections to and between the various contacts heretofore described. These

FIG. 4

Figure IV-5: Excerpts of the patent [Noyce'59] describing a monolithic "device and lead" Silicon integrated circuit.

Such an approach would have been much more complicated on Germanium, as Germanium oxides are known to be unstable, non-stoichiometric and water soluble. By contrast, Si offers the possibility of simply obtaining chemically stable, thermally grown SiO_2. Moreover, SiO_2 is a good insulator (*ie* ideal for monolithic circuits processing), and has a good interface with Si (*ie* ideal as gate dielectric in MOSFETs). In addition to the popularity of this design, the following points disfavored Ge:

- The early point-contact MESFET architecture did not work well on Si, but it was no longer a problem for bipolar junction transistors and MOSFETs (invented in 1959 by Kahng and Atalla from Bell Labs, patent filed the next year [*Kahng'60*]).
- Germanium represents roughly 0.00015% of the lithosphere (against 20.4% for Silicon) and is difficult to extract (essentially present in small concentrations in Zn or Zn-Cu minerals). As a consequence, Ge is much more expensive than Si.

These are some of the reasons why no one has ever heard of the « Germanium Valley ». From the mid-1960's and for roughly 40 years, Silicon would overwhelmingly dominate the microelectronics industry. In the meantime, applied research on Germanium devices for digital and analog circuits would become very scarce, if not invisible.

IV.1.1.c. "Back to the future"?

Ge being a high-mobility semiconductor, it was unlikely to be completely forgotten, due to an increasing need for high-speed logic. Germanium MOS technology also remained of interest for the construction of monolithic high-speed fiber-optic receivers (*ie* Ge photodiodes integrated with Ge amplifiers and signal processing circuitry operating at 1.3-1.5µm wavelengths).

The primary challenge was to develop a gate dielectric with a low interface state density on Ge [*Wang'75*]. In 1983, Rosenberg demonstrated Ge nFETs with a thermally grown Germanium nitride (Ge_3N_4) gate dielectric and $D_{it} < 2\times10^{11}$ cm^{-2} [*Rosenberg'83*]. A few years later, the process had evolved into the nitridation of native GeO_2 on 6µm-long nFETs with an estimated channel mobility of 940 $cm^2.V^{-1}.s^{-1}$ [*Rosenberg'88*]. Ge pFETs followed, with a channel mobility observed for the first time at larger values than in Si (~1050 $cm^2.V^{-1}.s^{-1}$ [*Martin'89*], ~2000 $cm^2.V^{-1}.s^{-1}$ at L_g=0.6µm [*Ransom'91*]).

While techniques were developed to obtain Ge-rich substrates (virtual substrates [*Currie'98*], Ge enrichment [*Tezuka'01*]), a regain of interest for Ge devices sparkled worldwide in the early 2000's (Hannover [*Reinking'99*], MIT [*Lee'01*], IBM [*Shang'02*], Stanford [*Chui'02-a*], Taiwan [*Huang'03*], Tokyo-MIRAI [*Tezuka'04*], [*Maeda'04*], IMEC [*De Jaeger'04*], Leti [*Clavelier'05*], [*Le Royer'05*], [*Weber'05*] etc.).

This trend was consolidated in the next half-decade by the shifting of Si technologies towards the implementation of high-k gate dielectrics (as a key for lower gate leakage with same gate capacitance) to improve power consumption and reliability of decananometric devices. The main reason why Ge had been set apart in the early 1960's was then no longer valid, and it was argued that the past of microelectronics could become its future again.

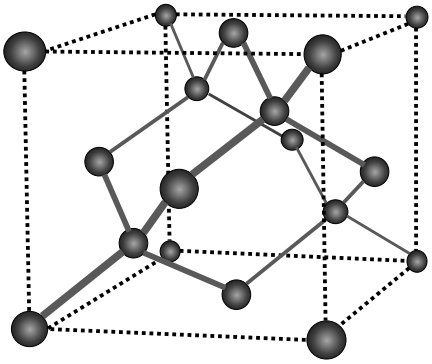
IV.1.2. **Carriers transport in Ge**

Even though Silicon is losing its SiO_2 advantage, Germanium remains rare, expensive, and its technology has to be adapted to the preexisting Si processing lines. Yet, in the context of the end of the "happy scaling era", with the investigation of new materials and device architectures, sustained interest in Ge-based devices for CMOS logic stems from intrinsically superior transport properties which will be briefly evoked in this section.

IV.1.2.a. Crystal structure and basic electronic properties

Silicon and Germanium present the same crystal diamond structure, with the difference of a ~+4.2% larger lattice parameter for Ge. As shown in Figure IV-6 both

materials have quite similar chemical affinities, but the dielectric constant is larger in Ge (theoretically causing slightly more pronounced Short Channel Effects).



Material property	*Si*	*Ge*
Crystal structure	Diamond	Diamond
Distance to the nearest atom (Å)	2.35	2.45
Lattice parameter (Å)	5.431	5.658
Number of atoms per cube centimeter	5×10^{22}	4.4×10^{22}
Chemical affinity (eV)	4.05	4
Dielectric constant	$11.9\,\varepsilon_0$	$16.2\,\varepsilon_0$

Figure IV-6: Crystalline diamond structure of Si and Ge, and some elementary properties of bulk Si and Ge at 300K.

In spite of similar structures, different lattices imply different periodic potentials and therefore different E-**k** dispersion relationships (schematically drawn Figure IV-7).

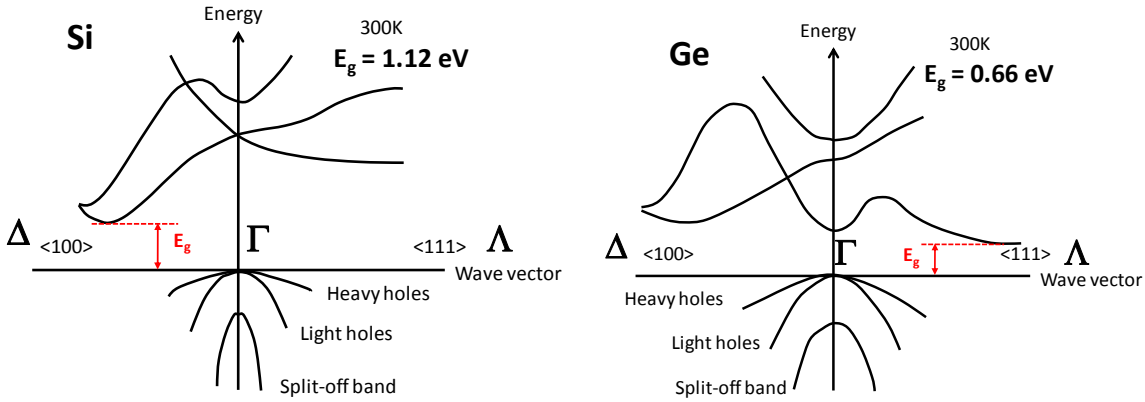


*Figure IV-7: E-**k** diagrams of Si and Ge at 300K.*

Both Si and Ge are indirect bandgap semiconductors. Their conduction band minima correspond respectively to <100> and <111>-directed wavevectors, and the bandgap is roughly two times smaller in Ge (~0.66eV versus 1.12eV).

IV.1.2.b. A smaller bandgap: pros and cons

As a consequence of the smaller bandgap, the intrinsic carrier concentration n_i in Ge is about 2000 times larger than in Si at 300K ((eq. IV-1 and Table IV-1).

$$n_i = \sqrt{N_C \cdot N_V} \cdot \exp\left(\frac{-E_g}{2 \cdot k \cdot T}\right)$$

(eq. IV-1)

N_C and N_V are respectively the effective density of states in the conduction band, and in the valence band.

Parameters at 300K	Si	Ge
Density of states in the conduction band N_C (cm^{-3})	2.8×10^{19}	1.04×10^{19}
Density of states in the valence band N_V (cm^{-3})	1.02×10^{19}	6×10^{18}
Intrinsic carriers concentration n_i (cm^{-3})	1.45×10^{10}	2.4×10^{13}

Table IV-1: Density of states in the conduction and valence band, and intrinsic carrier concentrations in bulk Si and Ge at 300K.

An immediate consequence of this increase in intrinsic carrier concentration on device operation is a larger current density in p/n junctions. If we look at the reverse current density of a p^+/n junction:

$$J_R = q \cdot \sqrt{\frac{D_p}{\tau_p}} \cdot \frac{n_i^{\,2}}{N_d} + \frac{q \cdot n_i \cdot W_{SCR}}{\tau_n}$$

(eq. IV-2)

The first term ($\propto n_i^2$) is a diffusion term, and the second ($\propto n_i$) is a generation term. W_{SCR} is the SCR width, τ_p and τ_n are respectively the holes and electrons lifetimes on the n and p side of the junction. They can be expressed in terms of trap densities:

$$\tau_p = \frac{1}{\sigma_p \cdot v_{th} \cdot N_t}; \tau_n = \frac{1}{\sigma_n \cdot v_{th} \cdot N_t}$$

(eq. IV-3)

Where σ_p and σ_n are the hole and electron capture cross sections, v_{th} the carrier thermal velocity equal to $(3kT/m^*)^{1/2}$ and N_t the trap density. It follows that:

- The **forward current density** is typically **higher in p/n Ge junctions** vs. Si
- Unfortunately, the **leakage current** is also **much higher**
- The **generation/recombination currents** are **higher than in Si**, but **proportionally less important** with respect to the diffusion term…
- … this last observation being valid if we assume the same trap density and carrier lifetimes as in Si. **In practice though**, the trap density is often larger and the **minority carriers lifetime is often lower than in Si**. TCAD fitting of experimental I_D-V_{GS} curves on GeOI pFETs [*Romanjek'08-a*] suggested carrier lifetimes at least one order of magnitude lower than the typical values used for Si.

Another aspect of the smaller bandgap is that it facilitates leakage due to direct Band-To-Band Tunneling (BTBT) and Trap-Assisted Tunneling (TAT), as seen on Figure IV-8.

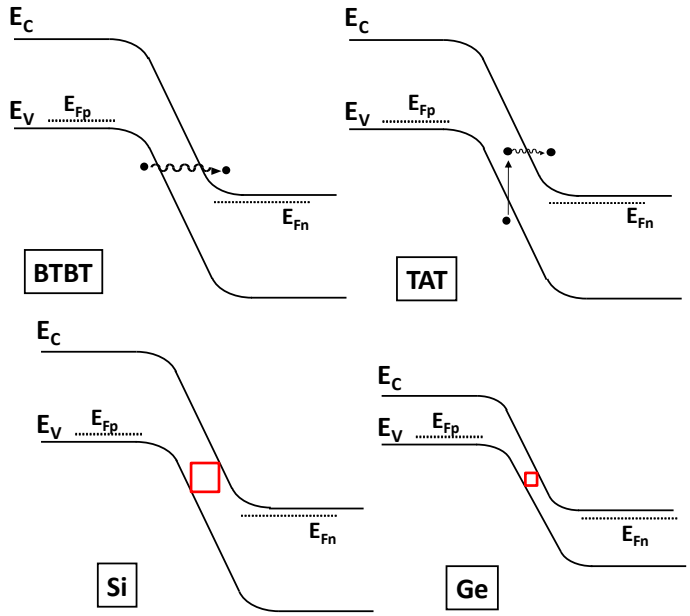


Figure IV-8: Schematic band diagrams explaining BTBT and TAT processes in reverse-biased p/n junctions, and comparative band diagrams of Si and Ge p/n junctions under the same reverse bias.

These side-effects are undesirable in conventional MOSFETs, but can be beneficial for the operation at low supply voltage of small-slope switches such as Impact Ionization or Tunnel FETs (**I-MOS**, **TFETs**) [*Mayer'08*]. Additionally, as in metal/semiconductor contacts, the Fermi-level is pinned within the bandgap, a smaller bandgap results in lower Schottky Barrier Heights, which is an advantage for **SBFETs**.

IV.1.2.c. Effective masses, drift velocity and mobility

The tensor of the conductivity effective masses is derived from the E-**k** dispersion relationship as inversely proportional to the curvature of the bands at their extrema:

$$\frac{1}{m_{ij}^{*}} = \frac{1}{\hbar^2} \cdot \frac{\partial^2 E(k)}{\partial k_i \partial k_j}$$

(eq. IV-4)

As visible on Figure IV-7, the conduction band minima in Si are on the <100> axis (4 equivalent directions), whereas they are located on the <111> axis (8 equivalent directions) in Ge. The constant energy surfaces are therefore located accordingly and can be approximated as 4 (respectively 8) ellipsoids as pictured below in Figure IV-9.

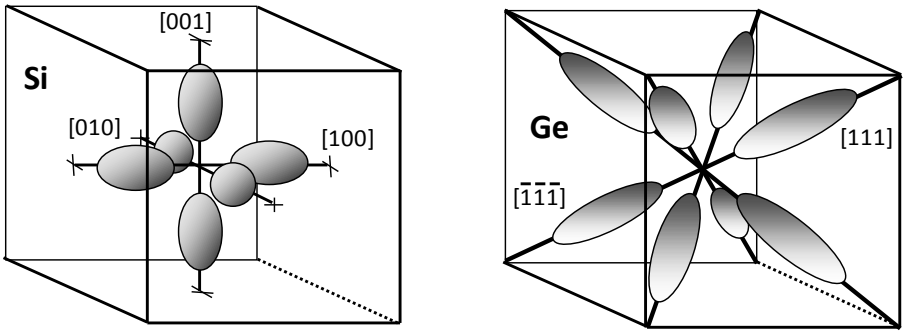


Figure IV-9: Shapes of the CB constant-energy surfaces in Si (left) and Ge (right). The centers of the ellipsoids are located in the case of Si at ¾ of the Γ-X distance (X: boundary of the first Brillouin zone on the Δ axis), and in the case of Ge on the point L (boundary of the first Brillouin zone on the Λ axis). Therefore, eight half ellipsoids, ie 4 ellipsoids should be accounted for projection on a particular transport direction prior to effective mass calculation.

The Valence Band minima are located on Γ for both Si and Ge. Table IV-2 below summarizes the effective masses for Si and Ge along the <100> directions of transport.

Parameters	**Si <100>**	**Ge <100>**
Longitudinal effective mass m_l (kg)	**0.98 m_0**	**1.59 m_0**
Transverse effective mass m_t (kg)	**0.19 m_0**	**0.082 m_0**
Light holes effective mass m_{lh} (kg)	**0.16 m_0**	**0.043 m_0**
Heavy holes effective mass m_{hh} (kg)	**0.49 m_0**	**0.3 m_0**
Split-off holes effective mass m_{SO} (kg)	**0.29 m_0**	**0.084 m_0**

Table IV-2: Longitudinal, transverse, light holes, heavy holes and split-off holes effective masses for Si and Ge for transport along the <100> equivalent directions.

These generally lighter carrier effective masses result in higher drift velocity and mobility. The mobility μ is defined (under the appropriate conditions thoroughly discussed in [*Barral'08*]) as the ratio of the drift velocity ||**v**|| to the applied electric field ||**E**||:

$$\mu = \frac{v}{\mathrm{E}}$$

(eq. IV-5)

A charge travels in a straight line until it is influenced by a scattering mechanism. The average time between collisions, or mean-free time, is τ. By equating the momentum gained by the electron during its mean-free drift (submitted to a force -q.**E**) to the momentum lost in a collision, we obtain:

$$-q \cdot \mathrm{E} \cdot \tau = m^* \cdot v$$

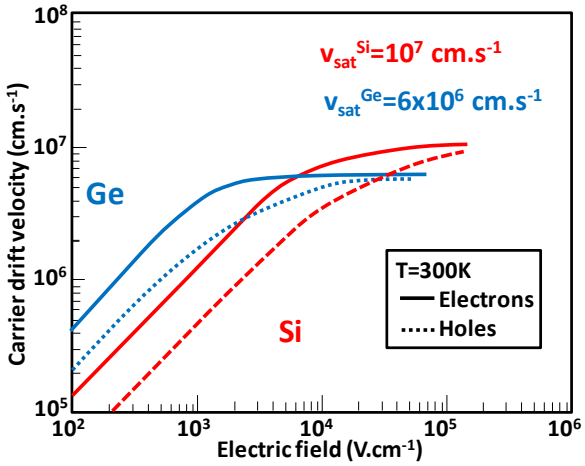
(eq. IV-6)

Hence, μ is inversely proportional to the conductivity effective mass:

$$\mu = \frac{q \cdot \tau}{m^*}$$

(eq. IV-7)

As a consequence, the drift velocity and bulk mobility is higher both for holes and electrons in Ge than in Si, as shown below on Figure IV-10.



Bulk mobility at 300K (cm².V⁻¹.s⁻¹)	Si	Ge	
Electrons	1500	3900	x 2.6
Holes	450	1900	x 4.2

Figure IV-10: Drift mobility versus electric field for electrons and holes in Si and Ge (left) and corresponding bulk mobility at 300K (right) [Sze'07].

The carrier saturation velocity v_{sat} is reached for lower laterals electric fields (typically effective in sub-micronic devices), and is smaller in Ge than in Si. However, this is compensated for by a more favorable non-stationary transport in Ge. The carrier energy relaxation times are larger in Ge than in Si (electrons: ×6.5 – holes: ×8.6, hence a larger velocity overshoot) and the effective masses remain lower, resulting in an expected higher injection velocity v_{inj} at short channel lengths [*Pala'06*].

IV.1.2.d. Summary of the general trends

Intrinsically, carriers transport in Ge is characterized by low effective masses, which should result in higher drive current than in Si. The downside is that the smaller bandgap and the resulting intrinsic carrier concentration are responsible for increased reverse junction current and tunnel leakage. To this, we might add that the trap density is often experimentally found to be larger than in Si, which reduces the minority carriers lifetime and further accentuate the leakage issue. For these reasons Ge-channel devices seem mostly suitable to High Performance applications.

IV.2. Germanium-based substrates

Now that several factors strongly hint the interest of Germanium as a high-mobility semiconductor for High Performance CMOS logic applications, we will review in this section the most usual ways to fabricated Ge substrates. As mentioned before, Ge is rare, expensive, dense, heavy (and most of tools available on the market are calibrated for Si wafers handling). Using bulk Germanium wafers for device fabrications would therefore lack sustainability and cost-effectiveness. This is the reason why we will present the techniques to obtain Germanium-On-Silicon (bulk-like) and Germanium-On-Insulator (GeOI) wafers.

IV.2.1. **Ge on Si**

The lattice mismatch of 4.2% between Ge and Si is such that it is relatively difficult to achieve, through heteroepitaxy, Ge layers with the desired properties (*ie* planarity compatible with advanced lithography steps and layer transfer, minimal defects density etc.). The critical thickness h_c beyond which defects tend to form and propagate (threading dislocations, Figure IV-11) is of ~2-4nm [*People'85-a*].

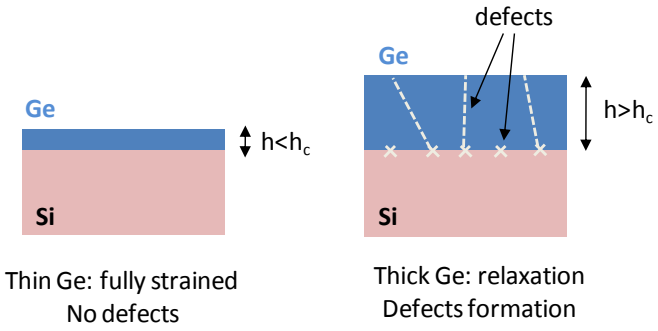


Figure IV-11: Appearance of point defects and threading dislocations through strain relaxation for epitaxially grown Ge on Si above the critical thickness h_c.

This critical thickness is quite extreme for device fabrication, and the active layer is still fully strained (which is not bad from the viewpoint of transport properties, but can later lead to defects formation due to process-induced strain relaxation). We will present below two techniques for obtaining relaxed Ge layers on top of Si substrates.

IV.2.1.a. Virtual substrates and graded buffer layers

The virtual substrate approach [*Currie'98*] consists in gradually increasing the Ge concentration of stacked SiGe layers from 0% to 100% over roughly 10µm (10% Ge.µm^{-1}). It leads to a fully relaxed Ge top layer with threading dislocations densities of a few 10^6 cm^{-2}. However, this method results in a high surface roughness with pronounced cross-hatch

patterns, and therefore requires intermediate and/or final CMP steps to smooth the surface (Figure IV-12).

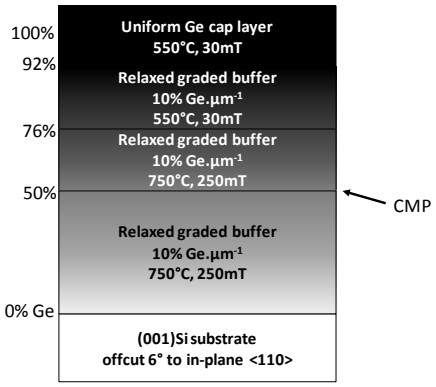


Figure IV-12: Example of a graded buffer SiGe structure with a relaxed Ge layer on top, as reported in [Currie'98].

This approach is advantageous in that it confines the dislocations away from the top layer, resulting in a good crystalline quality of the relaxed Ge. However, it is a slow and expensive process, subject to thickness uniformity issues (substrates "bulging" over ~250nm).

IV.2.1.b. Thermal cycling

The thermal cycling approach was first evoked in [*Colace'98*] and patented shortly after [*Hernandez'01*]. It starts with depositing at "low" temperature a thin (~200nm) precursor film of Germanium, followed by deposition at a higher temperature of a thicker (~2µm) Ge layer. The low temperature used for the first step (330°C-400°C) enables the occurrence of plastic strain relaxation without inducing an excessive amount of surface undulations. The high temperature of the second step (600°C-850°C) leads to a drastic reduction of the emergent dislocations density as well as a faster growth. Subsequently, thermal cycling steps may be performed (typically in the range of 750°C-900°C) so as to provoke thermal assisted propagation of the emergent threading segments towards the substrates edges and therefore further reduce the density of crystalline defects (Figure IV-13).

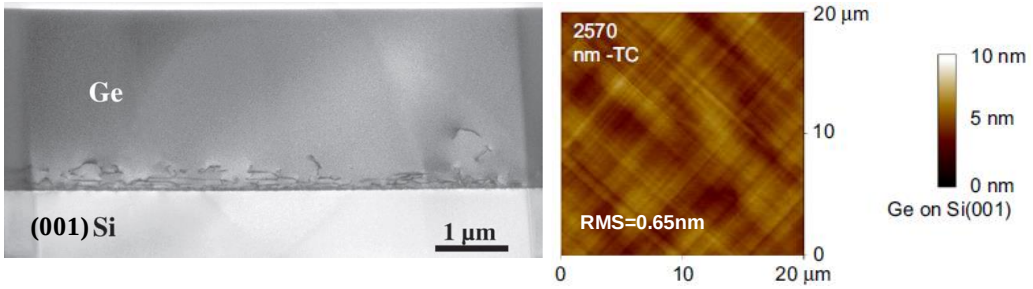


Figure IV-13: XTEM image along the [110] direction of a 2570nm thick Ge layer grown on (001)Si, after thermal cycling showing misfit dislocations confined within the first 0.5µm of the Ge layer (picture: A.-M. Papon), and corresponding tapping mode AFM 20µm×20µm scan of the surface showing RMS roughness of 0.65nm [Hartmann'08].

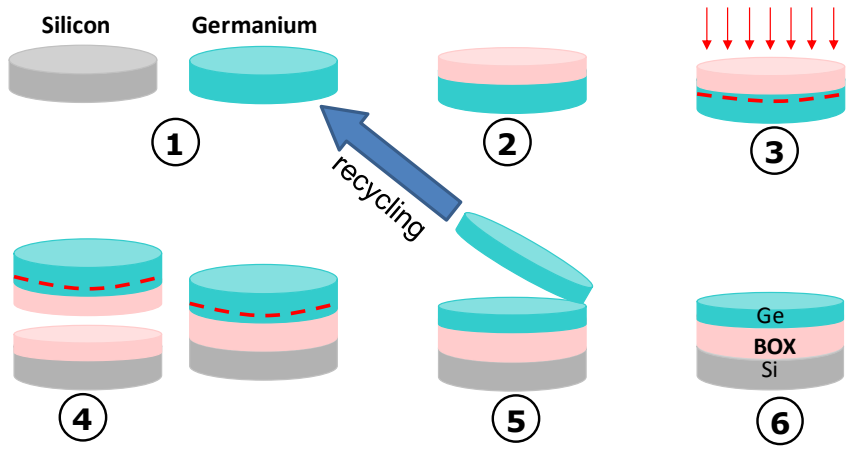
Finally, threading dislocations densities (TDD) of ~10^7 cm^{-2} can be obtained in Ge layers grown on (001)Si after thermal cycling [*Hartmann'05-a*]. This is slightly higher than in virtual substrates using graded buffer layers, but the process is faster, cheaper and results in better thickness uniformity.

IV.2.2. **Germanium-On-Insulator (GeOI)**

We previously presented methods aiming at fabricating bulk-like substrates. However, substrates on insulator present basically the same interest for Ge than for Si, *ie* an improved electrostatic integrity, being of paramount importance at short gate lengths. Additionally, it allows partially getting rid of junction leakage, which is a major issue in Germanium-based devices.

IV.2.2.a. Smart Cut™

Invented by Michel Bruel in the 1990's [*Bruel'91*], [*Bruel'95*], the Smart Cut™ technology (trademarked by Soitec) replaced SIMOX (Separation by Implantation of OXygen [*Izumi'78*]) as the main technique to fabricate Silicon-On-Insulator substrates and represents nowadays about 90% of the SOI market. It can be applied to manufacture GeOI substrates as illustrated in Figure IV-14.



1. **Initials wafers A (Ge) & B (Si)**
2. **Oxide deposition on Germanium wafer**
3. **H^+ Implantation into Germanium**
4. **Bonding on Si or oxidized Si**
5. **Splitting**
6. **Final treatments**

Figure IV-14: Schematic flow of the Smart Cut™ process to manufacture GeOI wafers.

The initial Germanium donor wafers can either be epitaxially grown Ge On Si [*Deguet'05*] or bulk Ge [*Deguet'06*]. A HF-based Ge cleaning process with low Ge

consumption and a high particle removal rate enables to maintain a surface RMS roughness comparable to the one of the starting materials (less than 0.2 nm for a 5µm×5µm AFM scan, Figure IV-15).

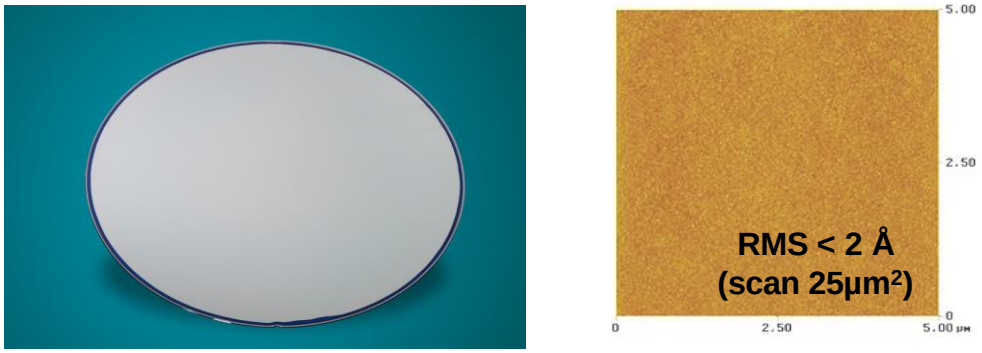


Figure IV-15: A 200m Smart Cut™ GeOI wafer, with RMS surface roughness lower than 2Å (5µm×5µm scan).

As the germanium oxidized phase cannot play the role of an insulating film due to its instability, a plasma enhanced chemical vapor deposition (PECVD) SiO_2 layer is performed on the germanium donor wafer in order to form a part of the final buried oxide (BOX). This oxide is deposited (thickness: a few hundreds of nm) and densified at temperatures around 600°C. Capped germanium wafers are then ion implanted with H^+, with doses and energies in the mid 10^{16} at/cm^2 and in the 50 to 100 keV range, respectively. Surfaces are then cleaned and prepared for room temperature hydrophilic bonding to thermally oxidized Si base substrates. Depending on the donor wafers type (bulk or epitaxial), the main difficulty consists in managing the splitting, due to the difference between the thermal expansion coefficients of Si and Ge [*Clavelier'06*]. Once the transfer step is optimized in terms of implantation and splitting conditions, GeOI structures are formed on 200mm wafers (Ge thickness from 30 to 200nm depending on the targeted applications). Final treatments like annealing and polishing generate GeOI surfaces fully compatible with device processing.

The most recent GeOI wafers featured an average of less than 10 defects per cm^2 in surface, which is approaching that of the Ge bulk wafers with about 3 defects per cm^2. The fact that no extended defects observable on plane-view TEM suggests a defect density below 10^5 cm^{-2} for GeOI realized with bulk Ge donor wafers. Raman measurements have demonstrated that the wafer fabrication process does not induce any significant strain [*Akatsu'06*].

IV.2.2.b. Ge enrichment

The Ge enrichment technique, somewhat abusively called Ge "condensation" was first developed in Japan (University of Tokyo, Mirai, Toshiba) roughly ten years ago [*Tezuka'01*], [*Nakaharai'03*]. The starting material is an SOI wafer, on top of which a SiGe layer with a

low Ge content is epitaxially grown (*eg* 10%, to avoid a large lattice mismatch and subsequent dislocations). The process relies on the fact that Si atoms are preferentially oxidized with respect to Ge atoms. Therefore, during annealing steps in O_2, a SiO_2 layer forms on the surface, consuming the Si while the Ge atoms tend to be "pushed" towards the buried oxide. These oxidation anneals are alternated with homogenization annealing steps in an inert gas (Ar, or N_2), and the process is pursued until the desired Ge content is reached. For some reason still unclear at the moment, the RMS surface roughness seems to be decreased by performing homogenization anneals under Argon rather than Nitrogen [*Souriau'09*], (Figure IV-16).

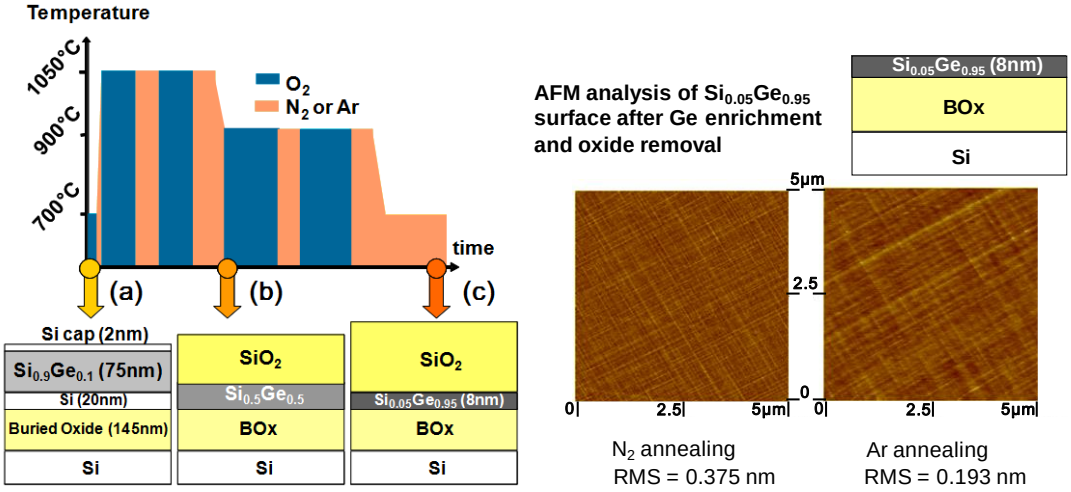


Figure IV-16: Schematics of a Ge enrichment process used for obtaining 95% SiGe On Insulator [Vincent'07-a], [Hutin'10-b]. On the right, tapping mode AFM scans of the surface after oxide removal in the case of N_2 and Ar homogenization anneals.

The enrichment technique can therefore be used to obtain almost pure Ge (~95%) on Insulator (Figure IV-17). Eventually, a pure Ge layer can be epitaxially grown after oxide removal for fabricating pure GeOI devices on relaxed substrates [*Hutin'10-a&b*].

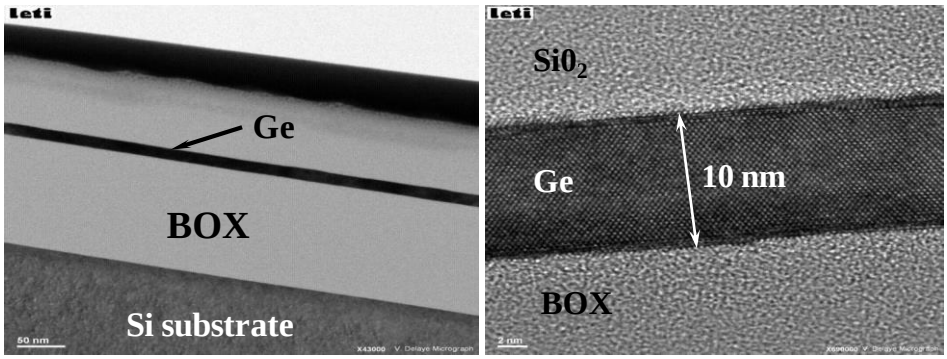


Figure IV-17: TEM pictures of a 10nm thick enriched SiGe On Insulator film (x_{Ge}>95%) on a 200mm substrate (pictures: V. Delaye).

It is of course also possible to cease the enrichment process as soon as the desired Germanium fraction and film thickness are reached. In this case, the initial low-Ge-content SiGe layer thickness can be tuned to obtain various concentrations of compressively strained, higher Ge content SiGe [*Hutin'10-c*].

As we will see later on, there are some concerns regarding the interest of Ge and SiGe nFETs (paragraph IV.3.2.). A significant strength of this technique is that it can be localized so as to allow co-integrating Si nFETs and SiGe or Ge pFETs [*Tezuka'05*], [*Tezuka'06*], [*Le Royer'10-a*] for Dual Channel On Insulator (DCOI).

IV.2.3. **Hybrid substrates for advanced CMOS and optoelectronics**

As mentioned above, the enrichment technique can be used to fabricate hybrid n-SOI/p-GeOI substrates, or even n-sSOI/p-sGeOI (strained SOI, strained GeOI) substrates [*Clavelier'07*] to take advantage of an optimal mobility configuration for electrons and for holes. This planar co-integration can be achieved by masking the n-type active regions prior to SiGe selective epitaxy, as shown on Figure IV-18.

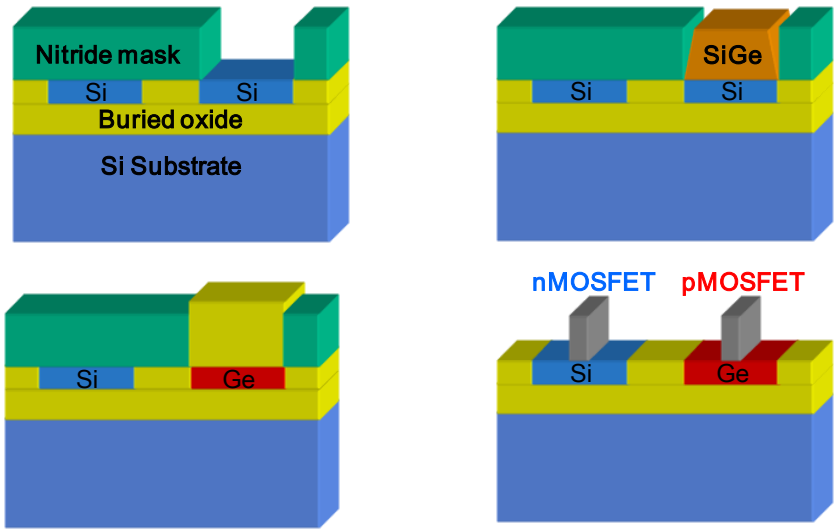


Figure IV-18: Simplified process flow to obtain n-SOI/p-GeOI hybrid substrates through selective epitaxy and Ge enrichment [Clavelier'07].

This approach has been realized in a "checkerboard" configuration on 200mm SOI substrates in Leti [*Le Royer'10-a*] (Figure IV-19). Functional GeOI pFETs and SOI nFETs were successfully co-integrated on the same wafer (different dice, Figure IV-19).

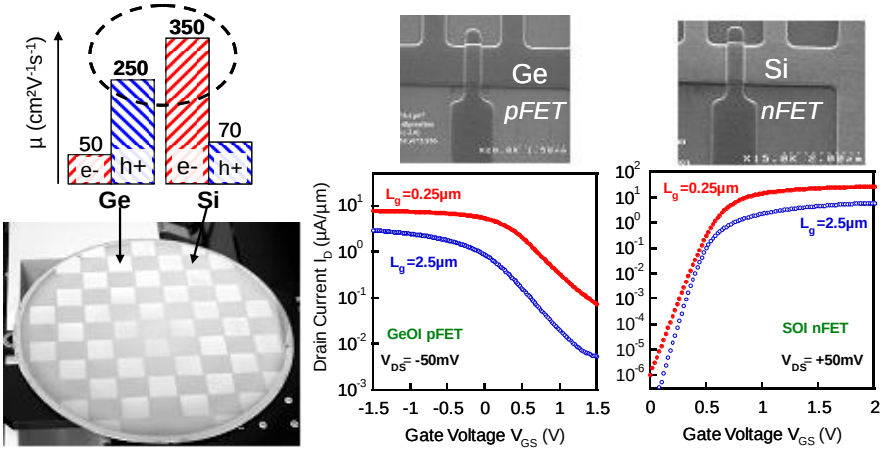


Figure IV-19: 200mm « checkerboard » hybrid SOI and GeOI wafer with functional Ge pFETs and Si nFETs [Le Royer'10-a] taking advantage of the best-case mobility for holes and electrons (data for mobility: pseudo-MOS measurements from [Nguyen'07].

GeOI and SOI can also be co-integrated in a non-planar way. Vertical 3D monolithic co-integration can be realized either in parallel, or sequentially. The parallel co-integration consists in separately fully processing the GeOI and SOI transistors prior to stacking them on top of each other. The sequential co-integration starts with the processing of the SOI bottom layer, growth and planarization of an interlayer oxide, and is pursued by the bonding of the Ge film and fabrication of the upper stage transistors (Figure IV-20). This is preferably carried out in this order, as the processing temperatures are higher for Silicon than for Germanium (dopant activation annealing temperatures in Si are typically above 937°C, which is the melting point of Ge). This 3D approach represents an average density gain over planar integration of ~40% (computed for a 16 bits Multiply ACcumulate gate with 45nm node design rules [*Batude'09-c*]).

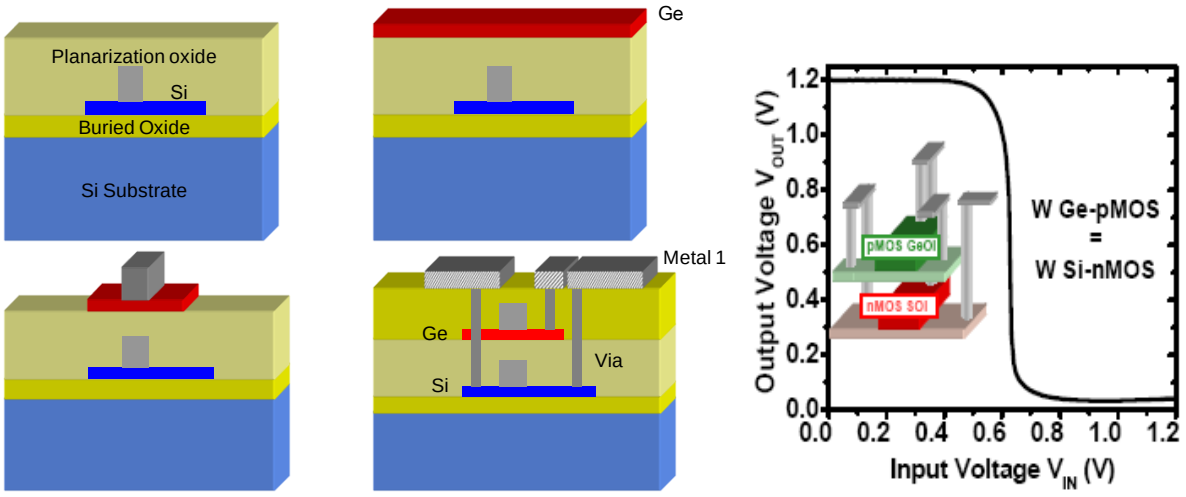


Figure IV-20: Vertical 3D sequential monolithic co-integration of SOI and GeOI [Batude'09-a], and demonstration of a functional inverter with a bottom SOI nFET and top Ge pFET [Batude'09-b].

Beyond CMOS applications, the lattice parameter of Ge is known to closely match that of some III-V semiconductors (InP, GaAs, InGaAs…). The direct bandgap of these III-V materials make them especially interesting for optoelectronics applications (*eg.* LED arrays). Ge can then used as a buried growth template enabling co-integration of Si CMOS with III-V optoelectronics. This is the concept of Silicon On Lattice-Engineered Substrates (SOLES) developed at MIT. SOLES were originally fabricated by bonding of a Si film onto a SiGe virtual substrate [*Dohrman'06*], [*Chilukuri'07*]. The latter can also be replaced by a GeOI substrate [*Fitzgerald'08*], forming a "Ge sandwich" in the buried oxide as shown on Figure IV-21. The top oxide layer is etched away, exposing the Ge template on which a III-V epitaxy is facilitated with respect to Si due to a smaller lattice mismatch.

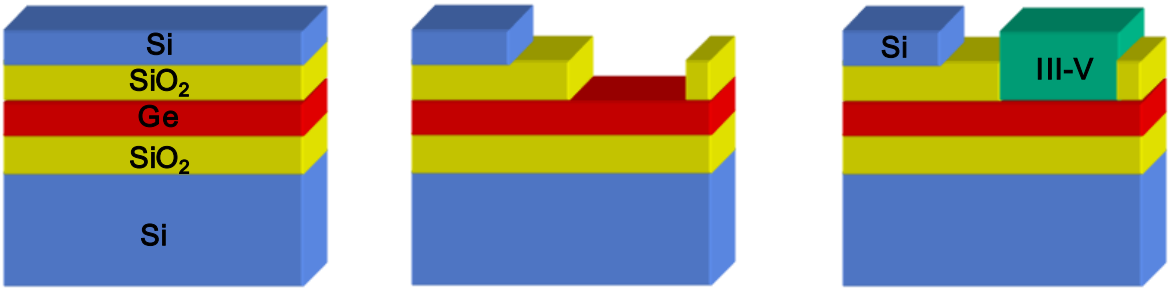


Figure IV-21: Silicon On Lattice-Engineered Substrate (SOLES) fabricated from a GeOI wafer [Fitzgerald'08], for monolithic co-integration of Si CMOS and III-V optoelectronics.

After reviewing several aspects of Ge-based substrates fabrication and applications, the next part will focus on CMOS devices processing on Germanium.

IV.3. Ge and GeOI CMOS devices

IV.3.1. **Generalities on technological modules**

The well-known process conditions used to fabricate MOSFETs on bulk Si or SOI wafers have to be adapted when changing the semiconductor material. Silicon is a very well known material thanks to 40 years of extensive research for microelectronics applications. In comparison, very few studies on Ge were conducted since the 1960's. The basic properties of Germanium have to be accounted for in order to optimize Ge MOS technology, such as lower characteristic temperatures for processing (melting point at 937°C in Ge versus 1420°C for Si), increased sensitivity to metal contamination, higher point defects diffusivity [*Vanhellemont'07*] and a general intolerance towards treatments based on aqueous solutions (due to the instability and volatility of Ge oxides).

IV.3.1.a. Wet etching and cleaning

Although Ge is a group IV element like Si, its etch rate can be very different from that of Si. A fundamental difference is that a thin passivating oxide is formed on top of Si in oxidizing solutions (H_2O_2, ozonated water), which limits the etch rate of Si in HF-free solutions. GeO_2, however, is water soluble. Thus, the simultaneous oxidation of Ge and etch of GeO_2 results in a net Ge etch. Additionally, Si does not etch in hot water, H_2O_2, HCl:H_2O_2, and H_2SO_4:H_2O_2, whereas Ge does [*Onsia'05*]. A large variety of wet chemistries and corresponding Ge etch rates are reported in [*Brunco'08*]. In Leti, the Ge cleaning treatments are based on HF/HCl and ozonated HCl.

IV.3.1.b. Resist stripping

In a Ge or GeOI CMOS technology, it is necessary to determine a Ge dedicated resist stripping process, because of the germanium non-compatibility with usual cleaning solution. As a matter of fact, the Si dedicated stripping processes are generally based on H_2O_2 solutions which lead to a large Ge consumption (>1µm/min). Compatibility studies showed a passivation effect on germanium during dry steps for high $N_2/(O_2+N_2)$ plasma ratios [*Lachal'06*]. Thus, for the post-active area etching, dry stripping shows a good compatibility on GeOI, as the lateral Ge consumption due to the water rinse step is avoided. Using a ramping temperature process, good resist removal efficiency can also be achieved during post-implant stripping [*Lachal'06*].

IV.3.1.c. Gate stack and interface with high-k dielectrics

The increasing use of high-k materials (like HfO_2) as gate dielectrics contributed to the come-back of Germanium as a serious alternative to Silicon-channel devices. However, an interfacial layer between channel and high-k appears absolutely necessary to prevent Ge atoms from diffusing into the gate dielectric and degrade the electrical characteristics.

Surface treatment by NH_3 so as to form a Germanium oxynitride (GeON) was proven to prevent Ge diffusion and improve the MOS capacitance behavior [*Chui'04*], [*Van Elshocht'04*], [*Le Royer'05*]. It was also shown that HfO_2 or ZrO_2 high-k combined with GeON interlayers (ILs) could be scaled to EOT values lower than 1nm while maintaining a low gate leakage [*Chui'02-b*], [*Chen'04*], [*Dimoulas'05*], [*Ritenour'06*]. However, this technique was ultimately judged insufficient in terms of passivation, resulting in non-ideal hysteretic C-V characteristics and high D_{it} (typically 5×10^{12} - 10^{13} $eV^{-1}.cm^{-2}$).

Since this large interface states density was believed to originate from the process of Germanium oxidation, other interlayer schemes were investigated, such as AlN [*Whang'04*] or partially oxidized Si cap [*Wu'04*]. Concerning the latter, the diffusion of Ge atoms within

the cap has been identified as a critical point with regards to the structural, physico-chemical and electrical aspects of Si-passivated gate stacks on Ge [*Caymax'09-a*]. It is yet considered to be the most scalable option and has been widely adopted for sub-micron Ge pFETs fabrication. For instance, sub-nanometer EOT (HfO_2 2nm/ 0.5nm SiO_x /8 Si monolayers) with relatively low gate leakage was recently demonstrated on L_G=70nm Ge pFETs [*Mitard'09*].
Yet, it was shown in [*Dimoulas'07*] that avoiding Ge oxidation at all cost was neither a necessary nor a sufficient condition for achieving a good interface. This is supported by the fact that no Ge oxidation is observed after deposition of HfO_2 directly on Ge, which does not prevent a poor electrical behavior of the interface. On the other hand, rare earth oxides deposited on Ge (such as CeO_2, La_2O_3, Dy_2O_3, Gd_2O_3) provide a good barrier for Ge diffusion, with relatively limited D_{it} (~10^{12} $eV^{-1}.cm^{-2}$, *ie* lower than GeON), and reduced hysteresis with respect to GeON/HfO_2 stacks. This is presumably due to the large polarizability of rare earth metal ions in oxides, which may affect the electrical activity of the interface states. However, due to insufficiently large energy bandgaps, these rare earth oxides should be associated to HfO_2 (and serve as IL) to limit the gate leakage current.

IV.3.1.d. Dopant diffusion, solid solubility and activation

IV.3.1.d.i. Diffusion

The data on the diffusivity of the usual dopant species in Germanium are reported in this paragraph. The various diffusion mechanisms in Germanium are thoroughly explained in [*Koffel'08*]. In short, the diffusion of impurities is linked to that of defects, in that defects can be seen as vehicles for the displacement of dopant atoms. In a crystal under thermodynamic equilibrium, the thermodynamic theory shows that a non-zero concentration of defects [X^*] exists, equal to:

$$\left[X^*\right] = N_S \exp\left(\frac{-\Delta G_X^F}{kT}\right) = N_S \exp\left(\frac{\Delta S_X^F}{kT}\right)\exp\left(\frac{-\Delta H_X^F}{kT}\right)$$

(eq. IV-8)

where N_S is the density of sites in the crystal (4.41×10^{22} cm^{-3} in Ge), ΔG_X the free enthalpy (Gibbs free energy) corresponding to the formation of the defect X, ΔH_X and ΔS_X are respectively the associated enthalpy and entropy variations. The higher [X^*], the higher the number of defects which can pair up with impurities and enable their diffusion. Hence, the diffusivity of dopants within a crystal can be expressed in a compact way as an Arrhenius law:

$$D = D_0 \cdot \exp\left(\frac{-E_a}{k \cdot T}\right)$$

(eq. IV-9)

The pre-exponential factor D_0 and the activation energy E_a can be determined by fitting SIMS measurements after the introduction of dopant atoms and activation anneals on a given temperature range. The density of defects plays a major role in dopant atoms diffusion, therefore the initial crystalline quality of the semiconductor as well as the damages provoked during ion implantation influence the extracted parameters. The data presented below collected from various sources is thus very scattered (one can almost see the improvement of the material quality over the years), but is sufficient to provide general trends.

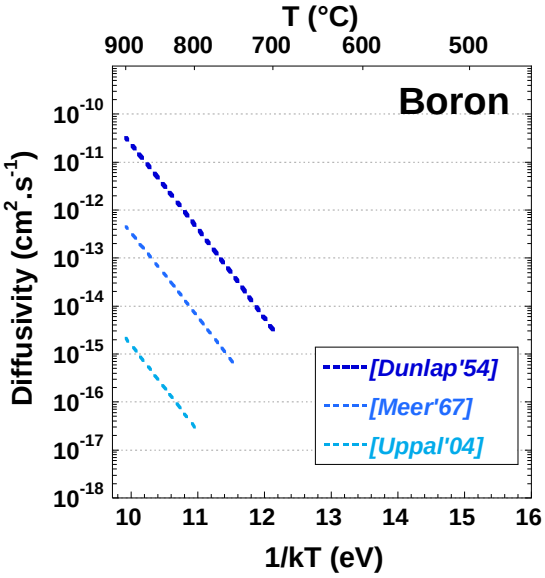


Figure IV-22: Arrhenius plot of the diffusivity of Boron in Germanium as reported in the literature.

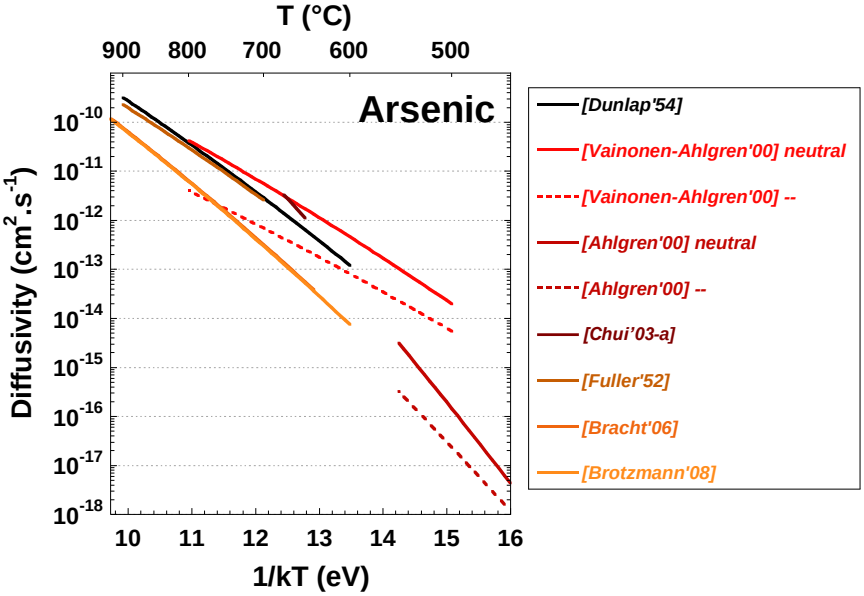


Figure IV-23: Arrhenius plot of the diffusivity of Arsenic in Germanium as reported in the literature. In [Ahlgren'00] and [Vainonen-Ahlgren'00], neutral refers to the diffusion through neutral defects, and - - to diffusion through defects with a double negative charge.

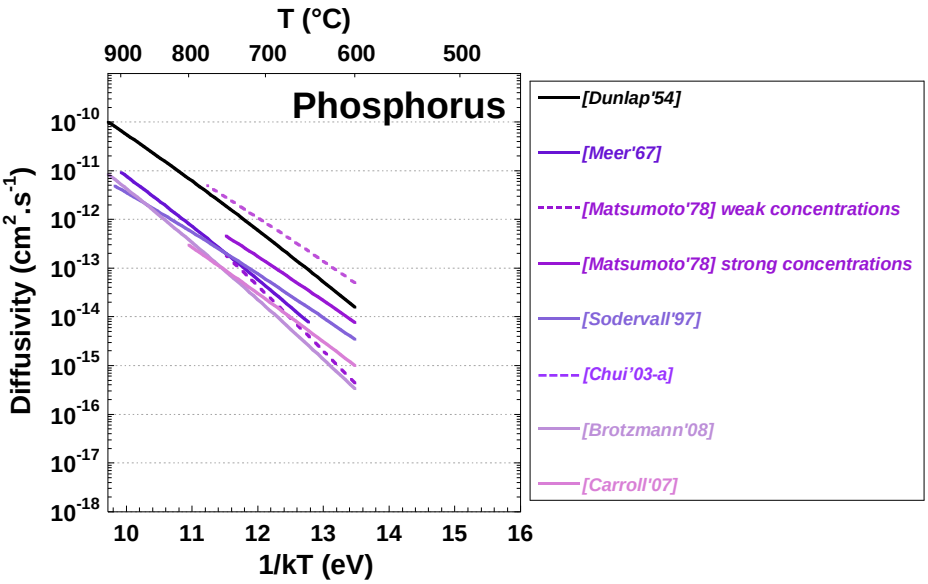


Figure IV-24: Arrhenius plot of the diffusivity of Phosphorus in Germanium as reported in the literature.

Unlike in Si, the diffusion is most limited for p-type impurities (Boron), while it is large for n-type impurities (Arsenic, Phosphorus). It is now commonly admitted that Boron atoms will display very little to no diffusion for Rapid Thermal Anneals (RTA) below 800°C. On the other hand, Phosphorus and Arsenic diffuse very rapidly above 550°C. As a consequence, this RTA activation annealing temperature should not be exceeded in the framework of shallow junction formation for Ge CMOS. The duration of the RTA should be comprised between 10 and 60 seconds [*Koffel'08*].

IV.3.1.d.ii. Solid solubility

When dopants are introduced within a semiconductor, they should be placed in a substitutional site (*ie* take the place of a Silicon or Germanium atom) in order to be electrically active. However, only a limited number of atoms can occupy such a position, and this limit is the solid solubility. When the concentration of dopant atoms exceeds this solid solubility limit (SSL), the excess impurities form electrically inactive clusters. The SSL can be computed by *ab initio* calculations, although it is most of the time deduced from resistivity measurements. These measurements give an estimate of the maximal concentration of electrically active dopants, which is often directly interpreted as the solid-solubility limit. Nevertheless, such an interpretation raises two issues:

- The SSL corresponds to the conditions of thermodynamic equilibrium. If the doping process is metastable, *eg* activation through Solid Phase Epitaxial Regrowth (SPER) or Laser Thermal Annealing (LTA), the electrically active dopant concentration might exceed it.

- Deducing the active concentration from resistivity measurements imply an excellent knowledge of the carriers mobility at high impurities concentration. Unfortunately, as it will be shown in the next paragraph, this is not so obvious in Germanium.

These are probably the main reasons why the SSL values reported below Table IV-3 appear so scattered (in the case of Boron, over almost two decades).

Element	Solid Solubility (cm^{-3})	Ref.
B	5.5×10^{18}	[*Trumbore'60*]
B	6.5×10^{18}	[*Uppal'01*]
B	2×10^{18}	[*Uppal'04*]
B	1×10^{19}	[*Delugas'04*]
B	2×10^{20}	[*Suh'05*]
B	1×10^{19}	[*Chao'05*]
B	5.5×10^{18}	[*Satta'06*]
P	2×10^{20}	[*Trumbore'60*]
P	2×10^{20}	[*Satta'06*]
As	8.1×10^{19}	[*Trumbore'60*]
As	5×10^{19}	[*Ahlgren'00*]
As	8.1×10^{19}	[*Satta'06*]
Sb	1.2×10^{19}	[*Trumbore'60*]
Ga	4.9×10^{20}	[*Trumbore'60*]

Table IV-3: Solid solubility limits of p-type (blue) and n-type (red) dopants in Germanium, as reported in the literature.

IV.3.1.d.iii. Activation

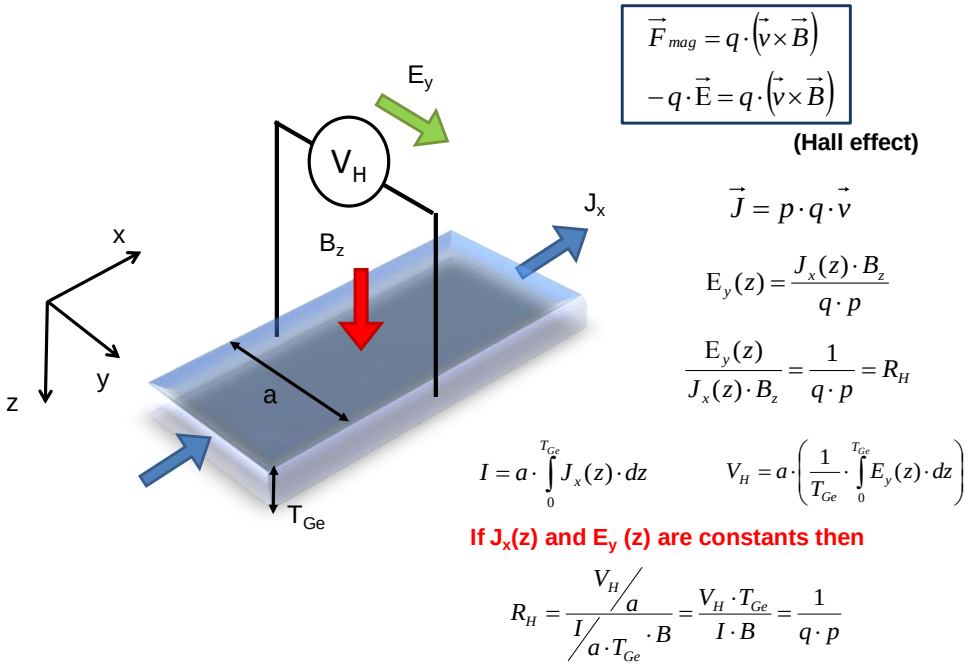
The activation level N_{act} is the concentration of electrically active impurities. The knowledge of N_{act} is important both for evaluating the quality of a doping process, for providing a good approximation the density of free carriers (*eg* for predictive simulation). Nonetheless, prior to giving typical values of activation levels for various dopant species in Germanium, it is important to review the uncertainties associated to N_{act} extraction according to the different measurement methods.

Hall-effect measurements

The density of free carriers can be extracted directly on thin films through Hall-effect measurements. The Hall effect occurs in metals and semiconductor when a magnetic field (*eg* B=0.8T) is applied perpendicularly to the current flow. An electric field appears so as to

counterbalance the effect of the resulting Lorentz force (vectorial product of the magnetic field and the carriers velocity). By measuring the Hall voltage V_H arising from this electric field, the density of free carriers can be determined.

The principle and the main equations are given below, Figure IV-25.



$$\vec{F}_{mag} = q \cdot \left(\vec{v} \times \vec{B}\right)$$

$$-q \cdot \vec{E} = q \cdot \left(\vec{v} \times \vec{B}\right)$$

$$\vec{J} = p \cdot q \cdot \vec{v}$$

$$E_y(z) = \frac{J_x(z) \cdot B_z}{q \cdot p}$$

$$\frac{E_y(z)}{J_x(z) \cdot B_z} = \frac{1}{q \cdot p} = R_H$$

$$I = a \cdot \int_0^{T_{Ge}} J_x(z) \cdot dz \qquad V_H = a \cdot \left(\frac{1}{T_{Ge}} \cdot \int_0^{T_{Ge}} E_y(z) \cdot dz \right)$$

$$R_H = \frac{V_H / a}{I / a \cdot T_{Ge} \cdot B} = \frac{V_H \cdot T_{Ge}}{I \cdot B} = \frac{1}{q \cdot p}$$

Figure IV-25: Principle of free carrier density extractions (case of p-type Germanium) through Hall-effect measurement. In practice, the current I is applied between two probes in the presence of the magnetic field B, and V_H is measured between two other probes. The measurement can be performed several times, switching the roles of each probe (apply current or measure Hall voltage), to apply a geometrical correction factor.

This method is simple, non-destructive, convenient, and cumulates relatively few uncertainties. Unfortunately, it is not adapted to samples with non-uniform doping. The formula for the Hall factor R_H is the following:

$$R_H = \frac{V_H \cdot T_{Ge}}{I \cdot B} = \frac{1}{q \cdot p}$$

(eq. IV-10)

It can be derived **under the condition that the current density J_x is constant across the sample depth**. This assumption is incorrect if the electrically active dopant concentration varies with the depth, which is generally the case after dopant implantation and activation annealing on Si or Ge. In SOI or GeOI, as the amorphization of the semiconductor down to the Buried Oxide should be avoided at all cost during implantation, there is little chance that the impurities concentration exceeds the SSL over the entire film thickness.

Using (eq. IV-10) on a sample with non-uniform doping would yield some kind of "averaged" carrier concentration in a fictional equivalent uniformly doped semiconductor of

same thickness, which is irrelevant in terms of activation level extraction. Integrating $J_x(z)$ would (ironically) require the knowledge of both the carriers concentration and mobility as $J_x(z)=q.p(z).\mu(z).E_x(z)$.

Spreading Resistance Probe (SRP) profiling

Another method for determining the activation level consists in measuring the sheet resistance of a doped semiconductor layer, which is the inverse of the conductivity integrated over the sample thickness (below for a p-type semiconductor):

$$R_{sh} = \frac{1}{\int_0^{T_{Ge}} \sigma(z)\cdot dz} = \frac{1}{q\cdot \int_0^{T_{Ge}} p(z)\cdot \mu_h(z;p(z))\cdot dz}$$

(eq. IV-11)

The most common protocol is to perform Spreading Resistance Probe profiling. It is a destructive method, because the sample should be beveled so as to allow the probe to measure the resistivity versus depth (Figure IV-26).

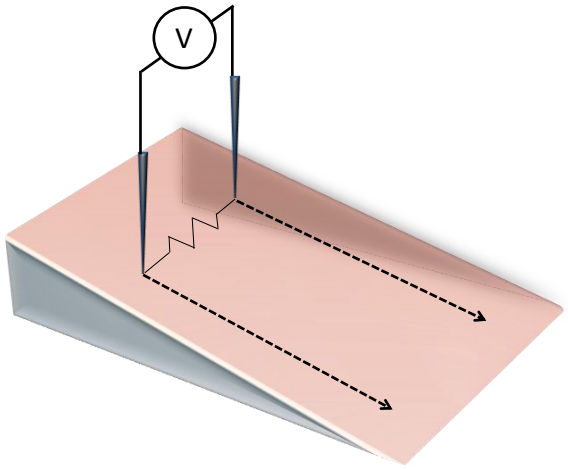


Figure IV-26: Principle of Spreading Resistance Probe profiling on a beveled sample.

Since the resistance is linked to the µ.p product, the interpretation of the resistance measurement in terms of carriers concentration requires:

- **The knowledge of the relationship between µ and p**, as the mobility depends on scattering by ionized impurities
- **Complementary SIMS measurements** to evaluate the impurities concentration at a given depth (for concentrations far below the solid solubility limit, one can consider that the "chemical" concentration detected by SIMS is equivalent to the concentration of electrically active dopants). A very common assumption is indeed to consider that the carrier concentration is that of the

ionized impurities $p \approx N_A^-$, and that all the impurities are available for conduction when their concentration is below the solid solubility limit (this point will be discussed shortly thereafter).

Sheet resistance measurements and spectroscopic ellipsometry

This method is a non-destructive alternative to SRP, applied in [*Hutin'08-a&b*] to the case of GeOI wafers of different thicknesses. The "chemical" depth profile is determined by Crystal-TRIM Monte Carlo simulation [*Posselt'94*], and the Germanium thickness is measured by spectroscopic ellipsometry. The sheet resistance is measured on Van der Pauw structures (VdP), and the activation level N_{act} is extracted by fitting using (eq. IV-11) as shown on Figure IV-27.

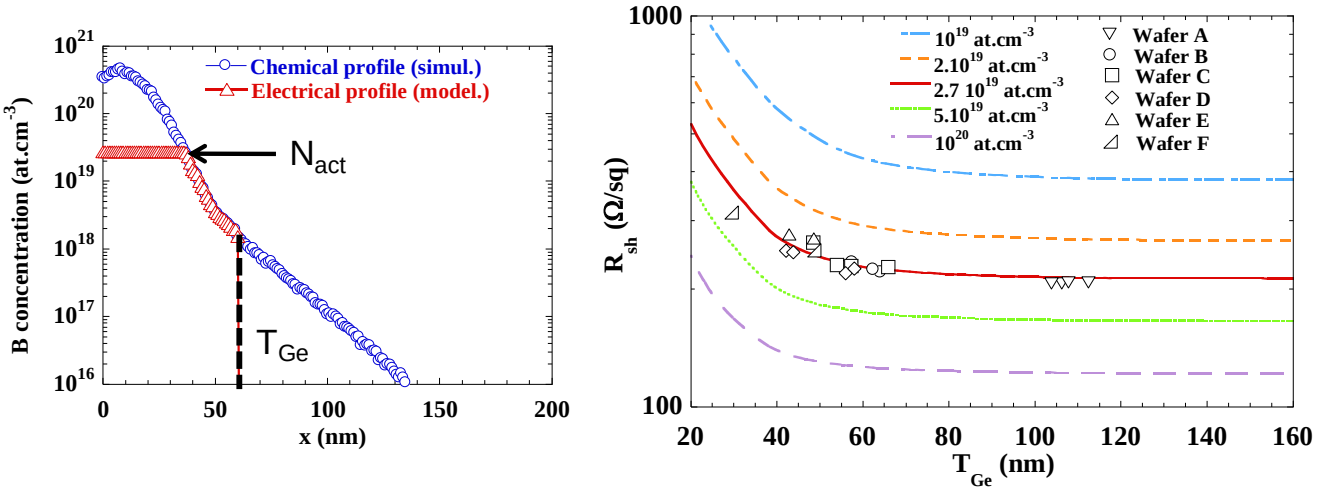


Figure IV-27: (Left) Simulated chemical Boron profile, and corresponding modelling of the electrically active Boron profile, delimited by N_{act} and T_{Ge}. (Right) Sheet resistance versus Germanium thickness for various N_{act} , and experimental points corresponding to VdP measurements on wafers of various thicknesses subject to identical doping conditions.

The method described above is very easy to use but relies on several simplifying assumptions. First, we consider that Monte Carlo simulation reproduces accurately the chemical profile. Second, a constant, flat electrical concentration profile is assumed when the chemical profile exceeds an arbitrarily chosen N_{act}. And last but not least, as for SRP, we suppose that the relationship linking carrier mobility and carrier concentration is known with precision. As we will discuss below, this is far from granted in Germanium.

Mobility versus impurities concentration in Germanium

The knowledge of μ(n) or μ(p) is of paramount importance for SRP calibration or N_{act} extraction from sheet resistance measurements. In the case of Germanium, some studies

report on the hole mobility in p-doped Ge [*Prince'53*], [*Trumbore'58*], [*Golikova'62*], [*Chun'92*], [*Chun'96*], [*Nguyen'03*] and on electron mobility in n-doped Ge [*Prince'53*], [*Fistul'62*], [*Hilsum'74*], [*Nguyen'03*]. The corresponding plots are reproduced in Figure IV-28 and Figure IV-29.

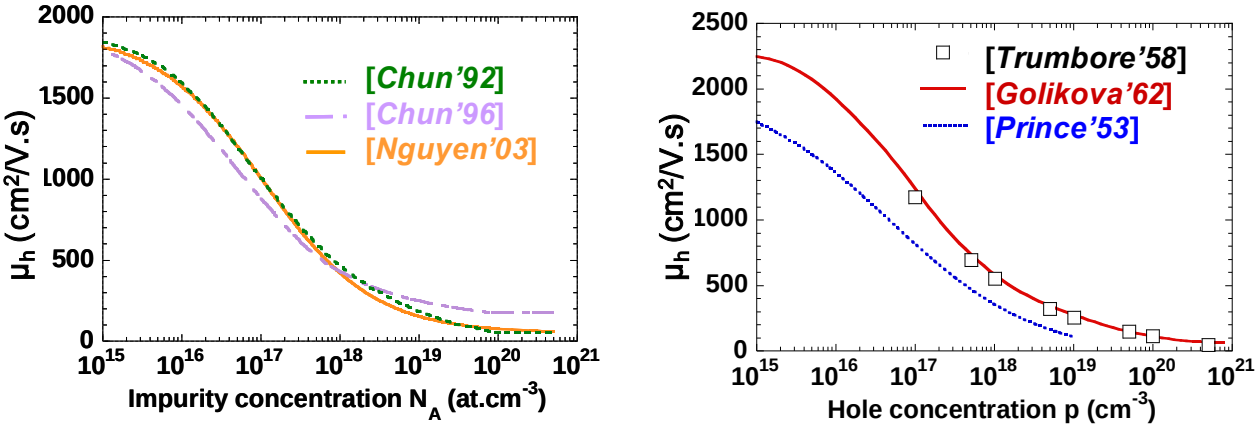


Figure IV-28: Hole mobility versus impurity or hole concentration in Germanium as reported in the literature.

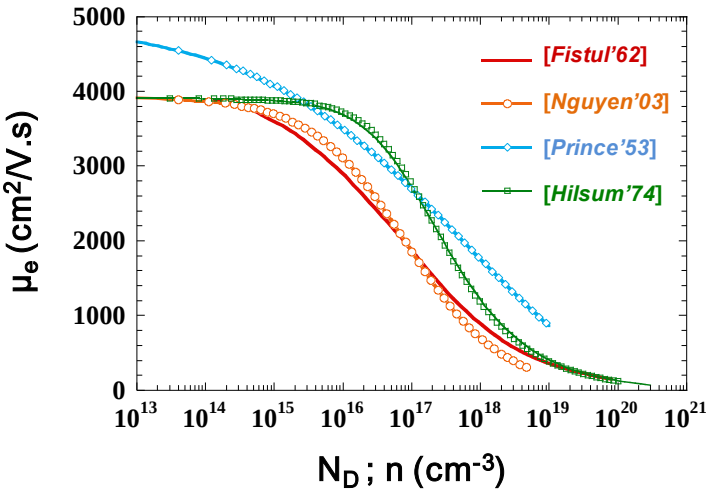


Figure IV-29: Electron mobility versus impurity or electron concentration in Germanium as reported in the literature.

The data is fairly scattered both for hole and electron mobility, which especially inconvenient at high concentrations at which the $\mu.N_{act}$ product becomes large. This can lead to large uncertainties on N_{act} extraction from sheet resistance measurements, as shown on Figure IV-30 (nearly one decade). As in the literature, the reported activation levels associated to a doping process are very often reported without mentioning the mobility model used for SRP calibration; this explains the variety of the SSL values in Table IV-3.

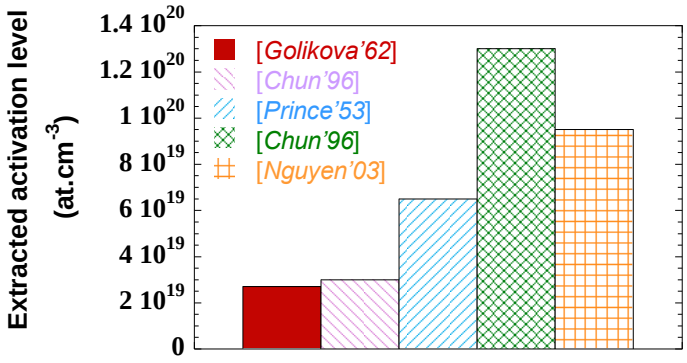


Figure IV-30: Various activation levels extracted from the experimental data on Figure IV-27, according to the chosen mobility models among those shown on Figure IV-28.

In order to choose the model which is the most suitable to N_{act} extraction, the hypotheses on which each of them relies shall be examined and discussed. When impurity atoms are implanted in a semiconductor, a certain amount is substitutionally incorporated in the lattice after annealing, according to the solid solubility of the species. Among these atoms, not all are necessarily available for conduction, due to deionization effects depending on concentration and temperature [*Sah'91*]. For example, in bulk Ge at T=300K and $N_A=10^{19}$ at.cm^{-3}, the ionization degree has been evaluated near 30% of the total impurities concentration ($N_A^-\approx10^{18}$ at.cm^{-3}, [*Chun'92*]), whereas for even higher concentrations (above 10^{20} at.cm^{-3}), no deionization is expected [*Mamontov'95*].

Therefore, whether a model depicts the evolution of hole mobility as a function of the carrier concentration (p), or the total acceptor atoms concentration (N_A), should be made explicit in order to avoid confusion. Not only is N_A in practice superior to p, but the deionized impurities may participate to hole scattering, and thus further limit the mobility at high concentrations.

Prince's mobility curve [*Prince'53*] is derived from experimental minority carriers drift time and resistivity measurements, with subsequent interpretation on the basis of the Conwell-Weisskopf [*Conwell'50*] and Brooks-Herring [*Brooks'51*] formulae for impurity scattering. Although the mobility curve presented by Prince is plotted as a function of N_A, the simplifying hypothesis $N_A \approx N_A^- \approx p$ was done for the calculations.

The data from [*Golikova'62*] and [*Trumbore'58*] correspond to Hall mobility measurements and considerations over the Hall coefficient. A carrier concentration (p) is therefore measured. Golikova *et al.* indicated that for hole concentrations as high as 4×10^{20} at.cm^{-3}, the experimental carrier mobility seemed to be dominated by Coulomb-field scattering induced by ionized impurities, rather than by the local disruptions of the periodic potential. This suggests that the scattering due to neutral impurities was negligible on the studied samples. The obvious difference with the data from [*Prince'53*] (Figure IV-28) might be attributed to the different measurement techniques, probably fewer approximations and a more accurate choice of the effective masses for light and heavy holes.

Concerning the theoretical modelling, Chun and Wang [*Chun'92*] calculated the relaxation times associated with each scattering mechanism to express the hole mobility as a function of acceptor impurities concentration N_A. A couple of years later, Chun corrected the model including screening effects [*Chun'96*]. Nguyen *et al.* [*Nguyen'03*] proposed a full-band Monte Carlo model for $\mu_h(N_A)$, compared with previous experimental data by means of a Caughey-Thomas law fitting. What is surprising concerning the three studies mentioned above, is that the agreement with the experiment is demonstrated by considering Prince's data [*Prince*'53] for low concentrations, and Trumbore's points [*Trumbore'58*] for high concentrations. These are not obviously compatible (cf. methodology and Figure IV-28) and were moreover plotted directly as a function of hole concentration (p), regardless of the ionization degree and neutral impurities scattering.

Under the approximation that $N_A^- \approx p$, the implementation of the model from [*Golikova'62*] for N_{act} extraction is straightforward. Sources of uncertainties subsist, as implanted samples might include a non-negligible amount of boron atoms remaining in interstitial sites of the lattice after annealing, which should be detrimental to the mobility. But adapting models from [*Chun'92*], [*Chun'96*] or [*Nguyen'03*] to the sheet resistance calculation would additionally require knowing the amount of substitutionally incorporated impurities in the Ge lattice and their degree of ionization to deduce the hole concentration, and these factors may vary with each set of implantation dose, energy, annealing temperature, and duration. Furthermore, recent Hall measurements on Germanium heavily doped with Boron [*Mirabella'08*] tend to confirm the validity of [*Golikova'62*] as a relevant reference. For similar reasons transposed to the case of donor doping, [*Fistul'62*] seems the most suitable source for N_{act} extraction on Arsenic or Phosphorus-doped Ge.

State-of-the-art dopant activation in Germanium

It is now clear that the various reported results on solid solubility or dopant electrical activation in Ge should be cautiously considered. For fair comparison, we will only consider in this paragraph the results for which the reference mobility models were specified. As it turns out, these are from [*Golikova'62*] and [*Fistul'62*].

After ion implantation in crystalline Germanium and RTA, the activation levels are usually in the range of $1\text{-}4\times10^{19}$ at.cm^{-3} for (p-type) Boron and (n-type) Arsenic, and slightly higher for (n-type) Phosphorus ($2\text{-}6\times10^{19}$ at.cm^{-3}) [*Satta'06*], [*Koffel'08*], [*Hutin'08-a*]. However, the fast diffusion of Phosphorus and Arsenic for annealing thermal budgets superior to (550°C; 10s) remains a liability for the realization of shallow n^+/p junctions.

These typical values can be raised to higher than 10^{20} at.cm^{-3} using less conventional techniques involving metastable activation processes, such as the Solid-Phase Epitaxial Regrowth (SPER) occurring in preamorphized Ge or GeOI substrates [*Chao'05*], [*Satta'05*]

(PAI). The pre-amporphization implant is carried out before dopant implantation, through a Ge^+ self-implant at high energy.

By combining PAI and excimer laser thermal annealing (LTA) [*Mazzocchi'09-a*], [*Mazzocchi'09*-b], activation levels larger than 10^{20} at.cm^{-3} were obtained for both Boron and Phosphorus, with for the latter an electrical profile abruptness of 8nm/dec. These results are very promising, but PAI on GeOI substrates is difficult to control due to the necessity to keep an amorphous/crystalline interface (α-c) within the thin Ge film.

IV.3.1.e. Germanidation

Due to its limited film roughness and sensitivity to oxidation, as well as its low sheet resistivity, temperature formation and Ge consumption, there is a consensus on NiGe as the best candidate for access germanidation of Ge-based MOSFETs [*Gaudet'06*]. While PdGe and PtGe also feature most of these qualities, the selective removal of unreacted Pt or Pd requires aqua regia solutions. Yet, pure aqua regia etches Ge at nearly 300nm/min, which makes the integration of these silicides particularly dangerous (in case of defects or discontinuous thin metal layers after germanide formation).

The standard process for germanidation starts with cleaning the Ge surface in order to eliminate the native oxide layer or any hypothetic metallic contamination. The metal is then deposited on the Ge surface (by sputtering or thermal evaporation) and annealed to form the germanide alloy NiGe. In the optics of MOSFET device fabrication, the annealing temperature should be compatible with that of silicidation, due to presence of silicided polycrystalline Si on the top of the gate stack [*Carron'07*].

It has been reported that Ni is the mobile species in NiSi formation [*Chu'74*] but also in NiGe [*Marshall'85*]. However, on mesa-isolated GeOI, we observed a huge amount of Ge transport leading to empty out the Source & Drain regions by fast diffusion of germanium in the Ni layer present on the insulating areas [*Nemouchi'08*]. The same phenomenon of overgrowth was observed on STI-isolated bulk Ge [*Brunco'08*]. This is of course highly detrimental to device operation, as it leads to bridging and shorts. It was speculated that Ge diffusion occured at NiGe/SiO_2 interfaces. A process has been developed limiting undesired Ge diffusion, based on the introduction of impurities (*e.g.* oxygen, fluorine) in the Ni films before annealing [*Nemouchi'08*]. In [*Brunco'08*], a two-step RTP before and after selective etching (respectively at 250°C and 330°C) was shown to drastically reduce germanide overgrowth, voiding and defects formation.

Several approaches are described in the literature for the selective removal of Ni with respect to NiGe [*Carron'06*], [*Brunco'08*] including:

- Aqueous acidic or alkaline and strongly oxidant chemistries, where the "Ni versus NiGe" selectivity is mostly based on the higher thickness of NiGe layer compared to

that of deposited Ni layer. In this frame, $NH_4OH/H_2O_2/H_2O$ and HNO_3/H_2O mixtures are used.

- Aqueous acidic and slightly oxidant chemistries which exhibit the highest Ni/NiGe selectivity. $HCl/HF/H_2O$ mixtures are used in this approach.
- Water-free and highly oxidant chemistries (*eg* H_2SO_4 96%) which also exhibit a good (but slightly lower compared to other techniques) "Ni versus NiGe" selectivity.

IV.3.2. **Ge nFETs: challenges and recent developments**

IV.3.2.a. N-type doping

The first obstacle for nFETs fabrication on Ge substrates stems from the low solid solubility, fast diffusion and relatively low activation levels of n-type dopants (As, P) in Ge. These are major setbacks to deal with for implementing shallow junctions with low access resistance and an abrupt lateral profile for extremely scaled MOSFETs. This whole doping problem is actually what initially triggered research on Schottky Ge transistors.

As we know now, Schottky transistors can anyway not be considered as a serious alternative to conventional CMOS without interfacial doping layers. Furthermore, the Fermi-level pinning at the Ge surface is such that a vast majority of the known metals feature a preference for holes injection, which sets the requirements for interfacial n-type doping even higher than those for p-type doping.

Now that activation levels superior to 10^{20}at.cm^{-3} and decent profile abruptness have been demonstrated, the difficulties seem to have been partially overcome. However, the processes involved (PAI, LTA) are not particularly simple to implement in a full transistor process flow, especially on thin films. In addition to this, the early Ge nFETs demonstrators suffered from degraded characteristics which could not owe solely to doping issues.

IV.3.2.b. Inversion layer and threshold voltage

In spite of a supposedly larger electron mobility than in Si, the first Ge-channel nMOSFETs were plagued by surprisingly low ON-State characteristics [*Chui'03-b*], [*Shang'04*], [*Whang'04*], when not entirely nonfunctional [*Ritenour'06*]. This remained a mystery for some time, until it was argued in [*Dimoulas'06*] that the phenomenon of Fermi-level pinning to a charge neutrality level close to the Valence Band at Ge surfaces might very well be responsible.

IV.3.2.b.i. Intrinsic surface states in Ge free surfaces

We have seen in Chapter II that Metal/Ge interfaces exhibit a strong pinning factor to an energy level E_{cnl} located at less than 0.1eV above the VB. This is due to the asymmetry of the interface states originating from the CB and the VB, which locates the branching point (energy at which both densities are equal) in the lowermost part of the energy bandgap. However, we evoked in Chapter II the case of metal/semiconductor contacts where MIGS (extrinsic surface states defined as a combination of VB and CB states) are believed to prevail, without discussing in details the case of a free surface for which E_{cnl} is determined by (intrinsic) native defects and dangling bonds (DBs). Yet, a good reason to do so is to validate the role of Fermi-level pinning at the Ge surface in MOS structures (*a priori* no MIGS), under the assumption that the insulating layer leaves most of the native defects unpassivated.

Recent experimental SRP measurements on Ge p^+/n junctions [*Clarysse'06*] have been hinting towards the fact that Ge surfaces tend to be p-type regardless of the bulk conductivity. It was shown [*Chagarov'08*] by *ab initio* calculations and surface tunneling microscopy that in presence of small amounts of oxygen atoms, a variety of defects formed on Ge surfaces among which dangling bonds, bond distortions, Ge atoms displacement and Ge adatoms formation. The dangling bonds are most likely to contribute to electrically charged surface states. The defect levels of the charged DBs in Ge were determined through hybrid density functionals [*Broqvist'08*]. According to this study, the peak density of charged acceptor DB states is located at E_V+0.05eV, whereas charged donor DB states peak at E_V+0.11eV, implying that the charge transition level is somewhere in between. The definition of this charge transition level is equivalent to that of E_{cnl} in that the net surface charge is negative when states of higher energies are occupied (and positive if it lies above the level up to which surface states are filled).

Therefore, the charge neutrality level predicted for Ge free surfaces from the analysis of charged DB states is, as the MIGS theory indicates for metal/Ge contacts, located very close to the VB (~0.09eV). As a consequence, in first approximation, Fermi-level pinning to E_{cnl}~E_V+0.09eV can be expected as well in MOS structures.

IV.3.2.b.ii. Consequences for MOS structures under positive gate bias

Figure IV-31 shows a diagram of the "Ge side" of a MOS structure (ignoring the presence of the insulator). When no bias is applied on the gate, the interface states are filled up to E_F which coincides with E_{cnl}, ensuring the neutrality of the surface. Upon application of a positive Gate bias, as E_F is driven away from E_{cnl}, an excess of filled acceptor-like CB interface states induces a net negative surface charge, which creates a scarcity of electrons in the vicinity of the surface.

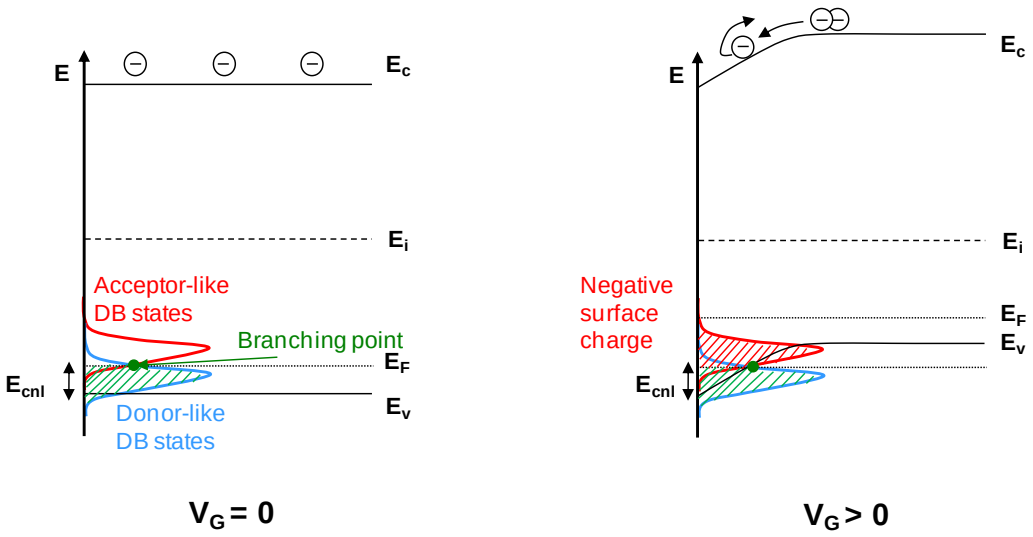


Figure IV-31: Energy band diagrams of the semiconductor side of a p-Ge MOS structure (E_F chosen so that V_{fb}=0V for the sake of clarity). The densities of CB and VB interface states are schematically represented (arbitrary scale) to show the branching point from which the charge neutrality level E_{cnl} is derived. Left: at V_G=0V - Right: upon application of a positive Gate bias V_G>0V (Figures adapted from [Dimoulas'06], [Tsipas'09]).

The larger E_F-E_{cnl}, the larger the number of unpassivated filled acceptor-like states (hence the negative charge) and the stronger this effect becomes. Because E_{cnl} is especially low in Ge, it is relatively easy to trigger it by applying a positive V_G. The consequence for nFETs is that this effect may screen the Gate potential and counteract the building up of an n-type inversion layer, as the surface states remain of p-type (acceptor). Conversely, the p-type inversion is facilitated in pFETs, which also explains the shifting of V_{th} towards positive values observed in Ge pFETs (treated in IV.3.3.).

It was in fact quantitatively confirmed by modelling [*Tsipas'09*], [*Dimoulas'09*] that for the usually measured D_{it} values (10^{12}-10^{13} $eV^{-1}.cm^{-2}$), lightly doped n-type Ge surfaces (N_D<10^{17} $at.cm^{-3}$) were already in weak or even strong inversion at V_G=0V. To compare to the Si case, even for D_{it}=5×10^{13} $eV^{-1}.cm^{-2}$ and N_D=10^{14} $at.cm^{-3}$, the surface is in depletion at zero bias. Similarly, the Fermi-level pinning is found to be responsible for positive V_{th} in Ge pMOSFETs for lightly-doped n-Ge (N_D<$10^{16}$$at.cm^{-3}$) and moderately high D_{it}, as experimentally observed (cf. IV.3.3.).

To conclude on Ge nFETs, the device performance is limited due intrinsic Ge surface properties. The net negative surface charge appearing at positive V_G biases "delays" the surface inversion. Additionally, it may induce excess Coulomb scattering, hence limiting the electron mobility in the channel [*Kuzum'07*].

There are two ways to solve this issue. Either the distance between E_F and E_{cnl} should be reduced as much as possible, or the surface states density should be drastically reduced. The first solution implies increasing the p-type channel doping, which is hardly acceptable in

terms of scalability, variability at small gate lengths, and with regards to the channel mobility. In consequence, optimizing the surface states passivation through gate stack engineering seems like the most critical (and relevant) challenge in order to fabricate functional, performant Ge nFETs.

IV.3.2.c. Recent progress

Over the last two years, the demonstration of high mobility Ge nFETs by improved surface passivation has been a hot topic. In [*Lee'09-b*] and [*Nishimura'10*], GeO_2 was formed by a two step process consisting in high-pressure oxidation (HPO: 550°C, 15 min, 70 atm O_2) and, subsequently, low temperature oxygen annealing (LOA, 400°C, 30min, 1 atm O_2). The resulting mid-gap D_{it} is found to be in the range of 10^{11} $eV^{-1}.cm^{-2}$, and the inversion layer mobility on Ge (111) surfaces exceeds the Si universal electron mobility [*Takagi'94-a&b*] ([*Lee'09-b*]: peak at 1100 $cm^2.V^{-1}.s^{-1}$; [*Nishimura'10*]: peak at 1480 $cm^2.V^{-1}.s^{-1}$). The obtained Ge(100) mobility is roughly equivalent to the Si universality. Similarly, after performing ozone oxidation at 400°C, GeO_2 passivation in [*Kuzum'09*] results in a ×1.5 electron mobility enhancement on Ge(111) with respect to the Si universal electron mobility.

The efficiency of this pure oxide interlayer (OIL) passivation approach is based on low temperature processing. As a consequence, a gate-last approach was used in [*Lee'09-b*] and [*Nishimura'10*]. The dopants were activated at only 350°C in [*Kuzum'09*], resulting in high access resistance (the mobility was therefore extracted on gate Hall structures to eliminate R_{SD}).

While it was shown in [*Nishimura'10*] that thin GeO_2 IL can be combined with high-k (Y_2O_3) with no interface degradation, a certain skepticism subsists concerning the scalability of GeO_2 interlayers [*Caymax'09-b*], [*Maeda'10*]. The main concern expressed in [*Caymax'09-b*] is that the relative amount of GeO_x sub-oxides will increase with EOT scaling. In fact, the only sub-micron Ge nFETs reported so far to our knowledge (L_g=0.75µm) with GeO_2 interlayer and high-k dielectric for an EOT of 1.25nm are reported in the same study, and exhibit a relatively poor mobility of 240$cm^2.V^{-1}.s^{-1}$ in spite of mid-gap D_{it} in the low 10^{11} $eV^{-1}.cm^{-2}$. In [*Maeda'10*], an oxygen-free nitride interlayer (NIL) is topped with HfN and HfO_2 (D_{it}~5×10^{11} $eV^{-1}.cm^{-2}$ - peak mobility: 870 $cm^2.V^{-1}.s^{-1}$ – EOT: 5.6nm).

We shall also recall that these OIL, NIL, low (~10^{11} $eV^{-1}.cm^{-2}$) D_{it} values and peak mobility values above Si universality are not exactly new (cf. IV.1.1.c. : [*Rosenberg'83*], [*Rosenberg'88*]). Nevertheless, there is currently an undeniable regain of activity to fabricate scaled Ge nFETs, a goal which had been partially abandoned so far. Indeed, the large majority of studies focused on the realization of Ge pFETs, which will be the subject of next section.

IV.3.3. **Focus on the GeOI pFET**

This section will be centered on pFET devices with a pure Ge channel. In particular, the reference case of study will be the pFET on GeOI substrates so as to highlight the results obtained during this thesis, although "bulk-like" Ge-On-Si devices will be occasionally evoked through benchmarking.

IV.3.3.a. pFETs on Smart Cut™ substrates

Over the last three years, several demonstrations of deep sub-micron GeOI pFETs were accomplished by Leti [*Le Royer'07*], [*Pouydebasque'08*], [*Romanjek'08-a*], [*Le Royer'09*]. Transistors as short as 70nm gate length (Figure IV-32) were fabricated from Smart Cut™ substrates [*Romanjek'08-a*], which was then close to the record for Ge-channel devices (considering bulk or bulk-like Ge pFETs with L_G=65nm [*Mitard'08*] and L_G=60nm [*Yamamoto'07*] which had been published shortly before by IMEC and MIRAI, respectively).

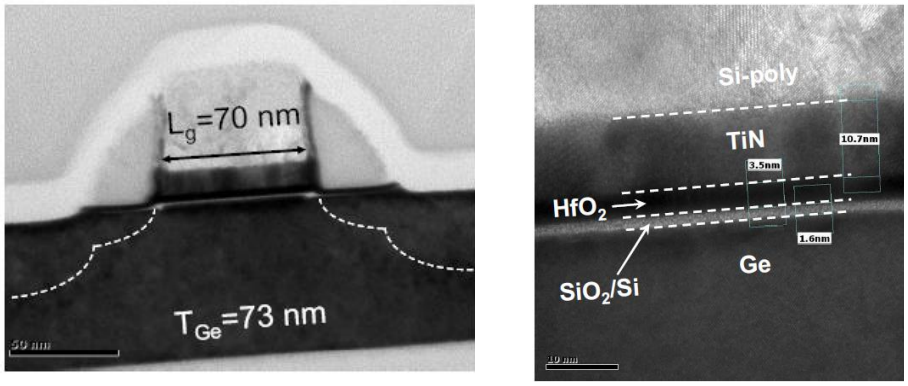


Figure IV-32: X-TEM micrograph of a 70nm gate-length pMOSFET on Smart Cut™ GeOI, and zoom on the gate stack [Romanjek'08-a] (pictures: R. Truche).

In the following, we will expose the conclusions to which this study led in terms of optimization challenges for scaled GeOI pFETs, supported by electrical characterization and TCAD simulation.

IV.3.3.a.i. Back-interface parasitic conduction

One of the critical issues affecting GeOI devices performance [*Le Royer'07*] is the parasitic conduction occurring at the Ge/BOX interface, for exactly the same reasons as mentioned in paragraph IV.3.2.b. As a result of an insufficient quality of the Ge/SiO_2 interface, unpassivated acceptor states at the bottom of the Ge film provoke a p-type inversion at zero back-gate bias (V_{bg}: the "back-gate" electrode is formed by the Si substrate and the

gate dielectric is the BOX). A parasitic pMOSFET of positive threshold voltage coexists with the actual "front-gate" pMOSFET, and degrades its characteristics in terms of threshold voltage, subthreshold swing, and leakage current. This effect has been extensively studied in [*Romanjek'08-b*], [*Van Den Daele'09*] and [*Van Den Daele'10-a*].

It can be counteracted by:

- Applying a back-gate bias (the amplitude of which depends on the BOX thickness)
- Increasing the control of the Front-Gate over the back-interface by reducing the Ge thickness
- Performing an n-type implant in the Ge film (counterdoping)

This last solution is the simplest to implement, as one can easily imagine that nobody wants a device requiring a +60V back-bias for correct operation, and considering that the GeOI Smart Cut™ process was, to date, never mastered to the point of obtaining a uniform 10nm thickness on 200mm wafers. However, introducing additional dopant atoms in the channel inevitably increases the scattering, hinders the mobility and results in a drive current loss. Nonetheless, the gain in OFF-State current can be spectacular, as shown on Figure IV-33.

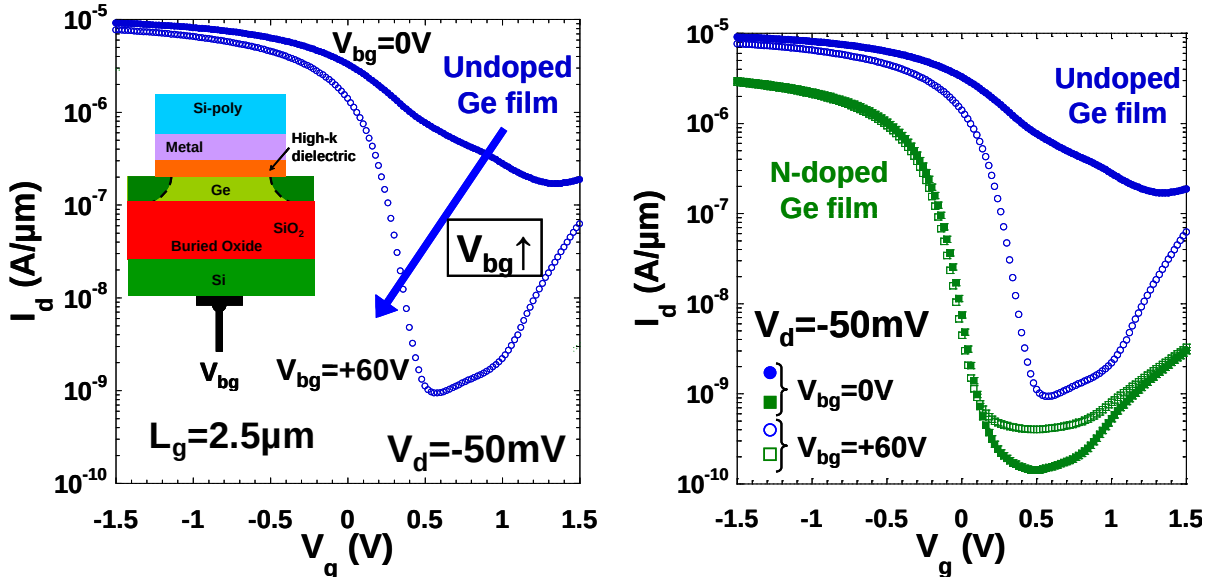


Figure IV-33: I_D-V_{GS} characteristics of 2.5µm long GeOI pFETs at V_{DS}=-50mV. [Romanjek'08-a] Left: In the case of an undoped channel, influence of a +60V back-gate bias V_{bg} on the parasitic conduction at the Ge/BOX interface. Right: Influence of n-type channel doping on the characteristics at V_{bg}=0V and V_{bg}=+60V [Romanjek'08-a].

It is noteworthy that the threshold voltage of pFETs becomes negative, suggesting that the issue of front-interface inversion at zero-bias is equally solved.

IV.3.3.a.ii. Short Channel Effects

Given the film thickness (~73nm, cf. Figure IV-32), the Short Channel Effects are expected to be relatively important for gate lengths inferior to 300nm. A well-known way to regain electrostatic control from the gate over the channel is to add n-type halos (or pockets), as successfully implemented earlier in bulk-like Ge devices [*Nicholas'07*] (and long before that in Si devices).

The Short Channel Effects can be modeled in terms of charge sharing [*Yau'74*]. A part of the channel depletion charge becomes increasingly controlled by the Source and Drain with decreasing gate lengths, thus reducing the depletion charge associated to the gate (Q_{dep}):

$$Q_{dep} = q \cdot N_{ch} \cdot T_{dep} = \pm\sqrt{2 \cdot \varepsilon_S \cdot q \cdot N_{ch} \cdot \left(2 \cdot \phi_f - V_{fb}\right)}$$

(eq. IV-12)

$$\phi_f = \pm \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_{ch}}{n_i}\right)$$

(eq. IV-13)

As the threshold voltage value is in direct relation with Q_{dep}/C_{ox}, a loss of Q_{dep} results in a diminution (for nFETs) or an increase (for pFETs) of V_{th}. In principle, the effect of pockets implantation is to raise the dopant concentration in the channel (N_{ch}), therefore increasing Q_{dep} and restoring the primacy of the gate in controlling the potential in the channel. Moreover, the electrical gate length is slightly augmented, as the pockets and LDD doping are of opposite types.

Once again, the improvement in terms of OFF-State behavior on the short-channels GeOI pFETs is dramatic, as shown in Figure IV-34. However, an additional loss of mobility (and therefore drive current) is observed.

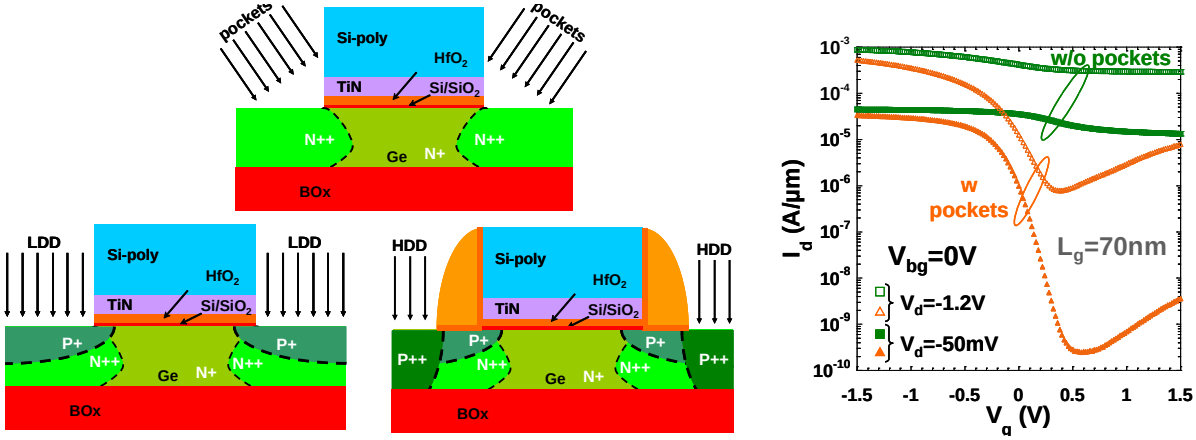


Figure IV-34: I_D-V_{GS} characteristic of 70nm long GeOI pFETs at V_{DS}=-50mV and V_{DS}=-1.2V. The channel is counterdoped and no back-gate bias is applied (V_{bg}=0V). The influence of pockets implantation is shown through the control of Short Channel Effects (V_{th} roll-off, subthreshold swing degradation) and reduction of junction leakage [Romanjek'08-a].

Figure IV-35 shows how pockets help maintaining the threshold voltage and substhreshold at short gate lengths. Yet, we can notice that the subthreshold swing still saturates at 100mV/dec even on long-channel devices, which is substantially higher than the ideal value of 60mV/dec on Fully-Depleted thin films. This is a consequence of the significant front-gate interface states density, and to a lesser extent of the back-gate D_{it} as well (given that coupling occurs between both interfaces). $D_{it}^{top}=7\times10^{12}$ $eV^{-1}.cm^{-2}$ and $D_{it}^{bottom}=2\times10^{12}$ $eV^{-1}.cm^{-2}$ were indeed extracted on the same devices using Lim&Fossum's model [*Lim'83*] in [*Romanjek'08-b*].

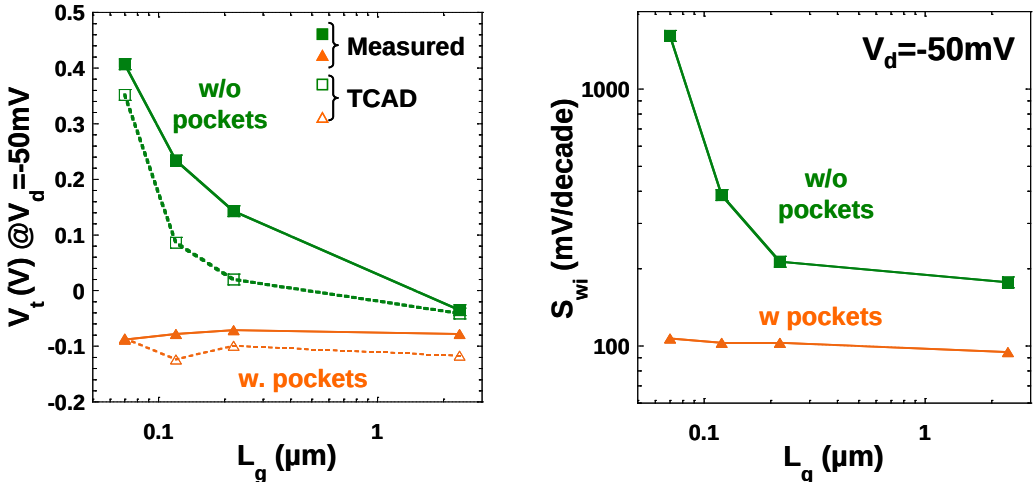


Figure IV-35: Left: Linear regime V_{th} versus gate length with and without pockets implantation (solid lines: measurement; dashed lines: TCAD simulation). Right: Subthreshold swing versus gate length with and without pockets [Romanjek'08-a].

The attenuation of the back-channel conduction and SCE is a priority to obtain decent OFF-State characteristics on relatively short pFETs. We will now see how the chosen technological solutions can affect the ON-State.

IV.3.3.a.iii. ON-State

In the following, the ON-State current is defined as I_D at $|V_{GS}-V_{th}|=2V_{dd}/3$ (with $V_{GS}<V_{th}$ for a pFET). This "V_{th}-relative" definition, as opposed to an "absolute" measurement at $V_{GS}=V_{dd}$ is suggested as a means to eliminate the influence of the (not necessarily yet optimized) V_{th} value from considerations over the performance of different (and not necessarily yet mature) technologies [*Chau'05*]. Similarly, I_{OFF} can be defined as I_D at $|V_{GS}-V_{th}|=V_{dd}/3$ (with $V_{GS}>V_{th}$ for a pFET). The low-field mobility μ_0 is extracted by short-channel C-V split [*Romanjek'04*] compared to the Y-function method [*Ghibaudo'88*].

Whereas low-field mobilities of ~250 $cm^2.V^{-1}.s^{-1}$ have been extracted on similar devices with undoped GeOI channel [*Le Royer'07*], [*Pouydebasque'08*], the channel and

pocket implants have the effect of reducing μ_0 down to 110 $cm^2.V^{-1}.s^{-1}$ at 300K (slightly more than a factor 2), which naturally impacts the ON-State current (Figure IV-36). No increase at lower temperatures is observed, which is the signature of strong Coulomb scattering.

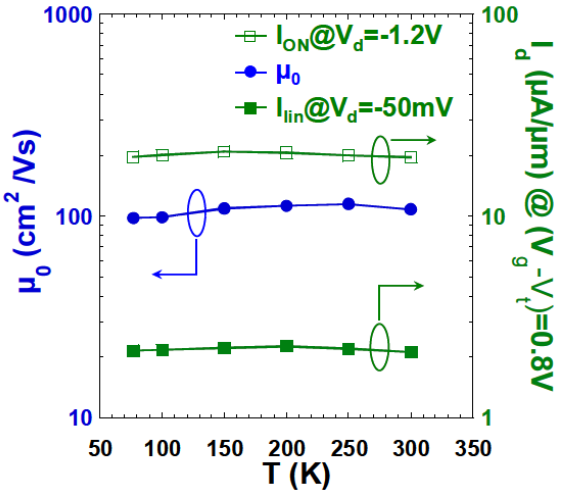


Figure IV-36: Low-field mobility (left axis) and ON-State Drain current (right axis) as a function of temperature in a 2.5µm long GeOI pFET with Ge n-type counterdoping [Romanjek'08-a].

Besides, the drive current is limited at short gate lengths by the access resistance. Given that the pFETs Source and Drain in [*Romanjek'08-a*] are not germanided, R_{access} is relatively high (870 Ω.µm). This can be visualized by a saturation of the I_{ON} versus L_g plot, straying from the $1/L_g$ slope (log-log scale) on long channel devices (Figure IV-37).

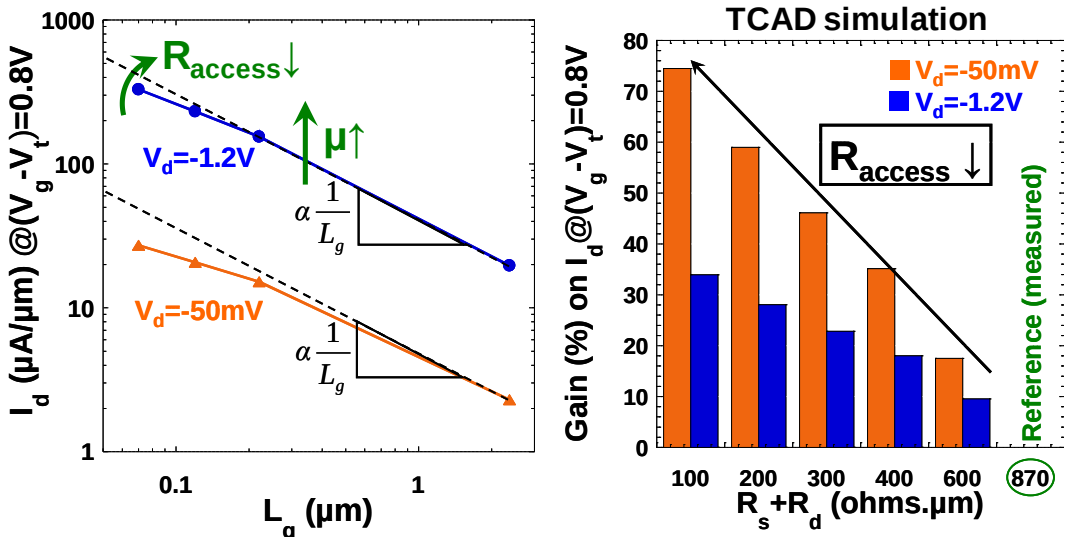


Figure IV-37: Left: ON-state Drain current in linear and saturated regimes versus gate length. Right: Simulated gain on the ON-State current (L_g=70nm) upon reduction of the measured R_{SD} (870 Ω.µm) down to state-of-the-art values which could be reached by access germanidation [Romanjek'08-a].

IV.3.3.a.iv. OFF-State

Regardless of the parasitic conduction and SCE, the leakage current remains very high in GeOI pFETs (I_{OFF}=1µA/µm at V_{DS}=-1.2V) with respect to the SOI counterparts. This is expected (cf. IV.1.2.b.), but the nature of this leakage can be evidenced by low temperature measurements (Figure IV-37).

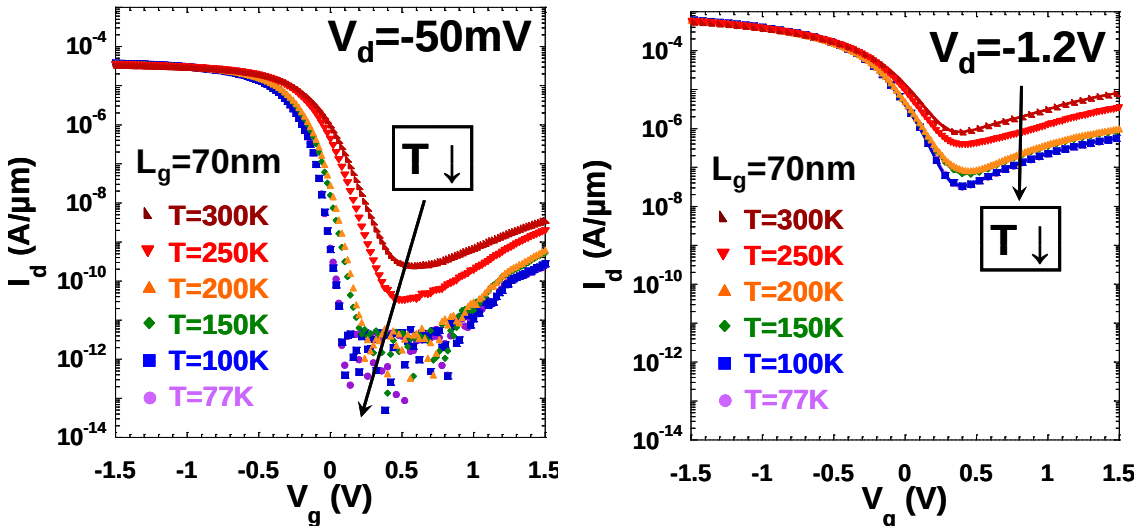


Figure IV-38: Left: I_D-V_{GS} characteristics of a 70nm long GeOI pFET at low (left) and high (right) V_{DS} for various temperatures ranging from 77K to 300K [Romanjek'08-a].

At V_{DS}=-50mV, the leakage current is strongly reduced (almost three decades from 300K to 77K), suggesting the predominance of a combination of Shockley-Read-Hall (SRH) recombination and Trap-Assisted Tunneling (TAT), which are thermally activated processes. At V_{DS}=-1.2V, however, the temperature reduction has less influence, suggesting that Band To Band Tunneling (BTBT) prevails, as it is a mostly temperature-independent process typically occurring at high V_{DS}.

Further reduction of the leakage current can be carried out by reducing the supply voltage and improving the crystal defectivity (Figure IV-39).

Since BTBT has a strong influence on leakage at high V_{DS}, reducing the electric field at the Drain junction is particularly efficient. This can be done directly by scaling V_{dd}, but also by optimizing the lateral doping profiles at the junction (*ie* decreasing the built-in electric field).

I_{OFF} could also be further improved by reducing the trap density which is responsible for a short carrier lifetime and hence high SRH and TAT rates. Note that the saturation in Figure IV-39 for τ > 10ns owes to the definition of I_{OFF}, which corresponds then to V_{GS} values in the subthreshold region (a steeper subthreshold slope would result in a lower saturation I_{OFF}).

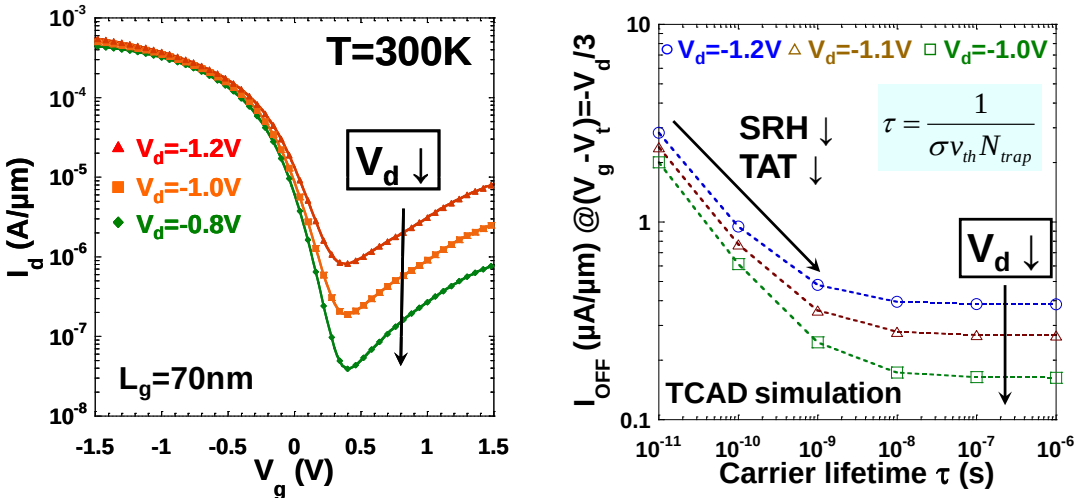


Figure IV-39: Left: I_D-V_{GS} characteristics of a 70nm long GeOI pFET in saturated regime for various supply voltages. Right: TCAD simulated I_{OFF} values in 70nm long devices versus carrier lifetime (itself function of the trap density). The τ value used for fitting the measured I_D-V_{GS} characteristics is500 ps.

IV.3.3.a.v. Synthesis and paths for performance optimization

The factors for ON-State, Subthreshold regime and OFF-State stressed in this paragraph are summarized on Figure IV-40.

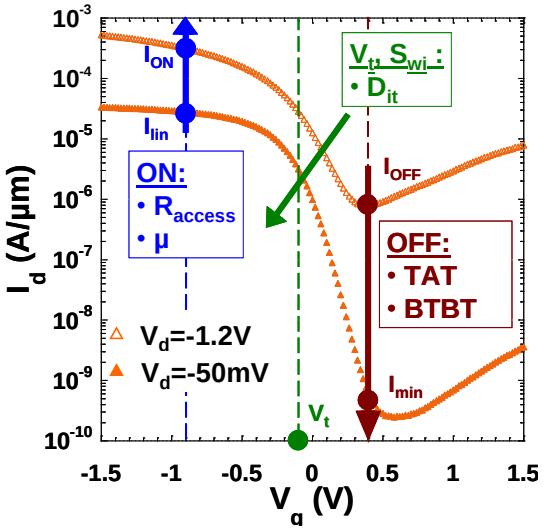


Figure IV-40: Recap of the improvement factors to optimize the electrical behavior of short-channel GeOI pFETs based on the discussion above.

The interface states densities at both Ge interfaces can be related to three major limitations of the GeOI pFETs performance. The most obvious ones are the V_{th} shift and saturation of S_{wi} to non-ideal values. The third link is indirect, yet non-negligible. The parasitic back-channel conduction arises from unpassivated acceptor interface states, and has

to be turned off by means of a channel implant which can significantly degrade the mobility, and subsequently the ON-State current. Therefore, (top and bottom) D_{it} reduction is arguably the most critical obstacle in the way of device optimization.

In addition, R_{access} diminution through germanidation also has a significant impact on I_{ON} at short gate lengths (~+30% expected at L_g=70nm, cf. Figure IV-37). Regarding I_{OFF}, BTBT-induced leakage can be reduced through lateral doping profile optimization at the junctions, and SRH/TAT leakage by improving the crystal defectivity.

Finally, thinner Ge films can surely be of interest as the electrostatic control by the front gate over the channel thickness would be improved. This would result in further attenuating the SCE, but also in lessening the importance of back-channel conduction and therefore relax the requirements in terms of channel doping. From this point of view, the Ge enrichment technique is promising as 10nm thick GeOI films with acceptable defectivity have already been demonstrated on 200mm wafers (cf. IV.2.2.b.).

IV.3.3.b. pFETs on Ge substrates obtained by enrichment

In this part, the results published in [*Hutin'10-a*] and [*Hutin'10-b*] will be presented, demonstrating pFETs processed on GeOI obtained by Ge epitaxy on enriched SiGeOI substrates (x_{Ge}~95%). The MOSFET process shares a certain number of similarities with that of [*Romanjek'08-a*], but the differences between the resulting devices are the following:

- Thinner, uniform substrates (T_{Ge}=25nm).
- The use of E-beam lithography allowed patterning down to a record of 30nm Gate length.
- The V_{th} value set at roughly -0.5V on long-channel devices (instead of -0.15V) enabled to advantageously consider "absolute" I_{ON} and I_{OFF} (*ie* I_D at respectively V_{GS}=V_{DD} and V_{GS}=0V) for I_{ON}/I_{OFF} benchmarking.

IV.3.3.b.i. Substrates and devices fabrication

Ultra Thin (001)GeOI substrates were fabricated based on the Ge enrichment technique (Figure IV-16, paragraph IV.2.2.b.). The enrichment was pursued until the Ge content reached ~95% for a final thickness of 8nm. Homogenization annealing steps under Ar were used instead of N_2, leading to a 50% decrease of the SiGe layer surface roughness (RMS: 0.375nm with N_2 annealing, 0.193nm with Ar, measured from 5×5µm^2 AFM scans). Figure IV-41 shows the subsequent pFET process flow. After SiO_2 removal, a 20nm thick Ge layer was deposited (by RP-CVD) on the enriched substrates. The overall thermal budget of the subsequent Si-compatible MOSFET process featuring TiN/HfO_2 gate stack with an ultra thin Si passivation layer (1nm at 525°C with SiH_4) did not exceed 600°C.

Channel As implant combined with P pockets were performed in order to control V_{th} and the SCE. Boron was used instead of BF_2 for S/D doping so as to limit defects in the Ge film [*Hellings'09*]. Hybrid Deep Ultra Violet/E-beam lithography enabled the fabrication of devices with L_g=30nm (Figure IV-41). The equivalent oxide thickness (EOT) of the gate stack was measured to be 1.6nm (Figure IV-42).

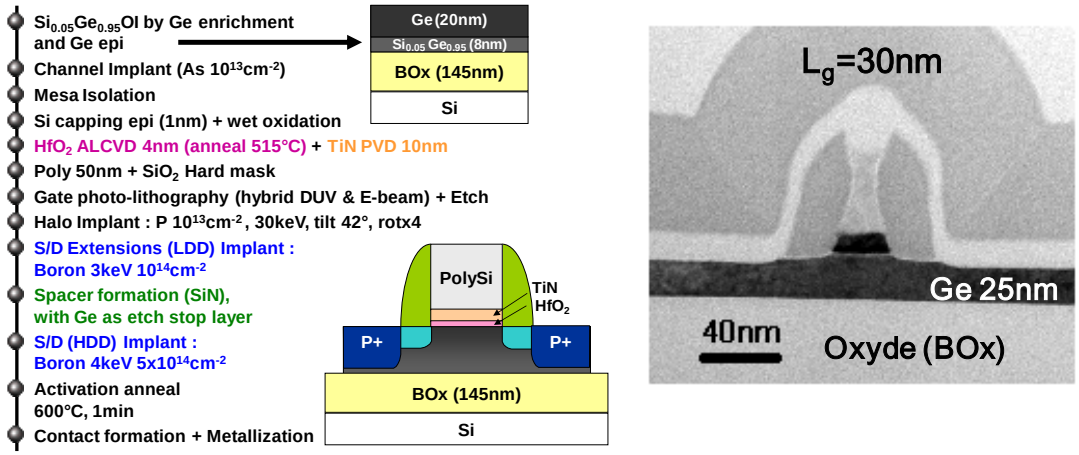


Figure IV-41: Left: Simplified process flow for pFET fabrication – Right: X-TEM image of a GeOI pMOSFET with physical gate length L_g=30nm. The Ge thickness under the gate is 25nm. (picture: D. Lafond)

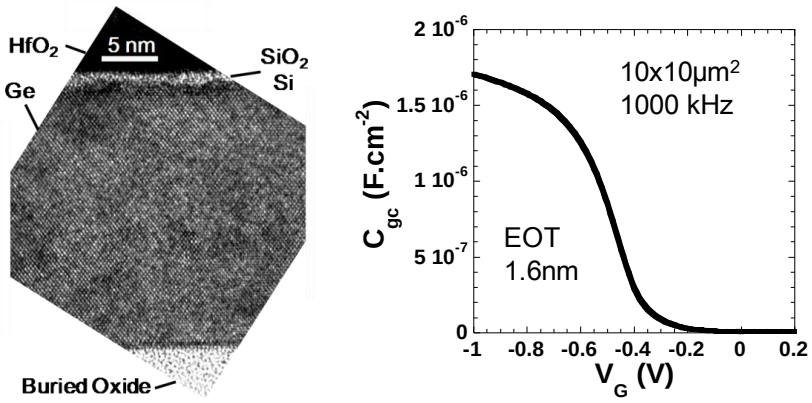


Figure IV-42: Left: X-TEM view of the device in Figure IV-41 zoomed in the vicinity of the gate stack, showing no extended defects in the channel (picture: D. Lafond). Right: C-V characteristics at 1000kHz of a W=L_g=10µm pFET. The extracted EOT is 1.6nm, and the Si cap is not visible on the curve (no double plateau).

IV.3.3.b.ii. Short channel devices

The resulting GeOI pFETs, including short-channel devices, exhibit well-behaved characteristics (Figure IV-43-a) with very low minimum Drain current (100pA/µm at L_g=55nm; V_{DS}=-1V). However, due to the L_g/T_{Ge} ratio reduction, the I_D-V_{GS} characteristics of devices shorter than 55nm show an increasing dependence on back-gate voltage (Figure

IV-43-b), which becomes then necessary to switch off the parasitic conduction at the inverted Ge/BOX interface (V_{BG}=+20V necessary at L_g=30nm).

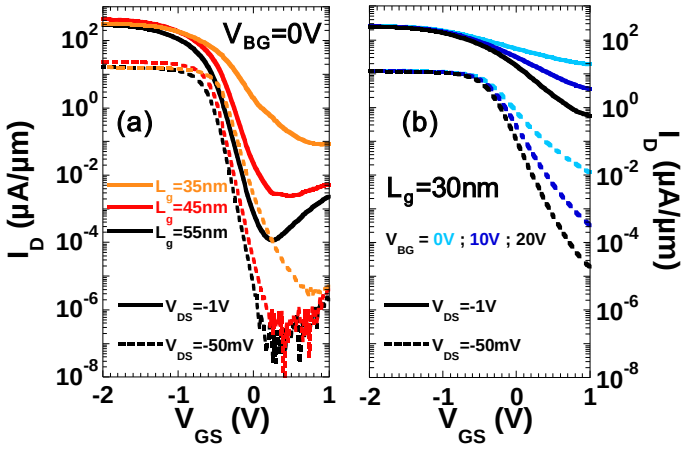


Figure IV-43: (a) I_D-V_{GS} characteristics of GeOI pFETs at low (-50mV) and high (-1V) V_{DS}, for gate lengths of 35, 45 and 55nm. No back gate voltage was applied (V_{BG}=0V). (b) Particular case of a L_g=30nm functional pFET, showing the influence of V_{BG} which improves the characteristics by switching off the back-channel parasitic conduction.

Fairly flat V_{th} and subthreshold swing S_{wi} (resp. -0.5V and 100mV/dec for long channel devices in linear regime) versus L_g are demonstrated (Figure IV-44-a,c). Besides, the Fully-Depleted GeOI devices display low Drain Induced Barrier Lowering (DIBL: 140mV/V for L_g=55nm) mostly due to the low Ge thickness, outperforming Ge state-of-art [*Yamamoto'07*], [*Mitard'08*], [*Romanjek'08-a*] (Figure IV-44-b).

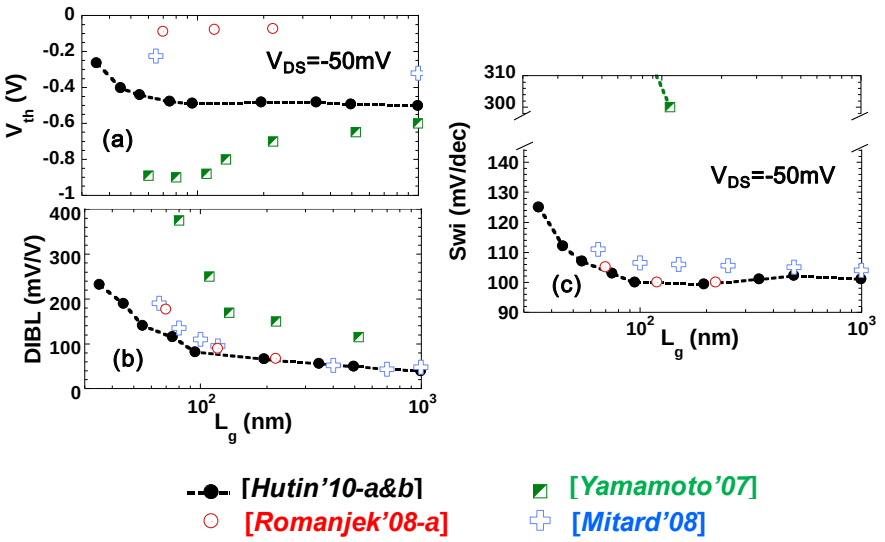


Figure IV-44: Benchmarking of the evolution with the physical gate length of: (a) the threshold voltage (V_{DS}=-50mV), (b) Drain Induced Barrier Lowering, (c) subthreshold swing (V_{DS}=-50mV).

IV.3.3.b.iii. I_{ON}/I_{OFF} ratio

Several issues had been limiting the I_{ON}/I_{OFF} ratio of Ge pFETs. The structures in [*Yamamoto'07*] suffered from high leakage, subthreshold swing and DIBL. In the case of [*Mitard'08*], although the Source current I_S OFF-State are comparable to the I_D characteristics Figure IV-43-a, a high leakage current towards the bulk across the Drain junction brought I_{OFF} four decades higher. This leakage is expected to be reduced by decreasing the flat-bed Drain area [*Hellings'09*]. The devices in [*Romanjek'08-a*] did not suffer from bulk leakage, being on GeOI, but rather from relatively thick channel and probably un-optimized junctions. This assumption is based on the evaluation by TCAD of the carrier lifetimes (cf. defects near the junction due to BF_2 implants) and the importance of TAT and BTBT in the leakage at high V_{DS}. Ge channel Gate-All-Around transistors in [*Feng'08*] demonstrated a large I_{ON}/I_{OFF} ratio (no bulk leakage, optimal electrostatic control), but only at a 1.3µm gate length.

If I_{ON} and I_{OFF} are defined relative to the threshold voltage ($I_{ONr}=I_D$ @ $V_{GS}=V_{th}-2V_{DD}/3$; $I_{OFFr}=I_D$ @ $V_{GS}=V_{th}+V_{DD}/3$), then the pFETs in [*Hutin'10-a&b*] exhibit an I_{ONr}/I_{OFFr} ratio nearly as high as in [*Feng'08*] (5-6 decades), but sustained to much shorter gate lengths (Figure IV-45-a). Another advantage of these devices is the fact that the threshold voltage is set for long-channel devices to a relatively high negative value (~-0.5V, cf. Figure IV-44). As a consequence, an absolute evaluation of I_{ON} and I_{OFF} ($I_{ON}=I_D$ @ $V_{GS}=V_{DD}$; $I_{OFF}=I_D$ @ $V_{GS}=0$), closer to what would happen in normal circuit operation leads to a significantly higher ratio with respect to other studies (Figure IV-45-b).

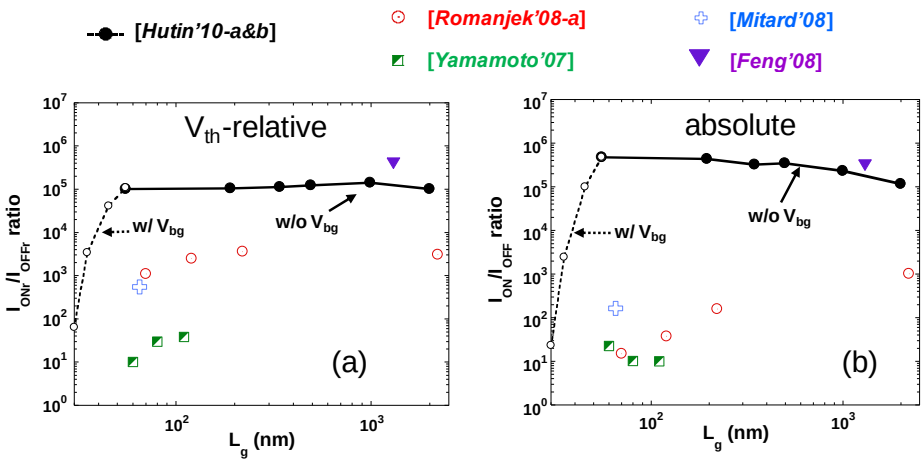


Figure IV-45: (a) I_{ONr}/I_{OFFr} (V_{th}-relative) and (b) absolute I_{ON}/I_{OFF} ratios versus gate length. In both cases, V_{DD}=-1V. For [Hutin'10-a&b] the ratios corresponding to gate lengths shorter than 55nm are corrected using a back-gate bias, in order to eliminate the contribution of parasitic conduction at the Ge/BOX interface.

In each case, this owes largely to the improved OFF-State, as the ON-State remains perfectible, as we will see in the next two paragraphs.

IV.3.3.b.iv. OFF-State improvement

The temperature dependence of leakage current density a low transverse field (V_{DS}=-50mV) was also studied (Figure IV-46-a). The slope of the Arrhenius plot (0.33eV) corresponds to half the Ge energy bandgap E_g^{Ge}. This is consistent with the theory for dominant generation currents in reverse-biased Ge junctions (proportional to n_i the intrinsic carrier concentration (eq. IV-2), which is an exponential function of $E_g^{Ge}/2kT$ (eq. IV-1)). The significant downward shift of the leakage current indicates a much increased minority carriers lifetime, confirming the improved quality of the Ge film compared to previous work based on similarly fabricated GeOI substrates [*Le Royer'08*]. Figure IV-46-b shows the influence of V_{DS} on I_{leak} (defined here as I_D measured at $V_{GS}=V_{th}+1V$), emphasizing Drain Off-state currents four decades lower compared to data in the literature. Besides, the slope versus V_{DS} is smaller compared to previous studies [*Romanjek'08-a*], [*Bedell'08*], indicating a reduced influence of tunneling-related currents (TAT, BTBT).

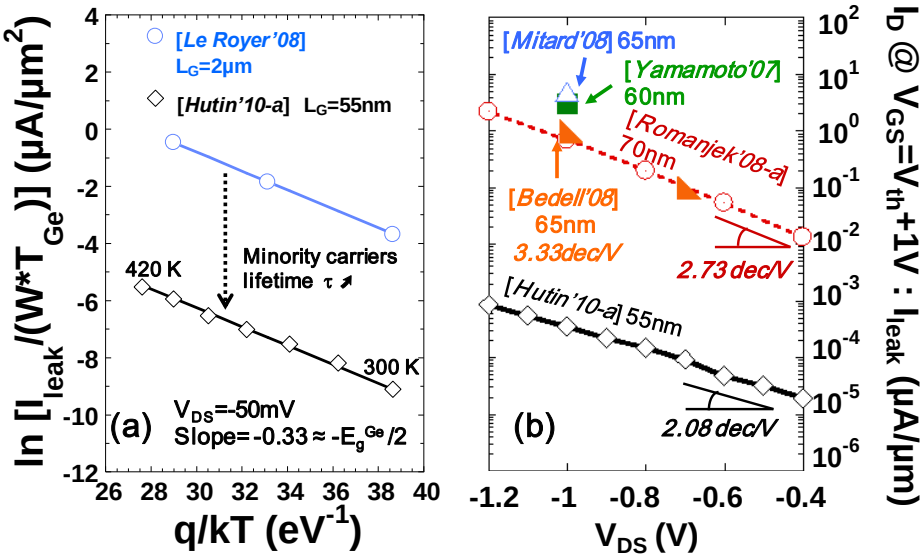


Figure IV-46: (a) Arrhenius plot of the Drain leakage current density at $V_{GS}=V_{th}+1V$ and low V_{DS}=-50mV for [Hutin'10-a] (diamonds) and previous work with GeOI obtained by Ge enrichment ([Le Royer'08], circles). The solid lines correspond to an activation energy of 0.33eV, which is half the Ge bandgap. (b) Evolution of leakage current I_{leak} (defined as $I_D@V_{GS}=V_{th}+1V$) as a function of V_{DS}. The smaller slope indicates reduced field-effect-related leakage (Trap Assisted Tunneling, Band To Band Tunneling) compared to [Romanjek'08-a], [Bedell'08].

IV.3.3.b.v. ON-State study and prospects

The structure of the fabricated transistors led to large access resistance (~2kΩ.µm) mainly due to the absence of raised S/D and germanide. For L_g=45nm, with a prospective

R_{access}=200Ω.µm (Figure IV-47-a), a +300% increase is expected for I_D in linear regime, while I_{ON} would shift from 260µA/µm to 460µA/µm (+77%). Using channel doping for V_{th} adjustment is at the cost of a lower mobility (~ -50%, Figure IV-47-b). In addition, a low T_{Ge} (in order to achieve electrostatic control at short L_g) tends to limit the mobility [*Nguyen'07*]. Nevertheless, larger mobility values compared to bulk Si are still obtained in narrow devices. The increase in mobility at narrow channel widths was already observed on Smart Cut™ GeOI [*Pouydebasque'09*]. It was speculated that the cause is that reducing W increases the fraction of conduction on the (110) mesa sidewalls, which would present improved mobility characteristics.

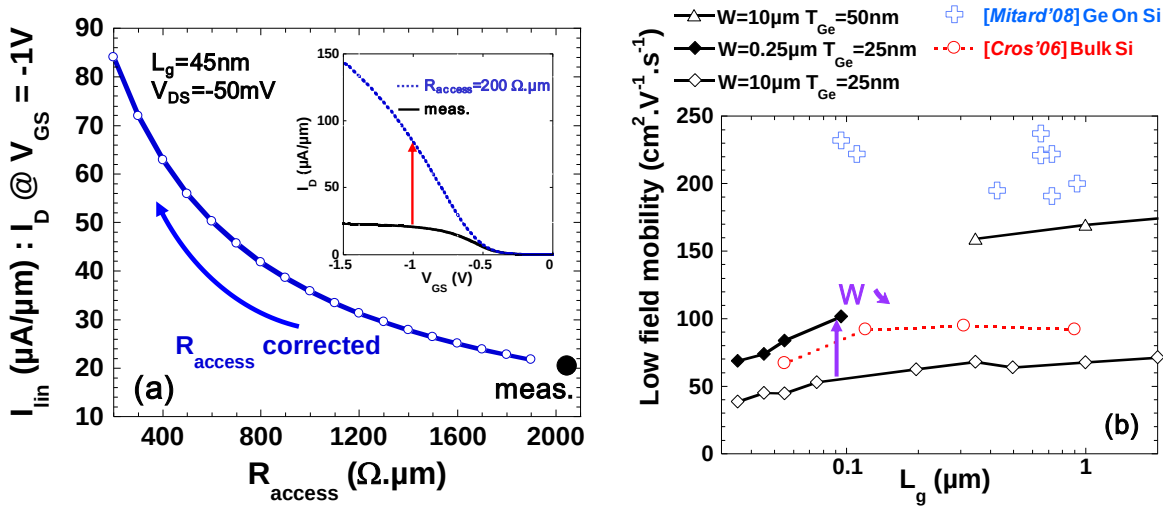


Figure IV-47: Left: I_{lin} (I_D @ V_{GS}=-1V; V_{DS}=-50mV) versus R_{access}. Long contact-to-Gate distance, thick spacers, thin Ge film, absence of raised S/D or germanidation result in high R_{access} limiting the ON-State current. Scaling R_{access} down to a state-of-the-art value of 200Ω.µm would lead to a +300% increase in I_{lin} (at L_g=45nm). Right: Holes low-field mobility versus gate length for the GeOI pFETs from [Hutin'10-a&b], the bulk Si pFETs from [Cros'06] and Ge On Si pFETs from [Mitard'08].

IV.3.3.b.vi. Summary

The I_{ON}/I_{OFF} ratio can be raised raised to more than 5 decades down to 55nm gate length thanks to the combination of a low defectivity near the junctions (B implantation instead of BF_2), a thin Ge layer (Ge enrichment followed by Ge epitaxy), well-controlled V_{th} and SCE (channel, pockets implantations).

The intrinsic gate delay versus I_{OFFr} figure of merit (Figure IV-48) shows an improved trade-off compared to literature due to low I_{OFFr}, in spite of perfectible I_{ON}. Smaller delays can be reached through the implementation of well-known technological modules (raised S/D, germanidation), and gate stack optimization to adjust V_{th} without channel doping.

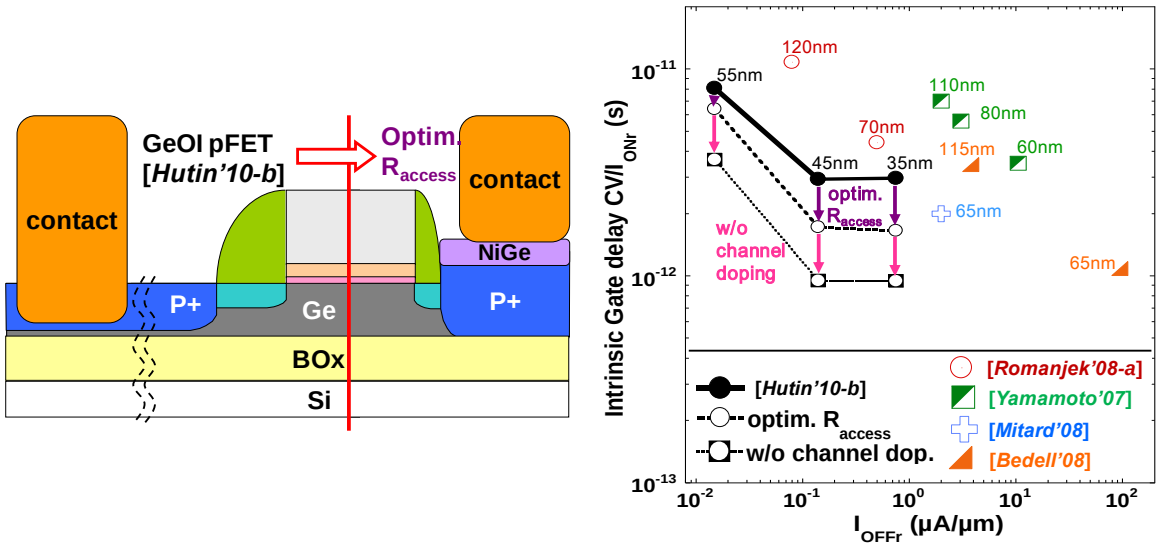


Figure IV-48: Intrinsic gate delay (CV/I_{ONr}) versus I_{OFFr} (ON- and OFF-State currents are set relative to V_{th}). I_{ONr} was defined as $I_D@V_{GS}=V_{th}+2V_{DD}/3$, I_{OFFr} as $I_D@V_{GS}=V_{th}+V_{DD}/3$ (V_{DD}=-1V). The prospective data points for this work with corrected R_{access} and assuming V_{th} adjustment is possible without channel doping (no mobility degradation) are reported on the graph.

IV.3.4. **Status on pure-Ge technology for conventional CMOS**

In paragraph IV.1.2. , we have reviewed a certain number of pros and cons regarding the expected electrical behavior of pure Ge devices, based on theoretical generalities. In section IV.3. , we have seen more specifically how the technological realities could complicate device integration on pure Germanium. Although significant progress has been achieved over the past few years (*eg* in terms of epitaxy, p-type doping, germanidation, gate length and EOT scaling), some of these critical issues remain unsolved, casting doubt over the future of pure-Ge CMOS.

IV.3.4.a. Persistent technological bottlenecks for Ge CMOS

IV.3.4.a.i. N-type doping and junction leakage

- **N-type** doping of Ge by P or As implantation suffers from **low solid solubility** (5-6×10^{19}.cm^{-3}), and **high diffusivities for temperatures as low as 550°C**. This is a significant obstacle for achieving highly-doped, shallow junctions for high performance nFETs.
- The small band gap of Ge leads to junction leakage through **Band-To-Band Tunneling** (BTBT). Unless the supply voltage is reduced to 0.7V and below ($V_{DD}<E_g^{Ge}/q$), this causes high I_{OFF} in Ge devices due to lateral junction leakage as

well as **Gate-Induced Drain Leakage** (GIDL) if the Drain extensions and Gate are overlapped.

IV.3.4.a.ii. Surface passivation

Interface passivation is still a major bottleneck delaying the scaling of Ge devices. Due to the asymmetric distribution of surface states over the band gap of Ge (larger density of CB-derived acceptor surface states), the charge neutrality energy level (located at the cross-over with an equal density of VB-derived donor states) is intrinsically close to the Valence Band, which results in a "p-type" electrical behavior of Ge interfaces.

- The consequences for **nFET** operation are serious, as it becomes more **difficult to create of an inverted n-channel** upon application of a positive Gate bias. Moreover, when functional, the devices exhibit **degraded electron mobility**.
- The consequences for **pFETs** are *a priori* lighter, but still eventually limit the performance. The **$V_{th,p}$ are pulled towards positive values**, which should be compensated for in order to obtain acceptable leakage currents at zero bias. In the case of GeOI, the Ge/BOX back-interface can generate additionally a **parasitic pFET in weak inversion at V_{BG}=0V**. This can be fixed by means of channel doping, but this solution can result in an almost twofold penalty on low-field hole mobility due to higher scattering rates. Finally, high D_{it} at the Ge/high-k interface degrade the subthreshold swing (typically **~100mV/dec instead of 60mV/dec on Fully-Depleted long-channel devices**). This can potentially **invalidate the perspective of scaling the supply voltage** for power consumption reduction, which is often cited as an advantage of high mobility semiconductors.

Si capping is currently the most developed passivation scheme, and has been extensively used in deep sub-micron scaled pMOSFETs fabrication. However, its passivation characteristics are insufficient for nMOSFETs which makes it unsuitable for Ge CMOS. The use GeO_2 looks like a promising alternative, as its passivating power on Ge surfaces is similar to the Si/SiO_2 system. Nevertheless, it is a "difficult" material setting additional constraints in terms of processing due to its limited thermal stability and high water solubility. Furthermore, the scalability of GeO_2 interlayers remains controversial.

IV.3.4.b. « Is it worth it? »

Given that all bottlenecks share the particularity of seeming impossible to overcome until someone proposes a solution, let us optimistically assume that all of the above mentioned issues will eventually be solved. Yet, it would be naïve not to take into account

industrial considerations when evaluating the potential of a given technology, especially in the framework of CMOS device fabrication for advanced nodes.
Caymax *et al.* recently listed three major threats for the sustainability of research on Ge CMOS in the near future [*Caymax'09-b*]: timing, cost-effectiveness, and Silicon.

- It is not granted that integrated device manufacturers can afford to wait until Ge technology is mature enough for large scale production
- It is not guaranteed yet that the final gain in performance can compensate for the additional costs related to the increased process complexity
- It is not even sure that Si CMOS can be outperformed by Ge for extremely aggressive gate lengths (cf. SCE, I_{OFF} increase versus I_{ON} gain in the fully and quasi-ballistic regimes [*Krishnamohan'08*], [*Rafhay'09*])

IV.3.4.c. Interest of SiGe alloys

Since concerns are raised in terms of I_{ON}/I_{OFF} trade-off because of a low bandgap and high tunnel-induced leakage at the usual supply voltage values, a solution could be to modulate the Ge concentration by using SiGe alloys as a channel material.
The bandgap dependence of unstrained $Si_{1-x}Ge_x$ at room temperature [*Braunstein'58*], [*People'85-b*] is shown below on Figure IV-49.

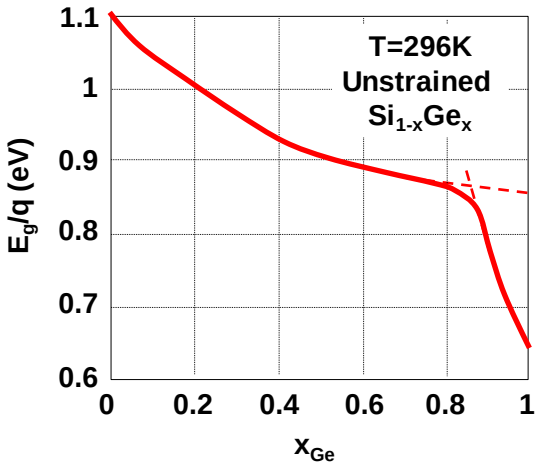


Figure IV-49: Energy bandgap of unstrained $Si_{1-x}Ge_x$ at 296K [Braunstein'58]. At about x=0.85, we observe a cross-over between Si-like (Γ-X) and Ge-like (Γ-L)-defined bandgaps (the minimal CB energy corresponds respectively to <100> and <111>-directed wavevectors).

As a rule of thumb, SiGe alloys with a Ge concentration lower than 85% should not be subject to significant tunnel effects as far as V_{DD}=0.85V. The effective masses are lower and the mobility higher than in unstrained Si [*Fischetti'96*], so SiGe devices with moderately high Ge contents should feature a gain in I_{ON} without the dramatic increase in I_{OFF} from which pure-Ge devices suffer.

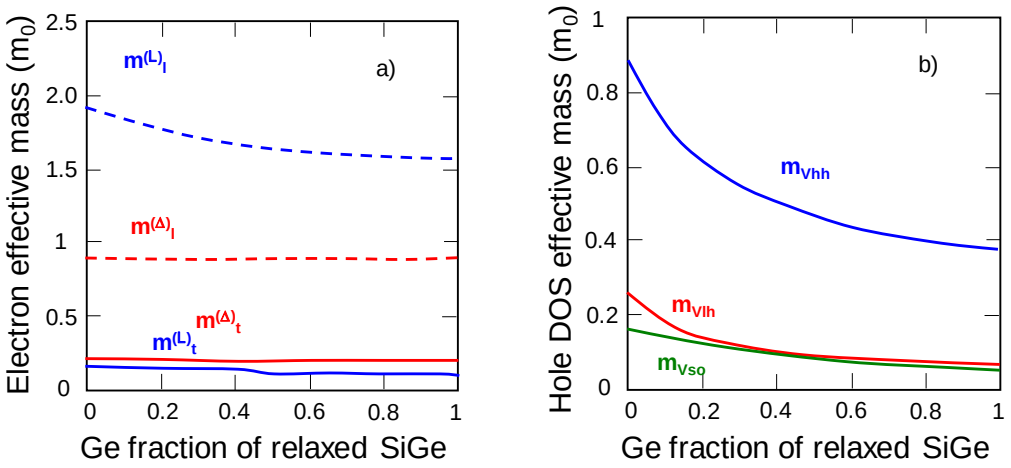


Figure IV-50: Electron effective masses and Hole density of states effective masses in unstrained $Si_{1-x}Ge_x$ versus Ge mole fraction [Fischetti'96].

Besides, the technology is bound to be more Si-like and cheaper, with fewer problems related to the oxidation state of Ge and their consequences on surface states. SiGe films can be obtained by heteroepitaxy on Si, and the Ge content can be raised by means of virtual substrates or Ge enrichment.

The lower lattice mismatch (lattice parameter of $Si_{1-x}Ge_x$: $5.431 + 0.20x + 0.027x^2$ [*Dismukes'64*]) alleviates the constraints in terms of active layer defectivity, and the critical thickness of heteroepitaxy on Silicon is compatible with device fabrication (> 10nm for moderately high x_{Ge}<50% [*People'85-a*]). It is therefore relatively easy to fabricate MOSFETs on globally, compressively strained SiGe. The results presented in the next paragraph will treat of compressively strained SiGeOI (or c-SGOI) for scaled CMOS, achieved either by Ge enrichment ([*Hutin'10-c*]: c-SGOI CMOS) or selective epitaxy ([*Hutin'10-d*]: co-integrated strained SOI nMOS and c-SGOI pMOS).

IV.4. Compressively strained SiGe-On-Insulator (SGOI)

IV.4.1. SGOI obtained by Ge enrichment

The use of mobility boosters as an effective way to reduce power consumption by lowering the supply voltage without losing circuit performance has been subject to significant advances over the last decade [*Takagi'08*]. In particular for pFETs, effective-mass engineered, uniaxially compressively strained SiGe presents the combined advantages of a substantial hole mobility gain [*Thompson'04*], [*Irisawa'05-a&b*], [*Irisawa'06*], [*Bera'06*] and an intrinsically lower pMOS threshold voltage $V_{th,p}$ making it a promising candidate for high-performance CMOS with single-metal gate [*Weber'04*]. The Ge enrichment technique now enables to obtain thin, fully-strained SGOI substrates with low defectivity. From this point, uniaxial stress can be achieved on sufficiently narrow active areas through the elastic strain relaxation process occuring during mesa patterning [*Irisawa'05-a&b*], [*Irisawa'06*]. In [*Hutin'10-c*], the advantages resulting from this approach were investigated for the first time in highly scaled devices down to 20nm gate length, 30nm active area width and 15nm c-SiGe (compressively strained SiGe) film thickness.

IV.4.1.a. Device Fabrication

The SGOI substrates process started with the epitaxy of 38 or 53nm thick $Si_{0.9}Ge_{0.1}$ films on 15nm thick (001)SOI wafers. The Ge enrichment process was pursued until the thicknesses of both types of substrates reached 15nm again, yielding Ge contents of 25% and 35%, respectively (Figure IV-51). These film thicknesses and Ge contents are such that the resulting SGOI substrates were fully strained before patterning [*Vincent'07-b*], [*Huang'98*].

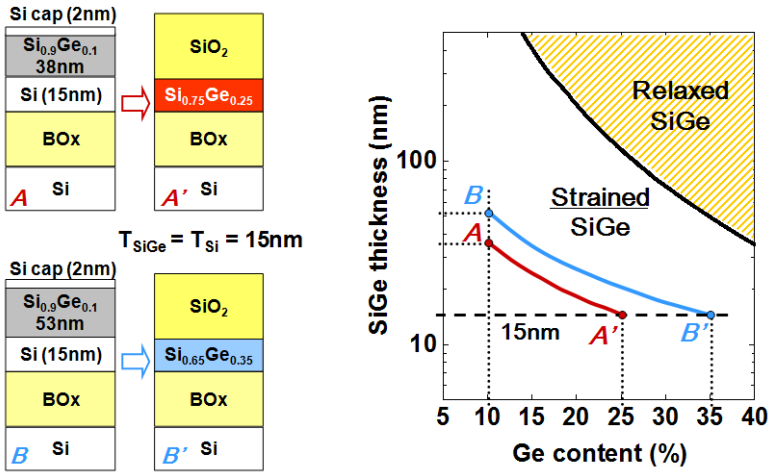


Figure IV-51: SiGe enrichment process yielding 15nm compressively strained $Si_{1-x}Ge_xOI$ (x=0.25 and 0.35). The theoretical relaxation limit is taken from [Huang'98].

After mesa isolation and Si passivation, a Poly-Si/TiN/HfO_2 gate stack was deposited and patterned (resulting EOT=1.8nm). Raised Si S/D were then grown for series resistance reduction. E-beam lithography enabled to fabricate n-&p-MOSFETs with gate lengths scaled down to L_g=20nm, and active area widths as low as W_{design}=30nm (W_{eff}=55nm, Figure IV-52). With a 15nm film thickness, these dimensions lead to trigate configurations for narrow channel devices.

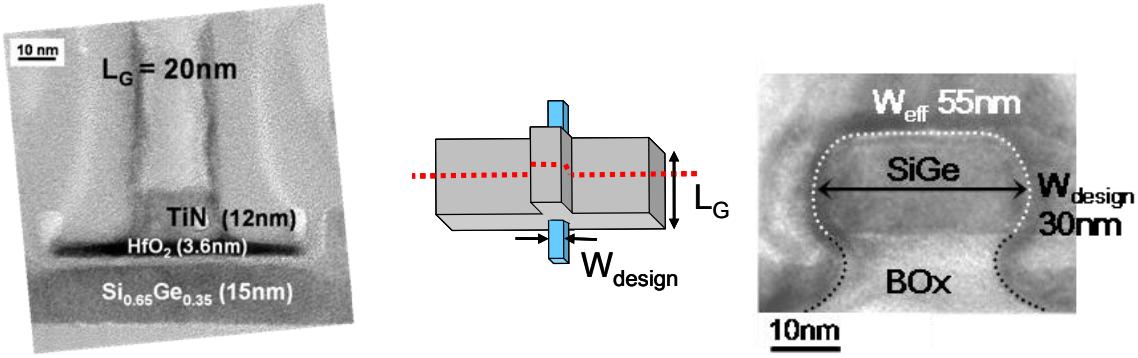


Figure IV-52: Left: Transverse X-TEM view of a pFET on c-SGOI 35% with Lg=20nm. Right: Longitudinal X-TEM view of a pFET on c-SGOI 35% with W_{design}=30nm (pictures: R. Truche).

IV.4.1.b. Long-channel FETs characteristics

The characteristics of long-channel devices typically show enhanced (resp. degraded) features for pFETs (resp. nFETs) as the Ge content increases (Figure IV-53), due to the antagonist impacts of compressive strain on hole and electron mobility [*Uchida'04*]. Likewise, the extracted series resistance decreases (resp. increases) with increasing Ge content in pFETs (resp. nFETs).

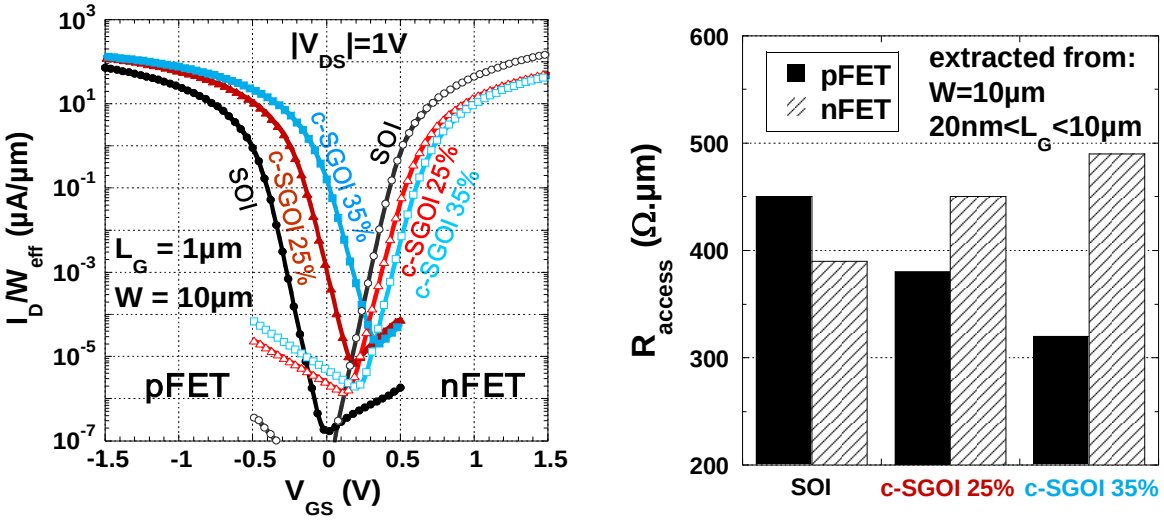


Figure IV-53:Left: I_D-V_{GS} curves of long, wide n- and pFETs on SOI and c-SGOI. Right: Extracted R_{access} on p- and nFETs with a wide channel and gate lengths from 10µm down to 20nm.

Indeed, mobility values using Y-function and CV split methods were extracted (L_g=W=10µm), showing an improvement of +67% for pFETs vs. SOI, and a –70% degradation for nFETs at 0.8 MV/cm (Figure IV-54).

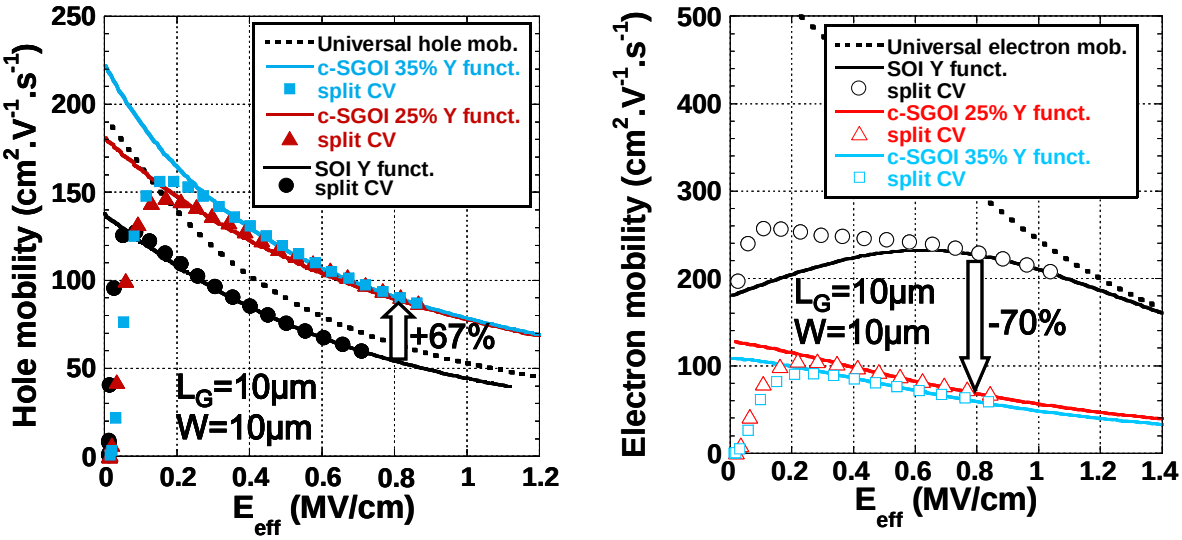


Figure IV-54: Effective mobility in long and wide channel pFETs (left) and nFETs (right) versus effective transverse electric field (extraction: Y-function and CV split).

IV.4.1.c. Low $V_{th,p}$ and NBTI

Charge pumping measurements [*Brugler'69*] were performed on dedicated gated p-i-n structures in order to extract average gate stack/channel interface states densities (Figure IV-55), showing D_{it} values increasing with the Ge fraction, which is generally attributed to the diffusion of Ge atoms within the Si passivation layer [*Kaczer'09*].

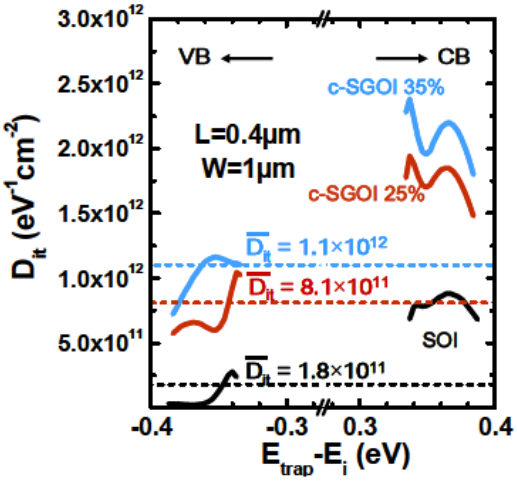
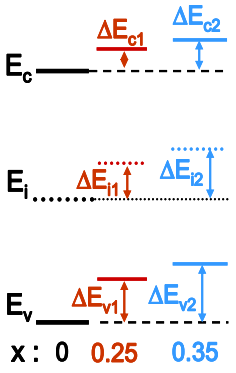


Figure IV-55: Averaged interface state densities (D_{it}) measurement using charge pumping.

The valence band offset between c-SiGe and Si cap forms a barrier impeding holes tunnelling into the gate dielectric, which is considered to be the initial step in NBTI (Negative Bias Temperature Instability) degradation. Hence, NBTI is drastically improved in c-SGOI compared to SOI pFETs (Figure IV-56), in good agreement with prior studies involving Ge or SiGe alloys [*Kaczer'09*], [*Lee'09-a*].

shift \ x	0.25	0.35
ΔE_c (eV)	0.1	0.13
ΔE_v (eV)	0.18	0.25
ΔE_i (eV)	0.14	0.19
ΔE_g (eV)	-0.08	-0.12



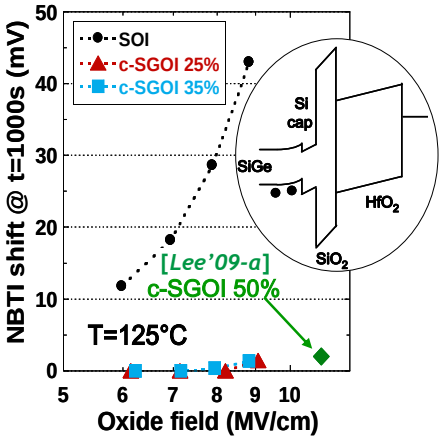


Figure IV-56: Band structures of SiGe under compressive (100) biaxial strain, according to the Ge fraction [Rieger'93]. NBTI shift (t=1000s) versus oxide field and band diagram showing the SiGe/Si cap interface barrier impeding hole tunnelling.

The band offsets and resulting bandgap narrowing also influence the V_{th} shifts relative to SOI (visible in Figure IV-53). The respective contributions of band structure, D_{it} and fixed charges Q_f on ΔV_{th} were evaluated in the Fully-Depleted case (Figure IV-57), providing insight into the expected V_{th} shifts using a further improved surface passivation. From the viewpoint of co-integration with Si-based nFETs (as enabled by localized Ge enrichment [*Vincent'07-a*], [*Tezuka'05*]), intrinsically positive $\Delta V_{th,p}$ values are an asset for realizing high-performance CMOS without resorting to dual metal gate integration schemes.

$$\Delta V_{th} \approx \frac{\Delta E_i}{q} \pm \frac{k \cdot T}{q} \ln\left(\frac{T_{SiGe} \cdot n_i^{SiGe}}{T_{Si} \cdot n_i^{Si}}\right) + \frac{\Delta Q_f + \Delta C_{it}}{C_{ox}}$$

Band structure
Interface states
Fixed charges

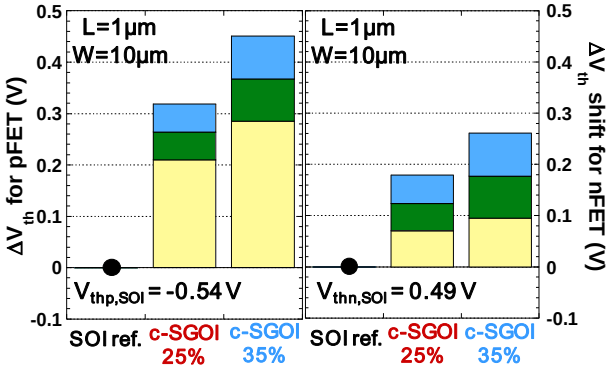


Figure IV-57: Measured V_{th} shifts on wide p- and n-FETs with calculated contributions of band displacement (cf. Figure IV-55), D_{it} (cf. Figure IV-56), and Q_f (to which the remainder is attributed).

IV.4.1.d. Short-channel FETs characteristics

Narrowing the active area down to a 30nm width enabled us to achieve a critically enhanced channel electrostatic integrity at short gate lengths through the emergence of a trigate effect. As shown on the I_D-V_{GS} curves at L_g=20nm (**Fig.13**), DIBL and subthreshold swing are strongly improved by scaling W from 100nm to 30nm channel width.

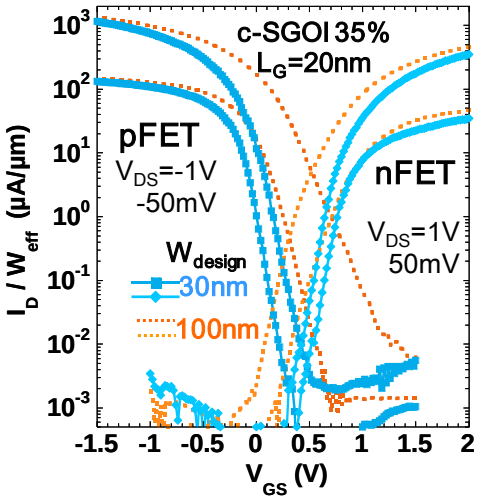


Figure IV-58: I_D-V_{GS} on short c-SGOI35% pFETs and nFETs, and effect of narrowing W towards trigate electrostatic control.

Similarly, Figure IV-59 demonstrates that the V_{th} roll-off is drastically reduced between W=10µm and W=30nm channel width. While short, narrow c-SGOI and SOI devices exhibit similar S_{wi} (90mV/dec at L_g=W=30nm), the lower DIBL for c-SGOI (120mV/V at L_g=W=30nm) is attributed to the reduction of p-type dopants diffusion at the source and drain edges in SiGe channel.

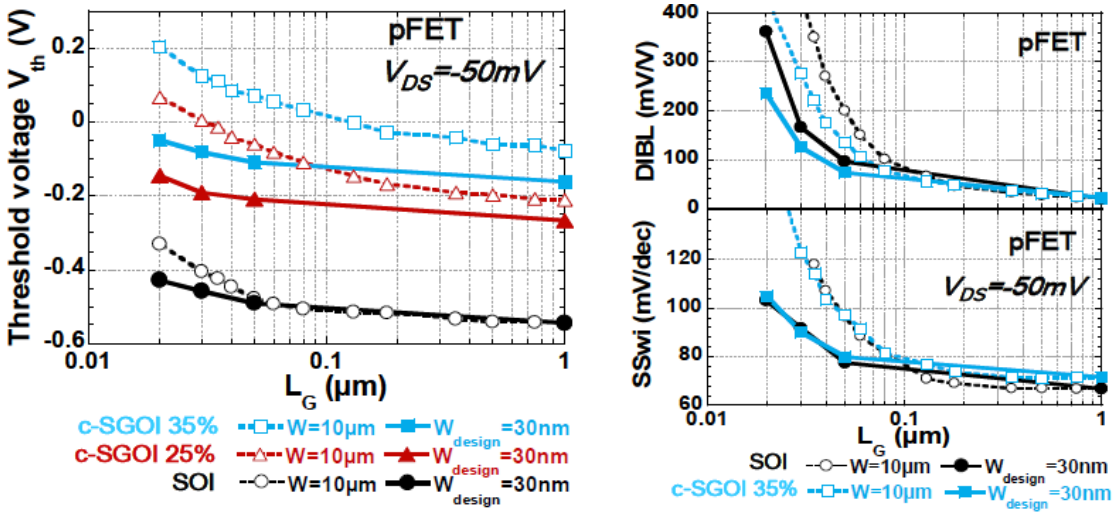


Figure IV-59: Left: V_{th}-L behavior of SOI and c-SGOI pFETs with wide and narrow W. Right: DIBL-L, S_{wi}-L behavior of SOI and c-SGOI 35% pFETs with wide and narrow W.

IV.4.1.e. Transport enhancement in narrow-channel pFETs

The mechanism of lateral relaxation occurring on mesa-isolated strained substrates has been comprehensively investigated [*Takagi'08*], [*Irisawa'05-a&b*], [*Bera'06*]. In wide devices we can consider that residual stress in both directions remains (biaxial compressive). In narrow devices, the strain in the direction perpendicular to the channel vanishes, resulting in quasi-uniaxial compressive strain along the transport direction, as qualitatively described on Figure IV-60.

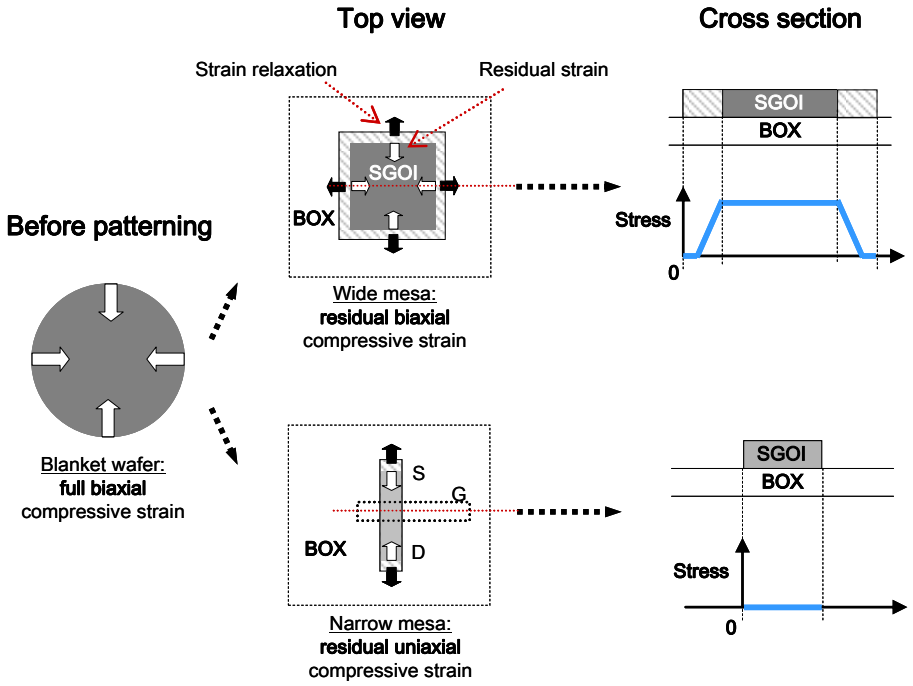


Figure IV-60: Principle of obtaining uniaxial stress in the direction of transport on narrow devices through the mechanism of lateral elastic strain relaxation.

The use of a thin SiGe film is crucial in order to keep the extent of the relaxation zone (in the direction of transport) inferior to the distance between gate edges and mesa free edges, therefore achieving maximized strain under the gate. The hole mobility enhancement resulting from uniaxial compressive stress is typically more efficient than the biaxial one. Indeed, and in spite of a lower band splitting than for biaxial stress (lower V_{th} shifts for long, narrow channel devices, see Figure IV-59), uniaxial stress along <110> induces a valence band warping (due to shear strain occurrence), which leads to hole effective masses reduction [*Thompson'04*].

Figure IV-61 shows the long channel <110> I_{Dlin} current enhancement with W scaling when the stress gradually becomes uniaxial. It culminates with a ×2.85 factor for c-SGOI 35% at W=100nm. The decrease observed for very low W is attributed to an increasingly predominant (due to the W_{side}/W_{top} ratio) degraded mobility on the sidewalls. Uniaxial stress along the <100> direction is found to be less efficient than along <110>, in good agreement

with [*Smith'09*], [*Uchida'04*]. This is due to the lack of shear strain under uniaxial stress in the <100> direction [*Weber'07*].

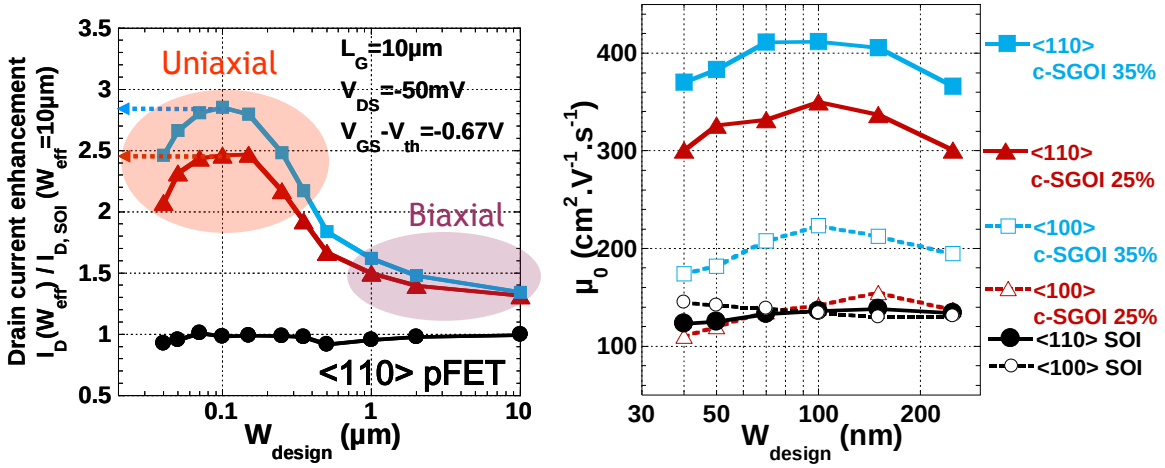


Figure IV-61: Left: I_D enhancement factor in linear regime of long, narrow channel pFETs vs. wide devices on SOI. Right: Influence of the uniaxial strain direction on the extracted hole low-field mobility μ_0.

A factor 1.8 compared to the SOI reference is maintained at L_g=20nm for narrow <110> c-SGOI 35% pFETs (Figure IV-62). For V_{DS}=-1V and the most aggressive dimensions (L_g=20nm, W_{design}=30nm), I_{ONr}=520µA/µm (at V_{GS}-V_{th}=-0.67V) and I_{OFFr}=130nA/µm (at V_{GS}-V_{th}= 0.33V) are reported in W_{eff} normalization (I_{ONr}=950µA/µm, I_{OFFr}=240nA/µm with a top view W_{design} normalization).

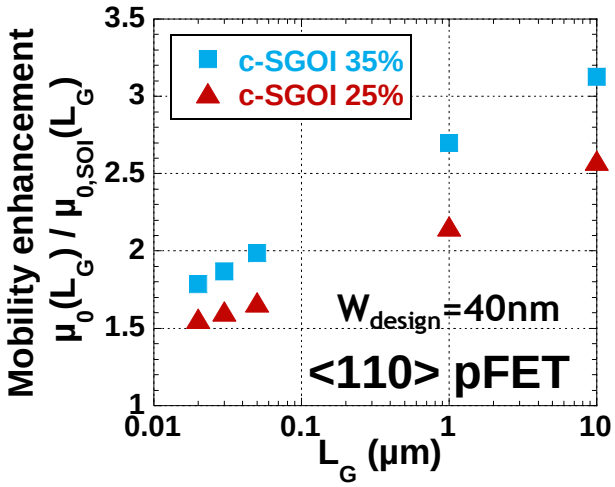


Figure IV-62: Low-field mobility μ_0 improvement relative to SOI versus L_G for narrow (W_{design}=40nm) pFETs strained along the <110> direction.

The CV/I_{ON} versus I_{OFF} figure of merit shown in Figure IV-63 illustrates the performance of the short, narrow SOI and c-SGOI pFETs in [*Hutin'10-c*] compared to other state-of-the-art c-SGOI and relaxed GeOI pFETs [*Smith'09*], [*Irisawa'05-a*], [*Hutin'10-b*].

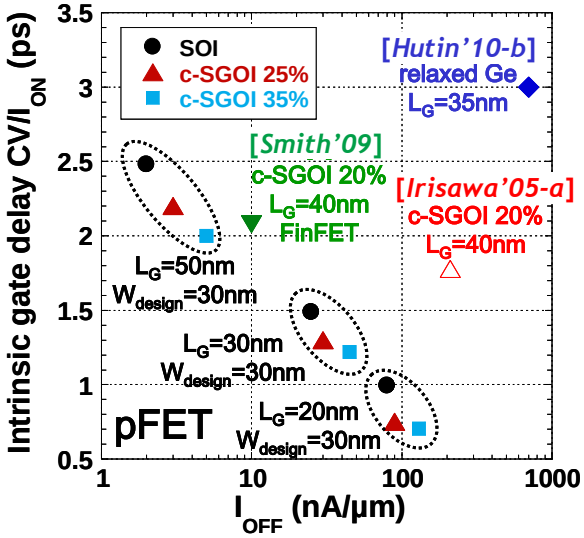


Figure IV-63: CV/I_{ON}-I_{OFF} figure of merit (V_{th}-relative, V_{DD}=-1V) and comparison with related studies.

IV.4.1.f. Summary

Ge enrichment was carried out so as to obtain 15nm of compressively-strained SiGe On Insulator. As compressive stress is not favorable to electron conduction, the focus was put on pFETs results. Uniaxial stress yields a better mobility than biaxial stress as it provokes a warping of the VB and reduces the holes effective masses. A way to achieve it is to take advantage of lateral strain relaxation occurring in narrow mesa-isolated active areas. A positive side-effect of this configuration is that the device architecture becomes trigate-like, which significantly improves the electrostatic integrity at short gate lengths, resulting in an interesting I_{ON}-I_{OFF} trade-off at short gate lengths.

Some paths for performance optimization have been identified for pFETs, but the nFETs characteristics are still not as good as on SOI, which brings us back to a Dual Channel approach. As Ge enrichment localized at the device level has not been demonstrated yet, a different integration scheme is proposed in the next paragraph, consisting in selective epitaxy of SiGe on SOI or tensily strained SOI [*Andrieu'05*], [*Hutin'10-d*].

IV.4.2. **Dual Channel CMOS by selective SiGe epitaxy**

In order to achieve low $V_{th,p}$ for high performance gate-first CMOS with high-k and metal gate, the Dual Channel (DC) approach emerges as a solution relying on the modulation by channel bandgap rather than by a change of workfunction [*Harris'07*], [*Witters'10*]. It is therefore particularly adapted to a single midgap metal gate integration scheme. Significant advances have been made recently [*Weber'06*], [*Takagi'08*], [*Smith'09*], [*Eneman'10*], in the optimization of strained SiGe pFETs, and DC n-Si/p-sSiGe co-integration schemes have been demonstrated so far on bulk [*Harris'07*], [*Park'10*], [*Witters'10*] and On Insulator [*Andrieu'05*], [*Le Royer'10-b*] substrates. We showed in [*Hutin'10-d*] an aggressively scaled planar Dual Strained Channel co-integration (n-sSi/p-sSiGe) on Fully-Depleted SOI, for the first time with ring oscillators and well-balanced SRAM cells owing to symmetrically low $V_{th,n}$ and $V_{th,p}$.

IV.4.2.a. Dual Channel and CMOS process on (s)SOI

We integrated Dual Channel materials (nFET on strained or unstrained Si and pFET on strained SiGe) thanks to a SiO_2 hard mask and selective epitaxy (Figure IV-64, [*Andrieu'05*]). Specifically, after a « HF-last » wet cleaning and a H_2 bake (800°C, 2 min), SiGe/Si cap stacks with various Ge contents (20%, 40% and 60%) were selectively grown in the pFET active regions. At this stage, the nFET regions were covered by SiO_2.

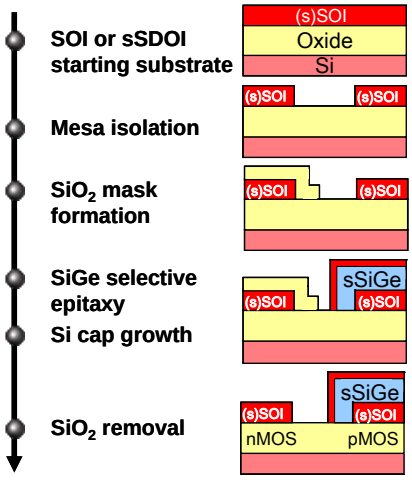


Figure IV-64: Scheme of the Dual Channel On Insulator (DCOI) integration. SiGe is deposited only on the pMOSFET active areas, either on SOI, or on sSOI. A Si cap (4nm) is deposited on top of the SiGe layer to passivate the interface with the high-k gate dielectric (HfO_2).

SiGe growth temperatures were reduced from 650°C (x_{Ge} = 20%) down to 550°C (x_{Ge} = 40% and 60%) and a dedicated Si capping procedure was used in order to minimize surface roughening. Loading effects had also to be accounted for in order to obtain the targeted SiGe

layer thickness [*Hartmann'05-b*], [*Hartmann'09*]. Nonetheless, elastic and plastic relaxation may still occur at high Ge contents. Featureless surfaces and well-defined XRD peaks suggest pseudomorphic stacks up to 50% Ge (Figure IV-65). Beyond this, the broad SiGe layer peak, the lack of thickness fringes and a Ge content extracted from dynamical theory fitting (~55%) inferior to the targeted 65% indicate partial relaxation. The corresponding AFM surface imaging is indeed characterized by small undulations and numerous short ploughing lines along the <110> directions (surface signatures of the propagation of the threading arms of misfit dislocations on {111} planes). The various D(S)COI integration schemes implemented in this work are summarized in Table IV-4.

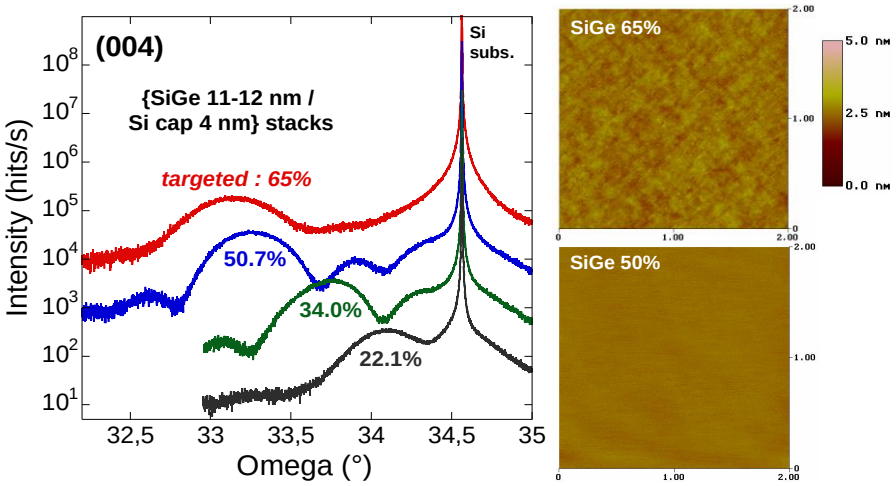


Figure IV-65: Omega-2Theta scans around the (004) XRD order (direction of growth) of {Si cap 4nm / SiGe 11nm} stacks on SOI for various Ge fractions up to a targeted concentration of 65%. On the right, tapping mode AFM images of the surfaces of the stack corresponding to the two highest Ge contents (50% and 65%).

Co-integration schemes	nMOS	pMOS
	SOI	SOI
	SOI	$Si_{0.8}Ge_{0.2}$ / SOI
	SOI	$Si_{0.6}Ge_{0.4}$ / SOI
	SOI	$Si_{0.4}Ge_{0.6}$ / SOI
	sSOI 20%	$Si_{0.6}Ge_{0.4}$ / sSOI 20%
	sSOI 20%	$Si_{0.4}Ge_{0.6}$ / sSOI 20%

Table IV-4: Table summarizing the various co-integrated schemes available in [Hutin'10-d]. SiGe layers with Ge fractions ranging from 20% to 60% were deposited either on SOI or on sSOI for pFET fabrication. The notation sSOI20% corresponds to tensily strained (001)Si epitaxially grown on relaxed $Si_{0.8}Ge_{0.2}$ before being transferred directly on Insulator (sSDOI) using Smart Cut™.

The subsequent CMOS technological steps followed a standard Fully-Depleted SOI process flow with single high-k/metal gate stack, raised and salicided Si Source and Drain (S/D) [*Barral'07*]. An sSOI nFET and a SiGe 40%/sSOI pFET co-integrated on the same die and with L_G~20nm are shown on TEM micrographs (Figure IV-66).

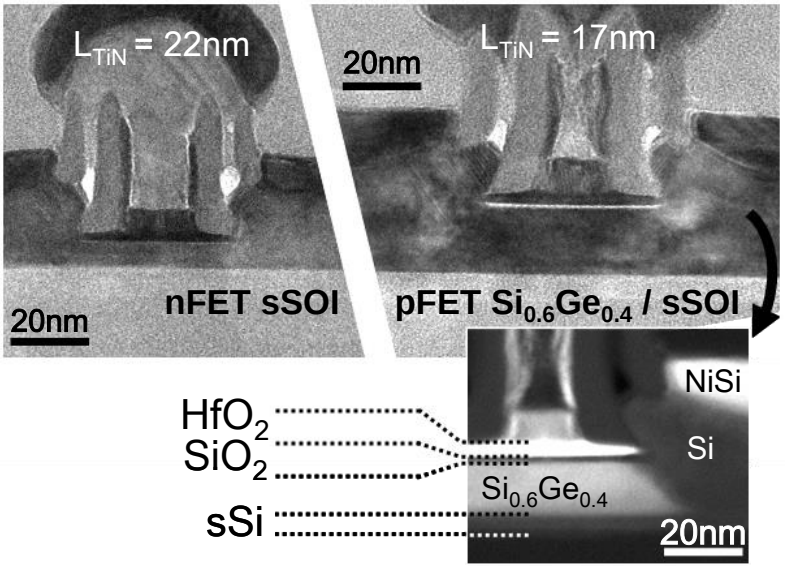


Figure IV-66: High Resolution Cross-Sectional TEM (HR XTEM) images of a sSOI 20% nFET co-integrated on the same die with a SiGe 40% / sSOI 20% pFET of respective gate lengths 22nm and 17nm. The High-Angle Annular Dark-Field (HAADF) STEM image below provides an additional view of the pFET with contrast between the SiGe and Si region (T_{sSOI} ~ 8nm; $T_{SiGe/(s)SOI}$ ~ 19nm) (pictures: D. Cooper, A. Béché).

IV.4.2.b. Strain characterization in the channel

The amount of strain within the pFET conduction channels has been investigated using two original techniques, Dark-Field Electron Holography (DFEH) and NanoBeam Electron Diffraction (NBED). The strain sensitivity of both methods is below 0.06% [*Hÿtch'08*], [*Béché'09*] and the resulting spatial resolution is 4-6nm. NBED and DFEH measurements on a L_G=500nm pFET ($Si_{0.6}Ge_{0.4}$/sSOI) are shown Figure IV-67. The DFEH image shows a strain relaxation zone at the edge of the channel, which is clearly confirmed by NBED. The $Si_{0.6}Ge_{0.4}$ is partially relaxed in the {220} direction on either side of the gate over L_{relax}~70nm. This is certainly due to the SiGe consumption in the S/D region during HfO_2 etching, as shown by Figure IV-66. the compressive strain is preserved in the central region (only +0.75% deformation versus Si, corresponding to the lattice mismatch of the underlying sSOI20%). As a consequence, strain relaxation can be neglected in long and large devices.

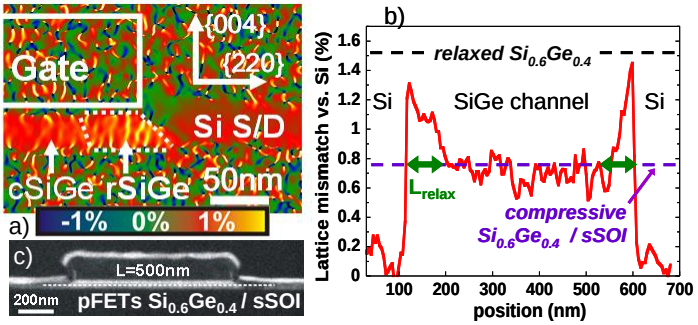


Figure IV-67: a) 2-D DFEH strain mapping and b) 1-D NBED strain profile of a LG=500nm pFET SiGe/sSOI showing the deformation relative to the unstrained Si substrate (below the BOX) in the {220} direction. The NBED profile was acquired in the SiGe region indicated by the dashed line in the HAADF STEM view in c) (pictures: D. Cooper, A. Béché).

IV.4.2.c. Trade-off between mobility gain & V_{th} shift

The long channel nFETs on sSOI feature a +106% increase in electron mobility as compared to SOI at E_{eff}=0.6 MV/cm (Figure IV-68-a). For SiGe/SOI pFETs, the mobility gain at 0.6MV/cm increases with the Ge content, by +68% and +92% for $Si_{0.8}Ge_{0.2}$ and $Si_{0.6}Ge_{0.4}$, respectively (Figure IV-68-b). Yet for a higher 60% Ge content, the gain is lowered (Figure IV-68-c), likely due to dislocations formation during the epitaxial growth (cf. Figure IV-65). This hypothesis is confirmed by the better results on $Si_{0.4}Ge_{0.6}$/sSOI 20% than on $Si_{0.4}Ge_{0.6}$/SOI. This clearly demonstrates that an optimum strain and Ge percentage can be reached for SiGe channels.

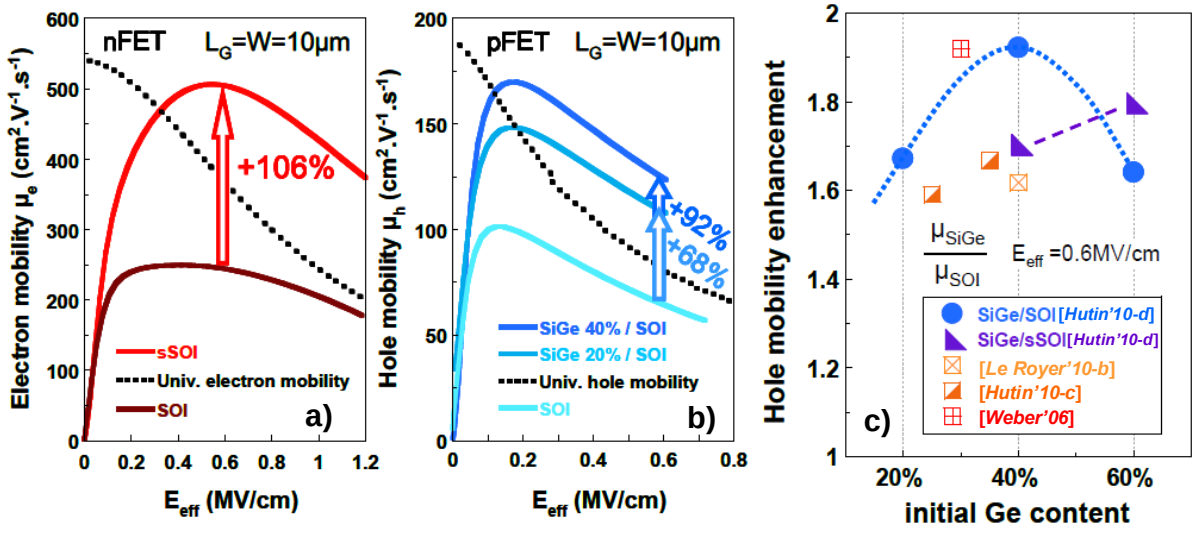


Figure IV-68: a) Electron mobility(μ_e) in SOI and tensily strained SOI nFETs and b) hole mobility (μ_h) in SOI and compressively strained SiGe/SOI pFETs versus effective electric field E_{eff} (split C-V technique). c) Hole mobility enhancement at 0.6MV/cm for pFETs on SiGe grown on SOI (circles) or sSOI 20% (triangles), as a function of the Ge fraction (and comparison with previously published data on SiGe channels).

The Si capping layers, initially at a 4nm thickness, are not visible on the C-V characteristics of SiGe pFETs (Figure IV-69-a, no additional plateau) suggesting a redistribution of Ge atoms towards the gate interface during the process integration. This is in agreement with the average D_{it} values extracted for the various SiGe devices (Figure IV-69-b, C-V/G-V technique, [*Batude'07*]), which increase with the Ge content. However, this diffusion of Ge atoms within the Si cap and in the vicinity of the dielectric/channel interface does not degrade the equivalent oxide thickness (EOT) compared to the SOI reference (Figure IV-69-c, EOT=1.8nm), as previously reported in [*Le Royer'10-b*]. Flat-band voltages are lowered with increasing Ge content (Figure IV-69-d). ΔV_{FB} varies almost linearly with the Ge fraction. This is due to Ge and strain-induced bands shifting, increasing interface states densities (D_{it}) and possible fixed charges (Q_f) [*Hutin'10-c*]. The role of the strain in V_{FB} shifting is highlighted by equivalent values for $Si_{1-x}Ge_x$ and $Si_{1-(x+0.2)}Ge_{x+0.2}$/sSOI20%.

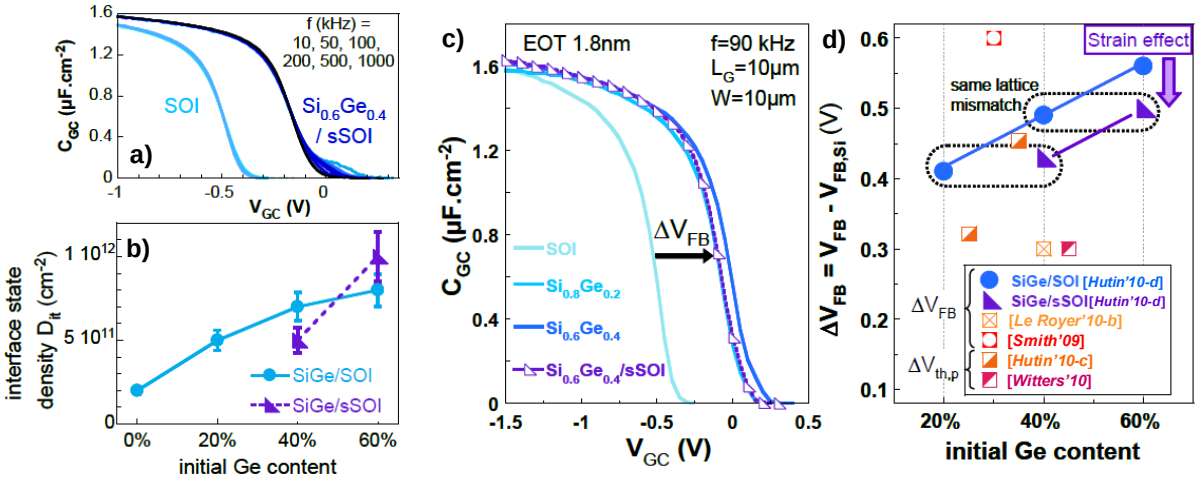


Figure IV-69: a) C-V characteristics measured at various frequencies (10 to 1000 kHz) on pFETs (W=L_G=10µm) highlighting the increase of the interface states density D_{it} with increasing Ge content. b) Extracted mean D_{it} values versus Ge content (C-V/G-V extraction) c) C-V characteristics measured at 90 kHz on pFETs (W=L_G=10µm). d) Corresponding Flat-band voltage shifts (ΔV_{FB}) with respect to SOI pFETs (and comparison with SiGe published data).

Finally, the SiGe 20%/SOI pFETs display roughly the same mobility enhancement, D_{it}, and V_{fb} shift as SiGe 40%/sSOI pFETs. Nevertheless, the latter benefit from the co-integration with sSOI nFETs (DSCOI scheme) featuring higher mobility and lower $V_{th,n}$ than their SOI counterparts (Figure IV-70).

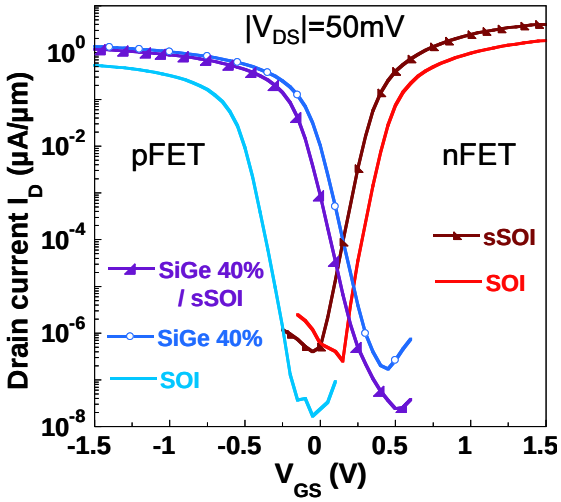


Figure IV-70: I_D-V_{GS} characteristics measured at $|V_{DS}|$=50mV on long channel co-integrated CMOS devices (L_G=W=10µm): pFETs on SOI, SiGe 40%/SOI and SiGe40%/sSOI; nFETs on SOI and sSOI 20%. For SiGe40%/(s)SOI based pFETs the use of the sSOI template enables to adjust the $V_{th,p}$ value.

IV.4.2.d. D(S)COI short channel devices & circuits

At short gate lengths (L_G<200nm), symmetrically low $V_{th,p}$ and $V_{th,n}$ are demonstrated in the DSCOI configuration. This threshold voltage adjustment at a low value (V_{th}≈0.2V) contributes to an I_D boost for pMOS on $Si_{0.6}Ge_{0.4}$/sSOI compared to SOI, as illustrated in the linear regime, Figure IV-71.

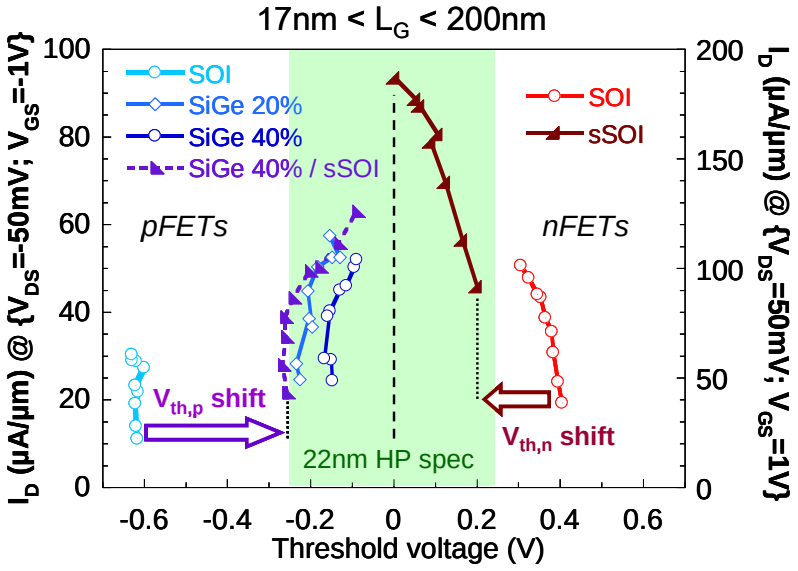


Figure IV-71: On-State Drain current in linear regime ($|V_{GS}|$=1V; $|V_{DS}|$=50mV) as a function of threshold voltage for short-channel pFETs and nFETs (L_G comprised between 17nm and 200nm). Threshold voltages of sSOI and SiGe devices are subject to an increased roll-off at short lengths with respect to the SOI reference since the film thicknesses are larger (T_{SOI} ~ 6nm; T_{sSOI} ~ 8nm; $T_{SiGe/(s)SOI}$ ~ 19nm).

In order to monitor the mobility contribution, we extracted the low-field mobility μ_0 down to short gate lengths (20nm). Figure IV-72 shows μ_0 degradation with scaling for all the channel types, and to a larger extent for SiGe channels (enhancement drops to 0-30%).

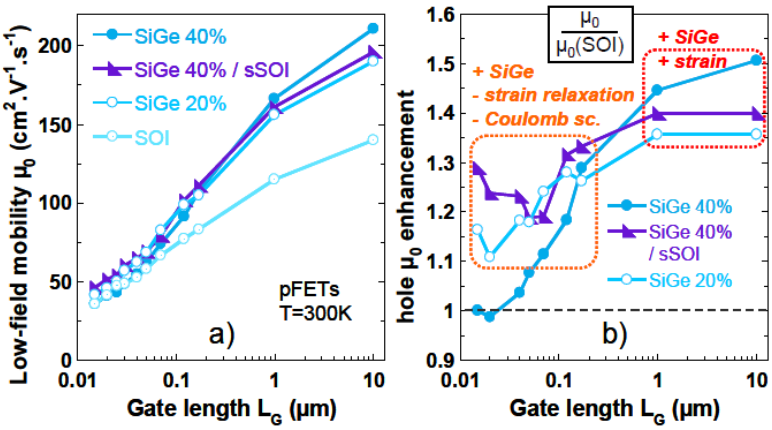


Figure IV-72: a) Low-field mobility μ_0 (Y-function extraction) versus gate length on pFETs from room-temperature measurements, showing a decrease of the mobility gain with L_G scaling, for all Ge contents. b) Corresponding mobility enhancement factor ($\mu_0/\mu_{0,SOI}$).

This suggests a relaxation of the strain, which is confirmed by DFEH map and NBED profile measured on short pFET (L_G=17nm, Figure IV-73). Indeed, the observed deformation (+1.55% versus Si) indicates a fully relaxed $Si_{0.6}Ge_{0.4}$ channel under the gate (in agreement with the 70nm typical lateral relaxation length observed on Figure IV-67).

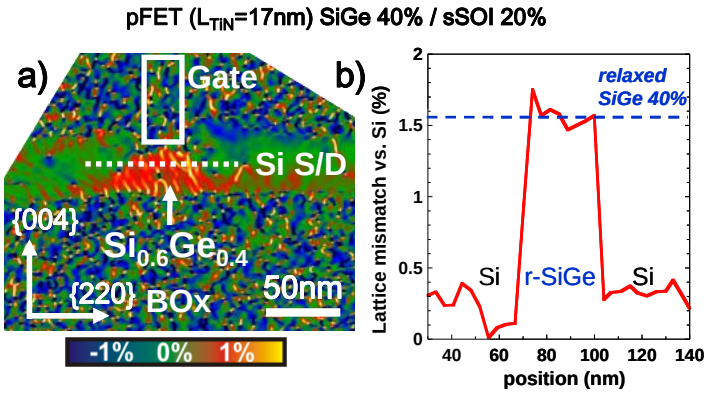


Figure IV-73: a) DFEH strain mapping of a $Si_{0.6}Ge_{0.4}$/sSOI 20% pFET with L_G=17nm showing the lattice mismatch with respect to that of the underlying Si substrate in the <110> direction (with dashed scan line for NBED strain profiling). b) NBED strain profile in the <110> direction of the SiGe area showing full strain relaxation under the gate.

Another explanation for the reduction of the sSiGe-induced mobility boost for scaled devices is linked to a change in transport limitation mechanisms. In fact, even the carrier mobility on SOI is affected by scaling (Figure IV-72). This decrease, confirmed at low temperature (Figure IV-74-a) is commonly attributed to an additional Coulomb Scattering

(CS) effect near the S/D junctions [*Cros'06*]. Both the strain relaxation and this additional CS at short L_G influence the hole mobility in scaled SiGe channels. The long channel μ_0 gain is larger at 20K (+70%, Figure IV-74-b) than at 300K (+45%), demonstrating the superiority of SiGe channels in a CS-limited regime due to lighter hole effective masses. This advantage and the strong CS influence for short channels explain the increase of the μ_0 gain at shorter L_G (up to +130% at L_G=20nm, 20K).

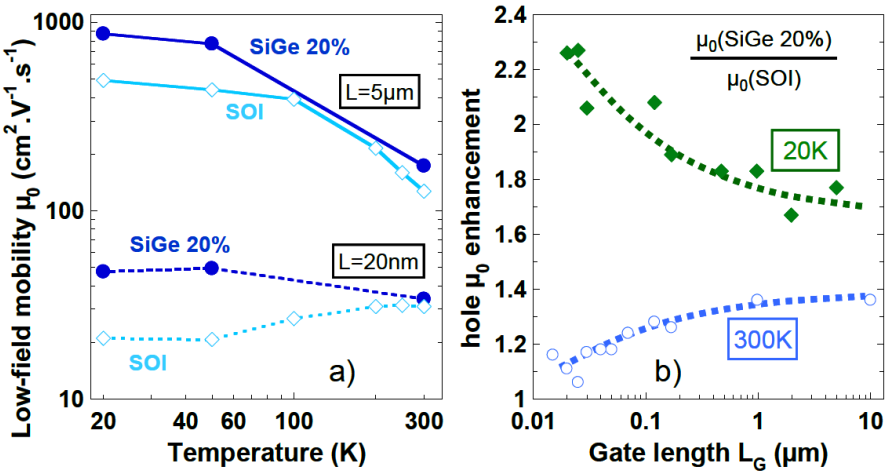


Figure IV-74: a) Impact of temperature on the hole low-field mobility for long and short gate length pFETs (SiGe20%/SOI and SOI ref.). b) Impact of L_G on the hole μ_0 enhancement (for SiGe 20%/SOI with respect to SOI pFETs) at 300K and 20K.

Thus, despite the partial strain relaxation in short channel devices, the reduced hole effective mass preserves the mobility enhancement at room temperature. This gain and the V_{th} adjustment with co-integrated short n-sSOI and p-SiGe40%/sSOI FETs (Figure IV-75) lead to a -39% improvement of the propagation delay in ring oscillators (101 inverters, L_G=40nm) at V_{dd}=0.9V compared to the n&p-SOI reference (Figure IV-76-a). Furthermore, the symmetry of the DSCOI threshold voltages at L_G=22nm result in well-balanced 6T-SRAM cells butterfly characteristic curves (Figure IV-76-b, RNM=100mV).

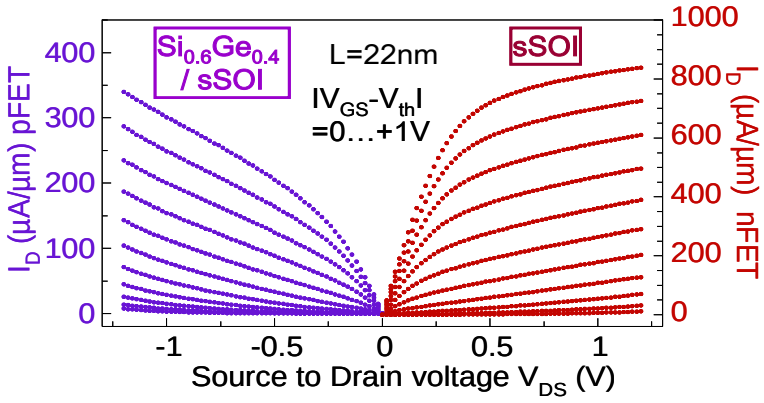


Figure IV-75: I_D-V_{DS} measurements (V_{GS} step=0.1V) of co-integrated CMOS devices (L_G=22nm) using the DSCOI integration scheme (sSOI nFETs and $Si_{0.6}Ge_{0.4}$/sSOI pFETs).

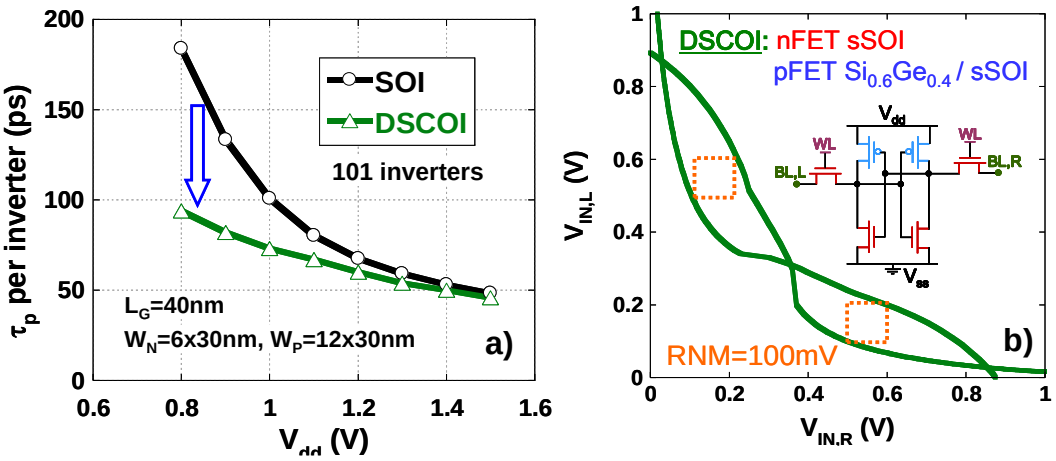


Figure IV-76: a) Propagation delay per inverter versus supply voltage in ring oscillators on SOI and DSCOI (n sSOI & p $Si_{0.6}Ge_{0.4}$/sSOI). Each transistor is a multi-channel device (n: ×6; p: ×12) with L_G=40nm and W=30nm. The gain at low V_{DD} results from both lower $V_{th,n}$ and $V_{th,p}$. b) Left bit line (BL,L) potential versus right bit line (BL,R) potential and reciprocally for a 6T SRAM cell featuring Dual Strained Channel CMOS (DSCOI: sSOI nFETs and $Si_{0.6}Ge_{0.4}$/sSOI pFETs) inverters with L_G=22nm. The RNM is 100mV.

IV.4.2.e. Summary

Dual Strained Channel (n-sSi, p-sSiGe) On Insulator n&pFETs scaled down to 17nm gate length were demonstrated for the first time with functional circuits (balanced SRAM cell characteristics and ring oscillators). We have seen the influence of process integration (Ge content, diffusion and overetch) and scaling on this architecture thanks to advanced strain characterization techniques (NBED, DFEH) and low temperature measurements.

Several points should be improved though:

- The SiGe overetch in the S/D areas should be avoided as it provokes strain relaxation (and a mobility drop) on short-channel devices.
- The $V_{th,n}$ and $V_{th,p}$ of sSOI nFETs and s-SiGe pFETs are indeed low. Nevertheless, they should remain a bit higher to limit I_D leakage at V_{GS}=0V. This implies that the gate stack passivation should be further optimized.
- With this approach, the pFET channels are thicker than the nFET channels. This is problematic in terms of SCE management. This could be avoided by slightly thinning the SOI on the pFET active areas prior to SiGe epitaxy.

IV.5. Ge channel Schottky Barrier MOSFETs

At this point of the manuscript, we have presented the basics of the theory of metal/semiconductor contacts, the operation and fabrication of Schottky-Barrier MOSFETs, as well as the assets and limitations of Germanium-based technology.

Therefore, in this section, we can analyze the characteristics of Ge-channel SBFETs knowing what to expect in terms of electrical behavior of metal contacts on Ge, basic SBFET operation, and Ge-channel FET performance.

IV.5.1. State-of-the-art, undoped interface

IV.5.1.a. pFETs

Between 2005 and 2008, several studies were published reporting on Schottky transistors on Ge or GeOI, none of them featuring interfacial doping to our knowledge. Although most of the key data are summarized in Table IV-5, some comments will be made regarding the reported SBH and the overall performance.

	[*Zhu'05*]	[*Li'06-a*]	[*Li'06-b*]	[*Maeda'06*]	[*Pethe'07*]	[*Li'08*]
Device type	pFET (ring-shaped)	pFET	pFET (ring-shaped)	pFET (back-gate)	pFET	pFET
Substrate type	n-Ge(100) bulk	n-Ge(100) bulk	n-Ge(100) bulk	p-GeOI enrichment (30nm)	Si/sGe 2nm/Si heterostructure	n-Ge bulk
Substrate doping (at.cm^{-3})	a few 10^{15}	a few 10^{15}	a few 10^{15}	a few 10^{15}	N.S.	N.S.
Gate stack	TaN/HfN/HfAlO	TaN/HfO_2	TaN/HfO_2	Si/SiO_2 (back-gate, BOX 210nm)	p^+ SiGe/LTO 20nm	TaN/HfO_2
Gate insulation from the S/D	Lateral selective etching of HfN during preclean	Spacers AlN 3nm + SiO_2 15nm	Spacers AlN 4nm + SiO_2 6nm	None other than BOX	LTO spacers	Spacers
S/D Metal	NiGe	NiGe	$PtGe_2$	PtGe	NiSiGe	Pt_xGe_y
Preclean	diluted HF	N.S.	N.S.	N.S.	N.S.	HF:H_2O = 1 :100
Metal deposition	N.S.	30nm sputtering	30nm sputtering	E-beam evap.	100nm sputtering	N.S.
Germanidation anneal	600°C 1min N_2	400°C 1min	400°C N_2	400°C 30min Forming Gas	450°C 1min N_2	Laser KrF 248nm, 23ns, 0.14J.cm^{-2}
Selective removal	NH_4OH:H_2O_2:H_2O = 1:2:5	HNO_3:H_2O = 1:20	diluted aqua regia	N.S.	Concentrated HCl	dry etch
Extracted SBH	Φ_{bp} = 0.16eV	Φ_{bp}= -0.08eV	Φ_{bp}= -0.1eV	Φ_{bp}= 0.05eV	Φ_{bp}= 0.1eV	Φ_{bp}= 0.08eV
Gate length (µm)	8	8	8	200	3	10
Subthreshold swing (mV/dec)	250	137	133	N.S.	N.S.	~600
I_{on}/I_{off} (dec)	2	2	3.5	N.S.	N.S.	1.5

Table IV-5: Summary of the main fabrication steps and results of state-of-the-art p-SBFETs on Ge. N.S. stands for "Not Specified". I_{on} and I_{off} are defined relative to V_{th}.

In [*Zhu'05*], the SBH for electrons is extracted by I-V fitting with a relatively high ideality factor η=1.49 and Φ_{bn}=0.5eV. The SBH for holes is deduced by complementarity: Φ_{bp}=0.16eV. The characterized devices (W/L=400/8µm) display a ×4 improved Drain current wirth respect to similar transistors on Si with PtSi S/D, which is consistent with a smaller barrier for holes injection (Φ_{bp}=0.25eV for PtSi/Si). However, the I_{ON}/I_{OFF} ratio is quite low (2 decades) owing to high leakage and degraded subthreshold slope (~250 mV/dec). Concerning the first one, it is attributed to a relatively low Φ_{bn}, and the use of thin films (GeOI) is proposed to decrease the NiGe/Ge contact surface. As for the subthreshold slope, it might be due to the distance separating the Gate edge from the Source edge. In fact, the selective etch of HfN by diluted HF during preclean resulted in a lateral encroachment (of unspecified length). From what we know on contacts on undoped semi-conductor and subthreshold slope dependence on Gate/Source distance, this is a probable cause. An alternate explanation would lie in the interface quality between Ge and HfAlO.

A different gate stack was implemented in [*Li'06-a*] and [*Li'06-b*]: TaN/HfO_2 (interlayer not specified). Additionally, AlN/SiO_2 spacers were defined prior to metal deposition. The subthreshold slope is significantly improved (respectively 137 and 133 mV/dec), although still non-ideal. The extracted SBH for NiGe/Ge contacts in [*Li'06-a*] is surprising, as it is said to be negative for holes (activation energy extraction of Φ_{bn}: 0.74eV; Φ_{bp}=-0.08eV). Considering the substrates are very lightly doped (~10^{15} at.cm^{-3}) and no extensions doping was performed, such a value is difficult to explain. Yet, in spite of these 0.24eV of difference with [*Zhu'05*], the ON-State current levels on devices of same dimensions are completely comparable. The leakage current is still high, but that may be due to an overlap between S/D and Gate (not shown, length not specified).

This assumption tends to be confirmed by the results in [*Li'06-b*], where $PtGe_2$ S/D were implemented on the same kind of substrates and devices. The extracted SBH (activation energy extraction of Φ_{bn}: 0.76eV; Φ_{bp}=-0.1eV) is fairly similar to NiGe/Ge contacts in [*Li'06-a*], yet the leakage current is drastically reduced. Overall, the reported SBH values in the last three cited papers are somehow confusing and not very consistent with each other in the light of the electrical results of the MOSFETs. What should be retained is that:

- There seems to be an improvement with respect to undoped PtSi/Si devices
- The leakage current is controlled in [*Li'06-b*] with PtGe S/D
- The performance remains limited by the subthreshold slope, which could be due either to the Gate stack interface D_{it}, or the underlap between Source and Gate

The fabrication of a p-SBFET on GeOI was for the first time reported in [*Maeda'06*]. The 30nm thick Ge-rich layer was obtained by "condensation" (final Ge content: ~99%). The

structure is not that of a classical MOSFET in that the gate electrode and dielectric are respectively the Si substrate and the BOX (back-gate configuration, BOX thickness 210nm). Therefore, it is not relevant to comment on the subthreshold slope and gate bias values (up to 40V). The extracted SBH for PtGe/Ge contacts was 0.05eV (TE I-V fitting, η=1.05) , which is consistent with other experimental observations and the Fermi-pinning theory. At low V_{DS}, the On-State to Off-State current ratio is in the range of 2.5 to 3 decades.

IV.5.1.b. nFETs

Rather than compensating for the high SBH for electrons on metal/Ge contacts using interfacial doping, thin (~2nm) depinning layers were integrated in [*Kobayashi'08*] and [*Nishimura'08*] (resp. of SiN and GeO_x) for Ge n-SBFET fabrication. Qualitatively, increasingly ohmic behavior with increasing the interlayer thickness is clearly shown on diodes on n-Ge.

The fabricated nFETs are functional, but the I_D-V_{DS} characteristics presented in both studies mostly aim at demonstrating a proof-of-concept rather than optimized performance (no information on subthreshold swing). We still can note that the ration between I_{ON} and I_{OFF} ([*Kobayashi'08*]: I_D at V_{DS}=1V; $V_{GS,on}$=10V and $V_{GS,off}$=0V - [*Nishimura'08*]: I_D at V_{DS}=1V; $V_{GS,on}=V_{th}$+0.6V and $V_{GS,off}=V_{th}$-0.2V) remains around 1 decade (Table IV-6).

	[*Kobayashi'08*]	[*Nishimura'08*]
Device	nFET	nFET
Substrate type	p-Ge(100) bulk	p-Ge(100) bulk
Substrate doping ($at.cm^{-3}$)	N.S.	undoped
Gate stack	Al/LTO/GeON	Au/GeO_2 30nm
Gate insulation from the S/D	SiN liner 2nm	None other than GeO_2
S/D Metal	Al +SiN 2nm (depinning)	Al +GeO_x 2nm (depinning)
Preclean	Wet treatment + nitride liner deposition	Oxidation before deposition
Metal deposition	N.S.	Thermal evap.
Germanidation anneal	No germanidation	No germanidation
Selective removal	No germanidation	No germanidation
Extracted SBH	Φ_{bn}=0.1eV	Φ_{bn}=0.17eV
Gate length (µm)	1.5	190
Subthreshold swing (mV/dec)	N.S.	N.S.
I_{on}/I_{off} (dec)	~1	~1

Table IV-6: Summary of the main fabrication steps and results of state-of-the-art n-SBFETs on Ge. N.S. stands for "Not Specified". I_{on} and I_{off} are defined relative to V_{th}.

Chapter IV. - References

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Chapter V. Summary and conclusion

We shall now recapitulate the main findings of each chapter in this thesis and, and thus conclude on the conditions under which the combination of metallic Source/Drain and a Germanium-based channel would be relevant and beneficial for aggressively scaled CMOS integration.

V.1. Metal/Semiconductor contacts

In reverse bias (current flowing from the metal towards the semiconductor), the interfacial current density across a metal/semiconductor contact is extremely dependent on the Schottky barrier height and shape. Besides, the barrier height and shape are generally extremely dependent on the doping level at the semiconductor interface and on the applied bias.

On Silicon and to a larger extent on Germanium, the formation of the Schottky barrier is strongly influenced by the phenomenon of pinning of the Fermi-level to a surface charge neutrality level located close to the Valence Band. As a consequence, the majority of metal/Si and metal/Ge contacts exhibit a strong preference for holes injection, with a weak dependence on metal workfunction. However, these barriers might still not be low enough to fulfil the ITRS requirements for contact resistivity, unless the semiconductor is highly doped. Therefore, we focused on contacts on p-type degenerate semiconductors in reverse bias, characterized by both low and thin Schottky barriers.

Regarding the prediction of the contact resistivity in such configurations, assuming we know exactly the intrinsic Schottky Barrier Height corresponding to a given metal and doping level values in the semiconductor:

- The simplifying assumption of pure thermionic emission current is irrelevant
- Even the simplifying assumption of **one** dominant current transport (should it be TE, TFE or FE) can be insufficient, as we have shown that the thermionic and field-emission processes could equally coexist at 0V or -1V bias on the semiconductor for the cases of interest

For quantitative evaluation, considering all the transport processes at once and not resorting to the simplified current density expressions, we still meet the following limitations:

- The use of the classical formulation of image force does not yield the same barrier height, or shape, than the self-consistent quantum-mechanical-based approach which is *a priori* more sound (no diverging potential issue, no assumption of point charges in the forbidden barrier region). This leads to an overestimation of the current density, and an underestimation of the contact resistivity.

- The current density varies linearly with the effective Richardson constant A^*, which is itself the result of several approximations: on the carriers effective mass values and on the distribution of states available for conduction (cf. "effective reduced" Richardson constant A^{**})

The above state facts led us to remark that at this point, it was somewhat illusory to pretend to precisely conclude on the required metal and doping level to meet the ITRS specifications for contact resistivity.

Qualitatively though, according to our 1-D case of study, even if the intrinsic SBH could be lowered to a value of 0eV (which in practice would require Fermi-level depinning), the contact resistivity on an undoped semiconductor at V=-1V would be superior of roughly one order of magnitude with respect to that of a contact on degenerately doped Si or Ge. This trend is even more pronounced for larger SBH values (at zero bias and on Ge: a difference of 2 orders of magnitude was observed at Φ_{bp0}=0.4eV between the cases $N_A=8.10^{18}$ at.cm^{-3} vs. $N_A=10^{20}$ at.cm^{-3}). We are therefore tempted to conclude that even in the most favorable case of metallization (for holes: Pt-based contacts on Si or Ge), the highest possible doping level at the interface is required so as not to lose in contact resistivity what has been earned in access sheet resistivity.

Yet, we should keep in mind these values are based on the assumption that the distance between the two electrodes is superior to the SCR width. In practice, if the distance between Source and Gate is less than W_{dep}, the barrier might become thinner and ρ_c lower. This calls for further examination in the framework of the Schottky-Barrier FET device as a whole.

V.2. Schottky-Barrier transistors on SOI

Replacing doped junctions by metal/semiconductor junctions in the Source and Drain of MOSFETs was originally considered for series resistance reduction, low temperature processing, immunity to SCE, and parasitic bipolar effects elimination. This last advantage can be directly discarded when it comes to device integration on Fully-Depleted SOI.

Concerning the first one, series resistance, the conclusion is not as obvious as it might first seem, as we have seen in Chapter II. As a rule of thumb, the contact resistivity should be kept below a maximum of 10^{-8} Ω.cm^2 [*Poiroux'09*], which does not occur naturally in metal-to-undoped Si contacts. If interfacial doping is the solution, then its implementation is likely to make the advantage of SCE immunity vanish.

Furthermore, a first-order analysis of the operation of a Schottky-Barrier MOSFET shows that for the usual range of biasing conditions (V_{dd}~1V), interfacial doping is required

not only to improve carrier injection in the On-State, but also to limit leakage current in the Off-State. It can be also necessary to avoid a degradation of the subthreshold swing which would typically occur otherwise in underlapped geometries. The resulting trade-off between performance and scalability in Schottky Barrier MOSFETs with interfacial doping has been investigated in [*Hutin'09*] with the demonstration of Single and Double Gate p-SBFETs with L_G down to 20nm.

In this particular study, neither the ON-State current nor the series resistance do strikingly outperform the state-of-the-art of conventional MOSFETs with doped S/D. Moreover, the use of Double Gate architectures seems necessary to recover the electrostatic integrity degraded by the implementation of highly-doped extensions (reducing the gate electrical length). Yet, the doping process implemented in [*Hutin'09*], Implantation Before Silicidation (IBS), is not *a priori* the most efficient technique to obtain abrupt doping profiles [*Dubois'08*].

Alternate solutions exist such as the Implantation Through Silicide (ITS) used in [*Khater'10*]. This recent publication demonstrates good electrical characteristics of both nFETs and pFETs with L_G down to 20nm with a single S/D metal and a low temperature process. These results are a step ahead of the dual metal S/D approach, currently held back by challenges related to the difficult integration of rare earth silicides having a preference for electrons injection [*Breil'09*].

Yet, this paper also shows that in spite of some of the lowest contact resistivities achieved to this day ($\rho_c = 6\sim7\times10^{-9}$ $\Omega.cm^2$ measured on similar contacts in [*Zhang'10*]) and no underlap between Gate and Source, the SBFET on SOI is still "running behind" the conventional SOI MOSFET in terms of performance. Of course there might be room for process optimization, but it still casts serious doubts over the hopes that in non-underlapped geometries (Source and Gate vertically aligned), the screening of the Schottky junction built-in potential by the Gate bias could eventually make contacts on undoped semiconductor compete with p/n junction in terms of carrier injection efficiency (cf. conclusion of last paragraph). In other words, this further points towards the need for interfacial doping on SOI.
The development of the fully-metallic Source and Drain technological modules does not look like an absolute necessity for improving the performance and scalability of planar, symmetrical single gate devices on FDSOI. Yet, it can be of prime importance in the elaboration of different architectures, such as the vertical Double Gate transistor presented in [*Vinet'09*]. Additionally, the segregation techniques can also be a solution for low-temperature junction formation.

We can finally remark that the constraints arising from SBH modulation through interfacial doping, and in particular the activation level needed, could be alleviated on lower-bandgap semiconductors such as Germanium or Silicon-Germanium alloys.

V.3. Ge-based devices

V.3.1. **Transistors on GeOI**

Due to its *a priori* superior transport properties, the Germanium MOSFET has seen a regain of interest after four decades of relative inactivity on the topic. This is linked to the introduction of high-k gate dielectrics, as the Germanium native oxide GeO_2 suffered from limited thermal stability and water solubility.

Yet, the Ge/high-k interfaces are most of the time not very good (degraded C-V characteristics) unless special care is taken in terms of interface passivation. Over the last few years, a partially oxidized Si capping has been developed as a scalable interlayer for that purpose, and has led to the fabrication of deep sub-micron Ge pFETs, down to a record of L_G=30nm [*Hutin'10-a&b*]. However, the resulting interface state densities are still a concern for the realization of Ge CMOS.

Indeed, it has been shown that an intrinsically large density of acceptor surface states was causing the Ge surfaces to electrically behave as if they were p-type [*Dimoulas'06*], [*Tsipas'09*]. This causes $V_{th,p}$ shifts towards positive values for pFETs, and hardly functional nFETs due to Coulomb scattering and a delayed n-type inversion at positive gate biases. Although the $V_{th,p}$ shift can be corrected by means of Ge film n-type counterdoping, it causes the holes mobility to be reduced to values close to those in Silicon [*Romanjek'08*], [*Hutin'10-a*]. Besides, the subthreshold swing remains non-ideal in long-channel devices due to the D_{it} (~100 mV/dec instead of 60 mV/dec at 300K).

The best way known to date in order to passivate a maximum of these acceptor states is through the implementation of GeO_2 interlayers (ironically, as GeO_2 used to be the reason why Ge was abandoned), but it implies a very low thermal budget processing (low temperature dopant activation or gate-last integration scheme). Moreover, concerns have been expressed in terms of GeO_2 IL scalability [*Caymax'09*].

Additionally for nFETs, the low solid solubility and high diffusivities of donor impurity species (As, P) make their realization even more difficult. As a result, attempts were made towards Dual Channel p-GeOI/n-SOI co-integration rather than towards pure Ge CMOS [*Le Royer'10*]. However, even on On-Insulator substrates, tunnel leakage currents at the Drain owing to the low bandgap of Ge limit the OFF-State characteristics for supply voltages larger than 0.7V.

Two solutions can be proposed to address these problems:

- The low-temperature formation of metallic Source and Drain could be more compatible with the passivating interlayer thermal stability, and remediate the problem of the high diffusivity of n-type dopants above 550°C.

- The use of SiGe alloys, with lower effective masses than in Si but a large bandgap and lower interface states density than in Ge could partially solve the issues of $V_{th,p}$ shifts and reduce the TAT, BTBT-induced junction leakage. Furthermore, the critical thickness of SiGe/Si heteroepitaxy is larger than for Ge, meaning less problems regarding the crystal defectivity, and the possibility to fabricate pFETs on fully compressively strained SiGe.

V.3.2. **Transistors on compressively-strained SGOI**

We demonstrated in [*Hutin'10-c*] transistors with gate lengths down to 20nm (nFETs and pFETs) compressively strained SGOI showing mobility enhancements over the SOI reference, especially at narrow channel widths where the process of elastic strain relaxation leads to a beneficial uniaxial stress in the direction of transport. However, the nFETs performance is not as good as on SOI (as the compressive stress is not good for electrons mobility), and the integration scheme based on Ge enrichment is currently not applicable at the device level.

A Dual Strained Channel co-integration scheme by selective SiGe epitaxy on SOI and sSOI was then demonstrated in [*Hutin'10-d*] down to L_G=17nm with functional 6T-SRAM cells and ring oscillators. The trade-off between mobility enhancement and $V_{th,p}$ shift with the Ge content was evidenced, along with the critical technological processes to optimize it (avoiding SiGe overetch in the S/D, and minimizing the D_{it} through gate stack passivation).

As a matter of fact, in [*Hutin'10-c&d*], although the tunnel leakage component seem to have been effectively reduced, the $V_{th,p}$ values still seem to undergo a too large shift, causing a high I_D at V_{GS}=0V. This $V_{th,p}$ shift is partly due to the band structure (reduced bandgap plus additional contribution of the compressive strain), but also to fixed charge and interface states density. This indicates that the gate stack passivation might still be a significant issue even at moderately high Ge contents (20-40%).

V.4. Ge channel and metallic Source/Drain

We have identified the use of Ge-based channels for SBFETs as an alternative to SOI, stressed by the need for lower intrinsic SBH provided by low bandgap materials. This was the reason already evoked in the introduction (Chapter I). Chapter II and Chapter III confirmed that an interfacial doping layer was necessary on SOI, and probably not even sufficient to compare with conventional SOI MOSFETs in terms of performance.

Conversely, we have identified Ge SBFETs as an alternative to conventional MOSFETs for Ge CMOS, but not exactly for the reasons cited in Chapter I.

In fact, as the study of the state-of-the-art of Ge-channel SBFETs shows in section IV.5, there is little chance that undoped metal/Ge interfaces can make competitive devices (high subthreshold swing, low I_{ON}/I_{OFF} ratio). SBFETs are therefore not the solution which could provide atomically abrupt junctions and the absence of n-type doping for Ge CMOS. However, it can provide low temperature activation through dopant segregation, therefore solving the issue of As and P diffusivity above 550°C, and that of the thermal instability of a GeO_2 passivating interlayer.

In conclusion:

- The passivation of acceptor states at the Ge or SiGe surfaces should be treated in priority. Recent studies indicate that low temperature processing is the key to avoid the wrong oxidation states of Ge. GeO_2 interlayers by high pressure oxidation (HPO) followed by low temperature oxidation annealing (LOA) seem like promising candidates [*Nishimura'10*]. But one must determine if they can lead to sub-nanometer EOT without losing their potential [*Caymax'09*].
- Even if the SBH are lower than on SOI, the SBFETs on Ge or SiGe most probably need dopant-segregated Source and Drain for performance optimization. The ITS technique seems to be the most efficient, and the drive-in anneal should be performed at low temperature so as not to degrade the gate stack passivation layer. This way, there is no need to resort to a gate-last integration scheme, and the high diffusivity of As and P in Ge should no longer be a source of concern. For a single S/D metal approach, NiGe is arguably the most appropriate choice, and the selective removal of the unreacted metal is easier than in the case of Pt germanidation.

These are the conditions under which the respective advantages of Ge channel and Schottky Source and Drain could cumulate. The feasibility of the first condition for aggressive nodes remains to be established, and the interest of the second one in terms of performance and scalability with respect to the conventional Si-based MOSFET remains to be quantified.

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Résumé en français

Chapter II. Contacts Métal/Semi-conducteur

II.1. Théorie des jonctions Schottky

II.1.1. Formation de la barrière Schottky

La barrière de potentiel qui se forme lorsqu'un métal et un semi-conducteur entrent en contact n'est pas totalement déterminée par l'affinité chimique et le travail de sortie du métal.
En pratique, le niveau de Fermi du semi-conducteur est fixé au niveau de neutralité de charge des états d'interface, d'autant plus fort que la densité d'états d'interface est élevée. Dans le Germanium en particulier, la contrôlabilité de la hauteur de barrière Schottky par le travail de sortie du métal est réduite à environ 5%. Les barrières intrinsèques sont à notre connaissance toujours favorable à l'injection des trous.

De plus, la force image tend à abaisser la hauteur de barrière en fonction du champ électrique ainsi qu'à la rendre plus étroite. Pour des niveaux de dopage élevés et de fortes polarisations, son impact sur le courant par effet tunnel et par conséquent sur la densité de courant totale à l'interface est non négligeable.

II.1.2. Transport de charges à l'interface

La théorie de la diffusion [*Schottky'38*] est incorporée à la théorie « classique » de l'émission thermoïonique [*Bethe'42*] à travers l'usage de la constant de Richardson effective réduite A^{**}. Cependant, cette dernière ainsi que sa dépendance vis-à-vis du champ électrique restent difficile à évaluer. Il est raisonnable en ce qui concerne les semi-conducteurs à haute mobilité tels que le Germanium de négliger l'aspect diffusif, étant donné que la vitesse de diffusion effective des porteurs majoritaires dans la zone de charge d'espace est très grande relativement à la vitesse de recombinaison thermoïonique. L'utilisation de la constante de Richardson effective A^{*}, plus simple à calculer, est justifiable.

Toutefois, ces modèles ainsi que leurs variantes sont surtout adaptés à la prédiction du comportement électrique de jonctions présentant des hauteurs de barrière élevées, avec un niveau de dopage faible, et en polarisation directe (porteurs circulant du semi-conducteur vers le métal). Or, le cas qui nous intéresse en raison des applications ciblées serait plutôt caractérisé par:

- Des hauteurs de barrière faible pour une grande efficacité d'injection
- Des niveaux de dopage élevés pour rendre la barrière plus petite et étroite
- Des polarisations en inverse puisque dans les MOSFETs Schottky, les porteurs sont injectés depuis la Source métallique vers le canal semi-conducteur.

Dans les cas précités, l'hypothèse d'un courant de saturation en inverse dépendant uniquement de la hauteur de barrière, et négliger le profil de la barrière qui conditionne l'émission par effet de champ à travers la barrière n'est plus une démarche acceptable. Prendre en compte la composante d'émission par effet de champ n'est pas immédiat, puisque qu'il faut en toute rigueur intégrer les probabilités d'occupation et de disponibilité des états énergétiques de chaque côté de la jonction, puis multiplier par le coefficient de transmission. Il existe au moins deux approches simplificatrices.

La première, qui repose sur l'utilisation d'un facteur d'idéalité η pour évaluer dans quelle mesure les caractéristiques s'éloignent du cas de l'émission thermoïonique pure (TE) en polarisation directe, reste très qualitative. La seconde [*Padovani'66*], [*Crowell'69-a*] qui propose des expressions simplifiées des densités de

courant dans les cas où les régimes TFE (émission par effet de champ des porteurs thermalisés) ou FE (émission par effet de champ) dominent, semble plus adaptée. En dépit d'imperfections des modèles jetant le doute sur la pertinence d'une comparaison directe avec des caractéristiques J-V expérimentales (fiabilité limité à de faibles valeurs de polarisation directe), l'avantage de cette approche consiste en la possibilité de dériver des résistivités de contact spécifiques pour des contacts ohmiques ou quasi-ohmiques sur semi-conducteurs dégénérés.

Tous ces modèles décrivent le transport des porteurs majoritaires, sous l'hypothèse de l'absence d'une éventuelle couche d'interface séparant le métal du semi-conducteur. A champs électriques élevés, la dérive des minoritaires peut prendre de l'importance dans le cas des semi-conducteurs faiblement dopés. A champs faibles, la présence d'une fine couche isolante (de 1 à 3nm d'épaisseur) peut affecter le phénomène d'ancrage du niveau de Fermi, ainsi que la densité de courant associée aux porteurs majoritaires.

II.2. Méthodes expérimentales de caractérisation de la barrière

La caractérisation précise de la hauteur d'une barrière Schottky n'est pas triviale, surtout lorsque l'on s'éloigne du cas idéal consistant en 100% d'émission thermoïonique au-dessus d'une barrière haute sur des semi-conducteurs non-dégénérés (cf. techniques C-V et photoémission), et d'une densité de courant suivant une loi d'Arrhenius (cf. techniques I-V et énergie d'activation).

Comme précisé précédemment, ce cas n'est pas pertinent pour les applications visées dans ce travail. Les études présentées dans le paragraphe II.2.6. du manuscrit montrent qu'il n'est pas facile de dé-corréler les contributions des mécanismes TE, TFE et FE. Leurs dépendances respectives en fonction de la hauteur de barrière et du dopage à l'interface ainsi que leurs importances relatives peuvent parfois se révéler contre-intuitives.

De plus, même si tous les paramètres requis pour tenir compte des composantes tunnel sont déterminés avec précaution, il n'est pas garanti qu'utiliser une expression approximative de la densité de courant correspondant à un mécanisme de transport supposé dominant (et négliger tous les autres) conduise à une évaluation fiable de la hauteur de barrière Schottky.

II.3. Modèle analytique à une dimension

Dans cette partie, nous nous sommes concentrés sur le modèle analytique à une dimension d'une diode métal/p-Si. Sans avoir recours aux expressions simplifiées, nous avons calculé les contributions respectives des courants thermoïonique et tunnel pour différentes conditions de dopage, température et différentes hauteurs de barrière Schottky (SBH). Le but est de fournir une compréhension plus fine des processus et dépendances en jeu dans l'émission de porteurs majoritaires à la source d'un MOSFET Schottky.

Le niveau de Fermi étant principalement ancré (dans le Si comme le Ge) du côté de la bande de valence, l'application la plus naturelle est celle du pMOSFET (canal semi-conducteur de type p).

II.3.1. **Dépendances**

II.3.1.a. Comportement ohmique et résistivité de contact

Un contact ohmique, c'est à dire une caractéristique J-V complètement linéaire, serait le cas idéal puisqu'il maximiserait la densité de courant en polarisation inverse (et ainsi l'injection à la Source d'un

MOSFET). Cependant, cela ne peut arriver que si les charges provenant du métal ne rencontrent aucune barrière (0% de courant tunnel), auquel cas la probabilité de transmission serait inférieure à 1. A 300K, cela nécessiterait une SBH négative, afin de compenser l'étalement de la distribution des porteurs autour du niveau de Fermi.

En pratique, la résistivité de contact évolue avec la tension appliquée, tout comme la proportion de courant tunnel. Bien que sa valeur dynamique à V=0 soit une figure de mérite standardisée, une définition plus pertinente du point de vue des applications MOSFET serait sa valeur statique $(J/V)^{-1}$ au point de fonctionnement du contact $V=V_{op}$, ce qui requiert de résoudre le partage du potentiel dans le canal et les accès lorsque $V_{GS}=V_{DS}=V_{dd}$ (la tension d'alimentation).

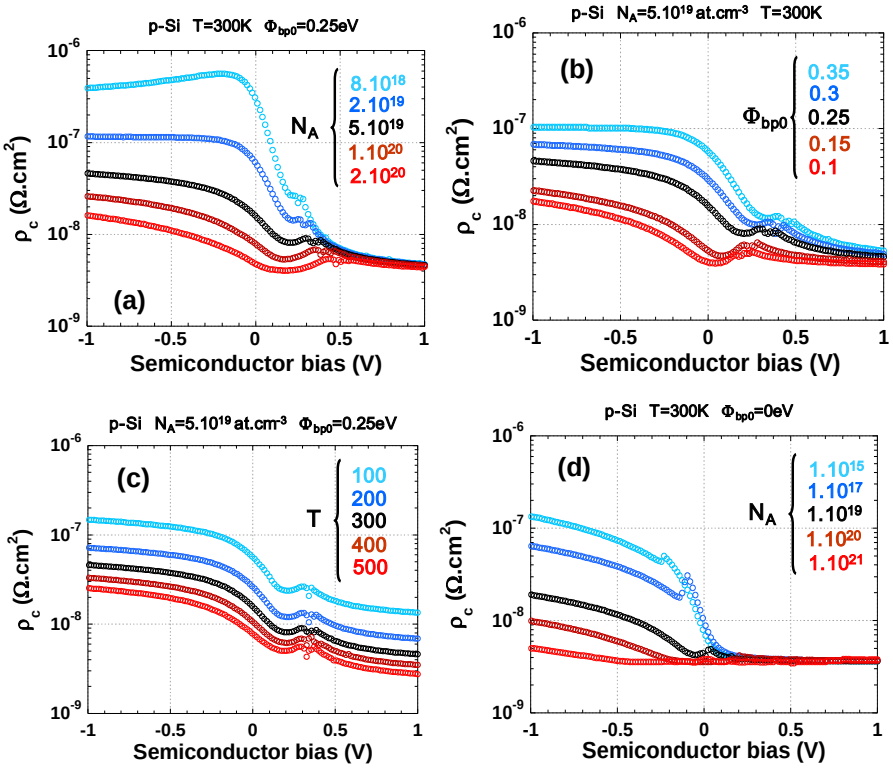

Figure II-1: Résistivité de contact définie par V/J en fonction de la tension appliquée du côté Si pour diverses a) concentrations d'impuretés acceptrices (b) SBH intrinsèques (c) températures. Le cas (d) montre l'influence du niveau de dopage pour un contact avec une SBH intrinsèque égale à 0eV (la SBH effective peut devenir négative à N_A élevé).

Dans la perspective d'un MOSFET « conventionnel » à Source et Drain dopés et accès siliciurés, ces valeurs de ρ_c peuvent être comparées avec les plus récentes spécifications de l'ITRS pour l'intégration sur SOI en désertion totale (Table II-2).

Year of production	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*
Contact maximum resistivity for FDSOI MPU/ASIC ($\Omega.cm^{-2}$)	**4.10^{-8}**	**2.10^{-8}**	**10^{-8}**	**8.10^{-9}**	**7.10^{-9}**	**6.10^{-9}**	**5.10^{-9}**

Manufacturable solution exist, and are being optimized

Manufacturable solutions are known

Manufacturable solutions are NOT known

Table II-1: Spécifications de l'ITRS 2009 pour la résistivité de contact spécifique maximale dans la catégorie FDSOI MPU/ASIC.

II.3.1.b. Cas des contacts Métal/Ge

L'examen des paramètres associés aux contacts sur Germanium (orientation de surface (100)), permettent de fournir des éléments de réponse qualitatifs concernant leurs propriétés électriques.

5. Dans le Ge, **les masses effectives des trous sont plus légères** que dans le Si, ce qui implique:
   - **des probabilités de transmission plus élevées** pour une largeur de barrière donnée, c'est-à-dire une émission par effet tunnel facilitée.
   - mais **une plus faible constante de Richardson A^***, soit un courant de recombinaison thermoïonique typiquement plus faible.
6. La **permittivité électrique du Germanium est plus élevée** que celle du Silicium:
   - **l'abaissement de la hauteur de barrière dû à la force image est plus faible** que dans le Si. Pour une SBH intrinsèque donnée, le courant TE sera *a priori* moindre.
   - **les zones de désertion sont plus étendues**. Les barrières de potentiel tendront donc à être plus larges que dans le Si dans les mêmes conditions de dopage et de température.
7. **L'ancrage du niveau de Fermi est plus fort et le niveau de neutralité de charge encore plus près de la bande de valence** que pour le Si:
   - **Typiquement, les hauteurs de barrière sont plus faibles pour les trous** dans le Ge (PtGe/Ge: Φ_{bp0}=0.06eV, vs. PtSi/Si: Φ_{bp0}=0.25eV).
8. La **mobilité des trous est plus grande** dans le Ge:
   - **A^{**} devrait être plus proche de A^* dans le Ge que dans le Si**, ce qui pourrait contrebalancer le fait que $A^*_{Si}>A^*_{Ge}$. Bien que ceci ne soit pas pris en compte dans les calculs de cette partie, rappelons que J varie linéairement avec la constante de Richardson, et que A^{**} peut se trouver entre A^* et $A^*/2$ dans le Silicium [*Andrews'70*].

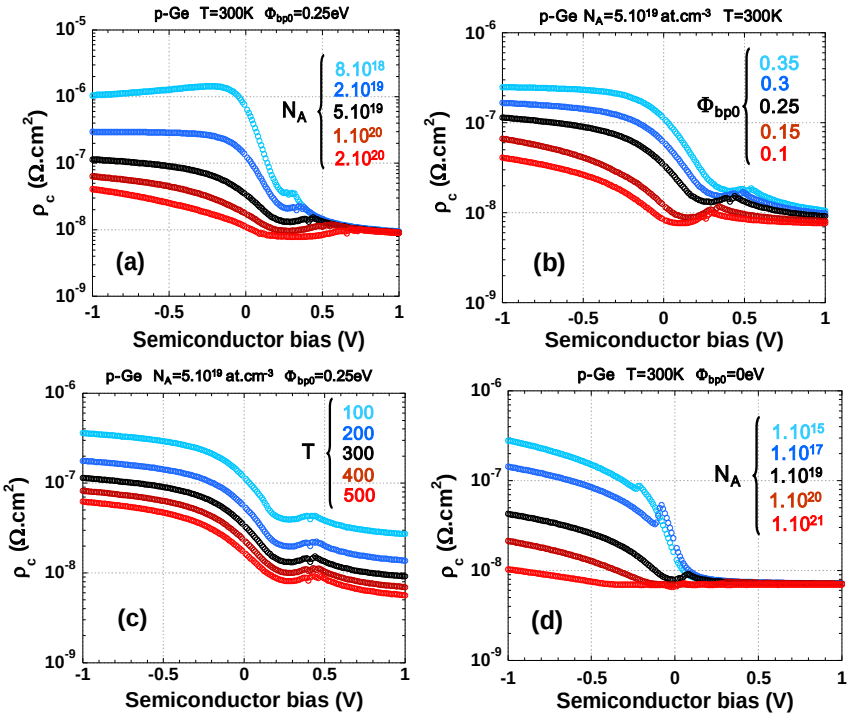

Figure II-2: Résistivité de contact définie par V/J en fonction de la tension appliquée du côté Ge pour diverses a) concentrations d'impuretés acceptrices (b) SBH intrinsèques (c) températures. Le cas (d) montre l'influence du niveau de dopage pour un contact avec une SBH intrinsèque égale à 0eV (la SBH effective peut devenir négative à N_A élevé).

En réalité, nous pouvons voir sur la Figure II-36 que les ordres de grandeur sont essentiellement les mêmes. Quantitativement, les résistivités de contact spécifiques sont plus élevées dans le Ge dans des conditions identiques, ce qui est notamment dû à une constante de Richardson plus faible (voir cependant la remarque sur A^{**} ci-dessus) ainsi qu'à un plus faible pourcentage de courant TE dû à l'impact moindre de la force image.

Quoiqu'il en soit, pour une métallisation donnée, la SBH intrinsèque sur Ge est souvent plus faible que sur Si, ce qui compense ce désavantage (Figure II-37).

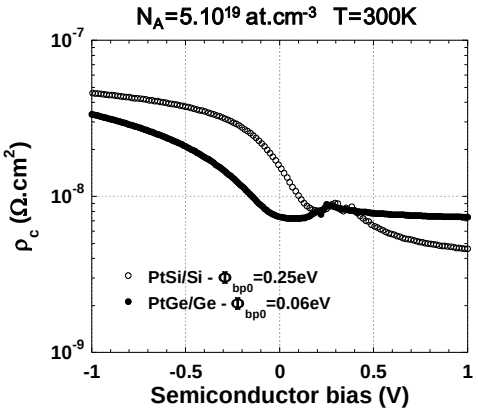

Figure II-3: Résistivité de contact définie par V/J en fonction de la tension appliqué du côté semi-conducteur) 300K et pour un niveau de dopage $N_A=5.10^{19}at.cm^{-3}$. Les cercles vides correspondent à un contact sur p-Si avec une SBH intrinsèque de 0.25eV (PtSi/Si). Les cercles pleins correspondent à un contact sur Ge avec une SBH intrinsèque de 0.06eV (PtGe/Ge).

La résistivité de contact sur Ge est tracée ci-dessous (à 0V et -1V) en fonction de la SBH intrinsèque pour divers niveaux de dopage.

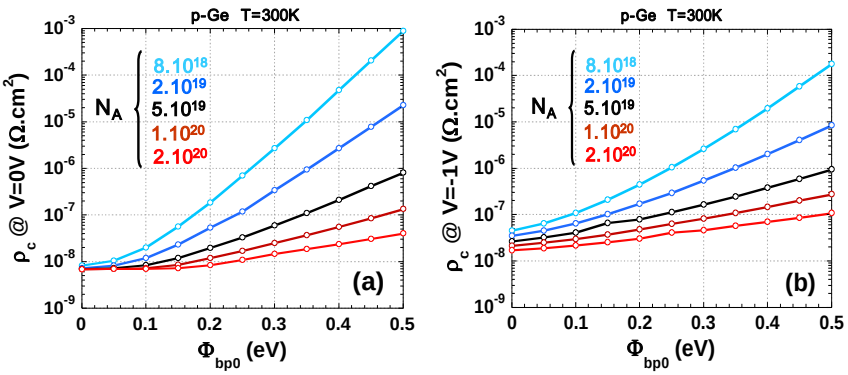

Figure II-4: Résistivité de contact sur Ge à 300K en fonction de la SBH intrinsèque pour les trous, pour divers niveaux de dopage et calculée (a) à V=0V et (b) à V=-1V.

II.4. Conclusion

La prédiction quantitative du comportement électrique d'une jonction Schottky est moins triviale qu'il n'y paraît au premier regard. Cependant, afin de conclure sur les caractéristiques requises pour qu'un contact métal/semi-conducteur soit adéquat pour des applications de logique CMOS, nous pouvons faire la Remarque

suivante. La résistivité de contact en polarisation inverse (porteurs circulant du métal vers le semi-conducteur) atteint son minimum lorsque la barrière disparaît **et** lorsque le niveau de Fermi du semi-conducteur franchit le seuil de la bande de valence (ou de la bande de conduction), de sorte à maximiser le nombre d'états disponibles pour les porteurs provenant du métal (cf. résistivité de contact à SBH=0eV sur Si ou Ge faiblement dopé Figure II-35 et Figure II-36). Dans le cas des MOSFETs, l'approche « Schottky pure » (c'est-à-dire sans dopage à l'interface) est intéressante pour le contrôle des effets de canaux courts (SCE). Mais, selon les calculs 1-D, même pour une SBH de 0eV (ce qui en pratique requerrait une couche d'interface visant à désancrer le niveau de Fermi), la résistivité de contact à V=-1V sur un semi-conducteur non-dopé serait supérieure d'environ un ordre de magnitude par rapport à celle d'un contact sur Si ou Ge dégénéré (cf. les cas $N_A=10^{15}$ at.cm^{-3} et $N_A=10^{20}$ at.cm^{-3}). Cette tendance est encore plus prononcée pour des valeurs supérieures de SBH (cf. Figure II-38). Cependant, rappelons que ces considérations quantitatives sont basées sur l'hypothèse que la distance entre les deux électrodes est supérieure à l'étendue de la zone de charge d'espace. En pratique, si la distance entre la Source et la Grille est inférieure à W_{dep}, la barrière peut devenir plus fine et ρ_c s'en trouver diminuée.

Il semble cependant qu'en dépit des avantages qu'une jonction atomiquement abrupte sur un semi-conducteur non dopé procurerait en termes de contrôle électrostatique, un niveau de dopage élevé à l'interface soit inévitable pour optimiser l'efficacité d'injection des porteurs à la Source. Une solution intermédiaire consisterait en obtenir le plus haut niveau de dopage possible tout en contrôlant le gradient latéral d'impuretés à l'entrée du canal. La différence d'une telle approche par rapport à celle du MOSFET « traditionnel » à jonction p/n et accès siliciurés serait alors ténue.

Chapter III. Le MOSFET à barrière Schottky sur substrat SOI

III.1. Introduction

III.1.1. Historique du MOSFET à barrière Schottky

L'idée d'utiliser des Source et Drain métalliques en lieu et place des jonctions p/n a d'abord été proposée par Yoshio Nishi en 1966, lequel a soumis un brevet publié en 1970 [*Nishi'70*]. Le premier papier sur le sujet fut publié en 1968 par Lepselter et Sze [*Lepselter'68*], s'agissant d'un pFET sur Silicium massif avec des Source et Drain en PtSi. Néanmoins, les performances limitées du dispositif présenté (courant à l'état passant inférieur d'un ordre de grandeur à ceux des MOSFETs conventionnels de l'époque) a débouché sur une décennie d'inactivité dans le domaine.

Un peu plus de dix ans plus tard, Koenecke a montré la forte dépendance du courant passant vis-à-vis de la distance entre le bord de grille et les S/D [*Koenecke'81*]. Ceci provoqua un regain d'intérêt pour les transistors Schottky, avec des études portant sur:

- Les avantages d'une couche de dopage d'interface pour augmenter le courant à l'état passant [*Koenecke'82*], [*Oh'84*], [*Swirhun'85*]
- Une première démonstration de nFET Schottky [*Mochizuki'84*]

- Des dispositifs asymétriques à Source métallique et Drain dopé sur Silicium [*Tsui'89*], [*Kimura'94*].

Il a également été démontré que l'implémentation de SBFETs pouvait éliminer les effets bipolaires parasites [*Sugino'82*], [*Sugino'83*], [*Swirhun'85*], par le biais d'une structure CMOS comprenant un nFET conventionnel et un pFET à barrière Schottky.

Depuis 1994, le SBFET a été étudié à la lumière de ses avantages pour les nœuds technologiques avancés [*Tucker'94-a*], [*Tucker'94-b*], [*Snyder'96*], ce qui a mené à des progrès significatifs du point de vue de l'état de l'art des procédés technologiques de fabrication.

III.1.2. **Les raisons de choisir des Source et Drain métalliques**

La Table III-1 ci-dessous résume les avantages supposes des MOSFETs à Source et Drain métalliques, et les conditions suivant lesquelles ces avantages restent pertinent dans le cadre d'une intégration sur substrat Silicon On Insulator (SOI).

Avantages	**Raisons**	**Remarques**
Réduction des résistances série	Faible résistivité de couche du métal	Avantage conservé sur SOI mince seulement si $\rho_c<10^{-8}$ Ω.cm^2 **Le dopage d'interface semble inévitable**
Fabrication à basse température	Siliciuration à basse température	Si un dopage d'interface est requis, **il est toujours possible d'activer les dopants grâce aux techniques de ségrégation**
SCE, variabilité	Immunité aux SCE et aux sources de variabilité associées	Valable si **pas de dopage**, et sans tenir compte de la **variabilité associée à l'inhomogénéité de Φ_b**
Effets bipolaires parasites	Les jonctions Schottky sont de mauvais émetteurs bipolaires	Latch-up: **seulement pertinent sur substrats massifs** Single transistor latch: **vrai s'il n'y a pas de dopage**, et seulement pertinent sur les substrats SOI partiellement désertés (PDSOI)

Table III-1: Résumé des avantages supposés des MOSFETs Schottky, et remarques relatives à la validité de ces avantages dans le cadre d'une intégration sur substrats SOI.

Le fait qu'il n'existe pas de métal connu pouvant fournir une SBH intrinsèque suffisamment faible pour satisfaire les conditions sur ρ_c met en évidence la nécessité de procéder à un dopage d'interface. Par conséquent, sur les substrats SOI, les seuls avantages qui subsistent par rapport à, par exemple, l'intégration de MOSFETs conventionnels à S/D partiellement siliciurés, sont le bas budget thermique de fabrication ainsi qu'**éventuellement** la réduction des résistances série.

III.2. Caractéristiques statiques des SBFETs

III.2.1. **Etat passant, état bloqué**

Considérons les exemples d'un pMOSFET conventionnel et celui d'un SBFET avec une barrière favorable à l'injection des trous (par exemple avec des Source et Drain à base de Pt ou Ni). Les conditions de polarisation à l'état bloqué sont définies par V_{GS}=0V et V_{DS}=V_{dd}<0V et à l'état passant par V_{GS}=V_{DS}=V_{dd}<0V.

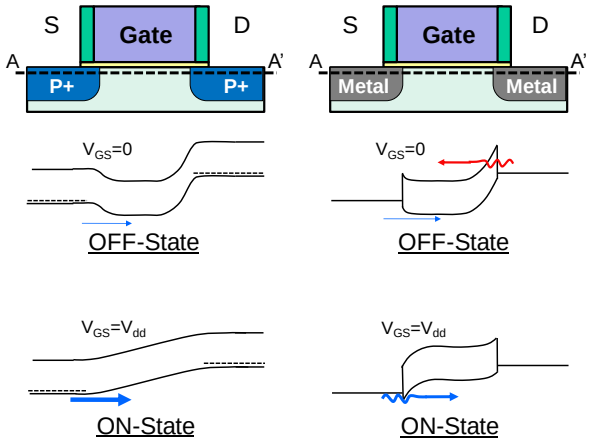

Figure III-1: Diagrammes de bandes longitudinaux simplifiés à l'état bloqué et à l'état passant pour un pFET conventionnel (à gauche) et pour un SBFET avec une faible barrière pour les trous (à droite).

Cas du MOSFET conventionnel

A l'état bloqué, les trous du côté de la Source font face à une barrière de potentiel émanant du potentiel interne de la jonction p/n (Ψ_{bi}) et correspondant à la différence des niveaux de Fermi entre la Source et le canal (*a priori* non dopé). Le courant de fuite est déterminé par la diffusion des trous dans la zone de charge d'espace. Du côté du Drain, la concentration en électrons est aussi négligeable que la concentration d'impuretés acceptrices ionisées est élevée. Il n'y a en principe pas de flux significatif d'électrons dérivant du Drain vers la Source, si ce n'est pour d'éventuels effets de Tunnel Bande à Bande (BTBT, qui se déclenche typiquement lorsque $V_{GD}+\Psi_{bi}>E_g/q$).

A l'état passant, dans la couche d'inversion, la barrière de potentiel disparaît et les trous peuvent circuler librement de la Source vers le Drain.

Cas du SBFET

A l'état bloqué, les trous du côté de la Source font face à une barrière abrupte résultant des mécanismes décrits dans le chapitre II. Pour garantir une injection efficace, cette barrière est choisie faible. Plus cette barrière est faible, plus elle est facile à franchir pour les porteurs ayant reçu une énergie thermique, ce qui a pour conséquence un courant de fuite associé à la circulation de trous de la Source vers le Drain. **De plus**, à la différence des MOSFETs conventionnels, le Drain métallique agit comme un réservoir d'électrons, lesquels peuvent la plupart du temps franchir la barrière de potentiel rendue étroite par la différence de potentiel entre la Grille et le Drain (il s'agit donc d'un flux d'électrons du Drain vers la Source). Ce comportement ambipolaire est caractéristique des MOSFETs Schottky, mais est indésirable dans le sens où il peut augmenter considérablement le courant à l'état bloqué.

A l'état passant, la jonction Source-Canal est en polarisation inverse, ce qui favorise l'émission thermoïonique (grâce à la force image) et facilite la transmission par effet tunnel du côté de la Source. Côté Drain, il devient impossible pour les électrons de franchir la barrière par effet tunnel.

L'ajout d'une couche dopée de type p à l'interface résulte en deux avantages, comme indiqué sur la Figure III-5 ci-dessous.

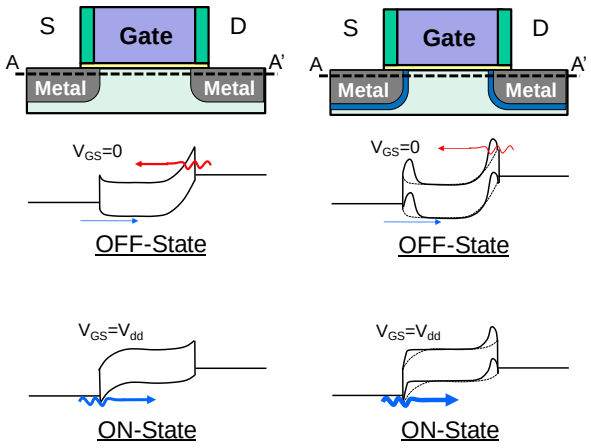

Figure III-2: Diagrammes de bandes longitudinaux simplifiés à l'état bloqué et à l'état passant pour un SBFET sans couche de dopage d'interface (à gauche) et pour la même structure avec une couche dopée de type p à l'interface (à droite). Les pointillés superposés à droite indiquent la configuration de bandes dans le cas non-dopé de gauche.

D'un côté, le dopage d'interface augmente le courant à l'état passant en rendant la barrière à la Source plus basse et plus étroite en polarisation inverse. De l'autre côté, la barrière côté Drain est augmentée à l'état bloqué, ce qui limite le courant de fuite associé aux électrons circulant du Drain vers la Source.

Avant de conclure qualitativement sur les hauteurs de barrière requises pour obtenir des contacts ohmiques à l'injection, il est important de mentionner une différence fondamentale entre les cas étudiés dans le chapitre précédent et la configuration électrostatique d'un MOSFET. Auparavant, nous avons traité la tension appliquée côté semi-conducteur comme une condition limite à l'infini de sorte que la zone de charge d'espace puisse se construire sur toute sa largeur. Dans un SBFET, si la distance entre Source et Grille est inférieure à la largeur de la ZCE, le potentiel interne de la jonction Schottky peut être écranté par la tension de Grille, de sorte que la densité de courant résultante n'est pas équivalente aux cas traités précédemment.

La distance horizontale entre bord de grille et bord de Source ou Drain est en réalité un paramètre important à considérer pour l'étude de l'état bloqué, de l'état passant et du régime sous le seuil d'un SBFET.

III.2.2. **Régime sous le seuil dans le cas FDSOI**

L'état bloqué d'un SBFET peut aussi être limité par ses caractéristiques dans le régime sous le seuil. Une approximation de la pente sous le seuil dans un SBFET à canal non dopé sur SOI a été proposée par Knoch *et al.* [*Knoch'06*] dans le cas où la Source est alignée avec le bord de Grille.

De façon intuitive, la pente sous le seuil est étroitement liée à l'évolution avec le potentiel de Grille de la probabilité de transmission à travers la barrière côté Source. Si le contact est ohmique (cf. comportement plat de la caractéristique $\rho_c(V)$ en polarisation inverse, comme vu dans le chapitre précédent), l'injection devrait être limitée par l'expansion de la couche d'inversion en fonction de V_G, et la limite idéale des 60mV/dec peut être atteinte dans un dispositif dont le contrôle électrostatique est optimisé. Réciproquement, une barrière importante

et un contact rectificateur ont pour conséquence une limitation du courant à faible V_{GS} qui a nécessairement un impact sur la pente sous le seuil.

Celle-ci peut être améliorée en diminuant l'épaisseur du SOI. S'il existe une zone de non-recouvrement entre la Grille et la Source, elle dépend du dopage du canal ou du dopage à l'interface du contact. Cette dépendance peut disparaître lorsque la zone de non-recouvrement est réduite ou éliminée.

III.3. Intégration des dispositifs SBFETs

III.3.1. Source et Drain damascènes

III.3.1.a. SBFET à Simple Grille

Le procédé de fabrication de dispositifs à Source et Drain métalliques damascènes à Simple Grille [*Poiroux'09*] est une variante du procédé standard FDSOI [*Andrieu'06*] utilisé au Leti. Le Silicium des régions Source et Drain est gravé après définition des espaceurs, et des cavités sont formées par lithographie inversée des zones actives. Une implantation tiltée peut être effectuée avant dépôt du métal des Source et Drain, en l'occurrence 6nm de Platine. Après recuit de siliciuration (à 450°C pour limiter la pénétration du siliciure sous les espaceurs), un empilement W/TiN/Ti est déposé pour remplir les cavités. Le TiN agit comme une barrière de diffusion pour le fluor (lors du dépôt CVD conforme de tungstène par un précurseur WF_6), et des études ont montré que les résistivités de contact étaient nettement diminuées par l'utilisation d'une couche d'accroche Ti. Finalement, le métal est planarisé pour libérer la Grille (Figure III-17).

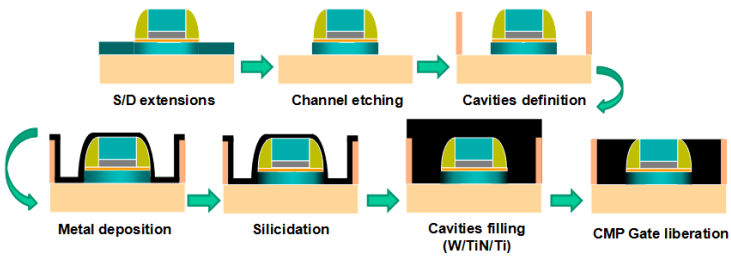

Figure III-3: Schéma d'intégration des Source et Drain métalliques damascènes pour SBFET Simple Grille sur SOI.

La valeur moyenne des résistivités de contact mesurées en utilisant ce procédé de métallisation et dopage d'interface est de 6×10^{-9} $\Omega.cm^2$, en phase avec les recommandations en termes d'optimisation des résistances série pour les MOSFETs à Source et Drain métalliques sur FDSOI [*Su'94*], [*Poiroux'09*]. Les pFETs ainsi fabriqués démontrent de bonnes performances (I_{ON}=345 µA/µm, I_{OFF}=30nA/µm, L_G=50nm, V_{DS}=-1V).

III.3.1.b. SBFET à Double Grille

Ce procédé a également été développé dans sa variante Double Grille [*Vinet'09*], [*Hutin'09*]. En partant de substrats SOI, l'empilement de grille arrière est tout d'abord déposé (3nm ALCVD HfO_2, 5nm PVD TiN, 50nm poly SiGe dopé *in situ*). Après dépôt et planarisation d'un oxyde d'encapsulation, un collage sur substrats de Silicium massif oxydé est effectué. Le canal de Silicium est ensuite gravé et l'empilement de grille avant est formé au-dessus. La Figure III-18 rend compte des étapes qui suivent.

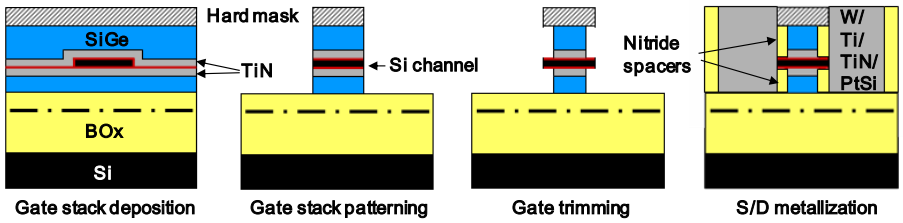

Figure III-4: Schéma simplifié du procédé auto-aligné de fabrication des MOSFETs à Double Grille et Source et Drain métalliques [Vinet'09], [Hutin'09].

L'empilement total (les deux grilles et le canal) est ensuite gravé jusqu'à l'oxyde enterré, par le biais d'une chimie HBr/O_2 pour le SiGe des grilles et le Si du canal, et par BCl_3 pour le diélectrique HfO_2. Les longueurs des grilles avant et arrière en SiGe sont définies simultanément par une gravure plasma sélective et isotrope (CF_4/O_2 laissant le canal et le masque dur intacts), et le TiN est gravé par une solution HCl/H_2O_2. Les extensions sont ensuite implantées, les espaceurs nitrure définis, suite à quoi l'approche S/D damascènes du paragraphe précédent est réalisée. Une vue X-TEM du dispositif final est montrée ci-dessous Figure III-19.

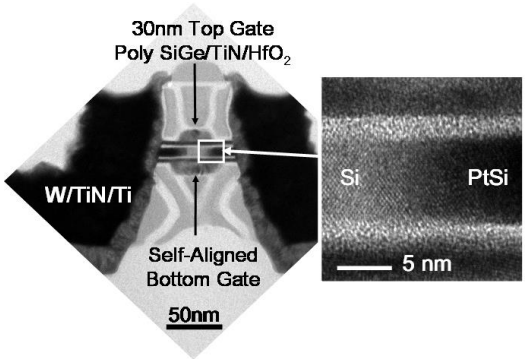

Figure III-5: Image de Microscopie Electronique en Transmission et en section transverse (X-TEM) d'un pFET à Double Grille avec L_g=30nm (à gauche) et zoom sur l'interface PtSi/Si au niveau des S/D (images: D. Lafond).

III.3.2. **Siliciuration auto-alignée suivi d'un retrait sélectif**

L'approche damascène précédemment décrite est particulièrement adaptée pour la fabrication de transistors Double Grille verticaux. Cependant, la définition des cavités ainsi que les étapes de CMP ajoutent une complexité qui peut être évitée pour des dispositifs planaires à Simple Grille. Dans ce cas, une procédure plus de siliciuration auto-alignée adaptée au SBFET consiste en 3 étapes (Figure III-24):

4. Dépôt du métal
5. Recuit de siliciuration
6. Retrait sélectif du métal n'ayant pas réagi pour former le siliciure

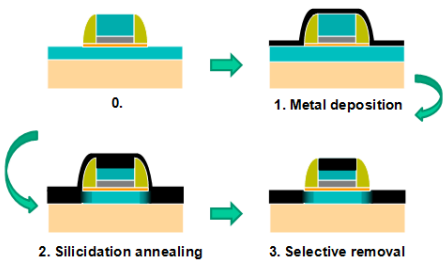

Figure III-6: Schéma simplifié des étapes de silicuration des S/D et retrait sélectif pour fabrication d'un SBFET sur SOI.

La troisième étape est critique puisqu'elle vise à isoler les Source, Drain et Grille, et le retrait doit être sélectif par rapport au siliciure formé à l'étape 2. Nous avons vu dans le chapitre précédent que le Platine était un candidat de choix pour garantir une injection de trous efficace dans les pFETs Schottky. Cependant, en raison de ses propriétés de métal noble, le Platine est difficile à graver et est connu pour ne se dissoudre que dans l'eau régale ($HCl/HNO_3/H_2O$).

On peut noter que l'intégration de siliciures de nickel NiSi au lieu de PtSi, en plus d'être moins chère, représenterait une solution technologique plus aisée en raison de la haute sélectivité de gravure vis-à-vis du Ni non réagi. En outre, le travail de sortie du NiSi est plus proche du milieu du gap du Si ($\Phi_{bp0}\approx 0.5$eV), ce qui en fait un bon candidat pour la réalisation de CMOS Schottky avec un seul métal S/D, mais nécessite plus d'efforts du point de vue des techniques de dopage d'interface pour atteindre les mêmes performances que les pFETs Schottky à base de PtSi.

III.3.3. **Techniques de ségrégation des dopants**

La nécessité de réduire le comportement ambipolaire des SBFETs par une couche d'interface fortement dopée a été soulignée dans ce qui précède. Cependant, afin de ne pas compromettre l'un des plus importants avantages des SBFETs, c'est à dire une certaine immunité aux effets de canaux courts, le profil latéral de dopage doit rester suffisamment abrupt, surtout dans le cadre d'une géométrie à Simple Grille.

III.3.3.a. Principe

Les techniques de ségrégation des dopants consiste à profiter de la tendance à l'accumulation des dopants à l'interface métal/Si pour limiter le budget thermique associé au recuit d'activation, et ainsi limiter la diffusion des dopants dans le canal.
Si l'on se réfère à la Figure III-24, l'implantation des dopants peut avoir lieu:

- Entre les étapes 0 et 1: implantation avant siliciuration (IBS)
- Entre les étapes 1 et 2: implantation à travers le métal (ITM)
- Entre les étapes 2 et 3: implantation à travers le siliciure (ITS) suivie par un recuit à basse température pour faire diffuser les dopants dans le siliciure (où leur solubilité solide est basse) jusqu'à l'interface

Le problème de l'approche IBS est qu'elle crée des defaults qui ne peuvent être guéris qu'à haute température. La solution ITS semble la plus efficace, avec une ségrégation abrupte d'atomes de Bore avec un pic de concentration mesuré 2×10^{20} at.cm^{-3} après un recuit basse température (500°C, 5min, N_2) [*Dubois'08*], conduisant à une SBH inférieure à 0.082eV. De même, des valeurs record de résistivité de contact ($\rho_c = 6\sim7\times10^{-9}$ Ω.cm^2) ont été obtenues sur des contacts NiPtSi/Si dopés n^+ comme p^+ (recuit à 550°C, 30s) [*Zhang'10*], menant au final à des performances de SBFET à l'état de l'art [*Khater'10*] (nFETs: I_{ON}=734 µA/µm @ L_G=30nm – pFETs: I_{ON}=532 µA/µm @ L_G=30nm).

La technique ITM semble pour l'instant moins probante (Φ_{bp}=0.13eV dans [*Dubois'08*]), ce qui est attribué à une perte de dopants par exo-diffusion lors de la réaction de siliciuration, qui pourrait pousser les dopants vers la surface.

III.3.4. **Source et Drain métalliques pour les nFETs**

Puisque les contacts métal/Si sont *a priori* (cf. ancrage du niveau de Fermi) favorables à l'injection des trous, une grande majorité d'études dans la littérature est focalisée sur la fabrication de pFETs. En vue de développer un schéma d'intégration CMOS Schottky, deux approches sont confrontées pour fabriquer des nFETs à Source et Drain métalliques.

La première consiste en intégrer des siliciures de terres rares, qui présentent une faible SBH intrinsèque pour les électrons. C'est une approche qualifiée de "Dual Metal", puisque les siliciures diffèrent suivant que le dispositif est un pFET ou un nFET. La seconde approche propose un procédé moins complexe avec le choix d'un siliciure unique (idéalement "ancré" vers le milieu du gap), et de faire le pari de l'efficacité du dopage par ségrégation (type n pour les nFETs, type p pour les pFETs).

III.3.4.a. Dual S/D Metal pour le CMOS Schottky

Les SBH intrinsèques pour les électrons des siliciures de terres rares tels que ErSi ou YbSi sont de l'ordre de 0.28eV [*Dubois'08*]. La contrainte sur les niveaux de dopage à atteindre est donc tout de même plus élevée que dans le cas de pFETs à S/D en PtSi. De plus, ces matériaux présentent en pratique plusieurs inconvénients, tels que la formation de cratères ou de défauts pyramidaux [*Tsai'04*], [*Tan'06*], [*Breil'09*] (ce qui dégrade la résistivité de couche, et probablement la résistance de contact avec les couches de métallisation supérieures), leur forte réactivité avec l'oxygène (présent dans les espaceurs, l'oxyde d'isolation ou l'oxyde enterré), ainsi que leur mauvaise stabilité thermique (une exo-diffusion significative de Si peut être observée dès 500°C [*Breil'09*]).

Ces contraintes imposent un budget thermique très limité et, sur SOI, préférablement une gravure partielle du canal avant le dépôt du métal. Des nFETs fonctionnels avec des extensions d'Arsenic, des S/D en ErSi et YbSi ont été démontrés jusqu'à L_g=45nm dans [*Hutin'09*] suivant le procédé damascène décrit plus haut. La compétitivité de l'approche Dual S/D metal est cependant loin d'être évidente. En plus d'ajouter en complexité de fabrication, les performances des dispositifs sont assez peu convaincantes.

III.3.4.b. Métal unique pour le CMOS Schottky

Puisque les tentatives d'intégration de siliciures à base de terres rares sont pour le moment peu récompensées par rapport à leur complexité, certaines études ont été publiées récemment visant à optimiser la ségrégation de dopants de type n pour des siliciures *a priori* plus favorables à l'injection de trous: PtSi [*Dubois'08*]; NiSi [*Vega'10-a&b*]; NiPtSi [*Zhang'10*], [*Khater'10*]. Cela permet aussi de ne considérer qu'une seule étape de siliciuration pour les nFETs et les pFETs.

Les SBH pour les électrons sont en effet considérablement réduites par la ségrégation d'impuretés As: 0.15eV [Dubois'08] (extraction sur courbes d'Arrhenius), 0.12eV [*Vega'10-b*] (Φ_{bp} extraite par mesures C-V et Φ_{bn} déduite par complémentarité), et même 0.06eV [*Zhang'10*] (même méthode que ce dernier).

En particulier, l'intégration CMOS à siliciure unique NiPt a été démontrée récemment sur du SOI de 10nm d'épaisseur [*Khater'10*] avec ségrégation de Bore pour les pFETs et d'Arsenic pour les nFETs jusqu'à des longueurs de grille de 20nm. Les tensions de seuil sont relativement symétriques, ainsi que les courants à l'état passant à $|V_{GS}|$=1V: 560µA/µm pour les nFETs et 490µA/µm pour les pFETs à L_g=30nm. Malgré un contrôle des effets de canaux courts encore perfectibles (DIBL ~150mV/V à L_g=30nm, ce qui est plutôt élevé pour cette épaisseur de Si et une diffusion des dopants supposée limitées), ces résultats sont pour le moment parmi les plus avancés dans la perspective de CMOS Schottky à métal unique pour les Source et Drain.

III.4. Conclusion

Remplacer des jonctions p/n par des jonctions métal/semi-conducteur dans les S/D des MOSFETs était à l'origine considéré pour diverses raisons évoquées au début de ce chapitre. S'agissant d'intégration sur SOI pour des applications de logique CMOS, les avantages qui restent pertinents se réduisent au bas budget thermique de fabrication et à la réduction des résistances série.

Concernant ce dernier, la conclusion est moins évidente qu'il n'y paraît. En amenant le contact métal semi-conducteur à l'entrée du canal, dans une région *a priori* non dopée, le gain représenté par une basse résistivité de couche dans les S/D risque d'être annihilé par une composante de résistivité de contact décuplée (ou plus). En règle générale, la résistivité de contact ne doit pas dépasser un maximum de 10^{-8} $\Omega.cm^2$, ce qui ne peut pas arriver naturellement dans des contacts sur semi-conducteur non dopé.

Si la solution est de doper l'interface de contact (ce qui rend la barrière plus fine et augmente le courant par effet tunnel), alors de telles valeurs de ρ_c sont expérimentalement associées à des concentrations de dopant de l'ordre d'au moins quelques 10^{20} $at.cm^{-3}$. Par conséquent, afin de rester une alternative crédible en termes de réduction des résistances série, le SBFET doit être muni d'extensions fortement dopées au même titre que les MOSFETs conventionnels.

De plus, une analyse au premier ordre du fonctionnement d'un SBFET montre que pour les valeurs usuelles de polarisation (V_{dd}~1V), le dopage d'interface est requis non seulement pour augmenter le courant d'injection, mais aussi pour limiter le courant de fuite à l'état bloqué. Il peut également être nécessaire pour éviter une dégradation de la pente sous le seuil qui a typiquement lieu dans les géométries où il existe une distance non nulle entre la Source et le bord de Grille.

Selon les arguments ci-dessus, le portrait d'un « bon » SBFET sur SOI ressemble à s'y méprendre à celui d'un MOSFET conventionnel sur SOI avec des accès siliciurés. Au final, les performances de l'un devraient s'approcher de celles de l'autre puisque la principale différence structurelle est l'épaisseur de la couche de siliciure.

La vraie spécificité des SBFETs à ségrégation de dopants aux Source et Drain est le mécanisme d'activation des dopants qui a lieu à basse température. En plus d'être en soi un avantage, cela pourrait représenter une opportunité de réduire la diffusion des dopants dans le canal et ainsi améliorer le contrôle des effets de canaux courts. Cela dit, cette amélioration potentielle vis-à-vis des jonctions p/n activées par RTP n'a pas été démontré jusqu'à présent. Qui plus est, il est possible qu'un profil latéral de dopants trop abrupt puisse dégrader les propriétés d'injection à l'interface métal/semi-conducteur.

Le développement des briques technologiques pour les Source et Drain totalement métalliques n'est probablement pas une nécessité absolue pour améliorer les performances et la réductibilité des dimensions des dispositifs planaires, symétriques et à simple grille sur FDSOI. Malgré cela, il peut être d'une importance capital pour l'élaboration d'architectures différentes, comme le transistor à Double Grille vertical présenté au paragraphe III.3.1.b.

En outré, les contraintes liées à la modulation de la SBH par un dopage d'interface, et en particulier les niveaux d'activation requis, peuvent-être relâchées par l'utilisation de semi-conducteurs à bande interdite plus faible tels que le Germanium ou les alliages Silicium-Germanium. Il s'agit toutefois d'un « monde » différent, qui sera présenté dans le chapitre suivant.

Chapter IV. Substrats et dispositifs à base de Ge

IV.1. Introduction

Bien que le premier transistor fonctionnel à point de contact ait été réalisé sur Germanium [*Bardeen'48-a&b*], ainsi que le premier circuit intégré [*Kilby'59*], l'apparition de circuits intégrant de façon monolithique des composants isolés ainsi que leurs interconnexions sur Silicium [*Noyce'59*] marqua le début du règne sans partage du Si. Une telle approche aurait été bien plus compliquée à réaliser à l'époque sur Germanium, puisque les oxydes de Germanium sont connus pour leur instabilité, leur non-stœchiométrie et leur solubilité dans l'eau. A l'inverse, le Si offre la possibilité d'obtenir simplement par croissance thermique un SiO_2 chimiquement stable. Celui-ci est un bon isolant (donc idéal pour la fabrication de circuits monolithiques), et possède une bonne interface avec le Si (donc idéal en tant que diélectrique de grille pour les MOSFETs). En plus de cela, les points suivants ont joué en défaveur du Ge:

- Les premiers MESFETs à point de contact ne marchaient pas bien sur Si, mais ce n'était plus un problème pour les transistors bipolaires et les MOSFETs (inventés en 1959 par Kahng et Atalla de Bell Labs, brevet soumis l'année suivante [*Kahng'60*]).
- Le Germanium représente environ 0.00015% de la composition de la lithosphère (contre 20.4% pour le Silicium), et il est plus difficile à extraire (essentiellement présent en petites concentrations dans des minerais Zn ou Zn-Cu). Par conséquent, le Ge est beaucoup plus cher que le Si.

Ce sont quelques unes des raisons qui font que personne n'a jamais entendu parler de la « Germanium Valley ». Depuis le milieu des années 1960 et pour plus de 40 ans, le Silicium aura dominé l'industrie de la microélectronique de façon écrasante. Dans le même temps, la recherché appliquée pour la réalisation de dispositifs sur Germanium est devenue rare, voire invisible.

IV.1.1.a. "Retour vers le futur"?

Le Germanium étant un semi-conducteur à forte mobilité, il était tout de même peu probable qu'il sombre définitivement dans l'oubli, étant donné la demande croissante pour des circuits logiques de plus en plus rapide. Le premier défi a été de développer un diélectrique de grille avec une faible densité d'états d'interface sur Ge [*Wang'75*]. En 1983, Rosenberg a démontré des nFETs sur Ge avec un nitrure de Germanium obtenu par croissance thermique comme diélectrique de grille, avec $D_{it} < 2\times10^{11}$ cm^{-2} [*Rosenberg'83*]. Quelques années plus tard, le procédé avait évolué en la nitruration d'un oxyde natif GeO_2 sur des nFETs d'une longueur de 6µm avec une mobilité dans le canal estimée à 940 $cm^2.V^{-1}.s^{-1}$ [*Rosenberg'88*]. Les pFETs sur Ge ont suivi, avec une mobilité dans le canal observée pour la première fois à des valeurs plus grandes que dans le Si (~1050 $cm^2.V^{-1}.s^{-1}$ [*Martin'89*], ~2000 $cm^2.V^{-1}.s^{-1}$ à L_g=0.6µm [*Ransom'91*]).

Alors que des techniques commencèrent à être développées pour obtenir des substrats avec une forte concentration de Germanium (substrats virtuels [*Currie'98*], condensation ou enrichissement de Ge [*Tezuka'01*]), un regain d'intérêt pour les dispositifs sur Germanium s'est déclenché à l'échelle mondiale au début des années 2000 (Hanovre [*Reinking'99*], MIT [*Lee'01*], IBM [*Shang'02*], Stanford [*Chui'02-a*], Taïwan [*Huang'03*], Tokyo-MIRAI [*Tezuka'04*], [*Maeda'04*], IMEC [*De Jaeger'04*], Leti [*Clavelier'05*], [*Le Royer'05*], [*Weber'05*] etc.).

Cette tendance s'est confirmée dans la demi-décennie qui a suivi avec le glissement des technologies Silicium vers l'utilisation de diélectriques de grille high-k (qui permettent d'obtenir un courant de fuite de grille plus bas à capacité de grille équivalente) afin d'améliorer la puissance consommée et la fiabilité des dispositifs de longueur déca-nanométrique. La raison principale pour laquelle le Ge a été mis de côté dans les années 1960 est donc apparue invalidée, et d'aucuns pensent que le passé de la microélectronique pourrait redevenir son futur.

IV.1.2. **Transport dans le Germanium**

Intrinsèquement, le transport de porteurs dans le Ge est caractérisé par des masses effectives faibles, ce qui doit avoir pour conséquence un courant à l'état passant plus élevé que dans le Si. L'inconvénient d'une bande interdite plus faible et de la concentration intrinsèque de porteurs plus élevée est une augmentation des courants de fuite de jonction en inverse et des effets tunnels par rapport au Si. A ceci, nous pouvons ajouter que les densités de pièges sont souvent expérimentalement déterminées comme étant plus importantes que dans le Si, ce qui réduit la durée de vie des porteurs minoritaires et accentue encore le problème des fuites (par génération/recombinaison). Pour ces raisons, les dispositifs à canal Germanium semblent surtout adaptés aux applications haute performance.

IV.2. Substrats à base de Germanium

Puisqu'un certain nombre de facteurs indiquent l'intérêt du Germanium pour les applications de logique CMOS à haute performance en tant que semi-conducteur à haute mobilité, nous allons voir dans cette section les façons les plus courantes de fabriquer des substrats à base de Ge. Comme évoqué précédemment, le Germanium est rare, cher, dense, lourd (et la plupart des outils de fabrication sur le marché sont calibrés pour la manipulation de substrats de Silicium). Utiliser des substrats de Ge massif est donc un mauvais choix en termes de rentabilité. C'est la raison pour laquelle les techniques présentées visent à obtenir des substrats de Germanium sur Silicium (bulk-like Ge on Si) ou de Germanium sur Isolant (GeOI).

IV.2.1. **Ge on Si**

Le désaccord de maille de 4.2% entre le Ge et le Si rend difficile à réaliser par hétéro-épitaxie des couches de Ge avec les propriétés désirées (c'est à dire d'une planéité compatible avec les étapes de lithographie avancée et de transfert de couche, une densité de défauts minimisée, etc.). L'épaisseur critique h_c au-delà de laquelle les défauts tendent à se former et à se propager (threading dislocations) est de ~2-4nm [*People'85-a*].

Cette épaisseur critique est assez extrême pour la fabrication de dispositifs, et la couche est entièrement contrainte (ce qui n'est pas une mauvaise chose du point de vue des propriétés de transport, mais qui peut mener plus tard à la formation de défauts liée à la relaxation de la contrainte induite par les étapes de fabrication). Les deux techniques qui suivent permettent d'obtenir des couches de Ge relâchées sur des substrats Si.

IV.2.1.a. Substrats virtuels

L'approche dite des substrats virtuels [*Currie'98*] consiste en augmenter graduellement la concentration en Ge de couches de SiGe empilées de 0% à 100% sur environ 10µm (10% Ge.μm^{-1}). Ce procédé mène à une

couche supérieure de Ge complètement relâchée avec une densité de dislocations de quelques 10^6 cm^{-2}. Cependant, cette méthode est caractérisée par des rugosités de surface importantes et nécessite de ce fait des étapes intermédiaires (ou finales) de polissage.

L'avantage est que les défauts et dislocations sont confinés dans les couches inférieures, et la qualité cristalline du Ge est préservée. Néanmoins, le procédé est long et cher, et sujet à des problèmes d'uniformité d'épaisseur (substrats bombés avec une flèche d'environ 250nm).

IV.2.1.b. Cyclage thermique

La méthode du cyclage thermique a d'abord été évoquée dans [*Colace'98*] et brevetée peu après [*Hernandez'01*]. Elle débute par un dépôt à basse température d'un film mince précurseur de Ge (~200nm), suivi par un dépôt à plus haute température d'une couche plus épaisse (~2µm) de Ge. L'étape à basse température (330°C-400°C) permet la relaxation plastique de la contrainte sans induire d'excessives ondulations de surface. L'étape suivante à haute température (600°C-850°C) conduit à une réduction conséquente des densités de dislocations émergentes, ainsi qu'à une croissance plus rapide. Ensuite, des étapes de cyclage thermique peuvent être réalisées (typiquement entre 750°C et 900°C) pour provoquer la propagation assistée thermiquement des segments émergents en bord de substrat, et ainsi réduire la densité de défauts cristallins.

Finalement, des densités de dislocations (TDD) de l'ordre de ~10^7 cm^{-2} peuvent être obtenues par cyclage thermique dans des couches de Ge par croissance sur (001)Si [*Hartmann'05-a*]. C'est un peu plus élevé que dans les substrats virtuels, mais le procédé est plus rapide, moins cher, et conduit à une meilleure uniformité d'épaisseurs.

IV.2.2. **Germanium-On-Insulator (GeOI)**

Les substrats sur isolant présentent le même intérêt qu'il s'agisse de Ge ou de Si, c'est-à-dire une intégrité électrostatique supérieure, ce qui est d'une importance capitale pour des longueurs de grille courtes. De plus, ils permettent d'éliminer en partie les fuites de jonction, qui sont un problème majeur dans les dispositifs sur Ge.

IV.2.2.a. Smart Cut™

Inventé par Michel Bruel dans les années 1990 [*Bruel'91*], [*Bruel'95*], la technologie Smart Cut™ (propriété de Soitec) a remplacé le SIMOX (Séparation par Implantation d' OXygène [*Izumi'78*]) comme la principale technique de fabrication de substrats Silicium sur isolant et représente de nos jours environ 90% du marché du SOI. Elle est appliquée à la fabrication de substrats GeOI en R&D depuis environ 2004.

Les substrats GeOI les plus récents présentent une moyenne de moins de 10 défauts par cm^2 en surface, ce qui approche la défectivité de substrats de Ge massif (environ 3 défauts par cm^2). Le fait qu'il n'y ait pas de défauts étendus observables sur des images TEM en vue plane suggère une densité de défauts inférieure à 10^5 cm^{-2} pour les substrats GeOI réalisés avec des substrats donneurs de Ge massif. Des mesures de spectroscopie Raman ont démontré que le procédé de fabrication de tels substrats n'induit aucune contrainte mécanique significative [*Akatsu'06*].

IV.2.2.b. Enrichissement en Ge

La technique d'enrichissement de Ge, désignée à son invention de façon abusive sous le nom de « condensation » de Ge, a d'abord été développée au Japon (Université de Tokyo, Mirai, Toshiba) il y a environ dix ans [*Tezuka'01*], [*Nakaharai'03*]. Le matériau de départ est un substrat SOI, sur lequel une croissance par épitaxie de SiGe avec une faible concentration en Ge (par exemple 10%, afin de limiter le désaccord de maille et la formation de défauts) est réalisée. Le procédé repose sur le fait que les atomes de Si sont préférentiellement oxydés par rapport aux atomes de Ge. Ainsi, durant les étapes de recuit sous oxygène, une couche de SiO_2 se forme en surface, consommant le Si alors que les atomes de Ge tendent à être repoussés vers l'oxyde enterré. Ces recuits d'oxydation sont alternés avec des recuis d'homogénéisation sous une atmosphère inerte (Ar, ou N_2), et l'opération est répétée jusqu'à ce que la concentration désirée en Germanium soit obtenue.

On peut ainsi parvenir à une couche de Ge presque pure (~95%) sur isolant. Ensuite, après retrait de l'oxyde en surface, une couche de Ge pure peut éventuellement être déposée par épitaxie pour la fabrication de dispositifs sur GeOI non contraint [*Hutin'10-a&b*]. Il est bien sûr également possible de cesser l'enrichissement à des concentrations moindres de Ge, et en fonction de l'épaisseur finale de film désirée [*Hutin'10-c*].
Comme nous allons le voir par la suite (paragraphe IV.3.2.), quelques doutes subsistent quant à l'intérêt de réaliser des nFETs à canal Ge ou SiGe. Un avantage de cette technique est qu'elle peut être localisée de façon à co-intégrer des nFETs à canal Si et des pFETs à canal SiGe ou Ge [*Tezuka'05*], [*Tezuka'06*], [*Le Royer'10-a*] pour une approche à canal dual sur isolant (Dual Channel On Insulator DCOI).

IV.3. CMOS Ge et GeOI

IV.3.1. **Généralités sur les briques technologiques de base**

Les points de procédés pour la fabrication de transistors sur substrats Si ou SOI sont à présent bien connus, après 40 ans de recherche intensive pour les applications en microélectronique. En comparaison, peu d'études ont été réalisées sur Germanium depuis les années 1960. Ses propriétés basiques doivent pourtant être prises en compte afin d'optimiser la technologie MOS sur Ge, telles que des températures caractéristiques plus basses que dans le Si (point de fusion à 937°C pour le Ge contre 1420°C pour le Si), une sensibilité plus importante envers la contamination métallique, une diffusivité plus haute des défauts ponctuels [*Vanhellemont'07*] ainsi qu'une intolérance générale vis-à-vis des traitements basés sur des solutions aqueuses (en raison de l'instabilité et de la volatilité des oxydes de Germanium).

IV.3.1.a. Gravure humide et nettoyage

Bien que le Ge soit un élément de groupe IV comme le Si, ses vitesses de gravure en sont radicalement différentes. Une différence fondamentale est qu'une fine couche passivante de SiO_2 est formée en surface du Si en présence de solutions oxydantes (H_2O_2, eau ozonée), ce qui limite la vitesse de gravure du Si dans des solutions sans FH. Le GeO_2, lui, est soluble dans l'eau. Ainsi, l'oxydation simultanée du Ge et la dissolution du GeO_2 ont pour résultat une augmentation de la vitesse de gravure. Un grand nombre de chimies humides et les vitesses d'attaque correspondantes sur Ge est rapporté dans [*Brunco'08*]. Au Leti, les nettoyages de surface du Ge sont basés sur des solutions HF/HCl et HCl/O_3.

IV.3.1.b. Retrait des résines

Il est également nécessaire d'utiliser un procédé de stripping (retrait de résine) dédié, sachant que dans l'eau oxygénée utilisée dans le cas du Si mène à une consommation de Ge supérieure à 1µm/min. Des études de compatibilité ont montré que les étapes sèches de gravure plasma avaient un effet passivant sur le Germanium pour des ratios $N_2/(O_2+N_2)$ élevés [*Lachal'06*]. Ainsi, après la gravure des zones actives, un stripping sec semble adapté au GeOI, et évite la consommation latérale de Ge associée à l'étape de rinçage à l'eau (démouillage). Une bonne efficacité de retrait a également été démontrée pour les strippings post-implantation en augmentant graduellement la température [*Lachal'06*].

IV.3.1.c. Passivation d'interface avec les diélectriques high-k

L'usage croissant de matériaux high-k tels que le HfO_2 comme diélectriques de grille a contribué au retour du Ge comme une alternative sérieuse au Si. La mise en place d'une couche de passivation d'interface (IL pour interlayer) entre la surface du Ge et le high-k apparaît toutefois absolument nécessaire pour empêcher la diffusion des atomes de germanium au sein du diélectrique de grille, ce qui dégraderait les caractéristiques électriques de l'empilement.

Des traitements de surface à base de NH_3 visant à former un oxynitrure de Ge (GeON) empêchent efficacement cette diffusion et améliore le comportement capacitif de la structure MOS [*Chui'04*], [*Van Elshocht'04*], [*Le Royer'05*]. Il a été montré que des couches de high-k HfO_2 ou ZrO_2 combinées avec une passivation GeON pouvaient être réduites à des épaisseurs d'oxyde équivalentes (EOT) sub-nanométriques tout en maintenant un faible courant de grille [*Chui'02-b*], [*Chen'04*], [*Dimoulas'05*], [*Ritenour'06*]. Cependant, cette approche a finalement été jugée insuffisante en termes de passivation d'états d'interface, débouchant sur des caractéristiques C-V non idéales et hystérétiques (D_{it} typiquement de l'ordre de 5×10^{12} - 10^{13} $eV^{-1}.cm^{-2}$).

Puisque cette densité élevée d'états d'interface était alors attribuée au processus d'oxydation du Ge, d'autres ILs ont été étudiées, telles que l'AlN [*Whang'04*] ou une fine couche de Silicium partiellement oxydé [*Wu'04*]. En ce qui concerne cette dernière, la diffusion des atomes de Ge dans le "cap" a été identifiée comme un point critique du point de vue des propriétés structurales, physico-chimiques et électriques des empilements de grille résultants [*Caymax'09-a*]. Le Si cap est toutefois considéré comme la solution la plus favorable à la réduction de l'EOT, et a été largement adoptée pour la fabrication de pFETs submicroniques sur Ge [*Mitard'09*].

Il a cependant été montré [*Dimoulas'07*] que l'évitement à tout prix de l'oxydation du Ge n'était ni une condition nécessaire, ni une condition suffisante pour obtenir une bonne interface. Par exemple, aucune oxydation en surface du Ge n'est observée dans cette étude dans le cas d'un dépôt direct de HfO_2, ce qui n'empêche pas un comportement électrique médiocre. D'un autre côté, des oxydes de terres rares déposés sur Ge (CeO_2, La_2O_3, Dy_2O_3, Gd_2O_3) constituent une bonne barrière de diffusion, avec des D_{it} relativement limitées (~10^{12} $eV^{-1}.cm^{-2}$, c'est-à-dire moins que dans le cas GeON). En raison de leur bande interdite insuffisante pour limiter les courants de grille, ces oxydes doivent néanmoins être associés au HfO_2 en tant que simple couche d'interface.

IV.3.1.d. Diffusion des dopants, solubilité solide et activation

IV.3.1.d.i. Diffusion

Contrairement au Si, la diffusion des espèces dopantes est limitée pour les impuretés de type p (Bore), et est importante pour les impuretés de type n (Arsenic, Phosphore). Il est maintenant communément admis que les atomes de Bore ne diffusent pas (ou peu) pour des recuits thermiques rapides (RTA) en-dessous de 800°C.

Par contre, le Phosphore et l'Arsenic diffusent très rapidement au-delà de 550°C. Par conséquent, cette température de RTA ne doit pas être dépassée dans le cadre de la réalisation de jonctions fines pour le CMOS sur Ge. La durée du RTA doit être comprise entre 10 et 60 secondes [*Koffel'08*].

IV.3.1.d.ii. Solubilité solide

La limite de solubilité solide (SSL) peut être obtenue par des calculs *ab initio*, mais elle est la plupart du temps déduite de mesures de résistivité. Ces mesures donnent une estimation de la concentration maximale d'impuretés électriquement actives, ce qui est souvent directement interprété comme la limite de solubilité solide. Cette interpretation soulève deux problèmes:

- La SSL correspond aux conditions d'équilibre thermodynamique. Si le procédé de dopage est métastable, par exemple dans le cas d'une recroissance par épitaxie en phase solide (SPER) ou d'un recuit laser (LTA), la concentration de dopants électriquement actifs peut la dépasser.
- Déduire la concentration de dopants actifs de measures de résistivité présuppose que la relation liant la mobilité des porteurs à la concentration en impuretés est bien connue. C'est moins le cas pour le Ge que pour le Si.

Ce sont probablement les deux raisons principales pour lesquelles les valeurs rapportées dans la Table IV-3 semblent si dispersées (dans le cas du Bore, sur presque deux décades).

Element	Solid Solubility (cm^{-3})	Ref.
B	5.5×10^{18}	[*Trumbore'60*]
B	6.5×10^{18}	[*Uppal'01*]
B	2×10^{18}	[*Uppal'04*]
B	1×10^{19}	[*Delugas'04*]
B	2×10^{20}	[*Suh'05*]
B	1×10^{19}	[*Chao'05*]
B	5.5×10^{18}	[*Satta'06*]
P	2×10^{20}	[*Trumbore'60*]
P	2×10^{20}	[*Satta'06*]
As	8.1×10^{19}	[*Trumbore'60*]
As	5×10^{19}	[*Ahlgren'00*]
As	8.1×10^{19}	[*Satta'06*]
Sb	1.2×10^{19}	[*Trumbore'60*]
Ga	4.9×10^{20}	[*Trumbore'60*]

Table IV-1: Limites de solubilité solide dans le Germanium pour les dopants de type p (bleu) et n (rouge), telles que rapportées dans la littérature.

IV.3.1.d.iii. Activation

Après implantation ionique dans du Ge cristallin et recuit de type RTA, les niveaux d'activation sont de l'ordre de $1\text{-}4\times10^{19}$ at.cm^{-3} pour le Bore (type p) et l'Arsenic (type n), et un peu plus élevés pour le Phosphore (type n: $2\text{-}6\times10^{19}$ at.cm^{-3}) [*Satta'06*], [*Koffel'08*], [*Hutin'08-a*].

Ces valeurs typiques peuvent être augmentées jusqu'à plus de 10^{20} at.cm^{-3} en utilisant des techniques moins conventionnelles impliquant des mécanismes d'activation métastables, tels que la SPER prenant place

dans des substrats de Ge ou GeOI préamorphisés [*Chao'05*], [*Satta'05*] (PAI pour Preamorphization-Assisted Implantation). L'implantation de pré-amorphisation, en utilisant par exemple des ions Ge^+ à haute énergie, est réalisée avant l'implantation des dopants.

En combinant la PAI avec un recuit par laser excimère (LTA) [*Mazzocchi'09-a*], [*Mazzocchi'09*-b], des niveaux d'activation supérieurs à 10^{20} at.cm^{-3} ont été obtenus à la fois pour le Bore et pour le Phosphore, avec pour ce dernier un profil électrique abrupt de 8nm/dec. Ces résultats sont prometteurs, mais la PAI est difficile à contrôler sur des substrats GeOI, du fait de la nécessiter de garder une interface amorphe/cristallin (α-c) dans le film mince de Ge.

IV.3.1.e. Germaniuration

En raison de sa rugosité et de sa sensibilité limitée à l'oxydation, ainsi que sa faible résistance de couche, sa faible température de formation et faible consommation de Ge, le NiGe fait consensus comme le meilleur candidat pour la germaniuration des accès de MOSFETs sur substrats Ge [*Gaudet'06*]. Bien que le PdGe et PtGe partagent un certain nombre de ces qualités, le retrait sélectif du métal non réagi requiert dans leur cas des solutions d'eau régale. Comme l'eau régale consomme le Ge à pratiquement 300nm/min, cela rend l'intégration de ces siliciures assez risquée (en cas de défauts ou de discontinuités des couches de métal après formation du germaniure).

Diverses approches sont présentées dans la littérature pour le retrait sélectif du Ni par rapport au NiGe [*Carron'06*], [*Brunco'08*] parmi lesquelles:

- Des acides aqueux ou alcalins ainsi que des chimies à fort pouvoir oxydant, pour lesquels la sélectivité "Ni vs. NiGe" est surtout basée sur l'épaisseur supérieure du NiGe par rapport à la couche déposée de Ni. Pour cette stratégie, des solutions $NH_4OH/H_2O_2/H_2O$ ou HNO_3/H_2O sont utilisées.
- Des acides aqueux ou chimies à faible pouvoir oxydant qui présentent la plus forte sélectivité Ni/NiGe. Des solutions $HCl/HF/H_2O$ sont alors utilisées.
- Des chimies non aqueuses et fortement oxydantes (par exemple, H_2SO_4 96%) qui ont une sélectivité acceptable.

IV.3.2. **Les défis du nFETs à canal Ge**

IV.3.2.a. Dopage de type n

Le premier obstacle à la réalisation de nFETs sur Germanium a pour origine la faible solubilité solide, la diffusion rapide et l'activation faible des dopants de type n (As, P). Ce sont autant d'inconvénients pour réaliser des jonctions fines avec de faibles résistances d'accès et un profil latéral abrupt dans des dispositifs à dimensions réduites. Ce problème de dopage est de fait ce qui déclencha la recherche sur les transistors Schottky sur Ge.

Comme nous le savons maintenant, les transistors Schottky ne peuvent de toute façon pas être considérés comme des alternatives sérieuses au CMOS conventionnel sans couche de dopage d'interface. Qui plus est, l'ancrage du niveau de Fermi à la surface du Ge est tel que pratiquement tous les métaux connus affichent une préférence pour l'injection des trous, ce qui rend les contraintes sur le dopage de type n encore plus difficiles à remplir que pour le dopage de type p.

Maintenant que des niveaux d'activation supérieurs à 10^{20}at.cm^{-3} avec des profils raisonnablement abrupts ont été démontrés, les difficultés semblent partiellement résolues. Cela dit, les procédés impliqués (PAI,

LTA) ne sont pas particulièrement simples à mettre en place dans la fabrication complète d'un transistor, surtout sur films minces. En plus de cela, les premiers démonstrateurs nFETs Ge souffraient de caractéristiques dégradées qui n'étaient pas seulement imputables aux problèmes de dopage.

IV.3.2.b. Couche d'inversion et tension de seuil

En dépit d'une mobilité d'électrons supposée plus grande que dans le Si, les premiers MOSFETs à canal n sur Ge étaient minés par d'étonnamment mauvaises caractéristiques à l'état passant [*Chui'03-b*], [*Shang'04*], [*Whang'04*], lorsqu'ils n'étaient pas purement non-fonctionnels [*Ritenour'06*]. Cette tendance est restée mystérieuse un certain temps, avant qu'il ne soit avancé dans [*Dimoulas'06*] que le phénomène d'ancrage du niveau de Fermi à un niveau de neutralité de charge près de la bande de valence en surface du Ge puisse en être responsable.

IV.3.2.b.i. Etats de surface intrinsèques en surface du Ge

Le niveau de neutralité de charge prédit pour les surfaces libres de Ge d'après l'analyse des états charges attribués aux liaisons pendantes (DB pour dangling bonds) est, comme indiqué par la théorie des MIGS (Metal Induced Gap States) dans le cas des contacts métal/Ge, localisé très près de la bande de valence (~0.09eV). En conséquence, en première approximation, l'ancrage du niveau de Fermi à $E_{cnl} \sim E_V + 0.09eV$ peut également être attendu dans des structures MOS sur Ge.

IV.3.2.b.ii. Conséquences pour les structures MOS polarisées positivement

La Figure IV-31 montre un diagramme de bandes du côté Ge d'une structure MOS (en ignorant la présence de l'isolant). En l'absence de polarisation sur la Grille, les états d'interface sont peuplés jusqu'à E_F qui coïncide avec E_{cnl}, assurant ainsi la neutralité de la surface. Lorsqu'une tension positive est appliqué sur la Grille, E_F s'éloigne de E_{cnl}, et un excès d'états accepteurs peuplés dérivés de la bande de conduction induit une charge négative en surface, ce qui crée une désertion d'électrons au voisinage de la surface.

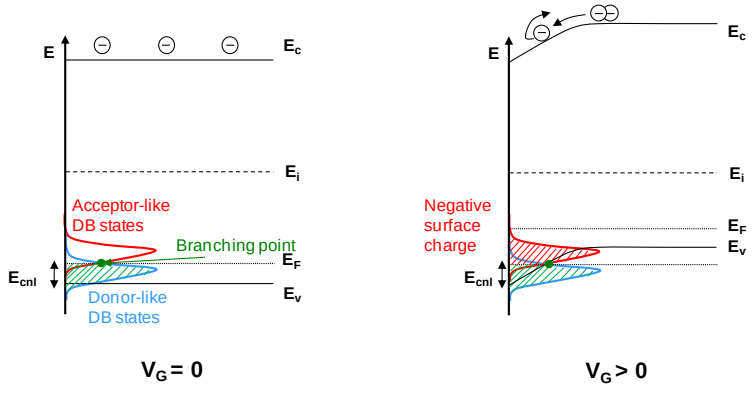

Figure IV-1: Diagramme de bandes du côté semi-conducteur d'une structure MOS sur p-Ge (E_F est choisi pour des raisons de simplicité de sorte que $V_{fb}=0$). Les densités d'états d'interface derives de la bande de conduction et de la bande de valence sont schématiquement représentés pour montrer le point d'embranchement dont est dérivé le niveau de neutralité de charge E_{cnl}. A gauche: à $V_G=0V$ – A droite: Après application d'une tension de Grille positive $V_G>0V$ (Figures adaptées de [Dimoulas'06], [Tsipas'09]).

Plus l'écart E_F-E_{cnl} est grand, plus le nombre d'états accepteurs non passivés et peuplés (à l'origine de la charge négative) est important. Comme E_{cnl} est particulièrement "bas" dans le Ge, il est relativement facile de déclencher cet effet. La conséquence pour les nFETs est que ce mécanisme s'oppose à la création du canal d'inversion en surface, surface qui reste de type p. Réciproquement, l'inversion de type p est facilitée dans les pFETs, ce qui explique au passage le décalage de $V_{th,p}$ vers des valeurs positives observé à maintes reprises dans les pFETs sur Ge.

Pour conclure sur les nFETs à canal Ge, leurs performances sont limitées par les propriétés intrinsèques de la surface du Germanium. La charge négative nette qui apparaît à des tensions de grille positives « retarde » l'inversion du canal, et limite de surcroît la mobilité du fait d'interactions coulombiennes [*Kuzum'07*].

Il y a deux façons de résoudre ce problème. Soit en réduisant la distance entre E_F et E_{cnl} par dopage de type p du canal, soit en passivant les états de surface. La première solution est difficilement acceptable en termes de compatibilité avec la réduction des dimensions du dispositif, mais aussi du point de vue de la variabilité et de la mobilité dans le canal. Par conséquent, l'optimisation de la passivation des états de surface par l'ingénierie de l'empilement de grille semble être le point critique à adresser pour fabriquer des nFETs à canal Ge fonctionnels et performants.

IV.3.3. **Emphase sur le pFET sur GeOI**

Ce paragraphe est centré sur les dispositifs à canal de Ge pur. En particulier, le cas de référence est le pFET sur substrat GeOI, afin de mettre en valeur les résultats obtenus au cours de cette thèse. Les pFETs sur substrats massifs seront toutefois évoqués à titre de comparaison.

IV.3.3.a. pFETs sur substrats Smart Cut™

Ces trois dernières années, plusieurs démonstrations de pFETs sub-microniques sur GeOI ont été publiées par le Leti [*Le Royer'07*], [*Pouydebasque'08*], [*Romanjek'08-a*], [*Le Royer'09*]. Des transistors jusqu'à des longueurs de grille de 70nm (Figure IV-32) ont été fabriqués sur substrats Smart Cut™ [*Romanjek'08-a*], ce qui était à l'époque tout près du record pour les MOSFETs à canal Ge (en considérant que des pFETs sur Ge On Si avec L_G=65nm [*Mitard'08*] et sur Ge massif avec L_G=60nm [*Yamamoto'07*] ont été publiés quelques mois avant par l'IMEC et le MIRAI, respectivement).

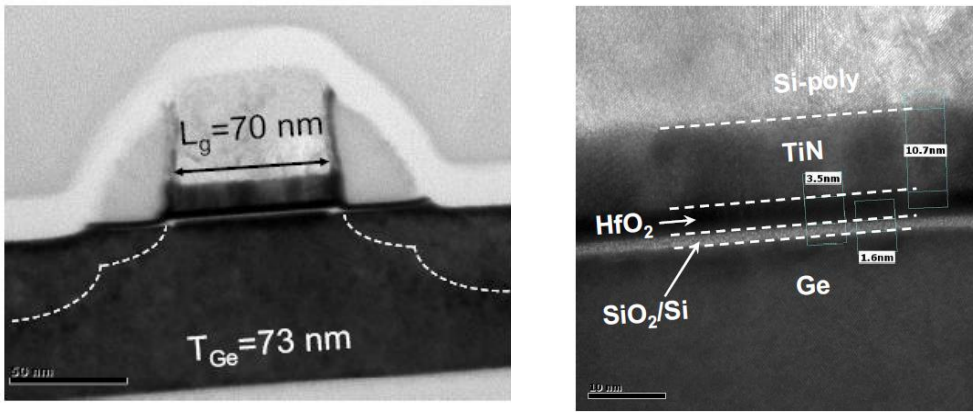

Figure IV-2: Micrographe X-TEM d'un pMOSFET de longueur de grille 70nm sur GeOI Smart Cut™, et zoom sur l'empilement de grille [Romanjek'08-a] (images: R. Truche).

Les facteurs d'amélioration de l'état passant, du régime sous le seuil et de l'état bloqué pour de tels dispositifs sont résumés sur la Figure IV-40.

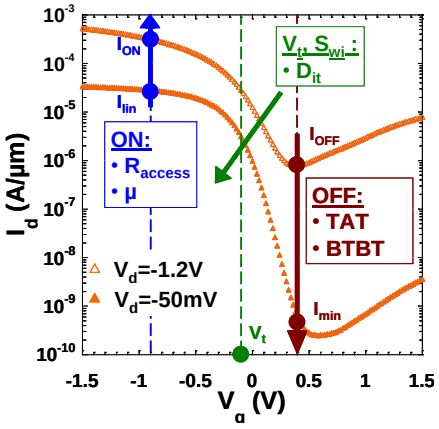

Figure IV-3: Récapitulation des facteurs d'amélioration pour les dispositifs de [Romanjek'08-a] (pFETs sur GeOI).

Les états d'interface à la fois avec l'empilement de grille et l'oxyde enterré peuvent être mis en relation avec trois limitations majeures des performances des pFETs sur GeOI. Les plus évidentes sont les valeurs non-idéales de la tension de seuil et de la pente sous le seuil. La troisième est indirecte, mais néanmoins importante. La conduction parasite à l'interface arrière résulte d'états d'interface de type accepteur non passivés, et doit être désactivée par une implantation de dopants dans le canal qui diminue sensiblement la mobilité, au détriment du courant à l'état passant. Il est donc justifiable de considérer que la diminution de D_{it}^{top} et de D_{it}^{bottom} est l'obstacle le plus crucial sur le chemin de l'optimisation de ces dispositifs.

De plus, la diminution des résistances d'accès par germaniuration a aussi un impact significatif sur I_{ON} pour les grilles courtes (~+30% attendus à L_g=70nm). En ce qui concerne I_{OFF}, les fuites liées au BTBT peuvent être amoindries par l'optimisation du profil latéral des jonctions, et les fuites liées au tunnel assisté par les pièges (TAT) et la génération/recombinaison Shockley-Read-Hall (SRH) en réduisant la concentration de défaut près des jonctions.

Enfin, l'utilisation de films de Ge plus fins n'est certainement pas sans intérêt, puisque le contrôle électrostatique par la grille avant sur toute l'épaisseur du canal s'en trouverait amélioré. Les conséquences seraient un contrôle encore amélioré des effets de canaux courts, mais aussi une diminution de l'influence de la conduction parasite à l'interface arrière, ce qui relâcherait les contraintes en termes de dopage du canal. De ce point de vue, la technique d'enrichissement en Ge est prometteuse puisque la possibilité de fabriquer des substrats GeOI d'une épaisseur de 10nm avec une bonne uniformité et une densité de défauts acceptable a déjà été démontrée sur des substrats de 200mm.

IV.3.3.b. pFETs sur substrats enrichis en Germanium

Dans cette partie sont présentés les résultats de [*Hutin'10-a*] et [*Hutin'10-b*], démontrant le fonctionnement de pFETs sur GeOI obtenu par épitaxie de Ge pure sur substrats SiGeOI enrichis à 95%. Le procédé de fabrication de transistors partage un certain nombre de points communs avec ceux de [*Romanjek'08-a*], mais les différences sont les suivantes:

- Les substrats sont plus fins et uniformes (T_{Ge}=25nm).
- L'utilisation de lithographie E-beam a permis d'obtenir des longueurs de grille record de 30nm (Figure IV-41).

- La tension de seuil sur les canaux longs est d'environ -0.5V (au lieu de -0.15V), ce qui permet d'avantageusement considérer les I_{ON} et I_{OFF} « absolus » (c'est à dire I_D à respectivement $V_{GS}=V_{DD}$ et $V_{GS}=0V$, définition plus proche du fonctionnement réel dans un circuit que la mesure effectuée relativement à la tension de seuil).

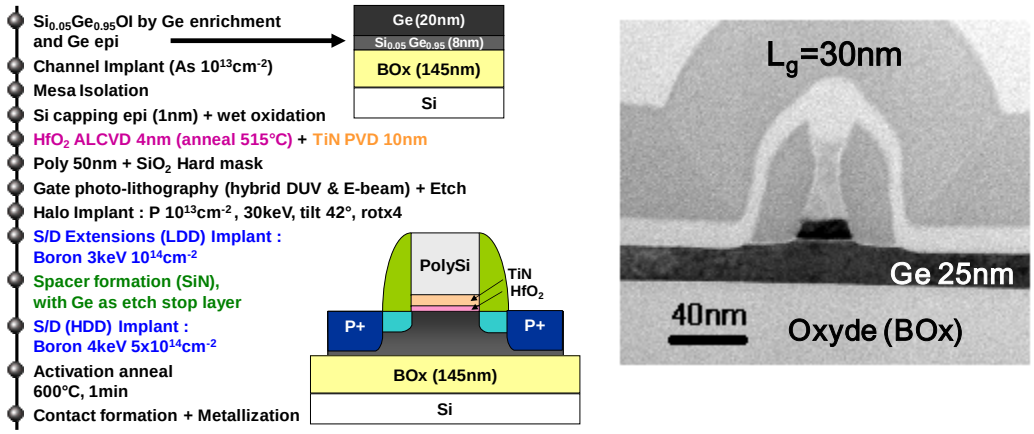

Figure IV-4: Gauche: Process flow simplifié de la fabrication des pFETs –Droite: image X-TEM d'un pFET sur GeOI de longueur de grille L_g=30nm. L'épaisseur de Germanium sous la grille est de 25nm.

Le rapport I_{ON}/I_{OFF} est dans ces conditions maintenu à plus de 5 décades jusqu'à une longueur de grille de 55nm (ce qui est un double record), grâce à une bonne qualité cristalline au voisinage des jonctions (implantation de B au lieu de BF_2), un film mince de Ge (enrichissement suivi par une épitaxie de Ge pur), ainsi qu'une tension de seuil et des effets de canaux courts bien contrôlés (dopage du canal et implantation de halos).

La figure de mérite représentant le délai de grille intrinsèque en fonction du courant à l'état bloqué (Figure IV-48, I_{ON} et I_{OFF} mesurés cette fois relativement à V_{th} pour une comparaison plus juste) montre un compromis amélioré par rapport à la littérature dû notamment à des fuites basses, et en dépit d'un courant à l'état passant perfectible. Celui-ci peut être amélioré par l'implémentation de briques technologiques connues (élévation des S/D, germaniuration), et l'optimisation de l'empilement de grille permettrait d'ajuster V_{th} sans avoir recours au dopage du canal.

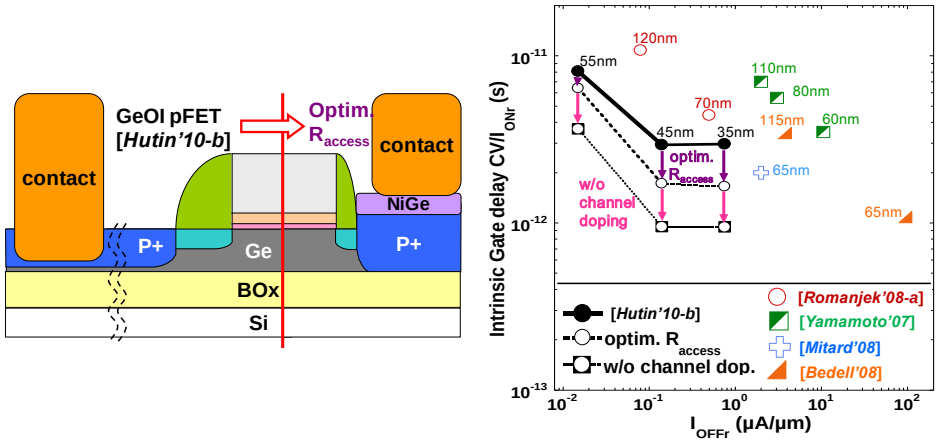

Figure IV-5: Délai intrinsèque associé à une grille (CV/I_{ONr}) en fonction de I_{OFFr} (relativement à V_{th}). I_{ONr} est défini par $I_D@V_{GS}=V_{th}+2V_{DD}/3$, I_{OFFr} par $I_D@V_{GS}=V_{th}-V_{DD}/3$ (V_{DD}=-1V). Des points prospectifs sont reportés sur le graphe, en corrigeant les résistances d'accès et en supposant que l'on puisse se passer du dopage de canal (qui dégrade la mobilité).

IV.3.4. De la technologie Ge pour le CMOS conventionnel

IV.3.4.a. Les problèmes persistants

IV.3.4.a.i. Dopage de type n et fuites de jonction

- **Le dopage de type n** dans le Ge par implantation d'Arsenic ou de Phosphore souffre d'une **basse limite de solubilité solide** ($5\text{-}6\times10^{19}$.cm^{-3}), et de **diffusivités élevées au-delà de 550°C**.
- La faible bande interdite du Ge le rend sujet au **Tunnel Bande à Bande** (BTBT). A moins que la tension d'alimentation ne soit réduite à des valeurs inférieures à 0.7V ($V_{DD}<E_g^{Ge}/q$), cela provoque une augmentation de I_{OFF} due aux fuites latérales de jonction, ainsi que **des fuites de Drain induites par le potentiel de Grille** (GIDL) si les zones d'extensions et la Grille se chevauchent.

IV.3.4.a.ii. Passivation de surface

En raison de la distribution asymétrique des états de surface dans la bande interdite du Ge (densité plus élevée d'états accepteurs dérivés de la bande de conduction), le niveau de neutralité de charge (localisé à l'énergie pour laquelle la densité d'états donneurs dérivés de la bande de valence devient égale à celle des accepteurs) se situe près de la bande de valence, ce qui a pour conséquence un comportement électrique de type p aux interfaces avec le Ge.

- Les consequences pour le fonctionnement des **nFETs** sont sérieuses, puisqu'il devient **plus difficile de créer un canal d'inversion de type n** en appliquant une tension de Grille positive. De plus, lorsque les dispositifs sont fonctionnels, **les interactions coulombiennes dégradent la mobilité des électrons**.
- Les consequences pour les **pFETs** sont *a priori* plus légères, mais finissent tout de même par limiter les performances. Les **$V_{th,p}$ sont décalés vers les valeurs positives**, ce qui doit être compensé pour limiter les courants de fuite à V_G=0V. Dans le cas du GeOI, l'interface Ge/BOX peut en plus générer un **canal de conduction parasite en inversion faible à V_{BG}=0V**. On peut y remédier en dopant le canal (dopage type n), mais cette solution dégrade la mobilité des trous. Enfin, les D_{it} importantes à l'interface Ge/high-k dégrade la pente sous le seuil (typiquement **~100mV/dec au lieu of 60mV/dec sur des canaux longs en désertion totale**). Ceci peut potentiellement **invalider la perspective de diminuer la tension d'alimentation** pour réduire la puissance consommée, ce qui est souvent cité comme un avantage des semi-conducteurs à haute mobilité.

Le capping Silicium est pour l'instant la solution de passivation la plus développée, et a été largement utilisé pour la fabrication de pFETs sub-microniques. Cependant, ses propriétés électriques sont insuffisantes pour les nFETs, ce qui le rend inadapté au CMOS Ge. L'utilisation de GeO_2 semble une alternative prometteuse, puisque son pouvoir de passivation sur les surfaces de Ge est similaire à celle du système Si/SiO_2. Mais il s'agit d'un matériau difficile à maîtriser, qui fixe des contraintes additionnelles en termes de fabrication à cause de sa stabilité thermique limité et sa haute solubilité dans l'eau. De plus, l'adéquation des couches intermédiaires de GeO_2 aux dimensions très réduites fait encore débat.

IV.3.4.b. « Tout cela en vaut-il la peine? »

Evidemment, les obstacles persistants ont tous la particularité de paraître infranchissables jusqu'à ce que quelqu'un trouve la solution. Cependant, il serait naïf de ne pas prendre en compte quelques considérations industrielles lorsque l'on évalue le potentiel d'une technologie, en particulier dans le domaine de la logique CMOS pour les nœuds avancés.

Trois menaces majeures ont été récemment listées par Caymax *et al.* concernant la viabilité de la recherche sur le CMOS Ge dans le futur proche [*Caymax'09-b*]: le timing, la rentabilité, et le Silicium.

- Il n'est pas évident que les fabricants de circuits intégrés puissent se permettre d'attendre que la technologie sur Germanium atteigne a un degré de maturité compatible avec la production à grande échelle
- Il n'est pas garanti que le gain final en performances puisse compenser les coûts additionnels de fabrication d'un procédé relativement complexe
- Il n'est même pas sûr que le CMOS sur Silicium puisse être battu sur le terrain de la performance pour des longueurs de grille extrêmement courtes (cf. effets de canaux courts, augmentation de I_{OFF} par rapport au gain en I_{ON} dans les régimes balistique et quasi-balistique [*Krishnamohan'08*], [*Rafhay'09*])

IV.3.4.c. Intérêt des alliages SiGe

Puisque la faible bande interdite et les effets tunnel font craindre pour le compromis I_{ON}/I_{OFF} aux tensions d'alimentation usuelles, une solution pourrait être de moduler la concentration de Ge en utilisant des alliages SiGe dans le canal. La Figure IV-49 montre la dépendance de la bande interdite vis-à-vis de la concentration en Ge dans du $Si_{1-x}Ge_x$ non contraint à température ambiante [*Braunstein'58*], [*People'85*].

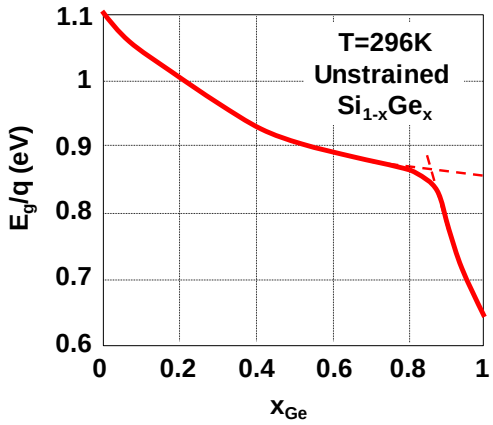

Figure IV-6: Bande interdite du $Si_{1-x}Ge_x$ non contraint à 296K [Braunstein'58]. A environ x=0.85, on peut voir la transition entre des bandgaps définis de façon Si-like (Γ-X) et Ge-like (Γ-L) (l'énergie minimale des sous-bandes de conduction correspondant respectivement à des vecteurs d'onde dirigés suivant <100> et <111>).

En règle générale, les alliages SiGe avec des concentrations en Ge inférieures à 85% ne devraient pas donner lieu à des effets tunnel importants jusqu'à V_{DD}=0.85V. Les masses effectives des porteurs sont plus basses et la mobilité plus haute que dans le Si non contraint [*Fischetti'96*], donc les dispositifs sur SiGe à concentration modérément élevée en Ge devraient présenter un gain de courant à l'état passant sans voir le courant I_{OFF} augmenter de façon spectaculaire, ce dont souffrent les transistors à canal Ge pur.

De plus, la technologie de fabrication est nécessairement plus proche de celle du Si, et moins chère, avec moins de problèmes liés à l'état d'oxydation du Ge et à ses conséquences sur les états de surface. Les couches de SiGe peuvent être obtenues par hétéroépitaxie sur Si, et la concentration en Ge peut éventuellement être augmentée par les techniques de substrats virtuels ou d'enrichissement en Ge.

Le désaccord de maille plus faible (paramètre de maille du $Si_{1-x}Ge_x$: $5.431 + 0.20x + 0.027x^2$ [*Dismukes'64*]) soulage les contraintes en termes de défectivité des zones actives, et l'épaisseur critique de l'hétéroépitaxie sur Si est compatible avec la fabrication de transistors (> 10nm pour un x_{Ge} modérément élevé). Il est donc relativement aisé de fabriquer des MOSFETs sur SiGe globalement contraint, en contrainte compressive. Les résultats présentés dans les paragraphes suivant traiteront du SiGeOI en contrainte compressive (ou c-SGOI) pour les nœuds CMOS avancés, obtenu soit par enrichissment ([*Hutin'10-c*]: c-SGOI CMOS), soit par épitaxie sélective ([*Hutin'10-d*]: co-intégration de SOI nMOS en contrainte tensile et de SGOI pMOS en contrainte compressive).

IV.4. SiGe sur Isolant (SGOI) en contrainte compressive

IV.4.1. **SGOI obtenu par enrichissement en Ge**

La technique d'enrichissement en Ge permet d'obtenir des couches fines de SGOI en contrainte compressive. A partir de cette contrainte biaxiale, une contrainte uniaxiale peut-être obtenue sur des zones actives suffisamment étroites par le mécanisme de relaxation latérale de la contrainte intervenant pendant la grauvre des mesa [*Irisawa'05-a&b*], [*Irisawa'06*]. Dans [*Hutin'10-c*], les avantages de cette approche ont été étudiés pour la première fois sur des transistors de longueur de grille de 20nm et des largeurs de zone active de 30nm active sur du c-SGOI d'épaisseur 15nm (Figure IV-52).

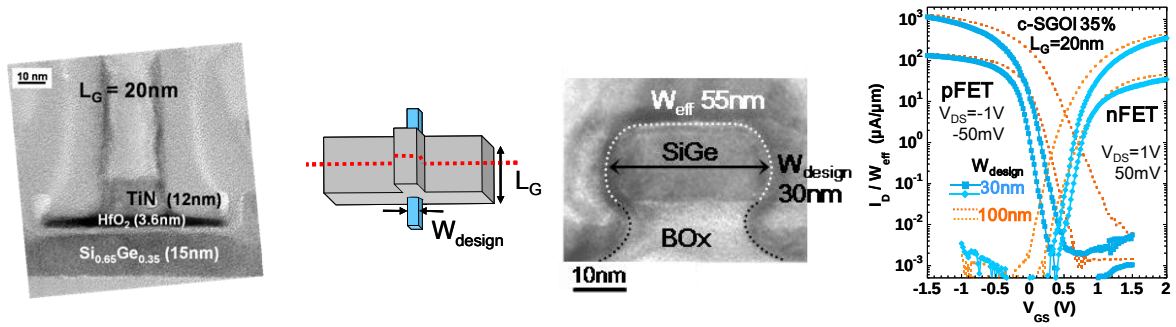

Figure IV-7: Gauche: X-TEM transverse d'un pFET sur c-SGOI 35% avec Lg=20nm. Milieu: X-TEM longitudinale d'un pFET sur c-SGOI 35% avec W_{design}=30nm (images: R. Truche). Droite: I_D-V_{GS} sur des pFETs et nFETs courts sur c-SGOI35%, et effet de la réduction de W sur le contrôlé électrostatique « trigate ».

L'enrichissement en Ge a été mené jusqu'à obtenir 15nm de c-SGOI avec une concentration en Ge de 25% et de 35%. Comme la contrainte compressive n'est pas favorable à la conduction des électrons, nous nous focalisons sur les résultats des pFETs. La contrainte uniaxiale a pour résultat une meilleure mobilité car elle provoque une déformation de la bande de valence et réduit les masses effectives des trous. Un effet secondaire positif est que ce type de contrainte est obtenu sur des canaux étroits, pour lesquels la configuration électrostatique devient de type trigate, ce qui améliore le contrôle des effets de canaux courts et donc le compromis I_{ON}-I_{OFF} dans les canaux courts.

Malgré cela, les caractéristiques des nFETs ne sont toujours pas aussi bonnes que sur SOI, on se ramène donc à une approche de type canal dual (Dual Channel). Comme l'enrichissement en Germanium localisé à l'échelle du dispositif n'est pas encore une réalité, une stratégie différente est présentée dans le paragraphe suivant, qui consiste en une épitaxie sélective de SiGe sur du SOI non contraint ou en contrainte tensile [*Andrieu'05*], [*Hutin'10-d*].

IV.4.2. **CMOS Dual Channel par épitaxie sélective de SiGe**

Afin d'obtenir un bas $V_{th,p}$ pour des applications CMOS haute performance gate-first avec grille métal et diélectrique high-k, l'approche Dual Channel émerge comme une solution basée sur la modulation de la tension de seuil par la bande interdite du canal plutôt que par un changement de travail de sortie de grille [*Harris'07*], [*Witters'10*]. Nous avons démontré dans [*Hutin'10-d*] une co-intégration Dual Channel en contrainte (tensile côté n, compressive côté p, n-sSi/p-sSiGe) à des dimensions réduites (Figure IV-66), et pour la première fois avec démonstration de cellules SRAM et d'oscillateurs en anneau fonctionnels (Figure IV-76).

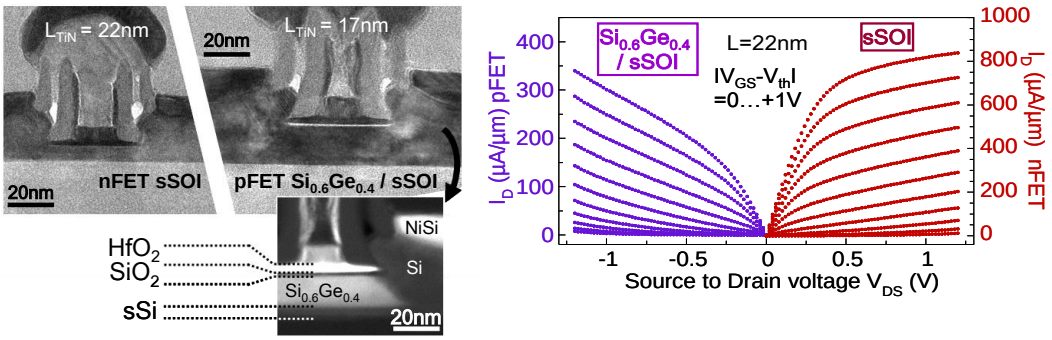

Figure IV-8: Gauche: Images HR XTEM d'un nFET sur sSOI 20% co-intégré sur la même puce qu'un pFET SiGe 40% / sSOI 20%, de longueurs de grille respectives 22nm et 17nm (T_{sSOI} ~ 8nm; $T_{SiGe/(s)SOI}$ ~ 19nm) (images: D. Cooper, A. Béché). Droite: I_D-V_{DS} mesurées (V_{GS} step=0.1V) de CMOS co-intégré (L_G=22nm) dans le cas DSCOI (nFETs sSOI et pFETs $Si_{0.6}Ge_{0.4}$/sSOI).

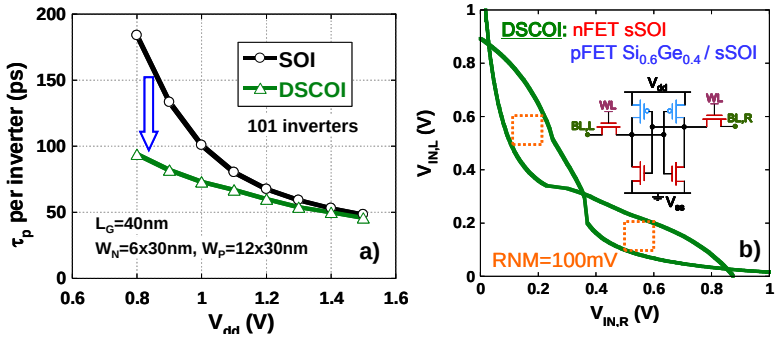

Figure IV-9: a) Temps de propagation par inverseur en fonction de la tension d'alimentation dans des oscillateurs en anneau sur SOI et DSCOI (n sSOI & p $Si_{0.6}Ge_{0.4}$/sSOI). b) Potentiel (BL,L) en fonction de (BL,R) et réciproquement pour une cellule SRAM 6T sur DSCOI avec des longueurs de grille L_G=22nm.

Nous avons mis en évidence l'influence des procédés technologiques (concentration de Ge, diffusion et surgravure) et de la réduction des dimensions sur cette architecture grâce aux techniques de caractérisation de contrainte NBED et DFEH, ainsi que des mesures à basse température. Les points suivants restent à améliorer:

- La surgravure du SiGe dans les régions S/D doit être évitée car elle provoque une relaxation de la contrainte dans la direction du transport (et donc une chute de mobilité) dans les canaux courts.
- Les $V_{th,n}$ and $V_{th,p}$ des nFETs sur sSOI et des pFETs sur s-SiGe pFETs sont effectivement bas. Par contre, il faudrait qu'ils soient légèrement moins bas pour limiter les fuites I_D à V_{GS}=0V. Cela implique (à nouveau) une optimisation de l'empilement de grille.
- Avec cette approche, les canaux des pFETs sont plus épais que ceux des nFETs. Cela est problématique au niveau du contrôle des SCE. Un amincissement du SOI avant épitaxie du SiGe pourrait y remédier.

IV.5. Transistors Schottky à canal Germanium

A ce point du manuscrit, nous avons présenté les bases de la théorie des contacts métal/semi-conducteur, du fonctionnement et de la fabrication des MOSFETs à barrière Schottky, ainsi que les atouts et limites de la technologie sur Germanium. Nous pouvons donc dans ce paragraphe analyser les caractéristiques de transistors Schottky sur Ge.

IV.5.1. **Etat de l'art, interface non dopée**

IV.5.1.a. pFETs

Entre 2005 et 2008, plusieurs études furent publiées, traitant de transistors Schottky sur Ge massif ou GeOI. Aucune d'entre elles à notre connaissance ne présente des structures avec dopage d'interface. Les données principales sont reportées dans la Table IV-5.

	[*Zhu'05*]	[*Li'06-a*]	[*Li'06-b*]	[*Maeda'06*]	[*Pethe'07*]	[*Li'08*]
Device type	pFET (ring-shaped)	pFET	pFET (ring-shaped)	pFET (back-gate)	pFET	pFET
Substrate type	n-Ge(100) bulk	n-Ge(100) bulk	n-Ge(100) bulk	p-GeOI enrichment (30nm)	Si/sGe 2nm/Si heterostructure	n-Ge bulk
Substrate doping ($at.cm^{-3}$)	a few 10^{15}	a few 10^{15}	a few 10^{15}	a few 10^{15}	N.S.	N.S.
Gate stack	TaN/HfN/HfAlO	TaN/HfO_2	TaN/HfO_2	Si/SiO_2 (back-gate, BOX 210nm)	p^+ SiGe/LTO 20nm	TaN/HfO_2
Gate insulation from the S/D	Lateral selective etching of HfN during preclean	Spacers AlN 3nm + SiO_2 15nm	Spacers AlN 4nm + SiO_2 6nm	None other than BOX	LTO spacers	Spacers
S/D Metal	NiGe	NiGe	$PtGe_2$	PtGe	NiSiGe	Pt_xGe_y
Preclean	diluted HF	N.S.	N.S.	N.S.	N.S.	HF:H_2O = 1 :100
Metal deposition	N.S.	30nm sputtering	30nm sputtering	E-beam evap.	100nm sputtering	N.S.
Germanidation anneal	600°C 1min N_2	400°C 1min	400°C N_2	400°C 30min Forming Gas	450°C 1min N_2	Laser KrF 248nm, 23ns, $0.14J.cm^{-2}$
Selective removal	NH_4OH:H_2O_2:H_2O = 1:2:5	HNO_3:H_2O = 1:20	diluted aqua regia	N.S.	Concentrated HCl	dry etch
Extracted SBH	Φ_{bp} = 0.16eV	Φ_{bp}= -0.08eV	Φ_{bp}= -0.1eV	Φ_{bp}= 0.05eV	Φ_{bp}= 0.1eV	Φ_{bp}= 0.08eV
Gate length (µm)	8	8	8	200	3	10
Subthreshold swing (mV/dec)	250	137	133	N.S.	N.S.	~600
I_{on}/I_{off} (dec)	2	2	3.5	N.S.	N.S.	1.5

Table IV-2: Résumé des étapes de fabrication principales et des résultats de l'état de l'art des p-SBFETs à canal Ge. N.S. signifie "Non Spécifié". I_{on} et I_{off} sont définis par rapport à V_{th}.

Il convient de noter que les valeurs de SBH rapportées dans [*Zhu'05*], [*Li'06-a*] et [*Li'06-b*] ne sont pas cohérentes les unes avec les autres. On pourra cependant retenir que:

- Les niveaux de courants semblent plus élevés que sur des dispositifs PtSi/Si équivalents
- Les courants de fuites sont diminués dans [*Li'06-b*] avec l'implémentation de S/D en PtGe
- Les performances restent limitées par la pente sous le seuil, ce qui peut soit être dû aux D_{it} à l'interface avec l'empilement de Grille, soit à la distance de non-recouvrement entre la Source et la Grille

La première fabrication d'un p-SBFET sur GeOI a été publiée dans [*Maeda'06*]. La couche de Ge de 30nm d'épaisseur a été obtenue par enrichissement (fraction molaire finale: ~99%). La structure finale n'est pas celle d'un MOSFET classique puisque la face arrière du substrat et l'oxyde enterré (210nm d'épaisseur) jouent respectivement le rôle de l'électrode de grille et du diélectrique de grille. Il n'est donc pas pertinent de commenter la pente sous le seuil et les valeurs de V_{GS} jusqu'à 40V. La SBH extraite pour le contact PtGe/Ge (0.05eV, méthode TE I-V, η=1.05), est cohérente avec d'autres observations expérimentales et la théorie de l'ancrage du niveau de Fermi. A V_{DS} faible, le ratio des courants à l'état passant et l'état bloqué est de l'ordre de 2.5 à 3 décades.

IV.5.1.b. nFETs

Plutôt que de compenser une SBH élevée pour les électrons par une couche de dopage d'interface, de fines couches de « désancrage » du niveau de Fermi (~2nm) ont été intégrées dans [*Kobayashi'08*] et

[*Nishimura'08*] (respectivement SiN et GeO_x) pour la fabrication de n-SBFETs à canal Ge. Qualitativement, il est clairement démonté que le comportement électrique de diodes sur n-Ge devient progressivement ohmique avec l'augmentation de l'épaisseur de la couche d'interface.

Les nFETs fabriqués sont fonctionnels, mais les caractéristiques I_D-V_{DS} présentées dans les deux études ont surtout pour but de démontrer la faisabilité du concept plutôt que des performances optimales (pas d'information sur la pente sous le seuil). On peut tout de même noter que le rapport entre I_{ON} et I_{OFF} ([*Kobayashi'08*]: I_D à V_{DS}=1V; $V_{GS,on}$=10V et $V_{GS,off}$=0V - [*Nishimura'08*]: I_D à V_{DS}=1V; $V_{GS,on}$=V_{th}+0.6V et $V_{GS,off}$=V_{th}-0.2V) reste voisin d'une décade (Table IV-6).

	[*Kobayashi'08*]	[*Nishimura'08*]
Device	nFET	nFET
Substrate type	p-Ge(100) bulk	p-Ge(100) bulk
Substrate doping ($at.cm^{-3}$)	N.S.	undoped
Gate stack	Al/LTO/GeON	Au/GeO_2 30nm
Gate insulation from the S/D	SiN liner 2nm	None other than GeO_2
S/D Metal	Al +SiN 2nm (depinning)	Al +GeO_x 2nm (depinning)
Preclean	Wet treatment + nitride liner deposition	Oxidation before deposition
Metal deposition	N.S.	Thermal evap.
Germanidation anneal	No germanidation	No germanidation
Selective removal	No germanidation	No germanidation
Extracted SBH	Φ_{bn}=0.1eV	Φ_{bn}=0.17eV
Gate length (µm)	1.5	190
Subthreshold swing (mV/dec)	N.S.	N.S.
I_{on}/I_{off} (dec)	~1	~1

Table IV-3: Résumé des étapes de fabrication principales et des résultats de l'état de l'art des n-SBFETs à canal Ge. N.S. signifie "Non Spécifié". I_{on} et I_{off} sont définis par rapport à V_{th}.

Conclusion générale

Il s'agit à présent de récapituler les points importants de chaque chapitre de ce manuscrit, et sur cette base de conclure quant à la pertinence de combiner des Source/Drain métalliques avec un canal à base de Germanium pour l'intégration CMOS à dimensions agressivement réduites.

Contacts métal/semi-conducteur

En polarisation inverse (courant circulant du métal vers le semi-conducteur), la densité de courant d'interface d'un contact métal/semi-conducteur est extrêmement dépendante de la taille et de la forme de la barrière Schottky. De plus, celles-ci sont généralement fortement dépendantes du niveau de dopage à l'interface (position du niveau de Fermi dans le semi-conducteur), et des tensions appliquées.

Dans le Silicium et à plus forte raison dans le Germanium, la formation de la barrière Schottky est fortement influencée par le phénomène d'ancrage du niveau de Fermi à un niveau de neutralité de charge surfacique localisé près de la bande de valence. En conséquence, la majorité des contacts métal/Si et métal/Ge sont caractérisés par une forte préférence pour l'injection des trous, avec une faible dépendance vis-à-vis du travail de sortie du métal. Malgré cela, ces valeurs de hauteur de barrière pourraient ne pas être suffisantes pour satisfaire les conditions fixées par l'ITRS en termes de résistivité de contact, à moins que le semi-conducteur ne soit fortement dopé.

De nos observations sur les contacts sur semi-conducteurs dégénérés de type p, caractérisés par des barrières à la fois petites et fines, nous avons déduit qu'il était difficile de conclure qualitativement sur le choix du métal et du niveau de dopage exact pour arriver à une résistivité de contact donnée. Cependant, d'après notre cas d'étude à une dimension, il semble qualitativement que la SBH d'un contact semi-conducteur intrinsèque conduise dans le meilleur des cas (Φ_{bp}=0eV) à une résistivité de contact supérieure d'environ un ordre de grandeur (en polarisation inverse) par rapport au cas dégénéré.

Il est donc tentant de conclure qu'un dopage élevé à l'interface de contact est absolument nécessaire quel que soit le métal choisi, de sorte de ne pas perdre en résistance de contact ce que les S/D métalliques apportent en résistance de couche dans les accès. Il convient cependant de noter que ces valeurs dépendent de l'hypothèse selon laquelle la distance entre Source et Grille est inférieure à la zone de désertion de la jonction Schottky, d'où la nécessiter d'examiner le cas d'une structure SBFET complète.

Transistors à Barrière Schottky sur SOI

Le remplacement des jonctions dopées par des jonctions métal/semi-conducteurs est motivé à l'origine par la réduction des résistances série, un bas budget thermique de fabrication, une immunité aux effets de canaux courts, et l'élimination des effets bipolaires parasites. Ce dernier avantage peut être directement mis de côté dans le cas d'une intégration de dispositifs sur films minces de SOI en désertion totale (FDSOI).

Concernant le premier, la réduction des résistances série, la conclusion n'est pas triviale. En règle générale, on peut considérer que la résistivité de contact doit être pour cela inférieure à 10^{-8} $\Omega.cm^2$, ce qui n'est pas le cas naturellement pour des contacts métal/Si intrinsèque. Si le dopage d'interface est une solution, alors celle-ci emporte avec elle l'avantage de l'immunité aux effets de canaux courts. De plus, il résulte également d'une analyse du fonctionnement d'un SBFET que le dopage d'interface est souhaitable pour la réduction des courants de fuite à l'état bloqué, et l'optimisation de la pente sous le seuil dans le cas où la distance latérale Source/Grille serait non nulle. Le compromis performances/contrôle des effets de canaux courts a été étudié au cours de cette thèse dans des p-SBFETs à simple et double grille jusqu'à 20nm. En particulier, l'architecture à double grille permet effectivement de compenser par un regain du contrôle électrostatique sur le canal l'implantation d'extensions fortement dopées.

Il existe diverses techniques de ségrégation des dopants à l'interface parmi lesquelles la plus efficace semble être l'implantation à travers le siliciure (ITS). Celle-ci a d'ailleurs permis la démonstration par IBM de nFETs et pFETs Schottky à métal unique relativement performants jusqu'à une longueur de grille de 20nm. Ces résultats montrent d'ailleurs l'avance de l'approche à métal unique par rapport à celle dite « dual metal », pour laquelle des difficultés liées à la difficulté d'intégrer des siliciures de terres rares (favorables à l'injection d'électrons) sont actuellement rencontrées. Néanmoins, ils montrent aussi qu'en dépit de résistivités de contact parmi les plus basses mesurées sur de tels contacts (ρ_c = 6~7×10^{-9} $\Omega.cm^2$), et en dépit d'une Source dont le bord est situé à l'aplomb de la Grille, que les performances des SBFETs sur SOI restent derrières celles des MOSFETs conventionnels. Cela infirme donc la remarque de la fin du paragraphe précédent, quant à l'éventuel rôle bénéfique d'écrantage du potentiel de grille sur le potentiel interne de la jonction Schottky Source/Canal. En d'autres termes, la nécessité du dopage d'interface est confirmée pour les SBFETs sur SOI.

L'implémentation de S/D totalement métalliques ne semble pas être une nécessité absolue pour améliorer les performances de dispositifs planaires, symétriques et à simple grille sur FDSOI, ni pour faciliter la réduction de leurs dimensions. Ce module peut par contre

être important pour l'élaboration d'architectures différentes telles que le transistor à Double Grille vertical. De plus, les techniques de ségrégation des dopants permettent d'activer les dopants à basse température. On peut finalement remarquer que les contraintes concernant la modulation de la SBH par le dopage d'interface, et en particulier le niveau d'activation électrique recherché, peuvent être amoindries par le choix d'un semi-conducteur à bande interdite plus faible tel que le Germanium ou les alliages Silicium-Germanium.

Transistors sur GeOI ou SiGeOI en contrainte compressive

En raison de ses propriétés de transport *a priori* supérieures, le MOSFET à canal Germanium a suscité un regain d'intérêt faisant suite à quatre décennies de relative inactivité sur le sujet. Cela est lié à l'introduction des diélectriques de grille high-k, puisqu'auparavant l'oxyde natif de Germanium causait des problèmes dus à sa solubilité dans l'eau et sa stabilité thermique limitée.

Pourtant, les interfaces Ge/high-k ne sont la plupart du temps pas très bonnes (caractéristiques C-V dégradées), à moins que des précautions particulières ne soient prises pour la passivation d'interface. Au cours des dernières années, des couches de Silicium partiellement oxydé ont été largement utilisées pour servir d'interface avec le high-k, menant en particulier à la fabrication de pFETs Ge submicroniques jusqu'à une longueur de grille de 30nm démontrée dans le cadre de cette thèse. Malgré cela, les densités d'états d'interface alors obtenues continuent d'entretenir les doutes quand à la réalisation de CMOS Ge.

En effet, il a été montré qu'une densité d'états de surface de type accepteur intrinsèquement élevée était à l'origine du comportement "type p" des surfaces de Germanium. Dans les pFETs, cela provoque un décalage de $V_{th,p}$ vers les valeurs positives, et pour les nFETs un retardement de l'inversion du canal aux tensions de grille positives ainsi que des interactions coulombiennes limitant la mobilité des électrons. Bien que le problème de $V_{th,p}$ puisse être compensé par un contre-dopage de type n du film de Ge, cette solution fait diminuer la mobilité des trous jusqu'à des valeurs proches de celles observées dans le Silicium. De plus, à cause des D_{it}, la pente sous le seuil reste non-idéale dans les canaux longs (100mV/dec au lieu de 60mV/dec à 300K).

La meilleure façon connue aujourd'hui de passiver un maximum de ces états de surface accepteurs est de faire croître des couches d'interface de GeO_2 (ironiquement, puisque le GeO_2 fut le point bloquant qui justifia l'abandon temporaire du Ge). Cela implique en revanche un bas budget thermique de fabrication (activation des dopants à basse température ou schéma d'intégration "gate-last"). De plus, la possibilité de réduire l'épaisseur de la couche de GeO_2 tout en conservant son efficacité est de nos jours un sujet controversé.

En outre et concernant les nFETs, la faible solubilité solide et la diffusivité élevée des impuretés de type donneur (As, P) rend leur fabrication encore plus difficile. En conséquence,

le CMOS Ge a tendance à se trouver délaissé au profit d'essais de co-intégration "Dual Channel" p-GeOI/n-SOI. Néanmoins, même lorsqu'il s'agit de substrats sur isolant, les fuites par effet tunnel côté Drain limitent les caractéristiques à l'état bloqué pour les tensions d'alimentation supérieures à 0.7V.

Deux solutions peuvent alors être proposées:

- La formation à basse température de Source et Drain métalliques qui pourrait être compatible avec la stabilité thermique de la couche de passivation de surface, ainsi que remédier au problème de la diffusivité des dopants de type n au-delà de 550°C.
- L'utilisation d'alliages SiGe, avec des masses effectives plus faibles que le Si mais une bande interdite plus grande et des densités d'états d'interface moins élevées que dans le Ge. Cela pourrait partiellement résoudre les problèmes de décalage de $V_{th,p}$ et réduire les fuites de jonction par effet tunnel (TAT, BTBT). De plus, l'épaisseur critique d'hétéro épitaxie SiGe/Si est plus élevée que pour le Ge, ce qui implique moins de problèmes de défauts cristallins, et la possibilité de fabriquer des pFETs sur SiGe en contrainte compressive complète (sans relaxation).

Des transistors n- et pFETs de longueurs de grille jusqu'à 20nm sur SGOI en contrainte compressive ont été étudiés dans le cadre de cette thèse, montrant des mobilités supérieures au cas SOI de référence, en particulier dans les canaux étroits pour lesquels le processus de relaxation latérale mène à une contrainte uni-axiale bénéfique dans la direction du transport. Cependant, les performances des nFETs sont inférieures à celles de leurs homologues sur SOI, et le schéma d'intégration basé sur l'enrichissement en Germanium n'est pour le moment pas applicable au niveau transistor.

Une co-intégration "Dual Strained Channel" a par ailleurs été réalisée par le moyen d'une épitaxie sélective de SiGe sur SOI ou sSOI, avec des transistors jusqu'à 17nm de longueur de grille ainsi que des cellules SRAM 6T et des oscillateurs en anneaux fonctionnels. Le compromis entre l'augmentation de la mobilité et le décalage de $V_{th,p}$ avec la concentration en Germanium a été mis en évidence, et les étapes technologiques critiques pour l'optimiser ont été identifiées (éviter la sur-gravure du SiGe des S/D, minimiser les D_{it} par la passivation de l'interface avec le high-k).

Bien que la composante tunnel du courant de fuite ait été efficacement réduite, les valeurs de $V_{th,p}$ semblent par contre subir un décalage trop important qui a pour conséquence un courant de drain élevé à V_{GS}=0V. Ce décalage de $V_{th,p}$ sur les dispositifs sur c-SGOI étudiés est en partir dû à la structure des bandes (bande interdite réduite et contribution additionnelle de la contrainte compressive), mais aussi à des charges fixes et à la densité d'états d'interface. Cela indique que la passivation d'interface avec le high-k resterait un problème non négligeable même pour des concentrations modérées en Germanium (20-40%).

Canal Ge et Source/Drain métalliques

Nous avons identifié l'intérêt des substrats à base de Germanium comme alternative au SOI pour les SBFETs, souligné par le besoin de SBH intrinsèques plus faibles que procureraient des matériaux à faible bande interdite. Telle était déjà la raison évoquée dans l'introduction générale. Nous avons entretemps confirmé que le dopage d'interface était nécessaire sur SOI, et probablement à peine suffisant pour obtenir des performances comparables aux MOSFETs conventionnels sur SOI.

De la même façon, nous avons identifié l'intérêt des SBFETs comme alternative aux MOSFETs conventionnels pour le CMOS Ge, mais pas exactement pour les raisons citées dans l'introduction générale.

En effet, l'étude de l'état de l'art des SBFETs à canal Ge montre qu'il y a peu de chance que les dispositifs à Source et Drain métalliques sans couche de dopage d'interface soient des compétiteurs crédibles (pente sous le seuil élevée, rapport I_{ON}/I_{OFF} faible). Les SBFETs ne sont donc probablement pas la solution espérée pour obtenir des jonctions extrêmement abruptes ou se passer du dopage de type n pour le CMOS Ge. Par contre, leur intégration peut permettre l'activation à basse température par ségrégation des dopants, résolvant ainsi les problèmes de diffusivité de l'Arsenic et du Phosphore au-delà de 550°C, ainsi que ceux liés à l'instabilité thermique d'une couche de passivation en GeO_2.

En conclusion:

- La passivation des états accepteurs en surface du Ge ou du SiGe doit être traitée en priorité. Des études récentes indiquent qu'un procédé à basse température est capital pour éviter des états d'oxydation du Germanium indésirables. Les couches d'interface de GeO_2 obtenues par oxydation haute pression (HPO) suivies par recuit d'oxydation à basse température (LOA) représentent une voie prometteuse. Cependant il convient de déterminer auparavant si ces couches permettent effectivement d'obtenir des EOT subnanométriques sans pour autant perdre de leurs qualités.
- Même si les SBH sont plus faibles que sur SOI, les SBFETs sur Ge ou SiGe requièrent probablement des Source et Drain dopés par ségrégation pour l'optimisation de leurs performances. La technique d'implantation à travers le siliciure (ITS) semble la plus efficace, mais le recuit pour amener les dopants à l'interface doit être effectué à basse température afin de ne pas dégrader la couche de passivation d'interface avec le diélectrique high-k. De la sorte, il n'est pas nécessaire d'avoir recours à un schéma d'intégration "gate-last", et la

diffusivité des dopants de type n dans le Ge ne devrait plus être un problème. Pour une approche à métal unique pour les S/D, le NiGe est sans doute le choix le plus approprié, et le retrait sélectif du métal n'ayant pas réagi est de surcroît plus aisé que dans le cas de la germaniuration Pt.

Telles sont les conditions sous lesquelles les avantages respectifs du canal Ge et des Source et Drain Schottky pourraient se cumuler. Il reste cependant à établir la faisabilité de la première condition pour les nœuds agressifs, ainsi qu'à démontrer quantitativement l'intérêt de la seconde en termes de performances et de contrôle des effets de canaux courts vis-à-vis des MOSFET conventionnels à canal Si.

Liste de publications

Publications en tant que premier auteur

1. **L. Hutin**, S. Koffel, C. Le Royer, P. Scheiblin, V. Mazzocchi, S. Deleonibus, "On the extraction of dopant activation level for Boron-doped Thin Germanium-On-Insulator (GeOI)"; *Proceedings of the 4th Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits (EuroSOI 2008)*; pp. 118-119; 2008

2. **L. Hutin**, C. Le Royer, S. Deleonibus; "Le transistor Schottky sur substrat Germanium sur Isolant (GeOI): Etude préliminaire" ; *Proceedings of the Journées National du Réseau des Doctorants en Microélectronique 2008 (JNRDM 2008)*; 2008

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2. "Activation Level in Boron-doped Thin Germanium-On-Insulator (GeOI): Extraction Method and Impact of Mobility"; **E-MRS 2008 Spring Meeting** Symposium J: Beyond Silicon Technology: Materials and Devices for Post-Si CMOS, Strasbourg, France

3. "Schottky Barrier Height Extraction in Ohmic Regime: Contacts on Fully Processed GeOI Substrates"; **ECS 2008 Fall Meeting** Symposium SiGe, Ge and Related Compounds, Honolulu, HI, USA

4. "Dual Metallic Source and Drain Integration on Planar Single and Double Gate SOI CMOS down to 20nm: Performance and Scalability Assessment"; **IEDM 2009**, Baltimore, MD, USA

5. "A New Step in GeOI pFET Scaling and Off-State Current Reduction: 30nm Gate Length and Record I_{ON}/I_{OFF} Ratio"; **VLSI TSA 2010**, Hsinchu, Taïwan

6. "20nm Gate Length Trigate SGOI pMOSFETs for High Performance CMOS"; **VLSI 2010**, Honolulu, HI, USA

7. "Dual Strained Channel Co-Integration into CMOS, RO and SRAM cells on FDSOI down to 17nm Gate Length"; **IEDM 2010**, San Francisco, CA, USA (décembre 2010)

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1. "Le transistor Schottky sur substrat Germanium sur Isolant (GeOI): Etude préliminaire" ; **JNRDM 2008**, présentation d'un poster, Bordeaux, France

2. "Ge-based substrates and devices"; **Séminaire invité à l'INP Grenoble (Master nanotech)**, Grenoble, France

3. Récipiendaire du **Norman Hackermann Young Author Award 2009** de l'Electrochemical Society

TITLE: Study of Schottky Barrier MOSFETs on SOI, SiGeOI and GeOI Substrates

ABSTRACT

Until the early 2000's Dennard's scaling rules at the transistor level have enabled to achieve a performance gain while still preserving the basic structure of the MOSFET building block from one generation to the next. However, this conservative approach has already reached its limits as shown by the introduction of channel stressors for the sub-130 nm technological nodes, and later high-k/metal gate stacks for the sub-65 nm nodes. Despite the introduction of high-k gate dielectrics, constraints in terms of gate leakage and reliability have been delaying the diminution of the equivalent oxide thickness (EOT). Concurrently, lowering the supply voltage (V_{DD}) has become a critical necessity to reduce both the active and passive power density in integrated circuits. Hence the challenge: how to keep decreasing both gate length and supply voltage faster than the EOT without losing in terms of ON-state/OFF-state performance trade-off?

Several solutions can be proposed aiming at solving this conundrum for nanoscale transistors, with architectures in rupture with the plain old Silicon-based MOSFET with doped Source and Drain invented in 1960. One approach consists in achieving an I_{ON} increase while keeping I_{OFF} (and V_{th}) mostly unchanged. Specifically, two options are considered in detail in this manuscript through a review of their respective historical motivations, state-of-the-art results as well as remaining fundamental (and technological) challenges: i/ the reduction of the extrinsic parasitic resistance through the implementation of metallic Source and Drain (Schottky Barrier FET architecture); ii/ the reduction of the intrinsic channel resistance through the implementation of Germanium-based mobility boosters (Ge CMOS, compressively-strained SiGe channels, n-sSi/p-sSiGe Dual Channel co-integration). In particular, we study the case of thin films on insulator (SOI, SiGeOI, GeOI substrates), a choice justified by: the preservation of the electrostatic integrity for the targeted sub-22nm nodes; the limitation of ambipolar leakage in SBFETs; the limitation of junction leakage in (low-bandgap) Ge-based FETs. Finally, we show why, and under which conditions the association of the SBFET architecture with a Ge-based channel could be potentially advantageous with respect to conventional Si CMOS.

KEYWORDS

Microelectronics, MOSFET, CMOS Technology, Schottky Barrier, SBFET, Silicon On Insulator, Germanium On Insulator, high mobility channels, Dual Channel

TITRE: Etude des transistors MOSFET à barrière Schottky, à canal Silicium et Germanium sur couches minces

RESUME

Jusqu'au début des années 2000, les règles de scaling de Dennard ont permis de réaliser des gains en performance tout en conservant la structure de la brique de base transistor d'une génération technologique à la suivante. Cependant, cette approche conservatrice a d'ores et déjà atteint ses limites, comme en témoigne l'introduction de la contrainte mécanique pour les générations sub-130nm, et les empilements de grille métal/high-k pour les nœuds sub-65nm. Malgré l'introduction de diélectriques à forte permittivité, des limites en termes de courants de fuite de grille et de fiabilité ont ralenti la diminution de l'épaisseur équivalente d'oxyde (EOT). De façon concommitante, la diminution de la tension d'alimentation (V_{DD}) est devenue une priorité afin de réduire la densité de puissance dissipée dans les circuits intégrés. D'où le défi actuel: comment continuer de réduire à la fois la longueur de grille et la tension d'alimentation plus rapidement que l'EOT sans pour autant dégrader le rapport de performances aux états passant et bloqué (ON et OFF) ?

Diverses solutions peuvent être proposées, passant par des architectures s'éloignant du MOSFET conventionnel à canal Si avec source et drain dopés tel que défini en 1960. Une approche consiste en réaliser une augmentation du courant passant (I_{ON}) tout en laissant le courant à l'état bloqué (I_{OFF}) et la tension de seuil (V_{th}) inchangés. Concrètement, deux options sont considérées en détail dans ce manuscrit à travers une revue de leurs motivations historiques respectives, les résultats de l'état de l'art ainsi que les obstacles (fondamentaux et technologiques) à leur mise en œuvre : i/ la réduction de la résistance parasite extrinsèque par l'introduction de source et drain métalliques (architecture transistor à barrière Schottky) ; ii/ la réduction de la résistance de canal intrinsèque par l'introduction de matériaux à haute mobilité à base de Germanium (CMOS Ge, canaux SiGe en contrainte compressive, co-intégration Dual Channel n-sSi/p-sSiGe). En particulier, nous étudions le cas de couches minces sur isolant (substrats SOI, SiGeOI, GeOI), un choix motivé par: la préservation de l'intégrité électrostatique pour les nœuds technologiques sub-22nm; la limitation du courant de fuite ambipolaire dans les SBFETs; la limitation du courant de fuites de jonctions dans les MOSFETs à base de Ge (qui est un matériau à faible bandgap). Enfin, nous montrons pourquoi et dans quelles conditions l'association d'une architecture SBFET et d'un canal à base de Germanium peut être avantageuse vis-à-vis du CMOS Silicium conventionnel.

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