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Abstract

Due to the continuously scaling down of CMOS technology, system-on-chips (SoCs) reliability becomes important in sub-90 nm CMOS node. Integrated circuits and systems applied to aerospace, avionic, vehicle transport and biomedicine are highly sensitive to reliability problems such as ageing mechanisms and parametric process variations. Novel SoCs with new materials and architectures of high complexity further aggravate reliability as a critical aspect of process integration. For instance, random and systematic defects as well as parametric process variations have a large influence on quality and yield of the manufactured ICs, right after production. During ICs usage time, time-dependent ageing mechanisms such as negative bias temperature instability (NBTI) and hot carrier injection (HCI) can significantly degrade ICs performance.

Design-for-reliability (DFR) aims to consider reliability problems during the design phase of integrated circuits (ICs) and systems. Coping with reliability issues has significant importance in terms of both cost reduction and product time-to-market. In order to realize design specification at required reliability levels, it is necessary to carry out research work on defects modeling, reliability methodology development, reliability analysis/simulation, failure prediction and reliability optimization/enhancement. Previous reliability-aware work during SoCs design phase can provide useful information to ICs designers, which help them to avoid pessimistic design and reserve appropriate design space to failure boundary.

This thesis concentrates on reliability-aware methodology development, reliability analysis based on simulation as well as failure prediction of CMOS 65 nm analog and mixed signal (AMS) ICs. Sigma-Delta ($\Sigma\Delta$) modulators are concerned as the object of reliability study at system level. A hierarchical statistical approach for reliability is proposed to analysis the performance of $\Sigma\Delta$ modulators under ageing effects and process variations. Statistical methods including correlation analysis, design of experiments, regression analysis and response surface modeling are combined into this analysis flow.

Based on 65 nm CMOS technology, some typical analog circuits are studied with reliability-aware simulation methodologies. A co-evaluation reliability analysis flow for ageing effects and process variations is proposed and applied to current mirrors and a dynamic comparator. A reliability simulation approach based on Pareto fronts is presented and used to a classic miller operation amplifier. Ageing degradation in a non-overlapping clock distributor is studied.

At system level, an ultra low power 400 Hz second order low-pass continuous-time (CT) $\Sigma\Delta$ modulator is designed for cardiac pacemaker application. The reliability study concludes that in low power, low order CT $\Sigma\Delta$ modulator, feedback loop is less reliable than analog loop filter. DAC is the most sensitive building block. Comparing with HCI, NBTI is the dominate effect in the designed CT $\Sigma\Delta$ modulator. Besides, a 125 kHz third order CT $\Sigma\Delta$ modulator is implemented to study clock jitter effects. It presents that NBTI mechanism can induce clock jitter in clock distributor for CT $\Sigma\Delta$ modulator. As a consequence, modulator performance is severely degraded due to NBTI effect. Moreover, reliability-aware design of CT $\Sigma\Delta$ modulator is summarized.

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List of Acronyms

AAF Anti-Aliasing Filter

ADC Analog-to-Digital Converter

AMS Analog and Mixed Signal

ANN Artificial Neural Network

ASIC Application-specific Integrated Circuit

BBD Box-Behnken design

BERT Berkeley Reliability Tools

BSIM Berkeley Short-channel IGFET Model

BTI Biased Temperature Instability

CAD Computer-aided Design

CCD Central Composite Designs

CENT Cost-Effective Noise-Tolerant

CHC Channel Hot Carrier

CHE Channel Hot Electron

CIFB Cascaded Integrators with Feedback

CRFB Cascaded Resonators with Feedback

CIFF Cascaded Integrators with Feedforward

CM Common-Mode

CMFB Common-Mode Feedback

CMOS Complementary Metal Oxide Semiconductor

CT Continuous-Time

dBFS dB Full Scale

DAC Digital to Analog Converter

DFR Design for Reliability

DoE Design of Experiments

DFY Design for Yield

DR Dynamic Range

DT Discrete-Time

EM Electron Migration

EMC Electro Magnetic Compatibility

ENOB Equivalent Number of Bits

FIR Finite Impulse Response

FIT Failure-in-Time

FSI Maximum average feedback current

GBW Gain Bandwidth product

HBD Hard Breakdown

HCD Hot Carrier Degradation

HCI Hot Carrier Injection

HKMG High-K Metal-gate

IBN In-Band Noise

IC Integrated Circuit

IEEE Institute of Electrical and Electronics Engineers

IM3 3^{rd}-order harmonics

ITRS International Technology Roadmap for Semiconductors

L transistor Length

LER Line Edge Roughness

LHS Latin Hypercube Sampling

LNA Low Noise Amplifier

LP Low Pass

LUT Lookup Tables

MAS-MRF Master-and-Slave MRF

MC Monte-Carlo

MOO Multi-objective Optimization

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MRF Markov Random Field

MTTF Mean-Time-to-Failure

NBTI Negative Bias Temperature Instability

NMOS N-Channel Metal Oxide Semiconductor

NMR N-tuple Modular Redundancy

NTF Noise Transfer Function

Op-Amp Operation Amplifier

OSR Oversampling Ratio

OTA Operational Transconductance Amplifier

OTV Oxide Thickness Variation

PB Plackett-Burman

PBTI Positive Bias Temperature Instability

PM Phase Margin

PMOS P-Channel Metal Oxide Semiconductor

POF Probability of Failure

PSD Power Spectral Density

PSG Poly-silicon Granularity

PVT Process-Voltage-Temperature

RC Resistor Capacitor

RDF Random Dopant Fluctuations

RF Radio Frequency

RMSE Root-mean-square Error

RRSE Root-Relative-Square Error

RSM Response Surface Modeling

RTN Random Telegraph Noise

RZ Return-to-Zero

SAR-ADC Successive Approximation Analog-to-Digital Converter

SBD Soft Breakdown

SC Switched Capacitor

SDM Sigma-Delta Modulator

SET Single Event Transient

SEU Single Event Upsets

SFDR Spurious-Free-Dynamic-Range

SNDR Signal-to-Noise-plus-Distortion Ratio

SNR Signal-to-Noise Ratio

SoCs Systems-on-Chip

SOFR Sum-of-Failure-Rates

SPICE Simulation Program with Integrated Circuit Emphasis

SQNR Signal-to-Quantization-Noise-Ratio

SSTA Statistical Static Timing Analysis

STA Static Timing Analysis

STF Signal Transfer Function

TBD Time-to-Breakdown

TCAD Technology Computer-aided Design

TDDB Time-Dependent Dielectric Breakdown

TFR Test for Reliability

TMR Triple Module Redundancy

TTF Time-to-Failure

W transistor Width

Résumé Français

I Introduction

A l'aide du développement de la technologie Complementary Metal-oxide-semiconductor (CMOS) dans le system on chips (SoCs), les circuits ainsi que les systèmes électroniques s'intègrent dans un seul chip. Du fait de la réduction de la géométrie des composants, la fiabilité devient un défi important. Le problème s'aggrave dans les SoCs fabriqué avec de nouveaux matériaux et d'architectures complexes. Les circuits intégrés (ICs) et les systèmes impliqués dans l'aéro-spatial, avionique, véhicule de transport et la biomedecine sont très sensibles au problème de fiabilité, entre autre, le mécanisme de vieillissement et les variations paramétriques du process.

L'ITRS (International Technology Roadmap for Semiconductors), un groupe de travail composé d'experts internationaux dans le domaine de la microélectronique, met annuellement à jour une feuille de route identifiant les objectifs et les verrous technologiques des futures technologies CMOS.

La fiabilité des ICs est définie ainsi : la capacité d'un circuit ou un système intégré à maintenir ses paramètres durant une période donnée sous des conditions définies. Les rapports ITRS 2011 considère la fiabilité comme un aspect critique du processus d'intégration. Par conséquent, il faut faire appel des méthodologies innovatrices prenant en compte la fiabilité afin d'assurer la fonctionnalité du SoCs et la fiabilité dans les technologies CMOS à l'échelle nanométrique. Cela nous permettra de développer des méthodologies indépendantes du design et de la technologie CMOS, en revanche, spécialisées en fiabilité.

Ce résumé en français est composé de six sections. La section II discute la physique des phénomènes de vieillissement et la variabilité des transistors. La section III donne un aperçu des méthodologies pour l'analyse de la fiabilité. Dans la section IV, on étudie le vieillissement et la variabilité des transistors en technologie CMOS 65 nm. La section V présente les méthodologies que on a proposé à section III, en CMOS 65 nm d'un modulateur $\Sigma\Delta$. La première est une implémentation temps continu. La simulation du circuit au niveau transistor permet d'évaluer une architecture monobit sur une bande passante de 400 Hz et une fréquence de sur-échantillonnage de 32 KHz. En plus, on étudie le bruit d'horloge dan le generateur d'horloges à phase decalee. Ce résumé est conclu dans la section VI.

II La Fiabilité

Avec la miniaturisation toujours plus poussée, la fiabilité des composants CMOS devient de plus en plus difficile à assurer. Parmi les sources de dégradation, on peut citer les champs électriques intenses qui, d'une part dégradent lentement la qualité de l'oxyde de grille conduisant à son claquage (Time Dependent Destructive Breakdown) et d'autre part altérent les caractéristiques des transistors tels que le gain de transconductance et la

tension de seuil par l'injection de porteurs chauds. Un autre phénomène appelé Negative Bias Temperature Instability, qui apparaît à des températures élevées et sous certaines conditions de polarisation des transistors PMOS, provoque également un décalage de la tension de seuil. Ces phénomènes de dégradation constituent des limitations critiques, notamment pour les circuits analogiques qui requièrent des tensions de seuil stables.

II.a Le vieillissement des transistors

La fiabilité est un facteur important dans la conception et l'opération des systèmes d'ingénierie. La problématique de la fiabilité des circuits intégrés est constituée notamment par les effets spatiaux, les effets environnementaux, les effets transitoires et les effets du vieillissement. Les effets spatiaux proviennent des variations du processus de la manufacture de silicone qui se traduit par des fluctuations de la performance des ICs. Lors les ICs s'opèrent au-dessous des conditions minimales exigées, la perte du champ aura lieu avant l'usage d'ICs. Le deuxième problème est celui des effets environnementaux (nommé également les variations dynamiques). Ceci contient les variations de la tension fournie (V_{dd}), les fluctuations de la température, la charge de travail dépendant et la compatibilité électromagnétique (EMC). Ces effets sont fortement dépendant de l'environnement de travail des ICs. Le troisième comportement non fiable est l'effet transitoire, entre autre, les radiations, la dialogue croisée ou rebond de base. Enfin et surtout, l'effet du vieillissement a fait l'objet des études intensives du fait de la réduction d'échelle durant les dernières décennies. Comme illustré dans la Figure 1, seuls les effets spatiaux auront lieu durant la phase de manufacture d'IC et impacte le champ paramétrique des ICs. Les trois autres effets auront lieu durant l'usage des ICs. En général, tous ces problèmes de fiabilité peut conduire à une dégradation significative de la performance des ICs.

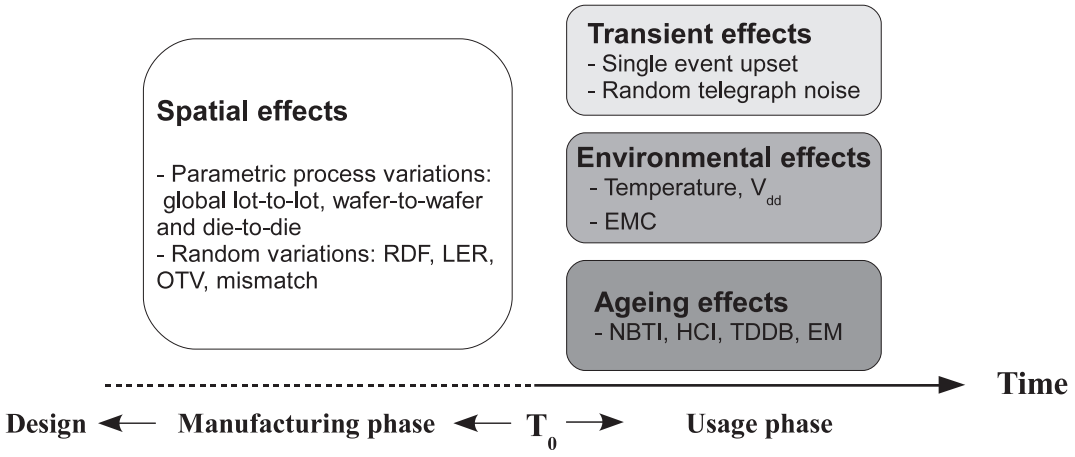


Figure 1: La classification de la fiabilité ICs

- Negative Bias Temperature Instability (NBTI)
- Hot Carrier Injection (HCI)
- Time Dependent Dielectric Breakdown (TDDB)
- Electromigration (EM)

II.b La variabilité des transistors

Les circuits intégrés sont affectés par une grande variété de variations. Ces variations se différencient tout d'abord par leur origine. On peut ainsi distinguer:

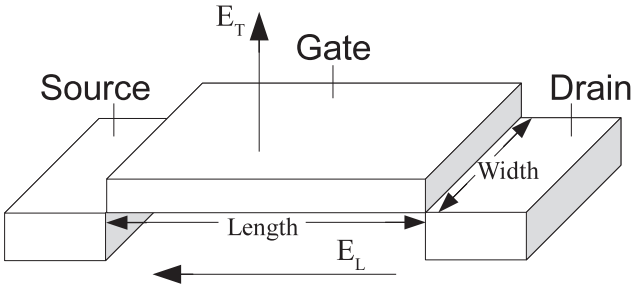


Figure 2: les champs électriques dans le transistor MOS.

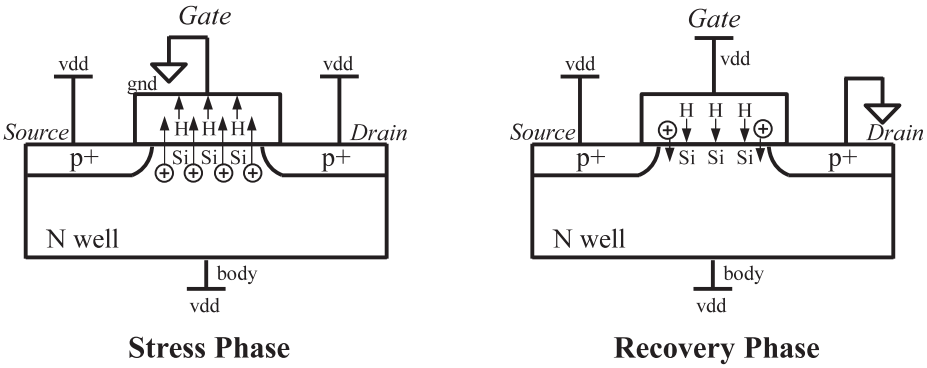
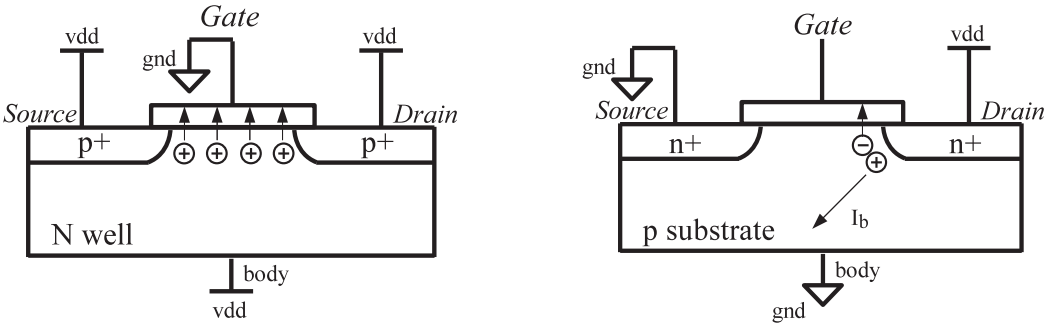


Figure 3: La phase de stresse et de rétablissement du mécanisme NBTI.



(a) NBTI causes positive oxide charge and generation of interface traps.

(b) Hot carriers inject into the dielectric at the transistor drain end.

Figure 4: les mécanismes NBTI et HCI.

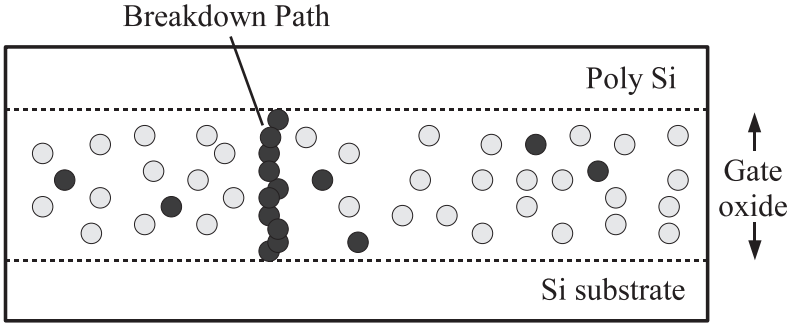


Figure 5: L'approche de percolation.

- les variations paramétriques qui résultent du processus de fabrication et affectent les valeurs nominales des paramètres technologiques comme la longueur du canal, l'épaisseur de l'oxyde de grille, la concentration des dopants ou encore les dimensions des interconnexions.
- les variations des conditions environnementales lors du fonctionnement du circuit comme la température et la tension d'alimentation.
- les variations causées par les phénomènes de vieillissement (HCI, NBTI, TDDB et EM) qui altèrent la fiabilité des composants comme l'injection de porteurs chauds, l'électromigration ou la dègradation.

La Figure 6 illustre l'origine spatiale des variations dans la variabilité totale.

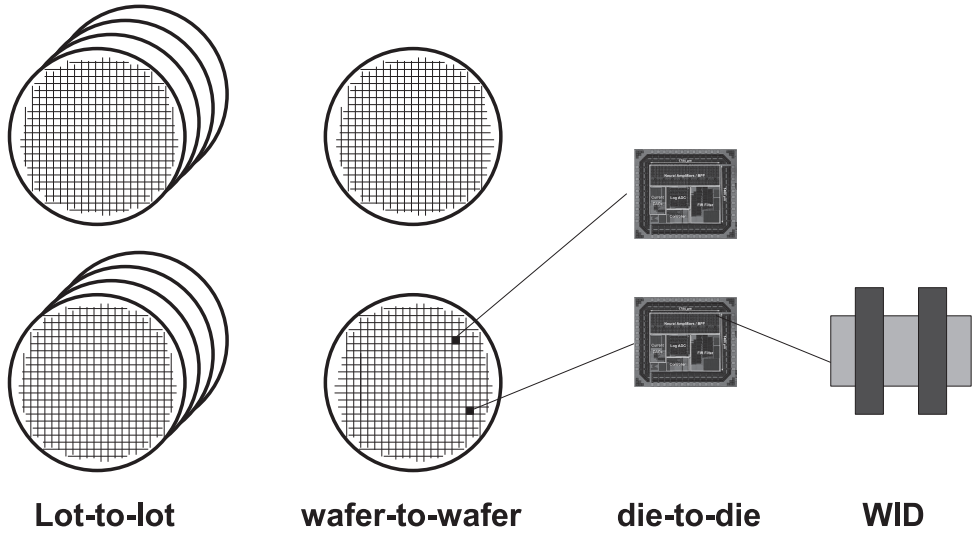


Figure 6: Répartition spatiale des variations paramétriques dans la variabilité totale.

III Les Méthodologies

Ce travail présente les méthodologie de conception basée sur des simulations multi-niveaux (défaut, transistor, circuit et system).

III.a Etat de l'art des méthodes

- Les modèle équivalent pour l'analyse des vieillissement
- Simulateur Eldo

  Le logiciel de simulation électrique Eldo est distribué par la société Mentor Graphics. La Figure 7 illustre une méthode de simulation de fiabilité nominale.

  Eldo fournit les modèles de dégradation de HCI et NBTI. La simulation commence avec la sélection de la modélisation du vieillissement et de la configuration de la durée du vieillissement. Le stress sur chaque transistor et préalablemant determiné par une analyse transitoire représentative du fonctionnement du circuit.La netlist qui contient des informations dégradées est générée. Les performances du circuit peuvent ensuite être évaluées par DC, AC, PSS (état d'équilibre périodique), Monte-Carlo et l'analyse du bruit dans l'environnement analogique. Le simulateur fournit à la fois

les performances du circuit idéal et la netlist dégradé, qui peuvent être visualisées à l'aide du logiciel EZwave.

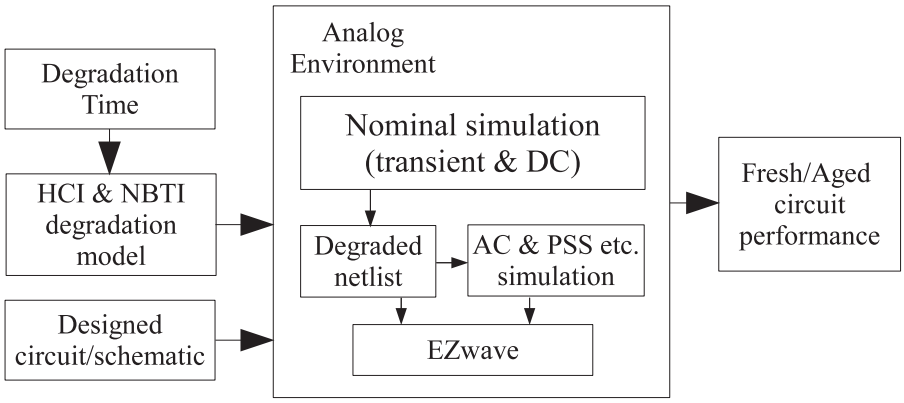


Figure 7: La méthode de simulation de fiabilité nominale

- L'analyse de pire-cas et Monte-Carlo

  Les méthodes d'analyse de la variabilité consistent généralement à évaluer une statistique qui caractérise cette variabilité (valeurs extrêmes, distribution des performances, etc.). Il y a deux méthodes classiques sont l'analyse pire-cas et l'analyse de Monte Carlo (voir Figure 8). L'analyse pire-cas a pour objectif de déterminer les valeurs extrêmes des performances en combinant les valeurs extrêmes des paramètres technologiques. Bien que très rapide, cette méthode est cependant imprécise dans le cas des circuits analogiques, conduisant à une estimation pessimiste des performances et donc un surdimensionnement. A l'opposé, l'analyse de Monte Carlo est d'une grande précision mais nécessite la simulation de milliers d'échantillons afin d'approximer la distribution des performances avec précision. De nouvelles méthodes d'analyse de variabilité, à la fois précises et efficaces en termes de coût calculatoire, sont donc nécessaires.

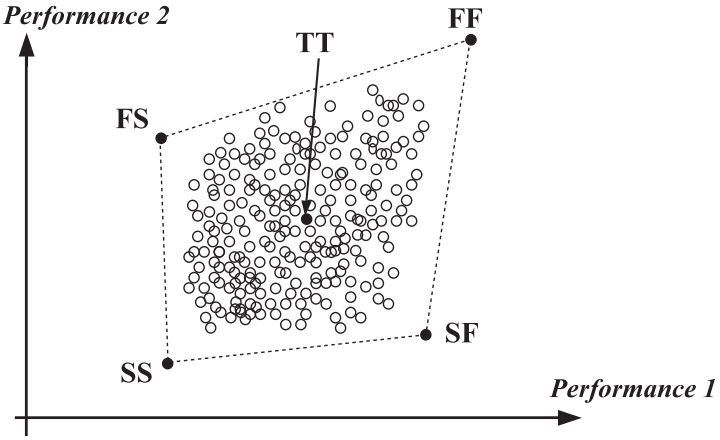


Figure 8: Une comparaison entre l'analyse MC et l'analyse pire-cas

III.b Les statistique de la variabilité

- Plan d'expréiences

  Les plan d'expréiences sont une procédure de collecte d'informations dans l'analyse statistique.

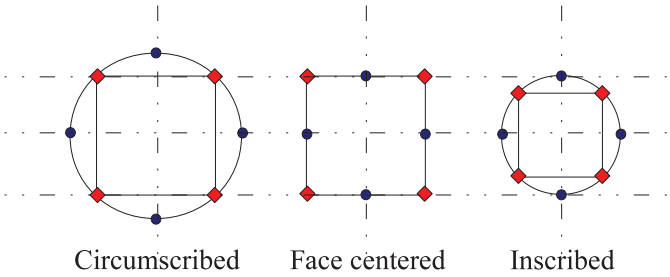


Figure 9: Le plan composite centré avec deux facteurs.

Number of factor	*2*	*3*	*4*	*5*	*6*	*7*
Full factorial	4	8	16	32	64	128
Fractional factorial ($\frac{1}{2}$)	2	4	8	16	32	64
Central composite	9/9	15/15	25/25	25/43	45/77	79/143
Box-Behnken	N/A	13	25	41	49	57

Table 1: Nombre d'essai pour l'analyse DoEs. Le plan CCD est de type full 1/2 fractional.

- Screening

  Le screening peut être employé avec certains plans où les interactions entre facteurs ne sont pas gérées (plans de Plackett-Burman). Les plans de Plackett-Burman sont une application particulière des matrices d'Hadamard.

		x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	x_{11}
1	+	+	+	+	+	+	+	+	+	+	+	+
2	+	-	+	-	+	+	+	-	-	-	+	-
3	+	-	-	+	-	+	+	+	-	-	-	+
4	+	+	-	-	+	-	+	+	+	-	-	-
5	+	-	+	-	-	+	-	+	+	+	-	-
6	+	-	-	+	-	-	+	-	+	+	+	-
7	+	-	-	-	+	-	-	+	-	+	+	+
8	+	+	-	-	-	+	-	-	+	-	+	+
9	+	+	+	-	-	-	+	-	-	+	-	+
10	+	+	+	+	-	-	-	+	-	-	+	-
11	+	-	+	+	+	-	-	-	+	-	-	+
12	+	+	-	+	+	+	-	-	-	+	-	-

Table 2: Le screening avec les plans de Plackett-Burman.

- Méthode des surfaces de réponses

  La méthode des surfaces de réponses a pour but d'explorer les relations entre les variables dépendantes et indépendantes impliquées dans les plan expériences.

  Cette méthode nécessite des essais supplémentaires. La précision du modèle est ensuite testée à partir d'autres critères de validité tel que l'erreur quadratique moyenne

RMSE (Root Mean Square Error en anglais).

$$RMSE = \sqrt{\frac{\sum_{n=1}^{N}(Y_{predicted,n} - Y_{simulated,n})^2}{N}} \tag{1}$$

$$Y_{linear} = \beta_0 + \beta_1 X_1 + \beta_2 X_2 \tag{2}$$

$$Y_{quad} = Y_{linear} + \beta_{12} X_1 X_2 + \beta_{11} X_1^2 + \beta_{22} X_2^2 \tag{3}$$

$$Y_{cubic} = Y_{quad} + \beta_{112} X_1^2 X_2 + \beta_{122} X_1 X_2^2 + \beta_{111} X_1^3 + \beta_{222} X_2^3 \tag{4}$$

III.c L'approche bottom-up

La Figure 10 illustre la procédure de l'analyse hiérarchique de fiabilité dans les modulateurs ΣΔ. La dégradation et les fluctuations induit par les impacts de la fiabilité (par exemple, le mécanisme du vieillissement et les variations du processus) au niveau physique peut atteindre le niveau produit (au travers le niveau de transistor, le niveau de circuits (OTA) et le niveau du système (modulateur ΣΔ)). La performance du système sous influence des variations du processus et du phénomène de vieillissement peut être évaluée de manière efficace. Une étude plus profonde sur les outils et les méthodes de simulation reliant tous les niveaux sera présenté dans la chapitre suivant.

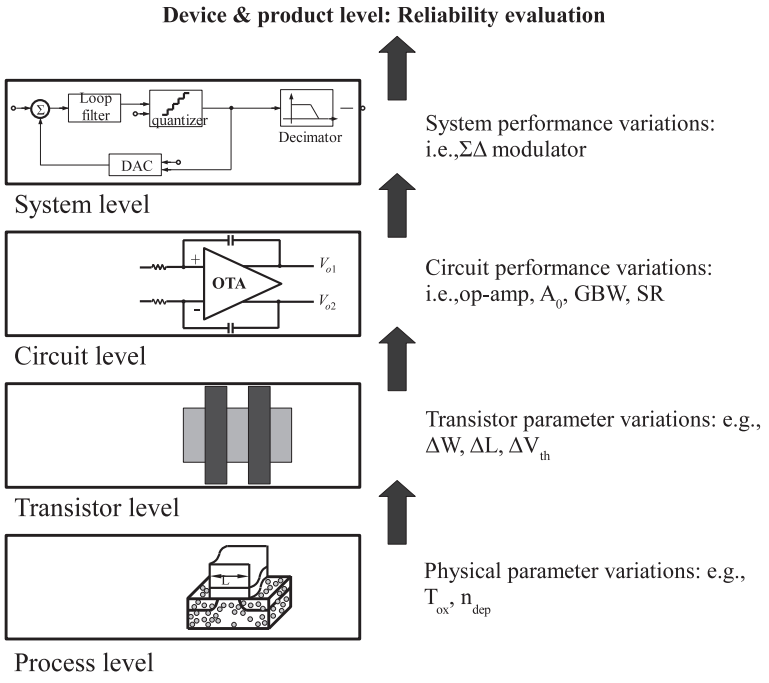


Figure 10: L'approche bottom-up pour Fiabilité

III.d Une frontière de Pareto

L'optimisation multiobjectif est une branche de l'optimisation combinatoire dont la particularité est de chercher à optimiser simultanément plusieurs objectifs d'un même problème.

Il est impossible de définir la valeur optimale d'un problème d'optimisation multiobjectif en toute généralité. Il existe plutôt un ensemble de valeurs optimales, formant une frontière de Pareto.

Selon leurs besoins spécifiques, les concepteurs doivent désigner et optimiser le circuit et les différents paramètres de performance du système. L'optimisation d'un paramètre de performance est souvent au prix des autres. Comparé avec l'optimisation à unique objectif, un ensemble de solutions existe pour l'Optimisation aux Objectifs Multiples (MOO). Les solutions dans ce set sont définies comme Pareto optimal ou non-dominé. Les frontières Pareto des pires cas représentent la pire performance simulée pour une topologie donnée de circuit. L'optimisation de la performance d'un circuit basée sur les frontières Pareto a été évoquée dans de nombreuses publications. Un lot de solutions aux objectifs multiples peut aider les concepteurs dans l'évaluation des paramètres de performance d'un point de vue objectif.

- Avec deux vecteurs x, y donnés, nous définissons que $x \leq y$, si $x_i \leq y_i$ pour $i = 1, \cdots, k$, ainsi x domine y ($x \prec y$).
- Il a été défini qu'un vecteur des variables de décision $x \in \mathcal{X}$ est non-dominé respectivement à $\mathcal{X}$, si aucun x' existe qui remplisse la condition de telle façon que $f(x') \prec f(x)$.
- Il a été defini qu'un vecteur des variables de décision $x^* \in \mathcal{F}$ ($\mathcal{F}$ est la région faisable) est Pareto-optimal si il est non dominé respectivement à $\mathcal{F}$.
- Le set Pareto Optimal $\mathcal{P}^*$ est:

$$\mathcal{P}^* \ = \ \{x \in \mathcal{F} \mid x \ est \ Pareto \ optimal\} \tag{5}$$

- Les frontières Pareto $\mathcal{PF}^*$ est $f(x)|x \in \mathcal{P}^*$.

L'algorithme évolutionnaire aux objectifs multiples basé sur le tri non dominé est utilisé afin de générer les frontières Pareto. La Figure 11 illustre une frontière de Pareto en présence de deux fonctions objectives. Nous définissons les paramètres du processus BSIM4 comme m, la variable de décision $\vec{\mathcal{B}}$ et l'ensumble des performances du circuit aux n objectfs $\vec{\mathcal{P}}$. Le problème d'optimisation aux objectifs multiples est:

$$Minimize \ \vec{\mathcal{P}} = \mathcal{F}(\vec{\mathcal{B}}) = (\mathcal{F}_1(b_1, ..., b_m), ...\mathcal{F}_n(b_1, ..., b_m)) \tag{6}$$

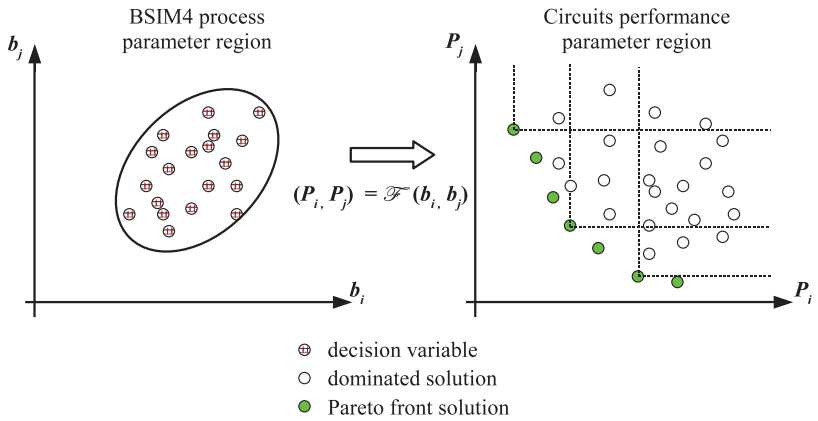


Figure 11: Une frontière Pareto à deux objectifs.

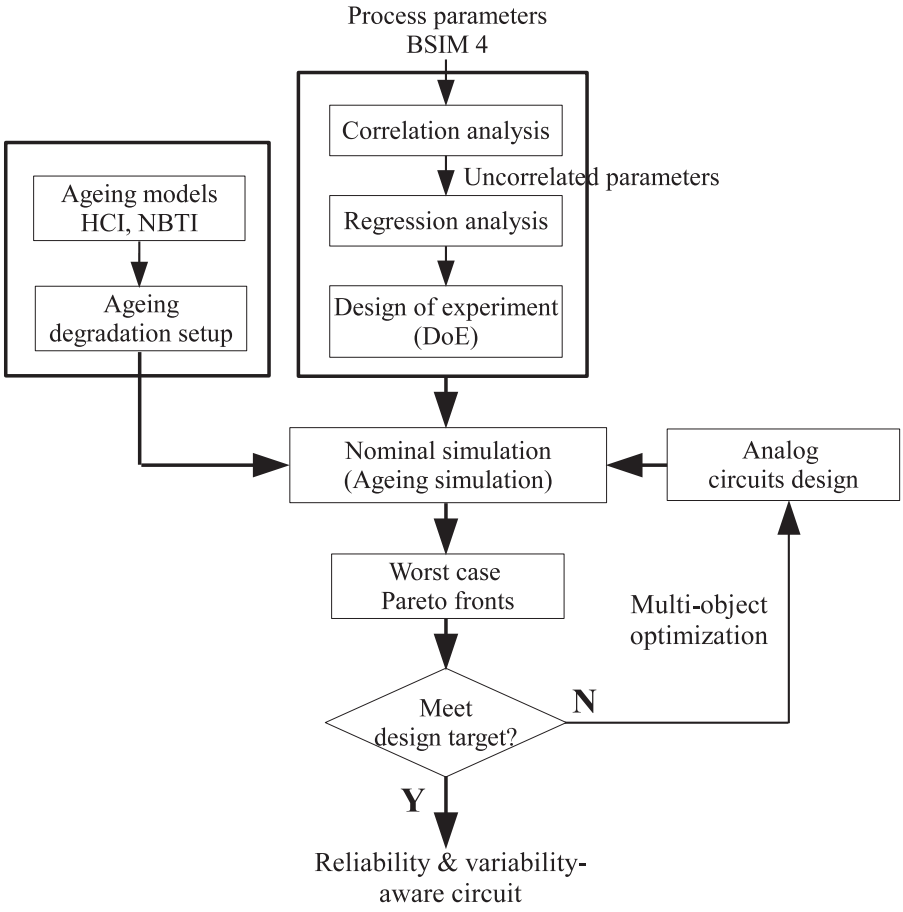


Figure 12: Les flux d'analyse de fiabilité avec l'optimisation Pareto

La Figure 12 illustre l'approche (l'optimisation Pareto) proposée. Cette dernière peut cartographier les paramètres du processus aux paramètres de performances de circuits. Avec l'analyse corrélative et l'analyse régressive, nous filtrons les paramètres BSIM4 non corrélés pour arriver aux paramètres dominants. Cinq paramètres de processus ont été sélectionnés : tension intrinsèque (v_{th0}), mobilité intrinsèque (μ_0), variation du longeur (x_l), épaisseur de la porte d'oxyde (t_{ox}) et la concentration du popage de canaux (n_{dep}). Tout d'abord, les préparations initiales sont nécessaires dans la sélection du modèle de vieillissement et la durée du vieillissement. Durant l'étape de DoEs, un Box-Behnken design de cinq facteurs est généré (pour remplacer la simulation MC). Puis, la simulation des circuits se réalise pour la performance idéale et vieillie du circuit. Afin d'évaluer la performance de dégradation du circuit sous les effets du vieillissement et des variations du processus, les frontières Pareto du pire des cas aux objectifs multiples (compte tenu des paramètres de performances différents) est générée par l'évolution de tri non dominé. De plus, si les paramètres de performance sont inférieurs au cible du design, il faut faire appel à l'optimisation.

La fidélité des frontières Pareto estimées statistiquement peut tre évaluée par l'équation RMSE. Il s'agit d'une mesure des décalages entre les valeurs du modèle statistique ($P_{stat,n}$) et les résultats issu d'une analyse standard MC ($P_{MC,n}$).

IV Fiabilisation en conception pour la technologie CMOS 65 nm

V Fiabilisation de Convertisseurs Analogique-Numérique à Modulation Sigma-Delta

V.a Modulateurs Sigma-Delta

L'architecture générale d'un convertisseur analogique-numérique de type sigma-delta est présentée à la Figure 13. Le modulateur ΣΔ à temps continu a quatre principaux blocs de construction: un filtre analogique, un comparateur dans le chemin direct, qu'un convertisseur numérique-analogique (CNA ou DAC) dans le chemin de retour, ainsi l'unité d'horloge. Le fonctionnement des modulateurs ΣΔ est caractérisé par deux principes fondamentaux: l'échange entre résolution et vitesse et la mise en forme du bruit de quantification.

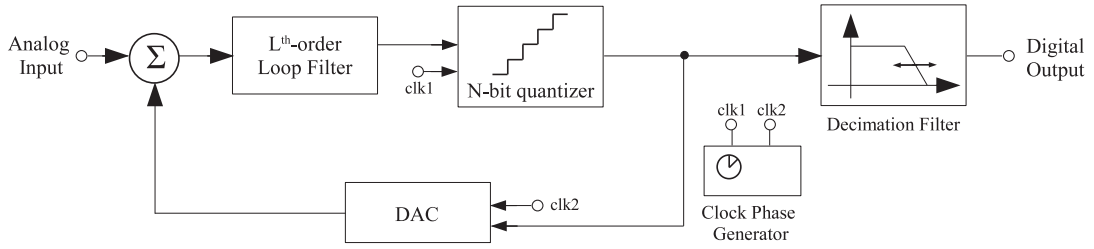


Figure 13: L'architecture générale d'un modulateur ΣΔ

La définition de l'OSR (OverSampling Ratio) pour un modulateur passe-bas s'écrit:

$$OSR = \frac{f_s}{2f_c} \tag{7}$$

f_c est la fréquence maximale du spectre du signal à convertir et f_s est la fréquence d'échantillonnage.

Dans un modulateur sigma-delta, la mise en forme du bruit de quantification dépend du filtre analogique. Par la modélisation du bruit de quantification comme un bruit blanc additionnel, il est possible d'exprimer la sortie du modulateur par la formule:

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{8}$$

et la fonction de transfert du bruit NTF(z):

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{9}$$

où:

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{10}$$

Y(z) est la sortie du modulateur, U(z) est le signal d'entrée, E(z) est le bruit de quantification et STF(z) et NTF(z) les fonctions de transfert vis-à-vis du signal et du bruit.

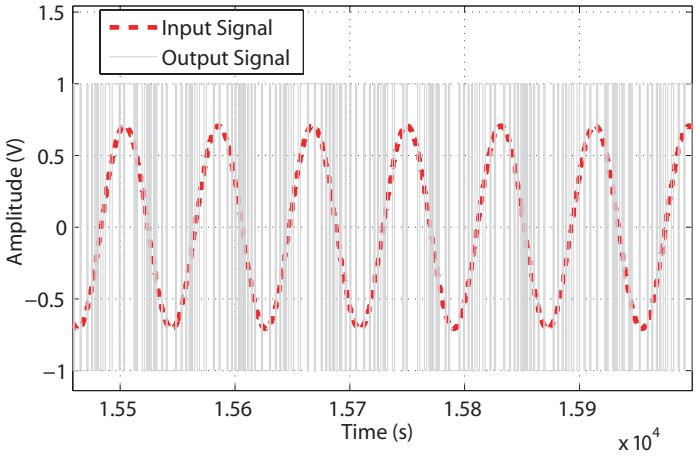


Figure 14: L'entrée et sortie d'un modulateur ΣΔ dan le domaine temporel

V.b Fiabilisation du Modulateurs Sigma-Delta

Les résultats obtenus sont illustrés par le Tableau 3.

Pour les modulateurs sigma-delta, la simulation nécessaire à l'évaluation des performances nominales est très coûteuse en temps. En conséquence, pour des considérations de conception de variabilité, l'application directe de la simulation Monte Carlo n'est pas réaliste du point de vue de temps de calcul. D'autre part, effectuer directement la simulation du vieillissement d'un système complexe au niveau transistor n'est pas aisée avec les outils commerciaux.

Ainsi, l'approche hiérarchique de la fiabilité est une solution efficace dans l'analyse des impacts du vieillissement et des variations de processus du modulateur sigma-delta. La méthode de co-évaluation statistique a été utilisée dans les simulations des impacts du vieillissement et de la variabilité. La méthode ascendante peut propager et remonter la dégradation du vieillissement des transistors et les variations du processus au niveau du système (par l'intermédiaire du niveau circuit). Par ailleurs, l'analyse des pannes est utilisée comme un cas d'études pour les modulateurs sigma-delta. La simulation du vieillissement se réalise en Eldo. L'analyse statistique et la conception assisté par ordinateur sont réalisés sous Matlab.

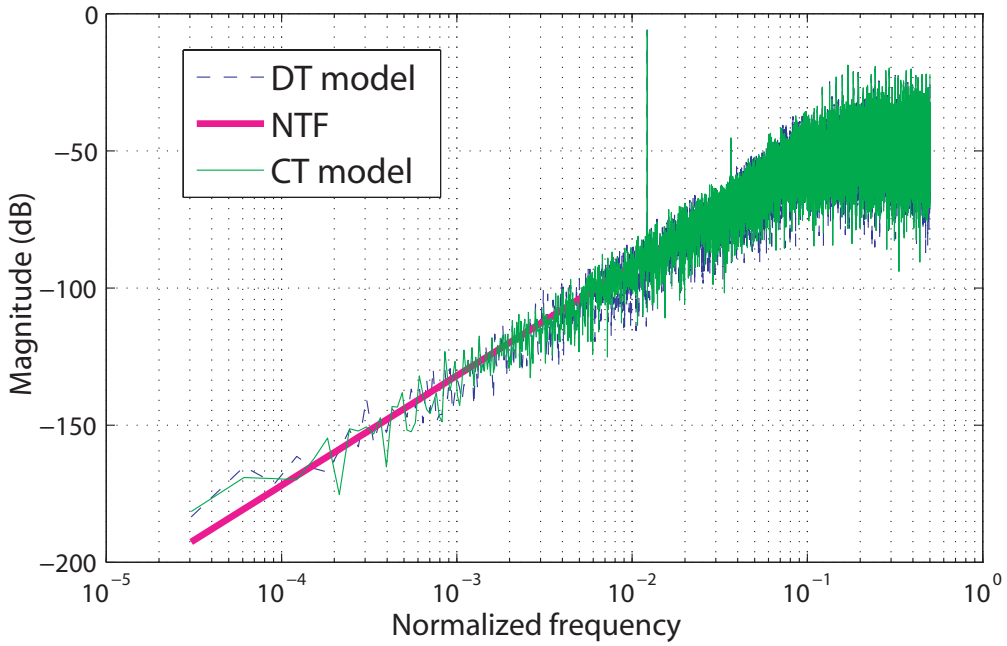


Figure 15: Entrée et sortie d'un modulateur ΣΔ dan le domaine des fréquences

Table 3: Literature review of reliability study in SDM and other types of ADC. N/A for CMOS node is not specified

Ref. (year)	Reliability sort	Applications	CMOS	Main methodology
Singh 2003	Transient faults	flash, SAR and SDM ADCs	N/A	Sensitivity analysis
Yu 2006	Parameter fluctuations	DT SDM	N/A	Statistical LUT
Andrejevic 2006	Fault Diagnosis	Digital part of SD ADC	N/A	Catastrophic defects
Tang 2007	Process variations	CT-SDM	0.18 μm	Hierarchical and statistical methods
Yan 2009	HCI,NBTI,TDDB	Flash ADC	90 nm	Failure in time (FIT) Failure prediction
Ferreira 2011	Process variations, HCI and NBTI	RF front-ends	65 nm	Bottom-up design
More 2011	HCI, NBTI	SAR-ADCs, DT-SDMs	32 nm	Hierarchical methodology
Cai 2012	Process variations, HCI and NBTI	CT-SDM	65 nm	Hierarchical and statistical methods

V.c Modulateur ΣΔ d'ordre 2

Le sujet de la fiabilité est important pour un dispositif médical implantable. L'application est pour détecter le signal de stimulation cardiaque. Un modulateur ΣΔ passe-bas (B = 400 Hz, monobit) du second ordre à temps continu a été conçu au niveau transistor et son analyse comportementale a été réalisée.

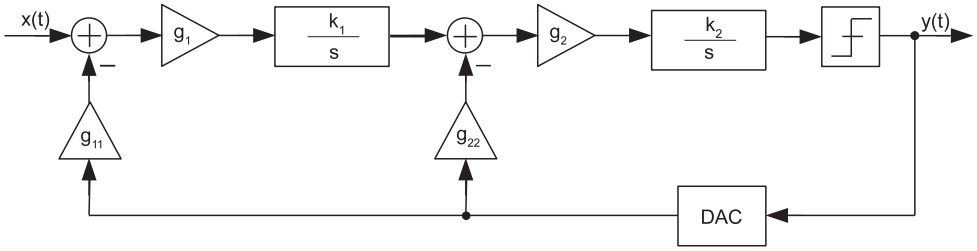


Figure 16: Le modèle du modulateur CT ΣΔ de 2^{eme} ordre.
Le modèle du modulateur CT ΣΔ de 2^{eme} ordre. g_1, g_2, g_{11} et g_{22} ont des coefficients feedforward et feedback.

Table 4: Expected specification

Parameter	Expected
Supply voltage	1.2 V
Clock frequency	32 kHz
OSR	40
SQNR	58 dB
SNR	49 dB
Power	200 nA
ENOB	8 bits

Les résultats obtenus sont illustrés parle Tableau 5.

La condition de panne à chaque bloc est:

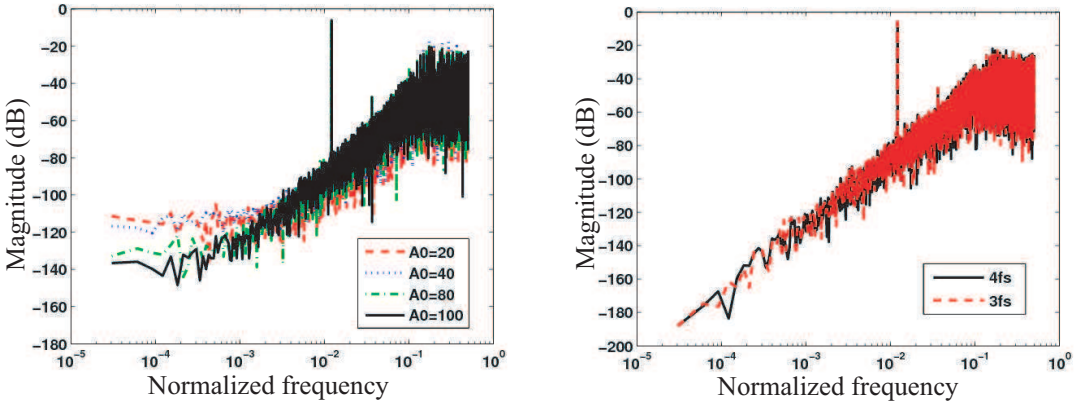
- $A_{dc-loss}$ = 3 dB,
- GBW_{loss} = 32 kHz (1*f_s);
- τ_{d-quan} = 7.812 us (25% T_{clk}),
- τ_{d-DAC} = 9.5 us (30% T_{clk}).

L'analyse de fiabilité est également effectuée au niveau du transistor.

Dans ce travail, une analyse fiabilité au niveau de transistor du modulateur ΣΔ a été effectuée. Nous concluons que pour cette application faible puissance, la boucle de retour est moins fiable que le filtre de boucle analogique. Le DAC est le bloc de construction le plus sensible. D'autre part, le circuit surdimensionné peut améliorer la fiabilité du système avec les compromis de puissance. Pour une fiabilité de la conception de circuits, si over-conception ou reconception est demandé, nous pouvons apporter des améliorations plus tôt dans la phase de conception en prévision du vieillissement. En comparant avec HCI, le NBTI est l'effet dominent pour le modulateur ΣΔ à temps continu.

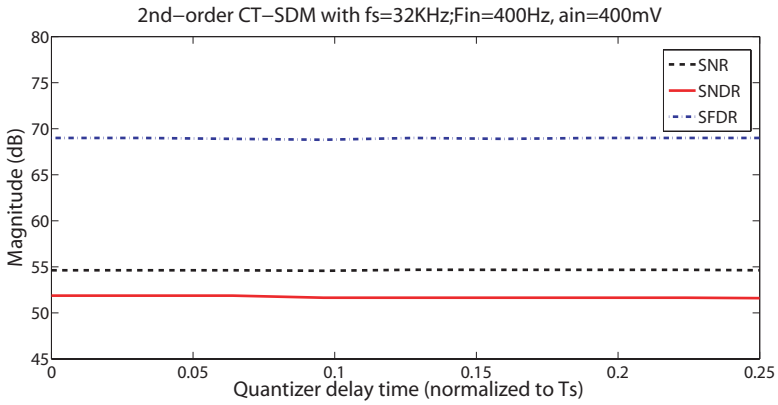
V.d Le bruit de l'horloge d'un modulateur ΣΔ d'ordre 3

Un modulateur ΣΔ à temps continu est étudiée dans le présent paragraphe. Il peut être utilisé en basse frénquence. L'effet du bruit de l'horloge induite par le vieillissement est étudié dans ce modulateur.

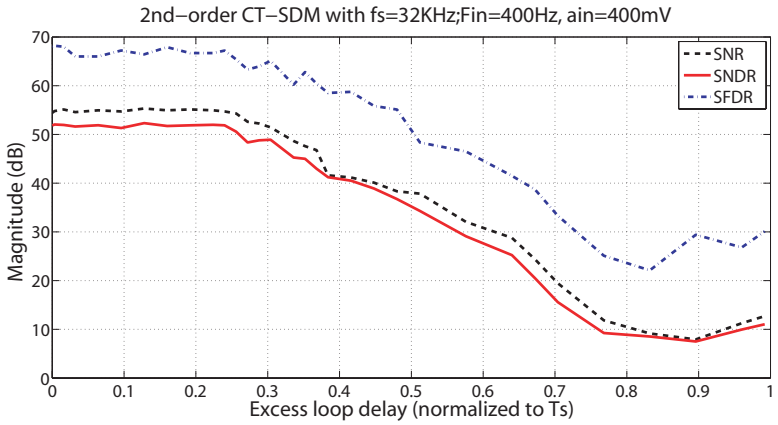


(a) Different DC gain (b) Different GBW

Figure 17: Les outputs spectres avec DC gain et GBW variance. SQNR est 55.0 dB, 55.0 dB, 54.5 dB, 51.3 dB quand (A_{dc}) est 100, 80, 40 et 20; SQNR est 54.9 dB, 54.8 dB quand GBW est 128 kHz et 96 kHz



(a) SQNR versus quantizer delay



(b) SQNR versus quantizer delay

Figure 18: La performance du quantificateur et du DAC

Table 5: Tableau des cas de test de défaillance pour les modulateurs sigma-delta. Oui est le cas en panne.

case	1^{st} int	2^{nd} int	Quan	DAC	$SQNR_1$(dB)	$SQNR_2$(dB)
0	non	non	non	non	54.6	55.1
1	non	non	non	oui	51.5	49.1
2	non	non	oui	non	54.6	55.1
3	non	non	oui	oui	49.6	49.1
4	non	oui	non	non	43.0	55.1
5	non	oui	non	oui	42.1	49.1
6	non	oui	oui	non	43.1	55.1
7	non	oui	oui	oui	42.1	49.1
8	oui	non	non	non	42.8	54.9
9	oui	non	non	oui	42.0	50.0
10	oui	non	oui	non	42.8	54.9
11	oui	non	oui	oui	42.0	50.0
12	oui	oui	non	non	42.4	54.9
13	oui	oui	non	oui	42.1	49.2
14	oui	oui	oui	non	42.4	54.9
15	oui	oui	oui	oui	42.0	49.2

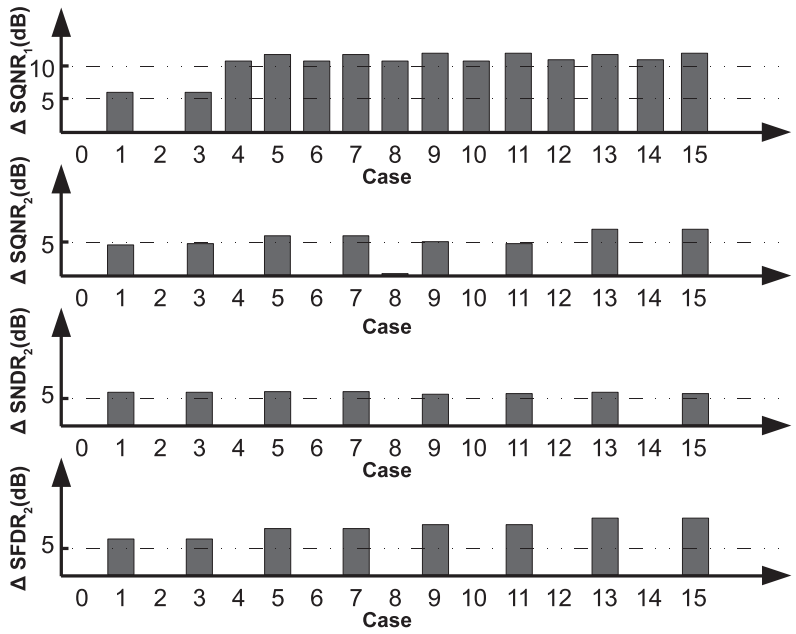


Figure 19: La dégradation de la performance versus le cas faillant du blocque par la barre graphique, $SQNR_1$ (cas minimum du design) et $SQNR_2$, $SNDR_2$, $SFDR_2$ (cas de sur-design). $\Delta = X_0$ - X_i est la paramètre de la performance, $'i'$ est l'index des cas.

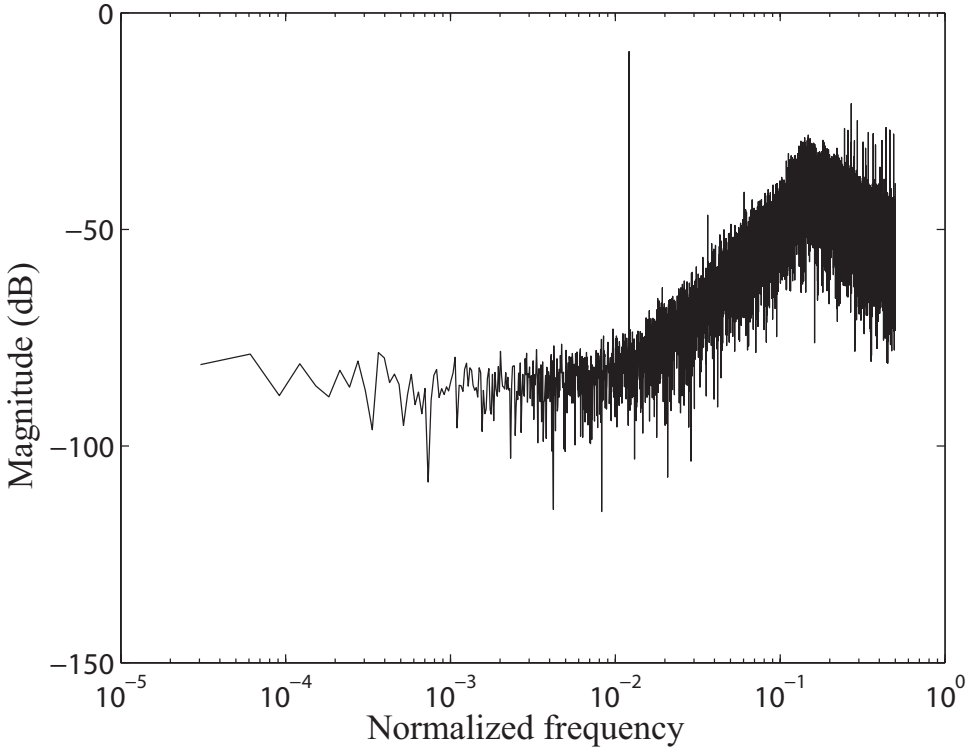


Figure 20: Le spectre réalisé d'un modulateur désigné

Table 6: Le vieillissement de simulation dans l'op-amp

Condition	A_{dc} (dB)	GBW (kHz)	SQNR (dB)
Fresh 27°C	33.5	100	54.5
Fresh 150°C	29.3	72	42.4
Ageing 27°C	33.5	100	54.5
Ageing 150°C	29.3	72	42.4

Table 7: Le vieillissement de simulation dans la feedback loop

Block	Comparator	DAC	Phase Gen.
τ_d (s)	22.5 p	13.1 p	1 n

Table 8: Performance attendue de 3 bits 3^{eme} ordre modulateur $\Sigma\Delta$ à temps continu.

Parameter	Expected
Supply voltage V_{dd}	1 V
OSR	16
Input frequency f_{in}	125 kHz
Clock frequency f_{clk}	4 MHz
Ideal SQNR	82.5 dB
Reference Voltage V_{ref}	0.425 V

Les mécanismes de vieillissement HCI et NBTI sont étudiés avec la méthode d'analyse de la fiabilité hiérarchique ascendante proposée.

Le modulateur CT est moins robuste contre le bruit de l'horloge et le retard du circuit comparé à leur homologue en temps discret (DT). Le distributeur de l'horloge est une section essentielle du modulateur sigma-delta. Tous les composants qui ont une horloge (par exemple, le quantificateur et le DAC) sont sensibles à l'incertitude de l'horloge. Basé sur un 3 bit 3^{eme} ordre CT modulateur idéalement designé, les mécanismes du vieillissement HCI et NBTI sont étudié avec l'approche de l'analyse ascendante de fiabilité hiérarchique proposée. Afin d'isoler dans la mesure du possible les impacts de l'incertitude de l'horloge, toute les autres sections du modulateur sont idéal (implantées avec Verilog-AMS et macro-modèles).

Un distributeur de l'horloge sans chevauchement conçu avec la technologie CMOS 65 nm a été évoqué. L'HCI et le NBTI peuvent induire tous les deux l'incertitude de l'horloge. D'un aspect quantitatif, l'HCI induit un décalage 100 fois moins important que le NBTI. Ainsi, le mécanisme NBTI est concerné en premier. Le NBTI peut induire les décalages et du bruit de l'horloge. Plus précisément, le distributeur de l'horloge avec le V_{th} stantard et le V_{th} bas montre des incertitudes exprimées par des décalages périodiques de l'horloge sous le NBTI. Nous constatons par ailleurs que le distributeur de l'horloge conçu avec un V_{th} haut souffre moins des problèmes de bruit.

Les signaux de l'horloge comportementale sont non-idéaux selon les bruits (transistor à V_{th} haut) et les décalages (transistor à V_{th} standard ou à V_{th} bas) induits précédemment par le NBTI. Afin d'analyser la dégradation du modulateur induit par le NBTI, la dégradation NBTI est popagée vers le haut niveau: du niveau défaut (mécanisme NBTI), via le niveau transistor (dégradation V_{th}), au travers le niveau du circuit (les décalages de l'horloge induits par NBTI) et enfin collecté au niveau du système. Comme montré dans la Figure 24, la performance du modulateur CT sigma-delta peut tre impactée de manière significative par les bruits induits au distributeur de l'horloge par le NBTI. A partir d'une simulation hiérarchique, on montre qu'un décalage de l'horloge de 20 ps dans un circuit de l'horloge à 4 MHz peut réduire le SNR de 82,5 dB à seulement 32,4 dB.

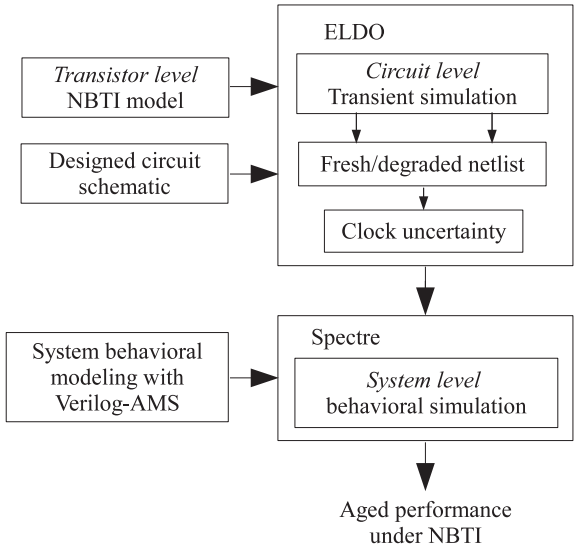


Figure 21: L'approche de la fiabilité hiérarchique.

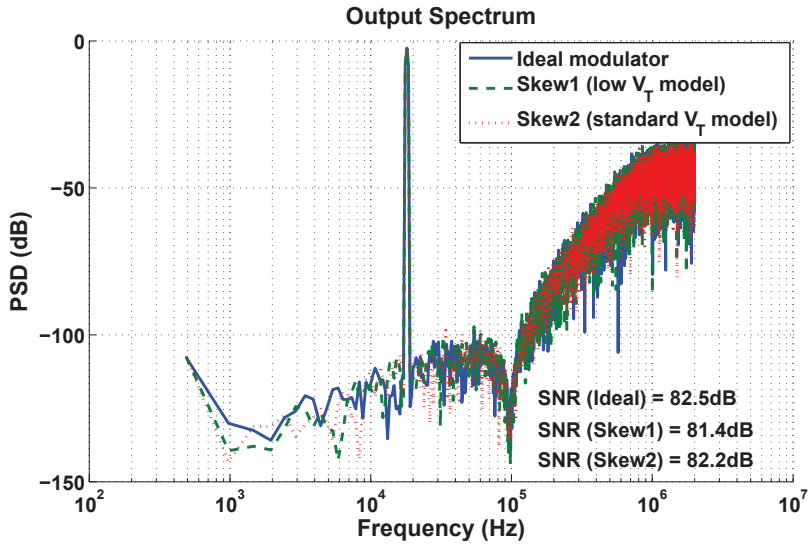


Figure 22: Les dégradation des circuits de l'horloge induits par NBTI.

VI Conclusions

Ce travail de thèse a porté sur des problèmes de fiabilité de circuits intégrés en technologie CMOS 65 nm, en particulier sur la conception en vue de la fiabilité, la simulation et l'amélioration de la fiabilité. Les mécanismes dominants de vieillissement HCI et NBTI ainsi que la variabilité du procédé de fabrication ont été étudiés et évalués quantitativement au niveau du circuit et au niveau du système. Ces méthodes ont été appliquées aux modulateurs Sigma-Delta afin de déterminer la fiabilité de ce type usuel de composant.

Les points dominants tout au long de cette thèse sont: la modélisation des défauts, les méthodes d'analyse de la fiabilité, la conception en vue de la fiabilité. Une grande partie de ce travail a porté sur les méthodes de fiabilité assistée par ordinateur. Le développement de méthodologies efficaces, indépendantes de la technologie, peut aider le concepteur de circuit pour accéder à des simulations de fiabilité efficaces. Les problèmes de dégradation de fiabilité et de variabilité existent pour les circuit CMOS 65 nm. Le degré est très dépendant de la conception du circuits, par exemple, de l'architecture, de la polarisation des transistor, de leurs dimensions. Au niveau du circuit, une conception soignée (par exemple, avec une marge de fiabilité) et une simulation précise de la fiabilité (par exemple, avec Eldo) peuvent contrôler efficacement la dégradation de la fiabilité.

Au niveau du système, la méthode de fiabilité hiérarchique est adapté aux systèmes AMS complexes. Les phénomènes physiques de dégradation peuvent tre remontés au niveau du système, via le transistor et le niveau circuit. En faible puissance et pour un modulateur sigma-delta temps continu, la boucle de retour s'avère moins fiable que filtre de boucle analogique. Le convertisseur numérique-analogique est le bloc de construction le plus sensible. D'autre part, un sur-dimensionnement peut améliorer la fiabilité du système avec un compromis de puissance consommée. Pour les modulateurs sigma-delta temps continu, les problèmes de fiabilité liée à la gigue d'horloge peuvent influer sur la quantification et le convertisseur numérique-analogique. Les modulateurs temps continu sont très sensibles à ces incertitudes d'horloge, en particulier avec des signaux de type RZ. Ces problèmes de fiabilité peuvent aussi causer un retard dans la boucle de rétroaction et doivent être traités avec une grande attention.

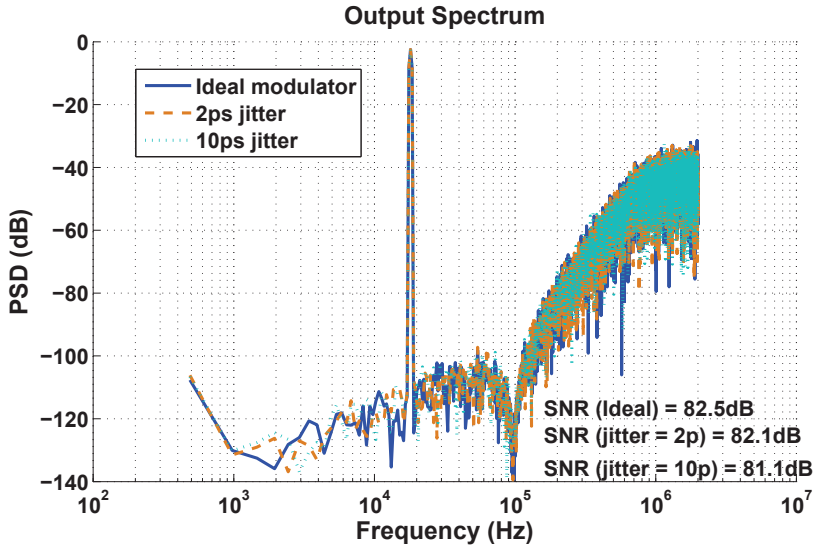


Figure 23: Le output spectrum: 2 ps et 10 ps jitter peux dégrader 0.4 dB et 1.4 dB de SNR, séparament.

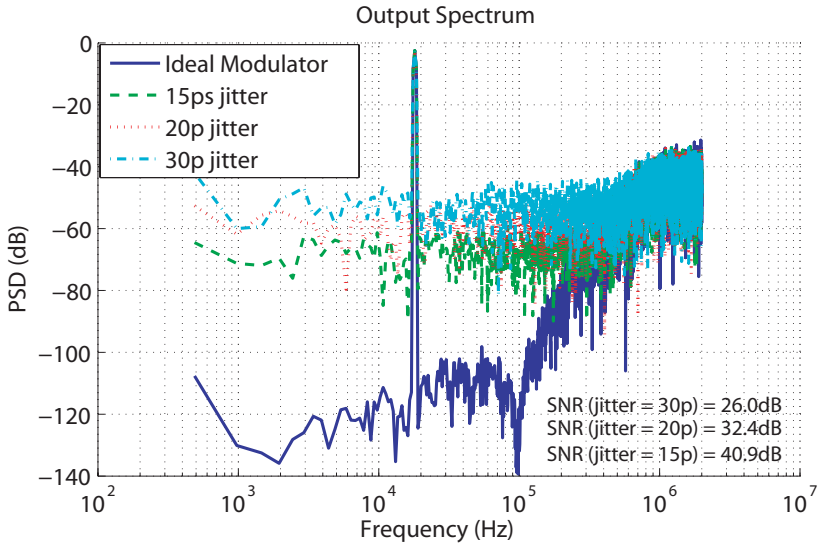


Figure 24: Le output spectrum: 20 ps jitter fait référence au niveau de jitter simulé du distributeur de l'horloge, qui peut conduire á 50,1 dB de perte SNR. Dans ce modulateur avec la stratégie de NRZ feedback, 11 ps de jitter est le seuil de la dégradation.

Chapter 1

Introduction

1.1 Motivations

With the development of Complementary Metal-oxide-semiconductor (CMOS) technology in system on chips (SoCs), electrical circuits and systems can be integrated into a single chip. As a direct result of scaling down of device geometries, reliability becomes a significant bottleneck. Novel SoCs with new materials and architectures of high complexity further aggravate reliability problems. Integrated circuits (ICs) and systems applied to aerospace, avionic, vehicle transport and biomedicine are highly sensitive to reliability problems such as ageing mechanisms and parametric process variations.

According to technique literatures from IEEE association and International Technology Roadmap for Semiconductors (ITRS), ICs reliability is defined as the ability of an integrated circuit or system to conform to its specifications over a specified period of time under stated conditions. ITRS 2011 reports [1] treat reliability as a critical aspect of process integration. Thus, it is required to apply innovative reliability-aware methodologies to fulfill both SoCs functionality and reliability levels in nanometer CMOS technologies. This allows us to develop reliability-aware methodologies which are independent to designs and CMOS technology, whereas are specific to reliability effects.

Design-for-reliability (DFR) [2] aims to consider reliability problems during the design phase of ICs. Coping with reliability issues has significant importance in terms of both cost reduction and product time-to-market. In order to achieve design specification at required reliability levels, it is necessary to carry out research work on defects modeling, reliability methodology development, reliability analysis/simulation, failure prediction and reliability optimization/enhancement. These reliability-aware frameworks during SoCs design phase can provide useful information to ICs designers, which help them to avoid pessimistic design and reserve appropriate design space to failure boundary.

Continuously scaling down of CMOS technology has resulted in smaller and faster analog-mixed-signal (AMS) circuits and systems but with degraded performance. For instance, Sigma-Delta ($\Sigma\Delta$) analog-to-digital converters (ADCs) have been widely applied to electronic systems. This type of ADC achieves attractive topologies for digitizing with high-resolution analog signals characterized by speed to resolution exchange and noise shaping [3]. In particular to $\Sigma\Delta$ modulators with continuous-time (CT) loop-filters, they gained great popularity in battery powered applications due to speed and power advantages over their discrete-time (DT) counterparts, enabling a higher clock rate and lower power consumption. Considering ICs reliability, $\Sigma\Delta$ modulators used in medical cardiac pacemakers sensing channel [4] and RF receivers in avionic [5], which are highly sensitive to the environment and require thus an extraordinary reliability of the system.

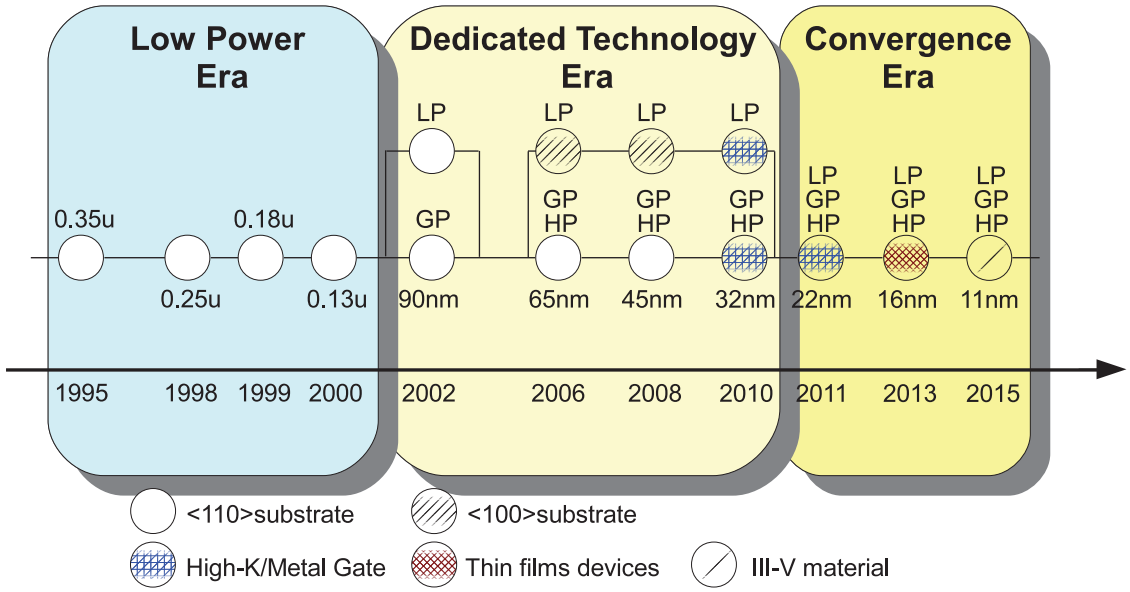


Figure 1.1: The scaling down of CMOS technology nodes in the recent years. Low-power (LP), general purpose (GP) and high-performance (HP) transistors can be realized in different CMOS technology nodes.

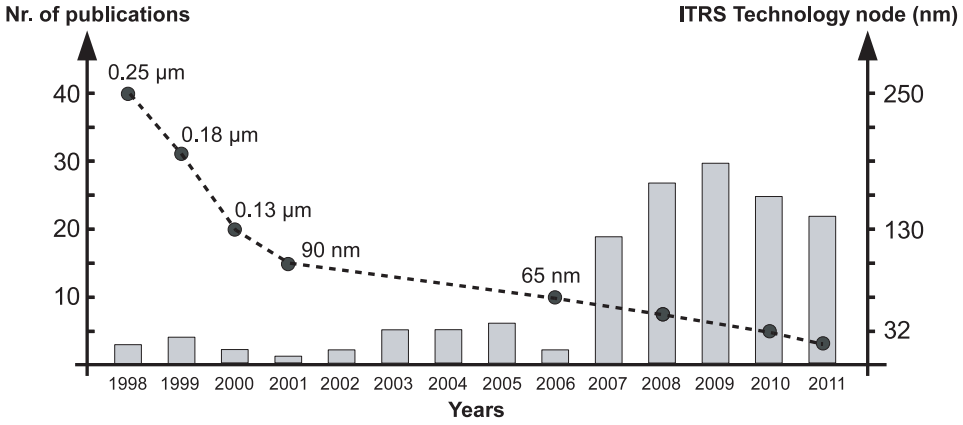
1.2 Current Research on CMOS Reliability

From the beginning of the 1970s, the down-scaling was important and effective way to achieve the low power consumption and high performance CMOS operation [6]. Figure 1.1 shows the different CMOS nodes in low power, dedicated technology and convergence era. Smaller device brings on new design constraints. Advanced CMOS nodes combined with new material under extreme work condition lead to degradations such as ageing mechanisms and process variations. ICs have reliability risks from initial infant mortality to random failure under normal usage, till ICs wear-out. The *bathtub* curve is widely accepted in reliability study and efficiently used in electronic equipments and systems [7] [8]. It describes the relative failure rate of an entire population of products over time.

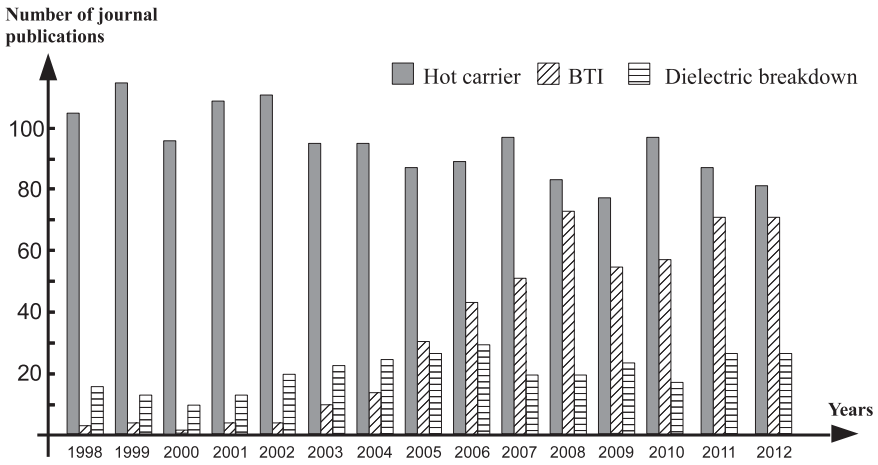
Research work on reliability mainly concentrates on defects modeling, reliability-aware methodology, reliability analysis and failure prediction. Defects modeling characterizes physical defects and maps the degradation to parameters at transistor level (e.g., BSIM4 model). Reliability problems such as transient faults, spatial effects and ageing mechanisms are studied separately. On the other hand, many reliability-aware methodologies and approaches have been developed since the 1990s. With relevant reliability models, it is necessary to perform reliability analysis and complete time-to-failure prediction at the circuit and system levels.

Figure 1.2(a) and 1.2(b) show the approximate IEEE journal publications from IEEE digital database in recent years, which focus on two fields: statistical CMOS variability and ageing degradation mechanisms (including hot carrier injection, bias temperature instability and dielectric breakdown). These works have provided theoretical study and experience to academic research and industry design. Extensive research is vastly important due to the continuous development of CMOS technology.

This thesis work concentrates on the following subjects: reliability-aware methodology development, reliability analysis based on simulation as well as failure prediction of CMOS 65 nm AMS integrated circuits and systems. Sigma-Delta ($\Sigma\Delta$) modulators are concerned as the object of reliability studies at system level. Two dominant ageing mechanisms hot carrier injection (HCI) and negative bias temperature instability (NBTI), as



(a) Approximate IEEE publications in the field of statistical CMOS variability, ITRS technology node 45 nm (2008), 32 nm (2010), 22 nm (2011).



(b) Approximate IEEE publications in the field of ageing effects: HCI, BTI and dielectric breakdown. There is an increasing trend of research on BTI and dielectric breakdown.

Figure 1.2: Approximation IEEE journal publications of process variations and ageing effects, based on IEEE *Xplore* database [9].

well as parametric process variations are mainly studied. The proposed reliability-aware methodologies can direct designer's progress during the IC design phase, towards producing CMOS circuits and system with reliable performance.

1.3 Thesis Organization

The thesis is organized as follows:

Chapter 2 presents a conceptual view of sorted reliability problems in CMOS SiO_2 Poly-Silicon technology, which includes transient faults, ageing mechanisms (HCI, NBTI, TDDB and EM). It reviews the sort of parametric process variations. It also introduces the yield in the manufacturing phase of semiconductor. Reliability in high-k metal gate (HKMG) technology is mentioned.

Chapter 3 reviews traditional reliability-aware methodologies and simulation flows. The state of arts reliability-aware methodology and simulation flows are studied. Considering ageing effects and process variations, efficient reliability-aware approaches for analog

and mixed circuits and systems are proposed, which include hierarchical reliability-aware approach, statistical modeling of process variations, multi-objective evaluation based on Pareto fronts and co-evaluation analysis flow.

Chapter 4 studies the ageing effects and process variations of 65 nm CMOS technology at transistor and circuit levels. The proposed methodologies in Chapter 3 are experimentally applied to 65 nm integrated circuits. Typical integrated circuits are designed and simulated under ageing effects and process variations. NBTI induced clock jitter is reported in a 65 nm clock distributor circuit. A classic 65 nm op-amp is studied with multi-objective aged Pareto fronts.

Chapter 5 gives an overview of the operation of $\Sigma\Delta$ modulators. It presents the design procedure, behavioral level design and low level circuit design. A 400 Hz 1 bit 2^{nd} order CT $\Sigma\Delta$ modulator applied to cardiac pacemaker is designed and simulated. Reliability analysis is performed at each level. A 125 kHZ 3 bits 3^{rd} order CT $\Sigma\Delta$ modulator is designed to analyze clock uncertainties in clock phase generator. A summary of reliability issues of $\Sigma\Delta$ modulators is presented. Mitigation of reliability degradation in $\Sigma\Delta$ modulator is discussed with reliability managements.

Chapter 6 shows conclusions of this work and presents perspectives and future research directions.

1.4 Contributions

The main contributions of this thesis are as follow:

- The reliability-aware methodology for CMOS integrated circuits and hierarchical reliability-aware approach for large and complex AMS systems [10] [11].
- Computer-aided reliability-aware statistical simulation flow including both ageing effects and variability during design phase [11] [12] [13].
- The influence of ageing effects and process variations on 65 nm CMOS integrated circuits and systems [14] [15].
- Systematic reliability analysis on low order CT $\Sigma\Delta$ modulators applied to medical cardiac pacemaker [10] [16].
- Reliability consideration in designing CT $\Sigma\Delta$ modulators [10].
- Reliability management at the abstraction level of AMS circuits and systems.
- Noise-tolerant model based on Markov Random Fields (MRF) [17].

Chapter 2

Reliability: Characterization and Modeling

Reliability is an important factor in design and operation of engineering systems. The discipline of reliability had its roots in the space and military applications, and spread to many other applications [18]. In microelectronics applications, reliability becomes a critical challenge of ICs in deep sub-micron region [1]. Gielen et al. defines reliability as the ability of a circuit to conform to its specifications over a specified period of time under specified conditions [19]. The reliability issue of integrated circuits mainly contains spatial effect, environmental effect, transient effect and ageing effect.

The spatial effect comes from silicon manufacturing process variations that result in performance fluctuations of ICs. When ICs operate below the minimum requirements, yield loss occurs before ICs usage. The second reliability problem is environmental effect (also named dynamic variations). It includes supply voltage (V_{dd}) variations, temperature fluctuations, workload dependent and electro magnetic compatibility (EMC) [20]. These effects are highly dependent on the working environment of ICs. Short-term and long-term workload dependent runtime variations exist in ICs operation time. Therefore, dynamically adapting a circuit to the behaviors of its workloads is necessary. Another important topic EMC has become a major cause of IC redesign, mainly due to inadequate design methods and lack of expertise in parasitic noise reduction and immunity improvement [21]. The third unreliable behavior is transient effect, such as radiations, cross-talk, or ground bounce among others. Last but not least, ageing effect has been intensively studied due to transistor scaling down in the last few decades.

As shown in Figure 2.1, only spatial effect occurs at IC manufacturing phase and affects the parametric yield of ICs. The other three effects occur during ICs usage time. In general, all of these reliability effects can significantly degrade ICs performance. In this chapter, we focus on reliability issues in 65 nm CMOS technology, which is with SiO_2 Poly-Silicon technology. Spatial effects and ageing effects will be discussed in detail.

2.1 Transient Faults

Transient effect (also known as transient fault) is caused by errors in the circuit output [22]. It mainly includes some radiation effects (e.g., single event transient (SET), single event upsets (SEU)), signal integrity issues and random telegraph noise (RTN). [23] refers to the relationship between transient faults at physical level and circuit failure at circuit/system level. Also, [1] reports that RTN as a new severe reliability issue. RTN induced V_{th} fluctuation are studied in [24], [25].

[26] reported that transient faults due to alpha-particles (α-particles, each contains two protons and two neutrons bound together into a particle) can be modeled as a current source which injects a current I_{inj} to hit the fault node of circuits. Figure 2.2 illustrates

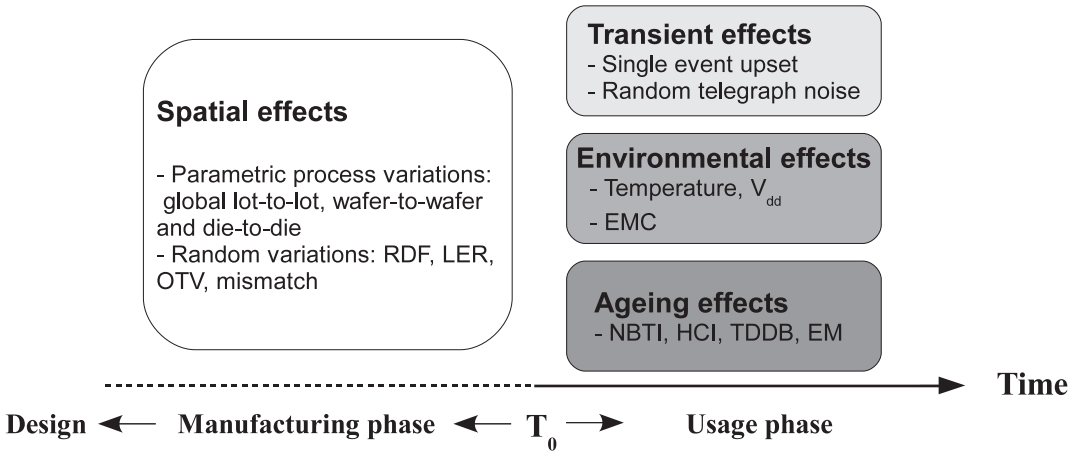


Figure 2.1: The classification of IC reliability

these transient faults in a NMOS transistor. The injection current I_{inj} at fault node is:

$$I_{inj}(t) = I_0 \cdot (e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}) \tag{2.1}$$

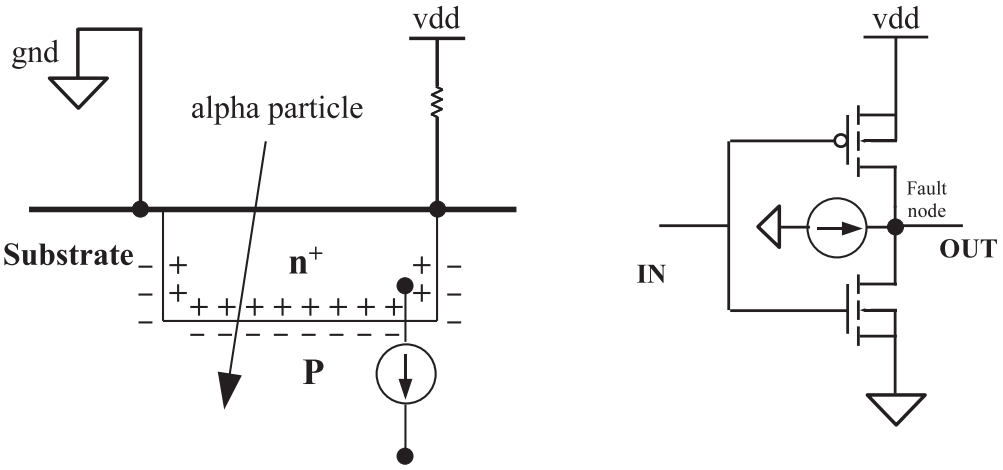


Figure 2.2: Transient fault due to alpha-particles in NMOS transistor, illustrated with physical model and current source equivalent model [26].

where I_0 is the maximum current, τ_1 is the collection time constant for a junction, and τ_2 is the ion track establishment time constant.

[22] proposes a fault estimation model to design fault-tolerant very large scale integration (VLSI) circuits. The probability of failure per year POF_Y can be calculated as:

$$POF_Y \;=\; POF_C \cdot area\ of\ circuit \cdot 100\ 000 \tag{2.2}$$

where POF_C is conditional probability of error. A detailed computational process is shown in [22], [27]. The mean time to failure (MTTF) is given by:

$$MTTF \;=\; \frac{1}{POF_Y} \tag{2.3}$$

2.2 Spatial Effects - Variability

Variability in CMOS technology is the deviation between realized parameters and expected parameters. There are several definitions of variability classification.

- According to the root causes, the variations can be divided into two main categories: systematic and random variations. Repeatable electrical characteristics variations between two identical designed transistors are systematic variations. For random variations, it can be further classified into inter-die variations (also defined as global variation between lot-to-lot, wafer-to-wafer and die-to-die) and intra-die (within-die or local) variations.

- [20] sorts physical variations and environmental variations as the two principle sources. Physical variations exist during SoCs manufacturing phase, which can be further decomposed into: lot-to-lot, wafer-to-wafer, die-to-die and intra-die (within die, WID) variations. Environmental variations include the fluctuations in supply voltage, environment temperature and switching activity, which arise during the usage of ICs.

- [28], [29] classify variability problems (except systematic within-die variations) as spatial reliability effects. Ageing effects are treated as temporal deterministic unreliability effects (NBTI and HCI) and temporal stochastic unreliability effects (i.e. soft breakdown).

All the variability problems depend on design implementation. Table 2.1 summarizes and sorts different variability problems [20], [30].

Table 2.1: Variability in 90nm node: Classifications.

Parameter variability	variation classification	Example
V_{th}	inter-die systematic, intra-die random	random dopant fluctuations
$\mu_{\Delta V_{th}}$ (mean)	inter-die systematic	die-to-die
width, length	inter and intra-die systematic/random	line edge roughness
temperature, V_{dd}	intra-die systematic	environment
passive R, C, L	inter-die systematic	wafer-to-wafer

2.2.1 Random Variations

Random variations are independent of the systematic effects. Typical random variations include poly-silicon granularity, random dopant fluctuations, line edge roughness, oxide thickness variation and intra-die variations.

- Poly-silicon Granularity (PSG)

  The granularity of the poly-silicon gate is a critical source of statistical variability due to enhanced diffusion and surface potential pinning along the grain boundaries. It can induce doping non uniformity within the poly-Si gate, so that dopants from the high-doping regions in the gate can penetrate through the gate oxide into the channel [31].

- Random Dopant Fluctuations (RDF)

RDF is the biggest contributor to the magnitude of mismatch in 45nm and 65nm transistors [32]. Figure 2.3 shows the random fluctuation of the relatively small number of dopants and their discrete microscopic arrangement in the channel of sub 100 nm CMOS technology. RDF leads to significant variations in the threshold voltage [33]. Transistors can have mutually independent V_{th} variation with respect to each other, regardless of their spatial location.

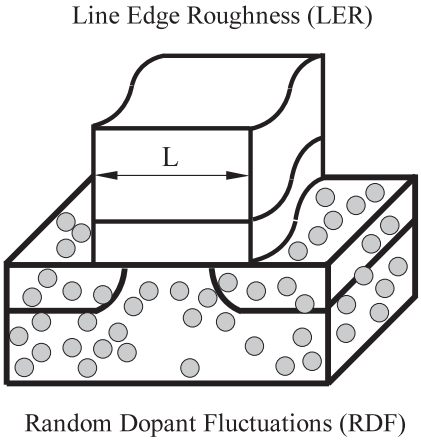


Figure 2.3: A general view of line edge roughness and random dopant fluctuations

- Line Edge Roughness (LER)

  As shown in Figure 2.3, due to the photolithographic and etching steps in submicron technology, LER constitutes a large fraction of the gate length and introduces significant intrinsic variations in the device parameters [34]. LER is induced by both sub-wavelength lithography and the etching process [35]. Both RDF and LER change the output current of a transistor by modifying the threshold voltage. Furthermore, RDF and LER can interact with each other, resulting in a significant increase in leakage current and leading to additional V_{th} variation.

- Oxide Thickness Variation (OTV)

  Random oxide thickness variations exist at Si-SiO_2 interface of MOSFETs. This variation induced threshold voltage variations are similar to fluctuations caused by RDF and become important, since the gate length of the devices becomes comparable to the correlation length of fluctuations at the Si-SiO_2 interface [36].

- Intra-die variations (within-die variations, WID)

  The intra-die variation (or within-die random variation or local variation - mismatch) is the parameter spatial deviation within a single die. Such WID variation may have several sources depending on the physics of the manufacturing steps [20]. Wafer-level variations and layout dependencies are key intra-die variations. Intra-die variations is also assigned to parametric process variations in Chapter 2.2.2.

  The statistical modeling of intra-die variations has been studied on mismatch variance modeling. A widely accepted model for random variations in V_{th} has been proposed by [37]:

$$\sigma^2(\Delta V_{th}) = \frac{A^2_{\Delta V_{th}}}{W \cdot L} + S^2_{\Delta V_{th}} D^2 \tag{2.4}$$

where $A_{\Delta V_{th}}$ and $S_{\Delta V_{th}}$ are constant determined by process technology, W and L are width and length of transistor, D is the spacing between two transistors.

Channel length variability results from LER phenomenon. The threshold voltage of a nanoscale transistor is severely affected by random dopant fluctuations and line-edge roughness. These random intrinsic variations can combine with each others (e.g., the combination of RDF, LER and PSG) which make every transistor microscopically different from its counterparts and introduces differences in the characteristics of topologically identical devices. The analysis of these random intrinsic effects should be considered in design for yield of ICs.

2.2.2 Parametric Process Variations

The parametric process variation (or manufacturing process variation, global variation, inter-die variation) appears on fabrication steps of ICs manufacturing. Although the fabrication techniques have been greatly developed, parametric process variations can still shift circuit performance and influence the yield. As shown in Figure 2.4, the parametric process variations is sorted as inter-die variations and intra-die variations. The variations occur between lots and wafers, between dies on a single wafer and within a die (see intra-die variations).

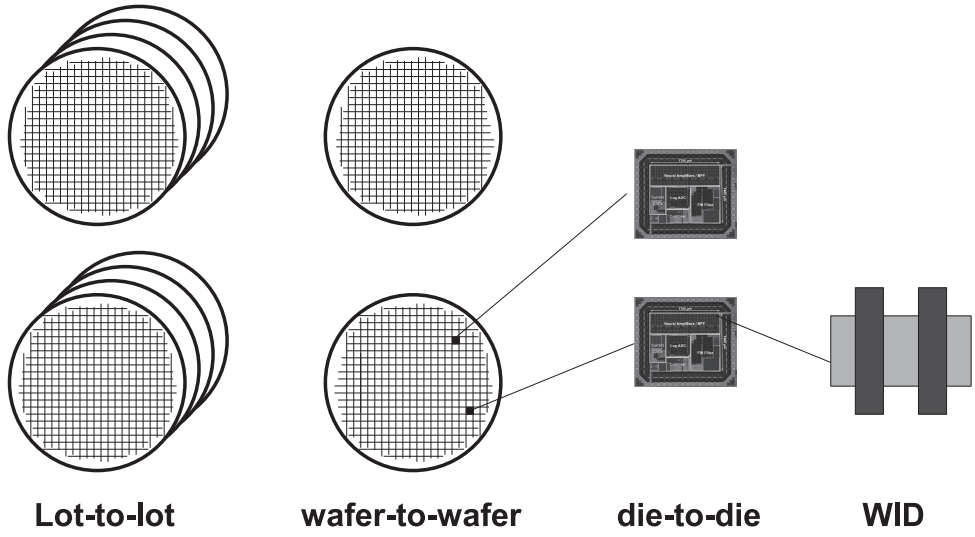


Figure 2.4: Parametric process variations: lot-to-lot, wafer-to-wafer, die-to-die. Intra-die variation (WID) occur within a die.

From the view of ICs designers, parametric process variations are induced by different physical independent phenomena. The variations can be represented by a deviation in the parameter mean of the circuit. [38] points out that the inter-die variation is generally much larger than intra-die variations. Analog circuits are sensitive to WID induced mismatch (e.g., offset voltage in symmetrical current mirror). Comparatively, WID variation is more critical in analog circuits than in digital circuits. Since the output of digital circuits depends on the value of transistor currents that charge or discharge the output capacitance. Another reason is that analog circuits with symmetrical design can effectively avoid inter-die variations.

2.3 Ageing Effects

Reviewing the research of ageing phenomena in CMOS technology over the last several decades, the main ageing effects of 65 nm CMOS transistor include Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time-Dependent Dielectric Breakdown (TDDB) and Electron migration (EM).

2.3.1 Temporal Ageing Effects

2.3.1.1 Negative Bias Temperature Instability

NBTI was first described by Miura and Matukura in 1966 [39]. It refers to the generation of positive oxide charge and interface traps at the Si-SiO_2 interface in CMOS transistors with negative gate bias, in particular at elevated temperature. As shown in Figure 2.5, when negative gate bias is applied to PMOS transistor, a transverse electric field (E_T) is generated and then weaken Si-H bonds at the Si-SiO_2 interface. Figure 2.8(a) shows the channel holes interact with the passivated hydrogen bonds in the dielectric, which result into positive oxide charge and interface traps.

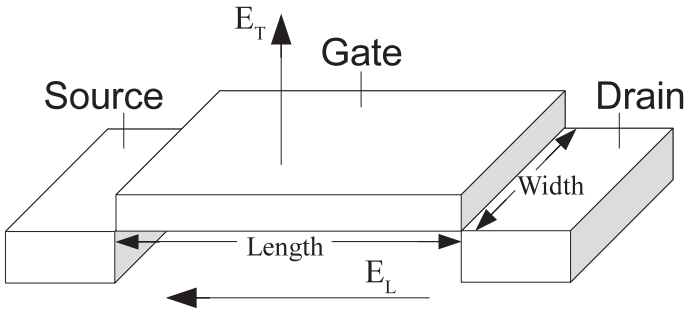


Figure 2.5: Electric fields in MOS transistor.

NBTI manifests itself as an increase in the V_{th} of the p-MOSFET transistor. Depending on the bias condition, NBTI has a stress phase (or static NBTI) and a recovery phase [40] (see Figure 2.6 and Figure 2.7). The dynamic NBTI (includes both stress and recovery phases) corresponds to the case where the PMOS transistor undergoes alternate stress (e.g., V_{gs} = - V_{dd}) and recovery (V_{gs} = V_{dd}) periods.

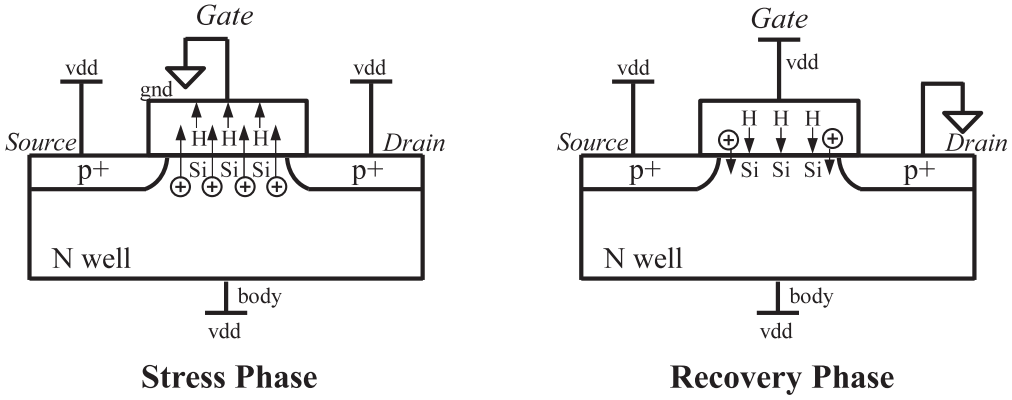


Figure 2.6: Stress and recovery phase of NBTI mechanism.

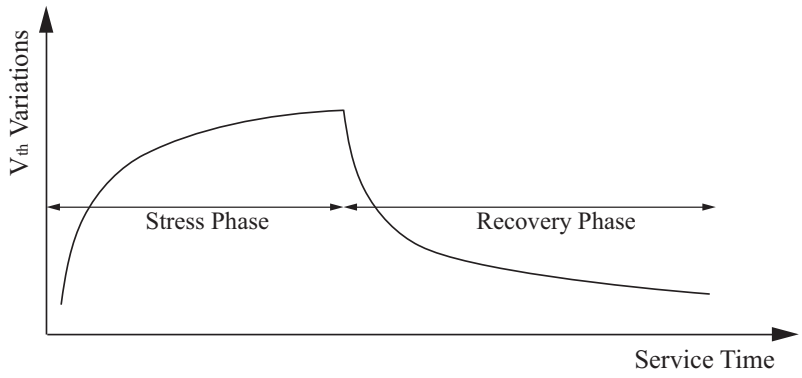


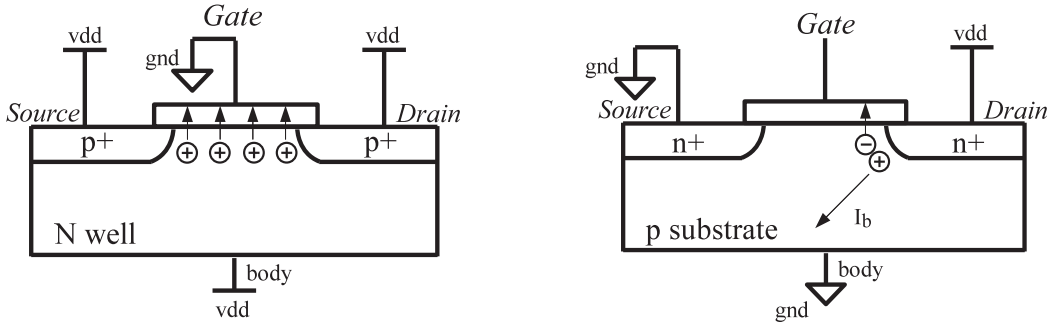
Figure 2.7: NBTI: V_{th} fluctutations versus ageing time

At system level, the effective techniques to mitigate the NBTI degradation are supply voltage tuning, PMOS sizing and duty cycle reducing [40] [41]. Besides NBTI, positive bias temperature instability (PBTI) also affects NMOS transistors. However, PBTI is not found in SiO_2 Poly-Silicon technology under normal use conditions. In sub-32 nanometer High-K technology, NMOS PBTI has higher V_{th} shift than PMOS NBTI [42].

[43] proposes a NBTI accelerated-lifetime model, the lifetime t_f is defined as the time to a fixed degraded V_{th} value:

$$t_f = A_{NBTI} \cdot (\frac{1}{V_{gs}})^{\alpha} \cdot exp(\frac{E_a}{kT}) \tag{2.5}$$

where A_{NBTI} is the process related prefactor, V_{gs} and T is gate-source voltage and temperature. k is Boltzmann's constant, α denotes the voltage acceleration factor, E_a is the activation energy.



(a) NBTI causes positive oxide charge and generation of interface traps.

(b) Hot carriers inject into the dielectric at the transistor drain end.

Figure 2.8: HCI (NMOS) and NBTI (PMOS) mechanisms at CMOS device level.

2.3.1.2 Hot Carrier Injection

Hot carrier injection (also named hot carrier degradation (HCD), channel hot carrier (CHC) or channel hot-electron (CHE) injection) emerges from the shrinking of transistor dimension and the electric field increasing in the channel. It is a temporal ageing unreliability effect as the density of interface states (N_{it}) produced by channel carriers peaks near the drain edge of the gate. When NMOS transistor switches on, V_{gd} is greater than or equal to zero and the V_{gs} is high enough, hot electrons can overcome the potential barrier

and inject into gate oxide due to high lateral electric field near the drain (see Figure 2.5 and Figure 2.8(b)). It causes the generation of the interface traps at the Si-SiO_2 interface which result in transistor parameters shift over time (e.g., threshold voltage (V_{th}) and electron mobility (μ)).

As mentioned above, NBTI occurs in the standby mode, while HCI stress conditions are inherent in CMOS circuit operation. There is no recovery phase in HCI since the annealing involving passivating a broken Si-H bonds towards a point of broken Si-H bonds [40]. CMOS Technology scaling causes voltage reduction, the relative lower drain current I_d will reduce HCI effects. However, this is not always feasible for gate lengths less than 50 nm. There is no significant reduction in gate voltage which is planned for additional scaling. On the other hand, noise and output charge represent a more important constraint in most design cases [44].

[43] also proposes a HCI lifetime model:

$$t_f = A_{HCI} \cdot (\frac{I_{sub}}{W})^{-n} \cdot exp(\frac{E_{aHCI}}{kT}) \tag{2.6}$$

where E_{aHCI} is the apparent activation energy, W is the device gate width, k is Boltzmann's constant, T is the temperature in kelvin, n is a technology dependent constant, and A_{HCI} is the model prefactor.

- Reaction-Diffusion model for NBTI and HCI

  The modeling of reaction-diffusion (R-D) mechanism dates back to the work of Jeppson and Svensson [45]. [46] [47] and [40] develop and verify R-D mechanism with NBTI and HCI ageing effects. R-D model can interpret the power law dependence of interface trap generation. Ageing effect induced degradation is represented by the degradation of process parameters (e.g.,V_{th} and carrier mobility (μ) degradation).

  - Reaction: When transistor is with electrical stress, electrical field can induce interface traps generation by breaking Si-H bonds at Si-SiO_2 interface. The positive holes in NBTI or hot electrons in HCI are generated because of the breaking of Si-H bonds.
  - Diffusion: Positive holes or hot electrons diffuse into the gate of transistor.

  The physical process of NBTI effect can be described as:

$$\text{Si-H} + \text{h}^+ \rightleftharpoons \text{Si}^+ + \text{H} \tag{2.7}$$

  where h^+ is positive hydrogen, a hydrogen (H) is removed from Si-H bond. During the stress phase of NBTI, Si-H bonds are weakening due to the presence of holes, positive charge (Si^+) and hydrogen atom are generated. Two generated hydrogen atoms combine together as hydrogen molecule and then diffuse away from Si-SiO_2 interface. P-MOSFET threshold voltage is impacted due to positive interface charge, thus:

$$\Delta V_{th} = \frac{Q_{IT}}{C_{ox}} = \frac{qN_{IT}}{C_{ox}} \tag{2.8}$$

  where Q_{IT} is the total interface charge, q is the electron charge, N_{IT} is the number of interface charges and C_{ox} is the oxide capacitance per unit area [40]. This R-D model can predict time-dependent variation of V_{th} and μ under NBTI stress and recovery phase. It is also validated on HCI ageing effect in [40].

There are some limitations in R-D model. With R-D model, NBTI is characterized as frequency-dependency. However, [48] shows a contradictory observations that NBTI is not frequency-dependent (at least for measurements up to 3 GHz). Besides, the application of R-D model is on digital circuits. Based on our knowledge, R-D model for analog circuits ageing simulation is not found in literature.

2.3.2 Time-Dependent Dielectric Breakdown

TDDB is a temporal stochastic oxide damage and also known as dielectric breakdown (BD). It is caused by defects generated in gate dielectric, which initiate the generation of traps in random positions inside the oxide and at the interface. The generated stress induced leakage current (SILC) forms a percolating path through the oxide and electrically short the gate to the substrate [19] [49]. Figure 2.9 represents the breakdown path in MOSFETs with percolation approach. Such a conducting path forms when a critical number of defects are locally generated between the polycrystalline Si (poly-Si) gate with a SiO_2 dielectric.

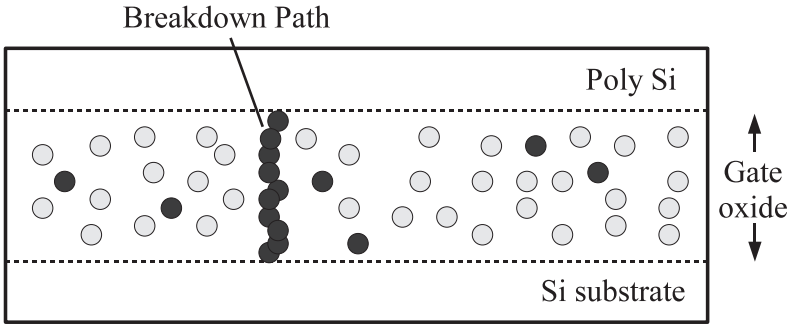


Figure 2.9: The percolation approach: generation of breakdown path between poly-Si and Si-substrate.

The statistics of breakdown are described using the Weibull distribution [28] [50], which are appropriate for a "weakest-link" type of problems:

$$F(x) = 1 - exp[-(\frac{x}{\alpha})^{\beta}] \tag{2.9}$$

where x represents the failure age (estimated time to breakdown), α and β are process dependent constants.

According to the thickness of gate oxide, there are different breakdown modes such as Hard-breakdown (HBD), Soft-breakdown (SBD) and Progressive-breakdown (PBD). The most harmful mode HBD can cause a catastrophic failure of the device and the entire circuit. For oxide thickness below 5 nm, HBD can be proceeded by SBD [19]. [51] reports that intrinsic breakdown defects are homogeneously distributed across the oxide area and follow the Poisson random statistics. The probability to have n^{th} SBD defects at time χ can be described with [28]:

$$P_n(t) = \frac{\chi^n}{n!} \cdot exp(-\chi) \tag{2.10}$$

$$\chi = (\frac{t}{t_{SBD}})^{\beta} \tag{2.11}$$

$$t_{SBD} = t_{63} \cdot (\frac{WL}{A_{ref}})^{\frac{1}{\beta}} \cdot (\frac{E_{ox}}{E_{ref}})^{\gamma} \tag{2.12}$$

β and γ are process dependent constants, where t_{63} stands for the time to breakdown at the 63^{rd} percentile in a transistor model with area A_{ref}, stressed at E_{ref}.

2.3.3 Electron Migration

Electron migration (EM) locates at the interconnect. This material migration is caused by the excessive current density stress which interacts with the ions of the metal [19]. As a result, during EM, metal atoms are removed from one end of the metal line and accumulates at the other end, forming voids at the entrance and hillocks at the exit of the metal line. Consequently, EM can result in open circuits (due to the voids) or line-to-line short circuits (due to the hillocks). EM can be accelerated by temperature and current density [19] [52].

EM effect must be considered in the layout design. Wires must be widened to reduce the degradation since in standard CMOS process, the thickness of the interconnect is fixed. Special layout technique like generating a bamboo structure, replacing aluminum with copper wires and depositing a passivation over the metal interconnect can be used to avoid the EM problem.

EM will remain a concern in advanced CMOS technology [53]. The technology scaling down leads to the growing of interconnect current densities. Advanced CMOS technology may reduce EM impact of increasing density but new performance requirements emerge that require increased interconnect reliability under conditions of decreased metalization [53].

Currently, there is no universal model to analysis EM mechanism and predict EM mean time to failure. [54] uses bimodal model for lifetime prediction under EM:

$$MTTF = A(j_e)^{-n} exp(\frac{E_a}{kT}) \tag{2.13}$$

where j_e is the current density and E_a is the EM activation energy. Results show that EM failure follows monomodal log-normal distribution. Besides, lifetime distribution and lifetime sensitivity model of EM are mentioned in [53]

A EM-aware physical design flow has been reported in [52]. It contains three current-density (current-driven routing, current-density verification and current-driven layout decompaction) driven design and verification tools, which can implement an effective consideration of EM-related constraints during physical design [52].

2.3.4 Ageing in High-K dielectric

[1] reported that new material brought about new reliability problems. From 45 nm node, the high-K metal-gate (HKMG) material has been used to replace Poly-Si-SiO_2 in dielectric layer of transistor [1]. It can characterize a gate impedance capacitor and exhibit significant reduction of gate leakage current. It also introduces more than 30% higher operating electric fields than 65nm node [55]. Thus, ageing effects are still stern challenge in 45 nm CMOS and below.

Figure 2.10 shows a NMOS transistor in high-k metal-gate structure. In 65 nm transistor with Poly-Si-SiO_2 technology, PBTI effect is not dominant compared to its NBTI counterparts and could be neglected. In 45 nm and below transistor with HKMG structure, PBTI occurs at the high-k stack in gate due to bulk-HK trap creation. These traps induce a high transverse electric field which mainly degrades transistor V_{th}.

Existing transistor ageing mechanisms such as NBTI, HCI and TDDB, remain and even become worse in HKMG transistors in advanced nanometer CMOS nodes [42]. Since the thin layer of SiO_2 (or SiON) has been maintained in between the substrate and the high-k stack, whereas the substrate/dielectric interface did not change, NBTI and HCI

remain a problem in HKMG technologies [56]. For TDDB mechanism, [56] presents the SBD in HKMG structure, which is caused by the generation of additional bulk traps under electrical stress. In high-k stacks, the increasing leakage current due to multiple SBDs can be a reliability threat for some applications.

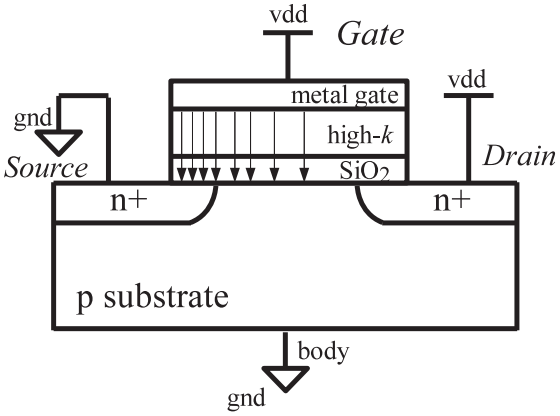


Figure 2.10: PBTI in high-k NMOS induced transverse electric field.

2.4 Yield

Yield in semiconductor industry is defined as the number of IC products that fulfill the design specifications (functionality and reliability) divided by the number of product that can be potentially made on the wafer surfaces [1]. Due to the influence of different manufacturing steps, the ICs fabrication yield can be further divided into two categories [57] [58]:

- Functional yield (also denoted as "hard" or catastrophic yield) explains the proportion of fully functional chips with no detected manufacturing defects. The functional yield is usually limited by processing defects and the catastrophic failure (e.g., short/open circuits), which in general destroy ICs functionality.
- Parametric yield (also known as "soft" or circuit-limited yield) shows the number of functional die meeting the required specifications. Parametric yield loss is related to process controlled practice, process and material variations.

ICs performance is qualified by different design specifications. Figure 2.11 shows the statistical spread of a certain performance parameter. The condition of functional yield loss and parametric yield loss are illustrated. In order to achieve high yield in ICs design and fabrication, yield modeling and simulation methods (e.g., design for yield (DFY) or design for manufacturability (DFM)) are proposed [59]. DFY and DFM methodologies conduce to mitigate yield loss with process controlled practices and manufacturing consideration.

As shown in Figure 2.12, yield loss exists in every manufacturing step [58]. The parametric yield can be calculated with Y_{wp} (wafer production yield), $Y_{functional}$ (functional yield), Y_{ap} (assembly and packaging) and Y_{bi} (burn-in):

$$Y_{parametric} = Y_{wp} \cdot Y_{functional} \cdot Y_{ap} \cdot Y_{bi} \tag{2.14}$$

Both process variations and ageing effects influence ICs yield. [60] and [61] define $Y_{parametric}$ in 2.14 as fresh yield or time0 yield (Y_{t0}). Besides fresh yield, aged yield ($Y(t)$ yield) is proposed for ICs under ageing effects, where t is the IC usage time.

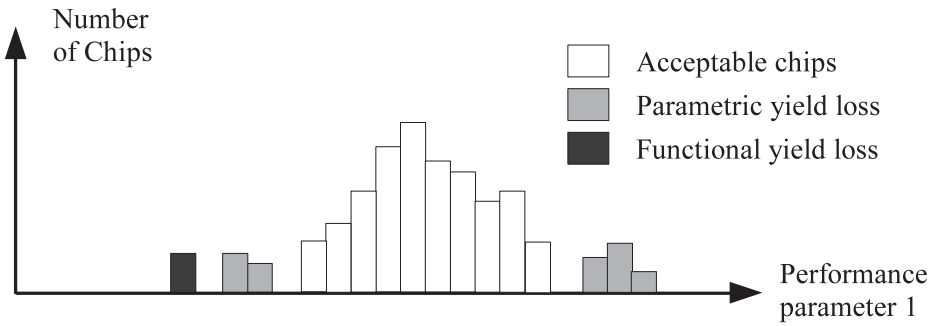


Figure 2.11: The performance parameters distribution of ICs: acceptable, parametric yield loss and functional yield loss

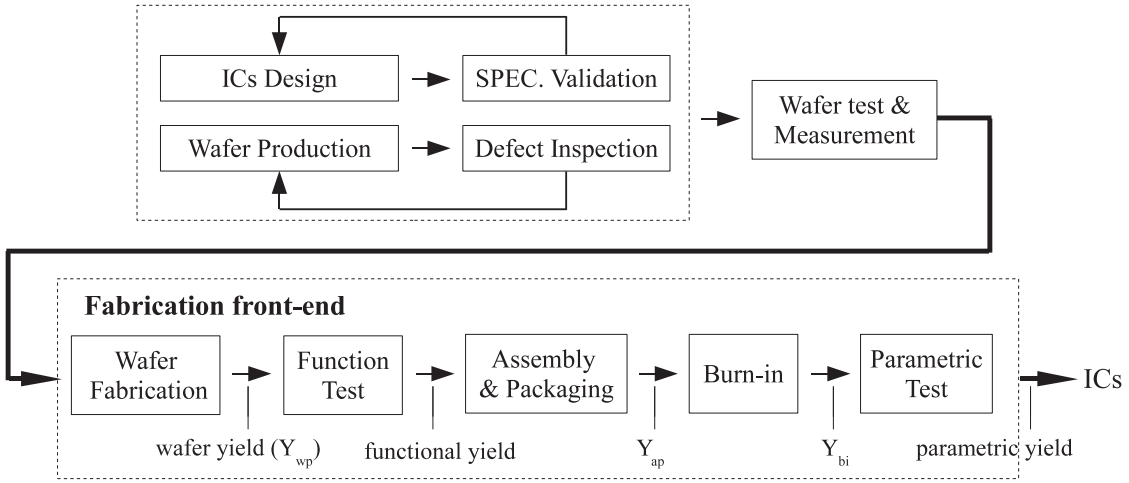


Figure 2.12: The manufacturing process flow of ICs: a perspective of yield in the fabrication fronts-end.

2.5 Conclusion

Transient faults, process variations, ageing mechanisms and yield are reviewed in this chapter. These reliability problems can influence ICs performance. As an example, Figure 2.13 shows the trend of parametric process variation and Electron migration. As the device technology is scaling down continuously, reliability issues have always attach great importance in both research and industry. Some reliability effects are well investigated and modeled at physical level. In order to estimate reliability of circuits and systems, it is highly important to develop reliability simulation tools and flows, reliability-aware methodologies and reliability enhancement approaches.

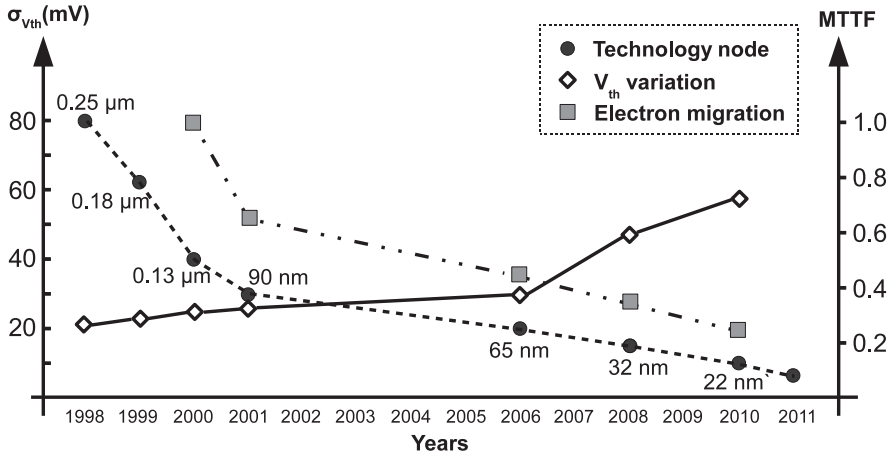


Figure 2.13: Examples of reliability trend: $\sigma_{V_{th}}$ of parametric process variation and MTTF of Electron migration [20].

Chapter 3

Methodology

The continuous minimization of CMOS transistor dimensions causes different reliability problems. It is necessary to develop reliability analysis tools and reliability-aware methodologies. Efficient tools and methodologies can help designers to realize reliability phenomena, reduce design failure rate and redesign costs [62], estimate ICs lifetime and develop integrated circuits with high robustness. In [2], Yang and Chern proposed the design for reliability (DFR) strategy which has been used in industrial design and manufacturing (e.g., aviation and automotive industry). Figure 3.1 shows this DFR loop applied to microelectronic field. Traditionally, ICs reliability test (test for reliability, TFR) is implemented after prototypes. For instance, screening, burn-in test and life time prediction have been widely used in practice. If the test results cannot satisfy the reliability requirement, redesign is needed. Afterwards, the DFR loop is used. ICs reliability simulation can be performed at ICs design phase.

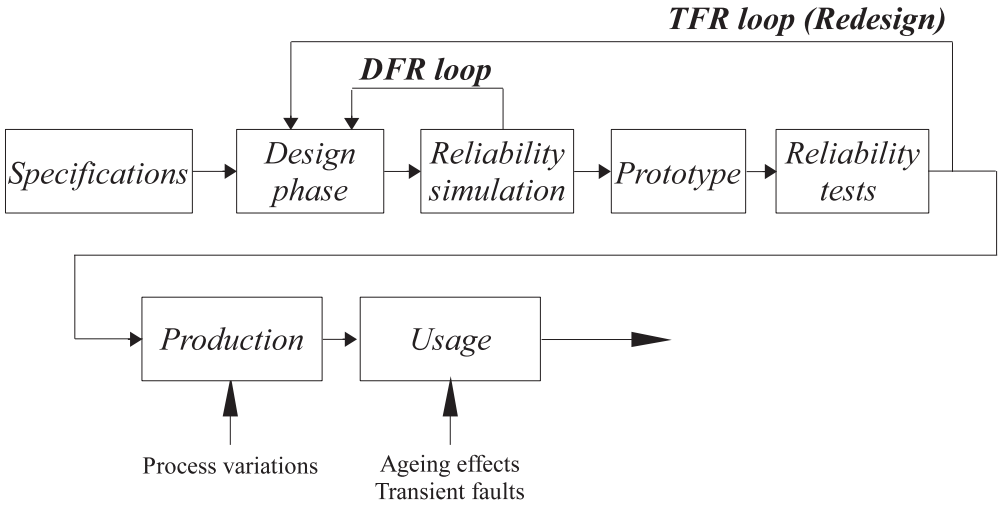


Figure 3.1: The design-for-reliability (DFR) flow [2]. Process variations, ageing effects and transient faults induced degradation can be estimated at ICs design phase.

In digital VLSI circuits, static timing analysis (STA) or statistical static timing analysis (SSTA) is a highly efficient method to characterize the timing performance and critical path [20]. While in analog ICs design, designers need to cover a lot of performance parameters which represent different figure of merits. Also, the efficiency and accuracy of reliability analysis are important. Computer-aided design (CAD) [63] or technology computer-aided design (TCAD) [38] methodologies become the trend of reliability tools

and methodologies.

Figure 3.2 illustrates reliability consideration of circuit performance. Reliability problems (introduced in Chapter 2) induced fluctuations and degradations are evaluated and estimated with proper methodologies. On the other hand, reliability enhancement methodologies can help designers to improve ICs under stress.

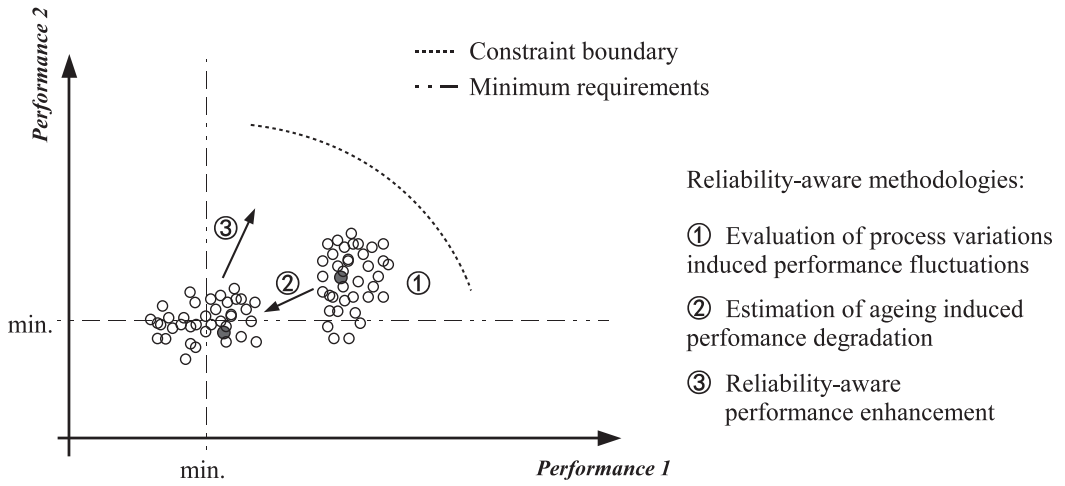


Figure 3.2: An illustration of reliability consideration on circuit performance. Process variations and aging degradations are included.

In this chapter, a state-of-arts of reliability-aware methodology is presented. CAD reliability approaches such as statistical modeling of process variations, hierarchical reliability analysis, co-evaluation for ageing effects and process variations, as well as reliability optimization are proposed for analog circuits and systems.

3.1 Lifetime Prediction

According to ITRS reports [1], reliability metric mean-time-to-failure (MTTF, or mean-time-between-failures (MTBF)) and failure-in-time (FIT) have been used to predict circuit lifetime and failure rate under wear-out mechanisms. In order to simplify the prediction model, it is assumed that different failure mechanisms are independent. The exponential distribution function is characterized by a constant failure rate over the lifetime of the device. This approximation is useful for representing a device in which all early failure mechanisms have been eliminated [64]. The standard sum-of-failure-rates (SOFR) model is used to calculate $MTTF$ in each unit:

$$MTTF = \int_0^\infty t \cdot \lambda_0 \cdot exp(-\lambda_0 t) dt \tag{3.1}$$

The sum of MTTF of a circuit, which is the combining failures from different mechanisms and different structures:

$$MTTF_{total} = \frac{1}{\Sigma_{i=1}^{m} \Sigma_{i=1}^{n} \frac{1}{MTTF_{ij}}} \tag{3.2}$$

where $\frac{1}{MTTF_{ij}}$ is the failure rate of the i^{th} structure due to the j^{th} failure mechanism and n is the number of structures and m is the number of failure mechanisms [65].

the FIT of the evaluated circuit or system:

$$FIT = \frac{10^9}{MTTF_{total}} \tag{3.3}$$

Lifetime prediction with MTTF has been accepted as the main reliability metric in industry. The advantage of lifetime prediction it that it can combine different reliability mechanisms together and predict the achievable lifetime. However, several works indicate that MTTF does not accurately capture the reliability characteristics [66] [67]. [67] also points out that MTTF loses too much information in averaging, which makes it an inaccurate indication for lifetime reliability, especially in the early-life reliability prediction. A novel metric called virtual age to model the ICs cumulative aging progress is proposed in [66]. The time-to-failure (TTF) model can predict system's failure point which is a proper cut-off cumulative failure rate during its operating lifetime.

3.2 Ageing Estimation

In principle, traditional ageing simulation methods and tools are similar: the classic Simulation Program with Integrated Circuit Emphasis (SPICE) type simulator manages the electrical simulation, while another software is used to process the simulation results. Based on the fresh simulation, ageing degradation models affect the electrical parameters values and generate aged circuit netlists. Another simulation is performed with aged netlists to calculate the degraded behavior at this stress time.

3.2.1 Commercial Simulation Tools

The underlying purpose of ageing simulation is to aid ICs designers to properly estimate degradations of performance parameters, so that design margins can be controlled. Figure 3.3 illustrates the commercial ageing simulation flow in Virtuoso UltraSim [62] and a similar solution is available for Mentor Graphics Eldo [68] simulators. Based on SPICE-level simulator, this flow can be applied to both analog and digital circuits. Ageing models are embedded in these simulators (e.g., Eldo with NBTI and HCI models).

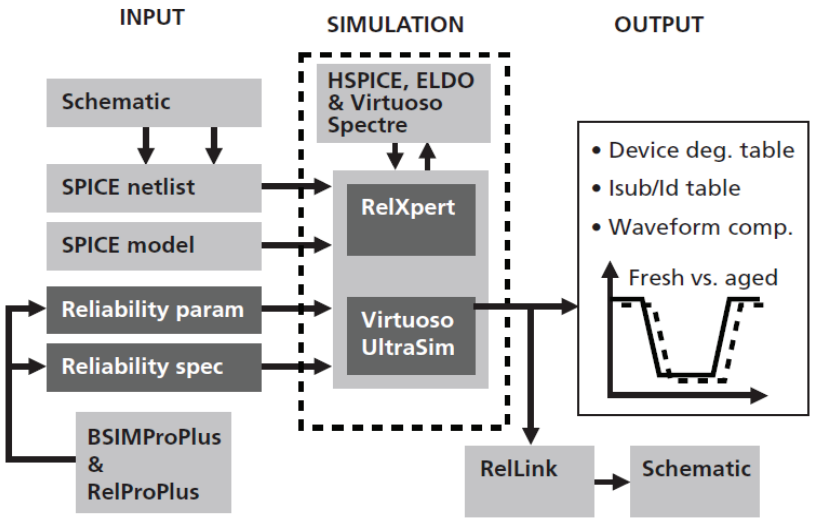


Figure 3.3: Ageing simulation with Virtuoso UltraSim [62].

Here, we briefly review the simulation procedure. First of all, with an initialization of ageing setup (e.g., ageing model selection, ageing time setup), a nominal circuit electrical

simulation (transient simulation) is performed. Then, ageing simulators (e.g., Relxpert or Eldo) is applied to process the simulation results with ageing degradation models. During this step, ageing effects can degrade physical parameters (e.g., V_{th0}, T_{ox}, n_{dep} in BSIM 4 model), transistor characteristics and parameters such as V_{th}, I_d and g_m can be affected. The aged netlist which includes degraded transistor parameters is generated. Ageing simulation is performed with this aged netlist. Finally, both fresh and aged circuit performance can be investigated by designers.

3.2.2 Ageing Equivalent Models

Main ageing effects (HCI, NBTI and TDDB) have been modeled with some equivalent circuits and methods, for example, the reaction-diffusion model discussed in Chapter 2.

3.2.2.1 A SPICE Model

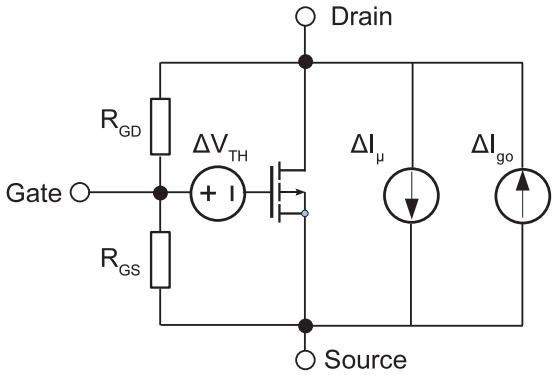


Figure 3.4: An equivalent transistor SPICE model for NBTI, HCI and SBD.

[28] and [69] developed the equivalent transistor SPICE model (see Figure 3.4) for NBTI, HCI and SBD. For HCI and NBTI effects, parameter degradation is modeled as V_{th}, mobility and output conductance degradation(ΔV_{TH}, ΔI_u and ΔI_{go} respectively). ΔV_{TH} is modeled as:

$$\Delta V_{th} = \frac{q(N_{IT} + N_{OT})}{C_{ox}} \tag{3.4}$$

N_{OT} is the number of oxide traps, where N_{OT} can be neglected under small gate bias.

$$\mu_{eff} = \frac{\mu_0}{(1 + \theta(V_{GS} - V_{TH}))(1 + \alpha\gamma\Delta V_{TH})} \tag{3.5}$$

θ and α are constant and varied in different CMOS process. γ depends on V_{DS}.

$$g_0 = (1 + \beta\Delta V_{TH}) \cdot \lambda_0 \cdot I_{DS0} \tag{3.6}$$

where λ_0 is channel modulation factor. I_{DS0} represents the drain current for an output conductance of zero.

SBD can be modeled with resistors R_{GD} and R_{GS}. The gate-source and gate-drain resistor can model the SBD induced increase of gate current. A further introduction will be proceeded in 3.2.2.2.

3.2.2.2 TDDB Equivalent Model

Otherwise from HCI and NBTI, so far there is no software that can evaluates TDDB degradation in integrated circuits. [70] and [71] reported electrical models of breakdown path in CMOS transistors. Since gate-to-diffusion (source or drain) breakdown are considered as the worst-case situations [72], SBD caused increasing gate current can be modeled by the Ohmic model (see Figure 3.5) with gate-source and gate-drain resistance R_{gd} and R_{gs}. The leakage current from gate to drain or gate to source in a transistor is:

$$I_{lek,gs} = \frac{V_{gs}}{R_{gs}} \quad and \quad I_{lek,gd} = \frac{V_{gd}}{R_{gd}} \tag{3.7}$$

On the other hand, voltage controlled current source (VCCS) based power law model is another solution in SBD study [71].

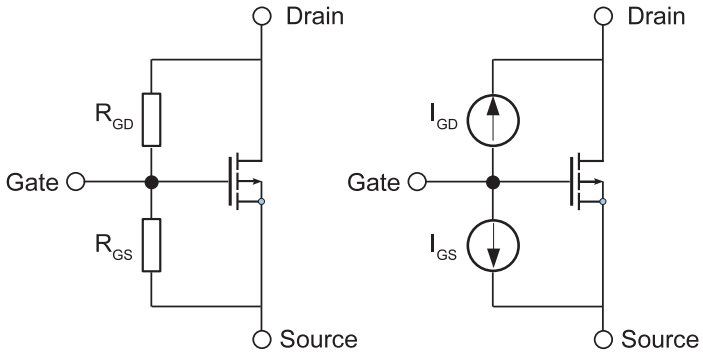


Figure 3.5: TDDB models: Ohmic (left) and VCCS (right) model

The traditional Ohmic model can build a current leakage path between transistor gate and source or drain diffusion. In [73], R_{gd} and R_{gs} are setup as a variable from 2.5 kΩ to 12.5 kΩ. The current source in VCCS model is calculated by:

$$I_{GD} = k(V_{GD})^a \; and \; I_{GS} = k(V_{GS})^a \tag{3.8}$$

a is a constant and K was calculated at $V = V_{dd}$. With a study to 40 nm SRAM memory, [71] concludes that traditional Ohmic model may overestimate SBD effect, whereas VCCS model presents a fair level of soft breakdown.

3.2.2.3 Aged Device Modeling with VHDL-AMS

Behavioral modeling of aged device for ageing simulation is a possible solution [74]. Figure 3.6 demonstrates the device ageing modeling with VHDL-AMS [74]. The solution is to model the ageing degradation law of each transistor with behavioral language, such as VHDL-AMS or Verilog-A. It can transform electrical VHDL-AMS MOS models into degraded MOS models. Once behavioral modeling of circuit/system is completed, aged device models can be used to simulate degraded circuit performances. The advantage of this method is that ageing simulation of circuits can be performed without external software to manage ageing effects. However, this methodology is not able to attract industry due to complex coding according to certain ageing effect.

```
ENTITY nmos is
     GENERIC (
              W : REAL;
              L : REAL;
             VT : REAL;
-- ...other param.
);


     PORT ( TERMINAL Tdrain, Tgrille,
              Tsource, Tbulk: ELECTRICAL );
END ENTITY nmos;


ARCHITECTURE mos1 OF nmos IS

   QUANTITY vds ACROSS ids THROUGH
            Tdrain TO Tsource;
   QUANTITY vdb ACROSS ibulk THROUGH
            Tdrain TO Tbulk;
   - .. other declarations

-- equations
-- ...
END ARCHITECTURE mos1
```

```
ENTITY nmos_degradable is
     GENERIC (
              W : REAL;
              L : REAL;
            VT0 : REAL;
-- parameters for hot carrier degradation
              B,M : REAL,
ageing_time_scale_factor : real=1.0;
-- ...other param.
);

     PORT ( TERMINAL Tdrain, Tgrille,
              Tsource, Tbulk: ELECTRICAL );
END ENTITY nmos;

ARCHITECTURE mos1 OF nmos_degradable IS

     QUANTITY vds ACROSS ids THROUGH
              Tdrain TO Tsource;
     QUANTITY vdb ACROSS ibulk THROUGH
              Tdrain TO Tbulk;
- .. other declarations
     QUANTITY VT:real :=VT0;
-- equations
- ...
     IF Ids>0 USE
          VT'dot ==ageing_time_scale_factor *
            B*Ids*(Ibulk/Ids)**M;
       ELSE
          VT'dot == 0;
     END USE;
END ARCHITECTURE mos1
```

Figure 3.6: Device ageing modeling with VHDL-AMS. Transformation of a MOS behavioral electrical VHDL-AMS model (left) into a model for ageing simulation [74]

3.3 A Review of Reliability Simulation Methodology

3.3.1 Ageing-aware Methodologies

3.3.1.1 BERT, ARET and RELY

The earliest reliability simulation method is DC wear-out modeling by SPICE-like simulators, which has been presented at the beginning of 1990. Hu developed the Berkeley reliability tools (BERT) [75] and Xuan implemented an ASIC reliability evaluation tool (ARET) [76]. Hsu proposed a systematic reliability approach named RELY [77]. Figure 3.7 shows the BERT design for reliability flow. It should be noticed that commercial ageing simulation tools, e.g., Eldo and UltraSim are developed on the basis of BERT. In detail, BERT, ARET and RELY apply a SPICE-type simulator and make circuit reliability analysis as follows:

- Step 1: Using SPICE simulator to extract the DC voltage stresses applied to each transistor in the circuit.
- Step 2: DC parameters are sent to degradation model to calculate the extrapolated degradation of every transistor over the stress time.
- Step 3: An aged netlist included every degraded transistor in the circuit will be generated.
- Step 4: Device/circuit is simulated again to calculate the aged behavior at this stress time.

These tools are easy to approach since there are only two SPICE operation points to simulate. However, the first drawback of BERT and ARET is that they cannot be applied

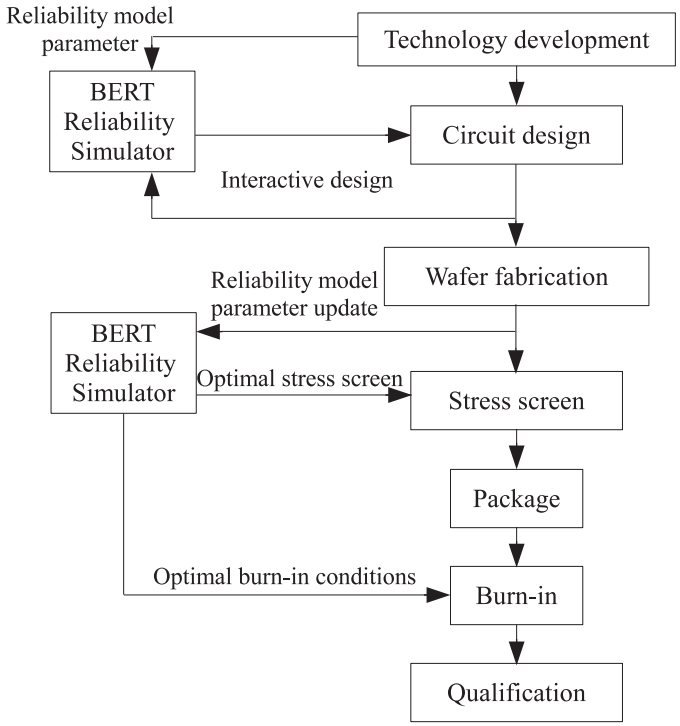


Figure 3.7: The BERT design for reliability flow [75]

to reliability analysis of large and complex circuits [28] [78]. Designers cannot evaluate the time-varying stress voltage of AC signal, the evaluation is only based on DC voltage. The BERT does not consider the potential time-dependent shift of circuit bias voltage during the aging process and its final result relies on extrapolation. These drawbacks may lead to errors accumulated by time [63].

3.3.1.2 Multi-level Modeling

The hierarchical structure of ICs include defect, transistor, circuit, system and device level. Based on behavioral modeling of aged device with VHDL-AMS, Bestory et al. proposed a simulation methodology by ageing modeling at circuit level [78], [79]. Figure 3.8 illustrates the reliability-aware multi-level modeling approach including bottom-up ageing modeling and top-down reliability simulation. [79] further develops behavioral ageing simulation with additional statistical simulation for technological dispersions. The bottom-up reliability modeling consists in the description of aging behavioral models following the ascending order of abstraction levels. The top-down reliability analysis is related to the descending order of abstraction levels, which intend to find out reliability critical circuits and architectures with reliability resilience.

[80] validates this multi-level modeling flow in the multi-standard RF front-end (see Figure 3.9), which is mainly comprised of low noise amplifier (LNA), mixer, digital controlled oscillator (DCO), low-pass filter and programmable gain amplifier (PGA). In the bottom-up approach, some design equations have been used to obtain an early estimation of the ageing of the circuit characteristics. In the top-down approach, architecture reliability improvements are proposed in order to avoid circuit overdesign. This reliability-aware methodology can link top-down and bottom-up approaches in a general method which has been the proposition of a new AMS/RF design flow increasing the circuit reliability [80].

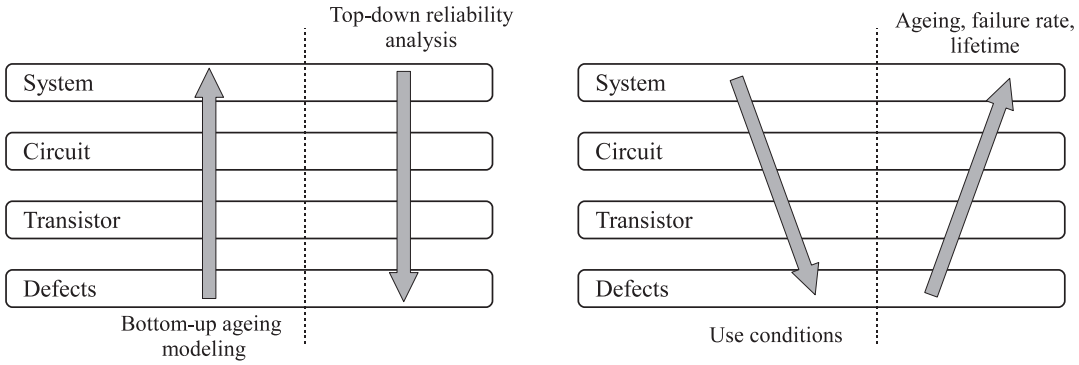


Figure 3.8: Reliability-aware multi-level approach. Left figure: bottom-up ageing modeling and top-down reliability simulation [78]. Right figure is the V-model for reliability. Researches work on the relationship between each level.

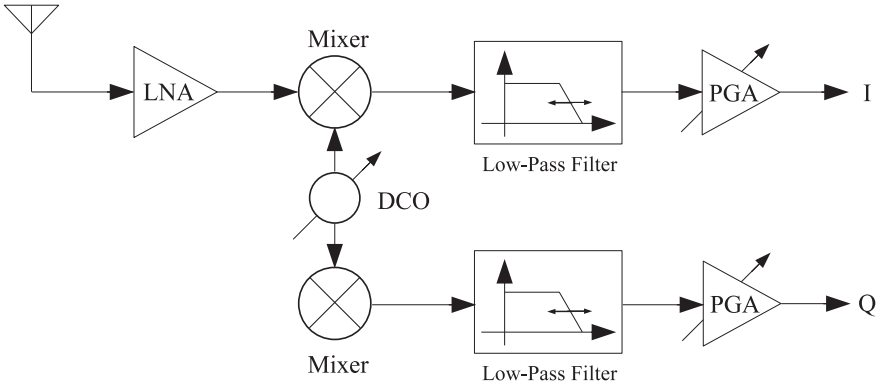


Figure 3.9: RF frontend

3.3.2 Variability aware Methodologies

Currently in ICs design and simulation, Monte-Carlo method and corner analysis are major concerned to analysis global/local process variations. With a general review, we discuss these two widely used analysis methods.

3.3.2.1 Monte-Carlo Method

Monte-Carlo (MC) method is used to predict the parameter fluctuations with the probability distribution. Without consideration of simulation times, MC techniques are inherently accurate as they do not involve any approximation of simulation results. In practice, MC simulation performs at a low level, demands excessive amounts of computer time, especially when combined with computationally intensive reliability. Figure 3.10 shows an example of the distributed simulation results.

In traditional MC sampling, a large number of simulation iterations is required to achieve a reasonably precise estimation of ICs fabrication yield. Advanced sampling techniques such as the stratified sampling, Latin Hypercube Sampling (LHS) and Quasi Monte Carlo (QMC) are applied to some digital circuits [81], [82]. They can achieve a faster convergence rate comparing with MC-based timing analysis. LHS is a type of stratified MC method with less number of samplings. Figure 3.11 illustrates the generation of LHS and the orthogonal LHS (OLHS) in a 2-D design space. LHS ensures that one sample is chosen per column and per row. While in OLHS, the sample space is divided into equally probable sub-spaces (In Figure 3.11, we divide the space into 4 sub-space). Thus, OLHS can further create a more even sample distribution than LHS.

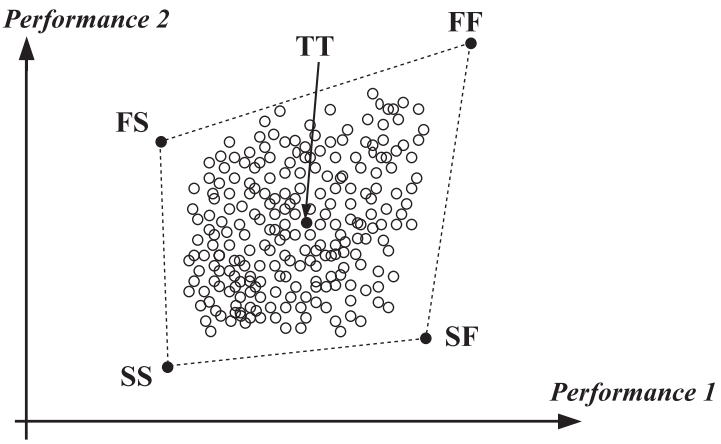


Figure 3.10: A comparison between MC analysis and corner analysis

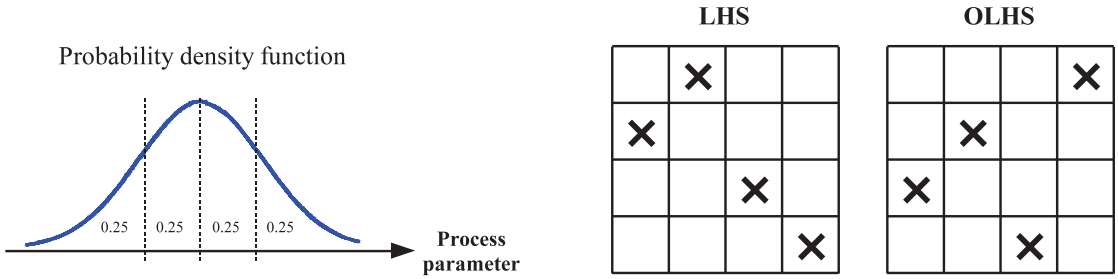


Figure 3.11: Probability density function, LHS, OLHS when sample size = 4.

Beside these MC-based methods, some non-MC variability analysis methods based on analyzing the linear sensitivity of performance metrics are proposed in [83]. Normally they calculate the total metric variance as the sum of the square of each linear component. In [83], a non-Monte-Carlo mismatch analysis method based on pseudo-noise modeling and PNOISE analysis is reported. Device mismatch is modeled as low-frequency pseudo-noise and the variation in performance is derived from the PNOISE simulation results.

3.3.2.2 Corner Analysis

From the perspective of ICs designers, in order to know the variability and yield information, traditionally is to setup guard-band with worst-case corner-based analysis. The process corners aim to show the general trends in the design quantities caused by the die-to-die process variations. Available performance corners are investigated. In SPICE-like simulator, NMOS and PMOS type transistors are defined with letter acronyms F, S and T (see Figure 3.10, F: fast, S: slow and T: typical). For example, NMOS and PMOS transistors with low oxide thickness, threshold voltage is represented with FF (fast NMOS, fast PMOS).

As shown in Figure 3.10, both MC and corner analysis are used to analysis performance variation. The corner-based analysis with one standard case (type TT) and four extreme ones (type FF, FS, SF and SS) can evaluate circuit variability at the risk of over-estimation. Excessive design margins is reserved in this condition. On the other hand, although MC analysis can achieve intrinsic accuracy with repeatedly simulations, long simulation time is unavoidable. Due to these drawbacks, in order to achieve efficiency-accuracy tradeoff, statistical methods are proposed in variability and yield analysis. A co-evaluation flow for both ageing effect and process variations is interesting.

3.4 Computer-aided Reliability-aware Methodology

In this section, current used computer-aided reliability-aware methodologies are introduced. This thesis mainly concentrates on ageing analysis, statistical estimation of process variation, variability-aware reliability analysis and reliability-aware performance optimization.

3.4.1 Reliability Analysis

3.4.1.1 Ageing Stress Evaluation Flow

Figure 3.12 shows the reliability-aware design flow with ageing stress evaluation [80]. It is a conceptual flow that involved ageing stress as a feedback to circuit designers. The selection of optimal design or reliable design is not well explained. The flow has been further expanded to nominal reliability analysis and variability-aware reliability analysis.

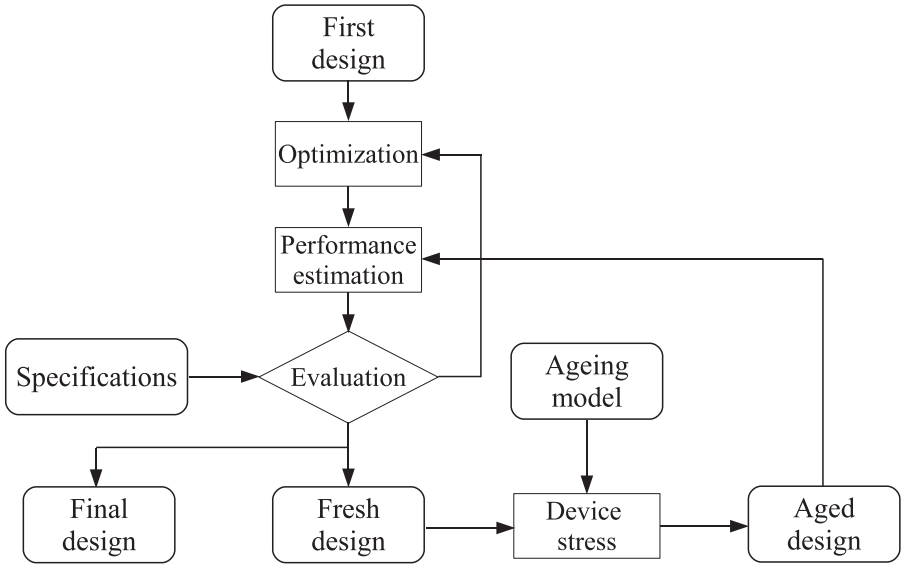


Figure 3.12: The reliability-aware design flow with ageing stress evaluation [80]

3.4.1.2 Nominal Simulation

The nominal reliability simulation [84] is widely used because of its high accuracy and easy accessibility. As shown in Figure 3.13, designed circuits and the stress time are the input of the ageing simulation process. Time-varying stress voltages have to be included. A transient simulation is required to simulate time-varying stress in every circuit node. With ageing degradation models, after extracting fresh netlist of designed circuits, a transient simulation over one period of the input signal is performed to generate a degraded netlist. This degraded netlist can be further applied to other types of simulations.

3.4.1.3 Worst-Case Distance Prediction

Antreich, Graeb and Wieser presented worst-case distance method for integrated circuits analysis and optimization in 1994 [85]. This methodology can be applied to worst-case analysis of circuit performance, which includes nominal design, worst-case analysis, yield optimization, and design centering. In addition, Pan and Graeb improved the worst-case

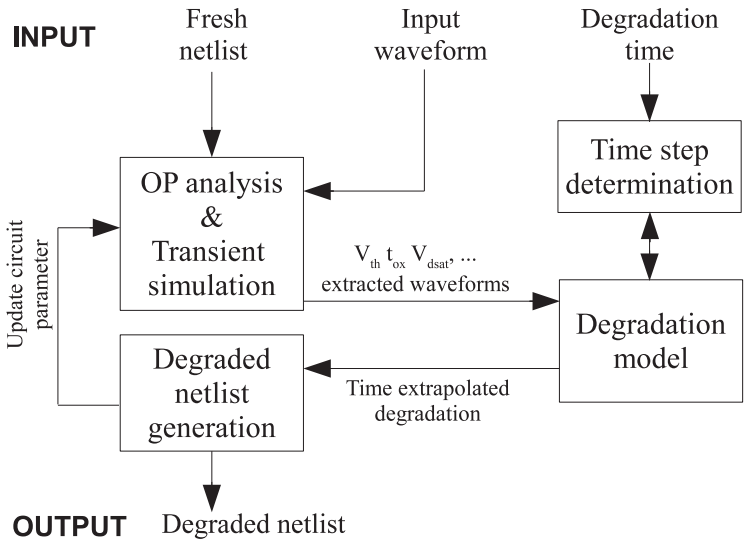


Figure 3.13: Nominal reliability simulation method with transient simulation [84].

distance methodology with ageing prediction [86]. They use a quadratic model (a second-order Taylor expansion in time domain) to evaluate degraded lifetime worst-case distance based on the fresh worst-case distance value:

$$\beta_W(t) \approx \beta_W(t_0) + \frac{d\beta_W(t)}{dt}(t - t_0) + \frac{1}{2}\frac{d^2\beta_W(t)}{dt^2}(t - t_0)^2 \tag{3.9}$$

where $\beta_W(t)$ stands for worst-case distance. t is the stress time node. Figure 3.14 demonstrates a general view of how to find the worst-case distance under ageing and process variations. Process parameters are modeled by Gaussian distribution as a 3σ range. According to design acceptance region, the worst-case distance under ageing effect is between the mean value and the boundary of the performance feature. The thick ellipsoid refers to the magnitude of the worst-case distance [60] [86].

This methodology is implemented with ageing models and reliability simulator (Relxpert). Simulation speedup is achieved with a tradeoff of accuracy loss [86]. The most attractive merit of this methodology is extensibility. Not only reliability prediction of circuit is achieved, also yield optimization and design centering is completed simultaneously.

3.4.1.4 Sensitivity Analysis and Failure Estimation

In [27], Singh and Koren proposed an efficient fault-sensitivity methodology to analysis transient faults. For complex circuits and systems, sensitivity analysis can also help designers to evaluate the sensitivity of all architecture characteristics for all building block characteristics [80]. [87] uses this method to analysis RF front-end, which contains block programmable gain amplifier (PGA), digital controlled oscillator (DCO) and Balun-LNA-I/Q Mixer (BLIXER). [10] also applies this method to reliability analysis of continuous-time sigma-delta modulator.

We assume that there are N different building blocks in a system: block 1, block 2,...block N. When unreliability effects happen, degradation occurred in block X may have high influence to whole system performance. Thus, block X is the most sensitive block and reliability-aware design of block X is essential. On the other hand, it is necessary to perform test case for all building blocks to find the weak spot. As shown in Table 3.1,

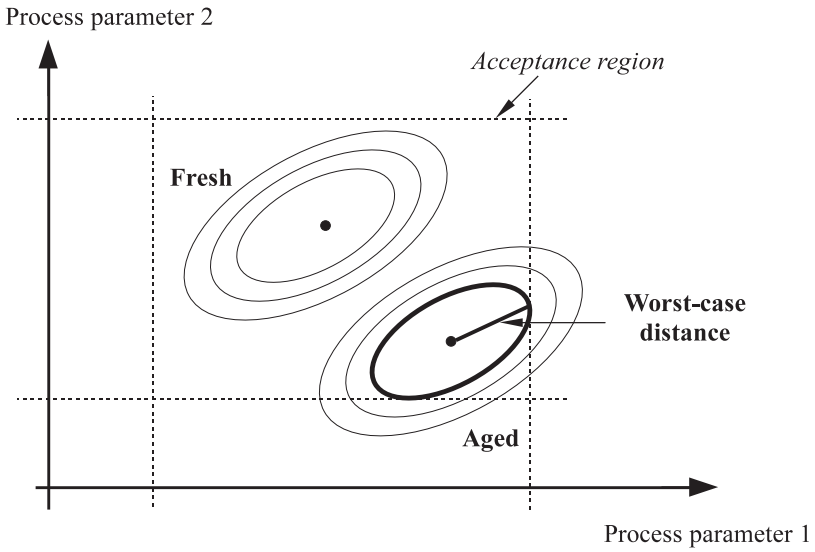


Figure 3.14: An illustration of worst-case distance [86] [60].

we denote 'No' for ideal case, 'Yes' for failure case. The block failure margin is always determined by the specification of each block. If $N = 3$, we have a test case:

Table 3.1: Block failure case, 'Yes' for failure.

case	Block 1	Block 2	Block 3
no failure	no	no	no
case 1	no	no	yes
case 2	no	yes	no
case 3	no	yes	yes
case 4	yes	no	no
case 5	yes	no	yes
case 6	yes	yes	no
case 7	yes	yes	yes

Sensitivity analysis and failure estimation can be performed with circuit simulators. The evaluation of weak spots in a circuit or a system is an important step to acquire reliability information. Designers can improve reliability and choose selective overdesign.

3.4.1.5 Reliability Analysis of Digital ICs

Traditional design process of digital ASICs includes implementations (behavioral described with VHDL/Verilog), simulations (particularly with functional simulation, RTL synthesis and post-layout simulation) and optimizations. When simulation results can satisfy design specifications, ASIC physical design is realized with place and route. RTL (register transfer level) synthesis is an important step in the design flow of digital ICs. It can transfer a given design (based on behavioral language) into gate level units, bring in the synthesis report and the circuit netlist.

The abstraction gap between reliability simulations of digital and analog circuits is that digital circuits are with time-constant stress signal (e.g., V_{gs}, duty cycle, frequency), whereas analog circuits are biased with time-varying stress signal (e.g., $V_{gs}(t)$). Based on

traditional design process of digital ASICs, Figure 3.15 illustrates the proposed ageing-aware design flow. According to design specification, behavioral modeling language for digital circuits (e.g., VHDL, Verilog) is used to describe the functions of circuits. The functional simulation is performed to verify the functional correctness of digital circuits. The statement of library includes necessary technology files. With RTL synthesis of designed circuits, the generated netlist is re-simulated by an ageing simulator, which contains NBTI and HCI models. A transient simulation is performed to evaluate the stress on each transistor/gate. Aged netlist which contains degraded information is generated and can be further applied to post-layout simulations. However, this method is not acceptable in reliability analysis of VLSI circuits and systems.

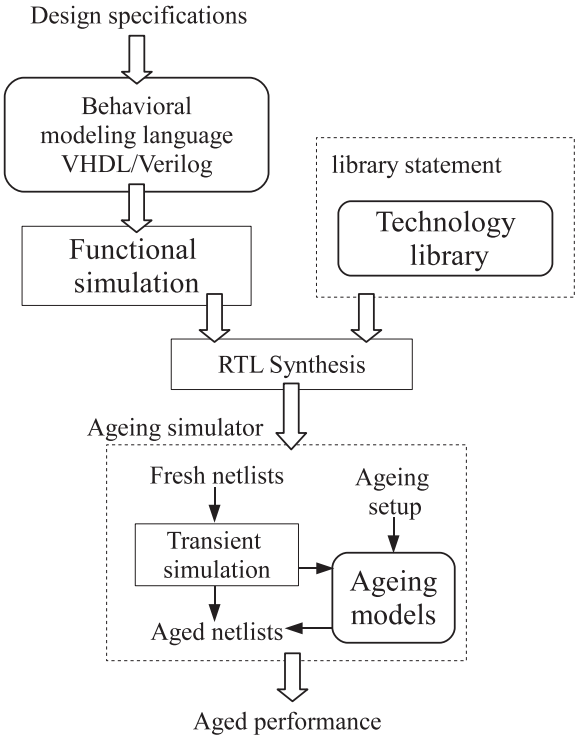


Figure 3.15: Reliability-aware flow of digital ICs

Instead, if reliability information is combined into technology library (see Figure 3.15), reliability-aware consideration can be implemented in synthesis step. A set of reliability models (e.g., failure models and ageing mechanism models) are developed for each failure manifestation. Both fresh and aged performance can be reported in synthesis results (with area constraint or speed optimization), which contained the number of ports/nets/cells, area (number of gates), time slack, the bottleneck (critical path) and maximum operation frequency. Furthermore, the generated aged netlist can be evaluated in the step place and route.

3.4.2 Statistical Modeling of Process Variations

Due to variability and time-dependent reliability problems, the nominal performance can not represent actual ability of ICs. In order to ensure robust designs, standard MC analysis of process variations has been widely used though it lasts very long simulation time. On the other hand, traditional corner-based analysis can describe NMOS/PMOS transistors as maximum and minimum values of characters e.g., threshold voltage, saturation currents [38]. However, this kind of worst case causes risks of over- or under-estimation of

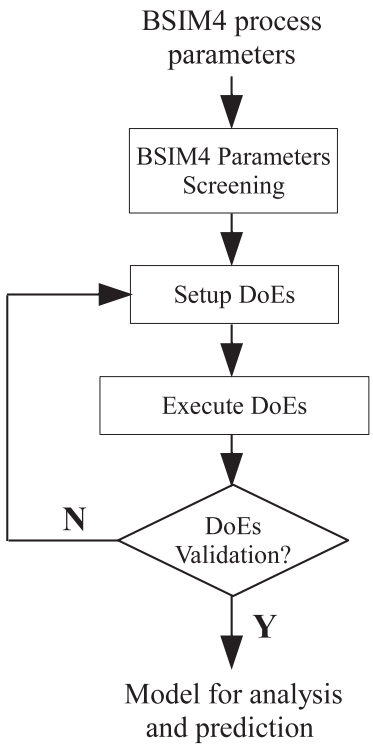


Figure 3.16: The DoEs analysis flow: parameter screening, setup DoEs and performance prediction

process variations.

In this section, statistical CMOS variability is studied based on BSIM4 model. It is a physics-based, accurate, scalable, robust and predictive MOSFET SPICE model for circuit simulation and CMOS technology development [88]. The impacts of process variations at physical level are investigated. Commonly used statistics methods are correlation analysis, regression analysis, design of experiments (DoE) and response surface modeling (RSM) (see Table 3.2).

Table 3.2: Statistics methods and corresponding functions in general

Statistics methods	Function
Correlation analysis	filter out correlated BSIM4 process parameters
Regression analysis	Screen out less significant BSIM4 process parameters
DoEs	Simulate circuit/system performance with controlled experiments
RSM	Map BSIM4 process parameters to performance parameters

3.4.2.1 Design of Experiments

Design of experiments (DoEs) is an information-gathering procedure in statistical analysis. Applying to ICs analysis, the purpose of statistical DoEs is to help designers to characterize the impact of the input factors on the output parameters. We can use it to select, compare process factors (e.g., BSIM4 physical parameters) and predict objectives (e.g., performance parameters). Figure 3.16 illustrates the detail steps of DoEs. Table 3.3 shows common applied DoE methods in screening and prediction.

DoEs can provide several solutions to generate experimental designs for various situa-

Table 3.3: Different DoE methods in screening and prediction, according to the number of factors

	$2 \leq$ Number of factors ≤ 4	Number of factors ≥ 5
Screening	Full factorial, fractional factorial	Fractional factorial, Plackett-Burman
Prediction	Central composite, Box-Behnken	N/A

tions. Commonly used design are the two-level full factorial (contains all combination of different levels of the factors) and the two-level fractional factorial design (with a fraction such as $\frac{1}{2}$, $\frac{1}{4}$ of the full factorial case, or other type, e.g.,Plackett-Burman (PB) designs, central composite designs (CCD)).

3.4.2.2 Parameter Screening

Screening is used to minimize the number of process parameters. Correlation analysis and stepwise regression analysis (execute by Plackett-Burman design) are discussed in this subsection. More than 800 process parameters exist in BSIM4 model (version 4.5). As shown in Figure 3.17, the total number of parameters in Part C and D is 39. Screening analysis is implemented with:

- Correlation analysis filters out correlated BSIM4 parameters.
- Stepwise regression analysis (Plackett-Burman design) determines the significant order of left BSIM4 parameters.

Correlation refers to the linear dependence between two variables (or two sets of data). In statistical BSIM4 parameter modeling, correlation analysis is used to filter out correlated BSIM4 parameters. The correlation coefficient ρ_{B_i,B_j} between two BSIM4 parameters B_i and B_j with expected values μ_{B_i}, μ_{B_j} and standard deviations σ_{B_i} and σ_{B_j} is defined as:

$$\rho_{B_i,B_j} = \frac{cov(B_i, B_j)}{\sigma_{B_i}\sigma_{B_j}} = \frac{E[(B_i - \mu_{B_i})(B_j - \mu_{B_j})]}{\sigma_{B_i}\sigma_{B_j}} \tag{3.10}$$

where E is the expected value operator, *cov* means covariance. If ρ_{B_i,B_j} is +1 or -1, the selected two BSIM4 parameters show a positive (-1 with negative) linear dependence to each other. One of these two BSIM4 parameters can be moved out from model. After correlation analysis, a design of experiments should be selected to verify this new model. To simplify this model, stepwise regression analysis is applied, analysis results such as p-value from hypothesis testing are evaluated to determine the significant sequence of left BSIM4 parameters.

Stepwise regression is used to further minimize the BSIM4 process parameters. According to Table 3.3, A two level Plackett-Burman design is selected to execute stepwise regression. Hadamard matrix can generate an orthogonal matrix for input parameters whose elements are all either plus signs or minus signs (Plus signs (+) represent factors with maximum values; minus signs (-) for minimum values). In this case (see Table 3.4), only 12 runs are needed with Plackett-Burman designs. A full factorial design would require $2^{11} = 128$ runs.

In detail, stepwise regression is applied to build regression models between BSIM4 process parameters (input factors) and performance parameters of circuits and systems (objectives). We can make hypothesis testing for this meta-model for every independent input factors. The p-value, partial F-values and R^2 value can be used to set a certain

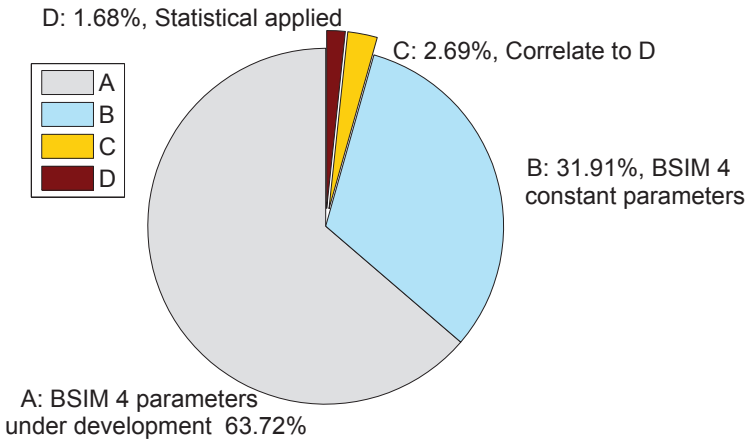


Figure 3.17: The total number of BSIM4 parameters is 893, some parameters (Part A) are still under development (currently equal to 0 or set to NaN), Part B represents constant BSIM4 parameters which are not influenced by process variations. BSIM4 parameters in Part C and D are proceeded with screening analysis.

		x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	x_{11}
1	+	+	+	+	+	+	+	+	+	+	+	+
2	+	-	+	-	+	+	+	-	-	-	+	-
3	+	-	-	+	-	+	+	+	-	-	-	+
4	+	+	-	-	+	-	+	+	+	-	-	-
5	+	-	+	-	-	+	-	+	+	+	-	-
6	+	-	-	+	-	-	+	-	+	+	+	-
7	+	-	-	-	+	-	-	+	-	+	+	+
8	+	+	-	-	-	+	-	-	+	-	+	+
9	+	+	+	-	-	-	+	-	-	+	-	+
10	+	+	+	+	-	-	-	+	-	-	+	-
11	+	-	+	+	+	-	-	-	+	-	-	+
12	+	+	-	+	+	+	-	-	-	+	-	-

Table 3.4: Screening experiments with Plackett-Burman design: 11 two-level factors for 12 runs. Plus signs (+) represent factors with maximum values; minus signs (-) for minimum values

threshold to test the hypothesis of regression model. At each step, the p value of an F-statistic is computed to test models with or without a potential BSIM4 parameter. If a parameter is not currently in the model, the null hypothesis is that the parameter would have a zero coefficient if added to the model. If there is sufficient evidence to reject the null hypothesis, this parameter is enrolled. Conversely, the parameter is removed from the model. Finally, the most optimum regression equation is built with the most significant BSIM4 parameters.

The number of BSIM4 parameters applied to the final meta-model is depend on the setup of threshold value. Further study with 65 nm circuits will be presented in Chapter 4.

3.4.2.3 Response Surface Methods

Response surface method (RSM) is another important statistical method to build relationship between input factors (BSIM4 process parameters) and objectives (circuit performance parameters). According to BSIM4 factors distribution, experimental runs are performed with circuit simulator. Central composite design (CCD) is a typical fractional factorial design applied to RSMs. CCD such as circumscribed (CCC), inscribed (CCI) and face centered (CCF) are different in range and rotation of factors. Figure 3.18 illustrates the distribution of different CCDs with two design factors. Besides three types CCDs, the Box-Behnken design (BBD) is an independent quadratic design which does not contain an embedded factorial or fractional factorial design. Since BBD does not have any combination point at any corners, some applications can benefit from BBD and avoid some extreme design cases.

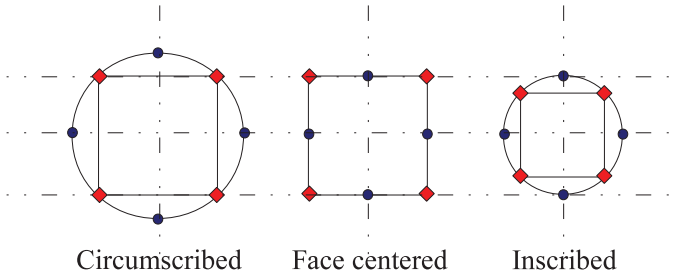


Figure 3.18: Comparison of the three type central composite designs

Number of factor	*2*	*3*	*4*	*5*	*6*	*7*
Full factorial	4	8	16	32	64	128
Fractional factorial ($\frac{1}{2}$)	2	4	8	16	32	64
Central composite	9/9	15/15	25/25	25/43	45/77	79/143
Box-Behnken	N/A	13	25	41	49	57

Table 3.5: Number of runs in different type of DoEs. Central composite is represented with full/$\frac{1}{2}$fractional.

The simulated performance parameter will be used to generate RSMs with BSIM4 parameters. The response surface model can be used for displaying graphically the mathematical model between BSIM4 process parameters and circuit performance. Successive building of RSMs can help designers estimate varied and aged circuit performance efficiently. Sometimes, using linear model is hard to achieve adequate accuracy because of

exponential complexity, quadratic model or even cubic model is required. The accuracy of RSMs can be evaluated by Root-mean-square error (RMSE). It is a measurement for differences between model predicted value ($Y_{predicted,n}$) and simulated value ($Y_{simulated,n}$), where:

$$RMSE = \sqrt{\frac{\sum_{n=1}^{N}(Y_{predicted,n} - Y_{simulated,n})^2}{N}} \tag{3.11}$$

$$Y_{linear} = \beta_0 + \beta_1 X_1 + \beta_2 X_2 \tag{3.12}$$

$$Y_{quad} = Y_{linear} + \beta_{12} X_1 X_2 + \beta_{11} X_1^2 + \beta_{22} X_2^2 \tag{3.13}$$

$$Y_{cubic} = Y_{quad} + \beta_{112} X_1^2 X_2 + \beta_{122} X_1 X_2^2 + \beta_{111} X_1^3 + \beta_{222} X_2^3 \tag{3.14}$$

For high order polynomial, Filiol and O'Connor proposed the piecewise-polynomial modeling approach based on statistical methods (e.g., DoEs and RSM) and splitting strategy [89]. This approach achieves good approximation properties and efficiency with analog circuits.

3.4.2.4 DoEs-RSMs

Algorithm 1 Statistical Flow

1: **INPUT**: BSIM4 parameters
2: Plackett Burman design for eight BSIM4 parameters $b_1, b_2, \cdots, b_8$
3: Building initial multiple stepwise regression model $P = f(b_i)$ and test p value of an F-statistical
4: **for** $i = 1$ to j ,$i \leq j$, $j \leq 8$, fit $P = f(b_1, \cdots, b_j)$, examine p-value of model in regression
5: **end for**
6: **if** b_i not in the model have p-value less than the entrance tolerance
7: **then** Add b_i with smallest p-value b_i in regression
8: **end if**
9: **if** p-value of b_i currently in model larger than the exit tolerance
10: **then** Remove b_i from current model
11: **end if**
12: Central composite design with selected b_i
13: Quadratic response surface modeling
14: **OUTPUT**: response surface, significant order of BSIM4 parameters

Figure 3.19 illustrates the statistical design flow aware process variation. BSIM4 physical parameters have variations that are statistically modeled by Gaussian, log-normal or uniform distribution. In BSIM4 model (Version 4.7 [88]), there are almost 900 different physical parameters in a standard 65 nm CMOS transistor. In order to evaluate the impact of process variations to circuit or system performance, statistical methodologies are implemented to achieve simulation efficiency. As shown in Algorithm 1, the first step is to extract physical parameters. Considering both accuracy and efficiency, a 100 runs Latin Hypercube Sampling (LHS) Monte Carlo experiment is performed to generate BSIM4 parameters with distribution $B = \overrightarrow{b_1}, \overrightarrow{b_2}, \overrightarrow{b_3}, \cdots, \overrightarrow{b_n}$ (see Algorithm 1). In this algorithm, we apply screening design based on Plackett Burman. Regression analysis is applied for seeking the dominant physical parameters. The central composite design (CCD) and response surface modeling (RSM) are used sequentially to process the statistical data.

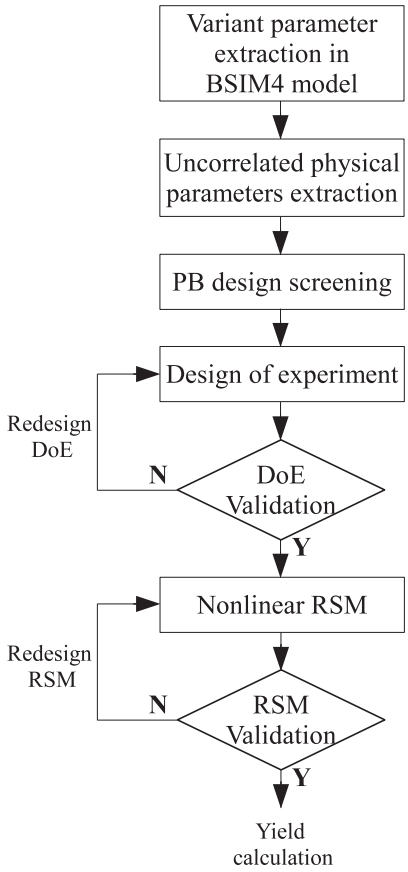


Figure 3.19: Statistical design flow aware process variation

3.4.3 Variability-aware Reliability Analysis

3.4.3.1 Time-dependent Variability Related to BTI Effects

[90] studied the relationship between time-dependent variability related to BTI effects in MOSFETs. The proposed simulation methodology can simultaneously evaluate process variability and BTI effects with a circuit simulator. A three-step simulation methodology has been mentioned in this work:

- Obtain the complete set of BSIM4 SPICE model parameters of the fresh transistors from the fresh $I_D - V_{GS}$ and $I_D - V_{DS}$ curves using AURORA software tool.
- Measure stressed $I_D - V_{GS}$ and $I_D - V_{DS}$ per stress time. This process is repeated until fitting convergence. When all the degraded device curves have been fitted for a given stress time, the V_{TH0} and U_0 mean values and their standard deviations (δV_{TH0} and δU_0) are calculated.
- Evaluate the circuit and device response after stress. The circuit and device response after stress are evaluated, combining MC and SPICE simulations.

This methodology has been validated with different configurations of amplifier circuits. Results showed that DC gain and BW of amplifiers can be evaluated under process variations and BTI effects.

3.4.3.2 Surrogate-model-based Reliability Analysis

The surrogate model (or meta-model) is an approximate, compact scalable analytic models that approximate the multivariate input/output behavior of complex systems, based on a

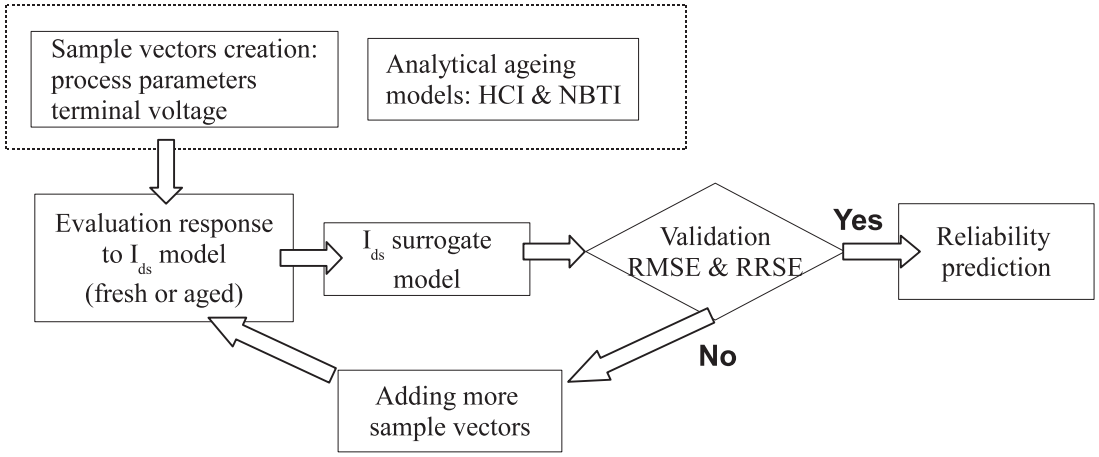


Figure 3.20: Circuit reliability analysis with surrogate model [91] [92].

limited set of computational expensive simulations [93]. Yelten et al introduced surrogate model into reliability analysis [91] [92]. Figure 3.20 shows the flowchart of surrogate modeling. The methodology includes:

- Sample vector selection: based on statistical methods, the proposed surrogate model includes six process parameters: intrinsic mobility (μ_0), intrinsic threshold voltage (V_{th0}), the variations due to mask/etch processes of effective gate length (ΔL_{eff}), the electrical gate equivalent oxide thickness (t_{ox}), channel doping parameter (N_{ch}), the zero-bias lightly doped drain-source resistance ($R_{ds,0}$); terminal voltages: the gate-source voltage V_{gs}, the drain-source voltage V_{ds} and the bulk-source voltage V_{bs}. OLHS sampling method (see Figure 3.11) is used to develop these sample vectors.

  The sample vectors of the surrogate models are formulated for both NMOS and PMOS type transistors as:

$$Deviation_{NMOS} = [T, t_{ox}, N_{ch}, \Delta L_{eff}, V_{bs}, V_{th0n}, \mu_0, V_{gs}, V_{ds}, R_{ds0}, t_{age}] \quad (3.15)$$

$$Deviation_{PMOS} = [T, t_{ox}, N_{ch}, \Delta L_{eff}, V_{sb}, V_{th0p}, \mu_0, V_{sg}, V_{sd}, R_{sd0}, t_{age}] \quad (3.16)$$

- Surrogate modeling: the saturation drain current I_{ds} is modeled approximately with BSIM model equation. Based on Kriging basis functions, surrogate model is built with MATLAB toolbox Design and Analysis of Computer Experiments.

- Reliability simulation: BSIM model is replaced by surrogate model. Reliability simulation is performed with a circuit simulator. The accuracy of surrogate model is evaluated by root-mean-square error (RMSE) or root-relative-square error (RRSE)

3.4.3.3 Co-evaluation of Ageing Effects and Process Variations

Figure 3.21 shows the shift of performance distribution due to ageing effects. In this case, a reliability aware variability simulation methodology is developed.

As shown in Figure 3.22, this methodology aims to:

- Judge the circuit ageing-immune or ageing-sensitive;

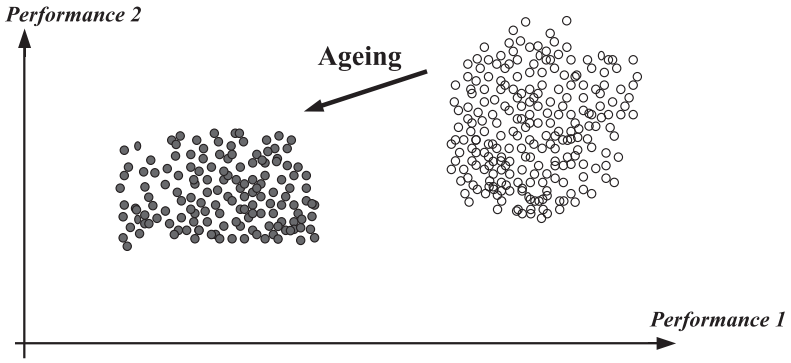


Figure 3.21: The shift of the performance distribution due to ageing

- Estimate degradation of circuit performance due to parametric process variations and ageing effects;

- Find the most critical process parameters.

The flow begins with ageing model selection (HCI and NBTI). The schematic of designed circuit and the stress time are the input of the ageing simulation process. With ageing degradation models, after extracting fresh netlist of designed circuits, a transient simulation is performed to generate an aged circuit netlist. On the branch of process variation, after filter out less important BSIM4 parameters, selected parameters are set up with a proper DoE mode. Ageing effect and process variation are evaluated by circuit simulator. Nominal simulation with transient and DC analysis is performed at transistor level. Other analysis such as AC, PSS (periodic steady-state) and Monte-Carlo can be performed with saved aged circuit netlist (degradation information included). Simulation data processing is followed in order to plot response surface. RSMs are used to help designers to obtain intuitionistic reliability information at circuit design phase. For ageing-sensitive circuits, varied RSMs are used to estimate ageing and variability. Meanwhile, for ageing-immune circuits, a fixed RSM can supply variability information to designers.

3.4.3.4 Hierarchical Reliability Analysis

For complex AMS circuits and systems, directly performing ageing analysis or Monte-Carlo simulation (for process variation) on flat transistor level is not suitable according to computation efficiency. [94] presented a hierarchical statistical method to analyze process variations of $\Sigma\Delta$ modulator. After, Huard proposed a bottom-up hierarchical approach for ICs reliability [95]. It aims to propagate reliability information from the lowest level (physical level) to higher levels (e.g., system level and product level). The intermediate levels also play important roles in this reliability information propagation chain. Different hierarchical levels are linked one-by-one with relevant reliability simulation tools and methods [95].

Figure 3.23 demonstrates this hierarchical reliability analysis flow with $\Sigma\Delta$ modulators. Reliability effects (e.g., ageing mechanisms and process variations) induced degradations and fluctuations at physical level can propagate up to product level (via transistor level, circuits level (OTA) and system level ($\Sigma\Delta$ modulator)). System performance under process variations and ageing phenomena can be efficiently evaluated. A further study of simulation tools and methods which link each level will be presented in the next chapter.

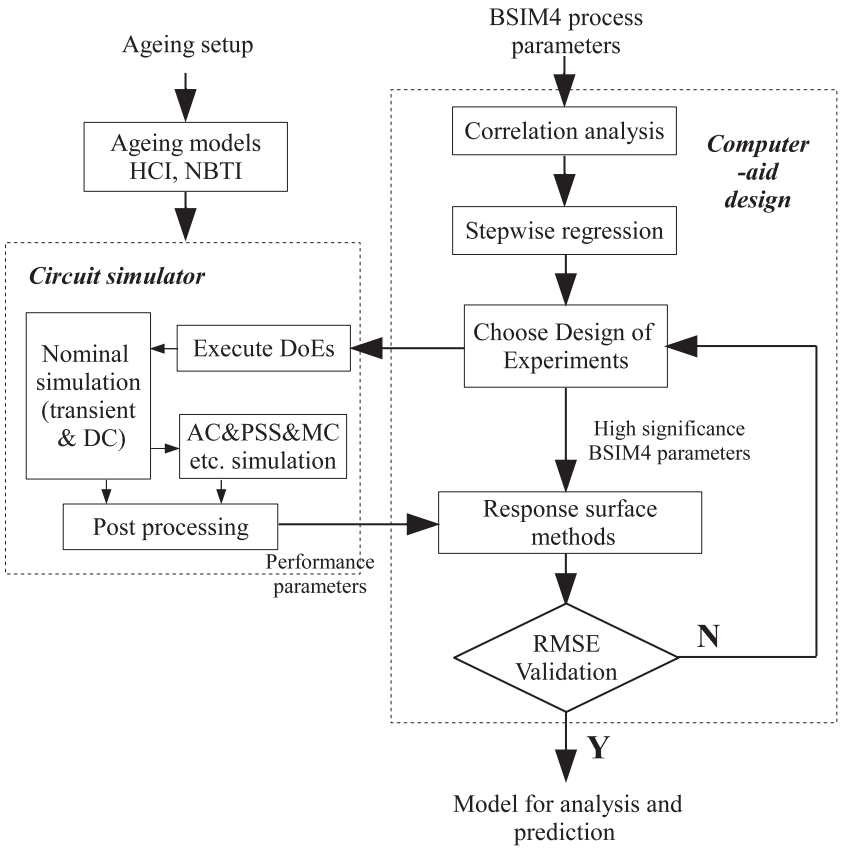


Figure 3.22: Reliability aware variability simulation methodology. A co-evaluation of ageing effects and process variations

3.4.4 Reliability-aware Optimization

The reliability-aware optimization flow based on worst-case distance method provides sizing rules to achieve performance enhancement [60]. Besides, Pareto fronts is an useful technique for evaluating the performance space. It provides the set of all optimal trade-offs of competing performances of a given circuit [14].

3.4.4.1 Reliability Optimization with Sizing Rules Method

Graeb et al. developed the sizing rules method [96]. They proposed 30 sizing rules for geometric or electrical constraints concerning function or robustness for important CMOS building blocks. Figure 3.24 illustrates the types of sizing rules, which consider circuit function, robustness, geometries and electrical properties.

[60] adds reliability as a new design metrics into sizing rules method. Based on the analysis and optimization of the fresh worst-case distance value for each circuit performance, reliability optimization for analog circuits with sizing rules has been proposed. Both process variations and aging effects (HCI, NBTI) are evaluated. As shown in Figure 3.25, fresh and aged sizing rules as well as the maximum area constraints are applied to yield analysis. The trade-off between approximated layout area and circuit reliability can be reported to ICs designers.

3.4.4.2 Multi-objectives Optimization with Pareto Fronts

According to design specifications, designers need to design and optimize analogue circuit and system considering different performance parameters. The optimization of one

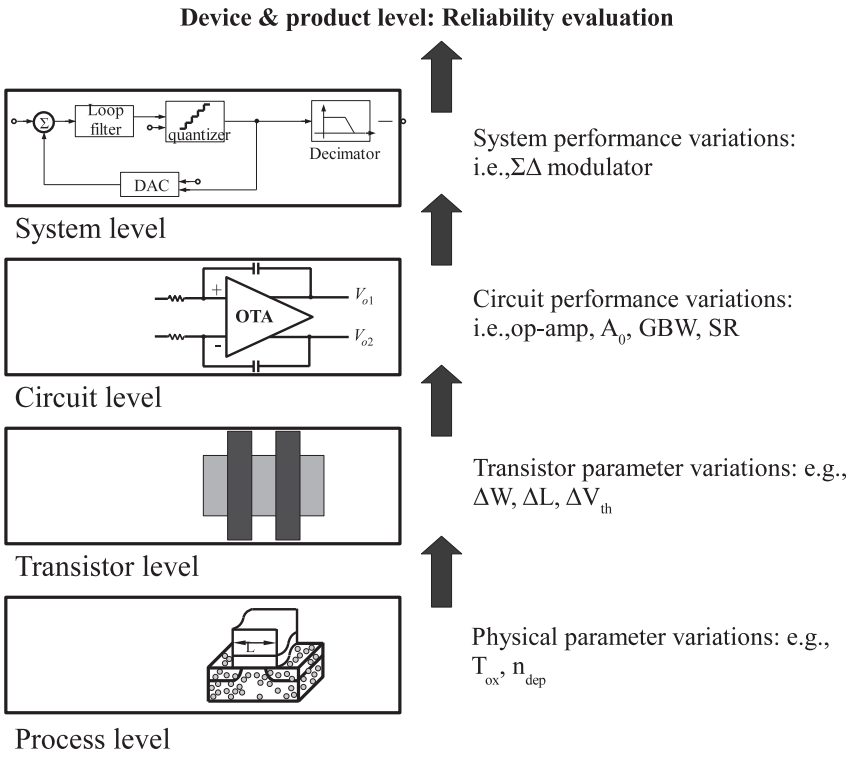


Figure 3.23: A bottom-up approach for reliability

performance parameter is often at the cost of others. Comparing to single objective optimization, there is a set of optimal solutions in Multi-objective Optimization (MOO). Every solution in this set is defined as Pareto optimal or non-dominated. Worst-case Pareto fronts represent the worst performance that can be simulated from a given circuit topology across the entire performance space. The optimization of circuit performance based on Pareto fronts has been reported in [97], [98]. A set of multi-objective solutions can help designers to evaluate performance parameters objectively.

- Given two vectors x, y, we define that $x \leq y$, if $x_i \leq y_i$ for $i = 1, \cdots, k$, thus x dominates y ($x \prec y$).
- It is defined that a vector of decision variables $x \in \mathcal{X}$ is non-dominated with respect to $\mathcal{X}$, if there does not exist another $x' \in \mathcal{X}$ such that $f(x') \prec f(x)$.
- It is defined that a vector of decision variables $x^* \in \mathcal{F}$ ($\mathcal{F}$ is the feasible region) is Pareto-optimal if it is non-dominated with respect to $\mathcal{F}$.
- The Pareto Optimal Set $\mathcal{P}^*$ is:

$$\mathcal{P}^* = \{x \in \mathcal{F} \mid x \; is \; Pareto \; optimal\} \tag{3.17}$$

- The Pareto Front $\mathcal{PF}^*$ is $f(x)|x \in \mathcal{P}^*$.

Non-dominated sorting-based multi-objective evolutionary algorithm [99] is used to generate Pareto fronts [100]. Fig. 3.26 illustrates a Pareto front in the presence of two objective functions. We define BSIM4 process parameters as m decision variable $\vec{\mathcal{B}}$, and

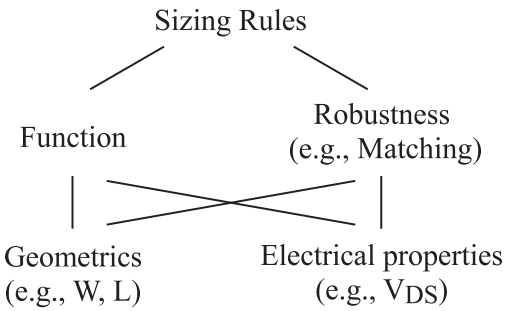


Figure 3.24: Sizing rules for important CMOS building blocks [96]

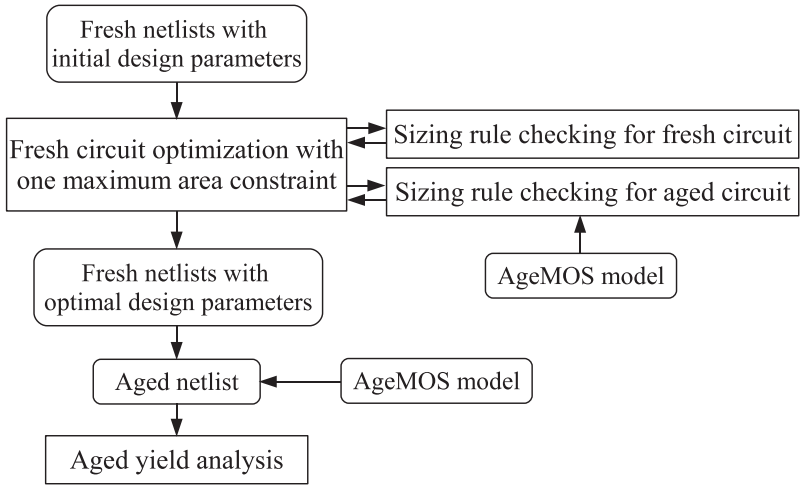


Figure 3.25: Reliability optimization flow with one maximum area constraint [60]

circuit performance set n objectives $\vec{\mathcal{P}}$. There is a multi-objective optimization problem [101]:

$$Minimize\ \vec{\mathcal{P}} = \mathcal{F}(\vec{\mathcal{B}}) = (\mathcal{F}_1(b_1, ..., b_m), ...\mathcal{F}_n(b_1, ..., b_m)) \tag{3.18}$$

$\mathcal{F}$ is made by circuit simulation. We can define that a vector of decision variables $b \in \vec{\mathcal{B}}$ is non-dominated with respect to $\vec{\mathcal{B}}$, if there does not exist another $b' \in \vec{\mathcal{B}}$ such that b dominates b' (denotes as $b \prec b'$, where $\mathcal{F}(b) \leq \mathcal{F}(b')$). This decision vector is also defined as Pareto-optimal, where $\mathcal{F}(b)$ is called Pareto front point.

Figure 3.27 illustrates the proposed reliability-aware approach which can map process parameters to performance parameters of circuits. With correlation analysis and regression analysis, we filter out uncorrelated BSIM4 parameters and find out dominant parameters. Five dominant BSIM4 process parameters are selected: intrinsic threshold voltage (v_{th0}), intrinsic mobility (μ_0), length variation (x_l), gate oxide thickness (t_{ox}) and channel doping concentration (n_{dep}). Firstly, initial setups are needed for ageing model selection and ageing duration time. In the step of DoEs, a five factor Box-Behnken design is generated (to replace MC simulation). Then, circuit simulation is performed for ideal and aged circuit performances. In order to evaluate the degraded performance of circuits under ageing effects and process variations, multi-objective (consider different performance parameters) worst-case Pareto fronts are generated by non-dominated sorting evolution. Besides, if the performance parameters are lower than design target, optimization is required.

The accuracy of statistical estimated worst-case Pareto front can be evaluated by equation 3.11. It is a measurement of differences between statistical model values ($P_{stat,n}$)

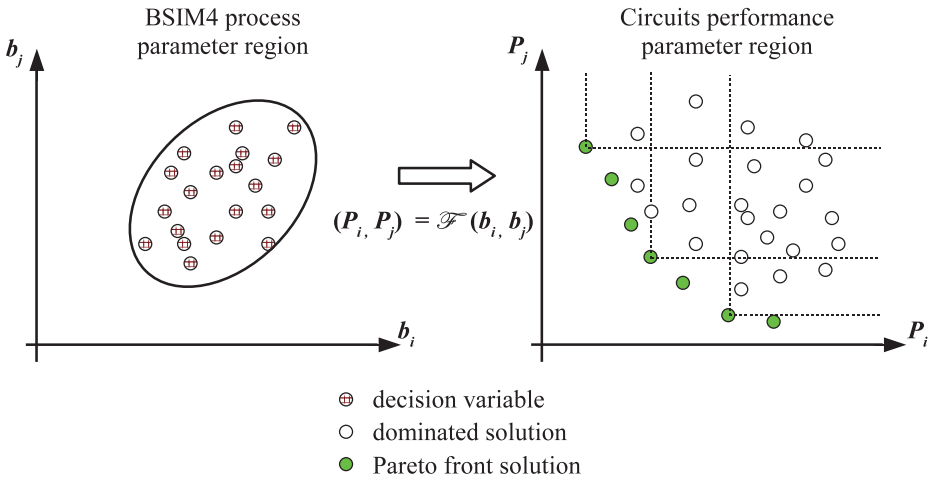


Figure 3.26: A two objective Pareto front. We define BSIM4 process parameters as m decision variable $\vec{\mathcal{B}}$, and circuit performance set n objectives $\vec{\mathcal{P}}$. The performance set as Pareto front is demonstrated with green points.

and standard MC based analysis results ($P_{MC,n}$).

3.5 Reliability Enhancement

3.5.1 Introduction

Since reliability issues become gradually important, many reliability enhancement techniques have been proposed. These techniques are always limited to certain circuit under certain reliability effect. Also, tradeoff exist between circuit design and reliability improvement.

- Redundancy and overdesign

  Redundancy techniques are implemented when analog and digital circuits suffer from transient upsets. Redundancy-based techniques have been widely applied to correct the faulty behavior of components and achieve high reliability. The N-tuple modular redundancy (NMR) is a classical technique to design fault-tolerant circuits and consists in the concurrent operation of replicated circuits [102]. A typical hardware redundancy is the famous triple module redundancy (TMR) where we replicate the main hardware unit three times and whose outputs are compared against each other by a majority voter [103]. However, few articles discuss redundancy techniques on analog circuits. [104] proposed the use of analog voting to increase the reliability of a 5-bit ADC with NMR comparator.

  Besides, when ICs suffer from variability and wear-out problems, the conventional way of handling such problems is to provide safety margins during the ICs design phase. From the point of design for reliability, although circuit overdesign adds unnecessary cost, it can make excessive guard-band to system reliability. [105] demonstrates a selective overdesign based strategy to enhance analog circuits reliability under NBTI effect.

- Other reliability enhancement techniques

  Auto zeroing and chopping stabilization are techniques for dynamic offset cancellation, especially used in differential configurations (e.g., OTAs). [106] used these two

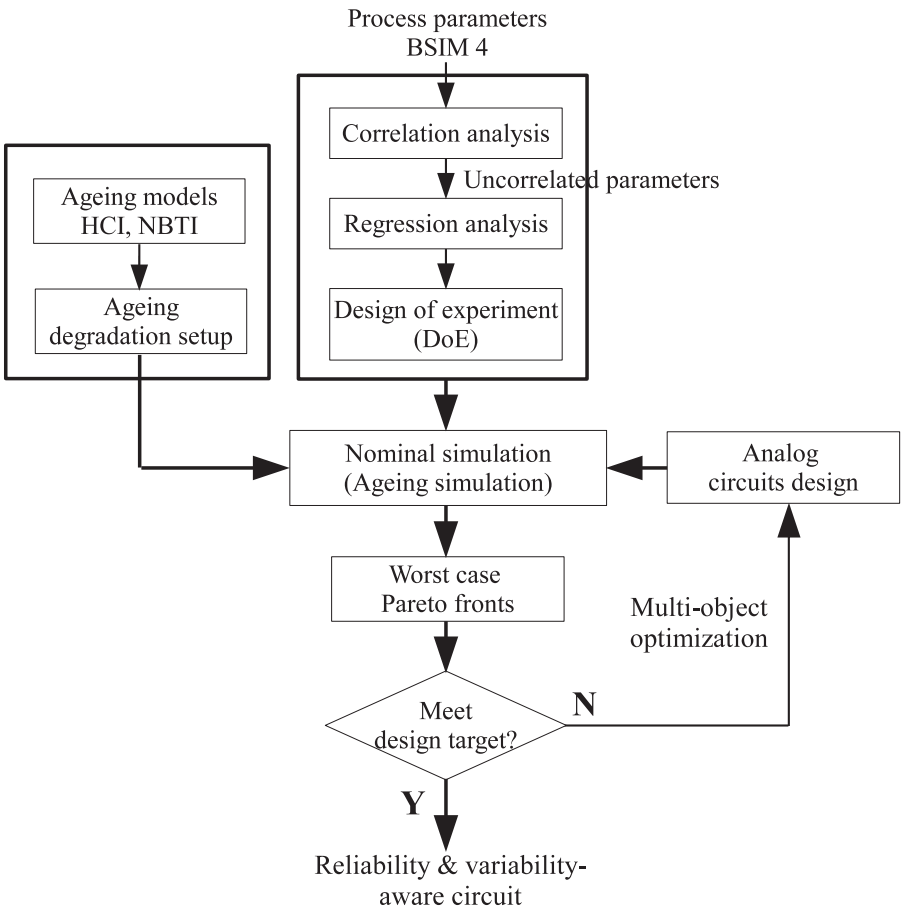


Figure 3.27: Reliability analysis flow with Pareto optimization. Parametric process variations and HCI, NBTI ageing effects are evaluated

techniques to reduce degradation-induced (HCI and BTI) offset in a 32 nm comparator. In [107], differential matching with switching input pair and body-biasing are proposed to mitigate the impact of NBTI.

3.5.2 Noise Tolerance

As the size of CMOS devices is scaled down to nanometers, noise can significantly affect circuit performance [108]. Noise immunity of a logic gate or a circuit is an important design criterion with dimension scaling to nanometers. [109] [108] present the basic idea of MRF design: under the probabilistic framework, we cannot expect logic values ("0" or "1") in a circuit at a particular time to be correct. We can only expect the probability distribution of the values to have the highest likelihood of being in a correct logic state.

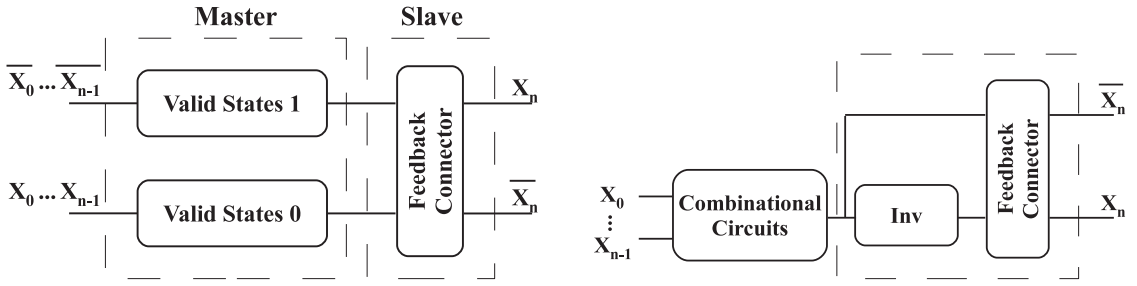
[110] proposes the noise-tolerant probabilistic-based designs based on Markov Random Field (MRF). In order to map the MRF to a noise-immune circuit, we follow three steps [110]:

- Step 1: for each variable x_i, a bistable storage element should exist with the value of "0" and "1".

- Step 2: generate each valid input-output states and evaluate the Gibbs energy function (stands for the joint probability of a clique of variables).

- Step 3: a feedback loop should exist for each valid state to enhance its stability, consequently maximizing the joint probability of correct logical values.

Since directly mapping the noise-immune combinational circuits costs considerable areas (as shown in Figure 3.29). Recently, many noise immune design structures for CMOS digital circuits have been reported, e.g., Differential Cascode Voltage Switch (DCVS) [111], MAS-MRF (Master and Slave MRF) [108] and CENT-MRF (Cost-Effective Noise-Tolerant MRF) [17]. Figure 3.28(a) 3.28(b) illustrate the block diagrams of MAS-MRF and CENT-MRF.



(a) The MAS-MRF structure (b) The Cent-MRF structure

Figure 3.28: The block diagram of two MRF structures [108] [17].

In order to demonstrate the efficiency of different noise tolerance methods, a NAND gate is studied. Figure 3.29 shows the circuit diagram of a noise-immune NAND. Three variables exist here: x_0, x_1 and x_2, each of them taking two values "0" or "1". Then each valid state should be generated by a combinational sub-circuit and finally the feedback loops enhances the valid states.

Figure 3.30 and Figure 3.31 show the MAS-MRF and CENT-MRF structures applied to the NAND gate. Supposing that an inverter requires 2 transistors and a NAND gate requires 4 transistors, the area overhead of the CENT-MRF structure is only 10 transistors. Compared with MRF NAND gate (see Figure 3.29) and MAS MRF NAND gate (Figure 3.30), the CENT-MRF NAND gate reduces the number of transistors from 60 to 14 (a 76.67% reduction) and from 28 to 14 (a 50% reduction), respectively. Note that this overhead is constant and independent of the target logical function. Another related benefit of CENT-MRF NAND is that it is a general design structure applicable to all the basic logic gates [17].

3.5.3 The Robust and Flexible Enhancement Methodology

Ageing effects impact every transistor in integrated circuits and systems. Since transistors are under relevant bias conditions, ageing induced degradation are completely different. Some transistor nodes can be high-sensitive to ageing effects. A partitioning method is used to highlight ageing sensitivity transistors. As both HCI and NBTI effects can impact transistor threshold voltage (V_{th}), V_{th} is selected as a dominant factor to perform sensitive transistor partitioning in this work.

Traditionally, circuit over-design (robust design) can reserve additional performance margin to cope with ageing degradations. The robust design could be multi-V_{th} selection of transistors. In Figure 3.32, a conceptual flexible method is also illustrated. During ICs service life, when the ageing degraded circuit performance reach failure boundary, a monitor which is in charge of detecting performance degradation can initialize circuits to improve degraded performance. We named it as flexible ageing resilience.

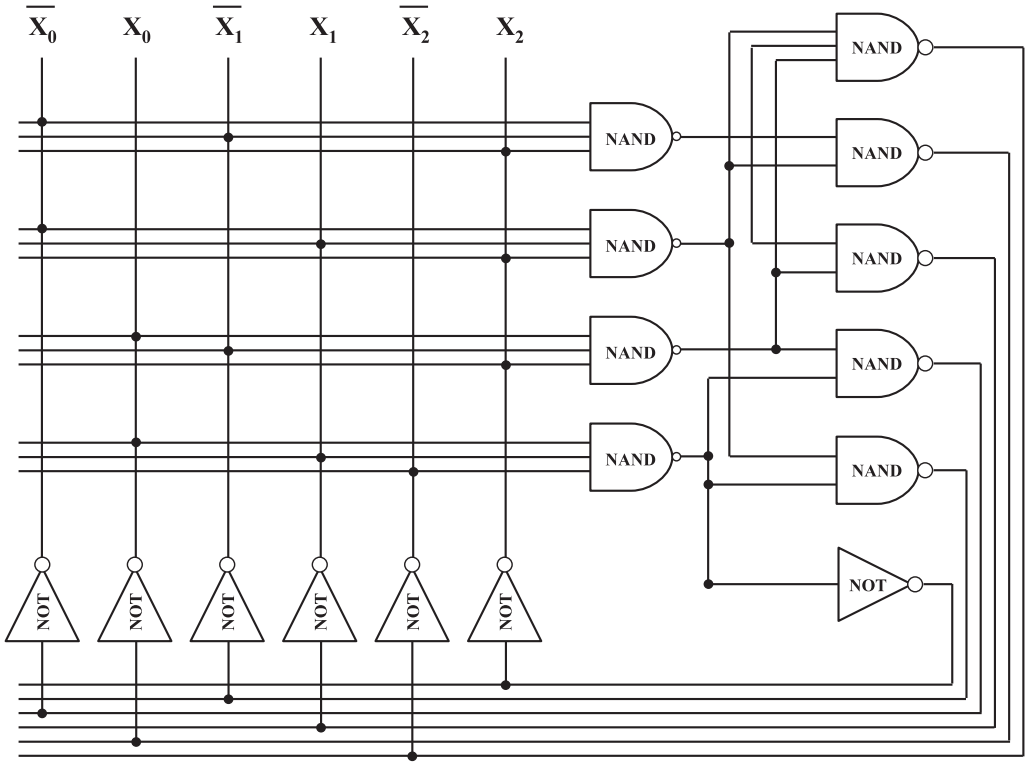


Figure 3.29: The MRF design structure applied to NAND gate.

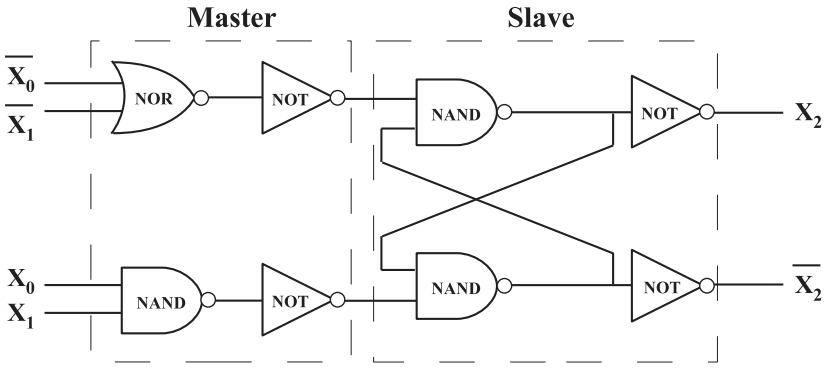


Figure 3.30: The MAS-MRF design structure applied to NAND gate.

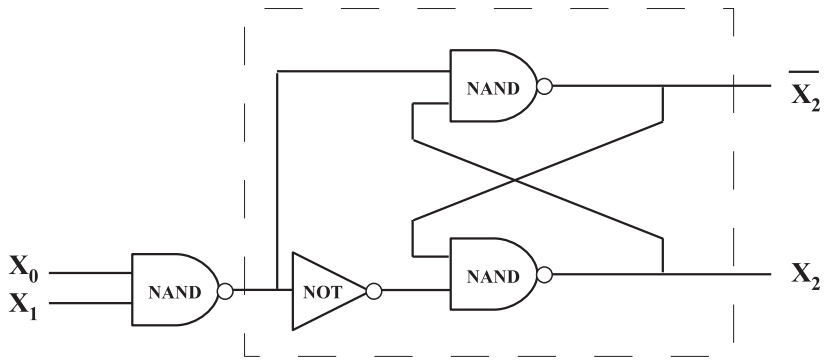


Figure 3.31: The proposed Cent-MRF circuit design for a two-input NAND gate.

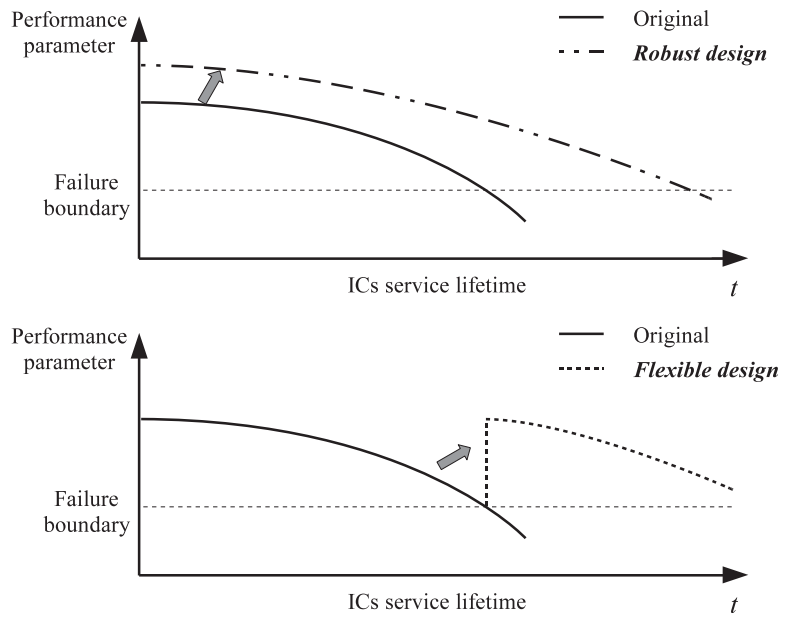


Figure 3.32: The robust and flexible method for reliability-aware design. In this paper, the robust method is executed by multi-V_{th} selection of critical transistors, the flexible one is completed by an additional ageing resilience circuit

Based on drain-source current (I_{ds}) equation in BSIM4 model, we can detect the degradation of I_{ds} in circuit,

$$I_{ds} = \frac{I_{ds0} \cdot NF}{1 + \frac{R_{ds} \cdot I_{ds0}}{V_{ds,eff}}} \cdot [1 + \frac{1}{C_{clm}}] \cdot \ln(\frac{V_A}{V_{Asat}}) \cdot \alpha \tag{3.19}$$

$$I_{ds0} = \frac{W \cdot \mu_{eff} \cdot Q_{ch0} \cdot V_{ds} \cdot (1 - \frac{V_{ds}}{2V_b})}{L \ \cdot \ (1 + \frac{V_{ds}}{E_{sat}} \cdot L)} \tag{3.20}$$

α stands for some effects, e.g., drain-induced barrier lowering (DIBL), substrate current induced body effect (SCBE) and drain-induced threshold shift (DITS). I_{ds0} is the saturation drain current, NF is the number of fingers, R_{ds} is the bias-dependent source-drain resistance, $V_{ds,eff}$ represents the effective drain-source voltage, C_{clm} is channel length modulation parameter and $V_{A,sat}$ is the early voltage at $V_{ds} = V_{ds,eff}$.

Once I_{ds} is degraded, we can increase W to compensate the degradation. Further study will be concentrated on detection-compensation circuits at transistor level.

3.5.4 The Ageing Resilience Reliability-aware Approach

An ageing resilience reliability-aware approach is proposed to alleviate HCI and NBTI induced degradations. Figure 3.33 demonstrates this approach in a flowchart. The reliability-aware approach begins with ageing simulation initialization (e.g.,ageing model selection, ageing stress duration). With ageing degradation models, after extracting fresh netlist of designed circuits, a transient analysis is performed to generate an aged circuit netlist. Nominal simulation with transient and DC analysis is performed at transistor level. In the step of reliability enhancement, if designed circuits can not meet ageing requirements, sensitivity partitioning is performed to find out high ageing sensitive transistors. Robust and flexible design are implemented to add ageing resilience to sensitive transistors.

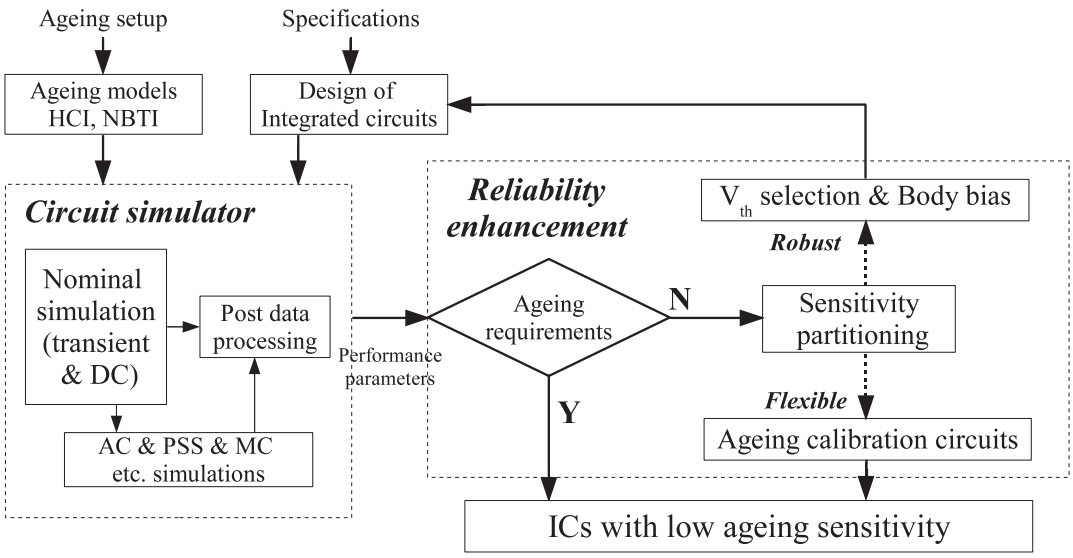


Figure 3.33: The flowchart of reliability-aware approach with sensitivity partitioning and ageing resilience

3.6 Reliability Management

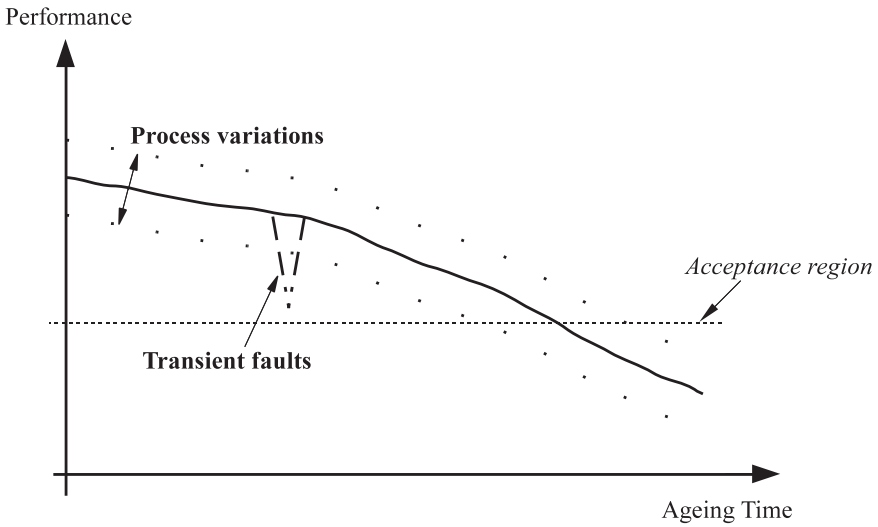


Figure 3.34: The performance degradation due to ageing mechanisms, process variations and transient faults

Reliability management is an evaluation method to ensure that the required safety margins are maintained. It has been widely applied to engineering field such as vehicle transport and nuclear power plant [112]. For reliability management of ICs, ageing mechanisms, process variations, transient faults are required to be considered in the management system. Figure 3.34 shows the performance degradation due to ageing effects, process variations and transient faults. They induce ICs malfunction and yield loss over the service lifetime.

Reliability management of ICs includes:

- Identification of reliability-critical components. The quantitative analysis can be

based either on physical degradation modeling (e.g., R-D model for HCI/NBTI mechanism) or statistical analysis of failure data (e.g., ageing simulation results).

- Prediction of reliability effects. Reliability-aware methods and approaches can be applied to reliability prediction. They can help designers to reserve reliability margins.
- Mitigation of reliability problems induced degradations. They can provide reliability design-tips (e.g., least sensitive circuit topology) to mitigate reliability influence.

Based on hierarchical reliability analysis and block failure estimation, we propose an ageing management approach which can aid circuit designer to complete reliability-aware design of large and complex AMS systems. Figure 3.35 describes the flowchart of ageing managements. AMS systems can be modeled with behavioral modeling language, e.g., Verilog-AMS. Sensitivity analysis with block failure is applied to find critical building blocks at the abstraction level.

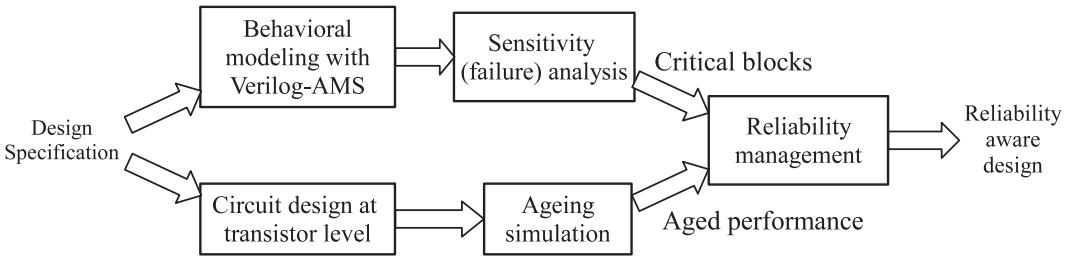


Figure 3.35: The flowchart of ageing managements with hierarchical reliability analysis and block failure estimation.

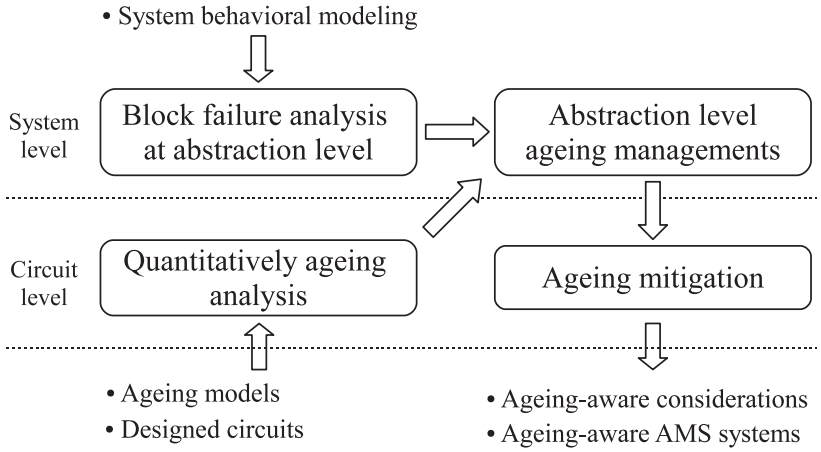


Figure 3.36: HCI and NBTI are considered as main ageing effects.

A further illumination of ageing managements is illustrated in Figure 3.36. When designed circuits are implemented with CMOS transistors, quantitatively ageing analysis is performed with ageing degradation models (e.g., NBTI and HCI mechanism models). This transient ageing simulation can provide accurate information about the stress at every circuit node. After gathering ageing performance of each building block, ageing management is performed at system (abstraction) level. Critical blocks (ageing sensitive blocks) are highlighted. In order to enhance system reliability, ageing mitigation is applied to critical blocks. A further study on ageing management is presented with $\Sigma\Delta$ modulators in Chapter 5.

3.7 Conclusion

With a review of the current reliability methodologies and tools, proper methodologies for analog circuits and AMS systems (e.g., RF front-end, Sigma-delta modulator) could be proposed from the state of arts:

- Circuit simulators such as Relxpert and Eldo can be applied in reliability-aware simulation flow.
- Based on CAD tools, Statistical reliability analysis of process variation and ageing effects achieve high efficiency.
- For large and complex AMS circuits and systems, the hierarchical flow (bottom-up) can propagate defect at transistor physical level to system level. Thus, the fluctuation and degradation of performance parameters can be evaluated.
- Reliability management of building blocks can be implemented with behavioral failure test case and reliability simulation at transistor level.

Reliability-aware methods are gathered and compared in Table 3.6, according to their features in process variations (Proc. var), ageing effects (Ageing eff.), simulation speed, simulation accuracy and the compatibility to different different technology node. As the continuously scaling down of transistor, it is important to develop proper reliability-aware methodologies which can be applied to different generations of CMOS technology. Especially for large and complex AMS circuits and systems, reliability-aware methodologies are validated in the following chapters.

Table 3.6: Comparison between reliability methodologies, in terms of process variations, ageing effects, simulation speed/accuracy and compatibility.

Methodology	Process	Ageing	Sim. speed	Sim. accuracy	Compatibility
BERT,ARET,RELY	no	yes	high	low	high
Behavioral ageing	yes	yes	high	medium	low
Monte-Carlo	yes	no	low	high	high
Corner analysis	yes	no	high	low	high
RelXpert, Eldo	no	yes	medium	medium	high
Worst case distance	yes	yes	medium	medium	low
Hierarchical	yes	yes	low	high	medium
Surrogate model	yes	yes	medium	high	low
DoEs-RSMs	yes	yes	medium	medium	medium
Sizing rules	yes	yes	low	medium	low
Pareto fronts	yes	yes	high	low	medium

∗ Compatibility is an important feature of reliability-aware methods. A method with high compatibility can apply to many types of CMOS circuits which designed with different CMOS technologies.

Chapter 4

Reliability of 65 nm CMOS Transistors and Circuits

The Chapter PIDS (Process Integration, Devices and Structures) in ITRS edition report 2011 emphasized that the reliability tradeoffs associated with new options [1]. In the near-term 2011 to 2018, reliability problems due to material, process, and structural changes, and novel applications, are important in the 65 nm era with Poly-Silicon structure. Furthermore, reliability problems such as ageing wear-out and manufacturing variability are/will be increasingly difficult to control for beyond 65 nm technology. Reliability study at 65 nm CMOS node has been launched during the last decade, e.g., transistor level study [113], AMS and RF circuits [114], [115], [116], digital circuits [117], [118] analog circuits [119], [120], [121].

In this chapter, we start reliability analysis at transistor and circuit level. Different transistor types (low, standard and high V_T) and transistor families (low power (LP) and general purpose (GP)) with 65 nm CMOS technology are evaluated. On the other hand, typical analog and mixed signal integrated circuits are reliability-aware studied. Reliability issues especially HCI and NBTI induced performance degradation are discussed with some methodologies.

4.1 Ageing Simulation Flow

Figure 4.1 illustrates Eldo reliability simulation flow used in ageing mechanism analysis [68]. Eldo provides HCI and NBTI degradation models. The simulation starts with ageing modeling selection and ageing duration setup. With an initialization of transient analysis, the stress on each transistor over a transient time is determined. Aged netlist which contains degraded information is generated. After, aged circuit performance can be evaluated by DC, AC, PSS (periodic steady-state), Monte-Carlo and noise analysis in analog environment. The simulator provides both fresh (ideal) and aged circuit performances, which can be visualized in software EZwave (Mentor Graphic).

4.2 Transistor Level

A 65nm CMOS technology platform is used throughout the simulation work in this report. In general, there are three transistors families: general purpose (GP), low power (LP) and high performance (HP). These options are typically distinguished from each other based on transistor physical parameters (V_{th}, T_{ox}, L_{eff} etc.). In every family, the library provides three types of transistors with different threshold voltage. Low V_T type represents low threshold voltage, which can achieve high speed. High V_T type with high threshold voltage

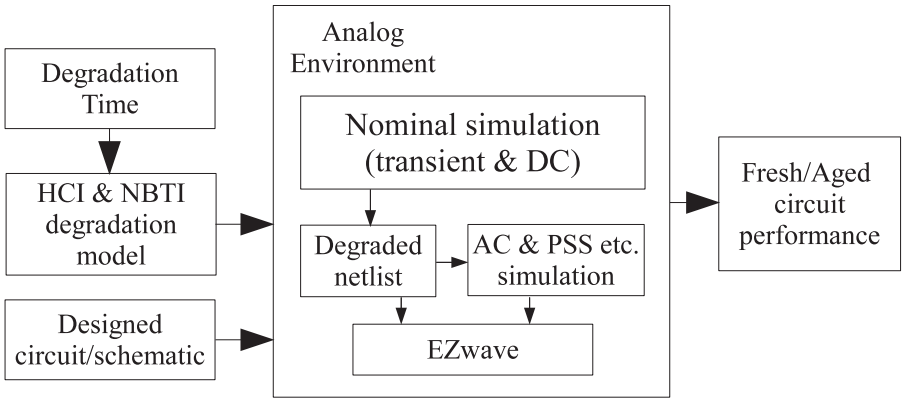


Figure 4.1: Nominal reliability simulation method with transient simulation. The reliability simulator Eldo contains ageing mechanism models. Circuit simulation is performed in analog environment.

can reduce leakage current. Standard V_T type is the standard type with compromise performance.

4.2.1 HCI and NBTI sensitivity of BSIM 4 parameters

With 65 nm CMOS design-kit, the transistor type $nsvtlp$ (low power NMOS with standard V_{TH}) is studied. The transistor dimension is set to $W = 0.36\ \mu m$, $L = 0.06\ \mu m$, where L is minimum transistor length. At physical level, ageing effects can degrade some BSIM4 parameters and influence the transistor performance [12]. The degradation of physical parameters are highly dependent on the transistor ageing duration time.

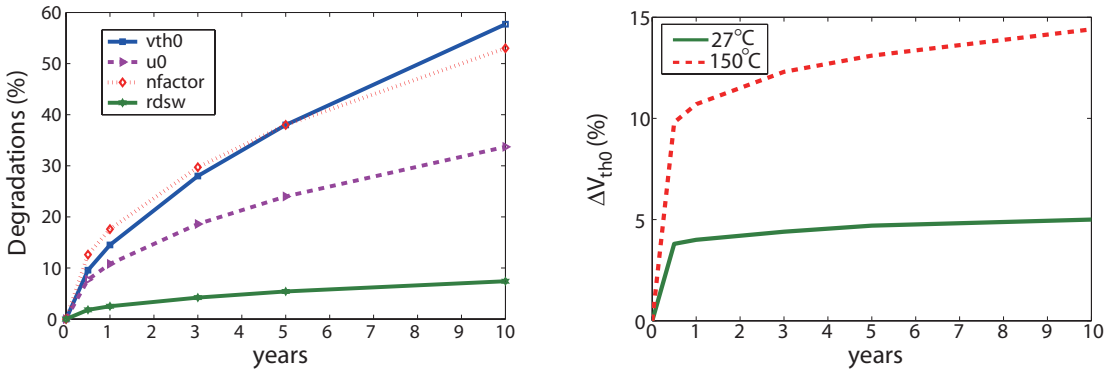
As shown in Figure 4.2(a), HCI can influence sub-threshold swing coefficient (n_{fac}), intrinsic threshold voltage (v_{th0}), intrinsic mobility (μ_0), saturation velocity (v_{sat}), drain source resistance per width (r_{dsw}), subthreshold region DIBL coefficient (eta_0) and threshold voltage offset (v_{off}). The correlation analysis is used to filter out some correlated parameter. v_{th0}, μ_0, n_{fac} and r_{dsw} are selected as the main degraded parameters of NMOS transistor. Besides, the only BSIM4 parameter affected by NBTI is v_{th0} of PMOS transistor (see Figure 4.2(b)). More severe v_{th0} degradation is observed when PMOS transistor work at high temperature ($150°C$).

We select one year ageing time as an example point. As shown in Figure 4.2(a) and Figure 4.2(b), since from t_0 (fresh) to one year, the degradation is more severe than the later periods (e.g., ageing degradation from one year to two years).

In Table 4.1, these BSIM4 parameters are sorted out as ageing sensitive and non-sensitive. In NMOS transistor, the dominant ageing nonsensitive BSIM4 parameters include: length variation (x_l), width variation (x_w), gate oxide thickness (t_{ox}) and channel doping concentration (n_{dep}). In PMOS transistor, except v_{th0}, other parameters mentioned above are ageing non-sensitive.

Table 4.1: HCI and NBTI sensitivity of BSIM4 parameters. Ageing effects degrade sensitive physical parameters

Mechanism	Ageing sensitive	Ageing non-sensitive
HCI	v_{th0}, u_0, n_{fac}, r_{dsw}	x_l, x_w, t_{ox}, n_{dep}
NBTI	v_{th0}	u_0, n_{fac}, r_{dsw}, x_l, x_w, t_{ox}, n_{dep}



(a) HCI effect to NMOS (b) NBTI effect to PMOS

Figure 4.2: HCI and NBTI induced physical parameters degradation in NMOS and PMOS transistor.

After, degraded physical parameters affect transistor performance. Transistor parameter such as drain current I_{ds} and V_{th} are influenced. They are modeled with the analytic equations in BSIM model [88]:

$$V_{TH} = V_{th0} + \gamma(\sqrt{\Phi_s - V_{BS}} - \sqrt{\Phi_s}) \tag{4.1}$$

where γ is the body bias coefficient, V_{BS} is the substrate bias voltage, Φ_s is the Fermi level.

$$\begin{aligned} I_{ds} = & \frac{I_{ds0} \cdot NF}{1 + \frac{R_{ds} I_{ds0}}{V_{ds,eff}}} \cdot [1 + \frac{1}{C_{clm}}] \cdot \ln(\frac{V_A}{V_{Asat}}) \cdot (1 + \frac{V_{ds} - V_{ds,eff}}{V_{A,dibl}}) \cdot \\ & (1 + \frac{V_{ds} - V_{ds,eff}}{V_{A,dits}}) \cdot (1 + \frac{V_{ds} - V_{ds,eff}}{V_{A,scbe}}) \end{aligned} \tag{4.2}$$

where NF is the number of device fingers, I_{ds0} is the saturation drain current, C_{clm} is the channel length modulation parameter, V_{Asat} is the early voltage at $V_{ds} = V_{dsat}$. $V_{A,dibl}$, $V_{A,dits}$, $V_{A,scbe}$ stands for the early voltage due to drain-induced barrier lowering (DIBL), drain-induced threshold shift (DITS) by pocket implant, substrate current induced body effect (SCBE), respectively. All the other parameters can also be built with analytic equations effectively [88].

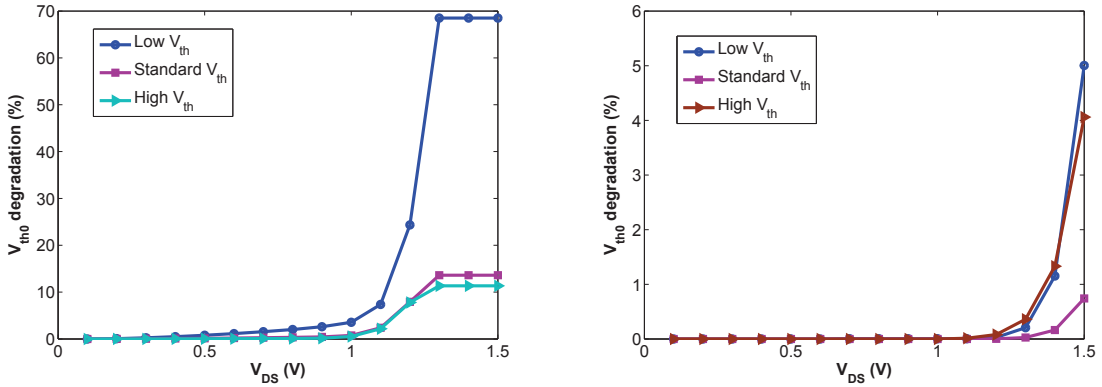
4.2.2 Ageing Study of Transistor Family

Based on 65 nm CMOS technology design kit, we perform one year ageing simulation at 27°C room temperature, respectively on the low, standard and high V_{TH} transistor model in both LP and GP transistor families. HCI and NBTI are considered as the main ageing effects. Figure 4.3(a), 4.3(b) show HCI induced V_{th0} degradation in single NMOS transistors. Figure 4.4(a), 4.4(b) show NBTI caused V_{th0} degradation in single PMOS transistors. In Figure 4.5(a), 4.5(b), we compare the aged transistor performance of LP and GP transistors.

4.3 Circuit Level

4.3.1 Ageing study of CMOS inverter

NBTI study of simple circuits can be performed with ELDO simulator. The non-linear shift of V_T can change transistor characteristics. In a simple CMOS inverter, NBTI induced



(a) W/L = 0.36/0.06 ($\mu m/\mu m$) (b) W/L = 10/0.5 ($\mu m/\mu m$)

Figure 4.3: One year HCI induced V_{th0} degradation in single NMOS transistors. HCI has strong dependence on transistor length, but independence on transistor width. Low V_{th} transistors are more sensitive to HCI, especially with minimum dimension. The degradation degree is related to transistor bias condition (V_{GS} and V_{DS}). The discontinuity of degradation in left figure is due to V_{th0} limitation 65 nm transistors.

V_T shift mainly influences '0' to '1' transition time (see Figure 4.6). Meanwhile, the skew at '1' to '0' transition can be neglected because the skew (τ_1) is considerably lower compared with '0' to '1' skew (τ_2).

Table 4.2 shows the NBTI induced skew of inverter under one year NBTI effect. Figure 4.4(a) shows that high V_T transistor model has relatively smaller V_T degradation. In contrast with the single PMOS transistor, the inverter with high V_T model is the most sensitive to NBTI, which manifests itself as additional change of both pulse width and pulse position (clock skew). The skew is worse with smaller width and larger length. Here, the characteristics of frequency independent in NBTI mechanism should be reviewed. Thus, the skew is more critical when inputing higher frequency signal to inverter because the clock skew has relatively higher error proportion.

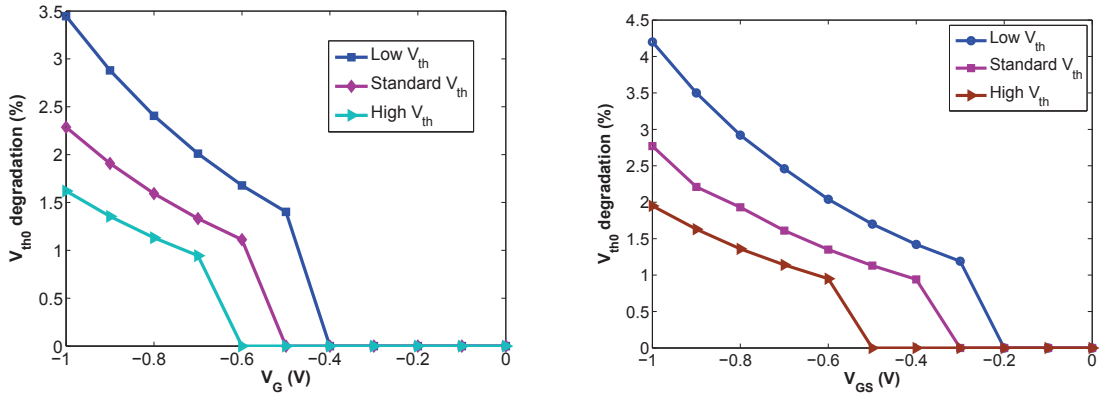
Table 4.2: One year NBTI induced clock skew. We select one year ageing time as an example point. Since from t_0 (fresh) to one year, the degradation is much more severe than other time periods (e.g., ageing degradation from one year to two years, see Figure 4.2a and 4.2b). Results show the worst-case skew with the non-monotonic characteristic. The average skew could be monotonic.

length / width	low V_t		standard V_t		high V_t	
	0.06	0.36	0.06	0.36	0.06	0.36
0.5 μm	46.36	116.8	38.4	329.2	65.3	567.6
0.72 μm	18.0	148.6	48.7	191.4	54.8	736.1
0.9 μm	16.7	138.5	46.7	163.2	51.5	411.3
1.44 μm	16.1	49.4	22.0	140.7	51.4	389.7

'0' to '1' skew, time unit in femto-second (fs)

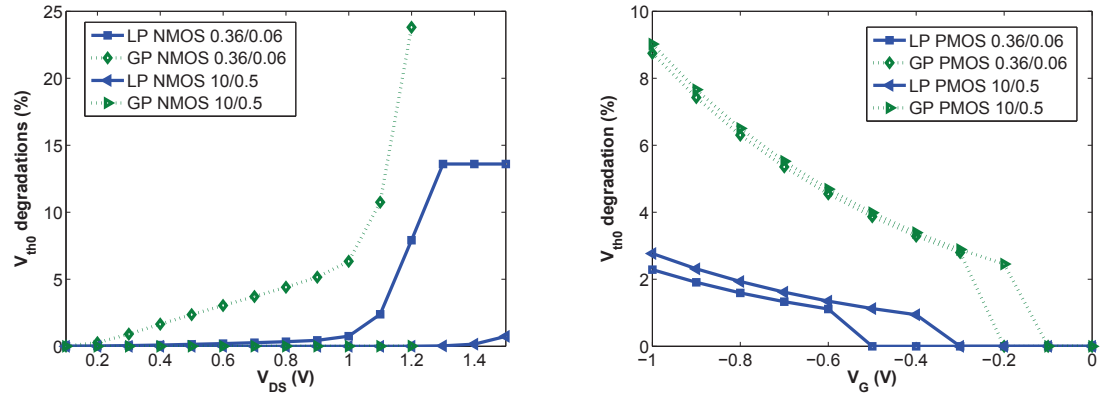
4.3.2 A study of Pareto method with Miller Op-amp

Traditionally, the variability of circuits and systems are performed by corner analysis or Monte-Carlo simulation. Figure 4.7 illustrates the performance variations of a 65 nm



(a) W/L = 0.36/0.06 ($\mu m/\mu m$) (b) W/L = 10/0.5 ($\mu m/\mu m$)

Figure 4.4: One year NBTI caused V_{th0} degradation in single PMOS transistors. NBTI effects is length independence and weak width dependence. NBTI risk: $lvt > svt > hvt$. The degradation degree are related to transistor bias conditions.



(a) One year ageing of HCI (b) One year ageing of NBTI

Figure 4.5: Aged transistor performance of LP and GP transistors. GP family transistors are more sensitive to HCI (NMOS) and NBTI (PMOS) than their LP counterparts.

Miller Op-amp.

The Pareto reliability-aware approach in last chapter is implemented to analyze a two-stage miller operation amplifier (see Figure 4.8). It aims to:

- use worst-case Pareto front to generate a performance set considering ageing effects and process variations.
- evaluate worst-case analogue circuit performance with statistical methods.

BSIM4 transistor physical parameters are investigated. With correlation analysis and regression analysis [12], we filter out uncorrelated BSIM4 parameters and find out dominant parameters. Five dominant BSIM4 process parameters are selected: intrinsic threshold voltage (v_{th0}), intrinsic mobility (μ_0), length variation (x_l), gate oxide thickness (t_{ox}) and channel doping concentration (n_{dep}).

Firstly, initial setups are needed for ageing model (exists in [68]) selection and ageing duration time. In the step of DoEs, a five factor Box-Behnken design is generated (to replace MC simulation). Then, circuit simulation is performed for ideal and aged circuit performances. In order to evaluate the degraded performance of circuits under ageing

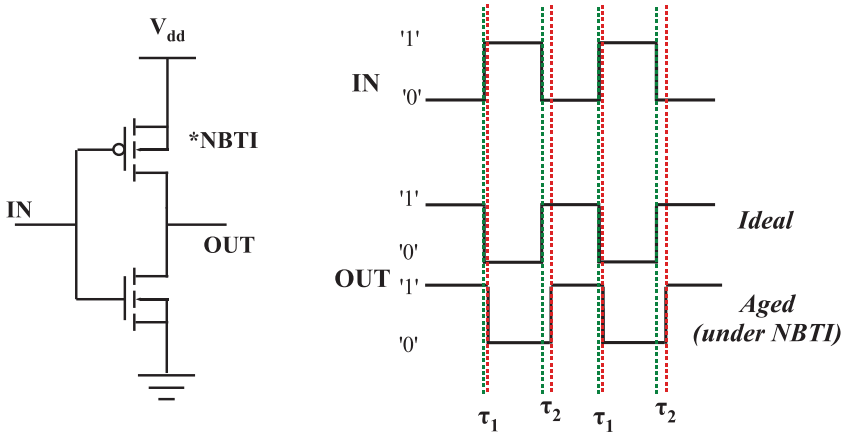


Figure 4.6: Inverter and its degradation under NBTI, τ_1 stands for '1' to '0' skew; τ_2 for '0' to '1' skew.

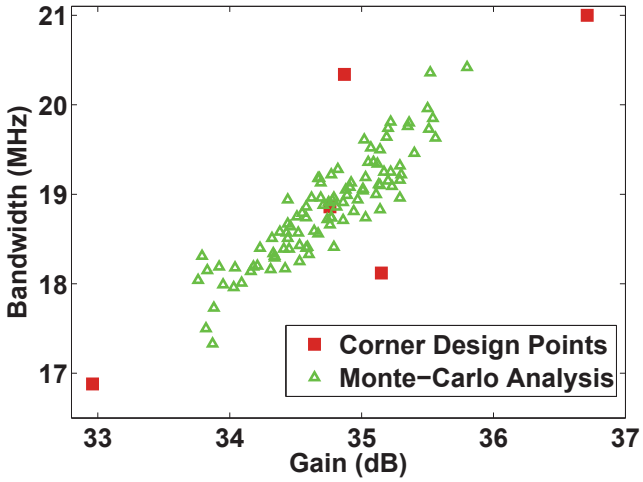


Figure 4.7: 100 runs MC and corner analysis of a 65 nm Miller Op-amp (performance parameters: DC gain and gain-bandwidth (GBW)).

effects and process variations, multi-objective (consider different performance parameters) worst-case Pareto fronts are generated by non-dominated sorting evolution.

Table 4.3 shows the detailed circuit parameter and transistor dimension. Transistor length is selected as 0.3 μm in order to satisfy minimum requirement of 65 nm analogue integrated circuit.

In CMOS 65nm and less scaled technology, although the gain bandwidth (BW) is highly improved with the scaling down, it becomes difficult to design Op-amp with high gain and safety phase margin (PM). In these study case, the above-mentioned performance parameters of Op-Amp will be examined.

We consider HCI (for NMOS transistor) and NBTI (for PMOS transistor) as main ageing effects. Reliability simulation is performed with ELDO [68]. The case study is executed on a dual-quad core 2.8 GHz Intel Xeon processor with 4 GB RAM. The range of process parameters variation are setup as follow: $\Delta v_{th0} = \pm 12$ %, $\Delta \mu_0 = \pm 6$ %, $\Delta x_l = \pm 20$ %, $\Delta t_{ox} = \pm 6$ %, $\delta n_{dep} = \pm 6$ %. The parameter variation ranges selection above is based on [91] [92], which particularly on variability of 65 nm nodes.

As a case study of ageing and process variations, performance parameters and transistor dimension have not been optimized. Pareto fronts can be generated with either

Table 4.3: Transistor dimension for Figure 4.8, L = 0.3 μm for all transistors

Circuit parameters	Transistor dimension (width/length μm)
$V_{dd} = 1.2\ V$	M1/M2 = 5/0.3
Temperature = 27 °C	M3/M4 = 18/0.3
$I_{bias} = 20\ nA$	M5 = 11.25/0.3
$V_{in} = 500\ mV$	M6 = 22.5/0.3
$C_L = 1\ pf$	M7 = 50/0.3
$C_{miller} = 2\ pf$	M8 = 15/0.3
ageing time = 1 year	M9 = 3/0.3

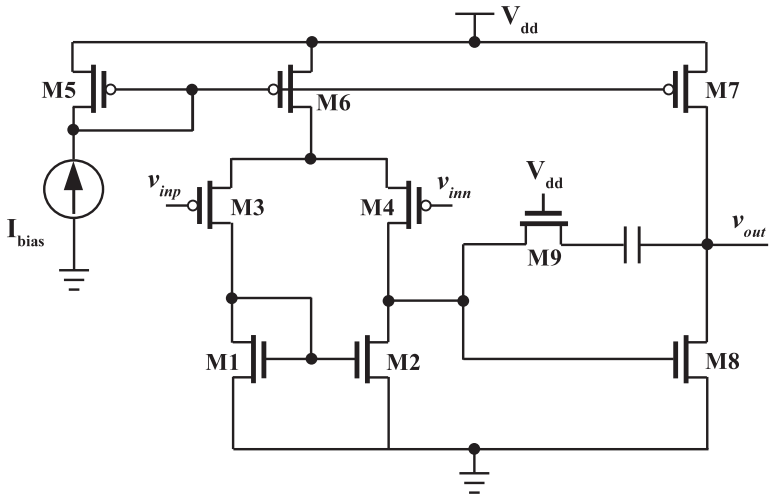


Figure 4.8: Schematic view of a two stage Miller op-amp

MC method or statistical method (in this proposed approach). In order to compare this approach with traditional MC method, a 200 runs MC simulation is implemented as a test case.

Figure 4.9 shows that NMOS transistors in this op-amp are immune to HCI degradation, while PMOS transistors suffer from NBTI degradation. The degradation of threshold voltage (v_{th}) of transistor M5, M6 and M7 belong to PMOS current source is 2.6%, 2.7% and 2.8% separately. Table 4.4 lists the nominal and corner-based simulation performance of this Op-Amp. Comparing with MC simulation result (see Figure 4.10), corner-based simulations have over-estimated the worst-case of circuit performance under one year ageing degradation.

With this approach, worst-case Pareto points has been generated as a set of non-dominated solutions. Figure 4.11 shows both ideal and aged Pareto fronts which are generated by proposed approach. Table 4.5 shows some solutions in the worst-case Pareto set, with worst-case gain, bandwidth and phase margin separately.

Trade-offs exist among simulation speed, memory usage and simulation accuracy. The occupied memory is nearly 15% of a standard 200 runs MC analysis. The MC analysis lasts 3.5 minutes, whereas the proposed approach takes only 1.2 minutes. The accuracy of statistically modeled Pareto worst-case front is evaluated by comparing with another Pareto worst-case front which is generated from a standard 200 runs MC simulation (see Figure 4.10, projections from three-dimensional Figure 4.11). The RMSEs are varied from 0.05% to 1.7% over three different performance ($RMSE_{BW} > RMSE_{gain} > RMSE_{PM}$).

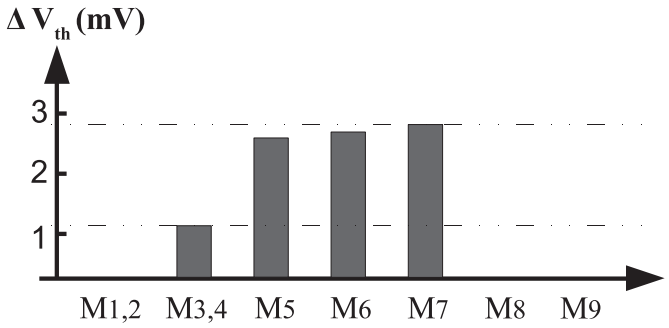


Figure 4.9: Ageing induced V_{th} degradation of every transistor. PMOS transistors suffer from NBTI induced degradation.

Table 4.4: Nominal and corner-based simulation performance: ideal and aged (1 year)

	Gain (dB)	BW (MHz)	PM (degree)
Nominal (ideal)	34.76	18.86	80.52
corner (ideal SS)	-5.2%	-10.5%	+2.1%
corner (ideal FF)	+5.6%	+11.3%	-1.9%
Nominal (aged)	32.36 (-6.9%)	17.63 (-6.5%)	81.01 (+0.6%)
corner (aged SS)	-11.7%	-17.0%	+2.7%
corner (aged FF)	-2.7%	+4.0%	-1.2%

As shown in Figure 4.10, due to the selected range of process parameters, the feasible region of statistical modeled Pareto front is larger than MC simulation generated Pareto fronts. Better approximation to MC simulation can be achieved through adjusting the range of process parameters.

4.3.3 NBTI Induced Degradation in Clock Distributors

Ageing mechanisms can cause clock uncertainty in clock circuits. Chacraborty *et al.* highlighted NBTI induced clock skew can increase by up-to 7x in gating enabled clock trees [122]. Recently, a new viewpoint of stochastic NBTI has been proposed in [123], inverters under NBTI can generate ageing-independent jitters due to random telegraph noise (RTN). Figure 4.12 illustrates the pulse width (PW) error and pulse position (PP) error. These uncertainties can be either deterministic skew or stochastic jitter [124] [125]. Both skew and jitter are the time-deviation of the clock transitions with respect to the ideal clock [126]. Skew is always a fixed constant from cycle to cycle, whereas jitter is typically subject to normal distribution and it can change quickly from cycle-to-cycle or

Table 4.5: One year aged performance, estimated by proposed model (example from worst-case Pareto front)

	Gain (dB)	BW (MHz)	PM (degree)
Worst Gain	**31.26** (-10.1%)	15.97	82.63
Worst BW	31.27	**15.95** (-15.4%)	82.53
Worst PM	33.79	19.52	**79.53** (-1.2%)

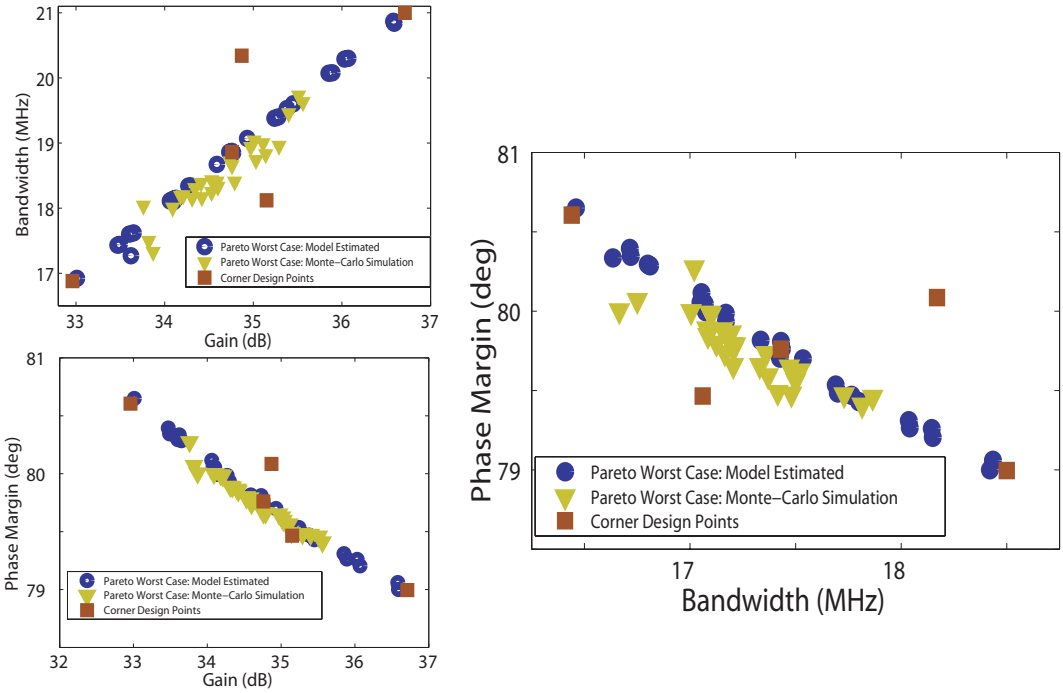


Figure 4.10: Pareto front: simulation of gain, bandwidth and phase margin.

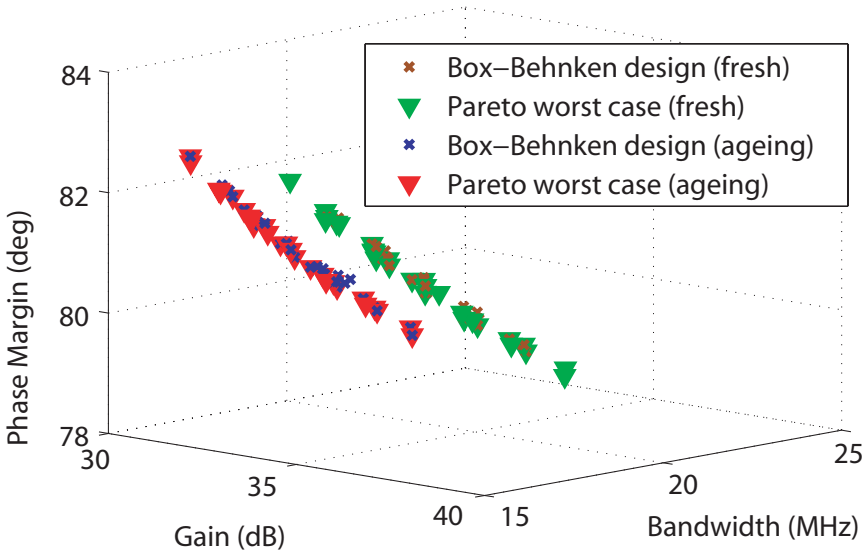


Figure 4.11: Ideal and aged worst-case Pareto front, estimated by proposed model

slowly over many clock cycles [125]. The appearance of skew and jitter is usually caused by on-die process-voltage-temperature (PVT) variations, PLL jitter and crosstalk. Jitter is always harmful but sometimes skew could be beneficial [125].

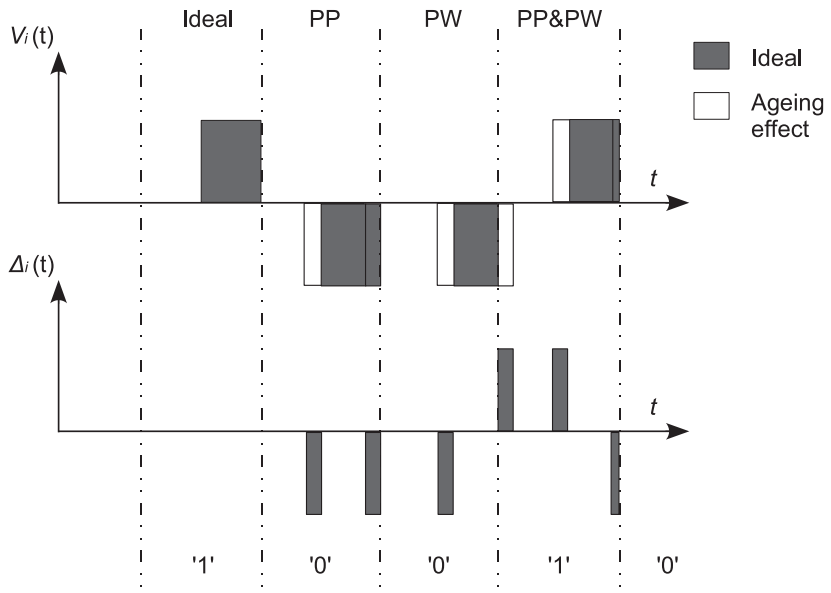


Figure 4.12: PW and PP error induced by ageing effects

The non-overlapping clock distributor can be used in clock distribution network. Figure 4.13 depicts the block diagram of a two phase non-overlapping clock distributor in a 65 nm CMOS process. It consists of an input buffer, two D-flip flops (DFF) and several delay blocks. Pulse signal Clk_0 and Clk_{90} are generated by the inverter chain with feedback, from a sinusoidal input waveform.

Figure 4.14 shows the simulation results. With a sinusoid signal input, a square wave signal with different phases can be generated.

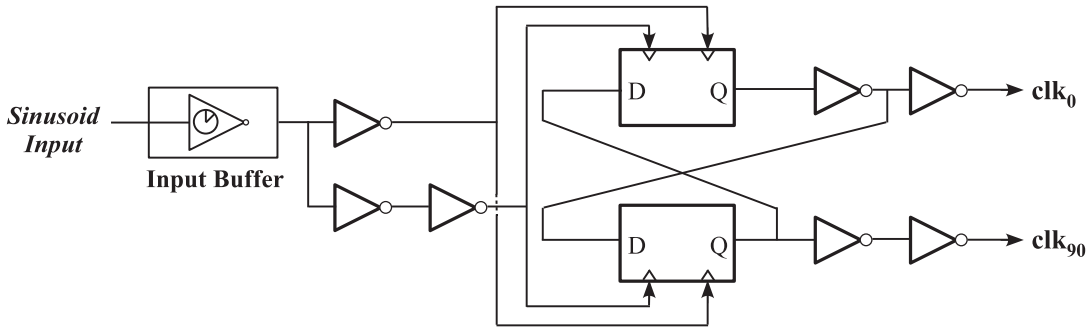


Figure 4.13: Block diagram of clock distributor

After normal simulation, Ageing simulation is performed to evaluate degraded performance of this clock distributor. Both HCI and NBTI can cause clock uncertainty. Quantitatively, HCI induced clock skew is less than 1/100 of NBTI. Thus, only NBTI mechanism is primarily concerned.

This clock distributor can be implemented with three different types of transistor models: high V_T, standard V_T and low V_T. NBTI reliability simulation is performed with a 4 MHz input signal. When distributor circuit is implemented with high V_T transistor, clock uncertainty is shown in Figure 4.15. A hypothesis testing is made with Kolmogonov-Smihnov (K-S) test [127] at a significance level of 0.05. The hypothesis results illustrate

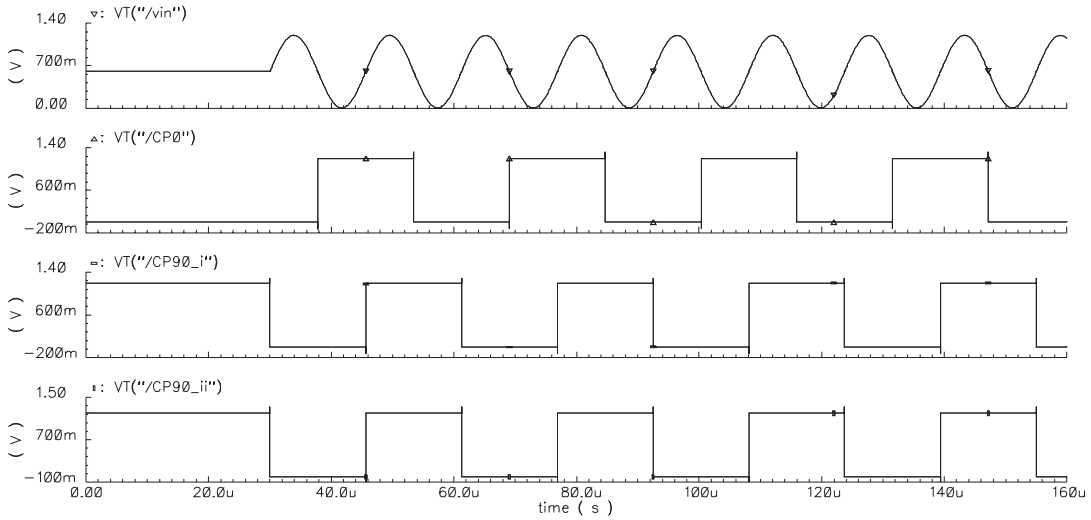


Figure 4.14: Simulation results of the designed clock distributor.

that four groups of data (clock uncertainties under 1, 3, 6 and 10 years NBTI) in Figure 4.15 are subject to normal distribution. Thus, for high V_T case, clock uncertainty manifest itself as clock jitter. Table 4.6 gives the mean and standard deviation value. In order to have an intuitionistic visual view, Figure 4.16 re-plots the distribution according to Table 4.6. Theoretically, NBTI is a time-dependent ageing mechanism. NBTI induced degradation are proportional to the time. It is shown that NBTI induced jitter is independent to ageing duration time. For instance, one year NBTI caused clock jitter is similar to ten years case with a standard deviation around 20ps under 4 MHz clock frequency.

Table 4.6: Mean and standard deviation of NBTI induced jitters with high V_T model.

NBTI ageing time	Mean $(\mu)(ps)$	Std. dev. $(\sigma)(ps)$
YEAR 1	3.071	22.768
YEAR 3	5.203	21.43
YEAR 6	3.615	19.937
YEAR 10	6.578	19.527

Standard V_T and low V_T models are also evaluated under NBTI effect. Otherwise from induced jitter in high V_T model, clock distributor with standard V_T and low V_T model show clock uncertainties as a periodic clock skew under NBTI. Both '0' to '1' and '1' to '0' skew is calculated. The NBTI skew in standard V_T model is slightly more complicated than low V_T because its cycle period is twice of low V_T model (see Table 4.7).

Table 4.6 and Table 4.7 show that 65 nm designed clock distributor with different V_T transistor model suffers from the NBTI degradation. Under the worst-case condition, the sequence of NBTI induced degradation degree is: high V_T model > standard V_T model > low V_T model. In high V_T transistor model, we suppose that the jitter source is from NBTI induced skew which is accumulated through many clock stages in distributor circuit. The fixed skew from one clock stage can be varied by switching activity. Low V_T and standard V_T model have a faster switch speed in clock circuit thereby under NBTI, they can avoid this jitter problem.

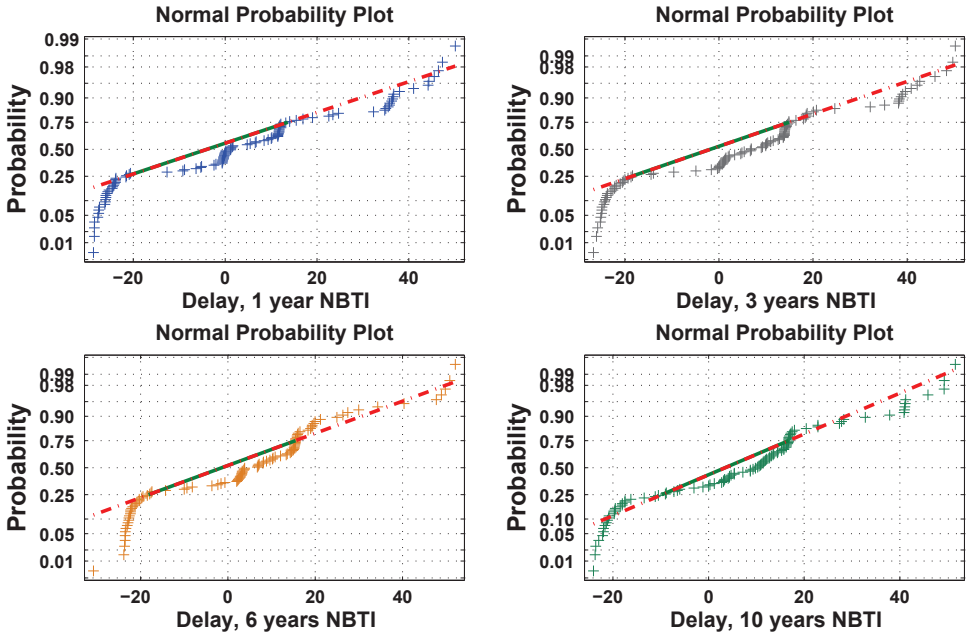


Figure 4.15: Clock uncertainties and data probability density under one, three, six and ten years of NBTI mechanism. The dashed line in each sub-figure represents standard normal distribution. The distributions of NBTI induced clock uncertainties follow the standard normal distribution.

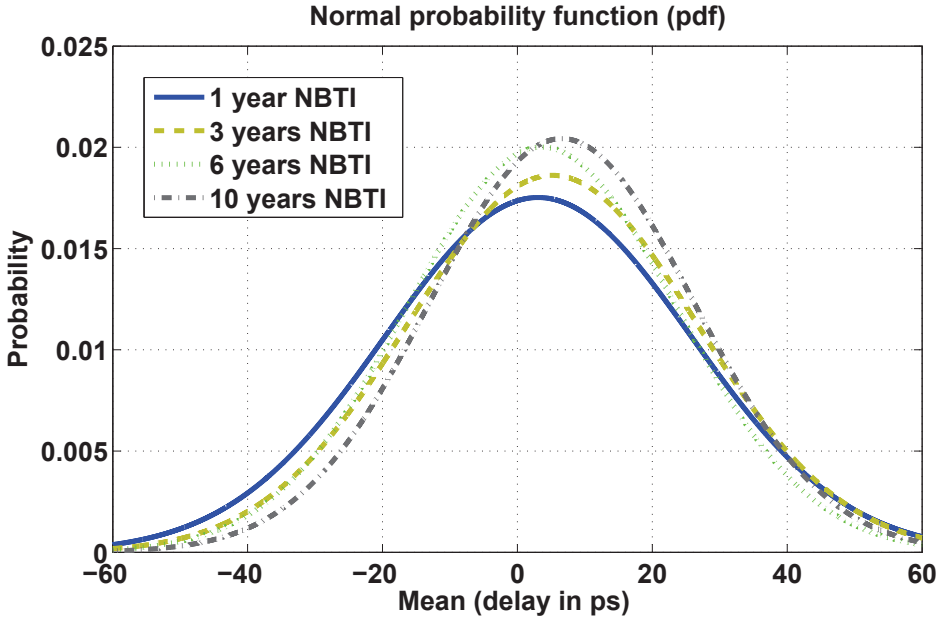


Figure 4.16: Time-independent NBTI induced jitters distribution. It is worth to notice that NBTI induced jitter is independent to ageing duration time in the clock distributor designed with 65 nm CMOS technology.

Table 4.7: NBTI induced periodic clock skew with standard and low V_T transistor model, time unit in ps (t_1, t_3 for '1' to '0' skew and t_2, t_4 for '0' to '1' skew). The cycle period of standard V_T model is 2 times of low V_T model.

	T	YEAR 1	YEAR 3	YEAR 6	YEAR 10
Std. V_T	t_1	-0.153	0.76	0.86	0.95
	t_2	1.62	1.77	1.85	1.94
	t_3	-0.56	0.39	0.47	0.55
	t_4	5.23	5.4	5.46	5.55
Low V_T	t_1	-4.0	-4.35	-4.48	-4.65
	t_2	-3.48	-3.44	-3.48	-3.5

4.3.4 Process Variation Analysis of Folded Cascode Op-amp

The DoE-RSM Methodology illustrated in Chapter 3 is applied to a 65 nm one stage folded cascode op-amp (schematic view is shown in Figure 5.16). The circumscribed type central composite design allocates the response distribution of process parameter. As show in Table 4.8, 15 different BSIM4 parameters have been screened out. DC and AC simulation is performed on single transistor. With Plackett Burman design (see Table 4.8), Table 4.9 and 4.10 illustrates the result of stepwise regression analysis with F-statistical model with entrance and exit tolerances p value 0.05 and 0.1 respectively (default values). The impact degree of process variation to performance is sorted by serial numbers, where v_{tho} and x_l have the highest impact on circuit performance. Consideration should also be given to process parameters such as u_0, x_w, n_{dep} and t_{oxe}.

Figure 4.17 shows the response surface modeling which reflects BSIM4 parameters V_{th0} (threshold voltage variation) and X_l (length variation) to circuit performance DC gain. We can evaluate the performance distribution according to process variation. This methodology can be extended to high system level to predict the system performance and calculate yield.

4.3.5 Statistical Co-evaluation of Current Mirror and Comparator

The statistical co-evaluation methodology is proposed in Chapter 3 (see Figure 3.22). The simple current mirrors (NMOS and PMOS type) and dynamic comparator are implemented with 65nm CMOS process technology to have experimental studies of the methodology. Minimum transistor dimension is used. Reliability simulation is performed with ELDO simulator (maximum ageing time = 20 years). HCI and NBTI are considered as the main ageing effects. The statistical flow is carried out with Matlab statistics toolbox [128]. Circuit process variation analysis is based on BSIM4 transistor model.

Figure 4.18 shows the schematic view of the dynamic comparator. In this application, the comparator should change its state when the positive and negative input voltages are equal to each other. According to this, we modify the classical resistive divider comparator to this simpler version. The operation principle of the comparator is as follows. When the clock signal is low, the comparator is in reset mode. M3 and M4 are cut off, so there is no current path existing between the voltage supplies. M9 and M10 pull both outputs to V_{dd} by charging the capacitance at the output node, meanwhile M7 and M8 are cut off and M5 and M6 are conducting. When the comparator is latched by the clock signal, it works in the regeneration mode. M3 and M4 immediately conduct at clock edge. If the current in the left branch is larger than that of the right one, *voutn* is discharged to 0 V earlier and at the same time M6 is cut off and M8 is conducting, which pulls *voutp* to V_{dd}.

Table 4.8: The Plackett Burman design for factor screening analysis in statistical flow: 15 two-level factors (BSIM4 physical parameters) for 16 simulation runs. Plus signs (+) represent process parameters with maximum values (upper range); minus signs (-) for minimum values (lower range)

	t_{ox}	n_{dep}	r_{sh}	r_{shg}	v_{tho}	u_0	n_f	r_{dsw}	c_f	x_l	x_w	jsw	c_j	c_{jsw}	c_{jg}
1	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
2	-	+	-	+	-	+	-	+	-	+	-	+	-	+	-
3	+	-	-	+	+	-	-	+	+	-	-	+	+	-	-
4	-	-	+	+	-	-	+	+	-	-	+	+	-	-	+
5	+	+	+	-	-	-	-	+	+	+	+	-	-	-	-
6	-	+	-	-	+	-	+	+	-	+	-	-	+	-	+
7	+	-	-	-	-	+	+	+	+	-	-	-	-	+	+
8	-	-	+	-	+	+	-	+	-	-	+	-	+	+	-
9	+	+	+	+	+	+	+	-	-	-	-	-	-	-	-
10	-	+	-	+	-	+	-	-	+	-	+	-	+	-	+
11	+	-	-	+	+	-	-	-	-	+	+	-	-	+	+
12	-	-	+	+	-	-	+	-	+	+	-	-	+	+	-
13	+	+	+	-	-	-	-	-	-	-	-	+	+	+	+
14	-	+	-	-	+	-	+	-	+	-	+	+	-	+	-
15	+	-	-	-	-	+	+	-	-	+	+	+	+	-	-
16	-	-	+	-	+	+	-	-	+	+	-	+	-	-	+

t_{ox}: t_{oxe}, electrical gate equivalent oxide thickness

n_{dep}: Channel doping concentration at depletion edge for zero body bias

r_{sh}: Source/drain sheet resistance

r_{shg}: Gate electrode sheet resistance

v_{tho}: Threshold voltage at v_{bs}=0 for long-channel devices

u_0: Low-field surface mobility at tnom

n_f: n_{factor}, subthreshold swing coefficient

r_{dsw}: Zero bias LDD resistance per unit width for RDSMOD=0

c_f: Fringing field capacitance

x_l: Length variation due to masking and etching

x_w: Width variation due to masking and etching

jsw: $jsws$, isolation-edge sidewall source junction reverse saturation current density

c_j: Zero bias bottom junction capacitance per unit area.

c_{jsw}: Sidewall junction capacitance per unit periphery.

c_{jg}: c_{jswg}, gate-side junction capacitance per unit width.

Table 4.9: BSIM4 parameters selection based on DC analysis of a 65 nm one stage folded cascode op-amp. The sequence of BSIM 4 parameters is determined by weight value from regression analysis.

	1	2	3	4	5	6	7	8
I_d	x_l	v_{tho}	u_0	x_w	t_{oxe}	r_{dsw}	n_{dep}	
V_{th}	v_{tho}	x_l	n_{dep}	t_{oxe}	x_w	r_{dsw}	r_{sh}	c_f
g_m	u_0	x_l	r_{dsw}	x_w	v_{tho}	t_{oxe}	t_{oxe}	

Table 4.10: BSIM4 parameters selection based on AC analysis of a 65 nm one stage folded cascode op-amp. Performance parameters (DC gain and gain-bandwidth) are evaluated. The sequence of BSIM 4 physical parameters is determined by weight value from regression analysis. Three physical parameters are highly concerned: v_{tho}, x_l and u_0.

	1	2	3	4
A_0	v_{tho}	x_l	u_0	c_{jswg}
GBW	x_l	v_{tho}	u_0	t_{oxe}

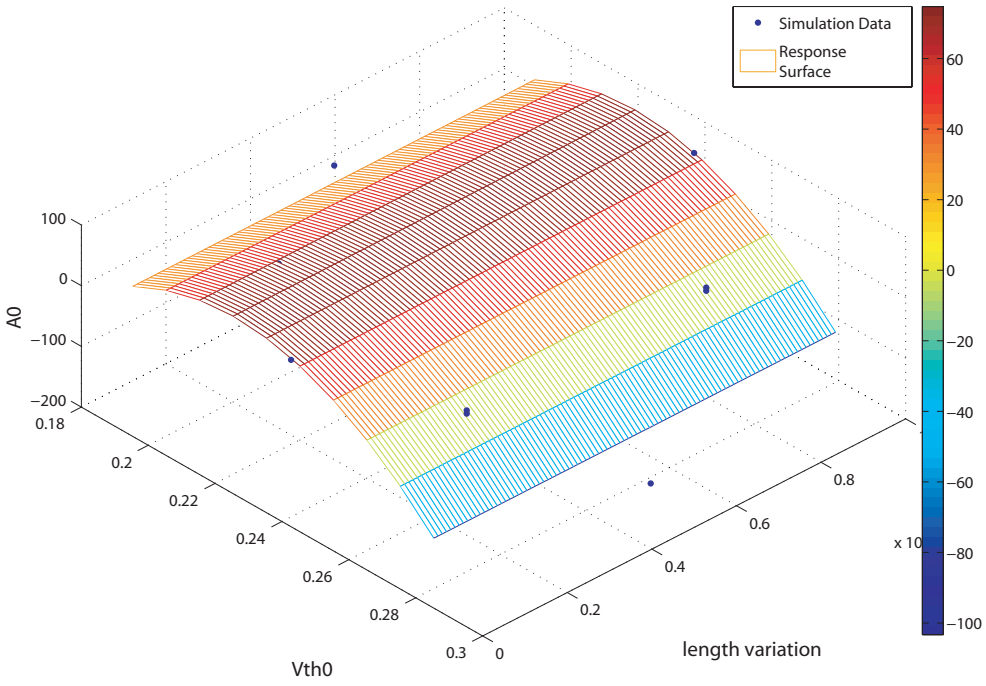


Figure 4.17: Using response surface model to study variations in a 65 nm one stage folded cascode op-amp: reflecting BSIM4 parameters V_{th0} (threshold voltage, standard value: 0.23972 V) and X_l (length variation due to masking and etching, standard value $5 * 10^{-9}$ m) to circuit performance DC gain. In this figure, the simulation point (data) is evaluated by central composite designs (CCD), which is a typical type in DoEs. The quadratic model is applied to implement this response surface. Further study of statistical DoEs-RSM methodology is demonstrated in Chapter 5.

The differential outputs are decided.

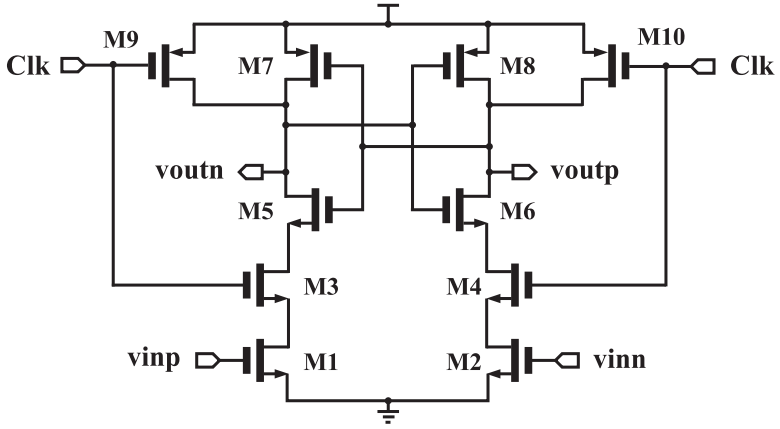


Figure 4.18: Schematic view of the dynamic comparator, transistor dimension W/L = 0.36um/0.06um.

The significant orders determined by regression analysis are shown in Table 4.11. The sequence is determined by weight values (p-value in regression analysis).

RMSEs between simulation result and RSMs' estimation are verified for different models. Table 4.12 presents the results based on 3.12 3.13 3.14 and 3.11. According to the RMSE results, quadratic model is used to plot RSMs.

Table 4.11: The significant orders of BSIM4 parameters in test circuits. The sequence is determined by weight values (p-value in regression analysis)

	1	2	3	4	5	6	7	8
NMOS CM	u_0	v_{th0}	t_{ox}	x_l	n_{fac}	n_{dep}	x_w	r_{dsw}
PMOS CM	v_{th0}	u_0	x_l	t_{ox}	n_{dep}	r_{dsw}	n_{fac}	x_w
Comparator (NMOS)	v_{th0}	t_{ox}	u_0	x_w	r_{dsw}	x_l	n_{fac}	n_{dep}
Comparator (PMOS)	v_{th0}	u_0	x_l	t_{ox}	r_{dsw}	x_w	n_{dep}	n_{fac}

Table 4.12: The RMSEs between circuit level simulation and RSMs estimation. The quadratic model is applied to plot RSMs.

	Current Mirror (N)	Current Mirror (P)	Comparator
Linear	0.041	0.038	0.068
Quadratic	0.002	0.003	0.046
Cubic	0.0001	0.0016	0.007

Both NMOS and PMOS simple current mirror have been simulated. The most significant parameters: v_{th0} and u_0 are selected and normalized as the representative of process variations. The RSMs are built between v_{th0}, u_0 and output current (I_{out} as the circuit performance). The ageing analysis indicated that both HCI and NBTI can degrade output current. Varied response surfaces (see Figure 4.19 and Figure 4.20) are used to estimate ageing degradation and process variations (v_{th0} and u_0). Comparing to HCI induced degradation in NMOS current mirror, the degree of NBTI induced degradation (PMOS current mirror) is lower than HCI.

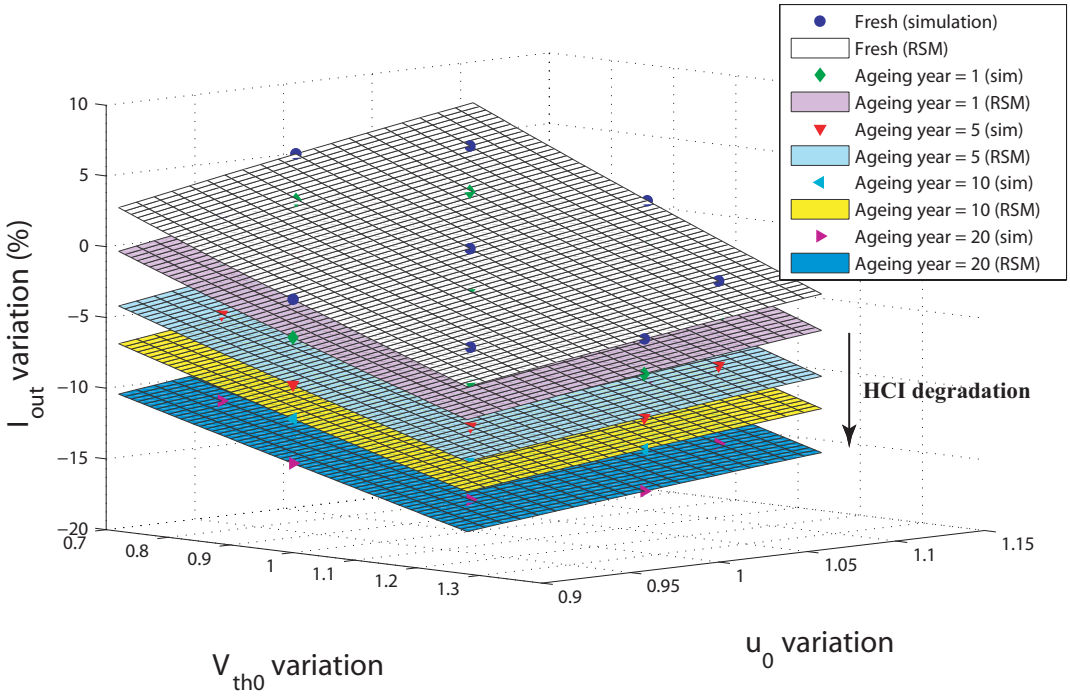


Figure 4.19: Statistical analysis of NMOS current mirror: varied RSMs between BSIM4 parameters and circuit performance.

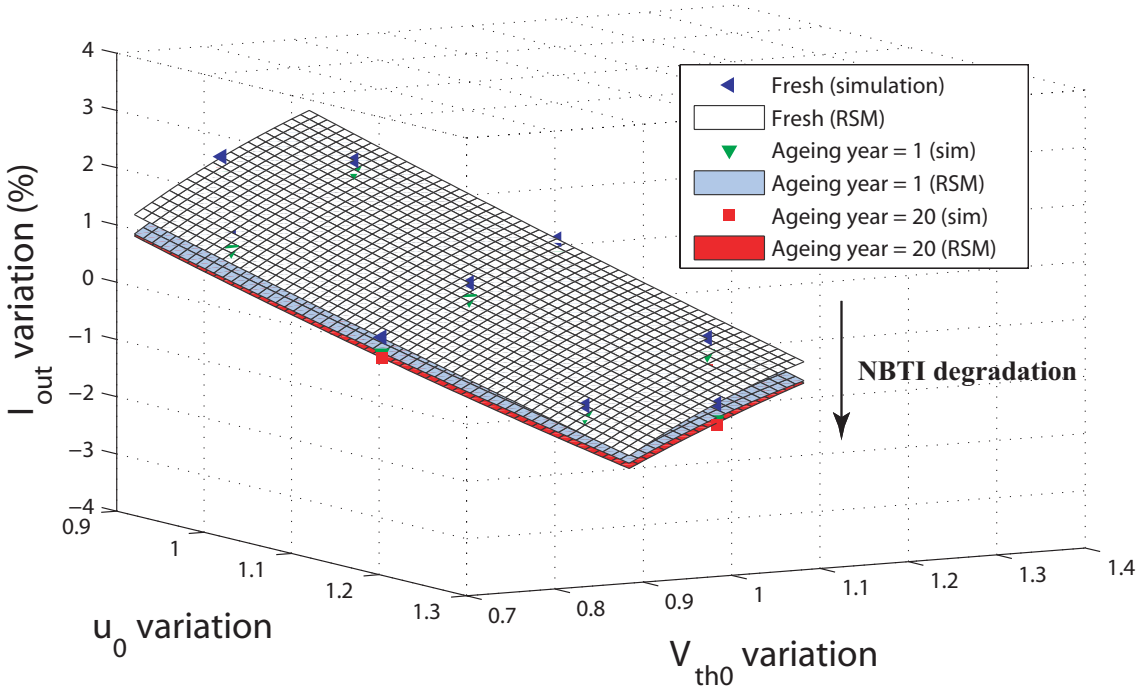


Figure 4.20: Statistical analysis of PMOS current mirror: varied RSMs between BSIM4 parameters and circuit performance.

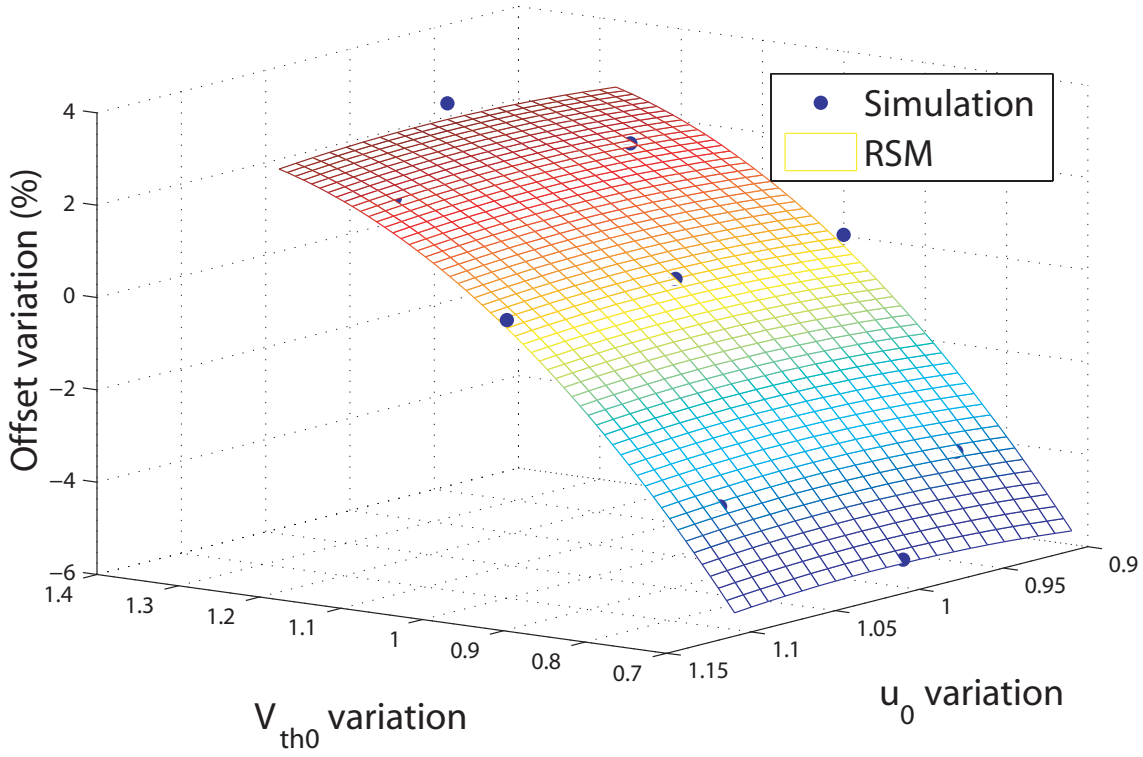


Figure 4.21: The fixed RSM between V_{th0}, μ_0 and comparator offset voltage.

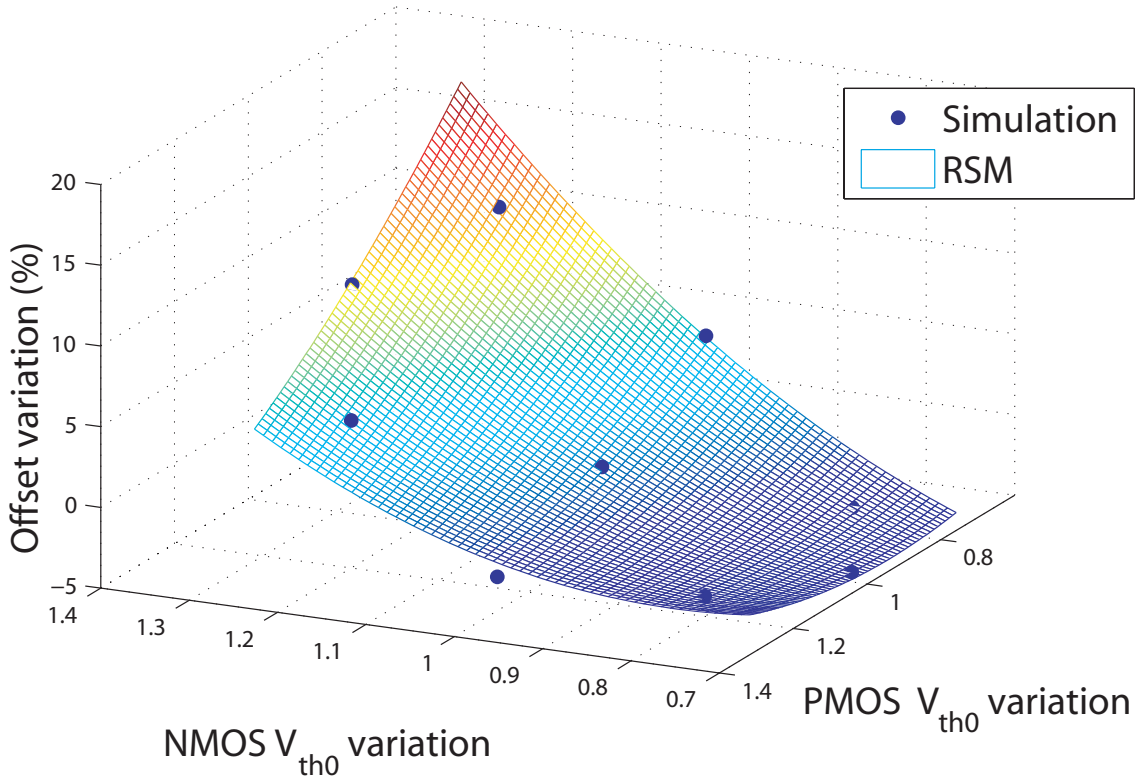


Figure 4.22: The fixed RSM between NMOS/PMOS V_{th0} and comparator offset voltage.

The simulation results of dynamic comparator shows that the comparator can achieve ageing-immunity with HCI and NBTI stress, not only in offset voltage, also in slew rate and propagation delay of the circuit. The balanced circuit structure benefits this ageing-immunity. Also, fully differential (symmetrical) stress is applied to comparator. [48] reported that when asymmetrical stress is applied to the comparator (e.g., comparator in flash ADCs), the offset increases over time due to the time-dependent mismatch at the input stage.

As an ageing-immunity case, the fixed response surface is used to illustrate the process variation only. The offset voltage is chosen as the circuit performance (see Figure 4.21). From the regression analysis, we find that the variations of other parameters except v_{th0} have little or no influence on comparator offset voltage. Thus, the v_{th0} is the dominant parameter (see Table 4.11), in both NMOS and PMOS transistor). Figure 4.22 shows the fixed response surface which reflect v_{th0n} and v_{th0p} to comparator offset voltage.

The DoE-RSMs methodology achieves statistical co-evaluation of ageing effects and process variations. Advantages firstly reflect to simulation efficiency. To obtain a varied or fixed RSM, 17 circuit simulation runs (8 runs for finding critical parameters, 9 runs for DoE simulation) are required with this co-evaluation method. However with MC method, in order to ensure accuracy of simulation results, we need to perform 100 circuit simulation runs at least.

Secondly, the information of process variation obtained from MC method is too general in mode of expression. Designers have no access to know the process variations happened at physical level. This methodology can help designers know the detailed variation of certain parameters (i.e.,V_{th0}, u_0) at physical level. Furthermore, ageing analysis is included. Co-evaluation for ageing effects and process variations can be applied in circuit design loop. Last but not least, this method can be used to simulate reliability performance of large circuits (e.g. analog-to-digital converters, RF front-end). From the point of view of computational efficiency, directly applying MC simulation is infeasible in these complex circuits, this non-Monte-Carlo simulation method is useful.

4.3.6 Summary of Ageing at Circuit Level

Based on some efficient circuit reliability simulation methods, some typical integrated circuits [129] [130] are designed with 65 nm CMOS technology and simulated in Cadence environment. Table 4.13 summarizes the degradation of circuits under HCI and NBTI mechanisms. It is important to note that the degree of ageing phenomena and variability degradation are highly dependent on design.

- The performance of analog circuits is represented by multiple performance parameters. The degrees of ageing induced performance degradation are different among the set of performance parameters.

- The impact of ageing induced degradation on typical 65 nm circuits has been simulated. Both ageing-immune and ageing-sensitive circuits (sometimes certain performance parameters) have been identified.

- In 65 nm CMOS technology, NBTI mechanism can be more dominant comparing to HCI mechanism in these examples. Large transistor length can effectively lower HCI effect because of weakness lateral electric field [10]. NBTI degradation still exists in transistor length (10 μm).

- Weak inversion design can reduce power consumption. For HCI mechanism, immunity to degradation can be achieved.

Table 4.13: Ten years ageing analysis of some typical 65 nm circuits. NBTI and HCI are considered as the main ageing mechanisms.

	Specification (unit)	Standard value	Ageing effects	
			HCI(%)	NBTI(%)
Current mirror	NMOS type, I_{out} (μA)	10	0	N/A
	PMOS type, I_{out} (μA)	10	N/A	-6
OTA	DC gain (dB)	26.1	0	0
	Bandwidth (GHz)	1.02	0	- 2.6
	Phase margin	65	0	+ 0.8
Miller Op-amp	DC gain (dB)	34.76	0	-8.8
	Bandwidth (MHz)	18.86	0	-8.3
	Phase margin	80.52	0	+0.85
Folded cascode Op-amp	DC gain (dB)	33.5	0	0
	Bandwidth (kHz)	99.9	0	0
	Phase margin	83	0	0
Comparator	Output V_{ref} (V)	1.2	0	0.003
	Propagation delay(ns)	78.67	15.1	16.5
DAC	Output V_{ref} (V)	0.2842	0.001	0.006
	Loop delay (ns)	1.2	0.49	0.02
Clock generator	Delay (ns)	1.909	-3.93	-1.1
Bias circuits	Reference Voltage (V)	N/A	0	0
CMFB	Reference Voltage (V)	0.6	0	0

- Comparing to balanced differential analog circuits, the degradations (ageing induced) and fluctuations (process variation induced) could become worse at unbalanced differential structure of analog circuits.

4.4 Conclusion

Reliability methodologies which proposed in previous chapters have been applied to 65 nm CMOS circuits. CMOS Transistors and typical analog circuits are simulated considering ageing effect and process variations. Eldo simulator is used and further applied to some reliability-aware methodologies. It has been reviewed that the degree of degradation is depend on transistor dimensions and circuit architectures. In 65 nm integrated circuits, NBTI induced degradation is more severe than HCI. In the statistical co-evaluation method, the number of statistically relevant parameters from the BSIM4 model varies at different circuits. DoEs can increase the efficiency of analysis flow with selected experiments. RSMs can reflect BSIM4 process parameters with performance parameters at circuit level.

The reliability methodology can be applied equally to more advanced CMOS nodes. To extrapolate this methodology alongside technology scaling down, we need some informations on the reliability models of transistors and they are not available in this work. With hierarchical reliability simulation methodology [95] [11], we will discuss reliability issues at system level in the next chapter. The Sigma-Delta ($\Sigma\Delta$) modulator is concerned as the system-level application.

Chapter 5

Reliability in Sigma Delta Modulators

ΣΔ modulator is a key component in many mixed-signal SoCs. Many different architectures for ΣΔ modulator have been proposed over the last decades, covering a wide range of performance characteristics [131] [132] [133]. Although ΣΔ modulator is enough robust, for some critical applications in medical and space, the circuits performance degrades over time due to ageing degradation effects. Thus, the reliability needs to be considered in the earlier design stage during a time analysis of an aged circuit. However, until now few published work concerned in reliability-aware design of ΣΔ modulator. In this Chapter, low pass sigma-delta ADCs are introduced and the design procedure of ΣΔ modulator is reviewed. Hierarchical reliability analysis is performed on continuous-time ΣΔ modulators with 65 nm CMOS technology. Statistical methods are applied to variability analysis. Also, reliability-aware design considerations are proposed in this chapter.

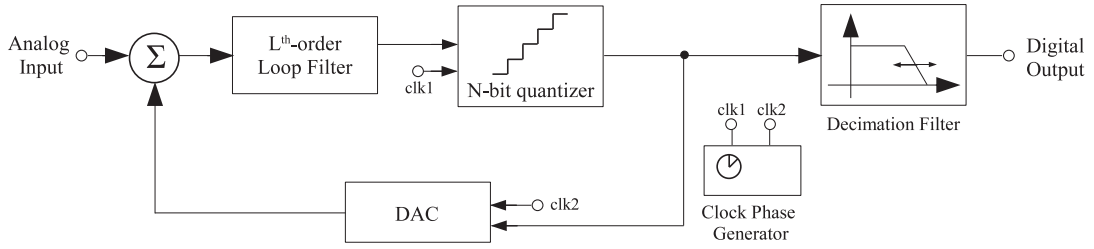


Figure 5.1: A general view of a CT ΣΔ ADC

5.1 Introduction to Sigma Delta Operation

The sigma-delta modulator is an ADC topology that can digitize high-resolution analog signals into lower resolution digital signals with oversampling technique. Figure 5.1 shows the general view of a CT ΣΔ ADC which contains a ΣΔ modulator and digital decimation filter. A ΣΔ modulator consists of an analog loop filter, a low resolution quantizer and a feedback digital-to-analog converter (DAC). Main types of ΣΔ ADCs are: low pass (LP) modulators, high pass (HP) modulators and band-pass (BP) modulators. The LP modulator will be elaborated in the following sections.

5.1.1 Preliminaries

Comparing with Nyquist-rate converters, oversampling converters gain the advantage in several fronts including over resolution, bandwidth and power efficiency. The oversampling technique is widely used for high-resolution A/D and D/A conversions of low-to-medium

bandwidth signals with applications ranging from sensor networks, audio interfaces to wireless communications.

The key advantage of oversampling is that the signal band occupies a small fraction of the Nyquist interval [134]. It is possible to use digital cancellation on the relatively large fraction of the quantization noise that is outside the band of interest. Second of all, comparing to high order digital filters, the anti-aliasing filter (AAF) has less complexity by relaxing the requirements of the filter at the cost of a faster sampler. In particular, continuous-time $\Sigma\Delta$ converter has the feature of inherent anti-aliasing. The amount of oversampling is described by the oversampling ratio (OSR), which is the ratio of the sampling frequency to the signal bandwidth $2f_c$

$$OSR = \frac{f_s}{2f_c} \tag{5.1}$$

On the other hand, oversampling can be implemented in order to achieve higher resolution. The equivalent number of bits (ENOB) can be potentially improved by OSR with:

$$ENOB \ = \ n \ + \ 0.5 \cdot Log_2 OSR \tag{5.2}$$

It is a tradeoff that oversampling data converters increase the resolution and linearity to system. Additional considerable amount of digital circuitry with some analog stages is required. Furthermore, the fast operation to digital circuit is a waste of power. Since oversampling ADCs require high oversampling-ratios, Nyquist rate ADCs with a lower sampling ratio might still be better suited for very high speed applications.

Figure 5.2 shows a linear $\Sigma\Delta$ modulator with additional quantization noise. The model can be written as the combination of the input $u(z)$ and the quantization noise $e(z)$. We can get signal transfer function STF(z):

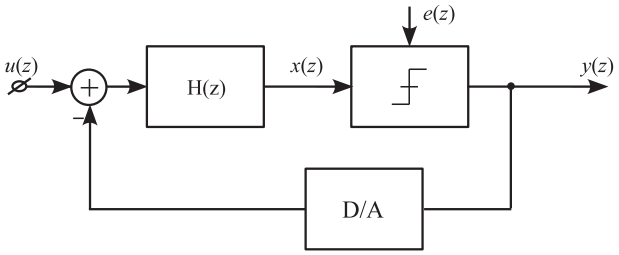


Figure 5.2: The linear model of $\Sigma\Delta$ modulator with quantization noise $e(z)$.

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{5.3}$$

and noise transfer function NTF(z):

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{5.4}$$

where:

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{5.5}$$

Figure 5.3 shows an example (with 1-bit DAC) of $\Sigma\Delta$ modulator output in time domain when applying a sinusoid input signal. As the input signal amplitude increases, the number of '1' in the output samples increases with respect to the number of '-1'. For example, when the signal is near to the maximum, the output is mainly '1', when the signal is near to the minimum the output is mainly '-1' and it is equally distributed when the

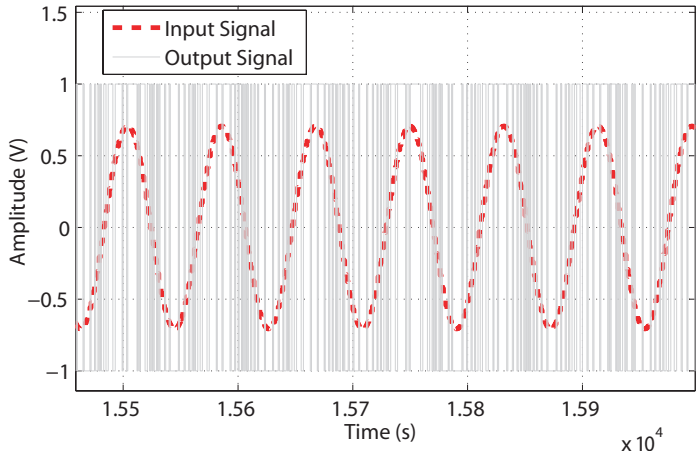


Figure 5.3: The single bit modulator response in time domain: a sinusoid input signal and modulator output.

input signal is around '0'. Hence it can be seen that the average of the output follows the average of the input [131].

Figure 5.4 illustrates the output spectrum of LP ΣΔ modulator. The bin around -3 dB magnitude represents the baseband signal. With the noise transfer function (NTF), the white spectrum of the quantization noise can be changed into a shaped spectrum. Afterward, the out-of-band noise must be removed by a digital low pass filter, which will improve the modulator performance significantly. Figure 5.4 also shows the CT and DT spectrum. These topics will be elaborated in the next subsection.

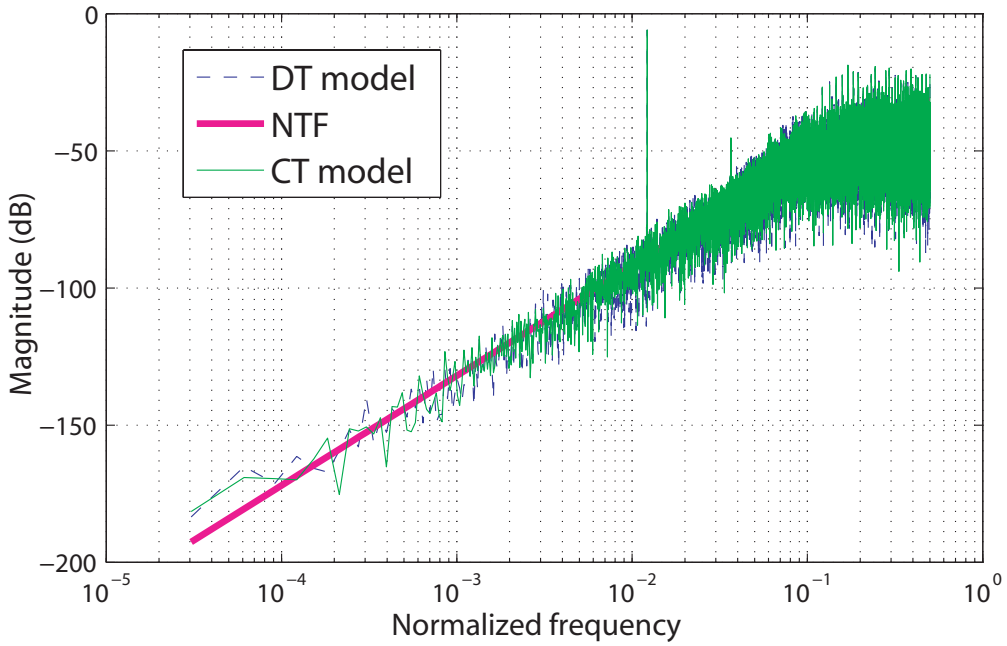


Figure 5.4: Modulator response in frequency domain: both DT and CT modulator model are in accordance with designed NTF.

5.1.2 Noise Shaping

When using oversampling, the high sampling rate transmits the delta between samples instead of the whole sample. It becomes more effective if we can shift most of the quantization noise towards high frequencies. In order to achieve this high-pass to the noise, a zero should be in included in the NTF. That is z=1. Since zero of NTF could be treated as a pole of STF. The STF (z) could be an integrator, where:

$$H(z) = \frac{1}{z-1} \tag{5.6}$$

The NTF of an ideal low pass L^{th} order modulator could be defined as:

$$NTF(z) = (1-z^{-1})^L \tag{5.7}$$

We assume that quantization noise $e(z)$ is white noise. The power spectral density (PSD) of quantizer noise is:

$$S_E(f) = \frac{\Delta^2}{12 f_s} \tag{5.8}$$

where Δ is quantization step. It can be related to $V_{ref} = \Delta \cdot 2^{n-1}$, V_{ref} is the reference voltage of the quantizer and of the feedback digital to analog converter (DAC). n is the number of bits of the quantizer. Once the quantization noise is shaped by a L-order LP modulator, we obtain:

$$S_Q(f) = S_E(f) \cdot |NTF(f)|^2 = S_E(f) \cdot (2sin(\frac{\pi f}{f_s}))^{2L} \tag{5.9}$$

For small x, the approximation $sin(x) \approx x$ is achieved. Hence, the in-band noise power can be calculated by integrating PSD over the signal bandwidth:

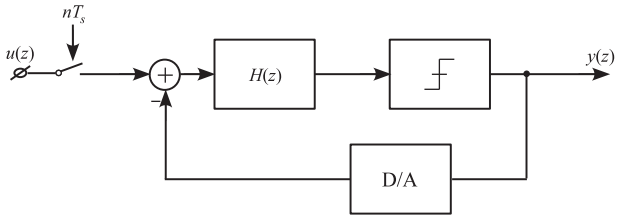
$$P_Q = \int_{-f_c}^{f_c} S_Q(f)df = \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \frac{1}{OSR^{2L+1}} \tag{5.10}$$

where Δ is the quantization step. When double increasing the OSR, the signal to quantization noise ratio (SQNR) will increase ($6L$+3) dB. The $\Sigma\Delta$ modulator can achieve high performance with oversampling technique and noise shaping. If the STF is unitary, the SQNR at the modulator output is calculated by:

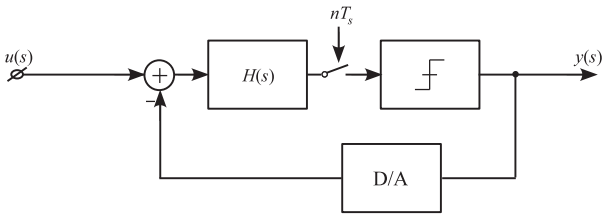
$$SQNR = 10 \cdot Log \frac{P_{signal}}{P_Q} \tag{5.11}$$

5.1.3 CT and DT

Figure 5.5(a) 5.5(b) show the block diagram of both DT and CT $\Sigma\Delta$ modulator. Even if the first SDM was with CT loop filter, majority of that used DT loop filter afterwards because of the attractive advantages in accuracy and linearity in DT modulators. But never forget that CT modulators have an important feature of inherent anti-aliasing. Through mathematic analysis, one can come to the conclusion that a DT modulators with an anti-aliasing filter in the front is equivalent to its CT counterpart without AAF. This simplifies the overall system analysis and simulation. What's more, because sampling of the signal now happens at the output of the loop filter, the error introduced by imperfect sampling can be suppressed by the noise shaping function. The other advantage of CT modulator regards to the limit of the clock rate. Since in CT modulator the clock rate is not such limited by the unity-gain frequency of the amplifiers in the filters as in its DT



(a) DT loop filter



(b) CT loop filter

Figure 5.5: DT and CT ΣΔ modulator

counterpart, the clock frequency can be much higher, or we can say the speed requirement of the inner amplifiers is largely reduced.

For CT modulator, a DT-to-CT conversion in needed. At every sample instants, if both the inputs to the DT and CT quantizers are equal to each other, the DT and CT model function are equivalent. According to this, we can write the equation [132]:

$$Z^{-1}\{H(z)\} = L^{-1}\{H(s)H_{DAC}(s)\}|_{t=nTs} \tag{5.12}$$

where $H_{DAC}(s)$ is the transfer function of the DAC in CT modulator. This is called the impulse-invariant transformation between the DT and CT ΣΔ modulator.

5.2 Design Procedure

This design procedure is based on Schreier's ΣΔ toolbox [135], Matlab/Simulink^{TM} environment and Verilog-AMS modeling in Cadence. For a systematic realization of ΣΔ modulator according to design specifications, designers should follow the steps below:

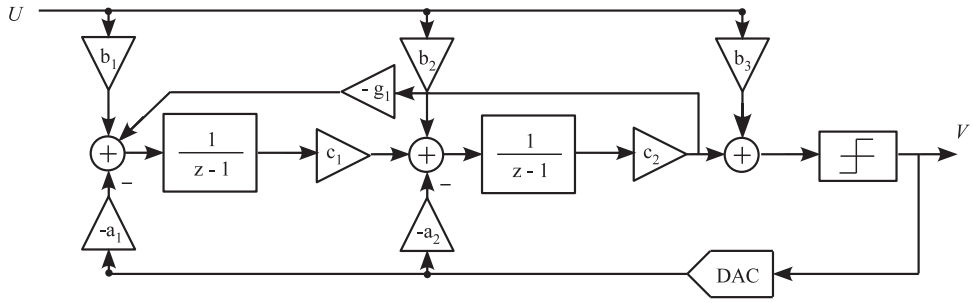
1. Selecting a proper architecture;
2. Determining the specifications of the building blocks (analog loop filter, quantizer and DAC) necessary to implement the selected architecture;
3. Considering the effects of non-idealities of each building circuit/block;
4. Simulating entire ΣΔ ADC.

5.2.1 Topology Selection

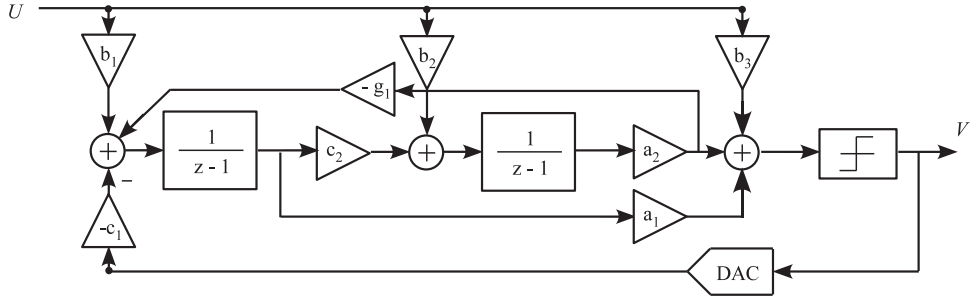
Topology selection is the first task of designing ΣΔ modulator. After deciding CT or DT system according to design requirements, there are still many specifics need to be drew up. According to formulas (sometimes rules of thumb) in [133], [132], we must relate OSR, modulator order and number of bit to SNR of modulator.

As shown in Figure 5.1, the CT modulator consists of an analog loop filter, a quantizer, a digital-to-analog converter (DAC) and clock distributor circuits. It is important to select an appropriate STF and NTF for the modulator. Figure 5.6(a) 5.6(b) show the two main

topology of ΣΔ modulator [136], cascade of integrator with distributed feedback and input coupling (CIFB) and chain of integrators with weighted feedforward summation structure (CIFF). Also, there are some derivative structure such as cascade of resonators feedback (CRFB), cascade of resonators feedforward (CRFF) and CIFB with input-signal feedforward (CIFB-IF).



(a) The CIFB loop filter



(b) The CIFF loop filter

Figure 5.6: The architecture of CIFB and CIFF analog loop filters, which are implemented with cascade-of-integrators. With cascade-of-resonators, we can realize CRFB and CRFF architectures.

In this work, CIFB structure is mainly concerned. In CIFB loop filter, all zeros of NTF are located at DC (z=1). In order to distribute zeros of NTF inside signal bandwidth, g-feedback loops can be added. The main advantage of the CIFB topology is its easy implementation. It is with low sensitivity to component variations. However, the main disadvantage of this topology is that the signals at the output of the integrators are a function of the input signal, so that the output swing is large at low-voltage applications. Meanwhile, it is sensitive to integrator nonlinearities [137].

In the following steps, analog loop filter is realized with integrators (e.g., resistor-capacitor (RC) integrator). Quantizer and DAC are behavioral modeled with Verilog-AMS.

5.2.2 High-level Design

- NTF and STF

  For a 2^{nd} order CIFB loop filter (see Figure 5.6(a)), the feedforward transfer function $L_0(z)$ is:

$$L_0(z) = \frac{b_1 + b_2(z-1) + b_3(z-1)^2}{(z-1)^2} \tag{5.13}$$

The feedback transfer function $L_1(z)$ is:

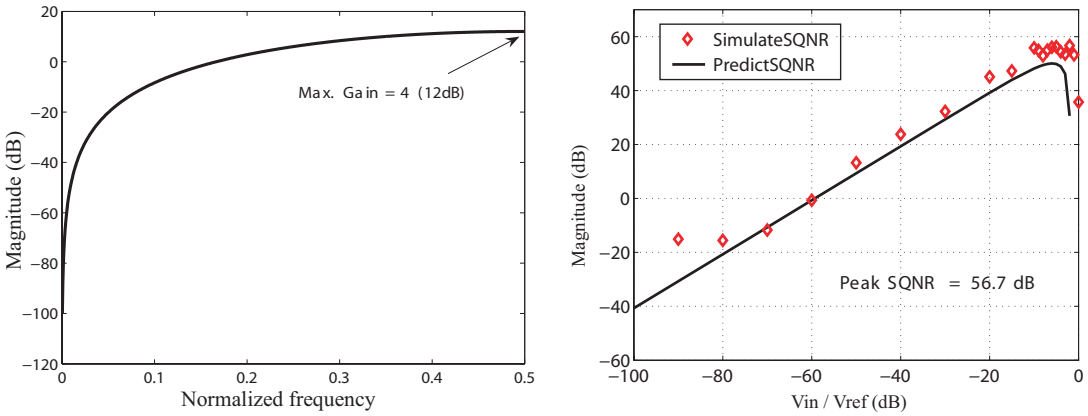
$$L_1(z) = \frac{a_1 + a_2(z-1)}{(z-1)^2} \tag{5.14}$$

So the NTF and STF is:

$$NTF = \frac{1}{1 - L_1(z)} = \frac{(z-1)^2}{a_1 + a_2(z-1)} \tag{5.15}$$

$$STF = \frac{L_0(z)}{1 - L_1(z)} = \frac{b_1 + b_2(z-1) + b_3(z-1)^2}{a_1 + a_2(z-1)} \tag{5.16}$$

Where poles of NTF and STF are controlled by a coefficients, zeros of STF are controlled by b coefficients. Coefficients calculation and dynamic range scaling are performed to realize the signal transfer function (STF) and noise transfer function (NTF). The SQNR is predicted. Output spectrum is evaluated. Figure 5.7(a) presents the NTF of a 1-bit 2^{nd} order modulator with CIFB architecture. Figure 5.7(b) illustrates two synthesis method to predict the SQNR. Now a DT $\Sigma\Delta$ modulator is ready to simulate in Matlab and simulink. For CT modulator, a DT-to-CT conversion must be performed to determine new CT coefficients.



(a) The function *synthesizeNTF* and ideal frequency response of desired NTF.

(b) SQNR prediction with Delta-sigma toolbox (function *simulateSNR* and *predictSNR*).

Figure 5.7: NTF synthesize and ideal SQNR predictions

- Noise budget

  When the architecture of the loop filter is decided, the next task is to figure out the values of the passive components. In $\Sigma\Delta$ modulator, noise sources include quantization noise, DAC noise, loop filter noise and clock jitter. This noise is partitioned according to the noise budget. The values of the passive components need to be figure out through noise budget. Noise generated over the loop filter usually contributes most part of the total noise. We can calculate the total maximum acceptable in-band noise (IBN) from the SNR expectation. A 2^{nd} order CT-RC (resistor-capacitor) $\Sigma\Delta$ modulator is introduced here to study noise budget. The SNR requirement of 49 dB at -6 $dBFS$ (dB Full Scale) input gives an IBN level requirement of the total IBN -55 $dBFS$. With the equation:

$$X = 10\ Log\frac{P}{FSI^2}\ (dBFS) \tag{5.17}$$

Where FSI is defined as the maximum average feedback current of the $\Sigma\Delta$ modulators. Correspondingly, FSI in voltage can be defined to be equal to V_{ref}. 3.16 μFSI^2 is realized. Where P is the power under consideration (in our case P stands for the power of the total IBN), and FSI is equal to the half of the maximum feedback current. FSI in voltage can be defined to be equal to V_{ref}.

Furthermore, the in-band quantization noise can be determined with:

$$\sigma_q^2 = \frac{\Delta^2}{12} \times \frac{\pi^4}{5} \times \frac{1}{OSR^5} \tag{5.18}$$

in which Δ is the *quantization step*, $\Delta = 1.2$ in our case. Now we assume that loop filter is responsible for 70% of the total noise. Table 5.1 summarizes the noise budget allocation.

Table 5.1: Noise budget allocation.

Noise source	Percent	Value (FSI^2)
Loop filter	70%	2.21 μ
Clock jitter	12%	0.38 μ
Quantization noise	6%	0.19 μ
DAC	12%	0.38 μ
Total	1	3.16 μ

For a 2^{nd} order CT-RC $\Sigma\Delta$ modulator, the noise introduced by the second integrator will undergo a first order noise shaping, the noise generated in first integrator directly injects to the input of the modulator. Thus, we assume 70% of the loop filter noise is attributed to the first integrator.

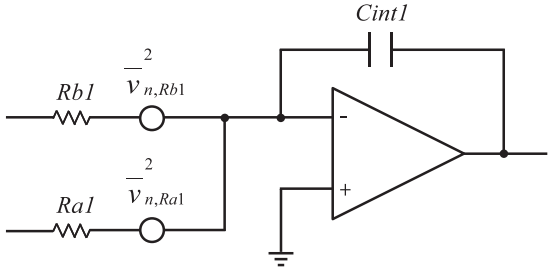


Figure 5.8: Noise calculation with RC integrator model.

Figure 5.8 shows the RC integrator for noise calculation, the thermal noise of the $Rb1$ and $Ra1$ are:

$$\overline{v}^2_{n,Rb1} = 4kT \times Rb1 \times f_B \tag{5.19}$$

$$\overline{v}^2_{n,Ra1} = 4kT \times Ra1 \times f_B \tag{5.20}$$

where f_B is the baseband frequency. The noise generated by the non-ideal op-amp is assumed to be equal to that by $Rb1$:

$$IBN_{opamp} = 4kT \times Rb1 \times f_B \tag{5.21}$$

The total input-referred in-band noise introduced by 1st integrator is:

$$IBN_{Int1} = \overline{v}^2_{n,Rb1} + \overline{v}^2_{n,Ra1} \times \frac{Rb1^2}{Ra1^2} + IBN_{opamp} \tag{5.22}$$

- Functional level design

  The high level design of SDM includes behavioral modeling in Matlab/Simulink^{TM} environment and Verilog-AMS modeling in Cadence. The modulator performance is still evaluated by the ΣΔ toolbox [135].

  Appendix 1 illustrates a complete ΣΔ ADC system designed with Simulink, included a second-order ΣΔ modulator in CIFB architecture and a digital decimation filter (sinc filter + 2 FIR filter). The functionality of modulator can be evaluated in Simulink and then compared to design specifications.

  The Loop filter, quantizer and DAC can be efficiently modeled with Verilog-AMS. Nonideality effects such as limited DC gain and GBW, signal distortion and excess loop delay are evaluated in this step.

  [132] concludes the in-band-noise caused by finite DC gain A_0 and GBW in 2nd-order single loop SDM:

$$IBN_{A_0} \approx \frac{\Delta^2}{12} \times (\frac{\pi^4}{5}\frac{1}{OSR^5} + \frac{2\pi^2}{3}\frac{1}{A_0^2 OSR^3} + \frac{1}{A_0^4 OSR}) \tag{5.23}$$

$$IBN_{GBW} \approx \frac{\Delta^2}{12} \times \frac{\pi^4}{5} \times \frac{1}{OSR^5} \times (1 + \frac{1}{RC \times GBW})^2 \tag{5.24}$$

5.2.3 Circuit level Design

Based on behavioral simulation results, all building blocks need to be implemented with CMOS transistors. Proper circuit architecture should be chosen and implemented at transistor level. For CT-ΣΔ modulator, the main building circuits include: op-amps in integrator (loop filter), comparator (quantizer), DAC and clock distributor. Each building block must be simulated and validated with system level simulation (e.g., a transistor-level DAC should be simulated with other blocks which are ideal modeled with Verilog-AMS). Finally, a whole modulator system simulation is required with all transistor implemented building circuits.

5.3 Reliability in Sigma Delta Modulators

In this section, reliability in ΣΔ modulators is studied. We review previous methodologies and relevant work in reliability evaluation of large and complex AMS systems. Hierarchical reliability analysis approach is implemented on ΣΔ modulators. We put emphasis on continuous-time ΣΔ modulators. The basic CIFB architecture of analog loop filter is designed and studied. A 400 Hz low power 1 bit CT-ΣΔ modulator and a 125 kHz 3 bit CT-ΣΔ modulator are two designed examples.

5.3.1 Literature Review

A large amount of work in ICs reliability focus on ageing mechanisms and process variations at transistor and circuit level. Few articles reported reliability study of large and complex AMS systems. Table 5.2 gathers the dominant work in recent years, which included reliability-aware methodologies and reliability analysis.

Table 5.2: Literature review of reliability study in SDM and other types of ADC. N/A for CMOS node is not specified.

Ref. (year)	Reliability sort	Applications	CMOS	Main methodology
[26] 2003	Transient faults	SAR, flash and SDM ADCs	N/A	Sensitivity analysis
[138] 2006	Parameter fluctuations	DT SDM	N/A	Statistical LUT
[139] 2006	Fault Diagnosis	Digital part of SD ADC	N/A	Catastrophic defects
[94] 2007	Process variations	CT-SDM	0.18 μm	Hierarchical and statistical methods
[119] 2009	HCI,NBTI,TDDB	Flash ADCs	90 nm	Failure in time (FIT) Failure prediction
[80] 2011	Process variations, HCI and NBTI	RF front-ends	65 nm	Top-down, bottom-up reliable design
[140] 2011	HCI, NBTI	SAR-ADCs, DT-SDMs	32 nm	Hierarchical methodology
[11] 2012	Process variations, HCI and NBTI	CT-SDM	65 nm	Hierarchical and statistical methods

[26] first proposed transient fault sensitivity analysis and reliability enhancement of analog-to-digital converters. Sensitivity analysis is used to grade blocks based on their sensitivity to *alpha*-particle faults. For $\Sigma\Delta$ ADC, it presented that the digital decimation filter is the most critical block. Reliability enhancement is implemented by using the transient pulse tolerant latch (TPTL) in decimation filter.

[94] presented a hierarchical method for statistical analysis of performance variations in CT $\Sigma\Delta$ modulator. a 0.18 μm 4^{th} order modulator was studied with DoEs and RSMs. This method can characterize the circuit-level performance parameters and relate them to design parameters in a high level behavioral model.

[138] proposed a methodology used in DT $\Sigma\Delta$ ADC. Each building block is modeled by lookup tables (LUT) to assess performance variations due to parameter fluctuations. To address the issue of parametric process variations, RSM is used to construct parameterizable LUTs in key process variables and facilitate efficient statistical analysis of $\Sigma\Delta$ ADC.

[139] examined effects of delay and catastrophic defects in Sigma-delta ADC. The artificial neural network (ANN) is presented to diagnosis of defects in the digital part of a nonlinear mixed-mode circuit.

[119] studied HCI, NBTI and TDDB degradation to 90 nm Flash ADC. This work is based on applying MTTF and FIT to quantitatively prediction of ageing mechanisms. It performed circuit failure analysis and critical block selection. The MTTF and FIT of ADC is estimated with a reliability model at system level. It concluded that PMOS transistor is the reliability-critical device and NBTI is the most critical failure mechanism for ADC under normal operation in submicrometer CMOS technology.

[140] completed the Ph.D work on ageing mechanisms study of AMS circuits and systems at 32 nm CMOS node. A fully differential DT switch-capacitor (SC) $\Sigma\Delta$ modulator is done in Cadence and Simulink environment. The analog noise-shaping circuit is implemented in Cadence environment using 32 nm high-k metal gate CMOS technology except for the multi-bit quantizer and DAC. It presented that the offset in the first integrator

stage outweighs by far the impact of aging on modulator degradation. Ageing induced gain errors in DAC also degrades modulator performance. The impact of aging degradation in the multi-bit quantizer and the DAC circuit was not significant due to its low resolution.

Besides, [80] studied reliability in RF front-end. It proposed a new design flow for AMS/RF circuits with the aim to improve the reliability. Failure evaluations, design space exploration and sensitivity analysis have been directed towards ageing effects and process variation in CMOS 65 nm transistors. Top-down and bottom-up reliable design of RF front-end are also included in the study.

In this work, reliability analysis is performed on a 400 Hz 1-bit second-order LP-CT $\Sigma\Delta$ modulator, and a 125 kHz 3-bit third-order LP-CT $\Sigma\Delta$ modulator, both are modeled in Matlab/Simulink^{TM} environment and Cadence environment, designed with CMOS 65 nm technology.

5.3.2 Simulation Methodology

For $\Sigma\Delta$ modulators, simulation for one performance parameter sample takes even days. As a result, for design variability considerations, directly applying the Monte Carlo simulation is not realistic from computational time point of view [94]. On the other hand, directly performing ageing simulation with transistor platform at system level can not be achieved with any commercial tools [28] [10].

Thus, hierarchical reliability-aware approach is suitable to analysis ageing effects and process variations in $\Sigma\Delta$ modulators [12] [11]. Statistical co-evaluation method has been used to ageing effects and variability simulation. Figure 5.9 demonstrates this approach. This bottom-up method can propagate transistor ageing degradation and process variations up to the system level (via the intermediate circuit level). On the other hand, failure analysis is used as a case study to $\Sigma\Delta$ modulators. Ageing simulation is performed in Eldo [68]. Statistical analysis and computer-aided design are completed in Matlab [128].

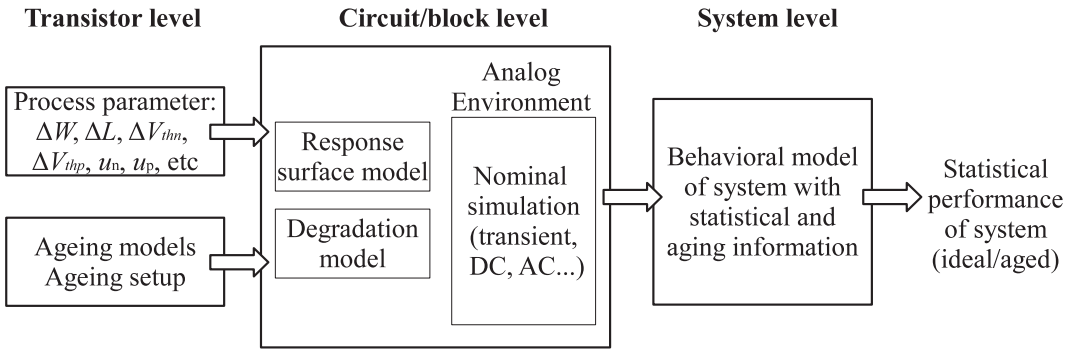


Figure 5.9: The hierarchical bottom-up approach for reliability.

5.3.3 A 400 Hz 1-bit Second-order LP-CT Sigma Delta Modulator

Reliability topic is important in implantable medical device. A 400 Hz 1-bit second-order low pass CT $\Sigma\Delta$ modulator is behavioral designed and implemented at transistor level. This application is to detect cardiac signal in medical cardiac pacemaker.

5.3.3.1 Behavioral Modeling

The proposed 2$^{\text{nd}}$-order LP CT $\Sigma\Delta$ modulator is shown in Figure 5.10. The modulator consists of a 2^{nd}-order loop filter, a one-bit quantizer with the return-to-zero (RZ) feedback

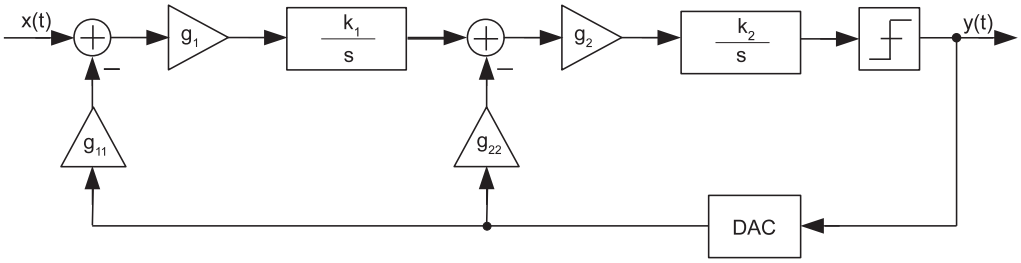


Figure 5.10: Model of 2^{nd} order CT $\Sigma\Delta$ modulator in CIFB architecture. g_1, g_2, g_{11} and g_{22} are feedforward and feedback coefficients.

DAC, operating at 32 kHz with an OSR of 40. Active RC integrators with operational-amplifier (op-amp) are used in the modulator because of its simplicity and high linearity. The loop filter is in CIFB architecture (presented in Figure 5.6(a)). A maximum NTF gain equal to 12 dB can be achieved. The expected performance parameters are shown in Table 5.3. Figure 5.11 illustrates the schematic view of the 2^{nd} order active RC loop filter.

Table 5.3: Expected specification of the 2^{nd}-order CT $\Sigma\Delta$ modulator.

Parameter	Expected
Supply voltage V_{dd}	1.2 V
Input frequency f_{in}	400 Hz
Clock frequency f_{clk}	32 kHz
OSR	40
SQNR	58 dB
SNR	49 dB
Power	200 nA
ENOB	8 bits

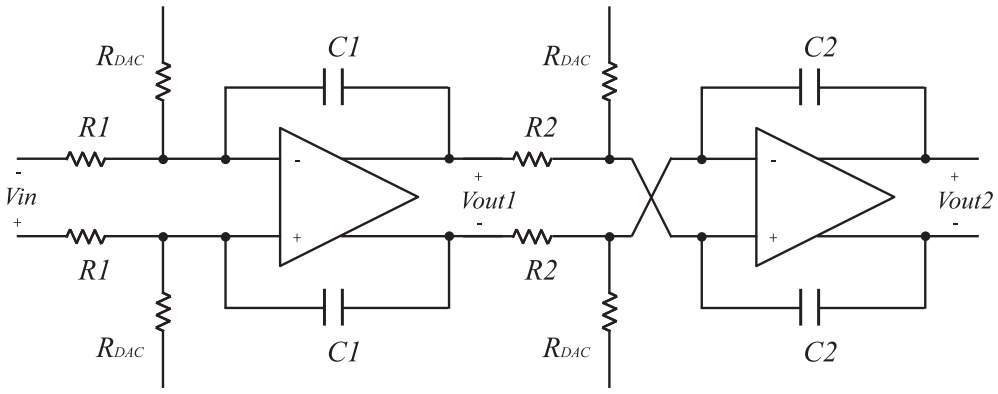


Figure 5.11: The schematic view of a 2^{nd} order active RC loop filter

Passive components value are determined through noise budget (see Subsection 5.2.2). Table 5.4 summarizes the values of passive components.

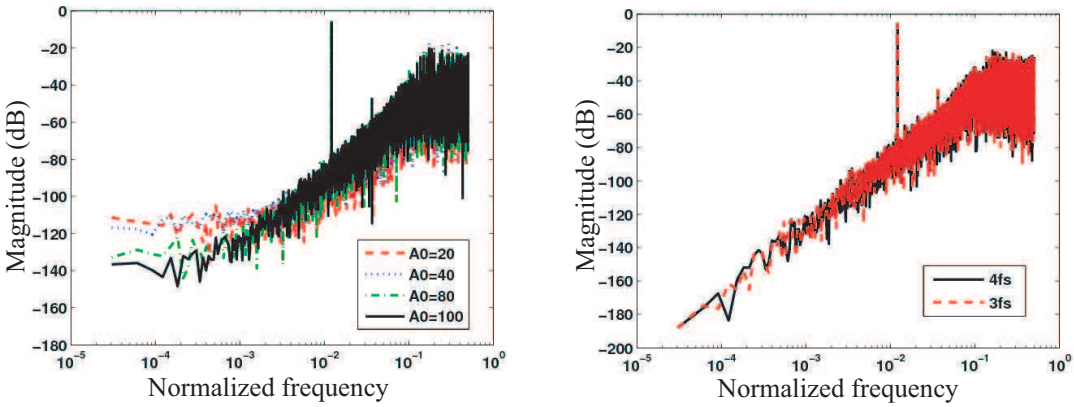
The modulator performance is predicted by Delta-Sigma Toolbox [133]. For 2^{nd}-order LP CT $\Sigma\Delta$ modulator, the ideal peak SQNR is 56.7 dB, which appears when the input signal amplitude around -6 dBFS. Taking into account the nonideality of the resistors in the integrator, the peak SQNR is a 1.3 dB lower than the ideal, which is 55.4 dB.

Table 5.4: Passive components in the loop filter

Component	Rb1	Ra1	Cint1	Rc2	Ra2	Cint2
Value	60 MΩ	30 MΩ	4.2 pF	11.25 MΩ	30 MΩ	5.6 pF

According to the noise budget calculation, integrators contribute some noise to the total in-band noise. This is caused by the nonidealities of the op-amps (i.e. the finite DC gain and GBW).

Figure 5.12(a) and Figure 5.12(b) show the output spectrum with different op-amp DC gain (A_{dc}) and gain bandwidth (GBW). Since low order LP-CT modulator is not sensitive to DC gain and GBW. With infinite GBW, the SQNR is almost the same when DC gain is larger than 40 (linear scale). Meanwhile, with infinite DC gain, the SQNR becomes worse if GBW is lower than $3*f_s$. Proceeding from the simulation results, we choose A_{dc} = 40 (linear) and GBW = 96 kHz as the parameter for both op-amps. SQNR is 54.6 dB in this case.



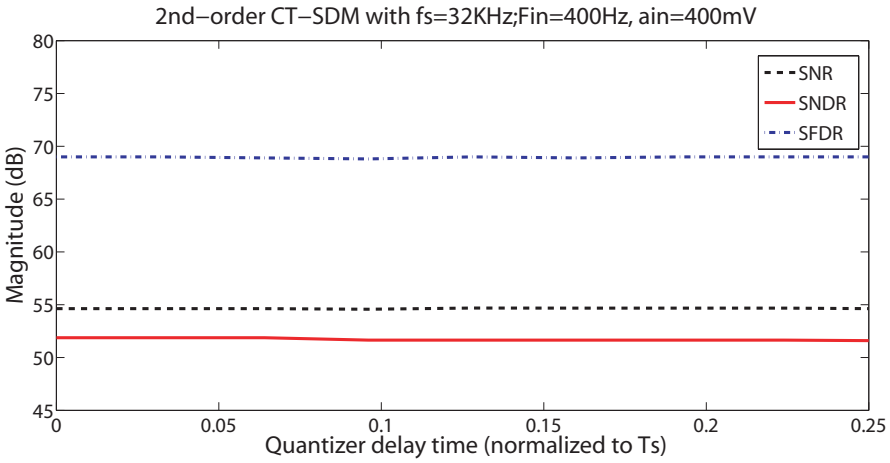
(a) Different DC gain

(b) Different GBW

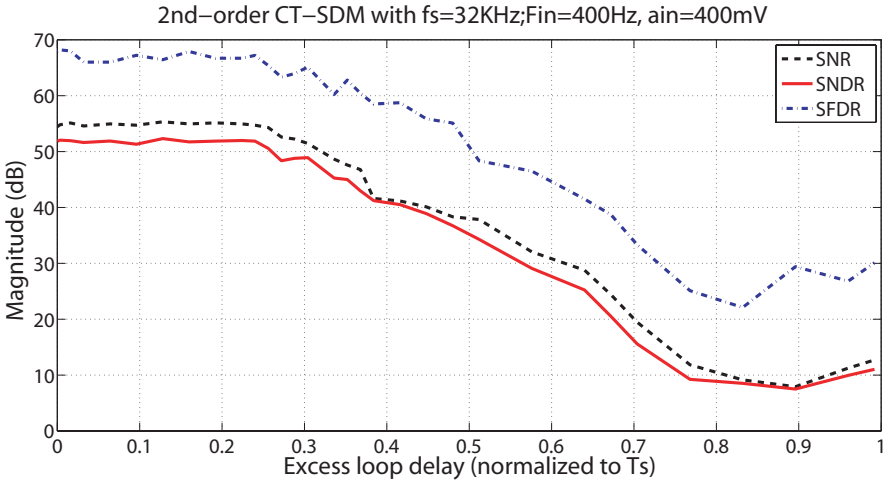
Figure 5.12: Output spectrums with DC gain and GBW variance. SQNR is 55.0 dB, 55.0 dB, 54.5 dB, 51.3 dB when (A_{dc}) is 100, 80, 40 and 20; SQNR is 54.9 dB, 54.8 dB when GBW is 128 kHz and 96 kHz

The excess loop delay should be mentioned in the return-to-zero (RZ) feedback loop, αT_{clk} delay is set in order to give a decision time to quantizer, where $\alpha = 0.25$. Excess loop delay arises because of nonzero transistor switching time, which makes the edge of the DAC pulse start after the sampling clock edge [141]. Since the area of the feedback pulse is directly proportional to the charge delivered to the loop filter. The CT ΣΔ modulator are very sensitive to feedback waveform generated from the DAC. The excess delay in feedback loop can affect the NTF and then influence the modulator performance [141]. System performance such as SQNR, signal-to-noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) are considered. Performance degradation with different τ_d is shown in Figure 5.13(a) and Figure 5.13(b).

In Figure 5.13(a), there is almost no degradation if the delay happened in quantizer. However, in Figure 5.13(b), for delays below about 20% of T_{clk}, the performance is roughly constant, but the performance decrease as delay increases. The degradation condition is serious for DAC when the delay is more than 0.3 T_{clk}.



(a) Modulator performance versus quantizer delay. There is almost no degradation if the delay happened in quantizer



(b) Modulator performance versus quantizer delay. The degradation condition is serious for DAC when the delay is more than 0.3 T_{clk}.

Figure 5.13: The performance of quantizer and DAC

5.3.3.2 Block Failure Test

CT ΣΔ modulator can be divided into loop filter and feedback loop. Feedback loop includes dynamic comparator (comprise quantizer and latch) and DAC. For return-to-zero feedback system, a clock phase generator is needed. According to the minimum requirement for each component, the failure condition of integrators (op-amps) is:

- $A_{dc-loss}$ = 3 dB,
- GBW_{loss} = 32 kHz (1*f_s);

Since during the modeling phase, the op-amps are implemented with minimum design (A_{dc} = 40 (linear) and GBW = 96 kHz). Lower A_{dc} and GBW will make obvious degradation to modulator performance. The failure condition in feedback loop is defined according to excess loop delay:

- τ_{d-quan} = 7.812 us (25% T_{clk}),
- τ_{d-DAC} = 9.5 us (30% T_{clk}).

In RZ DAC, α is chosen as 0.25, which is 7.8125 us clock signal delay for comparator. According to Figure 5.13(b), 9.5 us excess loop delay in DAC will degrade 3 dB from SQNR.

With the block failure case setup above, the specification of both minimum design (A_{dc}

= 40, GBW = 96 kHz) and over design (A_{dc} = 40, GBW = 128 kHz) for the loop filter is shown in Table 5.5.

Table 5.5: Reliability analysis ΣΔ modulator with behavioral modeling at system level: block failure case test of ΣΔ modulator. 'Yes' for failure case (at degradation boundary), 'no' for ideal case (no degradation). Building blocks include: 1^{st} integrator, 2^{nd} integrator, quantizer and DAC. $SQNR_1$ is with minimum design case (A_{dc} = 40, GBW = 96 kHz) in loop filter, $SQNR_2$ is with over-design (A_{dc} = 40, GBW = 128 kHz) for two integrators. All the even cases in $SQNR_2$ achieve failure-immunity because of over-design.

case	1^{st} int	2^{nd} int	Quan	DAC	$SQNR_1$(dB)	$SQNR_2$(dB)
0	no	no	no	no	54.6	55.1
1	no	no	no	yes	51.5	49.1
2	no	no	yes	no	54.6	55.1
3	no	no	yes	yes	49.6	49.1
4	no	yes	no	no	43.0	55.1
5	no	yes	no	yes	42.1	49.1
6	no	yes	yes	no	43.1	55.1
7	no	yes	yes	yes	42.1	49.1
8	yes	no	no	no	42.8	54.9
9	yes	no	no	yes	42.0	50.0
10	yes	no	yes	no	42.8	54.9
11	yes	no	yes	yes	42.0	50.0
12	yes	yes	no	no	42.4	54.9
13	yes	yes	no	yes	42.1	49.2
14	yes	yes	yes	no	42.4	54.9
15	yes	yes	yes	yes	42.0	49.2

Table 5.5 summarized 16 test cases used in the failure estimation of CT ΣΔ modulator. SQNR is calculated separately for both minimum design ($SQNR_1$) and over design ($SQNR_2$) modulator. For minimum design, no degradation case happens in case 2 where quantizer fails. Since after noise shaping, internal quantizer locates at the most error-insensitive point among ΣΔ modulator. Also, quantizer benefits from the RZ delay time. In case 1, the excess loop delay accumulated at the DAC will cause 3 dB degradation from the non-failure case. Meanwhile, the most SQNR degradation happened when minimum design integrator fails, there is almost 25% loss of SQNR.

Selective circuit over-design can make excessive guard-band to system reliability. When over-design is used in op-amps (see table 5.6) by increasing GBW with $1^{*}f_s$ = 32 kHz, the op-amps can move away from failure critical state. Figure 5.14 illustrates a bar graph of performance degradation $\Delta = X_0 - X_i$ (includes $SQNR_1$, $SQNR_2$, $SNDR_2$ and $SFDR_2$), where $'X'$ is the performance parameter, $'i'$ is the case index. In all even cases, when failure happens in op-amps (both A_{dc} and GBW are degraded), the system performance can still be guaranteed (DAC is failure, other blocks are in independent assortment). We can find that the most sensitive block is the DAC, there is 6 dB SQNR lost when failure happens in DAC (all odd cases). The SNDR and SFDR of the modulator are also degraded.

Figure 5.15 shows a histogram of Table 5.5 and Table 5.6. From the behavioral modeling of modulator block failure estimation, we can conclude that the reliability aware sequence in low power LP CT ΣΔ modulator is as follow: the reliability performance in loop filter is better than the feedback loop. For each block, by over design of op-amps, the second integrator is better than the first one. With the RZ feedback, the settling time is provided to satisfy the delay and decision time in the comparator. We find that the DAC is the most sensitive block. Its failure can degrade the modulator performance.

Table 5.6: Reliability analysis of ΣΔ modulator with behavioral modeling at system level: block failure case test with over design. Continued from Table 5.5, modulator performance: SNDR and SFDR are included. All the even cases in $SQNR_2$ achieve failure-immunity because of over-design as well.

case	$SQNR_2$(dB)	$SNDR_2$(dB)	$SFDR_2$(dB)
0	55.1	51.7	69.9
1	49.1	46.2	64.0
2	55.1	51.7	69.9
3	49.1	46.2	64.0
4	55.1	52.0	70.4
5	49.1	46.3	62.5
6	55.1	52.0	70.4
7	49.1	46.3	62.5
8	54.9	52.1	70.1
9	50.0	46.6	61.9
10	54.9	51.8	70.0
11	50.0	46.6	62.0
12	54.9	52.0	69.8
13	49.2	46.4	61.2
14	54.9	52.1	67.2
15	49.2	46.4	61.2

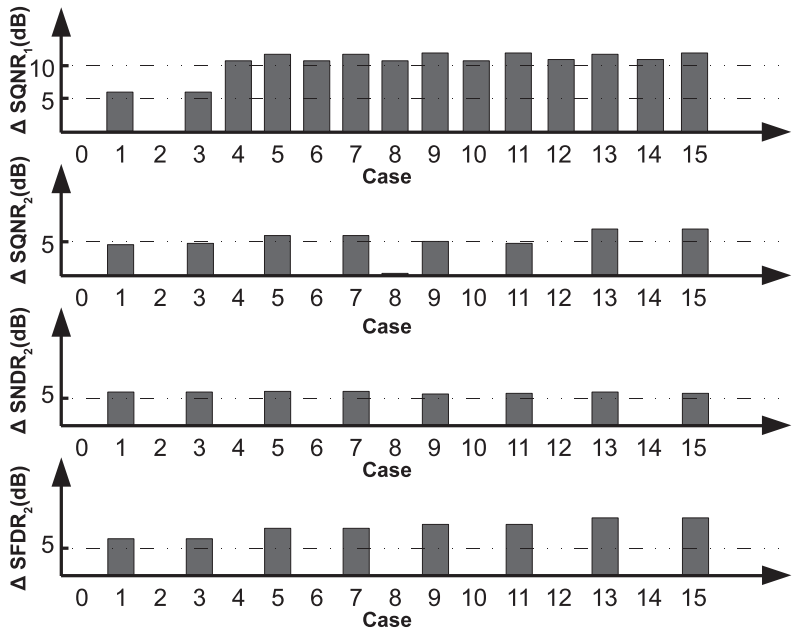


Figure 5.14: Performance degradation versus block failure case by bar graph, $SQNR_1$ (minimum design case) and $SQNR_2$, $SNDR_2$, $SFDR_2$ (over-design case). $\Delta = X_0$ - X_i is the performance parameter, $'i'$ is the case index.

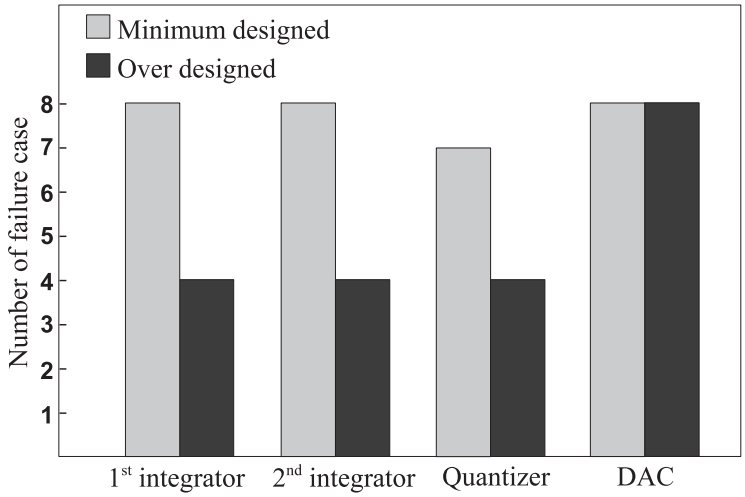


Figure 5.15: Histogram of minimum design and over design

5.3.3.3 Implementation of Analog Loop Filter

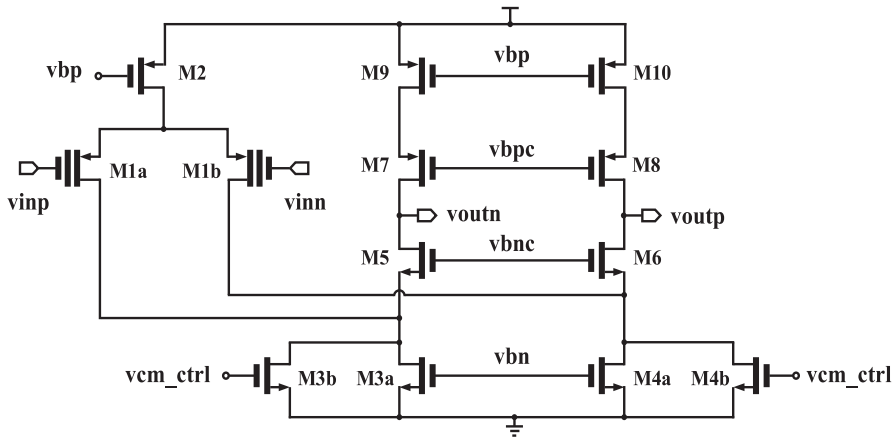
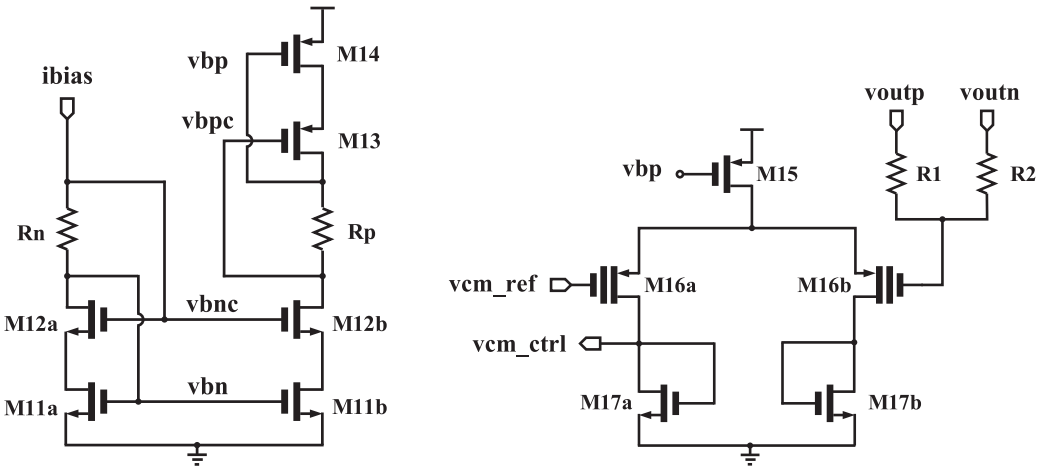


Figure 5.16: Schematic view of the one-stage folded-cascade op-amp

This CT-RZ ΣΔ modulator is designed in 65 nm CMOS technology. The static power consumed by the loop filter contributes more than 95% of the overall power consumed by the modulator. Low-power design is achieved by biasing the transistors in weak-inversion region, where the gate-source voltage is smaller than the threshold voltage ($V_{gs} < V_{th}$). In this application, the requirements DC gain and bandwidth are very relaxed (see results from system level simulation), i.e., $A_0 = 40$ (linear) and $GBW = 3{*}f_s$.

The implementation of building blocks at circuit level includes RC integrator, quantizer, DAC and clock distributor circuit. Active-RC integrator is chosen for the loop filter. Comparing to the telescopic-cascade op-amp, a folded-cascade single stage op-amp is applied because of the larger output swing and easier input common-mode (CM) level. Figure 5.16 illustrates the schematic view of the main circuit. According to the power consumption requirement, only 100 nA biasing current can be allocated to each op-amp. In order to ensure the maximized voltage swing of op-amp input and output, the common-mode input and output voltage are set to 600mV, which is half of the power supply. Thick-gate PMOS transistor (which have higher threshold voltage) M1a and M1b are chosen for the input pair. This is helpful to maximize the input voltage swing, because



(a) The biasing circuit (b) The CMFB circuit

Figure 5.17: The implementation of biasing and CMFB circuits

higher threshold keeps the transistor still working in the weak-inversion region when input voltage becomes larger. The output CM level is defaulted by the common-mode feedback (CMFB) amplifier.

Figure 5.17(a) shows the biasing circuit of designed op-amp. All the biasing voltage levels are generated by only two current-consuming branches (with resistances R_n and R_p). Drain of M12a and gate of M11a are connected together to leave more voltage headroom for the op-amp output, and the same situation with M13 and M14. 10 nA biasing current is set for i_{bias} to minimize the power consumption.

Because of the current mismatches in the real current sources implemented with transistors, the CMFB circuit is needed to fix the output common-mode voltage level to a desired value. Figure 5.17(b) presents the CMFB circuit in use. Equal resistances R1 and R2 forms the resistive divider to sense the output CM voltage. The CM-sense amplifier modeled by a source-coupled pair M16a and M16b, is diode connected loads M17a and M17b. The tail current source M15, follows to detect the difference between the real output CM voltage and the level desired, and returns it to the op-amp.

Simulation results of designed op-amp with biasing and CMFB circuits is presented in Table 5.7. Table 5.8 shows the power consumption allocation in this op-amp.

Table 5.7: Comparison of desired and simulated specifications of the op-amp

Parameter	Desired value	Simulated value
DC gain (linear)	40	46
GBW (kHz)	96	100
Phase margin (degree)	65	83
Current consumed (nA)	100	130

We model the active RC-integrator with the designed op-amp. A transient simulation is performed for analog loop filter. Figure 5.18 shows the output of each integrator.

5.3.3.4 Implementation of Feedback Loop

One bit quantizer is preceded by the high gain loop filter (see dynamic comparator in Figure 4.18). Pre-amplifier based comparator is usually employed in ADC. However, this dynamic comparator can take place of pre-amplifier based one because the former

Table 5.8: Allocation of the power consumption in the op-amp

Circuit part	Current consumption (nA)
Main circuit	80
CMFB	40
Biasing circuit	10
Total	130

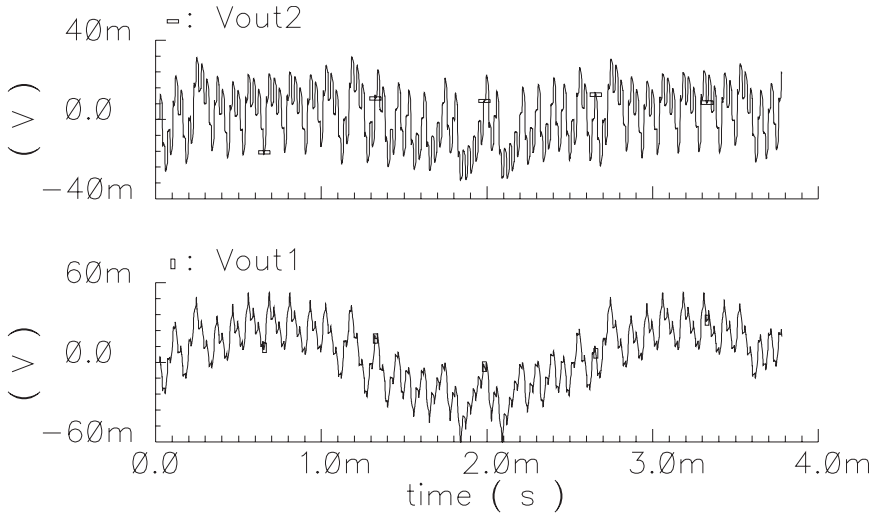


Figure 5.18: Output signal of integrators

consumes much less power due to its periodic operation. Although the nonidealities of the comparator mentioned above will be attenuated by the second-order noise shaping function, quantizer delay (or decision time) should be noticed. Figure 5.19 shows the decision time of comparator, with 0.1 mV differential input signal. Result shows that the decision time is approximately 10 ns, which is lower than the failure condition 7.812 μs mentioned above ($\tau_{d-quan} = 7.812\ us$ (25% T_{clk})).

The RZ DAC is designed using switches which are formed by the transmission gates (see Figure 5.20). Additionally, clock phase generator is included because 0.25 T_s delay (phase 90°) is needed in RZ feedback loop.

5.3.3.5 Achieved Performance

Table 5.9 lists the normal simulated performance of designed low power LP CT ΣΔ modulator at 27°C room temperature. The SNR is measured as 45.3 dB at -6 dBFS sinusoidal input (51.3 dB dynamic range), which is 3.7 dB lower than expected performance. The effective number of bits (ENOB) of the designed modulator is 7.2. Additionally, a two tone test is performed to measure the inter-modulation distortion of 3^{rd}-order harmonics (IM3). As shown in Figure 5.22, with two sinusoidal inputs at two adjacent frequency 397 Hz and 401 Hz, amplitude at -12 $dBFS$, IM3 is simulated at 47.3dB. This value is 1.7 dB lower than expected. Figure 5.21 shows the output spectrum of the designed modulator.

5.3.3.6 Ageing Simulation at Circuit Level

Reliability analysis is performed at 27°C and 150°C. Applying the ageing model with HCI and NBTI mechanisms separately, fifty years ageing degradation is exerted on modulator

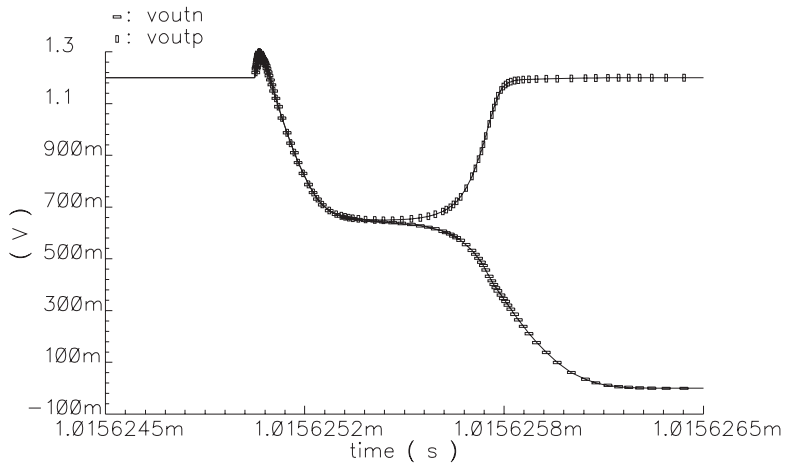


Figure 5.19: Transient simulation of dynamic comparator. The decision time is approximately 10 ns, which is lower than the failure condition 7.812 μs mentioned above (τ_{d-quan} = 7.812 us (25% T_{clk}))

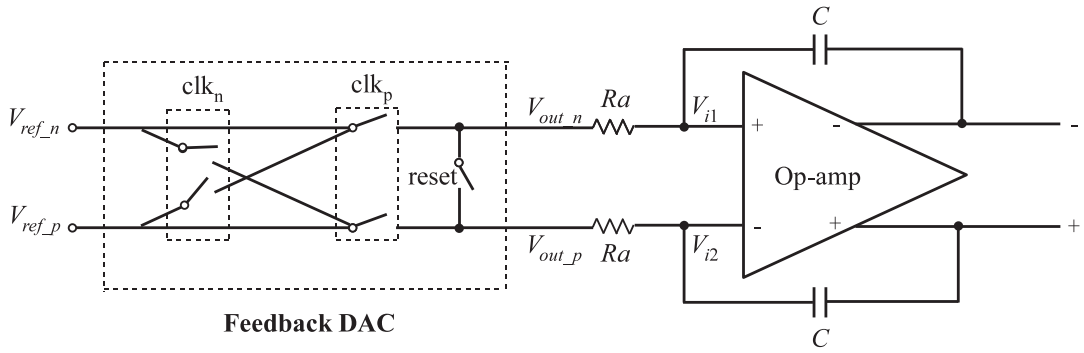


Figure 5.20: Schematic view of 1 bit RZ-DAC, based on transmission gates: Clk_p and Clk_n are generated by the preceding logic. They control the states of the outputs, to be $Vref_p$ - $Vref_n$ or inversely. *Reset* signal shorts two output ports, making the output return to common mode voltage of the amplifier. In order to avoid short circuit happening, all the switches are closed during a certain same period of the clock edges. Thus, nonoverlapping scheme is employed.

Table 5.9: Performance comparison between proposed and achieved

Parameter	Expected	Achieved
SQNR	58 dB	56.7 dB
SNR	49 dB	45.3 dB
ENOB	8 bits	7.2 bits
IM3	49 dB	47.3 dB
Power consumption	200 nA	260 nA

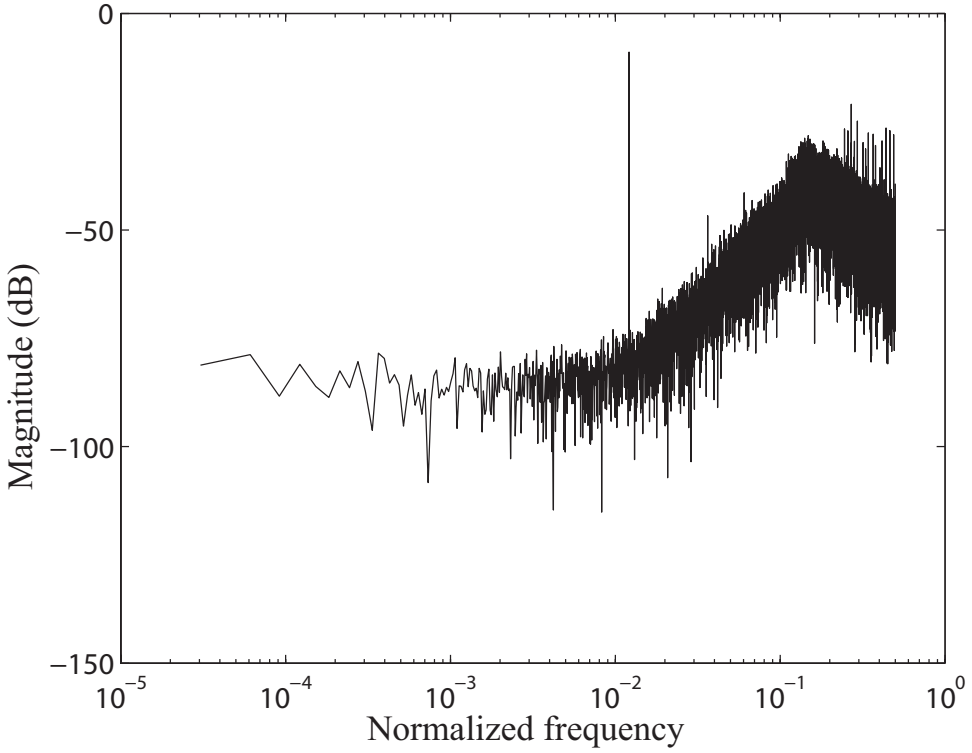


Figure 5.21: Output spectrum of modulator, simulation result based on 65 nm whole transistor platform

building circuits. Table 5.10 contains the simulation result of op-amps.

Table 5.10: Ageing simulation of op-amp

Condition	A_{dc} (dB)	GBW (kHz)	SQNR (dB)
Fresh 27°C	33.5	100	54.5
Fresh 150°C	29.3	72	42.4
Ageing 27°C	33.5	100	54.5
Ageing 150°C	29.3	72	42.4

Comparing the result in Table 5.10, there is no degradation caused by HCI and NBTI after 50 years ageing effect. When at 150°C, it should be mentioned that the performance degradation is cost by V_{th} change due to the high temperature. No SQNR cost by the transistor ageing effect. The main reason is that in ultra low power circuit design, transistors are all working in the weak-inversion region, where is almost no HCI effect due to the gate bias; the NBTI is tiny because of the large dimension PMOS in the op-amps. So the op-amps are reliable in the ageing simulation.

Table 5.11: Ageing simulation of feedback loop

Block	Comparator	DAC	Phase Gen.
τ_d (s)	22.5 p	13.1 p	1 n

For reliability consideration of feedback loop, circuit delay time after ageing is simulated. Table 5.11 show the τ_d of each block after 50 years ageing effect in the feedback

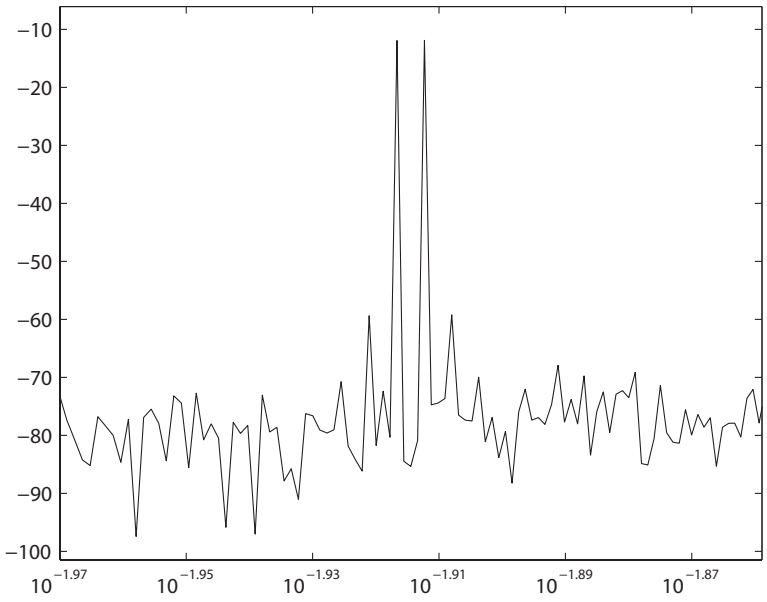


Figure 5.22: Two tone test of the designed modulator. with two sinusoidal inputs at two adjacent frequency 397 Hz and 401 Hz, amplitude at -12 $dBFS$, IM3 is simulated at 47.3dB.

loop. Comparing to 32 kHz clock frequency where $T_{clk} = 31.25\ us$, τ_d caused by HCI and NBTI in comparator and DAC is extremely tiny and can be neglected. The propagation delay in clock phase generator is worse in quantizer and DAC. In this case, 1 ns delay in clock phase generator cost 0.4 dB loss of SNR. Separately, NBTI induced τ_d is larger than HCI induced, especially at 150°C, since NBTI effect is remarkable at high temperature.

In this low power second order LP CT ΣΔ modulator with RZ feedback, ageing problems especially NBTI is prominent at clock generation unit. In loop filter, weak inversion achieved low power and large dimension transistors offer the ageing immunity to modulator. In feedback loop, the RZ mechanism provides clock delay margin to compensate the ageing caused delay. However, the clock phase generator in RZ feedback loop suffers from ageing problems.

5.3.3.7 Statistical Performance with Process Variations

Table 5.12: The significant orders of BSIM4 parameters in one stage folded cascaded op-amp. t_{ox} and v_{th0} are the most dominant BSIM 4 parameters.

	1	2	3	4	5	6	7	8
Folded cascade op-amp	t_{ox}	v_{th0}	u_0	r_{dsw}	n_{dep}	x_w	x_l	n_{fac}

To verify this methodology at system level, we evaluate the performance variation of ΣΔ modulator in terms of process variations. The performance parameter SQNR is considered. RSMs build the link from physical level, via circuit level, to system level. The evaluation of op-amp (see Table 5.12) shows that T_{ox} and V_{th0} are the most critical parameters (with fixed RSM, see Figure 5.23). After behavioral modeling and system

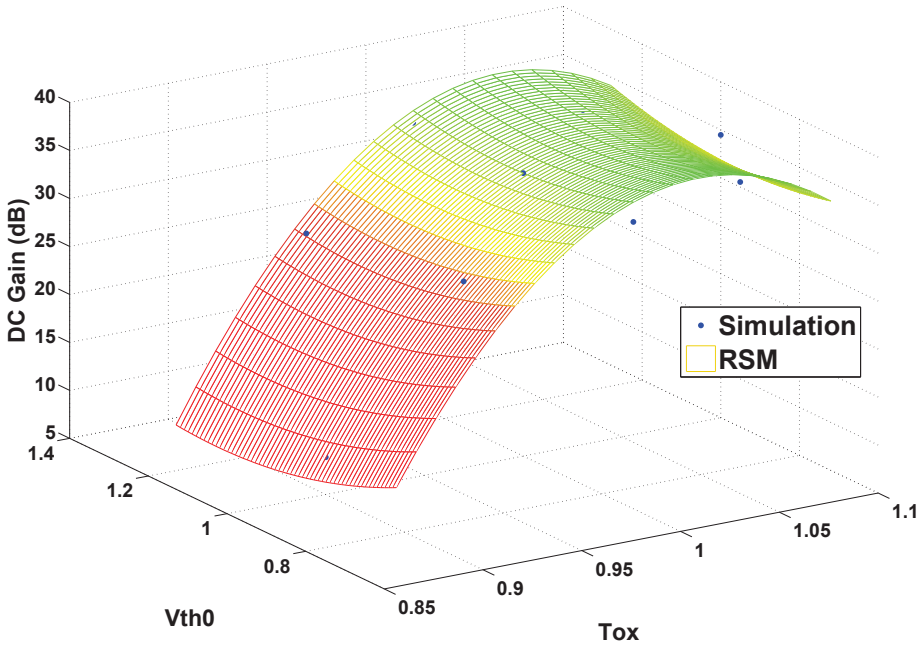


Figure 5.23: Fixed RSM reflects process parameter to op-amp performance

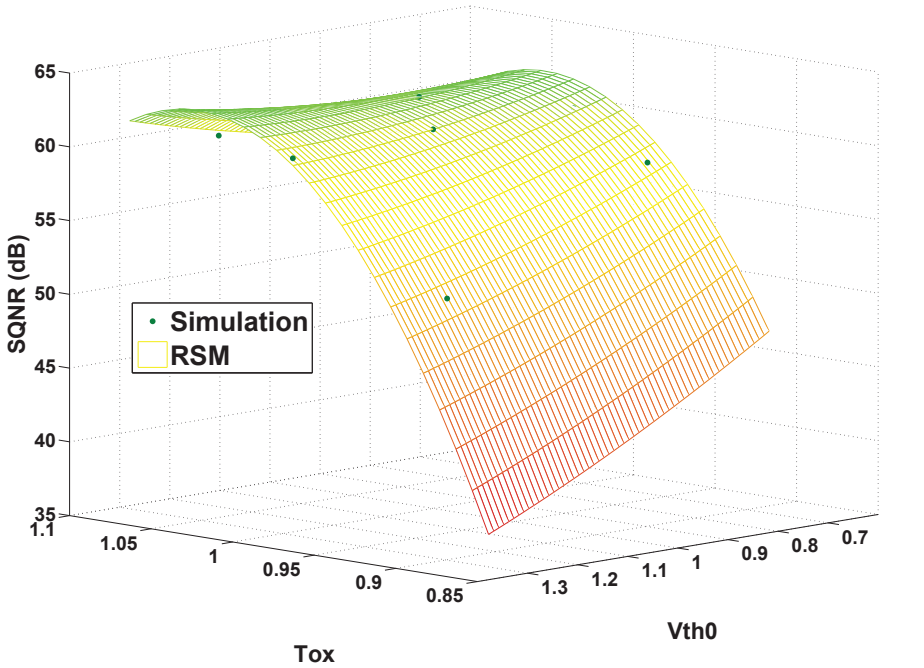


Figure 5.24: Fixed RSM reflects process parameter to ΣΔ modulator performance

level simulation, another fixed RSM is plotted between physical level and system level. Figure 5.24 reflects physical parameters t_{ox} and v_{th0} to SQNR of $\Sigma\Delta$ modulator. We find that the variations of T_{ox} can severely degrade the performance of modulator. A 8% shift of T_{ox} can degrade SQNR from 60.5 dB (ideal case) to 43 dB.

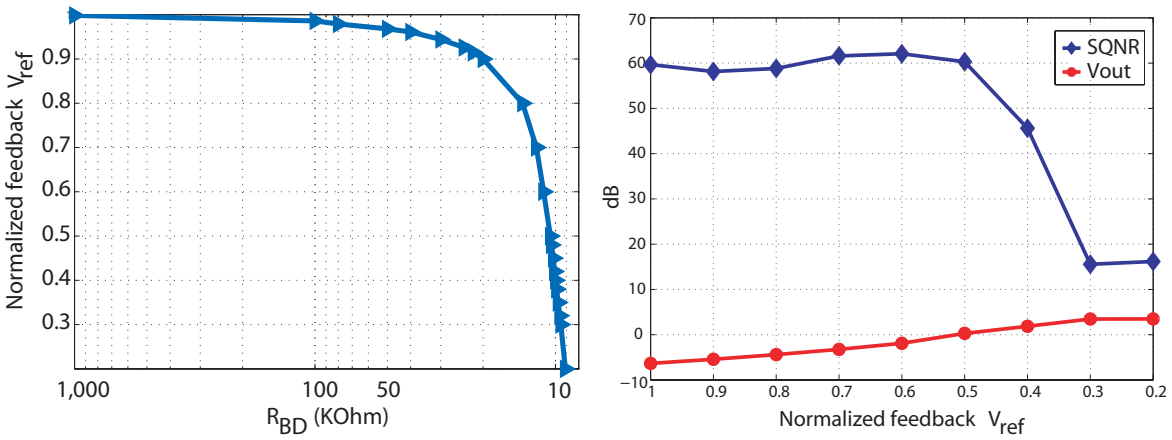
The above extraction flow discussed for op-amp can also be performed on other building blocks in $\Sigma\Delta$ modulator. Results show that RSME between simulation and RSM estimated are 0.54, 0.121, 0.049, with linear, quadratic and cubic model separately. In the view of computation efficiency, it costs 17 runs of circuit level simulation (8 runs to find critical parameters, 9 runs with DoE). With this proposed methodology, in total it takes 45 minutes to get reliability performance (process variations and time dependent ageing degradation) of the designed $\Sigma\Delta$ modulator.

5.3.3.8 A Tentative Study on TDDB

Currently there is no standard tool/method to analyze TDDB mechanism at circuit and system level. For the first time, we simulate TDDB (SBD) mechanism on $\Sigma\Delta$ modulator. The Ohmic model (see Subsection 3.2.2.2) is used to analyze soft breakdown induced performance degradations in $\Sigma\Delta$ modulator. A simple one-bit feedback digital-to-analog converter based on switches is studied. The breakdown causes an increasing of gate current in the degraded transistor, afterwards the breakdown paths (gate-to-source and gate-to-drain) influence the feedback reference voltage V_{ref} in DAC and cause performance degradation of $\Sigma\Delta$ modulator.

Since the SBD is a statistically rare event, only one transistor in switches (see Figure 5.20) is implemented with Ohmic model. The presented result is the worst case of breakdown condition. Figure 5.25(a) illustrates V_{ref} degradation versus different values of SBD resistance R_{BD}. V_{ref} degradation is behavioral modeled in performance simulation of $\Sigma\Delta$ modulator, Figure 5.25(b) presents the SQNR degradation due to V_{ref} changing. The degradation of SQNR starts from half of V_{ref}, which related to the SBD with 22 $k\Omega$ R_{BD} path.

It is a tentative study on TDDB (SBD), because theoretically there is no reference value of R_{BD}. The range of R_{BD} value at $k\Omega$ level is widely accepted in many presented TDDB articles. The designed 2^{nd} order CT $\Sigma\Delta$ modulator is robust to TDDB (SBD) induced V_{ref} degradation.



(a) V_{ref} versus R_{BD}

(b) V_{ref} degradation

Figure 5.25: A tentative study on TDDB mechanism in $\Sigma\Delta$ modulator. TDDB can influence the feedback reference voltage V_{ref} in DAC.

5.3.3.9 Summary

In this work, a second order CT ΣΔ modulator is implemented for cardiac pacemaker, a reliability-aware analysis at both behavioral and transistor level is performed. We conclude that in low power, low order CT ΣΔ modulator, feedback loop is less reliable than analog loop filter. DAC is the most sensitive building block. On the other hand, circuit over-design can enhance system reliability with power tradeoffs. For reliability-aware circuit design, if over-design or redesign is demanded, we can make improvement earlier in the design stage with ageing prediction. Comparing with HCI, NBTI is the dominate effect in the designed CT ΣΔ modulator.

5.3.4 A 125 kHz 3-bit Third-order LP-CT Sigma Delta Modulator

A 125 kHz 3-bit third-order LP-CT Σ Δ modulator is studied in this subsection. It can be used in low power audio and RF applications. Ageing induced jitter effect is concerned in this modulator.

5.3.4.1 Behavioral Modeling

Table 5.13: Expected performance of 3-bits third-order LP-CT ΣΔ modulator

Parameter	Expected
Supply voltage V_{dd}	1 V
OSR	16
Input frequency f_{in}	125 kHz
Clock frequency f_{clk}	4 MHz
Ideal SQNR	82.5 dB
Reference Voltage V_{ref}	0.425 V

A 125 kHz 3-bit third-order LP-CT ΣΔ modulator is designed with ΣΔ toolbox [135], Matlab environment and Verilog-AMS behavioral modeling in Cadence. Table 5.13 lists the specifications. The coefficients of CT modulator are obtained from DT-CT transformation. Noise budget determines the value of passive components (see Table 5.14). This modulator achieves an ideal 82.5 dB SQNR when the input signal amplitude around -3 dBFS.

Table 5.14: Passive components in the loop filter with NRZ-DAC

Ra1	Cint1	Ra2	Rc2	Rg2	Cint2	Ra3	Rc3	Cint3
35 kΩ	12.44 pF	36.7 kΩ	50 kΩ	2.17 MΩ	5 pF	32.86 kΩ	50 kΩ	5 pF

Figure 5.26 shows the designed 3^{rd} order modulator in CIFB architecture (presented in Figure 5.6(a)). Three RC integrators form the analog loop filter. A non-return-to-zero (NRZ) DAC is used in feedback loop. A further study of NBTI effect at system level is made with this 3-bits 3^{rd}-order LP CT ΣΔ modulator. To isolate as much as possible the clock uncertainties impact, all of the other blocks of the modulator are ideal (implemented with Verilog-AMS and macromodels). Figure 5.27 shows the input and output signal of modulator in time domain. Figure 5.28 presents the output spectrum of 3-bit third-order LP-CT Σ Δ modulator.

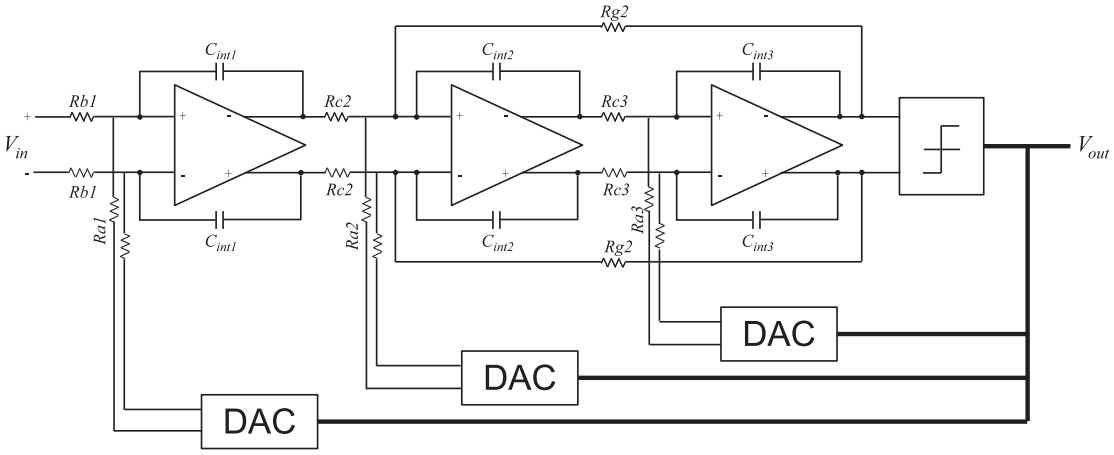


Figure 5.26: The schematic of a differential 3^{rd} active RC CIFB modulator

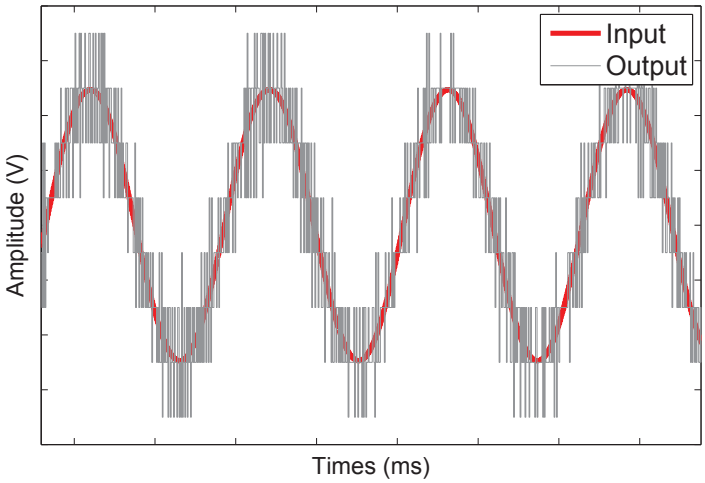


Figure 5.27: Input and output signal of 3 bits 3^{rd} order $\Sigma\Delta$ modulator in time domain

5.3.4.2 NBTI Induced Degradations

With the designed ideal 3 bit 3^{rd} order $\Sigma\Delta$ modulator, ageing mechanisms HCI and NBTI are studied with the proposed bottom-up hierarchical reliability analysis approach (see Subsection 3.4.3.4). CT $\Sigma\Delta$ modulator is less robust against jitter and loop delay compare to their discrete-time (DT) counterparts [142]. Clock distributor is an essential block in CT $\Sigma\Delta$ modulator. All clocked components (e.g., switches, quantizer and digital-to-analog converter (DAC)) are sensitive to clock uncertainty.

Subsection 4.3.3 presented NBTI induced clock skew and jitter in the non-overlapping clock distributor which designed with 65 nm CMOS technology. In order to analysis NBTI induced degradation of modulator, NBTI degradation is propagated: from defect level (NBTI mechanism), via transistor level (V_{th} degradation), through circuit level (NBTI induced clock jitter) and finally gathered at system level. Figure 5.29 shows the hierarchical reliability approach to analyze clock uncertainties in CT $\Sigma\Delta$ modulator.

Previous NBTI simulation results of clock distributor are simulated with other ideal blocks (e.g.,ideal analog loop filter) in modulator system. Behavioral clock signals are setup to non-ideal according to previous NBTI induced jitter (high V_T transistor) and

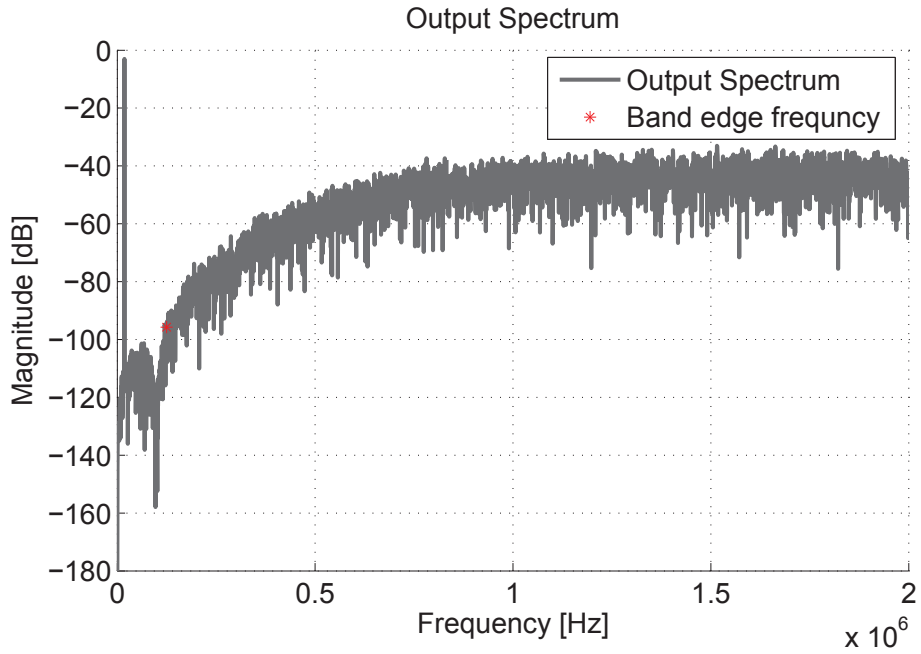


Figure 5.28: Output spectrum of 3-bit third-order LP-CT Sigma Delta Modulator

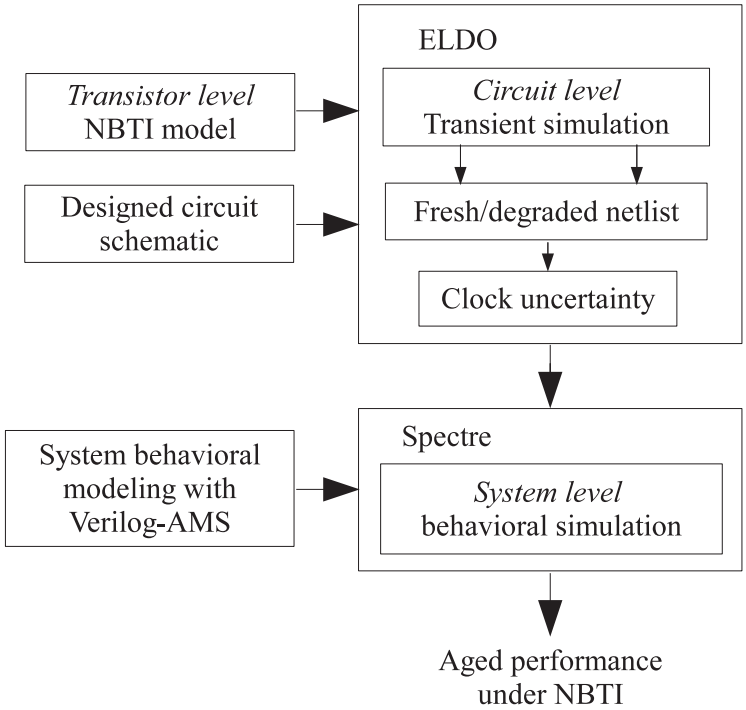


Figure 5.29: The hierarchical reliability approach to analysis clock uncertainties in the CT $\Sigma\Delta$ modulator. Ageing simulation is performed in Eldo. Behavioral level simulation is performed in Spectre.

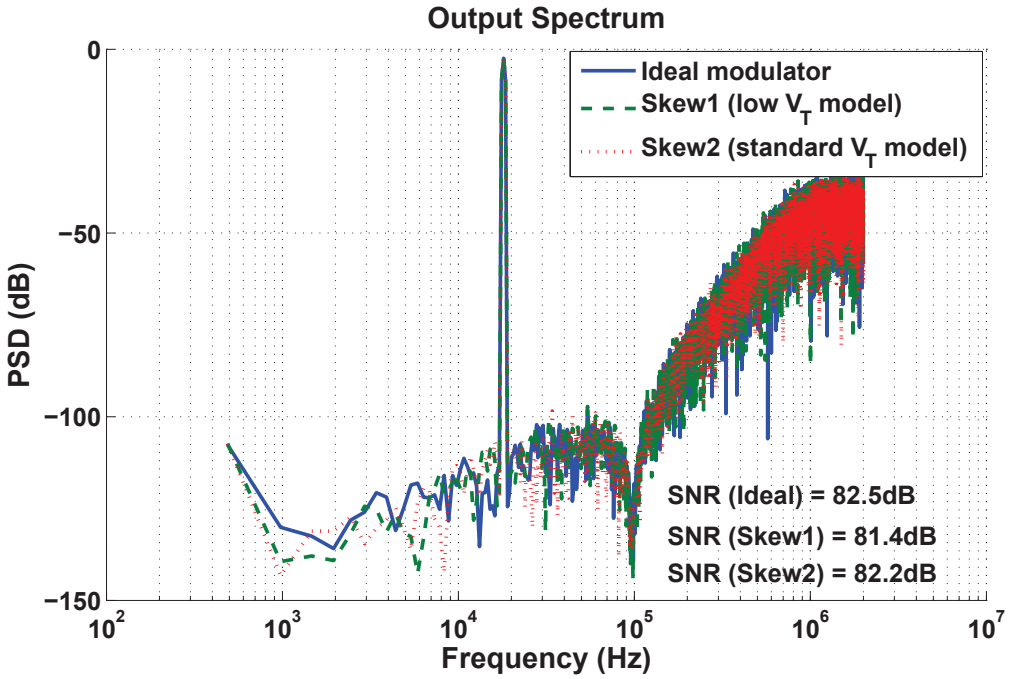


Figure 5.30: NBTI induced clock skews and their effect to modulator output spectrum. Skew1 for low V_T transistor model, skew2 for standard V_T model. NBTI induced skew problems (1 dB performance loss) is tolerable.

skew (standard, low V_T transistor). Skew and jitter effects to modulator spectrums are illustrated in Figure 5.30, 5.31 and 5.32. We can notice that clock skews impact modulator performance slightly. However in Figure 5.32, clock jitters can significantly increase inband noise of spectrum and consequently SNR is severely degraded. Numerically from the hierarchical simulation, a 20 ps clock jitter in 4 MHz clock circuit can reduce SNR from 82.5 dB to only 32.4 dB.

In this work, NBTI induced problems has been bottom-up studied with single PMOS transistor, inverter, clock distributor and a CT $\Sigma\Delta$ modulator. We find that high V_T transistor model is sensitive to NBTI in clock circuits. A hierarchical reliability simulation flow is proposed for large complex AMS circuits and systems. We also demonstrate that in 65 nm CMOS clock distributor circuit, NBTI can cause clock uncertainties in form of clock skews and jitters. It is supposed that the jitter comes from NBTI induced skew which is accumulated through many clock stages in distributor circuit. Furthermore at system level, the performance of CT $\Sigma\Delta$ modulator can be significantly impacted by NBTI induced jitter which happens in its clock distributor.

5.3.4.3 RZ and NRZ Feedback

Since the difference between successive outputs of the modulator are smaller with a multi-bit quantizer, the sensitivity to clock jitter is greatly reduced when compared with a single-bit design.

Comparing to NRZ feedback strategy, RZ feedback has a better tolerance on excess loop delay [142]. However, RZ strategy is more sensitive to clock-jitter effect. Table 5.15 domonstrates the value of passive components in 3-bits modulator (based on noise budget, see Figure 5.26).

Figure 5.33 shows the output spectrums of designed third order LP CT $\Sigma\Delta$ modulator with NRZ and RZ feedback strategy. As shown in Figure 5.34, modulator with NRZ feed-

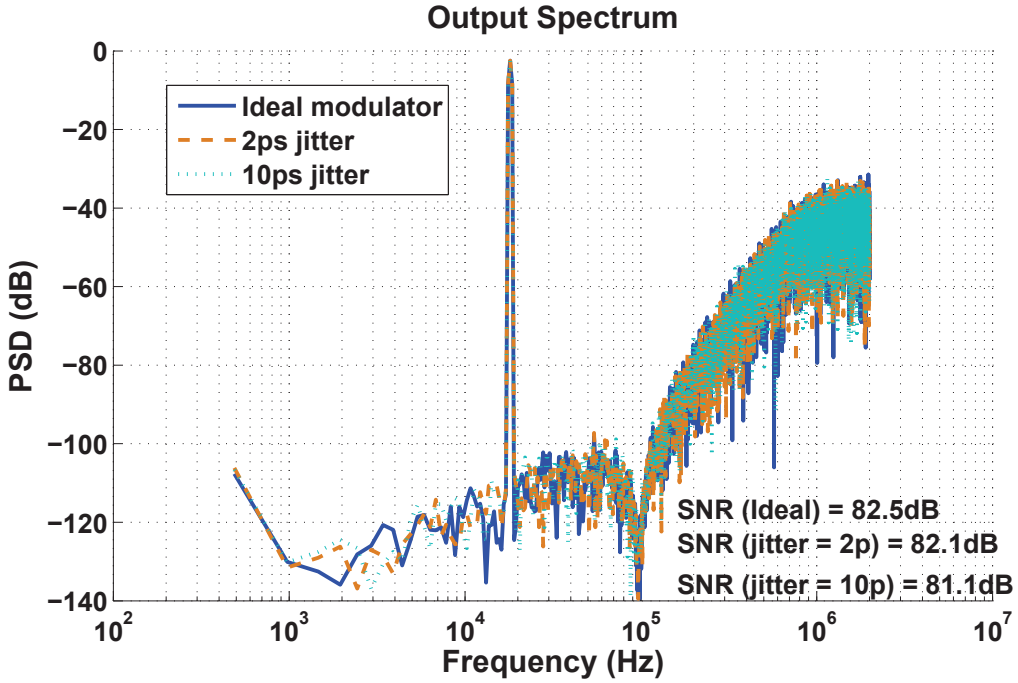


Figure 5.31: Output spectrum: 2 ps and 10 ps jitter can degrade 0.4 dB and 1.4 dB of SNR, separately.

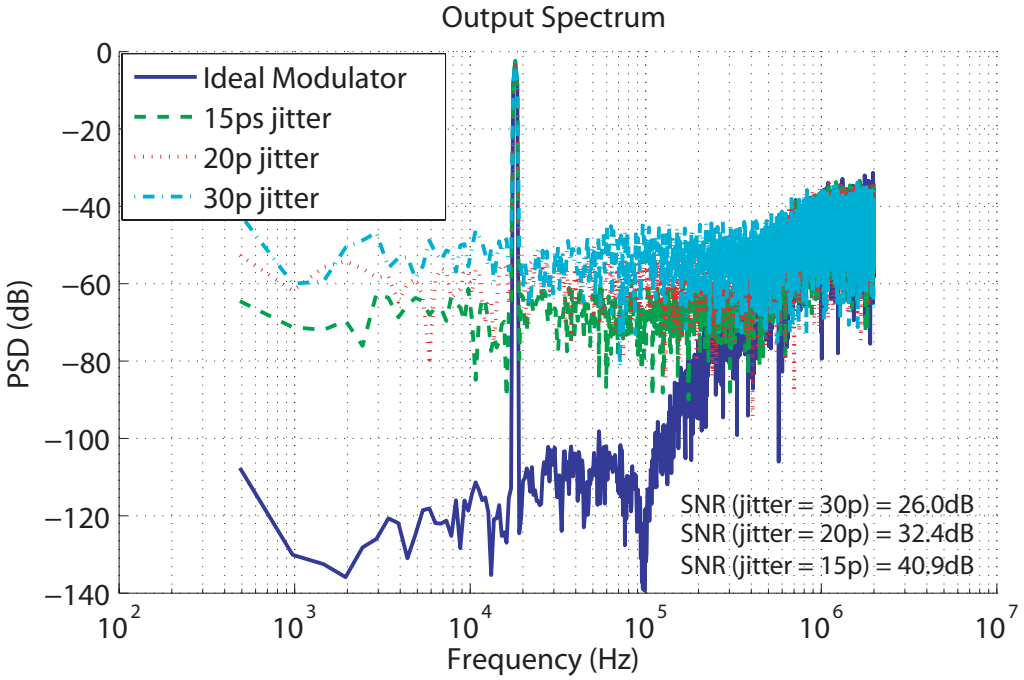


Figure 5.32: Output spectrum: 20 ps jitter refer to simulated jitter level from clock distributor, which can cause 50.1 dB SNR loss. In this modulator with NRZ feedback strategy, 11 ps of jitter is the degradation threshold.

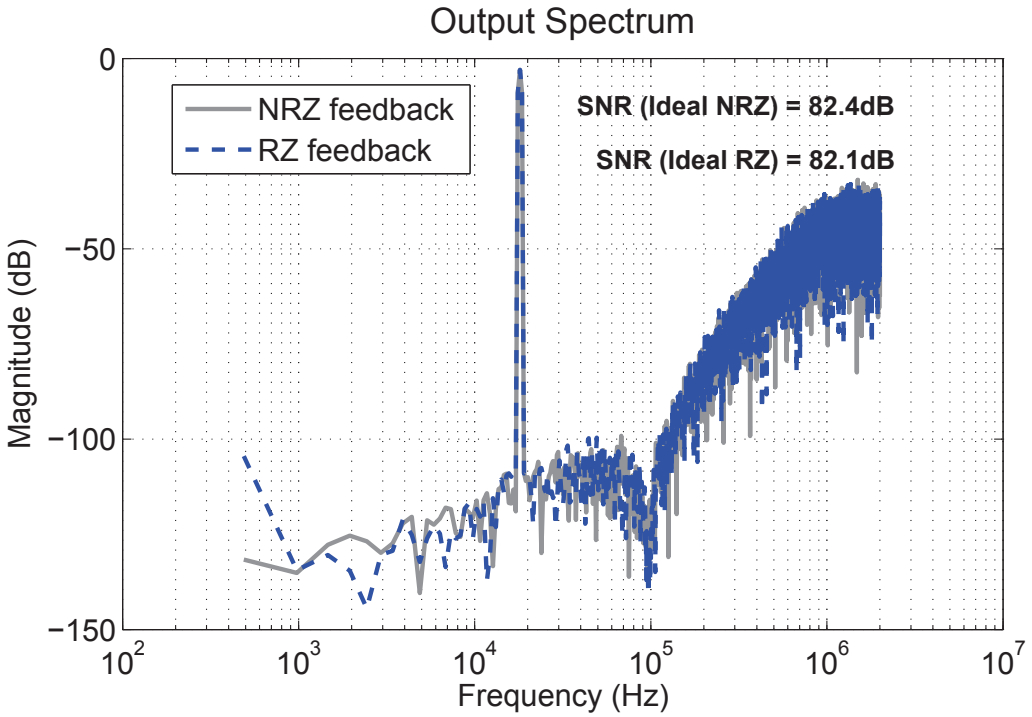


Figure 5.33: Output spectrum of designed 3_{rd} CT modulator, with NRZ and RZ feedback strategies.

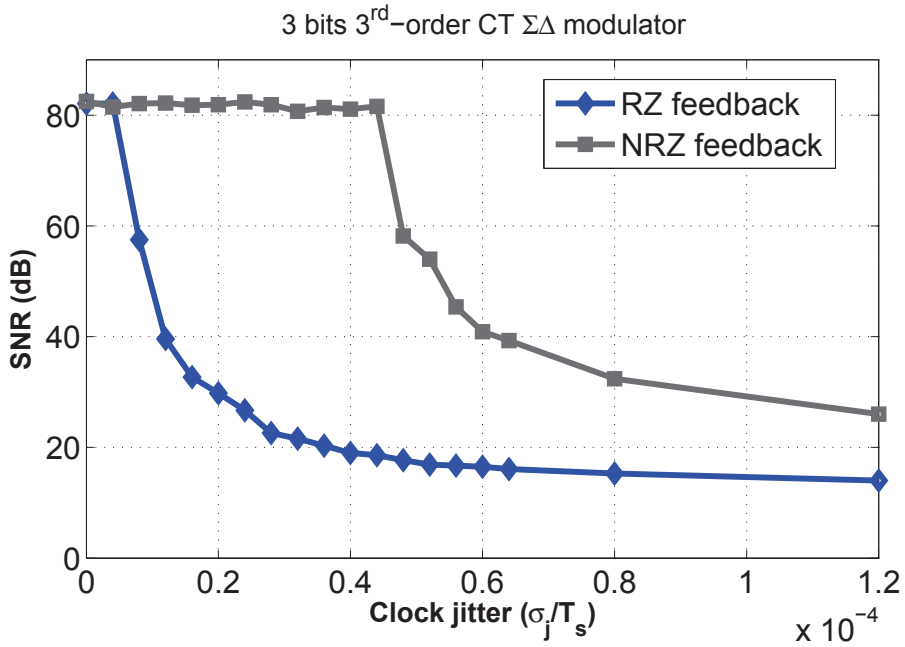


Figure 5.34: Jitter induced performance degradation in RZ and NRZ feedbacks.

Table 5.15: Passive components in the loop filter with RZ-DAC (see Figure 5.26).

Ra1	Cint1	Ra2	Rc2	Rg2	Cint2	Ra3	Rc3	Cint3
17.5 kΩ	12.44 pF	16.6 kΩ	50 kΩ	2.17 MΩ	5 pF	13.17 kΩ	50 kΩ	5 pF

back achieves better tolerance to clock jitter than RZ strategy. In the ageing management approach, clock jitter problems is highlighted.

5.3.4.4 Ageing Managements

Table 5.16: Ageing management of CT ΣΔ modulators

Building block	performance parameters
Loop filter	DC gain, GBW, slew rate, phase margin
Quantizer	delay (decision time)
DAC	excess loop delay, feedback pulse variations
Clock generator	clock uncertainties (clock jitter and skew)

Firstly, ageing management is executed at abstraction level of the ΣΔ modulator. We are interested in circuit sensitivity and failure boundary of each building block in modulator. Table 5.16 lists the critical performance parameters of different building blocks in the CT ΣΔ modulator.

Two important building blocks of CT ΣΔ modulator: analog loop filter and clock distributor, which are failure studied in this section. Figure 5.35(a) and 5.35(b) illustrate SNR loss due to nonidealities of DC gain and Gain-bandwidth product in analog loop filter. DC gain equals to 200 in linear (46 dB) and GBW equals to 20 MHz are selected to satisfy a minimum SNR performance.

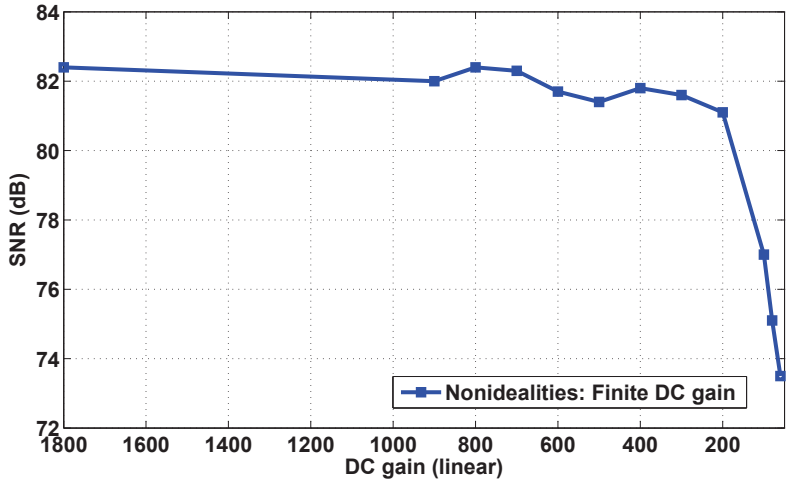
For clock signals which trigger quantizer and DAC, its failure could be clock jitter effects. The performance of this NRZ modulator with 4 MHz clock frequency have jitter tolerance which is less than 11 ps.

As a tentative study, a two stage Miller operational amplifiers are used to compose the analog loop filter in designed CT ΣΔ. The amplifier achieves a DC gain of 48.5 dB and a gain-bandwidth product of 26 MHz. One year ageing simulation with Eldo is performed. HCI and NBTI induced degradations are shown in Table 5.17.

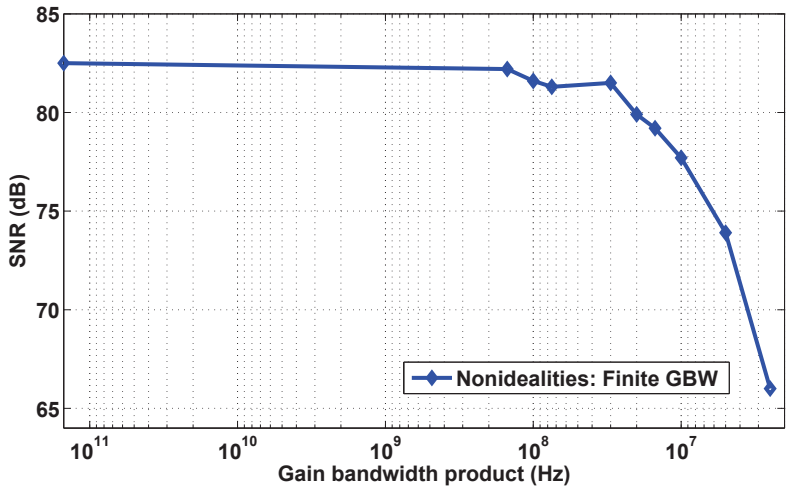
Table 5.17: One year ageing performance in miller op-amp

	DC gain (dB)	Gain-bandwidth (MHz)
Ideal	48.5	26.0
Aged (HCI)	48.4	26.0
Aged (NBTI)	48.1	26.0

The 3-bits 3rd-order LP CT ΣΔ modulator is behavioral modeled with Verilog-AMS language at abstraction level. The performance of designed ΣΔ modulator is obtained with behavioral simulation. Moreover, block sensitivity is evaluated, the failure boundary of performance parameters in each building block is presented in Table 5.18. With these



(a) SNR degradation due to nonidealities DC gain



(b) SNR degradation due to nonidealities GBW

Figure 5.35: Behavioral simulation result at system level: nonidealities of DC gain and Gain-bandwidth product in analog loop filter.

information, reliability (ageing) margins can be properly reserved during circuit design at transistor level.

5.4 Summary of Reliability in Sigma Delta Modulator

It is widely accepted that behavioral level modeling and simulation for $\Sigma\Delta$ modulator is essential in design procedure. In the view of reliability, the hierarchical reliability analysis approach achieves high simulation efficiency for ageing mechanisms. The sensitivity analysis with failure test case at behavioral level highlights the most critical block in modulator systems. From the designers angle of view, reliability issues especially on continuous-time $\Sigma\Delta$ modulator design are discussed in this part.

5.4.1 Loop Filter and Feedback Loop

- Quantizer offset

  Offset is one non-ideality in quantizer. It is caused mainly by parameter deviations

Table 5.18: Ageing management of CT ΣΔ modulators

Building block	Perf. parameters	Influenced by	Failure boundary	Ageing-aware consideration
Loop filter	A_0	NBTI, HCI	46 dB	Amplifier has enough margin to cope with ageing effects
	GBW	N/A	20 MHz	No degradation in GBW
Clk generator	clock jitter	NBTI	11 ps	Modulator with RZ feedback DAC has less jitter margin comparing with NRZ strategy. Designer should avoid using high V_T transistor.
	clock skew	NBTI, HCI	N/A	Low V_T and standard V_T transistor cause clock skew.

of dynamic latch transistors that are connected to the comparator input [143]. Subsection 4.3.5 presented that the dynamic comparator is non-sensitive to HCI and NBTI, process variations can influence the comparator offset. [131] reported that LP modulators are almost insensitive to offset.

- RZ, NRZ and HRZ feedback strategy

  Figure 5.36 illustrates return-to-zero (RZ), non-return-to-zero (NRZ) and half return to zero (HRZ) feedback strategies. From the view of design for reliability, ageing induced additional loop delay and jitter effects should be considered. Due to the increased feedback reference current I_{ref}, HRZ has the highest sensibility to jitter. Nevertheless, the HRZ relaxes the constraints in terms of loop delay since it gives the quantizer an extra time to settle. The NRZ pulse is widely applied because of its lower sensitivity to clock jitter comparing with other feedback strategies.

- Excess Loop Delay

  Excess loop delay arises from the propagation delay time in quantizer, latches, flip-flops, DACs included within ΣΔ modulators. Additional dynamic element matching (DEM) circuits as well as layout parasitic capacitors during layout step are the source of excess loop delay. It can be expressed as a time proportion of the sampling period [141]. The time proportion (see Figure 5.37) is determined by clock frequency, transistor switching speed and number of transistors in the feedback path. In ΣΔ modulator, ageing mechanism NBTI and HCI can degrade the switching speed of transistors in quantizer and feedback DAC. There is an incremental decision time in quantizer and excess loop delay in the whole feedback loop. Figure 5.38 shows excess loop delay with RZ and NRZ feedback. [10] gives a reference ageing induced τ_d at 32 kHz clock signal. A RZ-DAC can successfully compensate this ageing induced loop delay which aids CT ΣΔ modulator to achieve reliability immunity.

- Clock skew and jitter

  Since quantizer is located at the most error insensitive point in the modulator, its nonidealities are noise shaped. The dominant jitter error is caused by the feedback DAC, since the feedback waveform is integrated over time by the loop filter. This increases the in-band-noise thus degrades modulator performance [141] [132]. CT ΣΔ modulators suffer from a critical limitation due to the high sensitivity in feedback DAC to clock jitter. It introduces a random variation in every clock cycle [141]. As a consequence it causes uncertainty in the pulse width of the feedback waveform and hence the integrated values at the outputs of the loop filter integrators.

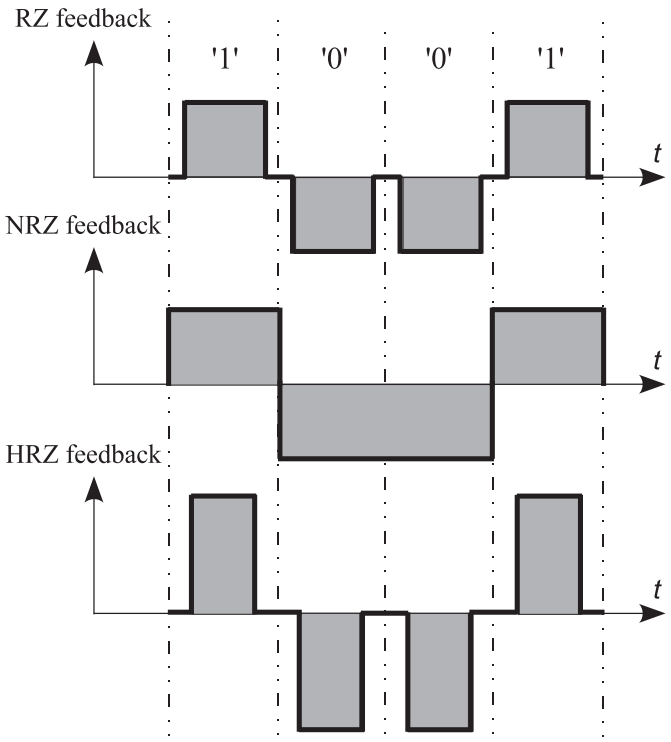


Figure 5.36: The illustration of return to zero (RZ), non return to zero (NRZ) and half return to zero (HRZ) feedback strategies

It is worth mentioning that NBTI effect has non-frequency-dependent characteristic (e.g.,in reaction-diffusion model). NBTI induced clock degradation is more serious in higher frequency application of CT ΣΔ modulators.

- Feedback pulse

  Since degradation of quantizer can be shaped by NTF, ageing induced pulse position and pulse width errors are dominant in the feedback loop. The area of feedback pulse is directly linked to average feedback current (I_{FSI}) of ΣΔ modulators. Where FSI is defined as the maximum average feedback current of the ΣΔ modulators. Correspondingly, FSI in voltage can be defined to be equal to V_{ref}. With a 1.2 V supply voltage, we may take $V_{FSI} = V_{ref} = 0.6\ V_{pk.diff}$. The modulator performance will be affected by relevant V_{ref} as:

$$\begin{aligned} SQNR \approx 1.76 \ + \ 20Log(\frac{V_{in}}{V_{ref}}) \ + \ 6.02n \ + \ 10Log(2L+1) \ - \ 9.9L \\ + \ (6L \ + \ 3)ln_2(OSR) \ - \ 20Log(\pi) \end{aligned} \tag{5.25}$$

  The equation shows that the SQNR of ΣΔ modulator depends on the modulator order L, the number of bits of the quantizer n, the oversampling ratio OSR, the input amplitude V_{in} and reference voltage V_{ref}. As shown in Figure 5.39, the variation of V_{ref} can impact on modulator stability. Both pulse position and pulse width errors can influence V_{ref} and vary the V_{in}/V_{ref}. Small V_{in}/V_{ref} can reduce the simulated SQNR, whereas large V_{in}/V_{ref} can induces a risk to bring the modulator system into the instability region.

  From the simulation result of 2^{nd} order CT ΣΔ modulator [10], it was presented that a 1.5% PW error can cause 1 dB SQNR loss. It has been simulated that

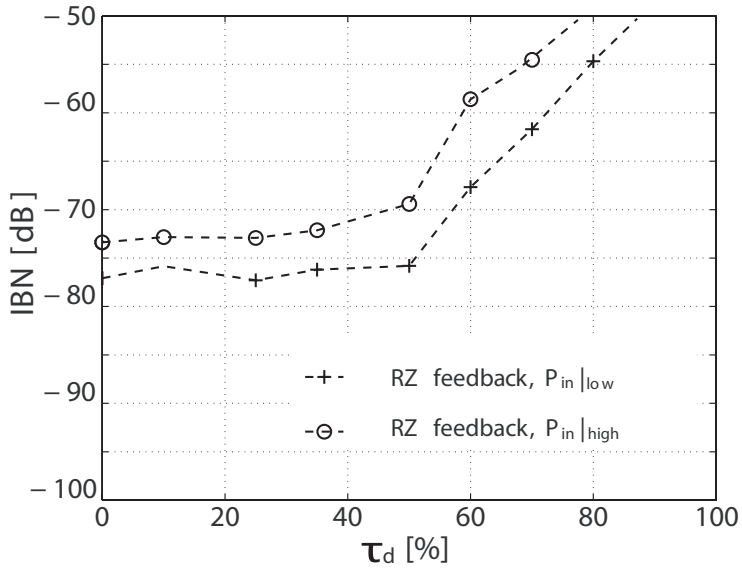


Figure 5.37: The second order CT modulator noise performance with excess loop delay

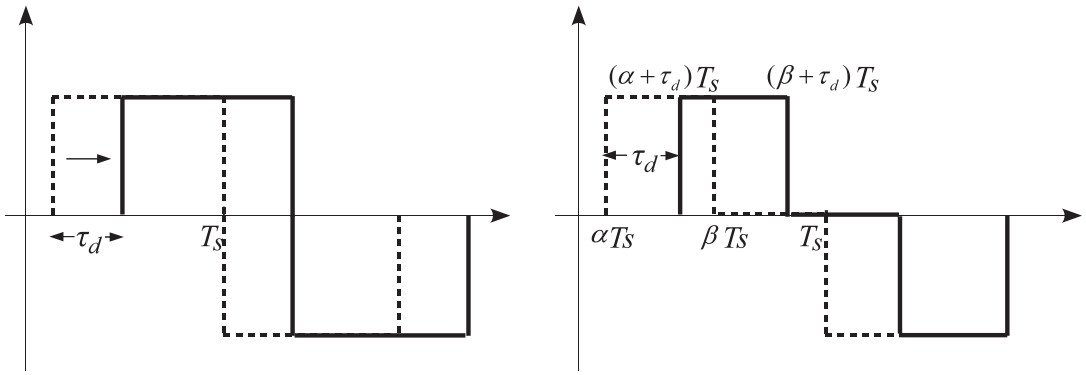


Figure 5.38: Excess loop delay in NRZ and RZ feedback pulse

HCI mechanism influences the rising and falling edge of feedback pulse randomly. As distinct from HCI, NBTI mechanism can narrow the width of feedback pulse as a pulse width error, which can decrease the V_{ref} thereby leading to instability. However, the reliability simulation on transistor level shows that with 1.2 V supply voltage, 150°C, the NBTI degradation caused pulse width error is only 0.25%. So that the modulator system is guaranteed in a reliable margin.

5.4.2 Design Specifications

Now we discuss about why the designed CT ΣΔ modulator has gained such ageing immunity. Weak inversion design of integrator directly achieves insensitivity to HCI mechanisms. As mentioned above, the designed modulator is operated at a 32 kHz clock frequency. If increasing the clock frequency up to 1 MHz or even higher than it, T_{clk} will be at ns to μs level. The excess loop delay (in DAC) and clock phase delay (in clock phase generator) due to the ageing degradation could become principal reliability problems. More serious degradations could occur and degrade the modulator performance.

Figure 5.40 studies SNR with different OSR and op-amp DC gain of a 2^{nd}-order

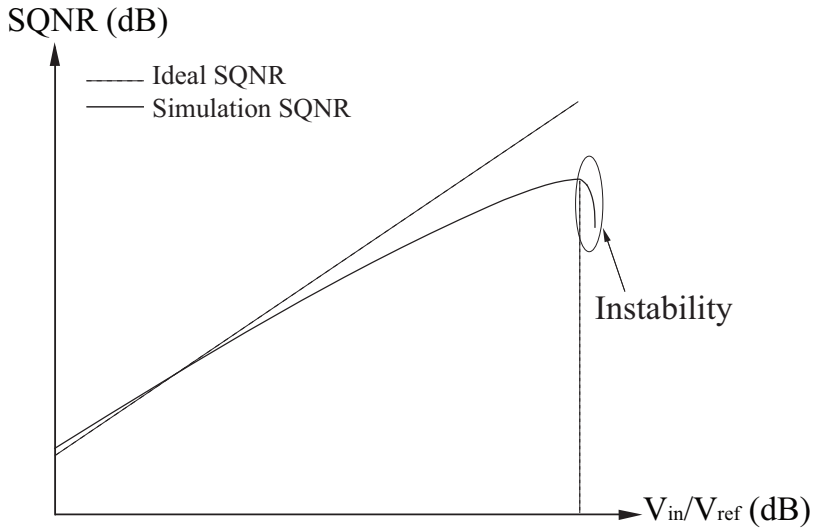


Figure 5.39: V_{ref} degradation can influence modulator stability. Small V_{in}/V_{ref} can reduce the simulated SQNR, whereas large V_{in}/V_{ref} can induces a risk to bring the modulator system into the instability region.

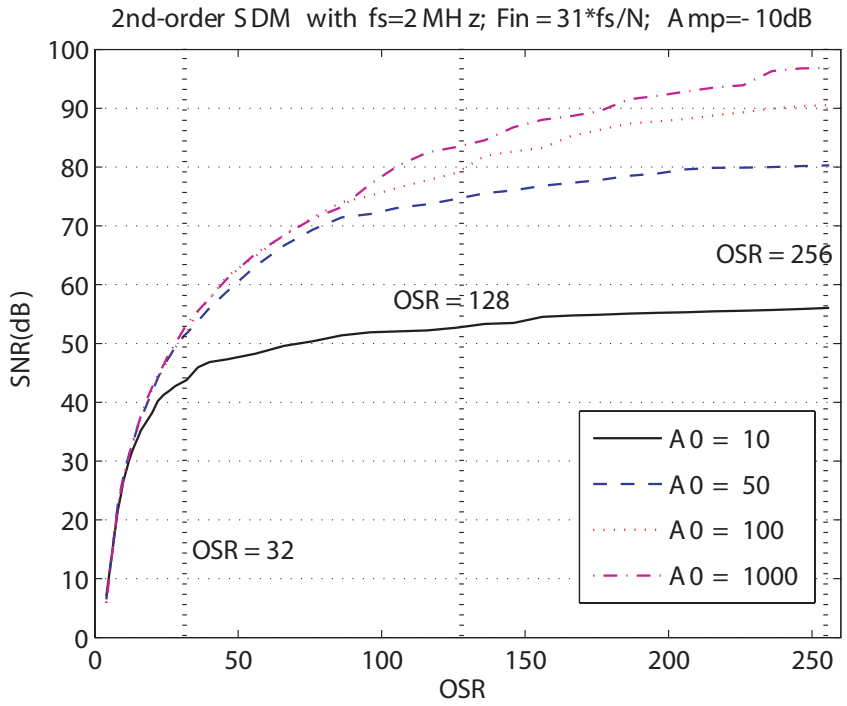


Figure 5.40: SNR with different OSR and op-amp DC gain of a 2^{nd}-order SDM [134].

SDM. The low order loop filter with low OSR gives the designed modulator another point to obtain the minimum ageing effects [134]. The A_{dc} and GBW variation of op-amps in analog loop filter are not evident in low order CT ΣΔ modulator, at OSR of 40 (see Figure 5.12(a) and 5.12(a)). If op-amps suffered from ageing problems, more SQNR degradation will occur with higher OSR (i.e., OSR = 128 or 256), which will contribute distinct SNR variation to the modulator.

In Section 5.3, the designed 2^{nd} order 65 nm LP ΣΔ modulator achieves ageing immunity to HCI and NBTI. The weak inversion bias of transistor not only can be applied to low power design, but also enhance modulator reliability. This study also pointed out that loop filter is more sensitive than analog loop filter. In CT modulator, both quantizer and DAC are clocked. The frequency-dependent ageing mechanism (e.g., NBTI) is important. As the frequency is increased further, the NBTI degradation alleviates significantly.

5.5 Conclusion

Sigma-Delta (ΣΔ) modulators are concerned as the object of reliability study at system level. The design procedure of ΣΔ modulator is presented in this chapter. Reliability-aware methodologies proposed in Chapter 3, include failure analysis, nominal ageing simulation, statistical methods and hierarchical reliability analysis, have been applied to reliability analysis of ΣΔ modulators. An ultra low power 400 Hz second order low-pass continuous-time ΣΔ modulator is designed for cardiac pacemaker application. The reliability study concludes that in low power, low order CT ΣΔ modulator, feedback loop is less reliable than analog loop filter. DAC is the most sensitive building block. Comparing with HCI, NBTI is the dominate effect in the designed CT ΣΔ modulator. Besides, a 125 kHz 3 bits third order CT ΣΔ modulator is implemented to study clock jitter effects. It presents that NBTI mechanism can induce clock jitter in clock distributor for CT ΣΔ modulator. As a consequence, modulator performance is severely degraded due to NBTI effect. Reliability managements of this third order CT modulator is well presented.

Chapter 6

Conclusions and Perspectives

6.1 Conclusions

This thesis work focused on reliability aware issues of CMOS 65 nm AMS integrated circuits and systems, in particular with reliability aware methodologies, reliability simulation and reliability enhancement. The dominant ageing mechanisms HCI and NBTI, as well as process variation were studied and quantitatively evaluated at circuit and system level. The well-known Sigma-Delta modulators were concerned as the object of reliability consideration.

Chapter 2 reviewed the main reliability problems, which include ageing degradation mechanisms, parametric process variations and yield issues. A combined effect of these reliability issues on the performance degradation is significant in sub-90 nm integrated circuits and systems.

Chapter 3 centered on computer-aided reliability methodologies and simulation flow, especially for large and complex AMS circuits and systems. Commercial reliability simulation tools and some reported reliability aware methodologies were studied. Reliability aware approaches were developed during the thesis, such as the hierarchical reliability analysis approach, statistical modeling of process variations, the ideal and aged Pareto fronts, the ageing effects and process variations co-evaluation flow.

Chapter 4 presented simulation results of 65 nm CMOS reliability issues at transistor and circuit level. Some typical 65 nm circuits were designed and studied with reliability-aware methodologies proposed in Chapter 3.

Chapter 5 achieved an intensive study on $\Sigma\Delta$ modulator. First of all, the design flow of $\Sigma\Delta$ modulator were reviewed. Secondly, $\Sigma\Delta$ modulators were implemented at behavioral level and realized at transistor level. Reliability evaluation of modulators were performed with a 2^{nd} order single bit CT-$\Sigma\Delta$ modulator, and a 3^{rd} order three bits CT-$\Sigma\Delta$ modulator. Reliability-aware approaches, e.g, hierarchical reliability analysis approach, the ageing and process variations co-evaluation flow were used in simulations. Furthermore, reliability issues in $\Sigma\Delta$ modulator were technically summarized.

The dominant cue throughout this thesis is: defect modeling, reliability-aware methodologies/approaches, reliability-aware analysis and reliability-aware design. A large portion of this work concentrated on computer-aided methodologies/approaches for reliability. The development of efficient reliability-aware methodologies, which is independent to CMOS technology scaling down, can aid circuit designer to access efficiency reliability simulations.

The reliability problems induced degradation and variation exist in 65 nm CMOS circuits and systems. If only concerning the design loop, the degree is highly dependent on circuit design, e.g., architecture/structure, transistor bias, transistor dimension. At circuit level, careful design (e.g., reserve reliability margin) and accurate reliability simulation

(e.g., with Eldo simulator) can effectively control the reliability degradation.

At system level, the hierarchal reliability methodology is suitable to complex AMS systems. Reliability defects at physical level can be realized at system level, via intermediate transistor and circuit level. In low power, low order CT $\Sigma\Delta$ modulator, feedback loop is less reliable than analog loop filter. DAC is the most sensitive building block. On the other hand, circuit over-design can enhance system reliability with power tradeoffs. For CT $\Sigma\Delta$ modulators, reliability induced clock skew/jitter problems can influence the quantizer and the DAC. CT modulator are very sensitive to these clock uncertainties, especially with RZ feedback. Reliability problems also cause excess loop delay and feedback pulse variations. These problems should be with high attention when designing 65 nm and below CT $\Sigma\Delta$ modulator.

6.2 Perspectives

6.2.1 Co-estimation of Reliability

Currently there is no universal model for different reliability issues in integrated circuits and systems. We need to develop relevant methodologies to complete co-estimations of different reliability problems. There are three main issues that need to be considered: transient faults, ageing effects and process variations.

- Find the relationship between transient faults and transistor physical parameters (e.g., threshold voltage, mobility). From the other point of view, it is also worth finding the statistical approach for ageing effects and process variations.
- Based on our 65 nm design-kit, this co-estimation flow can be implemented with both analog and digital circuits. Practically, this co-estimation methodology can supply reliability information to circuit designers.

6.2.2 Reliability consideration of Sigma-Delta ADCs

Decimation filter is an important part in $\Sigma\Delta$ ADCs. Considering ageing effects and process variations induced degradation in decimation filter, it is valuable to synthesis circuit performance under reliability problems.

- Based on 65 nm design kits, aged netlists can be evaluated at the synthesis step (RTL compiler) in digital design flow.
- Synthesis results: e.g., number of gates, power consumption, critical path, f_{max} are examined at ageing effects and process variations.
- Find out the frangible node with sensitivity analysis. Try to point out design suggestion from the view of reliability considerations.
- Reliability analysis of the whole ADC system. Supply reliability-aware design tips for both analog and digital circuits.

In this thesis, only low-pass CT $\Sigma\Delta$ modulators with RC loop filter in CIFB architecture are reliability-aware studied. It is necessary to evaluate other types of loop filter (e.g., CRFB, CIFF), high order modulators and band-pass, high-pass $\Sigma\Delta$ modulators. The counterpart DT $\Sigma\Delta$ modulators is also interesting to study.

Appendix A

MATLAB Scripts

A.1 MATLAB Scripts: Sigma-delta Modulator

```
clear all
L = 2;        % Order of the loop filter
opt = 1;      % Flag for NTF optimization.
means = 1;    % Number of means (Number of times to average the fft)
nfft = 2^15;  % Number of fft points
len = means * nfft;  % Total length of the data
skip = 1;     % Number of points to skip initial transients

Fin = 400;             % Input signal bandwidth
Fs = 32e3;                % Sampling frequency
OSR = Fs / (2 * Fin);    % Oversampling ratio

f1 = linspace(0, 0.5, nfft/2+1);
fin_edge = round (nfft / (2 * OSR));     % Band edge frequency bin

N = 1;                   % Number of bits in the quantizer
nlev = 2^N;              % Number of quantizer levels
Hinf = 4;                % Maximum gain of the NTF
VrefDac = nlev - 1;      % Reference voltage

AdBFS = -3;
Ampl = VrefDac*10^(AdBFS/20);  % Amplitude of input signal
t = [0 : nfft-1];        % Time vector
u = Ampl*sin(2*pi*Fin/nfft*t);

H = synthesizeNTF (3, OSR, opt, 3.8);
v = simulateDSM (u, H, nlev);
figure(1);
stairs(t, u, 'b-');
hold on
stairs(t, v, 'g-');

window = 1;           %Hann1
figure;
hold on;
```

```
spec=calcScaledfft(v, window, VrefDac);
spec_inband = spec(1 : fin_edge);
snr = calculateSNR(spec_inband(1:401), Fin);
plot(f1, dbv(spec(1:nfft/2+1)),'r-');
grid on
title('Output Spectrum');
xlabel('Frequency (Hz)');
ylabel('Magnitude (dB)');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%        Dynamic range scaling of the modulator         %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

form = 'CIFB';
[a,g,b,c] = realizeNTF(H,form);
b(2:end) = 0; % for a maximally flat STF

abcd = stuffABCD(a,g,b,c,form);
[ntf,stf] = calculateTF(abcd);
magntf = dbv(evalTF(ntf,z));
figure
plot(f,magntf,'m-',f,magstf,'c-','Linewidth',2);
legend('NTF','STF');

xlim = 0.4;
f0 = 0;
[abcds,umax] = scaleABCD(abcd,nlev,f0,xlim);
[a1,g1,b1,c1] = mapABCD(abcds,form);
```

A.2 MATLAB Scripts: Decimation Filter

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%       Demonstration of filtering and decimation       %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all
open_system('DSADC')
N = 32768;          % Number of fft points
D = 8;              % Decimation factor
fNorm = 32000;      % Frequency normalization factor
k = 396;            % Number of periods of the input signal (an integer)
freq = 2*pi*k/N;    % Calculate the frequency of the input signal

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%             Prepare and start simulation              %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

options=simset('InitialStep', 1, 'RelTol', 1e-3, 'MaxStep', 1,...
    'Fixedstep', 1);
```

```
sim('DSADC');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                  Calculate the spectras                                 %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Use the function calcfft to calculate the spectras
spec1 = calcfft(out.signals.values');
% Spectre without decimation filter
spec2 = calcfft(outfilt8.signals.values');
% Output spectre of Sinc3 filter
spec3 = calcfft(outfilt.signals.values');
% Output spectre of first stage decimator
spec4 = calcfft(outdec.signals.values');
% Output spectre of second stage decimator
spec5 = calcfft(outdec1.signals.values');
% Final output
y = outdec1.signals.values';

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                   Plot the results                                      %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

n = 0 : N / 2 - 1;
fn = n * (fNorm / N);

figure(1)
plot(fn,20*log10(spec1),fn,20*log10(spec2))
grid

figure(2)
plot(fn,20*log10(spec1),fn,20*log10(spec3))
grid

figure(3)
plot(fn(1:N/D/2/2),20*log10(spec4))
grid

figure(4)
plot(fn(1:N/D/2/2/2),20*log10(spec5))
grid
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%                       Calculate SNR                                     %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Sort out the inband bins
spec1_inband = spec1(1:513);
spec2_inband = spec2(1:513);
spec4_inband = spec4(1:513);
spec5_inband = spec5(1:512);
```

```
% Calculate the SNR in band
SNRunfilt = calculateSNR(spec1_inband,396)
SNRfilt = calculateSNR(spec4_inband,396)
SNRfilt1 = calculateSNR(spec5_inband,396)

dlmwrite('D:\sim\data.txt', y);   % Save date
```

Appendix B

The block diagram of Sigma-Delta ADC in Simulink

B.1 Simulink

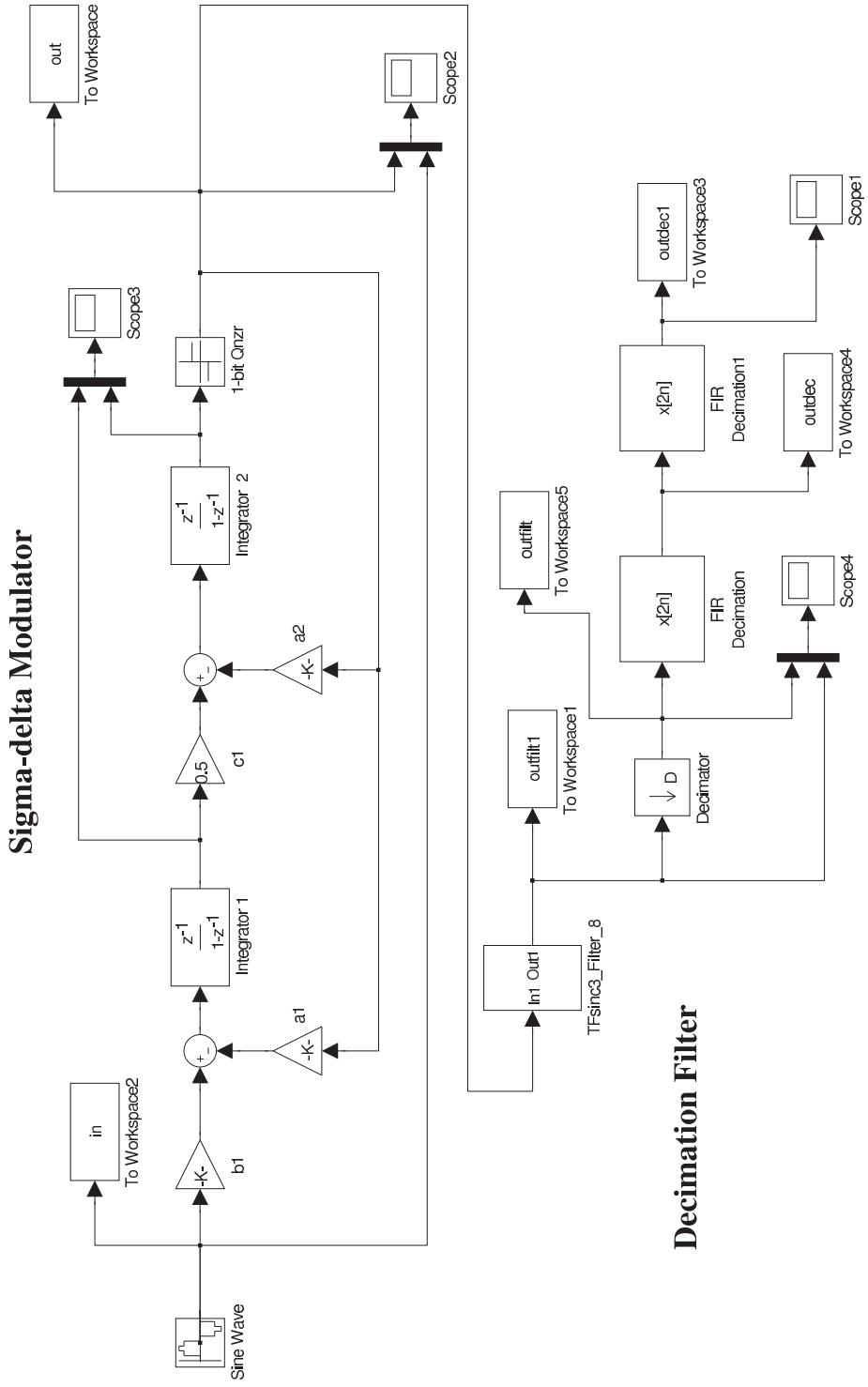


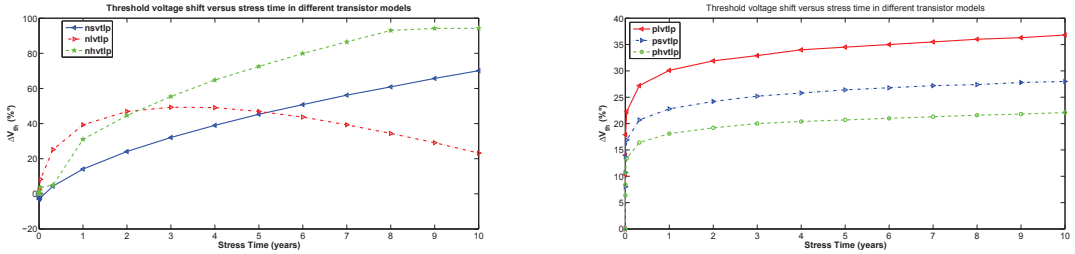
Figure B.1: The block diagram of Sigma-Delta ADC designed with $Simulink^{TM}$

Appendix C

Time-dependent ageing study of 65 nm NMOS/PMOS transistors

HCI and NBTI effects are studied at transistor level. Parameters degradation of NMOS transistors are caused by HCI. For PMOS transistor, NBTI is the dominated degradation. The test environment is $V_{ds} = V_{gs} = 1.2$ V (absolute value in PMOS transistor) at room temperature ($27°C$). A ten years ageing degradation is setup to study V_{th} (threshold voltage, see Figure C.1(a) C.1(b)), I_d (drain current, see Figure C.2(a) C.2(b)) and g_m (transconductance, see Figure C.3(a) C.3(b))

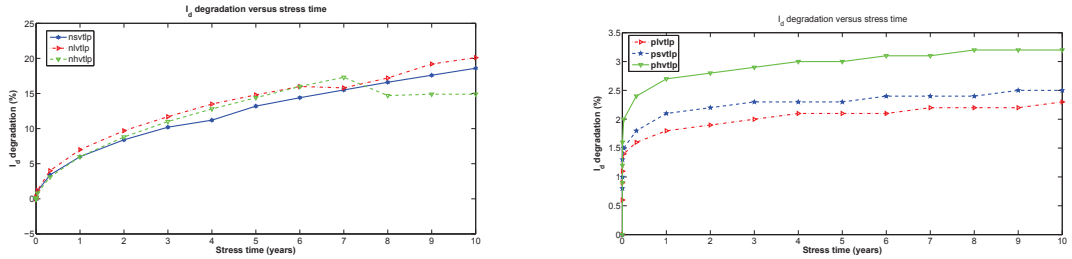
These simulation results figure out that degradation speed is fast in the initial degradation time. With the stress time increasing, the speed is slow down. We also find that low-V_{th} transistors suffer more V_{th} degradation than other two types. In mixed circuits, using low-V_{th} transistor will cause larger ageing degradation than other two types. On the other hand, we find HCI caused I_d degradation in NMOS is worse than NBTI in PMOS at room temperature. HCI caused g_m shift in NMOS is larger than NBTI caused in PMOS. Threshold voltage is decreased when temperature goes up. In 65 nm CMOS technology, the threshold temperature dependence $dVth/dt = -0.55mV/\circ C$. When environment temperature is increased, V_{th} will decrease. However the NBTI degradation will be worse. Figure C.4(a) C.4(b) and Figure C.5(a) C.5(b) show the V_{th} and I_d degradation at $150°C$ for ten years of ageing degradation. At high temperature ($150°C$), HCI effect to NMOS is weaker than at room temperature, reflect from V_{th} and I_d. The degradation rate caused by NBTI effect to PMOS is increased several times over $27°C$.



(a) HCI induced V_{th} degradation

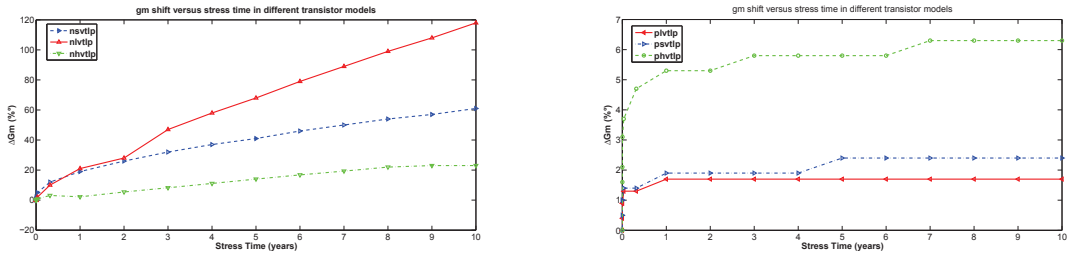
(b) NBTI induced V_{th} degradation

Figure C.1: Time-dependent V_{th} degradation of signal NMOS and PMOS in low V_t, standard V_t and high V_t type. The HCI degradation trend in *nlvtlp* is irregular.



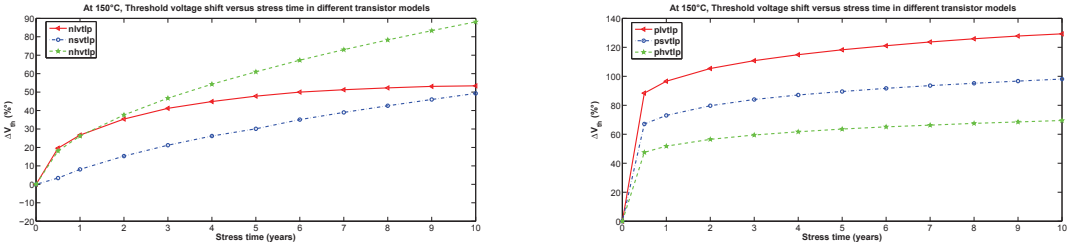
(a) HCI induced I_d degradation (b) NBTI induced I_d degradation

Figure C.2: Time-dependent I_d degradation of signal NMOS and PMOS in low V_t, standard V_t and high V_t type.



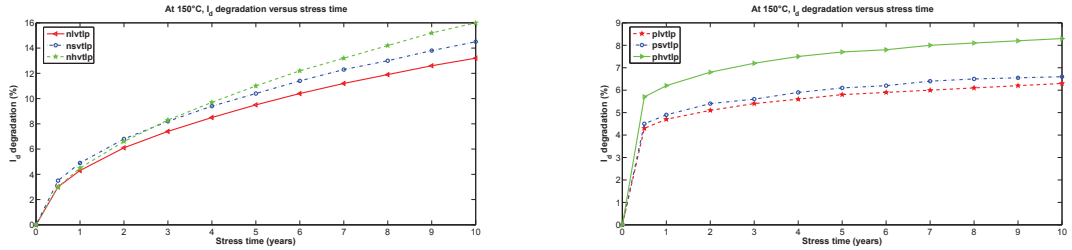
(a) HCI induced gm degradation (b) NBTI induced gm degradation

Figure C.3: Time-dependent g_m degradation of signal NMOS and PMOS in low V_t, standard V_t and high V_t type.



(a) HCI induced V_{th} degradation at $150°C$ (b) NBTI induced V_{th} degradation at $150°C$

Figure C.4: Aged transistor at high temperature, V_{th}.



(a) HCI induced I_d degradation at $150°C$ (b) NBTI induced I_d degradation at $150°C$

Figure C.5: Aged transistor at high temperature, I_d.

Appendix D

Correlation analysis of BSIM4 parameters

- t_{ox}: or t_{oxe}, electrical gate equivalent oxide thickness,
- n_{dep}: Channel doping concentration at depletion edge for zero body bias,
- r_{sh}: Source/drain sheet resistance,
- r_{shg}: Gate electrode sheet resistance,
- v_{tho}: Threshold voltage at v_{bs}=0 for long-channel devices,
- u_0: Low-field surface mobility at tnom,
- n_f: n_{factor}, subthreshold swing coefficient,
- r_{dsw}: Zero bias LDD resistance per unit width for RDSMOD=0,
- c_f: Fringing field capacitance,
- x_l: Length variation due to masking and etching,
- x_w: Width variation due to masking and etching,
- jsw: $jsws$, isolation-edge sidewall source junction reverse saturation current density,
- c_j: Zero bias bottom junction capacitance per unit area,
- c_{jsw}: Sidewall junction capacitance per unit periphery,
- c_{jg}: c_{jswg}, gate-side junction capacitance per unit width.

	t_{oxe}	n_{dep}	r_{sh}	r_{shg}	v_{tho}	u_0	n_{factor}	r_{dsw}	c_f	x_l	x_w	$jsws$	c_j	c_{jsw}	c_{jswg}
t_{oxe}	NaN	0	0	-0.022	0	-0.0045	-0.0197	0	0.0005	0	0	0	0	0	0
n_{dep}	0	NaN	0	-0.016	0	-0.0035	-0.0038	0	-0.1171	0	0	0	0	0	0
r_{sh}	0	0	NaN	0.036	0	-0.0045	0.0378	0	-0.0024	0	0	0	0	0	0
r_{shg}	-0.022	-0.016	0.036	NaN	0.0526	0.0065	-0.024	-0.0223	0.1359	-0.0126	-0.0479	0.0129	-0.041	-0.0156	0.0322
v_{tho}	0	0	0	0.0526	NaN	-0.0045	0.0226	0	0.0024	0	0	0	0	0	0
u_0	-0.0045	-0.0035	-0.0045	0.0065	-0.0045	NaN	0.0205	-0.0125	-0.0908	0.05	0.0045	-0.0125	0.0045	-0.0125	0.0045
n_{factor}	-0.0197	-0.0038	0.0378	-0.024	0.0226	0.0205	NaN	0.0351	0.0892	0.0575	-0.041	-0.0168	-0.0361	-0.0355	0.0226
r_{dsw}	0	0	0	-0.0223	0	-0.0125	0.0351	NaN	0.0226	0	0	0	0	0	0
c_f	0.0005	-0.1171	-0.0024	0.1359	0.0024	-0.0908	0.0892	0.0226	NaN	0.3866	-0.2304	-0.0024	0.1219	-0.2366	0.1175
x_l	0	0	0	-0.0126	0	0.05	0.0575	0	0.3866	NaN	0	0	0	0	0
x_w	0	0	0	-0.0479	0	0.0045	-0.041	0	-0.2304	0	NaN	0	0	0	-0.0018
$jsws$	0	0	0	0.0129	0	-0.0125	-0.0168	0	-0.0024	0	0	NaN	0	0	0
c_j	0	0	0	-0.041	0	0.0045	-0.0361	0	0.1219	0	0	0	NaN	0	0
c_{jsw}	0	0	0	-0.0156	0	-0.0125	-0.0355	0	-0.2366	0	0	0	0	NaN	0
c_{jswg}	0	0	0	0.0322	0	0.0045	0.0226	0	0.1175	0	-0.0018	0	0	0	NaN

Appendix E

Matlab Scripts for Statistical Analysis

```
uiopen('INPUT.dat');
Vth0=INPUT(:,1)
Xl=INPUT(:,2)
Tox=INPUT(:,3)
A0=INPUT(:,4)
one=ones(length(A0),1)
X=[Vth0,Xl,Tox,one]
x1=Vth0
x2=Xl
x3=Tox
X1=[x1,x2,x3,one];
X2=[x1.*x1,x1.*x2,x1.*x3,x2.*x2,x2.*x3,x3.*x3,X1];
X3=[x1.^3,x1.^2.*x2,x2.^2.*x1,x2.^3,x1.^2.*x3,
x3.*x2.*x1,x2.^2.*x3,x3.^2.*x1,x3.^2.*x2,x3.^3,X2];
[B,BINT,R,RINT,STATS] = regress(A0,X3)     %regression analysis
plot(X3*B, A0,'o')
table = [X3*B,A0,(A0-X3*B)./A0];
x1fit = min(x1):0.01:max(x1);
x2fit = min(x2):1E-10:max(x2);
[X1FIT,X2FIT] = meshgrid(x1fit,x2fit);

X = [ones(size(x1)) x1 x2 x1.*x2 x1.^2 x2.^2];
b = regress(A0,X)
YFIT = b(1)+b(2)*X1FIT+b(3)*X2FIT+b(4)*X1FIT.*X2FIT+b(5)*X1FIT.^2+
       b(6)*X2FIT.^2

scatter3(x1,x2,A0,'filled')
hold on

mesh(X1FIT,X2FIT,YFIT)            %plot response surface
xlabel('Vth0')
ylabel('length variation')
zlabel('A0')
```

Bibliography

[1] [Online] www.itrs.net/Links/2011ITRS/Home2011.htm. International technology roadmap for semiconductors (ITRS), 2011.

[2] Ping Yang and Jue-Hsien Chern. Design for reliability: the major challenge for VLSI. *Proceedings of the IEEE*, 81(5):730–744, 1993.

[3] B.E. Boser and B.A. Wooley. The design of sigma-delta modulation analog-to-digital converters. *Solid-State Circuits, IEEE Journal of*, 23(6):1298–1308, 1988.

[4] A. Gerosa, A. Maniero, and A. Neviani. A fully integrated two-channel a/d interface for the acquisition of cardiac signals in implantable pacemakers. *Solid-State Circuits, IEEE Journal of*, 39(7):1083–1093, 2004.

[5] M. White and Bernstein J. B. Microelectronics reliability: Physics-of-failure based modeling and lifetime evaluation. NASA technical report JPL Publication 08-5 2/08, Jet Propulsion Laboratory, 2008.

[6] H. Iwai. Roadmap for 22nm and beyond (invited paper). *Microelectron. Eng.*, 86(7-9):1520–1528, July 2009.

[7] L. Oshiro and R. Radojcic. A design reliability methodology for CMOS VLSI circuits. *Integrated Reliability Workshop, 1995. Final Report., International*, pages 34–39, 1995.

[8] Milos Stanisavljevic, Alexandre Schmid, and Yusuf Leblebici. *Reliability of Nanoscale Circuits and Systems - Methodologies and Circuit Architectures*. Springer, first edition, 2011.

[9] [Online] http://ieeexplore.ieee.org/Xplore. IEEE digital library, 2013.

[10] H. Cai, H. Petit, and J.-F. Naviner. Reliability aware design of low power continuous-time sigma-delta modulator. *Microelectronics Reliability*, 51(9-11):1449–1453, 2011.

[11] H. Cai, H. Petit, and J.-F. Naviner. A hierarchical reliability simulation methodology for AMS integrated circuits and systems. *Journal of Low Power Electron*, 8(5):697–705, 2012.

[12] H. Cai, H. Petit, and J.-F. Naviner. A statistical method for transistor ageing and process variation applied to reliability simulation. In *3rd European Workshop on CMOS variability*, pages 49–52, 2012.

[13] H. Cai, H. Petit, and J.-F. Naviner. Computer-aided reliability-aware approach for analog/mixed integrated circuits and systems. In *Journées Nationales du Réseau Doctoral de Microélectronique (JNRDM)*, 2013.

[14] H. Cai, H. Petit, and J.-F. Naviner. A fast reliability-aware approach for analogue integrated circuits based on pareto fronts. In *New Circuits and Systems Conference (NEWCAS), 2013 IEEE 11th International*, 2013.

[15] H. Cai, H. Petit, and J.-F. Naviner. NBTI effects on clock uncertainty and applications in continuous-time sigma-delta modulator. In *EdaWorkshop 13*, pages 7–12, 2013.

[16] H. Cai, H. Petit, and J.-F. Naviner. Reliability analysis of continuous-time sigma-delta modulators. In *European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF)*, 2011.

[17] K. Liu, T. An, H. Cai, L. Alves de Barros Naviner, J.-F. Naviner, and H. Petit. A general cost-effective design structure for probabilistic based noise-tolerant logic functions in nanometer CMOS technology. In *Proceedings of IEEE International Conference on Computer as a Tool (EUROCON), Zagreb, Croatia, July*, 2013.

[18] B.S. Dhillon. Engineering reliability management. *Selected Areas in Communications, IEEE Journal on*, 4(7):1015–1020, 1986.

[19] G. Gielen, P. De Wit, E. Maricau, J. Loeckx, J. Martin-Martinez, B. Kaczer, G. Groeseneken, R. Rodriguez, and M. Nafria. Emerging yield and reliability challenges in nanometer CMOS technologies. *Proc. Design, Automation and Test*, pages 1322–1327, 2008.

[20] C. Forzan and D. Pandini. Statistical static timing analysis: A survey. *Integration, the VLSI Journal*, 42(3):409–435, 2009.

[21] M. Ramdani, E. Sicard, A. Boyer, S. Ben Dhia, J.J. Whalen, T.H. Hubing, M. Coenen, and O. Wada. The electromagnetic compatibility of integrated circuits - past, present, and future. *Electromagnetic Compatibility, IEEE Transactions on*, 51(1):78–100, 2009.

[22] A. Maheshwari, W. Burleson, and R. Tessier. Trading off transient fault tolerance and power consumption in deep submicron (DSM) VLSI circuits. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 12(3):299–311, 2004.

[23] J. Sosnowski. Transient fault tolerance in digital systems. *Micro, IEEE*, 14(1):24–35, 1994.

[24] N. Tega, Hiroshi Miki, M. Yamaoka, H. Kume, T. Mine, T. Ishida, Yuki Mori, R. Yamada, and K. Torii. Impact of threshold voltage fluctuation due to random telegraph noise on scaled-down SRAM. In *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, pages 541–546, 2008.

[25] S.M. Amoroso, A. Ghetti, A.R. Brown, A. Mauri, C. Monzio Compagnoni, and A. Asenov. Impact of cell shape on random telegraph noise in decananometer flash memories. *Electron Devices, IEEE Transactions on*, 59(10):2774–2779, 2012.

[26] M. Singh and I. Koren. Fault sensitivity analysis and reliability enhancement of analog-to-digital converters. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 11(5):839–852, 2003.

[27] M. Singh and I. Koren. Fault-sensitivity analysis and reliability enhancement of analog-to-digital converters. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 11(5):839–852, 2003.

[28] E. Maricau and G. Gielen. Computer-aided analog circuit design for reliability in nanometer CMOS. *IEEE transactions on emerging and selected topics in circuits and systems*, 1(1):50–58, 2011.

[29] V. Huard, N. Ruiz, F. Cacho, and E. Pion. A bottom-up approach for system-on-chip reliability. *Tutorial session of 22th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, 2011.

[30] P.S. Zuchowski, P.A. Habitz, J.D. Hayes, and J.H. Oppold. Process and environmental variation impacts on ASIC timing. In *Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on*, pages 336–342, 2004.

[31] A.R. Brown, G. Roy, and A. Asenov. Poly-Si-gate-related variability in decananometer MOSFETs with conventional architecture. *Electron Devices, IEEE Transactions on*, 54(11):3056–3063, 2007.

[32] T. Chawla, S. Marchal, A. Amara, and A. Vladimirescu. Local mismatch in 45nm digital clock networks. *Integrated Circuits, ISIC '09. Proceedings of the 2009 12th International Symposium on*, pages 466–469, 2009.

[33] A. Asenov. Local mismatch in 45nm digital clock networks. *Electron Devices, IEEE Transactions on*, 45(12):2505–2513, Dec. 1998.

[34] A. Asenov. 3D statistical simulation of intrinsic fluctuations in decanano MOSFETs induced by discrete dopants, oxide thickness fluctuations and ler. *International Conference on Simulation of Semiconductor Processes and Devices*, pages 162–169, 2001.

[35] Yun Ye, F. Liu, Min Chen, S. Nassif, and Yu Cao. Statistical modeling and simulation of threshold variation under random dopant fluctuations and line-edge roughness. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 19(6):987–996, june 2011.

[36] A. Asenov, S. Kaya, and J. H. Davies. Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations. *Electron Devices, IEEE Transactions on*, 49(1):112 –119, jan 2002.

[37] M. J M Pelgrom, Aad C J Duinmaijer, and A.P.G. Welbers. Matching properties of MOS transistors. *Solid-State Circuits, IEEE Journal of*, 24(5):1433–1439, Oct.

[38] A.A. Mutlu and M. Rahman. Statistical methods for the estimation of process variation effects on circuit operation. *Electronics Packaging Manufacturing, IEEE Transactions on*, 28(4):364–375, oct. 2005.

[39] Y. Miura and Y. Matukura. Investigation of silicon-silicon dioxide interface using mos structure. *Japan Journal of Apply of Physics*, 5:180, 1966.

[40] W. Wang. *Circuits aging in scaled CMOS design: modeling, simulation and prediction*. PhD thesis, Arizona State University, 2008.

[41] R. Vattikonda, Wenping Wang, and Yu Cao. Modeling and minimization of PMOS NBTI effect for robust nanometer design. In *Design Automation Conference, 2006 43rd ACM/IEEE*, pages 1047–1052, 2006.

[42] G. Gielen, E. Maricau, and P. De Wit. Analog circuit reliability in sub-32 nanometer CMOS: Analysis and mitigation. In *Design, Automation Test in Europe Conference Exhibition (DATE), 2011*, pages 1–6, March.

[43] Xiaojun Li, Jin Qin, and J.B. Bernstein. Compact modeling of MOSFET wearout mechanisms for circuit-reliability simulation. *Device and Materials Reliability, IEEE Transactions on*, 8(1):98–121, 2008.

[44] J.W. McPherson. Reliability challenges for 45nm and beyond. In *Design Automation Conference, 2006 43rd ACM/IEEE*, pages 176–181, 2006.

[45] Kjell O. Jeppson and Christer M. Svensson. Negative bias stress of MOS devices at high electric fields and degradation of mnos devices. *Journal of Applied Physics*, 48(5):2004–2014, May.

[46] M.A. Alam, H. Kufluoglu, D. Varghese, and S. Mahapatra. A comprehensive model for PMOS NBTI degradation: Recent progress. *Microelectronics Reliability*, 47(6):853–862, 2007.

[47] J.H. Stathis and S. Zafar. The negative bias temperature instability in MOS devices: A review. *Microelectronics Reliability*, 46(2C4):270 – 286, 2006.

[48] E. Maricau and G. Gielen. Transistor aging-induced degradation of analog circuits: Impact analysis and design guidelines. In *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, pages 243–246, sept. 2011.

[49] J.H. Stathis. Percolation models for gate oxide breakdown. *Journal of Applied Physic*, 86(10):5757–5766, 1999.

[50] J.H. Stathis. Physical and predictive models of ultrathin oxide reliability in CMOS devices and circuits. *Device and Materials Reliability, IEEE Transactions on*, 1(1):43–59, Mar.

[51] Ernest Y. Wu and Jordi Suné. Power-law voltage acceleration: A key element for ultra-thin gate oxide reliability. *Microelectronics Reliability*, 45(12):1809 – 1834, 2005.

[52] Jens Lienig. Introduction to electromigration-aware physical design. In *Proceedings of the 2006 international symposium on Physical design*, ISPD '06, pages 39–46, 2006.

[53] Joseph B. Bernstein, Moshe Gurfinkel, Xiaojun Li, Jorg Walters, Yoram Shapira, and Michael Talmor. Electronic circuit reliability modeling. *Microelectronics Reliability*, 46(12):1957 – 1979, 2006.

[54] A.H Fischer, A Abel, M Lepper, A.E Zitzelsberger, and A von Glasow. Modeling bimodal electromigration failure distributions. *Microelectronics Reliability*, 41(3):445 – 453, 2001.

[55] Sangwoo Pae, A. Ashok, Jingyoo Choi, T. Ghani, Jun He, Seok hee Lee, K. Lemay, M. Liu, R. Lu, P. Packan, C. Parker, R. Purser, A. St.Amour, and B. Woolery. Reliability characterization of 32nm high-k and metal-gate logic transistor technology. In *Reliability Physics Symposium (IRPS), 2010 IEEE International*, pages 287–292, 2010.

[56] R. Degraeve, M. Aoulaiche, B. Kaczer, P. Roussel, T. Kauerauf, S.A. Sahhaf, and G. Groeseneken. Review of reliability issues in high-k/metal gate stacks. In *Physical and Failure Analysis of Integrated Circuits, 2008. IPFA 2008. 15th International Symposium on the*, pages 1–6, 2008.

[57] Gary S. May and Costas J. Spanos. *Fundamentals of Semiconductor Manufacturing and Process Control*. John Wiley & Sons, Inc., first edition, 2006.

[58] C.h Ha. *Reliability-Yield Allocation for Semiconductor Integrated Circuits: Modeling and Optimization*. PhD thesis, Texas A & M University, 2004.

[59] M. Buhler, J. Koehl, J. Bickford, J. Hibbeler, U. Schlichtmann, R. Sommer, M. Pronath, and A. Ripp. Date 2006 special session: DFM/DFY design for manufacturability and yield - influence of process variations in digital, analog and mixed-signal circuit design. In *Design, Automation and Test in Europe, 2006. DATE '06. Proceedings*, volume 1, pages 1–6, 2006.

[60] Xin Pan and Helmut Graeb. Reliability optimization of analog integrated circuits considering the trade-off between lifetime and area. *Microelectronics Reliability*, 52(8):1559 – 1564, 2012.

[61] Xin Pan and H. Graeb. Degradation-aware analog design flow for lifetime yield analysis and optimization. In *Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on*, pages 667–670, Dec. 2009.

[62] Cadence design system Inc. Reliability simulation in integrated circuit design, white paper, 2003.

[63] E. Maricau and G. Gielen. Efficient variability-aware NBTI and hot carrier circuit reliability analysis. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 29(12):1884–1893, 2010.

[64] Xiaojun Li, Jin Qin, Bing Huang, Xiaohu Zhang, and J.B. Bernstein. A new SPICE reliability simulation method for deep submicrometer CMOS VLSI circuits. *Device and Materials Reliability, IEEE Transactions on*, 6(2):247–257, 2006.

[65] P. Ramachandran, S.V. Adve, P. Bose, J.A. Rivers, and J. Srinivasan. Metrics for lifetime reliability. UIUC CS technical report UIUCDCS-R-2006-2762, University of Illionis at Urbana Champaign, August 2006.

[66] Yao Wang and S. Cotofana. A novel virtual age reliability model for time-to-failure prediction. In *Integrated Reliability Workshop Final Report (IRW), 2010 IEEE International*, pages 102–105, 2010.

[67] P. Ramachandran, S.V. Adve, P. Bose, and J.A. Rivers. Metrics for architecture-level lifetime reliability analysis. In *Performance Analysis of Systems and software, 2008. ISPASS 2008. IEEE International Symposium on*, pages 202–212, 2008.

[68] Mentor Graphics Corporation. Eldo user manual, 1999.

[69] E. Maricau, P. De Wit, and G. Gielen. An analytical model for hot carrier degradation in nanoscale CMOS suitable for the simulation of degradation in analog ic applications. *Microelectronics Reliability*, 48(8-9):1576–1580, 2008.

[70] P. Roussel B. Kaczer, R. Degraeve and G. Groeseneken. Gate oxide breakdown in fet devices and circuits: From nanoscale physics to system-level reliability. *Journal of Applied Physic*, 47(4-5):559–566, 2007.

[71] R. Chevallier S. Cheffah, V. Huard and A. Bravaix. Soft oxide breakdown impact on the functionality of a 40 nm SRAM memory. *International Conference on Reliability Physics Symposium (IRPS)*, pages CR.3.1–CR.3.2, 2011.

[72] R. Degraeve, B. Kaczer, A. De Keersgieter, and G. Groeseneken. Relation between breakdown mode and breakdown location in short channel NMOSFETs and its impact on reliability specifications. In *Reliability Physics Symposium, 2001. Proceedings. 39th Annual. 2001 IEEE International*, pages 360–366, 2001.

[73] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P.J. Roussel, and G. Groeseneken. Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability. *Electron Devices, IEEE Transactions on*, 49(3):500–506, 2002.

[74] F. Marc, B. Mongellaz, and Y. Danto. Reliability simulation of electronic circuits with VHDL-AMS. In *Languages for System Specification*. Springer US, 2004.

[75] C. Hu. IC reliability simulation. *IEEE Journal of Solid-State Circuits*, 27(3):241–246, 1992.

[76] Xiangdong Xuan, A. Chatterjee, A.D. Singh, N.P. Kim, and M.T. Chisa. Ic reliability simulator aret and its application in design-for-reliability. In *Test Symposium, 2003. ATS 2003. 12th Asian*, pages 18–21, 2003.

[77] W.-J. Hsu, B.J. Sheu, S.M. Gowda, and Chang-Gyu Hwang. Advanced integrated-circuit reliability simulation including dynamic stress effects. *Solid-State Circuits, IEEE Journal of*, 27(3):247–257, 1992.

[78] C. Bestory, F. Marc, and H. Levi. Multi-level modeling of hot carrier injection for reliability simulation using VHDL-AMS. In *Forum on specification and design language*, 2006.

[79] C. Bestory, F. Marc, and H. Levi. Statistical analysis during the reliability simulation. *Microelectronics Reliability*, 47:1353–1357, 2007.

[80] P.M. Ferreira. *Méthodologie de conception AMS/RF pour la fiabilité: conception d'un frontal RF fiabilisé*. PhD thesis, TELECOM ParisTech, 2011.

[81] V. Veetil, D. Sylvester, and D. Blaauw. Efficient monte carlo based incremental statistical timing analysis. *Proc. of IEEE/ACM on Design Automation Conference*, pages 676–681, 2008.

[82] J. Jaffari and M. Anis. On efficient monte carlo-based statistical static timing analysis of digital circuits. *Proc. of IEEE/ACM on Computer-Aided Design, ICCAD*, pages 196–203, 2008.

[83] J. Kim, K. D. Jones, and M. A. Horowitz. Fast, non-monte-carlo estimation of transient performance variation due to device mismatch. *Proc. of IEEE/ACM on DAC*, pages 440–443, 2007.

[84] E. Maricau and G. Gielen. Variability-aware reliability simulation of mixed-signal ICs with quasi-linear complexity. *Design, Automation Test in Europe Conference Exhibition (DATE), 2010*, pages 1094–1099, March 2010.

[85] K.J. Antreich, H.E. Graeb, and C.U. Wieser. Circuit analysis and optimization driven by worst-case distances. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 13(1):57–71, 1994.

[86] Xin Pan and H. Graeb. Reliability analysis of analog circuits using quadratic lifetime worst-case distance prediction. In *Custom Integrated Circuits Conference (CICC), IEEE*, pages 1–4, 2010.

[87] P.M. Ferreira, H. Petit, and J-F Naviner. WLAN/WiMAX RF front-end reliability analysis. In *Argentine School of Micro-Nanoelectronics Technology and Applications (EAMTA), 2010*, pages 46–49, 2010.

[88] [Online] http://www device.eecs.berkeley.edu/bsim/bsim4.htm. BSIM4 homepage, version 4.7, 2012.

[89] H. Filiol, I. O'Connor, and D. Morche. Piecewise-polynomial modeling for analog circuit performance metrics. In *Circuit Theory and Design, 2009. ECCTD 2009. European Conference on*, pages 237–240, 2009.

[90] J. Martin-Martinez, R. Rodriguez, M. Nafria, and X. Aymerich. Time-dependent variability related to BTI effects in MOSFETs: Impact on CMOS differential amplifiers. *Device and Materials Reliability, IEEE Transactions on*, 9(2):305–310, 2009.

[91] M.B. Yelten, P.D. Franzon, and M.B. Steer. Surrogate-model-based analysis of analog circuits; part i: Variability analysis. *Device and Materials Reliability, IEEE Transactions on*, 11(3):458–465, 2011.

[92] M.B. Yelten, P.D. Franzon, and M.B. Steer. Surrogate-model-based analysis of analog circuits; part ii: Reliability analysis. *Device and Materials Reliability, IEEE Transactions on*, 11(3):466–473, 2011.

[93] [Online] http://www.sumo.intec.ugent.be. Webpage, sumo lab, ghent university, 2013.

[94] Hua Tang. Hierarchical statistical analysis of performance variation for continuous-time delta-sigma modulators. *Very Large Scale Integration, 2007. VLSI-SoC 2007. IFIP International Conference on*, pages 37–41, 2007.

[95] V. Huard, N. Ruiz, F. Cacho, and E. Pion. A bottom-up approach for system-on-chip reliability. *Microelectronics Reliability*, 51(9-11):1425–1439, 2011.

[96] H. Graeb, S. Zizala, J. Eckmueller, and K. Antreich. The sizing rules method for analog integrated circuit design. In *Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Conference on*, pages 343–349, 2001.

[97] D. Mueller J. Zou, H. Graeb and U. Schlichtmann. Optimization of sc $\sigma\delta$ modulators based on worst-case-aware Pareto-optimal fronts. *Proc. Custom Integrated Circuits Conference (CICC)*, pages 607–610, 2007.

[98] S. Tiwary, P. Tiwary, and R. Rutenbar. Generation of yield-aware pareto surfaces for hierarchical circuit design space exploration. *Proc. Design Automation Conference (DAC)*, pages 31–36, 2006.

[99] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan. A fast and elitist multiobjective genetic algorithm: NSGA-II. *IEEE Transactions on Evolutionary Computation*, pages 182–197, 2002.

[100] David E. Goldberg. *Genetic Algorithms in Search, Optimization and Machine Learning*. Addison-Wesley Publishing Company, Massachusetts, 1989.

[101] S. Das and P. Suganthan. Differential evolution: A survey of the state-of-the-art. *IEEE Transactions on Evolutionary Computation*, 15(1):4–31, 2011.

[102] Denis Teixeira Franco. *Fiabilité du Signal des Circuits Logiques Combinatoires sous Fautes Simultanées Multiples*. PhD thesis, TELECOM Paristech, 2008.

[103] A. Namazi and M. Nourani. Gate-level redundancy: A new design-for-reliability paradigm for nanotechnologies. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 18(5):775–786, 2010.

[104] M. Nourani, A. Namazi, and S. Askari. Fault tolerant circuits for highly reliable systems. In *Aerospace conference, 2009 IEEE*, pages 1–10, 2009.

[105] S. Askari and M. Nourani. A design for reliability methodology based on selective overdesign. In *Design and Test Workshop (IDT), 2010 5th International*, pages 73–77, 2010.

[106] S. More, M. Fulde, F. Chouard, and D. Schmitt-Landsiedel. Reducing impact of degradation on analog circuits by chopper stabilization and autozeroing. In *Quality Electronic Design (ISQED), 2011 12th International Symposium on*, pages 1–6, 2011.

[107] A. Ghosh, R. Franklin, and R.B. Brown. Analog circuit design methodologies to improve negative-bias temperature instability degradation. In *VLSI Design, 2010. VLSID'10. 23rd International Conference on*, pages 369–374, 2010.

[108] I-Chyn Wey, You-Gang Chen, Chang-Hong Yu, An-Yeu Wu, and Jie Chen. Design and implementation of cost-effective probabilistic-based noise-tolerant VLSI circuits. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 56(11):2411–2424, 2009.

[109] S. Z. Li. *Markov Random Field Modelling in Computer Vision*. New York: Springer-Verlag, 1995.

[110] S. Sayil, A.B. Akkur, and N Gaspard III. Single event crosstalk shielding for CMOS logic. *Microelectronics Journal*, 40(6):1000–1006, 2009.

[111] Zheng Hao Lu, Xiao Peng Yu, Yang Liu, Jia Ning Su, and Chang Hui Hu. Design of nano-scale noise tolerant CMOS logic circuits based on probabilistic Markov random field approach. *Nanoscience and Nanotechnology Letters*, 4(9), 2012.

[112] Kaisa Simola. *Reliability methods in nuclear power plant ageing management*. PhD thesis, Helsinki University of Technology, 1999.

[113] Wenping Wang, V. Reddy, A.T. Krishnan, R. Vattikonda, Srikanth Krishnan, and Yu Cao. Compact modeling and simulation of circuit reliability for 65-nm CMOS technology. *Device and Materials Reliability, IEEE Transactions on*, 7(4):509–517, 2007.

[114] T. Quemerais, L. Moquillon, J. Fournier, P. Benech, and V. Huard. Design-in-reliable millimeter-wave power amplifiers in a 65-nm CMOS process. *Microwave Theory and Techniques, IEEE Transactions on*, 60(4):1079–1085, 2012.

[115] P.M. Ferreira, H. Petit, and J-F Naviner. A synthesis methodology for AMS/RF circuit reliability: Application to a DCO design. *Microelectronics Reliability*, 51(4):765–772, 2011.

[116] Yidong Liu and J.-S. Yuan. CMOS RF low-noise amplifier design for variability and reliability. *Device and Materials Reliability, IEEE Transactions on*, 11(3):450–457, 2011.

[117] J. Keane, Xiaofei Wang, D. Persaud, and C.H. Kim. An all-in-one silicon odometer for separately monitoring hci, bti, and tddb. *Solid-State Circuits, IEEE Journal of*, 45(4):817–829, 2010.

[118] Yi Gang, Weisheng Zhao, J-O Klein, C. Chappert, and P. Mazoyer. A high-reliability, low-power magnetic full adder. *Magnetics, IEEE Transactions on*, 47(11):4611–4616, 2011.

[119] Baoguang Yan, Qingguo Fan, J.B. Bernstein, Jin Qin, and Jun Dai. Reliability simulation and circuit-failure analysis in analog and mixed-signal applications. *Device and Materials Reliability, IEEE Transactions on*, 9(3):339–347, 2009.

[120] Anh-Tuan Do, Zhi-Hui Kong, Kiat-Seng Yeo, and Jeremy Yung Shern Low. Design and sensitivity analysis of a new current-mode sense amplifier for low-power SRAM. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 19(2):196–204, 2011.

[121] H. Mostafa, M. Anis, and M. Elmasry. NBTI and process variations compensation circuits using adaptive body bias. *Semiconductor Manufacturing, IEEE Transactions on*, 25(3):460–467, 2012.

[122] A. Chakraborty, G. Ganesan, A. Rajaram, and D.Z. Pan. Analysis and optimization of NBTI induced clock skew in gated clock trees. In *Design, Automation Test in Europe Conference Exhibition, 2009. DATE '09.*, pages 296–299, 2009.

[123] B. Kaczer, S. Mahato, V.V. de Almeida Camargo, M. Toledano-Luque, P.J. Roussel, T. Grasser, F. Catthoor, P. Dobrovolny, P. Zuber, G. Wirth, and G. Groeseneken. Atomistic approach to variability of bias-temperature instability in circuit simulations. In *Reliability Physics Symposium (IRPS), 2011 IEEE International*, pages XT.3.1–XT.3.5, 2011.

[124] V. Gutnik. *Analysis and characterization of random skew and jitter in a novel clock network*. PhD thesis, Massachusetts Institute of Technology, 2000.

[125] A. Chattopadhyay and Z. Zilic. Flexible and reconfigurable mismatch-tolerant serial clock distribution networks. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 20(3):523–536, 2012.

[126] A. Ashry and H. Aboushady. Modeling jitter in continuous-time sigma-delta modulators. In *Behavioral Modeling and Simulation Conference (BMAS)*, pages 53–56, 2010.

[127] [Online] http://www.itl.nist.gov/div898/handbook. Nist/sematech e-handbook of statistical methods, 2013.

[128] Statistics toolbox for use with MATLAB, 2010.

[129] Paul R. Gray, Paul J.Hurst, Stephen H.Lewis, and Robert G.Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Inc, fourth edition, 2001.

[130] Ken Martin David A. Johns. *Analog Integrated Circuit Design*. John Wiley & Sons, Inc, first edition, 1997.

[131] Chadi Jabbour. *Reconfigurable Parallel Delta Sigma Analog to Digital Converters*. PhD thesis, TELECOM ParisTech, Paris, 2010.

[132] M. Ortmanns and F. Gerfers. *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion*. Springer, first edition, 2006.

[133] Schreier. R and Temes. G. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE, first edition, 2004.

[134] Franco Maloberti. *Data Converters*. Springer, first edition, 2007.

[135] [Online] http://www.mathworks.com/fcentral/fileexchange. R. Schreier. The delta-sigma toolbox version 7.1 (delsig.zip), software toolbox and user's manual, 2004.

[136] Steven R. Norsworthy, Richard Schreier, and Gabor C. Temes. *Delta-Sigma Data Converters: Theory, Design and Simulation*. IEEE Press, first edition, 1997.

[137] A. Gharbiya, T. C. Caldwell, and D. A. Johns. High-speed oversampling analog-to-digital converters. *International Journal of High Speed Electronics and Systems*, pages 1–21, 2005.

[138] G. Yu and P. Li. Lookup table based simulation and statistical modeling of sigma-delta ADCs. *Proc. of IEEE/ACM on Design Automation Conference*, pages 1035–1040, 2006.

[139] M. Andrejevic and V. Litovski. Fault diagnosis in digital part of sigma-delta converter. In *Neural Network Applications in Electrical Engineering, 2006. NEUREL 2006. 8th Seminar on*, pages 177–180, 2006.

[140] Shailesh More. *Aging Degradation and Countermeasures in Deep-submicrometer Analog and Mixed Signal Integrated Circuits*. PhD thesis, Technischen Universitat Munchen, 2011.

[141] J.A. Cherry and W.M. Snelgrove. Excess loop delay in continuous-time delta-sigma modulators. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 46(4):376–389, 1999.

[142] J.A. Cherry and W.M. Snelgrove. Clock jitter and quantizer metastability in continuous-time delta-sigma modulators. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 46(6):661–676, 1999.

[143] P. Cusinato, M. Bruccoleri, D.D. Caviglia, and M. Valle. Analysis of the behavior of a dynamic latch comparator. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, 45(3):294–298, 1998.

Fiabilisation de Convertisseurs Analogique-Numérique à Modulation Sigma-Delta

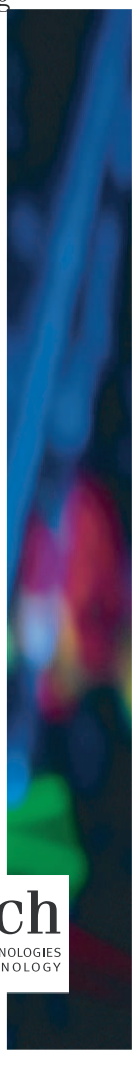
Hao CAI

RESUME: Ce travail de thèse a porté sur des problèmes de fiabilité de circuits intégrés en technologie CMOS 65 nm, en particulier sur la conception en vue de la fiabilité, la simulation et l'amélioration de la fiabilité. Les mécanismes dominants de vieillissement HCI et NBTI ainsi que la variabilité du procédé de fabrication ont été étudiés et évalués quantitativement au niveau du circuit et au niveau du système. Ces méthodes ont été appliquées aux modulateurs ΣΔ afin de déterminer la fiabilité de ce type usuel de composant.

MOTS-CLEFS: Fiabilité, CMOS 65nm, Modulateurs ΣΔ, Variabilité, Vieillissement

ABSTRACT: This thesis concentrates on reliability-aware methodology development, reliability analysis based on simulation as well as failure prediction of CMOS 65 nm analog and mixed signal (AMS) ICs. Sigma-Delta (ΣΔ) modulators are concerned as the object of reliability study at system level. A hierarchical statistical approach for reliability is proposed to analysis the performance of ΣΔ modulators under ageing effects and process variations. Statistical methods are combined into this analysis flow.

KEY-WORDS: Reliability, CMOS 65nm, ΣΔ modulator, Process variation, Ageing



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