Towards thermoelectric metamaterials based on vertical superlattices : fabrication and challenges

Jayalakshmi Parasuraman

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Vers des Métamateriaux Thermoélectriques à Base de Super-Réseaux Verticaux : Principes et Défis Technologiques.

Towards Thermoelectric Metamaterials Based on Vertical Superlattices:
Principles and Technological Challenges.

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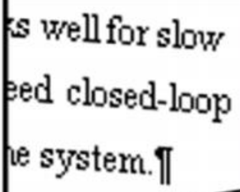

"I almost wish I hadn't
gone down that rabbit-hole
—and yet—and yet—
it's rather curious, you know,
this sort of life!"

- Alice

“Success is not a result of spontaneous combustion. You must set yourself on fire.” - Fred Shero

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Resumé

Les métamatériaux offrent la possibilité d'obtenir des propriétés physiques nettement améliorées en comparaison avec celles des matériaux naturels. Dans ce travail, nous explorons une nouvelle variété de métamatériaux thermoélectriques à base de micro- et nano-structuration du silicium, sous la forme de super-réseaux verticaux, avec comme visée applicative la récupération d'énergie thermique ainsi que le refroidissement. En outre, nous focalisons nos efforts sur une méthodologie expérimentale permettant la réalisation de ces métamatériaux par des moyens simples et peu coûteux. La première partie de cette thèse sert d'introduction aux phénomènes thermiques qui constituent la base de la conduction électrique et de la dissipation de chaleur dans les nanostructures, respectivement par émission thermo-ionique et par la diffusion de phonons. Cette partie détaille également les principes et résultats de caractérisation thermique à l'aide des méthodes 3 et 2 . La deuxième partie de cette thèse décrit les approches de micro- et nano-structuration descendante "top-down" et ascendante "bottom-up", en vue de la fabrication de super-réseaux nanométriques sur du silicium monocristallin. La nouvelle architecture verticale proposée soulève des défis technologiques qui sont traités à travers l'exploration de techniques expérimentales originales pour produire, d'une manière efficace et sur de grandes surfaces, des structures submicroniques à fort facteur de forme. Ces techniques comprennent l'utilisation de motifs résultant de lithographie traditionnelle combinée à l'extrusion pour en produire des structures volumiques. En outre, l'utilisation de nanofibres et de diblocs copolymères comme nano-motifs géométriques sont également présentés pour nous rapprocher davantage de l'objectif ultime du projet.

Mots clés : Métamatériaux, Superréseaux, micro et nano-structures en silicium, DRIE.

Abstract

Metamaterials offer the benefit of obtaining improved physical properties over natural materials. In this work, we explore a new variety of thermoelectric metamaterials based on silicon micro- and nanostructuration, in the form of vertical superlattices for use in energy-related applications. Additionally, we focus on a route towards fabricating these materials using simple and low-cost means compared to prior attempts. The first part of this thesis serves as an introduction to the thermal phenomena which form the basis for electrical conduction and heat dissipation by thermionic emission and phonon scattering at the nanoscale. These principles forms the crux of the device. This section also details the characterization principles and results using the 3 and 2 methods for thermal measurement. The second part of this thesis describes both top-down and bottom-up approaches towards fabricating nanoscale superlattices from single-crystalline silicon. The novel proposed vertical architecture raised technological challenges that were tackled through the exploration of original experimental techniques for producing high aspect ratio (HAR) structures in an effective manner and over large surface areas. These techniques include the use of traditional lithography patterning and subsequent extrusion of volumetric structures. Additionally, the use of nanofibers and diblock copolymers as templates for further etching of HAR silicon nanostructures are also presented to bring us closer to the ultimate goal of the project.

Keywords: Metamaterials, Superlattices, HAR structures, DRIE.

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List of symbols and acronyms

TE	Thermoelectics
TEM	Thermoelectric Module
RTG	Radioactive Thermoelectric Generator
Z	Thermoelectric figure of merit
SL	Superlattice
TEP	Thermoelectric Power
TCR	Temperature Coefficient of Resistance
MEMS	Micro Electro Mechanical Systems
PVD	Physical Vapour Deposition
RIE	Reactive Ion Etching
DRIE	Deep Reactive Ion Etching
AR	Aspect Ratio
HAR	High Aspect Ratio
FOM	Figure Of Merit
SEM	Scanning Electron Microscope
FIB	Focused Ion Beam
ALD	Atomic Layer Deposition
SThM	Scanning Thermal Microscope
AFM	Atomic Force Microscope
PCB	Printed Circuit Board
BNC	Baynoet Neil-Concelman
CMP	Chemical Mechanical Polishing
DMF	Dimethyl Formalamide
PS	Polystyrene
PMMA	Poly Methyl Methacrylate
PDMS	Poly Dimethyl Siloxane
UV	Ultraviolet
AA	Acetic Acid
LB	Langmuir-Blodgett
BS	Black Silicon

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Chapter 1
Introduction

1.1. Background and motivation

With increasing demand for sustainable energy technologies, research in the area has escalated over the past couple of decades. Conventional renewable energy sources (solar, wind, and geothermal) supply only a small fraction of the electricity consumed, owing primarily to their relatively high cost with the key limitation of the wastage of heat as a by-product [1-5]. With the possibility of heat being an untapped source with huge potential, there is also significant interest in finding high efficiency and cost-effective technologies for generating electricity from residual heat.

A typical thermoelectric device consists of two different materials connected at both ends which either generates electrical power when subjected to a temperature difference (Seebeck effect) or generates a temperature difference when supplied with electrical power (Peltier effect). Depending on what effect takes place, the device may act as an electrical power generator or a refrigerator. In current world applications, thermoelectrics thus far have only found use in niche applications such as Peltier coolers for small-scale or localized cooling, mainly due to their moderate energy conversion efficiency and relatively high cost. In these applications, conventional mechanical refrigerators do not scale well from the weight, cost and efficiency point of view. Thermoelectric devices have also been used in radioisotope thermal generators for deep-space satellites [6-9] and remote electrical power generation for unmanned systems. Additional applications such as vehicle exhaust waste heat recovery [10-12] and autonomous sensors on the body [13-15] are actively being studied. Thermoelectric coolers are currently widely used for cooling of infrared detector cameras and temperature stabilization of semiconductor lasers. The use of Peltier coolers in relation to refrigeration of biological specimens/samples is an upcoming application of thermoelectrics as well. They offer an environmentally “green” solution as opposed to conventional methods using chlorofluorocarbons which are harmful to the atmosphere in terms of waste gas released. However, most efforts to this end are restricted to small-scale applications requiring localized cooling of small components in portable systems. Recently, a thermoelectric climate control system has been commercialized, and applications for small-scale beverage

coolers are expanding as well [16]. In general, when considering the performance of small electronic systems, cooling is considered as a fundamental limit of performance improvement because temperature directly relates to noise. For example, cooling of laser diodes and infrared detectors to temperatures (T), between 100 and 200 K, would greatly improve performance and sensitivity of the device, hence leading to further applications that it can be put to use to. Thus, the payoff for the development of low-temperature thermoelectric refrigeration devices is escalating, and the requirement for compounds with properties optimized over wide temperature ranges has led to a much-expanded interest in new thermoelectric materials.

On the other hand, electrical power generation applications are also being investigated by the automotive industry, among others, as a means to produce electrical power from wasted heat of the engines for development of the 'next generation vehicle'. The research in applications range from power generation utilizing waste engine heat from the exhaust and radiator cooling system to seat coolers/warmers for comfort or electronic component cooling including beverage heaters or coolers [16-18]. In a similar manner, the deep space applications of NASA's *Voyager* and *Cassini* missions use radioactive thermoelectric generators (RTGs) to produce electrical energy [19-21]. In this case, the primary heat is produced by a radioactive material as it decays into non-radioactive state.

Study of thermoelectric materials is an extremely well-studied area of research spanning over 5 decades. Of particular interest when studying these materials are their characteristics that govern their performance in related applications. Traditionally, a good thermoelectric material is described based on its Figure of Merit (FOM), Z, which is defined as the dimensionless quantity

$$ZT = \frac{\sigma S^2 T}{\lambda} \tag{1.1}$$

where, σ is electrical conductivity of the material; λ, its thermal conductivity; S, the Seebeck coefficient of the material and T, the absolute temperature of the device. This dimensionless quantity, ZT, quantifies the material's ability to produce thermoelectric power.

An ideal thermoelectric material would thus have a high electrical conductivity to minimize Joule heating, low thermal conductivity to prevent thermal shorting and a high Seebeck coefficient to maximize the conversion efficiency between heat and electricity. But when attempting to achieve the qualities desired as discussed above, one is faced with some trade-offs in trying to maximize each of these quantities. Figure 1.1 (a) [23] is an illustration of the trade-

offs encountered through the maximization of the figure of merit of a ‘natural’ thermoelectric material. For instance, consider the example of metals as a thermoelectric material. A high electrical conductivity is almost always accompanied by a high thermal conductivity *and* a low Seebeck coefficient. On the other hand, for an engineered semiconductor material, the parameter that helps in achieving maximum *ZT* is the doping concentration. When the doping is high and the Fermi level of the semiconductor is around its band edge (the conduction band for an *n*-type semiconductor and the valence band for a *p*-type semiconductor – see Figure 1.1 (b)), the charge carriers occupy the highest energy state for excitation. Hence when provided with the momentum, they are released into the conduction band and thereby enhance the electrical conductivity of the material. The effects of the different thermoelectric properties with respect to the level of doping in the semiconductor are illustrated in the Figure 1.1 (a). As can be inferred, the semiconductor doping level can be used as a tuning parameter to maximize σS^2 which is shown in green as the bell curve, which is the quantity directly proportional to increasing *ZT*. The desired properties are highlighted by the blue region in the image.

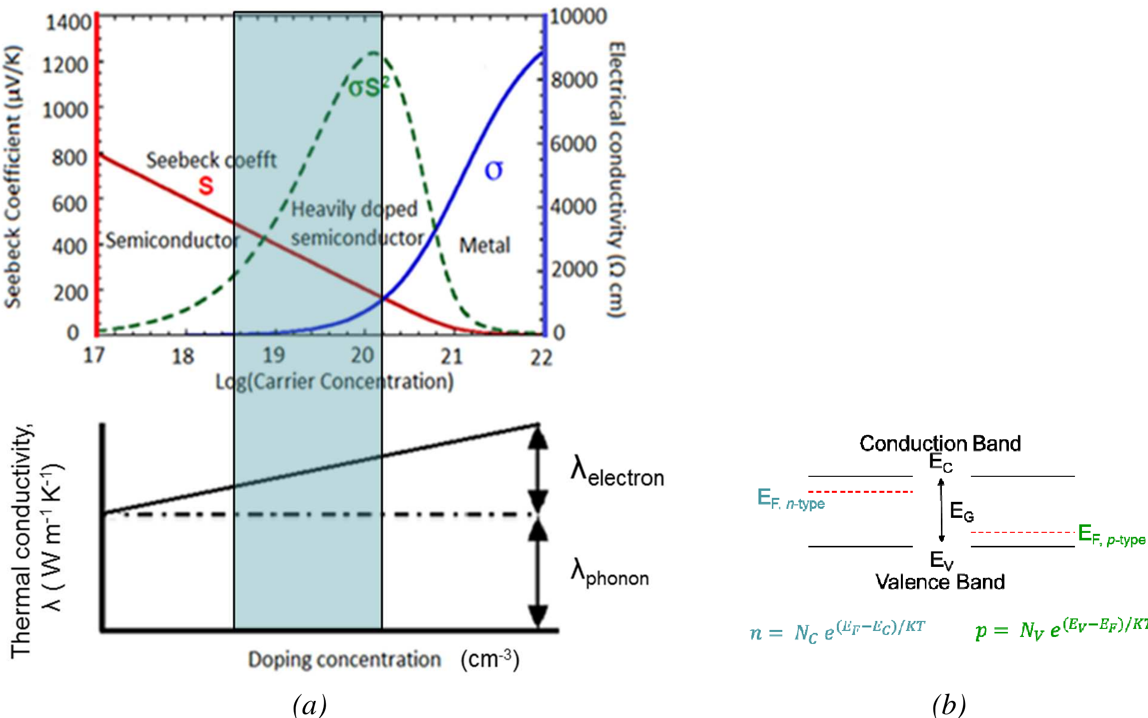

Figure 1.1. (a) Illustration of FOM optimization and representation of the trade-offs. In the case of a semiconductor material, doping concentration is used as a tuning parameter (reproduced from [23]) and (b) Representation of the band energies and Fermi levels for highly doped n-type and p-type semiconductors.

Also it can be noted from Figure 1.1 (a) that the lattice contributions of the thermal conductivity, λ_{phonon} increase with doping over the electronic contributions, $\lambda_{electron}$. Typically

$\lambda_{electron}$ is 1/3rd λ_{phonon} [19]. Thus, since the phonons are the vibrational lattice components that primarily carry heat, they can be dissipated by interface scattering and thus it is beneficial to maximize their contributions with higher doping [19].

Over the years, semiconductor composites such as Bismuth Telluride (Bi_2Te_3), Silicon Germanium (SiGe), *etc.* have found applications in thermoelectricity with *ZTs* in the range of 1-3 [24-28].

Continued interest in improving the thermoelectric figure of merit, *ZT* has led to research for new engineered materials and metamaterials, including material nanocomposites with improved thermal characteristics for applications in micro and nanoscale devices. The most actively studied materials of this kind include, but are not restricted to, improved Silicon Germanium stacked superlattice structures [29, 30] and thermoelectric oxide materials [31]. One can also cite other advanced materials such as half-Heusler alloys [32], Skutterudites [33] and complex chalcogenides [34], which are beyond the scope of this thesis.

1.2. Thermoelectric metamaterials

Appendix I recalls the basic theoretical background on thermoelectric effects. Detailed explanations of the basic thermoelectric effects like the Seebeck, Peltier effects and the physics of these phenomena are explained in detail. In the next few sections, we concentrate on the thermoelectric behavior of metal-semiconductor multi-layered stacks, with special interest to those with nanometric thicknesses, namely, thermoelectric superlattices.

1.2.1 Peltier effect and thermionic emission in metal-semiconductor junctions

While the Peltier effect in semiconductor pairs gave rise to the concept of thermoelectric generators and thermoelectric coolers (see Appendix I for more details), it is interesting to revisit the Peltier effect in metal-semiconductor-metal junctions as it is very relevant to the work done in this thesis. Figure 1.2 [35] is an illustration of a typical metal-semiconductor-metal junction (a) in *n*-type configuration and then (b) in *p*-type configuration.

Consider the current flow in the clockwise direction. For electrons to enter the semiconductor conduction band from the metal, they must overcome the difference between E_C and E_F.

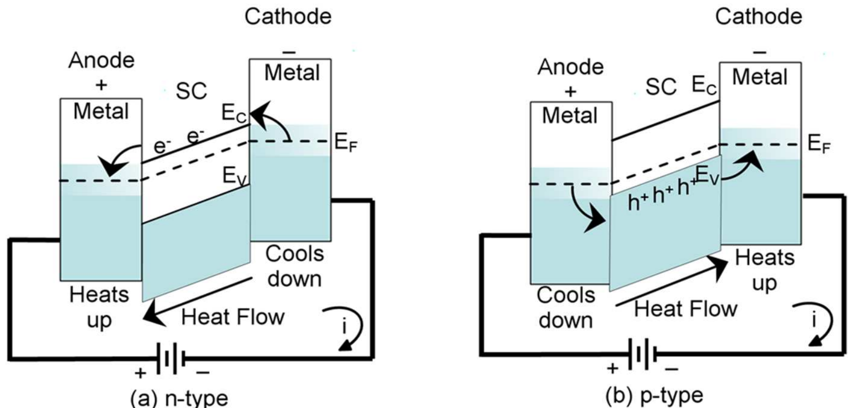

Figure 1.2. Illustration of a typical metal-semiconductor-metal junction in (a) n-type configuration and (b) p-type configuration (redrawn from [35]).

Only the 'hottest electrons' (those with the highest kinetic energy) are likely to surmount the barrier (by thermionic emission). These electrons travel from right to left encountering no barrier while entering the metal again, hence creating depletion on the cathode and a gain on the anode. Therefore, one side heats up while the other cools down. The same concepts hold good for the *p*-type material with the primary charge carriers being the holes instead of the electrons.

1.2.2. Thermionic emission

Considering a multilayered metal-semiconductor stack (Figure 1.3), the band offset between each pair of junctions (Figure 1.4) acts as a 'hot electron filter', allowing through, only the highest energy electrons [35] surmount the barrier by *Thermionic Emission.* These hottest electrons will be the main contributors to the electrical conduction. Furthermore, in case each succeeding layer interface is spaced very close (nanometric range) from one another, we can also have *Phonon Scattering*, which is a mechanism which by scattering the heat carrying lattice vibrational component, the phonons, can reduce thermal conductivity at the interfaces between successive layers when they are in the nanometer scale. At the end, the net result can be a reduction of thermal conductivity while maintaining a high electrical conductivity, leading to a potential increase of the figure of merit, *ZT,* which scales as σ/λ.

1.2.3. Barrier thickness requirements

It has been theoretically ascertained in literature that thermoelectric parameters are enhanced when the layer thickness is lesser than the mean-free-path of the electrons. (~100 nm for most semiconductor [36]).

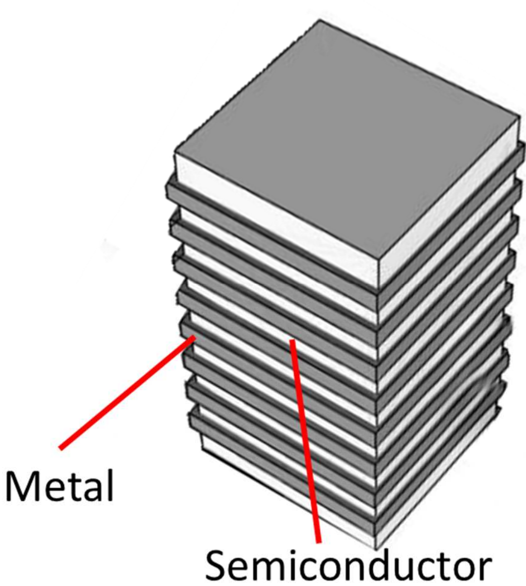

Figure 1.3. Schematic diagram of a typical two material superlattice structure.

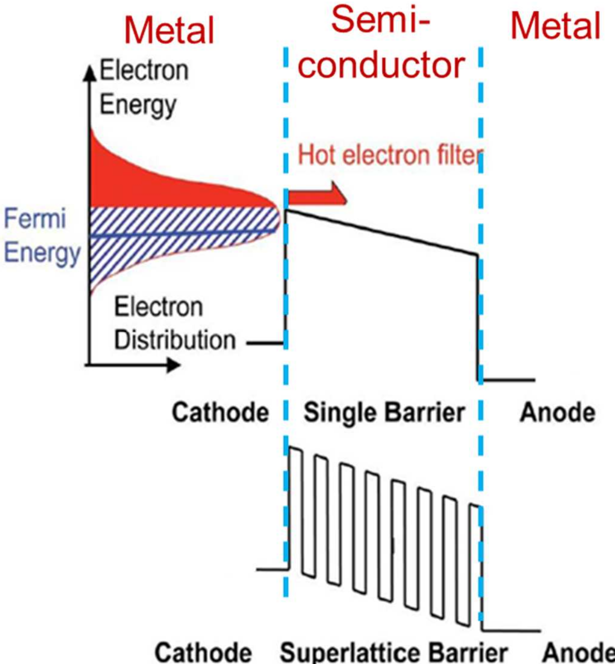

Figure 1.4. Representation of barrier thresholds for increased thermionic emission.

To ensure thermionic emission, i.e., by overcoming the energy barriers, the barrier thickness should be greater than 10 nm at ambient temperatures. If the barrier is inferior to 10 nm, there is a *tunneling effect*, i.e., the electrons simply pass through the barrier rather than overcoming them. The thermionic emission threshold and succession of barriers is shown in Figure 1.4 [36]. It then follows that a succession of barriers might be better than a single barrier for increased thermionic emission. Concluding from the above-stated points, we can conservatively conclude that barrier thickness should be between 10 and 100 nm.

Having a succession of barriers allows for heat dissipation by band offset as well as electrical conduction by thermionic emission. Through research of previous work done in this area, it has been theoretically concluded that a resultant structure made with this concept will have better thermoelectric properties when compared to bulk material. We therefore arrive upon the structure of a *superlattice* (see Figure 1.3). A superlattice is a metamaterial which is composed of a heterogeneous material resulting from a multilayer structure of two or more materials with a succession of potential barriers, thus allowing better thermoelectric conversion than classical bulk materials by cross-plane carrier transport.

1.3 Conclusions from previous work

Whilst trying to introduce some novelty into solving this conundrum, it is important to take the inferences from the work done by other groups in this area. The following is a synopsis of the conclusions drawn from the bibliography of the relevant papers:

- Tall metal barriers associated with a degenerated semiconductor will increase the density of ‘hot electrons’ that are filtered [37].
- Multiple barriers using Metal-Semiconductor Interfaces can increase thermoelectric power factor due to non-conservation of lateral momentum [37].
- Controlled roughness at heterostructure interfaces can break the in-plane translation variance and lateral momentum conservation. This allows the high-energy electrons in any direction to participate in current transport [41].
- Reducing barrier thickness increases thermionic emission. However reducing them too much may result in *Tunneling* [40].

It thus follows that we are likely to have an effective device in fabricating a superlattice using a metal-semiconductor junction ensuring that they are spaced closely to each other (in the nanometer scale) to allow ‘hot-electron’ filtering and effective thermoelectric cooling.

Traditionally, superlattices have been fabricated in the planar form [43-47]. Typically, to accomplish this requires multiple planar deposits using molecular beam epitaxy (MBE) which is a very expensive form of depositing successive ultrathin layers. Figure 1.5 is a schematic representation of conventional planar superlattices.

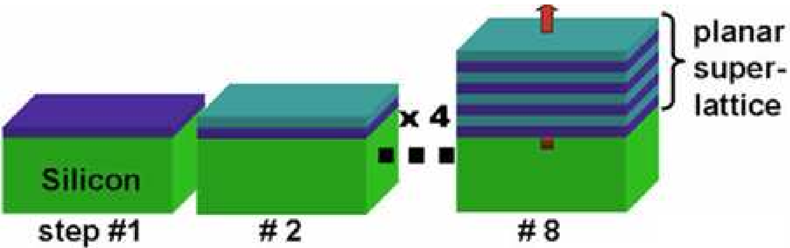

Figure 1.5. Schematic representation of planar superlattices used in the traditional approach.

1.4. Objectives and scope of this thesis

The focus of this thesis is on the study and realization of new silicon-based structured metamaterials with improved thermoelectric performances and which might be suitable for use in various applications such as hot-spot cooling on overheating chips, to construct more efficient thermoelectric modules for use in refrigeration and in energy harvesting, as described the applications of thermoelectric devices in the previous section. The motivation behind using silicon as the base material stems from its familiarity in the semiconductor and MEMS industries whilst being able to accurately control dimensions of the structures to be fabricated down to the nanoscale and with extremely high aspect ratio, which appears as a great advantage towards achieving a new class of novel thermoelectric metamaterials based on vertical superlattices, as detailed hereafter. The technologies for working with silicon are fairly well developed and this presents us with the opportunity to improve further open studied techniques to achieve high aspect ratio feature sizes in the nanoscale as is required towards reaching our objective. Besides, working with silicon reduces the cost of the end product and it allows co-integration with electronic circuits as well. These are other driving forces behind exploring technologies in making metamaterials using silicon in order to enhance thermoelectric performances for usage in on-chip thermal management.

With the Moore's law predicting the number of transistors on an IC doubles approximately every two years [42], the dissipation of heat is also a significant issue preventing the realization of more advanced devices due to high device failure rate as the heat overcomes the device

capabilities. The inclusion of microscale integrated coolers on the microprocessor chips could be a highly significant advancement, allowing higher clock speeds to be realized.

The ultimate objective of our research team is to design, produce and use thermoelectric devices fashioned from improved thermal property materials for heat dissipation of a hot spot on a chip. The basic thermoelectric device built in this thesis involves metamaterials in the form of ‘vertical superlattice’ structures in silicon. Conventional superlattices have been already fabricated but they are limited to the planar form [23] involving multiple-layer deposition of ultra-thin films. Indeed, the traditional way of fabrication superlattices involves multiple planar deposits using molecular beam epitaxy (MBE) leading to nanoscale multi-layered material stacks, which turns out to be an extremely lengthy and expensive fabrication step. The key disadvantages of such structures can be summarized as below:

- Energy conversion efficiency is proportional to the number of layers in the superlattices In other words, efficient devices need a large number of deposits.
- Such devices only transmit electrons whose kinetic energy (KE) in the direction perpendicular to the potential barrier is large enough. Therefore, many “hot electrons” with large in-plane momentum are blocked by the barrier and do not contribute to heat transfer. The electrons have to be seen as carriers of an electrical charge as well as heat quanta, namely phonons.

Hence, the refrigeration function is not cost effective compared to the traditional techniques, even by using chemical vapour deposition (CVD) instead of MBE.

In this thesis we propose exploring a solution to the disadvantages of the conventional superlattices: *Vertical superlattices in silicon*. The main advantages of these are as below:

- Vertical Superlattices could be fabricated directly into Silicon with just 3 main steps: (i) a single patterning step, (ii) a single etch step with high aspect ratio and finally (iii) a conformal deposit of a complementary material to silicon.
- Proceeding this way greatly facilitates in principle, the manufacturing process and it also significantly reduces the manufacturing costs.
- The proposed approach offers alternative shapes to the one-dimensional periodic superlattices. Several two-dimensional shapes, either periodic or not, can be considered.
- High-energy electrons in any direction can potentially contribute to heat transfer, therefore increasing electrical conductivity by further introduction of *controlled*

roughness at the interfaces (achievable by the 'scalloping effect' of the DRIE Bosch process as described below).

Though unique and risky in the same time, the targeted transition from te planar multilayered superlattices to the vertical superlattices is somehow similar to a successful recent experience of our group in producing another kind of structured metamaterial, which consists of vertical Bragg reflectors, produced in a two-step patterning-etching process, and proposed as an alternative to the conventional planar Bragg reflectors, which consists of multilayered stacks of thin film deposits [43-45]. However, the main difference between the above-mentioned photonic metamaterial and the targeted new thermoelectric metamaterial lays in the range of dimensions involved in their operation. While the former requires odd multiples of quarter wavelength thickness, which is in the order of micrometers, the latter requires thicknesses in the order of tens to hundreds of nanometers. This considerably raises the level of the challenge.

1.5. Thesis outline and organization

Following this brief introduction, this thesis is divided into three main parts:

Part I deals with meta-materials and vertical superlattices. Chapter 2 presents the state of the art of structured meta-materials, specifically on multi-layered thin-film stacks and those based on micro and nanostructures. Having discussed the basic fundamentals of thermo-electricity and understanding the key focus of this thesis brings us to Chapter 3 which is about thermoelectric materials based on vertical superlattices. In this section, detailed analysis of the available materials, their usability in this thesis, the processes required for the fabrication and characterization of the thermoelectric devices are discussed in detail. Part I concludes with the challenges faced in the fabrication processes of micro-scale vertical superlattices, which led us to put more efforts to raise the technological barrier towards achieving our targeted new thermoelectric metamaterials.

Therefore, the second part of this thesis, Part II, focusses on the fabrication of HAR silicon-based micro and nanostructures. Chapter 4 is a brief introduction to the contemporary state of the art of HAR feature fabrication. Chapter 5 focusses solely on our Deep Reactive Ion Etching experiments and their results to achieve HAR structures in silicon. Chapter 6 is a foray into the techniques of electrospinning and advanced transfer of HAR structures for a top-down approach on nanoscale silicon based meta-materials. Chapter 7 deals with a brief description of Focussed Ion Beam (FIB) etching techniques used as a patterning method to obtain HAR structures by

subsequent DRIE. And finally Chapter 8 is a bottoms-up approach of nanoscale silicon based meta-materials using diblock copolymers as templates for etching into silicon.

Part III offers conclusions and perspectives on this body of work and suggests future directions of work to carry the work done in this thesis to its final purpose.

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Part I –

Metamaterials and superlattices

Chapter 2
State of the art of structured metamaterials

2.1. Introduction

Artificially engineered materials have emerged in design with properties and functionalities previously unattainable in naturally occurring materials. The scientific advances made in this area of new metamaterials is closely interconnected with progress in physical development of structural design, novel fabrication and characterization methods. The intrinsic behavior of these new metamaterials is thus being studied from both fundamental and practical points of view.

Typically, they are assemblies of multiple elements of individual materials fashioned from conventional materials, for example, metals or plastics. However they form metamaterials when they are typically arranged in a periodic manner. These metamaterials gain their properties from the intricacies of their structure and not necessarily from their composition. Their characteristics such as size, shape, geometry or orientation can influence the waves of light or sound in an unconventional manner, creating material properties which are otherwise unattainable in conventional materials. For instance, electromagnetic and acoustic metamaterials achieve desired properties by incorporating structural elements of sub-wavelength sizes in their designs [1, 2].

Most of the current research in electromagnetic metamaterials investigates materials with negative refractive index [3-5]. These materials permit the creation of super-lenses which can have a spatial resolution below that of the wavelength. Although the first metamaterials were electromagnetic [3], acoustic and seismic metamaterials are also areas of active research [6, 7]. Potential applications of metamaterials are diverse - including remote aerospace applications, sensor detection, smart solar power management, public safety, high-frequency battlefield communication and lenses for high-gain antennas, improving ultrasonic sensors, and even shielding structures from earthquakes [7-10]. Figure 2.1 shows an illustrative chart [11]

of the progress made in scaling artificial magnetism, negative refraction and other novel phenomena such as sub-diffraction imaging to optical frequencies [12-16].

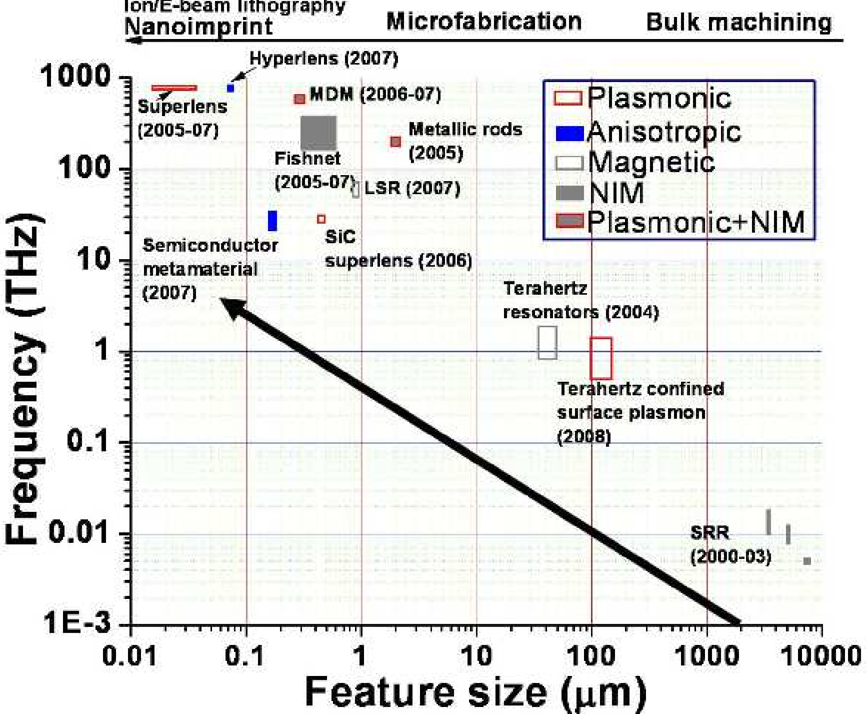


Figure 2.1. Progress made in scaling metamaterials from microwave to optical frequencies with change in feature size and the fabrication technology listed on top (reproduced from [11]).

Considering that our goal in this thesis is to create metamaterials with improved thermoelectric properties, we start exploring the state of the art of metamaterials developed in other areas of physics. In this chapter, we focus on metamaterials based on thin film stacks through a variety of examples which will be discussed in subsequent sections

2.2 Metamaterials based on multi-layered thin-film stacks

As described in the previous section, metamaterials have different specific characteristics that define their applications – magnetic (giant magnetoresistance – GMR) [17], optical (Bragg mirrors) [18], piezoelectric [19] or thermal [20] among others. The realization of metamaterials utilizes many different well-established techniques depending on the geometry and application. These include (but are not exhaustive) giant magnetoresistance (GMR) structures, giant magnetostiction devices, lasers, III-V semiconductors, superlattices for lasers and other optoelectronic devices, composite materials for piezoelectric and plasmonic

applications. A couple of these applications and techniques to fabricate them are described below.

2.2.1 Giant Magnetoresistance (GMR)

Giant magnetoresistance (GMR) is defined as a quantum mechanical magnetoresistance effect that has been observed in thin-film structures composed of alternating ferromagnetic and non-magnetic conductive layers. In fact the Nobel Prize in Physics for the year 2007 was awarded to Peter Grünberg and Albert Fert for this discovery. The effect is indicated by a significant change in the electrical resistance depending on the orientation of the magnetization of the adjacent ferromagnetic layers - in parallel or an antiparallel alignment [21]. The overall resistance is relatively high for antiparallel alignment and relatively low for parallel alignment. The direction of magnetization can be controlled, for example, by applying an external magnetic field. The effect is also dependent on electron scattering and on the spin orientation. One of the main applications of GMR is in magnetic field sensors, which are used to read data in hard disk drives and biosensors, amongst other MEMS devices [22, 23].

2.2.2. III-V semiconductor superlattices

Semiconductors are particularly attractive for integration into reconfigurable metamaterials. The conductivity of a semiconductor can be modulated by a variety of mechanisms, including applied voltage or applied heat or even illumination by light. Semiconductor fabrication is well developed, with methods for integration of many active devices now well established. In 2006, Padilla *et al.* [24] applied photo doping to change the carrier concentration in a high resistivity GaAs substrate, the top of which, a copper metamaterial structure was patterned using traditional photolithography techniques. The background available in III-V semiconductor-based superlattices to create new planar metamaterials is extensive and vastly studied [25-28]. These superlattices are typically fabricated by molecular beam epitaxy to deposit successive layers of materials to make periodic structures that function differently from their component layers [29-31].

2.3. Metamaterials based on silicon micro- and nano-structuration

The previous section detailed applications of metamaterials created from different component materials like III-V semiconductors, electromagnetic and ferromagnetic materials in the form of ultra-thin films whose thickness is on the order of a few or a few tens of

nanometers. In this section, we focus on metamaterials based on silicon micro and nano-structuration at different scales for realizing a variety of applications like photonic crystals including Bragg mirrors [32-35], Terrahertz metamaterials [36] and super hydrophobic surfaces [37], among others.

2.3.1. Photonic crystals

Photonic crystals are periodic arrangements of dielectric materials that exhibit strong interactions with light. They can be fabricated for one, two, or three dimensions. Bragg mirrors fall under thus category can be seen as a 1D photonic crystal. One-dimensional photonic crystals can be made of layers deposited one on the other (*e.g.* Bragg grating); two-dimensional by, drilling holes in a suitable substrate, and three-dimensional structures can be made by, for instance, stacking spheres in a matrix and then dissolving the spheres [38]. In principle, photonic crystals can find uses wherever light needs to be manipulated. Existing applications include thin-film optics with coatings for lenses and mirrors and colour changing paints. Two-dimensional photonic-crystal fibers are used in filters and nonlinear devices.

2.3.2. Phononic crystals

Phononic crystals [39] are similar to some extent to photonic crystals as they result from periodic arrangement of two materials. The main difference with photonic crystals is that they relate to the acoustic domain instead of the electromagnetic domain. Therefore, phononic crystals can be designed so that they act as filters to acoustic waves extending to the ultrasound range, in a specifically designed wavelength range. This behavior can be seen as similar to an optical Bragg reflector that filters light in a given wavelength range. More interestingly, phononic crystals can be seen as selective filters to phonons, including acoustic phonons that carry not only acoustic waves but also heat. At the end, phononic crystals can act as filters to heat propagation and hence to a passive way of reducing thermal conductivity [40].

2.3.3. Vertical periodic structures as opposed to planar

Traditionally all these metamaterials used to be fabricated in planar or stacked forms, mainly multilayered thin film deposits, as described above. In fact, traditional Bragg mirrors are fabricated using similar technologies. However, there is an alternative to this planar form, which consists of constructing a vertical arrangement of multilayers, as the result of a single etching step of several deep trenches, whose widths are precisely controlled. The photonics group of our laboratory has successfully fabricated *vertical* Bragg mirrors of this kind [43].

Figure 2.2 shows (a) the schematic illustration of the vertical Bragg mirror and (b) the SEM of the realized structure.

The mirror is realized using a two-step DRIE etch process. The key advantage of this type of structure is the ability to use a single wafer for the realization of the metamaterial (in this case, a Bragg mirror), the ability to benefit from lithography in cavity design as well as the ease of fabrication as opposed to conventional Bragg mirrors [43], which require lengthy multiple steps of deposition of very precise thickness, in order to achieve the required periodic structuration.

It is envisioned that the same technology may be extended to realize other kinds of metamaterials. Our aim is to try achieving such metamaterial from vertical structured silicon with specifically optimized thermoelectric properties.

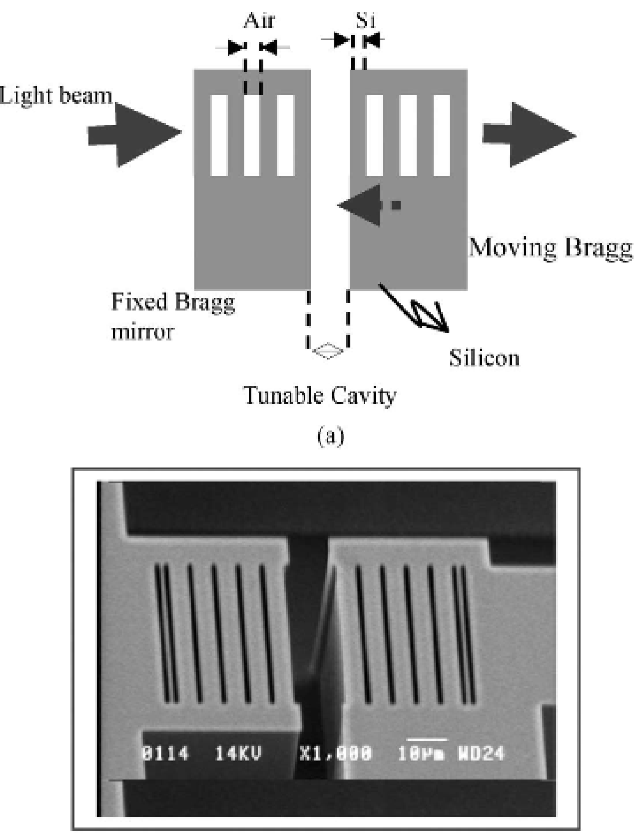


Figure 2.2. (a) Schematic of the vertical Bragg mirror and (b) its realization imaged under SEM.

2.4. Conclusions

Metamaterials are an extremely important class of materials used for engineering new materials with improved characteristics. In the previous section, we have described in Bragg mirrors that by making a single change of fabricating them in a vertical fashion as opposed to planar, a huge impact was created in performance and cost effectiveness.

In a similar manner, we seek to improve the fabrication process of the planar superlattices that are currently being used in thermoelectric applications with a similar methodology. This is the focus of this work – to fabricate vertical superlattice silicon based metamaterials with improved thermoelectric characteristics.

Chapter 3
Towards thermoelectric materials based on vertical superlattices

3.1. Vertical Superlattices

Chapters 1 and 2 focused on the principles of thermoelectricity and the characteristics of metamaterials. Based on these discussions, we have drawn some valuable conclusions from a study of literature available, on which our device needed to be based on. One of the key goals of this work is to reduce fabrication costs of the device and hence we have devised the idea of fabricating vertical superlattices as a solution to the problem of hotspot cooling by thermoelectric means. Figure 3.1 shows a comparison of conventional superlattices as opposed to vertical superlattices.

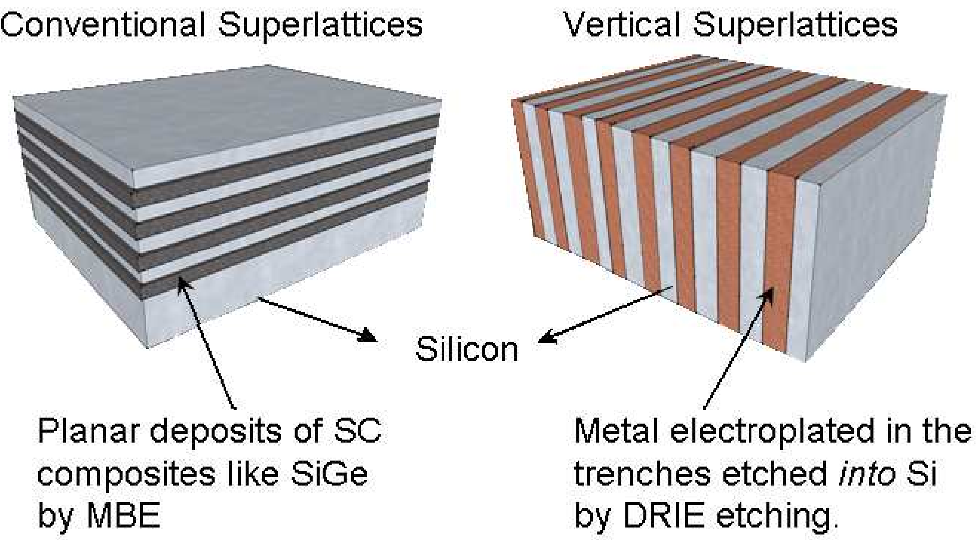
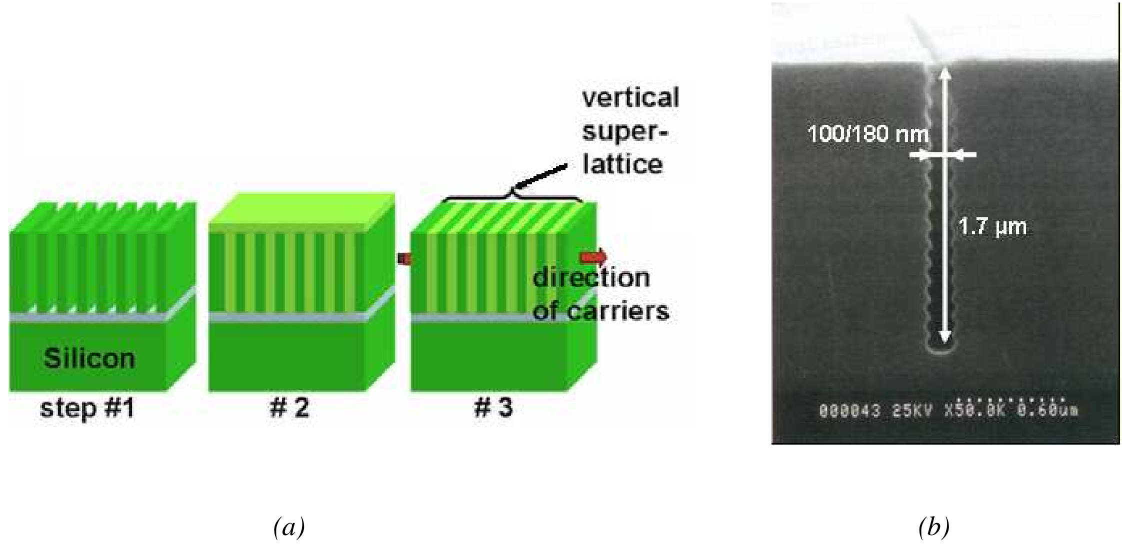


Figure 3.1. Comparison of conventional superlattices with vertical superlattices.

The most significant features of a vertical superlattice configuration are as described below –

- Vertical superlattices are achievable directly into Silicon (just 3 main steps: 1 patterning/etch step followed by a deposit step and a final leveling step)
- Significantly reduce manufacturing time and costs.

- High-energy electrons can potentially contribute to heat transfer in a structured material, therefore reducing thermal conductivity while maintaining high electrical conductivity. Heat transfer can be produced in any direction, upon modification of the periodic 1D pattern into 2D. Further improvement can be achieved by the introduction of *controlled roughness* at the interfaces (achievable by the 'scalloping effect' of the DRIE Bosch process – See Figure 3.2 (b) [44]), which provides additional structuration in the third dimension.



(a) *(b)*

Figure 3.2. (a) Schematic of vertical superlattices (b) SEM image of scalloping effect from DRIE.

Microscale vertical superlattices

It is clear from the discussion in the previous sections that the thermionic effect that should result in ballistic transport of 'hot' electrons is achievable only at the nanoscale. However, in the work done in for this thesis, we have attempted to fabricate 'microscale' vertical superlattices before attempting the fabrication of nanoscale superlattices. This intermediate step is of high significance in extracting key empirical parameters such as thermal conductivity, thermopower, etc. of the metamaterial free of the quantum effects that are likely to be present at the nanoscale during characterization of the devices [45-48]. Theoretical models for prediction of thermal models have been studied by our partners at CETHIL in Lyon. The extraction of actual experimental data will aid in improving the theoretical model to a better accuracy. Aspects of this model and some experimental details are described in Section 3.3 of this chapter. This step would also serve to validate most fabrication and characterization setup issues that are likely to arise whilst fabricating

nanoscale superlattices as well. To this end, it was decided to fabricate 5 µm and 15 µm –wide superlattices in silicon with a depth of over 100 µm into the substrate.

3.2. Materials and process selection

3.2.1 The first material

One of the two materials of the superlattice layer was chosen as highly doped single crystalline silicon for the following advantages that it has to offer over other materials –

- *n*-type
  - *Electrons* as the charge carriers in *n* type silicon have higher mobility than the *holes* in *p*-type silicon owing to their lower mass.
  - Higher carrier mobility is in turn important, for it directly contributes to the electrical conductivity of the material. Hence, higher the mobility of a material, the better the figure of merit, *ZT*.
- Possible monolithic IC integration.
- Established technologies with low fabrication costs and available facilities.

3.2.2 The second material

For the second layer for the superlattices, the following key criteria are to be met:

- The chosen material should *not* diffuse into silicon at high temperatures. This is important because the first material has been chosen as silicon and since the likely application of this thermoelectric device is in 'hot spot' cooling, the whole setup can be expected to experience at least >100°C temperature. The diffusion of a metal into silicon largely varies it's electrical and thermal properties and is unsuitable for utilization in solving the thermoelectric cooling problem [49-51].
- High electrical conductivity
- High Seebeck Coefficient
- Low thermal conductivity

These characteristics have been discussed in previous chapters as the ideal characteristics to have for a good figure of merit of the thermoelectric material. For our purpose of fabricating a thermoelectric cooling device, we desire a metal with work function comparable to the Fermi level of the semiconductor of choice in order for possible thermionic emission as detailed in Chapter 1. Table 3.1 is a summary of the different electronic parameters of different materials.

Table 3.1. The numerical data pertinent to different materials as compared with highly doped *p*-and *n*-type Silicon. The highlighted boxes in blue represent the values of the material most desired with respect to our selection of the second material.

Metals that diffuse into Silicon	Metals that do not diffuse into Silicon	Seebeck Coefft. @ 300K (μV K^{-1})	Fermi Energy* @300K (eV)	Work Function** @ 300K (eV)	Electrical conductivity (/Ωm) x 10^6	Thermal conductivity at 300K (W/mK)
Highly doped *n* type Silicon		+540[55]	0.55[55]	4.52[53]	0.05[55]	150[55]
Highly doped *p* type Silicon		+450[55]	-0.55[55]	4.52[53]	0.0285[55]	147[55]
Copper (Cu)		+1.84[52]	7.00[53]	4.7[53]	59.17[53]	401[53]
Gold (Au)		+1.94[52]	5.50[53]	5.1[53]	45.2[53]	310[53]
Chromium (Cr)		--	4.5[53]	--	7.74[53]	93.7[53]
Aluminum (Al)		-1.8[52]	11.6[53]	4.08[53]	37.45[53]	250[53]
Nickel (Ni)		-20[53]	5.15[53]	5.01[53]	14.3[53]	91[53]
	Titanium (Ti)	+7.5[56]	-4.33[54]	4.45[53]	2.34[53]	21.9[53]
	Tungsten (W)	+7.5	4.5	4.55[53]	162.0[53]	174[53]

* The Fermi level is the level at which electron/hole occupancy is the highest filled at 0K. The corresponding energy of the charge carriers at that level is the Fermi energy.

** The work function is the energy required to remove the uppermost electrons or the lowermost holes from this energy state.

3.2.3. Material choices and limitations

From the values in the above table, we can conclude that the material that seems best suited to our application is *Tungsten*. However, it must be noted that through electrodeposition, mostly an oxide of tungsten is deposited for very limited thicknesses in the nanometer range under very controlled conditions [57-60]. Hence for the microsuperlattices with depths of over 100 µm to be filled, this option is unfortunately, ruled out. However tungsten is a common material in Atomic Layer Deposition (ALD) [61-63]. Thus, this is a viable option for the nanoscale vertical superlattices. And this is especially important for the reasons discussed in the previous section pertaining to thermionic transport at the nanoscale.

Hence while considering the microsuperlattices, we need to pursue other options to fill the trenches. With well-developed copper electrodeposition techniques and facilities at our cleanroom, in ESIEE, it was decided to attempt to fill the microsuperlattices with copper as the main metallic material. However this posed some additional considerations. This is due to the fact that copper does not have good adhesion to silicon [64]. Hence, it needs an additional layer – an *adhesion layer* for it to "stick" on silicon. In our cleanroom, we use *Titanium* as the adhesion layer [65] because of its availability to be sputtered at our cleanroom and its excellent anti-diffusion properties as detailed in Table 3.1 and additionally in Table 3.2.

Table 3.2. Metal diffusion into silicon at elevated temperatures [66, 67].

Metals that readily diffuse into silicon	**Metals that don't diffuse into silicon**
Cu, Au, Cr, Al (sparse), Ni	Ti, W

The choice of these metals results in additional problems that were initially unexpected. We now have two metals (Cu and Ti) instead of one. This means that the interface properties will be greatly modified from the initial assumptions. However this will not affect the nano-superlattices as we expect to be able to deposit a single metal (W) by ALD.

3.3. Characterization of Microsuperlattices

To be able to design a suitable mask to fabricate the microsuperlattices, it is prudent to visualize the characterization and measurement systems that need to be in place to measure thermal parameters from the fabricated devices. To this end a sound understanding of the

physics of heat transfer between materials and a design to measure thermal elements is required.

3.3.1. Thermal conductivity of nanomaterials

The final objective of this work is to fabricate multilayer metamaterials with high thermoelectric power. The performance of these materials depends on their thermal and electrical conductivity, and thermoelectric conversion factor among others. The lower the thermal conductivity, the better the conversion efficiency, all else being equal.

Considering a classical macroscopic approach, the heat transfer in multilayer materials is governed by the behavior of heat-carriers within each layer and the interactive behavior between each layer [68-70]. A thermal resistance can be associated with these two phenomena: R_c for the resistance of each layer and R_i as the interface resistance [69-71].

The thermal resistance R_c of the layer depends on the following parameters:

- The nature of the material: Heat conduction across metal interfaces with dielectrics and semiconductors governs the behavior of many nanostructured materials and devices [72]. In the past, the importance of interface resistance in metal/dielectric multilayers with periods of a few nanometers has been observed [73]. Conduction normal to these interfaces is complicated by thermal energy conversion between electrons and phonons near at the interface. This conversion facilitates the lowest possible thermal resistance because phonons are the dominant heat carriers in dielectrics and most semiconductors, while electrons are the dominant heat carriers in metals [74].
- The material structure: Crystalline or amorphous. The crystalline structure of course favors the propagation of phonons. This transfer mode is particularly effective and contrary to popular belief, the thermal conductivity of dielectric crystals such as Si, SiC, SiGe is of the same order of magnitude at room temperature the thermal conductivity of most metals. Amorphous materials such as SiO_2 (glass) have a thermal conductivity of one or two orders of magnitude below the crystalline dielectric materials and electric materials. The presence of defects (grain boundaries, dislocations, interstitial gaps, substitution etc.) restricts the transfer of heat.
- The thickness of the layer: If the layer thickness is greater than the mean free path of free carriers traveling across the heat gradient so that the heat transfer is described by the diffusion equation, the thermal conductivity is maximal and does not depend on the thickness. When the thickness becomes the same order of magnitude or less than the

mean free path of the carriers, the thermal conductivity decreases. The difficulty lies in the coupling between the heat transfer in the layer and interfaces.

- The temperature: At around room temperature, the thermal resistance due to heat transport by phonons is almost constant and can even increase slightly as the temperature increases.

An important conclusion was drawn from literature review concerning the effect of the layer thickness coupled with the presence of defects [75, 76]. When having a starting layer of nanometric thickness, the thermal conductivity of the multilayer material increases when the layer thickness increases. This is explained by the increase of free carriers traveling through each layer. However, it has been shown in the case of materials Si / Ge, the thermal conductivity decreases from beyond a certain value of the layer thickness. This effect can be explained by the presence of defects in larger quantities (e.g. dislocation).

For metallic materials, the magnitude of the electron mean free path is typically a few nanometers. However, it has been shown that the thermal conductivity of metal films decreases with increase in film thicknesses. This effect is attributed to the decrease in grain size, increasing the number of grain boundaries and thus the thermal resistance associated with their presence. It is therefore particularly important to keep in mind the important role of defects on the value of the thermal conductivity.

Interface thermal resistance or contact resistance involves the Kapitza thermal resistance and thermal resistance of constriction. The thermal resistance of constriction is associated with the presence of roughnesses [77-79] which does not conform to the surface of the two materials in contact so that the contact surface is less than the apparent contact surface (See Figure 3.3 [78]). Thus the heat flux lines crossing the interface undergo constriction from one material to another, extending their path and thus increasing the thermal resistance. Where there is no constriction, there remains a phenomenon called Kapitza resistance which is related to the difference between the phonon vibration behavior and energy level of the electrons (for electrical materials) of the two materials in contact.

When the dimensions of the surface roughness are greater than the average mean free path of the free carriers then heat constriction resistance can be evaluated from the classical model of heat conduction equation by solving the heat diffusion equation.

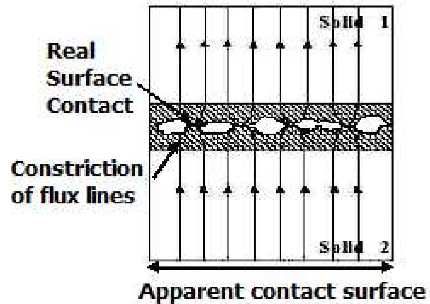


Figure 3.3. Representation of the phenomenon of constriction of flux lines during real contact vs. apparent contact of two surfaces [reproduced from 78].

The orders of magnitude range from 10^{-3} to 10^{-6} m² K / W depending on:

- The dimensions of the roughness.
- The nature of the materials in contact via their thermal properties (shape constriction) and mechanical properties (deformation of the asperities).
- The pore fluid in the cavities.
- The contact pressure.

The Kapitza resistance is typically of the order of 10^{-8} to 10^{-10} m²K/W. This assessment is difficult. It relies, for dielectric materials on the modeling of the vibrational behavior of materials. It can also be approximated by calculations in molecular dynamics. However it is possible that the two resistances can coexist when the contact is perfect but the contact interface is not planar (See Figure 3.4), which makes for complex phenomena [79]. Furthermore, when the characteristic scale of the constriction resistance is greater than the atomic dimensions, the former dominates and the Kapitza resistance becomes negligible.

In the case of materials to be fabricated for this thesis, the materials considered (Si, metals) have thermal conductivities of the same order of magnitude [80]. The quality of the interface is directly related to the fabrication technique of the trenches in silicon. For instance, if the trenches are fabricated through the Bosch process, there is a “scalloping effect” which was described in Figure 3.2 (b).

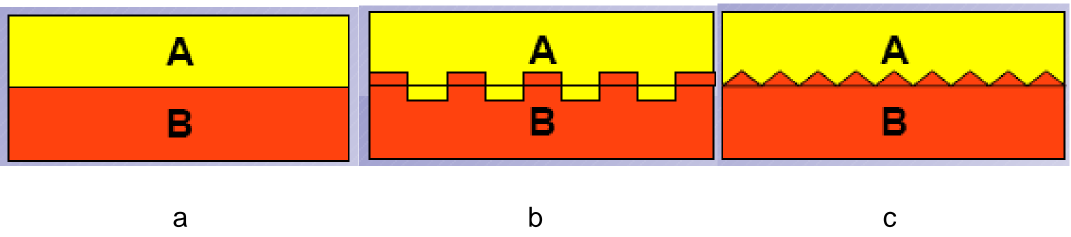


Figure 3.4. Perfect contact interface for materials A / B. (a) surface with only the Kapitza resistance (b, c) non-planar interfaces -- the Kapitza resistance and the constriction resistance involved.

The technique of depositing the second material will directly affect the quality of the contact. There will clearly be a contact resistance due to constriction phenomenon and a contact Kapitza resistance [78]. Experimental observations of the interface will determine the relative importance of these two phenomena.

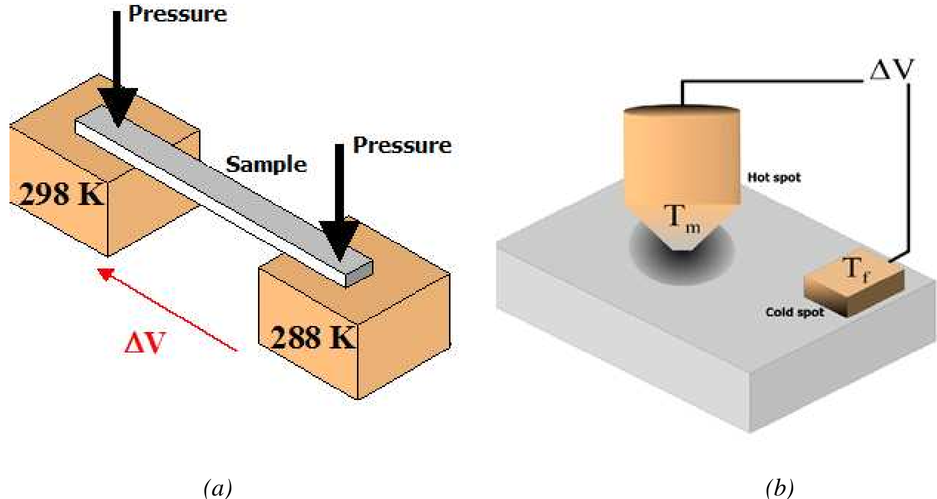
3.3.2. Measuring principle of the thermoelectric power (Seebeck coefficient) for metallic materials:

This section describes the techniques developed at INSA-Lyon (CETHIL and MATEIS laboratories) to characterize the heat transfer and thermoelectric power in structures with microscale and nanoscale dimensions.

For metallic materials, the measurement of thermoelectric power (TEP, also called Seebeck coefficient) can be achieved in two ways [81, 82]:

- ❖ In the MATEIS laboratory, the measurement of TEP occurs with a conventional measuring device shown schematically in Figure 3.5 a. Samples are then used in the form of plates of small sections (60 x 4 x 0.5 mm^3 approximately). Pressure is applied on the two ends of the samples using two blocks consisting of the same metal as a reference (for example copper). These parts are held respectively at temperatures T and $T + \Delta T$, where ΔT is small (typically $T = 15$ ° C (288 K) and $\Delta T = 10$ K). The temperature difference ΔT between the contact points of reference-sample is determined by a thermocouple. The thermoelectric power on the reference metal, $S = \Delta V / \Delta T$, and the average temperature $T + \Delta T / 2$ (typically 20 ° C), is calculated at each time. The duration is a measure of the order of one minute. For homogeneous samples, the TEP is a quantity measured independently of the geometry and dimensions of the sample. For heterogeneous samples, the TEP measured is representative of the volume of the sample to the temperature gradient. Metals having a very low TEP and therefore a tiny potential difference ΔV, low level amplifier has been specially designed to get viable output [83].

- ❖ Measurements on large parts or on-site non-destructive evaluation can be performed with a device whose principle is shown schematically in Figure 3.5 (b). This device comprises two copper plates (metal reference) applied to the surface of the piece:



(a) (b)

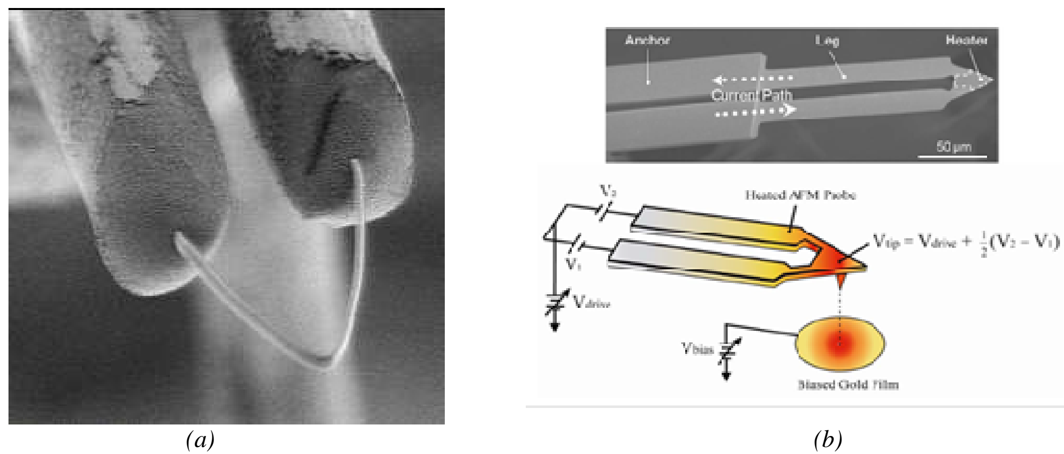
Figure 3.5. (a) Principle of the measurement of the thermoelectric power on sample plates and (b) principle of the measurement of the thermoelectric power of bulk sample (device tip)

- A plate that is called "cold spot", which is very small and takes the temperature *T* of the room
- A plate that is called "hot spot", in the shape of a cone whose apex is truncated by a plane surface. This end of the plate, and a circular shape of diameter *d* (*d* = 0.2 - 0.4 mm), is kept in contact with part of a controlled force. This plate is maintained at a temperature T_m, with a micro furnace consisting of a heating element surrounding the hot plate [84].
- A thermoelectric voltage ΔV appears between the two plates. The contact temperature of the hot plate $T + \Delta T$ is determined from T_m by performing an adjustment taking into account the field temperature. Finally, the TEP from the copper is determined as above. The value obtained is representative only of the area of the piece subjected to the thermal gradient: the hemisphere of radius about 3*d*. As the temperature *T* is imposed by the part, the average temperature of measurement is variable and it is necessary to restore the values of the TEP at a fixed temperature. This requires prior determination of a coefficient of variation of the TEP based on the temperature.

3.3.3. Development of characterization tools for thermal measurements on superlattices.

The technology and tools mentioned above cannot be directly applied to the superlattices fabricated in this thesis. In fact, they involve semiconductor materials whose electrical conductivity is much lower than that of metallic materials. The measuring chain, and amplifiers, etc. are not at all suitable for this type of measurement. In addition, the fragility of superlattices will also require adapting systems to contact the sample with reference blocks (See Figure 3.6(a)).

Simultaneous measurement of thermal conductivity properties and TEP requires further adaptation of the measurement system. With the prototype currently available at the laboratories of CETHIL [85], it was planned to modify it such that it can characterize the samples developed in this project in addition to the metallic samples that it is already equipped to deal with. To finely characterize the localized TEP (See Figure 3.5 (b) [86], it was planned to modify a scanning thermal microscope tip (SThM) in order to perform measurements at the micrometer scale (Figure 3.6(a)). For this, the SThM tip will be heated to a certain temperature and the resultant electric potential is measured. Upon contact with the superlattice, the potential difference appears between the two contact zones. Knowledge of this difference will be applied back to the TEP measurements. Mapping the thermoelectric properties of superlattices can thus be performed.



(a) *(b)*

Figure 3.6. (a) Scanning thermal microscope tip and (b) heated Si AFM tip heated (from [86]).

Figure 3.6 (b) shows a demonstration of the feasibility of measuring the thermoelectric power using a heated AFM tip [86]. The tip is heated to several degrees Celsius which then allows TEP measurement of the 200 nm silicon film. .

3.3.4. Calculations for sample design and *in situ* characterization

The accurate characterization of thermal properties of thin films poses many challenges. Many methods already exist for the measurement of thermal conductivity, *e.g.* the 3ω method, through thermal diffusivity measurement or the steady state technique [87]. However these techniques are effective on bulk materials more than thin films. When considering thin films, the determination of thermal conductivity in different directions, *i.e.* cross-plane, perpendicular to the film surface and in-plane, parallel to the thin film surface encounters further challenges. These are required to be done because a typical thin film has anisotropic thermal properties. Figure 3.7 (reproduced from [87]) shows the challenges associated with the measurements. The cross-plane measurements face the challenge of creating a substantial temperature drop across the film without causing a large rise in the temperature of the substrate whilst in-plane measurements are plagued by heat leakage through the surface, making it difficult to determine the actual heat flow in the plane of the film.

Over the years various techniques have evolved in trying to overcome these challenges. These have been illustrated in Figure 3.7 (b) (reproduced from [87]). These involve for the cross-plane measurements, the creation of a large heat flux through the substrate and measuring the surface temperature rather than the heat flux through the film. As for the in-plane measurements, the films are deposited on low-conductivity substrates so as to minimize leakage and enable spreading through a narrow heater or a buried insulation [87].

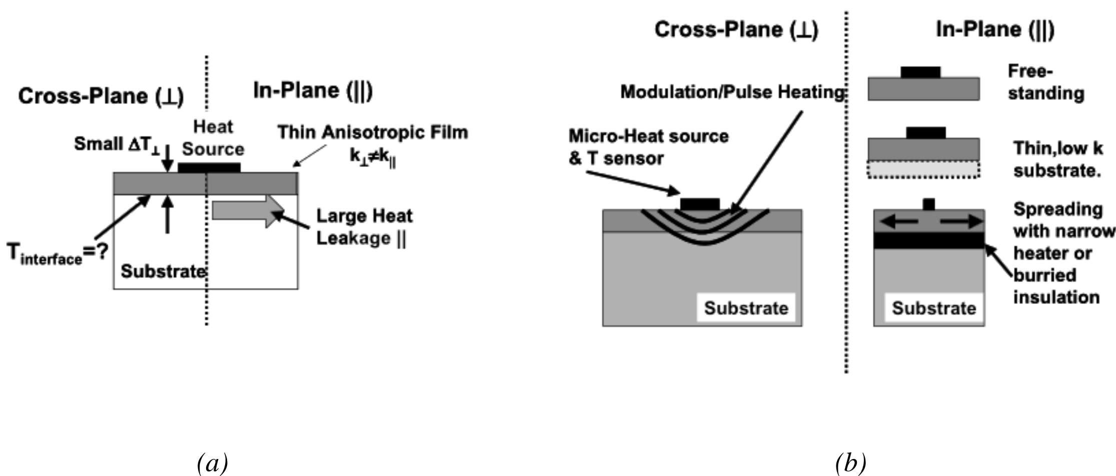


Figure 3.7. Illustration of (a) thin film sample configuration and characterization challenges and (b) strategies to overcome these challenges (reproduced from [87]).

To this end, the traditional 3ω method remains a popular choice for making cross-plane thermal conductivity measurements on a thin film. And later in this chapter we describe a modified 2ω method for making in-plane measurements consistent with our samples consisting of superlattices. These techniques have been described in the following sections.

3.3.4.1. 3ω method

3ω methods are an important class of techniques for measuring the thermal properties of thin films, wires, bulk samples and even liquids. These methods were standardized by Cahill [88] and by Birge and Nagel [89], who observed that for a certain set of thermal experiments driven by a current at frequency, ω, and the voltage at the third harmonic (3ω) contains important information about the thermal properties of the system. It was discovered that the second and first harmonics also contain the same information. In general, using the 3rd harmonic is still the best approach, although in certain special cases the 2nd or 1st harmonics may be preferred and rendered useful.

Figure 3.8 is an illustration of the traditional 1ω, 2ω and 3ω methods [90]. As seen in the figure, the sample has a metal heater that also acts as a temperature sensor (since its electrical resistance depends on temperature). The heater is driven by a sinusoidal current at frequency, ω. The resulting joule heating is at the second harmonic, 2ω and leads to a temperature fluctuation. This temperature fluctuation causes a ripple in the heater's electrical resistance, also at 2ω. Finally, the product of current (at 1ω) and resistance leads to a voltage contribution at 3ω, due to the mixing of sinusoids at different frequencies. This 3ω voltage is then used to extract the thermal properties of the system.

However, as the figure describes, it so happens that the analysis is richer than simplistically projected, particularly if the driving current is given a DC offset [90]. In this case the joule heating, temperature, and resistance all include components at DC, 1ω, and 2ω. As a result, the output voltage includes 1, 2, 3ω, and even a DC "0ω", all of which contain information about the thermal properties of the system.

Even when the DC offset is omitted from the driving current, for example in traditional 3ω, the 1ω output voltage can easily be used to study the thermal properties.

Consider a simple one dimensional heater deposited on the material to be measured as shown in Figure 3.9. It consists of four pads connected through a narrow line which acts as a heater wire.

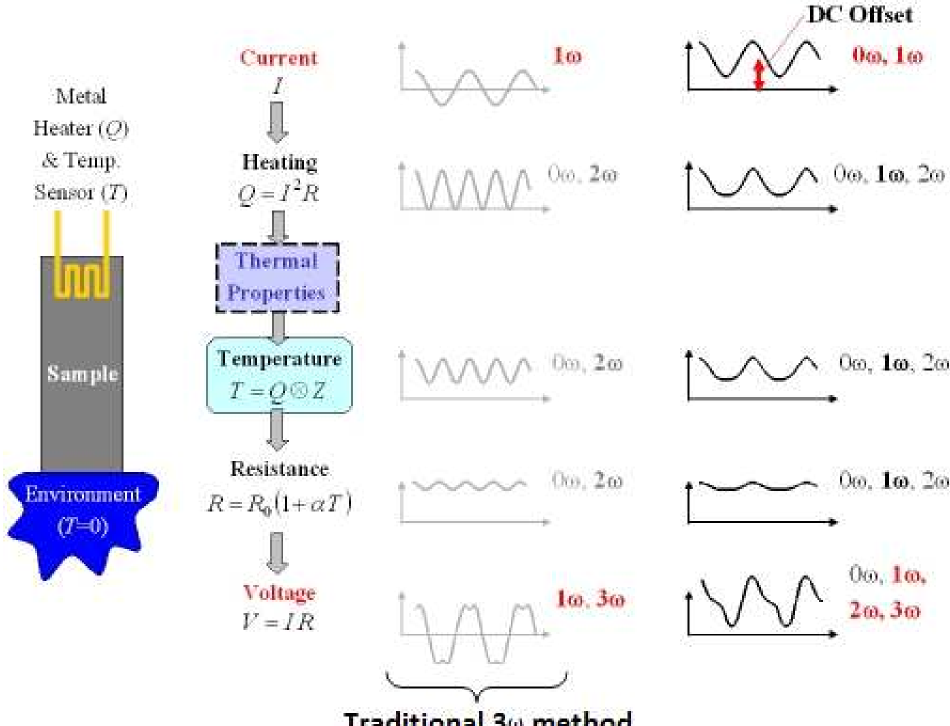


Figure 3.8. Illustration of the 1ω, 2ω and 3ω methods for thermal measurements (reproduced from [90]).

The outer pads are used for connecting probes to make a closed circuit while the inner pads are used to measure the electrical potential difference across the heater wire. Depending on the length (L) and width (w) of the wire, different resistances and voltages can be measured for a constant amount of current (by Ohm's law). The metal pads act simultaneously as a resistance heater and a resistance thermometer device (RTD).

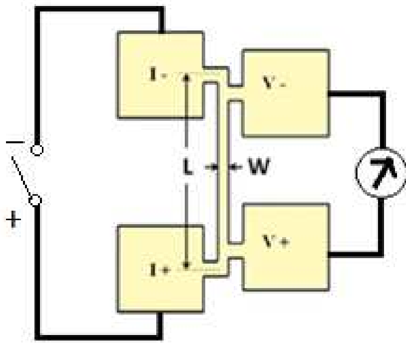


Figure 3.9. Schematic illustration of 1-d heater.

In an RTD, the equilibrium temperature of a specimen is determined by measuring the change in resistance of the metal filament in thermal contact with the specimen. For small temperature changes, the resistance of the filament varies with temperature as

$$R_h(t) = R_0(1+\beta_h \Delta T), \tag{3.1}$$

where β_h is the temperature coefficient of resistance (TCR) and R_0 and R are resistances at temperatures T_0 and $T_0 + \Delta T$, respectively [91]. Since the TCR for most metals is in the order of 10^{-3} K^{-1}, a Wheatstone's bridge is used to measure the minute changes in resistance by passing a DC signal through the RTD. The amplitude of the signal is kept small to minimize any heating from the RTD itself.

Now, consider an alternating current of frequency ω passing through the heater wire. It can be written as

$$I_{h,0}(t) = I_{h,0} \cos(\omega t), \tag{3.2}$$

where $I_{h,0}$ is the peak amplitude of the heater current at frequency ω and $I_{h,0}(t)$ is the instantaneous current passing through the heater. Assuming that the change in resistance is negligible compared to the amplitude of the current, it generates a Joule heating as stated below

$$P_h(t) = I^2_{h,0}R_{h,0} \cos^2(\omega t) = \frac{1}{2} I^2_{h,0}R_{h,0}(1+\cos(2\omega t)), \tag{3.3}$$

where $R_{h,0}$ is the nominal heater resistance and $P_h(t)$ is the instantaneous power produced by the heater. As it is observed, the instantaneous power can be split into two components; firstly the power attributed to the direct current (P_{DC}); and secondly, the alternate current power (P_{AC}).

$$P_{DC} = \frac{1}{2} I^2_{h,0}R_{h,0} = \frac{1}{2} P_{h,0}(t) \tag{3.4}$$

$$P_{AC} = \frac{1}{2} I^2_{h,0}R_{h,0} \cos(2\omega t) \tag{3.5}$$

The average power dissipated by the heater is called the root mean square (rms) power and is half the power dissipated by a DC current of the same amplitude. The oscillating component of the instantaneous power *does not* dissipate any average power over a single cycle. This power in turn generates a temperature change in the heater and the underlying substrate. This temperature change also has DC and AC components and can be written as follows

$$\Delta T = \Delta T_{DC} + |\Delta T_{AC}| \cos(2\omega t + \phi) \tag{3.6}$$

ΔT_{DC} is the steady-state temperature increase due to the rms power dissipated by the filament and $|\Delta T_{AC}|$ is the magnitude of the steady-state temperature oscillations due to the sinusoidal component of the power and ϕ is the phase angle between the temperature oscillations and the excitation current.

If the substrate has a thermal insulating layer, the heat stays in the heater and the temperature oscillation is substantial. Hence, measuring this temperature oscillation allows access to the thermal properties of the underlying substrate. To measure this temperature oscillation, one can measure the resistance of the heater and use the heater also as a temperature sensor. Moreover, the resistance of the heater varies with temperature as given by equation 3.1. It is worth mentioning that there is a difference between the rate of the resistivity change versus temperature $\frac{dR}{dT}$ and the TCR value

$$\beta_h = \frac{1}{R_0}\frac{dR}{dT} \tag{3.7}$$

By merging the equations (3.1) and (3.6), the general formula for resistance of the heater can be derived as follows [91]:

$$R_h(t)=R_{h,0}[(1+\beta_h\Delta T_{DC}+\beta_h|\Delta T_{AC}|cos(2\omega t+\phi)] \tag{3.8}$$

For us to now measure the resistance of the heater, the voltage drop across the heater must be measured. The expression of this voltage is given by multiplying equations (3.2) by (3.8) as follows using the Ohm's law (*V=IR*) -

$$V_h(t) = I_{h,0}R_{h,0}\ [(1+ \beta_h\Delta T_{DC})\cos(\omega t) + \frac{1}{2}\beta_h|\Delta T_{AC}|\ cos(\omega t + \phi)] + \frac{1}{2}\beta_h|\Delta T_{AC}|\ cos(3\omega t + \phi)] \tag{3.9}$$

From equation 3.9, it can be seen that the last voltage component is oscillating at third harmonic frequency. The magnitude of third harmonic voltage is typically 1000 times smaller than that of the first harmonic voltage [92] and also contains useful information about thermal conductivity of the specimen underneath. It is given by:

$$V_{h,3\omega} = \frac{1}{2}V_{h,0}\,\beta_h\,\Delta T_{AC} \tag{3.10}$$

Where $V_{h,0}$ and $V_{h,3\omega}$ are the peak amplitude of the nominal heater voltage at first and third harmonic frequency respectively. Both ΔT_{AC} and $V_{h,3\omega}$ are composed of in-phase and out of phase components.

Therefore with the information of the voltage at the third harmonic, the value of ΔT_{AC} and the knowledge of the input power and intrinsic properties of the material to be measured, it is possible to measure the TCR of the material (β_h).

3.3.4.2. 2ω method

Classic 3ω methods are typically used to make measurements on bulk samples and on thin-film samples by assuming that the thermal resistances through the thin films and substrate accrues in series. The thermal conductivity is then determined by measuring the thermal response of a film-on-substrate versus that in its absence. This measurement does not take the thermal contact resistance between the thin film and the substrate into account (which can be substantial at the microscale). More importantly, the estimated thermal parameters are on an effective volume that does not give access to directional thermal properties in the case of multilayered composite materials, for example [96].

In this work, we predominantly propose to use the 2ω method for making thermal measurements by decoupling the heating wire and studying the output voltage at the second harmonic for making cross-plane thermal conductivity measurements. This is more relevant to this work because it offers access to the directional thermal properties which is more suited to the topography of the superlattices under study. It is obtained by multiplying the 2ω resistance of a RTD, decoupled of the heating wire, by a small DC offset. It is noted that the DC current that is supplied is sufficiently small so as to not significantly heat the RTD and thereby heat the sample.

Most of the work described in this section have been done by our project partners at CETHIL-INSA Lyon. These principles and results have been published in a conference which is reference [96] of this section. They have been reproduced here with permission for the sake of congruity to this characterization section.

A schematic of the heater lines on the sample under consideration is shown in Figure 3.10. It consists of arrays of parallel heater lines deposited on the surface. The central line acts as the 3ω reference heater line and is supplied with a sinusoidal AC input of frequency $f = \omega/2\pi$. The other lines are supplied with a DC current. The lengths of the wires are chosen such that they can be assumed to be isothermal along their length and the heat diffusion is perpendicular to that (i.e., in the X direction).

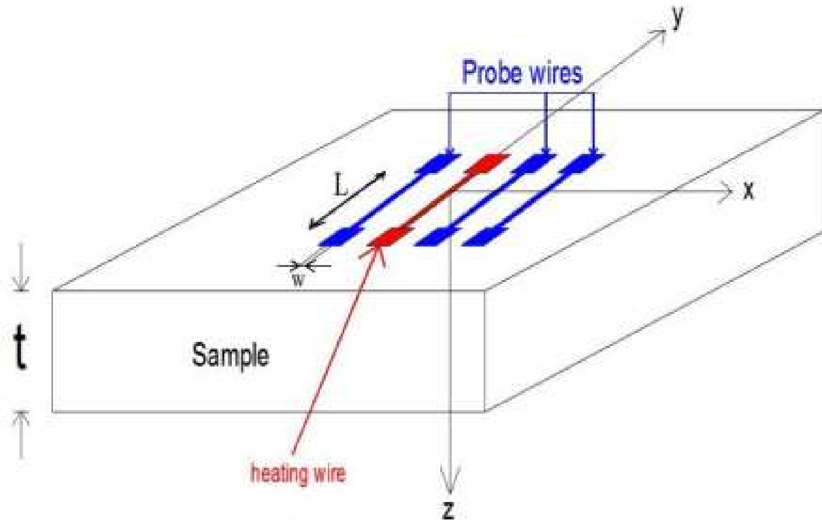


Figure 3.10. Schematic illustration of our sample (reproduced from [96]).

The conductive diffusion of this heat from the source in the material produces a rise in $\Delta T_{DC}(x)$ and a corresponding rise at $\Delta T_{2\omega}(x)$, where 'x' denotes the distance between the central heating source and the other resistive wires as shown in Figure 3.9.

Therefore for the 2ω case, equation 3.6 can be written as [96]

$$\Delta R_{2\omega}(x) = R_0(x)\, \beta_h \,\Delta T_{2\omega}(x), \tag{3.11}$$

where $R_0(x)$ is the electrical resistance of the wire at the ambient temperature.

For this change in resistance, a DC current input of low magnitude, I_0 is injected to measure the corresponding second harmonic voltage by a lock-in voltage amplifier at the ends of the wire, given as

$$\Delta V_{2\omega}(x) = \Delta R_{2\omega}(x)\, I_0 = R_0(x)\, \beta_h \,\Delta T_{2\omega}(x) I_0 \tag{3.12}$$

Now when considering our sample, we make a basic assumption that the thermal diffusion length μ of the material given by $\mu = \sqrt{\frac{D}{2\pi f}}$ (3.13)

is much larger than the thickness 't' of the suspended thin film wire array, i.e. $\mu \gg t$.

The condition $\mu >> t$ can be verified while working at adapted frequencies. In this case, the thermal gradient in the sample thickness may be assumed as 0 (in the Z direction) and the thickness t can be chosen so the Biot number defined as $B_i = h.d/k$ is much smaller than 0.1, where h is the convective heat transfer coefficient. Then, the thermal behavior of the sample may be described as one-dimensional in the X direction.

Consider that diffusivity is defined as

$$D = \frac{\lambda}{\rho C} \tag{3.14}$$

Where λ is the thermal conductivity, ρ is the density and C is the heat capacity of the material.

With such an assumption, the thermal gradient in the Z direction is zero and hence the thermal behaviour of the sample is restricted to 1-D in the X direction. Therefore with $\mu \gg t$, the second harmonic temperature decay measured along a distance 'x' from the heater can be written as [96]

$$\Delta T_{2\omega}(x) = \Delta T_{2\omega}(x=0) e^{-\frac{x}{\mu}} e^{-i\frac{x}{\mu}} \tag{3.15}$$

Thus, the thermal diffusivity, D can be deduced from the attenuation of the amplitude of $e^{-\frac{x}{\mu}}$ and the variation of the phase of ($-x/\mu$), both as a function of x. If D_{am} and D_{ϕ} are considered the amplitude and phase components of the diffusivity, they are extracted experimentally from the signal measured from the probe wires and from equations 3.11-3.15. Thus a theoretically sound knowledge of the electrical properties of the metal used for the wires, in this case, gold, is required.

Furthermore, by adjusting the amplitude of the AC current, I_{ac}, we can control the DC temperature of the sample at which the thermal diffusivity is measured. The value of this DC temperature is deduced from the measurement of the electrical resistance of the probe wires as shown

$$T_{DCexp} = \frac{1}{N}\sum_{i=1}^{N} \frac{(R(x_i) - R_0(x_i))}{R_0(x_i)\beta} + T_0, \tag{3.16}$$

where N is the number of probe wires, x_i is the discrete distance from the heating wire to the considered probe.

Hence by measuring the dependence of the temperature change at the modulating frequency at the second harmonic for a given distance of 'x', between the heating wire and the measurement probes, the thermal diffusivity of the sample can be determined. With all the other values known, determining the diffusivity of the material experimentally will allow the derivation of λ, the thermal conductivity of the material from equation 3.14.

3.3.5. Devices for measurement atop the superlattices

In order to make thermal measurements, it was decided to design a measuring device which would consist of a line of gold of 5 µm width, 200 nm thickness, and 7 mm length with two pads to apply current and two pads for measuring the voltage at 3ω. This thread will then serve as the heating and measuring element at 3ω as described in the previous section. Additionally, this design will be replicated in five or more copies of the same width and diameter, but shorter in length and arranged at regular intervals in the same side of the wire heater. The wire is used to probe, with measures of type 2ω. The devices are replicated to improve the quality of measurements and the schematic is shown in Figure 3.11. The different measurements from the different devices will help in obtaining the optimum measurements for the material beneath. To make the measurements of TEP on a scale of few hundreds of µm, the insulation layer covering the superlattices is removed (marked P on Figure 3.11) on each side of the pads to make 2ω measurements. The TEP measurements and conductivity in near-field could be carried out on these bare areas, using a type of SThM tip as discussed in previous sections.

The pads marked *I* used to bring the current, the pads marked *V* are used to make measurements by classic 3ω method. The C pads will be used for 2ω measurements, and the P pads used to measure the local electrical conductivity and TEP.

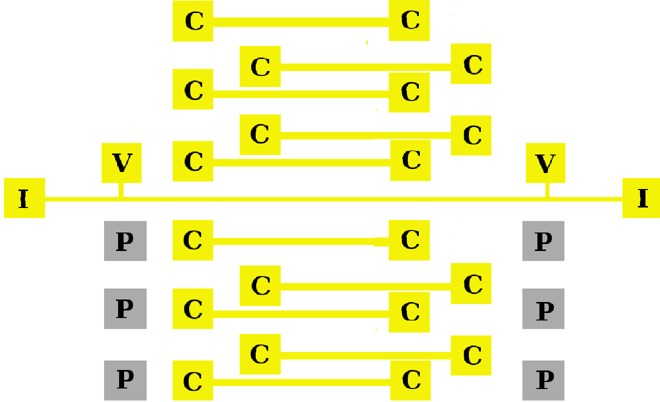


Figure 3.11. Configuration for the proposed 2ω measurement device.

The same device would be made into multiple copies:

- ❖ For calibration - on a blank wafer.

- For measurement parallel to the layers of the superlattices, in order to measure the thermal conductivity in the perpendicular direction, λ_{perp}
- For measurement perpendicular to the layers of the superlattices, in order to measure the thermal conductivity in-plane, λ_{para}.

The final design depicted in Figure 3.12. Elongated bonding pads are provided to facilitate dicing of the individual measurement wafer bits to serve for the different purposes such as calibration, in-plane and cross-plane thermal measurements. The areas have been colour coded to show their individual measurement goals in the figure.

3.4. On chip facilitation

The ultimate goal of designing the measurement devices is to fabricate them to facilitate measurement on top of the microsuperlattice structures. However, it is necessary to design a method to be able to interface the devices on the silicon die with the external electronics available for measurement. For this purpose, we propose to use 2 PCBs for the implementation, one which is individual to every device that is fabricated and another that is global to them all.

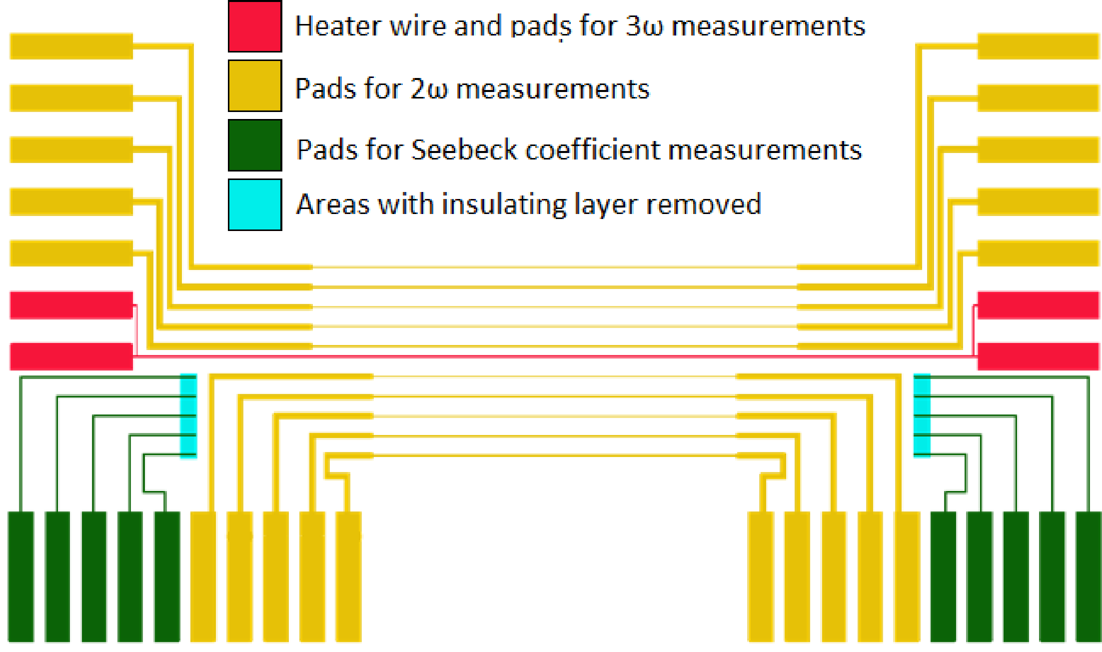


Figure 3.12. Final version of the measurement structures to be fabricated on top of the superlattices.

The individual PCBs would be slightly larger than the microfabricated silicon device itself only to facilitate wire bonding from it to the outside to provide connections to the rest of the circuit. The other PCB would be a global chip with connectors to connect with the measuring portals at INSA and with power sources and all other components relevant to the functioning of the chip.

The first PCB would then simply be able to plug on to the second one in order to make measurements. This is also economical, in that it would only be necessary to fabricate 1 of the larger PCB (with the connection electronics) and as many of the smaller PCB as there are devices for individual wire bonding. The 2 PCBs will henceforth be referred to as "Primary PCB", for the individual boards that will be used for wire bonding each of the silicon dies and "Secondary PCB", for the global board that houses all the connectors required to interface with the measurement electronics, throughout this manuscript.

3.4.1. Primary PCB

The logistics for the design of the PCB involve the following considerations:

- ❖ Incorporating 34 connection pads on which the measurement pads will be wire-bonded.
- ❖ Making a layout of the pads in such a way that there is the minimum distance needed to be wire-bonded, which is preferable to allow for lesser failures in the test devices.

With these considerations, the PCB was designed using Cadence and outsourced for fabrication.

3.4.2 Secondary PCB

The secondary PCB is to interface all the connections from the primary PCB and then make accommodations for interfacing with the measurement electronics on the outside. The electronic measurement instruments (the voltmeters, ampere-meters, etc.) possess BNC cables as their probes for making the measurements. Thus the secondary PCB is outfitted with BNC inputs.

Figure 3.13 shows the PCB interface assembly made for the measurement system. The silicon die is connected to the primary PCB by means of gold wire bonding. The thickness of these wires is ~25 μm and they serve as an electrical connection between the pads on the silicon die and the pads on the PCB. The length and strength of these wires determines the quality of the electrical contact and the signal strength for measurements. Also due to the

fragility of the wires, it is best to keep bonding length at the minimum possible. Figure 3.14 shows a picture of the interfacing between the chip and the PCB. The gold bonding threads are clearly visible.

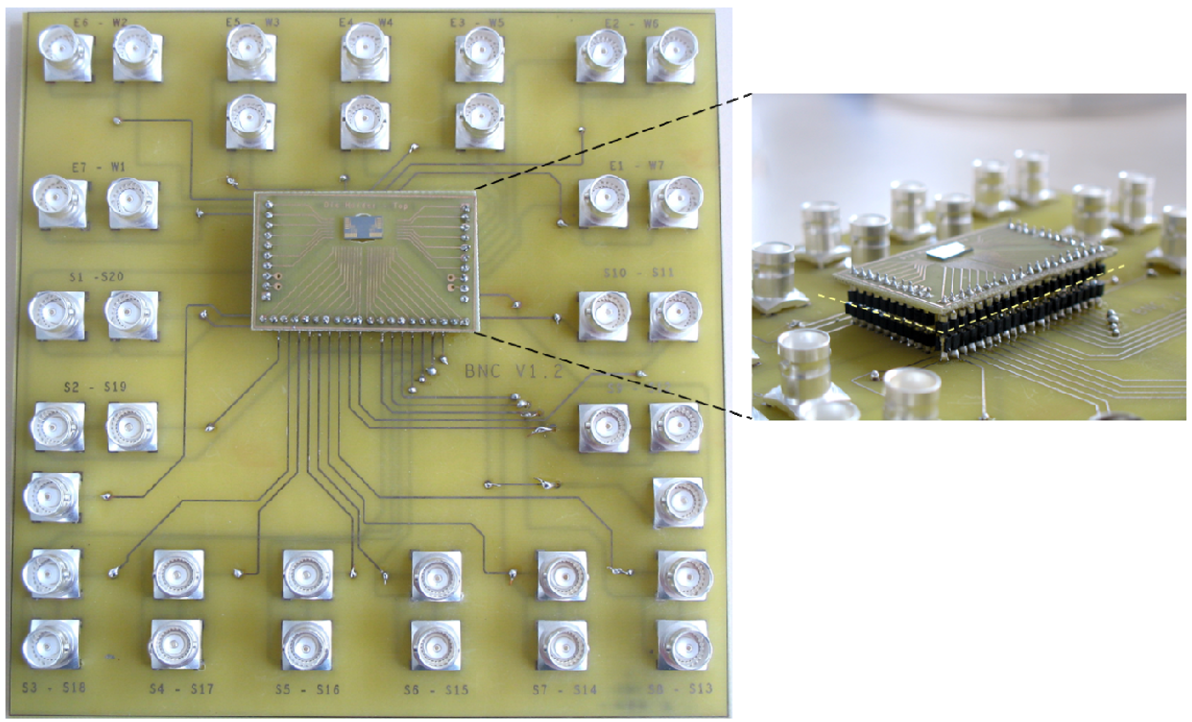


Figure 3.13. Completed PCB 2-board assembly. The secondary PCB (bottom) remains common across changing primary PCBs (top) with different samples.

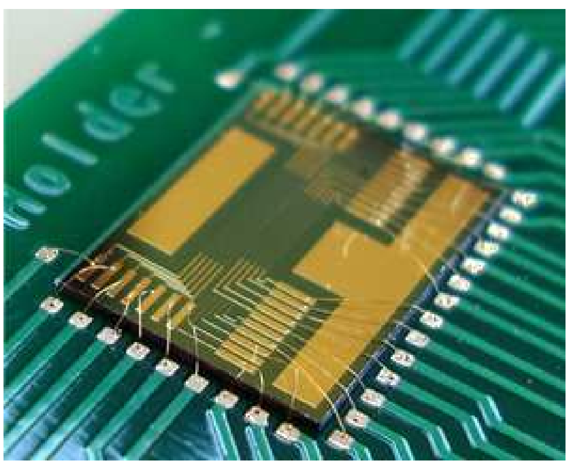


Figure 3.14. Chip wire-bonded to PCB

3.4.3. Challenges in wire bonding

Wire bonding of the chip to the PCB was a big challenge owing to number of bonds to be made in the small area. Each chip has 34 bonds to be made. The wire bonding setup at ESIEE is customized for IC fabrication. This resulted in additional challenges. The main challenges we faced were –

- The base for the wire bonder is customized to ICs which made it very difficult to hold the PCBs in place if not for the soldered connector pins.
- The gold tracks from the electroless plating are not very ‘thick’ or in other words effective enough to support good bonds.
- The strength of the bonds were not equally good for all 34 connections.

Additionally, the lengths of the wire bonds were significantly different for the 34 connections resulting in irregularities in measurement as well. This is an important consideration when interfacing with external electronics to get similar signal strengths.
Further challenges faced in the fabrication of the superlattices themselves will be discussed in detail in Section 3.7 of this chapter.

3.5. Test device and results

3.5.1. Fabrication of test devices

As a first attempt to validate the measurement setup and the fabrication of the characterization metal pads, we fabricate a chip on pure silicon substrate. Another reason for this is that since the thermal properties of pure silicon are well-documented in literature, it will be easy to validate our measurement system using the same. This intermediary step would also serve to tweak any device measurement parameters that needed to be modified in order to be able to make measurements on superlattices. Figure 3.15 shows the fabrication process in creating a measurement array on pure silicon.

The measurement device is of the form as described in Figure 3.12. The two main steps to achieving these patterns on the silicon substrate are photolithography and lift-off. For the lift-off, a 2 µm–thick nLOF® negative photoresist is spun on the silicon wafer and baked at 110°C for 1 minute on a hotplate. The patterns are exposed under and the sample is subject to a post-exposure bake of 1 minute at 110°C on the hotplate, followed by resist development

in a AZ-351B solution for 1 minute, creating an array of line openings into the resist layer on top of the sample. After the photolithography step, a bilayer chromium / gold, respectively of 50 nm-thick (Cr) and 450 nm thick (Au), is deposited on top of the sample by sputtering. The Chromium acts as an adhesion layer to allow gold to 'stick' on silicon. Lift-off is carried out under an ultrasonic acetone bath, thus completing the fabrication of the metal pads on silicon.

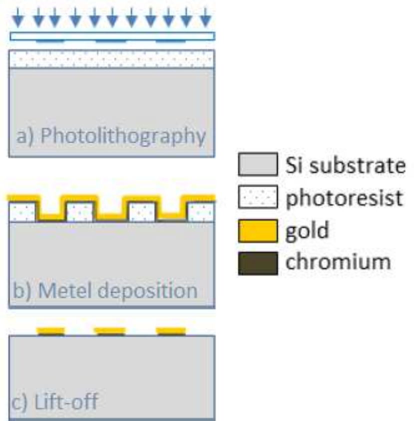


Figure 3.15. Fabrication steps for creating test measurement devices on pure silicon by lift-off.

3.5.2. Experimental setup

The work described in this section has been done by our project partners at CETHIL-Lyon. They have been reproduced here for the sake of lending clarity to the previously detailed description of the measurement system. A schematic of the experimental set-up is shown in Figure 3.16 (modified from [96]). It is of key importance to note that the same probe wire is used to detect the signal $V_{2\omega}$ and the phase lag Φ. The lock-in amplifier is synchronized with the AC generator to function with the same frequency f.

The electrical chip (silicon sample + gold wires measurement pads) is integrated in the electrical circuit via two Printed Circuit Boards (primary and secondary PCB as previously shown in Figure 3.13). As previously mentioned, the wire bonds are typically ~25 µm in thickness. As reported by Ji et al. [102], the electrical resistances of the bonding wires and the bond interfaces do not exceed 100 mΩ.

In this work, these resistances are considered negligible when compared to those of the chip gold wires. Moreover, it was verified using a multimeter that the electrical resistances of the connection between the primary and secondary PCBs are of few mΩ. Taking all of this

into consideration, it can be stated that the electrical resistance measured at the secondary PCB BNC plugs corresponds to the gold wire resistance of the electrical chip.

3.5.3. Results and discussion

Experiments performed were for frequencies of 20 to 80 Hz so that simple analytical modelling could be used. Two different magnitudes of current of 40 and 60 mA were generated in the heating wire for this domain of frequencies. The exponential tendency of $\Delta T_{2\omega}$ and the linear tendency of D are found for each current.

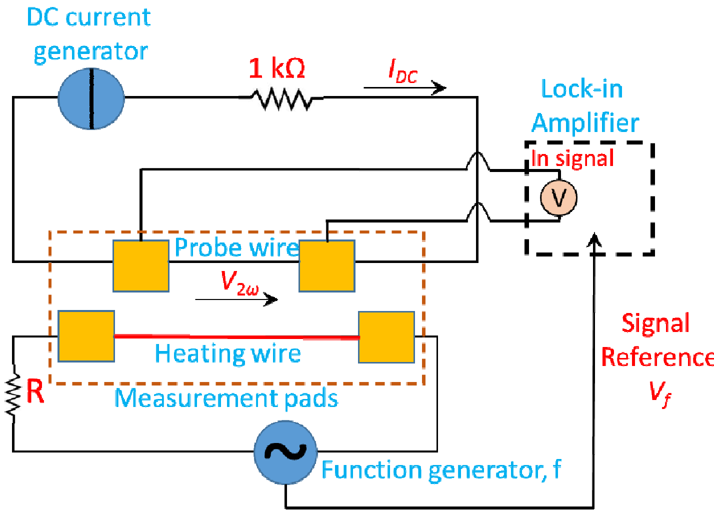


Figure 3.16. Schematic of the experimental setup for measurements on fabricated samples (modified from [96]).

Using equations 3.15 and 3.16, D_{am} and D_{ϕ} were determined. Table 3.3 summarizes the obtained diffusivities when compared to those in literature. We can see that these values lie in a similar range and are thereby congruent in validating our measurement method. Figure 3.17 (a) and (b) shows experimentally determined values of phase lag ϕ and $\Delta T_{2\omega}$ [96].

Table 3.3. Experimentally extracted diffusivity values for silicon [96].

Current I_{ac} (mA)	**$D_{theoretical}$ (x 10^{-5}m²/s)**	**$D_{experimental}$ (x 10^{-5}m²/s)**	**$T_{DCexperimental}$ (K)**
40	8.8	6.8±0.5	365
60	5.3	5.5±0.1	465

3.5.4. Conclusions and perspectives

The main advantage of this technique is that the thermal properties are predicted in-plane with the sample surface by the membrane method [87, 96]. Our partners at CETHIL-Lyon are currently performing a parameter influence study that shows that the accurate measurement of thermal properties at different temperature levels to imply a knowledge of the heat losses at the level of the system. The experimental results obtained are in agreement with the literature values for thermal diffusivity as well.

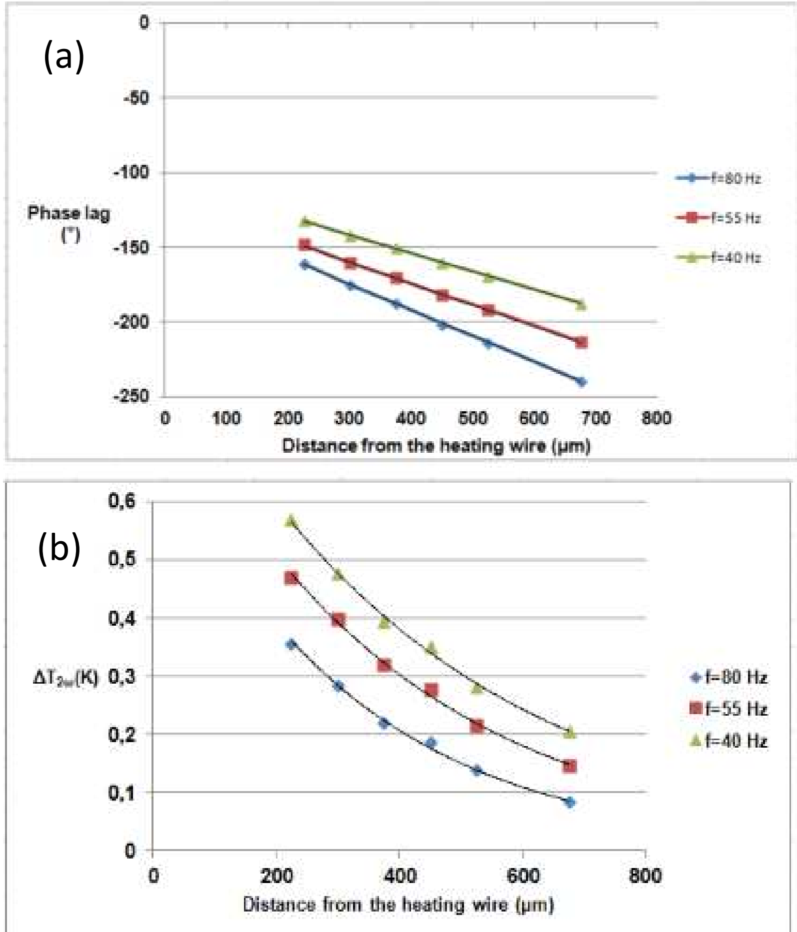


Figure 3.17. Results of experimentally determined (a) phase lag and (b) $\Delta T_{2\omega}$ as a function of the distance from the heating wire for Iac = 60 mA for different frequencies (reproduced from [96]).

3.6. Fabrication of microsuperlattices

In order to fabricate the microsuperlattices in silicon and subsequent measurement devices, a sequence of masks were designed to facilitate the simultaneous fabrication of both 5 µm and 15 µm features on the same wafer with separate zones designated for thermal conductivity measurements and for Seebeck coefficient measurements. Figure 3.18 is a detailed fabrication process flow chart for the fabrication of microscale vertical superlattices in silicon detailing the different fabrication steps that need to be performed in order to achieve HAR superlattices in silicon.

Fabrication results

Figure 3.19 (a) shows a scanning electron microscope image of the microsuperlattices that have been etched up to ~100 µm depth and Figure 3.19 (b) shows the cross-sectional view of these trenches then filled with copper by electrodeposition over a 100 nm sputtered Titanium adhesion layer. The voids at the bottom of the trenches result from lesser charge carriers and plating fluid being able to penetrate the trenches at these depths. Fortunately these voids serve to add the thermal conductivity of air into the trenches for effective heat dissipation [103, 104].

3.7. Challenges in fabrication

In this chapter, we discussed the need to fabricate vertical microsuperlattices in silicon and to characterize them to obtain thermal parameters free of quantum effects that are likely to be present at the nanoscale. While a part of this goal was achieved on a bulk silicon sample as discussed in the previous section, the use of the microsuperlattices by themselves as the base material proved to be more challenging than initially expected. The main problem was encountered at the polishing step post electrodeposition and during the wire bonding of the measurement pads to the PCB. All of the challenges faced and steps taken to surmount them will be discussed in detail in the following sections.

3.7.1. Electrodeposition

The electrodeposition of copper in wide trenches is very common in the area of Through Silicon via (TSV) manufacturing [105, 106]. However in the case of the microsuperlattice trenches, the electrodeposition is more challenging because (i) the trenches have smaller width and (ii) the trenches are in the form of wells which are not open through the wafer as in the case of vias. The electrodeposition setup at ESIEE was customized for our requirements. This involved the calculation of the time for the electrodeposition based on the applied current, the total surface area to be plated or vice versa. Higher the current, the higher the rate of deposition. However, the grain size of the deposit also increases. These factors have been taken into consideration while deciding on the best parameters for the electroplating experiments. Also in an effort to reduce the time consumed by a typical electrodeposition run at 0.1A (~6 hours), by doubling the current, the trenches caved in and result in what is called a 'dog-eared' formation. This phenomenon was observed with test trenches of 15 µm depth shown in Figure 3.20 (a).

The electroplating proceeds from the sides and 'meets' at the center. At higher currents, they tended to form a film on the sides and cave in from the top without filling them. Figure 3.20 (b) depicts a close up of trenches, which when filled properly still result in a crack-like feature at the center of the trench formed by the 'meeting' of the electrodeposited sidewalls.

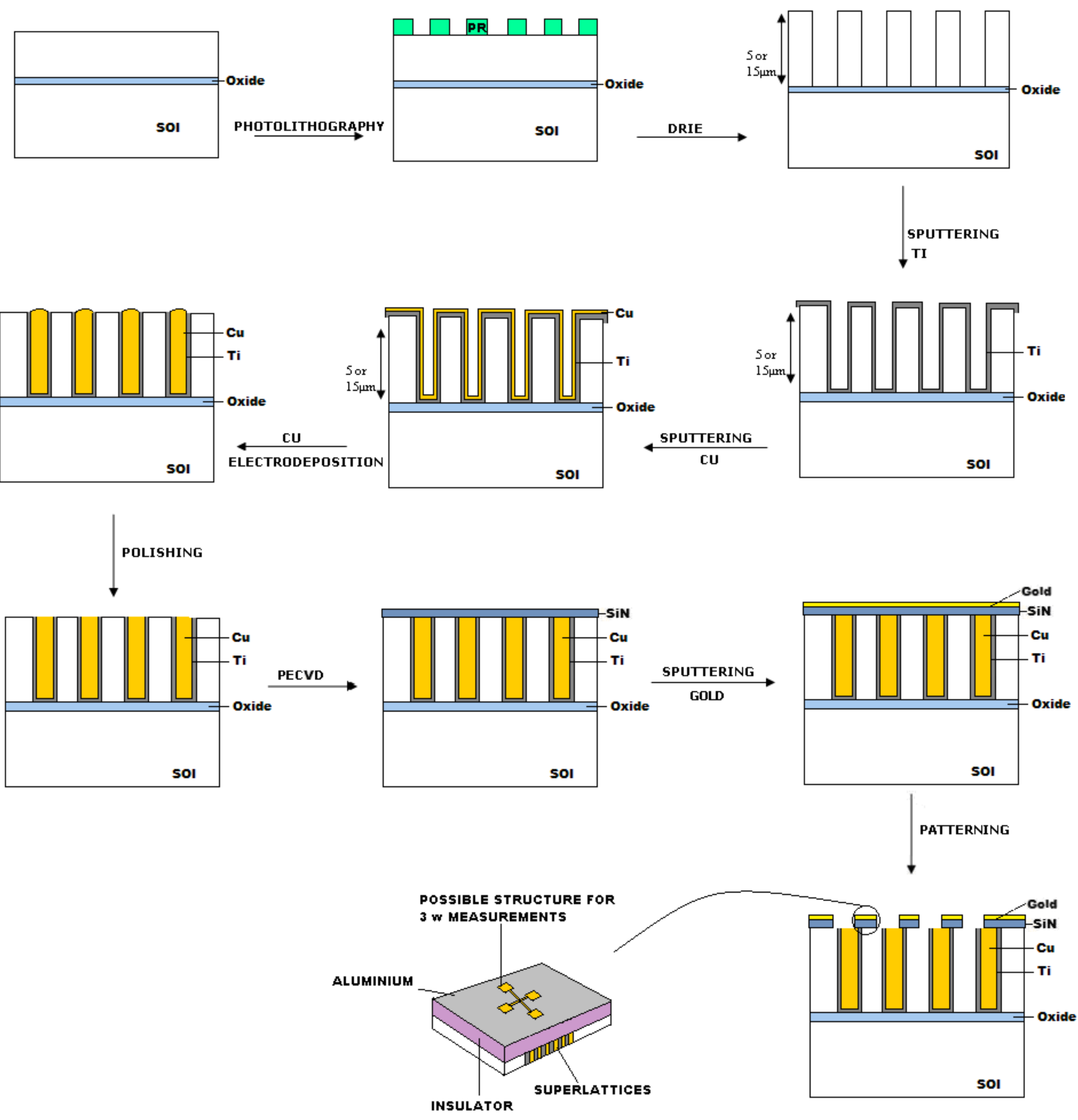
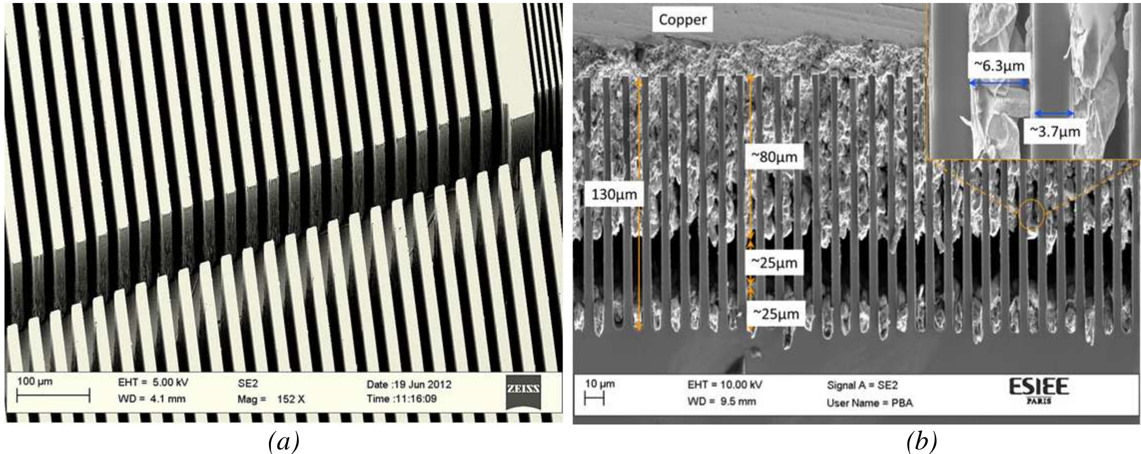


Figure 3.18. Process flow for the fabrication of microscale superlattices in Silicon.



(a) *(b)*

Figure 3.19. SEM images of (a) microsuperlattices post 100 µm-DRIE etch and (b) cross section of microsuperlattices post Cu electrodeposition on sputtered Ti adhesion layer.

However, the main issue in the electroplating step arose from having non-uniform features on the same wafer. Since there were both 5 µm and 15 µm trenches, both of ~100 µm depth, the difference in volume to be filled was 3-fold and hence resulted in the 5 µm trenches filling much faster than their 15 µm counterparts. However as it was impossible to 'stop' the plating at the regions already filled, the entire wafer continued to plate overall and resulted in a significant deposit of copper on top of the wafer (~6-12 µm) by the time all the trenches were filled. The conformal nature of the copper deposited on the entire wafer and the bright sheen presented in colour of the copper is due to the additives added to the electroplating bath. We currently use Transene's Copper electroplating acid which is a mixture of H_2O, H_2SO_4, $Cu_2(SO_4)_3$, HCl and other organic additives).

All the excess copper on the top of the trenches due to the presence of levellers in the copper additives presents a problem to the polishing step in the fabrication process. Figure 3.21 (a) and (b) present SEM images of the excess copper deposited after a full electrodeposition session of ~6 hours. The depth that needs to be polished was measured as ~10 µm. The polishing of the wafer was outsourced to Wafer Solutions Incorporated (WSI), France.

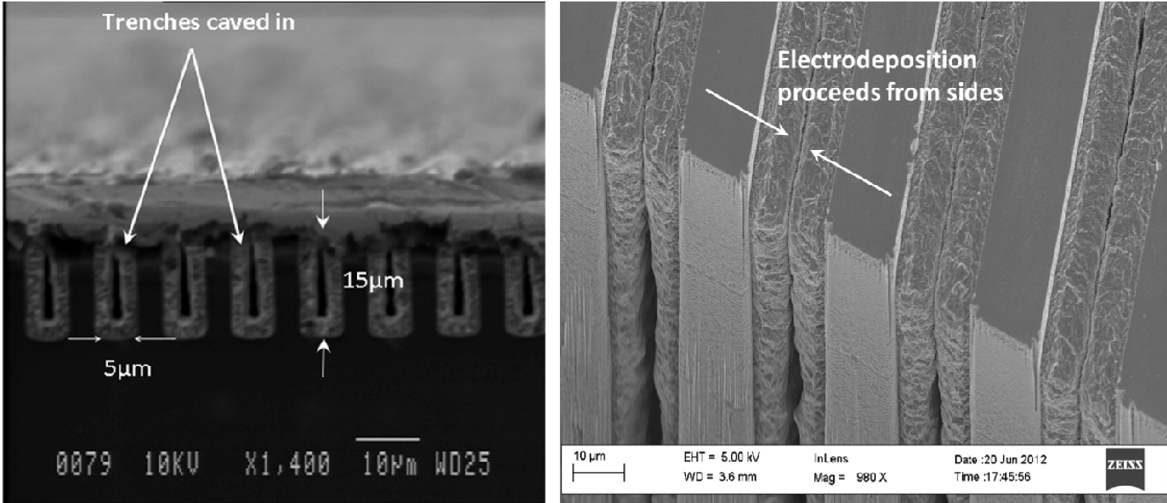
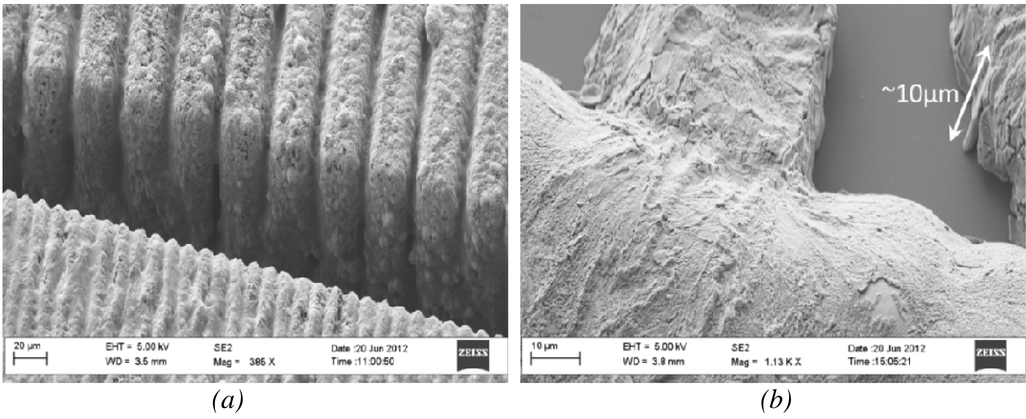


Figure 3.20.(a) 'Dog-ear syndrome' when plating with higher current resulting in caved trenches and (b) properly electroplated trenches showing evidence of plating proceeding sideways and resulting in a central 'crack'.

3.7.2. Copper polishing challenges

Due to the brittle nature of the copper, the CMP (Chemical Mechanical Polisher) had issues in trying to polish away the copper. Hence it was decided to 'etch' away by chemical means most of the copper at ESIEE and leave behind a small excess of silicon which would in theory be easier to polish away. This etching was done using 66% Nitric acid in the cleanroom. The acid was used to literally 'brush' away the excess copper from the top of the trenches to reveal the alternating silicon and copper trenches beneath. After a few runs of acid wash, the trenches were significantly identifiable from before and were then sent to WSI for silicon polishing to completely electrically isolate the trenches.



(a) *(b)*

Figure 3.21. (a) Trenches after 6 hours of electrodeposition and (b) Measure of excess copper on top of the trenches.

Figure 3.22 shows the successive acid washes to result in visually isolating the trenches of the superlattices prior to being sent for silicon polishing instead of copper polishing. Figure 3.23 shows a closer-up view of the superlattices after the acid-brush copper polishing at ESIEE. It can be seen that excess copper has been completely removed from the top of the trenches and leaves behind ~5-7 μm of silicon to be polished for the next step. This are elaborated in the next section.

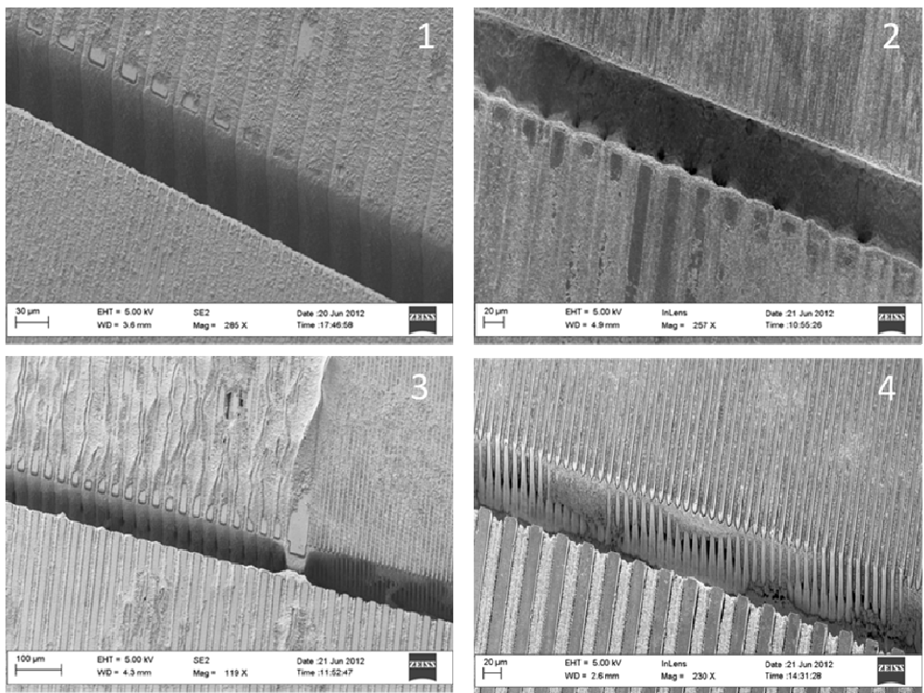
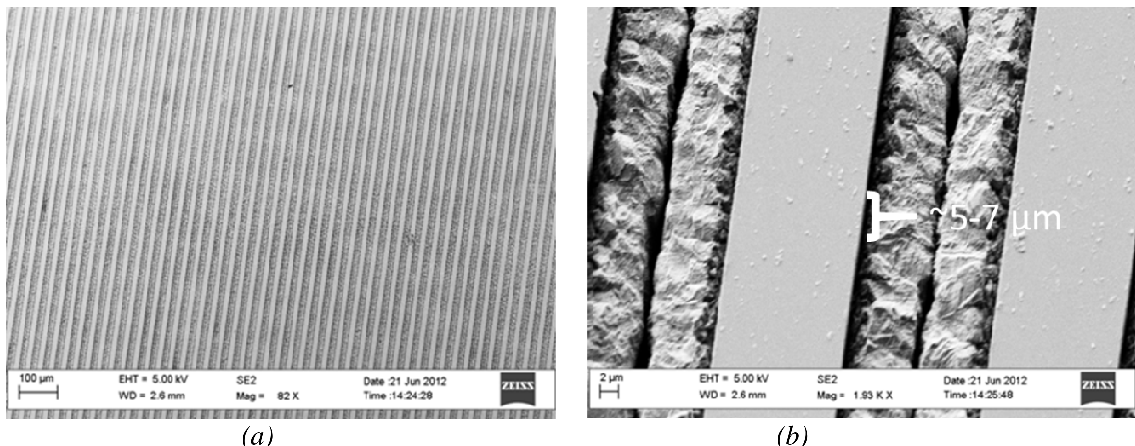


Figure 3.22. Sequence of nitric acid brushes to remove excess copper on top of superlattices.



(a) (b)

Figure 3.23 (a-b). Visually isolated superlattice trenches with ~5-7 μm silicon to be polished.

3.7.3. Silicon polishing challenges

The silicon polishing did turn up better results than the copper polishing ones by the CMP at WSI, France. While part of the trenches were isolated and perfectly aligned, a lot of the trenches were destroyed as well because of the circular polishing motion of the CMP. Also it is understood that the polishing action, pushed away the excess silicon that was being polished to the sides resulting in the formation of a distinct 'step' which renders the wafer useless for post processing. These results are illustrated in Figure 3.24.

The next section concludes Part I of this thesis. The results obtained and the challenges faced are discussed briefly. Following this, Part II details the different methods we have pursued in the fabrication of HAR nanostructures in silicon towards achieving nanoscale vertical superlattices.

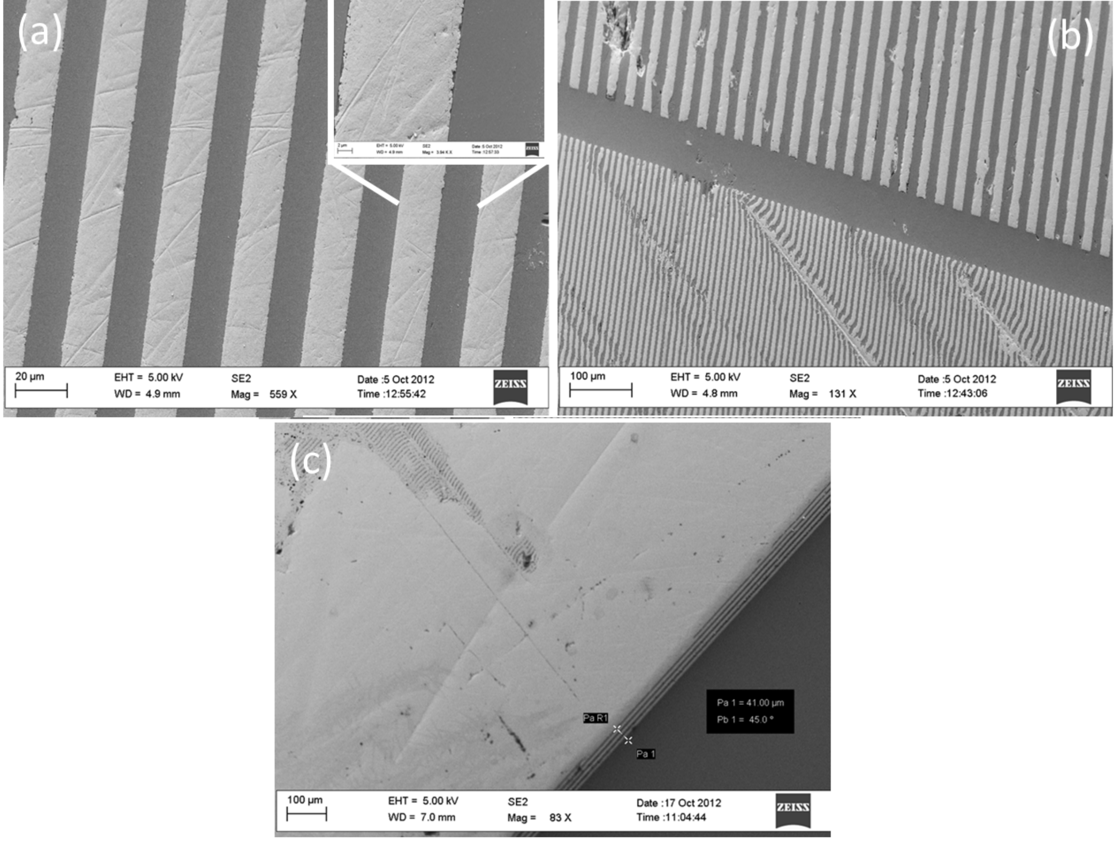


Figure 3.24. (a) Good results – electrically isolated trenches post-Si polishing, (b) broken trenches from polishing action and (c) Ridge formed at the edge of pattern by discarded Si.

Conclusions
End of Part I

As discussed in the previous chapter, a lot of progress was made towards the fabrication and characterization of vertical microsuperlattices in silicon. Process steps were elaborated, masks were designed and fabrication of the microsuperlattices were realized till the challenges listed below thwarted complete realization of the devices to their final goal –

- Polishing challenges – neither copper nor silicon proved easy to remove using CMP rendering the trenches not being electrically isolated which is a most crucial step before any of the other fabrication steps can be realized.
- Wire bonding challenges – Bond lengths and strengths were not uniform across the different pads of the characterization design. This resulted in added difficulty during measurements.

However the characterization setup was completely visualized, designed and realized to make measurements on bulk samples. Initial measurement results obtained by CETHIL-Lyon in the frame of the joint ANR project entitled 'COFISIS', on fabricated bulk silicon samples have been promising and comparable to results available in literature. This setup can be further tweaked to be able to make measurements on nanoscale superlattices which is the ultimate goal of this project. With the knowledge of the challenges and issues realized through the journey of microsuperlattices, at this time it was decided to focus on the fabrication of the nanoscale superlattices themselves using various novel techniques in their realization which involves etching of high density and high aspect ratio (HAR) nanostructures in silicon, as well as filling the resulting trenches and holes with a metallic material. While the latter filling step can be achieved using Atomic Layer Deposition (ALD), the former etching of HAR nanostructures is far from being obvious and is seen as a technological bottleneck, hence the focus on this nanostructuration issue in the next Part II of this thesis. We therefore detail in Part II of this thesis the different methodologies to obtain nanopatterning on silicon. These include different types of techniques, ranging from conventional photolithography-based techniques to different *bottom-up* approaches including the use of electrospinning and diblock copolymer lithography techniques to define nanopatterns on silicon which can then be used as

templates for further DRIE etching to obtain high aspect ratio structures in silicon. These techniques and concepts will form the crux of the second part of this thesis.

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Part II-

High Aspect Ratio (HAR) silicon-based micro- and nano-structures

Chapter 4
Top down approach for achieving HAR Si-based micro- and nanostructures

4.1. Obtaining HAR silicon structures by pattern transfer using Deep Reactive Ion Etching (DRIE)

Deep reactive ion etching (DRIE) is a time-multiplexed, highly anisotropic etch process to create High Aspect Ratio (HAR) structures in silicon substrates. Due to its high anisotropy, DRIE can lead to HAR structures with nearly vertical sidewalls, with controllable angles at 90° +/- 0.1°. The resulting structures can be seen as an extrusion of the masking patterns defined onto the silicon surface prior to etching. This procedure is schematically depicted in Figure 4.1.

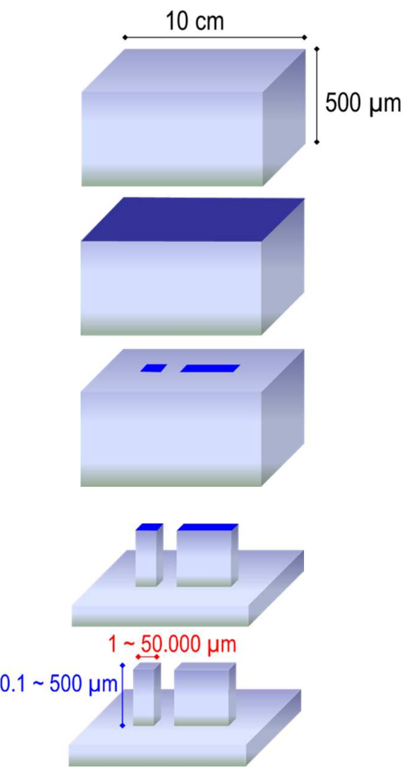


Figure 4.1. Sketch of the typical main steps for achieving vertical HAR silicon structures. Once the mask patterns are achieved on the top substrate surface (in this case using lithography on a thin-film deposited layer) one proceeds to DRIE for extruding those surface patterns into high-aspect ratio (HAR) structures having vertical sidewalls.

Though there might be several variants, the whole process for achieving HAR structures typically involves three main steps: (i) thin film deposition of the mask material, (ii) pattern definition from this thin film and (iii) DRIE etching. There are two main types of DRIE processes – the Bosch process and the cryogenic process. These processes will be briefly described in the following sections. Creation of micro and nanostructures in this manner is generally referred to as the *Top down* approach in microfabrication [1-3].

4.1.1. Bosch DRIE

The so-called 'BOSCH' process was developed at Robert Bosch GmbH, where F. Larmer received patents for developing this process in 1996 [4, 5]. This technology is in use in various dry etching plasma machines from different manufacturers like Alcatel, Adixen etc. [6]. This process has been used to etch structures in various substrates with feature sizes in the sub-micrometer range to several hundreds of microns. Very high etch depths can be obtained through optimizing this process. Typically patterns of SiO_2 and polymeric photoresists or metals such as Al or Cr are used as etch masks during this process.

Figure 4.2 is an illustration of the Bosch etching process. It consists of short bursts or phases of silicon etching, passivation and anisotropic depassivation which are cyclically repeated to achieve an overall anisotropic etch profile. Different gases are used for the different phases of the operation and at the transition between the phases, the gases are switched. For silicon etching, SF_6 plasma is used and for passivation, C_4F_8 plasma is used. For depassivation, either SF_6 or O_2 plasmas are used.

Because of its switching phases, the Bosch process is also known as a "Time Multiplexed Etching Process" or "Gas Chopping Etching Process". The curved ridges formed during each cycle while proceeding to the next is referred to as "scalloping". A lot of detailed studies have been made on different phases of the DRIE etching [7-12]. Figure 4.3 shows SEM images of a typical scalloping evidenced during a Bosch DRIE process by Summanwar [7]. The images show 75 µm diameter circular openings etched to a depth of ~300 µm for an aspect ratio of 4:1. Etching of features in the sub-micron domain have been discussed in detail in Chapter 6.

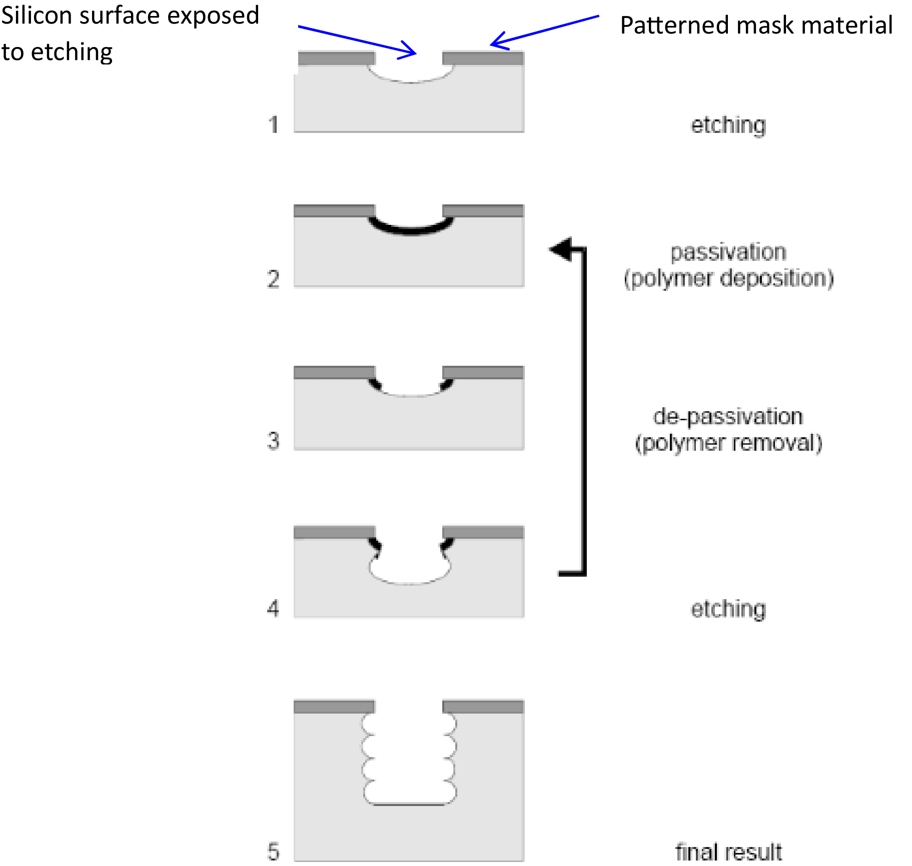


Figure 4.2. Steps in a typical 'Bosch' DRIE process.

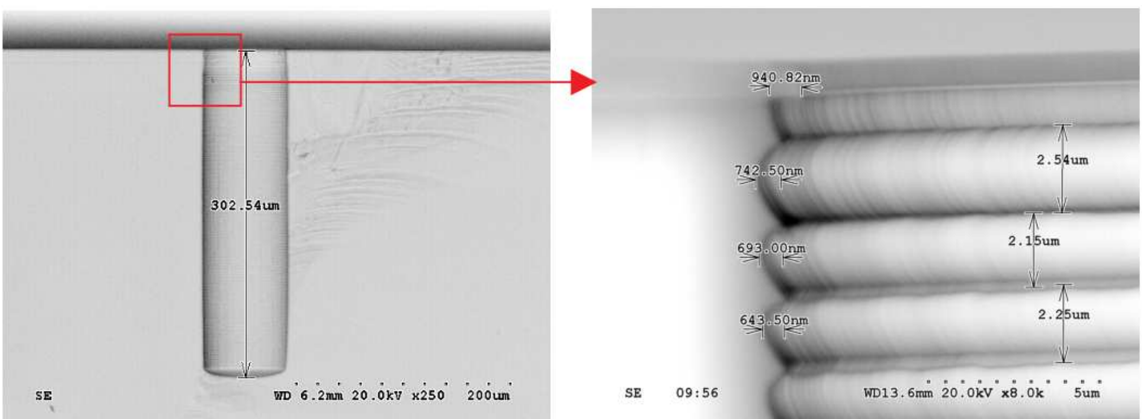


Figure 4.3. Typical Bosch process etching showing scalloping on the side walls on a circular trench of 75 µm etched to a depth of ~300 µm.

4.1.2 Cryogenic DRIE

As the name indicates, cryogenic DRIE is done at very low temperatures, typically -110°C. The reason for this is to slow down the chemical reactions that take place during the etch process and was first used for obtaining highly vertical walls by Tachi, et al [13]. Since that first effort however, a lot of research has been done in this area with results of achieving aspect ratios in the range of 30:1 and higher [14-17], while keeping excellent smoothness of the sidewalls, contrary to the Bosch process which exhibits the scalloping-related roughness.

One of the main concerns in using cryogenic etching is the nature of mask material to be used. It must be borne in mind that the temperatures being extremely low are unsuitable to certain photoresists. Thus metallic masks are usually preferred for this process [18]. The usual masks are Al/Cr. We discuss the use of cryogenic DRIE to achieve HAR microstructures in silicon in greater detail in Chapter 6.

4.2. Lithographically defined patterns as etching mask for HAR structures

Traditional pattern transfer of microstructures onto silicon is usually accomplished through photolithography [19-21] and subsequent etching. Photolithography is the process of obtaining (sub) micron scale geometrical shapes on the surface of a silicon wafer for further processing, such as etching of the underlying thin film material. Then, the lithography-defined thin film patterns can act locally as a protection layer (etching mask) for further etching of the bulk substrate. Conventionally there are two types of photosensitive resins (photoresists), positive and negative, which are used to produce the patterns onto the wafer, with both of them resulting in images opposite to one another. While there are numerous ways of achieving photolithography, we focus here on those methods based on parallel printing of the patterns (which excludes those based on scanning) and especially, the most common method, based on the use of a physical translucent mask embedding the desired opaque patterns, as illustrated in Figure 4.4. Photolithography has been in use for decades as the technology of choice to define patterns for further etching. This technique has been intensively exploited in getting superimposed sets of patterns of different thin film materials, leading eventually to transistors for instance or to other planar semiconductor components and circuits. In this section however, we focus on the use of a single set of lithography-defined thin film patterns thus imprinted on the wafer surface as templates for producing very high aspect ratio micro and nanostructures using Deep Reactive Ion Etching (DRIE).

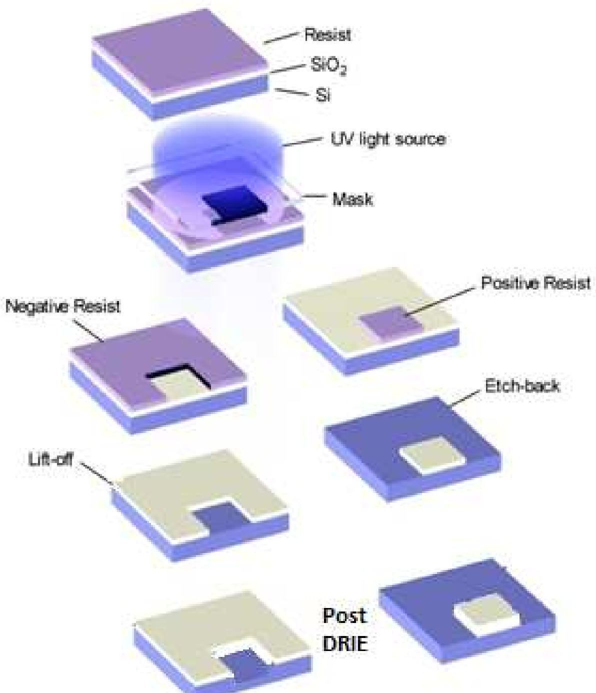


Figure 4.4. Illustration of the use of positive and negative photoresists to obtain contrasting thin film patterns on the wafer using the same mask. When needed, the thin film pattern can be used to produce etching of the underlying bulk of the substrate material.

The working principle of photolithography involves actual optical printing of features with improvement in lenses and imaging techniques accompanied by a decrease in wavelength of the imaging light source. In fact, the 'demise' of optical lithography has been predicted for years together [22]. Figure 4.5 shows the lithography wavelength trends with reduction in IC feature size [22]. The resolution of a lithography system is usually expressed in terms of its wavelength and numerical aperture (NA) as:

$$\text{Resolution} = k_1 \frac{\lambda}{NA} \tag{4.1}$$

Where k_1, the constant is dependent on the process being used. In IC manufacturing, typical values ranges from 0.5 to 0.8. It follows that higher the number, less stringent a process. The NA of optical lithography tools typically ranges from 0.5 to 0.6 in modern machines. Thus, the typical rule of thumb is that the smallest features that can be printed are about equal to the wave-length of the light used.

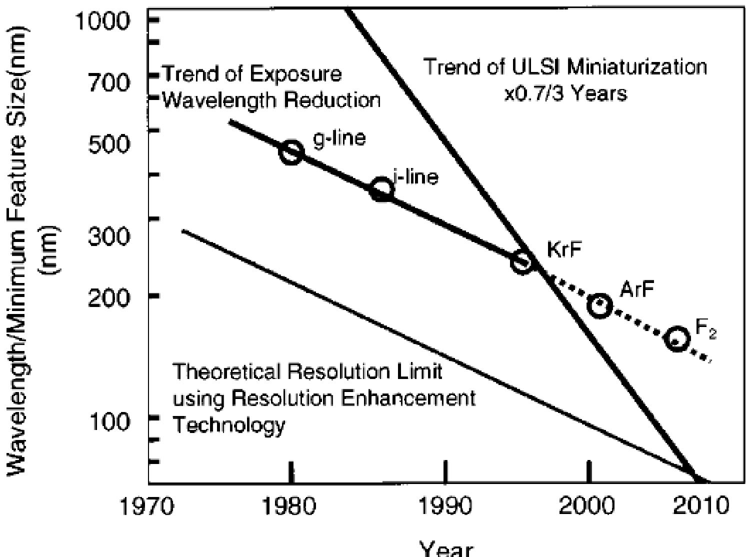


Figure 4.5. Comparison of photolithography wavelength trends with reduction in IC size.

Currently, leading-edge production lithography employs optical projection printing operating at the conventional Rayleigh diffraction limit [23]. Therefore, with reduction in wavelength, the pattern transfer of reducing dimensions cannot be accurately reproduced by optical lithography in the near future. Furthermore this trends towards reduction of feature size goes with a drastic increase of the fabrication costs, Thus, the research for novel and low-cost techniques in alternate lithography for sub-micron features has been in progress for over two decades now.

4.3. Non-conventional techniques for achieving micro- and nanopatterns

The techniques discussed in this section describe the possibility of achieving high aspect ratio micro and nanostructures by alternative techniques to those based on conventional lithography. These alternative techniques includes not only the so-called soft-lithography techniques but also the so-called *bottom-up* approaches such as self-assembly [24, 33] and hence involve *growth* of pillars or other patterns as opposed to the bottom-up techniques, which consists of etching away a material or modifying its topography to create patterns. The use of bottom-up techniques to produce HAR nanostructures will be discussed later in the next chapters. Under the top-down categorization, there are various techniques including soft lithography [24-26] nanoembossing [27, 28], nanomolding [29, 30], micro-electro-discharge machining (µ-EDM) [31, 32]. Of these techniques, soft lithography is the one with a lot of

interest generated because of its inexpensive methodology and excellent results. The next section describes soft lithography techniques in brief.

4.3.1 Soft lithography techniques

The term "soft lithography" was coined by Dr. George. M. Whitesides of Harvard University in 1998 as an umbrella term to refer to all those techniques of photolithography which use a "soft" mold usually made of elastomeric material to create patterns on substrates by *physical* contact [24-26]. Though stamp printing and lithography have been around for centuries, the two were first bought together in 1993 by Whitesides et al., when they discovered a technique called 'Microcontact Printing' [34]. Soft Lithography uses physical contact as the basis for pattern transfer to the substrate. Hence, a Poly Di Methyl Siloxane (PDMS) "mold" is fabricated and employed for this purpose. However these "molds" are used to make futher numerous copies using different kinds of replication techniques. The "master" is usually a silicon substrate with replicable patterns. The mold is usually prepared by replica molding [35] as shown in Figure 4.6. The "master" is typically fabricated from Silicon or otherwise using one of the conventional techniques: **(1)** E-beam lithography **(2)** Focused ion beam lithography **(3)** Photolithography **(4)** Micromachining **(5)** Holography **(6)** Scanning Probe Microscope (SPM) Lithography.

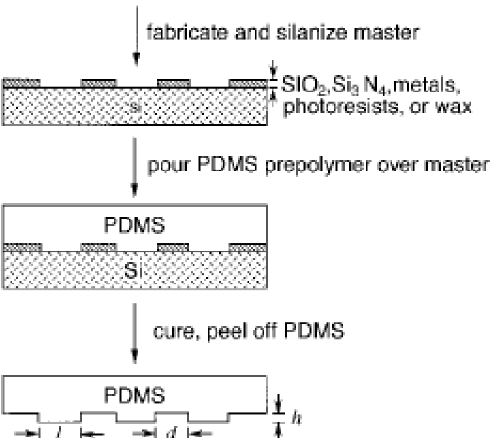


Figure 4.6. Replica molding process to create PDMS "molds" from a "master" silicon substrate.

Once the mold is ready, it can be used to cast a very large number of substrates very fast and cost-effectively. The mold regains its shape after being peeled away (See Figure 4.7) and so can be reused up to 100 times without noticeable deterioration [36].

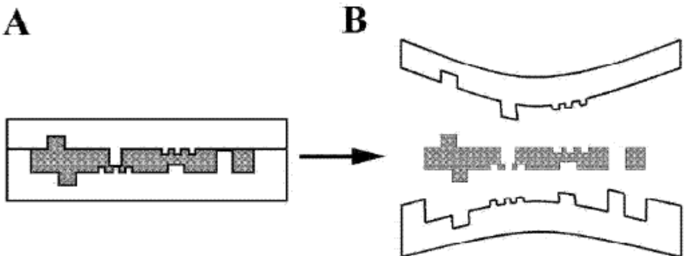


Figure 4.7. Schematic illustration of making replicas from a PDMS mold. The white surfaces show PDMS molds which imprint the grey (soft) substrate in between. Once cured, the two PDMS molds can then be peeled away leaving a patterned substrate behind.

PDMS plays a primary role in the success of Soft Lithography and is chosen for its following properties:

- PDMS being an elastomer, it conforms to the surface of the substrate over a relatively large area. It is deformable enough such that conformal contact can even be achieved on surfaces that are non-planar on the micrometer scale. The elastic characteristic of PDMS also allows it to be released easily, even from complex and fragile structures.
- PDMS provides a surface that is low in interfacial free energy and is chemically inert:
- PDMS is homogeneous, isotropic, and optically transparent down to about 300 nm: UV cross-linking of pre-polymers that are being molded is possible. It has been used to construct elastomeric optical devices for adaptive optics and to fabricate photomasks for use in UV photolithography and contact phase-shift photolithography.
- PDMS is a durable elastomer. The same “stamp” can be used up to about 100 times over a period of several months without noticeable degradation in performance.
- The surface properties of PDMS can be readily modified by treatment with plasma.

4.3.2. Non-lithography-based patterning techniques

Other non-optical lithography-based techniques to achieve micro and nano-patterning employ the use of self-assembled monolayers (SAMs), using diblock copolymer chemistry, nanofibers spun by electrospinning, *etc*. which form the *bottom-up* approach to micro and nanofabrication. These techniques will be explained in detail in Chapters 7 and 8 of this thesis.

4.4. Conclusions

With the scope of optical lithography already being maxed out by the decreasing feature sizes as required by the current IC trends, it seems that standardization of a new lithographic techniques to achieve critical dimensions in the nanometer range over large surface areas is the need of the hour. Many new promising replacement lithography methods have been probed over the past few years with varying degrees of success and spanning many different technologies. Some of these have been outlined the previous section in addition to giving the limitations of the current lithographic methods. They will be used to produce HAR sub-micron structures based on lithographically-defined patterns, as described in the next chapter.

In the next chapters of this thesis, we also detail the use of other methodologies to obtain feature sizes in the nanometer ranges *without the use of optical lithography*. Chapter 7 is a detailed explanation of the use of electrospinning to achieve nanofibers on Silicon and Chapter 8 deals with block copolymer lithography. These chapters give process recipes, experimental details and results from these forays.

Additionally in Part III of this thesis, as a perspective, we explore the potential of other methods to achieve nanometer critical dimensions of feature sizes through new promising *bottom up* methods. While the list of these methods or their implementation is by no means exhaustive, they provide an interesting insight into the future of the microfabrication industry to achieve diminishing feature sizes over large areas and at low cost for next generation devices.

Chapter 5
Deep Reactive Ion Etching (DRIE) On Lithography-defined sub-micron features

5.1. Introduction

Deep reactive ion etching (DRIE) as a method to achieve high aspect ratio features was discussed briefly in the previous chapter. One of the main contributions in this chapter is to try and characterize the ability of a given etch process to produce HAR structures, and thus to assist the user in the selection of the most appropriate process. Usually, one of two forms of the DRIE process are used in HAR etching –the "Bosch" process on one hand, which is based on alternating cycles of depassivation, etch and repassivation sub-steps [7, 8], and the cryogenic process on the other hand, which involves etching at temperatures, typically below -100°C [16]. Both have enjoyed grand success at etching micrometer and sub-micrometer features to great depths.

Using the Bosch process, very high aspect ratio trenches have been reported in literature. Trenches with aspect ratios of up to 107:1 were reported for 374 nm widths by Marty, et al [15]. More recently, aspect ratios of 97:1 have been reported by Owen et al [37] for trenches of 3 µm widths. Other results have been published for trenches ranging from 130 nm to 2.3 µm, where aspect ratios between 30:1 and 60:1 [38, 39] were achieved. When considering cryogenic etching results, aspect ratios of 48:1 have been reported by Tillocher et al [40] using the so-called "STiGer" cryo etching process, which is somehow similar to the multiplexed Bosch process, with close plasma chemistry, but with the specific feature of processing at a cryogenic temperature. It can be seen as a combination of the original "multiplexed" Bosch process and the "pure" cryogenic etching process.

In this chapter, we describe optimized Bosch processes to fabricate very deep silicon trenches with aspect ratios of 160:1 for trenches of 250 nm width, and of 124:1 for trenches of 800 nm width, respectively.

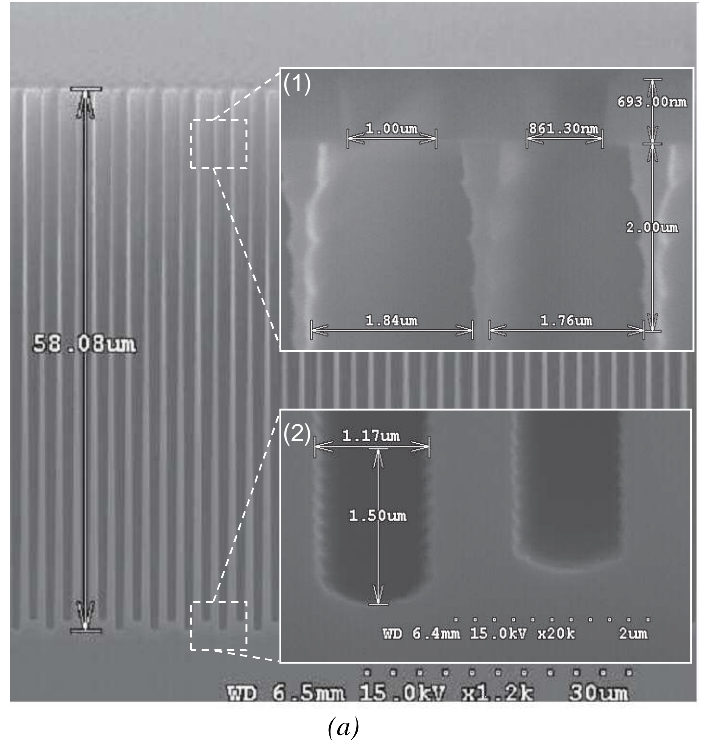
Furthermore, we show preliminary results suggesting that pure cryogenic etch processes can be used to produce aspect ratios greater than 120:1 for 35 nm trenches. To our knowledge, these are the highest values of the aspect ratio attained so far using DRIE in these dimension ranges. By combining our experiments with other reports published in the

literature, we show that the dependence of aspect ratio on feature width obeys a simple two-parameter logarithmic law for a wide range of process parameters and dimensions, including sub-micron features, allowing us to propose a new figure of merit to characterize the ultimate aspect ratio that can be obtained using a specific etch process. This figure of merit also allows achieving comparison of different aspect ratio performances, while taking into account in the same time, the dimension of the trench for which this performance is attained.

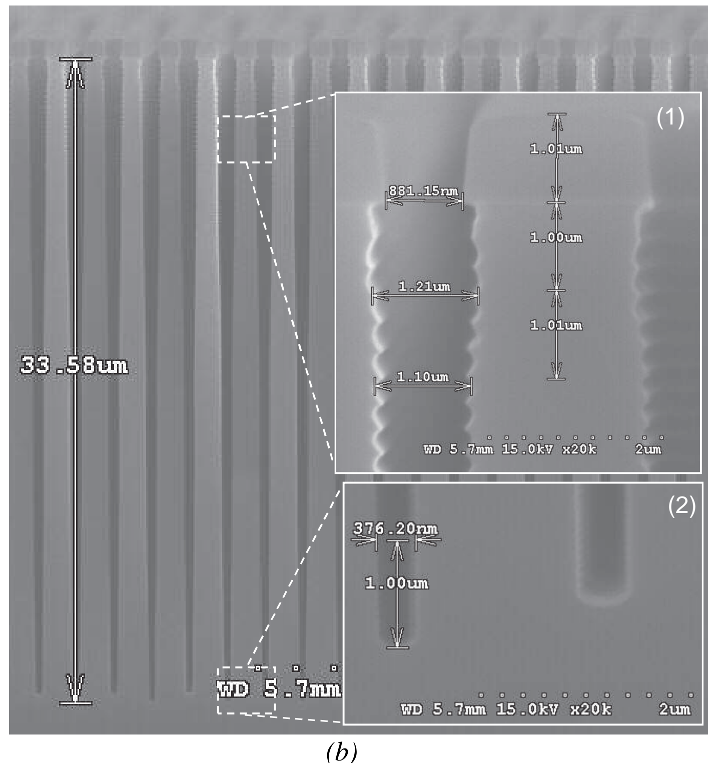
5.2. Results from Bosch DRIE process

The basic Bosch process is a time-multiplexed plasma etch process typically involving three distinct steps that alternate - depassivation, etch and repassivation. Some steps maybe performed concurrently [41-43]. To overcome the problem of excess bowing at the top of the trenches (See Figure 5.1(a)) and of narrowing at the bottom (see Figure 5.1(b)) [10], numerous etch trials accompanied by a detailed study of the relationship between the three etch steps were performed. The best etch profile was obtained using a two-step process in which the depassivation and the etching were combined in one step. Since silicon etching takes place in this case at a lower pressure than in the regular Bosch process, this leads in a decrease of both etch rate and selectivity [10, 44].

Two sets of experiments were performed with the optimized Bosch process. An Aluminum layer of 500 nm thickness was evaporated as a masking layer for the extremely high selectivity it offers during the DRIE process (>300:1). Set 1 constitutes simple trench test structures of 800 nm width, whereas Set 2 consists of trenches increasing in width from 250 nm to 5 µm, with spacing of ~250 nm between them. Set 1 experiments were performed as a part of the work by A Summanwar [10]. It must be noted that both sets were fabricated on Alcatel DRIE Systems, using standard <100> p-doped silicon (from Ultrasil – resistivity 0.01-0.015 Ω-cm). The detailed etch programs used for the two experiments are shown in Table 5.1, and the obtained results are represented in Figure 5.2. Using the Set 1 etching conditions in Table 1, 800 nm-wide trenches with extremely vertical profiles and no bowing were manufactured, reaching aspect ratios as high as 124:1 (Figure 5.2).



(a)



(b)

Figure 5.1. (a)Etch results with standard, non-optimized process, showing excessive bowing on top – inset (1) and available space at the bottom – inset (2) and (b) Etch results with increased passivation reduced bowing on top – inset (1) and narrowed trenches at the bottom – inset (2).

Table 5.1. Parameters for deep etching of sub-micron features using Bosch process.

(a) General parameters

	Source Power (W)	Pressure (mT)	Temperature (°C)	Duration (s)	Etch rate(µm/min)
Set 1	2800	25-50	10	6610	0.90
Set 2	1800	30	20	3600	0.66

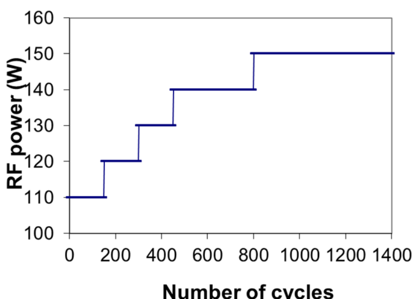
(b) Specific parameters for the passivation pulse

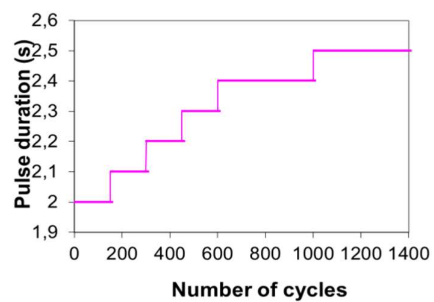
	C_4F_8 flow (sccm)	RF power (W)	Pulse duration (s)
Set 1	350	30	2,4
Set 2	200	100	2

(c) Specific parameters for the etching and depassivation pulse

	SF_6 flow (sccm)	RF power (W)	Pulse duration (s)
Set 1	300	see figure below	see figure below
Set 2	300	100	5

(d) Detailed ramped parameters used in set 2 for RF power and pulse duration





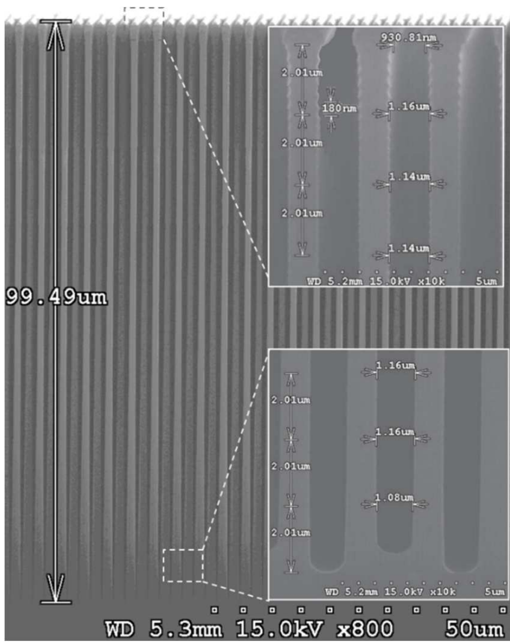


Figure 5.2. Extremely high aspect ratio (124:1) trenches having a width of 800 nm and a depth of 99.4 µm obtained using Set 1 parameters

When considering the etched depth (D) alone, a well-known trend is a decrease of the etched depth (D) while the feature size (W) decreases, as illustrated in Figure 5.3(a). This is related to different diffusion-related phenomena [42, 45-47], which includes the loading effects and the aspect-ratio dependent etching (ARDE). However, when considering the aspect ratio (D/W), a very interesting opposed trend is obtained: a decrease in feature size (W) can lead to higher aspect ratios (D/W). Those two trends are schematically depicted in Figure 5.3 (b) and (c).

The above-mentioned trend suggest that it might be interesting to experimentally explore the sub-micrometer range in terms of feature sizes, where the highest aspect ratio are expected. It is also naturally tempting to also explore what really happens with nanometer-scale features.

Achieving an aspect ratio of 124:1 on trenches as wide as 800 nm-wide trenches is therefore a challenge, because it is still in the upper region of the sub-micrometer range. Obtaining such performance required dynamic adjustments of both the duration of the steps and of the plasma power for Set 1.

It is also to be noted that the DRIE process is self-limiting due to the decrease in etch rate from radical depletion described by the Knudsen transport model [48], ion depletion due to sidewall scattering, electrostatic deflection and angular distribution [49]. Yeom, et al. [50] also describe a *critical aspect ratio*, corresponding to the ultimate aspect ratio that can be achieved by a process upon saturation and it turns to be no longer dependent on the etch duration. It is therefore reasonable to assume that any recipe of DRIE process has a maximum achievable aspect ratio.

Using the Set 2 etch conditions in Table I, the highest aspect ratio was obtained for the 250 nm-wide trenches. The etch extended 40 μm in depth, resulting in an extremely high aspect ratio, of 160:1. The post-etch dicing of the samples for the purpose of SEM observation resulted in collapsed walls, as apparent in Figure 5.4. However the effectiveness of etch is apparent from the regular square profile at the bottom of the trenches, which also suggests that even higher aspect ratios might be possible by further etching, as the saturation is not yet reached in this case.

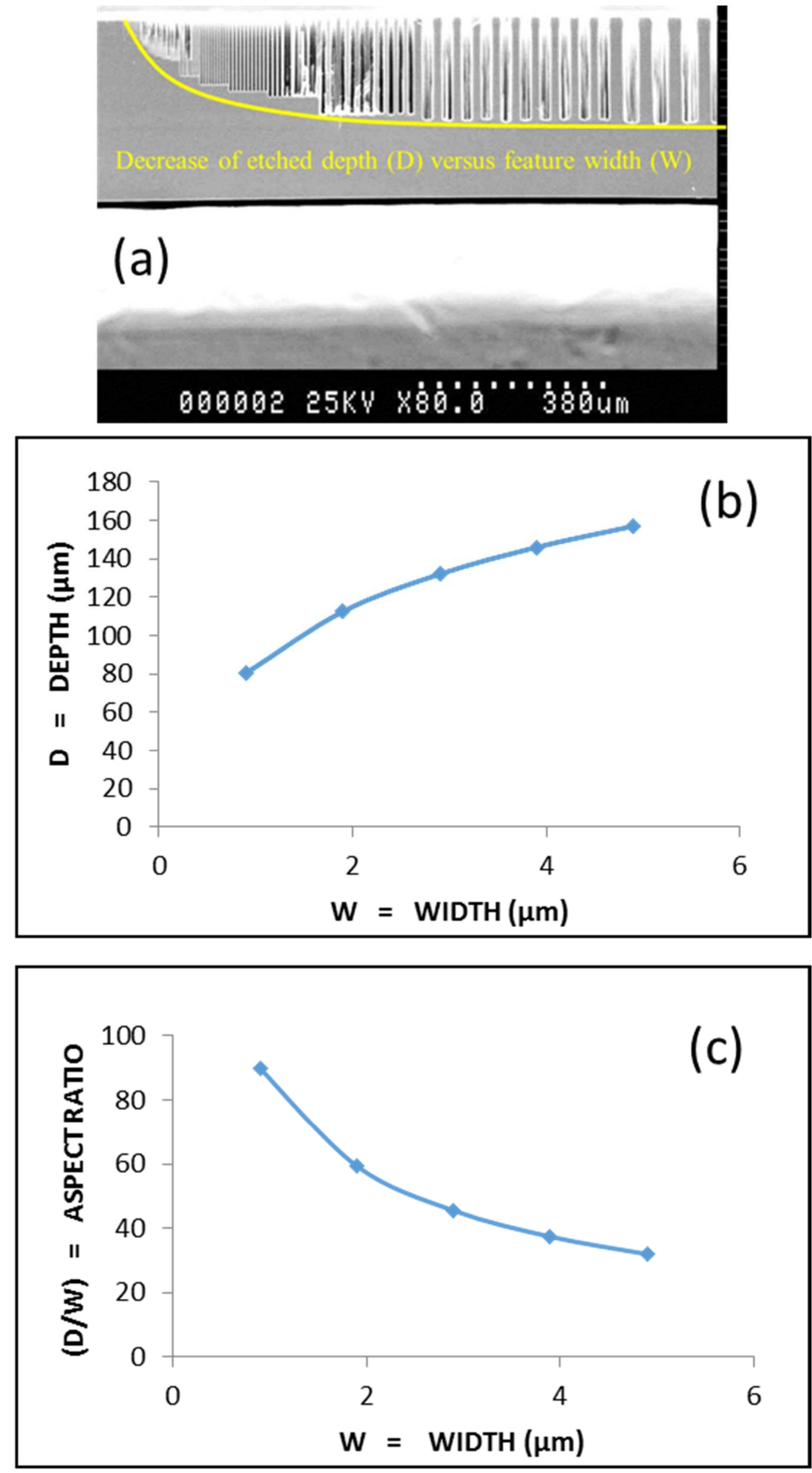


Figure 5.3 (a) Scanning Electron Microscope (SEM) image illustrating the typical trend of etched depth (D) versus feature size (W); (b) and (c) are the corresponding graphical trends for both the etched depth (D) and the aspect ratio (D/W), respectively, which have opposite variations.

Bosch process DRIE is also known to result in scalloping in the form of quasi-periodic sidewall roughness. Typical Bosch process surface roughnesses are in excess of 200 nm. However, when considering small trenches (in the range below 5 μm) and certainly like those used in our Set 1 & 2 experiments, this roughness drastically reduces to levels below 25 nm and eventually vanishes with increasing aspect ratios during the process, as detailed in a previous report [51] related to the so called "Aspect Ratio Depedent Scalloping Attenuation", which indicates that surface roughness induced by the cyclic nature of the Bosch process, is significantly attenuated when increasing the aspect ratio of deep trenches, which is especially true for the sub-micron trenches under consideration in the present work, whose aspect ratio is extremely high, leading to non-observable surface roughness.

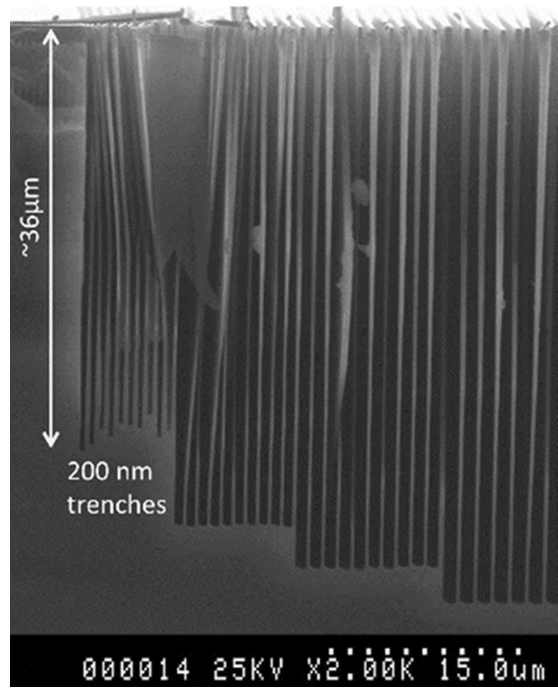


Figure 5.4. 250 nm-wide trenches with a depth of 40 μm (aspect ratio 160:1) obtained through the process in Set 2. Some of the walls collapsed during the dicing procedure.

5.3. Results from cryogenic DRIE

By comparison with the Bosch process, which is known to produce a periodic sidewall roughness of typically tens of nanometers peak-to-valley, cryogenic DRIE offers the benefit of producing vertical sidewalls with no observable roughness, even on large features. This advantage of the cryogenic process is of great significance. This is a consequence of the process being carried out at low temperatures using a plasma of combined sulphur

hexafluoride (SF_6) and oxygen (O_2), and results in efficient reduction of the isotropic etching of silicon.

The challenge in case of cryogenic etches is to use a suitable mask that will resist at such temperatures and that can be patterned at sub-micrometer length scales. Typical photoresist masks peel off without being able to withstand cryogenic temperatures and were therefore considered unsuitable. For the final set of experiments performed in this work (Set 3), we used a combination of focused ion beam (FIB) etching and cryogenic DRIE to achieve HAR trenches with widths in the tens of nanometers range. The FIB was used to pattern lines of 35 ± 10 nm width and 500 nm spacing on a 50 nm-thick aluminum film. All the details regarding the FIB patterning for this sample is discussed in detail in Chapter 8. This created a hard mask for the subsequent etching, which used the process parameters shown in Table 5.2. All etching experiments were performed on an Alcatel 601E machine which is equipped with a cryogenic chuck. Samples were mounted on top of sacrificial test wafers deposited with aluminum using high vacuum grease. Figure 5.5 shows the corresponding result in the form of an SEM picture, indicating that aspect ratios of more than 125:1 could be achieved. We also note that the FIB was used again, before the imaging, to etch a vertical rectangular hole that exposes a partial cross-sectional view of the etching.

When compared to the Bosch process described in the previous section, it can be noted that it is performed at almost twice the bias at which the cryogenic process is performed. This can be explained by the fact that the Al mask thickness for the Bosch process is of the order of 500 nm as compared to only 70 nm for the cryogenic process. In the latter, we lower the ion bombardment to avoid any damage (or sputtering) to the Al layer while maintaining enough energy to penetrate to the bottom of the trench. As for why this difference in terms of ion bombardment between Bosch and cryogenic process is needed, it is perhaps possible to link it to the passivation layer itself and the fact that we compare a process with a dedicated passivation step (Bosch process) to a continuous gas flow process (cryogenic process). With the Bosch process, the "teflon-like" passivation layer must be etched from the bottom of the trench to continue etching. However with the cryogenic process we only grow the passivation layer (thin silicon-fluorinated oxide) on the sidewalls as continuous ion bombardment induces no passivation at the bottom of the trench. So we don’t have the need to have very high ion bombardment in this case.

Table 5.2. Process parameters for the cryogenic etch process (Set 3).

Source Power (W)	SF6 flow (sccm)	O2 flow (sccm)	Pressure (mT)	Substrate bias (W)	Temp (°C)	Etch time (min)	Etch rate (μm/m)
1000	200	12	30	80	-110	10	0.45

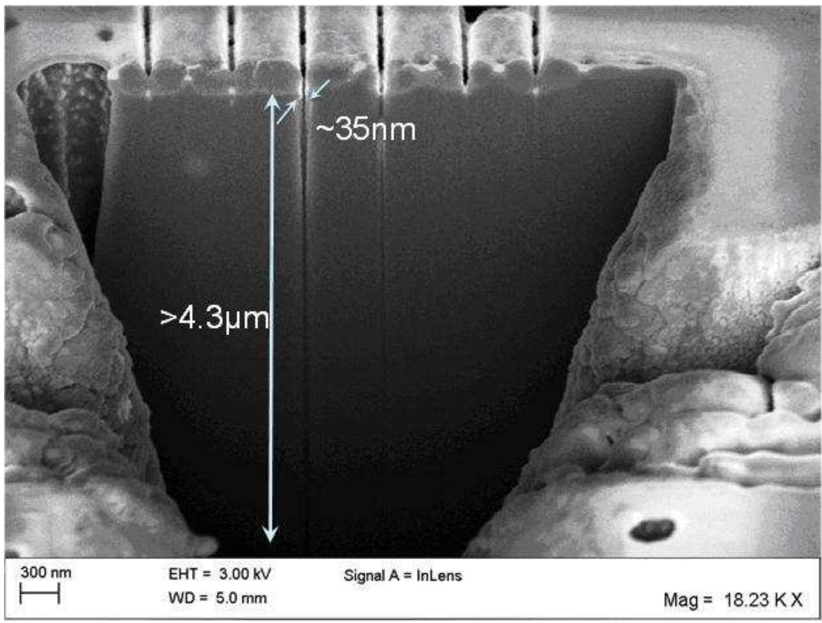


Figure 5.5. SEM image of ~35 nm trench etched to a depth greater than 4.3 μm using Set 3 parameters, hence with aspect ratio >125:1. A rectangular hole was etched using the FIB to allow cross-sectional visualization.

5.4. Aspect ratio *vs.* Feature Size

Figure 5.6 shows a comparison of the aspect ratio versus feature size as studied by various groups [37-39; 52-55] and updated here with our latest results. It appears that data pertaining to a particular etch process can follow a semi-empirical logarithmic law, which was previously reported for feature size in the tens of micrometer range [56] and which is found to still apply for the sub-micrometer range, considered in this paper:

$$AR = \frac{a\, log(\,1+b\,W)}{W} \tag{5.1}$$

where *AR* is the aspect ratio, *W* is width of the features (in µm), and *a* and *b* are constants with units of µm and µm^{-1} respectively, that depend on the etching recipe being used. The aspect ratio is calculated as *D/W*, where *D* is the etch depth at the bottom of the trench. The best fit

with this model was evaluated in five different cases and represented in Figure 5.5. As it appears from the figure, the law applies over a wide dimension range. It can therefore be assumed that such trend lines can be used to reasonably predict the aspect ratios in ranges where experimental results are not available. In particular, by extrapolating the results to the limit of vanishing width W, the *ultimate* aspect ratio corresponding to a particular etching recipe can be evaluated:

$$\lim_{W \to 0} \frac{a \log(1 + b W)}{W} = ab \equiv AR_{max} \tag{5.2}$$

This ultimate aspect ratio can be calculated by performing experiments such as the Set 2 presented above, and can provide a dimension-less figure of merit (FOM= AR_{max}) for the effectiveness of a specific process to produce HAR sub-micrometer structures. For the cases analyzed in Figure 2 we obtain the following FOM values: 3780 for our Set 2 process from Table I, 3240, 180, 3000, and 168, respectively, for data previously reported in [37], [38], [54] and [55]. We can see that the FOM for [38] and [55] is significantly lower than the other processes, thus implying that these processes were not pushed until saturation to achieve the corresponding maximum aspect ratio features. A regression analysis was performed to assess the accuracy of the curve fits. The values of the regression coefficient r^2 attained for the above cases were above 0.96, with percentage errors for the a and b fit parameters calculated in the range of 7-9 %, leading to an overall error on AR_{max} in the order of 15-20%. It must be noted that extending such trend-line extrapolation to dimensions above the micrometer range is not recommended, since most processes were optimized for the sub-micrometer range, and when applied to larger dimensions may result in dramatic undesired results such as the formation of silicon "grass".

5.5. Conclusions

Etching of sub-micrometer scale trenches was proven to give access to aspect ratios up to 124:1 and even 160:1, depending on the process parameters using both Bosch and cryogenic DRIE. A semi-empirical logarithmic law relating aspect ratio to decreasing dimensions, and which takes into account the decrease in etch rate induced by radical and ion depletion, was experimentally validated at these sub-micrometer scales. Furthermore, a figure of merit to evaluate the ultimate aspect ratio was proposed in the case of processes intended to achieve HAR features. The proposed figure of merit was also applied to available experimental data from the literature and compared to our achievements.

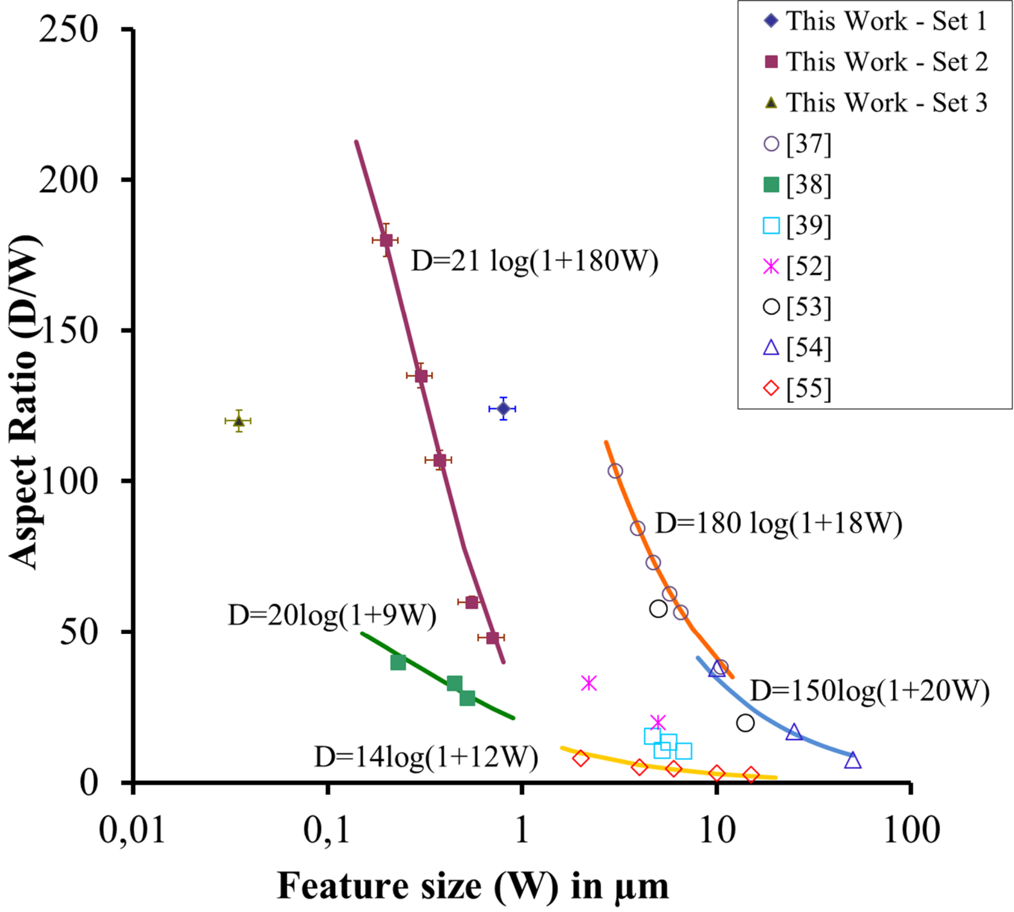


Figure 5.6. Aspect ratio versus feature size as studied by various groups in the micrometer range plotted on a logarithmic scale.

The next chapter discusses the methods and results obtained from the use of nanofibers deposited on a silicon substrate and used as templates for subsequent etching.

Chapter 6
Electrospinning for advanced transfer of HAR micro- and nanostructures

6.1. Introduction

Electrospinning is a centuries-old technique that has been used to draw out fibers from liquid solutions using electric potential [57-60]. Traditionally, it has been used in cell-culture and neurological applications [61-63] as well as in microphotonics and optofluidic devices [64-67].

However, in this chapter, we discuss the use of electrospinning for producing high aspect ratio micro-and nanostructures. Electrospinning is deployed as a technique to manufacture nanofibers on silicon, which are then used as a template for further DRIE etching, to yield high aspect ratio micro and nanostructures as a precedent to manufacturing nanoscale vertical superlattices. The next section elaborates on the basic physics of the electrospinning process and subsequent sections detail the specific process variations used to obtain the nanofibers on silicon and the DRIE processes carried out to achieve HAR structures from them.

6.2. Electrospinning to achieve nanofibers

Electrospinning is a process which uses an electrical charge to draw very fine (typically on the micro or nano scale) fibers from a liquid solution. The process does not require the use of coagulation chemistry neither the use of high temperatures to produce solid threads from a given (usually polymer) solution [68-71]. This makes the process particularly suited to the production of fibers using large and complex molecules. Figure 6.1. shows an illustration of a typical electrospinning process [72].

During the electrospinning process, a polymer solution is injected at a constant flow rate from the nozzle of a syringe which forms a Taylor cone (as illustrated above) when the syringe is positively biased and the collector is negatively biased [73]. Typically, the collector is an electrically conductive material such as an aluminium plate, a coated silicon wafer, etc. Another parameter affecting the process is the distance between the electrodes. It is usually

between 10 and 25 cm. The typical applied voltage of the setup is in the range of 0.5-30 kV, depending on the type of polymer solution being injected.

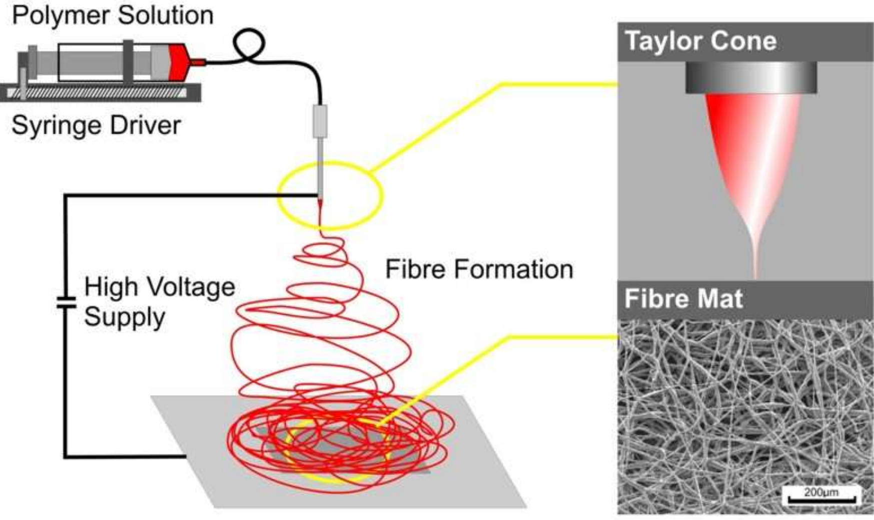


Figure 6.1. Schematic of the electrospinning process

When the electrical force surmounts the surface tension of the liquid, a jet is formed, and the solvent evaporates rapidly during its propagation to the target and the resultant dry, fibrous materials form the nanofibers on the collector [74, 75]. On the solution side, different properties like viscosity, concentration, molecular weight, etc. affect the quality and the characteristics of the nanofibers produced. It must be noted that the viscosity of the solution should be reasonably high enough to keep the fibrous nature of the deposition rather than forming beads, which is likely to occur when the solution is broken down by the electric field [76]. However, if the viscosity is too high, it will prevent jet formation or result in fibers of very large diameters. Since the viscosity of the solution is related to the concentration of the solution, the molecular weight of the polymer, in a diluted solution, the separation of the polymers results in bead formation. Polymer solutions of high molecular weight but relatively low concentration are ideal for electrospinning [77, 78]. If the molecular weight happens to be too small, no fiber can be produced even if the concentration of the solution is suitably hiked up.

For the ideal solvent, its dissolving ability and boiling point are key parameters. It is essential that the solvent evaporate completely when the fibers reach the collector. Else, they will hold the fibers together at the collector. Therefore, it would seem that a low boiling point

is ideal. It must be noted that a very low boiling point will result in the solvent evaporating too quickly and in the aggregation of the polymer at the nozzle tip resulting in a failed process.

In general, water is used as the solvent for hydrophilic materials such as gelatin. Other solvents include DMF (Dimethyl formalamide), ethanol, $CHCl_3$, and CH_2Cl_2. The resultant nanofibers range in diameter from a few tens of nanometers to a few hundred microns depending on the variation of the different parameters aforementioned [79-81]. In this work, we use Polystyrene (PS) 12.5% polymer and Gelatin 10% as the two materials for obtaining nanofibers. Through the different runs of this work, we have varied the molecular weight of gelatin between 30000 and 90000. Figures 6.2 is an illustration of the subsequent process steps to be performed on these nanofibers to further obtain a 'mask' to get HAR micro and nanostructures using subsequent DRIE on silicon. The lift-off of the nanofibers can be achieved by dissolving them in their respective solvents – DMF for PS and Water for Gelatin nanofibers.

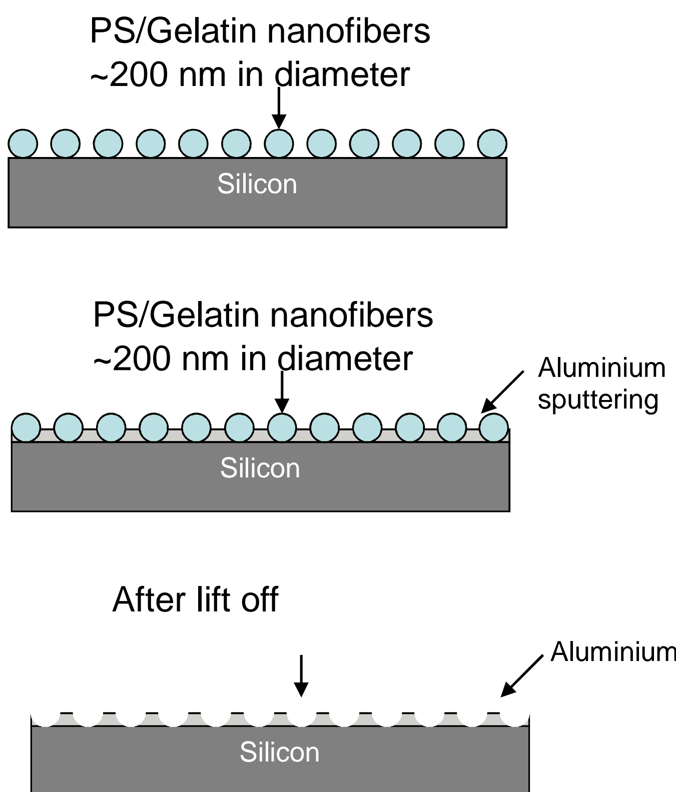


Figure 6.2. Post processing steps of nanofibers to obtain HAR micro and nanostructures in Si.

Alternatively, the polystyrene is an excellent mask by itself. Hence etching can be performed directly after a PS nanofiber deposit on Si. This will yield nano-walls. However when using gelatin, it is necessary to use a masking material like SiO_2 under the nanofibers because gelatin by itself does not form a good masking material. In this case, the underlying SiO_2 can be etched away by RIE. This process is briefly illustrated in Figure 6.3. When using PS fibers, it is also possible to create a 3D scaffolding structure of sorts with alternating trenches and walls of subsequent layers.

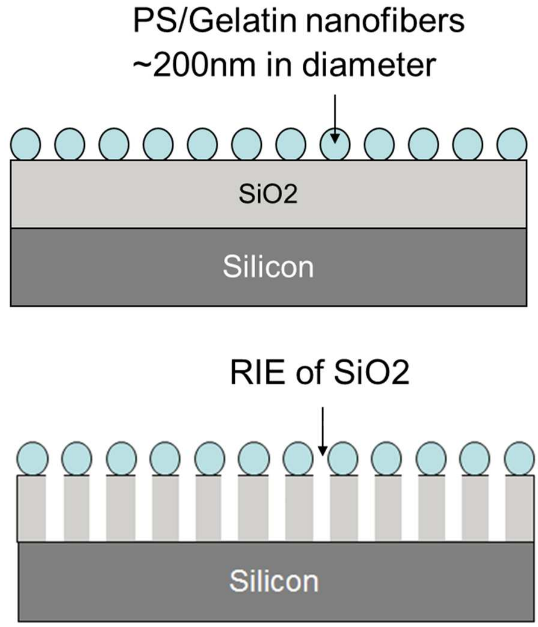


Figure 6.3. Illustration of post processing step to obtain nanofibers on SiO_2 or using PS as mask to produce nanowalls.

6.3. Electrospinning using PS 12.5% and Gelatin 10%

Table 6.1 details the conditions used for electrospinning, the diameters measured via SEM and an indication of if the sample was 'aligned' using parallel strips of conductive aluminium tape. The conditions highlighted in green are the standard conditions for electrospinning these kind of fibers on these kind of substrates at Ecole Normale Supérieure (ENS-Paris), where these experiments were conducted in collaboration with Professor Yong Chen's group. The yellow highlighted portions show the deviations made in our experiment in order to obtain different diameters of nanofibers. Figures 6.4 (a-c) show SEM images of the obtained nanofibers for different samples.

Table 6.1. Process parameters for various experiments of electrospinning to obtain nanofibers.

Sample Number	Nanofiber material	Minimum Diameter (measured)	Substrate	Electrospinning parameters: Applied voltage (kV)	Flow rate (ml/h)	Target distance (cm)	Time (min)	Aligned?
1	Polystyrene 12.5%	~500 nm-1µm	SiO_2	9	0.2	15	2	No
2		~500 nm-1µm						No
3		~500 nm-1µm						No
4		~150 nm		9	0.2	15	2	Yes
5		~280 nm		12	0.2	15	2	No
6		~500 nm						No
7		~200 nm		15	0.2	15	2	No
8		~500 nm						No
9		~200 nm		9	0.5	15	2	No
10		~170 nm						No
11		~300 nm		9	0.1	15	2	No
12		>500 nm						No
13		>500 nm		9	0.2	10	2	No
14		>500 nm						No
15		~250 nm		9	0.2	20	2	No
16		~330 nm						No
17		~220 nm		imprecise 12	0.2	15	2	No
18		~430 nm						No
19		>500 nm		imprecise 15	0.2	15	2	No
20		>500 nm						No
21		>500 nm						No
22	Gelatin 10%	~150 nm	Si	8	0.2	10	2	No
23		~170 nm						No
24		~200 nm		8	0.2	10	2	Yes
25		150 - 200 nm		8	0.2	10	0.5	No
26		150 - 200 nm						No
27		150 - 200 nm		8	0.2	10	1	No
28		150 - 200 nm						No
29	Polystyrene 12.5%	>200 nm		9	0.2	15	2	No
30		~180 nm						No
31		~200 nm		9	0.2	15	2	Yes

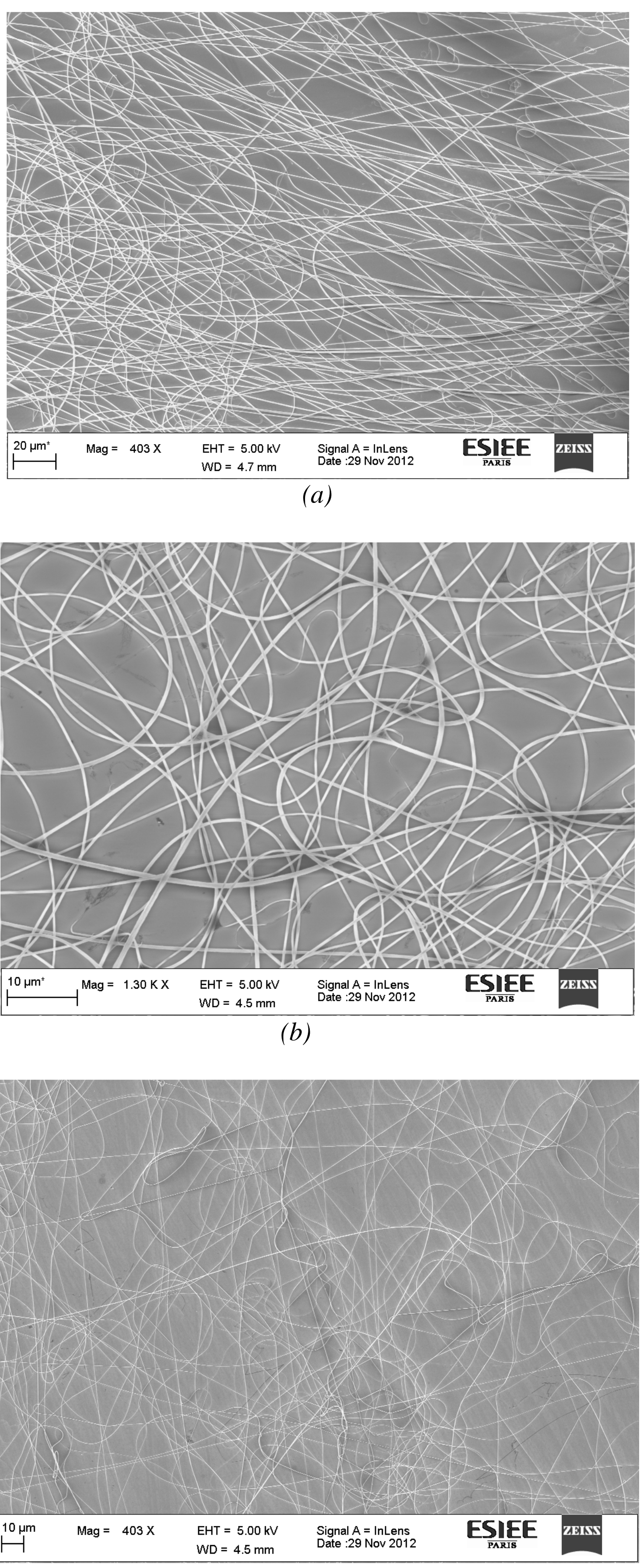


Figure 6.4. SEM images of the nanofibers obtained through electrospinning – (a) Sample 1, (b) Sample 6 and (c) Sample 22.

A study of the diameters of the nanofibers also made it possible to predict the trend of the diameter variation of these nanofibers with variation in electrospinning parameters. The associated trend is presented in Figure 6.5 below.

Subsequently, an Al-deposit step was performed for different samples with thicknesses varying from 50 - 200 nm to test the efficacy of the lift off at the least possible thickness. Through these experiments, it was found that 100 nm of Al was ideal for lift-off purposes providing a fairly workable template to perform DRIE on. However it must be noted that the lift-off was *not* successful in all the samples or across an entire sample. In some samples, prolonged exposure to solvent even under agitation *did not* result in lift-off. However the DRIE experiments were performed on samples with most of the surface that had a successful lift off.

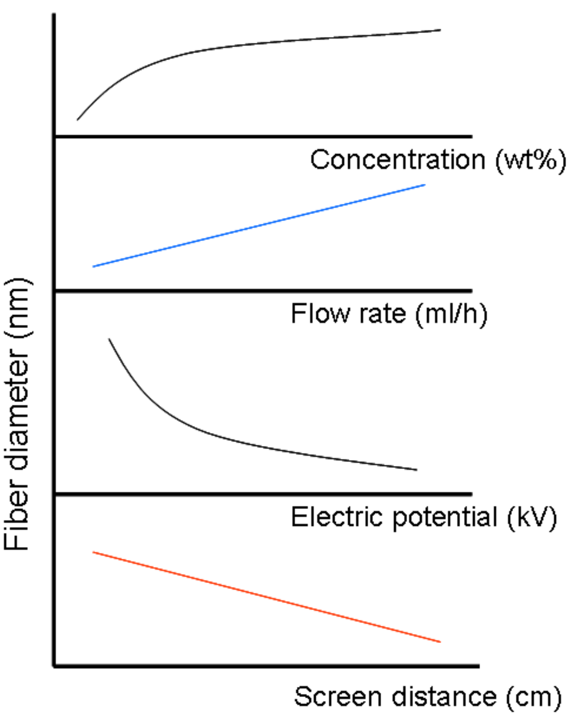
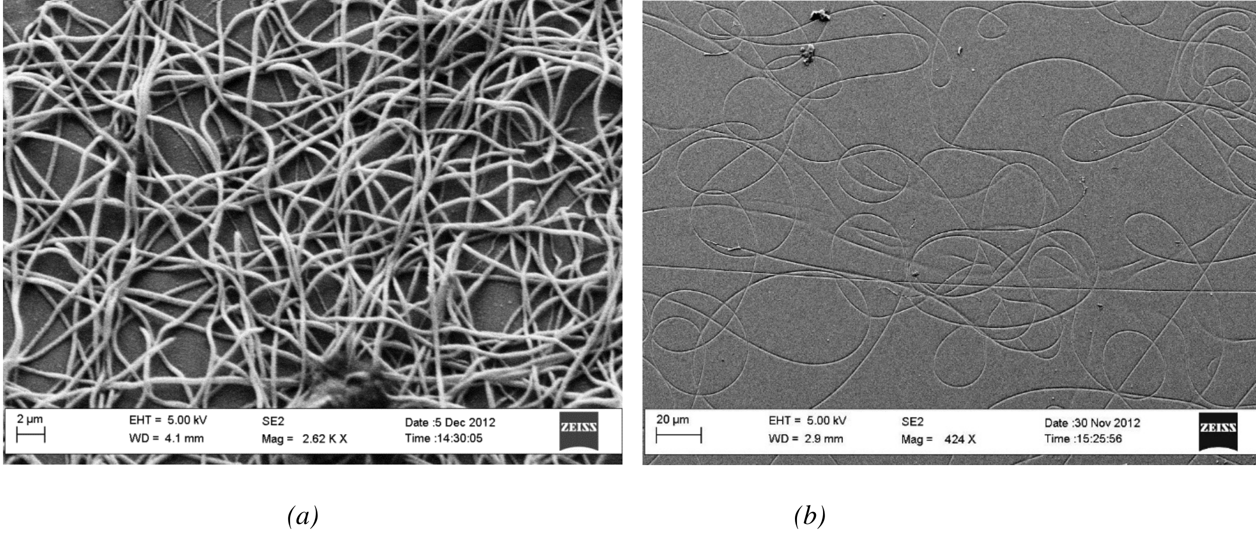


Figure 6.5. Trend of effect of variation of electrospinning parameters on nanofiber diameter.

Figures 6.6 (a) and (b) show the successful lift-off of Gelatin 10% fibers (Sample 22) by soaking in water for about 15 minutes under agitation. Figure 6.7 shows an SEM image of a partially successful lift off where some of the Aluminium still remains stuck on the gelatin nanofibers that failed to lift-off entirely.



(a) *(b)*

Figure 6.6. SEM image of (a) Sample 22 after Al deposition and before lift-off and (b) after lift-off.

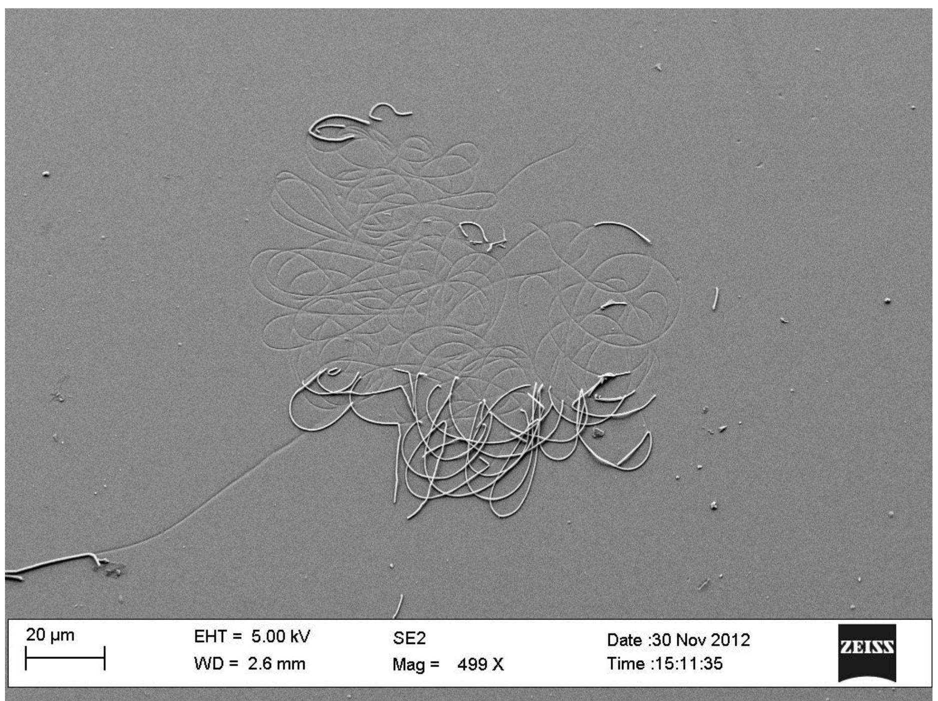


Figure 6.7. Partially successful Gelatin lift-off of Sample 23.

6.4. DRIE on nanofiber templates

6.4.1. Nano-trenches

Initial DRIE parameters were standard and et as shown in Table 6.2 for the first experiments of etching the nanofibers. The first samples to be etched were gelatin 10% standard samples used for etching with the standard Bosch process parameters for a duration of 5 minutes**.**

Table 6.2. Standard Bosch process conditions

Gas	**Pulse**	**Order**	**Power (W)**	**Bias (V)**	**Time (s)**
SF6	300	2	1500	60	5
C4F8	200	1	1500	60	2

The corresponding results were observed under SEM and are shown in Figure 6.8. An etch depth of ~9.1 µm was obtained in the 5 minutes of etching on 261 nm-wide trenches, establishing the efficacy of the recipe used. The inset shows a closer-up view of one of the trenches formed from the DRIE process, which indicates an aspect ratio of 35:1.

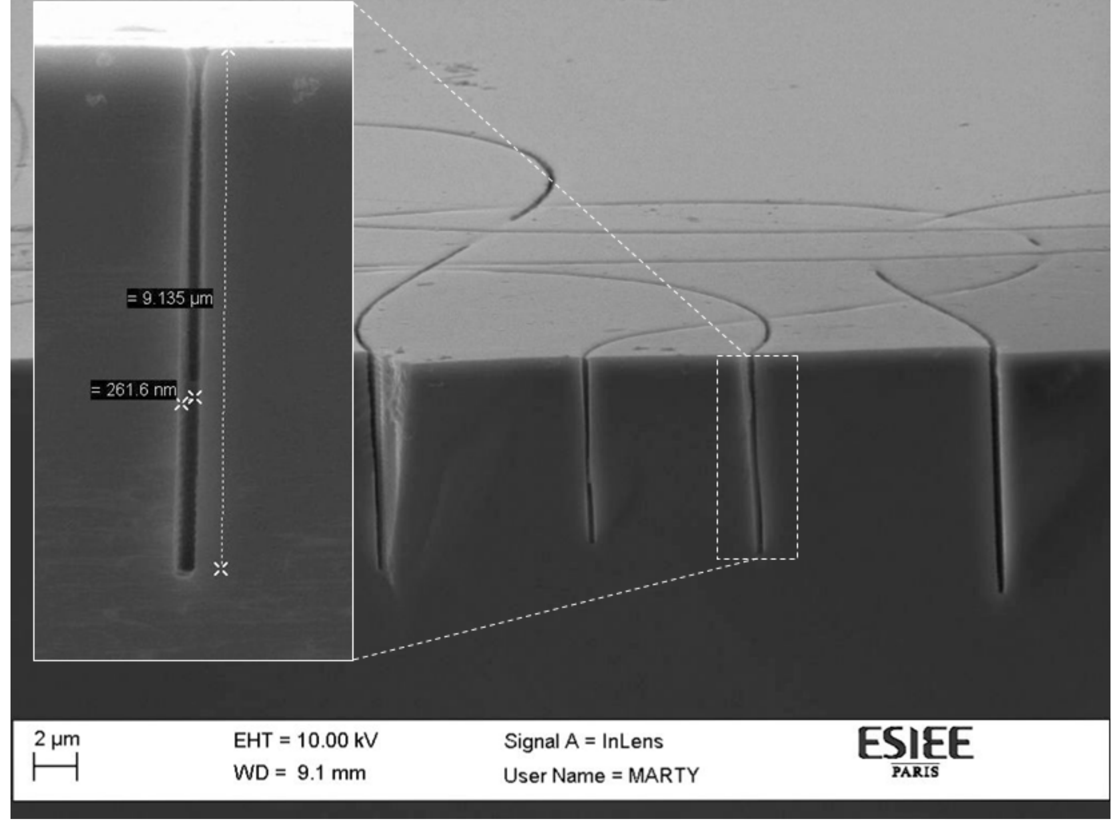


Figure 6.8. SEM image of Gelatin 10% nanofibers etched for 5 minutes using standard Bosch process. The result is a 261 nm-wide, 9.1 µm-deep trench, corresponding to an aspect ratio of 35:1.

With the promising results from the first trial, the Bosch process was continued for 30 minutes duration to observe what was obtained. Etch depths of up to 30 µm were obtained from this trial. The initial nanofiber diameter was measured as ~200nm. However it was observed that a large amount of undercut resulted from the Bosch process. A closer up view of these results are shown in Figure 6.9.

As evidenced in Figure 6.9, splicing the samples does not result in clean edges. This is thought to be due to the curved countenance of the nanofibers, which once etched presents as an angled wall which breaks along the axis of least tension in order to result in the irregularity as is witnessed. The undercut observed is shown in detail in Figure 6.10. The undercut is a side-effect of the typical Bosch process that proceeds by scalloping. This can be clearly witnessed in the etching of the nanofibers that ends up making the opening close to a 1 µm wide one as opposed to the very top which clearly shows that the width of these nanofibers is close to 140 nm. A possible solution to this problem will be to attempt cryogenic DRIE etching of these nanofibers.

6.4.2. Nano-walls

As was detailed in Figure 6.3, the polystyrene fibers were spun on SiO_2. 100 nm of aluminium was then sputtered onto this stack. RIE was used to etch away the SiO_2 to expose the Si beneath. Lastly an Aluminium lift-off was performed by dissolving the PS fibers in DMF resulting in an underlying SiO_2 mask for etching the Si. Similar conditions as shown in Table 6.2 were used to create nano-walls from PS 12.5% fibers on SiO_2. Figures 6.11 (a) and (b) show the PS-based nano-walls created by DRIE.

Further experimentation was not done on these type of samples as the initial goal was to obtain nano-trenches. However the results obtained in the above samples made us recognize that more impressive results of this variety were certainly possible given the need for them. As of now, they certainly make for an interesting perspective and hence similar processing can be used in a variety of other applications including the fabrication of 3D scaffold structures.

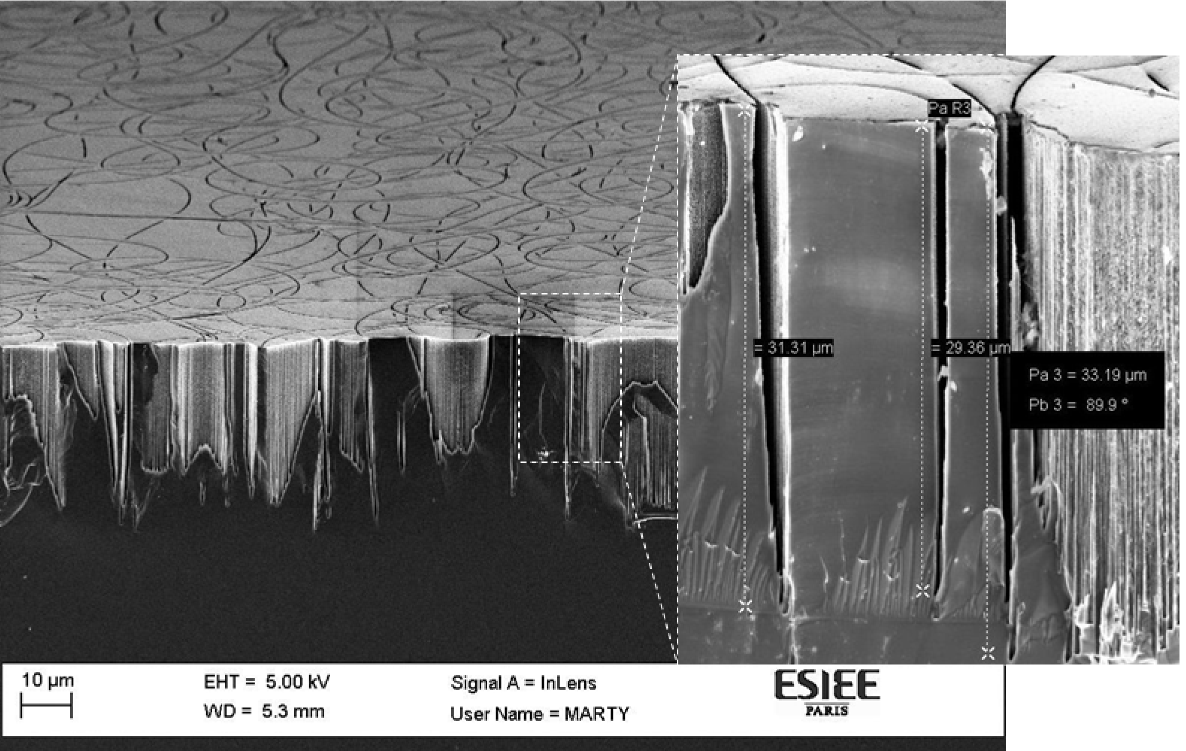


Figure 6.9. SEM image of Gelatin 10% nanofibers post 30 minute standard Bosch DRIE.

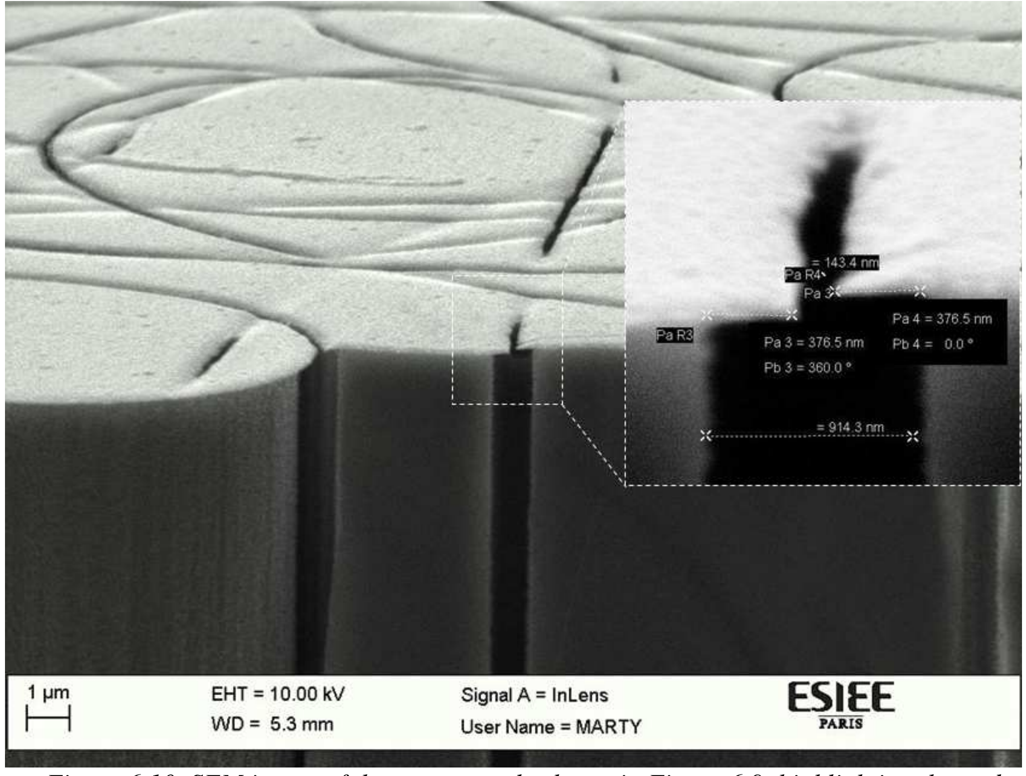
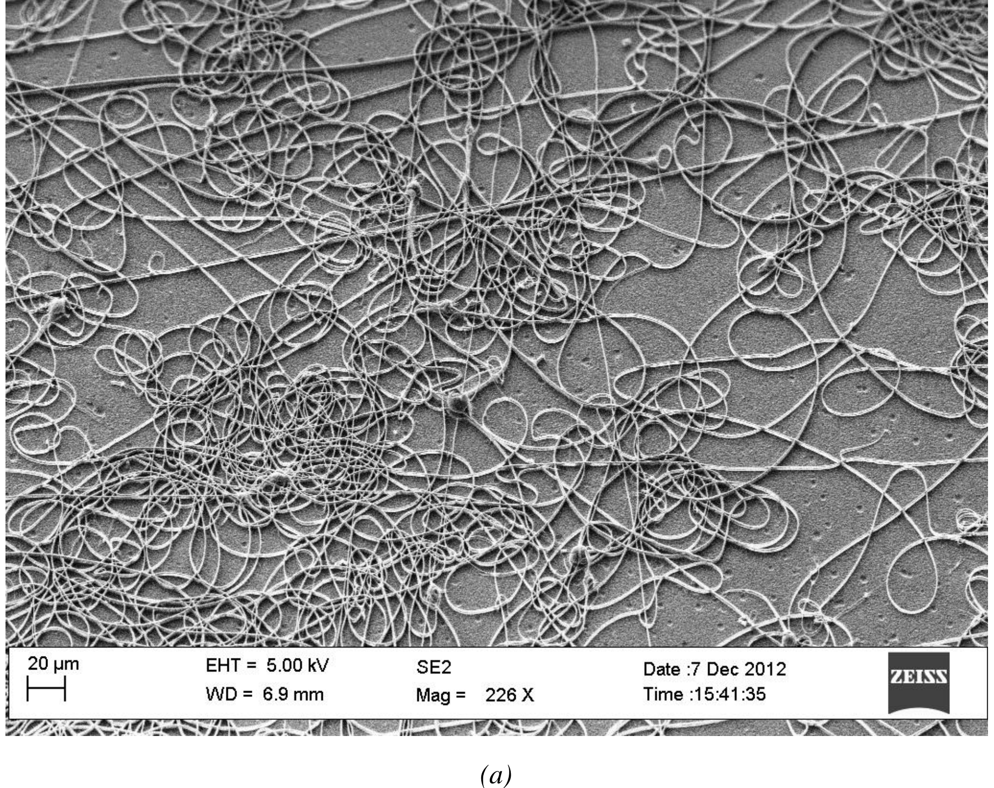
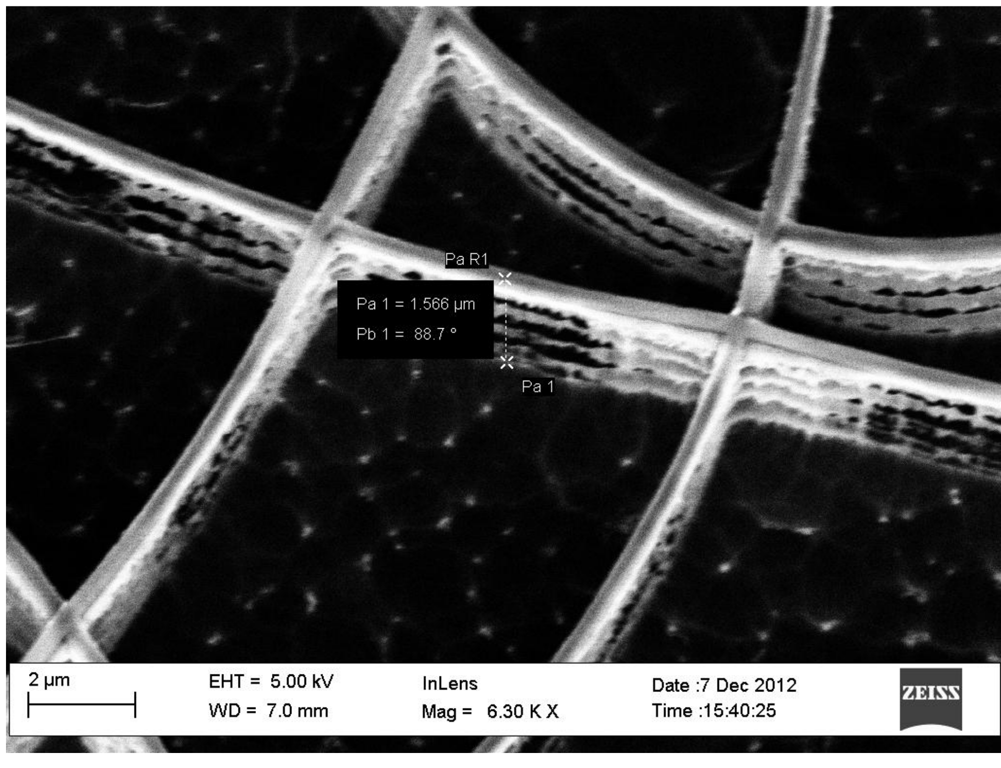


Figure 6.10. SEM image of the same sample shown in Figure 6.9, highlighting the undercut



(a)



(b)

Figure 6.11. (a) Nano-wall formation with PS 12.5% template on SiO_2 and (b) closer-up view.

However, at the end of the Set I experiments, we were equipped with sufficient success for DRIE trials using Al mask based on these nanofibers. Hence the goal with the next set of samples was to reduce as best possible the diameter of these nanofibers during the initial electrospinning step so as to have a finer template mask available for subsequent etching. Also from studying obtained diameters of the nanofibers from process variation we had an idea of changing the parameters in order to result in lesser diameters for future trials. Also, since PS 12.5% nanofibers consistently yielded larger diameters than Gelatin 10% nanofibers, it was decided to use Gelatin as the main nanofiber for Set II experiments.

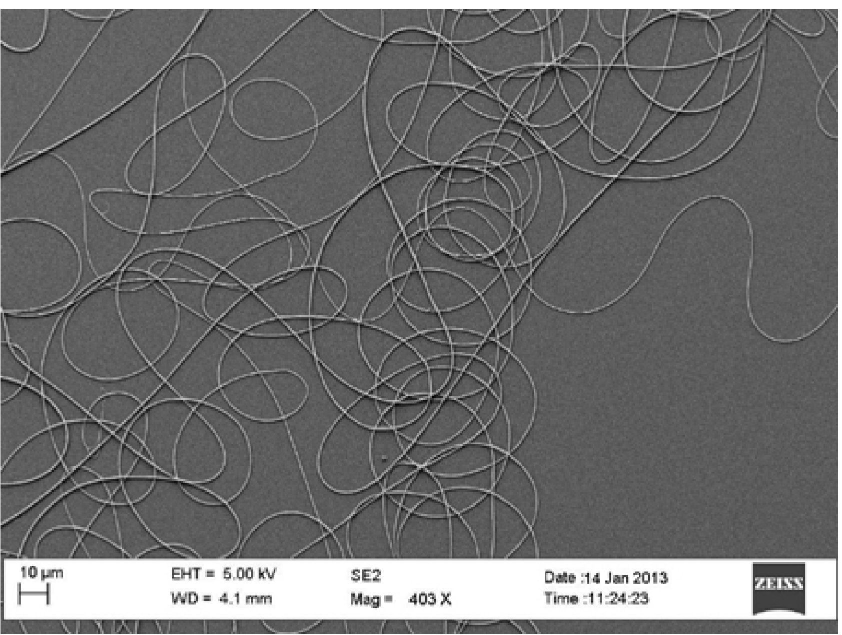
6.4.3. Nanofibers Trial #2

Table 6.3 represents the electrospinning conditions for obtaining the nanofibers for the Set II experiments. The Gelatin used was of lower molecular weight (30000 as opposed to the usual 90000) in order to promote the possibility of obtaining thinner nanofibers.

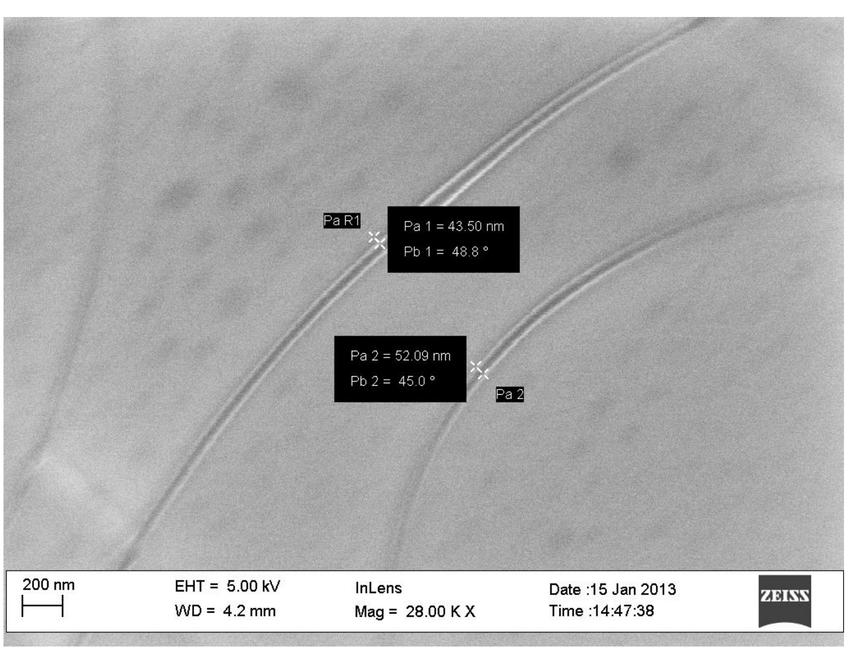
Table 6.3. Electrospinning parameters for Set II experiments.

Applied Voltage (kV)	Flow rate (ml/h)	Distance (cm)	Time (sec)	Min. measured diameter (nm)
8	0.2	10	30	~150
8	0.2	15	30	~100
8	0.2	12	30	~200
12	0.2	10	30	~150
15	0.2	10	30	~60
8	0.1	10	30	~50
8	0.5	10	30	~100

As can be seen from the table above and the corresponding SEM images below, the nanofibers were certainly of a lesser diameter than the previous batch. Also as can be seen from the following SEM image, they were less populated than the earlier trial. The pre and post-Al-lift off SEMs of some nanofibers from Set II experiments are shown in Figure 6.12 (a) and (b) respectively.



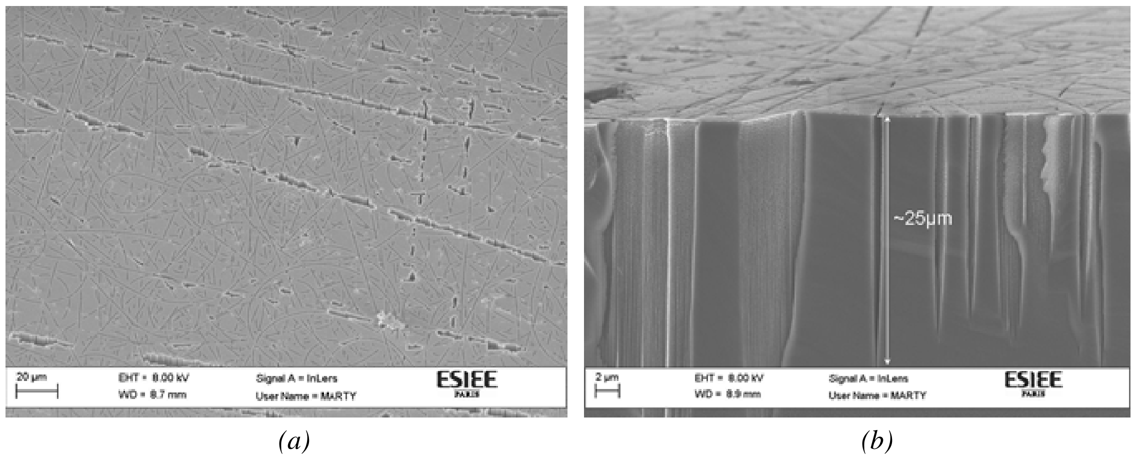
(a)



(b)

Figure 6.12. Set II nanofibers (a) before Al lift-off and (b) post lift-off.

The Aluminium lift off was *not* successful in a large majority of samples obtained in Set II. This can be explained by the fact that there are much fewer fibers on the samples than obtained in Set I due to increasing the screen distance in an attempt to reduce the nanofiber diameter. This meant that clumps of nanofibers could not act together in lifting off the Al deposited over them. Instead in most cases, the deposited Al weighed down the nanofibers and ended up not lifting off at all. However, DRIE was performed on the few successful samples. Once again, the same standard Bosch process conditions were used to perform DRIE and the Figure 6.13 (a) and (b) show SEM images of the top view and cross-section respectively of the sample post-etching. It can be seen that the sample appears to be in significantly worse shape than Set I. The undercut persists as well. Thus altering the electrospinning parameters to obtain 'thinner' nanofibers though successful to a degree has about the same degree of success as Set I in creating HAR structures.



(a) *(b)*

Figure 6.13. SEMs of nanofiber-based trenches post 30 minutes standard Bosch DRIE in (a) top view and (b) cross-sectional view.

6.4.4. Aligned nanofibers

Since the primary goal of using nanofibers as templates for DRIE to produce HAR nanostructures is to eventually use them as a technology for creating nano-superlattices, it is very interesting to the initial goal of this thesis to try and align these nanofibers. Since these nanofibers in fabrication are driven by an electric potential, having a biased collector will allow them to deposit in a more orderly fashion.

To this end, the sample to be electrospun is fixed with conductive aluminium tape a few millimeters apart to coax the nanofibers into depositing in a more aligned fashion. Figure 6.14 is a photograph of such a 'prepared' sample and Figure 6.15 (a) and (b) are SEMs image of quasi-aligned nanofibers. As can be seen from the SEM image, the nanofibers aren't clustered around and seem more orderly. While this is a far cry from perfectly aligned straight fibers, this is a promising first result and variations of the conductive collector can lead to more useful results. Ideally, with the preparation of a dedicated mask with electrodes of aluminium or a similar metal spaced a few 100 µm apart can yield excellent results of perfectly aligned nanofibers between electrodes. These can then be post-processed similar to the nanofibers as discussed above to lead to vertical nano-trenches in silicon as a step towards achieving nano-superlattices.

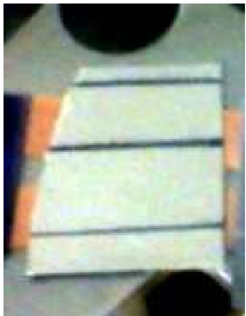
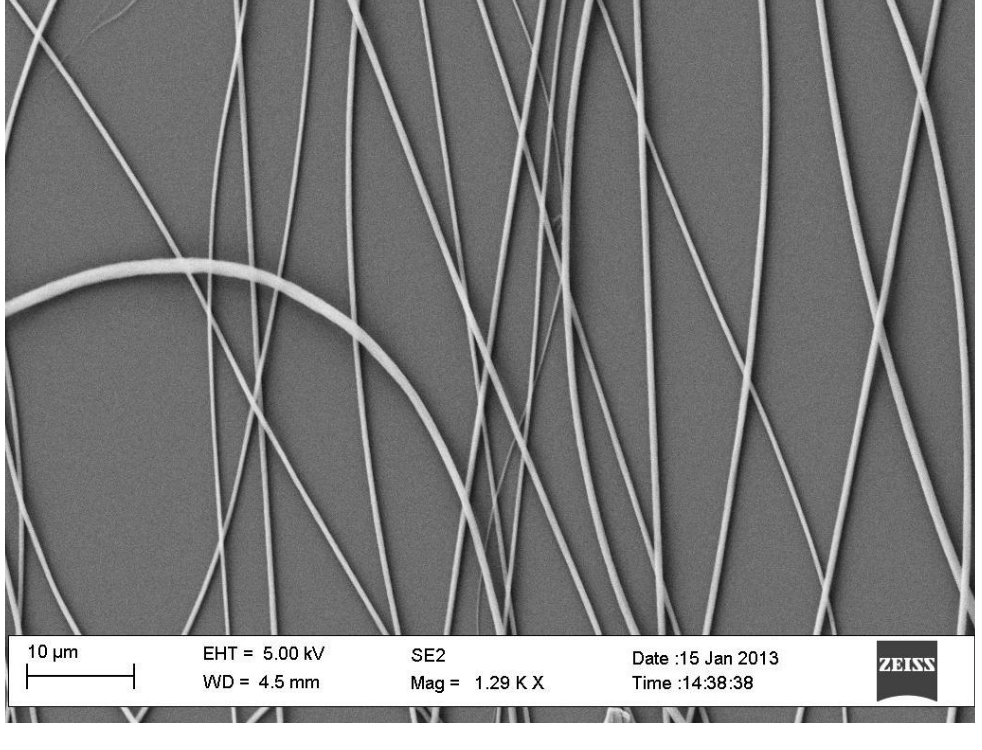


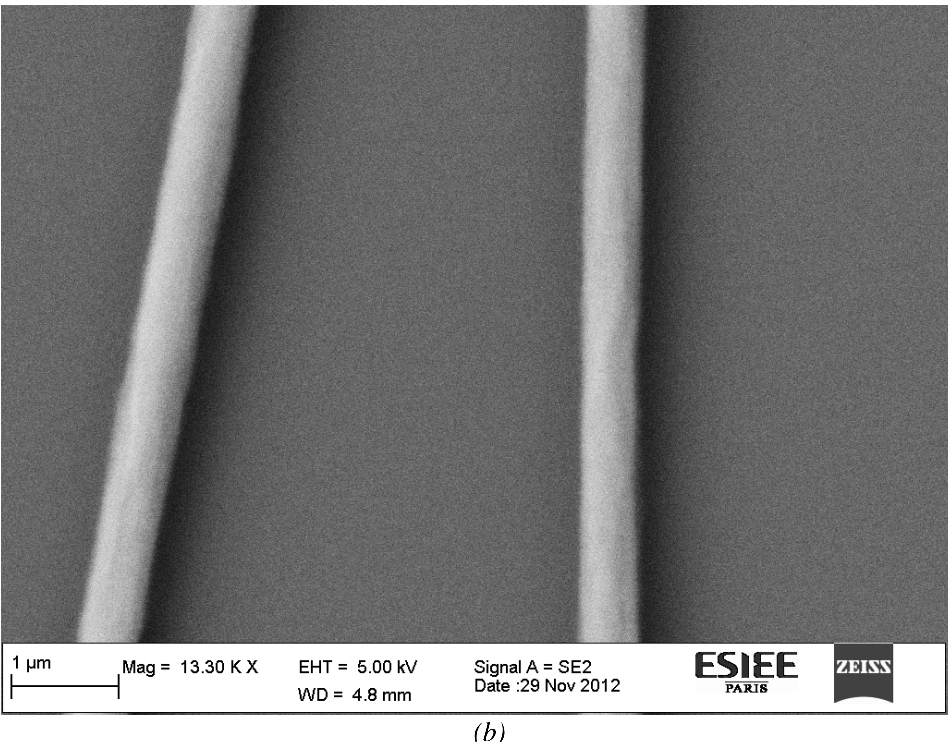
Figure 6.14. Photograph of sample prepared with strips of parallel conducting aluminum tape meant to act as alignment aides during electrospinning of nanofibers.

6.5. Conclusions

Clearly, using nanofibers as a template for DRIE is very promising to achieve HAR nanostructures especially for use in the fabrication of nanosuperlattices. The results achieved through these experiments have been very interesting and serve as a predecessor to further work that can be done with these techniques. For instance, these trenches can now be filled with a metal like Titanium using ALD (Atomic Layer Deposition) resulting in non-shape conformal superlattices at the nano-scale.



(a)



(b)

Figure 6.15 (a, b) SEM images of 'quasi-aligned' nanofibers using parallel strips of conducting Al tape as electrodes.

These can in turn be used to study the thermionic energy transfer at the atomic levels. This technique is also very novel and has not been used too much beyond cell culture and neuro-physiological applications thus far, though our contribution in extruding the 2D nanofiber patterns to obtain the corresponding 3D high-aspect ratio counterparts. Hence employing such a technique to fabricate not only potential thermal structures but also new kinds of scaffolds for cell culture, is a first and the direction is very promising for future applications.

Chapter 7

Focused Ion Beam (FIB) Patterning and Subsequent DRIE

7.1. Basic principles

In recent years, focused ion beam (FIB) instruments have become extremely handy in the microelectronics industry. One of the critical applications of FIB instruments is as a specimen preparation tool for subsequent analysis in other tools like the scanning electron microscope (SEM), transmission electron microscope (TEM), etc. [82].

The FIB instrument utilizes a finely focused ion beam from a Ga^+ liquid metal ion source (LMIS) to perform imaging and milling operations (See Figure 7.1) [83]. The interaction of the finely focused ion beam with the target material will produce the ejection of secondary electrons, secondary ions, and secondary neutrals. The ions and neutrals can be ejected as individual atoms, molecules, or clusters. The imaging capability of the FIB allows the use of either the secondary electrons or the secondary ions for the image formation. The milling operations are achieved through site-specific sputtering of the target material. Since sputtering is the basis for the milling operations, it is important to understand the ion beam–solid interactions and the sputtering process. An energetic incident ion, upon impact with a target material, will produce a collision cascade in the target material. If a surface atom receives enough of a normal component of momentum from the collision cascade to overcome the surface binding energy, the surface atom leaves the surface and is said to be sputtered [82].

The factors that affect sputtering include the atomic number, energy, and angle of incidence of the ion beam, the atomic density of the target, surface binding energy of the target, and crystallographic orientation of the target [84]. Among the various LMIS sources available, the most used is a Ga-based blunt needle source. Ga is used mainly for its advantages over other metals such as In, Bi, Sn, and Au because of its combination of low melting temperature (30°C), low volatility, and low vapor pressure. The low melting temperature makes the source easy to fire, Ga does not react with the material defining the needle (typically W) and evaporation is negligible. During operation, Ga flows from a reservoir to the needle tip (with an end radius of about 10 µm), where it is extracted by field

emission. A large negative potential between the needle and an extraction electrode generates an electric field of magnitude 10^{10} V/m at the needle tip [85-87]. The balance between the electrostatic forces and the Ga surface tension wetting the tapered W needle geometry results in the formation of a single Taylor cone at the needle tip. For typical emission currents used in FIB microscopes (~2 mA), a cusp forms at the tip of the Taylor cone with a tip radius of approximately 5 nm [88]. The simplest and most widely used ion beam columns consist of two lenses (a condenser and objective lens) to define the beam and then focus it on the sample, beam-defining apertures to select the beam diameter and current, deflection plates to raster the beam over the sample surface, stigmation poles to ensure a circular beam profile.

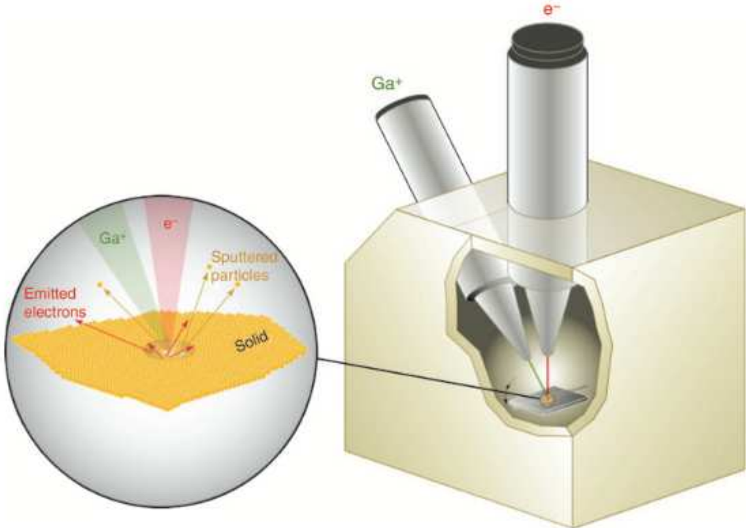


Figure 7.1. Dual beam microscope having one column each for SEM and FIB (reproduced from [83].

7.2. FIB Etching

The FIB is an expensive tool [89]. In this work, we have created patterns by ion milling using the FIB directly on an Aluminium thin film (~50 nm) deposited on silicon. Once these patterns were 'written', subsequent DRIE was performed to try and create HAR trenches in silicon. To aid us in locating the area where the FIB milling (and DRIE etching) was done, we have designed a mask with clearly demarcated crosses of hierarchically reducing dimensions (from 200 µm – 2 µm) with a numbering system. Figure 7.2 shows a close-up view of the design when zoomed into one of the highest level crosses. There are 3 levels of crosses in all to help us identify the exact spot of FIB etching during SEM observation of post-DRIE etched samples.

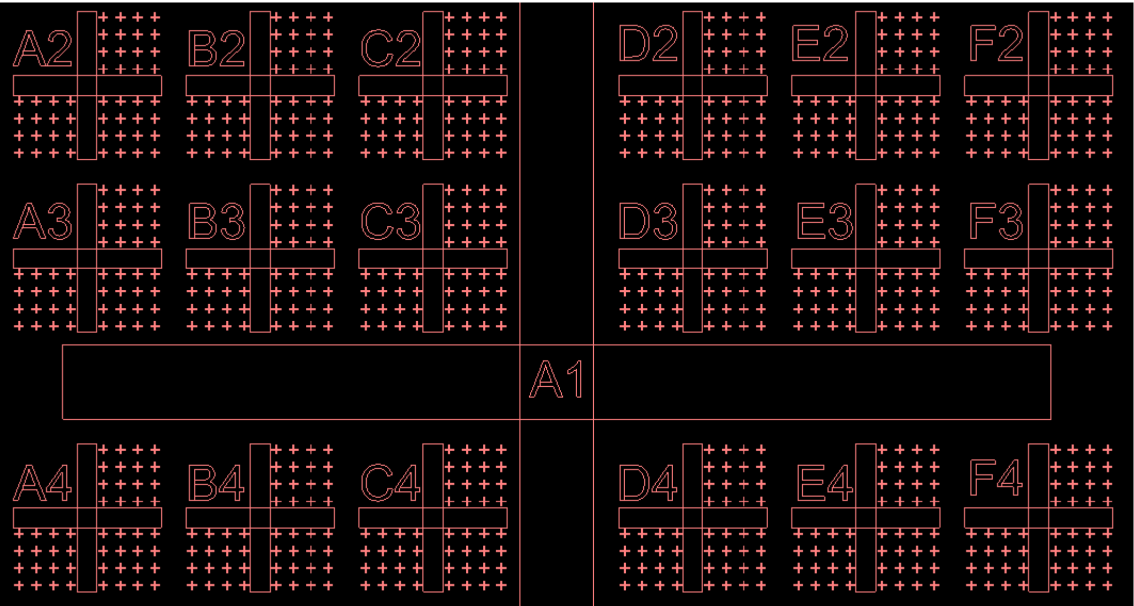


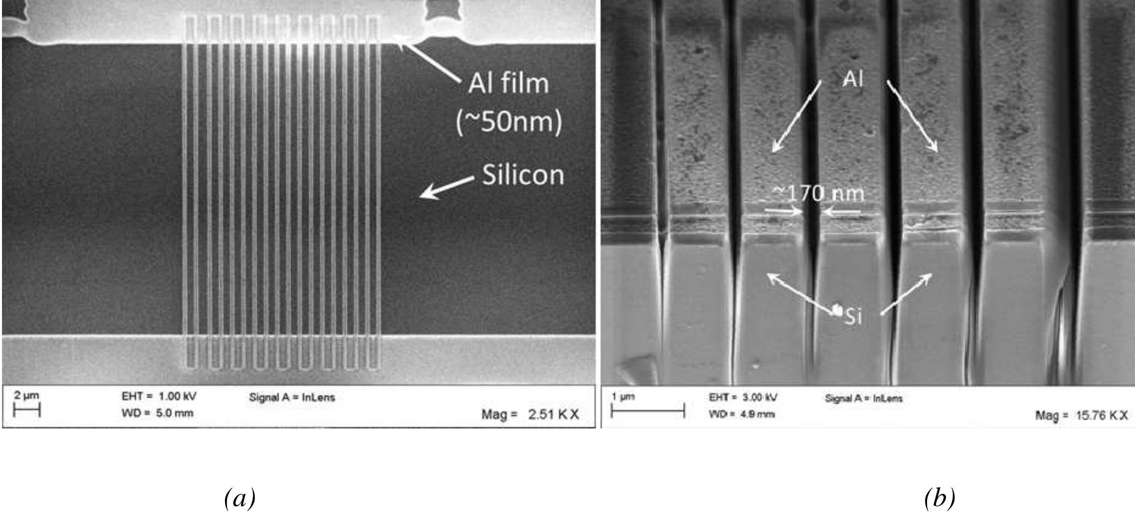
Figure 7.2. Magnified view of one of the higher level crosses on the mask showing the other 2 levels of crosses for easy identification under the microscope.

The FIB lines were created by using the ion milling feature of the FIB. For creating the electrode-like structures shown in Figure 7.3 (a), a beam current of 50-100 pA was used. The pattern was created over a 15 µm x 30 µm area. The depth of the etch was specified to be ~0.5 µm. Figure 7.3 (b) shows the slices that were created by the FIB. In this case, the current used was 5 nA. The initial slice was programmed and then repeated in equal intervals to create the slices about a micron apart. These samples were then etched by cryogenic DRIE to achieve HAR structures. The Al that rests on top acts as a mask during DRIE. The process and results from the etching are discussed in the next section.

7.3. DRIE Results

The width of the lines created by the FIB were typically in the 30-100 nm range. Subjecting this kind of sample to a Bosch process etching would most likely result in sample destruction because of the scalloping intrinsic to the Bosch process etching. Hence we performed only cryogenic etching on the FIB etched samples. Conditions used for cryogenic etching were standard parameters, summarized here in Table 7.1.

It is known that within a specific window, the cryogenic etching of silicon under SF_6/O_2 plasma results in the formation of "black silicon" (BS), a needle-shaped surface structure where "needles" are made of single-crystalline silicon and have a height above 10 microns and pitch of <1 micron when the ideal conditions are present [90-93].



(a) *(b)*

Figure 7.3. (a-b) Sets of lines/slices created by ion milling using FIB on Al over Si.

Table 7.1. Process parameters for standard cryogenic etch process.

Source Power (W)	SF6 flow (sccm)	O2 flow (sccm)	Pressure (mT)	Substrate bias (W)	Temp (°C)	Etch time (m)	Etch rate (µm/min)
1000	180	12	30	80	-110	10	0.45

These conditions, the processes used specifically to produce BS, etc. are discussed in detail in Appendix II of this thesis. On the SEM image of Figure 7.4 (a) one can see on one hand, the black silicon which was achieved unintentionally after the cryogenic etching of the widest openings of the FIB patterns. Figure 7.3 (a) and Figure 7.4 (b) shows a different part of the sample exhibiting different types of BS surfaces formed. On the other hand, Figure 7.5 shows the etching results obtained for the thinnest slices in Figure 7.3 (b). These very fine FIB lines, the thinnest of which is ~35 nm in width led to nano-trenches in the silicon bulk of about 4.3 µm in depth with an aspect ratio > 120:1. These results were discussed in the previous chapter.

7.4. Conclusions

The use of FIB etching is actual micromachining is a relatively recent one. It has been in use for mask corrections, specimen preparation, etc. We have indulged the option of using this tool to create patterns on an aluminium mask on silicon and to etch them by a well-developed plasma recipe to achieve HAR structures. Very high aspect ratios of ~120:1 have been achieved using this method.

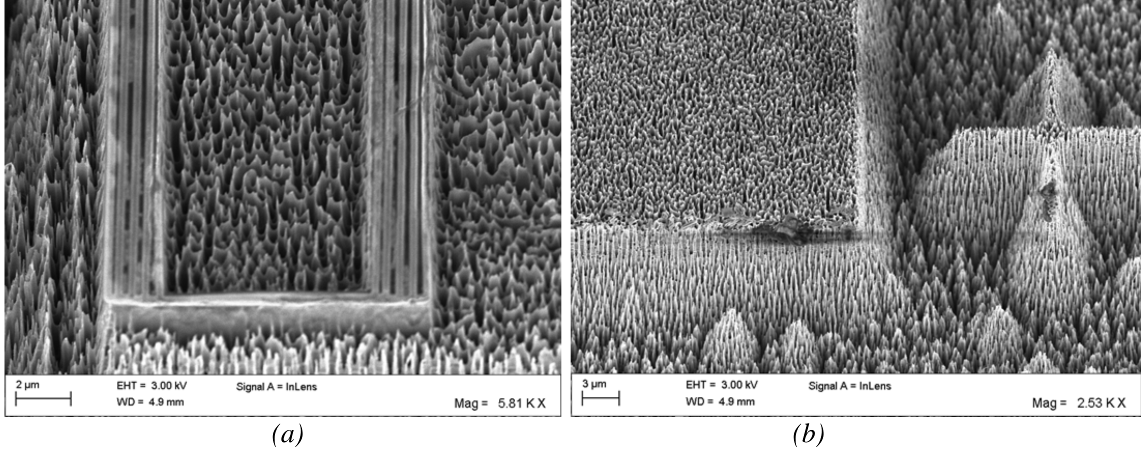


Figure 7.4. SEM image after cryogenic etching of (a) FIB lines from 7.2 (a) and (b) different parts of the same sample exhibiting a variety of BS surfaces.

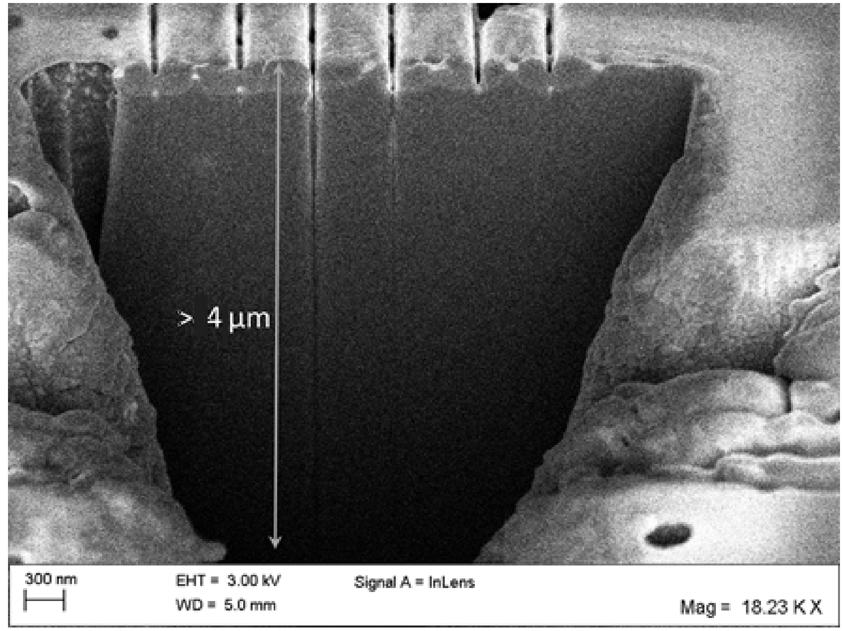


Figure 7.5. Cryogenic DRIE etch result for slices shown in Figure 7.3 (b).

These initial results have been encouraging and it is possible to conduct further experiments to better what has been achieved through the course of this work, even though FIB requires scanning over the surface, which is time-consuming and not cost-effective. The next chapter explores with another option with the primary aim of reducing costs and producing a high throughput. It deals with the bottom up approach of using diblock copolymer lithography to achieve *self-assembled* nanostructures in silicon which can then be used to create HAR nanostructures.

Chapter 8
Advanced Transfer of Micro and Nano-structures by *bottom up* approach: Diblock Copolymers

8.1. Introduction

The methods typically used to produce patterns in microfabrication are externally controlled by using tools to cut, mill, and shape materials into the desired shape and order. Previous chapters of this thesis dealt with the fabrication of the vertical superlattices using several micropatterning techniques such as photolithography and related techniques. This approach is called the 'top-down' approach in microfabrication.

Over the past decade the focus of microfabrication techniques has shifted to nanoscale dimensions due to the fact that the characteristic feature size required in many applications has gone down to the nanometer scale. The theoretical limitations of photolithography were discussed in detail in Chapter 5. Even with advancement in optics and improving numerical apertures, the research for alternate methods of nanoscale patterning have gained momentum over the past two decades. A new approach called '*bottom-up*' has been developed over the past few years. These techniques usually involve the chemical properties of single molecules to cause them to self-assemble or organize in a manner that could be useful for certain applications. Specifically, one of the methods that has seen a lot of success in this area is the fabrication of large-area periodic structures on the nanoscale using polymer based self-assembly. It is of great interest because of its potential simplicity and low cost [94].

Block copolymers (BCP) are a class of macromolecules that are produced by covalent bonding of two or more chemically distinct homopolymers (blocks). Depending upon the number n of constituent blocks, the nomenclature for such polymers is diblock ($n = 2$), triblock ($n = 3$), etc. They represent a subject of wide interest in fields of macro- molecular physics and chemistry because of their remarkable ability to self-assemble into a variety of

ordered structures with nanoscale periodicities. The nomenclature also denotes these distinct polymers by consecutive letters. Hence a diblock copolymer would be an A-B type of polymer (or A-*b*-B where the "*b*" denotes the "block"). A triblock could be of A-B-C or A-B-A architectures. The letters may be substituted by the polymer acronym: PS-*b*-PE for a polystyrene polyethylene diblock copolymer.

Microphase Separation and Morphology

In a diblock copolymer, AB, the two block components are usually immiscible in bulk - however, due to covalent bonding, the blocks cannot form macroscopically large phases of A and B. Instead they exhibit microphase separation where microdomains of the minority block form within the matrix of the majority block. If V_A and V_B were the effective volumes of the constituent blocks A and B of the diblock copolymer, in the order of increasing volume ratio $f = V_A/V_B$, the shapes of the microdomains would range from spheres (for f<<1) to cylinders, to gyroids – a rare phase of perforated lamellae and – finally lamellae (for f~1). It must be noted that the compositions of the microdomains and the matrix are reversed for V>1 [95]. This phase separation is driven by two opposing forces: unfavorable enthalpic interactions and entropic energy [95, 96]. The enthalpic interactions tend to separate the BCPs, whereas entropically the polymers tend to mix. It depends critically on the temperature and the strength of interaction to decide which tendency prevails. At elevated temperatures, the entropy dominates and the BCPs are in a disordered state. On reducing the temperature, the enthalpic interactions start dominating and microphase separated structures are formed. Figure 8.1 illustrates the bulk configuration of diblock copolymers [98].

The microphase separation can be thermodynamically expressed in terms of Flory-Huggins theory for a system with two components – A, with N_A molecules occupying a volume fraction f, and B, with N_B molecules occupying a volume fraction (1-f) [97].
For such a system, free energy of mixing, F, can be expressed as:

$$\frac{F}{(K_BT)} = \frac{f}{N_A}\ln(f) + \frac{1-f}{N_B}\ln(1-f) + \chi f(1-f) \quad (8.1)$$

where the first two terms are entropic contributions of the respective polymers

(proportional to N_A and N_B respectively) and the third term accounts for the energetic penalty due to mixing. The system will phase separate only when the entropic term is overcome by the energy gain due to phase separation. Thus, the product χN represents the enthalpic-entropic balance and is used to characterize phase behavior of BCP together with the volume fraction of one block (f).

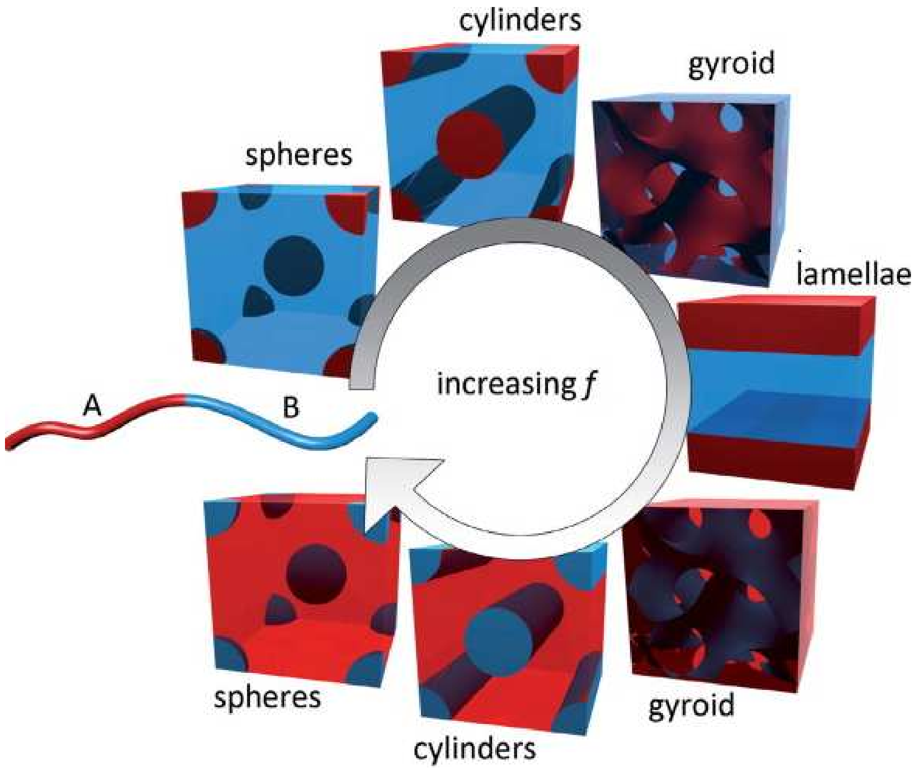


Figure 8.1. Bulk configurations of diblock copolymer phases for increasing volume, f, of Polymer A to Polymer B (reproduced from [98]).

Block copolymer lithography is similar to conventional lithography in that it provides a well-defined "stencil" on the substrate which can then be transferred successfully onto it. However, unlike photoresists which form a layer that can only provide a base to image a mask, the block copolymer films tend to self-assemble themselves autonomously at dimensions in the nanometer scale as defined by the ratio of the volumes and molecular weights of the constituent blocks. While block copolymer lithography offers an attractive alternative to traditional UV photolithography techniques, their limitation lies in the restricted number of patterns that are achievable by them. However, within these constraints by adjusting the

molecular mass of the polymer, and the composition (volume fraction, *f*), block copolymers provide a straightforward means for achieving feature sizes (<20 nm), pitches (<40 nm), and densities (~$10^{11}/cm^2$) that are currently not achievable by optical lithography [99-101], and can only be hardly obtained by electron lithography and at much higher costs. These length scales are attractive for numerous potential applications where nano-patterning is required, such as in electronics, optoelectronics and magnetic storage devices. Thus, block copolymers are a good choice, both in terms of thermodynamics and dynamics of self-assembly systems to create metamaterials. Figure 8.2 illustrates some of the possible areas of nanotechnological applications where block copolymers could be used [102].

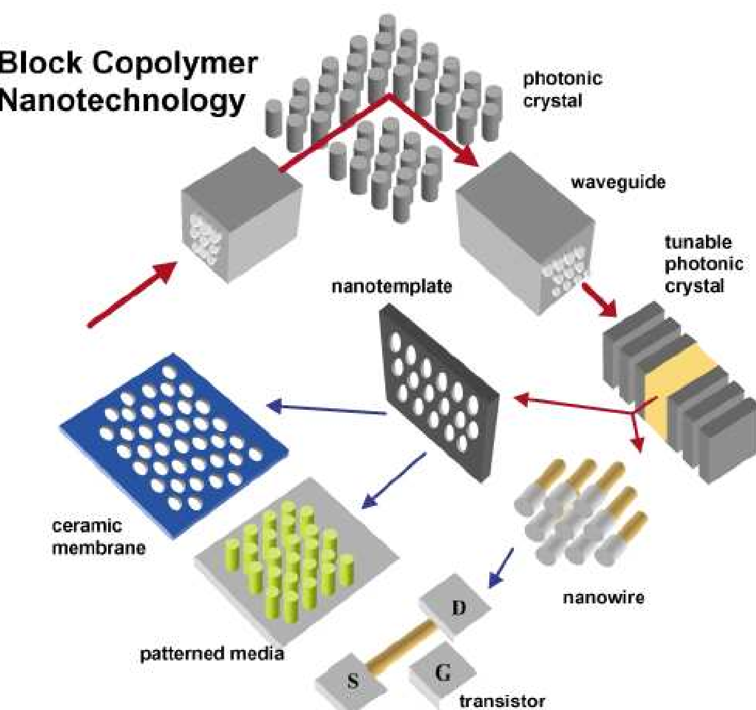


Figure 8.2. Illustration of possible nanotechnological applications of block copolymers (reproduced from [102]).

8.2. Diblock copolymers as a mask

In this work, we have used copolymer constituted of Polystyrene (PS) and Poly Methyl Methacrylate (PMMA). It is denoted as PS-*b*-PMMA. It is synthesized by living anionic polymerization, which is one of the most versatile methods of polymerization available [103-105]. In this method, it is made by first polymerizing styrene, and then subsequently polymerizing MMA from the reactive end of the polystyrene chains.

The particular sample used in this work is copolymer P6402 with the molecular ratio of PS: PMMA in cubic moles as 64-*b*-35.0 (determined by gel permeation chromatography). This polymer yields patterns in the shape of cylinders when synthesized. At room temperature and for the molecular weights of interest in this study, PS: PMMA presents itself in solid form. Its chemical structure is shown below in Figure 8.3 [103] –

*Figure 8.3. Chemical structure of PS-*b*-PMMA (reproduced by [103]).*

Block copolymer thin films have already been used as sacrificial etching masks in lithographic processes [94, 106]. The key however, is to have a block copolymer film with good chemical selectivity between its constituents so that one may be removed and the other can act as an etch mask to pattern an underlying film. For example, Park et al. fabricated hexagonal arrays of holes and dots in silicon nitride by using sphere forming Poly (styrene-*b*-butylene) (PS-PB) monolayer as an etching mask [94]. In this case, PS-PB was spin coated on silicon nitride and then reactive ion etching (RIE) used to selective remove the PS or PB, depending on the type of structure required. The remaining polymer then acted as a mask to transfer the microdomain pattern to the underlying silicon nitride in order to create dots or holes depending on which polymer was eliminated. Similarly in this work, we eliminate the PMMA domains and use PS as the masking layer to transfer patterns on to silicon for further high aspect ratio (HAR) structures in silicon.

The next few sections will describe in detail the copolymer lithography techniques performed with this block copolymer and the results obtained from them.

8.2.1. Fabrication process

The process for obtaining self-assembled features through block copolymer lithography involves a number of steps. The schematic for this process is shown in Figure 8.4.
The steps involved will be described in the following sections.

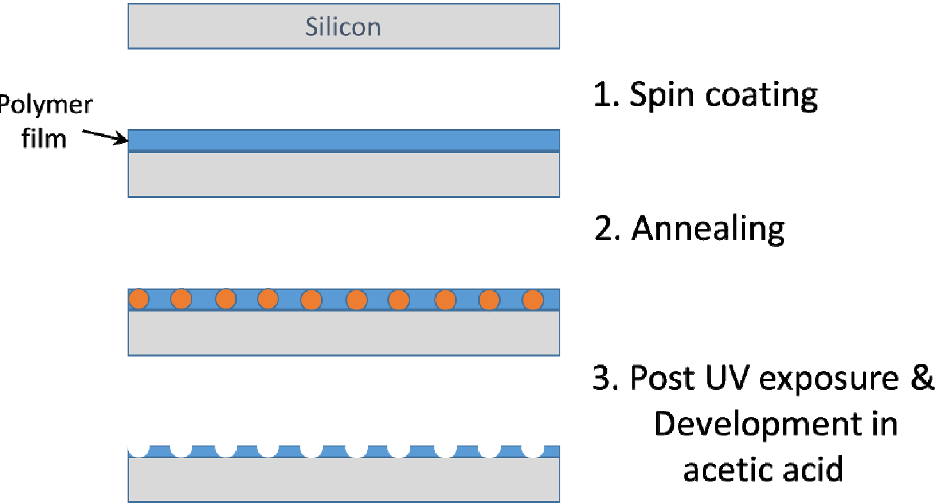


Figure 8.4. Schematic illustration of the process to obtain self-assembling block copolymer patterns on a substrate.

8.2.1.1. Spin coating

While thin films of copolymers can be obtained from a variety of methods, spin coating is one of the oldest ones in use especially in the semiconductor industry. The spin coating procedure consists of placing the target substrate on a holder where it is held in place by vacuum. The solution to be cast, usually the photoresist, is then dropped on the surface after which the substrate is rotated at an angular speed of many thousands of rotations per minute (rpm) for about 30 seconds. Excess material is scattered clear of the substrate by a centrifugal force, leaving a uniform layer of deposited material on the substrate. Figure 8.5 is a schematic of the spin coating process [107].

To use spin coating for getting a monolayer of the diblock copolymer, which is in the order of few tens of nanometers, a modified spin coating process is employed. The polymer is dissolved in a solvent that is effective on both its constituent blocks. In the case of P6402, toluene is an effective solvent. The concentration is usually very dilute, in the order of 1-2% [108-111]. The P6402 polymer is dissolved in toluene to make a 1.5% (w/v) solution for spin

coating. The theory is that when spun at extremely high RPMs, ramped up rapidly, the solvent rapidly evaporates, leaving behind a uniform layer of copolymer on the substrate.

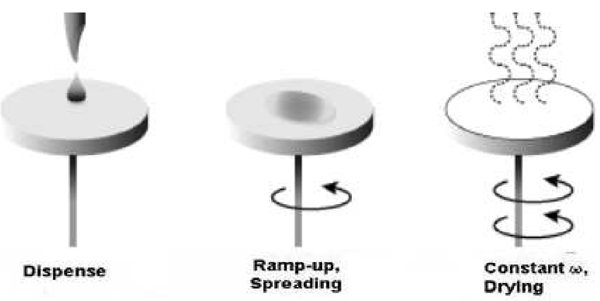


Figure 8.5. Illustration of the spin coating process (reproduced from [107]).

To arrive at a monolayer of the copolymer, experiments involving different spin speeds (1000-5000 rpm) were performed with a ramp of 10000 rpm/s. The thickness of the samples was measured by ellipsometry to determine the average thickness of the polymer films.

Figure 8.6 graphically represents the data obtained through these experiments. Corresponding optical microscope images of the films at different thicknesses post-annealing are depicted as well. The colour gradation is an indication of film thickness as well.

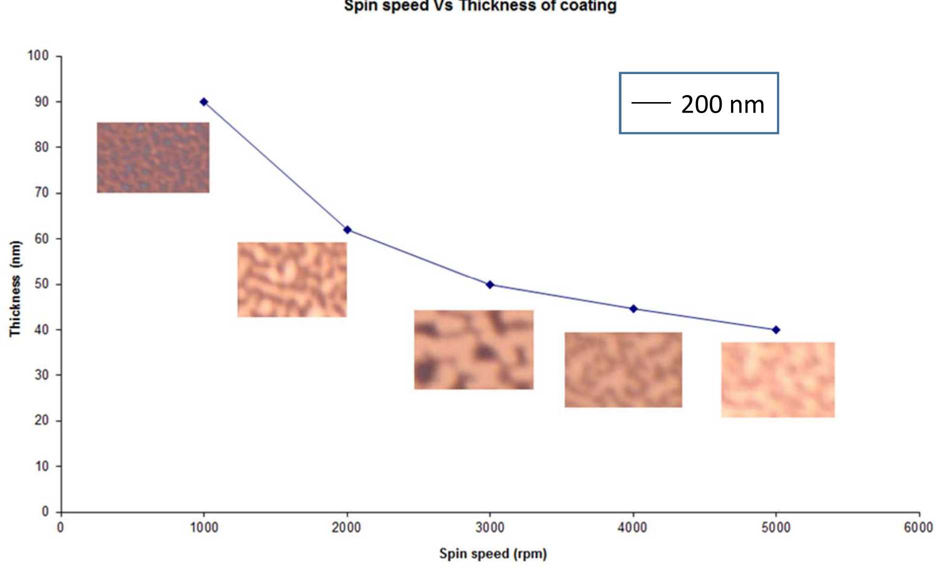


Figure 8.6. Spin speed vs. thickness obtained of polymer films with optical microscope images of films annealed after deposition at different spin speeds.

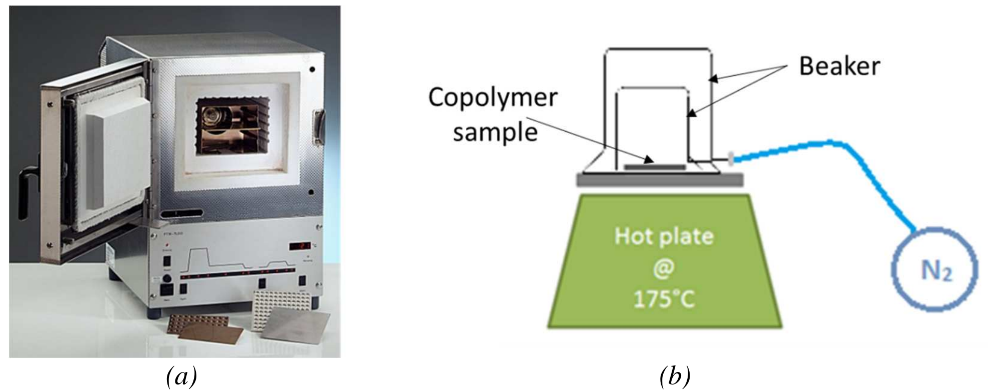
It is apparent from the plot that the curve flattens towards 5000 rpm, hence showing that the thickness of the layers tends to edge out at ~40 nm. It was concluded 4000 rpm was the spin speed most likely to result in a monolayer thickness of copolymer atop the substrate.

8.2.1.2. Annealing

For the polymers to be able to phase separate we need to anneal them at a temperature greater than the glass transition temperature of both the constituent polymers [112, 113], but below the melting transition. Annealing temperatures reported in the literature are typically around 175°C for PS-PMMA and annealing is performed either in vacuum or in a nitrogen flooded oven to avoid oxygenation of the polymer.

At temperatures above the glass transition temperatures of the constituent polymers, the molecules within are free to diffuse through the films, hence contributing to the coarsening of the 2D micro patterns [111]. The amount of ordering (as measured by bond correlation lengths) in existing lattices increases with annealing times [119].

Experiments have been done both with an oven with a chamber that has access to continuous nitrogen gas flow and on a hot plate with a simple setup of continuously flowing nitrogen with very different results. These results will be discussed in detail in subsequent sections. Figure 8.7 shows the annealing setups we have used in this work in the (a) oven configuration (typical annealing oven) and (b) schematic of the hotplate annealing setup. The double beaker configuration in 8.7 (b) is just to ensure complete nitrogen flooding in the inner chamber over the copolymer sample.



(a) *(b)*

Figure 8.7. Annealing setup for copolymer samples in (a) oven (not actual) and (b) hot plate

8.2.1.3. UV Exposure

In diblock copolymer lithography, we selectively remove one of the constituent polymers, usually, the weaker one, leaving behind the other polymer to serve as a template for the next step. In the case of the PS-PMMA diblock copolymer, the PMMA domains can be removed when irradiated by an ultraviolet source [114]. Guarini, et al [115] used peak wavelengths of 184 nm and 254 nm and a dose of ~ 10mW/cm^2 for about 2 minutes, i.e. a UV dose of ~1.2 J/cm^2, to destroy the PMMA in their samples. On the other hand, doses as high as 10 J/cm^2 have been tested with success by the group in Karlsruhe, Germany [116].

For the purpose of our experiments we use a 254 nm UV lamp. We decided to start with a dosage of ~500 mJ/cm^2 with a lamp intensity of 1.7 mW/cm^2, which would require ~5 minutes of short-range exposure. Initial experiments with 5 minutes of exposure time did not result in any visible damage to the PMMA domains. Hence in our experiments we have varied the UV exposure times from 30 minutes to 2 hours to obtain the correct dosage required to destroy the PMMA domains of our samples. However it is required to remove the destroyed polymer fragments before any imaging can be done. The removal of the polymer fragments using acetic acid and subsequent imaging is discussed in the next sub-section.

8.2.1.4. Acetic Acid Development

Once the PMMA has been destroyed by the UV, the destroyed polymer fragments can be rinsed away by acetic acid [99,117, 118]. Occasionally, this is followed by toluene rinse. The PS cross-links under UV exposure and hence is no longer endangered by the toluene.

In this work we tested a development times in acetic acid for durations of 1 minute, 10 minutes and 30 minutes using 60% and 100% strengths of acetic acid. These experiments were performed in tandem with the UV exposure times of 30 minutes, 1 hour and 2 hours, giving us a comprehensive sample set to draw conclusions from. All of the samples were prepared as discussed in Section 8.2.2.1 and were annealed in the oven overnight (~12 hours).

Table 8.1 shows the entire sample set of our experiments for exposure and development of the copolymer samples. Each of the samples were observed under SEM to arrive on the ideal UV exposure – acetic acid development combination required for PMMA domain destruction and removal.

Table 8.1. Different test conditions for UV exposure and acetic acid development.

Sample	UV exposure time (min)	Acetic Acid conc.	Acetic acid development (min)	SEM Observations
1	30	60%	10	PMMA domains still visible
2	30	100%	10	No visible patterns. Strong acid possibly destroyed sample.
3	30	60%	30	Very uniform phase separated polymer.
4	30	100%	30	Multiple layers. Both polymers visible.
5	60	60%	1	Multiple layers.
6	60	100%	1	Very high UV exposure destroyed sample
7	60	60%	10	Very high UV exposure destroyed sample
8	60	100%	10	Very high UV exposure destroyed sample
9	60	60%	30	Very high UV exposure destroyed sample
10	60	100%	30	Very high UV exposure destroyed sample
11	120	60%	1	Very high UV exposure destroyed sample
12	120	100%	1	Very high UV exposure destroyed sample
13	120	60%	10	Very high UV exposure destroyed sample
14	120	100%	10	Very high UV exposure destroyed sample
15	120	60%	30	Very high UV exposure destroyed sample
16	120	100%	30	Very high UV exposure destroyed sample

The best results obtained have been highlighted in blue in the table.

Results from UV exposure-Acetic acid development

Figures 8.8 (a), (b) and (c) show SEM images corresponding to Sample 2, 3 and 6, which show the sample destroyed by very strong acid, the best case parameters, and sample destroyed by high UV exposure respectively.

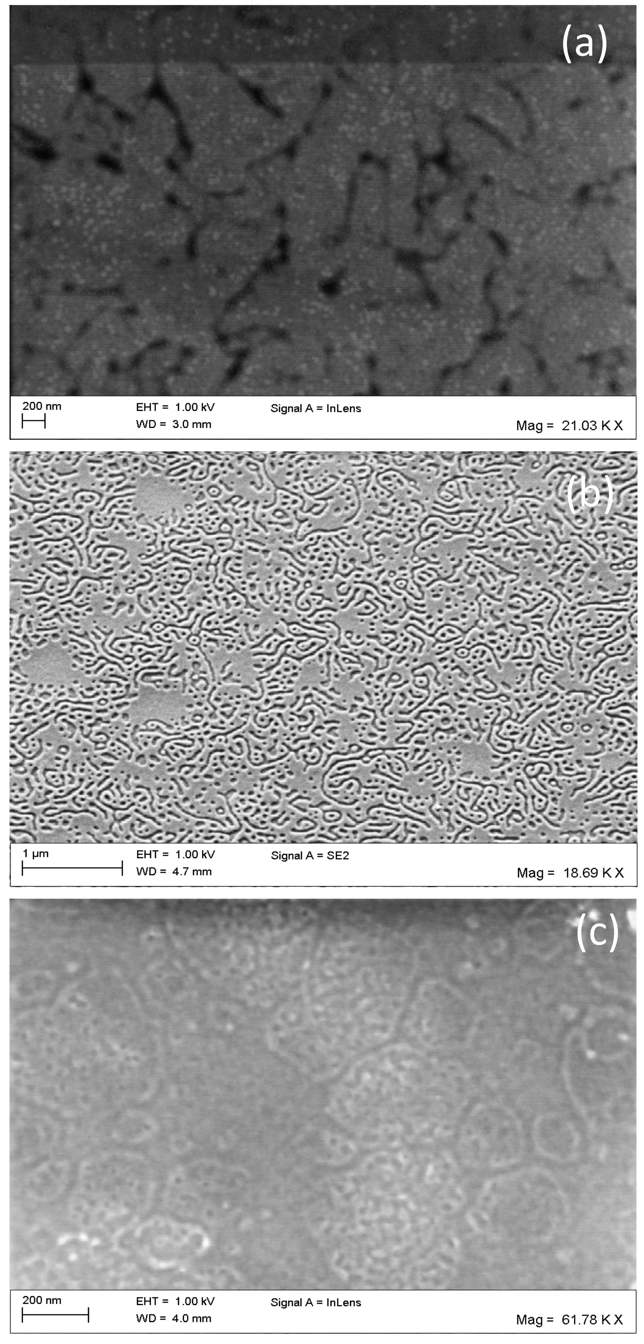


Figure 8.8. SEM images of sample (a) destroyed by strong acid, (b) well-exposed and developed and (c) destroyed by over-exposure to UV.

Here, we note that though patterns obtained for Sample 3 were phase separated, and had the right combination of UV exposure and acetic acid development, the morphology of these samples are very different from what was expected. Hence with a different sample, we performed annealing on the hotplate as shown in Figure 8.7 (b) with all other conditions kept

the same as best found. The SEM results from this sample are shown in Figure 8.9. It is clear that these patterns are typical of phase separated PS-PMMA planar cylinders and are very different from those in Figure 8.8 (b). We don't have any conclusive evidence as to why this discrepancy was observed. It must be noted that other groups have performed annealing in ovens and hotplates with similar degrees of success and this discrepancy is related to the specific equipment in our cleanroom [112, 115]. It is our hypothesis that the oven is probably not fully flooded with nitrogen due to some leak or due to a lack of sufficient in-oven nitrogen pressure.

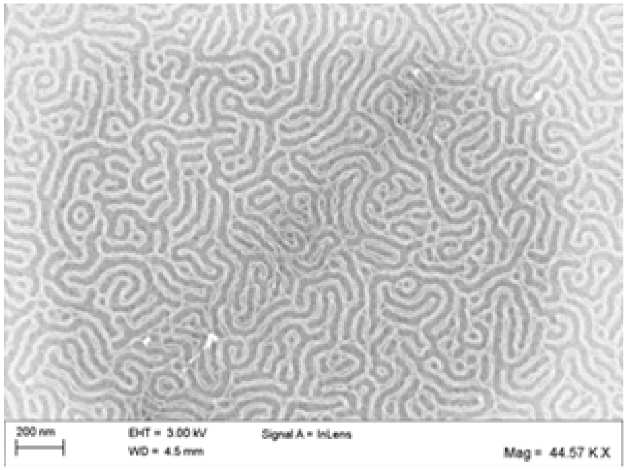


Figure 8.9. SEM image of P6402 samples annealed for 5 hours on a hotplate and then exposed to UV for 30 min and developed in 60% acetic acid for 30 min.

8.3. Etching Experiments

Figure 8.10 is a schematic illustration of the process of achieving HAR nanostructures in silicon using transfer of block copolymer templates. Two representations of the PS domains after PMMA removal have been depicted. This is because they could be present at different positions in the polymer film. At the polymer-silicon interface, there exists a thin wetting layer of PS [119]. A CF_4 based RIE etch is performed to remove the wetting layer and reach the surface of the silicon. This process and the results obtained from it are discussed in the next section.

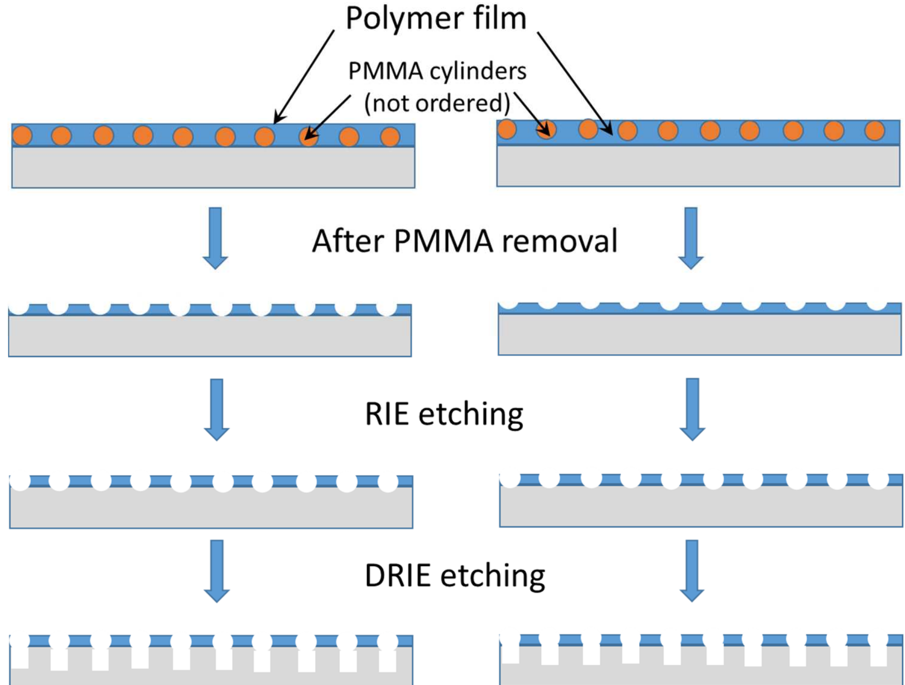


Figure 8.10. Patterning process with block copolymer nanostructure on silicon substrate: (a) PS domains after PMMA removal, (b) after RIE etching of polymer film, and (c) DRIE etching of exposed silicon using copolymer as template.

8.3.1. RIE Etching of polymer

Reactive Ion Etching is a form of dry etching, usually performed in order to obtain anisotropic etches on silicon. This principle can be applied to etch the parts of the polymer film in order to be able to reach the surface of the silicon and then transfer the overlying PS patterns onto the wafer (See Figure 8.10).

RIE etching of block copolymer has been successfully used by many groups to transfer patterns on to their substrates [120-122]. Typically the gases used for etching depend on the material to be etched away. In the past O_2 plasma, CF_4 plasma, SF_6 plasma and CHF_3 plasma have all been employed successfully to etch the polymer. In this work, we used CF_4 plasma for etching. Various experiments were conducted by varying all the parameters of the RIE etch including gas flow, power, pressure, bias voltage, and etch time in order to reach the underlying silicon substrate. The different etch conditions tested to etch away the polymer film are shown in Table 8.2 along with the observations made from the SEM imaging of these samples.

Table 8.2. RIE etch test parameters for etching away the polymer film.

Sample ID	Power (W)	Pressure (mT)	Bias (V)	Etch Time (s)	SEM Observations
1	60	15	100	5	Highly under-etched
2	60	15	100	10	Highly under-etched
3	60	15	100	15	Highly under-etched
4	60	15	100	20	Highly under-etched
5	60	15	100	30	Under-etched
6	60	15	100	40	Under-etched
7	60	15	100	60	Slightly under-etched
8	60	15	100	80	Slightly under-etched
9	60	15	100	90	Slightly under-etched
10	60	15	100	100	Slightly under-etched
11	60	15	100	120	Sample destroyed
12	60	15	100	300	Sample destroyed
13	90	15	160	90	Almost on Silicon
14	60	30	100	90	Sample destroyed
15	60	5	100	90	Almost on silicon
16	30	15	40	90	Polymer film etched completely
17	30	15	40	30	Slightly under-etched
18	30	15	40	60	Under-etched
19	30	15	40	120	Over-etched
20	30	15	40	150	Over-etched
21	10	15	5	300	Sample destroyed

The parameters that were used to successfully etch away the polymer film have been highlighted in the table. Figure 8.11 shows a SEM image after the etched sample. The scratches made on the surface of the sample help us focus better with the SEM during imaging.

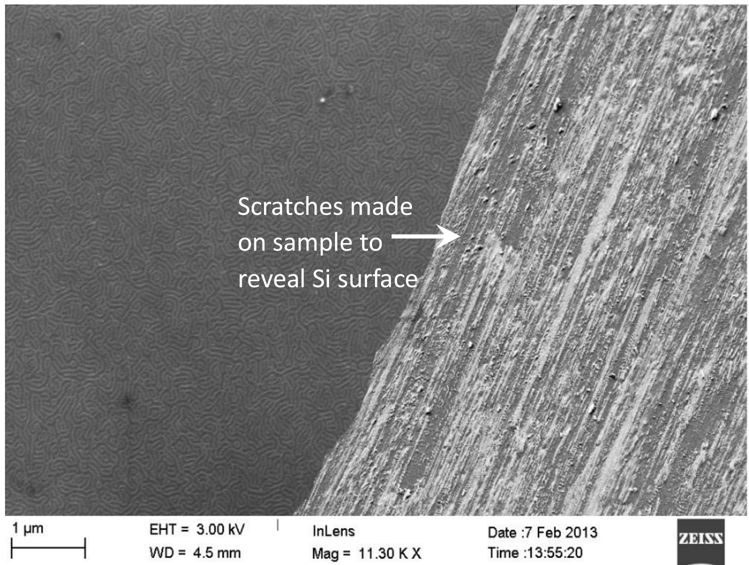


Figure 8.11. Successful RIE etching– 30W/15mT/40V/90s.

After the etching of the polymer film, the surface now exposes PS cylinders lying on silicon. Hence we can obtain HAR structures by deep etching of the silicon. We have attempted the following etching methods –

- Direct FIB etching
- FIB patterning followed by cryogenic DRIE etching
- Bosch DRIE after copolymer lift-off

We will describe the processes used in each of these methods of etching and their corresponding results in this section.

8.3.2. FIB Etching

The working principle of the Focused Ion Beam etching and its use with DRIE was previously discussed in Chapter 8. FIB systems operate in a similar fashion to the SEM systems, the major difference being that the etchants are a beam of ions (usually gallium, Ga^+ ions) as opposed to electrons in a SEM. The beam currents can be altered to be low or high to cause minimal milling (or sputtering) or indeed very rapid etching of the target material. Similar to the SEM, the substrate under observation is getting bombarded by Ga^+ ions even as it is being imaged. The FIB is a handy yet expensive tool to etch small quantities of materials from target substrates. In the case of block copolymers, it can be an alternate method as the

amount of material to be etched is relatively less because of the nanoscale dimensions of the BCP patterns.

In this work we have attempted to etch BCP samples using the FIB milling. It is to be noted that all these experiments were performed using the samples annealed in the oven (as shown in Figure 8.8 (b)). Sample mounting is of great importance when using the FIB. As the FIB column attaches to the SEM in a dual-imaging system, the angle of the sample to the normal stage position needs to be 54° which corresponds to the angle between the FIB beam and the SEM beam. The beam shift is then adjusted accordingly to have an image sharp in focus.

For etching the BCP we have used an ion milling current of 5 nA over a 10 μm^2 area for a duration of ~5 minutes. We took snapshots of the etched zone every 30 seconds to create a composite record of about 100 images to visualize the FIB etching as it proceeded. We imaged the area where on the sample we could visualize regions where there was no etching, some etching and over etching. These results are presented in the SEM image shown in Figure 8.12. This image is the last in the 5 minute FIB etching sequence and the portions with different etch profiles are clearly discernable in the sample and have been marked for the sake of clarity.

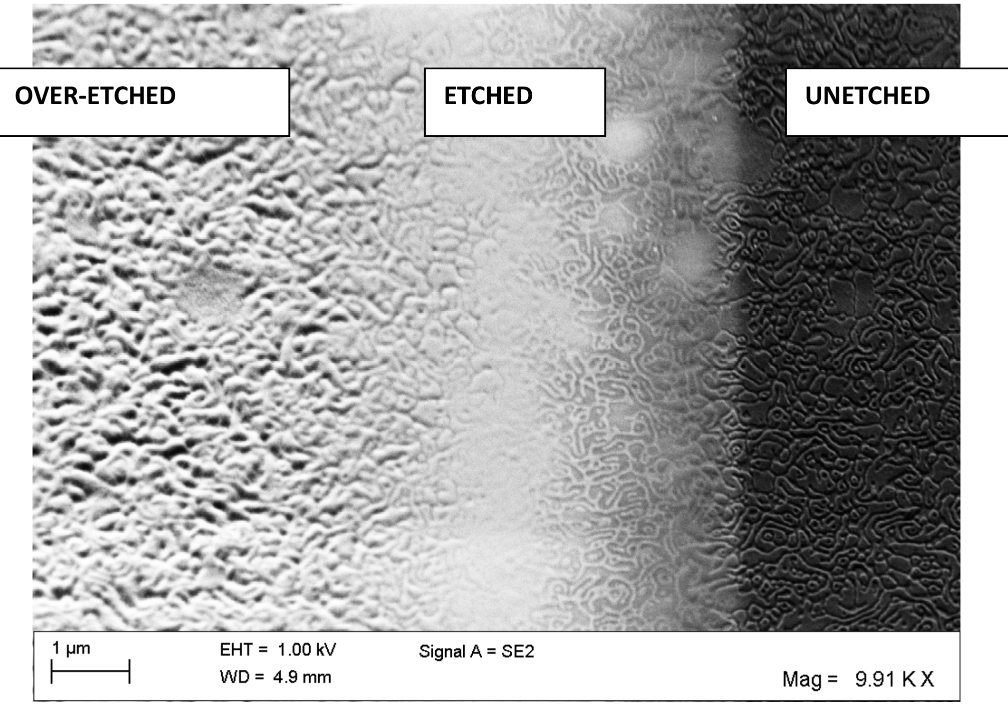


Figure 8.12. End of FIB etching using ion milling of 5 nA over an area of ~10 μm^2. Clearly the left part of the image shows the patterns etched into the substrate while the middle part has begun etching and the right part remains unetched.

8.3.3. FIB patterning followed by cryogenic DRIE

In the previous sub-section, we succeeded in etching the copolymer pattern into the silicon substrate using FIB etching. In this section we discuss our results from performing a subsequent cryogenic etch on such samples. This step is the attempt to obtain HAR structures in the copolymer patterns in silicon. A cryogenic etch is a deep reactive etch process that is performed at -110°C in a combined plasma of SF_6 and O_2 which results the etching of silicon [16]. A similar experiment was previously described in Chapter 6 in Section 6.3 for etching lines created by the FIB. In this section, we discuss results from copolymer DRIE after an initial FIB etching. The etching parameters for copolymer cryogenic etching are summarized in Table 8.3.

Table 8.3. Parameters for cryogenic etch of copolymer.

Source Power (W)	**SF_6 flow (sccm)**	**O_2 flow (sccm)**	**Pressure (mT)**	**Substrate bias (W)**	**Temp (°C)**	**Etch time (s)**	**Etch rate (µm/min)**
1000	200	12	30	46	-110	60	0.45

The etching resulted in producing Black silicon, the formation of which was described in Chapter 8 – Section 8.3. This is possibly due to the cryogenic process having a very high passivation regime (high O_2 gas flow) combined with a low bias voltage for lower etch rate. In this configuration a thick passivation layer is produced forming nanometric sized peaks that protect the surface of the Silicon in some regions from further ion bombardment, producing SiO_xF_y based nanostructures that can be columnar or cone shape depending on the cryogenic DRIE parameters. Figure 8.13 shows the black silicon patterns obtained during the cryogenic etching of the copolymer. It must be mentioned that these patterns are of smaller dimensions than previously observed in Chapter 8 and indeed more diminutive than typical black silicon patterns. For this purpose, we have coined the term '*nano-black silicon*' to refer to these patterns.

8.3.4. DRIE of copolymer – Bosch process

In this section, we focus on our experiments of Bosch DRIE on copolymer patterns. The Bosch DRIE process is an aggressive etch process with alternating cycles of depassivation, etch and repassivation steps [7, 8]. The process itself was discussed in detail in Chapter 6. The etch rates obtained on a regular Bosch process are ~1.5 µm – 4 µm per minute depending on the different parameters. Direct Bosch DRIE was attempted on the copolymer samples for reducing durations of 1 minute, 30 seconds and 5 seconds. In all cases, the copolymer film was destroyed probably due to the aggressive nature of the etching. Hence it was necessary to obtain

the patterns on silicon in a more durable material than the copolymer itself. We therefore attempted to perform a “lift off” process to obtain the copolymer templates in aluminium on silicon. Figure 8.14 shows a schematic illustration of the lift off process performed.

Block copolymer lift-off has achieved success in quantum dot applications [123] and nano pillars [124, 125]. We use aluminium as the lift-off material in our work owing to the high selectivity during DRIE and established etch recipes for the same. The aluminium layer has to be extremely thin (5-10 nm) to achieve lift-off. Dimethyl Formamide (DMF) was used as a solvent for PS to perform the lift-off. A standard Bosch DRIE process was used for etching. Table 8.4 lists the etch parameters. Figures 8.15 shows preliminary SEM results of (a) the 5 minute etch and (b) the sample after aluminium removal.

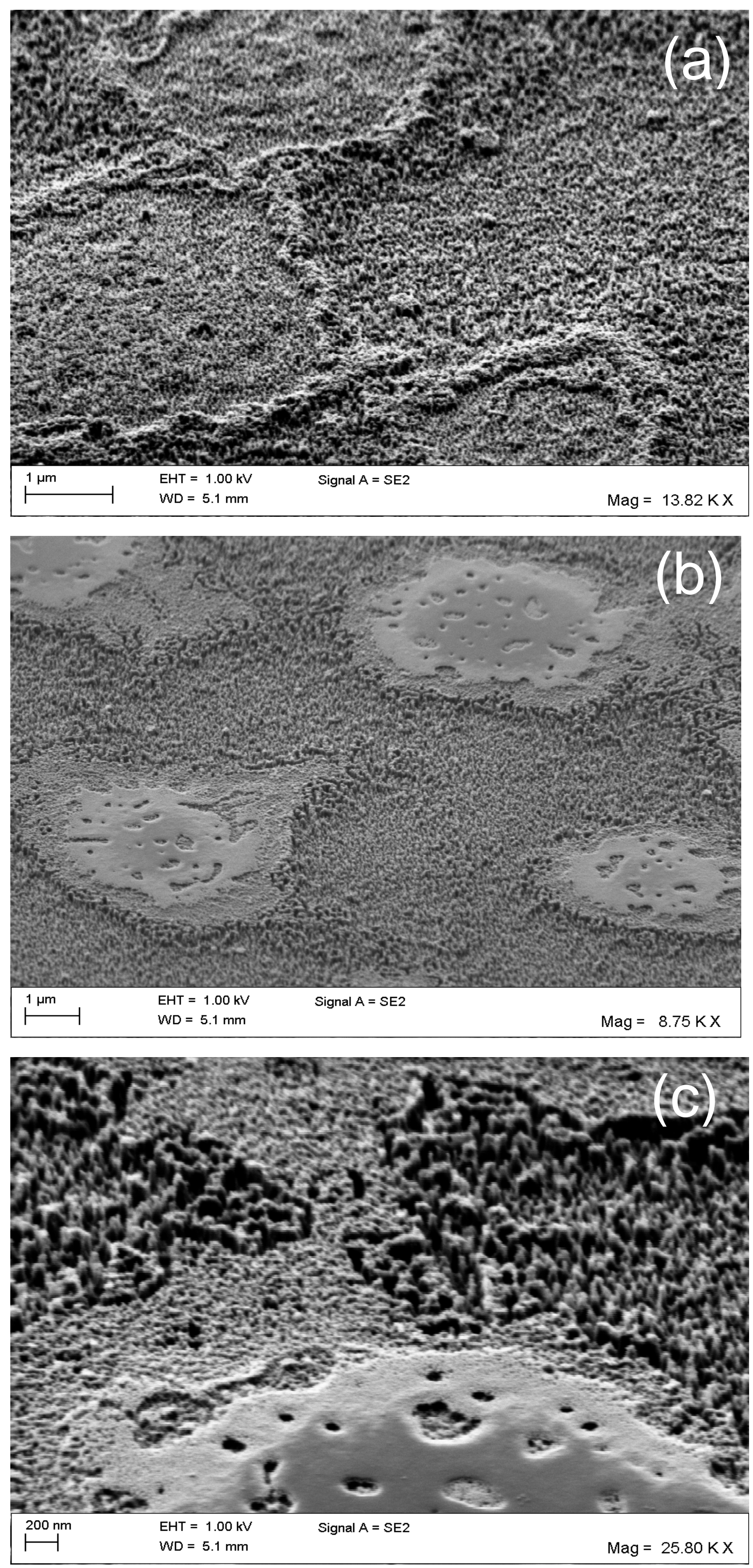


Figure 8.13. (a) "Nano-black silicon" (b) Polymer islands free of black Si and (c) Copolymer pattern-template for nano-black silicon peaks.

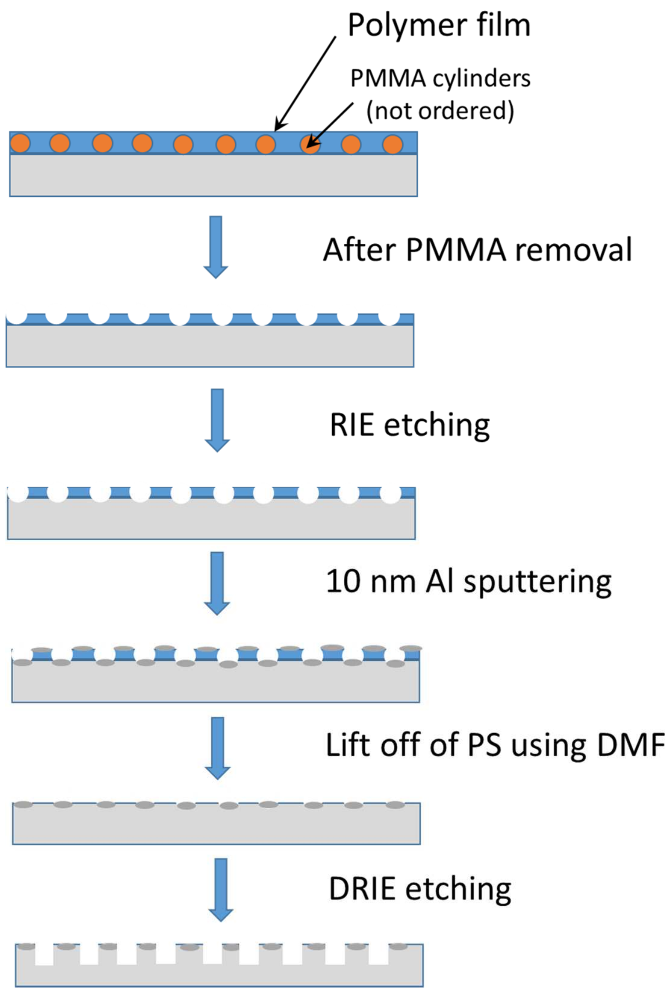
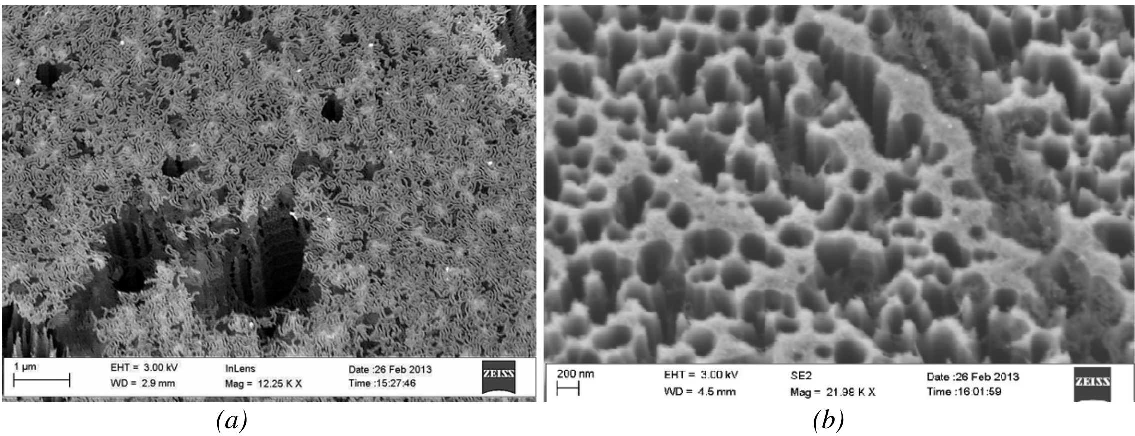


Figure 8.14. Schematic illustration of transfer of copolymer patterns to Al by lift-off.

Table 8.4. Bosch DRIE parameters for copolymer etching.

Source Power (W)	Pressure (mT)	Temperature (°C)	Duration of etch (mins)
1800	36	22	5

.



(a) *(b)*

Figure 8.15. SEM image of block copolymer DRIE (a) post Al-lift off and (b) after Al-etch.

As it can be observed from the above images, the lift-off is far from perfect. In fact whole sections of copolymer still remain on the surface without lifting off. This is possibly due to the aluminium layer being too feeble to lift off all of the copolymer. Thicker aluminium sacrificial layers need to be attempted in future. However, these preliminary results are encouraging as in Figure 8.15 (b), it is possible to observe that there are ~200 nm range holes etched through the silicon substrate. These are encouraging results and further experiments could possibly yield better results.

Black silicon formation

Etching of copolymer with the Bosch DRIE resulted in Black silicon peaks adjacent to the copolymer etched regions. Figures 8.16 (a-c) show the different SEM images of the black silicon obtained from the Bosch process. It is also interesting to note that this is 'typical' black silicon with peaks in the ~200 nm range and periodicity of ~400 nm unlike the 'nano' black silicon obtained in the previous section. One possible explanation for the reason for the formation of black silicon in a Bosch process could be the presence of dust in the plasma [126]. Dust is created when oxygen and silicon tetra fluoride (SiF_4 being the reaction product of silicon etching) coincide inside the plasma. This occurs in mixed oxygen plasma - the silica dust falls onto the wafer where it starts to form Black Silicon when directional etching occurs. Dust may also be caused to form when strong polymerizing gases are fed into the plasma, such as in Bosch DRIE. The particles, and consequently the Black Silicon, are observed to be limited when the SiF_4 and O_2 gases are time separated, which forms the basis of the proposed pulsed oxygen DRIE. More details regarding the process and properties of BS can be found in Appendix II.

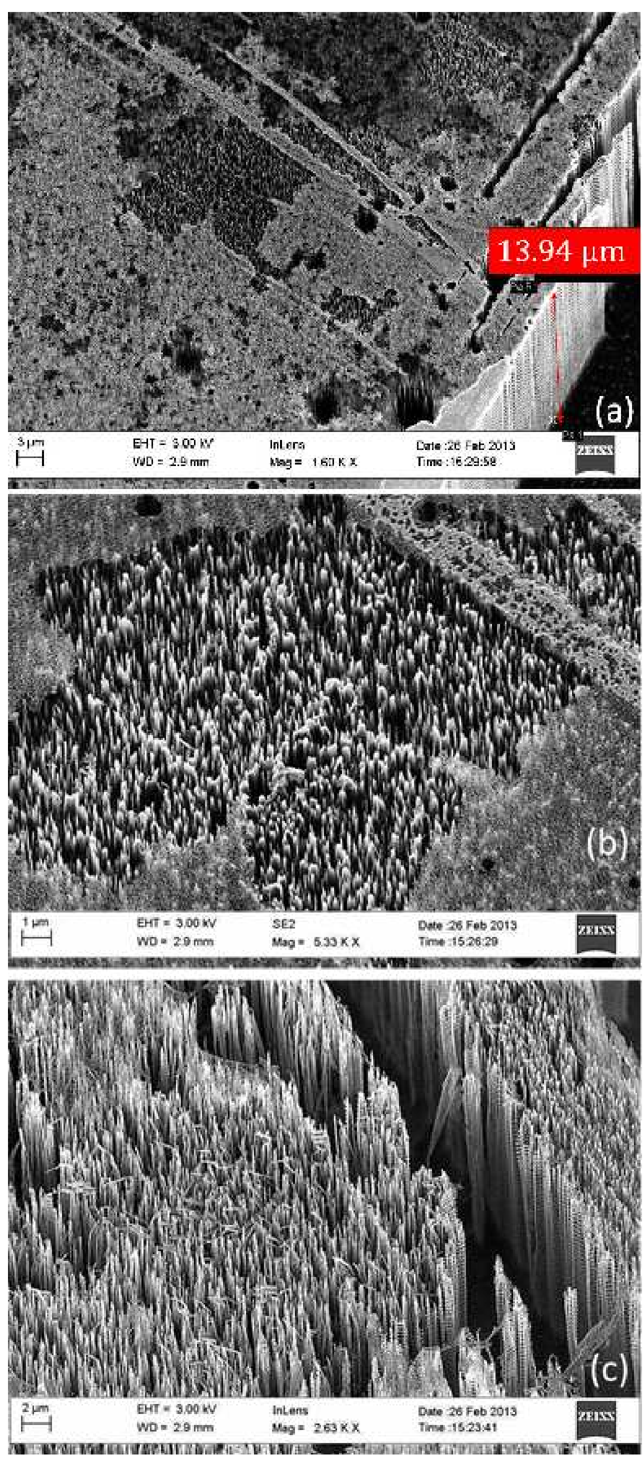


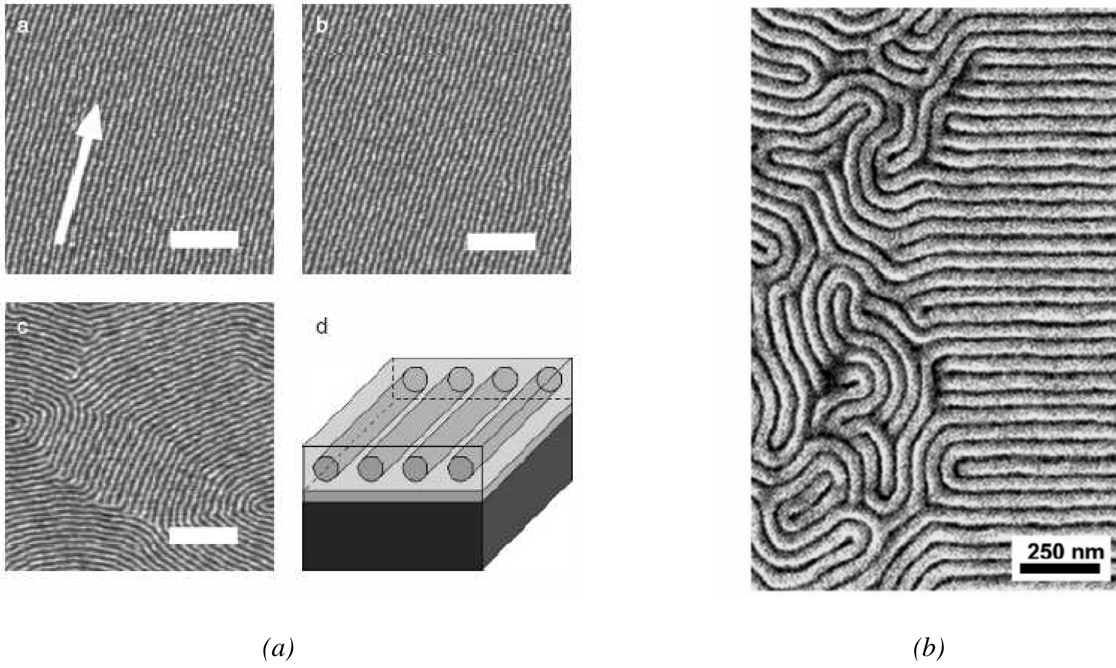
Figure 8.16. SEM images of (a) Black Silicon formed on the sample after Bosch DRIE, (b) seen alongside copolymer islands and (c) closer-up view of Black Si peaks.

8.4. Copolymer alignment experiments and perspectives

One of the ultimate goals of this project is to align the patterns obtained by the different block copolymers into straight lines. This has been done by a variety of methods in literature –

- Using shear stress [127,128]
  - Applying a shear force in a coplanar direction over the block copolymer (See Figure 8.17 (a)).
- Using an electric field [129, 130]
  - Using metallic pads over the BCP and applying an electric field across the pads forcing the copolymers to align in the direction of the electric field.
- Using an imaging layer [131]
  - A chemical layer that is grafted upon the native oxide on the wafer (hydroxyl-terminated polymer brush or a self-assembled trichlorosilane monolayer) [132]. Since the imaging layer is chemically homogenous, when the BCPs are deposited on them, they assume the form of no long range order and hence stretch out perpendicular to the surface (See Figure 8.17 (b)).

Examples from the resultant experiments are shown in Figure 8.14 (a) and (b).



(a) (b)

Figure 8.17. Alignment of block copolymer by (a) Shearing technique [128] and (b) using an imaging layer [131].

8.4.1. Electric field alignment

During the course of this work, we attempted to align the block copolymer patterns by employing the use of electric field and also by shearing. For using electric field, a mask was designed with metal pads for applying the electric field and electrodes in between them where the polymer is expected to align. These electrodes vary in dimensions from 2 to 32 µm so as to vary the strengths of the field applied. The schematic of a 'single cell' this setup is shown in

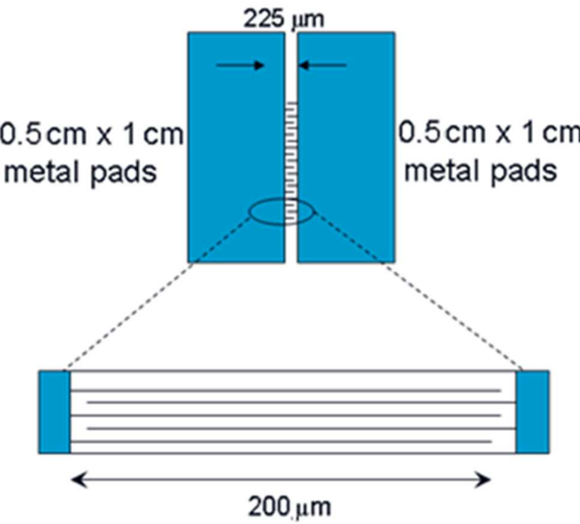


Figure 8.18.

Figure 8.18. Schematic of a single "cell" of the electric field layout. The electrodes in between the pads vary in dimension from 2 µm -32 µm.

Results

We first created the electric pads by photolithography using a 500 nm layer of Aluminium for patterning. Diblock copolymer was then spin coated as described in previous sections. The Al pads were cleaned with toluene and their electrical connectivity was confirmed through a multimeter. We then applied electric fields of $2 - 31\,V$ on the metal pads for a period of 8 hours whilst annealing. The setup was not in vacuum. However, instead of aligning, the samples all dewetted. Dewetting is the process by which an initially uniform film of liquid on a non-wetting substrate breaks up into droplets. Since we were unable to keep the setup in vacuum as it annealed, we decided to pursue shearing to try and align the BCP patterns.

8.4.2. Shearing alignment

A shear stress is a force applied in a coplanar direction to the cross-section of a material. The shear setup used in this work for attempting to align the block copolymers is modelled on the setup used by D.E. Angelescu et al [111, 128] in their work. . Figure 8.19 shows the schematic of the setup used in the laboratory to do shearing. To this end, a 1 cm x 1cm x 0.4 cm PDMS "stamp" was created (Dow Corning Sylgard 184) and cured for 1 hour at 80°C. The copolymer sample was placed beneath this stamp creating an airtight "seal". This was placed on a programmable hot plate.

Direct stress was applied to the sample using an aluminium weight. Using a pulley and stage setup, shear stress was applied across aluminium rollers. The annealing cum shearing of the sample occurred over a 4 hour period.

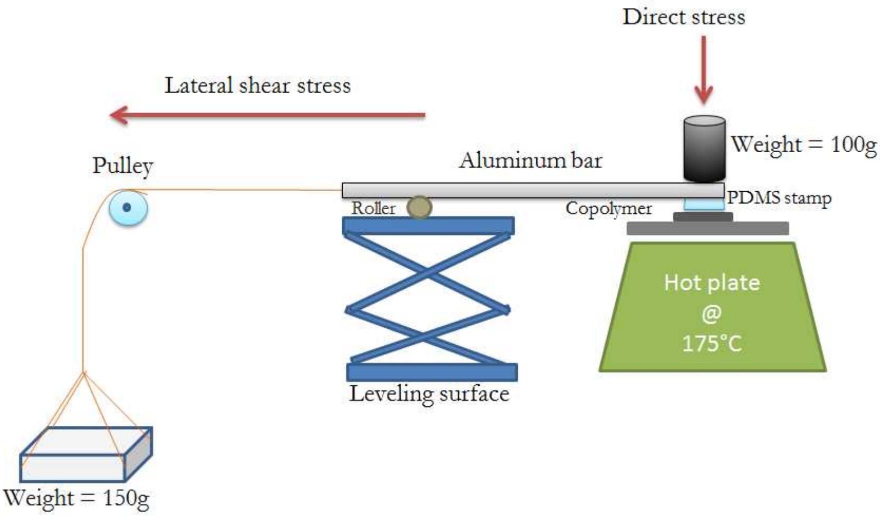


Figure 8.19. Illustration of the shear setup for aligning block copolymer.

Preliminary results

Initial results from the shearing experiments resulted in peeling off of the polymer layer possibly due to the stress from the combined weights added. Figure 8.20 shows a SEM image of one of these attempts. However even after altering the weights sufficiently, we weren't able to obtain a perfectly aligned BCP pattern. We then tried to isolate the chamber where the copolymer sample was placed. For this purpose, we created a make-shift bell-jar of sorts. The schematic of the modified setup is shown in Figure 8.21. However this didn't result in anything

better either. The setup needs to be entirely in vacuum or flooded with nitrogen or both. Perhaps this would then create the right conditions for the BCP samples to be shear aligned.

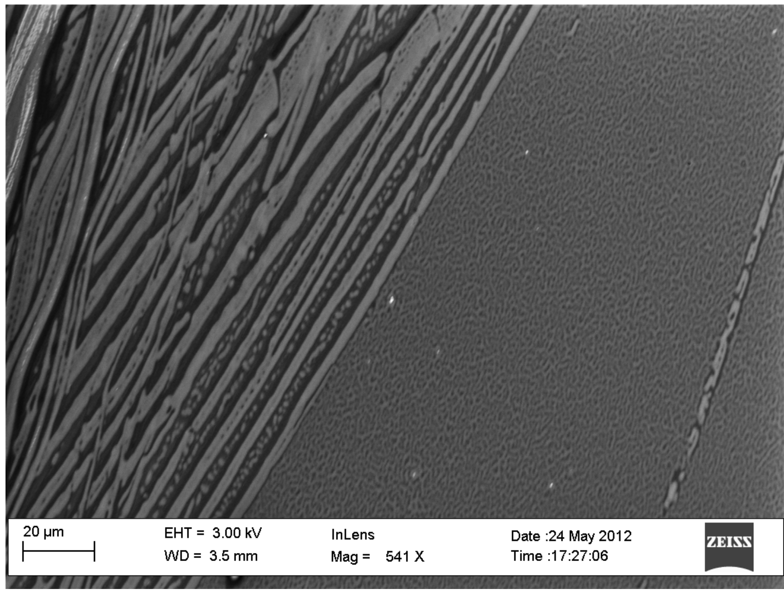


Figure 8.20. Peeled off layers from excessive stress during shearing of PS-PMMA.

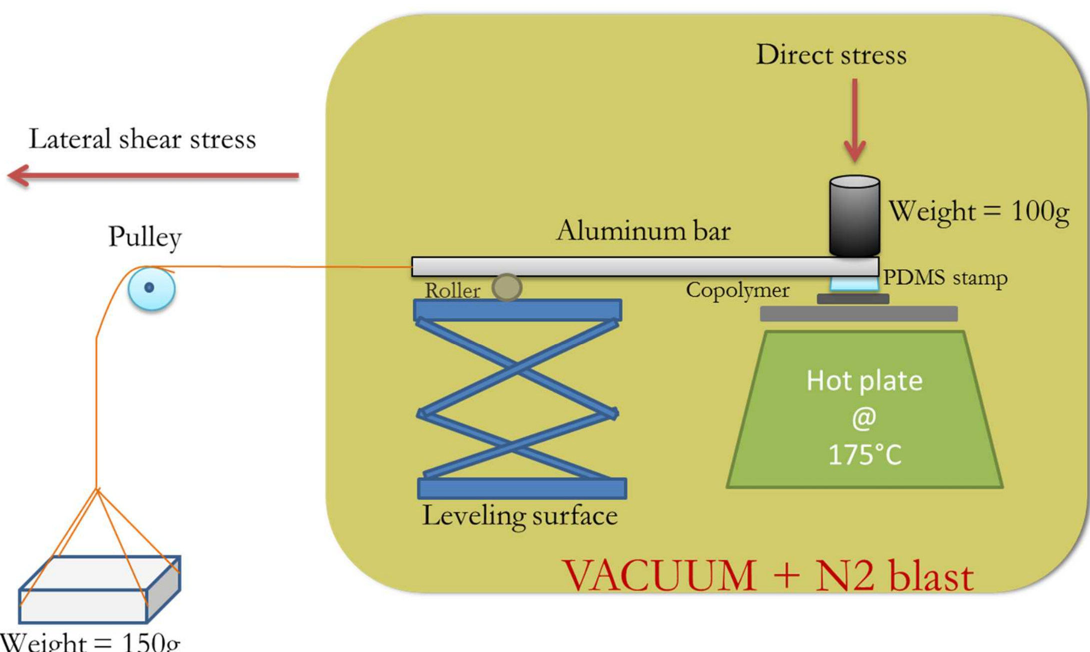


Figure 8.21. Modified shear alignment setup.

8.5. Conclusions and perspectives

The work done with diblock copolymers in this thesis has yielded promising results. The pattern transfer using the bottom-up approach yielded very promising first results and further experimentation using different techniques will help to improve the results achieved through this work. Depths of ~14 µm were achieved to obtain HAR nanostructures of widths ~200 nm through the block copolymer pattern transfer. However the lift-off wasn't entirely successful due to the bulky (~15 nm) aluminium film. Reducing the thickness of the Al film will likely result in better patterns and true transfer of the range of sub-50 nm patterns on to the substrate.

Another main area of work that can be done is to achieve successful alignment of the copolymer by using one of the above described techniques. Whilst our experiments in the given time frame did not yield actual success, the outlook is promising. As a next step, Ruthenium staining can be used to selectively "stain" the PS domains alone [133-135]. This could prove useful to conduct further experiments to visualize the two blocks of the copolymer distinctly.

Conclusions
End of Part II

The last few chapters have detailed the different techniques for attaining high aspect ratio micro and nanostructures in silicon with dimensions extending from tens of nanometers to hundreds of nanometers. The technologies corresponding to these achievements have ranged from conventional lithography mask-based patterning to various techniques in the *bottom-up* realm of microfabrication. We have achieved extremely high aspect ratios using DRIE etching with success in both Bosch (160:1 for 250 nm trenches) and cryogenic processes (120:1 for 35 nm trenches).

With the need for smaller patterns with more precise engineering many bottom-up techniques are being fashioned from a variety of materials to attain self-assembly in the range of nanometers on different substrates. In this part of the thesis, we have detailed our forays into this area of research by working with a focus on nanofibers and with diblock copolymer lithography to pattern the silicon substrate for further transfer into silicon to achieve HAR structures.

However there are still many more interesting procedures which are worth considering and which can result in the formation of HAR nanostructures. These include the use of porous alumina formed by self-organized anodizing; self-assembled nanocrystals using opals and the use of black silicon as masking templates to create patterns on silicon that may be further etched by optimizing one of the DRIE procedures discussed in this thesis.

Part III of this thesis describes some of these techniques in brief, their synthesis and the approach to obtain nanopatterning using them. These techniques and procedures form the perspectives to the work done in this thesis and can be realized in future to attain the goals aforementioned. Part III of this thesis also makes a summary of our results together with the most promising prospects, in order to better visualize the whole picture towards achieving our ultimate goal of realization of the targeted vertical nano-super-lattices.

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Part III-

Perspectives, future work and conclusions

Chapter 9

Conclusions and Perspectives - Other *bottom up* approaches

9.1. Introduction

In Part II, we described in detail some of the *bottom up* techniques that we have used in this work to fabricate HAR micro and nanostructures in silicon. However there are still many other techniques that also fall into this category of microfabrication which combine traditional microelectronics and surface engineering for self-assembly. We created forays into attempting to fabricate some HAR micro and nanostructures using some of the techniques discussed in the following sections. However due to limited time and resources at this time, we consider this part of the work incomplete and something that can be taken up in future.

9.2. Porous alumina formed by self-organized anodizing

With new lithographic methods sparking from a variety of material, the spotlight is on synthesizing self-organized nanostructured materials with possible periodic arrangements. Over the past few decades, anodizing of aluminum has raised interest due to its diverse applications including dielectric film production for use in electrolytic capacitors, decorative layers by incorporation of metallic or organic pigments, etc. Porous alumina in the form of self-ordered hexagonal arrays of cells containing cylindrical pores has been studied more than three decades [1-4]. The pore formation mechanism during anodization is not yet fully understood. However, research has been extensively conducted in this area to understand its formation [5-9].

9.2.1. Fabrication

Porous alumina templates can be fabricated from bulk aluminium or from deposited aluminium on desired substrates depending on the application [2, 5, 7-9]. In principle, one can create nanohole arrays on an area that depends on the size of the desired material over relatively large areas, for instance, even over a 100 mm substrate. There are four key advantages to using porous alumina as a basis for nano-patterning – the nanometric proportions of the pores,

possibility to control the size of these pores over large areas achievable by varying the oxidation conditions, their high aspect ratio and highly organized nature of the pore arrays. Additionally, they have very high resistivity (upto 10^{18} Ω cm^{-1}), optical transparency over a wide spectral range, and chemical robustness [10-12].

Porous alumina has a honeycomb structure of fine channels characterized by a closed-packed array of columnar hexagonal cells, each containing a cylindrical pore at the center, as shown in Figure 9.1. Pore diameters ranging from below 30 to 400 nm, oxide thickness from 0.3 to 200 µm and pore densities in the range 10^{9}-10^{11} cm^{-2} can be obtained. The size and interval can be easily controlled by changing the processing conditions.

Porous alumina templates are grown gradually in acid baths that work continuously by anodizing aluminium under the electric field between two electrodes. Various electrolytes have been employed for the anodization process such as sulphuric acid (H_2SO_4), oxalic acid ($H_2C_2O_4$) and phosphoric acid (H_3PO_4) yielding different pore diameters and interpore distances. Variation in the applied voltage can also modify the characteristics of the template formed. Some typical results are summarized in Table 9.1 [13, 14].

Table 9.1. Comparison of porous alumina characteristics with different electrolytes.

Electrolyte	Pore diameter (nm)	Inter-pore distance (nm)	Voltage (V)
H_2SO_4	30-35	60-70	25-27
$H_2C_2O_4$	40-100	80-200	30-80
H_3PO_4	130-250	250-500	100-195

The actual fabrication process involves immersing of high purity (99.999%) aluminium foils are into the chosen electrolyte. The pores then propagate through the surface of aluminium. To get self-ordered nanohole arrays, a two-step anodization process is introduced. Masuda and Fukuda [15] reported that the pore regularity can be improved by a long anodization time under appropriate conditions. They described that, after stripping away the thick oxides obtained from the first long anodization, a thin alumina film with highly ordered pores can be obtained by a subsequent re-anodisation, as shown in Figure 9.2 [16].

During the self-assembly process, the pores initiate at random positions and order thereafter by self-adjusting during an anodizing process of long duration. The pore arrangements on the surface are generally disordered and have a broad size distribution. Ordered pore domains can only be obtained at the bottom of the layers. Hence, the pores produced in the first anodization step are not parallel to one another. To fabricate ordered nanopore arrays, the first porous oxide film (see Figure 9.2 (a)), which contains the barrier

layer at the bottom, has to be removed by wet chemical etching. The barrier layer is not flat but consists of periodically arranged crests and troughs. These fluctuations result in a dimpled and undulating surface that has the same spatial ordering as the barrier layer. After the removal of the porous film, the periodic concave patterns that remain, as shown schematically in Figure 9.2 (b), act as a self-assembled template for the second anodization process. An ordered nanopore array is obtained during the second anodization if the same parameters are used as in the first anodization step. The periodicity of an ordered nanopore array is demonstrated in Figure 9.2 (c). Finally, the rest of aluminium is removed by wet chemical etching to get ordered porous anodic alumina layer as show in Figure 9.2 (d).

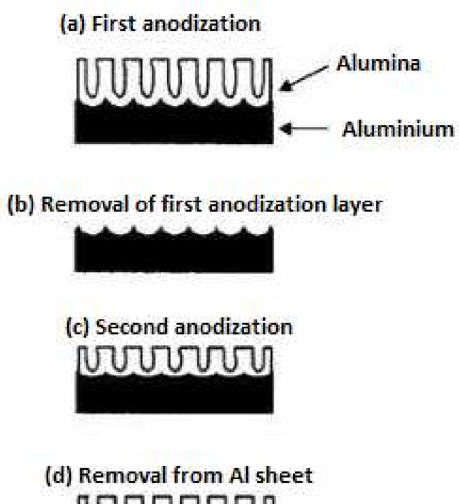


Figure 9.1. Two-step anodization process for fabrication of porous alumina.

9.2.2. Porous alumina sample results

Figure 9.2 (a) and (b) show SEM images of the porous alumina structure in (a) top view and (b) cross-section [16]. The highly ordered structures in hexagonal formations are clearly visible.

9.2.3. Conclusions

From Figure 9.3 (b), we can see that the cross section of the porous alumina shows extremely straight columns formed during the anodization process. From the point of view of the ultimate goal of this work to create vertical superlattices in the nanoscale, these structures will be extremely suitable. Their ease of manufacture and the well-developed techniques make this option extremely attractive to work with to create thermal devices in the nanoscale.

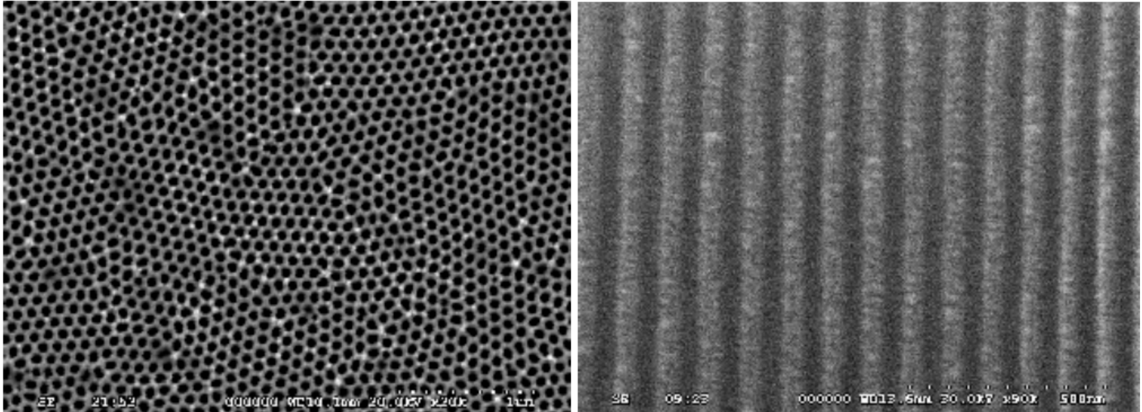
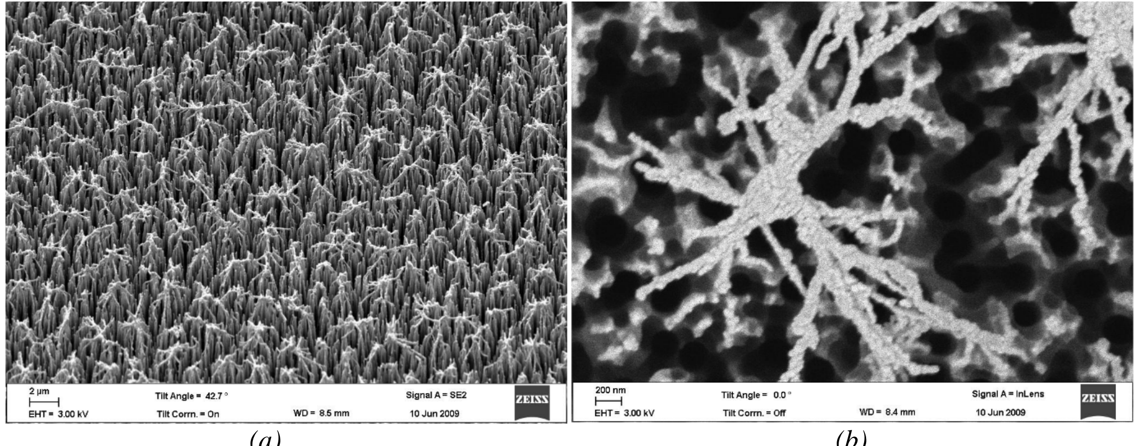


Figure 9.2 SEM images of porous alumina in (a) Top view and (b) Cross-sectional view

9.3. Black silicon templates as mask

As described in previous chapters of this thesis, we have reasonably good experience in producing black silicon from a variety of initial substrates using both Bosch and cryogenic processes. We have obtained a wide variety of black silicon substrates with patterns of the range of 200 nm – 200 µm peaks with a period of 250 nm – 2 µm depending on the type of black silicon we obtain – normal or 'nano' as described in Chapter 8 and Chapter 9 of this work. Additional information on the fabrication process and applications of black silicon can be found in Annex II of this thesis.

After obtaining BS, we deposit a layer of aluminium by sputtering which settles on the peaks and can act as a mask for further etching. The aluminium used in our experiments is ~100 nm in thickness and can act as a mask for further DRIE etching. Figures 9.3 (a) shows a SEM image of black silicon with Al on top and (b) closer up image of the black silicon peaks with Al netted on top. The peaks shown in our results are ~220 nm in diameter with periods of ~1 µm.



(a) *(b)*

Figure 9.3. SEM images of (a) black silicon with aluminium on top and (b) closer up view.

With our experience in DRIE, we hope that it will be possible to replicate templates such as these to act as masks for further DRIE to produce HAR micro and nanostructures in silicon. This is a viable option for future work to attain the ultimate goal of producing materials with better thermoelectric properties, especially since black silicon is an excellent material for photo absorption.

9.4. Synthetic opals fabricated by Langmuir-Blodgett – as masks

9.4.1. Langmuir-Blodgett films

A Langmuir-Blodgett film consists of one or more monolayers of an organic material deposited from the surface of a liquid onto a solid by simple immersion [17, 18]. A monolayer is adsorbed homogenously with each immersion step and therefore films of very accurate thicknesses can be formed. This technique is very promising because it enables (a) precise control over the thickness of the films deposited, (b) homogenous deposition over relatively large areas, (c) possibility of making multilayer structures with varying layer compositions and (d) possibility of depositing monolayers over any kind of substrate [19].

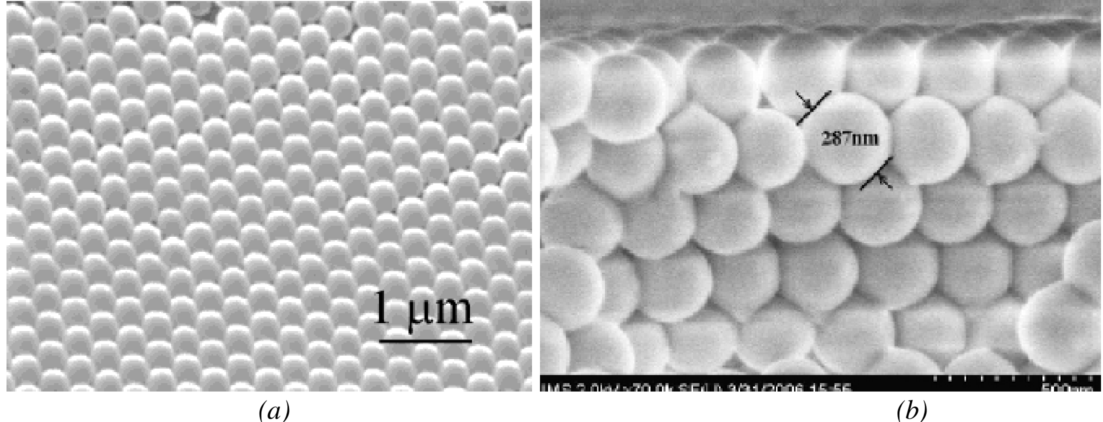
9.4.2. Fabrication of synthetic opals

Opals are either amorphous or poorly crystallized varieties of silica containing a small amount of water. Typically synthetic opals are almost always produced by the methods pioneered by Stober, et al. [19]. The process involves hydrolysis of tetraethyl orthosilicate (TEOS) using ammonia as a catalyst and ethanol and acetone as solvents [20-22]. The reactions are controlled in glass flasks at room temperatures. Subsequently alkyl silicate is added and stirred by a magnetic stirrer. This initiates an invisible hydrolytic reaction forming silicic acid which then condenses over a short time indicated by the opalescence of the solution. This is followed by a succession to a turbid white suspension occurring over the next few minutes. Samples for observation are simply immersed in this suspension [21].

9.4.3. Sample results

Figures 9.4 (a) and (b) show sample results obtained by [22] and [24]. Opals of 300 nm and lesser have been fabricated through these methods. Typically synthetic opals are used in photonics as photonic crystals and for diverse applications in optoelectronics [22-24]. However as a means to reach the final goal of this work, we propose the use of these synthetic opals as a

mask for subsequent DRIE. Since the opals are silica, which acts as a good mask during DRIE, these opals could act as a template to achieve HAR nanostructures in silicon.



(a) (b)

Figure 9.4. SEM images of opals obtained by L-B method by (a) M.Bardosova, et al [22] and (b) J. F. Dechézelles, et al. [24].

9.5. Nanosuperlattices

In this work, we have achieved a first step towards achieving nanosuperlattices in silicon – the creation of HAR nanostructures in silicon. However, there remain a few more process steps that need to be realized in order to obtain these nanosuperlattices in silicon which can then act as an effective thermoelectric metamaterial, thus realizing the ultimate goal of this work. Figure 9.5 is a schematic of the fabrication steps that need to be performed to realize nanosuperlattices in silicon.

Atomic Layer Deposition (ALD) is a thin film deposition technique based on the use of a sequential gas phase chemical process. In microfabrication, ALD is to deposit conformal thin films that can be accurately controlled to obtain layers as thin as 10 pm per cycle of deposition [25-28]. With ALD it is possible to deposit a wide variety of materials, ranging from metals like Pt, Ru, Ir, oxides (Al_2O_3, TiO_2, etc) to nitrides(TiN, TaN, etc). The number of cycles of deposition determines the thickness of the film deposited. For nanolayer dimensions, the 'slowness' of ALD may not be a limiting factor.

Realizing these fabrication steps to achieve nanosuperlattices through one of the various methods of nano-patterning that have been discussed over the past few chapters; characterizing them using 3ω or 2ω measurements and measuring their thermal properties are the future perspectives from this work.

An example of ALD deposition to fill nanotrenches is shown in Table 9.2.

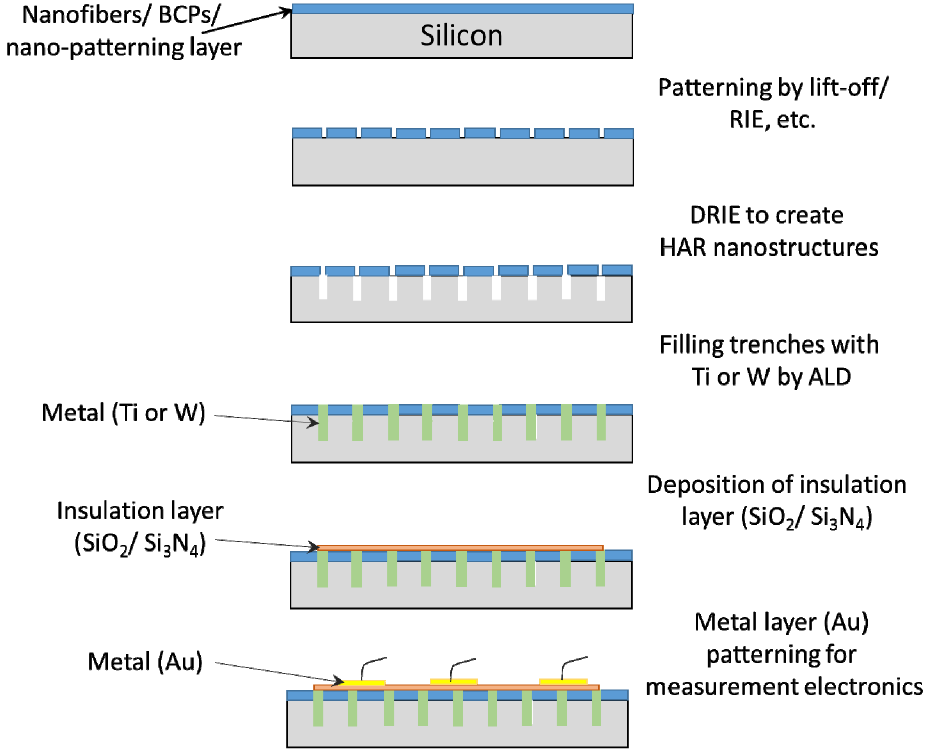


Figure 9.5. Schematic of the fabrication steps required in the realization of nanosuperlattices.

9.6. Summary of results

Table 9.2 offers a summary of the results achieved in terms of HAR micro/nanostructures through this work and the possible future prospects and direction to obtaining HAR nanostructures in silicon which can then be used to achieve nanosuperlattices. This table includes a summary of etching results obtained for different ranges of dimensions in an effort to construct the nanosuperlattices. Following this creation of trenches, the final realization of the nanosuperlattices will be as discussed in the precious section.

Table 9.2. Summary of HAR results achieved in Silicon with possible future direction of work to achieve nanosuperlattices.

Micromaching technique	Width of openings	Depth of trenches	Aspect ratio	Realized?	Sample image	Trench filling
Top down approach						
Photolithography + DRIE	15 µm	105 µm	6.5:1	Yes		Electrodeposition (Cu) - realized.
Photolithography + DRIE	5 µm	105 µm	21:1	Yes		Electrodeposition (Cu) - realized.
Photolithography + DRIE	800 nm	~100 µm	124:1	Yes		Electrodeposition (Cu) - can be done.
Photolithography + DRIE	250 nm	~36 µm	~144:1	Yes		Possible trench filling by atomic layer deposition (ALD) - prospects.

Bottom up approach						
Electrospinning + DRIE	~850 nm	~34 μm	~40:1	Yes		Possible trench filling by atomic layer deposition (ALD) - prospects.
Diblock copolymer lithography	~180 nm (possibly down to 30 nm)	~14 μm	~40:1	Yes		Possible trench filling by atomic layer deposition (ALD) - prospects.
Future prospects						
Synthetic opals on Si as mask + DRIE [22]	< 300 nm	Future work		No		Possible trench filling by atomic layer deposition (ALD) - prospects.
Black silicon surface tempering with Al mask + DRIE	180 nm - 2μm	Future work		No		Possible trench filling by atomic layer deposition (ALD) - prospects.
Porous alumina mask + DRIE	30 nm - 300 nm	Future work		No		Possible trench filling by atomic layer deposition (ALD) - prospects.

Example of Atomic Layer Deposition filling of trenches	
MSELS4700 5.0kV 5.2mm x 150k SE(U) 3/31/2004 22:31 300 nm	Sub 100 nm trenches filled by ALD [26]

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Appendix A
Basic Thermoelectric Principles

A.1. Seebeck Effect

In 1821, Thomas Johann Seebeck performed experiments showing that when a temperature difference was applied and maintained at the junction of two dissimilar metals, an electromotive force was created. This is illustrated in Figure A.1 (a) [1]. This phenomenon has come to be known as the Seebeck effect. To understand the physics behind this phenomenon, consider figure A.1 (b) [2] which is an illustration of the Seebeck effect with the electron charges and velocity distributions indicated. For the sake of simplicity, instead of the junction of two materials, the figure represents a single material.

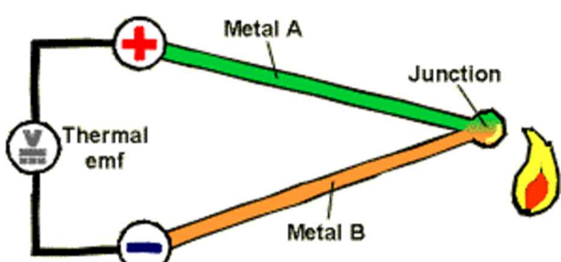


Figure A.1(a). Illustration of the Seebeck effect between two metals (reproduced from [1]).

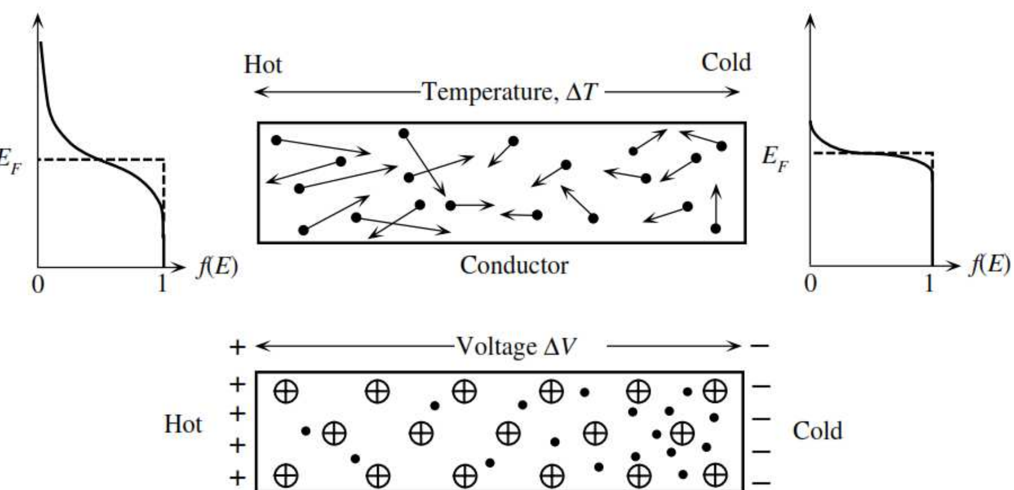


Figure A.1(b). Illustration of the physics of Seebeck effect. Sketch of electron velocities with longer arrows in the hot region, the corresponding energy distributions and the resultant equilibrium state, which leads to more electrons in the cold region, thus creating a voltage difference between the two regions (reproduced from [2]).

Consider that one end of this bar is maintained at a higher temperature than the other. The free electrons in the metal or the material behave in a manner similar to a gas. The kinetic theory of gases predicts that the free electrons in 'hot' side will have a higher kinetic energy and will move at greater speeds than those in the 'cold' side. As the faster moving electrons diffuse through the material, there is a net flow of hot electrons from the hot side to the cold side, resulting in an accumulation of negative charges at the cold side, preventing further charge build up and will continue to flow as long as the temperature gradient is maintained. The net result is that the imposed temperature gradient drives an electric current *if* the circuit is effectively completed. The electric field is proportional to the temperature gradient [2] and can be quantified by the *Seebeck coefficient* or *Thermopower, S.* It is defined as the potential difference developed per unit temperature.

$$S = \frac{dV}{dT} \qquad \text{(I.1)}$$

The sign of 'S' represents the potential of the cold side with respect to the hot side. If electrons diffuse from the hot to cold end, then the cold side is negative with respect to the hot, thus obtaining a *negative* Seebeck coefficient. In a *p*-type semiconductor, on the other hand, holes would diffuse from the hot to cold end which would in turn make the cold end positive with respect to the hot end, thus deriving a *positive* Seebeck coefficient.

Why dissimilar metal/materials?

In the previous section, we used the example of a single metal bar to understand the basics of the physics behind the Seebeck effect. Consider Figure A.2 (a) [5] which represents the physical process of moving the charge carriers within the conductor in the same direction as the heat. Figure A.2 (b) represents a circuit completion using the same conductor (metal). In this configuration, the flow of thermal energy will create equal potential for equal charge movements in both conductors, thus canceling out one another resulting in no potential output. On the other hand, consider Figure A.2 (c) which represents the completion of the circuit using two dissimilar metals or conductors. With *different* capacities for moving charge carriers in response to the thermal gradient, the current level in one conductor will overcome or complement the potential in the other, resulting in a continuous current flow across the two junctions provided the temperature gradient is maintained [5].

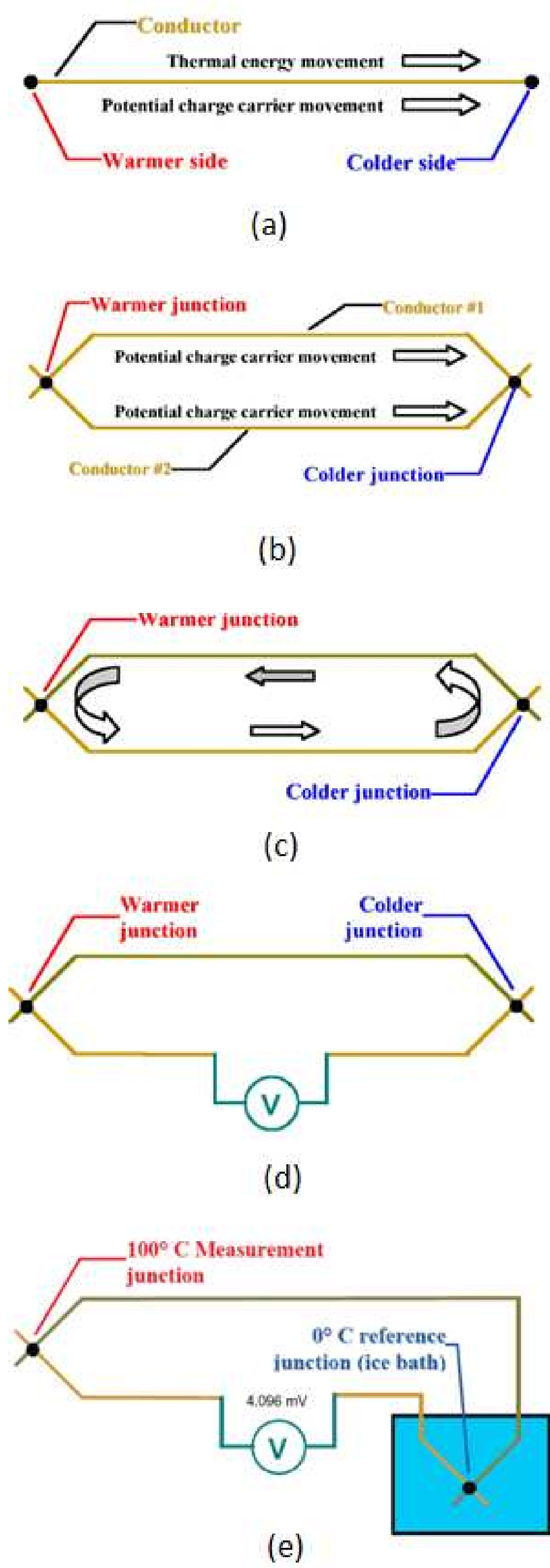


Figure A.2. Illustration of (a) capacity for charge carrier movement when excited by a thermal gradient, (b) similar conductors used to complete the circuit resulting in canceling out of net potential created, (c) dissimilar conductors employed to result in continuous flow of current in the closed circuit when the temperature gradient is maintained, (d) breaking the circuit allows for measurement of this voltage and (e) example of a thermocouple using a 0°C reference (reproduced from [5].

As shown in Figure A.2 (d), it is possible to break this circuit and connect a voltmeter across the ends to make a direct measurement of this potential difference. This is the *Seebeck voltage*. The best-known example of this phenomenon is the common thermocouple (see figure A.2 (e)) where two wires – one composed of a Ni-Cr alloy and one Ni-Al alloy are maintained at 100°C and a 'reference' of 0°C, a potential of approximately 4.096 mV is produced. It is a widely known fact that this voltage is a function of (a) temperature difference between the two junctions and (b) the nature of the conductors employed.

Figure A.3 represents the Seebeck effect at the junction of two dissimilar semiconductors (*n* type and *p* type as their majority charge carriers are different) [3].

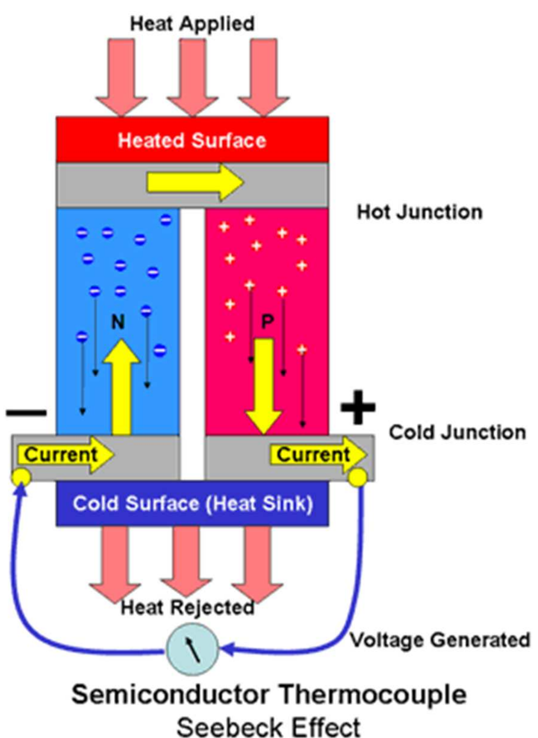


Figure A.3. Seebeck effect at the junction of two dissimilar semiconductors (reproduced from [3]).

Consider the heat being applied to the top of the semiconductor thermocouple shown in the above figure. The thermal energy causes charge carriers to be released into the conduction band, electrons in the *n*-type material and holes in the *p*-type material. The charge carriers concentrated at the hot side of the device will repel each other with the result is that they tend to diffuse towards the cold side of the device. In the *n*-type material this electron flow constitutes a current flowing from the cold side to the hot side and the movement of the electrons causes a negative charge to build up at the cold side with a corresponding positive charge on the hot side due to the deficit of electrons there. In the *p*-type material the migration

of the holes constitutes a current flowing in the opposite direction and a positive charge to be built up at the cold side and a corresponding negative charge at the hot side.

By connecting the junctions together with metallic interconnections as shown in the diagram above, a current will flow in an external circuit. The current generated is proportional to the temperature gradient between the hot and cold junctions and the voltage is proportional to the temperature difference. Heat must be removed from the cold junction otherwise the migration of the charge carriers will equalize their distribution in the semiconductor eliminating the temperature difference across the device causing the migration and hence the current to stop.

A.2. Thermoelectric Figure of Merit

The dimensionless quantity *ZT* refers to the figure of merit [4] of a thermoelectric material which is very useful in determining its efficacy in thermoelectric applications.

$$ZT = \frac{\sigma S^2 T}{\lambda} \tag{A.2}$$

where, σ is electrical conductivity of the material; λ, its thermal conductivity; *S*, the Seebeck coefficient of the material and *T*, the temperature of the device. As discussed earlier, an ideal thermoelectric material would thus have a high electrical conductivity to minimize Joule heating, low thermal conductivity to prevent thermal shorting and a high Seebeck coefficient to maximize the conversion efficiency between heat and electricity.

A.3. Peltier Effect

The Peltier Effect is perhaps the most important of the thermoelectric effects on a material when it comes to the description of the “heating or “cooling” effects, which have been used in the principle of thermoelectric generation or thermoelectric cooling. The Peltier effect is that in which a current flow induces heat flow and hence temperature difference between the 2 ends of the material. The direction of the heat transfer is controlled by the polarity of the current.

The principle of the Peltier effect is that when a voltage is applied across a semiconductor thermocouple, any surplus charge carriers present in the material (semiconductor) will be attracted towards the terminal with the opposite polarity. This is the mechanism of current flow through any conductor. Thus electrons in an *n*-type material

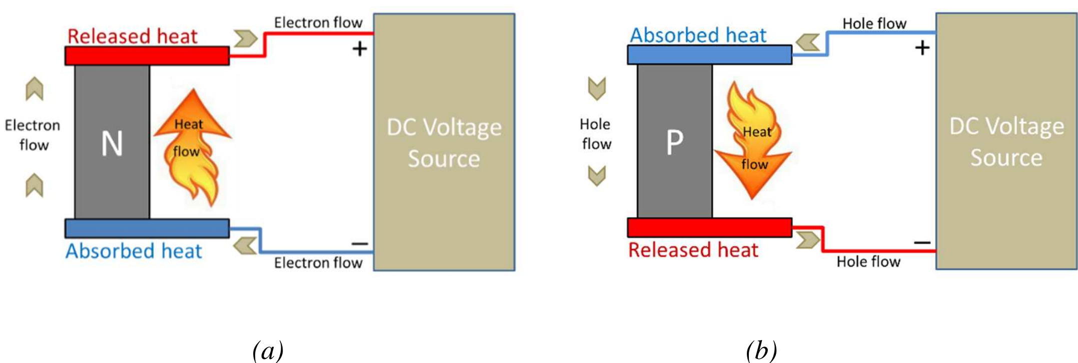
migrate towards the positive terminal causing a surplus to accumulate in the region of the semiconductor next to the terminal leaving a deficit at the negative side of the device. Similarly holes in the *p*-type material migrate towards the negative terminal. In simple terms, this means that the charge carriers are swept through the material accelerating as they do so, due to the electric field created by the voltage between the terminals of the device and the increased kinetic energy manifests as heat.

The temperature within the device depends on the number and the kinetic energy of the charge carriers. The temperature will therefore be higher in the region where the charge carriers are concentrated and lower in the region they have just vacated where charge density is consequently lower. Thus a temperature gradient, proportional to the magnitude of the applied current, builds up across the device. This temperature gradient can only be maintained however, if heat can be removed from the hot junction, otherwise the temperature will tend to equalize across the device and continued current flow will cause the device to overheat.

The heat absorbed or created at the junctions is proportional to the electrical current flow and the proportionality constant is known as the Peltier coefficient. Contrary to Joule heating (I^2R), the Peltier effect is reversible depending on the direction of the current.

Figure A.4 [5] is an illustration of the Peltier Effect in a (a) n-type material and (b) p-type material.

It is important to note that the heat will be moved (or 'pumped') in the direction of charge carrier movement throughout the circuit (actually, it is the charge carriers that transfer the heat).



(a) *(b)*

Figure A.4. Illustration of Peltier Effect in (a) n-type and (b) p-type material.

In Figure A.4 (a), an *n*-type semiconductor material is used to fabricate the device so that electrons (with a negative charge) will be the charge carriers when the Peltier effect is induced. With a DC voltage source connected as shown, electrons will be repelled by the negative end of the supply and attracted by the positive end; this forces electron flow in a clockwise direction (as shown in the figure). With the electrons flowing through the *n*-type material from bottom to top, heat is absorbed at the bottom junction and actively transferred to the top junction—it is effectively pumped by the charge carriers through the material. Similarly, the *p*-type semiconductor has the "holes" as the charge carriers. The corresponding charge movement is shown in Figure A.4 (b).

Why are 2 materials required?

Though it is possible to make a simple thermoelectric device with a single semiconductor material, it is not possible to pump an appreciable amount of heat through it for it to be used in any real-world application. In order to give a thermoelectric device greater capacity, multiple materials are used together. The initial idea would be to simply connect them in parallel—both electrically and thermally—as shown in Figure A.5 (a). While this is possible, it does not make for a very practical device. The major flaw in this device is that the typical TE semiconductor will draw impractical amounts of current for a very low voltage. For example, a single unit in an ordinary TE device might draw 5 amps or more with only 60 mV applied. This becomes enormous when trying to make a practical device with thousands of individual semiconductor units.

On the other hand, should the semiconductors in series, such that they are thermally in parallel (i.e., pumping together in the same direction), we achieve a configuration as illustrated in Figure A.4 (b). While theoretically this is sound, the electrical interconnections between each unit introduces thermal shorting that significantly compromises the performance of the device. The obvious solution is to form a junction between semiconductors of opposing doping configurations and construct a series circuit which can keep all of the heat moving in the same direction. As shown in Figure A.6 (a), with the free end (bottom) of the *p*-type device connected to the positive end of the voltage supply, and the free end (bottom) of the *n*-type device similarly connected to the negative end of the voltage supply, we arrive at the ideal solution.

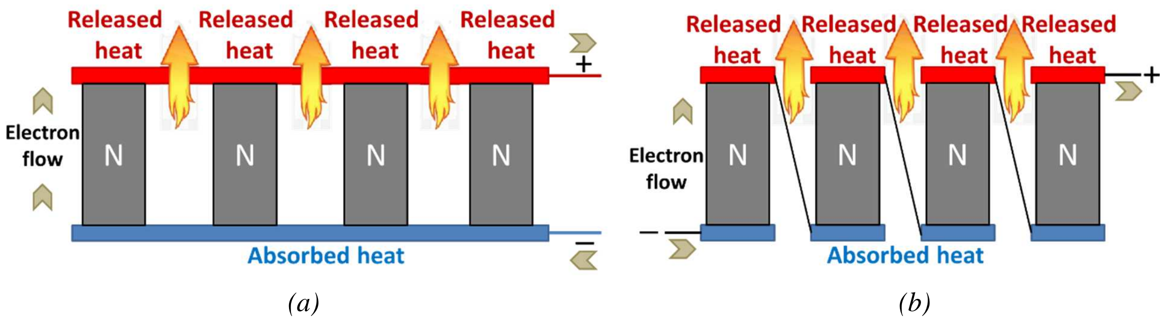


Figure A.5. Similar semiconductor material electrically connected in (a) parallel and (b) series. In both cases, they are connected thermally in parallel.

The positive charge carriers in the *p*-type material (i.e., holes) are repelled by the positive potential voltage and are hence attracted by the negative pole while the negative charge carriers (electrons) in the *n*-type material are likewise repelled by the negative potential and attracted by the positive pole of the voltage supply. Typical metal junctions wiring have electrons as the charge carriers. When these electrons reach the *p*-type material, they simply flow through the holes within the crystalline matrix of the *p*-type device. Thus the electrons flow continuously as a closed circuit from the negative pole of the voltage supply, into the *n*-type material, and then through the metal junction, and finally through the *p*-type device, and back into the positive pole of the supply. However, because of utilizing two different types of semiconductor material, the charge carriers and heat are all flowing in the same direction through the devices. Using these special properties of the thermocouple, it is possible to team many individual devices together in rectangular arrays to create practical thermoelectric modules. These devices can hence channel appreciable amounts of heat in addition to being very suitable for commonly-available DC power supplies because of their serial wiring. This is the currently used industrial method to connect different material types together to function in a coherent manner as a thermoelectric cooling device.

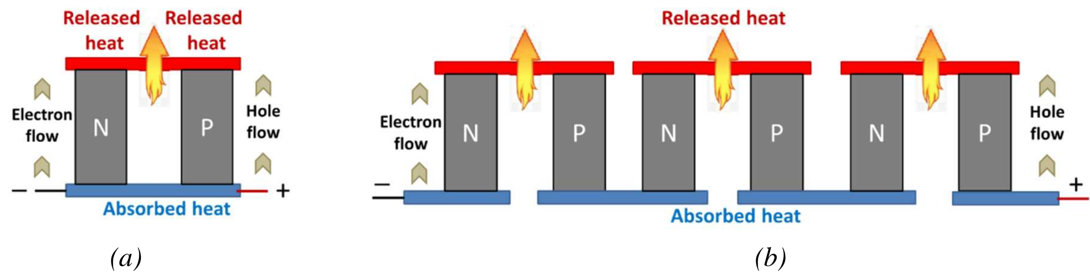


Figure A.6. Ideal configuration of semiconductor units (a) single pair and (b) in sequence.

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Appendix - B
Black Silicon

B.1. Introduction

Black silicon (BS) is a material produced by the surface modification of silicon and presents with very low reflectivity, and correspondingly high absorption of visible (and infrared) light. It was discovered in the 1980s as an unwanted side effect of reactive ion etching (RIE) [1, 2]. It has a needle-shaped topography where the needles are single-crystal silicon and have a height above 10 microns and diameter less than 1 micron. However by controlling process parameters, many variations of the surface geometry have been discovered. In this thesis, we have fabricated different types of BS as detailed in Chapters 7 and 8. The main feature of BS is an increased absorption of incident light—the high reflectivity of the silicon, which is usually 20–30% for quasi-normal incidence, is reduced to about 5% [3].

B.2. Fabrication parameters

Typically BS is manufactured using a cryogenic DRIE process. The temperature of the chamber is reduced to -110°C which slows down the chemical reaction that produces isotropic etching of silicon, which in turn allows the simultaneous use of the etching plasma (SF_6) and the passivation plasma (O_2). During the process, a passivating layer of SiO_xF_y forms on top of the silicon surface. With directional ion bombardment, the passivation layer is removed only in the desired direction (vertical for example).

For Black Silicon fabrication, the cryogenic process is adapted to a high passivation regime (high O_2 gas flow) combined with a low bias voltage for lower etch rate. What happens is that a thick passivation layer is generated, forming nanometric sized particles that protect the surface of the silicon wafer in some regions from the ion bombardment, producing SiO_xF_y based nanostructures that can be columnar or cone shape depending of the Cryo-DRIE parameters [4-6].

The fabrication of black silicon is relatively simple because the process is mask-less and the required etching time is of the order of a few minutes. Table B.1 shows an estimation of the range of the Cryogenic DRIE parameters in order to generate BS.

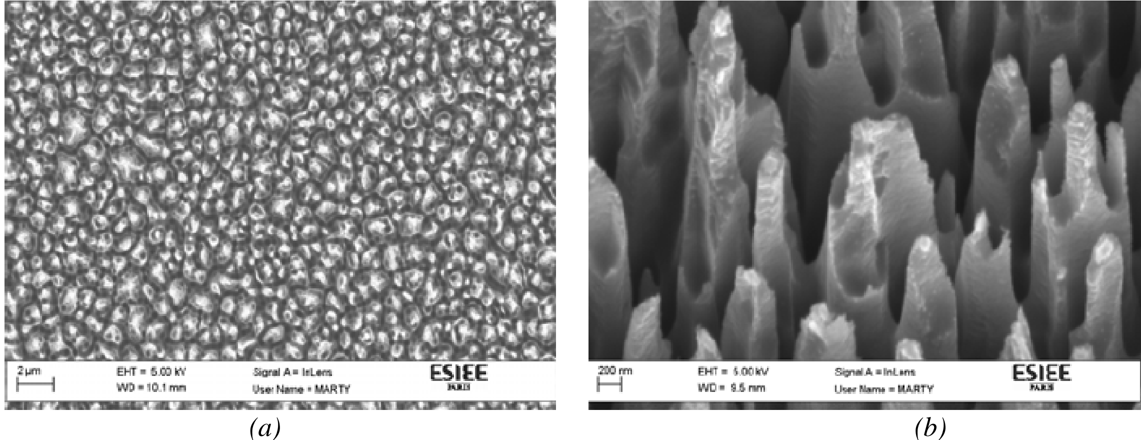
Table B.1. Range of cryogenic DRIE parameters for BS formation [4-6].

Etch parameter	**Lower limit**	**Upper limit**
Temperature (°C)	-160	-10
ICP (W)	350	2500
Bias voltage (V)	0	-50
Pressure (mTorr)	9	67
O2 flow (sccm)	6	28
SF6 flow	25	300
Time (min)	5	30

A lot of research has been done in our laboratory on Black Silicon and the fabrication parameters for producing different types of BS structures [7]. Table B.2 lists sample parameters for obtaining BS and Figure B.1 (a) and (b) are the corresponding SEM images of the top-view and side-view obtained from this recipe.

Table B.2. Sample parameters to achieve BS and their physical characteristics under SEM (reproduced from [7]).

DRIE Parameters	**Temperature (°C)**	-120
	ICP Power (W)	1000
	Bias voltage	-20
	O2 flow (sccm)	16
	SF6 flow (sccm)	200
	Pressure(Pa)	1.5
	Time (min)	10
Structure physical characteristics as measured under SEM	**Structure type**	Micro holes
	Structure mean height (µm)	2.54
	Structure mean diameter (µm)	0.3
	Aspect ratio	8.3



(a) *(b)*

Figure B.1. SEM images of (a) top view and (b) side view of BS samples from our lab (reproduced from [7]).

During the course of this work, we have also obtained BS through a traditional Bosch process. These results were discussed in Chapter 8. A possible reasoning for this occurrence in a Bosch process could be the presence of dust in the plasma [8]. Dust is created when oxygen and silicon tetra fluoride (SiF_4 being the reaction product of silicon etching) coincide inside the plasma. This occurs in mixed oxygen plasma - the silica dust falls onto the wafer where it starts to form BS when the directional etching occurs. Dust may also be caused to form when strong polymerizing gases are fed into the plasma as is the case in a typical Bosch DRIE process. The particles, and consequently the BS, are observed to be limited when the SiF4 and O2 gases are time separated, which forms the basis of the proposed pulsed oxygen DRIE.

B.3. Applications of BS

Photodetectors

Photodetectors are semiconductor structures which are able to receive and convert optical signals into electrical signals, based on the quantum photoelectric effect. Silicon based photodetectors are widely used for applications in which the operating wavelength range is between 300 nm and 1200 nm. However they have two basic limitations [9, 10] –

- ❖ Energy gap of the silicon (1.11eV), which if considering the relation between the photon energy and the transition energy in the structure, will result in a maximum detectable wavelength of around 1.11 µm.

- Low reflection coefficient - in the best scenario, a planar surface of silicon will absorb only 41% of the photon energy at 370 nm while it is almost transparent for wavelengths equal and greater than 1200 nm.

Black Silicon can be utilized to reduce the reflectivity and increase the performance of photodetectors based on silicon, by both increasing the absorption coefficient of the silicon and the wavelength range of detection for infrared applications.

Similar use of BS as an improved texturing method as opposed to silicon, are in the fabrication of photodiodes [11] and photovoltaic cells [12]. Additionally it is used in creating hydrophobicity of the silicon suface [13] for use in self-cleaning surface applications, etc.

B.4. Conclusions

As an unexpected result in this work, BS nevertheless has many promising applications especially in the field of optoelectronics and photodetectors. The obtained results from this work can be better characterized to achieve greater texturing of surfaces and better control over the surface morphologies of the BS peaks.

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Résumé Long

1. Introduction

1.1.Introduction

Avec la demande croissante de technologies énergétiques durables, la recherche dans le domaine a inévitablement connu un essor considérable et ce, depuis plus de deux décennies. Pour autant, les sources d'énergie renouvelables qui sont devenues désormais classiques (solaire, éolienne et géothermique) ne fournissent qu'une petite fraction de l'électricité consommée, principalement en raison de leur coût qui demeure relativement élevé mais aussi du fait de la limitation clé du gaspillage de chaleur comme un sous-produit [1-5]. Avec la possibilité de valoriser la chaleur, souvent laissée comme une source inexploitée d'énergie, il y a là donc un important potentiel économique et un vaste champ de recherche, en vue du développement de technologies rentables pour la production d'électricité à partir de la chaleur résiduelle, et ce à différentes échelles, y compris celles des composants et équipements électroniques, dont le fonctionnement donne lieu non seulement à de la consommation d'énergie électrique mais aussi à de la dissipation de chaleur. Cette dernière est par ailleurs souvent considérée comme un facteur limitant des dispositifs électroniques, qui se traduit par une dégradation de leur fiabilité et de leurs performances, de façon plus générale. Il y a donc un intérêt supplémentaire à réduire cet échauffement en captant la chaleur et par la même occasion, pour en produire de l'énergie électrique. Pour ce faire, les propriétés thermoélectroniques des matériaux vont jouer un rôle déterminant, puisqu'elles vont conditionner le rendement de conversion. Il est donc intéressant d'utiliser les matériaux présentant le facteur de mérite thermoélectrique le plus intéressant. Il est même tentant d'essayer de faire mieux que la nature, en concevant un méta-matériau présentant un facteur de mérite thermoélectrique encore plus élevé que ses homologues naturels. C'est l'objectif que nous poursuivons dans cette thèse, en vue de réaliser un tel méta-matériau, sous forme de super-réseaux verticaux résultat d'une nano-structuration du silicium.

Un dispositif thermoélectrique est constitué de deux matériaux différents reliés à leurs deux extrémités. Ils peuvent générer une puissance électrique lorsqu'ils sont soumis à une différence de température (effet Seebeck) ou produire une différence de température en utilisant une alimentation électrique (effet Peltier). Selon l'effet visé, le dispositif peut agir comme un générateur d'énergie électrique ou comme un réfrigérateur. Outre les applications

aux capteurs de température basés sur des thermocouples, les effets thermoélectriques ont donné lieu à une autre importante application exploitable de façon viable ; il s'agit de dispositifs à effet Peltier, utilisés à des fins de refroidissement à petite échelle ou de façon très localisée. Cette limitation est due principalement à leur rendement de conversion d'énergie modérée ainsi qu'à leur coût relativement élevé [1-5]. Dans ces applications, les dispositifs à effet Peltier présentent un réel avantage car les lois d'échelles des réfrigérateurs thermodynamiques classiques ne sont pas favorables à la miniaturisation, du point de vue du poids, du coût et de l'efficacité.

Traditionnellement, un bon matériau thermoélectrique est décrit en fonction de son facteur de mérite, *Z*, une grandeur sans dimension définie par :

$$ZT = \frac{\sigma S^2 T}{\lambda} \qquad (1)$$

avec, σ la conductivité électrique du matériau, λ, sa conductivité thermique; S, le coefficient Seebeck du matériau et T la température absolue du dispositif. Un matériau thermoélectrique idéal devrait donc avoir une conductivité électrique élevée pour minimiser l'échauffement par effet Joule, une faible conductivité thermique pour éviter un court-circuit thermique et un coefficient Seebeck élevé afin de maximiser le rendement de la conversion entre la chaleur et l'électricité.

Effet Peltier dans les jonctions métal-semiconducteur

L'effet Peltier dans les paires de semi-conducteurs de type *n* et *p* est à la base du concept de générateurs thermoélectriques et de refroidisseurs thermoélectriques. Pour autant, c'est l'effet Peltier dans les jonctions métal-semiconducteur-métal qui est le plus pertinent dans le cadre du présent travail. La Figure 1.1 [6] est une illustration d'une jonction typique métal-semiconducteur-métal (a) en configuration de semiconducteur de type *n* et (b) configuration de type *p*. Supposons que le flux de courant est dans le sens horaire. Pour que les électrons puissent entrer dans la bande de conduction du semi-conducteur à partir du métal de cathode, ils doivent surmonter la barrière d'énergie entre E_C et E_F. Seuls les "électrons chauds" ayant la plus grande énergie cinétique, sont susceptibles de surmonter cette barrière (par voie d'émission thermoionique). Ces électrons se déplacent dans le sens horaire et ne rencontrent aucun obstacle en entrant à nouveau dans le métal, ceci crée ainsi une déplétion de la cathode et un gain d'électrons chauds sur l'anode. Ainsi, un côté se réchauffe tandis que

l'autre se refroidit. Les mêmes concepts sont valables pour le matériau de type *p* pour lequel les porteurs de charge majoritaires sont les trous au lieu des électrons.

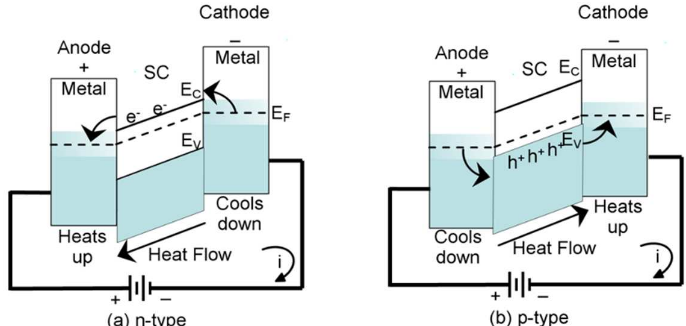


Figure1.1. Illustration d'une jonction métal-semiconducteur-métal typique ; en (a) la configuration de semiconducteur de type n et (b) de configuration de type p. [6]

Épaisseur de la barrière et l'émission thermionique

Les paramètres thermoélectriques sont améliorés lorsque l'épaisseur de couche semiconductrice est inférieure au libre parcours moyen des électrons. (~ 100 nm pour la plupart de semi-conducteur [7]). Afin d'assurer une émission thermionique, c'est-à-dire, en surmontant les barrières d'énergie, l'épaisseur de la barrière doit être supérieure à 10 nm à la température ambiante. Si la barrière est inférieure à 10 nm, il s'agit de l'*effet tunnel*, pour lequel les électrons traversent simplement la barrière plutôt que de la surmonter. Le seuil de l'émission thermionique et de la succession de barrières sont présentés dans la Figure 1.2 [7]. Il s'ensuit qu'une succession de barrières pourrait être mieux adaptée qu'un seul obstacle pour l'augmentation de l'émission thermo-ionique. Donc à partir des points énoncés ci-dessus, nous pouvons conclure que l'épaisseur de la barrière doit être comprise dans ce cas entre 10 et 100 nm.

Avoir une succession de barrières permet la dissipation de la chaleur par le décalage de bande et l'émission thermionique. Nous arrivons donc à la structure d'un super-réseau (voir Figure 1.3). Un super-réseau est un matériau hétérogène consistant en une structure de multicouches de deux ou plusieurs des matériaux avec par conséquent, une succession de barrières de potentiel, ce qui permet une meilleure conversion thermoélectrique que les matériaux naturels. La figure représente les différences entre les super-réseaux classiques et les super-réseaux verticaux proposés dans cette thèse. Cette solution permet une réduction du coût de fabrication ainsi qu'une fabrication en volume en utilisant seulement deux étapes, par

opposition aux méthodes conventionnelles, qui requièrent autant de dépôts de couches minces que nécessaire (typiquement plusieurs dizaines) pour l'obtention d'un super-réseau.

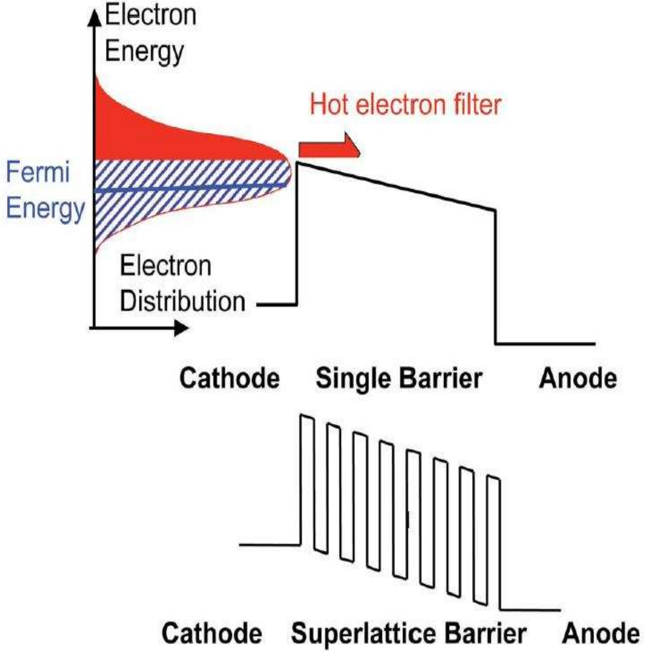


Figure 1.2. Représentation des seuils de barrière pour une meilleure émission thermionique.

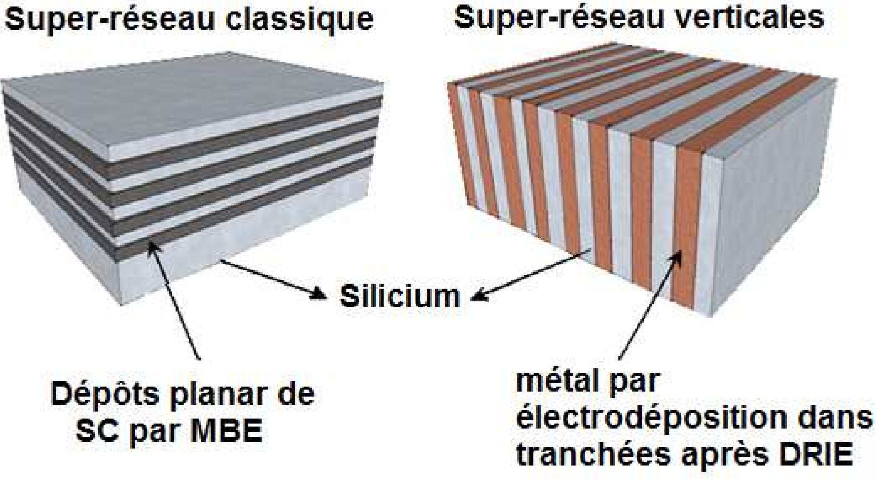


Figure 1.3. Structure de super-réseau de deux matériaux.

2. Fabrication de super-réseaux verticaux

Nous avons fabriqué des super-réseaux verticaux de taille micrométrique avant d'aborder la fabrication, beaucoup plus contraignante, des super-réseaux de taille nanométrique. Cette étape intermédiaire est d'une grande importance; elle a pour but l'extraction de paramètres physiques telles que la conductivité thermique, le pouvoir thermoélectrique du méta-matériau dénué des effets quantiques, mais qui sont susceptibles d'être présents à l'échelle nanométrique lors de la caractérisation des dispositifs [2-5]. A cet effet, nous avons fabriqué des super-réseaux de largeur de 5 µm et de 15 µm avec une profondeur de plus de 100 µm dans le substrat.

2.1. Choix des matériaux

Nous avons fabriqué les super-réseaux avec du silicium de type *n* comme matériau semi-conducteur en raison des techniques de microfabrication correspondantes qui sont bien établies. Le métal choisi est le cuivre, malgré sa tendance à diffuser dans le silicium à haute température. Ce choix est dû à la disponibilité des installations pour l'électrodéposition du cuivre. Toutefois, étant donné que le cuivre n'a pas pu adhérer directement au silicium, une couche de 100 nm de titane a été utilisé en tant que couche d'adhérence intermédiaire entre le cuivre et le silicium.

2.2 Etude de Caractérisation

Nous utilisons les méthodes dites 3ω et 2ω modifiée pour faire des mesures sur les super-réseaux. Toutefois, nous avons initialement choisi de calibrer le système de mesure en utilisant un substrat nu de silicium revêtu d'une couche d'isolant (SiO_2). La mesure a été effectuée selon l'approche de la mesure 3ω classique. Le dispositif fabriqué est représenté dans la Figure 2.1. Le schéma du dispositif expérimental utilisé pour la réalisation de ces mesures et les résultats obtenus sont représentés dans la Figure 2.2. Les premières mesures donnent de bons résultats (nous avons obtenu un résultat de diffusivité thermique du silicium pur comme 6.8 ± 0.5 (x 10^{-5} m^2/s), qui sont parfaitement conformes aux données théoriques trouvés dans la littérature [9]. La Figure 2.3 illustre le processus de fabrication pour réaliser des super-réseaux verticaux à l'échelle micrométrique dans le silicium et la Figure 2.4 présente l'image obtenue en microscopie électronique à balayage (MEB) de (a) la vue de

dessus de tranchées profondes de 100 µm et (b) la vue en coupe après leur eléctrodéposition avec du cuivre.

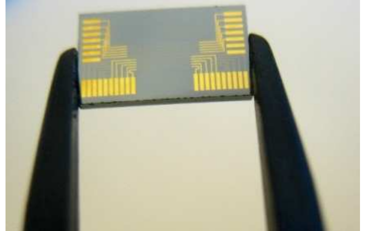
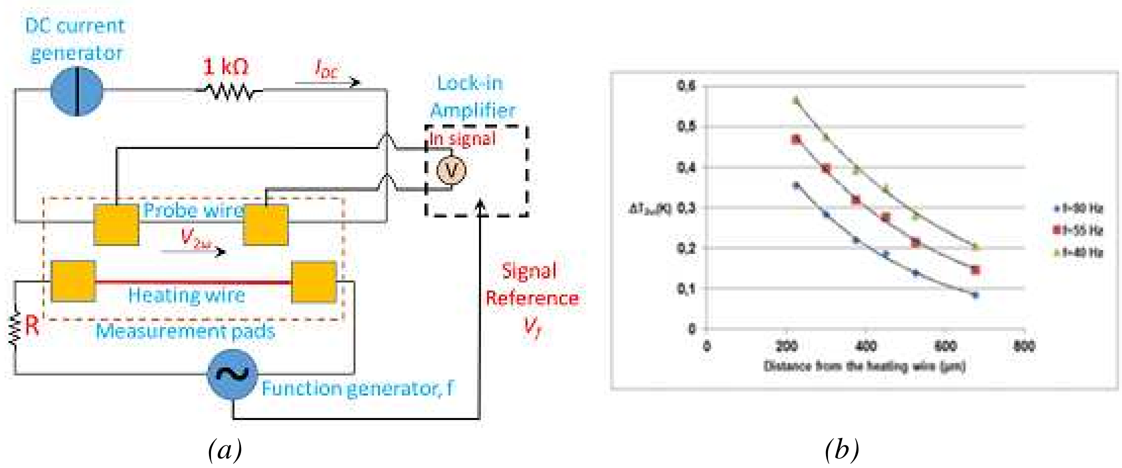


Figure 2.1. Photographie de la structure de test réalisée sur Si massif.



(a) (b)

Figure 2.2. (a) Schéma du dispositif expérimental de caractérisation et (b) les résultats.

Difficultés rencontrées

Le polissage de cuivre et /ou du silicium a été très difficile. Après le dépôt électrolytique, il restait environ 8-10 µm de cuivre sur la surface supérieur du substrat et qui nécessitait un polissage. Le polisseur mécano-chimique (CMP) n'a pas été concluant pour polir ce cuivre en raison de la nature robuste du cuivre. Par conséquent, nous avons utilisé l'acide nitrique dans le but de graver l'excès de cuivre sur le dessus, ceci laissant environ 2-5 µm de silicium pour être poli. Ce fut aussi un défi. L'action de la CMP a fini par détruire les tranchées. La figure 2.5 montre (a) les tranchées polies par l'acide nitrique et (b) les tranchées cassés suite à l'étape de polissage par CMP qui a suivi. Avec la connaissance des problèmes rencontrés par la fabrication des super-réseaux à l'échelle micrométrique, nous avons décidé de commencer la fabrication des super-réseaux à l'échelle nanométrique à l'aide de diverses techniques novatrices dans leur réalisation. Les chapitres suivants décrivent ces techniques de façon sommaire.

Oxide
SOI
PHOTOLITHOGRAPHY
PR
Oxide
SOI
DRIE
5 or 15µm
Oxide
SOI
SPUTTERING TI
Cu
Ti
Oxide
SOI
CU ELECTRODEPOSITION
Cu
5 or 15µm
Ti
Oxide
SOI
SPUTTERING CU
5 or 15µm
Ti
Oxide
SOI
POLISHING
Cu
Ti
Oxide
SOI
PECVD
SiN
Cu
Ti
Oxide
SOI
SPUTTERING GOLD
Gold
SiN
Cu
Ti
Oxide
SOI
PATTERNING
POSSIBLE STRUCTURE FOR 3 w MEASUREMENTS
ALUMINIUM
INSULATOR
SUPERLATTICES
Gold
SiN
Cu
Ti
Oxide
SOI

Figure 2.3. Procédé de fabrication des micro- super-réseaux micrométriques.

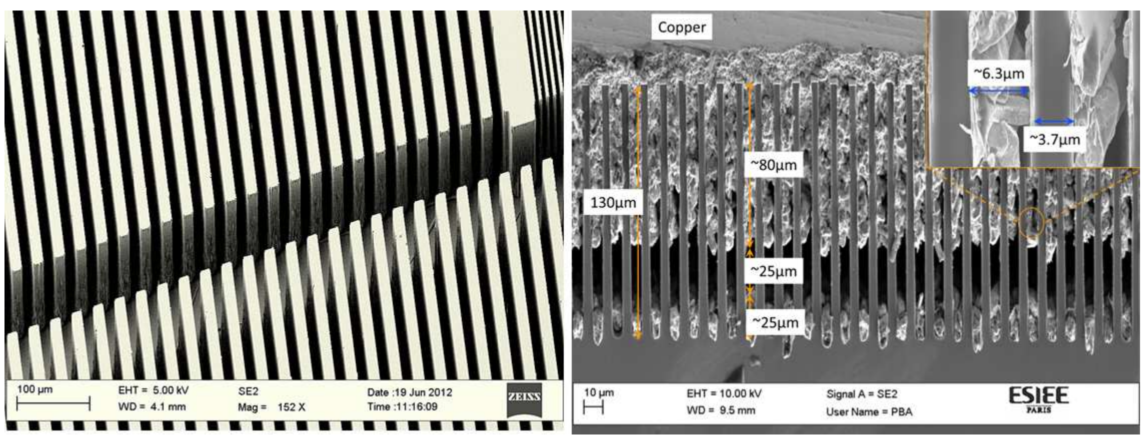


Figure 2.4. Les super-réseaux de taille micrométrique réalisés par DRIE.

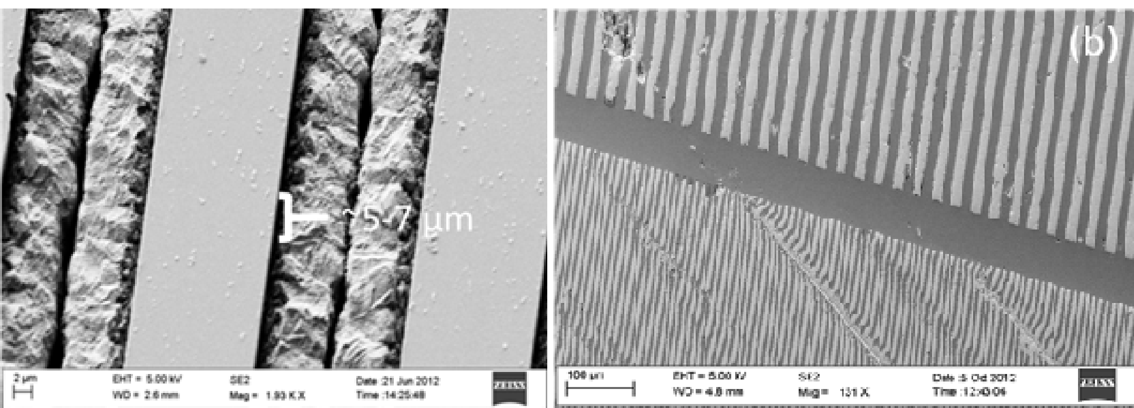


Figure 2.5. Vue de dessus de tranchées polies par l’acide nitrique et (b) Tranchées brisées par l'action du polissage CMP.

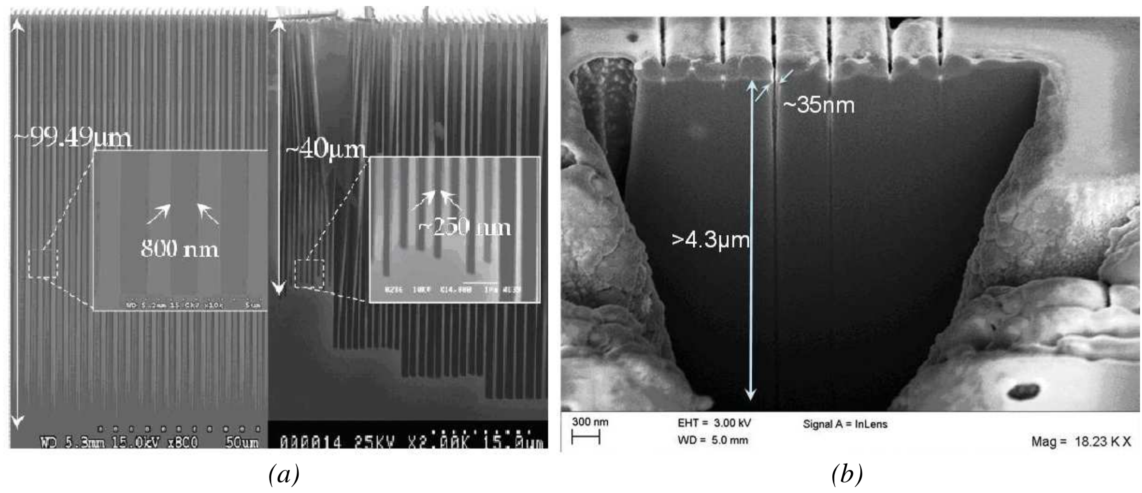
3. Fabrication de nanostructures à haut facteur de forme en silicium

3.1. Nanostructures obtenues par lithographie conventionnelle

Le principe de la photolithographie optique comprend l'impression par voie optique des motifs géométriques de taille (sub)micrométrique, la résolution étant limitée à la longueur d'onde utilisée, ce qui permet de réaliser des motifs dont les dimensions peuvent être de l'ordre de quelques 0,1 µm. Quant à l'obtention de motifs de l'ordre de la dizaine de nanomètres, elle peut se faire soit en recourant à la lithographie électronique, soit en recourant à des techniques non lithographiques, qui incluent les méthodes d'auto-assemblage décrites plus loin.

Nous décrivons des procédés de gravure DRIE Bosch, qui ont été optimisés pour obtenir les tranchées de silicium très profondes : avec un facteur de forme de 160:1 pour des tranchées de largeur de 250 nm ; et avec un facteur de forme de 124:1 pour les tranchées de largeur de 800 nm, respectivement. Nous avons présenté les résultats préliminaires qui suggèrent que les procédés de gravure cryogéniques purs peuvent être utilisés pour produire des facteurs de forme supérieurs à 120:1 pour les tranchées de largeur de 35 nm. A notre connaissance, ce sont les valeurs les plus élevées du facteur de forme qui ont été atteintes à ce jour en utilisant la gravure DRIE dans ces gammes de dimensions.

En combinant les résultats de nos expériences avec ceux d'autres rapports publiés dans la littérature, nous montrons que la dépendance du facteur de forme vis-à-vis de la largeur de la tranchée obéit à une loi logarithmique simple de deux paramètres, appliquée pour un large nombre des paramètres du procédé et des dimensions, y compris dans la gamme de dimensions sub-microniques, Ceci nous permet de proposer un nouveau facteur de mérite pour caractériser le facteur de forme final pouvant être obtenu en utilisant un procédé de gravure spécifique. La Figure 3.2 illustre les résultats obtenus avec (a) le procédé DRIE Bosch et (b) le procédé DRIE cryogénique.



(a) *(b)*

Figure 3.2. Les résultats de gravure (a) DRIE Bosch et (b) DRIE cryogénique.

3.2. Fabrication de nanostructures par approche Bottom Up

Les techniques présentées dans cette section détaillent la possibilité de réaliser des micro- et nano- structures de facteur de forme élevé par une approche bottom-up et donc ceci implique de la croissance des piliers ou des couches, par opposition à l'association lithographie-gravure qui enlève de la matière pour la création des motifs nécessaires à l'obtention des structures de facteur de forme élevé. En cette catégorisation, il existe différentes techniques, y compris la soft lithographie [10-12] le nanoembossing [13, 14], le nanomolding [15, 16], et micro-usinage par électro-érosion (EDM-μ) [17, 18].

3.2.1. Résultats obtenus par la technique d'Electrospinning

L'électrospinning est une technique pour fabriquer des nanofibres, qui sont ensuite utilisées sur le silicium comme un motif pour la gravure profonde par DRIE, pour produire des micro- et nano- structures du facteur de forme élevé comme un préalable à la fabrication des super-réseaux verticaux à l'échelle nanométrique. L'électrospinning est un procédé qui utilise une charge électrique pour étirer très finement (typiquement sur la micro- ou nano-échelle) des fibres à partir d'une solution liquide. Lorsque la force électrique surmonte la tension de surface du liquide, un jet est formé, et le solvant s'évapore rapidement au cours de sa propagation à la cible et les matières résultantes sèches, fibreuses forment les nanofibres sur le collecteur [19, 20]. Du côté de la solution, différentes propriétés comme la viscosité, la concentration, le poids moléculaire, etc influent sur la qualité et les caractéristiques des nanofibres produites. La figure 3.3 montre l'évolution de la variation du diamètre des nanofibres produites avec le changement des paramètres du procédé de l'électrospinning.

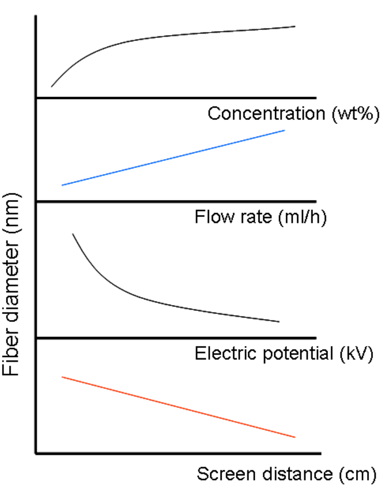


Figure 3.3 Variation du diamètre de nanofils avec des paramètres du procédé d'électrospinning.

Nous déposons les nanofibres de silicium et après nous réalisons par pulvérisation cathodique (sputtering) une couche d'aluminium d'une épaisseur de 100 nm. Nous effectuons ensuite un 'lift-off' qui laisse la trace des nanofibres entourées par la pulvérisation cathodique d'aluminium. Cela sert comme un masque pour la gravure DRIE. La figure 3.4 représente (a) les nanofibres déposés, (b) les nanofibres après le lift-off de Al et (c) la section des modèles gravées par DRIE.

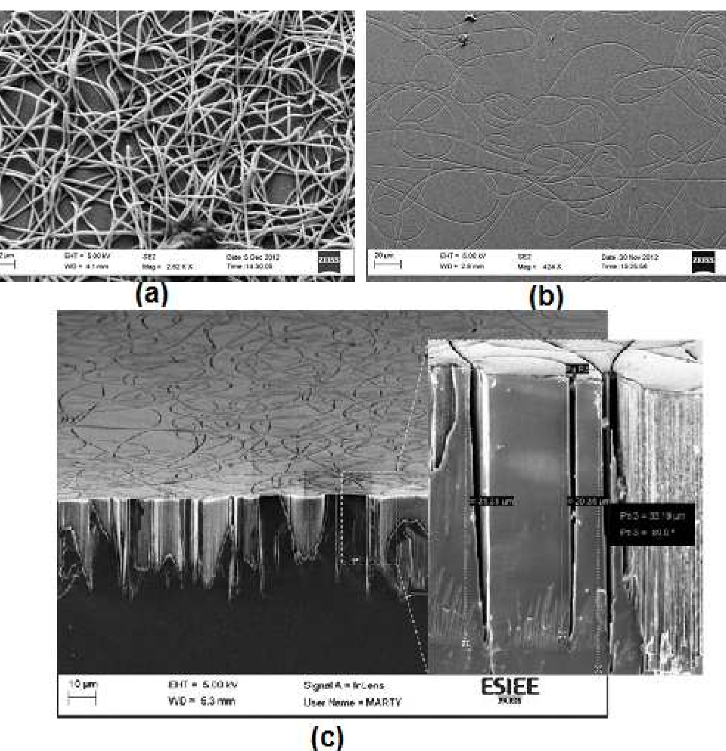


Figure 3.4. Image MEB de (a) nanofibres déposés, (b) nanofibres après le lift-off de Al et (c) section de modèles gravées par DRIE.

3.2.2. Résultats obtenus par di-blocs copolymères

Nous avons également utilisé des diblocs copolymères comme les motifs pour la gravure DRIE dans ce travail. La figure 3.5. illustre les différentes étapes de structuration par dibloc copolymère. Après avoir obtenu des motifs de copolymères à blocs, nous effectuons une gravure DRIE pour obtenir des nanostructures à grand facteur de forme (HAR – high aspect ratio *en anglais*) en silicium. La figure 3.6 illustre (a) une phase séparée de copolymère séquencée et (b) une gravure DRIE du bloc copolymère. Le silicium noir est produit comme un effet secondaire du procédé DRIE Bosch lors de la gravure des copolymères.

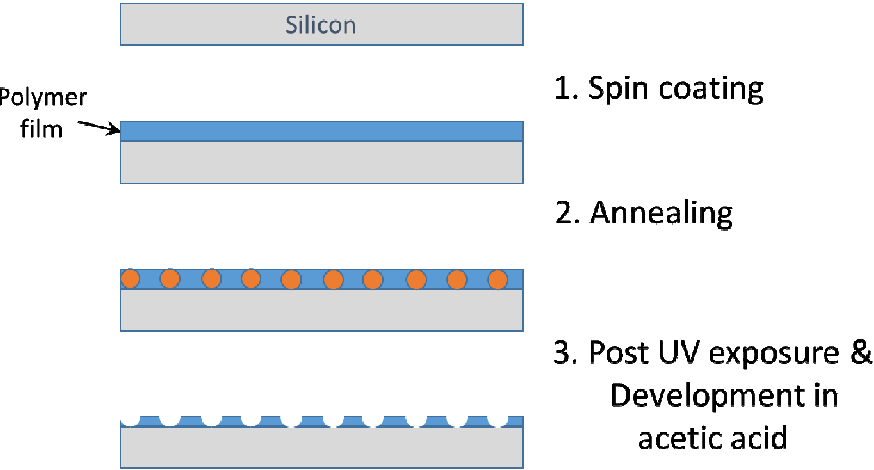


Figure 3.5 Différentes étapes de réalisation des copolymères diblocs.

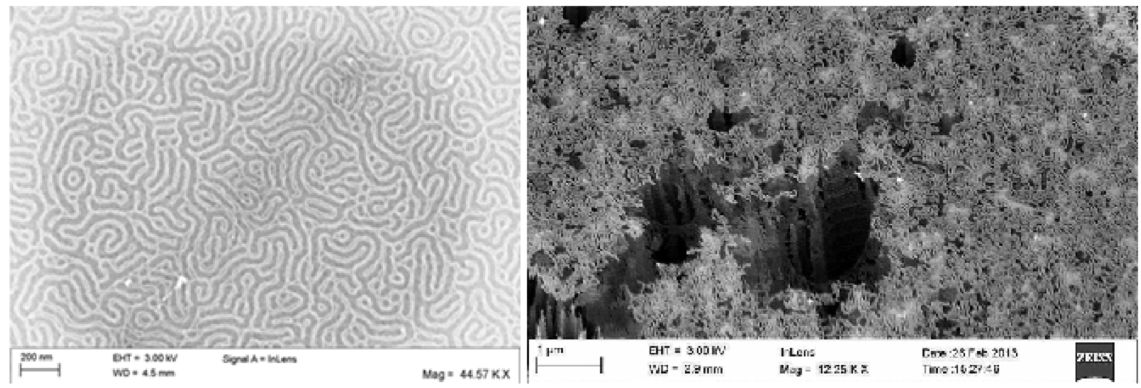


Figure 3.6 Image MEB de (a) copolymère dibloc et (b) après la gravure DRIE.

4. Conclusions et Perspectives

Dans ce travail, nous avons réalisé de nouveaux métamatériaux à base de silicium sous la forme de super-réseaux verticaux en vue de réaliser un matériau ayant de meilleures propriétés thermoélectriques. Nous avons fabriqué super-réseaux verticaux à l'échelle microscopique par micro-gravure de tranchées sur silicium et remplissage avec du cuivre. Nous avons conçu un système de caractérisation de mesure du coefficient Seebeck et de la conductivité thermique en utilisant la méthode dite 3ω. Alors que nous avons été confrontés à certains défis dans la réalisation des micro super-réseaux en vue de leur objectif final, certains des problèmes rencontrés ont été très utiles pour l'orientation qui a été donnée à ce travail.

Nous avons réalisé de nombreuses nanostructures de ratio d'aspect élevé en silicium en développant une variété de techniques expérimentales susceptibles de satisfaire aux exigences du concept des super-réseaux verticaux. Nous avons utilisé la gravure par DRIE sur les structures définies par lithographie classique. De plus, nous avons fait des incursions dans la nano-fabrication en utilisant l'approche "*bottom up*". A cet effet, nous avons recouru à l'electrospinning et la chimie de copolymère dibloc en tant que nouvelles techniques définissant des motifs de taille nanométrique.

Toutefois, pour les travaux futurs, il y a encore d'autres approches de nanostructuration ascendantes qui peuvent être testées afin de réaliser des nanostructures de ratio d'aspect élevé dans le silicium. Celles-ci incluent l'utilisation de billes poreuses d'alumine, les nanocristaux auto-assemblés sous la forme d'opales ou alors en utilisant le silicium noir comme un masque. Nous avons, dans la dernière partie de cette thèse, donné une introduction à chacune de ces méthodologies et comment ces principes peuvent être utilisés pour réaliser des nanostructures en silicium et in fine, des super-réseaux nanométriques aux propriétés thermoélectriques améliorées.

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Résumé: Les méta-matériaux offrent la possibilité d'obtenir des propriétés physiques nettement améliorées en comparaison avec celles des matériaux naturels. Dans ce travail, nous explorons une nouvelle variété de métamatériaux thermoélectriques à base de micro-et nano-structuration du silicium, sous la forme de super-réseaux verticaux, avec comme visée applicative la récupération d'énergie thermique ainsi que le refroidissement. En outre, nous focalisons nos efforts sur une méthodologie expérimentale permettant la réalisation de ces matériaux par des moyens simples et peu coûteux. La première partie de cette thèse sert d'introduction aux phénomènes thermiques qui constituent la base de la conduction électrique et de la dissipation de chaleur dans les nanostructures, respectivement par émission thermo-ionique et par la diffusion de phonons. Cette partie détaille également les principes et résultats de caractérisation thermique à l'aide des méthodes 3ω et 2ω. La deuxième partie de cette thèse décrit les approches de micro- nanostructuration descendante « top-down » et ascendante « bottom-up », en vue de la fabrication de super-réseaux nanométriques sur du silicium mono-cristallin. La nouvelle architecture verticale proposée soulève des défis technologiques qui sont traités à travers l'exploration de techniques expérimentales originales pour produire, d'une manière efficace et sur de grandes surfaces, des structures submicroniques à fort facteur de forme. Ces techniques comprennent l'utilisation de motifs résultant de lithographie traditionnelle combinée à l'extrusion pour en produire des structures volumiques. En outre, l'utilisation de nanofibres et de diblocs copolymères comme nano-motifs géométriques sont également présentés pour nous rapprocher davantage de l'objectif ultime du projet.

Mots clés: Metamateriaux, Super-réseaux, micro- et nano-structures en silicium, DRIE.

Abstract : Metamaterials offer the benefit of obtaining improved physical properties over natural materials. In this work, we explore a new variety of thermoelectric metamaterials based on silicon micro- and nano- structuration, in the form of vertical superlattices for use in energy-related applications. Additionally, we focus on a route towards fabricating these materials using simple and low-cost means compared to prior attempts. The first part of this thesis serves as an introduction to the thermal phenomena which form the basis for electrical conduction and heat dissipation by thermionic emission and phonon scattering at the nanoscale. These principles forms the crux of the device. This section also details the characterization principles and results using the 3ω and 2ω methods for thermal measurement. The second part of this thesis describes both top-down and bottom-up approaches towards fabricating nanoscale superlattices from single-crystalline silicon. The novel proposed vertical architecture raised technological challenges that were tackled through the exploration of original experimental techniques for producing high aspect ratio (HAR) structures in an effective manner and over large surface areas. These techniques include the use of traditional lithography patterning and subsequent extrusion of volumic structures. Additionally, the use of nanofibers and diblock copolymers as templates for further etching of HAR silicon nanostructures are also presented to bring us closer to the ultimate goal of the project.

Keywords: Metamaterials, Superlattices, HAR structures, DRIE.