DESIGN, TECHNOLOGY AND PACKAGING OF CESIUM VAPOR CELLS FOR MEMS ATOMIC CLOCKS

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Thèse

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CONCEPTION, TECHNOLOGIE ET PACKAGING DE CELLULES À VAPEUR DE CÉSIUM POUR LES HORLOGES ATOMIQUES DE TYPE MEMS

(DESIGN, TECHNOLOGY AND PACKAGING OF CESIUM VAPOR CELLS FOR MEMS ATOMIC CLOCKS)

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Résumé

Les horloges atomiques sont de nos jours parmi les normes de temps et de fréquences les plus précises et sont utilisées, par exemple, pour les services de distributions travaillant à l'heure internationale ou pour les systèmes de navigation globaux par satellite. Au cours des dernières années, un travail considérable a été accompli par différents groupes à travers le monde pour développer une version miniaturisée des horloges atomiques, basée sur la technologie des systèmes microélectromécaniques qui est fiable, bien stabilisée et sur la disponibilité de lasers sur puces (diode laser monomode à cavité verticale émettant par la surface ou VCSEL : Vertical-Cavity surface emitting Laser). Ce type d'horloge atomique est appelé horloge atomique MEMS ou horloge atomique sur puce (CSAC : Chip Scale Atomic Clocks).

L'objectif de cette thèse était de concevoir et développer la technologie des cellules à vapeur de Césium (Cs) ainsi qu'une analyse thermique pour sa gestion thermique lorsqu'elle est complètement packagée pour les horloges atomiques MEMS. Ce travail a été réalisé dans le cadre du projet européen "MEMS atomic clock for timing, frequency control and communication" (MAC-TFC). Deux conceptions différentes de la cellule à vapeur de Cs ont été considérées. La première est basée sur la transmission de la lumière à travers la cellule et donc au travers de la vapeur de Cs et est appelée cellule transmissive ou T-cell. Ces T-cells sont réalisées à base de cavités profondes générées dans du silicium et prises en sandwich entre deux wafers de verre borosilicaté. Pour leur fabrication, le processus de gravure profonde par ions réactifs (DRIE-Deep reactive ion etching) a été optimisé afin de produire des cavités dans le silicium dont les parois soient suffisamment lisses. De plus, le procédé de soudure anodique a été développé pour remplir les cavités avec du gaz tampon à la pression requise. La deuxième version de la cellule à vapeur de Cs est basée sur la réflection de la lumière du laser à l'intérieur des cavités gravées dans le silicium par KOH et scellées par un wafer de verre borosilicaté. Cette cellule est appelée cellule réfléchissante ou R-cell. Les R-cells permettent, par rapport aux T-cells, une interaction lumière/atome plus longue dans les cavités contenant du Cs, tandis que la localisation de la source optique et des éléments de détection du même côté de la cellule permet la réalisation d'une horloge plus compacte. Pour leur fabrication, la gravure humide par KOH, employée pour générer les cavités à l'intérieur du silicium avec des parois dont la surface est proche de celle d'un miroir (111), a été étudiée et optimisée. De plus, les réseaux de diffraction pour le guidage de la lumière polarisée circulairement ont été conçus, fabriqués et intégrés sur la partie supérieure de la R-cell à vapeur de Cs. Pour les deux versions des cellules à vapeur de Cs, notre objectif était de simplifier l'assemblage relatif à l'horloge en faisant un maximum d'intégration et d'alignement à l'échelle du wafer, grâce à des composants micro-optiques réfractifs et diffractifs. Une

analyse thermique a aussi été effectuée pour la gestion thermique de la cellule à vapeur de Cs complètement packagée (T-cell) à base de céramiques cofrittée à basse température (LTCC : Low temperature Co-fired ceramics).

Mots-Clés : Horloges atomiques, MEMS, cellules à vapeur de Cs, composants micro-optiques, analyse de l'état d'équilibre thermique

Abstract

Atomic clocks are nowadays among the most accurate time and frequency standards, and are used, e.g., for international time distribution service or in global navigation satellite systems. During the last several years, based on reliable and well-stabilized microelectromechanical systems (MEMS) technology and on the availability of lasers on chip (single-mode vertical-cavity surface-emitting laser; VCSEL), considerable work has been performed by different groups around the world to develop miniaturized version of atomic clocks, called MEMS atomic clocks (MAC) or chip scale atomic clocks (CSAC).

The goal of this thesis was to design and develop the technology of Cs vapor cells along with thermal analysis for the thermal management of fully packaged Cs vapor cell for MEMS atomic clock. This work has been carried-out in the framework of European project "*MEMS atomic clock for timing, frequency control and communication*" (MAC-TFC). Two different architectures of Cs vapor cell have been considered. The first one operates on the transmission of light through the cell and thus the Cs-vapor, and is called *transmissive* cell or T-cell. Such T-cell is made of silicon based deep-cavities sandwiched between two borosilicate glass wafers. For their fabrication, deep reactive ion etching (DRIE) process has been optimized in order to produce smooth enough side walls of silicon cavities. In addition, specific anodic bonding process has been developed to fill the cavities with buffer gas at the required pressure. Second version of Cs vapor cell is based on the reflection of laser light inside the KOH etched silicon cavity sealed by one borosilicate glass wafer and is called *reflective* cell or R-cell. R-cells, as an advantage over the T-cells, allow e.g. a longer interaction of light/atom inside the Cs cavity, whereas location of optical source and detection elements on the same side of cell leads to better clock compactness. For their fabrication, wet KOH etching, employed to realize the cavities inside the silicon with near mirror like (111) planes, has been studied and optimized. Further, diffraction gratings for routing of circularly polarized light have been designed, fabricated and integrated on top of the Cs vapor R-cell. In both versions of Cs vapor cells, our goal was to simplify the related clock assembly by doing maximum integration and alignment at the wafer level, thanks to refractive and diffractive micro-optical components while thermal analysis has been also performed for the thermal management of fully packaged Cs vapor cell (transmissive one) based on the Low temperature co-fired ceramics (LTTC) packaging.

Keywords: Atomic clocks, MEMS, Cs vapor cells, micro-optical components, steady-state thermal analysis.

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General introduction

When we talk about clocks, people at large first think about the clock that they use in everyday life (wrist watch, wall clock etc.) which are based on the motion of dial to and fro or based on quartz crystal oscillator to tell second, minute and hours. However, if it seems that a second difference does not affect our daily life, technologies that surround us, such as, e.g. telecommunications or power distribution (networks synchronization), requires much more precise timekeeping. For instance, satellites used for navigation or communications are located between hundreds and thousands of kilometers from the earth. Since radio waves travel nearly 300,000 km every second, slight inaccuracies in time can lead to massive differences. Thus, frequency or time references have been developed for decades, among which the atomic clocks are one of the most accurate. Atomic clock is an instrument that provides a reference signal based on the transition between two energy states of atoms. More precisely, an atomic clock is a clock that uses the resonance frequencies of atoms as its resonator. The resonator is regulated by the frequency of the microwave electromagnetic radiation emitted or absorbed by the quantum transition (energy change) of an atom or molecule. The advantage of this approach is that atoms resonate at extremely consistent frequencies.

However, to probe the resonance frequency of the atoms without perturbing it, complicated and cumbersome setups are usually required. Thus, high power consumption and large size have prevented the development of hand-held devices. For several years, thanks to the fabrication method of Micro-Electro-Mechanical-Systems (MEMS) and availability of Vertical Cavity Surface Emitting lasers (VCSEL), a new generation of miniaturized atomic clocks has been developed. This thesis is then devoted to the realization of such micro-atomic clock. The related work was performed in the frame of the European project “MEMS Atomic Clock for timing, Frequency Control and Communication” (MAC-TFC). Goal of MAC-TFC [MAC-TFC 2008] is to develop and demonstrate all the necessary technology to achieve a first European ultra-miniaturized, low power Cesium atomic clock with a short term stability of $5x10^{-11}$ over

one hour while operating on the power of an AA battery with less than 200mW power consumption. This project relies on a consortium bringing together various European research institutes and industries.

I have joined this project from its beginning in September 2008 as full time PhD student. My work was mainly devoted to the design, packaging and development in technology for Cs vapor cells, which are the "alkaline vapor containers". Two architectures have been studied, the transmissive one (T-cells) and the reflective one (R-cells). My work concerned technology development such as deep reactive ion etching, wet etching, anodic bonding and buffer gas filling processes. It included also the steady state thermal analysis of fully LTCC (low temperature co-fired ceramic) packaged Cs vapor cell for its thermal management and micro optical components realization for the R-cell architecture.

Thus, the manuscript is organized as follows: Chapter 1 describes general principle of atomic clock along with description of atomic structure and use of alkali atom for the atomic clock application. History of atomic clock is then reported, consisting of various existing atomic clock technology up to date and state of the art of miniaturized atomic clocks.

Chapter 2 focuses on the development in T-cells technology which includes design of photo-mask, Deep reactive ion etching (DRIE) optimization, anodic bonding in buffer gas environment and optical measurements of vapor cells (linear absorption, CPT measurement, aging tests).

In Chapter 3, thermal analysis of fully low temperature co-fired ceramic [LTCC] packaged Cs vapor cells for the thermal management of MEMS atomic clock is described. Various solutions in terms of LTCC design, vacuum environment, metal coating have been considered to achieve conditions for thermal management.

Chapter 4 is devoted to the design and fabrication development of the second architecture (reflective version) of vapor cells. It concerns mainly wet- (KOH) etching optimization and fabrication of optical components by means of electronic lithography. Optical measurements, performed to validate the technology, are also presented.

Finally, complete thesis work is concluded in conclusions and perspectives.

Chapter 1 General Principle and state of the art of atomic clock

1.1 General principle of atomic clock

Every clock should consist or should be connected to an apparatus that oscillates at uniform rate in order to control the rate of change of clock digits. In case of, e.g. pendulum clocks by Christian Huygens in 1656 in which weight moves at constant frequency and clockmaker finds a mechanical way to count the swing and move the clock hands. In the case of atomic clock [Lyons 1949]; the oscillations are the ones of an electromagnetic field that results from transitions between two energy states of atoms. In the commonly used cesium 133 atoms, this field oscillates at about 9.19 billion times per second (f=9.192 GHz) and is used as a frequency standard for the clock timekeeping elements. In an atomic clock, a quartz crystal oscillator (called the local oscillator) is used for keeping clock time.

Thus, atomic clocks consist mainly in a physical package (part used to probe the atoms), a tunable microwave synthesizer, and a control loop which is used to lock the local oscillator onto the exact frequency of the hyperfine splitting of the atoms. In the next section, principle of passive atomic clock is described.

1.1.1 Passive atomic clock

Figure 1.1 shows the schematic for passive atomic clock [Lyons 1949] which consists in a local oscillator, a microwave synthesizer, a physics package and a control loop. Passive atomic clock delivers a signal, as its output, which is generated by the quartz crystal based local oscillator locked on some atomic transition. Local oscillator itself does not have sufficient well-defined frequency, i.e. it fluctuates within time due to

unstable environmental parameters like temperature, pressure, vibration, etc. Then, to deliver more stable and accurate frequency signal (especially at longer time), it needs to be compared with a more stable reference signal provided by the atomic transitions.

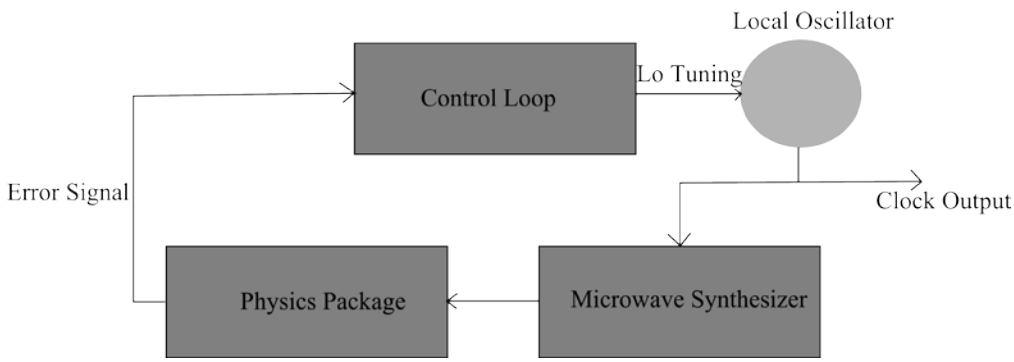


Figure 1.1 Schematic of passive atomic clock.

In the passive atomic clock as shown in Figure 1.1. The local oscillator (usually a voltage controlled quartz oscillator *VCXO*) is followed by a frequency synthesizer that delivers a RF signal close to the clock frequency. This signal is modulated in order to probe the resonant signal in the physical package that contains the atoms. Thanks to synchronous demodulation, an error signal, e.g. cancelled when the two frequencies (probe and resonant) are equal, is extracted and allow locking of the local oscillator. Frequency of the local oscillator is then corrected and is delivered as the clock output. Thus, accuracy of atomic clock depends on the stability of atomic frequency reference, i.e. on the atomic resonance. Typical atomic resonance can be seen from Figure 1.2.

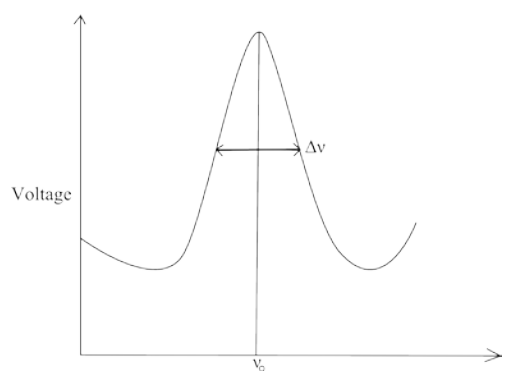


Figure 1.2 General atomic resonance signal.

Thus, short-term stability of a clock is usually described by means of Allan deviation (Equation 1.1) [Vanier 1989]. This statistical tool, actually the standard deviation of relative fluctuations of frequency,

describes the deviation of the oscillator frequency from the mean frequency over a specified period of time and is written as:

$$\sigma_y(\tau) = \frac{\Delta\nu}{\nu_0}\frac{1}{S/_N}\tau^{-\frac{1}{2}} \tag{1.1}$$

Where, ν_0 is the resonance frequency or atomic transition frequency (for example: 9.192631770 GHz for Cesium atoms) and $\Delta\nu$ the full width at half maximum (FWHM) that will be often called signal linewidth in the following. S/N is the signal-to-noise ratio as results from the resonance at 1Hz bandwidth. It can be noted that such deviation does not take into account the local oscillator noise. Short term stability of atomic clock can then be improved by reducing the signal linewidth and/or by increasing the signal-to-noise ratio. For example, in the case of vapor cell based atomic clock, linewidth can be reduced by introducing buffer gas in the atomic vapor cells as it will be detailed later on. Whereas long term stability further depends on the environmental stability like temperature, laser intensity, magnetic field and so on. For example, first ever atomic clock based on the ammonia molecules had stability of 2×10^{-8} [Lyons 1949] while most accurate clock nowadays is characterized by a stability of 3×10^{-16} [NIST 2011].

1.1.2 Atomic structure

Atoms are basic building block of matter whose interesting feature is the invariance in time and space of their energy levels. Thus, splitting between energy levels can be considered constant. For atomic clocks, alkali atoms are used because of their single valence electron. Thus, energy levels of such electron are the one involved in the clock operation.

1.1.2.1 Alkali atoms

Alkali metals (H, Li, Na, K, Rb, Cs) are located in the first column of the periodic table and under *s* block which means their single valence electron is in an outer *s* orbital. Then, because of spin-orbit interaction, coupling of the orbital angular momentum *l* of this valence electron to its spin angular momentum *s*, only levels characterized by a total angular momentum *j* equal to:

$$j = l \pm s = l \pm \frac{1}{2} \tag{1.2}$$

where $|l - s| \leq j \leq l + s$, can exist (See Table 1.1).

Table 1.1 Full notation of fine structure of alkali atoms.

Levels	*l*	*s*	Multiplicity [2*s*+1]	*j*	Full notation
S	0	1/2	2	1/2	$^2S_{1/2}$
P	1	1/2	2	3/2 , 1/2	$^2P_{3/2}$, $^2P_{1/2}$
D	2	1/2	2	5/2 , 3/2	$^2D_{5/2}$, $^2D_{3/2}$
F	3	1/2	2	7/2 , 5/2	$^2F_{7/2}$, $^2F_{5/2}$

Further coupling of the total angular momentum *j* and the total angular momentum of the nucleus (nuclear spin) *I* give rises to the total atomic angular momentum:

$$F = j + I \tag{1.3}$$

where magnitude of *F* lies between

$$j - I \leq F \leq j + I \tag{1.4}$$

Though quantum mechanical in nature, the interaction can be visualized as the interaction between two magnets, that of the nucleus and that of the electron, leading to two very closely spaced energy levels based on whether the nuclear and electron spins are parallel or anti parallel. This splitting results in the so called "hyperfine structure".

So, for alkali atoms, fundamental state of single valence electrons ($nS_{1/2}$) is made of two hyperfine levels. It can be mentioned that the magnetic dipole transition between those two levels is used as the clock transition, being, as mentioned earlier, in the radiofrequency range. In addition, optically pumped atomic clocks use excited levels such as ($nP_{1/2}$) or ($nP_{3/2}$). Up to now, H, Rb and Cs atoms have been used for atomic clocks, out of which Cs clocks are some of the most stable.

1.1.2.2 Cesium atoms for atomic clock application

The cesium atom has 55 protons in its nucleus and 55 electrons in orbit around it to be a neutral atom. The structure of the Cs is then equivalent to the one of the noble gas xenon (54 electrons) plus one additional electron. According to Aufbau principle, xenon structure fills all the levels up to the *5p* orbital so that the additional electron of Cs is located onto the *6s* orbital.

Thus, according to the processes described in the previous section, the cesium ground state is characterized by L=0 and s=1/2 so that j=1/2 (leading to $6^2S_{1/2}$) whereas the first excited states are characterized by L=1 and j=1/2 or j=3/2 leading to $^2P_{1/2}$ and $^2P_{3/2}$. Then, the transitions D_1 (λ=894.6nm) and D_2 (λ=852.3nm) corresponds to the transitions $6^2S_{1/2} \rightarrow 6^2P_{1/2}$ and $6^2S_{1/2} \rightarrow 6^2P_{3/2}$, respectively (as shown in Figure 1.3). In addition, the cesium nucleus exhibits a magnetic influence, so that I= 7/2.

The energy levels resulting from this hyperfine splitting (Equations 1.3, 1.4), are:

For the Cs ground state $6^2S_{1/2}$ and the first excited state $6^2P_{1/2}$: j=1/2, I=7/2 => hyperfine energy level: F =3, 4.

For the second excited state $6^2P_{3/2}$: j=3/2, I=7/2 => hyperfine energy level: F =2, 3, 4, 5.

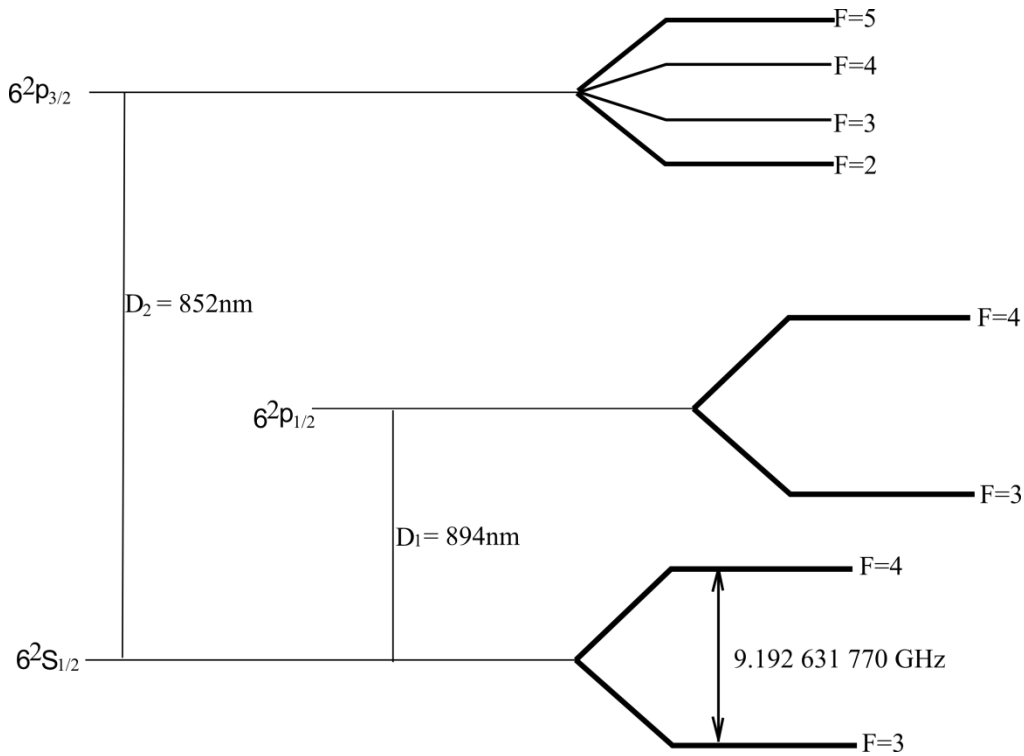


Figure 1.3 Cesium energy level showing two kinds of transition (D1 and D2) at ground state and their hyperfine level.

It is important to mention that the B.I.P.M.0F[1] chose during the "13ème conference générale des Poids et des Mesures" in 1967 to define the second as *the duration of 9192631770 periods of the radiation corresponding to the transition between the two hyperfine levels of the ground state of the cesium 133 atom* [Allan 1997]. This value was fixed according to the measurement of Markowitz *et al*. [Markowitz 1958]. Cs is obviously not the only possible atom to be used in an atomic clock. However, it is still today interesting since it exists only one stable isotope, the two excited states can be pumped by VCSEL lasers and the fusion temperature is low (28°C).

In case of no external magnetic field, these hyperfine levels are degenerated. In order to break the degeneracy, exposure to weak magnetic field is required in order to split each F level into $2F+1$ magnetic Zeeman sublevels (m_f). Fine structure of Cs along with the hyperfine splitting and magnetic sublevel is shown in the Figure 1.4.

[1] Bureau International des Poids et Mesures

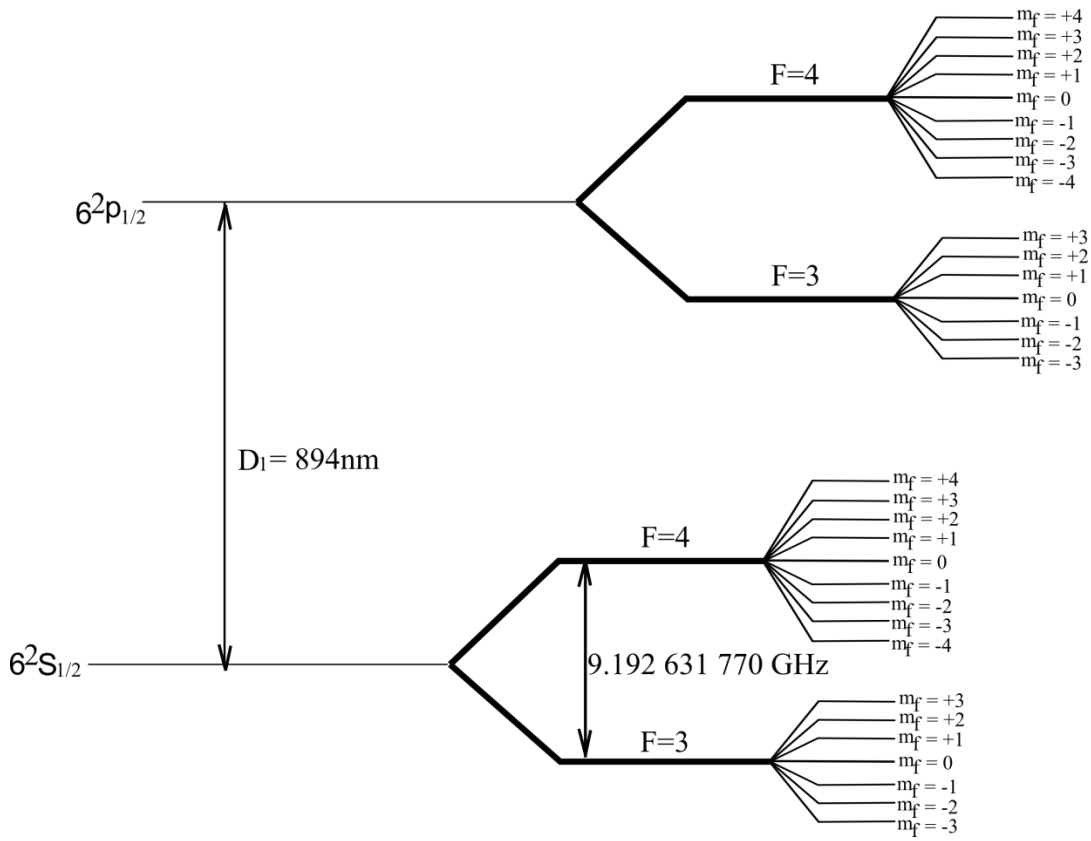


Figure 1.4 Cs D1 transition line along with hyperfine and Zeeman level.

Thus, Cs state F=3 has seven Zeeman sublevels (m_f =[-3,+3]), and F=4, 9 Zeeman sublevels (m_f =[-4,+4]). Zeeman sublevel energy depends on B_0, linearly for $|F, m_f \neq 0>$ and quadratically for $|F, m_f = 0>$. Then, in weak magnetic field, splitting of hyperfine level to the lowest order is given by equation 1.5.

$$\Delta E\left|F, m_f\right\rangle = \mu_B g_F m_f B_O \qquad (1.5)$$

Where μ_B is Bohr Magnetron and g_F is Landé factor of the hyperfine level.

Here frequency of hyperfine transition from F=3 to F=4 is of particular importance for timekeeping and useful in the atomic clock standard. Cs clock uses this transition as a reference frequency for its oscillator. There are 16 possible magnetic states m_f of cesium, but only the transition between $|F = 4, m_f = 0\rangle$ and $|F = 3, m_f = 0\rangle$ states is useful, because this transition is, to first order, insensitive to magnetic fields (sensitive only to the second order). This $|4,0\rangle \leftrightarrow |3,0\rangle$ hyperfine transition produces the frequency used to define the SI second. It is consequently mandatory to produce a weak and homogenous static magnetic field around the Cs atoms.

1.2 Up-to-date atomic clocks

The idea of using atomic transitions to measure time was first suggested by Lord Kelvin in 1879, but it is only in 1930 that Professor Isidor Rabi exploited the idea with the atomic beam magnetic resonance technique. 15 years later, Rabi tried to use the latter in order to build a very accurate clock [Rabi 1945]. Then, in 1949, the first atomic clock based on the vibrations of ammonia molecule (Figure 1.5) was built by the US National Bureau of Standards (NBS) [Lyons 1949] with inaccuracy better than 10^{-8}. However, its performance being not better than existing standards, attention shifted quickly to more-promising, atomic-beam devices based on cesium and then in 1952, the first cesium atomic clock was built at NBS. The first clock, called NBS-1 with inaccuracy of 10^{-10}, became the calibration source for all other clocks.

In 1955, Dr Louis Essen developed the first practical laboratory cesium atomic clock [Essen 1955] by integrating the cesium atomic standard with conventional quartz crystal oscillators to allow calibration of existing time-keeping as shown in Figure 1.6. Since the 1950, Cs based atomic clocks become the first interest for the various research laboratories aiming to develop frequency standards such as the National Physical Laboratory (NPL) in U.K and the NBS. Soon after, i.e. in 1967, the 13th General Conference on Weights and Measures redefined the SI unit of time, the second, in terms of the cesium standard so as to equal the second of Ephemeris Time. The Conference defined the second as "*the duration of 9,192,631,770 periods of the radiation corresponding to the transition between the two hyperfine levels of the ground state of the cesium-133*". Development of atomic clock at NBS for primary standards, from 1950 when they made first version of atomic clock with inaccuracy of 10^{-10} until 2000 when NIST-F1 with inaccuracy of 10^{-15} was developed, is summarized in the Figure 1.7.

Figure 1.5 Clock based on ammonia vibration (1949).

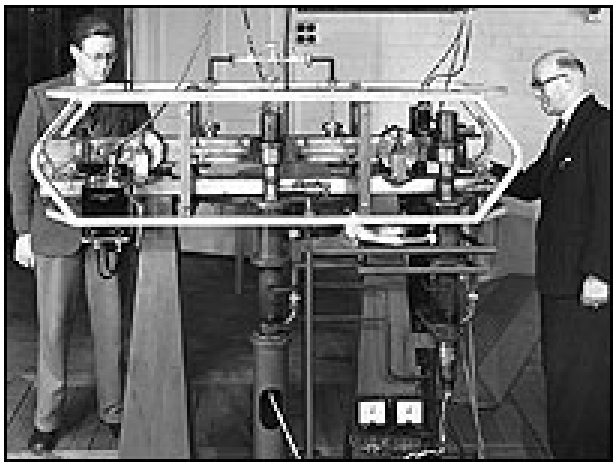


Figure 1.6 First cesium based atomic clock (1955).

Much of modern life has come to depend on precise time. Transportation, communication, manufacturing, electric power and many other technologies have become dependent on super-accurate clocks. Scientific research and the demands of modern technology continue to drive our search for more accurate clocks ever. The next generation of cesium time standards is presently under development in different laboratories around the world.

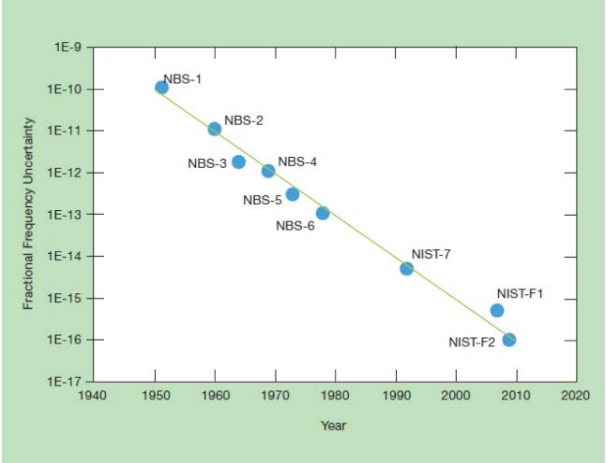


Figure 1.7 History of NIST atomic clocks and their inaccuracy [Lombardi 2007].

Brief description about various technology involved in the development to more accurate atomic clock is described in the following section.

1.2.1 Some technologies for time references

There are two kinds of atomic clock; one is laboratory standard also known as primary clock which is usually room size, whereas other one is secondary standard or commercial clock whose size is the one of a suitcase. Laboratory standard clocks are few as they are used inside the research laboratories for frequency measurements of high accuracy for example; NIST-7 standard at National Institute of Standards and Technology (NIST) in Boulder and the atomic fountains at NIST, Physikalisch-Technische Bundesanstalt (PTB), Germany, Paris Observatory, France, and United States Naval Observatory (USNO). Beside laboratory standards, smaller and commercial clocks have been also developed. They are cheaper, but still provide state-of-art measurement of precise time and time intervals.

1.2.1.1 Cs beam atomic clock

First ever made cesium clock [Essen 1955] was based on a cesium beam tube (Figure 1.8). In such a cesium clock, liquid cesium is heated to a gaseous state in an oven. The oven has a hole from which the atoms escape at high speed toward the tube. In the tube, two electromagnets generate a field that separates the atoms into two beams, depending on their spin energy state, corresponding to the two hyperfine ground state energy levels (F=3 and F=4) .Those in the lower energy state (F=3) then pass through the ends of a U-shaped cavity (known as Ramsey cavity) in which they are irradiated by microwaves of 9.192Ghz frequency (λ=3.26cm). Interaction with microwaves leads to switch their spin and consequently shift from F=3 to F=4. The beam at the exit of the U-cavity, passes through another pairs of electromagnets that deflects atoms in F=3 so that only the higher energy state (F=4) atoms hit the detector (made of a hot wire to ionize the atoms, a mass spectrometer to select the cesium one from any impurities and an electron multiplier).

Figure 1.8 Cesium beam tube; Cs store in the oven (left), Ramsey U-shaped cavity (middle) and ion collector (right) [Tycho].

Then the microwave frequency of the Ramsey cavity is adjusted until the output current is maximized, constituting the measurement of resonance frequency of atom. Such frequency is then used in feedback loop to lock the quartz crystal based local oscillator to a frequency of 5 MHz, which is the actual output of

the clock, along with a one-pulse-per-second signal. This complete set-up is shielded from external magnetic fields.

1.2.1.2 Atomic Hydrogen maser

The first atomic hydrogen maser was reported as a free running oscillator in 1960 [Goldenberg 1960] at Harvard by Goldenberg, Kleppner and Ramsey. It is a specific type of maser based on hydrogen atoms used as a frequency standard. The hydrogen atoms, generated from H_2 molecules by discharge and magnetically selected are sent into a storage bulb located within a microwave cavity. This cavity is tuned to the 1420 MHz resonance frequency of the atoms, in order to reverse the spin of the electron. Active and passive hydrogen masers exist, depending on the quality of the cavity. The stability of hydrogen masers can be better than 1×10^{-15} over several hours.

Non-commercial as well as commercial hydrogen masers are used in an increasing number of very demanding applications, including:

- very long base line interferometers (VLBI) for radio astronomy;
- NASA deep space network;
- Laboratory reference standards for measurements of high spectral purity.

1.2.1.3 Atomic fountain based on laser cooling

Microwave cavity design, introduced by Norman Ramsey in late 1940s, resulted in the cesium beam clocks that dominated the field of primary atomic frequency standard until the mid 1990s.

In 1953, Zacharias proposed to use slow atomic beams for atomic clocks [Wyanands 2005]. His idea was to direct the thermal atomic beam vertically so that the atoms slow-down, eventually turn around and fall under gravity in order to pass a second time in the microwave cavity. Such architecture known as atomic fountains, allow longer interaction time.

However, with this method of atomic fountain, only a small fraction of sufficiently slow atoms was useful. Thus, an additional technique, namely the laser cooling [Cohen-Tannoudji 1990, Buell 1998] was developed to further slow down the atoms. As a result, atomic fountain clocks based on the laser cooling are today the most stable and accurate clocks in the world.

Laser cooling allows slowing the atoms by means of optical forces. 6 different laser beams (3 counter-propagating pairs) are incident onto atoms moving with the velocity v in the opposite direction of one

beam. When laser is tuned to the resonance frequency of atoms, they absorb a photon and experience the momentum leading to their slowdown. After many absorption/emission cycle (90000 for Cs), atoms get slow down significantly.

Figure 1.9 shows the schematic of an atomic fountain. After trapping (cooled until few mK), atoms are pushed upwards to the microwave cavity, where they interact with the microwave field which transfers them to quantum superposition state. Then, they fall back under gravity, and passes through the microwave cavity once again. Finally, the populations of both sub-levels are measured by fluorescence induced by two laser probe beams.

The first atomic fountain was built by Steve Chu at Stanford University. Today the world's most stable and accurate clock is a cesium atomic fountain (NIST F1) at NIST with inaccuracy of $3 \times 10^{-16}/\sqrt{\tau}$, where τ is the integration time in seconds.

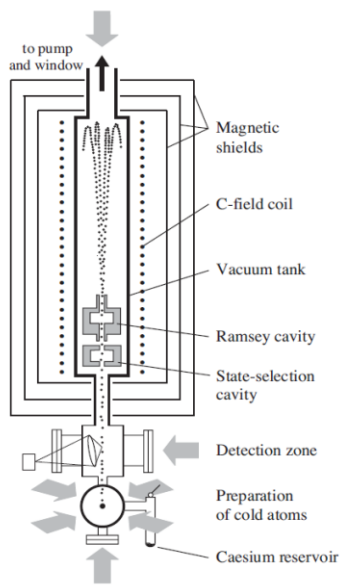


Figure 1.9 Schematic of an atomic fountain with laser cooling.

1.2.2 Optically pumped atomic clocks

However atomic clocks mentioned above and providing high accuracy are characterized by large size, large power consumption and high cost. Thus, further development of atomic clock aimed to reduce these parameters mostly thanks to optical pumping. For instance, optically pumped rubidium standard

[Affolderbach 2003, Chantry 1996, Ho 1998, Koyama 2000 and Suzuki 1998] has a volume of 100cm^3 and a power consumption of few watts. They are known as rubidium atomic frequency standard (RAFS).

1.2.2.1 RAFS

Rubidium Atomic frequency standards (RAFS) are based on a double-resonance process: [Happer 1972] an optical and a microwave resonance. The source for optical pumping of ^{87}Rb is a ^{87}Rb discharge lamp followed by a filter based on ^{85}Rb (absorbing the light corresponding to the transition $|3\rangle$ to $|2\rangle$ of ^{87}Rb) (Figure 1.10(b)). ^{87}Rb atoms, contained in the resonance cell, are then optically pumped from ground state $|1\rangle$ into excited state $|3\rangle$(Figure 1.10(a)). From there, atom can decay into either of two ground states but large fraction of atom will be trapped in $|2\rangle$ which makes cell transparent because fewer atoms can absorb the light. However, when the applied microwave frequency is equal to the atom transition frequency (6.83Ghz for ^{87}Rb), atoms can decay from $|2\rangle$ to $|1\rangle$, and can be excited again. This microwave resonance (Figure 1.10(c)) can then be detected through a change in absorption of light field.

Frequency stability of RAFS can reach $10^{-11}/\tau^{1/2}$. Since the time RAFS become available commercially, they have been used in cellular telecommunication networks and global navigation satellites systems (GNSS) so that they are nowadays the most common atomic references. However, their power consumption is still large mostly because of the discharge lamp. In addition, size of such clocks is limited by the size of microwave cavity; since the clock frequency is close to 4cm. Then, such atomic clocks are still not suitable for various batteries operated portable applications. Indeed, miniaturization of vapor cell clocks requires avoiding the use of a discharge lamp as well as the microwave cavity.

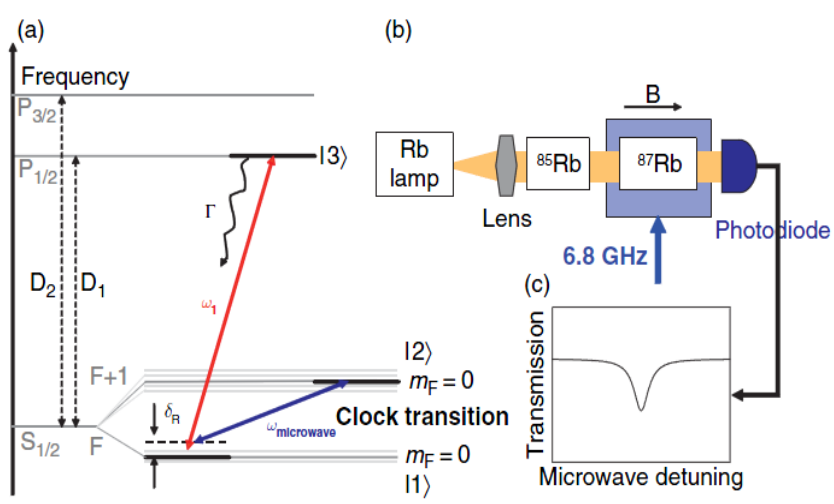


Figure 1.10 Schematic of Rb atomic frequency standard (RAFS), (a) Optically pumped microwave resonance, (b) Spectroscopic set up, and (c) Picture of microwave resonance [Knappe 2007].

During the last decade, significant progress toward the goal to achieve miniaturized version of atomic clock, to use in battery operated portable application, has been done thanks to the availability of single mode vertical-cavity surface emitting laser (VCSEL) with large modulation bandwidth [King 1998] and to the Coherent Population Trapping phenomenon presented in the next section.

1.2.2.2 Coherent population trapping (CPT)

The CPT is a phenomenon that has been observed for the first time in the fluorescence spectra of sodium atoms having dark lines [Alzetta 1976]. It can be explained as a destructive quantum interference effect which occurs when two coherent optical light fields become resonant with ground state transition of alkali atoms. This phenomenon can be described by means of three energy states (if Zeeman degeneracy is neglected), in which two long-lived ground states $|1\rangle$ and $|2\rangle$ split by clock frequency Δ_{HFS} are connected with an excited state $|3\rangle$ in a so-called (lambda) Λ system as shown in Figure 1.11(a). The two light fields E_1 and E_2 with frequencies ω_1 and ω_2 then couple the transitions $|1\rangle \leftrightarrow |3\rangle$ and $|2\rangle \leftrightarrow |3\rangle$. If the frequency difference ω_1-ω_2 matches exactly the clock frequency Δ_{HFS}, then all the atoms are driven into a superposition of the two ground state hyperfine levels that is not coupled to the optical field. This state, so called coherent dark state, traps the atoms which do not absorb light anymore. Such quantum interference phenomenon, called coherent population trapping, is then detected as a local maximum in the transmitted optical power or a local minimum in the fluorescence emission. Hence, it is possible to generate the clock transition from an optical field only [Vanier 1989].

Experimental setup of CPT atomic clock based on a single VCSEL is shown in Figure 1.11(b). VCSEL current is modulated at half of the hyperfine frequency of alkali atom (Rb or Cs). As a result of this modulation, the first two side bands are separated by twice the modulated frequency and are used as the two radiation fields at ω_1 and ω_2. Quarter wave plate is used in order to get circular polarized light required for excitation process by transition selection rules. The resonance cell contains the alkali vapor (Cs or Rb) Figure 1.11(b). When Raman detuning delta= ω_1-ω_2 - Δ_{HFS} is scanned around Zero, CPT phenomenon is observed (Figure 1.11(c)) as a maximum in the transmission of light field.

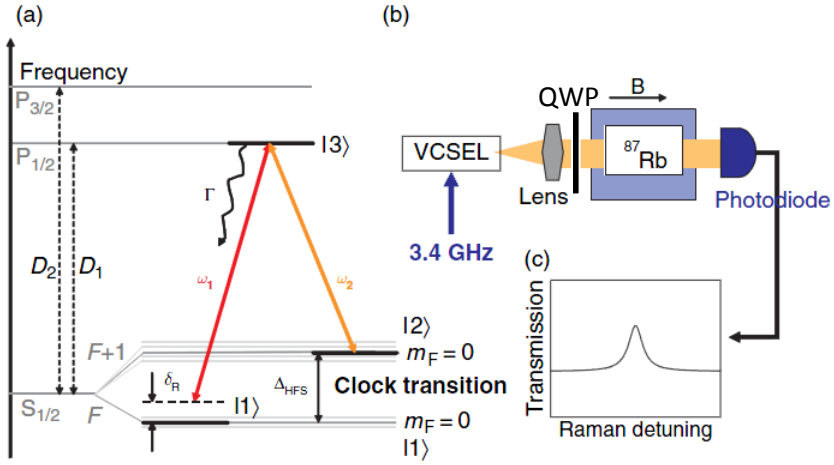


Figure 1.11 Schematic of three level systems to observe (a) CPT resonance, (b) spectroscopic set up, and (c) Picture of CPT [Knappe 2007].

In a perfect three levels system, the transmission of the cell at resonance would be equal to 100%. However, in real case, all the atoms are not trapped in the dark state because of their velocity distribution within the vapor as well as the Zeeman structure. If the degeneracy is broken, and because of the circularly polarized light, the Λ-system (made of $|1, m_f = 0\rangle$, $|2, m_f = 0\rangle$ and $|3, m_f = 1\rangle$) is not a closed system. The atoms e.g. can be optically pumped and pushed until the $|3, m_f = 4\rangle$ level (in case of D_1 line for Cs). Then, they do not participate to the CPT signal whose contrast is much lower than for a perfect three levels system. In the case of Cs, it can be noted that two different excited states can be used ($6^2P_{1/2}$ and $6^2P_{3/2}$) corresponding to D_1 (λ=894.6nm) and D_2 (λ=852.3nm) lines. The choice of the D_1 wavelength rather than D_2 for the MAC-TFC project was dictated by much higher contrast and reduced linewidth of the CPT signal [Lutwak 2002, Stahlar 2002] due to the transitions rules between the ground states and the hyperfine structure of such excited states.

1.2.2.3 Buffer gas

The resonance linewidth should be as thin as possible to obtain good short term stability. Since the lifetime of the hyperfine levels of the ground state of alkali atoms is very large, thinness of the linewidth is limited by the time of interaction. Then, the longest possible time interval for this interaction is most desirable. In atomic beam frequency standards, such time interval is the time of flight through the electromagnetic structure; consequently the physical length of the microwave cavity compared to the atom velocity is the limiting factor. In CPT clocks, the resonance linewidth is actually linked to the dark state lifetime. Since the dark state can disappear when atoms hit the sidewalls of the cell, it is mandatory, especially in the case of MACs where the cell dimensions are small, to find ways to limit collisions.

Adding a selected gas (buffer gas) to the alkali vapor provide a medium in which diffusion limits the rate of movement of the active atomic particles that reduces the number of wall collisions. Later, reduces the residual Doppler broadening through the lamb-Dicke effect [Vanier 1989]. This buffer gas is usually noble gas without any magnetic properties. Practically, utilizing buffer gas along with alkali atoms allows a significant reduction of the resonance linewidth (e.g. from 200 KHz to few kHz) if the buffer gas pressure is sufficient. However, buffer gas collisions and interactions with alkali atoms produce in addition a non-negligible frequency shift of the hyperfine transition [Strumnia 1976, Beverini 1981]. Such frequency shift is pressure as well as temperature dependent. Whereas pressure dependence is little part in 10^7, temperature dependence can be large. Since the absolute value of this frequency shift depends on the gas, one solution is to use a mixture of two buffer gases with opposite temperature coefficient. Such solutions will be explained more in details in the third chapter.

1.2.2.4 Wall coated cells

Wall coating has been shown to be an alternative to the buffer gas introduction. The idea of using wall coated cell was proposed by Norman Ramsey [Ramsey 1983]. He showed that, e.g. Teflon is a good candidate for wall coating since it allows wall collisions without disturbing hyperfine energy states. The experiment, referred to as a broken atomic beam resonance experiment, was performed by Daniel Kleppner who was then a graduate student of Professor Ramsey. Later, paraffin used for wall coating was found to be better than Teflon [Ramsey 1983]. It can be noted that wall coating have been used alone and instead of buffer gas in optically pumped rubidium masers [Davidovits 1966].

1.3 MEMS atomic clock

During the last decade, thanks to Coherent Population Trapping (CPT), availability of VCSELs at proper wavelengths and MEMS technology, different research groups focused their effort on the development of miniaturized atomic clocks, characterized by low power consumption. Indeed, nowadays, more and more applications become mobile and consequently, the demand for small and low-power clocks is increasing. Although less stable than primary standard (short term stability target in the range of 10^{-10}, 10^{-11}), miniaturized clocks are demanded by many civil and military applications ranging from communication systems to global positioning as well as synchronization of communication networks which require frequency sources with instabilities below 10^{-11} over one day, i.e. instabilities that cannot be afforded by quartz-based clocks. Then, miniaturized version of the atomic clock, better known as chip scale atomic clock (CSAC) or MEMS atomic clock (MAC) have been under intense study [Kitching 2002, Lutwak 2003, Liew 2004, Knappe 2005, Perez 2008, Douahi 2007, Nieradko 2008 and Youngner 2007]. MEMS based vapor cells makes possible to reduce the overall size of atomic clock more than hundredfold, as well

as their power requirement and their cost in comparison to the optically pumped atomic clocks. Actually, the first prototype of highly miniaturized atomic clock, proposed by Kitching *et al.* in 2002 [Kitching 2002], was claimed to be one-hundredth of other existing version of atomic clocks while requiring low power. In such miniaturized clocks, the VCSELs and vapor cells are ones of the core components. This section will report the state of the art of MACs.

Schematic of a miniaturized CPT-based clock is shown in Figure 1.12. The main part of such MEMS atomic clock is the physics package which consists in: the micro-fabricated vapor cell, the VCSEL and photodetector, the optics for collimation and polarization beam shaping, the heaters for temperature management, and finally the coils for static magnetic field generation and the magnetic shield.

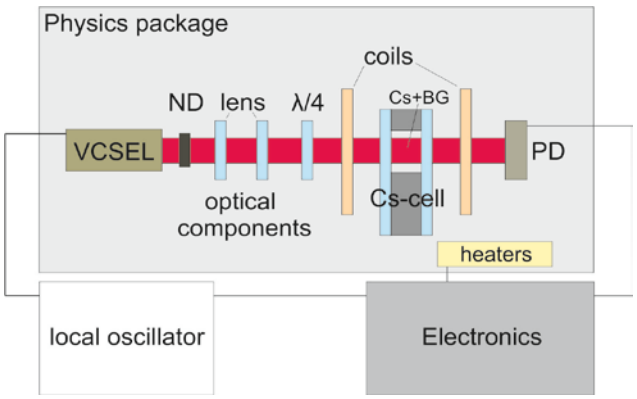


Figure 1.12 Schematic of CPT based micro atomic clock consisting in three major parts, physics package, local oscillator, and control electronics.

1.3.1 VCSEL

In order to achieve the CPT effect, it is possible to use two separate lasers, or a laser and an electro-optical modulator. However, since the hyperfine splitting between the two ground states is rather small, it is also possible to produce a light beam with the two required wavelengths by modulating a single laser source with a frequency that is equal to half of the hyperfine splitting frequency, then using the modulation sidebands. Vertical-Cavity Surface-Emitting Lasers (VCSEL) are ideal laser sources for this purpose owing to high speed, high-efficiency modulation capability and low power consumption. The VCSEL is a type of semiconductor laser diode with laser beam emission emerging from the top surface, contrary to conventional edge-emitting semiconductor lasers which emit from surfaces formed by cleaving the individual chip out of a wafer. VCSEL has several advantages over conventional edge-emitting laser diodes, such as:

- Circular output beam
- low power consumption,

- capability of on-wafer testing,
- simplified packaging,
- longitudinal single-mode emission spectrum, and
- Suitability for 2D-array integration.

For miniaturized atomic clocks, the same gases as in more classical atomic clocks are used, namely Rb and Cs, requiring laser wavelengths of 780.2 nm (Rb D_2 transition), 795.0nm (Rb D_1), 852.4 nm (Cs D_2), or 894.6 nm (Cs D_1) [Serkland 2006]. For MAC-TFC project, Cs has been chosen, and as mentioned earlier, the D_1 optical transition was preferred because of a higher figure of merit.

Several specific requirements [Serkland 2006] are needed for CPT based clocks. First, the single-mode VCSEL has to emit at the correct wavelength of D_1 line of Cs with a narrow linewidth, then, single polarization (linear) is required to be able to convert it into circular polarization using a quarter wave plate. In addition, low threshold current (for low power consumption) as well as sufficient modulation bandwidth (~5 GHz) at low driving current is needed. Finally, high operating temperature (60-80°C) and low relative intensity noise (RIN) is mandatory. In the framework of the MAC-TFC project, the University of Ulm (Germany) developed dedicated VCSELs working at λ=894.6nm. One distinctive feature of these VCSELs is the integrated grating patterned onto the top Distributed-Bragg-Mirror. Made of GaAs by electron beam lithography, this subwavelength grating allows differentiating the thresholds between parallely and perpendicularly polarized modes (by changing the top mirror reflectivity). It leads to a polarization ratio greater than 25dB without increasing significantly the threshold current. For MAC-TFC, flip-chip bondable VCSELs (300x300μm^2) with low-threshold current and sufficient modulation bandwidth (>5 GHz) at low driving current while operating at high temperature (80°C) have been developed [Al-Samaneh 2011].

1.3.2 Circular polarized light

For CPT in miniaturized atomic clocks, only $m_f = 0 \rightarrow 0$ Zeeman ground states are used in the Λ system (Figure 1.13) as they are less sensitive to the external magnetic field (only quadratically sensitive). In order to excite this Λ system between $m_f = 0 \rightarrow 0$, circular polarized light (σ^+ or σ^-) is required to optically pump the atoms into the common excited state since linearly polarized light fields (π) would not connect $m_f = 0$ of the ground states to the common excited state due to electric dipole selection rules. However and as explained earlier, it can be noted that circularly polarized light tends also to pump the atoms into $|F = 4, m_f = 4\rangle$ Zeeman state (Figure 1.13) because the dipole selection rules allow the excitation of all Zeeman ground states except the $|F = 4, m_f = 4\rangle$ which does not participate to the CPT [Huang 2007].

The CPT contrast is then reduced. To produce the circularly polarized beam, a quarter wave plate is placed before the vapor cell (Figure1.12).

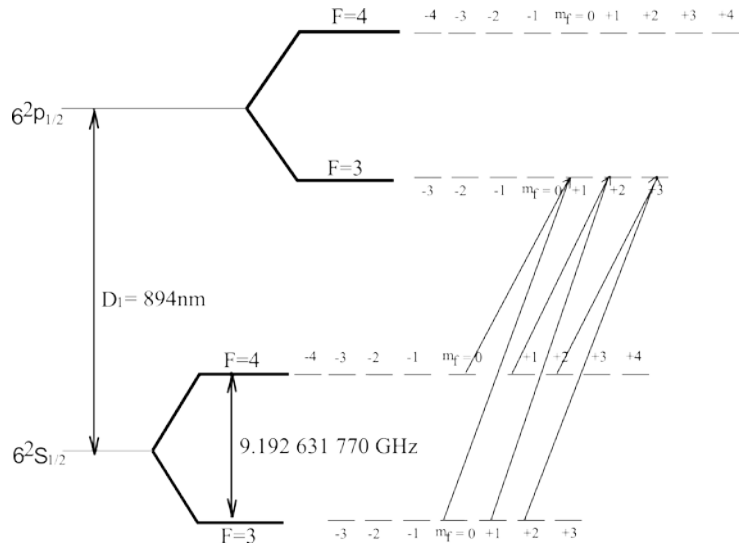


Figure 1.13 Three-level transition system or Λ system in the Cs.

1.3.3 State of art of MEMS atomic clock

Since the first idea of MEMS based frequency references has been presented, various efforts and inputs (helped by DARPA program in United States since 2001 and French and European funding in Europe since 2005) have been done in the development of MEMS based clocks by different research and industrial groups (NIST, Symetricom/Sandia, Honeywell, FEMTO-ST, etc.) around the world. Brief description of their achievements is presented below;

1.3.3.1 NIST

NIST was the first group to theoretically propose a MEMS based frequency reference in 2002 [Kitching 2002] and to demonstrate a first prototype of Chip-scale-atomic-clock in 2004 [Knappe 2004, Knappe PTTI 2004].

Figure 1.14 shows the demonstrator of the chip-scale-atomic-clock physics package. It consists in four main parts; a VCSEL at the bottom; optics (neutral density, quarter wave plate and collimating lens) and micro-fabricated vapor cell and photodiode at the top. The microfabricated vapor cell is a sandwiched type structure in which cavities, made of silicon, are sandwiched between two glass plates. Fabrication steps of such vapor cell are shown in the Figure 1.15.

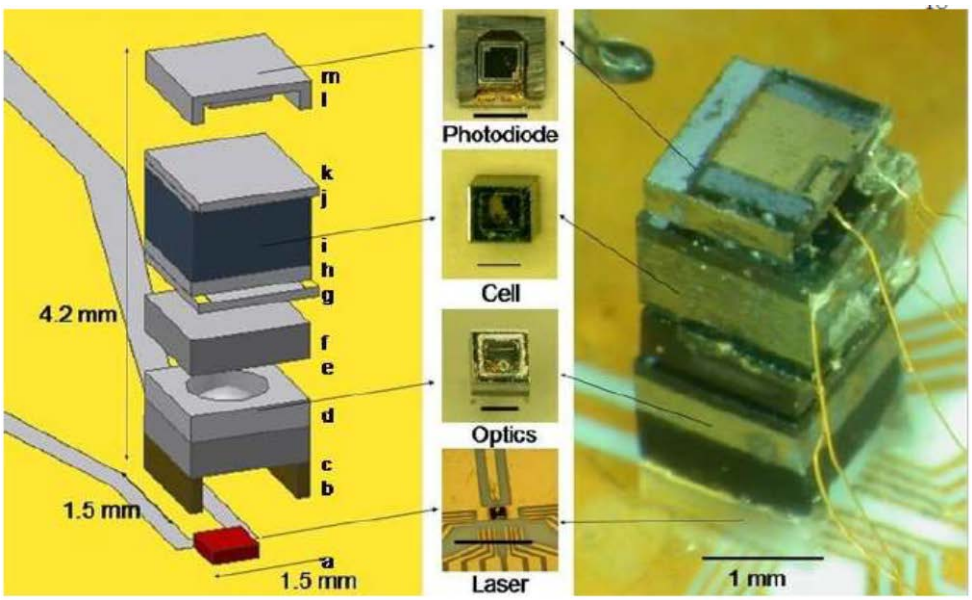


Figure 1.14 First chip-scale atomic clock demonstrated at NIST [Knaape PTTI 2004].

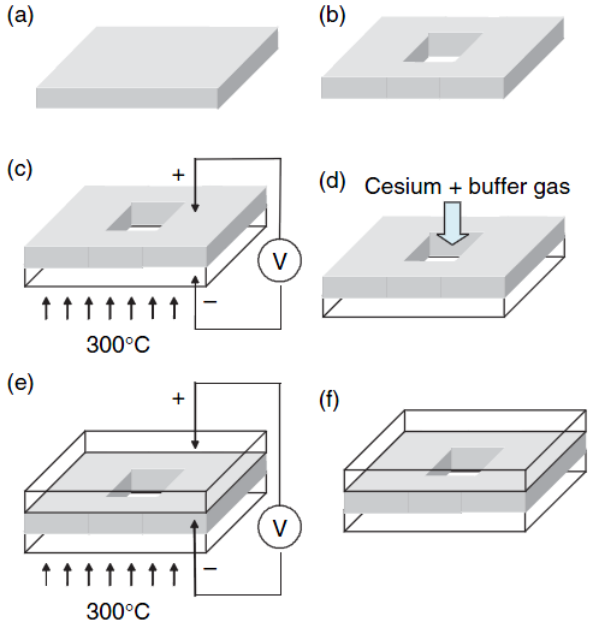


Figure 1.15 Schematic of fabricated Cs cell filled with Cs and buffer gas [Liew 2004].

After generating the cavities in silicon (by wet etching - KOH - or Deep Reactive Ion Etching), a first anodic bonding is performed, before to fill the cells with Cs in buffer gas atmosphere. The second anodic bonding is then performed to seal the cells. Vapor cells are filled with a mixture of buffer gas (argon and neon) at a pressure of 25kPa. In order to increase the density of Cs, the cell is heated at a temperature of 85° so that at least 30% of light is absorbed. In addition to the cell, the VCSEL delivers a signal at λ=852nm (D_2 line) which passes through the cell and is then detected by the photo-detector.

Total size of the physics package is 9.8mm^3 with 0.8 mm^3 vapor cell interior volume. The achieved short term frequency stability was 3x10^{-10} for 1s integration time [Knappe 2004]. Further, because of more favorable selection rule of D_1 line of Rb over D_2 line of Cs, such short term frequency stability was improved [Knappe PTTI 2004] near an order of magnitude. Figure 1.16 shows the measurement of Allan deviation at various integration time for this chip scale atomic clock where fractional instability of 6x10^{-11} was measured at 1s integration time and 4x10^{-11} at 1000s for the Rb cells (D1 line).Long term stability of such frequency references at the primarily level was reported by a substantial linear drift of the fractional frequency of roughly -2×10^{-8}/day. But such frequency drifts are still under study in order to improve the long term stability of CSAC. It can be noted that NIST CSAC has not yet been commercially available.

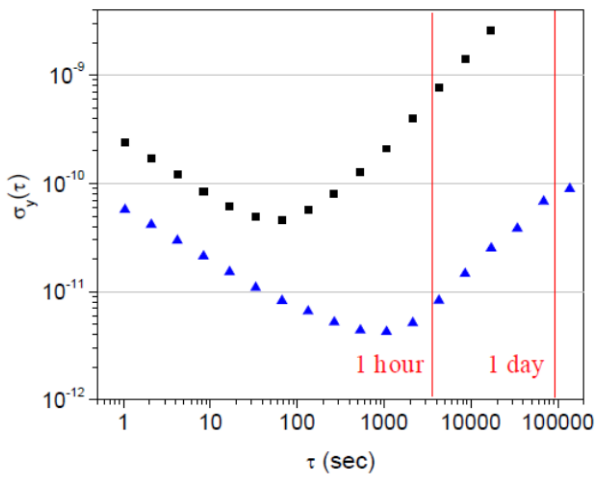


Figure 1.16 Allan deviations for the CSAC for the D2 line [Knappe 2004] of Cs (squares) and for the D1 line of Rb [Knappe PTTI 2004] (triangles).

1.3.3.2 Honeywell

The main issue with all MEMS based atomic clocks is that cost of manufactured parts is dominated by the cost of packaging and assembling of the components. Honeywell lab tried to decrease such problem by developing solutions aiming to facilitate the assembly and packaging, i.e. by doing most of the integration of clock components at wafer level [Youngner 2007]. Honeywell developed the design and processes for an atomic clock having a total volume of 1.7 cm^3 that consumes 57mWatts and shows instability of 5x10^{-12} over one hour, which is comparable to many of the larger commercially available atomic clocks. This atomic clock (described in Figure 1.17) is based on the D_1 line of Rb.

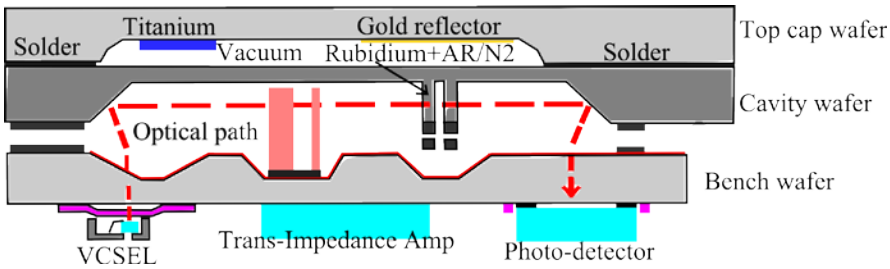


Figure 1.17 Schematic of CSAC proposed by the Honeywell [Youngner 2007].

Most of the components are placed onto three wafers that are bonded together at wafer level. Bottom wafer (Pyrex) acts as a bench where all optical components are integrated such as VCSEL, photodetector on the back side and neutral density and quarter wave plate on the other side. Middle wafer is made of silicon where KOH-etched cavity with 54.7° planes that allows to direct the light into a suspended and transparent Rb cavity. Top and third wafer is made of Pyrex and contains a titanium getter to preserve the vacuum around the cell. To interrogate the alkali atoms, two refractions through the lower glass wafer and two reflections at silicon (111) 54.7° planes take place. SEM images of fabricated Rb cavity are shown in Figure 1.18 where the suspension springs for thermal control can be noticed.

Measurements of Allan deviation for Honeywell CSAC are shown in the Figure 1.19. Short term frequency stability was measured to be 1.5×10^{-10} at 1s and long term frequency shift of 0.06Hz/day, which is below the requirements set by the DARPA project.

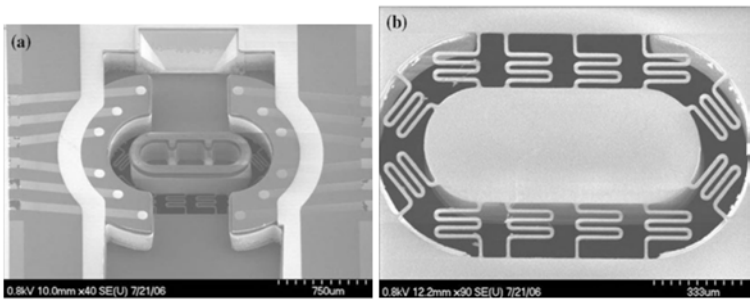


Figure 1.18 SEM images of front and back side of Rb cavity used in the design of Honeywell CSAC [Youngner 2007].

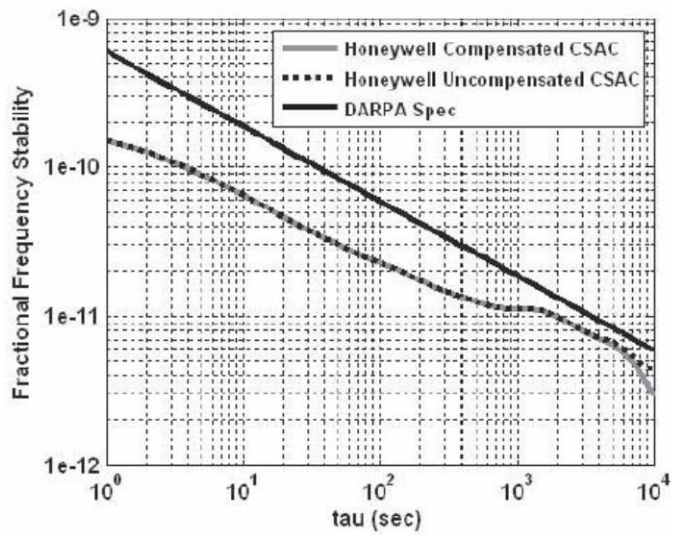


Figure 1.19 Frequency instability measurement of Honeywell CSAC [Youngner 2007].

1.3.3.3 Symmetricom/Sandia CSAC

Symmetricom has been also involved in the development of CSAC project funded by the DARPA. The Symmetricom designed and developed (Figure 1.20) a CSAC in collaboration with Sandia National laboratories which is one of the most advanced and complex CSACs reported. In the beginning of the CSAC project, several parameters for the clock has been studied and optimized for conventional double resonance interrogation and CPT as well [Lutwak 2002]. They also compared D_1 and D_2 Cs line based CPT resonances and, as mentioned earlier, showed that D_1 resonance provides 3-4 times better figure-of-merit [Lutwak 2003**]**. Their first prototype was then presented in 2005 [Lutwak 2005] having a size of $10cm^3$ and a measured short-term stability of $4x10^{-10}$ for 1 to100 seconds while consuming only 155 mW of power. This design is based on the suspension of the vapor cell (compatible with MEMS technology) as shown in the Figure 1.20 to minimize conductive thermal losses. Heart of the physical package is the silicon cesium cell designed as a sandwich of two layers of 250 µm thick glass (Pyrex™) spaced by 1500 µm thick silicon wafer.

In 2007, Symmetricom built and tested 10 miniature atomic clock prototypes, with volume ≈15 cm3 and power consumption ≈125mW. All 10 devices exhibit short-term stability of $3x10^{-10}$. Over a temperature range of 0-50°C, the power varies by less than 5 mW. The frequency drift, based on long-term measurements of a single unit, is better than $1x10^{-10}$/month, after 200 days of operation. Nowadays, CSAC demonstrated at Symmetricom is the only miniaturized atomic clock available commercially.

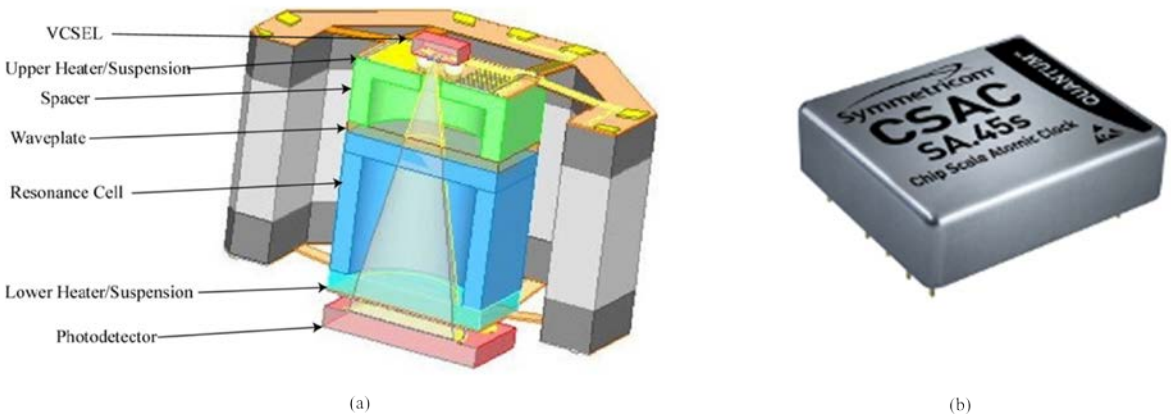


Figure 1.20 Symmetricom CSAC; (a) physics package (b) fully assembled clock [Lutwak, 2007].

1.3.3.4 European version

In Europe, technology development for the microcell for MEMS atomic clock started in 2005 at FEMTO-ST with the idea of Cs filling method using Cs dispenser [Douahi 2007]. Functioning of dispenser based microcell was reported in 2007-2008 [Nieradko 2008, Douahi 2007] and shows the stable and improved cell gas environment. Fabrication process of FEMTO-ST microcell is shown in Figure 1.21. During this work, microcell technology has been characterized and showed reliability for the batch process. The tests performed showed absence of degradation of the absorption signal demonstrating the potential of such technique to ensure high stability of cesium contents inside the microcell [Douahi 2007].

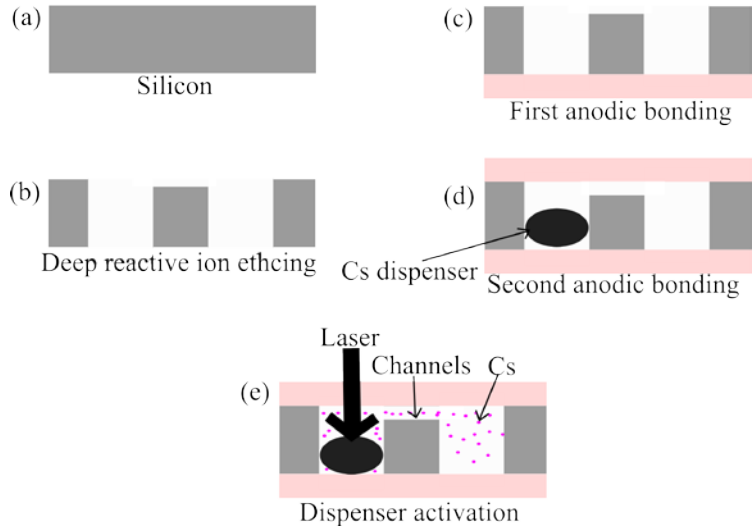


Figure 1.21 Fabrication process for Cs vapor cell using Cs dispenser to fill the cavities with Cs by means of laser light after the complete sealing of cavities.

1.3.3.5 Focus on alkali atoms filling

Filling the microcell with alkali atoms is actually a key step of the microcell fabrication.

At NIST, different methods have been proposed for this purpose [Liew 2004]. In one of those, a stable cesium compound is deposited into the cells [Liew 2004, Knappe 2004, Knappe 2005] and reacts to produce the pure cesium by using the following reaction:

$BaN_6 + CsCl \rightarrow BaCl + 3N_2 + Cs$

The decomposing starts at 200°C inside UHV chamber. The problem in small cells is to pump off nitrogen from the cell without pure Cs metal leaving the cells at elevated temperature. Whereas in big cells, remaining barium can be useful as it behaves as a getter for residual nitrogen, in small cells at high temperature, this gettering process can change significantly the cell pressure that results in clock frequency changes [Knappe 2005]. Since the clock frequency of cesium is very sensitive to the nitrogen pressure [Beverini 1981], pressure needs to be stable at 2 Pa to get frequency stability of 1x 10^{-11}.

Another method used by NIST group was to insert Cs by micropipetting [Liew 2004, Knappe 2004] into the opened side of cavities before to seal the cavities under the buffer gas atmosphere by anodic bonding (Figure 1.15). Although this method seems simple and inexpensive, it is difficult to control the anodic bonding chamber environment during sealing of cavities containing Cs. As for the first method, the presence of volatile alkali metal complicates the operation of anodic bonding (used to seal the cavity) usually performed at high temperature since there is a large probability of Cs to react with residual oxygen. This reaction can produce Cesium oxide along with other gases inside the cells. Those gases can in turn affect significantly the clock stability since it is more difficult to achieve controlled mixtures of different buffer gas [Vanier 1982] for temperature coefficient compensation. Above all that, direct injection of liquid alkali elements or utilization of barium azide and alkali chloride limit the anodic bonding temperature to 250°C if one wants to avoid alkali atom vaporization onto the surfaces to be bonded. Such temperature is not sufficient to ensure a strong sealing of cavities. It can be noted that a strong sealing of silicon/glass surface requires a bonding strength of at least 30MPa [Dziuban 2006] and that it is not possible to obtain bonding strength over 20 MPa for temperatures below 250°C. Thus, in order to have strong enough anodic bonding process, temperature needs to be around 350°C-400°C.

In order to overcome such technical problem of cell filling method, several solutions have been tried. For instance, one method [Radhakrishnan 2005] was based on encapsulated rubidium in wax micro-packets as shown in Figure 1.22. Performance of such method for the application of atomic clock is still not reported. Further vapor cells containing Cs and nitrogen have been made by [Liew 2006] in which deposited thin

film of Cs azide is evaporated in the cavity, thanks to exposition to ultraviolet light, after the sealing of cavity using anodic bonding. However, the main disadvantage of this method is UV exposure duration to release the Cs which can take up to 100h. In another method reported by Gong [Gong 2006], glass used for sealing the cavity has a part enriched with Cs that is partially melted by local heating after the anodic bonding (Figure 1.23) to release the Cs inside the cavity.

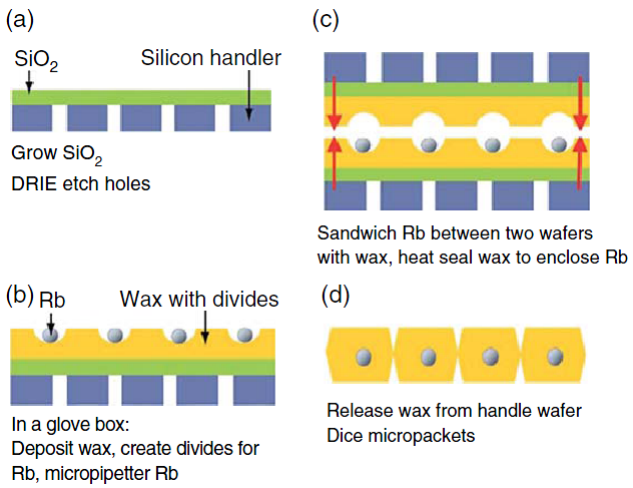


Figure 1.22 Process to enclose the Rb in wax micopackets [Knappe 2007].

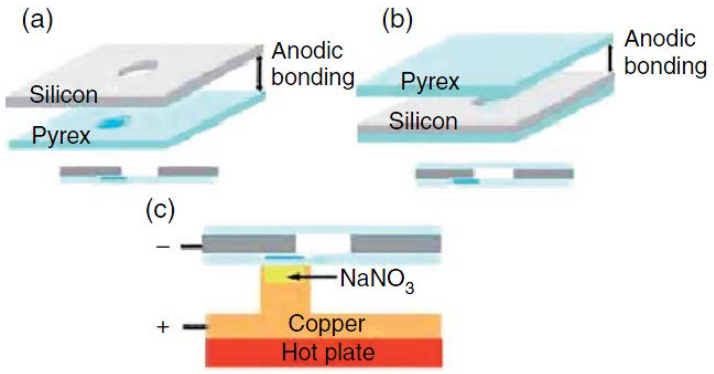


Figure 1.23 Process of fabrication of vapor cell using Cs enriched glass to fill the cavity with in Cs and buffer gas (a) Silicon with through etched hole with glass wafer consisting Cs enriched part (dark blue) (b) sealing of silicon/glass structure with another glass by anodic bonding (c) releasing Cs by heating Cs enriched glass side close to dark blue part of glass [Knappe 2007].

In this framework, the method proposed at FEMTO-ST [Douahi 2007] was based on the generation of Cs vapor from a solid Cs alloy (provided by SAES Getter company) stable at temperatures used during anodic bonding. The pill-like dispensers are made by mechanically cutting a “wire” of Cs dispenser. Such Cs dispenser contains a mixture of an air-stable Cs compound which remains stable up to at least 500°C.

The used Cs dispenser includes a mixture of Cs chromate and alloy of percent composition by weight Zr 84% -Al 16%. Then, the Cs vapor can be released from the alkali metal dispenser by heating (= activation of the dispenser) according to the following reaction:

$$2Cs_2CrO_4 + Zr_3Al_2 \rightarrow 2\ Cs\ [gas] + Cr_2O_3 + Al_2O_3 + 3ZrO_2$$

Once the cavity is sealed, local heating of the dispenser is then performed by laser illumination through a glass window. The Cs vapor migrates to the test window via channels connecting the two cavities as it can be seen on Figure 1.21(e). Complete fabrication process for such cells is shown in Figure 1.21.

1.4 MAC-TFC approach

Based on first developments concerning microcell fabrication made at FEMTO-ST, a collaborative European project called Micro-Atomic Clock for Timing, Frequency Control & Communications (MAC-TFC) was funded in 2008. The goal of MAC-TFC project is to develop and demonstrates all the necessary technology to achieve an ultra-miniaturized, low power cesium atomic clock, presenting a short term stability of $5x10^{-11}$ over 1 hour while operating on the power of an AA battery, with less than 200mw power consumption. MAC-TFC brings together a consortium made of four major academic institutions, FEMTO-ST (coordinator), University of Neuchatel, Wroclaw University of Technology, University of ULM; and research institutes, VTT and CEA-Leti; and three industrial partners, SAES, Italy, SWATCH Group and Oscilloquartz from Switzerland.

1.4.1 General approach and objective of MAC-TFC

The approach of MAC-TFC is to rely on MEMS technology with its ability to shrink mechanical feature and mechanism down to micron scales, to provide substantial size and power reduction of frequency and timing references. MAC-TFC aims to achieve a European version of integrated portable atomic frequency references with comparable performance than the competing target US version.

Identified research issues which have been included in MAC-TFC program are;

1. Temperature stability, magnetic shielding, hermetic encapsulation and means to maintain atomic ground-state coherence within the confinement cell
2. Dispensing and activation of Cs vapors as well as gettering of internal atmosphere of micro-cell
3. Vertical cavity surface emitting laser (VCSEL) working on Cs D1 line with high operating temperature and stable polarization.
4. Assembling and 3D packaging

5. Miniaturized low power ASIC integration of analog Radio Frequency (RF) and Phase locked electronic.

Three kind of different architectures of vapor cell (T, R and I-cell) were proposed for MAC-TFC program whereas at femto-st Besancon, we studied two kind of vapor cells, one is transmissive version of vapor cell (T-cell) privileging high frequency stability with Allan deviation around $5x10^{-11}$ over 1 hour based on a sandwich glass-silicon-glass structure (Figure 1.24). The other proposed version of vapor cell (R-cell) is based on the reflection of light inside the silicon cavity allowing an adjustable optical path (Figure 1.25).

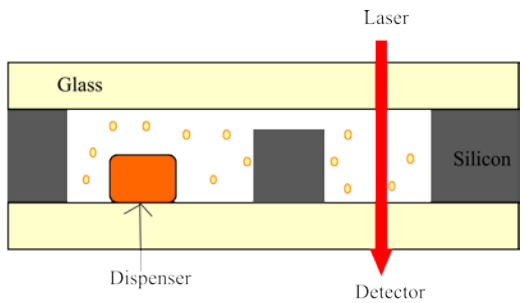


Figure 1.24 Transmissive version of vapor cell.

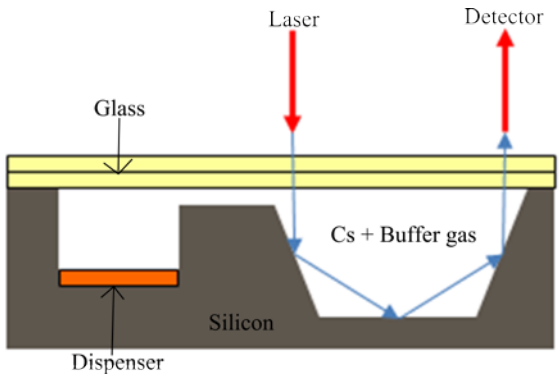


Figure 1.25 Scheme proposed for reflective version of vapor cell in the beginning of MAC-TFC project.

To get complete demonstration of MEMS atomic clock, various technical challenges concerning the microcell, which will be considered in the next chapters, were studied;

1. First challenge was to fabricate the vapor T-cell with improved alkali-atom filling along with inserting buffer gas inside the cell at controlled pressure (to control the atom-wall collision which degrade the quality of CPT resonance and improve the short-term stability). (second chapter)
2. Second challenge was to control the power budget for complete MEMS atomic clock T-cell package (third chapter)
3. Third challenge was to develop the second architecture called the R-cell (fourth chapter). .

By keeping in the mind the initial goal and parameters set in the beginning of the project, this thesis work is devoted to technology development of vapor cell and thermal analysis of fully packaged micro clock in order to optimize the packaging with controlled thermal environment around the cell.

Chapter 2 Technology and testing of transmissive version of atomic vapor cells

In this Chapter we describe the transmissive version of our wafer-scale alkali vapor cells based on silicon micromachining and anodic bonding. The principle of proposed micromachined alkali cell is based on an extremely compact sealed vacuum cavity of few cubic millimetres containing Cs vapor and a unique buffer gas (Ne). The optical cavity of transmissive micro-cell (T-cell) is illuminated by a high-frequency modulated laser beam. The alkali cells are formed by sealing an etched silicon wafer between two glass wafers. The technique of cell filling involves the use of an alkali dispenser. The activation of cesium vapors is made by local heating of the dispenser below temperature range causing degradations of cesium vapor purity. Thus, the procedure avoids negative effects of cesium chemistry on the quality of cell surfaces and sealing procedure. To demonstrate the clock operation, cesium absorption as well as Coherent Population Trapping resonance was measured in the cells.

2.1 Approach of fabrication and dispensing of micromachined Cs vapor T-cell

Recently, different methods of filling the micromachined MEMS (microelectromechanical systems) cell with alkali vapors (Cs or Rb) and introducing the buffer gas have been reported by several US teams which are described with their respective technology in the chapter 1 and briefly explained below:

- Pipetting of liquid Cs or Rb drops under anaerobic atmosphere [Liew 2004, Lutwak 2004],
- Formation of atomic Cs vapor by thermally activated chemical reactions between barium azide (BaN_6) and cesium chloride inside vacuum sealed cell [Liew 2004],
- Formation of Cs vapor by UV-light induced decomposition of thin-film deposited cesium azide (CsN_3) inside high-vacuum sealed cell [Liew 2007],
- Laser ablation of liquid Cs encased in metal-wax micropackets [Radhakrishnan 2005], and

- Evaporation of alkali atoms into a micromachined cell cavity through a glass nozzle [Knappe 2005].

In the first three methods, the filling of Cs vapor inside the micromachined cavity is made prior to its sealing. The resulting alkali cells is formed by sandwiching a silicon wafer with a through-hole between two glass plates and joining silicon and glass plates by means of anodic bonding. The difficulty of anodic bonding and mechanically weak glass/silicon sealing done under non optimal conditions (low temperature ~250°C, short process) are the drawbacks of first and second methods. Advantageous feature of the third method is higher temperature of anodic bonding (~350°C) giving stronger sealing, but UV-light induced decomposition of cesium azide needs 12-hours processing. Finally, in all methods, unwanted products of chemical reactions or results of laser treatment influence negatively the quality of cell. Additionally, anodic bonding process done at low temperature, introduces increased degassing of oxygen, hydroxide groups and water from bonded interface. Oxidizing agents react with atomic Cs, resulting in a short-term instability of the parameters of atomic clocks. Even if the previous methods improve relatively the purity of alkali atmosphere of the micro-cell, there is a need for techniques in which the conflict of anodic bonding process with cesium chemistry is fully avoided, improving its potentiality of mass production. Pursuant to solving this problem, FEMTO-ST proposed [Douahi 2007] an approach making the fabrication of atomic micro-clock much simpler. This solution uses a Cs dispenser commercially available from SAES Getters, making possible to heat locally the Cs dispenser inside sealed micro-cell. It is made below the temperature range causing degradation of micro-cavity as well as reducing the negative effects of Cs chemistry. This will improve the control of internal cell atmosphere purity as well as the presence of buffer gases.

The development of MEMS technologies permits to push the miniaturization of atomic clock cell, making the fabrication simpler and increasing the potentiality for mass production. As previously reported, the solution developed by US teams is commonly based on the fabrication of alkali cells formed by sandwiching an etched silicon wafer between two glass wafers, as shown in Figure 2.1.

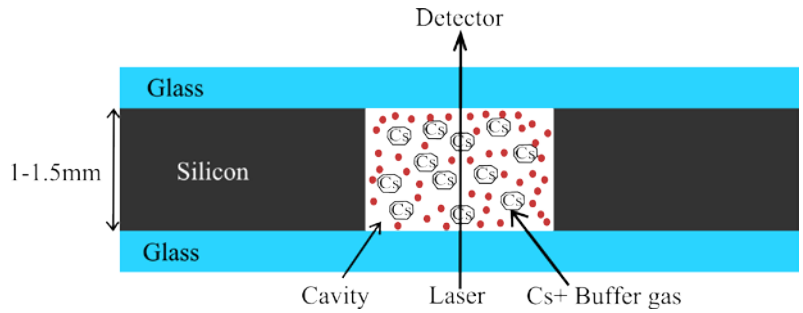


Figure 2.1 Architecture of transmissive micro vapor cell (T-cell).

However, atomic clocks based on highly miniaturized alkali cells present lower short-term frequency stability when compared with compact atomic clocks based on larger cells. This is due to the shorter interaction of read-out laser beam with Cs atoms as well as more frequent collisions with side walls of cell. The frequency stability of atomic clocks is usually characterized by Allan deviation, which measures the fractional frequency uncertainty of the atomic clock output frequency when it is averaged for a time less than 10 seconds. It has been demonstrated in [Kitching 2002] that a short-term relative frequency stability of $1x10^{-11}$ can be potentially obtained with 1.5-mm length and lateral surface of 3.9 mm^2 of the cell.

Our approach of fabrication propose a wafer-scale method for filling the MEMS cell with atomic Cs and a buffer gas, based on the activation of Cs vapor from a solid pill made by mechanical cutting the wire of Cs dispenser, available from the company SAES Getters. The dispenser material is a mixture of Cs compound with a reducing agent compressed together. Similar materials are used for the release of alkali metals for organic light emitting displays (OLEDs) [Boffito 2004].

The Cs dispenser contains a mixture of an air-stable Cs compound with a reducing agent, presenting high stability up to temperatures of at least 500 °C. The used Cs dispenser includes mixtures of Cs chromate and an alloy of percent composition by weight Zr 84% - Al 16% (also known as St 101®). The Cs dispenser can release the metal by simple heating. Thus, Cs evaporates from alkali metal dispensers by the following reaction:

$2\ Cs_2CrO_4 + Zr_3Al_2 \rightarrow 2Cs\ (gas) + Cr_2O_3 + Al_2O_3 + 3ZrO_2$

Many buffer gas candidates have been extensively characterized and optimum mixtures have been developed in particular for Rb-buffer gas. However, to date a very little data are available on Cs-buffer gas collisional shifts. We demonstrated that N_2 is not applicable because of strong absorption by the used Cs dispenser.Since Cs dispenser does not react with noble gases, T-cells were firstly constructed with a

spectrum of well-controlled partial pressures of Ar and Ne. Recently, we demonstrated experimentally the temperature-dependence cancellation of the Cs clock frequency in a T-cell filled with a unique Ne buffer gas at an operational temperature of 80°C [Miletic 2010]. In consequence, the T-cell reported in this manuscript will be filled by only one buffer gas Ne, situation releasing the difficulty to control precisely the content of buffer gas mixtures

The proposed micro-cell is formed in a wafer of silicon with glass wafers bonded to both sides, containing two cavities, as shown in Figure 2.2. The first cavity is playing the role of dispensing cavity where the metallic Cs dispenser is placed. The second cavity includes the measuring window, where the laser beam generating the CPT signal is collimated to measure the absorption of Cs atoms. Both cavities are connected by a filtration mesh. Internal volume of alkali cell reaches 20 mm^3.

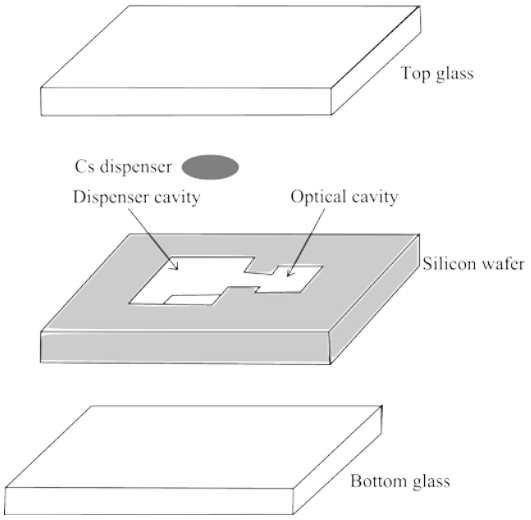


Figure 2.2 Schematic of Cs micro-cell based on silicon etch, anodic bonding and dispenser technology.

2.2 Fabrication process flow of T-cell

The T-cells are formed by sandwiching a Si wafer, with two cavities etched through it, between two borosilicate glass wafers anodically bonded. Typically, the size of interior volume of the cells is about 20 mm^3, with the diameter of circular optical cavity of 2 mm and square dispenser cavity of size 1.65x1.65 mm^2. These cavities are connected through filtration channels which is blocking the contamination from the Cs dispenser during its activation process. Figure 2.3 shows schematic of fabrication process that is similar to that described in [Kitching 2002], developed for microcells without the buffer gas. Double polished p-type (100) Si wafer (1.4 mm thick, 4”) is photo lithographically patterned and etched in using deep RIE to produce an array of the optical and Cs dispenser cavities (through holes) and the surface filtration channels (20 µm-wide and 0.9 mm-deep trenches), as shown in Figure 2.3(b). Then, borosilicate

glass wafer (Borofloat 33, Schott®) was anodically bonded to silicon in the vacuum chamber to obtain an forming an array of sealed Si/glass cavities (see Figure 2.3(c)). Subsequently, the operation of dispensing starts by introduction of the Cs dispensers into the dispenser cavities. The sample is placed on top of a heated table in vacuum chamber of the anodic bonder while the cover glass wafer is positioned above the Si substrate, distanced about 200 µm and maintained using electromagnetically removable flags. The inner gas atmosphere is evacuated to obtain vacuum and the chamber is pressurized in presence of buffer gas (Ar or Ne) at a required pressure. The top glass is finally sealed by the second anodic bonding, as shown in Figure 2.3(d).

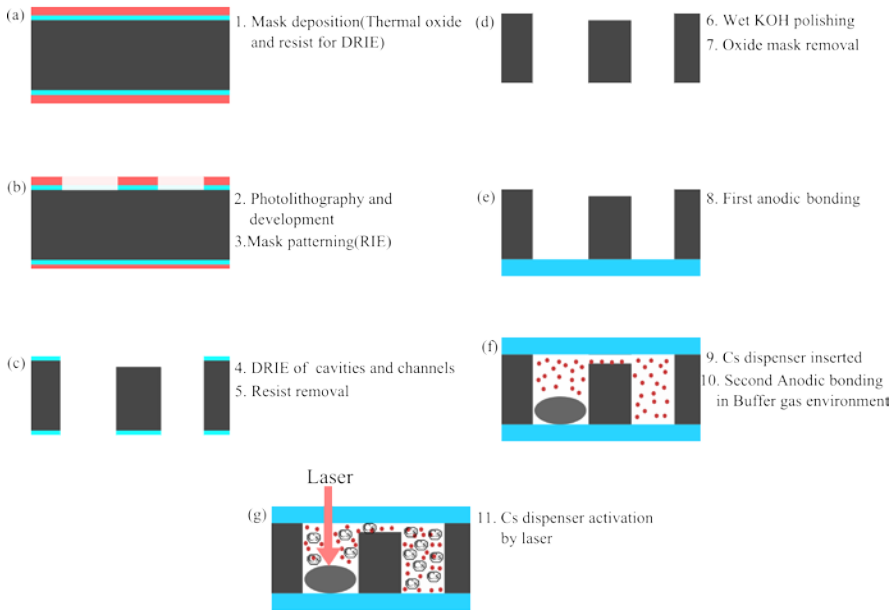


Figure 2.3 Microfabrication process steps for T-cell fabrication.

2.3 Smoothing out the side walls of T-cell cavity

For silicon etching of T-cell, sidewall quality is critical to atomic clock performances. When developing smooth-sidewall process, excess passivation of metal cesium on the rough sidewalls must be avoided because it will decrease the amount of active alkali metal within the atomic clock cavity. Two approaches have been tried to achieve optically smooth sidewall quality: an optimized process based on the classic Bosch process and a process using an aqueous solution of etchant KOH to smooth the surface as well as to remove the fluorocarbon contaminants remaining after DRIE process. This double-step procedure combining the dry etching with wet etching permits to smooth the surface roughness generated by standard Bosch process of DRIE.

2.3.1 Optimizing the etch parameters of DRIE process

There are two main well known approaches for sidewall etching: the Bosch process used here and Cryo process. The mechanism of Bosch process, described in Appendix (A.2.2.3) etches via sequential etches and deposition steps using SF_x and C_xF_y plasmas [Laermer 1996]. The etch-to-deposition ratio process parameters determine sidewall roughness (i.e., scallop size), removal of deposited material and the deposition rate of the polymer layer. The vertically directed ion bombardment of classic RIE is repeatedly interrupted here by passivation periods [Wu 2010] which coat the sidewalls and trench bottom with a thin layer of polymer. During etching the trench bottom polymer is preferentially removed, followed by a short isotropic silicon etch. The resulting sidewalls should be near vertical, reflecting an overall balance between the etching and passivating steps, but with a scalloped appearance due to alternating etches and passivation cycles. Scallop size depends on cycle times and plasma parameters, such as coil power and pressure, rate of removal of deposited material and the deposition rate of the C_xF_y polymer.

Thus, Bosch process can lead to bowing of high aspect-ratio (HAR) structures, made with high etch rate when operating in presence of SF_6 as etch gas and CHF_3 (or C_4F_8) and Ar used as a passivation gases. Bosch process became very useful for HAR silicon etching of MEMS devices requiring important deepness of trenches in the range from few microns to several hundreds of microns. In our application of vapor T-cell, we need to etch a 1.4-mm thick cavity which is of extremely deep.

It was demonstrated that by simply reducing the overall cycle times and maintaining the continuous flow of etch gas with same etch-to-deposition ratio, scallop size can be reduced [Ayon 1999], smoothing the roughness of cavity side walls. However, the application of such unique procedure can result in reduced etch rate, increasing the time of DRIE. Here, continues flow of gases helps to reduce the scallop size resulting from the succession of etch and passivation steps. There are several features of DRIE such as profile angle of trenches, uniformity and anisotropy are related to the pattern geometry and these features are strongly depending on etching parameters such etch rate, step time (etch and passivation cycling times), process temperature gas flow, gas pressure, operating RF power, aspect ratio dependent etching (ARDE), and micro loading. The effect of some of these parameters will be now briefly discussed:

- Gas flow dependence. Etch rate of silicon increase with the SF_6 flow. In practice, for a particular flow of fluorine there is a point at which more power is required to ionize the SF_6 gas, and if this power is not supplied then the additional gas will not ionized resulting in no change of etch rate.
- Pressure dependence. The process pressure has a great impact on etch results. Generally, higher etch pressures lead to higher etch rates resulting from the increased number of SF_6 radicals

available. However, in certain situations increasing pressure of SF_6 gas further results in an etch rate decrease [Ayon 1999]. So SF_6 flow as well as pressure of gases must be optimized for each specific application. Thus, SF_6 gas flow Bosch process was characterized by [Mizuhata 2008**]** for the pillar like shape and trenches with the reduction of scalloping effect. Further silicon etch rate also decreases as the depth or aspect ratio AR [Taylor 2006]. Further various silicon etch rate at high aspect ratio were reported [Kiihamaki 2000] with conclusion that at high aspect ratio the profile of trenches made at high pressure present an effect of positive angle, as shown in Figure 2.4. In conclusion, processing high aspect ratio structures at high pressures causes such bowing and closing up towards the base of the trenches due to the increased scattering of ions at high pressure. Keeping the process at low pressure results in better profile angle. However, this will also reduce the selectivity of the masking material as a consequence of the increased ion energy because the selectivity of the resist decreases with the decreased process pressure.

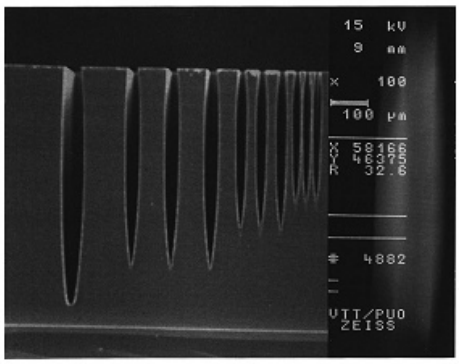


Figure 2.4 Changes in etched profile with different line width after one particular time [Kiihamaki 2000].

- Cathode electrode temperature. Etch rate in Bosch process is highly depending on the feature size [Walker 2001] and cathode temperature [Nagarajan 2006]. In particular, the passivation step depends on the temperature of the substrate. Higher temperature reduces the passivation rate, resulting in process at higher etch rate that leads to a decrease of selectivity of the masking material as well as in increase of side wall roughness and undercut [Tian 2008]. Etch rate of 10 micron/min was reported [Laermer 1999] in 1999 while in order to improve the profile quality by adjusting process parameters, etch rate was reduced to the 6 micron/min. This process was carried at room temperature in ICP-RIE. After one year, etch rate of silicon up to 7 micron/min using Bosch process by utilizing inductive coupled plasma (ICP) at room temperature [Kiihamaki 2000] was reported. With Bosch process, straight vertical profiles can be achieved with angle 90±2 by using photo resist or thermal oxide as a mask layer.

- ARDE and micro loading effects. Decrease in the etch rate with increasing etch-able area is called micro loading and it is an important source of depth non-uniformity. It is caused by the depletion of reactant species and can be reduced by decreasing the etch rate, increasing for example the supply of reactants. Decrease in etch rate for narrow trenches with increasing aspect ratio is called aspect ratio dependent etching (ADRE.) Here, the reduction of etch rate is due to decreased transport of reactive species in the narrow deeper features [Gottscho 1992]. The origin of these effects relates to the ion and neutral transport. The ARDE consists of RIE lag, ion-neutral shadowing, and charging effect whereas micro loading effects mainly concern to local loading like pattern density on the wafer.

- Step times. Step times are the individual etch and passivation times cycling during the Bosch process. They have a large impact on the profile and the etch rate. Generally the larger the step time for the etch step, the larger the scallops or increased roughness of the sidewall. Increasing the switching frequency of the plasma gases decreases the scallops size and reduce the roughness of sidewalls by decreasing the isotropic etch time at the bottom of the trench before the next passivation step protects the sidewall.

As a part of this thesis work, DRIE process is optimized to produce smooth sidewalls of etched cavity of T-cell across the complete thickness of silicon wafer (1.4 mm). If standard Bosch process is enable to produce high anisotropic etch with well controlled etching rate, this generates rough side walls with scalloping effect and grass formation visible at the bottom of the trenches. Scalloping occurs because the SF_6 etch is somewhat isotropic. The grassing is due to the insufficient etching radicals in the etch step or too much passivation step. Also micro masking, oxide or mask residues cause grassing. Such surface quality of the cavity of T-cell is not sufficient for atomic clock application. The excessive roughness of sidewalls will increase the collisions of Cs atoms with T-cell sidewalls, thus increasing Cs relaxation time and affecting the contrast of CPT signal. In addition, the contaminants deposited by passivation process of DRIE can also contaminants which may react with Cs. Moreover, it should be noted here that fluorocarbon passivation layers resulting from DRIE process may also affect the chemical stability of Cs vapor because the fluorocarbons are known to react with alkali metals to form alkali fluorides

The experiments aiming to optimize the quality of our DRIE process include the control of parameters like process temperature, uniformity and selectivity of masking materials (resist thickness, etching mask in thick resist and thermal oxide), ARDE, appropriate photo mask design and line width effect reducing side wall roughness and to improving the quality of surface are reported below.

Figure 2.5 shows the drawing of the layout used for optimization of DRIE process. Thus, we use a photo-mask presenting two cavities connected with thin channel. The etch mask will protect a 1.4 mm thick piece of silicon.

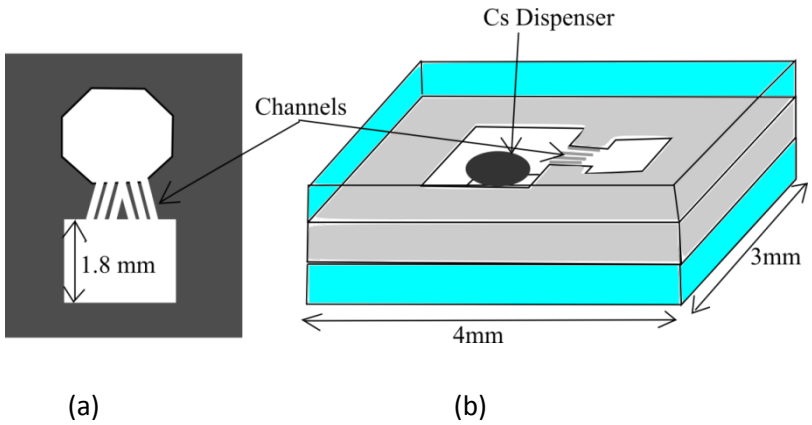


Figure 2.5 Mask layout: (a) cross section of T-cell, (b) 3D view of T-cell.

To produces an array of T-cells, 4-inch p-type and 1.4 mm thick silicon wafer and (100) oriented has been used. The photoresist AZ 9260 were coated and soft baked. Several variables were studied for the optimization of masking process: the impact of DRIE process temperature on the thickness of deposited photoresist with respect to grass deposition on the side wall after the through etch of cavities. Figure 2.6 shows the optical micrograph showing the zoom of etched cavities performed at different DRIE process temperatures and different thickness of resist.

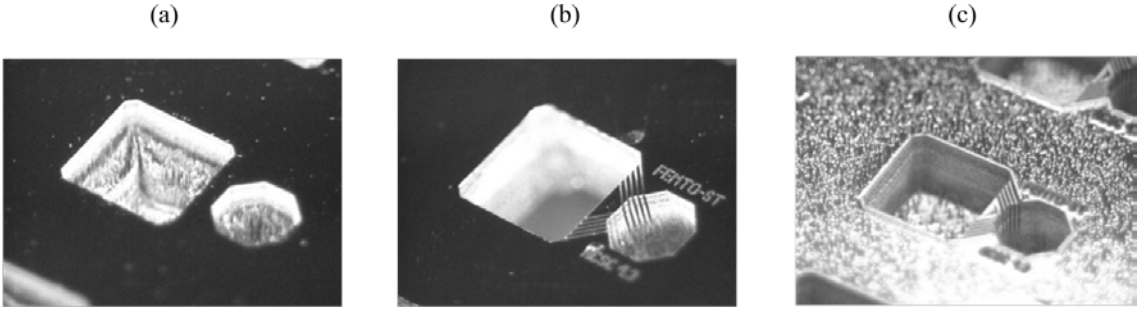


Figure 2.6 SEM photographs of silicon cavitires of T-cell made at different DRIE teperatures and for different thicknesses of mask resist: (a) temperature -5°C with resist thickness 10 µm. (b) temperature 10°C with resist thickness 30 µm; and (c) temperature 15°C with resist thickness 30 µm.

In this experiment the range of process temperature is from -5°C to +15°C with increment of 5°C and resist thinckness is either 10µm or 30µm. Figure 2.6 (a) shows T-cell cavity etched through 1;4 mm of silicon with 10µm thick resist mask, DRIE process operating at -5°C. Figure 2.6(b) demonstrated the similar T-cell cavity made with resist thickness of 30µm and processed at the temperature of 10°C. Finally, Figure 2.4(c) presents the T-cell cavity DRIE processed at the temperature of 15°C and 30µm

thick resist. We can see the grassing effect at the bottom of the cavity in case of -5°C process temperature whereas resist at top is burned at 15°C. In case of 10°C process temperature there is a less significant deposition of grass inside the cavity moreover resist at the top wafer also survived. From these rsults, process temperature of 10°C and resist thinkness of 30 µm has been chosen for DRIE experiment. Completed experiment data are summerized in the Table 2.1.

Table 2.1 DRIE process temperatures and resist thickness.

DRIE Process Temperature	**-5°C**	**0°C**	**5°C**	**10°C**	**15°C**
Grass	Red grass deposition	Red grass deposition	Red grass deposition	Grass deposition after 2h20 of DRIE	
Resist (AZ9260) 10µm	Survived	Survived	Survived	Removed after 3-4h of DRIE	
Resist (AZ9260) 30µm				Survived	Significantly damaged after 20min of DRIE

2.3.2 Polishing of T-cell cavity by KOH etch

An ideal smoothing process will combine the profile of the standard Bosch process with the excellent control of surface quality of the KOH etch. In addition to DRIE process, the surface quality of sidewalls of T-cell cavities is improved by performing KOH wet etching on the plasma etched surfaces. This chemical polishing of DRIE processed surfaces will reduce the sidewall roughness. Silicon DRIE etched T-cell cavity is immersed in KOH aqueous solution (41 wt. %, 55°C). T-cell cavity is treated in KOH solution with varied time of etches. Thus, we removed three different thicknesses of silicon performing 1-µm, 5 µm and 10 µm deep KOH etch. Figure 2.7 shows how this KOH polishing is improving the quality of DRIE etched surfaces. As is seen in these images, the surface defects were almost removed without any significant changes in the dimensions of cell-cavities. The magnified SEM images show very well that the scallop-shaped micro-defects on the surface were totally polished and the crystal plans of silicon start to appear on the surface in case of deeper KOH etch. From this result, we consider that the fluorocarbon layers which were on the surface of the etched sidewalls were also totally removed by the polishing procedure. In particular, it can easily be observed that up to 5 µm of KOH etch (Figure 2.7(c)) of DRIE etched surface there is a decrease of Surface RMS (root mean square). Further etching of such surface up to 10-µm deep etch reveals the crystallographic planes of silicon (Figure 2.7(d)). Consequently, up-to 5

µm deep KOH etching of DRIE etched surface is corresponding to the optimal improvement of surface quality.

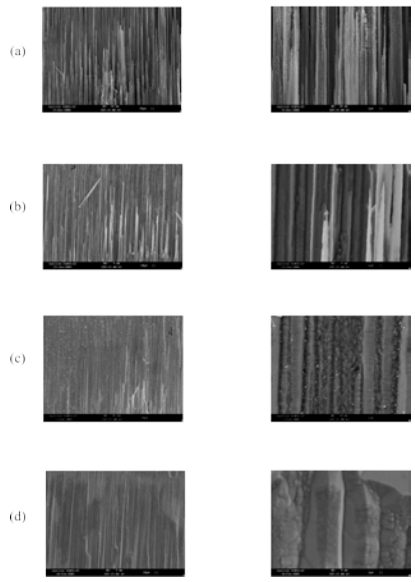


Figure 2.7 SEM images of side wall of DRIE etched T-cell cavities; (a) after DRIE process; (b) 1 µm KOH etch following DRIE; (c) 5 µm KOH etch following DRIE; and (d) 10 µm KOH etch following DRIE.

2.3.3 Improvement of DRIE process by use of thermal oxide etch mask

In some cases, the masking material is a photoresist which has been patterned using photolithography. Other situations DRIE require a more durable etch mask, such as silicon oxide or combination of both. We studied three different configurations shown in Figure 2.8: (i) photoresist and thermal oxide used as materials of the etch mask deposited on on the both side (top & bottom) of T-cell cavity; (ii) photoresist and thermal oxide etch mask only deposited on top side of T-cell cavity r and photoresist etch mask at bottom side; and (iii) only photoresist is used as a masking material on the both sides of T-cell cavity.

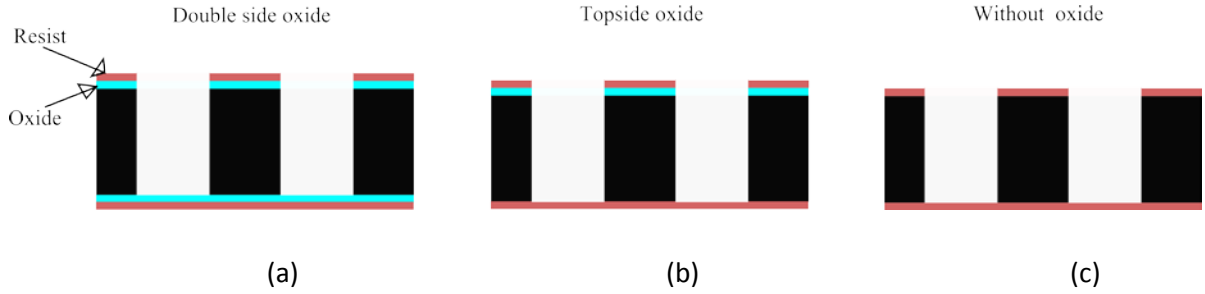


Figure 2.8 Configurations of etch mask (a) double side oxide; (b) oxide at the top side; and (c) only resist masks on both sides.

In order to see the effect of etching mask on the quality of DRIE etched side wall SEM analysis is performed. Figure 2.9 shows the SEM images of these three masking situations where it can be see the difference in the quality of T-cell sidewalls in term of grass deposition at the bottom and relative defects at the top. The increasing grassing effect is observable from Figure 2.9(a) to Figure 2.9(c). This degradation demonstrates clearly the interest to use silicon oxide as an etch stop layer.

(a) (b) (c)

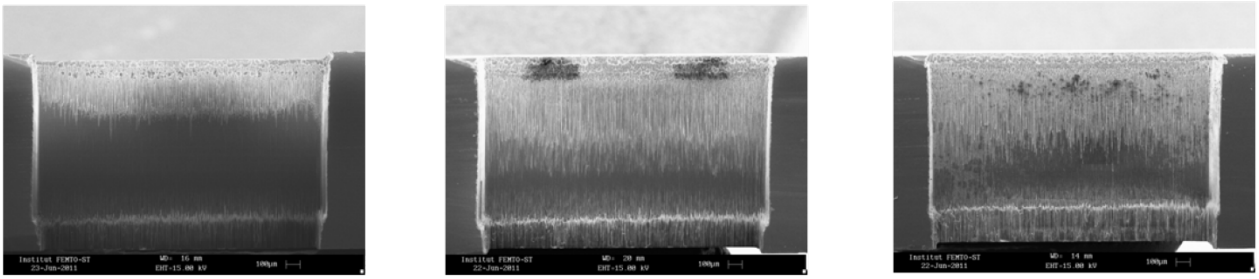


Figure 2.9 SEM images of DRIE etched surface utilizing different etching masks: (a) double side oxide, (b) top side oxide, (c) only photoresist.

2.3.4 Aspect ratio dependent DRIE

DRIE etch rate is dependent on the aspect ratio which is defined as the ratio = etch depth/width of feature of etched structure. Areas with more open silicon etch faster compared to areas with lower amounts of open areas, such as in trenches and small width features. The design of T-cell contains two large cavities connected by an array of thin trenches. This trench array introduce the path from the dispenser cavity to optical cavity for the Cs vapor playing also the role of filter preventing any contaminants from the dispenser cavity to the optical cavity. The channels need not to be deep enough equal to the cavities and for that we need to control the etching rate of trenches according to the etch rate of silicon cavity which should be less than etch rate of cavity. Such effect can be produce by adjusting the aspect ratio of trenches in comparison to that of cavities. To know the aspect ratio dependence of DRIE, a test DRIE process is performed using the photo-mask including several rectangular line with different line width varying from 5µm to 1mm in order to control the etch depth of trenches between the cavity until the big cavity etched through up to 1.4mm of silicon. Figure 2.10 shows the SEM image of DRIE etch demonstrating the variation of etching depth of trenches with different line width. We can see that with the reduction of aspect ratio the etching depth is increasing. These data are summarized in the Figure 2.11 showing the combined effects of etch depth and etch time for the various line with of etching mask.

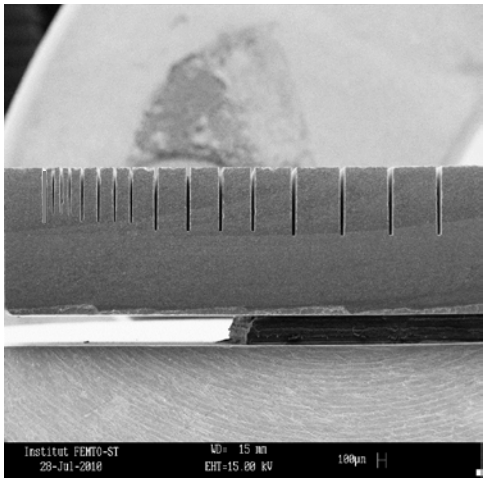


Figure 2.10 SEM image for aspect ratio dependent DRIE etching.

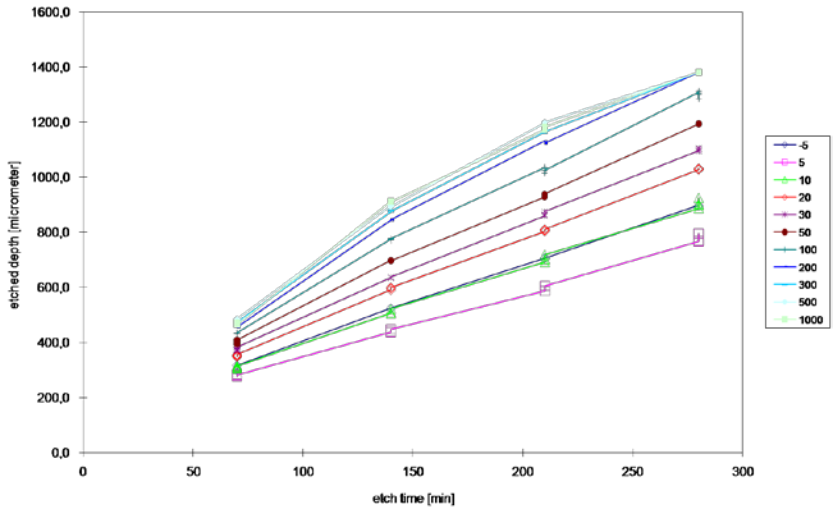


Figure 2.11 DRIE etching depths with respect to the etching time for the various line widths.

From these result we can define precisely the trench depth as required in comparison to that of etched big cavities.

2.3.5 From linewidth effect to DRIE etch mask with optimized photomask design

Following the above experiment, surface quality of DRIE sidewalls further observed is depending on the line-width of etching pattern. To check the effect of line-width on the quality of etched surface for 1.4mm deep etching, we consider different pattern with line-width varying from 100µm until 1mm. Here, the process is performed with the etch mask made of oxide and photo-resist as shown in Figure 2.12. DRIE is performed until the big cavities are etched through i.e. 1.4 mm of silicon. And experimental results compared, as shown in SEM images of Figure 2.13. We can see that the line-width of etched pattern is increasing; damages at the top of the surface are increasing too. However, this effect is accompanied by a

reduction in the bottom grass deposition. Such damages at the top surface are due to the intensification of plasma activity: larger will be the opening, larger surface will be exposed to the plasma. In conclusion, line-width between 200µm and 300 µm seems to produces a better quality of surface. Considering these result, different mask patterns are designed for fabrication of final T-cell cavities as reported in the next paragraph.

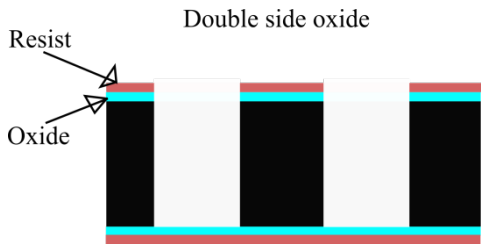


Figure 2.12 Bothside oxides along with photoresist as a DRIE etching mask.

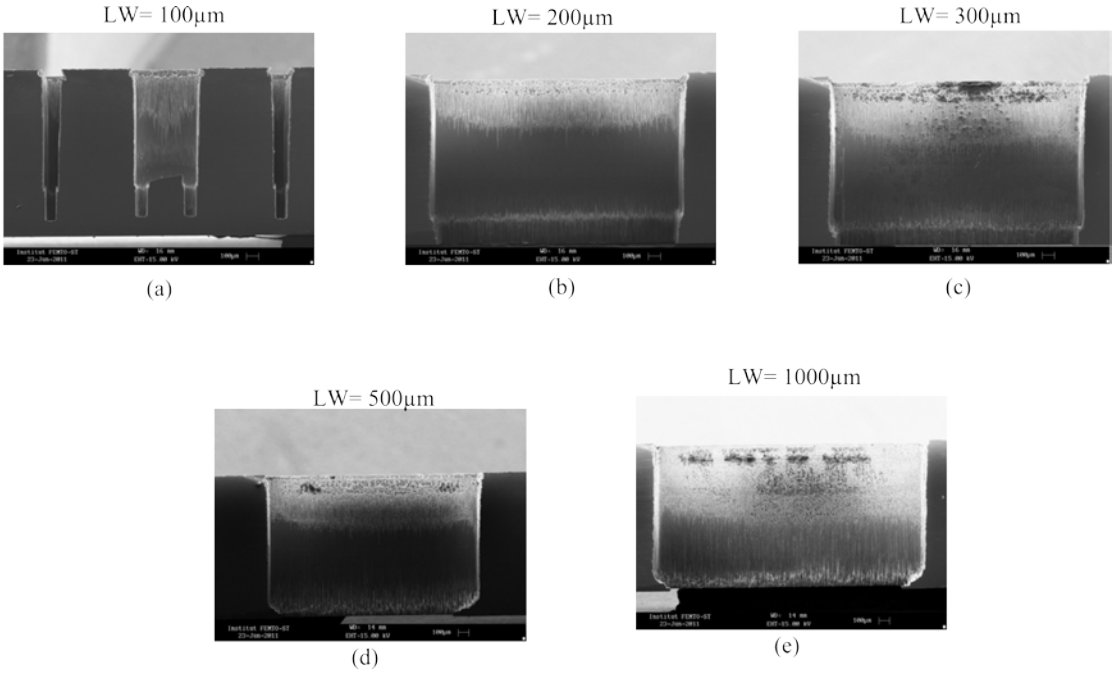


Figure 2.13 Line-width effect on the quality of DRIE etched surfaces.

Considering all the parameter of DRIE optimization reported previously, as a final step photo-mask is designed with different line-width opening know as a halo mask towards final optimization of parameter for DRIE process. Cell cavity dimensions are kept same as that of Figure 2.5 and the designs of photo-mask can be seen in the Figure 2.14 accompanied by their SEM images. We can see that etched cavity from mask with large opening has rough surfaces while the cavity etched with 300-µm mask has smoth surface with reduced grassing effect.

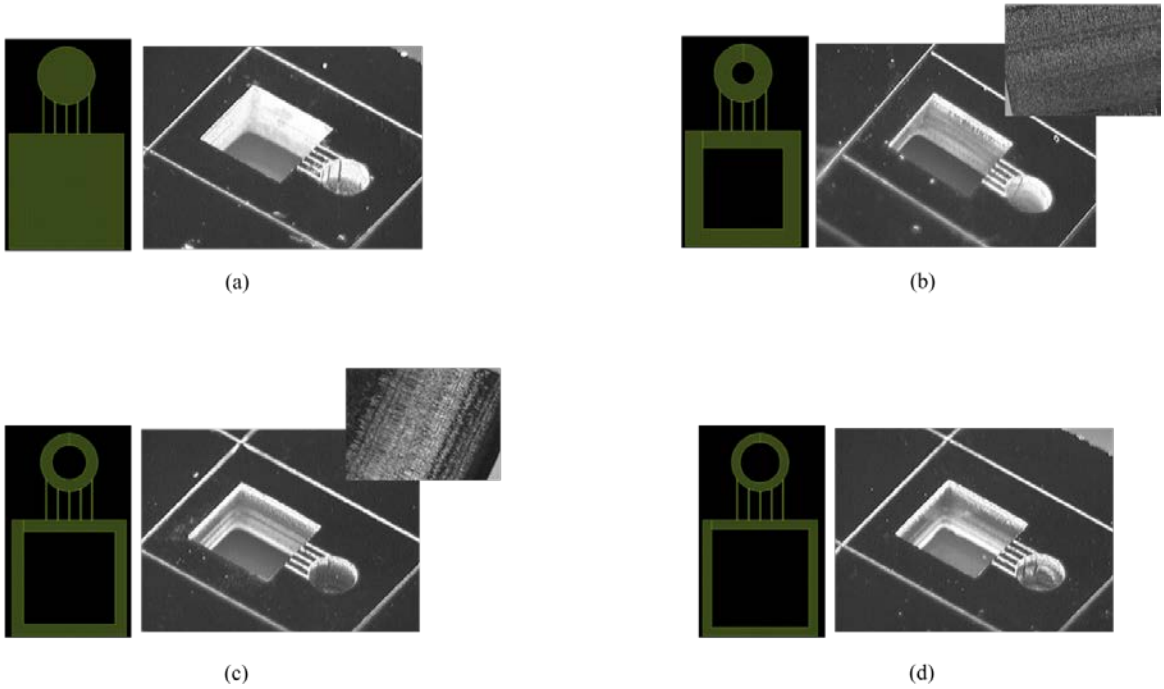


Figure 2.14 Images of DRIE etching of T-cell with different size mask opening: (a) mask opening equal to the cavity dimension; (b 300µm; (c 200µm; and (d) 150µm.

To improve further quality of DRIE etched surface, we perform two DRIE steps: front sides etch and back sides etch, as shown in Figure 2.15. The front side etch is formed down to several hundreds of micron. Then the back side etch is followed by DRIE deep etch completing the total depth of wafer. Upon completion of cell cavity etching, the standing bulk silicon is easily removed. Following such DRIE process, during the second step of DRIE, sample act as SOI wafer and gives the notching effect at the silicon/oxide interface, resulting from the lateral over-etching at Si/SiO_2 interface.

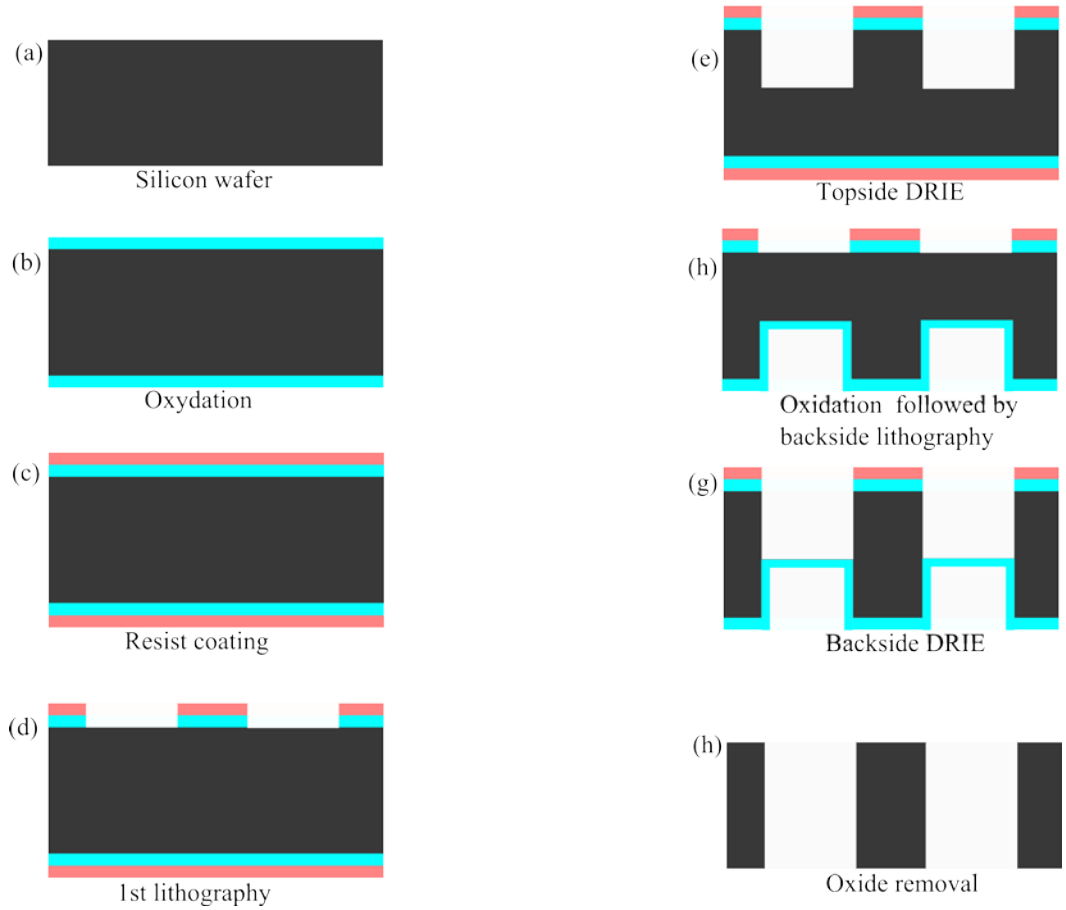


Figure 2.15 Process flow for the DRIE for T-cell cavities from both side of silicon cavity.

Figure 2.16 shows the SEM images of double-side etched trenches with different line-width (100µm, 200µm and, 300µm) with the same etch time. We obtain a significant improvement of surface quality of T-cell cavity with decreased damages and grassing effect during the second step of DRIE. However, notable footing effect appears in the center of cavity as results of over-etching of silicon at the Si/SiO_2 interface. The bowing effect is also present which is in agreement with previously reported work [Ishihara 1999, Zhang 2006]. This demonstrates from the Figure 2.16 that notching effect appears between the 200µm and 300µm. The footing effect can be avoided by appropriate control of etch time. Over a wide range of parameter space, there is demonstrated that increase of sidewall passivation can decrease the footing effect, but creates undesirable side effects. In particular, we found that it is difficult to control the footing effect in a narrow trench and also avoid the appearance of grass in a wide trench at the same time. The impact of footing effect for the quality of T-cell cavity in atomic clock application is negative because it will be the trapping Cs inside such trenches, affecting the CPT signal contrast. But still such results from the both side DRIE etching of silicon can be utilized for further improvement of quality of vapor cell side walls. In practice, the experimental results will demonstrate the insignificance of such over etching effect

on the performance of atomic clocks.

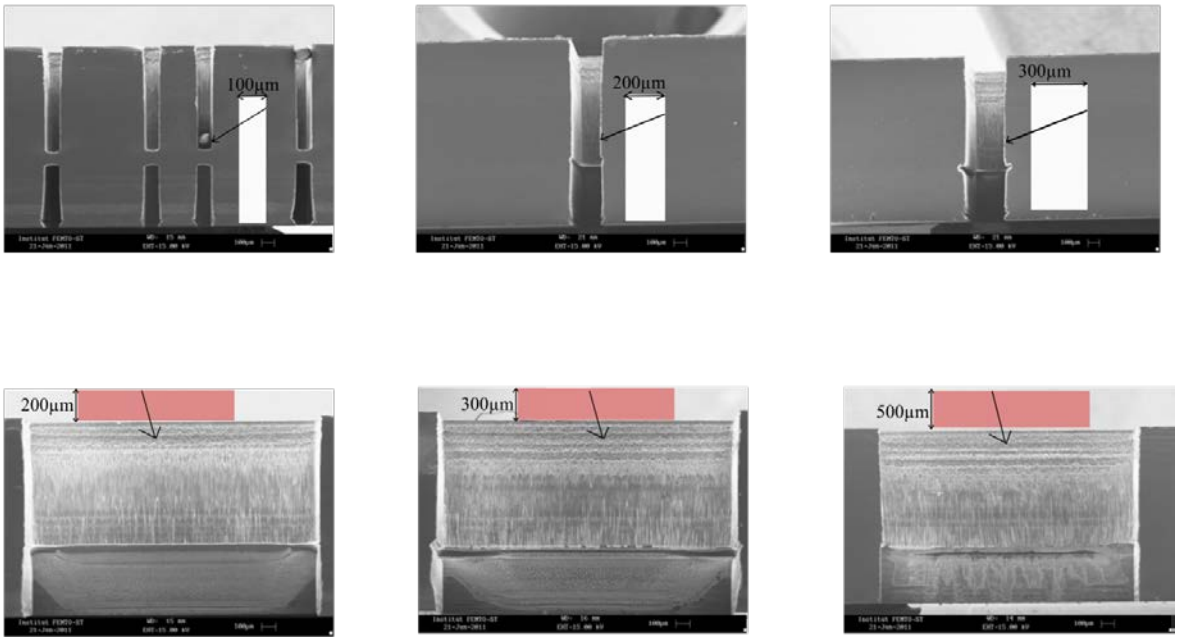


Figure 2.16 SEM images for the doubled side DRIE etching.

2.4 Anodic bonding of T-cells filled with pressure-controlled buffer gas

2.4.1 Introduction to bonding charges and currents

After DRIE etching of cell-cavities in a Si wafer, the wafer was anodically bonded to a glass wafer to produce silicon/glass structure, as shown in Figure 2.17(a). This anodic bonding is performed in the standard conditions, described in details in Appendix A.3. Subsequently, Cs dispensers are inserted in the dispenser cavities. Then, the T-cell is sealed by anodic bonding of the Si/glass structure and the second glass wafer placed in the chamber filled with the buffer gas at a required pressure (Figure 2.17(b)). Anodic bonding is the key technology of Cs vapor MEMS cells. The Chapter 3 challenge is to solve the problem of the electrical breakdown in the gas atmosphere and to demonstrate the reliable procedure of anodic bonding well operating in presence of buffer gas atmosphere.

It is known that, when performed in the gas atmosphere, the anodic bonding is often disturbed by the electrical breakdown cased by the ionized gas. Therefore, in order to optimize the conditions to perform the anodic bonding, the electrical breakdown voltage was examined in the buffer gas atmosphere at the pressures usually required for the Cs-vapor cells for atomic clocks (up to 20 kPa). To avoid the electrical breakdown while obtaining the sufficient bonding strength, the bonding process was carried out in two steps: the pre-sealing step in the gas atmosphere and then the supplemental sealing step to improve the

bonding strength. Electrical breakdown voltage is following the Paschen's curve where breakdown voltage is determined by gas pressure and electrode separation [Boyle 1955]. This phenomenon also depends on many other parameters like gas species content and electrode material [Boyle 1955, Braithwaite 2000, Carazzetti 2008].

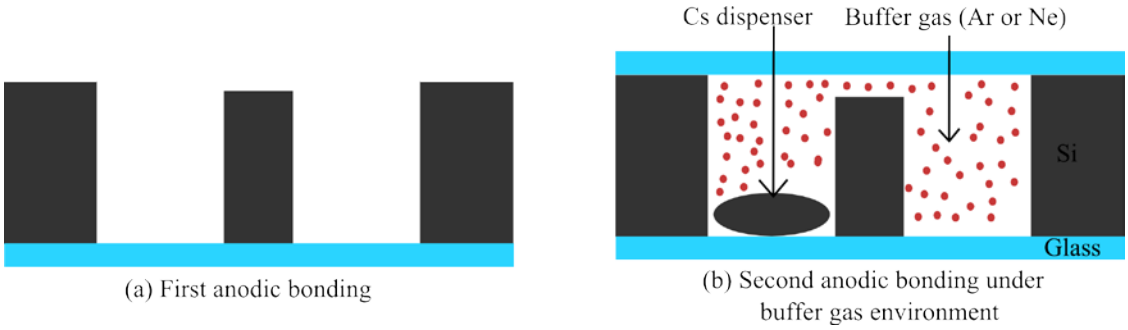


Figure 2.17 Sealing procedure of Cs T-cell: (a) silicon/glass stack after the first anodic bonding; and (b) glass/silicon/glass sandwiched structure including Cs vapor and buffer gas.

Therefore, in order to optimize the conditions to perform the anodic bonding, the electrical breakdown voltage was examined in the buffer gas atmosphere (Ar or Ne) at the pressures usually required for the Cs-vapor cells for atomic clocks (up to 20 kPa). In addition to this problem of voltage breakdown which is specific in case of fabrication process for Cs vapor cells filled by a noble buffer gas, there are few other parameters of bonding that need to be investigated to guarantee a strong bonding. Some of them are described in appendix A.3. The influencing parameters on the bonding quality include the bonding temperature, the applied voltage, the pressure, the bonding time and vacuum level. However, the temperature and the voltage play the most important role in anodic bonding process. In particular, it has been demonstrated that good bond quality can be achieved at voltage corresponding to the higher current peak which is possible to perform at high voltage or high temperature that further permits to reduce the bonding time. Controversially, bonding time increases at low operating temperature, low voltage and n-type silicon. In practice, anodic bonding takes place immediately on the application of temperature (which cause high current) [Cozma 1995] and the external voltage. At the start of the bonding process, the value of the current is high but falls rapidly, especially for high bonding temperatures. High temperatures generate high ion mobility in the glass substrate. As the temperature is raised, the conductivity of glass increases exponentially. A rapid build up of the space charge occurs at the interface, giving rise to electrostatic forces, which brings the two wafers into intimate contact. Therefore, high temperatures cause high current and result in good bond quality because of larger electrostatic force improving the bond quality [Esashi 1990, Kanda 1990]. Bonding strength also supposed to be increased with the increase of temperature [Dziuban 2006] for example in order to have strong enough anodic bonding with strength up-to 30 MPa, process temperature should be 350°C or more. Moreover low temperature results in the less

conductivity within the glass in turn space charge at interface reduces exponentially and low voltage gives the lower electric field at the interface which reduces the drift velocity of oxygen anions to maintain the oxidation rate at bond site [Cozma 1995]. It has been shown [Lee 2000] that bonding takes longer time (38 minutes) for n-type silicon in comparison to 4 minutes for p-type as p-type silicon has extra holes so these can migrate toward the interface under strong electric field. Another parameter having a strong impact on current peak and consequently on bonding quality concerns the type of working atmosphere: bonding performed in air, vacuum or presence of any residual gases like Argon. In particular, it has been demonstrated that current peak is larger in air than that obtained in vacuum or Argon atmosphere [Cozma 1995]. The charge transport during anodic bonding is formed by the drift of sodium ions, playing an important role in creating depletion layer at the interface as well as is useful to determine the rate processes which occur during anodic bonding [Albaugh 1991]. The activation energy of such charge flow in glass has been investigated [Schmidt 1998] using elastic recoil detection analysis (ERDA), Finally, bonding current will depend on temperature and polarization voltage, on type and thickness of glass, and on type of working atmosphere. The shape and type of cathode electrode and its force exerted on bonded surface have a strong impact on the value of bonding current as well as on current fluctuations as a function of time.

2.4.2 Description of EVG anodic bonder

Now, the process of anodic bonding will be studied in the situation where T-cell is filled with the buffer gas at an appropriately controlled pressure and with the sufficient sealing quality. As the standard procedure of bonding is disturbed by the electrical breakdown caused by the ionized gas so in order to avoid the electrical breakdown while obtaining the sufficient bonding strength, the bonding process was carried out in two steps: the pre-sealing step in the gas atmosphere and then the additional sealing step to improve the bonding strength. To perform the complete sealing of DRIE etched T-cell cavity a p-type (100) Czochralski silicon wafer and two Borofloat glass wafers from Schott are used. Anodic bonding experiments are carried out in computer assisted EVG501 Wafer Bonding System from EV Group. Figure 2.18 shows schematic of anodic bonder chamber.

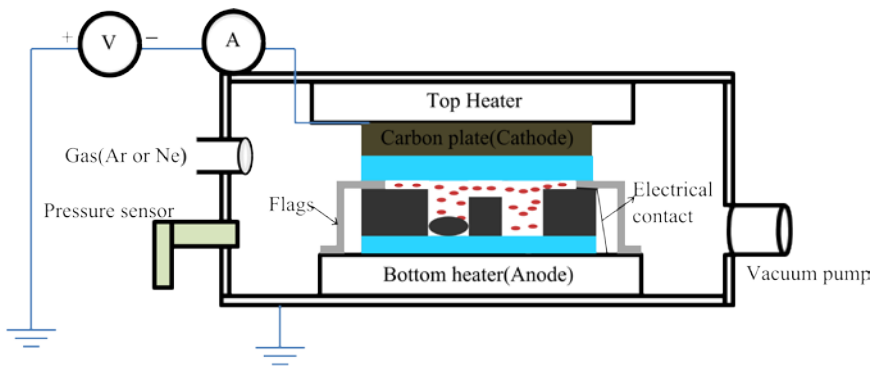


Figure 2.18 Schematic of anodic bonding chamber.

In the situation of standard bonding, two wafers (silicon and glass) are places in the chamber of wafer bonder, separated by three "flags" and clamped by two clamps on a bonder chuck. The bonder chuck is then loaded into the EVG501 chamber which is pumped down to approximately 10^{-4} mbar. The bonder chuck is heated to a given temperature while the flags keep the wafers physically separated. The bonding is started by pressing in the center of the top wafer to create an initial point of contact, while the wafer flags are removed. Upon removal of the flags, a uniform bonding down pressure is applied over the wafer pair. The wafer pair is then further heated to complete the bonding. Finally, the wafers are slowly cooled and unloaded. The maximum processing temperature for EVG501 is 400°C.

2.4.3 Procedure of anodic bonding for sealing T-cells

The fabrication of T-cells contains two operations of anodic bonding. The first anodic bonding is performed at vacuum with standard conditions of bonding, forming a silicon/glass structure, as shown in Figure 2.17(a). Prior to the bonding process both silicon and glass wafer were cleaned with piranha solution (H_2SO_4: H_2O_2, mixing ratio 3:1) and rinsed in deionized water. The wafers were then dried with N_2, and finally baked on the hot plate at 150°C to remove the residual water. The anodic bonding of the Si and glass wafers is performed in the vacuum chamber ($1x10^{-3}$ Pa) at 350°C. The bonding voltage was increased in multiple steps from 300 V up to 900 V. Total bonding time was 20 min. After the successful bonding, a silicon/glass stack is produced (Figure 2.17(a)).

Subsequently, Cs dispenser is placed inside the dispensing cavity of T-cell. Then the cell is prepared for the second anodic bonding, sealing the silicon/glass structure by a cover glass wafer, forming the sandwiched structure shown in Figure 2.17(b). This anodic bonding is made in buffer gas atmosphere. Buffer gas plays an important role because at a sufficient buffer gas pressure, the motion of Cs atoms becomes the diffusion process, leading to an increase in the interval of time between wall-collisions, which in turn limit the resonance broadening. However, it must be noted that the slight interactions between Cs atoms and the buffer gas atoms or molecules bring about a frequency shift of the clock

transition. Moreover, this phenomenon depends on the pressure of the gas as well as the nature of the gas and operating temperature. In consequence, the nature of buffer gas pressure should be carefully optimized and controlled to obtain the better performance of the clock. We perform the second operation of anodic bonding in presence of buffer gas by two-step procedure, improving the quality of sealing and considering the effects of breakdown voltage in buffer atmosphere. This is the key step of fabrication process of T-cells, guarantying their long-term reliability.

The first step of anodic bonding in buffer gas atmosphere is carried out with noble gases (Ar or/and Ne), This bond, performed at room temperature in the chamber filled with a controlled amount of the buffer gas and requesting the application of bonding voltage lower than the breakdown voltage of the buffer atmosphere, permits the pre-sealing of T-cells. Here, the bonding voltage is varies from 200 to 350 volt. This voltage is not enough for a strong bonding. For this reason we perform an additional step of bonding in which bonding is performed in air by applying consequently high voltage up 900 V. This second step of bonding is carried out in air at a high voltage to get the definitive strong sealing of T-cell cavity. This improvement in bonding process was required to get rid of gas discharge inside the bonding chamber at the voltage higher than breakdown voltage. Several experiments were preformed to evaluate the breakdown voltage at specific pressure of gas inside the chamber. Various process steps for this two-step procedure of bonding are summarized in Table 2.2.

Table 2.2 Process for filling of Ar and Ne in T-cell and procedure of two-step anodic bonding in buffer atmosphere.

Process steps
1. Cleaning both surface to be bonded with piranha solution
2. Load both wafer inside anodic bonding chamber separated by flags
3. Close the chamber and start pumping to get vacuum close to 10^{-4}mbar
4. Heating upto 350°C both bottom and top plates
5. Cooling to room temperature
6. Introduction of gas(Ar or Ne)
7. Flags out
8. Piston down to apply contact force on the wafers up to 500 N
9. Heating (350°C)
10. Pre-sealing, first step of bonding in Ar or Ne (bonding voltage<breakdown voltage).
11. Introduction of air inside the chamber
12. Second step of bonding at high voltage to get sufficiently strong bonding by applying voltage 600V (10min) and 900V (20min).

Before the bonding procedure we measured the breakdown voltage for specific buffer atmospheres [Hasegawa 2011].

To carry out this experiment, the Si/glass stack was placed on the bottom heater (anode) of bonder chamber with the silicon side up. A metal wire was added to provide the electrical contact between the anode plate and the silicon surface of the silicon/glass structure, as shown in Figure 2.18. Wafers were annealed at 350°C in vacuum (pressure: $1x10^{-3}$ Pa). A glass wafer was placed above the Si/glass structure. The glass wafer was attached to the carbon plate (cathode), which was connected to the power supply. The Si and glass wafers were separated by three movable flags (200 µm thick) inserted between them. During the annealing step, temperature of the top and bottom heaters was regulated at 350°C. It must be noted that temperature is controlled only at the portion of the heaters and thus temperature across the chamber is not uniform during the annealing step. This non-uniformity in temperature will affect the accuracy of the pressure of gas (Ar or Ne) when the gas is introduced in the chamber. Therefore, after the annealing step, the whole chamber was cooled down to room temperature to eliminate the temperature

gradient across the chamber. After establishing the temperature equilibrium in the chamber, Ar or Ne gas was introduced until a desired pressure (0.1 to 20 kPa at 25°C). Then, the substrates were contacted by removing the separation flags. Subsequently, the portion of the top heater moved downwards to provide the contact force of 500 N on the wafers in order to trap the gas in the cavities. After that, temperature was increased again to 350°C to start the measurements. The applied voltage was increased in multiple steps until the breakdown occurred. The maximum bonding voltage applicable for each gas pressure was determined according to these breakdown voltage measurements. The breakdown voltages examined as the function of the pressure of Ar and Ne are plotted in Figure 2.19. The results follow the well-known characteristic of the Paschen curve, where the breakdown voltage reaches the minimum at a partial vacuum pressure. Generally, the mechanism of the electrical breakdown behavior is explained by ionization of gas atoms by inelastic collisions of electrons accelerated by the electric field. The breakdown voltage increases with an increase in pressure because the large drift energy of electrons is required to ionize many gas atoms (high-pressure insulation) However, as the pressure is reduced to a critical value, the breakdown voltage reaches the minimum. At further reduced pressures, the breakdown voltage increases steeply because the number of gas atoms is not sufficient to start a spark in these conditions (vacuum insulation).

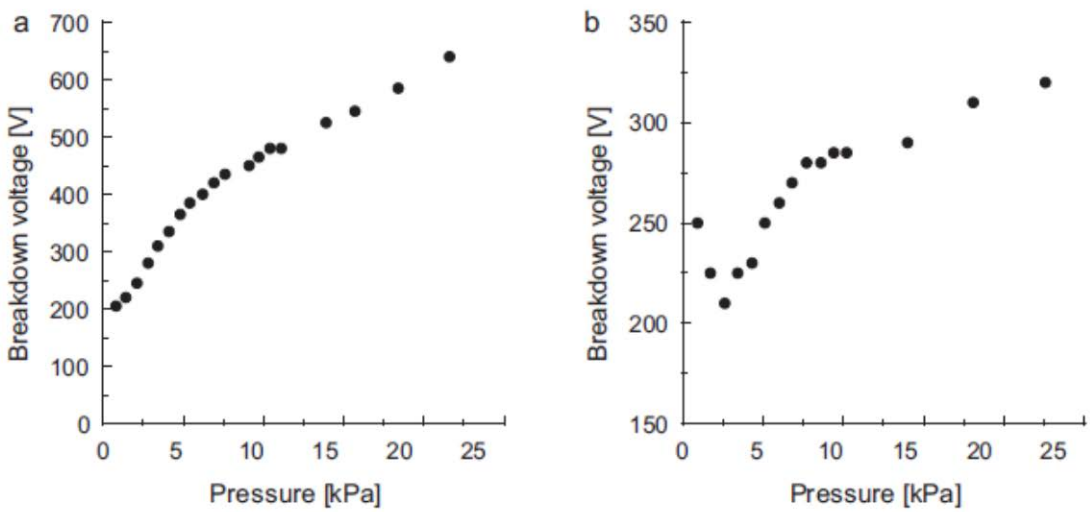


Figure 2.19 Electrical breakdown voltages in the wafer bonder in (a) Ar and in (b) Ne at various pressures.

From this measurement of breakdown voltage at various gas pressures, we can determine the maximum applicable voltage for specific pressures for two buffer gas atmosphere. Thus, at the pressure of 10 kPa the breakdown voltage is 450 V for Ar while the breakdown of 300V is obtained for Ne. In both cases these voltage values are useful to fix the value of bond voltage required for the pres-sealing and for strong bond of silicon and glass wafers. It is clear that the application of bond voltage close to the value of the breakdown values is not sufficient to guaranty acceptable bond strength. The proposed two-step bonding procedure for bonding in buffer atmosphere is made in conditions where the bonding voltage of pre-sealing is always less than breakdown voltage and voltage of strong sealing is bigger than breakdown voltage. A similar two-step bonding has also been previously [Blasquez 2002], where the process of anodic bonding in nitrogen has been investigated. In this case, the second step of bonding was also carried out in nitrogen environment. However, we could not apply this process for Ne because the breakdown voltage in Ne was lower than 600 V even at atmospheric pressure. Whereas it is not possible in our case as for neon gas (particularly), breakdown voltage is less than 600 V even at atmospheric pressure.

Following the procedure detailed in Table 2.2, our two-step bonding procedure require the bonding process to be performed in Ne (10 kPa) atmosphere. For this pressure of Ne, the pre-sealing step was performed at 250V (0-530 s). The voltage was applied until the bonding current was sufficiently low (0.01 mA/cm^2). The time of this step was usually 5 to 10 min. Subsequently air was introduced in the chamber, and then the second step of bonding (the supplemental bonding) was performed (from 535 s) at 600 and then at 900 V. As shown in Figure 2.20, a sharp current peak is observed when the first bonding voltage (250 V) was applied (0 s). This bonding current is attributed to the drift of alkali ions, mainly sodium ions, in glass toward the cathode, which results in the formation of the depletion layer beneath the surface of

glass to be bonded. Because the formation of the depletion layer is the rate-determining step for the bonding reaction, the current characteristic is very important information to discuss the bonding reaction. It is empirically known that a high and sharp initial current peak indicates that the depletion layer is successfully started [Albaugh 1991, Cozma 1995]. The other important parameter in the current characteristics may be the charge transfer during the process. The relationship between the charge transfer and the bonding strength was investigated by [Albough 1991], who examined the bonding strength of the samples by the fracture tests. They found that charge transfer, required to complete the bonding of more than 80% of the surface area was 4mC/cm^2 regardless of the bonding temperature and voltage. For our process shown in Figure 2.20, the charge transfer during the first 60 sec of the bonding step in Ne (250 V) was 4.3mC/cm^2. The result indicates that the bonding was almost complete during the bonding step in Ne, in particular for the first 60 sec, and thus that subsequent introduction of air did not significantly affect the atmosphere of the pre-sealed cells. The current peaks were clearly observed in the beginning of the voltage steps (600 and 900 V) of the supplemental bonding in air (535 and 843 s). These peaks are attributed to the further formation of the depletion layer, which contributes to the enhancement of the density of the bonding sites. From these results, it was considered that both the pre-sealing step in the buffer gas and the supplemental bonding step in air were performed successfully.

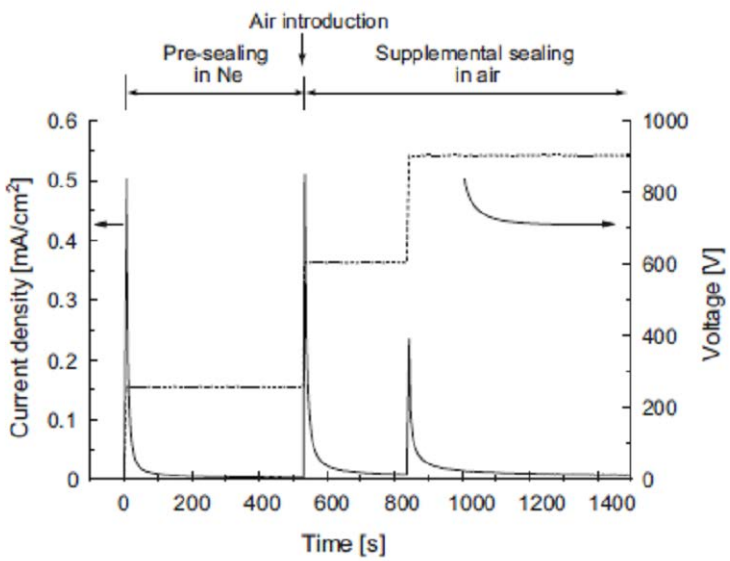


Figure 2.20 Current response and voltage during the anodic bonding. The result was obtained in Ne (10 kPa at 65ºC).

After the second anodic bonding, an array of microcells is diced into the single cell of external dimension 4mm x 6mm x 2.4mm shown in Figure 2.21. Now the cells are ready for activation of Cs dispenser to release the Cs inside the sealed cavity by means laser and activation process explained in the following section.

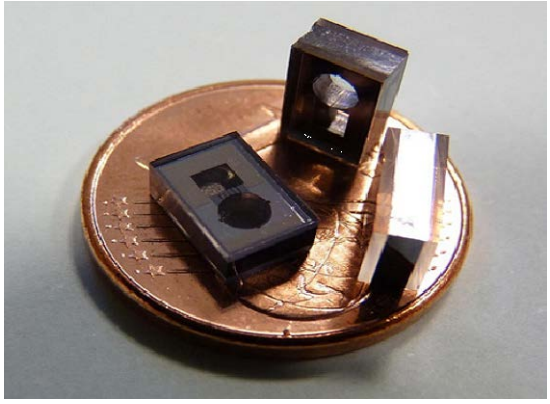


Figure 2.21 Microfabricated Cs vapor cell.

2.5 Activation of Cs vapor

Cs vapors are activated by using a laser source, to locally heat the Cs mini-pill dispenser inside the sealed micro-cells. The mini-pill is a compressed powder mixture, consisting of Cs salt and reducing agent. It has a cylindrical shape; the diameter is about 1 mm, while the height is about 0.5 ± 0.1 mm, as shown in Figure 2.22. The technology of mini-pill was developed by SAES Getters SA in the frame of MAC-TFC project. To ensure repeatability of the activation process, a semi–automatic activation bench has been designed and constructed at FEMTO-ST [Dziuban 2011], as shown in Figure 2.23. The system contains 808-nm, pigtailed, 5W laser diode. Due to high power losses, the laser diode is mounted on 80 W Peltier modules and a heatsink. The laser beam is focused onto the Cs dispenser using three lens systems, with possibility to change the focal distance. To give possibility to precisely focus the laser beam onto the dispenser, an x-y stepper motor stage was implemented into the bench. The stage can move in both directions within 150-mm with single step 10 µm and high repeatability. Whole targeting and the activation procedure can be viewed in real time using B/W imaging system. Thus, the dispenser is heated to the temperature of about 700° while the rest of micro-cell remaining below 100°C. Operating typically at the power of 1.25 W, the laser is collimated onto the dispenser. Dispenser is exposed by such laser light from 1 to 2 minutes in order to release Cs from the dispenser. As a consequence of activation procedure, liquid Cs fulfills the cell and forms a metal thin-film layer on the inner glass window.

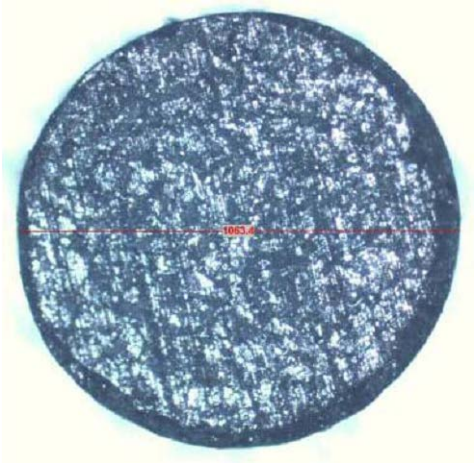


Figure 2.22 View of a Cs mini pill dispenser.

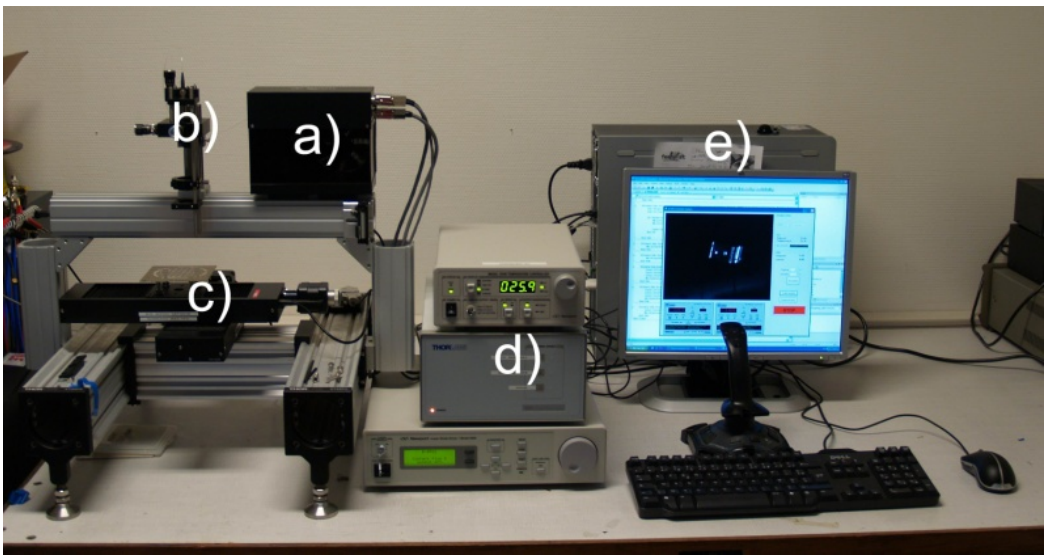


Figure 2.23 Computer controlled activation system for Cs dispensers: a) pigtailed laser diode; b) collimating, focusing and imaging system; c) xy stage; d) laser current control, laser temperature control, xy stage controller; and e) control computer.

2.6 Characterisation of T-cell performances

2.6.1 Linear Absorption spectroscopy

Long-term linear optical absorption measurements were performed to confirm the presence of Cs in the cells made using our filling method. The schematic for optical linear absorption is shown in Figure 2.24. The laser source was a DBR laser diode operating at 852 nm scanned over the Cs D2 transition by modulating the current with a triangular waveform. The first part laser beam passed through the measuring windows of micro-cells heated to a temperature between 75°C and 95°C. The second part was sent through a reference cm-scale cell with pure Cs Figure 2.25(a) shows the absorption spectra Cs vapor

microcells filled with Ar (expected pressure of 6.7 kPa) at 70, 80, 90, 95°C and for Cs reference cell at ambient temperature. For the pure Cs reference cell, the two peaks are separated by Cs frequency of 9.192631770 GHz and broadened by Doppler effect. On the other hand for, in tested microcells, the presence of buffer gas is proved by the optical frequency shift and homogeneous broadening of absorption peaks. Pressure of Ar inside the microcell is estimated by fitting absorption curves using a Voigt profile [Beverini 1981] utilizing red shift coefficients reported in [Bernabeu 1980]. This coefficient is given to be -7.40MHz/kPa for Ar at 21°C. Consequently, we estimate that the pressure in our microcells is 6.1±0.2kPa which is in close agreement with the expected pressure. In this measurement method, the uncertainty in the pressure estimation is due to the lack of frequency resolution estimated to be about ±3MHz in this measurement method. Moreover it is noted that the amplitude of absorption peaks increases with the increase in the temperature as expected due to increase in Cs vapor density.

Same kind of linear absorption spectroscopy method was used for Ne-filled (expected pressure 10kPa) Cs microcells whose absorption spectra are shown in Figure 2.25(b). Measurements for Ne cells are carried out at 80, 90, and 100^0C. The red shift coefficient is given to be -4.25MHz/kPa at 21^0C [Bernabeu 1980] for Ne. In our case, pressure of Ne is estimated around 9.8±0.09kPa, which is also in close agreement with required pressure.

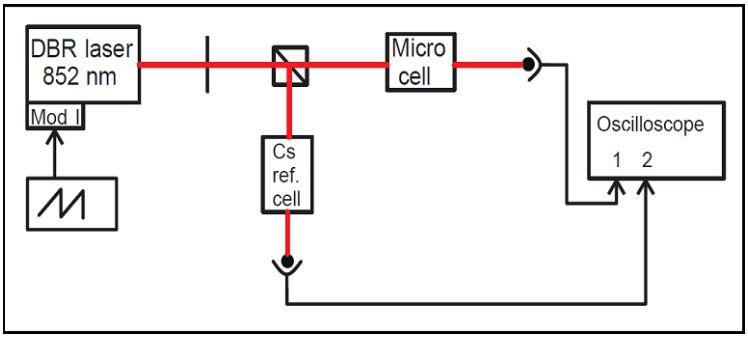


Figure 2.24 Schematic of metrology bench to measure the optical linear absorption in Cs-buffer gas vapor microcells.

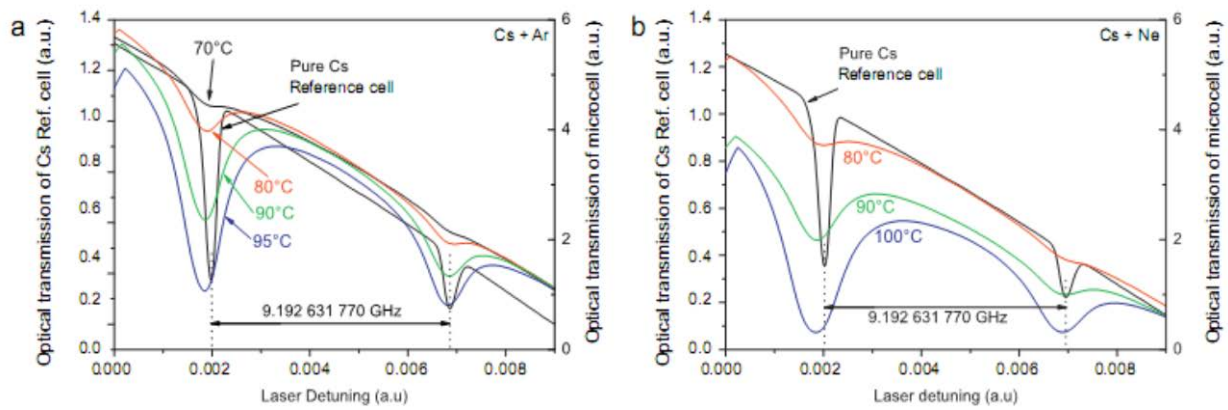


Figure 2.25 Optical linear absorption (a) for Ar filled Cs microcell (b) for Ne filled Cs microcell.

2.6.2 CPT Spectroscopy

2.6.2.1 First experiment

For further investigation, the buffer gas pressure in Cs vapor microcells has been estimated by detecting the CPT resonance signal. The presence of buffer gas causes a slight frequency shift of the clock transition because of collisions between Cs atoms and buffer gas. This frequency shift depends on the buffer gas nature and on the cell temperature. Buffer gas collisional frequency shift coefficients are reported in [Beverini 1981, Kozlova 2010]. Our buffer gas pressure estimation is then based on a measurement of the clock transition. Measurements were done in different cells coming from the same wafer to estimate uniformity of buffer gas in cells coming from the same wafer. For these measurements, a DFB laser resonant on the Cs D1 line at 894 nm is frequency stabilized on the on Cs 4-4' transition using saturated absorption spectroscopy in a pure Cs reference cell. A pigtailed electro-optical phase modulator driven at 9.192 GHz by a low noise frequency synthesizer is used to create the optical sidebands required for CPT detection. The CPT resonance is detected by scanning slowly the LO frequency with a typical deviation of 100kHz. The cell temperature was kept at 60°C at the m°C level during such measurements.

Figure 2.26 reports an example of a CPT resonance detected in a Cs-Ne microcell. The resonance linewidth is measured to 2.52 kHz while it is expected to be about 250-300 kHz in a pure Cs cell with same dimensions and same experimental parameters. Such line width measurement for Ne filled Cs microcell is in good agreement with previously reported results for Ne-Cs cells [Knappe 2004b] and agrees with theoretical calculations [Vanier 1989]. Moreover, we note that the CPT resonance contrast, defined as the ratio between the peak height and the DC background (S/B ratio on Figure 2.26) is measured to be 0.91%.

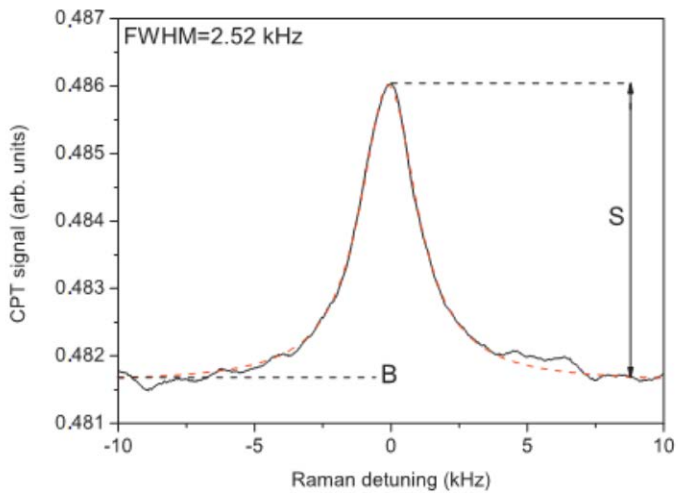


Figure 2.26 CPT resonance signal obtained in Ne-Cs microcell.

Table 2.3 shows the results of buffer gas pressure measurements inside two different batches of wafer producing several cells. Batch 1(wafer 1) has 12 cells with measured pressure of 9.2±0.2 kPa and in the batch 2(wafer 2), 8 cells with pressure 10.6±0.2kPa expect one cell (53.02kPa) in which pressure was measured bit higher (11.24kPa). However this measured pressure is lower than the expected pressure (13.3kPa) but a nice reproducibility or uniformity of buffer gas pressure is found in the different samples or cells coming from a same wafer (Table 2.3).

Table 2.3 Measured pressure values of two different batches of cell fabrication.

Batch 1	**Pressure (kPa)**	**Batch 2**	**Pressure (kPa)**
5201	9.079	5301	10.425
5202	9.052	5302	11.239
5203	9.092	5303	10.439
5204	9.065	5304	10.479
5205	9.105	5305	10.572
5206	9.180	5306	10.545
5208	9.410	5307	10.825
5209	9.079	5309	10.519
5210	9.105		
5212	9.005		
5213	9.025		

2.6.2.2 Characterization of CPT resonances in Cs-Ne microcells

For proving further the potential of our Cs cell technology, we decided to implement some of them in a VCSEL-based Cs CPT Clock prototype and characterize in depth the impact of some experimental parameters on the CPT resonance shape and frequency. Figure 2.27 shows the schematic of this set-up.

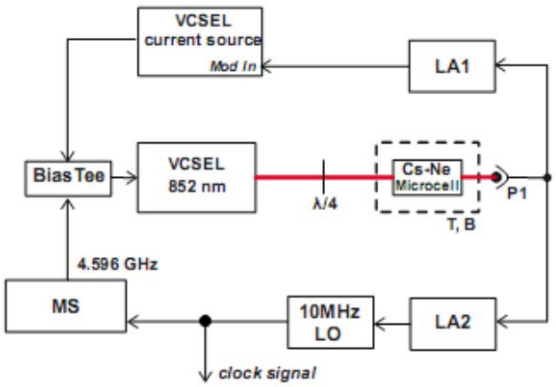


Figure 2.27 Schematic for experimental setup for CPT measurements of microcells.

A VCSEL source resonant at 852 nm is used. The VCSEL injection current is modulated at 4.596 GHz (half of the Cs frequency) to produce two-phase coherent side bands separated by frequency 9.192GHz A quarter-wave plate is placed at the output of the VCSEL to produce circular polarization. The optical power transmitted through the cell is detected by a low noise photodiode. The cell is temperature stabilized and surrounded by a solenoid applying a static magnetic field to raise the Zeeman degeneracy. The cell resonator ensemble is inserted into a cylindrical mu-metal magnetic shield to avoid external perturbations. The resulting voltage signal at the output of the photodiode is used both for laser frequency stabilization and CPT resonance detection. The laser frequency is locked near the centre of the Doppler broadened absorption line by modulating the laser DC current at 60 kHz and demodulating the photodiode signal with a lock in amplifier (LA1). The dark line resonance is detected by scanning the frequency of the microwave synthesizer (MS) and measuring the transmitted power through the cell. To increase the signal-to-noise ratio, the synthesizer frequency is modulated at 1-3 kHz Hz and the photodiode signal is demodulated with a second lock-in amplifier (LA2). The locking amplifier LA2 then produces an error signal allowing to lock the local oscillator frequency onto the Cs clock frequency.

Main results of these experiments are reported in [Boudot 2011] and some of them are shown below. These tests were done with Cs-Ne microcells with different buffer gas pressure.

Figure 2.28 reports the linewidth of the CPT resonance versus the laser intensity for two cells with different buffer gas pressure. It is clearly seen that the CPT linewidth increases linearly with laser

intensity. The zero-intensity linewidth and curve slope is found to be smaller for cells with higher buffer gas pressure as expected.

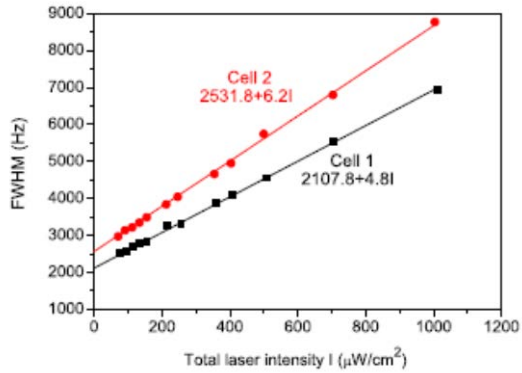


Figure 2.28 CPT resonance linewidth versus the laser intensity in Cs-Ne microcells (Cell 1: 8.1 kPa, Cell 2: 6.6 kPa).

Figure 2.29 reports the Cs clock frequency versus the cell temperature. It is clearly seen that the temperature dependence of the clock frequency can be cancelled around a so-called inversion temperature of about 80°C. This inversion temperature is found not to be dependent on the cell buffer gas pressure. This very important result allowed us to propose the development of chip-scale atomic clocks with microcells containing a single Ne buffer gas instead of usual buffer gas mixtures in vapor cell frequency standards [Vanier 1982].

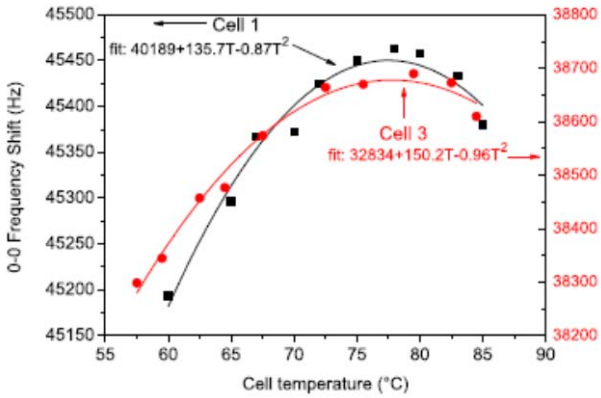


Figure 2.29 CPT resonance frequency shifts (from the unperturbed Cs atom frequency) versus the cell temperature in Cs-Ne microcells (Cell 1: 8.1 kPa, Cell 3: 6.7 kPa).

Following these tests, we demonstrated a clock frequency stability measurement shown in Figure 2.30. It is measured to be 1.5×10^{-10} at 1s, going down to 3.5×10^{-11} at 40s and increasing again for long term integration because of temperature variations and laser-intensity induced clock frequency shifts.

Nevertheless, the short-term frequency stability results, similar to state-of-the-art results published by other groups with D2 line VCSEL, prove the potential of our Cs cell technology for micro-clocks applications.

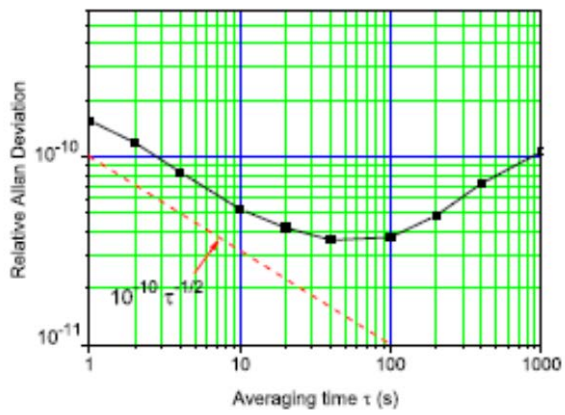


Figure 2.30 Allan standard deviation of the Cs-Ne microcell based clock.

2.6.2.3 Preliminary cell aging tests

For estimating preliminary the quality of microcells in term of sealing and stability of the cell atmosphere, several aging tests were performed. In a first test, a microcell filled with Ar was kept at 75°C during one month while optical absorption lines were scanned all along the test. By measuring the absorption peaks amplitude, no significant change was observed in the Cs density proving the strong sealing of cell. Further accelerating aging tests were performed by keeping cells filled with 6.6kPa of Ar at higher temperature. Cells were first heated at 115°C for 500h and then at 105°C for 2256h (about 94 days). Again, no significant change was observed. By utilizing the Q_{10}=2 method [Lambert 2000] in which life time of cell estimated by considering that rate of aging increase by the factor of 2 for every 10°C rise in temperature so lifetime of cell at 75°C clock operation temperature is at least 26048h (approx. 3 year).

Further, we did a set of CPT measurement to observe the variation of buffer gas pressure inside the microcell during accelerated aging tests. Microcells were kept inside the oven at 125°C. Every 2-3 days, the cell was taken out from the oven and inserted in the clock prototype to measure the Cs clock. For each CPT measurement, each parameter is kept constant like laser power, cell temperature, static magnetic field, locking parameter etc.

Figure 2.31 reports the evolution of the Cs clock frequency versus time. Each point is a measurement of the CPT clock frequency. No significant drift of the clock frequency was observed showing the good

quality of sealing of cells. Considering the experimental error during measurements, the clock frequency variation during the test is noticed smaller than 3 Hz. Such variation corresponds to a total variation of Ne pressure within the cell less than 6.13×10^{-4} kPa during the complete 3-weeks long aging test. Such results, even if not sufficient to prove to validate fully the cell aging, shows strong sealing of cell and correct stability of gas atmosphere inside the cell. Note also that this test was done onto a single cell and should be repeated with other cells to confirm the potential of the technology.

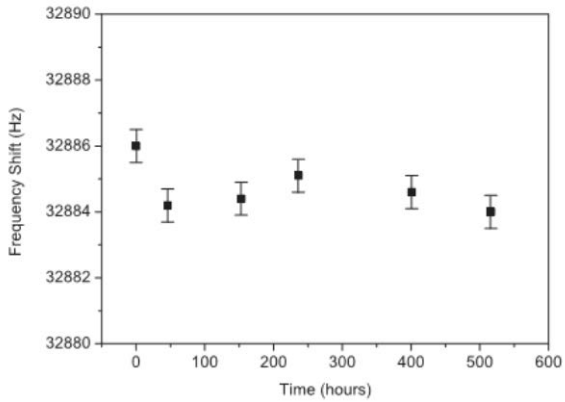


Figure 2.31 Aging test of microcells showing frequency shift around the unchanged frequency of Cs with respect to time of aging.

2.7 Conclusion

In this chapter, our main motive was development of the technology for transmissive version of micro vapor cell (T-cell). In the beginning of this chapter, DRIE process has been optimized in order to fabricate deep silicon cavity up-to 1.4mm. Several DRIE process parameters (like resist thickness as an etching mask, process temperature, oxide etch stop, aspect ratio dependent etching and post DRIE wet KOH etching) and pattern design as well has been optimized to have sufficiently smooth side walls of cell. Following the DRIE, anodic bonding process was developed to seal the silicon/glass stack (resulting from the standard anodic bonding of glass and silicon consisting through etched cavities) and glass under buffer gas atmosphere to fill the cells with buffer gas. Original anodic bonding process was proposed to fabricate the microcells filled with Ar or Ne at required pressures. Considering the electric breakdown of gas at required bonding voltage, a two-step bonding process was proposed to achieve a strong and high-quality sealing. In this method, the cells are pre-sealed by anodic bonding in the buffer gas atmosphere at a voltage lower than the breakdown voltage, followed by the complete sealing of the cells by the additional bonding performed in air at high voltages. Microcells were characterized through the optical and CPT spectroscopy. It was demonstrated that microcells are filled with buffer gas at an appropriate pressure for CSAC applications. Aging tests proved the quality of the cell sealing reliability and the stability of the cell

atmosphere (Cs and buffer gas) for a long time. All these results suggest that these microcells are suitable for the integration into portable atomic frequency references. Towards the further miniaturization of vapor cells thus micro atomic clock, another version of vapor cell based on the reflection of light inside the silicon is presented in the chapter 4.

Chapter 3 Thermal analysis for thermal management of fully LTCC packaged Cs vapor cell

In this chapter, we study the thermal behaviour of the fully packaged transmissive version of Cs vapor T-cell for the thermal management of MAC-TFC. In the framework of MAC-TFC, alkali vapors micro-cells along with the different components of the clock (VCSEL, detector, micro optical components, etc.) are embedded in a Low Temperature Co-fired Ceramics (LTCC) structure, which is highly suitable for hybrid integration. LTCC is a well-established multi-layer technology, featuring the ability to integrate various elements (heaters, sensors, electronics, wires, shielding) in one module only, with high reliability, stability and alignment accuracy [Karioja 2006]. In the case of MACs, where magnetic and thermal environment have to be controlled, LTCC technology will allow to achieve a high level of miniaturization with low processing costs.

This LTCC structure has then to be temperature controlled since VCSEL frequency and various properties of CPT resonances in Cs vapor cells are temperature dependent [Knappe 2002]. Indeed, because of the mean velocity of the Cs atoms (typically 230 ms^{-1} at 60 °C) in comparison with the cavity dimensions (order of magnitude: 1mm), the CPT line-width is easily broadened. Thus, the frequency stability of the clock cannot be achieved without the addition of a so-called buffer gas (usually N_2, He, Ne, Ar) [Beaty 1958, Allard 1982]. The buffer gas is then required in order to prevent wall relaxation, to increase the atom-light interaction and to reduce the Doppler broadening. However, interactions between caesium atoms and buffer gas introduce a shift of the atomic hyperfine transition frequency. This phenomenon depends on the nature of the gas, pressure and temperature according to a two order polynomial law [Vanier 1989]. In general, the resulting thermal frequency sensitivity is too high and, thus, a mixture of two gases inducing opposite linear frequency-shifts is required (i.e. by means of a compensation method: Ar and Ne for example). Recently, in the framework of MAC-TFC, a quadratic temperature dependence of the Cs ground state hyperfine resonance frequency in a single Neon buffer gas has been observed [Miletic 2010]. The relatively low inversion temperature, around 80°C, allows using one gas only and relaxes

slightly the constraints onto the cell fabrication and, in particular, on the pressure control. Nevertheless, the thermal management remains a challenging part since the temperature of the cell must be maintained to within several hundreds of milli Kelvin at all times during operation, using as little power as possible, although the range of ambient temperature can be 0 to 55°C. Then, a reasonable aim for the temperature sensitivity of the Cs-cell to the ambient temperature, once the temperature-control operates, is a few tens of milli Kelvin per Kelvin.

In this work, a thermal management approach considering a LTCC-based structure is presented. Several solutions are investigated in order to achieve a low-power temperature control.

3.1 Basic Thermal guidelines and concept

Basically, the MAC is made of several components that have to be temperature controlled. The Cs-cell, i.e. the heart of the clock, is surrounded by opto-electronic components (VCSEL and photo detector) to produce and detect the modulated optical beam, as well as optical components for shaping and polarizing the beam, and electronics to close the feedback loop of the modulating signal (Figure 3.1(a)). All these components are packaged in a LTCC structure.

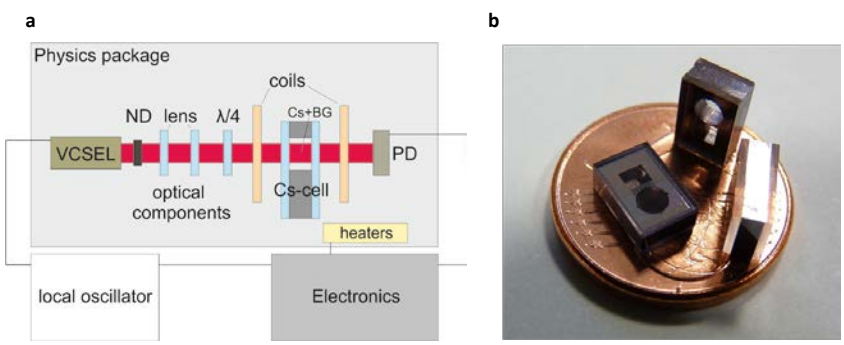


Figure 3.1 Schematic of a micro atomic clock. Physics Package is made of a VCSEL, several optical components (ND: neutral density, λ/4: quarter wave plate), coils to generate the static magnetic field, a cell containing Cs and buffer gases (BG) and a photo-detector (PD). The inner temperature of the physics package, especially the VCSEL and the Cs-cell, has to be controlled. (b) Photograph of Cs-vapor cells.

The objective is then to maintain the inner temperature of the physics package constant whatever the external temperature is, within a determined range. The latter changes depending on the applications of the atomic clock and should be ideally as large as [-40°C, 60°C] [Kitching 2004b] or [-40°C, 70°C] [Knappe 2007]. The definition of this range is actually essential because it fixes the thermal management approach and the amount of required power. For a rough assessment, the inner target temperature (T_{set}) can be written as:

$$T_{set} = T_{amb} + R \times (P_{elec} + P_{T-control}), \quad (3.1)$$

where T_{amb} is in Kelvin, P_{elec} (in *Watt*) is the power dissipated by the electronics (assumed to be a constant) located inside the volume to be temperature-controlled, $P_{T\text{-}control}$ (in *Watt*) is the controlled power ($0 \leq P_{T\text{-}control} \leq P_{T\text{-}control\_Max}$) dissipated by the heaters in order to maintain the inner temperature of the volume at T_{set} independently of the value of T_{amb}. Finally, R (in $K.W^{-1}$) denotes the overall thermal resistance of the system, from its heart at T_{set} to its surrounding at T_{amb}.

At first sight, it sounds reasonable to insulate as much as possible the physics package to reduce the power consumption. Indeed, when the ambient temperature is very low (for instance T_{amb} = -40°C), the overall thermal resistance R should be high in order to consume as less power as possible ($P_{T\text{-}control}$) and maintain an uniform temperature distribution inside the package. However, the waste heat generated by the embedded electronics cannot be ignored. Because of it (P_{elec}), high overall thermal resistance, i.e., well insulated packages, can lead to overheating of the cell, if the ambient temperature is high. Thus, in this case, the overall thermal resistance (R) should be low, since the maximum ambient temperature is defined by $T_{set} - R*P_{elec}$.

As a consequence, practically, such "ideal" ranges are difficult to achieve if one wants meanwhile to strongly reduce the power consumption. Indeed, for this purpose, it could be tempting to use a lot of waste heat coming from the embedded electronics (for lower ambient temperatures), but for high ambient temperatures, the waste heat has to be evacuated, thus R cannot be very high. After preliminary studies, obtained at room temperature [Kitching 2004b, Mescher 2005] and in order to evaluate the solutions required to contain the power budget (among which utilization of waste power), more complicated devices utilizing waste heat were developed. They include, e.g., variable thermal resistors made of an array of suspended thin gold beams electro statically actuated [Kim 2008], or thermal switches made of a bimetallic buckling disk [Laws 2008] in order to change, actively or passively respectively, the thermal resistance as a function of the ambient temperature. Although these solutions could allow to reach a wide range of temperature such as [-40°C, 50°C] with a limited power consumption (especially during transient regime), they strongly complicate the system and its fabrication, and are probably not yet highly reliable [Kim 2008] or not yet miniaturized enough [Laws 2008]. Consequently, for now, it seems more efficient to well insulate the physics package without benefiting from all the waste heat, as it can be seen in a recent and extensive thermal study of a CSAC, free of thermal switch, for which a range [0°C, 50°C] was considered [Laws 2009].

In addition to the range of ambient temperature, another important parameter is the target temperature (T_{set}). Indeed, depending on the alkali atoms or the buffer gas mixture composition, operating temperatures can be 70°C [Laws 2008, Laws 2009], 75°C [Mesher 2005, Kim 2008] or 80°C [Kitching 2004b] and are always above the ambient temperature. Thereby, only warming, less power consuming than cooling, is required, so that, in steady state, the thermal flux always flows from inside (the warmest elements are the heaters) to outside, through the enclosure.

In the following study, we will consider a Cs (in Ar-only environment) cell set at a target temperature equal to 80°C. This cell will be packaged in a LTCC structure so that the clock can be operated over the temperature range [0, 55°C] with power consumption lower than 150 mW in steady state. Several solutions will be examined in order to increase the thermal resistance of the system. It will be paid also attention to avoid overheating when the ambient temperature gets high. In addition, one aim will be to obtain a stable and uniform temperature inside the Cs vapor cell. It can be noted that depending on the application of such clock, the temperature range could be extended provided that an increase of the power consumption is acceptable.

In addition, the VCSEL has also to be temperature controlled. Nevertheless, because of its small volume (a 300µm x 300µm chip, a few 10µm thick), heating can be done with a limited amount of energy. It can be noted that the VCSELs used in the framework of MAC-TFC [Al-Samaneh 2010] are made and optimized to work at high temperature and then, should not see their lifetime decrease for such operating temperatures. Consequently, in the following, we will focus mostly on the temperature control of the cell, although the same solutions will be applied to the VCSEL.

It has to be noted that the total electrical power, required to run the clock, is used by the electronics (4.6 GHz oscillator, modulator, Synthesizer, control unit, RF oscillator, VCSEL power supply, etc.) and by the thermal management. Typically, one third of the total power budget can be attributed to maintain the physics package at a specific temperature, thus, requiring a careful optimization of the thermal performances.

Hence, we choose first to simplify the addressed problem as follows: control the temperature of a quite big volume (the cell) by means of a very small temperature sensor (typically a resistive transducer like a thermister, a deposited resistor, or a diode-based sensor) (Figure 3.2).

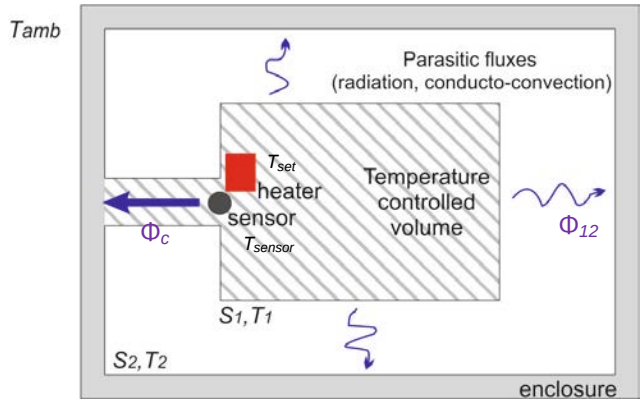


Figure 3.2 Sketch of exchanges. In case of vacuum inside the enclosure, radiation exchanges Φ_{12} exists. Otherwise, Φ_{12} is due to conduction by the air inside enclosure, and convection. Φ_c symbolizes conductive exchanges through solid supports between the cell and the enclosure. Ideally, if the parasitic flux Φ_{12} is negligible in comparison with $\Phi_c \approx P_{T\text{-control}}$, and when the main flux Φ_c is concentrated into a controlled path, the volume can then be temperature-controlled and is rather isothermal at $T_1 \approx T_{sensor} = T_{set}$ (without power source other than that of the heater).

In this framework, a servo-control is able to lock the sensor temperature at the set temperature, by managing the power dissipated by the heaters. The ideal situation requires then, firstly, a small section of the conductive path at the sensor location so that the section temperature is the same than the sensor temperature, and, secondly, negligible thermal exchanges between the inner volume and the enclosure ($\Phi_{12}\approx 0$). Such situation would lead to a uniform temperature distribution inside the volume to be temperature controlled. It can be mentioned, referring to Equation 3.1, that *R* denotes the equivalent thermal resistance of both the conductive path and the "parasitic" path. In the following, two points have to be discussed to get an isothermal volume at the desired temperature: the conductive thermal path where the thermal flux can be controlled must be calibrated (Φ_c symbolizes conductive exchanges through solid supports), and the parasitic exchanges (flux Φ_{12}) all over the surfaces must be minimized (i.e., must be negligible in comparison with the controlled conductive flux).

In addition to the exchanges through solid support (Φ_c), i.e. made by "bulk" conduction, the exchanges between the volume to be controlled and the enclosure can have different origins. Indeed, the non-controlled flux (Φ_{12}) can be attributed to gas conduction and convection, or to radiation between the two surfaces S_1 and S_2. Let us, in the following, evaluate the relative importance of each way of heat transfer involved.

3.1.1 Analytical approach

3.1.1.1 Convection

Gaseous conduction and convection depends on the volume and the pressure inside the enclosure. Free convection of the air inside the enclosure can be examined according to the Rayleigh number R_a. In our case, the general characteristic length L (i.e. size of the gap between the temperature controlled volume and the enclosure) would be typically about 1 or 2 mm. For this value, R_a is much smaller than the critical value for which convection takes place, even at atmospheric pressure $p = 10^5$ Pa.

3.1.1.2 Gas conduction

Although convection does not exist in our case, heat conduction by air has to be considered. It can be sorted in four regimes according to the Knudsen number $K_n = l_{mfp} / L$, where l_{mfp} is the molecular mean free path inversely proportional to the pressure p. Then, in secondary vacuum, i.e., for $p < 1$ Pa and $K_n > 10$, the relevant regime is the so-called free-molecule regime; for 1 Pa $< p < 10^2$ Pa and $10^{-1} < K_n < 10$, it is the transition regime; for 10^2 Pa $< p < 10^3$ Pa and $10^{-2} < K_n < 10^{-1}$ the slip-flow regime (or temperature jump), and finally, $p > 10^3$ Pa, $K_n < 10^{-2}$ corresponds to the continuum regime.

The academic model of conduction through a gas layer between two parallel plates at temperatures T_1 and T_2 is usable and rather close to the actual concerned situation (see Figure 3.4(c) and Figure 3.6). In the free molecule regime, the thermal flux per unit of area (in W.m^{-2}) between the plates can be written [Bird 1994, Springer 1971, Kennard 1938]:

$$\varphi_{FM} = -\left(\frac{8k_B}{\pi m}\right)^{1/2}\left(\frac{\alpha_1\alpha_2}{\alpha_1+\alpha_2-\alpha_1\alpha_2}\right)\left(1+\frac{\xi}{4}\right)\left(T_1^{1/2}-T_2^{1/2}\right)p \qquad (3.2(a))$$

where k_B is the Boltzmann constant, m the molecular mass, ξ the number of internal degrees of freedom, and α_1 and α_2 the accommodation coefficients of the hot plate at T_1 (close to T_{set}) and the cold plate at T_2 (close to T_{amb}), respectively.

In the continuum regime the heat flux (in W.m^{-2}) is given by the well-known Fourier heat conduction law:

$$\varphi_C = \frac{k(T)}{L}\left(T_1 - T_2\right) \qquad (3.2(b))$$

Where *k(T)* is the gas thermal conductivity which depends on temperature *T*. It can also be described by means of the dynamic viscosity of air, its heat capacity at constant volume, and the ratio between the heat capacity at constant pressure and the one at constant volume.

Between both previous regimes, F. S. Sherman proposed the following interpolation for a practical calculation of the transition regime [Sherman 1963]:

$$\varphi_{TR} = \frac{1}{1+\frac{\varphi_{FM}}{\varphi_C}} \cdot \varphi_C \qquad (3.2(c))$$

This model of two parallel plates is relevant for the heat exchanges between each surface of the warm Cs-cell at T_{set} (S_1 or one part of S_1 at $T_1 = T_{set}$ in Figure 3.2) and the facing surface at the ambient temperature (surface S_2 at uniform temperature $T_2 = T_{amb}$).

In the case of conduction through the air, the thermal flow (in W) outgoing from S_1 can be expressed as:

$$\Phi_{12\_c} = S_1 \times \varphi_{12\_c} = S_1 \times h \times (T_{set} - T_{amb}) \qquad (3.3)$$

Where h is an exchange coefficient (in$Wm^{-2}K^{-1}$), and φ_{12_c} is given by one of the equations (3.2), depending on the gas pressure.

3.1.1.3 Radiation

Further heat exchanges have needed to be considered is radiation exchanges between the surfaces. Many surfaces are involved in radiation exchanges inside the enclosure because of the multiple reflexions. Let's consider more general condition of radiation exchange by a surface j with surface k which is described by the equation given below.

Net radiation flux from the surface = outgoing radiation –incident radiation

$$\varphi_j^R = \varphi_j^{out} - \varphi_j^{inc} \qquad (3.4)$$

Based on the same assumptions of opaque grey surfaces, isotropy, etc, the leaving flux per unit of area φ_j^{out} can be described as the sum of the emitted flux according to the Stefan-Boltzmann law, i.e., $\varepsilon_j \sigma T_j^4$, and the reflective part of the incident flux, equal to $(1-\varepsilon_j)\varphi_j^{inc}$, since the absorption coefficient is equal to the emissivity:

$$\varphi_j^{out} = \varepsilon_j \sigma T_j^4 + \left(1 - \varepsilon_j\right)\varphi_j^{inc} \tag{3.5}$$

Moreover, inside an enclosure, the incident flux φ_j^{inc} is the sum of the fluxes coming from all the *n* surfaces of the enclosure, seen by the surface *j*.

$$\varphi_j^{inc} = \sum_{k=1}^{N} f_{jk} \varphi_k^{out} \tag{3.6}$$

Where the view factor[2] f_{jk} is the fraction of the thermal flux leaving the surface *k* that reaches the surface *j* [Holman 1986].

This gives

$$\varphi_j^R = \frac{\varepsilon_j}{1 - \varepsilon_j}\left[\sigma T_j^4 + \varphi_j^{out}\right] \tag{3.7}$$

Thus, it is possible to write each net radiation flux φ_j^R ($1 \le j \le n$) versus the *n* surface temperatures T_j (working as T_j^4) from Equations 3.4, 3.5, 3.6, involving the *n* emissivities and the $n \times n$ view-factors. Moreover, relationships exist between all the view factors.

Considering the simple case of two surfaces S_1 and S_2 which exchange only between them, and where both are assumed to be isothermal, at T_1 and T_2, respectively, opaque, diffuse and grey (with emissivity's ε_1 and ε_2 respectively), and characterized by uniform radiosity and irradiation. Then, the resulting net flux is (see [Taine 1995] for example, σ being the Stefan constant)

$$\varphi_{12\_r} = \frac{\varepsilon_1 \varepsilon_2 f_{12} \sigma (T_1^4 - T_2^4)}{\varepsilon_1 \varepsilon_2 + \varepsilon_1 (1 - \varepsilon_2) f_{21} + \varepsilon_2 (1 - \varepsilon_1) f_{12}} \tag{3.8}$$

With $S_1 f_{12} = S_2 f_{21}$

[2] http://www.engr.uky.edu/rtl/Catalog/

$$\Phi_{12\_r} = S_1 \times \varphi_{12\_r} = S_1 \times \frac{\sigma T_1^4 - \sigma T_2^4}{\frac{1-\varepsilon_1}{\varepsilon_1} + \frac{1}{f_{12}} + \frac{S_1}{S_2}\left(\frac{1-\varepsilon_2}{\varepsilon_2}\right)} \tag{3.9}$$

f_{12} being the associated view factor.

3.1.1.4 Comparison

Based on Equations (3.2) and (3.3), air conduction and radiation (Equation 3.9) between both surfaces are compared in Figure 3.3, as a function of the air pressure. It is clear that the air conduction can be almost suppressed by a pressure reduction until the secondary vacuum ($p < 10^{-1}$ Pa). In this case, radiation becomes the dominant heat transfer process and, a special attention should be paid to the emissivity coefficients of the surfaces.

One way to reduce them is to deposit low emissive coatings over the exchanging surfaces. As mentioned previously, the cell is made of a glass-silicon sandwich, sealed by anodic bonding. The silicon is a rather good conductor ($\lambda_{Si} \approx 140$ W.m^{-1}K^{-1}) but also an emissive material ($\varepsilon_{Si} = 0.5$ [Ravindra 2003], and glass is particularly emissive ($\varepsilon_{Glass} = 0.9$ [Lienhard 2008]) and a poor conductor ($\lambda_{glass} \approx 1.2$ W.m^{-1}K^{-1}). Once packaged, the cell has its surfaces facing LTCC ones made of ceramics, whose emissivity and conductivity are respectively $\varepsilon_{LTCC} = 0.9$ [VTT data] *and* $\lambda_{LTCC} \approx 2.8$ W.m^{-1}K^{-1}. Emissivity can then be easily lowered by a metallic coating onto the surfaces: aluminium emissivity is for instance equal to 0.05 [Touloukian 1970], silver and gold ones are even lower. Consequently, coating all the surfaces of the cell and of the surrounding LTCC could, according to the Equation 3.9, reduce the amount of radiations by a factor 20. In addition to the vacuum environment, this solution is important to minimize the thermal budget, and especially to reduce temperature gradients inside the cell. Indeed, the larger the radiation exchanges are, the larger the inner temperature gradients. It has to be noticed that magnetic materials used for soldering/bonding pads or coatings- are prohibited because of the high sensitivity of atoms to the magnetic field, which can affect the CPT process.

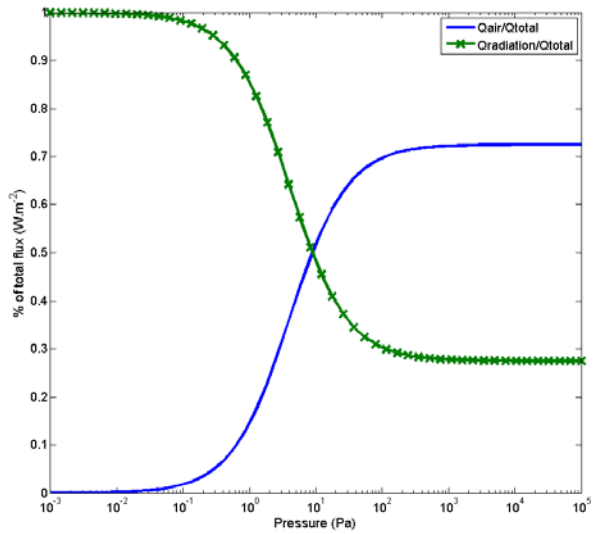


Figure 3.3 Relative importance of air conduction and radiation between two surfaces, versus pressure, according to Equations (5.2) - (5.9). For these calculations, the accommodation coefficients of both surfaces are equal to 0.8, emissivities are equal to 0.9, the view factor is f_{12} = 0.9, and the ratio S_1/S_2 is 0.1.

3.1.2 Selected topology

From the simple approach described above, parasitic fluxes Φ_{12} can then have different origins such as conduction/convection of air and radiation of surfaces. On the one hand, convection is negligible due to the small gap between the volume to be temperature controlled and the enclosure and, on the other hand, solutions such as, second vacuum packaging (typically 10^{-1} Pa) and proper metallic coatings on surfaces, should allow decreasing air conduction and surface radiation respectively. Therefore, we should now consider the problem of embedded electronics, and the thermal fluxes by bulk conduction that should be minimized and canalized in order to be controlled. It requires a more accurate description of the physics package architecture as it is done in the Figure 3.4.

Regarding the solid conduction, the principle of “bridges” as high thermal resistance links between the area to be temperature-controlled and parts submitted to ambient temperature changes has been selected. They allow the creation of an “island” on which the cell is hanged (Figure 3.4(a)). It has to be noted that the same structure, although a bit smaller, is made to suspend the VCSEL (Figure 3.4(b)). These “bridges”, similar to the one made of cirlex in [Laws 2009], are made of LTCC, i.e., a rather insulating material (≈ 2.8 $W.m^{-1}K^{-1}$), and their dimensions can be easily calibrated. A resistance of 17 *°C/mW* per bridge can then be achieved (bridges are about 0.5 mm width, 6 mm long, resistance calculation does not include the electrical leads). In addition, only one temperature sensor is needed to control the area

temperature, since symmetries operate. This sensor, along with the heaters, is buried into the multi-layers LTCC material.

From the data and guidelines discussed above, various topologies have been examined, e.g., a unique temperature-controlled insulated area supporting all the components (including some of the dissipative electronics) such as in [Laws 2008, Kim 2008], or a unique temperature-controlled insulated area incorporating the cell, VCSEL and the optics such as in [Mesher 2005, Laws 2009] or only the cell [Yougner 2007]. Finally, our selected solution (see Figure 3.4(b)) consists of two insulated islands: one including the Cs-cell and the photodiode, and one corresponding to the VCSEL. Each block is separately temperature-controlled at its own set temperature. The optics sub-system (including neutral density, two lenses and a quarter-wave plate) is itself separated from the VCSEL Island. Thus, the suspensions support only the VCSEL or the cell. The power dissipated by the integrated electronics located near the VCSEL (about 15 mW), is directly evacuated to the outside by conduction and does not heat the elements to be temperature-controlled. The enclosure surrounding the two LTCC packages is under vacuum.

In order to discriminate roughly the different topologies, simple calculations based on the electrical analogy have been performed. This approach allows to easily considering the temperature-control feedback loops and a trade-off between the insulation and the power distribution can be found. An example of resulting data is given in Figure 3.5.

Such approach can also allow the rough estimation of the transient behaviour of the mean temperature of the Cs-cell. For instance, at room temperature, and if the available heating power is limited to 100mW, less than a minute would be required to warm-up the Cs-cell at an operating temperature of 80°C.

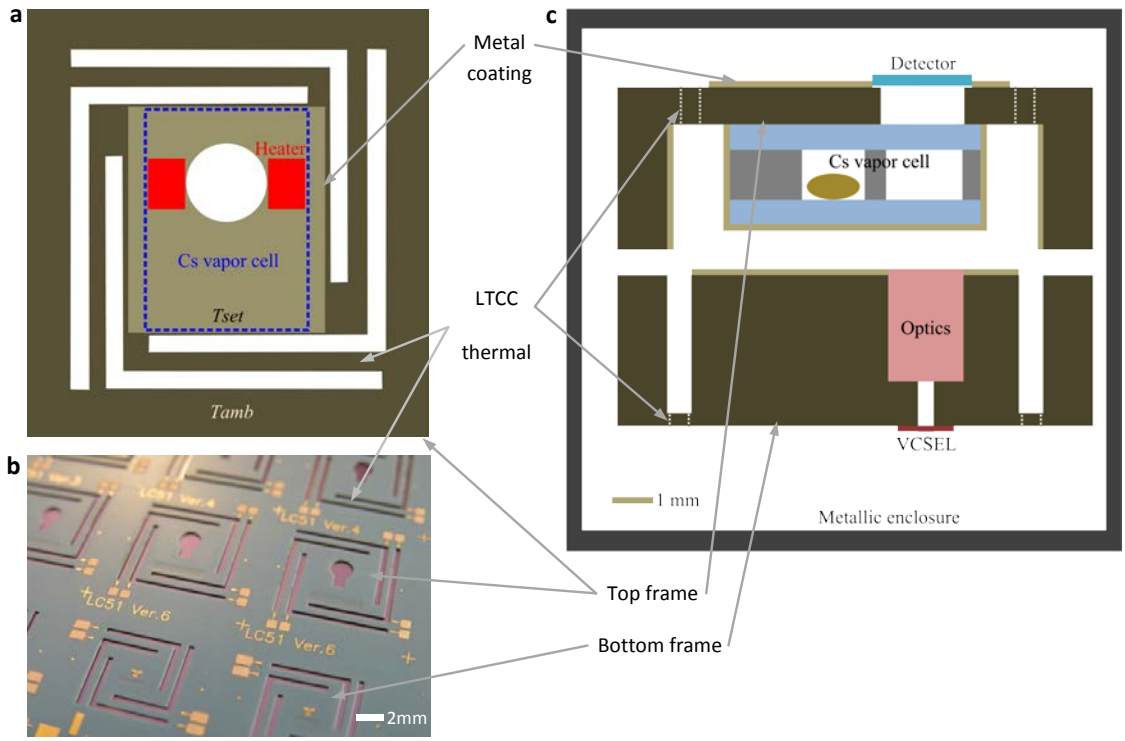


Figure 3.4 (a) Top View of demonstrated assembly that consists of 4 bridges and frame monolithic system to support the Cs-cell. The same principle is applied for the VCSEL temperature control. (b) Frames made of LTCC for hanging the cell (Top frame) or the VCSEL (Bottom frame). (c) Sketch of the cross-section demonstrator assembly; upper part is cell sub-system and lower part is VCSEL sub-system. All these components are packaged in a multi-layers LTCC structure and encapsulated under vacuum.

3.2 Finite element based analysis of selected packaging structure

According to Figure 3.6, heat exchanges through radiation should be examined for two different areas: The first one (case n°1), includes exchanges between the LTCC cell support and the metallic enclosure, whereas the second one (case n°2) concerns the exchanges between the cell surfaces and its facing ones made of LTCC, surrounding it similarly to a closed box.

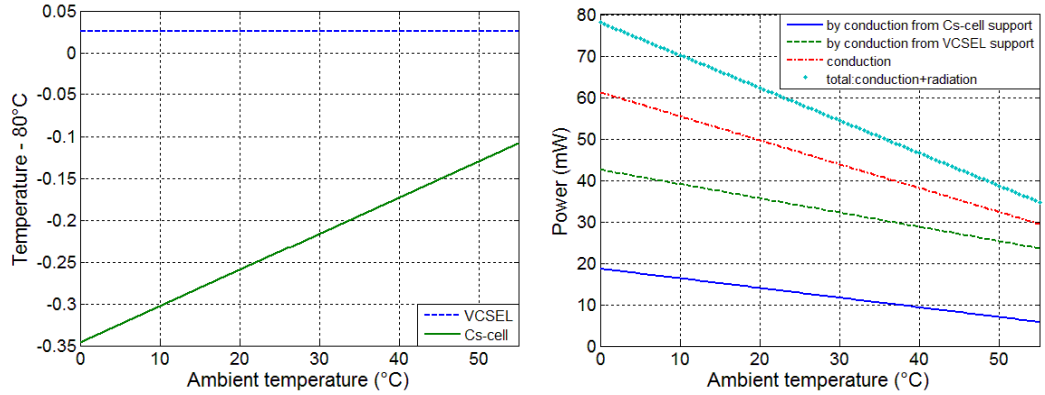
For the 2nd case, five sides of the cell are considered for exchanges with the facing LTCC surfaces. Since the cell is based on a glass-silicon sandwich, side's surfaces can be either only glass (bottom side) or include three "layers" made of silicon and glass.

Based on the same assumptions as for Equation 3.9 (opaque grey surfaces, isotropy, etc.), the net radiation fluxes φ_j^R $(1 \leq j \leq n)$ can be related to the n surface temperatures T_j (working as T_j^4) from Equations 3.4, 3.5, 3.6, involving the n emissivities and the $n \times n$ view-factors.

Although relationships exist between the view-factors, the system is difficult to solve analytically when more than three surfaces are considered. Then, it is relevant to use Computer-Aided-Design software, provided that it can take into account the complete radiation problem. *Intellisuite* is user-friendly and has been consequently employed to get a preliminary assessment. Basically, *Intellisuite* is able to simulate exchanges at boundaries thanks to an exchange coefficient h as described by Equation 3. This method, although convenient for conduction or convection exchanges, requires few approximations to consider radiation-based exchanges.

For instance, surfaces have been gathered in order to limit to two the number of surfaces involved in a system and expressions such as $(T_i^4 - T_j^4)$ have been derived into $4T_i^3\ (T_i - T_j)$, i.e. an expression compatible with a conduction or convection-type law, since the maximum temperature difference never exceeds 100°C inside the device. Then, for the case n°2 mentioned above, all the cell-surfaces are gathered into one having a mean emissivity equal to the weighted emissivities of silicon and glass according to their relative surfaces. This cell-surface exchanges only with one surrounding surface in LTCC, as described by Equation 3.9 where an appropriate view factor f_{12} is set[3]. Thanks to the previous assumptions, Equation 3.9 is then transformed in the form of Equation 3.3, which exhibits an exchange coefficient h.

[3] http://www.engr.uky.edu/rtl/Catalog/



(a) (b)

Figure 3.5 (a) Resulting offsets of Cs-cell and VCSEL temperatures versus the ambient temperature, in steady state, (b) Main thermal fluxes involves in the analyzed network, versus ambient temperature, in steady state. This type of results shows that the heaters are working all over the ambient temperature range, especially up to 55°C if necessary.

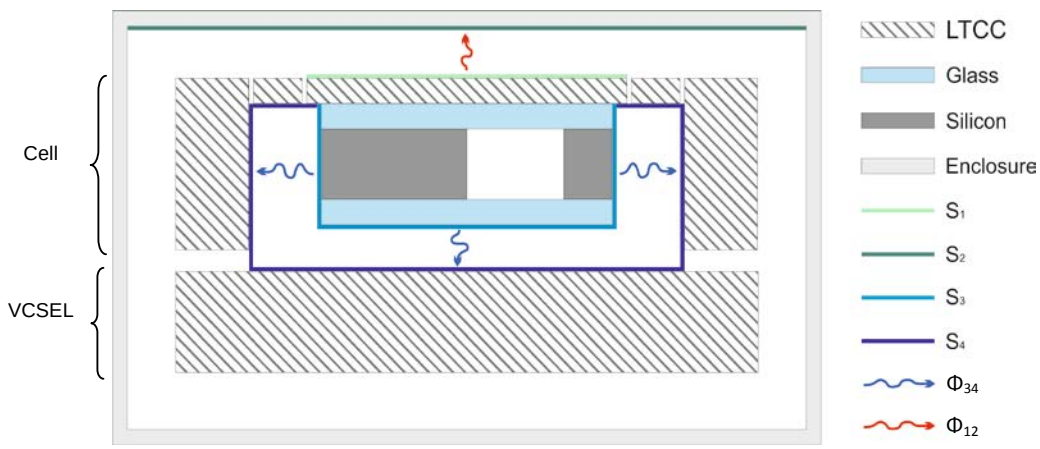


Figure 3.6 Radiation exchanges between various faces of packaged Cs cell.

Similarly, in case n°1, the rectangular LTCC Island supporting the cell is assumed to exchange only with its facing enclosure surface. For the both cases heat exchange coefficients, in order to perform static analysis using intellisuit to analysis radiation exchanges between the main couples of surfaces, as shown in Figure 3.6 that is to say: the LTCC cell-support with the enclosure in one hand, and on the order hand, the cell with the surrounding LTCC. The surfaces exchanging by radiation are assumed to be ideal like for Equation 3.3.

$$\Phi_{12\_c} = S_1 \times \varphi_{12\_c} = S_1 \times h \times (T_{set} - T_{amb})$$

For the case 2, radiation exchanges as shown in Figure 3.6 can be described as.

$$\Phi_{34\_r} = S_3 h_{34} \left(T_{set} - T_{amb}\right) \tag{3.10}$$

With heat exchange coefficients

$$h_{34} = \frac{\sigma T_{set}^3 \left(1+\frac{T_{amb}}{T_{set}}\right)\left(1+\left(\frac{T_{amb}}{T_{set}}\right)^2\right)}{\frac{1}{\varepsilon_3}+\frac{S_3}{S_4}\left(\frac{1}{\varepsilon_4}-1\right)} \tag{3.11}$$

And Radiation exchanges between the LTCC support with a surface area S_1 and the enclosure with S_2 (Figure 3.6.) can be described by the equation given below;

$$\Phi_{12\_r} = \frac{\sigma T_{set}^3 \left(1+\frac{T_{amb}}{T_{set}}\right)\left(1+\left(\frac{T_{amb}}{T_{set}}\right)^2\right)\left(T_{set}-T_{amb}\right)}{\frac{1-\varepsilon_1}{S_1\varepsilon_1}+\frac{1}{S_1 f_{12}}+\frac{1}{S_2}\left(\frac{1}{\varepsilon_2}-1\right)} \tag{3.12}$$

This equation describes the radiation exchange between two concentric rectangles and f_{12} is the view factor between these two concentric surfaces[4]. Once linearized, this equation becomes:

$$\Phi_{12\_r} = S_1 h_{12}\left(T_{set}-T_{amb}\right)$$

With

$$h_{12} = \frac{\sigma T_{set}^3 \left(1+\frac{T_{amb}}{T_{set}}\right)\left(1+\left(\frac{T_{amb}}{T_{set}}\right)^2\right)}{\frac{1-\varepsilon_1}{\varepsilon_1}+\frac{1}{f_{12}}+\frac{S_1}{S_2}\left(\frac{1}{\varepsilon_2}-1\right)} \tag{3.13}$$

Further, to get this exchanges coefficient values, three different cases have been considered: no metallic coatings, metallic coatings onto the LTCC part, and metallic coatings on both LTCC and the cell surfaces.

[4] http://www.engr.uky.edu/rtl/Catalog/

one with metal coated surfaces with which emissivity values of metal coated surfaces are considered 0.1 and another without any kind of metal coating for which emissivity values depends on the material which are ε_{Si}=0.5 for silicon, ε_{LTCC}=0.9 for LTCC, ε_G=0.9 glass, and ε_2=0.1 of metallic enclosure. And various surface areas are S_1= 36 x 10^{-6} m^2, S_2 = 625 x $10^{-6}m^2$, S_3 = 58 x $10^{-6}m^2$, S_4 = 246 x $10^{-6}m^2$. In the Equation 3.13, as radiative surface is much smaller than collective surface and all the radiations will be collected by surface 2 so view factor has been taken f_{12} ~1. Whereas T_{set} is the set temperature which is ~80 °C (converted in Kelvin in h_{34} and $h_{12,)}$ and T_{amb} is the ambient temperature which considered to be varied from 0^oC to 55^oC.

3.2.1 Applied power

The system temperature is measured by a sensor (T_{sensor}) embedded in the LTCC suspension and heaters are power-controlled through a feedback loop system amplifying the temperature difference between the sensor temperature and the set temperature (T_{set} ≈ 80°C in our case). The feedback loop (limited to a proportional action of gain G), controlling the dissipated power over a surface area S is then described by (the heating flux φ_h goes from outside the heater towards the area to heat):

$$\varphi_h \times S = -G(T_{sensor} - T_{set}) \tag{3.14}$$

In *Intellisuit*, an exchange coefficient h can then simply be identified as:

$$\varphi_s = -\varphi_h = h \times (T_{surf} - T_{env}), \tag{3.15}$$

where $h = G/S$, φ_s being the thermal flux going out from the surface, T_{surf} the surface temperature equal to that of an ideal sensor located at the temperature-controlled surface, and T_{env} the temperature of the imaginary environment. With such assumption, the controlled-power looks like a classical convection-type exchange usable in *Intellisuite*, and if G is sufficiently high, the heater surface temperature T_{surf} (i.e.T_{sensor}) tends to T_{env} which is set at T_{set}.

3.2.2 Simulation results

After testing different positions of heaters (and sensor), simulations with *Intellisuite* have been performed for three different cases; i.e. no metallic coatings, metallic coatings onto the LTCC part, and metallic coatings on both LTCC and the cell surfaces. Each case has been studied at three different ambient temperatures, i.e., 0°C, 25°C and 55°C in order to get the temperature sensitivity of silicon with respect to change in ambient temperature. Various simulation results are shown in Figure 3.7 for one interesting topology, and summed-up in Table 3.1.

3.3 Preliminary experiments

Preliminary experiments have been performed with a prototype of the Cell-submount, in order to validate the heating resistors and sensor for temperature control of the cell. The aim is to estimate the required power and the resulting temperatures. This prototype is made of a LTCC suspension structure where heating resistors and temperature sensor are embedded. The structure hangs a Cs-cell and the whole prototype is placed in a vacuum chamber (1 Pa) at 25°C. It can be mentioned that the LTCC as well as the Cs-cell are not coated with metal. Since the chamber is large compared to the prototype, it can be consider that the environment is equivalent to a black-body (emissivity close to 1). This situation is actually not optimal in terms of power consumption and thermal control. Thus, it corresponds more to the case without coating considered in the previous simulations. Some records are given in Figure 3.8.

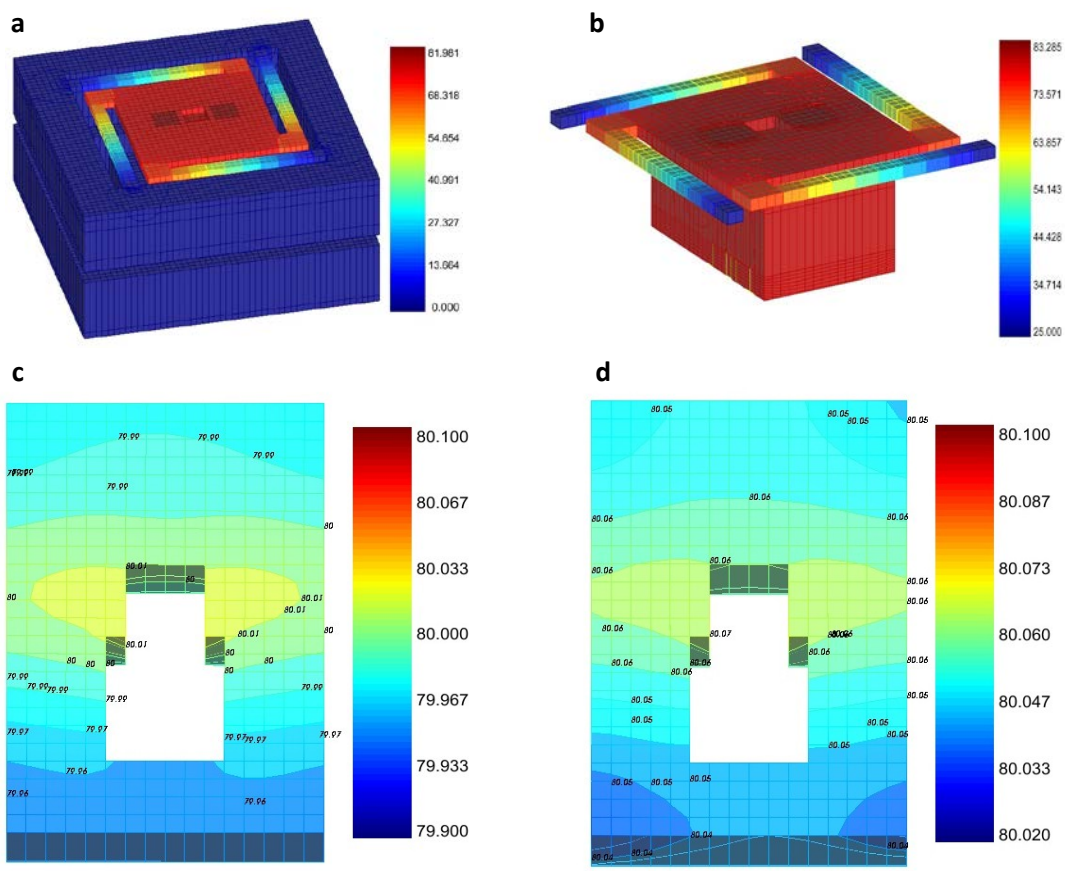


Figure 3.7 Simulation results as a temperature distribution of packaged Cs-cell, a) full package (Cell sub-mount and VCSEL sub-mount), b) cell hanged from LTCC bridge structure (with no coatings), c) Simulation results as a temperature distribution inside the silicon part, at 25°C ambient temperature, where surfaces are not coated and T_{set} = 83.3°C (set temperature to obtain T_{Si} =80°C). Maximum and minimum temperatures of silicon are 80.02°C and 79.95°C respectively, d) Temperature distribution inside the silicon part, at 25°C ambient Temperature where all surfaces are metal coated and T_{set} = 81.1°C. Maximum and minimum temperatures of silicon are 80.07°C and 80.04°C respectively.

Table 3.1 Mean temperatures and temperature gradients in the silicon part as a function of the ambient temperature considering or not metallic coating (values obtained from *Intellisuite*).

	No metal coatings			Metal coating onto LTCC			Metal coating on both LTCC & cell		
T_{amb} (°C)	T_{set} (°C)	Mean T_{Si} (°C)	Temperature Gradient in Silicon (°C)	T_{set} (°C)	Mean T_{Si} (°C)	Temperature Gradient in Silicon (°C)	T_{set} (°C)	Mean T_{Si} (°C)	Temperature Gradient in Silicon (°C)
25	83.32	80.00	0.075	81.64	80.00	0.040	81.10	80.00	0.030
0		78.92	0.100		79.46	0.056		79.61	0.041
55		81.53	0.040		80.88	0.020		80.62	0.014

Different values of the heat power have been applied to the heaters and the temperature has been recorded accordingly. From these different steps, a prototype thermal resistance (see Equation 3.1) around 830 $K.W^{-1}$ can be deduced. Then, 66mW and 96mW would be required to reach 80°C at T_{amb}=25°C and T_{amb}=0°C, respectively. With metal coatings, as shown by the previous simulations and a better vacuum, such power consumption should be significantly reduced.

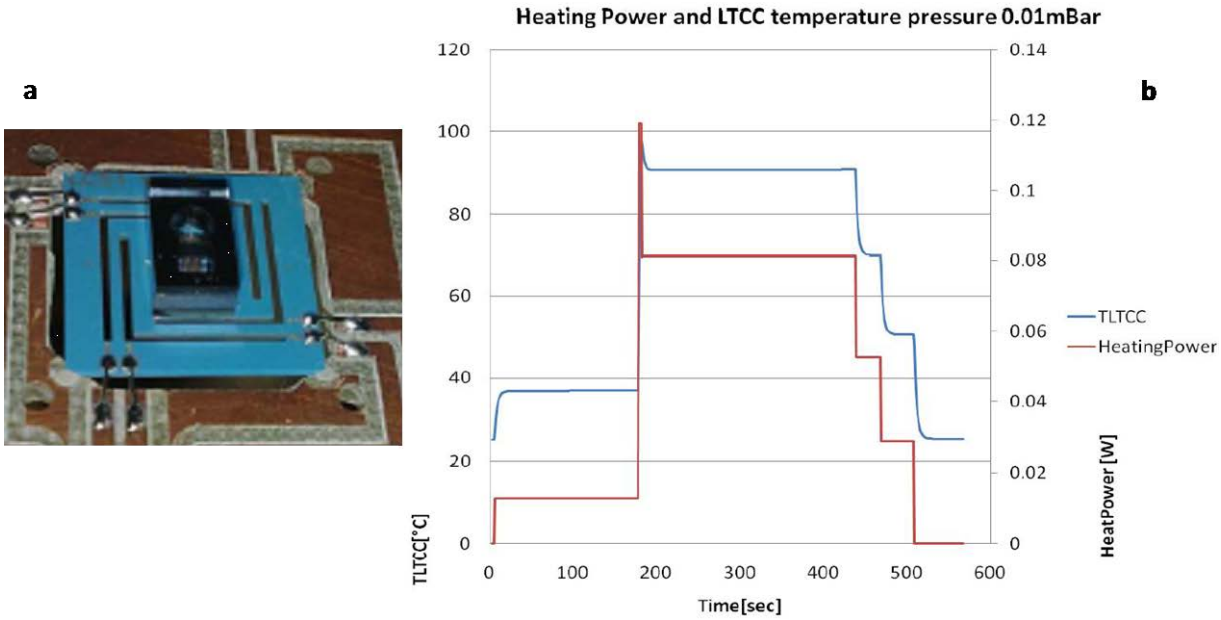


Figure 3.8 (a) The tested submount, i.e. the Cs-cell without coating glued on its LTCC support in which are embedded the heaters and the sensor, (b) Temperature in the LTCC island of the Cell-submount, measured by the embedded sensor, and power dissipated by the embedded resistors at room temperature. This is performed inside and enclosure at 1 Pa (10^{-5} Bars).

3.4 Dynamic adjustment of the set temperature

Simulations results described in Section 3.2.2 have shown that, in addition to vacuum packaging and bridges suspensions, metallic coatings improve significantly the temperature control by reducing the gradients inside the core, i.e. the Cs-cell, as well as the difference between the mean cell temperature and the set temperature. However, as it was mentioned previously, The temperature shift between the sensor and the silicon part of the cell still strongly depends on the outer temperature so that over 1°C shifts can be observed when the ambient temperature varies from 0°C to 55°C. This is a consequence of the cell architecture and the way it is glued on its LTCC stand. Because of the bad thermal conductivity of glass, the thermal conductance between the best temperature-controlled part, i.e. the sensor, and the interesting part, the silicon slice, is still quite low. The remaining parasitic flux flowing from the heaters close to the sensor through the sandwich of glass-silicon-glass generates this undesirable temperature gradient, and as a consequence, leads to a strong link between the temperature of the sensitive part and the ambient temperature. Thus, it would be preferable to adjust the set temperature as a function of the ambient temperature to compensate the resulting gradient as it is shown in Table 3.2.

Table 3.2 Mean temperatures and temperature gradients in the silicon part as a function of the ambient temperature when the set temperature is adjusted in order to get T_{Si}≈80°C (values obtained from *Intellisuite*).

T_{amb} (°C)	Mean T_{Si} (°C)	T_{set} (°C)	Temperature Gradient in Silicon (°C)
0	80	81.55	0.042
25		81.15	0.030
55		80.55	0.013

In such case, although the temperature gradient into the silicon still depends on the ambient temperature, the mean temperature remains equal to 80°C. The relationship between the silicon temperature and the ambient temperature can actually be electronically compensated [Galliou 2001]. This compensation consists in adjusting the set temperature as a function of the ambient temperature (measured by a second sensor at T_{amb}, for example or by monitoring the consumed power) instead of maintaining it constant (Figure 3.9). This correction function is obviously related to the ratio of the thermal resistances between the sensor, the silicon slice at T_{Si} and the outer enclosure at T_{amb}. By means of this electronic correction, the resulting temperature change in the silicon cell-core versus the ambient temperature change can be reduced by an expected factor of 10, typically,

Without any substantial increase of the power consumption, Consequently, such adjustment should allow to reach a temperature control of the solid parts of the cell around 100mK over the range [0°C, 55°C], with gradients smaller than 50mK.

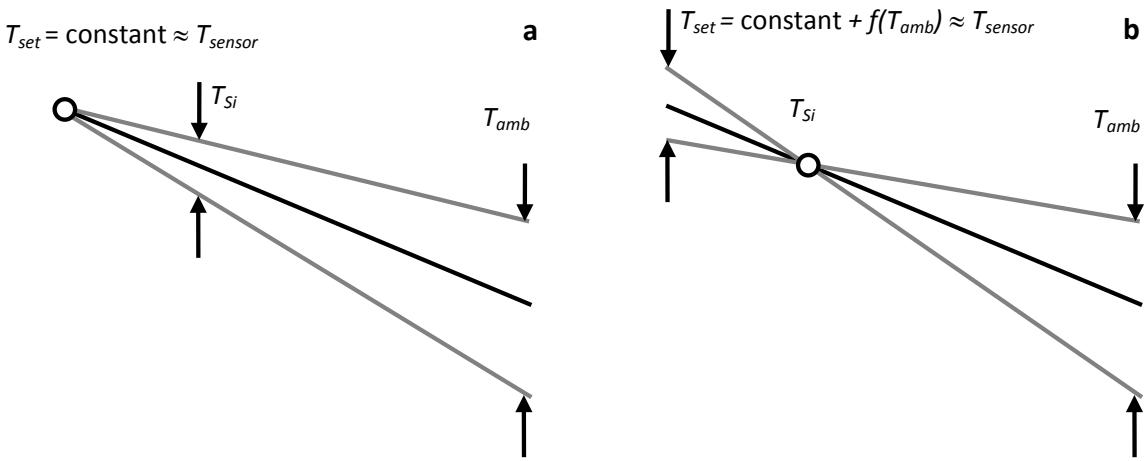


Figure 3.9 The actual situation where the set temperature T_{set} is a constant. Thus the silicon temperature T_{Si} still depends on the ambient temperature T_{amb}, (b) An illustration of the compensated set temperature varying according to the ambient temperature change: in such a way, the change of T_{Si} can be strongly reduced (ideally zero).

3.5 Conclusion

A study of the thermal behaviour of Cs-vapor cell packaged in a Low Temperature Co-fired Ceramics (LTCC) structure for chip-scale atomic clock application has been presented. . Different contributions to the thermal behaviour, such as bulk conduction, gaseous conduction and convection, and radiation, have been investigated by analytical modelling or finite element based softwares and several solutions have been proposed in order to keep the cell temperature constant during ambient temperature variations. Thanks to LTCC suspensions made of bridges, vacuum environment, and metallic coatings, it has been shown that reasonable power consumption, in the range of several tens of milliwatts, can be achieved for thermal control of the Cs-cell at an operating temperature of 80°C. In addition, thermal gradients inside the cell have been studied and it was shown that they can be limited to few millikelvins with appropriate coatings limiting radiations. Dependence of these gradients to the ambient temperature variations can moreover be significantly reduced by a dynamic adjustment of the set temperature.

Chapter 4 Design and technology of reflective version of atomic vapor cells

For miniaturized atomic clocks, different vapor-cell geometries have been proposed. As seen in the previous chapters, most of them are based on the transmission of light through the vapor-cell, which is generally based on sandwiched structures [Kitching 2002, Liew 2004, Nieradko 2008] and can then be called transmissive. Slightly different transmissive versions, based on glass blown spherical microcells [Eklund 2008], or on a reflective surrounding architecture [Youngner 2007], have also been proposed. For the latter case, the aim was to place the source and detector on the same side (see chapter 1, Figure 1.24) while routing the beam thanks to flat mirrors made of silicon outside of the cell (for better compactness). However, the beam was still going through the microcell which had limited thickness. "Real" reflective versions have been proposed in the phase II of the Symmetricom/Sandia project where the beam was crossing twice the Rb vapor (back and forth thanks to a mirror on one end) before to hit the detector located around the VCSEL (Figure 4.1(a)) [Mescher 2005]. It can be noted that such architecture has been withdrawn in the phase III of the project where a transmissive one has been preferred [Lutwak 2007]. Another reflective architecture was proposed by Perez et al. based on a wet-etched silicon cavity with suitable reflectors [Perez 2009]. The incoming beam was then vertical and reflected parts were collected by a photodetector located near the source (Figure 4.1(b)). The compactness was also the main argument for this architecture.

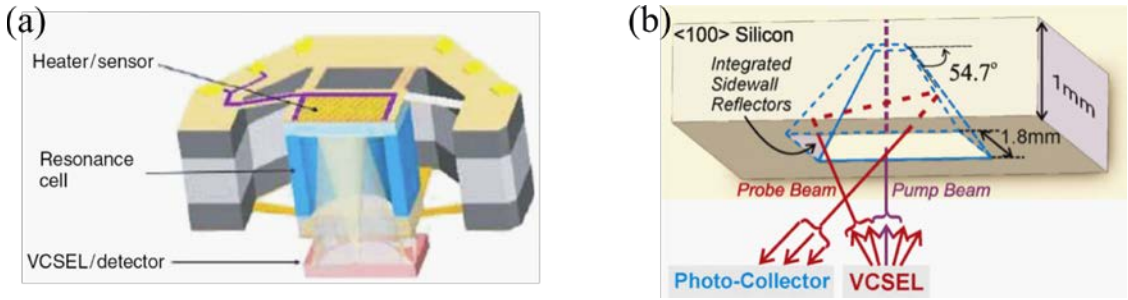


Figure 4.1 (a) reflective architecture of Symmetricom project with a flat mirror [Mesher 2005], (b) reflective architecture from Perez et al (NIST) with a reflective cavity made of (111) planes of silicon.

Our approach was different. In addition to better compactness, our wish was to be able to freely adjust the cavity length, i.e. in order to increase the light/atoms interaction, while removing technology constraints. In particular, and as shown in the previous chapter, the maximum length of the transmissive version is limited by the depth, achievable by deep reactive ion etching, e.g. 1.4mm in our case. Then, the first requirement was to propagate the light along the wafer plane (or wafer surface). In addition, for better compactness of the whole clock, choice was to locate source and detector on the same side (Figure 4.2) of a silicon cavity with integrated reflectors sealed by one borosilicate glass wafer.

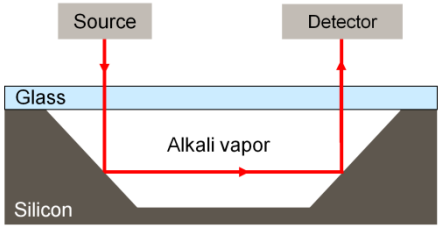


Figure 4.2 Basic idea of our Reflective R-cell.

However, to be able to use cavity sidewalls as reflectors, they have to be facing each other and be characterized by high surface quality. Such conditions require to use (111) crystallographic planes as sidewalls, which are orientated at 54.74° from the bottom plane (and not at 45° as drawn in Figure 4.2) (Figure 4.3(a)).

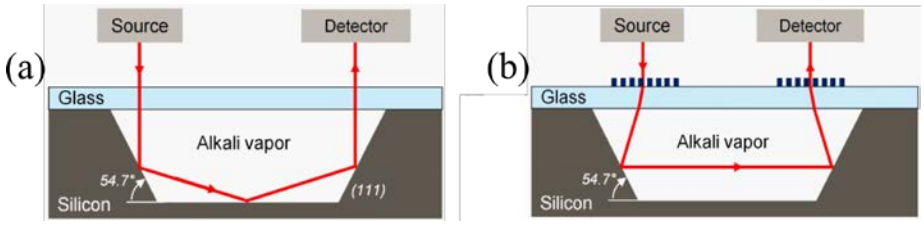


Figure 4.3 (a) silicon cavity with (111) planes (b) Gratings for angle compensation.

Since the consecutive additional reflection on the bottom plane (Figure 4.3(a)) was not suitable (for polarization state quality and colinearity of the light beam with static magnetic field), our proposition was to use diffraction gratings in order to compensate the angle of reflection resulting from the sidewall orientation (Figure 4.3(b)). With such architecture, the cavity length, i.e. interaction length, is freely adjustable by means of mask design during the lithography. The purpose of this chapter is then to describe the fabrication of such vapor cells, that we call Reflective (although light beam passes only once through the alkali vapor). This includes the cavity generation by wet-etching and gratings fabrication, and a report on their first characterization. It can be noted that increasing the interaction length is not the only advantage. In term of compactness, the interaction length might allow to reduce the beam diameter, requiring less cumbersome optical collimation setup. Thus, ideally, all the optical components could be integrated at a wafer level (Figure 4.4) ensuring a higher alignment accuracy (related to lithography) and less pick-and-place processing during packaging (by using e.g. molded microlenses and form-birefringent quarter wave plates). Moreover, the thermal control could be done from the cell bottom-side, made of silicon, far better thermal conductor than glass.

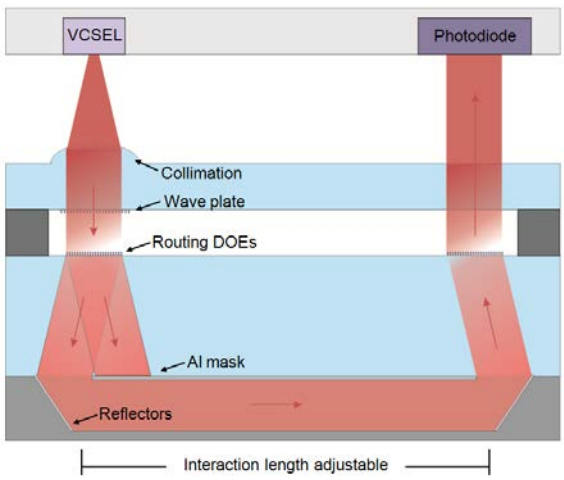


Figure 4.4 R-cell integration where all the packaging would be made at wafer level with micro-optical components leading to high compactness.

<u>Main points to consider for R-cell fabrication</u>

- *Sidewall quality of etched cavity should be smooth enough, i.e. close to a mirror surface. Efficiency of reflection has to be high.*
- *Diffraction gratings should allow maximum efficiency in the required direction without any perturbation of the circular polarization state of the incident beam.*

- *As for the T-cell, anodic bonding between silicon and glass under buffer gas environment has to be strong.*

4.1 Fabrication process

Figure 4.5 shows the process flow for reflective cell (R-cell) fabrication. First, cavity for the optical interrogation is etched by wet anisotropic etching (KOH) after deposition of a suitable mask for long wet-etching (Figure 4.5 (a), (b)). In the second step, cavity, intended to receive the Cs dispenser, along with the thin filtration channels (similar as for the T-cell) are etched by means of DRIE (Figure 4.5 (c), (d)). Channels connect then the two cavities with each other. Once the silicon, except sidewalls, has been protected (Figure 4.5 (e)), metallic mirrors (Al) are deposited onto the silicon (111) planes in order to increase the reflection efficiency (Figure 4.5 (f)). After placing the dispenser, the next technological step consists in anodic bonding of the silicon wafer to a borosilicate glass wafer under the buffer gas environment in order to seal the cavity (Figure 4.5 (g)). Apertures are then deposited on top of this sealed cavity for diffraction orders discrimination (Figure 4.5 (h)). The diffraction orders results from the symmetric type gratings as it will be explained later in this chapter. In parallel, diffraction gratings are fabricated on top of another glass wafer (Figure 4.5 (i), (j), (k)) which is subsequently aligned and bonded onto the cell wafer ((Figure 4.5 (l)). Finally, dicing of the wafer stack with protected gratings provides the individual R-cells (Figure 4.5 (m)).

For first R-cell characterization, dimension of the optical cavity was set to 650µm deepness and 1300µm width. Different cavity lengths, varying from 3mm to 9mm, in order to test the dependence of the CPT signal to the interaction length were patterned on the same wafer. In addition, dimensions of dispenser cavity are 1.3(length) x 1.3(width) x1mm (depth) to receive the dispenser of 1mm diameter and 0.6mm thickness.

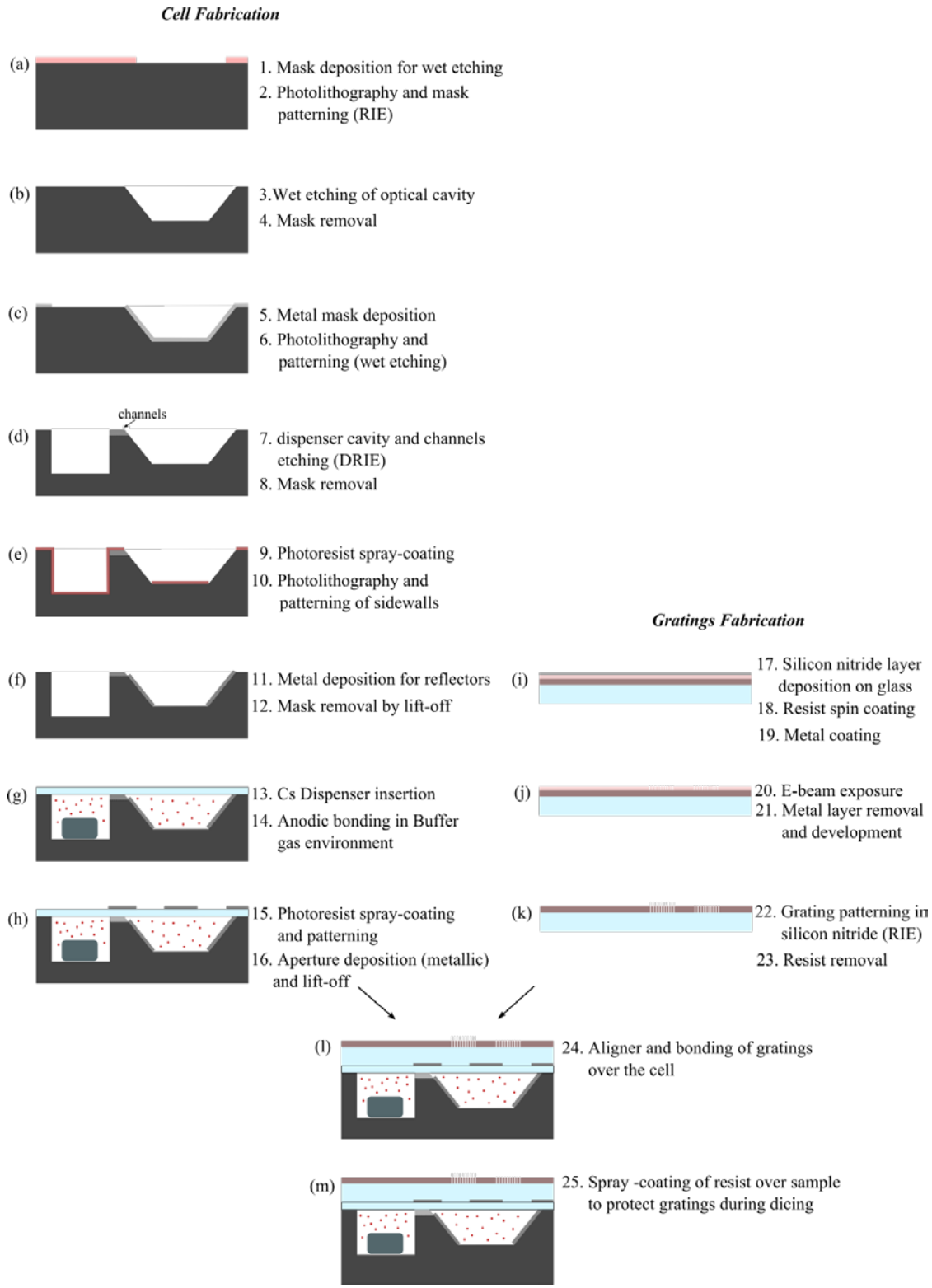


Figure 4.5 Fabrication process flow for the reflective cell.

4.2 Wet KOH etching of silicon R-cavity

As mentioned in the previous chapter, one important requirement of vapor-cell is to provide smooth sidewalls in order to reduce the atom/wall collisions (or wall relaxation of atoms) inside the cell. In chapter 3 dealing with technology of T-cell, DRIE process has been optimized to have smoothed enough sidewalls. Wet anisotropic etching of silicon is an alternative to DRIE that enables to provide usually smoother sidewalls, especially (111) silicon planes. In the case of R-cell, those planes are also used as reflectors, requiring even more flat surfaces (mirror-like) in order not to disturb the beam wavefront. Thus, the cavities are fabricated by chemical anisotropic wet-etching of bulk silicon, with alkaline solution. Because of the diamond structure of single crystal silicon, each crystalline plane is etched at a specific rate, leading to anisotropic shapes.

Among wet anisotropic etching solutions, we have chosen potassium hydroxide (KOH) because of its advantages over other alkaline solutions. Compared to, e.g. EDP, EDW, ethanolamine, NH_4OH/H_2O_2, hydrazine and TMAH solutions, KOH toxicity is low and it is rather cheap and not so sensitive to experimental factors (temperature, concentration, etc.). TMAH (tetramethyl-ammonium-hydroxide) is also widely used since selectivity of silicon dioxide in TMAH is higher than in KOH. However, TMAH creates rougher surfaces and anisotropic ratios are smaller.

Thus, KOH leads to strong anisotropy and also high etching rate. Etch rate of different orientated planes of silicon in KOH and TMAH solutions are given in Table 4.1 [Shikida 2000]. It can be observed that (111) plane has much lower etching rate than the other planes, which makes (111) plane an etch-stop. For example, etch rate of silicon (111) planes is 9nm/min whereas etch rate of (100) planes is 629nm/min. Thus, etching a (100) cut silicon wafer can result in a cavity whose sidewalls are made of (111) planes tilted at 54.74° from the surface (Figure 4.6).

Table 4.1 Silicon etch rate in KOH and TMAH [Shikida 2000].

	Etch rate ($\mu m\ min^{-1}$)		Etch rate normalized by that for (100)	
Orientation	34wt.% KOH (70.9°C)	20wt.% TMAH (79.8°C)	34wt.% KOH (70.9°C)	20wt.% TMAH (79.8°C)
(100)	0.629	0.603	1.000	1.000
(110)	1.292	1.114	2.054	1.847
(210)	1.237	1.154	1.967	1.914
(211)	0.983	1.132	1.563	1.877
(221)	0.586	1.142	0.932	1.894
(310)	1.079	1.184	1.715	1.964
(311)	1.065	1.223	1.693	2.028
(320)	1.285	1.211	2.043	2.008
(331)	0.845	1.099	1.343	1.823
(530)	1.273	1.097	2.024	1.819
(540)	1.283	1.135	2.040	1.882
(111)[a]	0.009	0.017	0.014	0.027

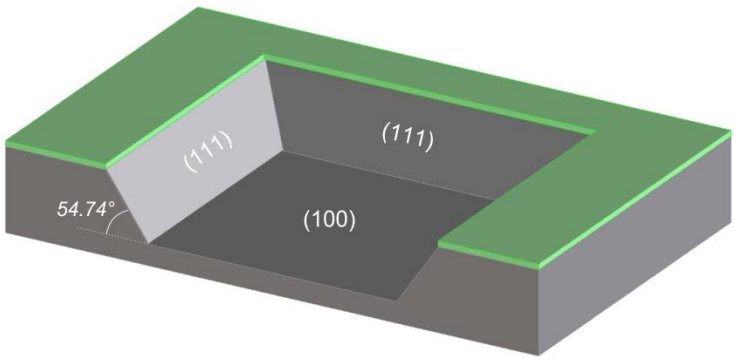


Figure 4.6 Cross-section of a R-cell cavity etched by anisotropic etching.

For R-cell fabrication, cavities generated by wet anisotropic etching are deep (in the range 600-800µm). Thus, few parameters are important, such as etch rate but also selectivity of the etching mask. For long etching, a high selectivity ensures mask protection (of parts not supposed to be etched) until the desired structure is obtained. Mask selectivity depends on solution concentration (e.g. Figure 4.7 showing the etch rate of SiO_2 as a function of the KOH concentration) and depends also on the method of deposition. Mostly used mask layers for anisotropic etching are thermally grown SiO_2 and/or low pressure chemical vapor deposited (LPCVD) silicon nitride (Si_3N_4). It can be noted that Si_3N_4 mask deposited by plasma-enhanced CVD (PECVD) is less resistive to the etchant. Finally, as mentioned previously, an important requirement concerns the sidewalls surface quality. Since the etching rate of (111) planes is low, their surfaces are usually assumed to be smooth, making them likely to be used as reflectors. However, as it can be seen in Table 4.1, (111) etch rate is small but non-negligible. Moreover, uniform etching does not depend only on the crystallographic orientation but also on parameters such as contaminants, oxygen

content inside Si, etc. Thus, if the etching lasts long, a uniform etch rate over the whole sidewall can be difficult to achieve in order to obtain a flat surface.

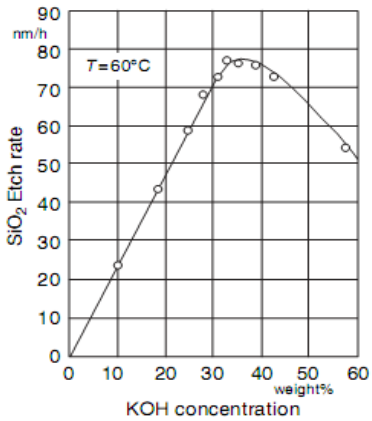


Figure 4.7 Etch rate SiO_2 with respect to KOH conc. At temp 60°C [Seidel 1990].

An etched silicon surface is actually always defined by some sort of persistent corrugations. Numerous studies have been devoted to the control of the roughness of the fast etching {100} faces. For instance, their surface roughness after etching was investigated using different purity grades of H_2O and KOH, different organic additives, such as isopropanol (IPA), or by dissolving oxygen or nitrogen gas in the etchant solution [Zubel 2001]. All these parameters were found to influence the roughness strongly. Compared to Si-(100), the roughness of the {111} faces received less attention. However, it has been reported that {111} surfaces are dominated by etch pits whose macrosteps are triangularly shaped (vertices pointing in the direction of the adjacent {100}) [Veenendaal 2001]. Depending on the concentration of etching solution, those macrosteps can also be hexagonally shaped with a different orientation [Gosálvez 2007]. The etch pits are said to be centered on edge dislocations bonding {111} stacking faults, induced by oxygen precipitation resulting in silicate formation during thermal process steps, such as deposition of a mask [Nijdam 2000]. This was actually reported initially by Kwa *et al*. who measured sidewall surface roughness as a function of the concentration and the temperature [Kwa 1995]. They found that minimum roughness is achieved for temperature equal to 50°C and concentration between 30 and 40 wt.% of KOH (Figure 4.8). In addition, they observed that float zone (FZ) wafers lead to roughness at least one folder smaller than the one obtained from Czochralski (CZ) grown wafers. Actually, a lower oxygen content can be expected from float-zone (FZ) wafers, i.e. below $10^{16}/cm^3$ while it is almost $10^{18}/cm^3$ for CZ-grown Si. Two years later, the same conclusions were obtained by Merveille [Merveille 1997], who found that temperature, metal contamination and mechanical stress due to holder have a minor influence onto the quality of Si{111}, unlike the mechanical stress in the bulk of the wafer material.

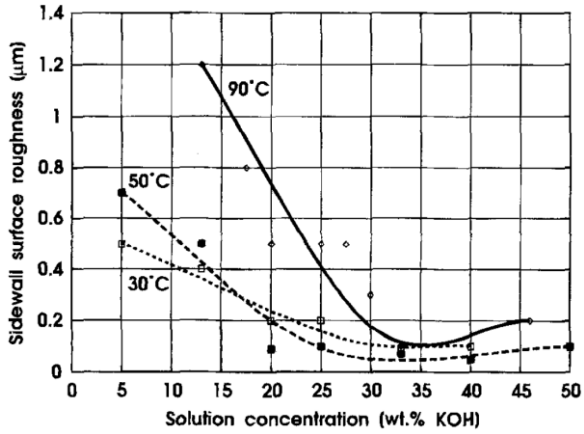


Figure 4.8 Sidewall surface roughness as a function of the solution concentration for different temperatures [Kwa 1995].

However, it is actually very difficult to unify the different features which appear somehow dispersed in the literature, especially since anisotropic etching depends on many parameters and since conclusions that can be applied to small cavities might not longer apply to deep cavities (a lot of articles studying {111} planes quality are based on 150µm deep cavities etched in (100)-cut wafers or directly onto (111)-cut wafers with short etching time). Thus, in the following, we tried to study different cases in order to improve the sidewalls quality of deep cavities needed for R-cell generation. These cases include study of mask alignment, solution stirring, mask type, etc.

According to Kwa *et al*. conclusions [Kwa 1995] (Figure 4.18), we use KOH solution with 40%.wt concentration to lower the roughness. Since the solution temperature is not so critical [Kwa 1995, Merveille 1997], the solution is warmed-up at 80°C (on a hot plate) to maintain a high-enough etch rate. KOH etching setup is shown in the Figure 4.9.

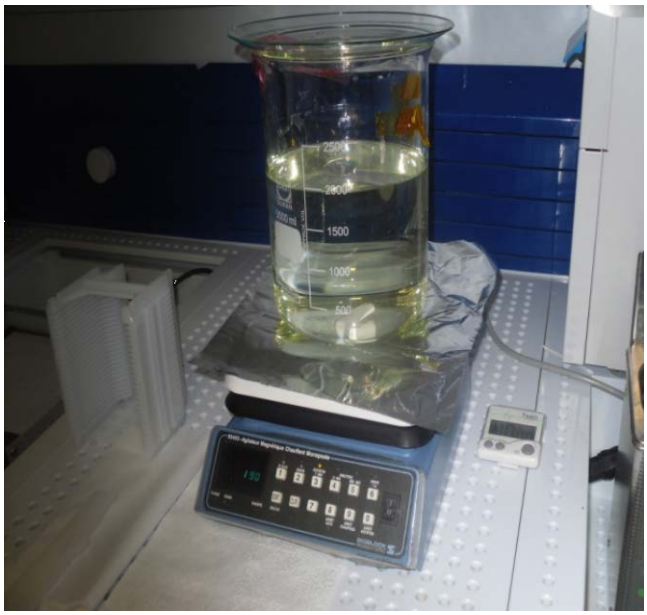


Figure 4.9 KOH etching setup.

4.2.1 Effect of mask alignment with crystalline plane of silicon

First concern for KOH etching experiments was about alignment requirements of the mask pattern with crystal planes at lithography level. Usually, wafer-flat is defined with accuracy not better than 0.5° to 1° compared to the actual crystalline planes. Thus, two options are available: either to perform a pre-alignment procedure requiring a first lithography step in order to identify the crystalline planes orientation, or to use a mask providing self-alignment, e.g. with an elliptical instead of squared footprint. In order to study the influence of such approaches onto the roughness of the {111} planes, we compared cavities etched with elliptical and squared mask openings, the latter being slightly misaligned by purpose between 0° and 1° (step of 0.1°).

For accurate alignment of the squared mask, one method proposed by Ensell [Ensell 1996] to align the mask to the 110 direction with the accuracy of 0.1^{o}C has been utilized. Basic principle is to perform a first lithography step on the sides of the wafer to etch a test pattern (Figure 4.10(a)) with the same KOH solution. The corresponding mask is made of a series of circles, set radially and symmetrically onto the sides of the wafer, whose total angular range varies between 0° and 2.5° with steps of 0.1°. Quick wet-etching performed through such mask made of circular openings leads to pyramids orientated along the wafer crystal planes (Figure 4.11). Then, square-shape windows will be seen from the top and most of these squares are misaligned with neighboring pyramids as shown in Figure 4.11(b). The three successive patterns, best aligned (Figure 4.11(a)) compared to tangent of the arc, define the position of the alignment window (Figure 4.11(c)).

Such alignment marks are used for the subsequent main etching mask during the KOH experiments. Following this method, it is possible to achieve alignment of mask pattern with crystalline plane up-to 0.1°, i.e. around 10 times more accurately than from wafer-flat.

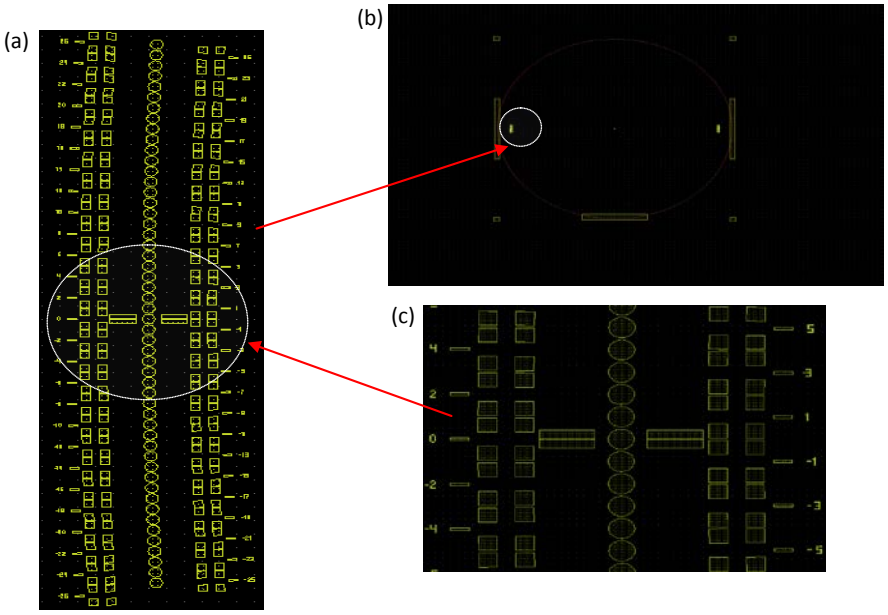


Figure 4.10 Mask design for mask alignment with crystal plane. (a) pattern etched on the two sides of the wafer (b) patterns location on the wafer, (c) detailed pattern with circular openings in the column at the middle.

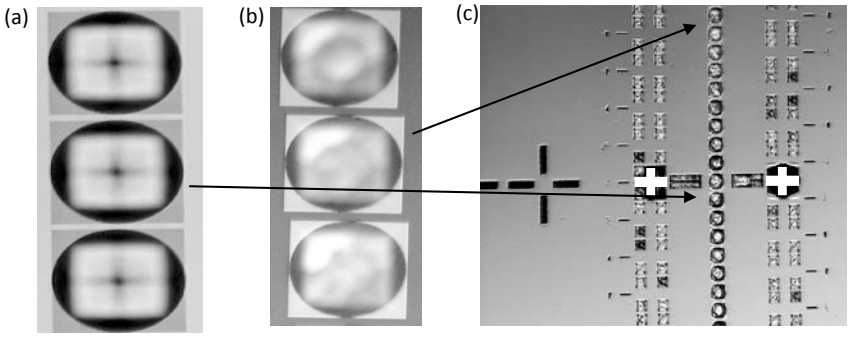


Figure 4.11 Circle converted into pyramid after KOH etching (a) best three aligned pyramids (b) misaligned pyramid (c) alignment of main etching mask of device.

Tests of alignment requirement were performed on CZ-grown and FZ-grown wafers with different types of masks. Typically, steps due to the misorientation appear from 0.3° misalignment. Figure 4.12 shows, as an example, sidewalls etched in a FZ-grown wafer through a SiO_2/Si_3N_4 mask without stirring (40%.wt KOH at 80°C). It can be noted that since, e.g. pits, are very shallow, randomly distributed and of different size, it is difficult to observe the morphology by profilometry or by AFM. To be able to observe the whole sidewall, simple optical microscopy was preferred (after dicing of the cavities), although the results are only qualitative. Thus, steps are visible for all misalignments larger than 0.3° (Figure 4.12). A pre-alignment procedure is then required since alignment requirement is stricter than the wafer-flat accuracy.

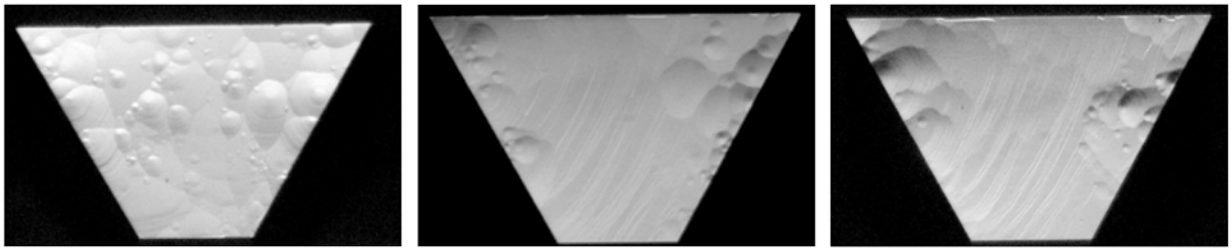


Figure 4.12 cavity sidewalls obtained after KOH etching, showing surfaces resulting from the mask alignment/misalignment with (100) plane of silicon.

Another option is to use a self-aligning mask, whose opening has an elliptical shape (Figure 4.13). For the same reasons than the pre-alignment procedure explained earlier, the cavity is consequently self-aligned and no steps are visible, even if the main axis of the ellipse is misaligned regarding the (110) direction (tested up to 1°) (Figure 4.14). In all our tests, sidewalls quality resulting from etching through elliptical masks was equivalent to the sidewall quality of well-aligned squared masks. Consequently, such mask shape could allow skipping the pre-alignment procedure, however, since the sides of the (111) planes are better protected, the cavity is, at first, still slightly elliptical and more opened in the middle than at the sidewalls used as reflectors (see top view of Figure 4.14). To overcome this, etching time needs to be longer than for squared masks, which can result in surface quality degradation. Consequently, in the following, we will consider square openings aligned with a pre-alignment procedure.

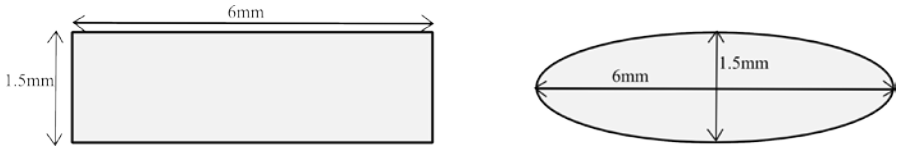


Figure 4.13 Main etching masks (rectangle and ellipse) for KOH experiment.

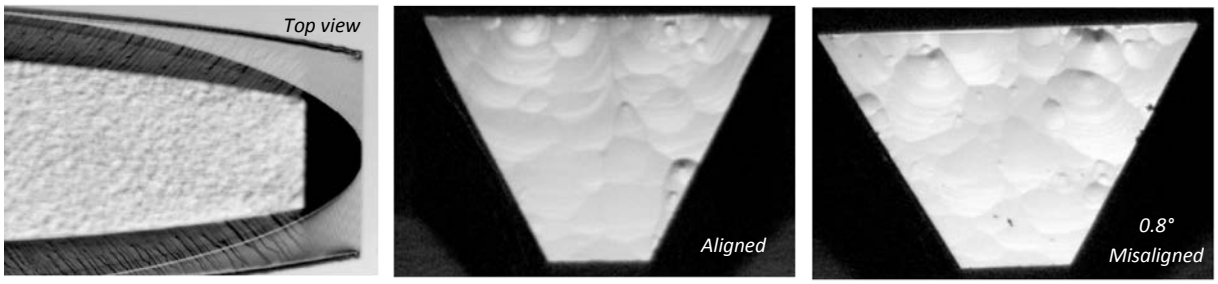


Figure 4.14 Cavity sidewalls obtained after KOH etching with an elliptical mask showing surfaces resulting from the mask alignment/misalignment with (100) plane of silicon.

4.2.2 Effect of stirring

From Figures 12 and 14, it can be seen that even with a correct alignment of the mask, (111) planes are not flat and covered with pits. Since (111) planes etching is a "birth and spread" mechanism, blocking locations resulting from insoluble compounds formation or deposition of stable agents can result in micromasking. Different reasons of micromasking have been considered in the literature such as hydrogen bubbles, SiO_2 precipitates, metal impurities, etc [Schroder 1999, Seidel 1990, Gosalvez 2007]. Thus, in order to improve mass transfer of the etching mixture, stirring was first applied. The same wafer types (FZ-grown with SiO_2/Si_3N_4 mask) were tested with and without stirring. From Figure 4.15, it can be seen that stirring improve significantly the surface quality by decreasing the total number of pits. Such improvement might be explained by an enhancement of hydrogen bubbles detachment and/or a better diffusion of the reactants and etching products.

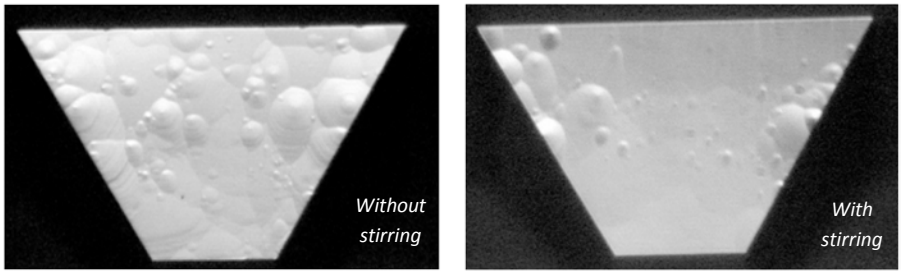


Figure 4.15 Cavity sidewalls from FZ-grown wafers (SiO_2/Si_3N_4 mask) etched without and with stirring of the KOH solution.

4.2.3 Effect of mask and wafer types

Nevertheless, the surface quality of (111) planes is not yet satisfactory. Another explanation of such micromasking (by blocking locations) might be {111} stacking faults, induced by oxygen precipitation resulting in silicate formation during thermal process steps, such as deposition of a mask [Nijdam 2000]. Since oxygen content is lower in FZ-grown than in CZ-grown wafers (by two orders of magnitude), and since different mask material can be used (requiring different processes having different operating temperatures), several combinations have been tested based on CZ- and FZ-grown wafers and SiO_2/Si_3N_4, LPCVD Si_3N_4, or PECVD Si_3N_4/Au masks which are summarized in Table 4.2.

Table 4.2 Tested samples (wafer and mask type).

	Wafer type	Mask	Oxygen content / crystal defaults	Process temperature for mask deposition
1	FZ-grown	SiO_2/Si_3N_4 (500nm/150nm) (thermal oxidation/LPCVD)	**Low**	**High** (1100°C/800°C)
2	FZ-grown	Si_3N_4 (80nm) (LPCVD)	**Low**	**Medium** (800°C)
3	CZ-grown	Si_3N_4 (80nm) (LPCVD)	**High**	**Medium** (800°C)
4	CZ-grown	Si_3N_4 /Cr/Au (80nm/20nm/220nm) (PECVD/PVD)	**High**	**Low** (450°C/200°C)

For the sample n°1, etching mask is made of thermally grown silicon dioxide (500nm) and LPCVD silicon nitride (150nm). Since selectivity of silicon dioxide for KOH etching is 1:200, LPCVD silicon nitride, whose selectivity is much higher 1:10000, is, in addition, deposited on top of it. Such mask can allow to achieve deep cavities inside the silicon. For the sample n°2 and sample n°3, thermal oxidation of silicon was skipped and LPCVD nitride (80nm - sufficient for etching depth down to 1mm) was deposited at 850°C directly onto the silicon surface (FZ-grown for sample n°2 and CZ-grown for sample n°3. Concerning sample n°4, gold was deposited onto a CZ-grown silicon wafer. To deposit gold layer (220nm) by means of PVD, first PECVD silicon nitride (80nm at 450°C) and then Chrome (20nm) was deposited on the silicon to enhance the adhesion to the substrate. During the gold deposition, the substrate was kept at 250°C.

After the mask patterning, RIE has been used to open the windows in the etching mask layers and expose the silicon surface to the KOH solution. Thus, etching was performed until cavities of ~750µm depth were generated inside the silicon with an etch rate of ~1µm/min (~12hours) (KOH concentration 40%.wt and 80°C temperature while the solution was stir with magnetic stirrer). This was done for the samples n°1, 2 and 3. However, for the sample n°4, cavities were etched only until 400µm with an etch rate of 0.4µm/min (~16hours) (KOH concentration 40%.wt and 65°C temperature). The temperature of the solution, lowered to 65°C because of stress induced in the gold layer at 80°C that results in pinholes, is the reason of the lower etching rate. In addition, although gold selectivity is very high (better than silicon nitride) in KOH, under etching during the increasing of etching depth results in mask edges breaking and then in gold particles deposited on the etched surfaces. This can lead to micro masking and to formation of micro pits. To avoid this contamination from the gold layer, substrate was cleaned with piranha solution

(H_2O_2/H_2SO_4) after every 70µm of etching (each ~3hours). Such subsistent cleaning of substrate during the etching was found really effective and resulted in very clean surfaces.

Resulting cavity sidewalls from KOH etching are shown in Figure 4.16. It appears that samples n°1, 2 and 3 are characterized by a lower quality than samples n°4. Although it can be noted that sample 4 was not etched so deeply than the other samples (400µm instead of 750µm), it seems that correlation between oxygen content / stacking defaults and high temperature processes to deposit the mask is the origin of the degradation of the sidewall quality. In other words, FZ-grown wafers are not of good enough quality to endure high temperature processes (see sample n°1 with thermally grown SiO_2 at 1100°C) whereas CZ-grown wafers could be of enough quality if a low temperature process is applied for mask generation (see sample n°4 with PECVD Si_3N_4/Au at maximum 450°C). The latter proves that with a proper lower temperature mask generation of better convenience and selectivity (at high temperature) than the one we used for the sample n°4 , it might be possible to use much cheaper CZ-grown wafers, e.g. for higher volume production.

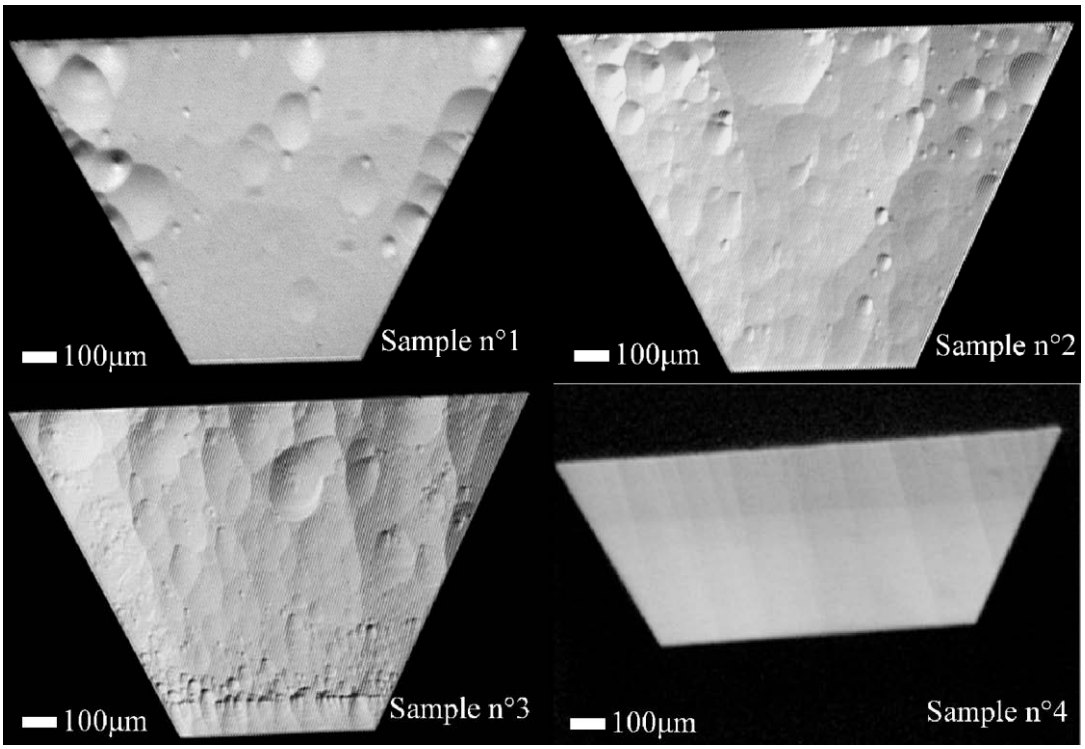


Figure 4.16 Cavity sidewalls from the four samples described in Table 4.2 etched with stirring of the KOH solution.

As a counterpart, quality of (100) bottom planes has been also checked (Figure 4.17). Such planes are not used as reflectors but a good quality is preferable for wall relaxation containment. For (100) planes, mask process temperature seems to be crucial since the quality of the bottom planes are getting better along with temperature decreasing. No significant difference can be noticed between FZ- and CZ-grown wafers with same mask (LPCVD Si_3N_4). It can be noted that temperature of the KOH solution was also lower for the sample n°4.

After the fabrication of wet-etched optical cavities inside the silicon, the next step consists in generating the dispenser cavity. This is done by DRIE after protection of the optical cavity by metallic mask (Figure 4.5 (c), (d)). During the same process, the channels connecting both cavities are also formed. However, their depth is smaller due to aspect ratio proportionality of DRIE etching. Thus, metallic mirrors are deposited onto the sidewalls after a new protection of the wafer (Figure 4.5 (e), (f)). Once placing the dispenser, and as for the T-cell, the cavities are sealed by means of anodic bonding under buffer gas environment. Few details are given in the next section.

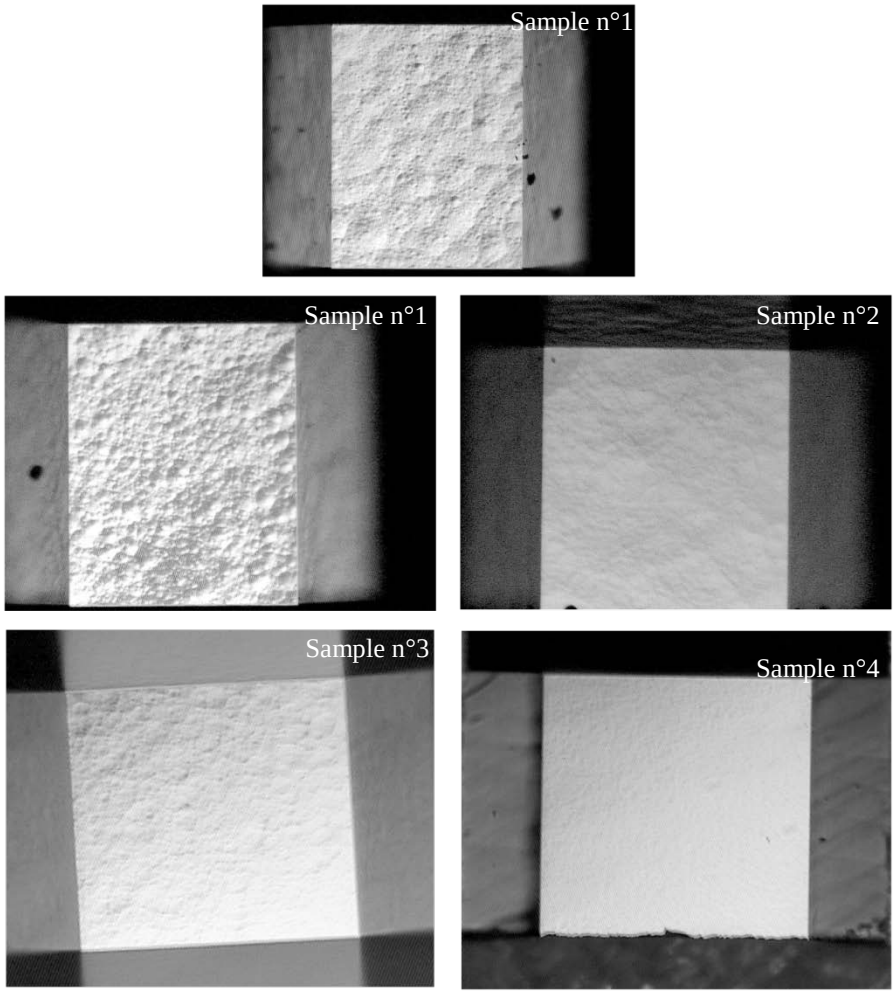


Figure 4.17 Cavity bottoms from the sample n°1 without stirring and from the four samples described in Table 4.2 etched with stirring of the KOH solution.

4.3 Anodic bonding

Anodic bonding process which was presented in the Chapter 3 for sealing of T-cell cavities under buffer gas has been also used for R-cell. Schematic of anodic bonding chamber in case R-cell is shown in Figure 4.18. Main difference for anodic bonding process between T-cell and R-cell is the space between the top and bottom electrodes. In case of T-cell space was 5.52 mm whereas it is equal to 5.02mm for R-cell. Since breakdown voltage depends on the spacing between the electrodes, according to the Paschen's law breakdown voltage for the R-cell needs to be determined as a function of the gas pressure. Thus, gas discharge experiments were performed similarly to the ones for T-cell. Silicon wafer was kept in contact with the bottom electrode (anode) and glass wafer was placed over the silicon wafer with a separation of 200microns (with separation flags). Resulting breakdown voltage values were recorded with respect to different values of gas pressure as it can be seen in the Figure 4.19. Following the two-step anodic

bonding explained in chapter 3, voltage should be, in the first step, lower than breakdown voltage at the corresponding gas pressure. For R-cell, gas (Ne) pressure of 150torr (20kPa) inside the cell is aimed and so, corresponding voltage must be lower than 300V. In the second step, anodic bonding is continued in air with application of high voltage (up-to 900V). It is important to note that the first round of R-cells that has been completed for characterization (presented later in this chapter) suffered from a technical problem (pressure gauge) during anodic bonding. As a result, the first set of fully integrated R-cells did not contain buffer gas (Ne). Another round of fabrication for which the problem has been solved is currently under progress during the writing of this manuscript.

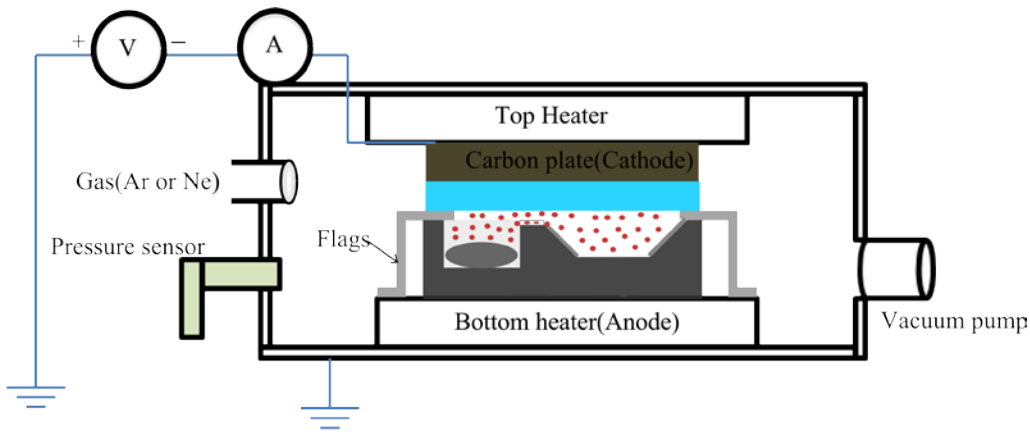


Figure 4.18 Schematic of anodic bonding chamber for R-cell fabrication.

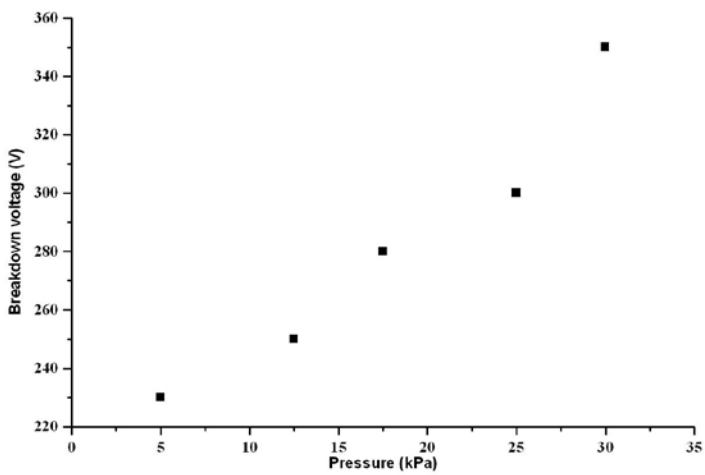


Figure 4.19 Breakdown voltages with respect to Ne gas pressure in case of R-cell.

4.4 Diffraction gratings for light routing

As it was explained in the chapter's introduction, once sealing of cavities by means of anodic bonding has been performed, we need to integrate diffraction gratings over the optical cavity in order to compensate the sidewalls slope and route the laser beam horizontally inside the cavity.. In order to compensate 54.74° angle of silicon (111) plane, light must be incident on the (111) plane at an angle of 35.26° compared to the normal of the sidewall and thus, must exit from the glass wafer with an angle of 19.48° (Figure 4.20). To achieve this angle, light should be diffracted by the grating inside the glass at an angle deduced from the Snell-Descartes law (Equation 4.1).

$$n_{Sio_2} \cdot \sin\beta = n_{inscell} \cdot \sin\alpha \tag{4.1}$$

Where n_{SiO2} is the refractive index of glass and $n_{inscell}$ the refractive index inside the cell.

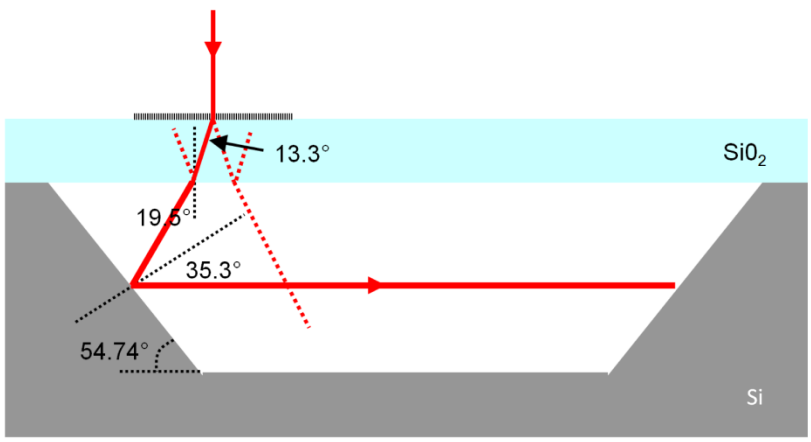


Figure 4.20 R-cell cavity with integrated gratings.

If we consider the refractive index of borosilicate glass (Borofloat) to be n_{SiO2}=1.4645 at λ=894.1nm, the angle of diffraction into the glass window has to be equal to 13.28°. It is important to mention at this point that such gratings have to diffract, into the latter angle, circularly polarized light, without disturbing the polarization state (for CPT). Considering the rather high diffraction angle and the requirements of circular polarization state, blazed gratings have not been chosen since their efficiency into the 1st order was not very high (~65%) although their aspect ratio was high and since they would have make order discrimination more complicated. Instead, we decided to employ binary symmetrical gratings (also more convenient for replication) and then, to use first diffraction order to route the light. The requirements for such gratings are consequently to diffract most of the light into the first order and also to maintain polarization state of the incident light in this first order. Since only one order out of -1 and +1 orders needs to be routed inside the cavity, apertures are incorporated for diffraction order discrimination (Figure 4.21 –

Al mask). This step is done after the sealing of the cavity before the assembly with the gratings wafer (Figure 4.5(h)). It can be noted that apertures could probably be integrated inside the cavity to keep only the thickness required for orders discrimination (as it is drawn on Figure 4.4), however, strict alignment during anodic bonding would be required and it was not done for the first tests. Further tests on the minimum diameter of the beam required for clock performances are also planned, since smaller diameter would allow quicker order discrimination and consequently using a thinner grating wafer.

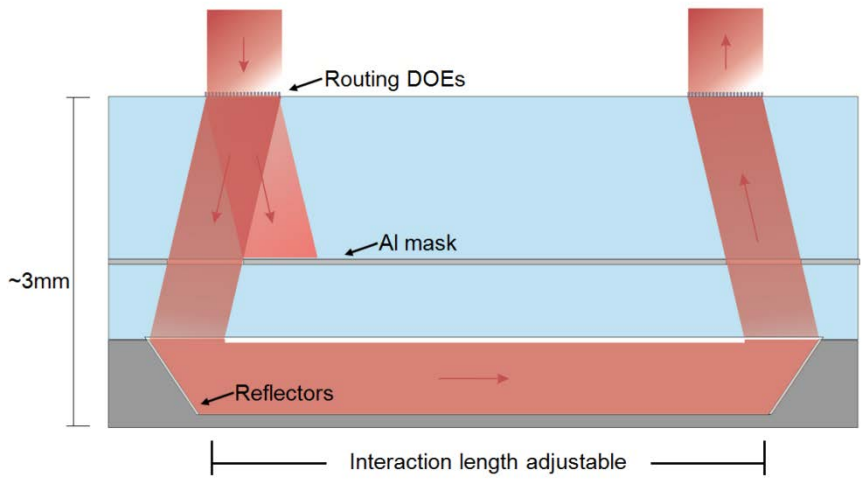


Figure 4.21 R-cell cavity with integrated apertures for diffraction order discrimination.

The angles in which the orders are diffracted are defined by the grating equation:

$$n_{Sio_2} \cdot \sin \alpha_m = n_{air} \cdot \sin i - m\frac{\lambda}{d} \tag{4.2}$$

Where i=0° and d is the period of the grating. Then, the period of the grating to diffract the first order, e.g. at λ=894.1nm into an angle of 13.28° is d=2683nm. The next step consists in grating thickness and fill-factor optimization in order to, on the one hand, maximize the efficiency into the first order whereas cancelling the zero and other higher orders, and on the other hand, avoid any polarization deterioration into the first order, i.e., that the gratings provide same efficiencies for TE and TM polarizations without phase shift. Such optimization is performed by rigorous Fourier modal method (FMM) [Turunen 1997].

Thus, experiment was done in two parts. First, gratings were designed and fabricated for λ=632.8nm for easiness of measurements so that the fabrication process can be optimized. . After the successful optimization, gratings for λ=894.1nm were fabricated to be integrated onto the R-cell. In addition, tests were performed for grating made directly in fused silica or in a silicon nitride layer deposited onto a glass

wafer. Grating parameters and expected efficiencies/phaseshift resulting from design are summarized in Table 4.3.

Table 4.3 Parameters for the binary gratings.

Wavelength λ (nm)	**632.8**		**894.1**	
Gratings stripes	SiO_2	Si_3N_4	SiO_2	Si_3N_4
Period *d* (nm)	1897.9		2682.3	
Fill factor *f*	0.45	0.465	0.433	0.461
Line-width *l* (nm)	854	882	1161	1236
Thickness *h* (nm)	700	312	1000	470
TM -TE efficiency / phaseshift in 1st order	39.41%-39.95%/0.42°	38.72%-38.72%/0.04°	39.19%-40.20%/0.01°	38.03%-37.58%/0.00°
TM - TE efficiency in 0 order	2.86% - 2.00%	1.32% - 0.75%	3.15% - 1.75%	0.45% - 0.25%

According to the design, gratings stripes made of Si_3N_4 allow a lower thickness and a lower zero order efficiency. Moreover, phaseshift is also smaller; however maximum transmitted 1st order efficiency is in the range of 38% whereas almost 40% can be achieved with SiO_2. It can be noted that better control of the thickness can be obtained with Si_3N_4 (RIE etching rate of Si_3N_4 being faster). For the tolerances, if phaseshift < 1° and maximum deterioration of efficiency of 1% are taken as criteria, typical linewidth tolerance is ±30nm and thickness ones are ±20nm (SiO_2) and ±12nm (Si_3N_4) (in case of a stable refractive index value).

4.4.1 Fabrication of gratings

To fabricate the diffraction gratings, electronic lithography (E-beam) has been utilized and several experiments have been performed in order to optimize various parameters such as exposure doses and exposure linewidth (to obtain correct grating linewidth after development and etching). Brief description of electronic lithography has been described in the second chapter. In this section, we present fabrication process flow for gratings.

The first grating tests were made with stripes made of SiO_2. We then used PMMA resist followed by lift-off to generate a metallic mask, resistant enough to etch glass until 700nm.Figure 4.22 shows the corresponding fabrication process flow. At first, SiO_2 wafer was cleaned by acetone and ethanol followed by 10min cleaning in oxygen plasma. It was then coated with PMMA A4 resist with thickness of 300nm and baked on a hot plate for 10min at 180°C. After baking, sample was kept at room temperature for 4 to 5 hours followed by sputtering of 10nm chrome over the resist in order to avoid charging during e-beam

exposure. Optimized e-beam parameters for our process were set at 10KV, 10μm aperture and 7mm working distance and 1.30 μC/cm^2 doses with 100 μC/cm^2 nominal doses. After the completion of e-beam exposure, chrome layer was removed and resist was developed in MIBK: IPA for 20-45s followed by inserting in IPA for 30s to stop the reaction Thus, chrome was evaporated on the sample and kept inside the remover 1165 for 3 hours to lift-off the resist from the sample and transfer the metallic pattern over the glass wafer. It was then etched by RIE (CHF_3:C_2F_6, 10:5) at 120W power and 60μbar pressure. Glass (SiO_2) sample was etched for 16 minutes at the rate of 40-45nm/min to get depth up-to 700nm.

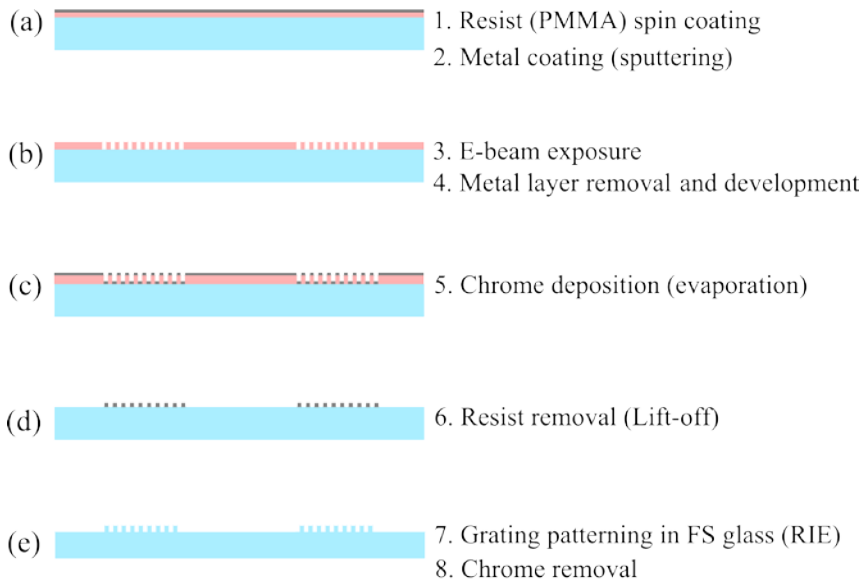


Figure 4.22 Fabrication process flow for gratings in fused silica.

Some of the samples were diced in order to control cross-sections of gratings with SEM. Figure 4.23 shows a SEM image of fabricated gratings. Resulting line-width and thickness of gratings are in the required ranges and summarized in Table 4.4.

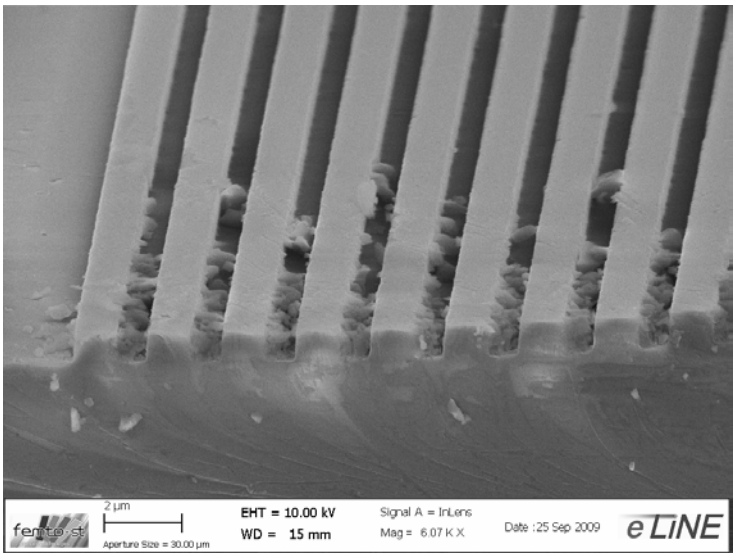


Figure 4.23 SEM image of the fabricated gratings in fused silica (dirt results from dicing).

Table 4.4 SEM results for grating cross-section.

Gratings parameters for λ=632.8nm	Target	Measured
Line width	854 ± 38nm	863nm
Thickness	690± 20nm	680nm

Gratings were tested optically utilizing He-Ne laser at λ=632.8 nm as shown in the Figure 4.24. During optical tests, angle of first diffracted order along with the efficiencies of all generated orders and associated polarization states were measured. Angle of 1st diffraction order was measured equal to 19.4°±0.3° whereas target angle was 19.43°. Measured efficiencies and ellipticities of generated diffractive orders are summarized in Table 4.5. It can be seen that most of the light is diffracted into the first orders whereas the zero order efficiency is low (0.6%). In addition the circular polarization state of the incident light (ellipticity = 1.05) is not disturbed significantly (-1st order ellipticity = 1.12) although depolarization is experienced in zero and second orders. Such results are in good agreement with design and requirements for light routing in R-cells.

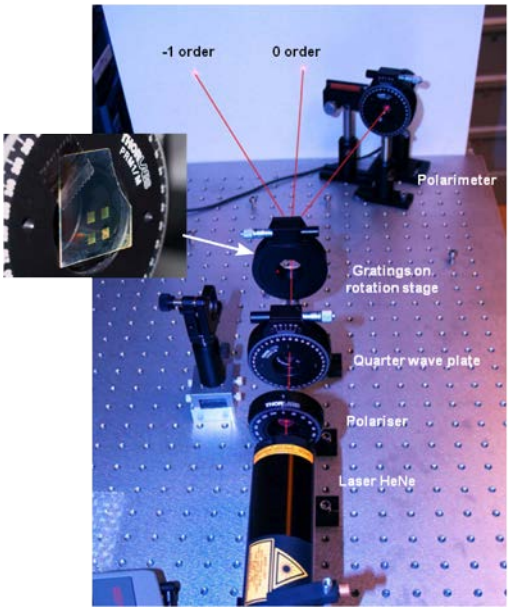


Figure 4.24 Optical setup for tests of gratings.

Table 4.5 Optically measured results for the gratings made in fused silica for λ=632nm.

Diffraction order	-2	-1	0	1	2
Efficiency	5.6%	**37.7%**	**0.6%**	**38.6%**	5.5%
Ellipticity	3.9	**1.12**	>20	**1.14**	7.2

For the fabrication of gratings for λ=894.1nm, silicon nitride instead of fused silica was selected because of high depth in fused silica. Further to simplify the fabrication process, ZEP resist was used instead of PMMA. Indeed, ZEP resist selectivity is high enough to use it as a mask for RIE etching of silicon nitride so that lift-off step can be avoided.

4.4.1.1 Gratings in Silicon nitride

E-beam optimization has been repeated for ZEP and for gratings parameters corresponding to λ=894nm. The process flow is shown in Figure 4.25. A 470nm-thick layer of Si_3N_4 was deposited by PECVD onto the glass wafer. After cleaning the wafer with acetone, ethanol and oxygen plasma, 325 nm resist (ZEP) was spin-coated (3000rpm) and then prebaked at 180°C for 2 mins before to be kept at room temperature for 4 hours. Chrome (10nm) was sputtered on the resist (to avoid charging) and sample exposed by e-

beam. Optimized e-beam parameters for the use of ZEP were set at 25kV, 10μm aperture, and 7mm working distance with the energy doses of 0.60 μC/cm^2 keeping the nominal doses 100 μC/cm^2. After the completion of exposure, chrome layer was removed and resist was developed in the Amlyacetate ($C_7H_{14}O_2$) for 2 mins and inserted in the stopper (MIBK: IPA, 30s) to stop the reaction. Sample was baked at 120°C for 3 mins in order to harden the resist used as mask for etching. Silicon nitride was then etched by RIE during 8mins at a rate of 60nm/min so that only 470nm Si_3N_4 stripes remained.. Finally, ZEP resist was removed from the sample by using remover (1165). As previously, geometry of fabricated gratings was observed with SEM. SEM images of fabricated gratings for λ=894nm are shown in the Figure 4.26 and parameters are summarized in the Table 4.6.

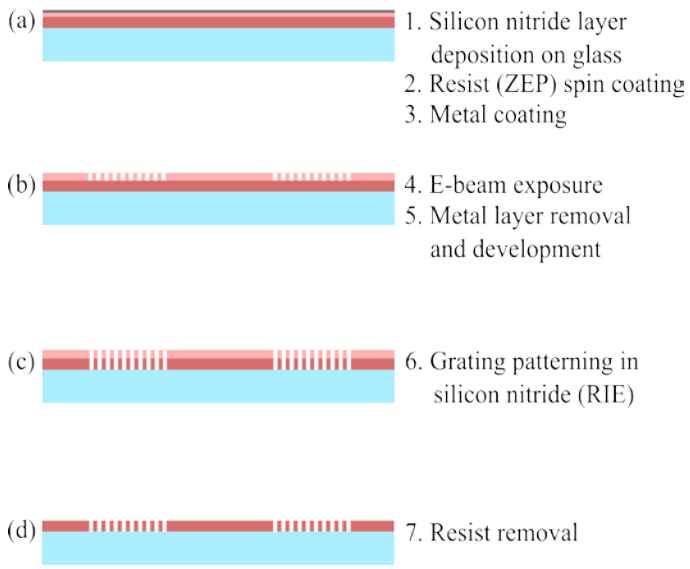


Figure 4.25 Fabrication process for the gratings in silicon nitride.

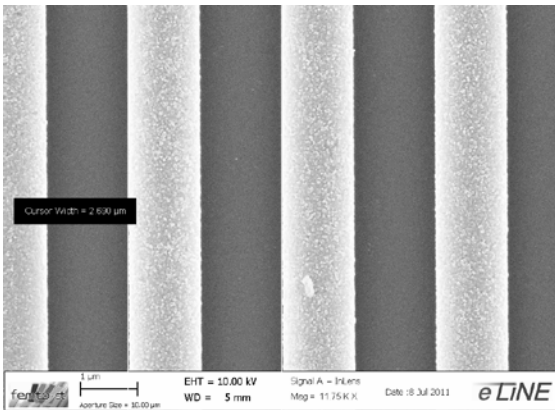


Figure 4.26 SEM images of the gratings fabricated for λ=894nm in silicon nitride.

Table 4.6 SEM results of fabricated gratings in silicon nitride for λ=894.1nm.

Grating parameters	Target	measured
Line width	1236±35nm	1244nm
Thickness	470±14nm	458nm
period	2698nm	2690nm

Following this fabrication procedure, gratings for the R-cell were fabricated at the wafer level and integrated on the R-cell cavity.

4.5 Integration of R- cells

For characterization, a first wafer stack including different sizes of R-cell was fabricated (cavity length = 3, 5, 7 and 9mm). For assembly of gratings with correct alignment compared to optical cavity and apertures, UV-curing bonding with material having matching refractive index with glass wafers was performed. A setup, allowing alignment of the two wafers (R-cell sealed cavities and gratings wafer) according to alignment marks, was installed (Figure 4.27). It allows, after deposition of UV-curable material, to align the two wafers while maintaining them in correct position during full UV-curing.

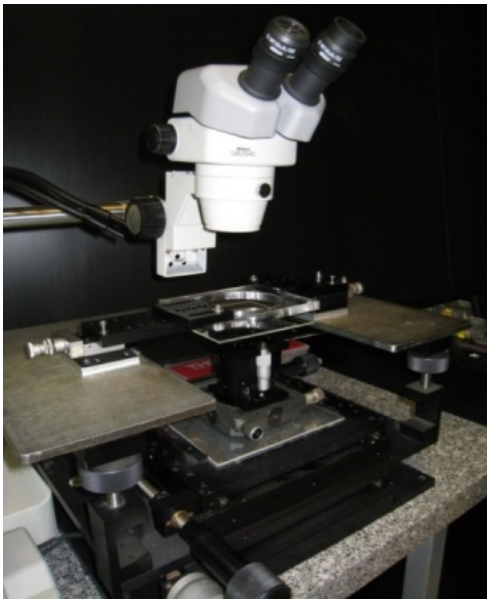


Figure 4.27 Wafer aligner system for UV-bonding of R-cell cavities and gratings wafer.

The obtained stack was then diced into individual R-cells. As it can be seen on Figure 4.28, the obtained R-cells are made of a stack of silicon glass layers where the apertures are embedded and where the gratings are located on the top. On the Figure, the dispenser cavity is clearly visible along with channels connecting it to the optical cavity (hidden behind the aperture).

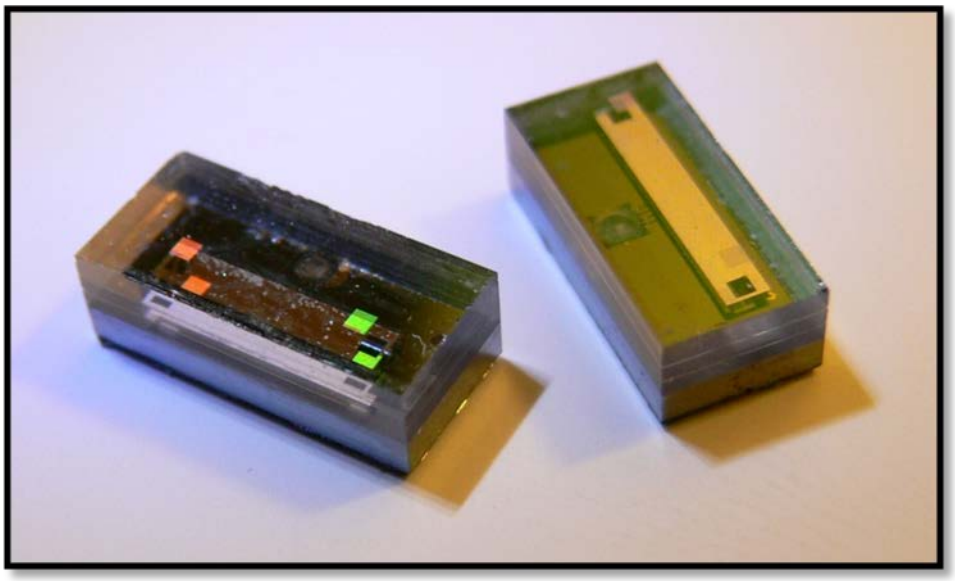


Figure 4.28 Fabricated R-cells (left: 7mm long optical cavity; right: 9mm long optical cavity).

4.6 R-cell characterization

In order to characterize the first round of R-cells, a dedicated bench was prepared, based on a coated prism that allow injection and collection of the probe beam into the R-cell. The probe beam is generated by a DFB (distributed feedback) laser working on the D_1 line of Cs and modulated by an electro-optical modulator (EOM) (Figure 4.29). The R-cell is located into a package made of POM (Polyoxymethylene) that includes coils for static magnetic field generation (to break the Zeeman degeneracy) and heaters and thermal sensors located right under the cell in contact with silicon (Figure 4.30).

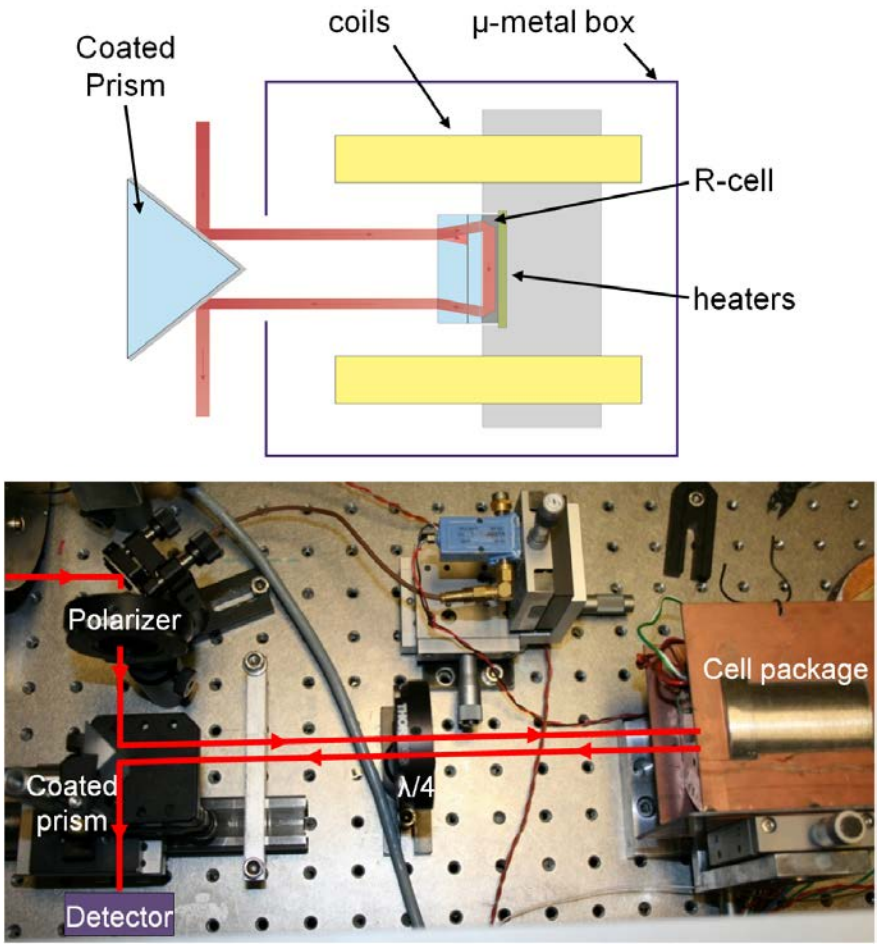


Figure 4.29 Setup for characterization of R-cells.

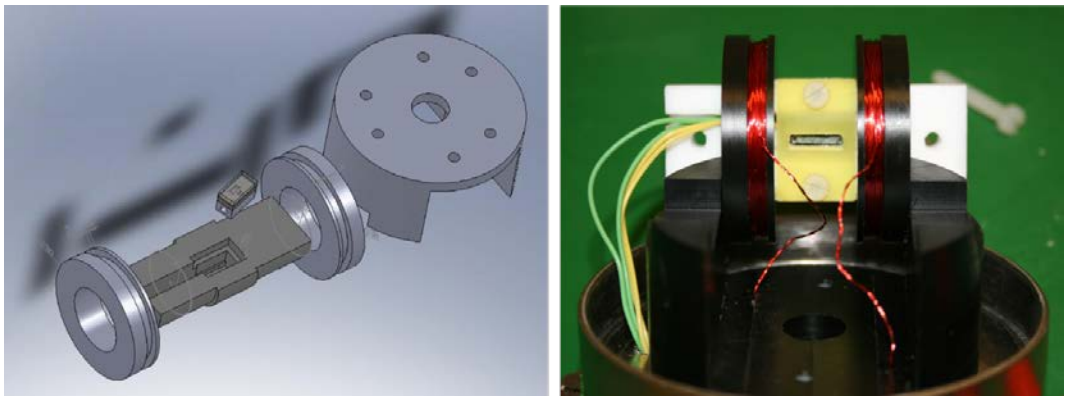


Figure 4.30 R-cell package for characterization.

Two different R-cells were activated and tested, namely the 7mm long cavity (Rcell 1) and 5mm long cavity (Rcell 2). CPT resonances were observed (Figure 4.31) and demonstrated the correct behaviour of gratings, apertures and reflectors; in other words, validated the principle of this new architecture of cells

for atomic clock application. However, and as it was mentionned earlier, those characterizations showed that no buffer gas was contained inside the cells. A problem on the anodic bonding system, not discovered at the time of cell filling and sealing, was identified and is now solved. Nevertheless, such R-cells can be compared to pure Cs T-cells.

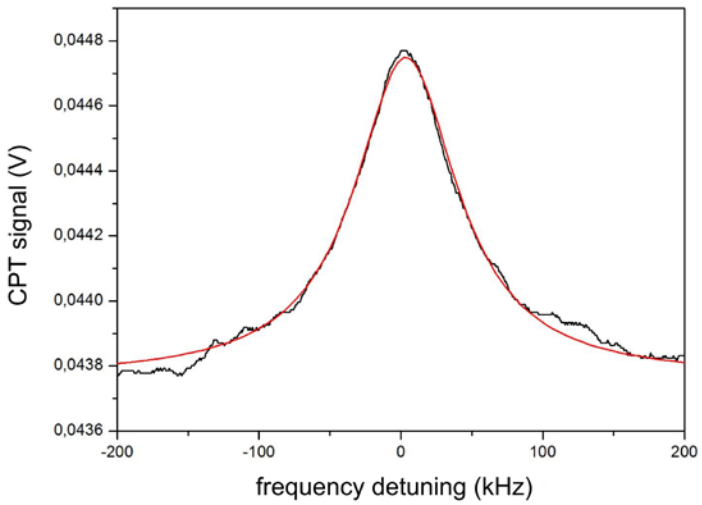


Figure 4.31 CPT signal measured from an R-cell.

From Figure 4.31, the CPT signal linewidth (FWHM) is slighlty lower than 50kHz. As a comparison, in pure Cs T-cells, typical CPT resonance linewdith are in the order of 250kHz, i.e. 5 times larger. In addition, according to the Figure 4.32 showing the CPT resonance linewidth as a function of the optical power for the 2 R-cells tested, the linewidth is clearly length-dependent, i.e., the longer cavity or the longer atom/light interaction, the thinner linewidth. The minimum linewidth of 45kHz achieved in a cell without buffer gas has never been observed in the various T-cells tested although the beam diameter, and so the cell diameter, is 3 times larger in T-cells than R-cells. Moreover, the CPT signal magnitude is also much better for the longer cell, as it can be seen in the Figure 4.33. Such results demonstrate a real potential for R-cell architecture. The next round of R-cells including buffer gas is, during the writing of this manuscript, under fabrication, for which an improvement factor of 5 to 10 compared to T-cells can be expected.

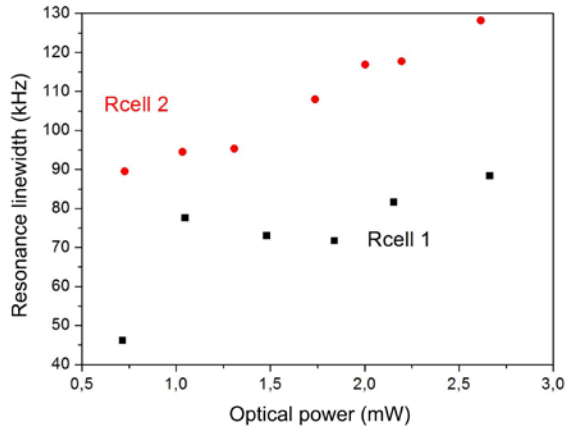


Figure 4.32 CPT resonance linewidth of the 2 tested R-cells as a function of the optical power incident onto the gratings.

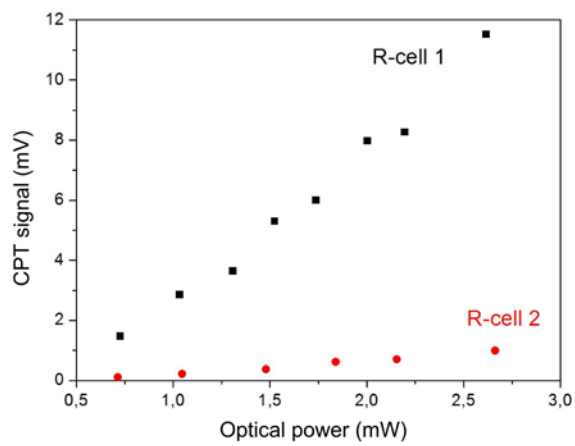


Figure 4.33 CPT signal of the 2 tested R-cells as a function of the optical power incident onto the gratings.

4.7 Conclusion

The chapter 4 presents a new architecture of vapor cells which is called Reflective cell. The basic principle is to use different routing of probing light, thanks to micro-optical components and reflectors embedded inside the cell, to provide a longer atom/light interaction. Complete fabrication and development of such architecture is then presented, with cavity wet etching optimization, dedicated diffractive optical element development and assembly of stack. The results of first measurements demonstrate the high potential of the R-cell to reduce significantly the linewidth of the CPT signal, and as a consequence to improve the stability of an R-cell based atomic clock. More experiments are now required with cells containing buffer gas, cells having different optical cavity lengths and diameters, to

find the best tradeoff between interaction length and CPT signal amplitude. From the first results, an improvement factor of 5 to 10 can be expected compared to T-cell architecture. In addition, the R-cell architecture could provide a better thermal control (thanks to the access to the silicon bottom side of the cell) and a better compactness (source and detector located on the same side, smaller beam diameter requiring less cumbersome beam shaping system). Finally, such architecture would be more adapted to mass production by integrating all the optical components at a wafer level and by requiring less individual alignments.

Conclusion and perspectives

Atomic clocks provide enhanced accuracy, stability, and timing precision compared to quartz-based technologies. However, the size and power consumption of existing atomic clocks far exceeds those of quartz-based clocks, preventing until now their deployment in portable or embedded applications. Atomic frequency references provide high-precision stable signals over long integration times because their frequency is determined by an atomic transition and would provide huge benefits in a wide number of applications. Recently, huge efforts have been led by several US teams to develop chip scale atomic clocks (CSAC) exhibiting typical fractional frequency stability of $2x10^{-10}$ and 10^{-11} at 1s and 1 hour integration time respectively, a power consumption of about 150 mW and a volume of a few cm^3. CSAC technology presents a lot of advantages compared to currently-used quartz crystal oscillators. Among them, micromachined vapor cell frequency references are batch fabricated by use of MEMS technologies, authorizing a very small physics package matching the requirements of low power consumption. Since the first demonstration of a MEMS-based physics package, significant advances in power dissipation, performances and integration with electronics have been made. To push the development of reduced atomic clocks, the US Defence Agency DARPA awarded in 2000 by $15 million the National Institute of Standards and Technology and the University of Colorado at Boulder. In 2005, Symmetricom, teamed with the Charles Stark Draper Laboratory in Cambridge and Sandia National Laboratories in Albuquerque, received $3.4 million funding from the same DARPA program. Both consortia developed CPT-based atomic clocks using MEMS fabrication techniques. In 2011, DARPA program continues, also supporting the implementation of chip-scale atomic magnetometers (CSAM). As a consequence of these efforts, CSACs starts to be a commercially available product, and its mass production will begin soon. CSAC technology have many potential applications such as wireless communications, GPS receivers, high-sensitivity magnetic sensors, etc.. As atomic clocks get smaller and cheaper and use less power, they could replace quartz crystal oscillators in many common products such as computers, offering several orders of magnitude better time keeping. In surveillance applications, chip-scale atomic clocks can be used to improve resolution in Doppler radars and to enhance accuracy of location identification of radio emitters.

Strong perspectives of evident market potentialities of miniature atomic standards motivated the recent work done at FEMTO-ST. We considered that it is crucial to promote a European version of CSAC technology, having a great potential in a wide number of telecom applications. We started to implement this new version of the atomic Cs clock in the frame of the collaborative project MAC-TFC (http://www.mac-tfc.eu/), Here, component-level functionality of the three subsystems of a complete

CSAC is reached: the physics package, the local oscillator and the control electronics. The volume of the clock is smaller than 10 cm^3, the short-term frequency instability is around $1.5x10^{-10}$ at 1s (about 100 times better than current crystal oscillators) while the total power consumption is about 155 mW at 25°C (about 100 times smaller than the smallest commercial clock technology). Many physics and fabrication issues have already been addressed and we see a clear path towards our miniature atomic clock with expected frequency stability of $10^{-11}/\sqrt{\tau}$ and the potential for commercialization in a few years. The aim of this PhD thesis is to partially contribute to this ambitious program with the optimization of the technology steps of Cs vapor miniature cells. During the last 3 years, we obtained several highlights in the realization and characterization of FEMTO-ST vapor cells. We pointed out the cancellation of the Cs clock frequency temperature-dependence in Ne buffer gas around 80°C. In this single buffer gas configuration, the inversion temperature does not depend on the buffer gas pressure. We then proposed the development of simple architecture CSACs operating with a unique buffer gas microcell with strongly relaxed constraints on the buffer gas pressure control. It has been demonstrated that linewidths of a few kHz can be achieved in our Ne microcells proving that they are excellent candidates for CSAC applications. A frequency stability of 1.5 10^{-10} at 1 s has been demonstrated with VCSEL working on the D_2 line of Cs. Recent accelerated aging tests demonstrated that FEMTO-ST microcells exhibit a lifetime higher than 3 years without any significant change of the cell inner atmosphere. This should allow an excellent long-term frequency stability of the CSAC. We also led extensive studies on the temperature dependence of the Cs clock frequency in microcells filled with a Ne/Ar mixture.

In the frame of this thesis, we focused firstly on the development of two cell architectures: the transmissive cell (T-cell, Chapter 2) and the reflective cell (R-cell, Chapter 4). Secondly, our role was to perform the thermal simulations for the thermal management of fully LTCC-packaged Cs vapor T-cell (see Chapter 3).

To improve the quality of CPT signal of the T-cells, content as well as quality of its internal atmosphere need to be well controlled. For this purpose, some technology improvements are necessary: first, smoothing of internal T-cell sidewalls in order to reduce the effect of Cs atom relaxation at each reflection on cell surfaces and secondly, realization of an excellent quality of cell sealing avoiding any kind of leak. In particular, several DRIE process parameters and pattern design have been optimized to have sufficiently smooth sidewalls of cell. In addition to the DRIE, anodic bonding process was developed to seal the silicon cavities under buffer gas atmosphere. Finally, original anodic bonding process was proposed to fabricate the microcells filled with Ar or Ne at required pressures. Taking into account that the applicable bonding voltage is significantly limited by the electrical breakdown of the gas, this process

is actually a two-step bonding procedure which allows to achieve a strong and high-quality reliable sealing. In this method the cell is pre-sealed by anodic bonding in presence of the buffer gas atmosphere at a voltage lower than the breakdown voltage, followed by the complete sealing of the cell by the additional bonding performed in air at high voltages. Thermal aging tests revealed that the microcells exhibit an excellent long-term thermal resistance (500 hours at 115°C and 3 months at 105°C). Metrology of the microcells performed by linear optical spectroscopy demonstrates that the actual buffer gas pressure in the microcell after its complete sealing corresponds well to the expected one within the uncertainty of the measurements. All these features may enable the integration of miniature cells into portable atomic frequency references and chip scale atomic magnetometers.

A study of the thermal behaviour of Cs-vapor cell packaged in a Low Temperature Co-fired Ceramics (LTCC) structure for chip-scale atomic clock application has been presented in Chapter 3. Different contributions to the thermal behaviour, such as bulk conduction, gaseous conduction and convection, and radiation, have been investigated by analytical modelling or finite element based softwares and several solutions have been proposed in order to keep the cell temperature constant during ambient temperature variations. Thanks to LTCC suspensions made of bridges, vacuum environment, and metallic coatings, it has been shown that reasonable power consumption, in the range of several tens of milliwatts, can be achieved for thermal control of the Cs-cell at an operating temperature of 80°C. In addition, thermal gradients inside the cell have been studied and it was shown that they can be limited to few millikelvins with appropriate coatings limiting radiations. Dependence of these gradients to the ambient temperature variations can moreover be significantly reduced by a dynamic adjustment of the set temperature.

An important and novelty aspect of this thesis concerns the development of R-type cell which is based on the reflection of the laser light beam inside the silicon based cavity with help of diffractive components. Here, the high quality surface of <111> angled inner sidewalls, wet etched (KOH) through a <100> silicon wafer, is used as optical reflectors. However, their orientation is inclined at 54.74 degrees and the incident beam would consequently suffer one (or more) additional reflection(s) at the bottom of the cavity, resulting in a strong deterioration of optical incident polarization state. Indeed, polarization state of the beam has to be circular in order to pump and saturate the correct Cs sublevels, and to produce a good CPT signal. Thus, we have proposed to incorporate diffractive microoptical components to avoid the reflection and the polarization state deterioration of the probing laser beam. The basic principle is to use different routing of probing light, thanks to micro-optical components and reflectors embedded inside the cell, in order to provide a longer atom/light interaction. Complete fabrication and development of such architecture is then presented, with cavity wet-etching optimization, dedicated diffractive optical element

development and assembly of complete stack. The results of first measurements demonstrate the high potential of the R-cell to reduce significantly the linewidth of the CPT signal, and as a consequence to improve the stability of R-cell based atomic clocks. More experiments are now required with cells containing buffer gas, cells having different optical cavity lengths and diameters, in order to find the best tradeoff between interaction length and CPT signal amplitude. From the first results, an improvement factor of 5 to 10 can be expected for optimized R-cell architecture compared to T-cell architecture. In addition, the R-cell architecture could provide a better thermal control (thanks to the access to the silicon bottom side of the cell) and a better compactness (source and detector located on the same side, smaller beam diameter requiring less cumbersome beam-shaping system). Finally, such architecture would be more adapted to mass production by integrating all the optical components at wafer level and by requiring less individual alignments.

To date, there are several consequences of research results reported by this doctoral manuscript.

First, an ANR proposal was accepted which will start officially on the 1st of December 2011. This project called "INNOVATIVE SOLUTIONS FOR IMPROVED MINIATURE ATOMIC CLOCKS" (ISIMAC) brings together a consortium made of two academic institutions (FEMTO-ST and SYRTE) with the goal to optimize the technology steps of Cs vapor miniature cells, focusing on R-cell with antirelaxation wall coating layers and/or buffer gas and having the objective to develop an original modulated laser scheme to enhance the clock performances. The R-cell will be sealed by reliable low temperature bonding techniques, non-invasive for the integrity of the wall coating. R-cell architecture aims to improve the thermal management and to decrease the power consumption as well as to increase the atom-light interaction time and consequently the clock frequency stability. ISIMAC will include all fundamental aspect of work which cannot be included in a STREP project such as MAC-TFC. Our ultime objective is to provide an European Premiere for miniature atomic clocks underscoring the primary physics, metrology tools and engineering challenges facing microsystems development.

Second, the industrial development is also envisaged with our Partner from MAC-TFC proposal, Oscilloquartz SA. Oscilloquartz objective is to use MAC-TFC technology in future development of 4G (4th generation) mobile services. Such services will need local frequency clocks with a typical deviation of 1µs per week in base stations. Crystal clocks currently used in mobile telecommunication systems reach their limits and cannot offer this stability level for such integration times. It seems that MAC-TFC technology is an ideal candidate for this 4G application.

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Appendix: Overview of micromachining technologies used in the development of MEMS atomic clocks

The development of MEMS technologies permits to push the miniaturization of atomic clock cell, making the fabrication simpler and increasing the potentiality for mass production. During the last few years, considerable work has been done by different US groups awarded by DARPA Chip Scale Atomic Clock (CSAC) program [Liew 2004, Lutwak 2004].

The principle of proposed miniature clocks is based on Coherent Population Trapping (CPT), obtained in an extremely compact sealed vacuum cell of few cubic millimeters. These cells contain alkali vapors and are illuminated by a high-frequency modulated laser beam. The frequency stability of such atomic clocks is based on transitions between the well-defined ground state hyperfine levels of alkali atoms such as cesium (Cs) or rubidium (Rb). In this solution, conversely to classical rubidium vapor cell clocks, the CPT frequency standard does not require a microwave cavity to probe the atomic resonance. This permits the very compact physical package of the micro-clock.

Our solution for the transmissive cells as well as the solution developed by US teams is commonly based on the fabrication of alkali cells formed by sandwiching an etched silicon wafer between two glass wafers. Most of the existing MEMS microcells are fabricated by the use of conventional microfabrication technologies including photolithography, dry etching [Douahi 2007, Nieradko 2008] or wet etching [Knappe 2004, Knappe 2005] of cavities in a Si wafer, and subsequent anodic bonding of thin glass wafers on both surfaces of the Si wafer.

In this part, we describe the main micromachining processes, necessary for our microcell fabrication. However, we focus our investigation on the operation of anodic bonding which is applied to seal the cells filled with a well-controlled pressure of buffer gas. In particular, when the anodic bonding is performed in the atmosphere of Ar or Ne, the process may be disturbed by the electrical breakdown caused by the gas

ionization, as like the case of the anodic bonding in N_2 atmosphere [Blasquez 2002]. Consequently, the bonding procedure is well optimized in order to maintain the long-term reliability of sealing and presented in the chapter 2.

In the next sections, we will introduce a general overview of micro fabrication processes used in fabrication of Cs vapor cell including the lithography techniques (both optical lithography and e-beam lithography), dry etching and wet etching of silicon, and our key technology: the anodic bonding of glass to the silicon.

A.1 Lithography techniques

In micro fabrication, Lithography is a process to transfer desired pattern to the substrate either silicon or glass by selectively removing the thin film. In this process, photosensitive material (photo resist) is exposed by the radiation with the intermediate mask which helps for selective exposure of photoresist (PR) on the substrate. Depending on the feature size needs to transfer to substrate, there are two kind of lithography are in use at various research labs and industries. First one is optical lithography with which pattern up-to few micron feature size can be transfer to the substrate and second one is E-beam lithography, with which it is possible to transfer feature down to the nanometer scale. Both methods are described in the following sections.

A.1.1. Photolithography (or optical lithography)

This is the mostly and often used technique of lithography in micro fabrication [Madou 1997] to selectively remove parts of a thin film or the bulk of a substrate. Figure A.1 depicts the lithographic process sequence.

Here, ultraviolet (UV) light is used to transfer geometrical pattern from the photo-mask to the sensitive polymeric material called resist (PR). The PR is applied as a thin coating, typically by spin coating over the substrate and then heated to remove the casting solvent. The PR film is subsequently exposed through a photo-mask and then developed by immersion in a developer solvent. As a result of radiation exposure, resist properties changes rending the resist film more soluble in the developer, thereby producing a positive-tone image of the mask or less soluble upon exposure resulting in generation of a negative-tone image. When the resist image is transferred into the substrate by etching and related processes, the resist film that is remains after the development, functions as a protective mask. The resist film must "resist" the etchant and protect the underlying substrate while the bared areas are being etched. The remaining resist film is finally stripped, leaving an image of the desired pattern in the substrate. The process is repeated

many times to fabricate complex semiconductor devices.

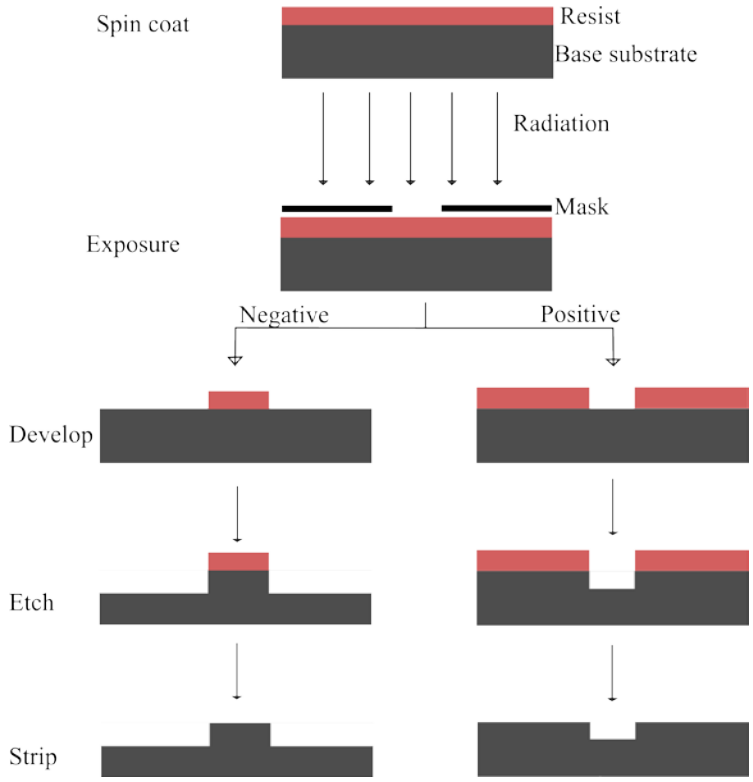

Figure A.1 Schematic representation of the lithographic process.

Photolithography is used in micro fabrication of MEMS because it affords exact control over the shape and size of generated objects and it can create patterns simultaneously over an entire surface of the wafer. But its main disadvantages are that it requires a flat substrate to start with, also it is not very effective at creating shapes those are not flat, and it can require ultra clean operating conditions. Before going for the UV exposure of PR resist, lets us start with general properties of PR. PR consists of three components [Pasquale]: a base material (resin), a photoactive compound (PAC) and a solvent (Figure A.2).

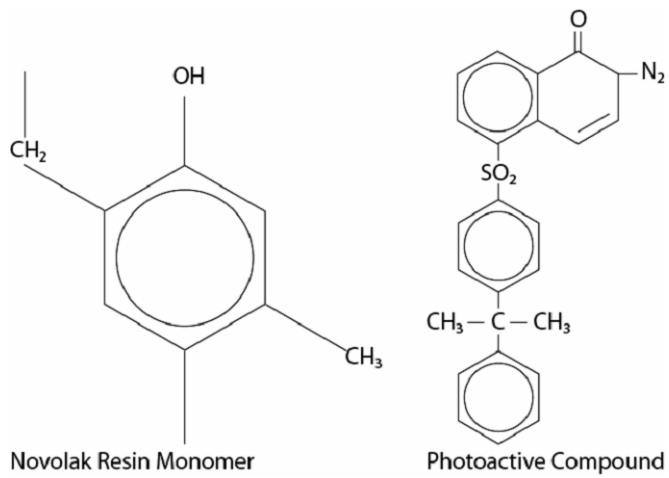

Figure A.2 Chemical components in PR.

The solvent role is to control the mechanical properties of PR, making it less or more liquid, and also controlling its viscosity. On the other hand, PAC is inhibiting the PR dissolution in the developer before the UV exposure. Controversially, it makes PR highly soluble after exposure the UV exposure. Before the spin coating of PR on the substrate, this last need to be cleaned making it free from dirt or residual particles of resist. Wafers are usually cleaned by chemical solution containing hydrogen peroxide like piranha or RCA in order to remove organic or inorganic contaminants from the wafer. Dehydration baking is also necessary to ensure that any particles of water molecules on the wafer evaporate out. This is especially important for samples that can be oxidized easily (such as Silicon) and the oxides then bond to the water vapor in the air. Because of this, during the PR coating, PR will adhere to the water molecule rather than to the silicon substrate.

After the Dehydration of substrate, it is recommended to first spin coat them with thin layer of hexamethyldisilazane (HMDS) primer which will ensure the strong adhesion of PR with substrate due to the bonding of HMDS with oxide groups. Sample should not be coated with the excess amount of HMDS that can reduce the photosensitivity of PR.

Spin coating produces a constant thickness of PR across the sample. The thickness of the PR (T_{PR}) after spin coating has a proportional relationship to the speed (in RPM) of the spin coater (Equation A.1).

$$T_{PR} = \frac{1}{\sqrt{Speed}} \qquad \text{(A.1)}$$

Spin rate can be fixed from 1000 to 8000 rpm depending on which thickness of resist needs to be deposited on the wafer. At such speeds resist spreads from the center to edges of wafer by means of centrifugal forces. After successful coating of resist, wafer needs to be baked before lithography so called prebaking, to remove any excess of solvent remaining in the PR and reduce the stress inside the resist in

order to increase adhesion of resist layer to the wafer. Temperature and time for this prebaking varies from resist to resist.

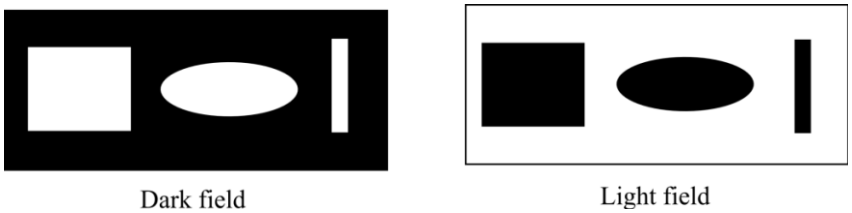

Figure A.3 Dark field and light field masks.

After the prebaking of PR coated wafer, it is then ready to be exposed to UV light through the photo mask which is a glass plate (transparent, white) with patterns (opaque, black). The pattern transfer is made when photo mask is placed in contact with resist coated wafer and exposed with UV to transfer the dark field or light field (Figure A.3) images from the mask to the resist. Only the clear region of photo mask is free to light transfer.

There are three main techniques of exposure shown in Figure A.4: (i) contact method which can damage the surfaces of both the mask and the wafer [Gatech, Wright 2009]; (ii) proximity method in which wafer is at few tens of micron away from the wafer; and (iii) projection printing in which mask is imaged by a high resolution optical system onto the resist coated wafer.

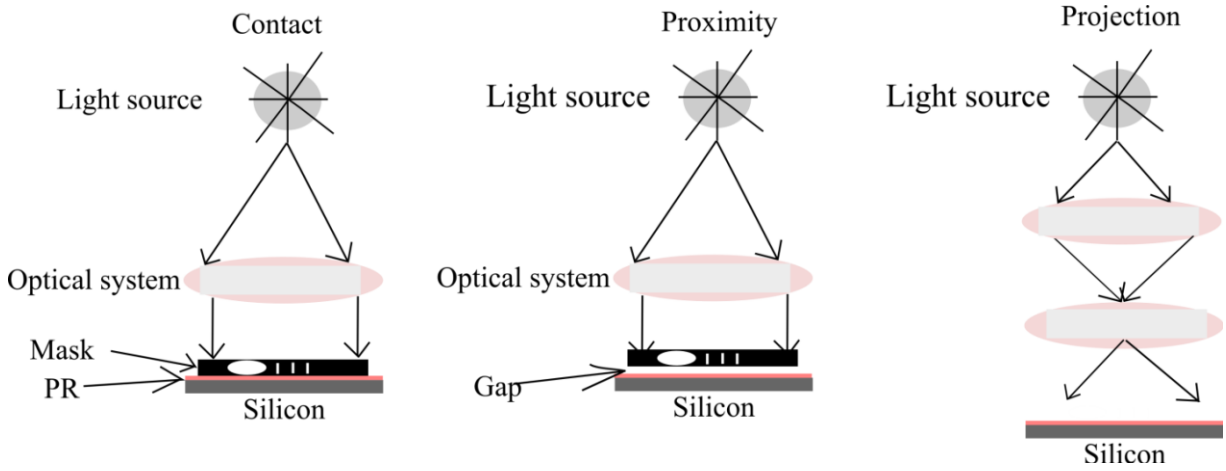

Figure A.4 Different exposure methods.

In the photolithography, UV lamps are used operating in the deep ultraviolet (DUV) region (150-300nm) or in UV region (350-500nm). The incident light intensity (in W/cm2) multiplied by the exposure time (in seconds) gives the incident energy *(J/cm2)* or dose, D, across the surface of the resist film. Radiation induces a chemical reaction in the exposed areas of the photo resist, altering the solubility of the resist in a solvent either directly or indirectly via a sensitizer. One can use either constant dose which can be calculated from lamp intensity or constant time that depends on the resist and should be characterized for

each resist. After exposure, exposed positive resist becomes soluble in the developer (organic solution) while the exposed negative resist stays insoluble. Post-exposure treatment is often desired, because the reactions initiated during exposure might not have run to completion.

In certain cases, post-exposure baking is performed by heating the exposed wafer from few seconds to few minute followed by developing the resist. Further after development, another heat treatment is needed, called hard baking. This helps to remove residual developer and to anneal the resist film enhancing the interfacial adhesion of resist with wafer which could be weakened by developer penetration through resist to substrate/resist interface or by swelling of resist (negative resist case). Hard baking further increases the hardness of resist which help in subsequent technological steps like wet and dry etching of resist. Also such heating treatment should optimized for each resist in terms of temperature and heating time as excessive heating can degrades the wall profile angle or it could make difficult to remove the resist layer.

Once lithography is successfully finished, one can go for further technology steps like etching of substrate or deposition of any devices layer followed by lift-off process and then after photo resist must be removed from the substrate by using a resist stripper or with oxygen plasma when there is no longer need of resist over the wafer.

A.1.2. E-beam lithography

In comparison to optical lithography where UV light is used for image transfer, in Electron beam lithography (abbreviated as e-beam lithography), a beam of electrons, operating at the wavelength range of pico-meters expose the surface covered with the resist. Such small wavelength can help to pattern the image on the substrate in the range of nanometer.

E-beam lithography systems can be classified according to both beam shape and beam deflection category. Older systems used Gaussian-shaped beams and scanned these beams in a raster fashion. The recent advanced E-beam lithography systems use shaped beams which may be deflected to various positions in the writing field. One of main advantages of E-beam lithography is to beat the diffraction limit of light, making thus possible to write nanometer-scale structures. This permits a wide range of applications in low-volume manufacturing of semiconductor components and research &development.

However, the key limitations of E-beam lithography are the high cost of commercially available systems as well as the very long time of exposure of an entire wafer. For research applications, it is common to convert an electron microscope available in laboratory into and less expensive E-beam writing systems using relatively low cost accessories. The long exposure makes it vulnerable to beam drift or instability which may occur during the exposure, limiting the potential of commercial applications. Despite the high

resolution of E-beam lithography, this technique is generating several categories of defects which will be discussed latter (energy dose variation, stitching errors, etc…).

The first step of E-beam lithography is to create a photomask by spin coating the resist onto the substrate like silicon or glass. After spin coating, the sample is loaded inside of E-beam chamber where it will be exposed under vacuum by the beam of electrons generated using a scanning electron microscope (SEM). In SEM, electrons are accelerated through an aperture down to the column in order to interact with sample. The beam of electrons is focused through a lens system where the beam shape is guided through the length of the column and focusing is done at the end of column. When a positive resist is exposed by an electron beam, some molecular chains in the resist molecules will break. This is accompanied by an increase in solubility and increases the etch rate. Following the exposure of resist, during the sample development, broken polymer chain gets dissolved in chemical (developer) and leaves behind the pattern on the sample. Quality of pattern transferred to the sample depends on the several factors: good control of the area on the sample to be exposed, well focus on the surface, pre-adjusted magnification, beam current, beam astigmation, writing field alignment, energy doses.

Although the parameters described above needs to be fixed before exposure to produce a good quality image on the sample, the resolution of transferred image in E-beam lithography depends on the category of electron sources used. Two types of electron sources are currently used. Thermionic sources formed from LaB_6 are employed, producing lower resolutions. Systems with higher resolutions need to use electron emission sources such as heated W/ZrO_2. Thermal field emission sources are preferred over the cold emission sources because they offer better stability over longer exposure of several hours. To focus the E-beam, a system of electrostatic and magnetic lenses may be used. Moreover, to get very fine focal point of E-beam, one needs to obtain a very narrow dispersion of e-beam energy. Typically, electrostatic deflection lenses are used for small beam deflection while electromagnetic scanning is employed for larger beams deflections. Before exposing the resist, write field must be align accurately to avoid the stitching in the pattern. Because of the inaccuracy and because of the finite number of steps in the exposure matrix the writing field is of the order from 100 µm to 1 mm. Larger patterns require stage moves. An accurate stage is critical for stitching (tiling writing fields exactly against each other) and pattern overlay (aligning a pattern to a previously made one).

The minimum time to expose a given area and dose is calculated by the formula [Parker 2000];

$$D.A = T.I \qquad \text{(A.2)}$$

Where D is dose and A is area need to expose whereas T is time of exposure and I is beam current.

This minimum write time is not the real time necessary for exposure because not including the time for the stage to move back and forth, write field alignment procedure, beam correction, dose adjustment, and current measurement, etc. It is clear that throughput is a serious limitation for E-beam lithography, especially when writing dense patterns over a large area.

Defects produced by E-beam lithography can be divided in two categories: data-related defects, and physical defects.

Data-related defects can be produced when beam deflection errors occurs or can appear when beam shaping errors occur. These errors can originate either from the electron optical control hardware or the input data that was taped out.

On the other hand, physical defects can include sample charging, backscattering errors, write field alignment, contamination, dose errors, beam instability, out-gassing or contaminations, etc.

It is possible to eliminate these defects by appropriate control of E-beam station and proper adjustment of various factors relating to exposure like dose, beam current, accurate write field alignments and also resist and substrate processing avoid charging effects. Another problem related to physical defect is charging of substrate by means of high electron energy unless these electrons don’t get quick path to ground. In case of substrate like silicon, these electrons get grounded as soon as they arrived to silicon surface but in case of glass substrate grounding electrons takes much time and can damaged the resist very effectively. Such charging problem can be avoided by depositing thin metal layer either over resist or under resist.

A.2. Etching Process

In order to form a functional MEMS structure on a silicon substrate, it is necessary to etch the thin films previously deposited and/or the substrate itself. In general, there are two classes of etching processes:

1. Dry etching where the material is sputtered or dissolved using reactive ions or a vapor phase etchant
2. Wet etching where the material is dissolved when immersed in a chemical solution

In the following, the most used technologies for wet and dry etching are discussed briefly.

A.2.1. Wet etching

Wet etching involves the use of liquid etchants. The wafers are usually immersed in the etchant solution and the exposed material is etched mostly by chemical processed. Wet etching of silicon has been utilized since 1960 for applications requiring orientation dependent etch including micro machined sensors and chemical analysis systems. Silicon exhibits anisotropic etching in certain chemicals. Anisotropic etchings in contrast to isotropic etching means different etch rates in different crystallography directions of silicon. The classic example of this is the (111) crystal plane sidewalls that appear when etching a hole in a (100) silicon wafer in a chemical such as potassium hydroxide (KOH). The result is a pyramid shaped hole instead of a hole with rounded sidewalls with a isotropic etchant. It is due to the fact that (111) crystalline plane of silicon is etched slower than other silicon plane during anisotropic wet etching and can be utilized to minimize the undercut during deep etching of substrate to realize the deep structure. Silicon has diamond like structure shown in Figure A.5.

In the most of micro fabrication processes, mostly used three different orientations of silicon explained by means of Miller index are 100, 110 and 111. These three different oriented plane of silicon has different etch rate. In Figure A.6 these different planes are described in term of dangling bond and surface bond. The bonds belong to the atoms at the surface are called dangling bonds. 111 surfaces have only one dangling bond and 100 have two whereas 110 has one dangling bond and two surface atoms. Lesser the dangling bonds and surface atoms, slower is the etch rate. This is why 111 is much slower etch rate in comparison to other two planes [Mizuhata 2008].

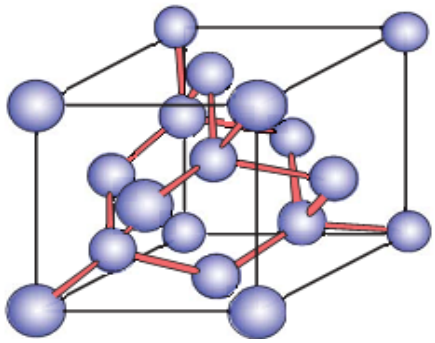

Figure A.5 Diamond like structure of silicon single crystal in which silicon is covalently bonded to four other atoms.

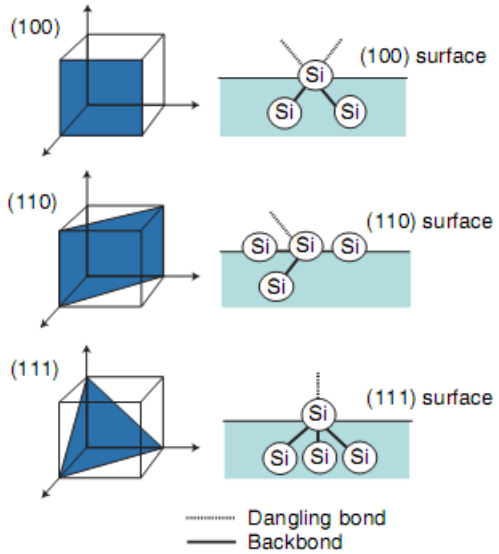

Figure A.6 Silicon 100, 110 and 111 oriented surfaces has dangling and back bond [Mizuhata 2008].

There are several etch solution which has been utilized to etch the silicon like KOH, TMAH, EDP, NaOH and CsOH. Each solution has its own advantage and disadvantages depending on the etch rate, selectivity and quality of etched profile. Anisotropic etching of silicon using alkaline solutions has been described to study the etch rate [Seidel 1990] as a function of temperature, crystal orientation and concentration.

Each of these solutions diluted with water and basic etching equation is described as;

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2$$

Silicon mainly reacts with water and OH^- and produces hydroxide ion and hydrogen bubbles. Examples of anisotropic etching are shown in Figure A.7.

The problem with substrate etching is that isotropic processes will cause undercutting of the mask layer by the same distance as the etch depth. Anisotropic processes allow the etching to stop on certain crystal planes in the substrate, but still results in a loss of space, since these planes cannot be vertical to the surface when etching holes or cavities. If this is a limitation for investigated application, we can consider dry etching of the substrate instead. However, the cost per wafer will be 1-2 orders of magnitude higher to perform the dry etching. If we making very small features in thin films (comparable to the film thickness), we may also encounter problems with isotropic wet etching, since the undercutting will be at least equal to the film thickness. With dry etching it is possible etch almost straight down without undercutting, which provides much higher resolution.

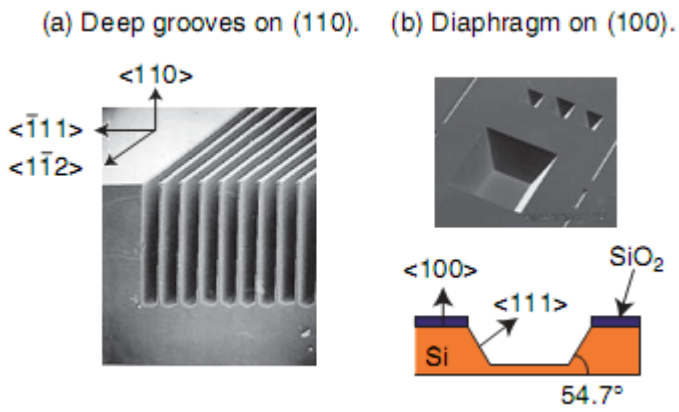

Figure A.7 Anisotropic etching of silicon (a) deep grooves in 110 silicon (b) diaphragm made in [100] silicon [Mizuhata 2008].

The problem with substrate etching is that isotropic processes will cause undercutting of the mask layer by the same distance as the etch depth. Anisotropic processes allow the etching to stop on certain crystal planes in the substrate, but still results in a loss of space, since these planes cannot be vertical to the surface when etching holes or cavities. If this is a limitation for investigated application, we can consider dry etching of the substrate instead. However, the cost per wafer will be 1-2 orders of magnitude higher to perform the dry etching. If we making very small features in thin films (comparable to the film thickness), we may also encounter problems with isotropic wet etching, since the undercutting will be at least equal to the film thickness. With dry etching it is possible etch almost straight down without undercutting, which provides much higher resolution.

A.2.1. Dry etching

Contrary to wet etching, that requires the immersion of the target in a gas, or more commonly in a liquid, dry etching consists in using plasma (partially ionized gases) to etch the target. The advantage of dry etching is to offer directional or anisotropic etching independent of the crystalline orientation of Silicon. As gases play the basic role in dry etching so it's important to understand its behavior. A gas is combination of free atoms or molecules. Atomic energy of gas is the form of translation kinetic energy of atoms and molecular energy in the form of rotation and vibrational energy states. There is a continuously exchange of energy between the constituents of gas by means of collision of molecules with each other as well as with container walls. In such case, Kinetic energy (K.E) of gas related to overall absolute temperature (Equation A.3).

$$\frac{1}{2}K.E = \frac{1}{\sqrt{2}}mv^2 = \frac{3}{2}kT \qquad \text{(A.3)}$$

Where m is mass of gas atom, v is the velocity of atom, k is Boltzmann's constant and T is absolute temperature. Gas pressure inside the container is simply total force of gas constituent on the side wall of container per unit area. According to ideal gas equation, pressure inside the chamber or container directly depends on its temperature. In case there are more than one gas is used inside the chamber for etching, pressure is sum of partial pressure of each gas. There are pressure units that used to define the pressure in such plasma process which are Torr, millibar (mbar) and Pascal (Pa). Relation between them is;

1Pa=7.5mTorr = 10^{-2}mbar

There are various pressure values or range has been defined for each plasma based process. At the high pressure greater than 10^{-2} Torr (1.33Pa), flow of the gas inside the chamber dominates by the collision between the gas constituent which is called viscous flow (laminar or turbulent). Once the pressure inside the chamber drops below the 10^{-2} Torr, gas flow turns to the molecular flow. Mean free path (MFP) of gas at this pressure becomes large and large until collision between the gas atoms become infrequent and more gas constituent starts to be adsorbed and desorbed by the chamber walls. MFP is the average distance travelled by the gas between two consecutive collisions between the walls of chamber which is between less than cm (viscous flow ultra low vacuum) to more than meter (ultra high vacuum). The directions of such motion are highly random that slow down the process of pumping. To increase the pumping process to get high vacuum inside the chamber, turbo pump are used in order to change the direction of atoms within its turbo rotor. Later helps to pump down the air from the chamber and in turn increases the vacuum condition to achieve the base pressure for required plasma process. Mostly plasma based dry etching needs the pressure between 10^{-4} to 10^{-7} Torr which comes under high vacuum range. Such range of vacuum based on the mean very path (MFP) of gas inside the etching chamber. To be in the range of high vacuum for Dry etching MFP of gas should be cm to meter leads to the molecular flow and can be achieved by using turbo pump. After achieving the base pressure for plasma process, selected gases for process are allowed to enter the chamber through mass flow controllers (MFC).

Here, three dry etching techniques are discussed: plasma etching, reactive ion etching (RIE) and deep reactive ion etching (DRIE).

A.2.2.1. Plasma etching

Plasma etching is a form of plasma processing involving a high-speed stream of glow discharge (plasma) of an appropriate gas mixture being shot at a sample. Here, plasma systems ionize a variety of source gases in a vacuum system by using RF (radio frequency) excitations which is generate by two electrodes situated inside the chamber. The target wafer is placed on an electrode connected to the ground. The

random movement of the ions inside the chamber makes them reach the target and chemical reactions etch the material. Plasma etching makes highly isotropic etching. R.F excitation creates ions by energetic collision of electrons with atom and molecules. These ions are mainly takes part to etch the material. Schematic of PE process is shown in Figure A.8 where the gases are ionized by applying the R.F at the top electrode and target material is placed on the bottom electrode which is connected to ground. Pressure inside the chamber varies from the few mTorr to few hundred mTorr. High gas pressure inside the chamber helps the ions to move randomly toward the target material and chemically etches the material [Matthieu].

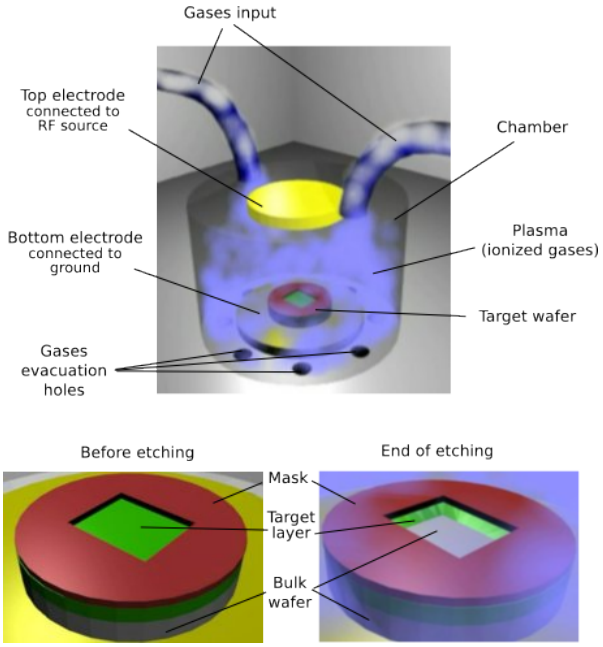

Figure A.8 Schematics of the principle of Plasma Etching [PE] [Matthieu].

A.2.2.2. Reactive ion etching (RIE)

RIE is a variation of PE. The principle of etching device is almost the same, but this time, the chamber top electrode is connected to the ground and the wafer is placed on the excitation electrode (Figure A.9). Since the wafer is connected to the R.F. signal instead of the ground in PE case, electrons are statistically more often in contact with the target than positive ions. When the substrate is placed inside a reactor several gases are introduced in the chamber. Plasma is struck in the gas mixture using an RF power source, breaking the gas molecules into ions. Ions are accelerated towards, and react at the surface of the material being etched, forming another gaseous material. This is known as the chemical part of reactive ion etching.

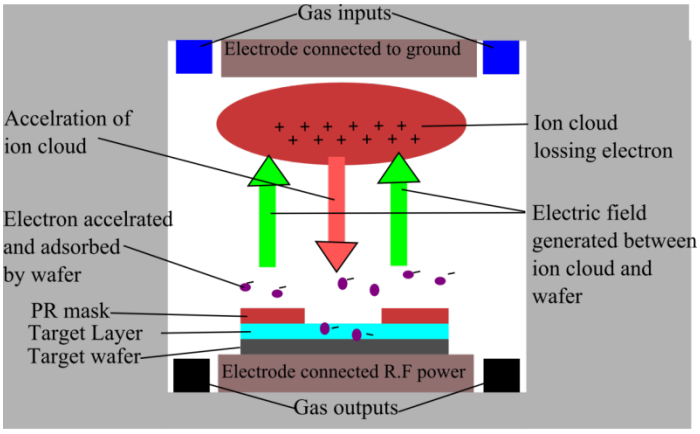

Figure A.9 Schematics of RIE chamber.

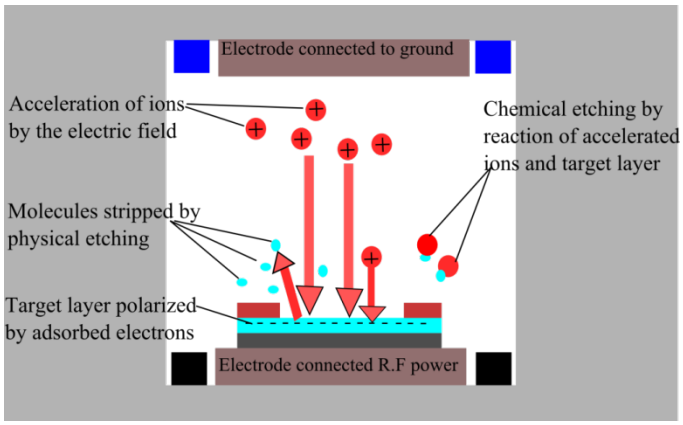

Figure A.10 Schematics of the physical and vertically directed chemical etching in RIE.

There is also a physical part which is similar in nature to the sputtering deposition process. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction. It is very complex tasks to develop dry etch processes that balance chemical and physical etching, since there are many parameters to adjust. By changing the balance it is possible to influence the anisotropy of the etching, since the chemical part is isotropic and the physical part highly anisotropic the combination can form sidewalls that have shapes from rounded to vertical. Schematic for such anisotropic etching process can be seen in Figure A.10.

In this way RIE offers the anisotropic etching but such process highly depends on the material to be etched. To have anisotropic etching during RIE, material which has to be etched should have ability to adsorb electron otherwise etching result will similar (isotropic) to the PE. Dielectric material has less ability to absorbed electron whereas semiconductors have high ability. Because of it, anisotropic etching mainly concern to the semiconductors and composite material etc. however etching rate in RIE is not very

high as etching highly depends on the chemical reaction products from plasma which gives electron and ion. Electron get adsorbed to wafer surface whereas ion etches the surface but should not be very fast as electron should get enough time to be absorbed on the surface. To calibrate the etch rate, process needs several run. Finally, RIE has advantage over the PE in order to get highly anisotropic etching. Another kind of plasma etch process to get anisotropic etching with high etch rate in comparison to RIE has been developed as Deep reactive ion etching (DRIE).

A.2.2.3. Deep reactive ion etching (DRIE)

A special subclass of RIE is deep RIE (DRIE). In this process, etch depths of hundreds of microns can be achieved with almost vertical sidewalls. The primary technology is based on the so-called "Bosch process" [Laermer 1996] where two different gas compositions are alternated in the reactor. In the first step of BOSCH process, etching is purely isotropic plasma etching and plasma contains some ions (often fluoride ion from SF_6 for silicon etch), which attack the wafer from a nearly vertical direction. In the second step, chemically inert passivation layer is deposited in the etched surface. Sources gas for such passivation layer is C_4F_8 (Octafluorocyclobutane) which yields a substance similar to Teflon. During these two steps, both phase, etch and deposition last for several second. Passivation layer protect the substrate from chemical attack for further etching however highly directional ion succeed to etch the layer from the bottom of trenches (but not from the side walls) and expose the bottom surface for further chemical etching. Figure A.11 shows the sidewall of silicon etched by BOSCH process. In order to achieve etch depth up-to several hundred microns, complete process needs several etch/deposit steps. Such etch/deposit cycles time can also be control according to requirement like short cycle provide smother walls and long cycle provide high etch rate.

Further DRIE is the only dry etching process, that can be used for deep etching up to few hundred microns with high etch rate, good mask selectivity, high aspect ratio, and high anisotropy which is requirement for several MEMS devices.

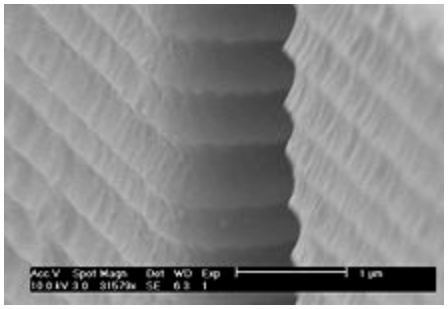

Figure A.11 Undulating sidewall of a silicon structure created using the Bosch process.

ICP technology can be used in various micro fabricated devices for example Figure A.12 shows the micro fabricated micro-needle with 300μm in height using ICP etching tool [Jing 2006]. Apart from several technological advantages especially really deep vertical cavity, DRIE also has several disadvantages like in comparison to wet chemical etching, DRIE machine itself very expensive and then materials required for the process like C_4F_8 and liquid nitrogen are also expensive. Moreover single process can be processed at the same time.

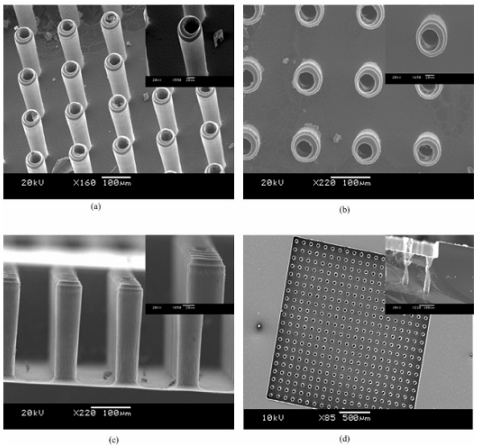

Figure A.12 Images of micro fabricated micro needle using ICP etching tool [Jing 2006].

A.3. Technology and mechanisms of anodic bonding

Anodic bonding was first mentioned in 1969 [Wallis 1969]. Since that time, anodic bonding has been studies and developed for several applications in semiconductor industry. Anodic bonding is mainly known as chemical bonding between sodium rich glass and silicon. In the following section, silicon-glass anodic bonding, its mechanism and basic parameters are described.

A.3.1. Silicon-glass anodic bonding

Basic equipment required to perform silicon to glass anodic bonding includes a heated conductive table with flat and smooth surface, high-voltage DC power supplier, DC current meter, and touch-type needle polarization electrode, as shown in Figure A.13.

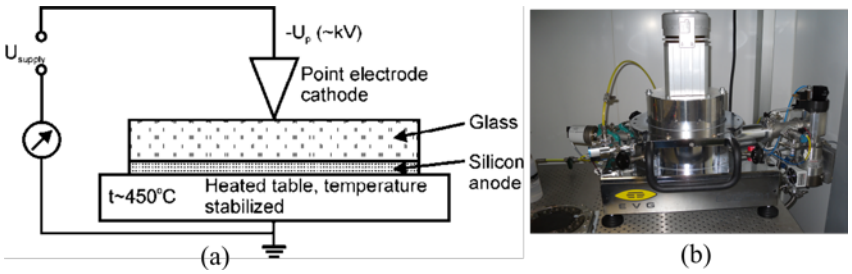

Figure A.13 Schematic of standard anodic bonder; (a) scheme, (b) photograph of EVG bonder at FEMTO-ST.

Here, the silicon wafer is placed on the hot table first, next the glass ones on top. Wafers adhere to each other and come to the close contact thanking to the Vander Waals forces. Silicon-glass sandwich is heated to the bonding temperature (300-500°C). Next, the sandwich is polarized by high voltage (500-2000 V): the silicon wafer, placed on the table, is polarized positively, while the glass wafer, located on silicon, is polarized negatively. The electrical conductance of hot glass is high, so, under the influence of strong electric field the ion current of movable positive charges - mainly sodium - flows in glass. As the result, the sodium depletion layer reach in negative charge evolves near the silicon-glass boundary, forming a kind of flat capacitor polarized by high voltage, which plates are distanced a few dozen nanometers.

Drop of polarization voltage occurs only at the silicon-glass boundary. The result is the formation of a very strong electrostatic attraction force pulling the bonded materials against each other. Surfaces of silicon and glass are brought to the ultimate contact, the distance between surfaces becomes so small, that direct siloxane bonds are formed between the sealed materials.

Bonding proceeds in a form of so-called wave of bonding [Dziuban 2006]. It propagates from the area of the initial bonding (bonding precursor) at a speed reaching a few cm per second. During the process of bonding the electric current flows in the circuit. Just after bringing of the materials into contact and applying the polarization the current is the highest; as the wave of bonding extends current decreases as a function of time. It is commonly believed, that the process of bonding is finished when the value of current reaches approximately 10% of its maximal value.

A.3.2. Chemical model of bonding

The interactions of physical forces, which lead to the alignment of silicon and glass surfaces, are accompanied by the reactions that form permanent chemical bonding between sealed materials. It is commonly accepted, that permanent bonding between silicon and glass is formed by strong siloxane Si-O-Si bonds but the course of the process of the formation of bonds has yet not been fully explained. According to the Baumann model [Baumann 1995] of bonding, the formation of Si-O-Si bonds is assumed.

The solid-state electrolysis of Na_2O under the influence of electric field in hot glass generates sodium ions and free oxygen:

$$Na_2O \rightarrow 2Na^{+} + O^{--}$$

Simultaneously occurs the dissociation of molecular water adsorbed on hydrophilic surfaces of silicon and glass and hydrogen coming from the decomposition of water diffuses to glass, where it takes part in the electrolysis of Na_2O according to the formula:

$$Na_2O + H^{+} \rightarrow 2Na^{+} + OH^{-}.$$

Oxygen coming from the decomposition of Na_2O and the OH^{-} groups from the decomposition of water migrate toward anode where they react with silicon, which results in the formation of SiO_2 and ≡SiOH (≡ symbolizes, that hydrated silicon surface atom is bonded by three bonds to silicon atoms, its neighbours). Sodium ions are neutralized near the cathode. Sodium consumes the atmospheric oxygen or oxidizes at the cost of non-bonded oxygen taken from the glass matrix forming Na_2O in the region near the cathode. Next, Na_2O forms with water from air sodium hydroxide NaOH, which attacks the cathode and glass in the region near the cathode:

$$Na^{+} + 4\,\bar{e} \rightarrow Na$$

$$2Na_2O + 2H_2O \rightarrow 2NaOH.$$

At the same time, on the closely “clamped” by electrostatic pressure bonded surfaces, the process of dehydration of partly oxidized surfaces proceeds:

$$\equiv Si\text{-}OH + OH\text{-}Si \equiv \rightarrow \equiv Si\text{-}O\text{-}Si \equiv + H_2O$$

Baumann assumed in the model electrolysis of Na_2O and the presence of non-bonded oxygen, coming from this process, in glass. Schmidt demonstrated that non-bonded oxygen, which could be a product of the decomposition of Na_2O, does not appear in the borosilicate glass during bonding. What is more, he demonstrated, that sodium ions form ion association complexes with $(BO_4)^-$ or $(AlO_4)^-$. According to that, the escape of sodium to the cathode has to be compensated by the inflow of hydrogen, which replaces sodium. The presence of H^+, in the quantity corresponding to the amount of sodium ions removed from the depletion layer in glass, was confirmed with use of the Elastic Recoil Detection Analysis.

Basing on these results, a mechanism of bonding have been proposed where in the first step molecular water adsorbed at the hydrophilic surface of bonded glass decomposes under the influence of temperature and electric field:

$$H_2O \rightarrow H^+ + OH^- \text{ or } 2H_2O \rightarrow H_3O^+ + OH^- .$$

Hydroxyl groups drift towards silicon:

$$Si + 4OH^- \rightarrow Si(OH)_4 + 4\bar{e} ,$$

And then the dehydration of Si-OH bond occurs, effecting in forming of siloxane bonds between silicon and glass:

$$Si(OH)_4 \rightarrow SiO_2 + 2H_2O.$$

Released water enters once more the cycle of decomposition and chemical reaction with silicon, until it is consumed. Hydrogen, being the by-passed product of molecular water decomposition drifts in electric field, through hot glass, toward cathode and replaces sodium in $(BO_4)^-Na^+$ association complex:

$$(BO_4)^-Na^+ + H^+ \leftrightarrow (BO_4)^- H^+ + Na^+ \qquad (AlO_4)^-Na^+ + H^+ \rightarrow (AlO_4)^-H^+ + Na^+$$

Sodium drifts in the direction of the cathode, where it is neutralized as described in Baumann's model. According to the model, the process of anodic bonding is activated by electric field. It is a type of anodic oxidation of silicon, where surface water is an essential component. Electrostatic pressure, caused by the escape of sodium ions and the formation of depletion layer, is also important. Electrolysis of Na_2O in glass does not occur.

However, it seems that the possibility of dissociation of Na_2O, compatible with the Baumann's model and confirmed indirectly by the change in composition of glass in depletion layer, cannot be excluded. It is possible that oxygen, coming from Na_2O, bonds with hydrogen and hence it does not appear in non-

bonded form, which is consistent with the results of Schmidt et al. [Schmidt 1998], as shown in Figure A.14.

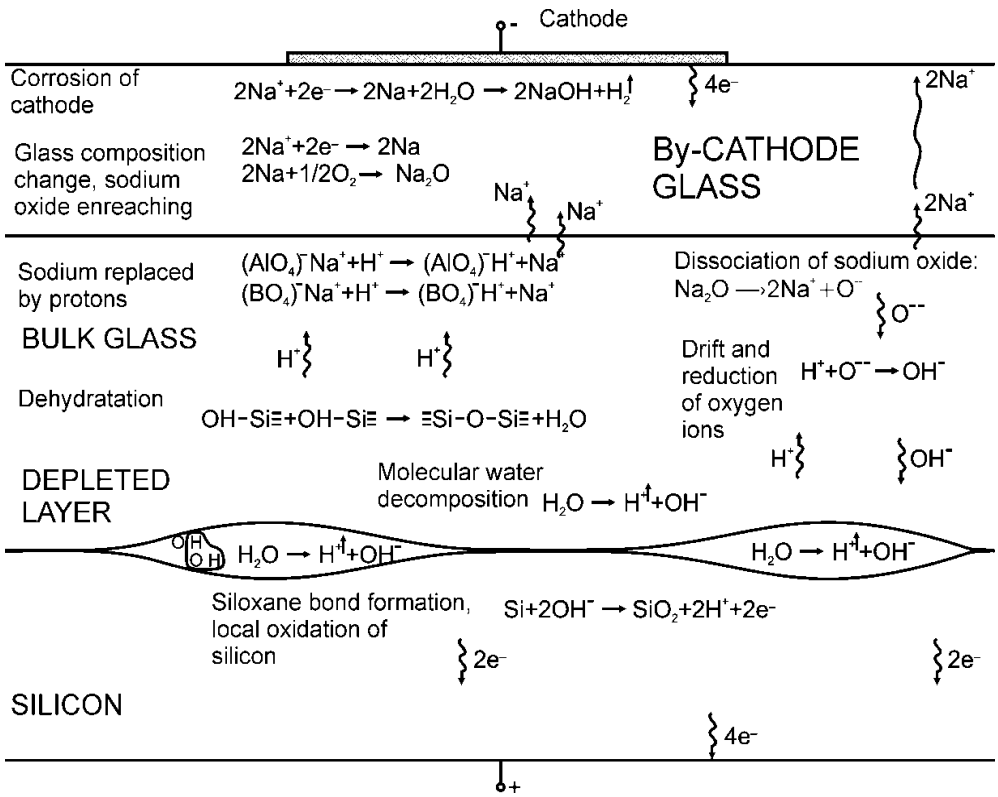

Figure A.14 Mechanism of bonding [Dziuban 2006].

In conclusion, J. Dziuban [Dziuban 2006] defines the process of anodic bonding as a three-step process:

- Stage1: hydrophilic surfaces of silicon and glass, after the preliminary bonding and heating to the temperature of a few hundred degrees centigrade, form a weak bond due to the attraction of Van der Waals forces and long hydrogen bonds, similar as observed for fusion bonding for two hydrophilic silicon substrates,
- Stage 2: polarization is applied. Sodium drifts in the direction of the cathode, bonding current increases rapidly; a quasi-quartz depletion layer is formed in glass, near the glass boundary, from the side of silicon. Bonded surfaces are electrostatically clamped. The distance between bonded surfaces approaches several parts of nm. Molecular water existing at hydrophilic surfaces of silicon and glass decomposes into hydrogen and hydroxide OH- groups. Hydrogen drifts through glass toward cathode. Dissociation of Na_2O causes generation of sodium ions, drifting under electrical field toward cathode, and oxygen ions, which react with hydrogen, forming additional OH^- groups. Those groups drift slowly toward anode, where together with OH^- groups being a by-

pass product of decomposition of surface molecular water oxide silicon at surfaces of bonded wafers forming ≡Si-OH-OH-SI≡, which replace long hydrogen bonds existing at the very beginning of sealing procedure. Hydrogen, being a product of the decomposition of water, replaces sodium in $(BO)_4^-Na^+$ and $(AlO_4)Na^{+-}$ in glass. The dehydration of surface occurs on the silicon-glass boundary. Weak ≡Si-OH-OH-SI≡ bonds are replaced by siloxane ≡Si-O-SI≡ bonds. Distance between bonded substrates reaches 0.3 - 0.5 nm. Wave of bonding propagates, substrates seal. In this model, the bonding current flow is proportional to the stream of hydrogen ions coming from surface water dissociation, but the maximal value of the current is limited by available number of sodium ions coming from dissociation of NaO_2. At the beginning of sealing, current increases rapidly, next, decreases slowly, following consumption of molecular water at the bonded surfaces. So long all water is not "consumed", so long current flows,

- Stage 3: when all of water had been consumed and the thin layer of transient silicon oxide layer was formed, the sealing process finishes. Bonding current stabilizes at low value, limited mainly by the leakage current of formed SiO_x dielectric layer. Surface energy of bonding γ exceeds 3.5 J/m^2, and the obtained silicon to glass bonding is stronger than the forces, which bond monolithic silicon.

The described mechanism of anodic bonding consists of the production of silicon oxides, resulting in siloxane bridging of the bonded surfaces. In the anodic bonding the formation of sealing proceeds as the process of oxidation of anode in the presence of electric field and at relatively low temperature (400-500°C). The most important here is alignment of surfaces by electrostatic pulling force (pressure), being the effect of the depletion layer formation in glass. The formation of the depletion layer is the effect of electrical charges flow through the bonded sandwich, manifested as a flow of anodic bonding current in an external polarizing circuit.

Now, becomes clear, why weaker sealing, obtained at low temperature must influence negatively the internal atmosphere of the vacuum sealed cavities. Molecular water and OH- groups, as well as gaseous oxygen generated in the near-surface area in glass (despite the scientific discussion on the detailed mechanism, authors agree that gaseous by-product are always the result of bonding) must be completely consumed during bonding procedure. This can be obtained under reasonably short sealing procedure, made at higher temperature, at least 400-450°C. Polarization plays secondary role, as the anodic bonding process is thermally activated. The non-direct measure of the course of anodic bonding process is the current-time curve. Good process, in which all water and resulting from chemistry of bonding OH- groups and oxygen is used for forming of siloxane bonds, results in sharp, fast decreasing in time current of bonding, which final value should not exceed 10% of its maximal value. Test shows (Figure A.15) that

even at 300°C, current curve does not fulfil this parameters. The interface silicon-glass of samples bonded at low temperature is chemically unstable.

(a) (b)

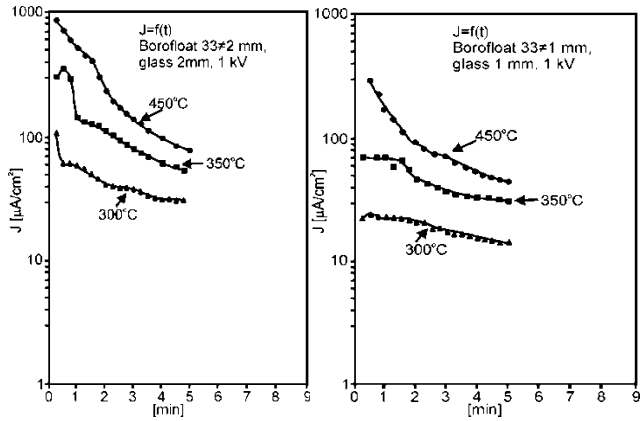

Figure A.15 Current characteristics of silicon to glass bonding, influence of temperature for Borofloat 33 glasses, constant polarization U_p=1 kV; (a) Borofloat 3, 1 mm glass; and (b) Borofloat 33, 2 mm glass.

A.3.3. Critical parameters of anodic bonding

Strength of anodic bonding sealing is depending on several factors but the bonding temperature and polarization voltage is the most important. Many tests have shown that lower temperature needs higher polarization and longer time of sealing. Thus, below 250 °C, borosilicate Pyrex glass cannot be strongly and vacuum-proof bonded to silicon even with application of extremely high polarization. The research on the influence of temperature and polarization voltage on the strength of bonding of silicon to different types of glass was carried out where the strength of bonding was estimated by means of destructive pull test method [Dziuban 2006]. Results are presented in Table A.1. Research showed that weak bond called bonding A (force equalling 20 MPa) was obtained under the conditions comparable to those, applied to seal our Cs cell. Bonding B, with strength equaling from 20 to 30 MPa, could be obtained for reasonably higher temperature. Finally, bonding C, with strength from 30 to 40 MPa, was satisfactory; small non-bonded areas were observed. Current-time curve was sharper; the final current was about 10% of its maximal value. Very good bonding (marked D) was characterized by high strength (above 40MPa) and rapid drop of bonding current in time. The final current met a condition attributed to the optimal conditions of bonding and equalled to 0.1 I_{max}. The conditions of C, C/D and D bonding, under which a strong bonding was obtained, are marked with a heavy line. As it is clearly shown that the pair of parameters of the process: temperature 250°C and voltage 1000-1500 V, applied in both procedures of MCSAC fabrication, as referred in [Liew 2004, Lutwak 2003, Kitching 2004], cannot ensure satisfactory

force of bonding, and, as will be shown later, cannot ensure stable post-bonding atmosphere inside a cavity containing buffer gases.

Table A.1 Strength of silicon to glass bonding according to [Dziuban 2006].

Type of glass	Thickness [mm]	Temperature [°C]	Voltage [V]					
			500	700	900	1000	1200	1500
Borofloat 33	1	250	A	A	A	A	A	A
		300	A	A/B	A/B	B	B	B
		350	A	B	B/C	B/C	C	C
		400	B	B/C	C	C	C/D	D
		450	B	C	D	D	D	D
	2	300	A	A	A	A	A	A
		350	A	A	A/B	A/B	B	B
		400	A	A	B	B	B/C	C
		450	A/B	B	B/C	C	C/D	D

Excellent bonding results, concerning 2 mm-thick Borofloat 33 glass, which seems to be the easiest bondable kind of glass, measured with use of the destructive test method are presented in Table A.2 [Dziuban 2006]. Results document that the good bonding must be done at least at 400°C, temperature of the process is more important than polarization value, although, from another reasons, higher polarization is acceptable but cannot cross a limit of electrical break-down of the glass.

Table A.2 Strength of bonding (MPa) in relation to the parameters of bonding according to [Dziuban 2006].

Temperature [°C]	Voltage [V]						
	500	700	900	1100	1300	1500	1700
300	-	-	-	-	-	2	5
350	-	10	15	15	17	25	26
400	15	16	23	29	30	33	40
450	20	23	30	38	40	44	46

A.4 Conclusion

General presentation of all microfabication technologies described here were used for this thesis work in the development and optimization of specific processes used in fabrication of two categories of Cs vapor cells: the transmissive version (T-cell) as well as reflective (R-cell) one. Thus, DRIE process was optimized to make T-cell cavities described in the Chapter 2 along with original two step anodic bonding procedure under the buffer gas environment developed for filling the cells with buffer gas at control pressure and strong sealing of cells. Further, Wet KOH etching has been optimized for development of R-cell fabrication and diffraction gratings were developed, fabricated using electronic lithography (E-beam) which was described in the Chapter 4.