Vectorial measurement methods for millimeter wave integrated circuits

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préparée au sein du **Laboratoire IMEP-LAHC**
dans **l'École Doctorale Électronique, Électrotechnique, Automatique et Traitement du signal (EEATS)**

Méthodes de Mesure pour l'Analyse Vectorielle aux Fréquences Millimétriques en Technologie Intégrée

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“Everything has been figured out, except how to live.”

— Jean-Paul Sartre

Résumé

Cette thèse porte sur l'étude des méthodes de mesure pour l'analyse vectorielle des circuits microélectroniques en technologie intégrée aux fréquences millimétriques. Pour réussir à extraire les paramètres intrinsèques de circuits réalisés aux longueurs d'ondes millimétriques, les méthodes actuelles de calibrage et de de-embedding sont d'autant moins précises que les fréquences de fonctionnement visées augmentent au-delà de 100 GHz notamment. Cela est d'autant plus vrai pour la caractérisation des dispositifs passifs tels que des lignes de propagation. La motivation initiale de ces travaux de thèse venait du fait qu'il était difficile d'expliquer l'origine exacte des pertes mesurées pour des lignes coplanaires à ondes lentes (lignes S-CPW) aux fréquences millimétriques. Etait-ce un problème de mesure brute, un problème de méthode de-embedding qui sous-estime les pertes, une modélisation insuffisante des effets des cellules adjacentes, ou encore la création d'un mode de propagation perturbatif ?

Le travail a principalement consisté à évaluer une dizaine de méthodes de de-embedding au-delà de 65 GHz et à classifier ces méthodes en 3 groupes pour pouvoir les comparer de manière pertinente. Cette étude s'est déroulée en 3 phases.

Dans la première phase, il s'agissait de comparer les méthodes de de-embedding tout en maitrisant les modèles électriques des plots et des lignes d'accès. Cette phase a permis de dégager les conditions optimales d'utilisation pour pouvoir appliquer ces différentes méthodes de de-embedding.

Dans la deuxième phase, la modélisation des structures de test a été réalisée à l'aide d'un simulateur électromagnétique 3D basé sur la méthode des éléments finis. Cette phase a permis de tester la robustesse des méthodes et d'envisager une méthode de-embedding originale nommée Half-Thru Method. Cette méthode donne des résultats comparables à la méthode TRL, méthode qui reste la plus performante actuellement. Cependant il reste difficile d'expliquer l'origine des pertes supplémentaires obtenues notamment dans la mesure des lignes à ondes lentes S-CPW.

Une troisième phase de modélisation a alors consisté à prendre en compte les pointes de mesure et les cellules adjacentes à notre dispositif sous test. Plus de 80 structures de test ont été conçues en technologie AMS 0,35 µm afin de comparer les différentes méthodes de de-embedding et d'en analyser les couplages avec les structures adjacentes, les pointes de mesure et les modes de propagation perturbatifs.

Finalement, ce travail a permis de dégager un certain nombre de précautions à considérer à l'attention des concepteurs de circuits microélectroniques désirant caractériser leur circuit avec précision au-delà de 110 GHz. Il a également permis de mettre en place la méthode de de-embedding Half-Thru Method qui n'est basée sur aucun modèle électrique, au contraire des autres méthodes.

Mots clés **:** *Méthodes de de-embedding, mesures de paramètres S aux fréquences millimétriques, modélisation électrique et electromagnétique*

Vectorial Measurement Methods for Millimeter Wave Integrated Circuits

Abstract

This thesis focuses on the study of vectorial measurement methods for analysing microelectronic circuits in integrated technology at millimeter wave frequencies. Current calibration and de-embedding methods are less precise for successfully extracting the intrinsic parameters of devices and circuits at millimeter wave frequencies, while the targeted operating frequencies are above 100 GHz. This is especially true for the characterization of passive devices such as propagation lines. The initial motivation of this thesis work was to explain the exact origin of the additional loss measured in Slow-Wave Coplanar Waveguides (S-CPW) lines at millimeter wave frequencies. Was it a problem of raw measurement or a problem of de-embedding method, which underestimates the losses? Or was it a problem of insufficient modeling of the effects of adjacent cells, or even the creation of a perturbation mode of propagation?

This work consists of estimating many de-embedding methods beyond 65 GHz and classifies these methods into three groups to be able to compare them in a meaningful way. This study was conducted in three phases.

In the first phase, we compared all the de-embedding methods with known electrical model parasitics of pad/accessline. This phase identifies the optimal conditions to use and apply these de-embedding methods.

In the second phase, the modeling of test structures is performed using a 3D electromagnetic simulator based on finite element method. This phase tested the robustness of the methods and considered an original de-embedding method called Half-Thru de-embedding method. This method gives comparable results to the TRL method, which remains the most effective method. However, it remains difficult to explain the origin of additional losses obtained in measured S-CPW line.

A third modeling phase was analysed to take into account the measurement of probes and the adjacent cells near our device under test. More than 80 test structures were designed in AMS 0.35 μm CMOS technology to compare the different de-embedding methods and analyse the link with adjacent cells, measuring probes and perturbation mode of propagation.

Finally, this work has identified a number of precautions to consider for the attention of microelectronic circuit designers wishing to characterize their circuit with precision beyond 110 GHz. It also helped to establish Half-Thru Method de-embedding method, which is not based on electrical model, unlike other methods.

Keywords: *De-embedding methods, S-parameter measurements at millimeter frequencies, electrical and electromagnetic modeling*

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General Introduction

The evolution of Silicon technologies, like Complementary Metal Oxide Semiconductor (CMOS) and Bipolar CMOS (BiCMOS) technologies, achieve a great place in the millimeter wave integrated circuits. It has many advantages such as low manufacturing cost, high integration density and low power consumption. These technologies driven RF applications into millimeter and sub-millimeter wave frequency range. In RF/Microwave, there are many applications serving each and every domain of science and technology, such as telecommunications (video-streaming (57-66 GHz), automotive radar (76-81 GHz)), imaging (around 140 GHz, 220 GHz, …)), security, medicine, environmental, etc. The development of the silicon technology causes the reduction in size of the devices and circuits, especially in millimeter wave integrated circuits. These devices have to be measured and characterized, before its implementation on the circuits or systems. Therefore, a dedicated measurement and characterization of these devices at millimeter and sub-millimeter wave frequency range should be required to ensure the best performance.

Generally, the silicon-based devices are measured on-wafer with the help of probe station and vector network analyser. The measurement of the device includes additional parasitic effects from the pads and interconnecting lines, which are used to connect the device for the measurement. This affects the actual characteristics of the device and this should be subtracted from the measured results to get the actual characteristics of the device. The process of mathematically removing these unwanted parasitic effects is called “De-embedding”. The calibration of the vector network analyser and de-embedding are highly required for the devices and systems working at millimeter wave and sub-millimeter wave range. A good calibration can be obtained for example by using LRRM (Line-Reflect-Reflect-Match) calibration with the Cascade Microtech systems for on-wafer measurement. After the calibration, measurement of the device and de-embedding should be performed to extract the actual characteristics of the device.

Currently, most of the de-embedding methods are investigated until millimeter wave frequencies, i.e. up to 60 GHz or 110 GHz. However, in the current scenario, more importance is given to develop the devices and applications at millimeter wave and sub-millimeter wave frequencies. So the development of de-embedding methods is quite challenging. There are many methods available at low frequency range. Most of the de-embedding methods are developed by considering the parasitics effects of pads and accesslines as lumped models or cascaded elements or the combination of both. Considering the high frequency and thus the small size of the devices, efficient de-embedding methods must be

considered to obtain accurate measurement results. TRL (Thru-Reflect-Line) algorithm is considered as a very good de-embedding method for high frequencies. Nevertheless, the few limitations restrict the TRL, such as the band limited operation and the value of characteristic impedance of the transmission line used to set the reference plane. This increases the complexity and number of de-embedding structures, thus increasing the cost for wide band de-embedding. In addition, many other de-embedding methods are not evaluated for the higher frequencies. In this thesis, we apply the efforts to analyse different de-embedding methods for millimeter wave and sub-millimeter wave frequencies. In addition, we develop new methods employing no unknown terms and good accuracy over a wide band de-embedding.

Beyond millimeter wave frequencies, the environmental measure around the device under test is very critical and the effects of the pads and the substrate are no longer simple localized parasitic elements. To understand these effects, an extensive study on both the measurement and modeling is required. These make DUT characterization and de-embedding at millimeter wave frequencies and above highly challenging. Accurate characterization and de-embedding of the devices in silicon technologies can enable greater performance over the circuits that are implemented. In addition, the accurate extraction of the characteristics of the device reduces the modeling efforts of IC design, thus the time and cost. Therefore, a need for an accurate and reliable de-embedding method to characterize the device at millimeter wave and sub-millimeter wave frequency is required.

Outline and aim of the thesis

In this thesis, we will study and develop de-embedding methods by considering S-CPW (Slow-Wave Coplanar Wave Guides) transmission line as the device under test. S-CPW transmission line is a miniaturized transmission line topology exhibiting a high quality factor compared to classical transmission lines like microstrip and CPW. IMEP-LAHC is developing applications and passive devices based on S-CPW transmission line until sub-millimeter wave frequency range. Therefore, it is important to characterize the S-CPW transmission line to ensure the best performance of the devices and applications. This work is performed in AMS 0.35 µm and BiCMOS 55 nm technology and focuses on the development of de-embedding methods to characterize the device, mainly transmission lines beyond 100 GHz. Thus, first we benchmark and explain different de-embedding methods for millimeter wave transmission line de-embedding other than proposing a new de-embedding method.

Chapter 1 gives a review of the state of the art of passive device measurements and characterization for millimeter wave and sub-millimeter wave frequency range. It includes the review about S-CPW transmission line and its applications in millimeter wave and sub-millimeter wave. Further, it describes the different problems in the electromagnetic modeling, de-embedding challenges and other issues on on-wafer measurement at millimeter wave frequencies and above.

Chapter 2 reviews and benchmarks the current de-embedding methods. It includes classification according to the de-embedding strategies and explanation of de-embedding methods. These methods are utilized to de-embed the devices, according to the size of the DUT and the range of frequency. This chapter benchmarks all the de-embedding methods, by considering first electrical modeling and second 3D electromagnetic (EM) modeling using simulation tool Ansys HFSS. In addition, the chapter explains the different limitations and different characteristics needed for a good de-embedding method for a wide band up to millimeter wave and sub-millimeter wave frequency range.

Chapter 3 explains the studies on novel de-embedding method called "Half-Thru De-embedding". This method has been developed to overcome the limitations of other de-embedding methods. Half-Thru de-embedding method has been developed to characterize the devices at millimeter wave and sub-millimeter wave frequency range. This chapter includes the theoretical analysis and proof of the method at millimeter wave and sub-millimeter wave frequencies. The method is tested for 3D EM models of S-CPW transmission lines, which are modeled in Ansys HFSS. Further, we explain the restrictions of this method and the solutions for it. Apart from the Half-Thru de-embedding method, we present a simplified method of Half-Thru de-embedding method called Thru-Load de-embedding method. Benchmarking and comparison with TRL are presented in this chapter.

Chapter 4 compares both simulated and actual de-embedding results from the measurements, where the DUT and the de-embedding structures were fabricated in the AMS 0.35 µm CMOS technology and BiCMOS 55 nm technology. The uncertainties in the measured de-embedding results and the excessive loss happening beyond millimeter wave frequencies are explained based on a new realistic EM simulation model by taking of all possible parasitics from the on-wafer measurement into account. Finally, we compare and benchmark the different de-embedding methods with Half-Thru de-embedding and the Thru-Load de-embedding methods.

Finally, the results of this thesis are summarized and the future perspectives are presented.

1. Millimeter Wave Device Measurement and Characterization in Silicon Integrated Circuits

In the present and future, there are large number of applications in the millimeter and sub-millimeter wave frequency range such as video streaming (57-66 GHz), automotive radar (76- 81 GHz) and medical imaging (around 140 GHz). The rapid growth and development in the millimeter wave technology cause miniaturization of components and circuits especially in millimeter wave integrated circuits. As the frequency of operation increases, the size of the devices reduces from millimeter to micrometer and nanometer. An increasing number of applications in the millimeter wave and sub-millimeter wave ranges and the reduced size of the devices require accurate measurement to ensure the best performance.

This chapter gives a review of the state of the art of passive device measurements and characterization for millimeter wave and sub-millimeter wave frequency range. It includes the review about S-CPW transmission line and its applications in millimeter wave and sub-millimeter wave. Further, it describes the different problems in the electromagnetic modeling, de-embedding challenges and other issues on on-wafer measurement at millimeter wave frequencies and above.

1.1 State of the Art and Problem Description

With the continuously emerging technologies and development of many applications in the millimeter wave and THz applications, design and characterization of the device become critical. The evaluation of silicon technologies [1], like Complementary Metal Oxide Semiconductor (CMOS) and the Bipolar CMOS (BiCMOS) technologies, leads the commercial RF and millimeter wave applications. Silicon integrated circuits are empowering the semiconductor growth in the past half a century. This exponential growth often referred to Moore's law and the cut-off frequencies of silicon transistors are reached above 100 GHz along with applications even at higher frequencies. Due to size reduction in the device geometries and technology improvement, it is possible to achieve operating frequencies up to THz in these technologies. The passive devices/structures serve a greater portion in all applications [2]. The main utilized passive structures in millimeter wave circuits are inductors, capacitors, **transmission lines**, transformers, etc. Transmission lines serve an important role to connect each device in all RF and millimeter-wave applications. The modeling and characterization of the

transmission lines are important for the millimeter wave applications and beyond, because its characteristics can vary beyond the normal expectation values.

1.1.1 Transmission Lines for Millimeter-Wave and Sub-Millimeter-Wave Frequencies and Applications

In general, a transmission line is a media that can carry or guide the electromagnetic energy between a generator and a load. There are many types of transmission lines available for guiding the signals, like twisted pairs, coaxial cables, optical fibers, strip line, microstrip transmission lines, coplanar transmission lines, etc. [3], [4]. These transmission lines are used for different applications according to their features, range of frequency and compatibility. Here we deal with the planar transmission lines such as Microstrip lines, Strip lines and Coplanar Wave Guides (CPW) that can be easily integrated in silicon technology.

RF microelectronics research started emerging with the development and use of planar transmission line / propagation structures, because of its features, like ease of fabrication, miniaturization and adaptability for both active and passive devices. With the increase in frequency, applications and the development of novel substrates led microstrip and CPW to widely used as transmission lines for RF applications[3]-[10]. Recently, **Slow-Wave Coplanar Wave Guides (S-CPW)**, a novel structure developed to use instead of microstrip and CPW. In this thesis, we characterize the emerging topology S-CPW along with coplanar waveguide transmission lines and microstrip transmission lines.

1.1.2 Slow-Wave Coplanar Waveguide (S-CPW) Transmission Line

S-CPW was introduced [11]-[15] to miniaturize and to improve the quality factor (Q-factor) of the passive structures. The major drawbacks of the microstrip transmission lines and the CPW transmission lines in the silicon-integrated technologies are their size and poor quality factor. There are different approaches that have been done to miniaturize the transmission lines, by using high permittivity substrates and lumped or semi-lumped components [15], but these are restricted to apply in the silicon integrated technologies. In the silicon integrated technologies the classical transmission lines such as CPW have high losses when the frequency increases, due to its dielectric loss effects in the low-resistivity silicon substrate and the conductive loss. Concerning microstrip lines, losses are limited because, the ground plane prohibiting the electromagnetic field to go through the low-resistivity substrate. Nevertheless, due to a low effective dielectric constant, a low Q- factor can be achieved.

The standard approach to miniaturize the transmission line is by increasing relative dielectric permittivity ε_r of the substrate, which eventually reduces the phase velocity, $v_p = c/\sqrt{\varepsilon_r}$. The "Slow wave" transmission line uses the principle of separating the electric and magnetic energy, to reduce

the phase velocity instead of using a high dielectric permittivity ε_r substrate. S-CPW are based on conventional CPW with floating metallic strips underneath the line as shown in Figure 1.1.

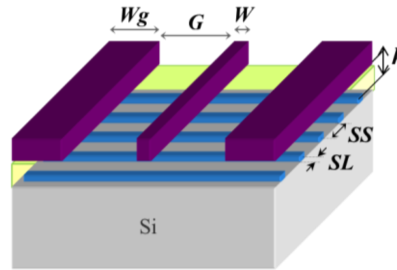
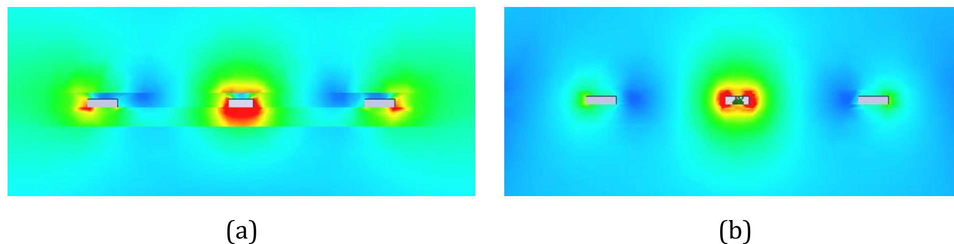


Figure 1.1. S-CPW Structure

Consider a classical S-CPW configuration, where *W* is the width of the signal strip *G is* the gap between signal and ground, *Wg* is the ground plane width, *SL* is the floating strips length, *SS* is floating strips space and *h* is dielectric thickness between floating strips and the CPW lines.

The electric and magnetic field propagation modes of S-CPW simulated using a 3D electromagnetic solver Ansys HFSS [16] are shown in Figure 1.2. In Figure 1.2 signal strip is in the center with two ground strips on both sides, like conventional CPW and with horizontal floating strip to reduce the phase velocity.



(a) (b)

Figure 1.2. S-CPW line: (a) E- Field (b) H- Field

From the S- CPW line in Figure 1.2(a), the fingers of length *SL* with a space of *SS* are created as a shield against the low resistivity substrate. If we use a whole ground instead of floating fingers (such as microstrip lines), we induce eddy currents in the thin lower metal layer and it would increase the significant conductive loss. In S-CPW, the transversal arrangement of the floating fingers prevents the currents flowing longitudinally to the signal propagation. Moreover, if fingers gap *SS* is optimized the electric field is confined between the signal and grounds of S-CPW. Since there is no electric field in the lossy silicon substrate, the losses due to the low resistivity silicon substrate are reduced. Hence S-CPW losses are comparable to microstrip line losses and lower than CPW ones. Finally, the floating shield results in the significant increase of the capacitance per unit length C_l compared to CPW. As shown in Figure 1.2(b) the magnetic field passes through the patterned ground, hence the inductance per unit length L_l is quite unchanged compared to CPW lines.

Thanks to the increase of the capacitance, the phase velocity in the S-CPW (1.2) decreases as compared to the CPW transmission line. Therefore, it is "Slow-Wave" coplanar waveguide. Due to this we can obtain (1.2) a high relative effective permittivity.

$$v_p = \frac{1}{\sqrt{L_l . C_l}} \tag{1.1}$$

$$\varepsilon_{reff} = C_0^2 . L_l . C_l \tag{1.2}$$

Also the quality factor [17] expressed as,

$$Q = \frac{\beta}{2\alpha} \tag{1.3}$$

The advantages of S-CPW lines are easy miniaturization and higher quality factor, about 2 to 3 times higher than the classical transmission lines in CMOS/BiCMOS technologies [15].

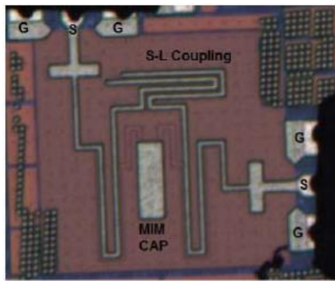
1.1.3 Motivation: Applications at Millimeter-Wave Frequencies and Above

The transmission lines are an essential passive component for any device/application from the low frequency to the high frequency. Concerning the applications of millimeter and sub-millimeter wave frequency circuits (Video-streaming 57-66 GHz, 76- 81 GHz automotive radar, medical imaging 140 GHz, etc.) the need and characterization of the transmission lines are very important. Transmission lines are used in wide variety of passive and active applications such as interconnection for the circuits, calibration and de-embedding circuits from vector network analyser (VNA) to devices, filters, baluns, power dividers, couplers, power amplifiers, detectors, mixers, antennas, trans receivers etc. They serve a major role in every two ports and multiport devices.

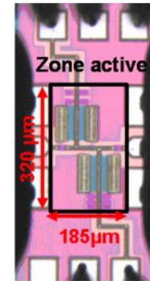
Some applications/devices using microstrip transmission lines and CPW Transmission lines are shown in Figure 1.3. Figure 1.3 (a) shows 60 GHz MM BPF[18] using a microstrip lines, Figure 1.3(b) is a Power Amplifier matching network using Microstrip Stubs [21], Figure 1.3(c) shows a chip microphotograph of the 30-GHz CPW filter[19] and Figure 1.3(d) shows a chip microphotograph of the 3-stage 60-GHz CPW amplifier [19].

Since S-CPW transmission lines have many advantages over microstrip and CPW transmission lines, they can be widely used in many passive and active circuits/applications. IMEP-LAHC is developing applications specifically based on S-CPW topologies. Figure 1.4(a) shows Band Pass Filter (Dual Behaviour Resonator (DBR) type) which uses S-CPW lines, [20], further examples with the power splitter and power dividers with S-CPW transmission lines [22], [15], which are shown in Figure 1.4(b)

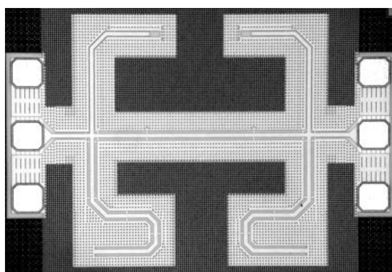
and Figure 1.4(c) and finally the matching network of a power amplifier is changed from microstrip to S-CPW [21] shown in Figure 1.4(d).



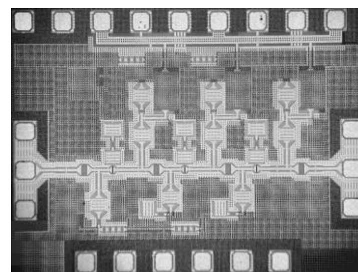
(a) 60 GHz MM BPF[18]



(b) Power Amplifier matching network Using Microstrip Stubs[21]

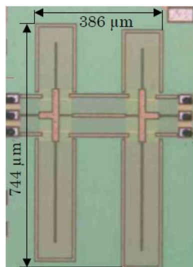


(c) Chip microphotograph of the 30-GHz CPW filter[19]

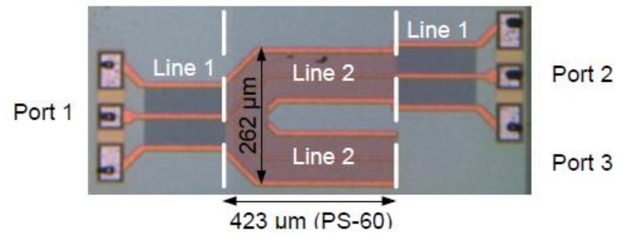


(d) Chip microphotograph of the 3-stage 60-GHz CPW amplifier[19]

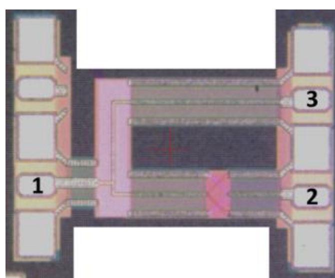
Figure 1.3. Different RF/millimeter wave applications utilize Microstrip and CPW transmission lines



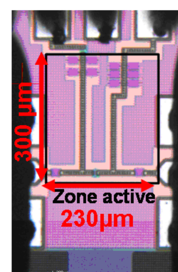
(a) Band pass Filter (DBR type)[20]



(b) Power splitters[15]



(c) Power divider balun[15]



(d) Power Amplifier matching network using S-CPW[21]

Figure 1.4. Different RF/millimeter wave applications utilize S-CPW transmission lines

The motivations of this Ph.D. thesis are to develop the de-embedding methods to characterize the transmission lines, especially, **S-CPW** at millimeter wave and sub-millimeter wave frequencies. Also analyse the various issues for **S-CPW**, CPW and microstrip transmission lines at millimeter wave and sub-millimeter wave frequencies and provide the solutions to overcome it [3]-[15].

1.1.4 Electromagnetic Modeling and Measurement Uncertainties

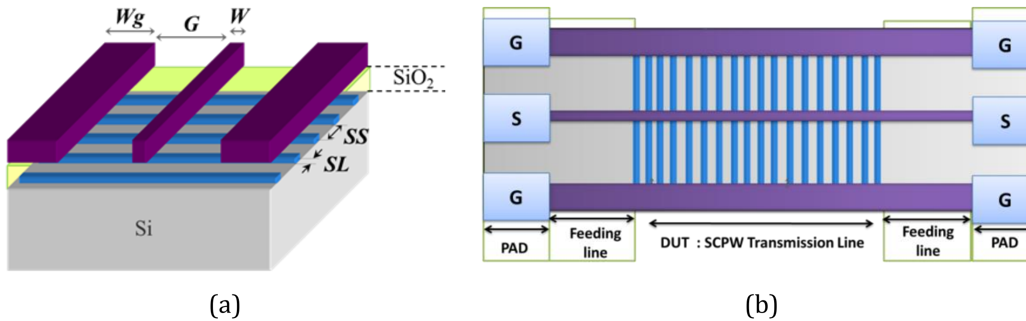
Considering the transmission line modeling, circuit designers use electrical scalable models (Using Agilent ADS or other circuit simulators) or electromagnetic (EM) models (Ansys HFSS, CST Microwave Studio, COMSOL Multiphysics…) to understand its characteristics.

Considering electrical scalable model and with its optimization, it is difficult to analyse the design problems at higher frequencies, especially when the targeting applications are in millimeter and sub-millimeter wave frequencies. The electrical scalable models are easy to use for designing and optimizing transmission lines. But considering all the parasitic and coupling elements of a transmission line model, especially at the millimeter wave frequency range, it is difficult and in many cases not even possible. It has the disadvantages of analysing proper electromagnetic behaviour of the transmission lines and difficulty to understand the radiation effects, higher order transmission modes, etc. [23]. Therefore, we need to have an EM (electromagnetic) model to characterize them properly for the different applications [24]. EM modeling helps to analyse all the physical effects of passive structures/devices such as losses, fields, radiation effects, higher order transmission modes, etc. The EM simulation is time consuming, but it gives more accurate results than the electrical scalable models.

Many 3D full wave Electromagnetic simulators are commercially available (Ansys HFSS, CST Microwave Studio, COMSOL Multiphysics…). These simulators use different mathematical techniques to solve and characterize electromagnetic structures. We utilize an industry-standard simulation tool Ansys HFSS (High Frequency Structure Simulator) [16]. This software is a 3D full wave frequency domain electromagnetic field solver based on the finite element method (FEM). HFSS automatically generates mesh and solves Maxwell's equations at several nodes of the meshing; also it allow us to generate our own strict meshing for the electromagnetic structures.

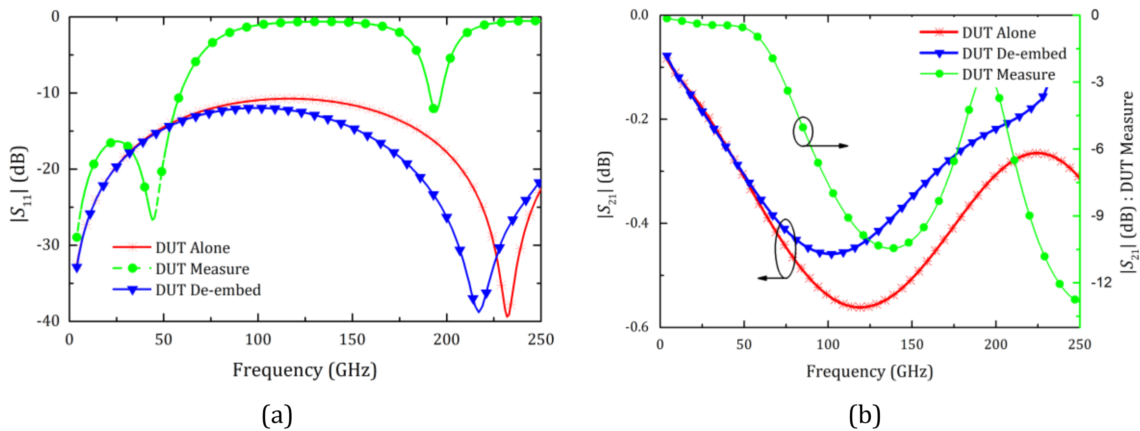
Consider a S-CPW transmission line [11]-[15] as shown in Figure1.5(a)as a Device under Test (DUT) . The transmission line is excited with wave port having an impedance of 50 Ω and with all the boundary conditions. The realistic measurement structure includes the pads and interconnects/accesslines to connect the DUT with the signal. Figure1.5 (b) shows the actual measurement model of of the S-CPW transmission line. The important factors for a realistic design of on-wafer passive structures are, to have a proper pad configuration (GS, GSG, GSSG, etc.) with a proper

probe pitch. In addition, pad size can vary with different probes, so it is better to have a minimum/proper pad size according to the probe used for the measurement.



(a) (b)

Figure1.5. (a) S-CPW alone (b) S-CPW under on-wafer measurement



(a) (b)

Figure 1.6. (a) $|S_{11}|$: reflection coefficient (b) $|S_{21}|$: transmission coefficient

The above S-CPW transmission lines are simulated up to 250 GHz using HFSS. The magnitude of the transmission and reflection coefficients (S_{21} and S_{11}) of the S-CPW transmission line are given in Figure 1.6(a) and Figure 1.6(b) respectively. DUT alone is S-CPW transmission line without pad and accesslines simulated in Ansys HFSS and DUT measure is the realistic measurement model with pad and accessline. As shown in Figure 1.6, the characteristics of the device alone and the actual measurement device (before de-embedding) are different. It is because of the parasitic effects from the pad and the interconnecting lines. We need to mathematically eliminate these effects from the measurement to know the actual device characteristics of the DUT. There are different mathematical methods, which are used to eliminate these parasitics from the measurement that is called de-embedding. Here we present the de-embed results using a general two transmission lines de-embedding method (Mangan method [28], [41]), which is also shown in the Figure 1.6. It shows the variations with the DUT alone >60 GHz in magnitude of S_{21} and S_{11}. So we need to investigate or develop new methods to characterise devices at millimeter wave and sub-millimeter wave frequencies.

The simulation and the fabrication of components in the silicon technology include different Back End of Lines (BEOL) for different technologies [1], [11], [15]. Consider a general BEOL stack of a CMOS technology shown in Figure 1.7. This consists of several metal layers, which are submerged in multiple layers of dielectric material. The dielectric material may have different dielectric permittivities depending on each layer. The dimensions depend on the technology used.

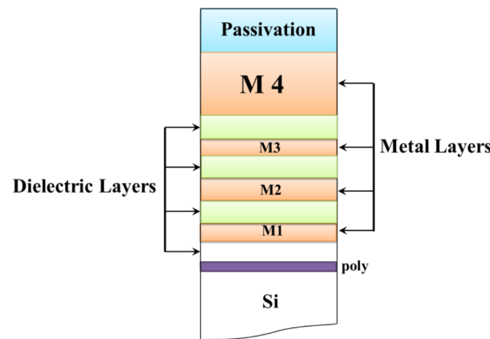


Figure 1.7. BEOL stacks of a Silicon Technology

The process variation and design rule densities of the silicon technologies can affect the electromagnetic modeling. In the electromagnetic modeling, we do not consider the metal density rules, and we use an effective dielectric permittivity of the substrate in the different stacks, this may create a variation in the electromagnetic design with the actual characteristics. This is not true in a modern CMOS process, where the permittivity can vary with the process. Generally, the materials used have a lower dielectric permittivity (ε_r) to reduce capacitive coupling between metal layers.

Actual CMOS processes require a certain percentage of metal in each metal layer. The Design Rule Check (DRC) checks these density rules. In order to satisfy the density requirements, most of the circuit is filled with metal-dummies. The metal-dummies can affect the performance and RF characteristics, which may introduce new parasitic effects and degradation in the quality factor of the passive structures by increasing the coupling losses at high frequencies. The other performance factors includes for a passive structure design is substrate conductivity, which increases the losses. Apart from the electromagnetic modelling, the major challenges for a millimeter-wave device characterisation are the measurement and the extraction of parasitic effects.

1.1.5 De-embedding and Challenges

The measurement model of device under test is shown in Figure 1.8. The DUT is connected with on-wafer interconnects and the pads for the measurement. Calibrating the vector network analyser, allows eliminating the effects of interconnects from VNA and probes, and setting the reference place at the probe tips. The measurement of the DUT includes the parasitic effects of the pads and interconnecting lines. These effects should be subtracted from the measured results to get the actual characteristics of the device. The process of mathematically removing the unwanted parasitic effects is

called "De-embedding" [26] -[44]. Thus, a de-embedding step must be performed to obtain the intrinsic parameters of the DUT. When we use the general calibration algorithms like Line-Reflect-Reflect-Match (LRRM), Thru-Reflect-Line (TRL), etc., the on-wafer de-embedding can often name as "On-Wafer Calibration". Generally, de-embedding is performed after the VNA calibration.

Similar to the calibration of the VNA, de-embedding is performed by measuring the various test structures like *Open, Short, Load, Line* and *Thru*, etc. depending on the method [25] - [40]. After De-embedding, the actual characteristic of the device is obtained. The reference plane de-embedding is shown in the Figure 1.8. Apart from the frequency and accuracy of the de-embedding method, it is important to use less number of de-embedding structures to reduce the cost. Also, it is important to reduce the number of steps to perform the de-embedding. A good de-embedding method should able to take care of the parasitic effects from the pads, interconnects and substrate coupling. Generally, a de-embedding method must be accurate, cost effective and reliable.

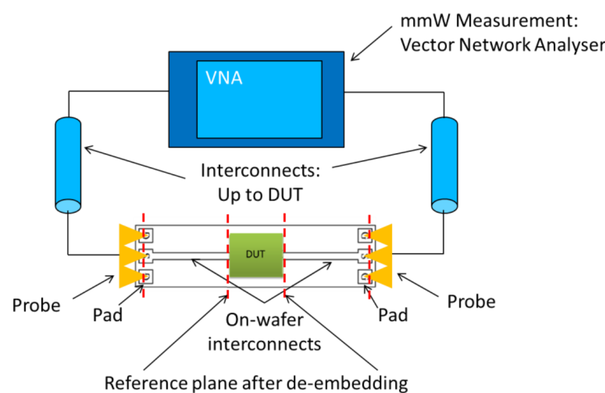


Figure 1.8. Measurement model: Reference plane after De-embedding

The de-embedding method can be modeled in many ways, like purely lumped, distributed microwave network parameter based, like *S, ABCD,* or *T-matrix* based on the combination of both lumped and distributed. Even different calibration techniques are also widely used to de-embed the parasitics. TRL is the most common and considered as a "standard" de-embedding/on-wafer calibration method [25], [26]. Considering the de-embedding methods, lumped de-embedding techniques were introduced first, in which the parasitic effects are considered as parallel and series lumped elements. This fundamental method is extended to "three-step" and improved "three-step" methods [30] - [33]. These methods are analysed from very low frequency to high frequencies. According to the frequency and the device model, there are different combinations of de-embedding structures are used, like *open*, *short* and *thru*. For higher frequencies, several steps of de-embedding have to be performed to achieve better characteristics of the device [27]. In the literatures, lumped methods are used for de-embedding both active and passive devices such as transistors, transmission lines, inductors, etc. [27]-[36]. Apart from lumped methods there are de-embedding methods based on distributed microwave network parameter based methods [37]-[40]. Mainly these methods consider the pad or pad interconnects

parasitics in to single to multiple cascaded based matrices. These types of methods are basically used to extract the characteristics of passive devices. TRL is considered as a cascaded matrix based method. Also, there are methods based on both lumped and distributed network based matrices [41] - [44]. These different types of methods and the limitations are explained in next chapter.

Nowadays there are many de-embedding methods available to de-embed the device. There are many de-embedding methods which will work for few “GHz” band. The important fact is that many methods are limited to the frequency. When the frequency increases to millimeter-wave, the parasitics cannot be localized only in to pad and interconnect. There are other parasitics associated with the on-wafer measurement environment, which can also affect measurement and de-embedding. Most of the de-embedding methods are investigated until millimeter wave frequencies, say 60 GHz to max 110 GHz. **Currently there are methods which can provide good de-embedding up to 100GHz. It is important to develop the de-embedding methods beyond 100GHz, because of the emerging applications in the range of millimeter wave and sub-millimeter wave frequencies.**

De-embedding methods have many limitations and challenges apart from the frequency limitation. The limitations of de-embedding methods are deeply involved in the test structures used, mathematical methods, and its mathematical limitations. Also on an on-wafer measurement, the parasitics are appearing not only from pads and interconnects from the DUT but there is also parasitics from the substrate, the adjacent cells, other coupling effects between probe-to-probe, probes to substrate, etc. In ideal, the parasitics are only from the pad and its interconnecting lines, but in an actual measurement of a device includes many adjacent devices as shown in Figure 1.9.

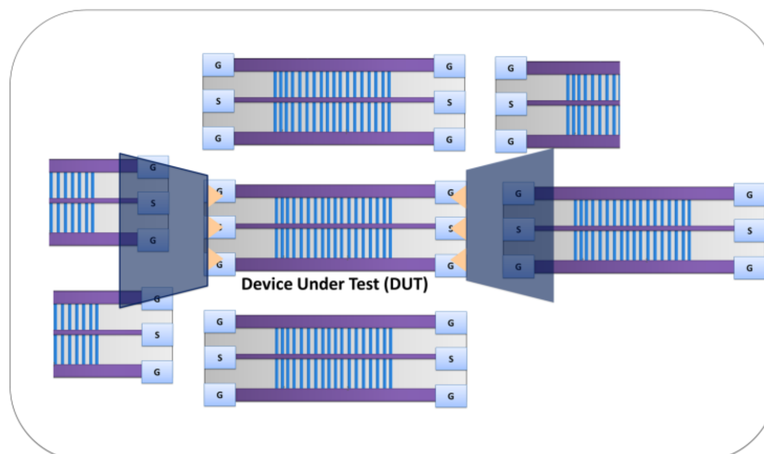


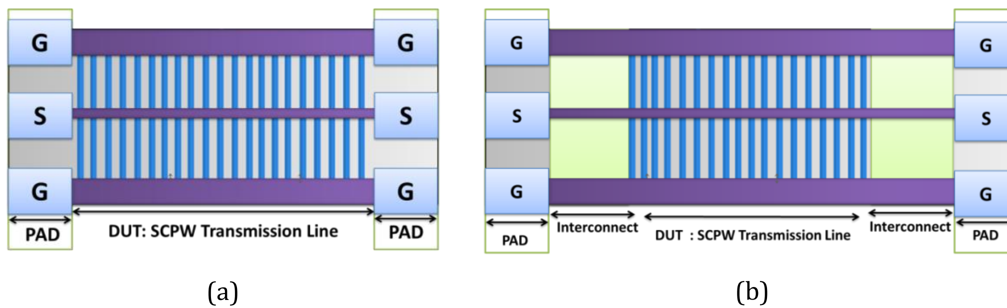
Figure 1.9. Actual measurement model of the DUT with adjacent devices

Generally, the calibration is performed until the probe tips. However, when you measure the DUT with probes, the probe can be coupled with substrate or can be coupled with other devices on the wafer. This creates other parasitic effects and losses [45]-[48]. Also the transition [40] from pad to interconnect and from the interconnect to DUT may make changes in the de-embedding. It is because

of the difference in the impedance at transition, further followed by a change in the parasitic variation, which may find difficult to calculate by de-embedding methods.

1.1.6 De-embedding with and without Interconnect/Accesslines

The measurement model of the DUT can be modeled in different ways. There are two kinds of de-embedding devices in the literature; (1) the DUT is directly connected to the PAD [41], [44], which is shown in Figure 1.10 (a), and (2) the DUT is connected to the PAD with interconnecting lines, which is shown in Figure 1.10(b) [32], [43].



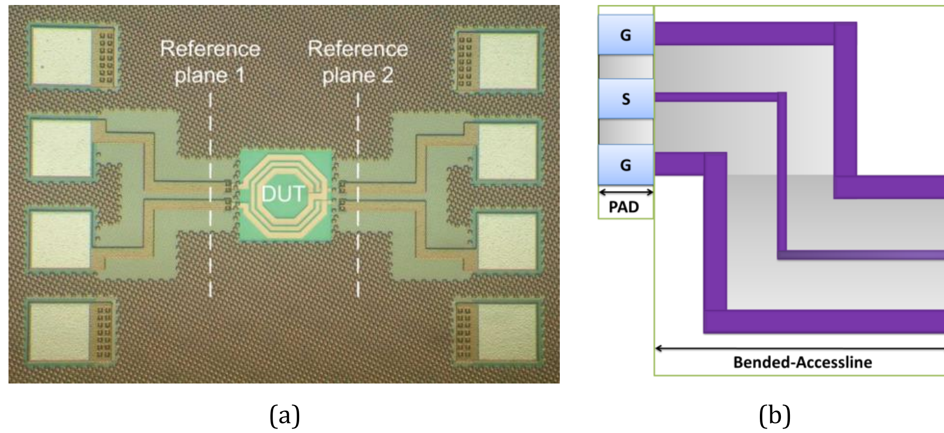
(a) (b)

Figure 1.10. (a) DUT: Directly connected to the PAD (b) DUT: Connected with both PAD and interconnect

These models can affect the de-embedding results. However, our DUT is a planar transmission line structure we can use either one of them. If we try to de-embed a transistor or any small passive device, it is necessary to have an accessline to avoid the cross coupling in the measurement and to establish the correct EM propagation mode. **Until now, there is no proper definition for a de-embedding measurement model in transmission line de-embedding. It is important to understand whether the direct connection/interconnect parasitics affects the transmission line de-embedding at millimeter wave frequencies or not.**

1.1.7 Bended-Accessline De-embedding

Bended-accesslines are used to interconnect the devices [49]. Mainly 4-port DUTs use Bended-accessline, an example is shown in Figure 1.11(a). The bended-accessline structure is shown in Figure 1.11(b). These kinds of lines are difficult to de-embed for very high frequency. Presently, lumped methods and TRL are used to de-embed these lines. Lumped methods are limited to the lower frequencies. The unknown line parameter (characteristic impedance) and the fact that more than one line is required to cover the entire frequency band up to millimeter wave are the disadvantages of TRL method. This increases the area and cost, so there is a need for better de-embedding method, which is applicable for these kinds of accesslines.

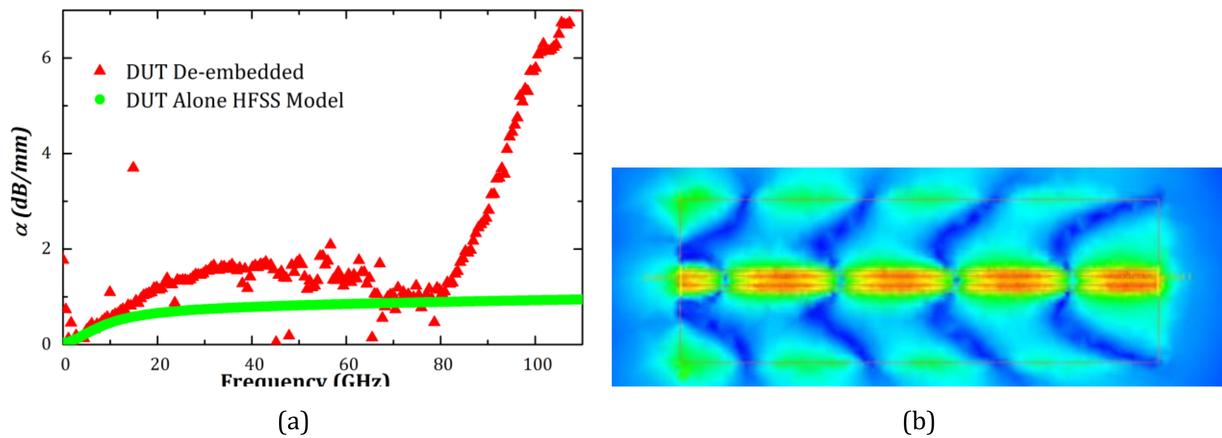


(a) (b)

Figure 1.11. (a) Bended-Accessline used in a 4-port DUT [49] (b) Model of Bended-Accessline

1.1.8 Excessive Losses at Millimeter Wave Frequencies and Above

The studies by A.L. Franc [11] identified the excessive loss happening for measurement above 60GHz for S-CPW. In most of the de-embedding methods, it remains the same. The methods are not able to take care of this specific problem. In addition, the same problem exists in the CPW transmission line (DUT De-embedded) and homogenous CPW transmission line (DUT Alone HFSS Model) as shown in Figure 1.12(a).



(a) (b)

Figure 1.12. (a) Attenuation of a CPW de-embedded line and CPW HFSS model (b) Parallel plate propagation in a CPW line [47]

The major reasons for the excessive loss are higher order modes, which introduces additional propagation of electromagnetic waves, into the lossy substrate, and to the adjacent devices. These propagations may happen with the potential difference of the probe and the conductors on the substrate. This introduces the parallel plate propagation [46], [47] as shown in Figure 1.12(b).

At low frequencies, the conventional transmission line supports quasi-TEM mode but at higher frequencies, these non-TEM modes may induce extra losses [14]. These losses are additive phenomena, apart from the normal conductive and dielectric losses. Thus, one of the important goal of this thesis is to analyse and identify the reasons and suggests the solutions for this problem.

1.1.9 Other Measurement Challenges

The results of the recent studies explain that there can be a possibility of coupling due to the adjacent structures on on-wafer measurement [48], [50]-[52] (see Figure 1.13).

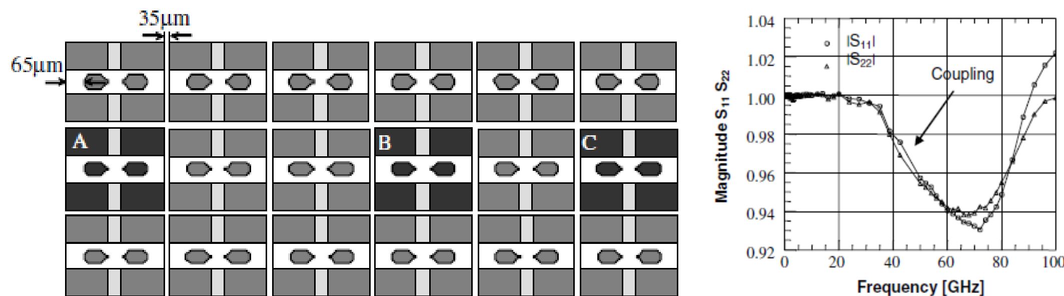


Figure 1.13. Measurement model: problem of adjacent cell coupling [48]

This shows a strong coupling from the adjacent cells near the DUT. All the studies show a strong influence from the substrate and the adjacent cells. There are different solutions to avoid the coupling between the adjacent cells. The best solution is to separate the adjacent cells far as about >250 µm, which is practically impossible, because of the large area required on the wafer and increased cost.

Apart from measurement and de-embedding challenges, on-wafer measurement environment and calibration can affect the accuracy of the de-embedding and characterization of the device. This explains in the section of on-wafer measurement and challenges at millimeter wave frequencies.

1.1.10 Conclusion of State of the Art and Problem Description

Section 1.1 explains the state of the art and the problem description. With the technology advances and applications in millimeter wave and sub-millimeter wave frequency makes the devices smaller. Thus, measurement and characterization of these devices are important to ensure the best performance. Generally, a device (in our case: S-CPW transmission line) on wafer cannot be measured easily. DUT requires additional parasitics such as pad and interconnects for measurement. To know the actual characteristics of the device, the parasitics should be removed mathematically, this is called de-embedding. But current de-embedding methods are limited by frequency. **Beyond 100 GHz, still there are methods to investigate and develop for the future, because of the large number of applications at millimeter wave and sub-millimeter wave band**. A new de-embedding method faces many challenges at this frequency. We describe the problem of different type of interconnecting line for example bended-accessline. In the measurement, there are other problems such as the excessive loss at higher frequencies and the coupling between the adjacent measurement cells, etc. These make DUT characterization and de-embedding at millimeter wave frequencies and above highly challenging.

1.2 On-Wafer Measurement and Challenges at Millimeter Wave Frequencies

De-embedding and characterization challenges are not only limited to the DUT, different type of interconnecting lines and adjacent devices problems. The characterization of the DUT beyond millimeter wave frequencies may affect the environment of the on-wafer measurement, such as on-wafer measurement setup, probes, the calibration substrate and algorithm. On-wafer measurement setup of a "complex system" is shown in Figure 1.14. This is developed by Cascade Microtech [53]. This system includes Probe station, VNA, measurement device on wafer, probes for measurement and interconnecting cables. The probe station also includes the on-wafer test chunks, micro-chamber, probe positioner for the positioning of the test wafer with DUT, microscope for viewing the test DUT, and other system controls. VNA used to measure the electromagnetic signals from the DUT and probes used for the measurement of the DUT.

Figure 1.14. On-Wafer Measurement Setup (Cascade Microtech Probe Station)

The simplified on-wafer measurement of a passive device (transmission line) is shown in Figure 1.15. This includes VNA, interconnects to the DUT, and the probes for the measurement. Generally the device is fabricated on a silicon wafer along with other devices. Considering the complexity of the system, the accurate measurement requires many corrections in the measuring setups and measured data [23].

Consider the above measurement setup of the DUT as shown in the Figure 1.15. To get the accurate measurement of the DUT, we need to eliminate the major errors occurring from the measurement setup, such as

- Error from the cables, which are using to connect the VNA
- Errors from the Pad and Interconnects
- Coupling between the Probes

Calibration of the VNA will eliminate the errors till the probe tips [54]-[56]. To eliminate the pad, interconnect errors and the coupling between the probes, we have to apply certain mathematical corrections called de-embedding, which are explained earlier.

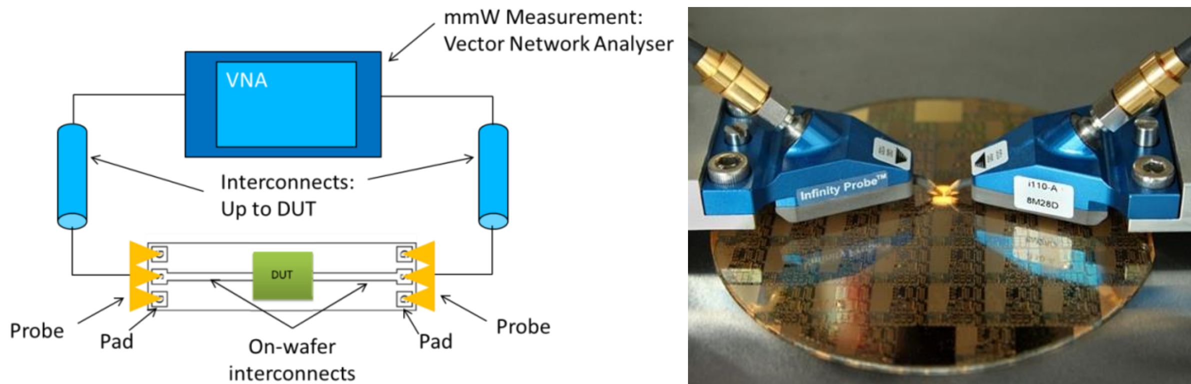


Figure 1.15. Simplified measurement setup of a device under test

1.2.1 Calibration and Challenges

Calibration is defined as the "set of operations that establish under specified conditions, the relationship between values of quantities indicated by a measuring instrument or measuring system, or values represented by a material measure or a reference material, and the corresponding values realized by standards" [57]. Calibration is critical for a VNA to make good S-parameter measurements [54]. Calibrating the VNA with standards at the probe tips allows to remove the repeatable errors from the VNA, cable, and probe losses and reflections. The calibration process utilizes the technique of vector error correction, in which error terms are calculated from measurement of known standards, these errors can be removed from actual measurements. There are different types of possible calibration algorithms that are available according to the number of error terms, and type of standards used to perform the calibration. Many of them are implemented within VNAs. SOLT, LRM, LRRM, and TRL are the four most commonly used wafer probe calibrations [54], [59]-[63]. In the case of on-wafer measurement, we perform calibration on the probe tip. After the calibration, the reference plane is moved to the end of the probe tip, which is shown in the Figure 1.16(a). Cascade Microtech utilizes LRRM method for probe tip calibration. The Figure 1.16(b) describes LRRM calibration that can be comparable with TRL calibration methods. While the frequency increases, the parasitics due to the environment is important, including the mechanical support on which the calibration set and the wafer is placed [64].

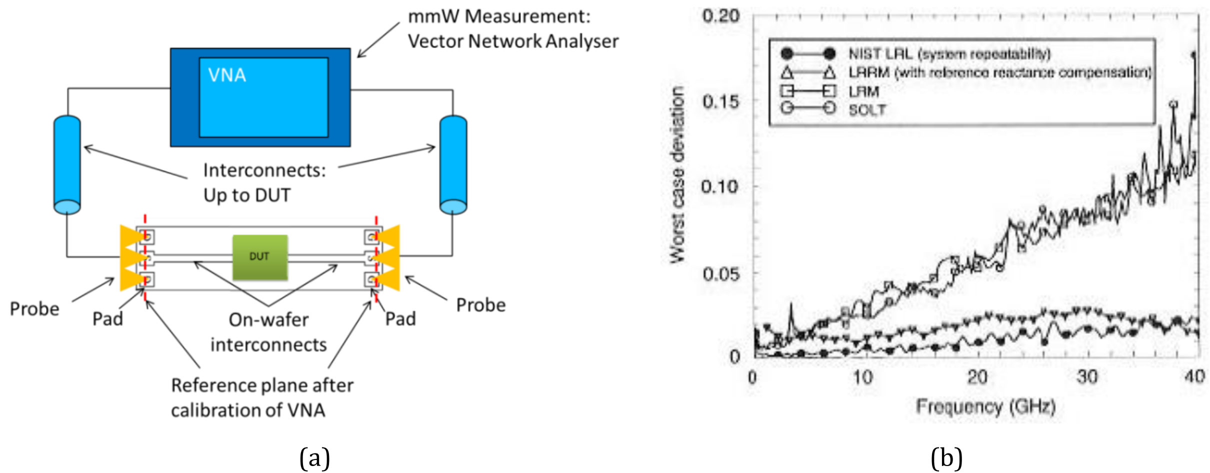


Figure 1.16. (a) Measurement set up: Calibration reference of the Vector Network Analyser (b) Comparison of probe tip calibration methods [56]

Contact substrate and calibration substrate are also used in calibration procedure. [58]. Calibration substrate or Impedance Standard Substrate (ISS) is used to perform the standard measurements and obtain the error terms for calibration. ISS uses alumina as a substrate because of its low loss characteristics. The commonly used calibration standards are *open, short, load, thru*, and *line* standards. These standards are often realized in the CPW design. Calibration accuracy depends on the calibration method, the probes used, probe tip physical placement accuracy and the ISS used.

1.2.2 RF Probes

There are different types of RF probes (shown in the Figure 1.17) available according to their use and frequency of operation. The features of a probe include the coaxial connector, probe body, probe tip, and the contacts at the probe tip end. The transition from coaxial line to a conventional transmission line is made within the probe. Since the electric field distributions are different from coaxial to the conventional transmission line used in the probe tip, the only difficulty is the transition at high frequencies. A good wafer probe has a good matching between the coax-conventional probe tips, and proper conversion of the electromagnetic energy between different propagation modes. For a good DUT measurement the electric field patterns at the probe tip are similar to the field patterns in the DUT and then there will be minimum parasitic coupling to the probe [65]-[68].

When high frequency probes are used for on-wafer measurement it is important that what is measured at the probe tips contact. This includes the parasitics from pad, and other parasitics associated with the on-wafer interconnects and other devices on your substrate. Measurements are sensitive to contact resistance by the probe tip. Conventionally tungsten tips are used in the RF probes, but tungsten tips increase the contact resistance with aluminium pad, because tungsten oxidizes and the aluminium easily accumulates on the probe tips. This results in poor measurement repeatability. A poor on-wafer probing causes more implications like inconsistent measurements, contact resistance

issues, often re-probing, and pad damage. It limits the re-probing, increase of the number of tests, time, cost and reduction in productivity. So considering the on-wafer measurement the major challenges for RF probes can be described as,

- Frequency limitations of the probe
- High measurement accuracy, reliability and repeatability
- Stable contact resistance between the probe tip and the pad, it should be very low for better performance
- Good crosstalk characteristics
- Less unwanted coupling between probe and the wafer, probe and the nearest devices

The three major RF probes are described by considering the frequency of usage, different applications and the probe tip configuration (See Figure 1.17).

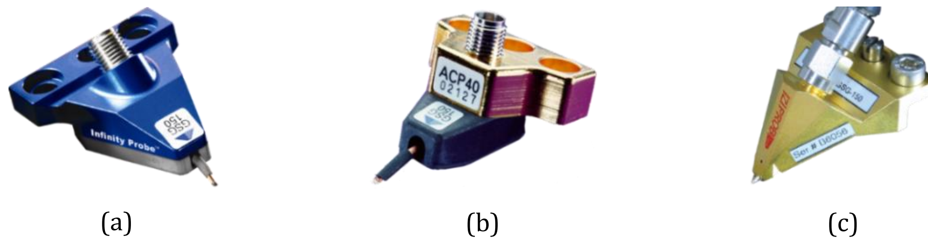


Figure 1.17. Different types of RF probes (a) Infinity Probe (b) Air Coplanar Probe (ACP) (c) |Z| Probe

Infinity probe: The model of the Infinity probe is shown in the Figure 1.17(a). Infinity probes are developed for high frequency characterizations of the RF devices. Infinity probe uses microstrip transmission lines to carry the signal between the co-axial connector to the probe tips. The transmission lines on the Infinity thin-film technology gives more confined fringing fields than conventional coplanar tips. The contact area of the probe tip is 12x12 μm

Air Coplanar Probe (ACP): The model of Air Coplanar Probe is shown in the Figure 1.17(b). The Air Coplanar Probe is a rugged microwave probe with a compliant tip for accurate and repeatable measurements on-wafer [67]. Air Coplanar Probes have excellent probe-tip visibility, lowest loss and good electrical performance.

|Z| Probe: The model of the |Z| Probe is shown in the Figure 1.17(c). It has a robust design for coplanar structures with long probe lifetime. The |Z| Probe has high impedance control with perfectly symmetrical coplanar contact structure, which eliminates the signal distortion. In |Z| probe the RF/Microwave signal is shielded and completely air isolated in the probe body which gives excellent performance even in vacuum environments.

Comparisons between three major RF probes are described in Table 1.1

Infinity Probes	Air Coplanar Probes	|Z| Probes
▪ From 40GHz to 325 GHz ▪ Low contact resistance, < 0.05 Ω on Al, < 0.02 Ω on Au ▪ High RF measurement accuracy and Highly reliable ▪ Reduced unwanted couplings to nearby devices and transmission modes ▪ Excellent crosstalk characteristics ▪ Only on-wafer/planar surface ▪ Maximum temperature 125°C ▪ Typical probe life time > 250,000	▪ From DC to 110 GHz ▪ Approximately 0.1 Ω on Al ▪ Stable and repeatable over-temperature measurements ▪ May be couplings to nearby devices and transmission modes because of coplanar structure ▪ Excellent crosstalk characteristics ▪ Great compliance for probing non-planar surface ▪ Temperature from -65 ° C to + 200° C ▪ Typical probe life time > 500,000	▪ From DC to 67 GHz ▪ Low contact resistance ~ 0.05 Ω on Al ▪ High-accuracy measurements ▪ May be couplings to nearby devices and transmission modes because of coplanar structure ▪ Excellent crosstalk characteristics ▪ Both planar and non-planar surface ▪ Maximum temperature 300° C ▪ Typical probe life time > 1,000,000

Table 1.1 Comparison between different RF Probes

1.3 Conclusion

The environment of on-wafer measurement including RF probes, calibration algorithms and calibration substrate can affect the device de-embedding and characterization.

In RF/Microwave/Millimeter-Wave circuit design, the characterization and de-embedding of the transmission line over millimeter and sub-millimeter wave frequencies are critical**. As we explained above, currently there are good de-embedding methods, which will work for lower frequency and up to 100GHz.** There are methods to **investigate and develop beyond 100 GHz** for the future, because of the large number of applications at millimeter wave and sub-millimeter-wave band. A good de-embedding method should eliminate all the parasitics. It should be accurate over wide band, reliable and cost effective. There are excessive losses at higher frequencies possibly due to higher order modes, surface waves, parallel plate propagation, and coupling, etc. So we need to investigate a good on-wafer model which can be free from all these unwanted parasitics, hence we can improve the measurement accuracy and able to characterize a device properly.

Next chapter reviews and benchmarks the current de-embedding methods. The chapter classifies and explains the current de-embedding methods according to various types, the size of the DUT and the range of the frequency. The chapter benchmarks all the de-embedding methods, by considering both electrical (controlled parasitics) and 3D EM simulation tool Ansys HFSS (realistic parasitics). The chapter also explains different limitations and different characteristics needed for a good de-embedding method for a wide band up to millimeter wave and sub-millimeter wave frequency range.

1.4 References

[1] A. Cathelin and J. J. Pekarik, “Silicon Technologies to Address mm-Wave Solutions,” in *mm-Wave Silicon Technology*, A. M. Niknejad and H. Hashemi, Eds. Springer US, pp. 25–57, 2008.

[2]A. Hamidian, “60 GHz transceiver circuits in SiGe-HBT and CMOS technologies.”, phdthesis, Technischen Universität Berlin, 2014

[3] D. M. Pozar, “Microwave Engineering”, 4th Edition Dec. 2011.

[4] R.Orta, “Lecture Notes on Transmission Line Theory”, Nov. 2012.

[5] D. D. Grieg and H. F. Engelmann, “Microstrip-A New Transmission Technique for the Klilomegacycle Range,” *Proc. IRE*, vol. 40, no. 12, pp. 1644–1650, Dec.1952.

[6] Jia-Sheng Hong, M. J. Lancaster, “ Microstrip Filters for RF / Microwave Applications”, 2nd Edition, Dec .2001

[7] I. J. Bahl and D. K. Trivedi, “A Designer’s Guide to Microstrip Line,” *Microwaves*, pp. 174–182. May 1977.

[8] C. P. Wen,‘‘Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Applications,’’ *IEEE Trans. Microwave Theory Tech.*,Vol. 17, No. 12, pp. 1087-1090,Dec. 1969.

[9] R.N. Simons “Coplanar Waveguide Circuits, Components, and Systems”, *Wiley-IEEE Press*, April. 2001.

[10] R. E. Collin, “Foundations for Microwave Engineering”, 2nd Edition., Dec. 2000.

[11] A.-L. Franc, “Lignes de propagation intégrées à fort facteur de qualité en technologie CMOS. Application à la synthèse de circuits passifs millimétriques,” phdthesis, Université de Grenoble, 2011.

[12] D. Kaddour, H. Issa, A.-L. Franc, N. Corrao, E. Pistono, F. Podevin, J. M. Fournier, J. Duchamp, and P. Ferrari, “High-Q Slow-Wave Coplanar Transmission Lines on 0.35 m CMOS Process,” *IEEE Microw. Wirel. Compon. Lett.*, vol. 19, no. 9, pp. 542–544, Sep. 2009.

[13] A.-L. Franc, E. Pistono, and P. Ferrari, “Design guidelines for high performance slow-wave transmission lines with optimized floating shield dimensions,” in *Microwave Conference (EuMC), 2010 European*, pp. 1190–1193, 2010.

[14] Ø. Bjørndal, “Millimeter wave interconnect and slow wave transmission lines in CMOS,” Masters thesis, Universitetet i Oslo, 2013.

[15] F. Burdin, “Nouvelles Topologies des diviseurs de puissance, balun et déphaseurs en bandes RF et millimétiques, apport des lignes à ondes lentes,” phdthesis, Université de Grenoble, 2013.

[16] ANSYS® HFSS, Release 14.0, ANSYS, Inc.

[17] H. P. Hsu, “On The General Relation Between /spl alpha/ and Q (Correspondence),” *IEEE Trans. Microw. Theory Tech.*, vol. 11, no. 4, pp. 258–258, Jul. 1963.

[18] K. Ma, S. Mou, and K. S. Yeo, “Miniaturized 60-GHz On-Chip Multimode Quasi-Elliptical Bandpass Filter,” *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 945–947, Aug. 2013.

[19] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, “Millimeter-wave CMOS design,” *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[20] A.-L. Franc, E. Pistono, D. Gloria, and P. Ferrari, “High-Performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Bandpass Filters,” *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1219–1226, May 2012.

[21] X. Tang, “Apport des lignes à ondes lentes S-CPW aux performances d’un front-end millimétrique en technologie CMOS avancée,” phdthesis, Université de Grenoble, 2012.

[22] A.-L. Franc, E. Pistono, N. Corrao, D. Gloria, and P. Ferrari, “Compact high-Q, low-loss mmW transmission lines and power splitters in RF CMOS technology,” in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, pp. 1–4, 2011.

[23] G. Crupi, D. Schreurs, “Microwave De-embedding From Theory to Applications", 1st Edition, Nov. 2013.

[24] S. Gharavi and B. Heydari, “mm-Wave Device Modeling,” in *Ultra High-Speed CMOS Circuits*, Springer New York, pp. 5–21, 2011.

[25] G. F. Engen and C. A. Hoer, “Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer,” *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 12, pp. 987–993, Dec. 1979.

[26] D. F. Williams, P. Corson, J. Sharma, H. Krishnaswamy, W. Tai, Z. George, D. S. Ricketts, P. M. Watson, E. Dacquay, and S. P. Voinigescu, “Calibrations for Millimeter-Wave Silicon Transistor Characterization,” *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 3, pp. 658–668, 2014.

[27] B. Zhang, Y. Xiong, L. Wang, S. Hu, and J. L.-W. Li, “On the De-Embedding Issue of Millimeter-Wave and Sub-Millimeter-Wave Measurement and Circuit Design,” *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 2, no. 8, pp. 1361–1369, 2012.

[28] A. M. Mangan, “Millimetre-Wave Device Characterization for Nano-CMOS IC Design.”, Masters thesis, University of Toronto, 2005

[29] R.F. Bauer and P. Penfield, “De-Embedding and Unterminating,” *IEEE Trans. Microw. Theory Tech.*, vol. 22, no. 3, pp. 282–288, Mar. 1974.

[30] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, “An improved de-embedding technique for on-wafer high-frequency characterization,” in *Bipolar Circuits and Technology Meeting, 1991., Proceedings of the 1991*, pp. 188–191, 1991.

[31] H. Cho and D. E. Burk, “A three-step method for the de-embedding of high-frequency S-parameter measurements,” *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1371–1375, June 1991.

[32] T. E. Kolding, “A four-step method for de-embedding gigahertz on-wafer CMOS measurements,” *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 734–740, April 2000.

[33] E. P. Vandamme, D. M. M. Schreurs, and C. van Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 737–742, April 2001.

[34] L. F. Tiemeijer, R. M. T. Pijper, J. a. van Steenwijk, and E. van der Heijden, "A New 12-Term Open–Short–Load De-Embedding Method for Accurate On-Wafer Characterization of RF MOSFET Structures," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 2, pp. 419–433, Feb. 2010.

[35] I. M. Kang, S. Jung, T. Choi, J. Jung, C. Chung, H. Kim, H. Oh, H. W. Lee, G. Jo, Y. Kim, H. Kim, and K. Choi, "Five-Step (Pad–Pad Short–Pad Open–Short–Open) De-Embedding Method and Its Verification," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 398–400, Apr. 2009.

[36] N. Waldhoff, C. Andrei, D. Gloria, S. Lepilliet, F. Danneville, and G. Dambrine, "Improved Characterization Methology for MOSFETs up to 220 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1237–1243, May 2009.

[37] X. S. Loo, K. S. Yeo, K. W. J. Chew, L. H. K. Chan, S. N. Ong, M. a. Do, and C. C. Boon, "A New Millimeter-Wave Fixture Deembedding Method Based on Generalized Cascade Network Model," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 447–449, Mar. 2013.

[38] C. Hu, S. B. Jan, and M. F. Chen, "TSV RF de-embedding method and modeling for 3DIC," *2012 SEMI Adv. Semicond. Manuf. Conf.*, pp. 394–397, May 2012.

[39] X. S. Loo, K. S. Yeo, K. W. J. Chew, L. H. K. Chan, S. N. Ong, M. a. Do, and C. C. Boon, "A Cascade-Parallel Based Noise De-Embedding Technique for RF Modeling of CMOS Device," *IEEE Microw. Wirel. Components Lett.*, vol. 21, no. 8, pp. 448–450, Aug. 2011.

[40] R. Torres-Torres, G. Hernandez-Sosa, G. Romo, and A. Sanchez, "Characterization of Electrical Transitions Using Transmission Line Measurements," *IEEE Trans. Adv. Packag.*, vol. 32, no. 1, pp. 45–52, Feb 2009.

[41] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb 2006.

[42] B. Zhang, Y.-Z. Xiong, L. Wang, L. Teck-Guan, Y.-Q. Zhuang, L.-W. Li, and X. Yuan, "On the accuracy of de-embedding technologies for on-wafer measurement up to 170GHz," in *IEEE International Symposium on Radio-Frequency Integration Technology, RFIT 2009*, 2009, pp. 284–287, 2009.

[43] Y. N. Yosuke Goto, "New On-Chip De-Embedding for Accurate Evaluation of Symmetric Devices," *Jpn. J. Appl. Phys.*, vol. 47, pp. 2812–2816, 2008.

[44] N. Li, K. Matsushita, N. Takayama, S. Ito, K. Okada, and A. Matsuzawa, "Evaluation of a Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design," *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.*, vol. E93-A, no. 2, pp. 431–439, Feb. 2010.

[45] G. N. Phung, F. J. Schmuckle, and W. Heinrich, "Parasitic effects and measurement uncertainties in multi-layer thin-film structures," in *Microwave Conference (EuMC), 2013 European*, pp. 318–321, 2013.

[46] Schmiickle, F.J., R. Doerner, G.N. Phung, W. Heinrich, D. Williams, and U. Arz. "Radiation, Multimode Propagation, and Substrate Modes in W-Band CPW Calibrations." In *Microwave Conference (EuMC), 2011 41st European,* 297–300, 2011.

[47] M. Spirito, G. Gentile, and A. Akhnoukh, "Multimode analysis of transmission lines and substrates for (sub)mm-wave calibration," in *Microwave Measurement Conference, 82nd ARFTG*, pp. 1–6, 2013.

[48] J. Bazzi, "Caractérisation des transistors bipolaires à hétérojonction SiGe à très hautes fréquences," Thèse de doctorat, Laboratoire d'Intégration du Matériau au Système, France, 2011.

[49] M. Wojnowski, V. Issakov, G. Sommer, and R. Weigel, "Multimode TRL Calibration Technique for Characterization of Differential Devices," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 7, pp. 2220–2247, Jul. 2012.

[50] G. N. Phung, R. Doerner, F. J. Schmuckle, and W. Heinrich, "On parasitic coupling in CPW structures," in *Microwave Conference (GeMiC), The 7th German*, pp. 1–4, 2012.

[51] M. Potereau, C. Raya, M. D. Matos, S. Fregonese, A. Curutchet, M. Zhang, B. Ardouin, and T. Zimmer, "Limitations of On-Wafer Calibration and De-Embedding Methods in the Sub-THz Range," *Comput. Commun.*, vol. 01, no. 06, pp. 25–29, 2013.

[52] C. Andrei, D. Gloria, F. Danneville, P. Scheer, and G. Dambrine, "Coupling on-wafer measurement errors and their impact on calibration and de-embedding up to 110 GHz for CMOS millimeter wave characterizations," in *IEEE International Conference on Microelectronic Test Structures, ICMTS '07*, 2007, pp. 253–256, 2007

[53] Cascade Microtech, "Complete RF Microwave probing solutions for every application," Application note, 2006

[54] A. Rumiantsev and N. Ridler, "VNA calibration," *IEEE Microw. Mag.*, vol. 9, no. 3, pp. 86–99, Jun. 2008.

[55] G. Fisher, "A guide to Successful on Wafer Rf characterisation", Application note, 2007

[56] D. F. Williams and R. B. Marks, "Calibrating On-Wafer Probes to the Probe Tips," in *ARFTG Conference Digest-Fall, 40th*, vol. 22, pp. 136–143, 1992.

[57] "International Vocabulary of Basic and General Terms Used in Metrology", 2nd Ed. *International Organization for Standardization,* Geneva, Switzerland, 1993.

[58] Cascade Microtech, "Impedance Standard Substrates to support all of your high-frequency probing applications", Application note, 2-3, 2007

[59] Cascade Microtech "On-Wafer Vector Network Analyzer Calibration and Measurements", Application note, 2002

[60] Cascade Microtech, "A Guide to Better Vector Network Analyzer Calibrations for Probe-Tip Measurements", Technical brief, 2002

[61] L. Hayden, "A Hybrid Probe-Tip Calibration for Multiport Vector Network Analyzers", *IEEE 68th ARFTG,* Dec.2006

[62] F. Purroy, L. Pradell, "New theoretical analysis of the LRRM calibration technique for vector network analyzers," *IEEE Trans. Instrum. Meas.*, vol. 50, no. 5, pp.1307-1314, Oct. 200l.

[63] L. Hayden, “An enhanced Line-Reflect-Reflect-Match calibration,” in *ARFTG Conference, 2006 67th*, pp. 143–149, 2006.

[64] A. Rumiantsev, R. Doerner, and E. M. Godshalk, “The influence of calibration substrate boundary conditions on CPW characteristics and calibration accuracy at mm-wave frequencies,” in *Microwave Measurement Symposium, 2008 72nd ARFTG*, pp. 168–173, 2008.

[65] A. Rumiantsev, “On-Wafer Calibration Techniques Enabling Accurate Characterization of High-Performance Silicon Devices at the mm-Wave Range and Beyond”,phdthesis, Brandenburgische Technische Universität Cottbus-Senftenberg, 2014.

[66] Cascade Microtech, “Mechanical Layout Rules for Infinity Probes.”, Application note,2006

[67] Cascade Microtech, “High-frequency performance with low, stable contact resistance on aluminum pads”, Application note, 2002

[68] Cascade Microtech, “High-frequency probes for every application, Application note, 2006.

2. De-embedding Methods

This chapter reviews and benchmark the current de-embedding methods. It includes classification according to the de-embedding strategies and explanation of de-embedding methods. These methods are utilized to de-embed the devices, according to the size of the DUT and the range of frequency. Each classification of methods is explained and proved by using both known and realistic parasitics. Known pad/interconnect parasitics are modeled using ADS by considering pad parasitics from ST BiCMOS 55 nm technology. Different levels of parasitics models are tested for these de-embedding methods, they are benchmarked by considering a lossless transmission line as DUT. The realistic parasitics are modeled using 3D EM simulation tool Ansys HFSS by considering S-CPW transmission line as a DUT in ST BiCMOS 55 nm technology. Finally, the chapter benchmarks all the de-embedding methods and concludes on the different limitations and characteristics needed for a good de-embedding method in millimeter wave and sub-millimeter wave frequency range.

2.1 Classification of De-embedding Methods

In the present scenario, there are different types of methods available to characterize the devices. De-embedding methods are categorized into different topologies according to the methodology. To know the actual characteristic of the device, the parasitic effect of the pad and on-wafer interconnects must be de-embed using these methods. Thus, a de-embedding step must be performed to obtain the intrinsic parameters of the DUT. These de-embedding methods [1]-[19] induce modifications of the design of passive and active circuits in the millimeter and sub-millimeter frequencies. Today, no solution provides a reliable and reproducible measurement of circuits in the silicon integrated technology for millimeter wave and sub-millimeter wave frequencies, especially beyond 100 GHz [3]. As we mentioned in the state of the art, with increased number of applications in the millimeter wave and sub-millimeter wave frequencies, it is important to have a performant de-embedding method to characterize the devices. Indeed, at these frequencies, environmental measure around the DUT is very critical and the effects of the pads and the substrate are no longer simple localized parasitic elements.

The de-embedding methods can be classified [3] into three types according to their de-embedding strategy.

- **Lumped Equivalent Circuit Model**
- **Cascaded Matrix Based Model**
- **Cascaded Matrix with Lumped Equivalent Models**

2.1.1 Lumped Equivalent Circuit Model

Lumped Equivalent Circuit Model [3]-[8] is used to de-embed the pad with or without feeding line lengths very small compared to the considered wavelengths. In the lumped circuit equivalent method the parasitic effects of the pads and interconnects are modeled as lumped elements as exhibited, for example, in [3]-[8] and shown in Figure 2.1(b). Figure 2.1(a) shows the parasitics to be de-embed using these methods. Hence, this method of de-embedding is especially effective to de-embed the devices at low frequencies. In this method the parasitic of the pads are modeled as capacitive effect and the on-wafer feeding lines (transmission line) which are used to interconnect the DUT is approximated by inductive parasitics [4]. The coupling between the probes and interconnects of the DUT has been taken care of, because this method mainly utilizes to de-embed short DUTs.

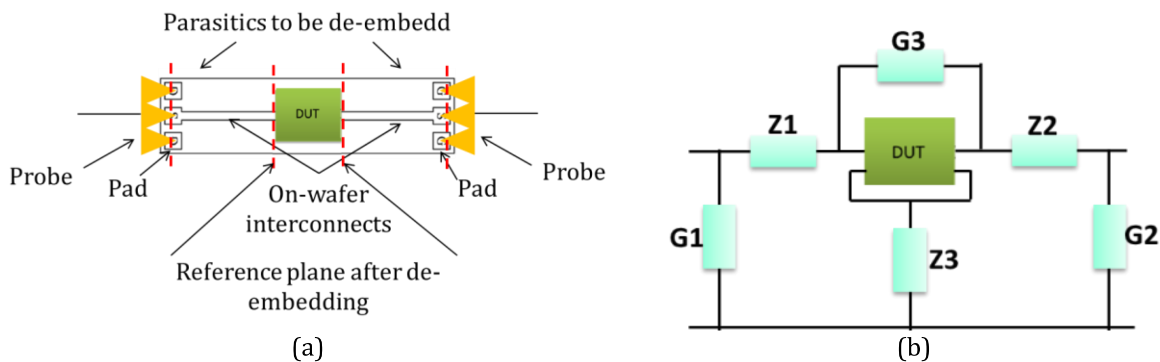


Figure 2.1. DUT De-embedding Model (a) Parasitics to be de-embed (b) Lumped Equivalent Circuit Model [4]

The important lumped equivalent circuit model methods are described below.

2.1.1.(a). Open De-embedding

Open de-embedding methodology [3], [7], [8] is simplest de-embedding method and used for low frequency range. Open de-embedding uses only "*Open*" de-embedding structure. In this method, the parasitics are modeled as parallel lumped elements. The intrinsic DUT is obtained from the following equation.

$$Y_{DUT} = Y_{Measure} - Y_{Open} \tag{2.1}$$

where, Y_{DUT} is the admittance matrix of the DUT, $Y_{Measure}$ is the DUT measured with the parasitics and Y_{Open} is the *open* de-embedding structure measured. Open de-embedding method can only de-embed the parallel parasitics. Any series parasitics which are present in the pad or interconnect can affect the accuracy of the de-embedding.

2.1.1.(b). Open-Short De-embedding

Open-Short de-embedding methodology [3], [7], [8] is an advanced method of open de-embedding. It uses both "*Open*" and "*Short*" de-embedding structure. In this method, the parasitics are modeled as

both parallel and series lumped elements. The intrinsic DUT is obtained from the following de-embedding steps.

$$Y_{OpenPad} = Y_{Measure} - Y_{Open} \tag{2.2}$$

$$Y_{ShortPad} = Y_{Short} - Y_{Open} \tag{2.3}$$

$$Y_{DUT} = \left(\left(Y_{OpenPad}\right)^{-1} - (Y_{ShortPad})^{-1}\right)^{-1} \tag{2.4}$$

where, Y_{DUT} is the admittance matrix of the DUT, $Y_{Measure}$ is the DUT measured with the parasitics, Y_{Open} is the *open* de-embedding structure measured and Y_{Short} is the *short* de-embedding structure measured. This method can de-embed both the parallel and series parasitic elements.

2.1.1.(c). Vandamme De-embedding Method

Vandamme de-embedding method [4] is an improved three step lumped element method. The parasitics are modeled as series and parallel lumped elements shown in Figure 2.2(a). Vandamme de-embedding method uses *Thru*, *Open*, and two different *Shorts* (*Short1* and *Short2*) as de-embedding structures, which are shown in Figure 2.2(b) to Figure 2.2(e).

The series and parallel parasitics can be determined by easily solving the de-embedding structures. The values of Z_1, Z_2, Z_3, G_1, G_2 and G_3 are obtained byusing the circuits detailed in Figure 2.2(b) to Figure 2.2(e). The model assumption for performing the Vandamme method is,

$$\frac{1}{G_3} + Z_x >> Z_3 \tag{2.5}$$

where, Z_x = Z_1 *or* Z_2. where the ratio $\frac{1}{G_3} + Z_x \Big/ Z_3$ decreases with frequency. However, it should be always greater than 60. Once this assumption is correct, the de-embedding steps can be performed, which is described below step-by-step [4]. First step is to eliminate the parallel admittances G_1 and G_2 from the measurement.

$$Y_A = Y_{meas} - \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \tag{2.6}$$

Convert the Y_A can be into impedance matrix Z_A, and remove the effects induced by Z_1, Z_2 and Z_3.

$$Z_B = Z_A - \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix} \tag{2.7}$$

Convert the Z_B matrix into admittance matrix to remove coupling between the two ports G_3,

$$Y_{DUT} = Y_B - \begin{bmatrix} G_3 & -G_3 \\ -G_3 & G_3 \end{bmatrix} \tag{2.8}$$

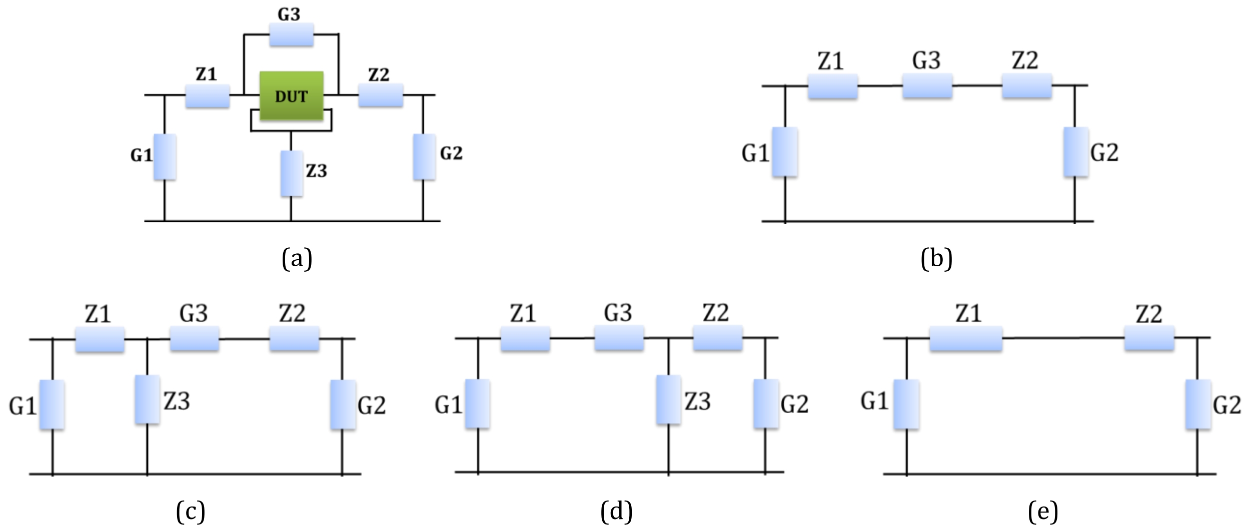


Figure 2.2. (a) DUT with parasitics (b) *Open* (c) *Short 1* (d) *Short 2* (e) *Thru*

2.1.2 Cascaded Matrix Based Models

The second methods are based on the Cascaded Matrix Based Model [3], [9], [10]. In this model the pad and interconnect parasitics are calculated differently, and multiply each parasitics effect to get the total effect of the parasitics. These methods are accurate to de-embed long feeding line lengths (compared to considered wavelengths, $l > \lambda/10$) and transmission lines. In the cascaded matrix based methods, the whole test structure is taken as cascaded network as shown in Figure 2.3. It considers distributed elements like matrix model.

Figure 2.3. Cascaded Matrix Based Model representation

2.1.2.(a). L-2L Kolding Method

L-2L Kolding de-embedding method [7], [10] is a transmission-line based de-embedding method. It follows the cascaded-matrix based solutions to find out the actual characteristics of the DUT. The parasitics are modeled as the cascaded matrix based, which is present in the form of multiplication in the DUT measurement. L-2L Kolding de-embedding uses two transmission lines, TL_1 with a length L_1, and TL_2 with a length $L_2 = 2.L_1$. The de-embedding structures for L-2L Kolding method is shown in Figure 2.4.

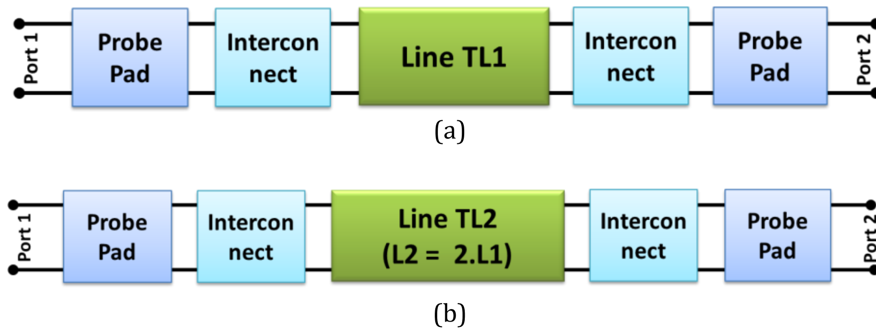


Figure 2.4. De-embedding structures (a) TL_1 (b) TL_2 (L_2 = 2. L_1)

The *Thru* ([PAD]. [PAD]), is obtained from the transfer matrix or *ABCD* matrix of the *TLs*.

$$[Thru] = [TL_1].[TL_2]^{-1}.[TL_1] = [PAD].[PAD] \tag{2.9}$$

where $[TL_1]$ is the ABCD matrix of the transmission line TL_1, and $[TL_2]$ is the *ABCD* matrix of the transmission line TL_2. While considering the pad as symmetrical (S_{11} = S_{22}), the parasitics can be derived directly from the S-parameters,

$$S_{11,p} = S_{22,p} = \frac{S_{11,t} + S_{22,t}}{2 + S_{21,t} + S_{12,t}} \tag{2.10}$$

$$S_{12,p} = S_{21,p} = \sqrt{\frac{1}{2}(S_{12,t} + S_{21,t})(1 - S_{11,p}^2)} \tag{2.11}$$

where $[S]_p$ is the S-matrix of the PAD. Similarly, $[S]_t$ is the S-matrix of the Thru, which is extracted from the lines using the equation (2.9). Then the DUT can be expressed as,

$$[T_{DUT}] = [PAD]^{-1}[T_{Measure}][PAD]^{-1} \tag{2.12}$$

where $[T_{Measure}]$ is the *ABCD* matrix of the measured device.

Consider the accessline with a length of TL_1 that can be derived from the PAD models without using any additional structure.

$$[T_{Accessline}] = [PAD]^{-1}[TL_1][PAD]^{-1} \tag{2.13}$$

where, $[T_{Accessline}]$ is the *ABCD* matrix of the accessline.

2.1.2.(b). TRL

TRL calibration was developed by Engen and Hoer [2] in 1979. TRL uses de-embedding structures *Thru*, *Reflect* (*Open* or *Short*) and *Line*(*s*). The *Thru* can be zero-length or non-zero-length thru. In general, for a zero- thru the S_{21} and S_{12} are equal to 1 and the S_{11} and S_{22} are equal to 0. The accurate

electrical length must be known to set the reference plane. The *Reflect* can be a *Short* or an *Open*, whose phase of the reflection coefficient must be specified within 1/4 wavelength or ±90 degrees for the center frequency *fc*. The reflection coefficient on all ports must be same. The third de-embedding structure is the *Transmission Line*(*s*). The electrical length of the *transmission line*(*s*) needs only be specified within 1/4 wavelength of the center frequency *fc*. The difference between the *thru* and *transmission line*(*s*) must be between 20 degrees and 160 degrees at center frequency *fc*. The optimal line length is 1/4 wavelength or 90 degrees relative to the *Thru* at the center frequency, f_C. The maximum usable bandwidth for a single line standard is 8:1. The maximum frequency is limited to $f_{max} = 8*f_{min}$, where, f_{max} = maximum frequency, and f_{min} = minimum frequency, so we need to use multiple lines to cover wide band.

The measurement model of a DUT test is shown in Figure 2.5. The Error Box A and the Error Box B are the pad/interconnect parasitics, which have to be de-embedded. The de-embedding structures are shown in Figure 2.6.

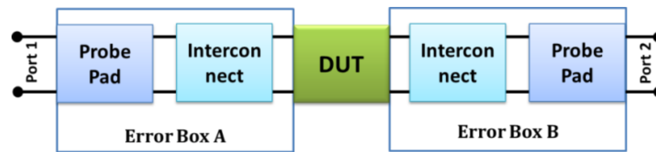


Figure 2.5. DUT measurement model

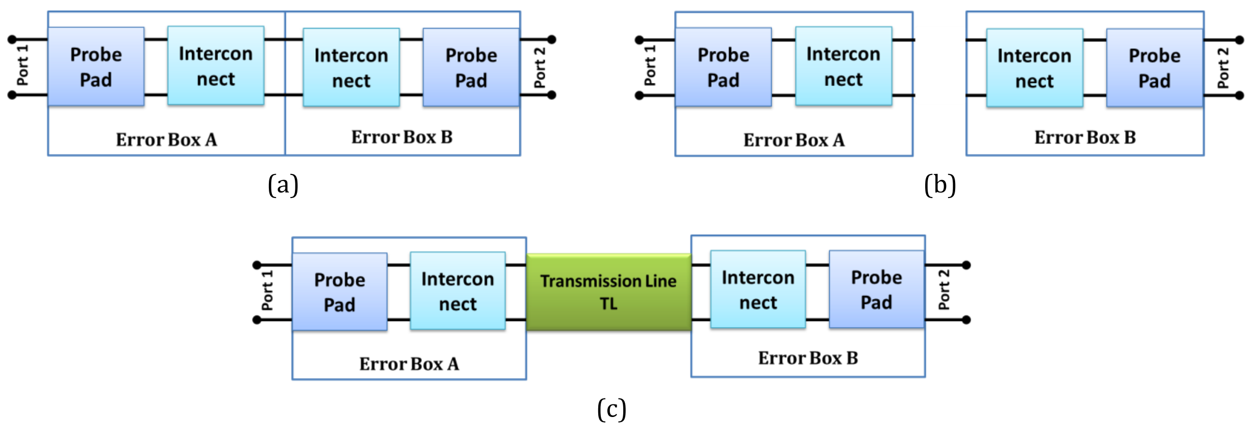


Figure 2.6. De-embedding structures (a) *Thru* (b) *Reflect: Open* (c) *Line*

TRL calibration uses the characteristic impedance of the *Transmission Line* standard to set the reference impedance. The accuracy of this method depends on the estimation of accurate value of the characteristic impedance of the *Line* standard. At low frequencies, the *line* standards become very long, this is one of the drawbacks of the TRL method. The algorithm for the TRL method is given in **APPENDIX - A.**

2.1.2.(c). Hernandez Method

It is an improved two-tier Line-Line method [16]-[18]. This method utilizes two uniform different transmission lines to extract the characteristics of the transmission line. The characteristic impedance and propagation constants of the transmission lines should be same, but the lengths should be different. The de-embedding structures are shown in Figure 2.7(a) and Figure 2.7(b). The length of the transmission lines is T_{L1}, and T_{L2}, where T_{L1} < *or* ≠ T_{L2}. The pad parasitics are considered as a transmission matrix T_A. For this method, the transmission line parasitics should be symmetric.

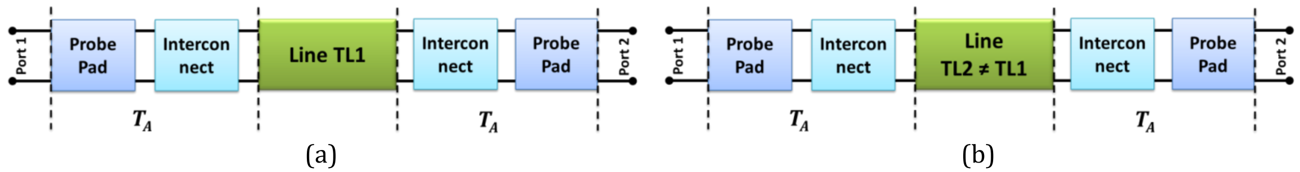


Figure 2.7. De-embedding structures (a) T_{L1} (b) T_{L2}

The extraction of the characteristic impedance and the propagation constant of the transmission lines are mentioned below,

From the Figure 2.7(a) and Figure 2.7(b),

$$M_1 = T_A T_{L1} T_A \tag{2.14}$$

$$M_2 = T_A T_{L2} T_A \tag{2.15}$$

Combining the equations (2.14) and (2.14),

$$M_1 M_2^{-1} = T_A T_{L1} T_{L2}^{-1} T_A^{-1} \tag{2.16}$$

Consider,

$$M_1 = \begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix} \text{ and } M_2 = \begin{bmatrix} p_{11} & p_{12} \\ p_{21} & p_{22} \end{bmatrix} \tag{2.17}$$

where, $m_{11} = p_{11}$ and $m_{22} = p_{22}$. These above equations can be solved by considering the *ABCD* Matrix of transmission line and matrix functions [16]-[18]. Finally, we can express the characteristic impedance (Zc) and propagation constant (γ) as,

$$Zc = \frac{p_{12}(Cosh(\gamma l_1) + m_{11}) - m_{12}(Cosh(\gamma l_2) + p_{11})}{det(K)} \tag{2.18}$$

where,

$$K = \begin{bmatrix} m_{11} + \cosh(\gamma l_1) & \sinh(\gamma l_1) \\ p_{11} + \cosh(\gamma l_2) & \sinh(\gamma l_2) \end{bmatrix} \quad (2.19)$$

$$\gamma = \frac{1}{L_2 - L_1} ln \left[1 - \frac{b_m}{a_m/c_m} \left(\frac{1}{t_{11} + \frac{a_m}{c_m} t_{12} - b_m t_{21} - \frac{b_m}{a_m/c_m} t_{22}} \right) \right] \quad (2.20)$$

2.1.3 Cascaded Matrix with Lumped Equivalent Models

Cascaded Matrix with Lumped Equivalent Models are considered as a combination of both Cascaded Matrix Based Model and Lumped Circuit Equivalent Model circuits [3]. This method is used to de-embed both feeding transmission lines (long and short) and couplings between input/output DUT devices accurately. In this method, the whole test structure is taken as cascaded matrix with lumped equivalent model for the pad-interconnects parasitics/coupling between the probes and interconnects as shown in Figure 2.8.

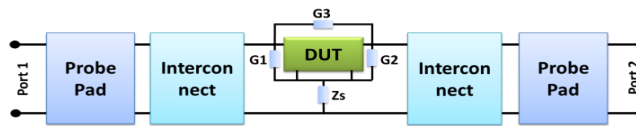


Figure 2.8. Cascaded Matrix with Lumped Equivalent Model representation

Many de-embedding methods are based on Cascaded Matrix with Lumped Equivalent Models. The important Cascaded Matrix with Lumped Equivalent methods are described below.

2.1.3.(a). L-2L YZ De-embedding

L-2L YZ de-embedding [11] is a transmission-line based de-embedding method. In this method, the parasitics are modeled as *Z-series* impedance with a *Y-shunt* admittance shown in Figure 2.9. This method uses both cascaded matrix and lumped equivalent based calculations, so it comes under Cascaded Matrix with Lumped Equivalent Model topology.

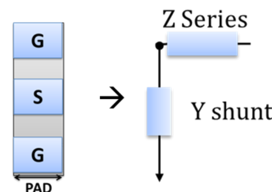


Figure 2.9. Pad parasitics as YZ model

L-2L YZ de-embedding uses transmission line with length of L_1, and 2nd the transmission line with the length of L_2 = 2. L_1. The de-embedding structures for L-2L YZ de-embedding is similar as L-2L Kolding method, which is already shown in Figure 2.4

$$T_{m1} = T_{lpad} T_{L1} T_{rpad} \tag{2.21}$$

$$T_{m2} = T_{lpad} T_{L2} T_{rpad} \tag{2.22}$$

where, T_{lPad} is the T matrix of the "left pad" and T_{rPad} is the T matrix of the "right pad". From these lines we can find the "Thru" using the following empirical equation,

$$T_{lpad} T_{rpad} = T_{m1} T_{m2}^{-1} T_{m1} = T_{thru} \tag{2.23}$$

Here, we assume the Pad as *Z-series* impedance with *Y-shunt* admittance [11], then the "left pad" and the "right pad" can be expressed as,

$$T_{lpad} = \begin{bmatrix} 1 & Z_{series} \\ Y_{shunt} & Y_{shunt} Z_{series} + 1 \end{bmatrix} \tag{2.24}$$

$$T_{rpad} = \begin{bmatrix} Y_{shunt} Z_{series} + 1 & Z_{series} \\ Y_{shunt} & 1 \end{bmatrix} \tag{2.25}$$

Finally, the DUT can be expressed as,

$$T_{DUT} = T_{lpad}^{-1} T_{meas} T_{rpad}^{-1} \tag{2.26}$$

2.1.3.(b). Mangan De-embedding Method

Mangan de-embedding method [12] is a transmission-line based method, where the parasitics are effectlively considered into a parallel admittance "*Y*". This method uses *two different transmission lines* to get the actual characteristics of the DUT transmission line, *TL Long* and *TL Short* (see Figure 2.10). These two de-embedding structures (*TL Long* and *TL Short*) should have the same characteristic impedance as DUT. The effective length of the DUT will be the difference between the two transmission lines used.

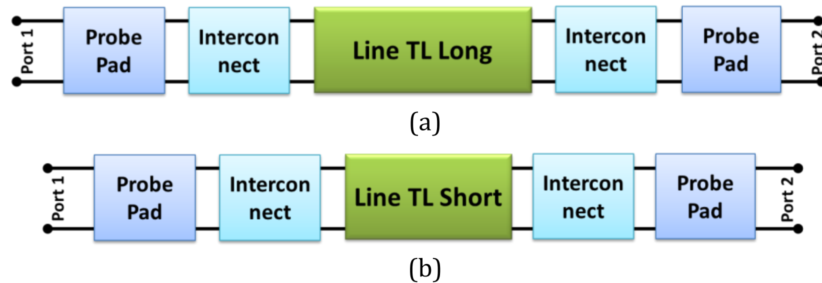


Figure 2.10. De-embedding structures (a) *TL Long* (b) *TL Short* (c) DUT = *TL Long* – *TL Short*

A hybrid structure can be derived by considering the *T-matrix* of the two lines, which is expressed as,

$$M^{h}_{l2-l1} \equiv M^{t}_{l2} \times \left[M^{t}_{l1}\right]^{-1} \tag{2.27}$$

Convert the hybrid matrix into *Y-matrix*. Considering the intrinsic device is symmetric, so its *Y parameters* can be isolated by connecting Y^{h}_{l2-l1} in parallel with a matrix-swapped version of itself, thus cancelling out the effects of the pads,

$$Y_{l2-l1} \equiv \frac{Y^{h}_{l2-l1} + Swap(Y)^{h}_{l2-l1}}{2} \tag{2.28}$$

The resultant matrix is the characteristics of the DUT.

2.1.3.(c). Thru-Only De-embedding

Thru-Only de-embedding method [13] is a transmission-line based method, where the parasitics are considered into a simple "*Y*" same as in Mangan method. This method uses only one de-embedding structure "*Thru*" shown in Figure 2.11. The intrinsic characteristics of the DUT can be calculated using the same steps as the Mangan method (see equations (2.27) and (2.28)). The transmission line long and transmission line short can be replaced by *Thru* de-embedding structure and device measured ($DUT_{Measure}$) respectively.

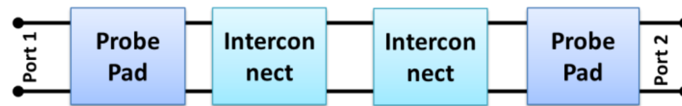


Figure 2.11. Thru de-embedding structure

2.1.4 Conclusion and Further studies of Classification of De-embedding Methods

De-embedding methods are categorized into different types and different methods from each types are explained. Currently, **all these types have been investigated only for frequencies up to 65 GHz or to maximum 170 GHz** [3].

In the present study, efforts have been payed to evaluate these methods up to 250 GHz by considering two kinds of parasitic approaches.

1. Known parasitics de-embedding: using Advanced Design System (ADS), Agilent .
2. Unknown parasitics de-embedding: 3D EM Model Simulation tool: (Ansys HFSS)

In the known parasitics de-embedding, the parasitics to be de-embedded using different methods are known. This method can be tested using ADS, Agilent [20]. **The parasitics can be modeled as known lumped or distributed elements or the combination of both distributed and lumped elements.** This helps to test the de-embedding method in the preliminary stage. To evaluate the accuracy of the

methods, we consider the characteristic impedance value (Zc). Considering all the parasitics values are known, we are expected to have a 0% error for characteristic impedance (Zc) over the entire band until 250 GHz.

In unknown parasitics, it is done by using a real model of pad or interconnect parasitics. This real model parasitics can be modeled using a 3D full-wave electromagnetic simulation tool (Ansys HFSS) [21]. Here the parasitics and the DUT tests are modeled in the ST BiCMOS 55 nm technology. Since the parasitics values are unknown, we are expected to have a 5% error for characteristic impedance (Zc), so a good method should have 5% error over the entire band until 250 GHz. Also, we used magnitude of the reflection coefficient (S_{11}), the transmission coefficient (S_{21}), and attenuation coefficient (α) to explain the variation in the results.

2.2 BiCMOS 55 nm Silicon Technology

The BiCMOS 55 nm technology is developed by STMicroelectronics. It provides silicon technology platform for radio frequency (RF) applications, millimeter wave applications and optical applications (THz). Specifically, this technology is intended for the development of automotive radar systems (77GHz / 120GHz), wireless networks (60 GHz), imaging and detection for biomedical and military applications, optical communications up to 400 Gbits/s, the mobile communication Photonics 4G / 5G generations, and ultimately for the development of in-situ measurements solutions for millimeter circuits beyond 110 GHz.

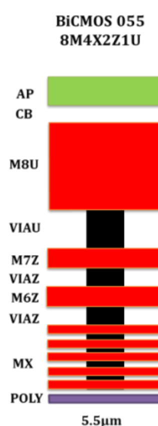


Figure 2.12. BEOL of BiCMOS technology 55 nm

The development of an efficient technology for very high frequency applications cannot be assured only by the optimization of the active components of the technology. The optimization of the active part must be accompanied by an optimization of the metal layers, forming the Back End of Line (BOEL) technology [22], [23]. The BEOL of B55 technology is dedicated to the millimeter applications. The BEOL of B55 nm technology is represented in Figure 2.12. Copper layers M_1 through M_7 and vias are

similar to those of the CMOS 55 nm technology, while the M_{8U} and via layer (ViaU) are equivalent, in terms of thickness, M_{IT} layer and ViaT of BiCMOS9MW technology.

The thick metal layers (M_6, M_7, and M_8) are intended to reduce resistive losses in the interconnections and thus enabling the realization of low-loss passive structures. However, the dimensions of the lower metallization levels (level M_1 to level M_5) are reduced in thickness and minimum widths. This decrease in thickness of the metal also results in a reduction of the thickness of the dielectric layers.

2.3 Proof of Concept with ADS

To verify the de-embedding methods, we realize the ideal de-embedding structures and the DUT using Advanced Design System (ADS), Agilent [20]. An *ideal transmission line* is chosen as the DUT. This lossless transmission line has the characteristic impedance of 30 Ω and 2 mm length. we consider a lossless transmission line with a different impedance than the 50 Ω. The 50 Ω lines have very low return loss and low loss, so it will be difficult to analyse the accuracy of the method. Nevertheless the de-embedding should work irrespective to the impedance or any other characteristics of the DUT.

The characteristics of the transmission line considered as DUT can be directly determined from the circuit shown in Figure 2.13. Since there are no parasitics associated with the DUT / Transmission line, the characteristic impedance of the transmission line can be derived from the *ABCD* matrix of the transmission line. However, this is not the actual case; normally the DUT is measured with the addition of pads and interconnects in silicon technology. This pad can be modeled from simple parasitic capacitance or contact resistance to complicated lumped/cascaded models. To eliminate these parasitic effects we need to model the different de-embedding structures to perform the de-embedding [1]-[19]. The number and type of the de-embedding structures depends on the method used.

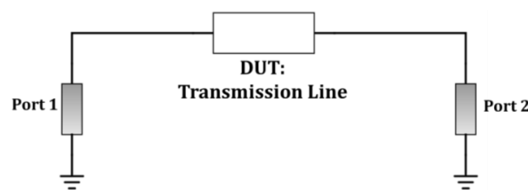


Figure 2.13. Lossless transmission line realized using ADS

The characteristic impedance is expressed as,

$$Z_C = \sqrt{B/C} \tag{2.29}$$

where B and C are taken from *ABCD* matrix of the transmission line.

2.3.1 Pad-Acceslines Parasitics Models

The known parasitics can be modeled as;

1. **Lumped parasitics**
2. **Distributed parasitics model**
3. **Distributed with Lumped parasitics model**

To evaluate and benchmark the de-embedding methods the parasitics of the pad and interconnects can be realized as known lumped [3], [7], distributed and distributed with lumped parasitics model. This helps us to understand the frequency limitations, different advantages and the disadvantages of the de-embedding methods.

1. **Lumped parasitics**

The PADs can be modelled with lumped electrical models as shown in Figure 2.14. As shown in **APPENDIX - B,** the pad can be modeled as a "*Pi*" model circuit with a parallel capacitance C_P, a series inductance L_S corresponding to inductive pad/interconnect length and a series resistance of R_S, series resistance which is very small and can be neglected. The values of each parameter can vary especially according to the technology. In this benchmark, the ST BiCMOS 55 nm technology is considered. A realistic *Pi-model* has been obtained (**APPENDIX - B**) with C_P = 18 fF, L_S = 3.95 pH and R_S = 0.18 Ω.

The de-embedding methods are evaluated step by step increment in the parasitics of the pad. **To benchmark the de-embedding methods, these known lumped parasitics can vary from simple parallel capacitance to the more realistic *Pi-model*.** This helps us to find out the limitations of each method.

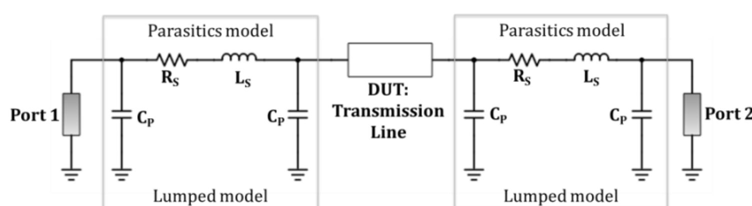


Figure 2.14. Lumped Model of Pad parasitics: DUT Measurement model

Various pad modelings are used to analyse the methods:

Pad as Parallel "C_P" (Pad Capacitance). By neglecting the other series elements, the parasitics of the pad/interconnect are considered as a simple parallel capacitance. This is the simplest parasitic model used to evaluate all the de-embedding methods. In general, a simple *open* de-embedding structure is enough to de-embed this kind of parasitics.

Pad as "C_P - R_S" (*C-R*) model: the series inductance L_S is neglected from the parasitics. In the simulation parasitic resistance R_S is very small, but in the reality, it can be an additive with the probe contact resistance. This pad contact resistance can even vary with different type of probes and the type of pads (aluminium or gold) used for the measurement.

Pad as "C_P-R_S-L_S" (*C-R-L*) model: An asymmetric pad/interconnect parasitics is formed with addition of inductive pad/interconnect length as series inductance L_S with pad capacitance C_p and probe contact resistance R_S.

Pad as *Pi-model* or "C_P-R_S-L_S-C_P" model: The parasitics of the pad/interconnects can be modeled as a "***Pi***" model to obtain a better modeling.

2. Distributed parasitics model

The second approach of modeling the parasitics is based on the distributed model. DUT measurement with a pad parasitics as **Distributed "*TL*"** model is shown in Figure 2.15. "*TL*" is nothing but a small (50 µm) loss less transmission line itself. These parasitics are much complex than the known lumped models.

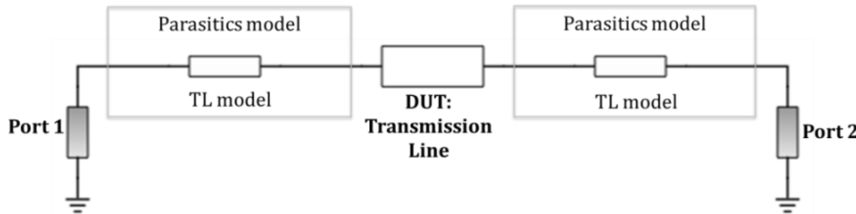


Figure 2.15. Pad parasitics as Distributed "*TL*" model

3. Distributed with Lumped parasitics model

The third model is a combination of Distributed and Lumped model. The pad parasitics are modeled as the **combination of both lumped and distributed models**. For example, pad/interconnect parasitics as a distributed "*TL*" model interconnect with parallel capacitance C_P and series interconnect with the length of L_L **(*C-TL-L*),** shown in Figure 2.16. Also we can consider pad/interconnect parasitics as a parallel capacitance with a "*TL*" model interconnect **(*C-TL*)** model. Different configurations can be applied to model these kind of parasitics.

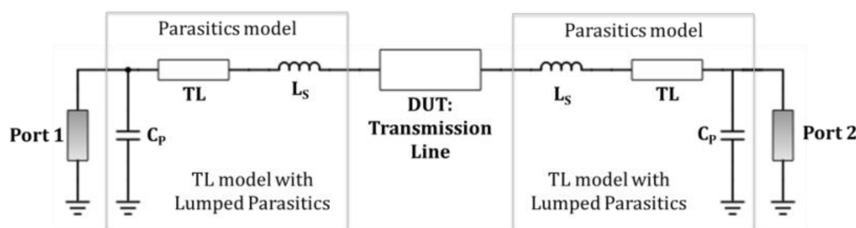


Figure 2.16. Pad parasitics as Distributed "*TL*" with Lumped model

2.3.2 De-embedding Structures: Known Parasitics De-embedding

The de-embedding structures used for different de-embedding methods are described in Table 2.1.

De-embedding Methods		De-embedding Structures			
		Open	Short	Thru	Line
Lumped Equivalent Circuit Model	Open De-embedding [3], [7], [8]	✓ *Open*			
	Open-Short De-embedding [3], [7], [8]	✓ *Open*	✓ *Short*		
	Vandamme De-embedding method [4]	✓ *Open*	✓ *Short 1* ✓ *Short 2*	✓ *Thru*	
Cascaded Matrix Based Models	L-2L Kolding Method [7]				✓ TL_1 of length L_1 ✓ TL_2 of Length = $2.L_1$
	TRL [2]	✓ *Open or Short*		✓ *Thru*	✓ *Line(s)*
	Hernandez Method [17]				✓ $TL_1 < or \neq TL_2$
Cascaded Matrix with Lumped Equivalent Models	L-2L YZ De-embedding [11]				✓ TL_1 of length L_1 ✓ TL_2 of Length = $2.L_1$
	Mangan De-embedding method [12]				✓ *Line Long* ✓ *Line Short*
	Thru-Only De-embedding [13]			✓ *Thru*	

Table 2.1 De-embedding Structures for Different de-embedding methods

All de-embedding structures with lumped model parasitics are shown in Figure 2.17. Depending on the parasitics, the lumped model has to be replaced with the proper parasitics model.

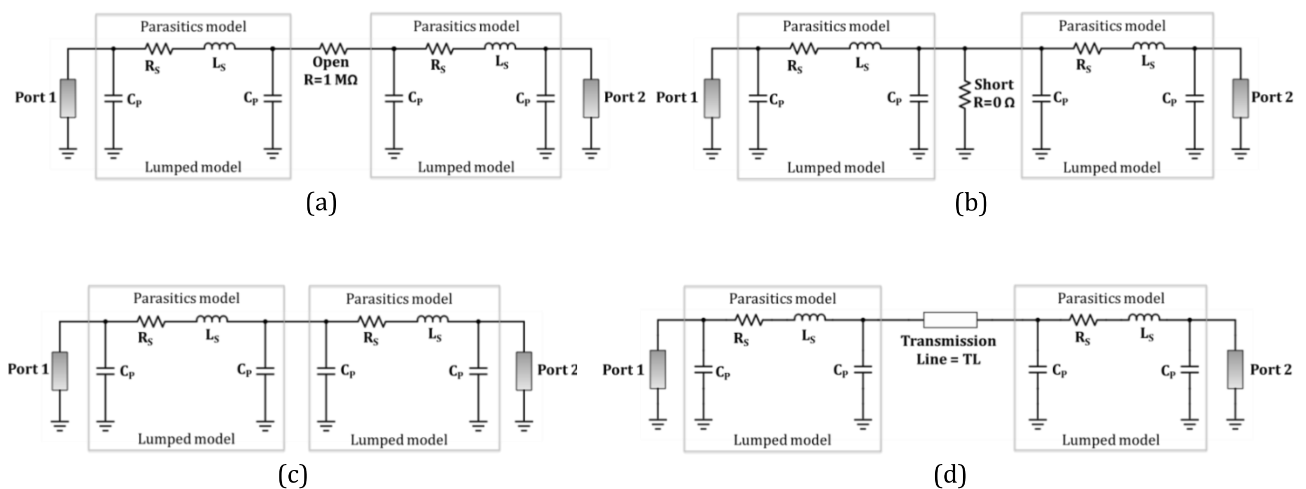


Figure 2.17. De-embedding structure (a) Open (b) Short (c) Thru (d) Line

With the known pad/interconnect parasitics, different de-embedding methods can be benchmarked and study the advantages and limitations of each method. This can be done by using ADS, where **the methods are simulated and analysed until 250 GHz. The goal is to evaluate the methods which are >100 GHz.** In the results we considered only 4 parasitics models (see section 2.3.1) i.e. *Parallel "C", "C-R-L" model, Pi-model* and the "*TL*" model are considered. Remaining lumped model "*C-R*" model, distributed and lumped model "*C-TL-L*" and "*C-TL*" can be co-related to the "*C-R-L*" model, since all models are asymmetric.

2.3.3 Analysis of Lumped Equivalent Circuit Model De-embedding Methods

A de-embedding method has good de-embedding results with *Pi-model* of the pad in our case, since the pad is modeled as "*Pi*" model for this study. Apart from this *Pi-model*, we considered asymmetric parasitic models such as series inductance or transmission line elements to have interconnect characteristics. However, a good de-embedding method should de-embed any kind of parasitics, from simple pad to pad with interconnect lines.

2.3.4.(a). Open De-embedding

The theory of the Open de-embedding [3], [7], [8] is explained in the section 2.1.1.(a). The characteristic impedance of the DUT is extracted using equation (2.29) from the de-embedded result shown in Figure 2.18.

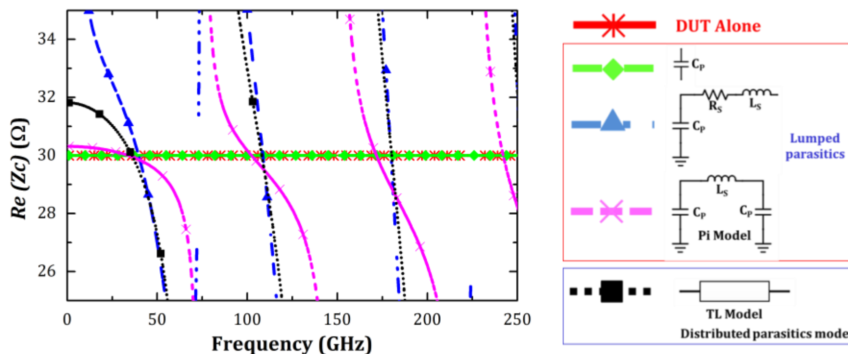


Figure 2.18. Open De-embedding: Characteristic Impedance of the DUT

As shown in Figure 2.18 the open de-embedding provides good accuracy when only the parallel capacitance (C_P) is considered since this method can only de-embed parallel element. Any series elements which are present in the pad or interconnect can affect the accuracy of the de-embedding. Hence, **considering the *Pi-model* parasitics, the accuracy of this method is limited to frequencies below 40 GHz. If a long accessline is considered, the series L_S reaches high value leading to a limitation of accuracy of this method dropping down to few GHz.** There is a presence of series element(s) in all other parasitic models (i.e. "*C-R-L*", "*Pi*" and "*TL*" model) described in the results. In a

real scenario, it will be difficult to assume a simple parallel capacitance as the only parasitics, especially in millimeter wave and above, hence this method will be no more efficient.

2.3.4.(b). Open-Short De-embedding

The theory of the open-short de-embedding [3], [7], [8] is explained in the section 2.1.1.(b). The characteristic impedance of the DUT is extracted using equation (2.29) from the de-embedded result and shown in Figure 2.19.

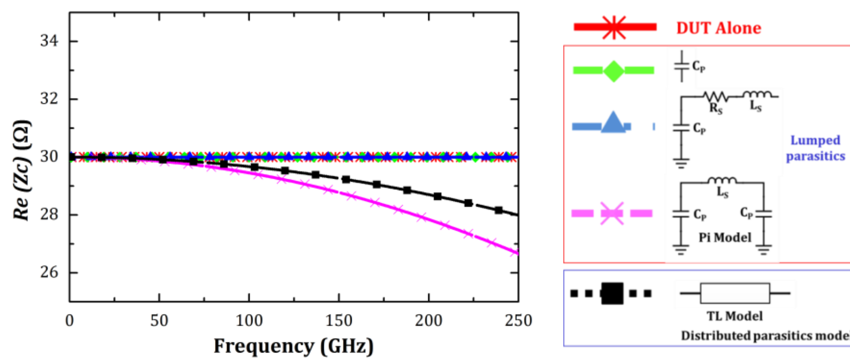


Figure 2.19. Open-Short De-embedding: Characteristic Impedance of the DUT

As shown in Figure 2.19 the Open-Short de-embedding has good accuracy in the case of both simple the parallel capacitance parasitics and with parallel capacitance and series elements. **Multiple parallel elements are difficult to de-embed using Open-Short de-embedding for a broad band of frequencies,** because this method can de-embed only a simple parallel - series parasitics. Since the lumped *Pi-model* is not simplified to a simple parallel element, **the accuracy is limited to frequencies below 50 GHz,** as same for the distributed "*TL*" parasitics model. The method is highly topology depend, so this method cannot consider any parasitics beyond its topology. In the real scenario the open-short de-embedding can face the problems before millimeter wave band, since it is a lumped element method.

2.3.4.(c). Vandamme Method

The theory of Vandamme de-embedding method [4] is presented in the section 2.1.1.(c). The characteristic impedance of the DUT from the de-embedded result is shown in Figure 2.20. The **accuracy of the method is limited for frequencies below *50* GHz, considering the *Pi-model* parasitics**. Since the method considers lumped element models, the **accuracy highly depends on the topology of parasitic model**. This method is accurate for lumped parasitic models, like simple pad capacitance (C_P) and the "*C-R-L*" model. The method is inaccurate for the complicated parasitic models, like lumped *Pi-model* or distributed "*TL*" models. Hence, these methods are not valid at high

frequencies, since feeding lines can be longer than $\lambda/10$. From the characteristic impedance it is clear that the accuracy drops off at higher frequency.

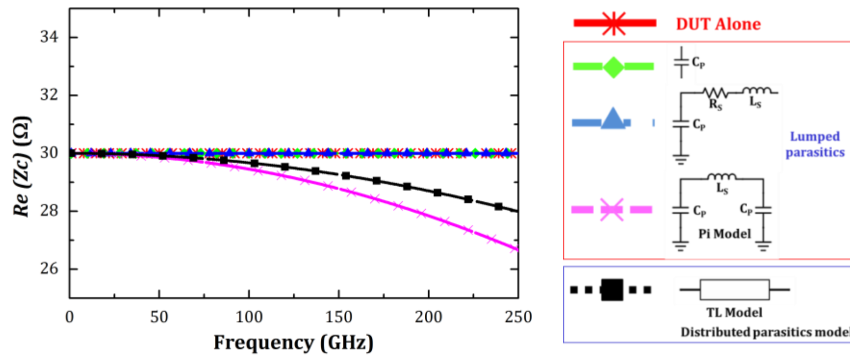


Figure 2.20. Vandamme De-embedding: Characteristic Impedance of the DUT

2.3.4 Analysis of Cascaded Matrix Based Model De-embedding Methods

In cascaded matrix model [9], [10] the pad – interconnect parasitics are calculated differently, and compute the total effects by taking the sum of each.

2.3.6.(a). L2L-Kolding Method

The theory L2L-Kolding method [7],[10] is detailed in the section 2.1.2.(a). The characteristic impedance of the DUT from the de-embedded result is shown in Figure 2.21.

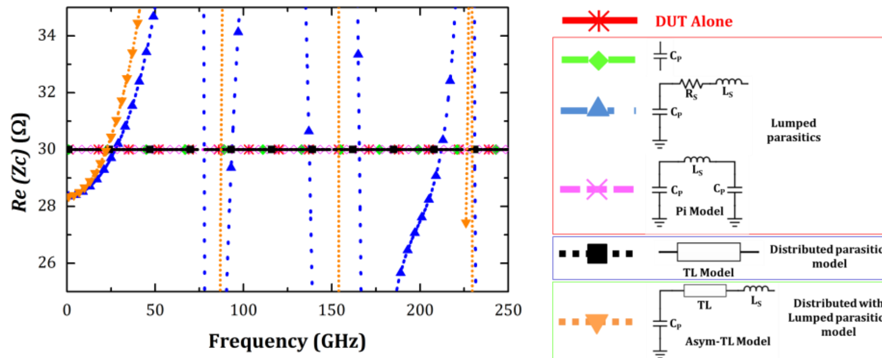


Figure 2.21. L2L-Kolding De-embedding: Characteristic Impedance of the DUT

The method shows good accuracy over a broad range of frequency, except the lumped parasitic model "*C-R-L*" and cascaded with lumped parasitics model "*C-TL-L*" (Asym-TL Model), because, this method has the theoretical assumption of the symmetrical (S_{11} = S_{22}) parasitics. The "*C-R-L*" and "*C-TL-L*" parasitic models are asymmetric in nature. The magnitude and phase of the S-parameters (S_{11} and S_{22}) of the "*C-R-L*" model are shown in Figure 2.22. The Figure 2.22 shows that the "*C-R-L*" model is not symmetrical, because the magnitude and phase of S_{11} and S_{22} are different ($S_{11} \neq S_{22}$). Hence the theoretical assumption of the symmetry ($S_{11} = S_{22}$) is not valid.

If the pad and the interconnect lines parasitics are symmetrical, this method can get good accuracy over a wide range of frequencies. This is the case with *Pi-model* or *TL* model as shown in Figure 2.21. **In reality, this is a rare case in the measurement.**

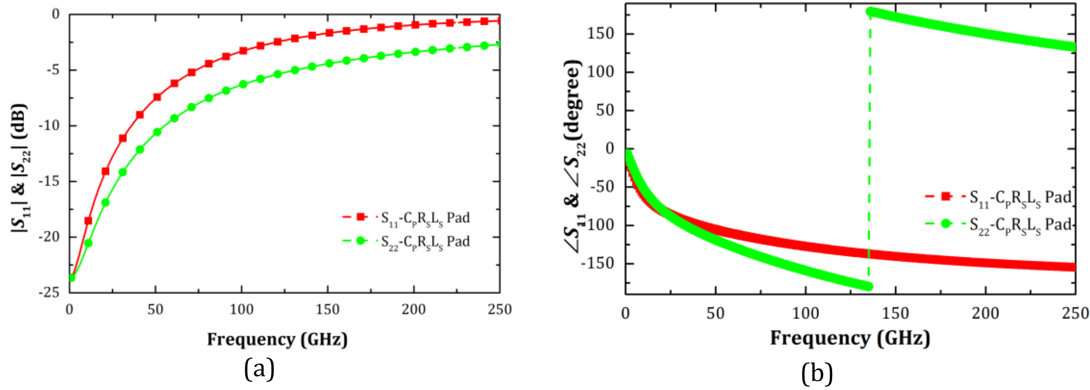


Figure 2.22. Magnitude and Phase plots: S_{11} and S_{22} of *C-R-L* parasitics

2.3.6.(b). TRL

The theory of TRL [2] is explained in the section 2.1.2.(b). The characteristic impedance of the DUT extracted using equation (2.29) from the de-embedded result is shown in Figure 2.23.

From the characteristic impedance, it is clear that the de-embedding using **TRL is highly accurate for a wide band of frequencies**. **Theoretically, there is no limitation** for TRL in the case of frequency. The major disadvantages for TRL are that the line impedance should be known and we use multiple lines to cover the wide frequency band. Also, we used the *open* which is perfectly open, but in reality it is difficult to have a perfect reflect throughout the frequency. TRL requires a large surface area in the wafer and therefore it will be expensive for the broadband frequency de-embedding.

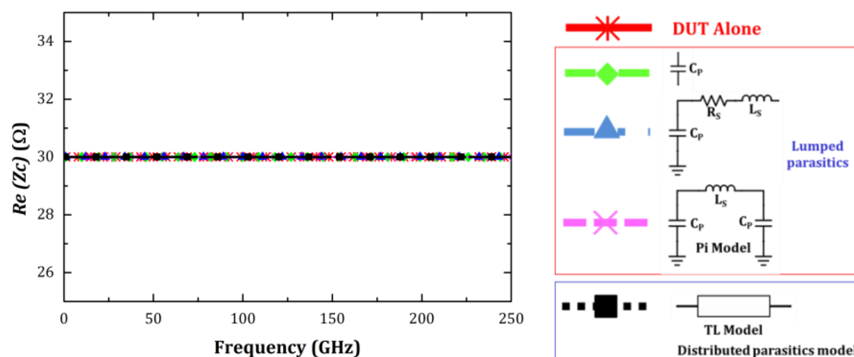


Figure 2.23. Characteristic Impedance of the DUT - TRL

Generally, the characteristic impedance of the line is obtained from a homogeneous line of 50 Ω, simulated using an electric or an electromagnetic simulation. Consider the line impedance is not 50 Ω; if it is varied in the real process approximately to ~47Ω. The transmission coefficient (S_{21}) and the characteristic impedance of the de-embedded results are shown in Figure 2.24.

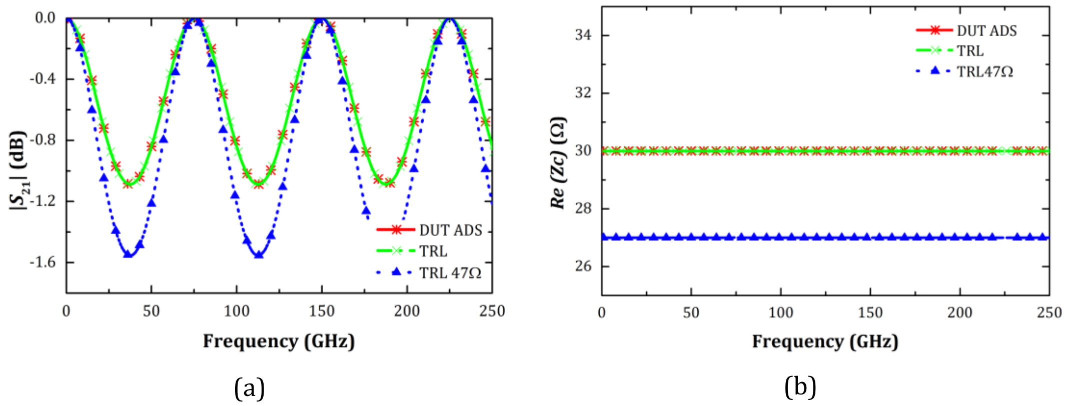


Figure 2.24. TRL: Line impedance ~ 47Ω (a) Transmission coefficient of DUT (b) Characteristic Impedance of DUT

This variation in the characteristic impedance affects the accuracy of the results. Since we consider DUT itself as a transmission line, the characteristic impedance is an important parameter to extract from the de-embedding. In addition, this error-factor (characteristic impedance values) might not be constant in the case of frequency.

2.3.5 Analysis of Hernandez Method

The theory of Hernandez Method [16]-[18] is explained in the section 2.1.2.(c). The characteristic impedance extracted from the de-embedded results is shown in Figure 2.25. The method is accurate over a broad range of frequency, except the lumped parasitic model "*C-R-L*", because this method is only with symmetrical ($S_{11} = S_{22}$) parasitics. So any asymmetry in the parasitics causes inaccuracy. The parasitics models like "*C-R-L*" and "*C-TL-L*" are asymmetric in nature. Asymmetry ($S_{11} \neq S_{22}$) of the "*C-R-L*" parasitics model are shown in Figure 2.22.

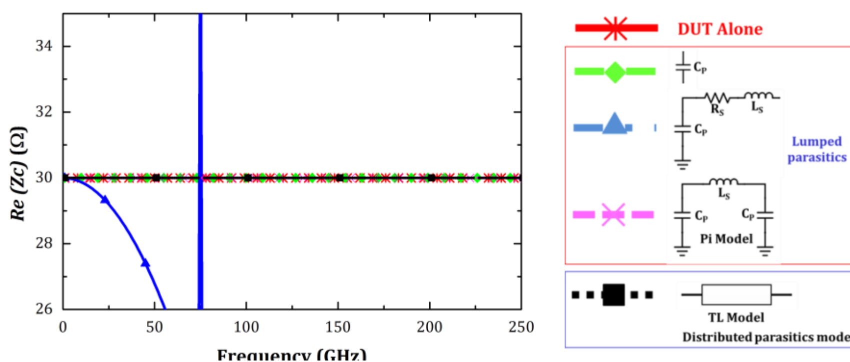


Figure 2.25. Characteristic Impedance of the DUT – Hernandez Method

2.3.6 Analysis of Cascaded Matrix with Lumped Equivalent Model De-embedding Methods

2.3.6.(a). L-2L YZ De-embedding:

The theory of L2L – YZ de-embedding method is presented in the section 2.1.3.(a). The characteristic impedance of DUT is extracted from the de-embedded result and is shown in Figure 2.26.

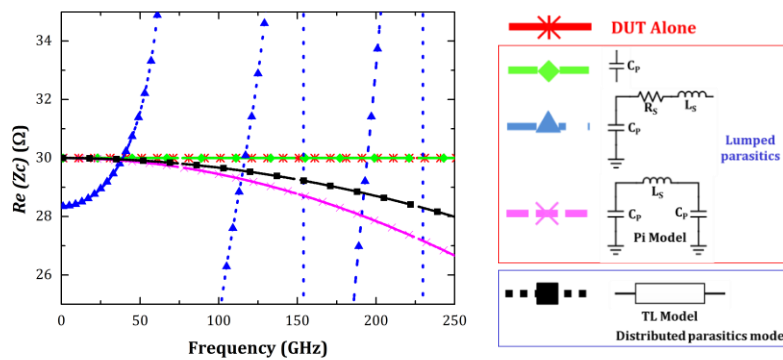


Figure 2.26. L2L -YZ De-embedding: Characteristic impedance of the DUT

The method works with only single lumped approximation of *Y* and *Z* elements. So, this method is only accurate with "*C*" and "*C-R*" lumped parasitics models. Since the method is using lumped circuit element approximation with the cascaded matrix based model, the method is **depends on the topology of lumped equivalent model used**. In addition, **multiple elements are difficult to de-embed for a broad band of frequencies.** Therefore, the accuracy of *Pi-model* and the distributed "*TL*" parasitics model is limited below 50 GHz. "*C-R-L*" parasitics model has multiple series elements, where the value of the 2nd series element cannot be approximated using this method, so that the accuracy drops off at lower frequency itself.

2.3.6.(b). Mangan De-embedding:

The theory of Mangan de-embedding method [12] is explained in section 2.1.3.(b). The characteristic impedance extracted from the de-embedded results is shown in Figure 2.27.

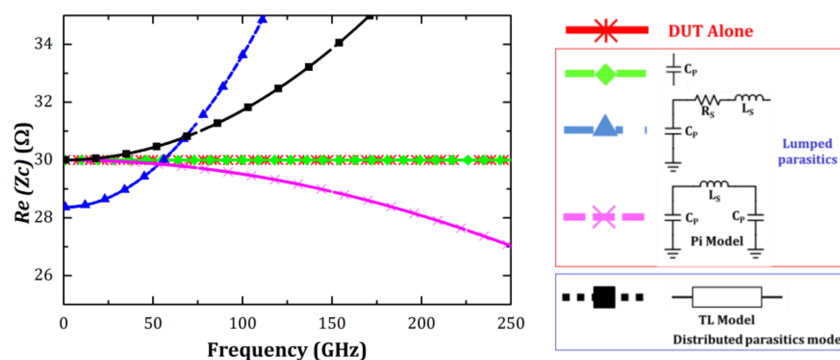


Figure 2.27. Mangan De-embedding: Characteristic Impedance of the DUT

This method approximates the pad or pad-interconnect parasitics as a simple "*Y*", so any series element that will create an error in the de-embedding. Apart from the simple pad capacitance parasitic models, the method is inaccurate for the models with series elements, like "*C-R-L*" model, *Pi-model* or "*TL*" models. Depending on the value of the series element present in the parasitics determines the accuracy of the method, it can be even limited to few GHz. Mangan method is not good for long accessline de-embedding.

2.3.6.(c). Thru-Only De-embedding:

The theory of Thru-only de-embedding method [13] is explained in the section 2.1.3.(c). The characteristic impedance extracted from the de-embedded results is shown in Figure 2.28.

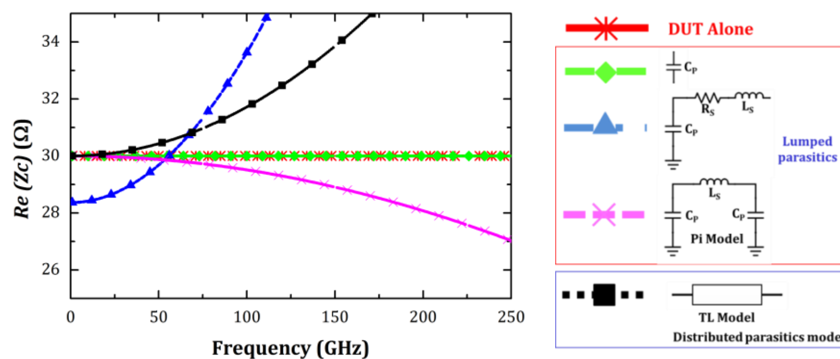


Figure 2.28. Thru-Only De-embedding: Characteristic impedance of the DUT

As same as Mangan method, **this method also approximates the parasitics as simple "*Y*".** The only difference is that this method always needs an accesslines to connect the DUT to the pad, because it utilizes only *thru* de-embedding structure. Zero-thru (PAD-PAD) is not possible in the measurement due to the coupling. Depending on the value of the series element (length of the accessline) the accuracy can drops to even few GHz. Apart from the simple pad capacitance parasitic models, this method is inaccurate for the models with series elements, like "*C-R-L*" model, *Pi-model* or "*TL*" models. Therefore, it is difficult to achieve a good accuracy until sub-millimeter wave range if the measurement model of the DUT has accesslines.

2.3.7 Conclusion of Proof of Concept with ADS

Different de-embedding methods [2]-[18] are benchmarked using the known parasitics. Lumped Equivalent Circuit Model methods, Cascaded Matrix Based Model methods and Cascaded Matrix with Lumped Equivalent Based Model methods are evaluated until 250 GHz for DUT as a lossless transmission line of 30 Ω.

Considering all the Lumped Equivalent Circuit Model methods [3]-[8] and Cascaded Matrix with Lumped Equivalent Model methods [11]-[13], the "*Pi-model*" lumped parasitics are difficult to

de-embed. **The accuracy of all the methods is limited to frequency below 50 GHz, considering the "*Pi-model*" parasitics**. The characteristic impedance extracted from the different Lumped Equivalent Circuit Model methods and Cascaded Matrix with Lumped Equivalent Model methods, with the parasitics of lumped "*Pi-model*" is shown in Figure 2.29(a).

Considering the **Lumped Equivalent Circuit Model methods**, Open de-embedding method cannot de-embed any series elements in the parasitics. Open-short de-embedding and Vandamme method cannot multiple lumped elements. Considering the **Cascaded Matrix with Lumped Equivalent Model methods**, L2L-YZ method approximates the parasitics as parallel Y and series Z elements. Any series parasitic element in measurement model will create an inaccuracy. The accuracy drops off for Mangan method and the Thru-only de-embedding. **In conclusion, lumped circuit equivalent model and cascaded matrix with lumped circuit equivalent model uses a physical model. It is a topology dependent, so that we can model the parasitics as a simple lumped model to the complex/multiple lumped model. Also, the interconnect lines should be taken as negligible $< \lambda/10$. Thus, these methods are no more valid at high frequencies since feeding lines can be longer than $\lambda/10$.**

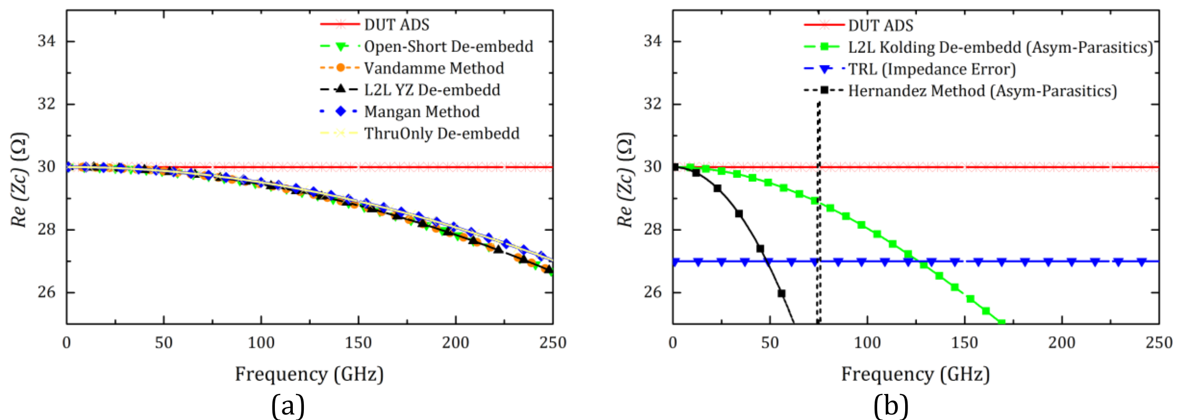


Figure 2.29. De-embedding Methods Limitations: Characteristic Impedance of DUT (a) Lumped equivalent methods (b) Cascaded Matrix based methods

The limitations of **cascaded matrix based methods** [2], [7], [10] shown in Figure 2.29(b). **Considering the cascaded matrix based methods, the "*Pi-model*" parasitics works well, because it is a symmetrical model. However, asymmetry in the parasitics makes the de-embedding method inaccurate**. L2L-Kolding method and Hernandez method are inaccurate to de-embed the asymmetrical parasitics. The characteristic impedance plot of DUT de-embedded using L-2L Kolding with the asymmetric parasitic model shown in Figure 2.29(b). As shown in Figure 2.29(b), the accuracy drops off for frequency below 40 GHz, because of the asymmetrical limitations. In reality, it is not sure that we can have good symmetrical parasitics assumptions beyond 100 GHz. **TRL is highly accurate for a wide band of frequency,** but TRL gives results referenced to the characteristic

impedance of the line which is unknown a *priori.* As shown in Figure 2.29(b), the characteristic impedance of DUT de-embedded using TRL with the line impedance of ~47 Ω (process variation error value of 50 Ω line impedance) shows the inaccurate results. TRL is limited to a certain band of frequency according to the line standard. To cover the entire frequency range, we require multiple lines. This increases the area in the wafer; thus the cost.

This is not enough to conclude a best de-embedding method for millimeter wave and sub-millimeter wave frequencies. This is a circuit model analysis. For an extensive study we need to perform the studies in the 3D full-wave electromagnetic solver.

2.4 Proof of Concept with HFSS

For an effective testing and analysis of the de-embedding methods, the de-embedding structures are modeled in 3D Full-wave Electromagnetic Simulator by Ansoft HFSS v14 [21]. As we mentioned in the state of the art of the thesis, IMEP-LAHC is developing devices and application based on Slow-Wave Coplanar Wave Guides (S-CPW) [24], [[25]. So, Here the DUT is considered as S-CPW transmission Line with a length of 400 µm, modeled in BiCMOS 55nm technology (see Figure 2.30).

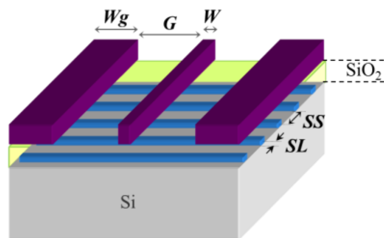


Figure 2.30. S-CPW Transmission line

The dimensions of the coplanar strips are given by a signal width of the S-CPW W=4 µm, a ground width Wg = 12 µm and a gap between the signal and ground G =40 µm*.* The fingers have strip width of SL = 0.16 µm and are separated by a distance of SS = 0.2 µm. The characteristic impedance of the line is about 70 Ω. The DUT impedance is chosen different from 50 Ω, because the transmission line with 50 Ω has a very low return loss so it will be difficult to analyse the accuracy of the method. However the de-embedding should work irrespective to the impedance or any other characteristics of the DUT.

The characteristics of the S-CPW transmission line can be directly determined from the *ABCD* matrix of the transmission line. Since there is no parasitics associated with the S-CPW Transmission line alone, the characteristic impedance (Zc) of the transmission line can be found using equation (2.29) and the attenuation constant (α) of the transmission line having length of "L" can be found using equation (2.30).

$$\alpha = \frac{Cosh^{-1}A}{L} \tag{2.30}$$

The effective permittivity (ε_{reff}) of the transmission line can be expressed as,

$$\varepsilon_{reff} = \left(\frac{c\beta}{\omega}\right)^2 \tag{2.31}$$

where, c is velocity in free space, β is the phase constant and ω is the angular frequency.

2.4.1 Parasitics Model: Unknown Parasitics De-embedding

To evaluate and benchmark the de-embedding methods [2]-[18] in a realistic scenario, DUT is connected with the pad-accessline parasitics and modeled in 3D full-wave electromagnetic simulation tool (Ansys HFSS) [21]. These parasitics are unknown parasitics; it depends on the EM model of pad or interconnect parasitics in the technology. To evaluate the de-embedding methods the parasitics of the pad and interconnects are realized according to the de-embedding methods. Mostly, all the methods are evaluated with only pad parasitics, except Thru-only de-embedding. The actual measurement of the S-CPW transmission line is shown in Figure 2.31.

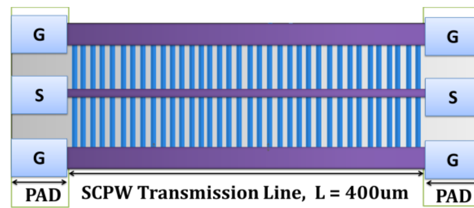


Figure 2.31. DUT SCPW measurement without interconnect/accessline

The measurement includes the pads to connect the DUT with the signal. These rectangle pads are 50 µm long, width of 35 µm and with the 50 µm of pitch from signal to ground. The optional accessline have the length of 100 µm with characteristic impedance of 50 Ω [26], [27].

2.4.2 De-embedding Structures

De-embedding structures for different de-embedding methods are modeled in Ansys HFSS and shown in Figure 2.32. The de-embedding structures needed for each methods described in section 2.3.2.

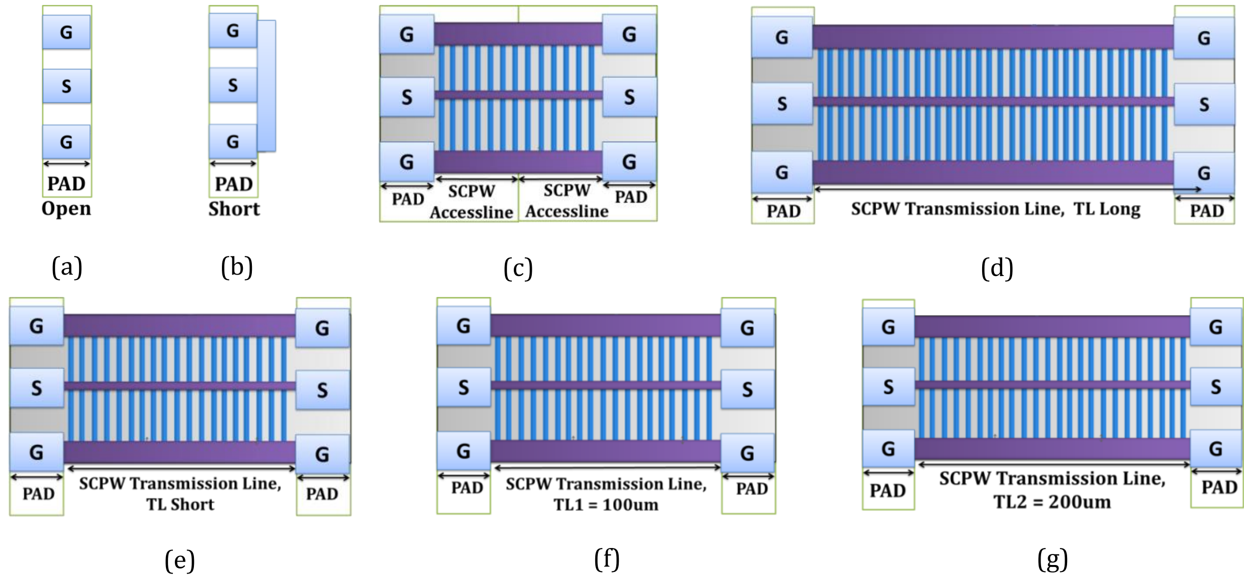


Figure 2.32. De-embedding structures: (a) *Open* (b) *Short* (c) *Thru* (d) T_{L1} (e) T_{L2} (f) *TL* Long (g) *TL* short

2.4.3 Benchmarking and Comparison of De-embedding Methods

Here we are comparing and benchmarking different de-embedding methods with standard calibration method TRL [2]-[18]. All the methods are tested based on its original measurement topology. The de-embedded results for S-CPW transmission line are shown in Figure 2.33 and Figure 2.34. As shown in Figure 2.33 and Figure 2.34, the DUT SCPW400µm (red curve) corresponds to electromagnetic simulations of the DUT without any access lines and PADs in order to know the *a priori* true parameters of the DUT. The characteristic impedance and the attenuation constant of the S-CPW transmission line is calculated from the de-embed results.

Figure 2.33 shows the comparison between **Lumped Circuit Equivalent method** (Vandamme [4]), and **both Cascaded Matrix Based methods** (L-2L Kolding [7]-[10], Hernandez method [16]-[18] and TRL [2]). From the characteristic impedance (*Zc*) results (Figure 2.33 (a)), TRL method gives more accurate results (error smaller than about 2 % up to 250 GHz) than other de-embedding methods. The characteristic impedance of the transmission line is chosen as 50 Ω, which is obtained from the simulation using Ansys HFSS. Since all parameters of the TRL are known, the probability of having an error in the de-embedding using TRL is less. That is why TRL shows good accuracy for the entire band.

Concerning the improved, three step method (Vandamme method), the limitations appear at very low frequencies, due to lumped circuit approximations and lumped methods are not valid at high frequencies, since feeding lines can be longer than $\lambda/10$. The approximation of the pad symmetry makes L-2L Kolding and Hernandez method inaccurate above 100 GHz, the error started increasing beyond 5% to 20% and more. These methods are only good for symmetrical pad structures and even

if symmetrical pads are considered herein, poor results are obtained above 100 GHz, especially concerning the characteristic impedance because of the discontinuity between pads and access lines.

Considering the attenuation constant (α) results (Figure 2.33 (b)), it is very difficult to analyse the results since all the methods have similar results all over the frequency. So we choose the magnitude of S_{21} results (Figure 2.33 (c)) to analyse the methods. From the results, except TRL, all other methods are limited below 100 GHz, similar as the characteristic impedance. TRL calibration technique promises good results over the 200 GHz. However, the limitation of TRL calibration is that multiple lines are required to cover a wide band of frequencies; also, the impedance of the line should be known. If the impedance of the line varies the results can be less accurate as we mentioned earlier in Figure 2.24. Also, the variation in the propagation constant, attenuation constant can affect accuracy of the method.

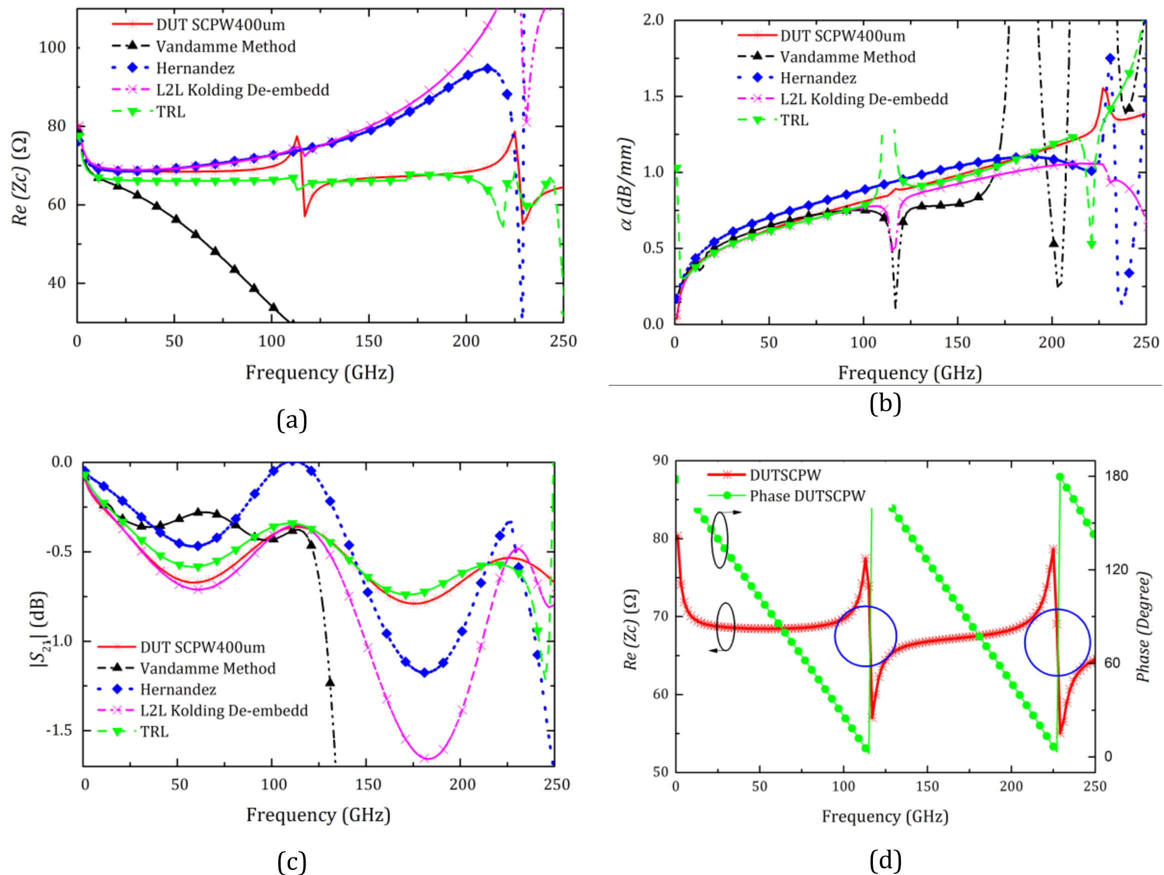


Figure 2.33. Benchmarking (a) Characteristic Impedance of the line (b) Attenuation coefficient of the line (c) Transmission coefficient of DUT (d) Characteristic impedance and Phase of the Transmission line

Note: The resonance points are avoided while calculating the percentage of error of Zc and α, because the resonance points are due to the mathematical limitation, which is mentioned below.

Characteristic impedance (Zc) and phase of the line of the S-CPW transmission line is shown in Figure 2.24(d). It shows a sudden variation which is happening in the extracted characteristic impedance. It is

because of the phase delay due to the length of the transmission line (phase change between 0 and pi) causes the numerical limitation. The characteristic impedance, ($Zc = \sqrt{B/C}$) can give inaccurate values, where the B= C ≈0 at $\lambda/2$ length of the transmission line.

Figure 2.34, shows the comparison and benchmarking between **Cascaded Matrix with Lumped Equivalent methods** (L-2L YZ method [11], Mangan method [12] and Thru only de-embedding [13]) and TRL is performed. From the characteristic impedance results (see Figure 2.34(a)), it is clear that accuracy of the Cascaded Matrix with Lumped Equivalent methods drops of about 100 GHz compared to TRL. Even the S_{21} results (see Figure 2.34(b)) shows the similar trend. Nearly 100 GHz all the methods have good accuracy, but the frequency increases the error drastically, between 5% to 10% and more over the100 GHz. This is due to the lumped parasitic assumption (especially the series lumped elements) in the topology.

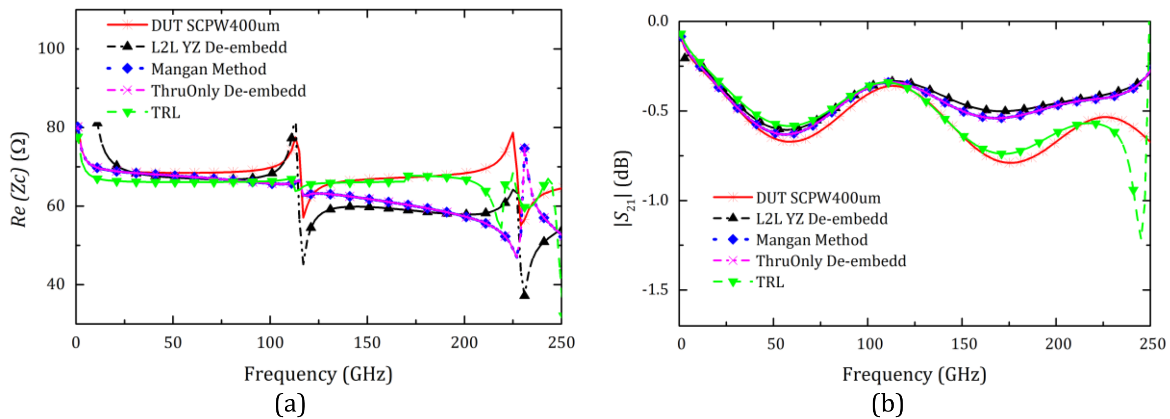


Figure 2.34. Benchmarking (a) Characteristic Impedance of the line (b) Transmission coefficient of DUT

2.5 Conclusion

The benchmarking and comparison between the methods are evaluated based on the results presented in the previous sections (Figure 2.33 and Figure 2.34) and presented in Table 2.2. The limitations of each method briefly described in section 2.3.7. Considering all the lumped equivalent method (Vandamme) is less accurate for millimeter wave frequencies. Cascaded Matrix with Lumped Equivalent methods (L-2L YZ method, Mangan method and Thru only de-embedding) are limited to 100 GHz. Considering the cascaded matrix based methods, L-2L Kolding give good accuracy until 100 GHz, because the pad parasitics are symmetrical. **TRL is highly accurate for a wide band of frequency, but it has limitation over unknown characteristic impedance parameter and band limited operation.** Comparing the de-embedding structures, Vandamme method and TRL uses the maximum number of de-embedding structures.

In conclusion, we describe the characteristics of a good de-embedding method. Since we are looking for a wide band de-embedding method, the method should work over a wide range of frequencies, especially from low frequency to millimeter wave and sub-millimeter wave range approximately 250GHz. In addition, a good de-embedding method should able to de-embed any kind of parasitics, from a single pad to pad-interconnect parasitics. The "short devices" such as transistors, inductors, other passive/active devices utilize both pad and interconnect/accesslines.

From the previous results, it is clear that a good de-embedding method preferred not have any lumped assumptions or any symmetrical assumptions. It is good not to have frequency limitation theoretically and practically.

A good de-embedding method should able to take into account of,

- Effects of contact pads, interconnects and substrate.
- Transitions between pad and interconnect, or pad and DUT, or interconnect and DUT should be taken into account
- Accuracy, cost and reliability of the measurement
    - Over wide range of frequencies: millimeter wave and sub-millimeter wave range
    - Less number of de-embedding structures: smaller area and cost effective

Next chapter studies and explains another de-embedding method called "Half-Thru De-embedding". This method is developed to overcome the above limitations of other de-embedding methods. The method is proven until millimeter wave and sub-millimeter wave frequency with S-CPW transmission line as DUT. Half-Thru de-embedding method is developed to characterize the devices at millimeter wave and sub-millimeter wave frequency range. In addition, we will present a simplified method of Half-Thru de-embedding method called Thru-Load de-embedding method.

De-embedding Methods		De-embedding structures	Frequency Limitation UnKnown Parasitics (Ansys HFSS)		Assumptions/ Limitations
Lumped equivalent circuit Models	Vandamme Method [4]	*Open, Short1, Short2* and *Thru*	< 30 GHz	☹	▪ Lumped approximations ▪ Small Interconnecting lines < λ/10. ▪ Highly depend to the topology
Cascaded Matrix with Lumped Equivalent methods	L-2L YZ Method [11]	TL_1 and TL_2 =2. TL_1	< 100 GHz	☹	▪ Lumped approximations; such as series and parallel lumped elements ▪ Highly depend to the topology
	Mangan Method [12]	*TL Long* and *TL Short*	< 100 GHz	☹	
	Thru Only De-embedding [13]	Thru	< 100 GHz	☹	
Cascaded Matrix Based Models	L-2L Kolding [7],[10]	TL_1 and TL_2 =2. TL_1	<100 GHz	☹	▪ L2L-Kolding: ▪ TRL: Unknown line Impedance value, Band Limited; multiple lines required for wide band
	TRL [2]	*Thru, Reflect* and *Line*(*s*)	> 100 GHz	☺	
	Hernandez Method [16]-[18]	TL_1 and TL_2 > TL_1	< 100 GHz	☹	▪ Symmetrical assumptions

Table 2.2 Benchmarking of different de-embedding methods with Unknown parasitics (HFSS)

2.6 References

[1] G. Crupi, D. Schreurs, “Microwave De-embedding From Theory to Applications", 2013.

[2] G. F. Engen and C. A. Hoer, “Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer,” *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 12, pp. 987–993, Dec. 1979.

[3] B. Zhang, Y.-Z. Xiong, L. Wang, S. Hu, and J. L.-W. Li, “On the De-Embedding Issue of Millimeter-Wave and Sub-Millimeter-Wave Measurement and Circuit Design,” *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 2, no. 8, pp. 1361–1369, Aug. 2012.

[4] E. P. Vandamme, D. M. M. Schreurs, and C. van Dinther, “Improved Three-Step De-Embedding Method to Accurately Account for the Influence of Pad Parasitics in Silicon On-Wafer RF Test-Structures,” *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 737–742, Apr. 2001.

[5] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, “An Improved De-Embedding Technique for On-Wafer High-Frequency Characterization,” in *Bipolar Circuits and Technology Meeting, 1991., Proceedings of the 1991*, pp. 188–191, 1991.

[6] H. Cho and D. E. Burk, “A Three-Step Method for the De-Embedding of High-Frequency S-Parameter Measurements,” *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1371–1375, Jun. 1991.

[7] T. E. Kolding, “A Four-Step Method for De-Embedding Gigahertz On-Wafer CMOS Measurements,” *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 734–740, Apr. 2000.

[8] A. Hamidipour, M. Jahn, F. Starzer, X. Wang, and A. Stelzer, “On-Wafer Passives De-Embedding Based on Open-Pad and Transmission Line Measurement,” in *2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 102–105, 2010.

[9] X. S. Loo, K. S. Yeo, K. W. J. Chew, L. H. K. Chan, S. N. Ong, M. A. Do, and C. C. Boon, “A New Millimeter-Wave Fixture De-embedding Method Based on Generalized Cascade Network Model,” *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 447–449, Mar. 2013.

[10] Y. Lin, H.-T. Yen, H.-H. Chen, C.-P. Jou, C.-W. Kuo, M.-C. Jeng, F.-L. Hsuch, C.-H. Hsiao, and G.-W. Huang, “An extended de-embedding method for on-wafer components,” in *2012 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, pp. 166–168, 2012.

[11] N. Li, K. Matsushita, N. Takayama, S. Ito, K. Okada, and A. Matsuzawa, “Evaluation of a Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design,” *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.,* vol. E93-A, no. 2, pp. 431–439, Feb. 2010.

[12] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, “De-Embedding Transmission Line Measurements for Accurate Modeling of IC Designs,” *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[13] Y. N. Yosuke Goto, “New On-Chip De-Embedding for Accurate Evaluation of Symmetric Devices,” *Jpn. J. Appl. Phys.*, vol. 47, pp. 2812–2816, 2008.

[14] J., R.F. Bauer and P. Penfield, “De-Embedding and Unterminating,” *IEEE Trans. Microw. Theory Tech.*, vol. 22, no. 3, pp. 282–288, Mar. 1974.

[15] N. Erickson, J. Fan, X. Gao, B. Achkir, and S. Pan, “De-Embedding Techniques for Transmission Lines: An Application to Measurements of On-Chip Coplanar Traces,” in *2014 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, pp. 660–666, 2014.

[16] J. A. Reynoso-Hernandez, “Unified method for determining the complex propagation constant of reflecting and nonreflecting transmission lines,” *IEEE Microw. Wirel. Compon. Lett.,* vol. 13, no. 8, pp. 351–353, Aug. 2003.

[17] J. E. Zúñiga-Juárez, J. A. Reynoso-Hernández, J. R. Loo-Yau, and M. C. Maya-Sánchez, “An improved two-tier L-L method for characterizing symmetrical microwave test fixtures,” *Measurement*, vol. 44, no. 9, pp. 1491–1498, Nov. 2011.

[18] H. J. Saavedra-Gomez, J. R. Loo-Yau, P. Moreno, B. E. Figueroa-Resendiz, and J. A. Reynoso-Hernandez, “On-wafer CMOS transistors de-embedding method using two transmission lines of different lengths,” in *2012 IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* pp. 417–420, 2012.

[19] R. Torres-Torres, G. Hernandez-Sosa, G. Romo, and A. Sanchez, “Characterization of Electrical Transitions Using Transmission Line Measurements,” *IEEE Trans. Adv. Packag.*, vol. 32, no. 1, pp. 45–52, Feb. 2009.

[20] Advanced Design System (ADS), ADS 2014.01, Keysight EEsof EDA, Keysight Technologies.

[21] ANSYS® HFSS, Release 14.0, ANSYS, Inc.

[22] Chevalier, P.; Meister, T.F.; Heinemann, B.; Van Huylenbroeck, S.; Liebl, W.; Fox, A.; Sibaja-Hernandez, A.; Chantre, A., "Towards THz SiGe HBTs," *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011 IEEE* , vol., no., pp.57,65, 9-11 Oct. 2011.

[23] Chevalier, P.; Lacave, T.; Canderle, E.; Pottrain, A.; Carminati, Y.; Rosa, J.; Pourchon, F.; Derrier, N.; Avenier, G.; Montagne, A.; Balteanu, A.; Dacquay, E.; Sarkas, I.; Celi, D.; Gloria, D.; Gaquiere, C.; Voinigescu, S.P.; Chantre, A., "Scaling of SiGe BiCMOS Technologies for Applications above 100 GHz," *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2012 IEEE* , vol., no., pp.1,4, 14-17 Oct. 2012.

[24] A.-L. Franc, E. Pistono, N. Corrao, D. Gloria, and P. Ferrari, “Compact high-Q, low-loss millimeter wave transmission lines and power splitters in RF CMOS technology,” in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, pp. 1–4, 2011.

[25] A.-L. Franc, E. Pistono, D. Gloria, and P. Ferrari, “High-Performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Band pass Filters,” *IEEE Trans. Electron Devices,* vol. 59, no. 5, pp. 1219–1226, May 2012.

[26] V. Velayudhan, E. Pistono, and J.-D. Arnould, “Half-Thru de-embedding method for millimeter-wave and sub-millimeter-wave integrated circuits,” in *Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph.D. Research in*, pp. 1–4., Jul. 2014.

[27] V. Velayudhan, E. Pistono, and J.-D. Arnould, “Comparison of De-embedding Methods for Long Millimeter and Sub-Millimeter-Wave Integrated Circuits,” presented at the *JCMM 2014, 13èmes Journées de Caractérisation Microondes et Matériaux*, Nantes, 24-26 March, 2014.

3. Half-Thru De-embedding

This chapter explains the studies on a novel de-embedding method called "Half-Thru De-embedding". This method has been developed to overcome the limitations of other de-embedding methods. As we explained in the previous chapter, the accuracy of the current methods is restricted by frequency and other measurement parasitic parameters. Half-Thru de-embedding method is developed to characterize the devices in millimeter wave and sub-millimeter wave frequency ranges. This chapter includes the theoretical analysis and proof of the method until millimeter wave and sub-millimeter wave frequencies using both electrical model and EM model. The method is tested and validated for Slow-Wave Coplanar Wave Guide (S-CPW) transmission line modeled in Ansys HFSS. Further, we explain the restrictions of this method and the solutions for it. Apart from the Half-Thru de-embedding method, we present a simplified method of Half-Thru de-embedding method called Thru-Load de-embedding method. This chapter also includes the benchmarking and comparison with TRL.

3.1 Half-Thru De-embedding

Half-Thru de-embedding method is a method [1], [2] based on matrix calculation without any electrical model. The model of the measured Device Under Test (DUT) to perform the Half-Thru de-embedding is shown in Figure 3.1.

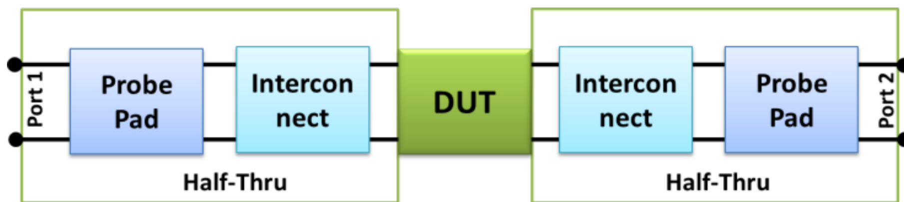


Figure 3.1. Parasitics model of Half-Thru De-embedding method

In this method the pad- interconnects parasitics are modeled as "Half-Thru" sections. The aim of this method is to well take the parasitic effects into "Half-Thru" sections (pad and on-wafer feeding interconnect). In DUT measurement, we can have either pads or both pads and interconnect parasitics depending on the measurement model. To de-embed the parasitics we use three de-embedding structures, two *Transmission Lines* and a *Load*. These de-embedding structures must be considered to obtain the intrinsic characteristics of the DUT.

3.2 Theoretical Analysis

First, this method must consider two de-embedding structures called TL_1, and TL_2 (two *transmission lines*), in order to obtain the real parasitic effects induced by each Half-Thru sections, shown in Figure 3.2.

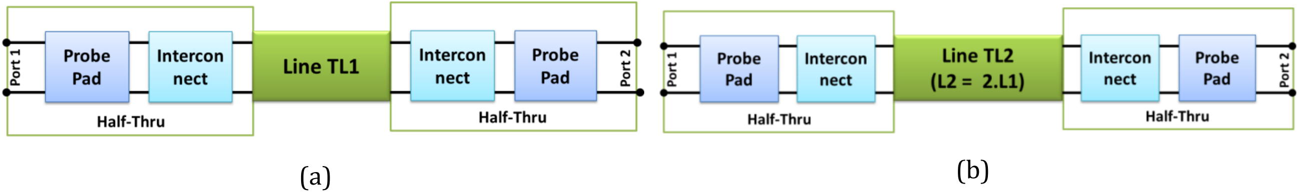


Figure 3.2. De-embedding structures (a) TL_1 (b) TL_2

Each of these test fixtures TL_1, and TL_2 consists of the on-wafer pads with a transmission line of same characteristic impedance Zc, propagation constant γ. TL_1 has a physical length, L_1 and TL_2 has a physical length, L_2; where L_2 = $2.L_1$. The equivalent model of a *Thru* can be obtained from the *ABCD* Matrix of TL_1, and TL_2 by converting the [*S*] matrices of TL_1 and TL_2 into [*ABCD*] matrices [3]-[5]. This procedure is illustrated in the following equation (3.1).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Thru} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{TL_1} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{TL_2}^{-1} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{TL_1} \tag{3.1}$$

The obtained *Thru* from this operation is shown in Figure 3.3.

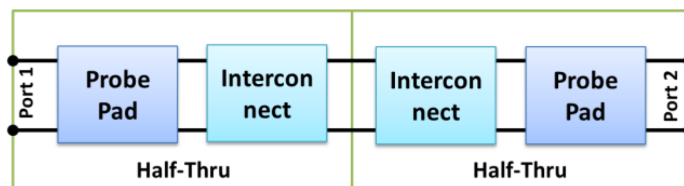


Figure 3.3. Thru from TL_1 and TL_2

The signal flow graph of the *Thru* is shown in Figure 3.4 obtained from the two *Transmission Lines*.

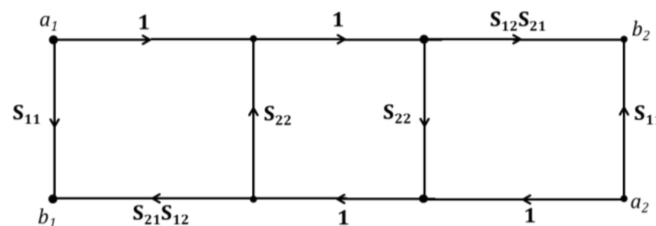


Figure 3.4. Signal flow graph of *Thru*

From the signal flow graph theory (Masons Rule) [6], we can derive the transfer functions of the *Thru*,

$$S_{11T} = S_{11} + \frac{S_{21}S_{12}S_{22}}{1 - S_{22}^2} \tag{3.2}$$

$$S_{21T} = \frac{S_{21}S_{12}}{1 - S_{22}^2} \tag{3.3}$$

Where, S_{11T} and S_{21T} are the transmission coefficient and the reflection coefficient obtained from the *Thru*.

Then, to derive the equivalent model of the Half-Thru (pad and accessline) of the DUT, it is necessary to measure the reflection coefficient Γ_{Load} of the *Load*. This reflection coefficient of the *Load* determines the point of reflection in the center of the *Thru*, which is our "Half-Thru". Therefore, it is better to use a load value which differs from the pad/interconnecting line characteristic impedance. In this case, for example, the Half-Thru is loaded with a *known Load* of Z_{Load} of 100 Ω, shown in Figure 3.5 to derive the "Half-Thru" (pad and accessline) of the DUT [7], [8].

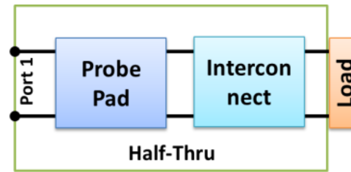


Figure 3.5. Half-Thru loaded with a known load Z_{Load}

The signal flow graph of the *Load*, Z_{Load}, is shown in Figure 3.6.

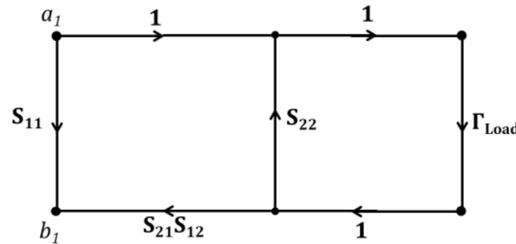


Figure 3.6. Signal flow graph of *Load*

Considering the signal flow graph theory,

$$S_{11L} = S_{11} + \frac{S_{21}S_{12}\Gamma_{Load}}{1 - S_{22}\Gamma_{Load}} \tag{3.4}$$

where S_{11L} is the reflection coefficient obtained from the Half-Thru loaded by a known *Load*, Z_{Load}. From the above equations (3.2), (3.3) and (3.4) we can extract the effects of the pad and accessline from the *Thru* and *Load*. The resultant S-parameters of the parasitics are given below,

$$S_{22} = \frac{S_{11L} - S_{21T}.\Gamma_{Load} - S_{11T}}{S_{11L}.\Gamma_{Load} - S_{11T}.\Gamma_{Load} - S_{21T}} \quad (3.5)$$

$$S_{21} = S_{12} = \sqrt{S_{21T}.(1 - S_{22}^2)} \quad (3.6)$$

$$S_{11} = S_{11T} - S_{21T}.S_{22} \quad (3.7)$$

The *'L'* and *'T'* in the equations indicate the known *Load* and *Thru* (obtained from the measure of TL_1 and TL_2).

Simulations and analysis are performed with **known electrical model (Agilent Advanced Design System (ADS)** [9]**)** and **unknown EM model (Ansys HFSS** [10]**)** parasitics to prove the method.

3.3 Proof of Concept with Known Electrical Model Parasitics

To verify the Half-Thru de-embedding method we realize the de-embedding structures and the DUT using ADS. An ideal transmission line with characteristic impedance of 30 Ω and 2 mm length is chosen as the DUT, which is shown in Figure 2.13(see Chapter 2, section 2.3). The actual measurement model of the transmission line includes parasitics of the pad/interconnects. The parasitics of the pad and interconnects can be modeled from simple parallel capacitance to the complicated lumped/ cascaded models [12]-[18].

As explained in the **Chapter 2,** section2.3 the lumped parasitics "*Pi- model*", distributed parasitics model "*TL*" and distributed with lumped parasitics model are considered as difficult parasitics to de-embed for different de-embedding methods. Except TRL [11], all other lumped equivalent circuit methods [12]-[15] and cascaded matrix with lumped equivalent models [16]-[18] are failed to de-embed the parasitics over millimeter wave frequencies band. Nevertheless, the limitations of the TRL, such as the characteristic impedance knowledge and the multiple lines (space on wafer) create a space for new method, which should work on all kinds of parasitics models. Therefore, the key idea is to prove that the Half-Thru de-embedding method is efficient with all these parasitics. The simulations and the de-embedding are performed until 250 GHz.

3.3.1 Simulation and De-embedding Results with Known Parasitics using ADS

To perform the Half-Thru de-embedding method we need to have three de-embedding structures such as *two Lines* and a *Load* loaded at the "Half-Thru" parasitics. These de-embedding structures are simulated according to the parasitics of the measurement. For example, de-embedding structures with lumped parasitics are shown in Figure 3.7. The *Line* de-embedding structure is shown in Figure 3.7(a),

where, "*TL*" can be replaced by both TL_1, and TL_2. Figure 3.7(b) shows Half-Thru loaded with a known *Load* de-embedding structure, Z_{Load}, where, Z_{Load} is taken as 100 Ω. These lumped parasitics can be replaced by distributed parasitics and distributed with lumped parasitics to analyse the Half-Thru de-embedding method.

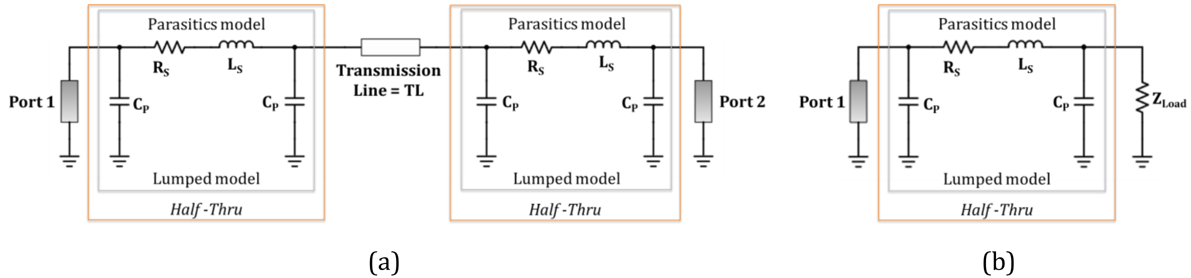


Figure 3.7. (a) Line De-embedding structure (b) Load

The characteristic impedance of the de-embedded transmission line is calculated from the *ABCD* matrix shown in Figure 2.23. Considering the de-embedded results, the characteristic impedance plot shows a very good agreement with the DUT alone, which is the ideal transmission line. The de-embedding result shows a very good accuracy with respect to the DUT alone all over the frequency range, until 250 GHz for all parasitics models.

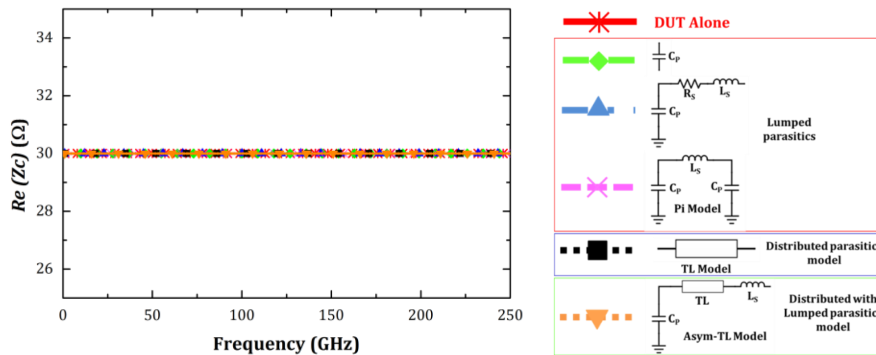
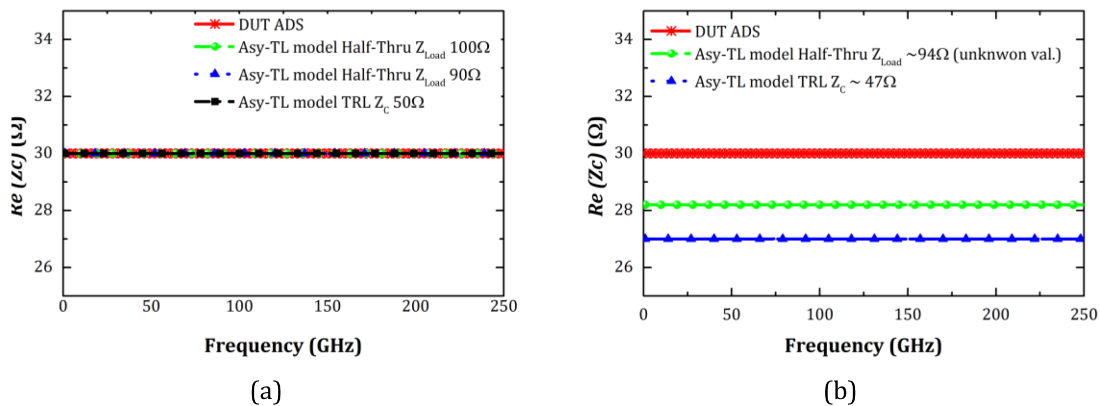


Figure 3.8. Half-Thru De-embedding: Characteristic impedance of the DUT

This proves Half-Thru de-embedding method can de-embed all difficult parasitics such as "*Pi- model*" lumped, distributed "*TL*" and distributed with lumped parasitics or *asymmetrical-TL* Parasitics. Indeed, Half-Thru de-embedding method allows considering all the parasitics into "Half-Thru" model. Therefore, any kind of parasitics, such as the lumped model to the complex distributed with lumped model parasitics can be modeled as "Half-Thru". Moreover, this method uses the scattering parameter based calculations, so theoretically there is no frequency limitation. Since the method considers the parasitics as "Half-Thru", there are no lumped circuit equivalent ([12]-[16]) models or symmetrical assumptions ([17], [18]). The major challenge of this method is to find the value of the *Load* de-embedding structure used for Half-Thru de-embedding. Since ADS uses electrical model, the *load* value is constant and well known, and it is measured in the Half-Thru de-embedding procedure.

Because of these reasons the Half-Thru de-embedding method, performed over the ADS simulations gives the perfect results over a wide range of frequency. Comparing with TRL [11], the major advantage of this method is that it does not require the characteristic impedance of the line and the number of de-embedding structures is less. TRL require multiple lines to cover the entire range of the frequency.

Comparison of the Half-Thru de-embedding and TRL for distributed with lumped parasitics is shown in Figure 3.9. As shown in Figure 3.9(a), the Half-Thru de-embedding has greater accuracy over the entire frequency range compared with the DUT alone or ideal transmission line, if the load (Z_{Load}) value is known. Similarly TRL shows a very good accuracy with respect to the DUT ADS with the known transmission line characteristic impedance, where this value is obtained from the simulation.



(a) (b)

Figure 3.9. Half-Thru De-embedding and TRL: Comparison (a) Known parameters (b) Unknown parameters

As shown in Figure 3.9(b), if there is any change or process variation of impedance in the fabricated *Line*, and the value of Z_{Load}, the de-embedded result can be less accurate. De-embedding is performed with 6 % inaccuracy in unknown parameters for TRL (value of characteristic impedance) and Half-Thru de-embedding (value of Z_{Load}). The result shows that the TRL has about 3 % more error than Half-Thru de-embedding. In addition, these value of the characteristic impedance of the line and Z_{Load} are obtained from simulation rather than real measurement.

3.3.2 Conclusion of Proof of Concept with ADS

Half-Thru de-embedding method validity is proved using known electrical parasitics by considering ADS simulation. Half-Thru de-embedding method is able to de-embed any kind of parasitics, either all lumped, distributed or both, beyond 100 GHz. The results show good accuracy if the *Load* value is known all over the frequency band in millimeter wave and sub-millimeter wave range. This value can be measured rather than the simulated value of the characteristic impedance used in TRL. Compared to TRL, the number of de-embedding structures is less, thus method is cost effective. TRL is also giving good results, but the characteristic impedance of the line Z_C must be known *a priori*, which is a

limitation while considering a DUT itself as a transmission line. In addition, TRL has about 3 % more error than Half-Thru de-embedding considering similar inaccuracy in unknown parameters (*Zc* for TRL and Z_{Load} for Half-Thru de-embedding). Now, the detailed and realistic study using a 3D electromagnetic tool (Ansys HFSS) of the Half-Thru de-embedding will be explained in the coming sections of this chapter.

3.4 Proof of Concept with Unknown EM Model Parasitics

The effective analysis of the Half-Thru de-embedding method is done by using 3D fullwave electromagnetic Simulator by Ansoft HFSS v14 [10]. In this analysis, the parasitics are not known, a *priori*, which are close to the real scenario. The DUT is considered as an S-CPW transmission Line [21], [22], with a length of 400 µm, modeled in BiCMOS 55nm technology. The dimensions of the coplanar strips are given by a signal width of the S-CPW W = 4 µm, a ground width Wg = 12 µm and a gap between the signal and ground G = 40 µm. The fingers have a strip width of SL = 0.16 µm and are separated by a distance of SS = 0.2 µm. The characteristic impedance of the line is about 70 Ω.

The de-embedded results of the S-CPW transmission line can be analysed from its characteristics such as the transmission and reflection coefficient, characteristic impedance of the transmission line and attenuation coefficient.

3.4.1 Measurement Setup and De-embedding Structures

The measurement setup of the device under test (S-CPW Transmission line) ([21], [22]) is shown in Figure 3.10. The measurement includes the pads to connect the DUT with the signal. These rectangle pads are 50 µm long, 35 µm wide and with a pitch of 50 µm depending on the dimensions. The DUT can be connected directly to the pad or connected using both pad and accessline. Here we use S-CPW accessline with a length of 100 µm and characteristic impedance of 50 Ω to connect from pad to DUT. **The reasons for using S-CPW accesslines are explained in further section 3.4.3.** Here the parasitics effects from both pad and S-CPW accessline are effectively considered as a “Half-Thru”. The coupling effects of probes and interconnections are not taken into account, since the device is long.

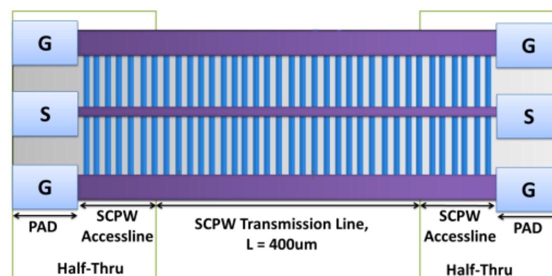
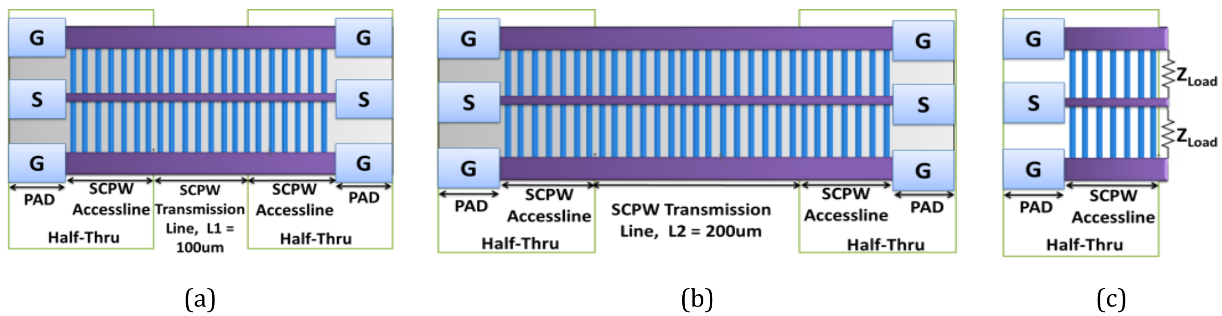


Figure 3.10. Measurement setup of Half-Thru De-embedding

The de-embedding structures needed to perform Half-Thru de-embedding are TL_1 with length of 100 µm, TL_2 with the length of 200 µm (2. L_1) with S-CPW accessline and the *Load* (Z_{Load}) of 100 Ω which is loaded at "Half-Thru" [1], [2]. The de-embedding structures are shown in Figure 3.11 (a), (b) and (c) respectively. The TL_1, and TL_2 are used to obtain the *thru*, which includes two Half-Thru sections. The "Half-Thru", can be obtained from the *thru*, calculated from the *two lines* and the *load* (Z_{Load}) of 100 Ω is used. The *load* (Z_{Load}) value is chosen different from the characteristic impedance of accesslines, which is 50 Ω, that will help us to find the better reflect point of the *thru*.



(a) (b) (c)

Figure 3.11. (a) TL_1 (b) TL_2 ($L_2 = 2.L_1$) (c) *Half-Thru Load* (Accessline line+Load)

3.4.2 Simulation and Results: Benchmarking and Comparison with TRL

The comparison between the DUT alone (simulated without any parasitics: S-CPW transmission line), the de-embedded result of S-CPW transmission line using the Half-Thru de-embedding and TRL [11] is plotted. In order to understand the performance of the de-embedding, the S-parameters, the characteristic impedance and attenuation of the S-CPW Transmission line are calculated. The plots S_{11} and S_{21} vs frequency are shown in Figure 2.33(a) and Figure 2.33(b) respectively. The *Zc* and the α of the S-CPW transmission line vs frequency are shown in Figure 2.33(c) and Figure 2.33(d) respectively. From the plots, it is clear that **Half-thru de-embedding and TRL show comparable** results in the entire band. **Comparing with TRL, the major advantage of this method is that, it does not require the characteristic impedance of the line to set the reference plane and the number of de-embedding structures is less.** Considering TRL, it requires minimum three de-embedding structures, *Thru, Reflect* and *Line*. Since a broad range (from very low frequency up to 250 GHz) de-embedding method is expected, TRL requires multiple lines to cover the entire band, thus costly. Another major advantage is the transition between the pad and interconnect can easily and efficiently modeled by using Half-Thru de-embedding method.

The **major challenge** of this method is to find the load value of the *load* de-embedding structure used for Half-Thru de-embedding. The fabrication of a perfect load is impossible for millimeter wave and sub-millimeter wave frequencies, because of the parasitics associated with the technology, and other modeling parameter of the *load*. So it is important to know the exact *load* value to perform a very good de-embedding. The *load* value variation study is performed after the accessline study.

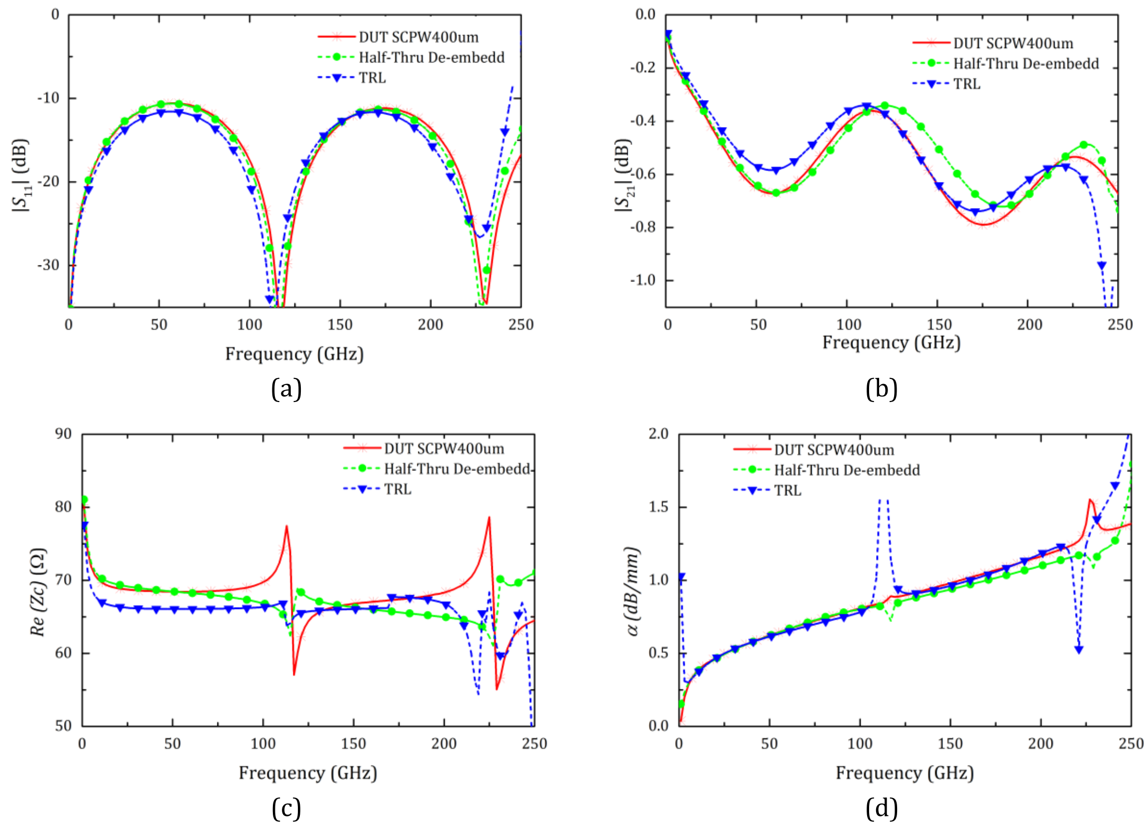


Figure 3.12. Half-Thru De-embedding (a) Reflection coefficient (S_{11}) (b) Transmission coefficient (S_{21}) (c) Characteristic impedance (Zc) (d) Attenuation coefficient (α)

Note: The resonance points are avoided, while calculating the percentage of error of Zc and α, because the resonance points are due to the mathematical limitation (see Chapter 2 section 2.4.3, Figure 2.33(*d*)).

3.4.3 Simulation with and without accessline

As we explained in the state of the art (see Chapter 1, Section 1.1.6), the measurement model of the DUT can be modeled in different ways. There are two kinds of de-embedding devices, (1) directly connected to the PAD [16], [20] or, (2) connected with both PAD and interconnecting lines/accesslines [17],[19]. Since our DUT is a planar transmission line, we can have both configurations. If we try to de-embed the transistor or any small passive device, it is necessary to have an accessline, to avoid the cross coupling in the measurement. These models can affect the de-embedding results. S-CPW measurement model with and without accessline for a pitch of the pad 50 µm is shown in Figure 3.13.

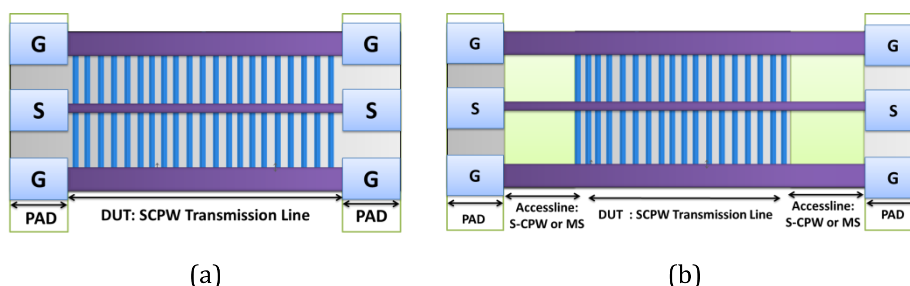


Figure 3.13. S-CPW measurement model (a) without accessline (b) with accessline (MS/S-CPW)

Here we compare the results of the Half-Thru de-embedding with and without the accesslines. Both microstrip and S-CPW accesslines are chosen to evaluate the problem of discontinuity in the field at the point of excitation for S-CPW. This simulation will help us to explain the importance of similar accesslines as DUT.

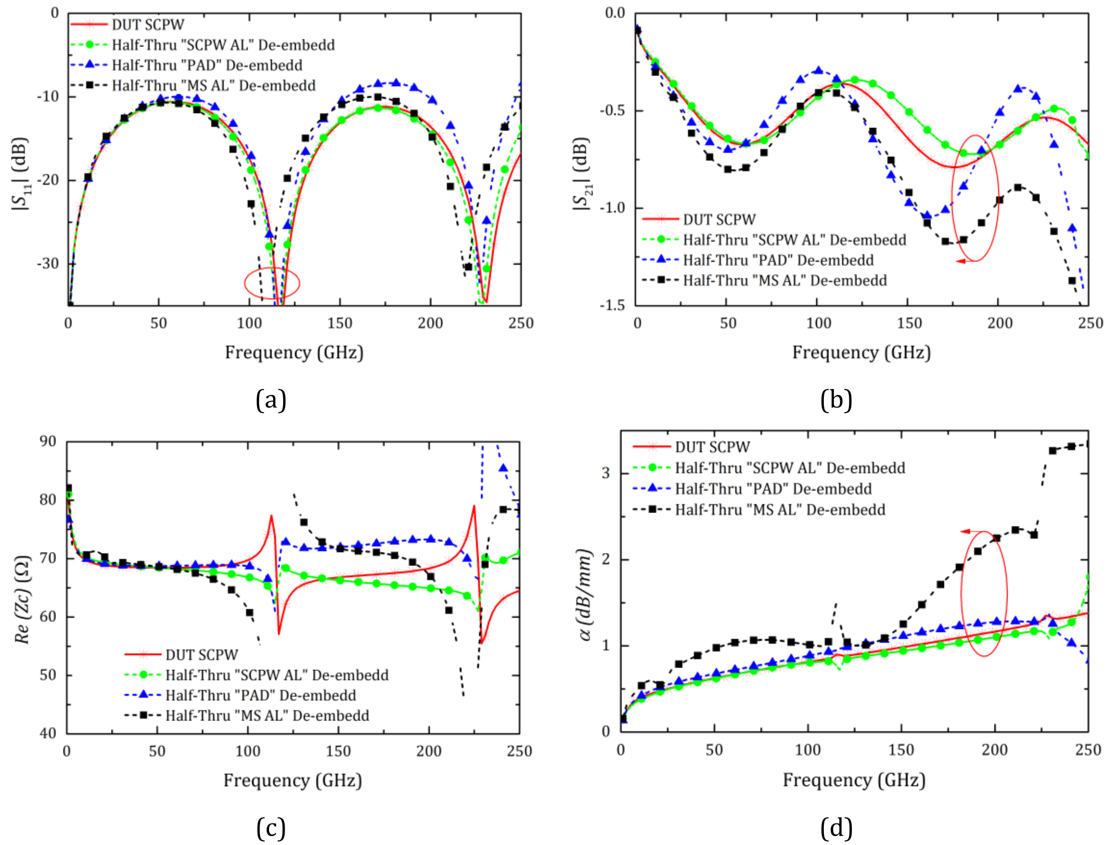


Figure 3.14. Half-Thru de-embedding (a) Reflection coefficient (S_{11}) (b) Transmission coefficient (S_{21}) (c) Characteristic impedance (Zc) (d) Attenuation coefficient (α)

The plots (see Figure 3.14) S_{11}, S_{21}, Zc and α show the de-embedded results using Half-Thru de-embedding method compared with DUT alone (simulated without any parasitics: S-CPW transmission line). Considering the de-embedded results of the different measurement models, the DUT is connected using S-CPW accessline (green colour line), DUT is directly connected to the pad (blue colour line) and the DUT is connected using MS accessline (black colour line) are compared with the DUT alone (red colour line). The Zc for the Half-Thru de-embedding method with S-CPW accessline measurement model shows a better agreement with the DUT alone until 250 GHz, than DUT with MS accessline and directly connected. The other measurement models have variation over 5% at higher frequencies, above 100 GHz. **From the S_{11}, all the de-embedded results of all the measurement models show good results, but there is a frequency shift, that is marked (red circle) for the MS accessline model. This is due to the transition problems due to microstrip to S-CPW.** Considering the S_{21} and α, it is clearly visible that the results are less accurate for the *no*

accessline model (DUT is directed connected with pad) and the MS accessline model, over 100 GHz, this is also due to the transition problem, which is explained above.

From these results, it is clear that a better de-embedding for S-CPW is obtained with S-CPW accessline. Indeed, if the DUT is directly connected to the pad without interconnects and with the MS accessline, the discontinuity between the pads/accessline and the DUT will not be well taken into account. This will affect the accuracy of the de-embedding, especially for very high frequencies; a good de-embedding requires a continuity of propagated waves in between the pad and DUT. The field of the accessline should be continuous with the field of the DUT; any discontinuity in this case will affect the accuracy of de-embedding, at higher frequencies ([23], [25], [26]). Since the field is continuous, there is less probability to have the errors due to the transitions. From these results, we can conclude that the field should be continuous or same as the DUT at the point of excitation or in front of the DUT.

3.4.4 Effect of the Load Value Analysis

The limitation and the challenge of the Half-Thru de-embedding method is to well-known its load value. The value of the load embedded in the de-embedding structure can affect the accuracy of the Half-Thru de-embedding. With known *load* value, Half-Thru de-embedding have good accuracy, but in the actual case the value of the *load* can vary with the frequency. Since the frequency increases the load value cannot be a pure resistance, it can have inductive or capacitive reactance. Here we analyse, how much variation can happen for the Half-Thru de-embedding with the value of the load ±10% (worst case), when it is unknown.

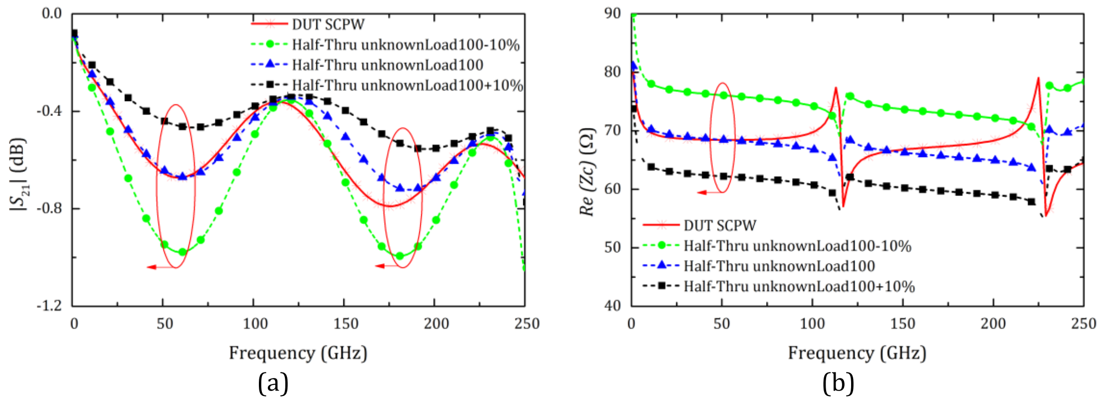
The error is calculated as follows,

$$Error\ |S_{21}| = \left| \frac{|S_{21}|\ (DUT\ Alone) - |S_{21}|\ (Half\ Thru\ De-embedding)}{|S_{21}|\ (DUT\ Alone)} \right| \times 100\% \tag{3.8}$$

$$Error\ |Z_C| = \left| \frac{|Z_C|\ (DUT\ Alone) - |Z_C|\ (Half\ Thru\ De-embedding)}{|Z_C|\ (DUT\ Alone)} \right| \times 100\% \tag{3.9}$$

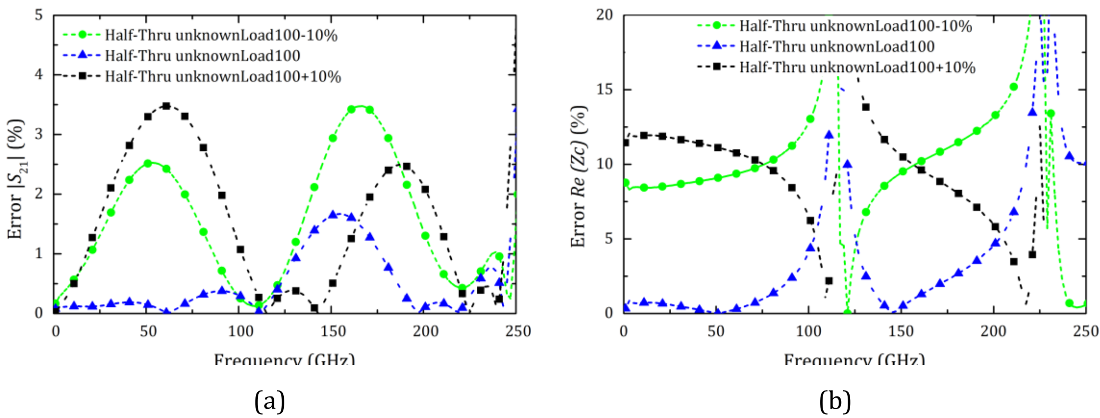
Consider the *Load* at the Half-Thru (parasitic effects of the pad and interconnects) is 100 Ω. Consider a maximum unknown load variation of ±10% with the measured load value (100 Ω) to estimate the accuracy of the Half-Thru de-embedding. The de-embedded results of the Half-Thru de-embedding method with the unknown load variation of ±10% with the measured load value (100 Ω) is compared with DUT alone (S-CPW transmission line). The plots S_{21} and Zc vs frequency are shown in Figure 3.15(a) and Figure 3.15(b) respectively. The S_{21} and the Zc of the de-embed results with unknown load

values, show variation from the de-embedded result with the known load value. Therefore, the unknown load value variation with ±10 %, affect the accuracy of the de-embedding.



(a) (b)

Figure 3.15. Half-Thru de-embedding with ±10 % unknown *Load* value (a) Transmission coefficient (S_{21}) (b) Characteristic impedance (Zc)



(a) (b)

Figure 3.16. Half-Thru de-embedding: % Error with unknown value of load (a) Transmission coefficient $|S_{21}|$ (b) Characteristic impedance (Zc)

Figure 3.16 shows (a) the percentage of error in the S_{21} and (b) shows the percentage of error in the Zc with the load value in Half-Thru de-embedding. The error is calculated using the above equations (3.8) and (3.9). Half-Thru de-embedding method has approximately 0.5 % to 3.5 % errors until 250 GHz for S_{21} and approximately 10 % error for 250 GHz for the Zc. The unknown value of the load can change the value of the reflection (Γ) at the reference point of the Half-Thru parasitics; this makes an error in the de-embedding.

3.4.5 Comparison with Effect of the Characteristic Impedance of the Line of the TRL

Before concluding the error analysis of the load, we analyse the variation of the TRL results with normalizing line impedance Zc of 10% error as same as Half-Thru de-embedding. Figure 3.17 shows the comparison results of TRL and Half-Thru de-embedding with error in its unknown parameters, such as value of *Load* for Half-Thru de-embedding and value Zc for TRL.

Considering *Zc* (see Figure 3.17(b)) of the de-embed results, TRL has about 2% to 3% more error than Half-Thru de-embedding with 10% error in its unknown value. The variation with TRL is about 12% with respect to DUT while considering 10% in its unknown value, but it is less than 10% for Half-Thru de-embedding with respect to the DUT S-CPW. The value of the load can be measured or de-embed, but the normalization impedance *Zc* for TRL is taken from simulation data. The higher error is visible even by considering the magnitude of S_{21} (see Figure 3.17(a)) of the de-embed results. This shows **Half-Thru de-embedding can be comparable with TRL and higher accuracy than TRL. In conclusion, the value of the load in Half-Thru is important, otherwise, it can affect the accuracy, similar as the TRL. Therefore, we need to find a method to obtain the load value to have a good de-embedding method.**

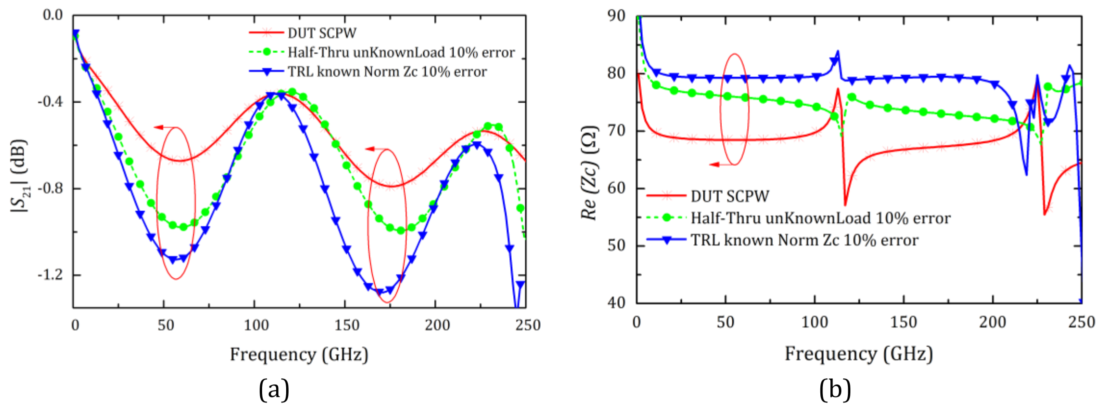


Figure 3.17. TRL and Half-Thru De-embedding with 10% error (a) Transmission coefficient (S_{21}) (b) Characteristic impedance (*Zc*)

3.4.6 Conclusion of Proof of Concept with HFSS

Half-Thru de-embedding method evaluated for S-CPW transmission line using 3D electromagnetic tool Ansys HFSS. Comparison and benchmarking with TRL is performed. Half-Thru de-embedding method shows agreeable results with TRL until 250 GHz. The problem of the accessline is analysed. The studies showed that we need a good propagation in front of DUT. Any discontinuity in this case will affect the accuracy of de-embedding especially at higher frequencies. Also Half-Thru de-embedding and TRL is analysed by considering ±10 % in its unknown values. The results shows, TRL has about 2% to 3% more error than Half-Thru de-embedding. So Half-Thru de-embedding has higher accuracy than TRL, if the *Load* of the Half-Thru de-embedding method is measurable. The value of the *Load* in Half-Thru is important, otherwise it can affect the accuracy. Therefore, we need to find a method to extract the *Load* value to perform a good de-embedding method.

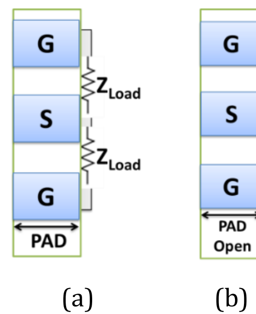
3.5 Extraction of the Load value for Half-Thru De-embedding

The most challenging part of the Half-Thru de-embedding is the extraction of the load value in the load de-embedding test structure. In practice, a fixed value for a resistance is difficult to obtain at

millimeter wave frequencies. The load is a small device and thus we must de-embed the device effectively to get its model. For de-embedding the load values, we can use different de-embedding methods such as (1) Open [12], or (2) Open- Short, ([12]). In addition, we introduce a new method based on *S*-parameters, called (3) Load value extraction with Kolding's Method [17].

3.5.1 Open De-embedding

Open de-embedding methodology [12] is the simplest de-embedding method, which can apply to extract the load value. Open de-embedding uses only "*open*" de-embedding structure.



(a) (b)

Figure 3.18. Open De-embedding (a) *Load* as DUT (b) *Open*

The Load as DUT is fabricated and shown in Figure 3.18(a) and the *open* de-embedding structure is shown in Figure 3.18(b). Since the load is implemented only on the pad, it will have only small parasitics. This parasitics can be removed and the load value can be extracted by using the equation (3.10).

$$Z_{Load} = (Y_{DUT\ measure} - Y_{Open})^{-1} \tag{3.10}$$

Where, $Y_{DUTmesausre}$ is the admittance matrix of the DUT measured with the parasitics and Y_{Open} is the measured *open* de-embedding structure.

3.5.2 Open-Short De-embedding

Open- short de-embedding methodology [12] uses both "*Open*" and "*Short*" de-embedding structures. The Load as DUT is fabricated and shown in Figure 3.19(a); the "*open"* de-embedding structure is shown in Figure 3.19(b) and the "*short*" de-embedding structure shown in Figure 3.19(c). Open-short de-embedding allows de-embedding the both the parallel element and the series element due to the pad parasitics in the DUT measurement. This parasitics can be removed and the load value can be extracted by using the equation (3.11).

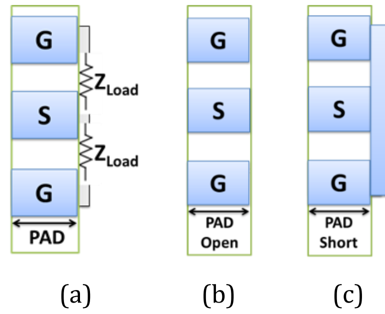


Figure 3.19. Open-Short De-embedding (a) *Load* as DUT (b) *Open* (c) *Short*

$$Z_{Load} = (Y_{DUT\ measure} - Y_{Open})^{-1} - (Y_{Short} - Y_{Open})^{-1} \tag{3.11}$$

Where, $Y_{DUTmesausre}$ is the admittance matrix of the DUT measured with the parasitics, Y_{Open} is the *open* de-embedding structure measured and Y_{Short} is the *short* de-embedding structure measured.

3.5.3 Load value extraction with Kolding's Method

To extract the load value we must consider the Kolding's pad, which is extracted using Kolding's method [17], [18]. To do this, the load is implemented in a pad as DUT as similar as the open and short method, which is shown in Figure 3.20(a). By using L -2L Kolding's method, we can extract the pad parasitics using the two transmission lines. Transmission line TL_1 with a length L_1 and transmission line TL_2 with a length L_2 = 2.L_1 are shown in Figure 3.20(b) and Figure 3.20(c). With these two lines we can extract the *Thru*, shown in Figure 3.20(d). From the *Thru*, by considering Kolding's equations ((2.10) and (2.11)), we can extract the equivalent pad parasitics.

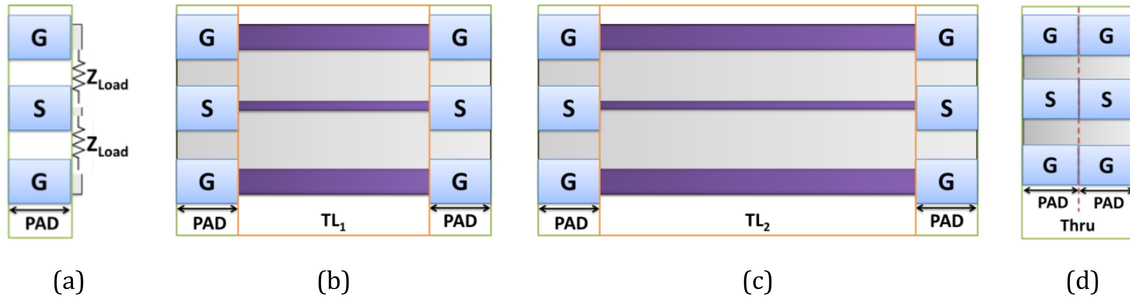


Figure 3.20. (a)*Load* as DUT with pad (b) TL_1 (c) TL_2 (L_2= 2. TL_1) (d) *Thru*

The transfer function of the load can be written by considering the signal flow graph,

$$S_{11L} = S_{11} + \frac{S_{21}S_{12}\Gamma_{Load}}{1 - S_{22}\Gamma_{Load}} \tag{3.12}$$

By considering the equation (3.12), we can extract the Γ_{Load}, shown in equation (3.13). Further, we extract load value, using the equation (3.14).

$$\Gamma_{Load} = \frac{S_{11Load} - S_{11Pad}}{S_{21Pad}^2 + S_{11Load}.S_{11Pad} - S_{11Pad}^2} \tag{3.13}$$

$$Z_{Load} = Z_O \frac{1 + \Gamma_{Load}}{1 - \Gamma_{Load}} \tag{3.14}$$

Where, S_{11Load} is the one port measurement from the DUT implemented in the pad. S_{11Pad} and S_{21Pad} are extracted using the Kolding's method [17] and the *Zo* is the characteristic impedance of the port (50Ω).

The method we developed here does not have the any conversions/approximations to *Y parameters* or the parallel or series elements. Load value can be directly derived using the *S*-parameter functions. One more method based on *S*-parameter described in **APPENDIX - C**, which is less efficient beyond 100 GHz.

3.5.4 Simulation and Results of Load Extraction Methods

All the de-embedding structures and load are modeled using 3D electromagnetic modeling tool Ansys HFSS. To model the load, we used the "Lumped RLC" boundary on HFSS and we considered perfect boundaries for *open* and *short* de-embedding structures. The results of the extracted load value using the de-embedding methods are shown in Figure 3.21. Figure 3.21(a) shows the real part of the load value and the Figure 3.21(b) shows the imaginary part of the load value.

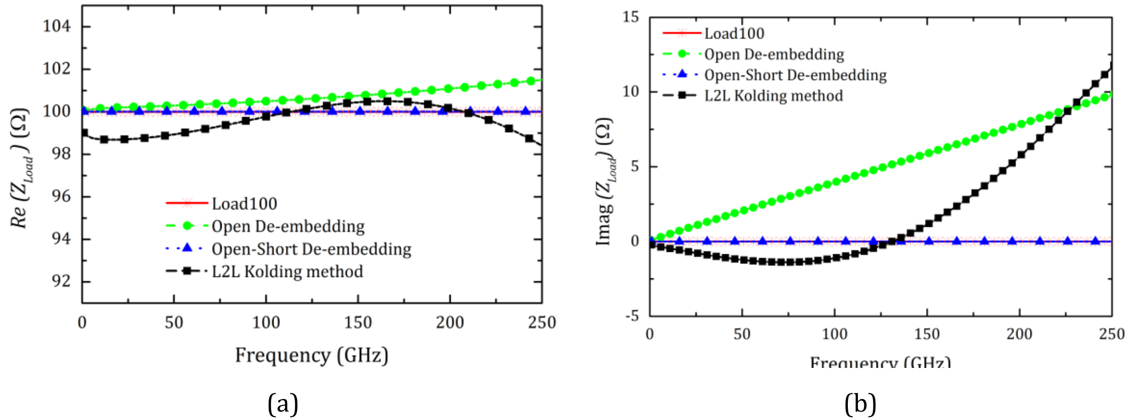


Figure 3.21. Load Value Extraction (a) Z_{Load} (Real) (b) Z_{Load} (imag)

The *"Load* 100" (red line) shows the DUT alone, which is loaded by 100 Ω. The Open de-embedding and Open-Short de-embedding show the good accuracy with respect to the real part of "Load 100" over 250 GHz. In the imaginary part of the load, open de-embedding is not able to de-embed the series parasitics present in the pad. Open-Short de-embedding de-embeds both the parasitics, but for the preliminary analysis, these *open* and *short* de-embedding structures are considered as perfect. In reality it may not be perfect. **Considering the load value extraction with Kolding's method, the real part of load value having about <2 % of error ~ 250 GHz.** The change

in the accuracy is due to the approximations in the Kolding's pad [17], [18]. The real part of the *Load* value is more important than the imaginary part, because, error in the real part makes more impact in the reflection coefficient (*Γ*), than the imaginary part.

In reality, the *short* de-embedding structure in the open-short de-embedding is not a perfect *short*. Consider the *short* is with a slight resistive and the inductive value, for example the *short* is about 1 Ω with 1 pH (worst case in the case of Bi-CMOS 55 nm technology). The comparison with open-short de-embedding with perfect *short* and non-perfect *Short* is shown in Figure 3.22(a) and Figure 3.22(b). The real part of the load value has about 2% error until 200 GHz and about 4% until 250 GHz, because of the imperfection in the short.

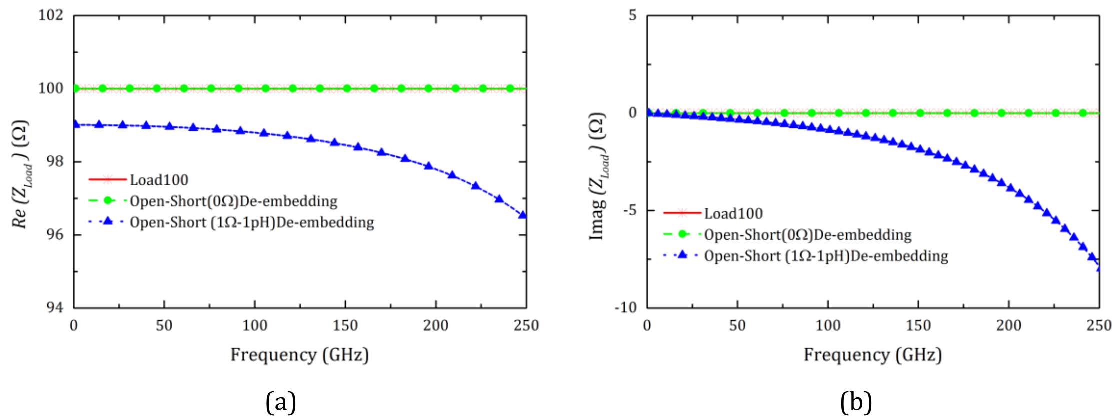
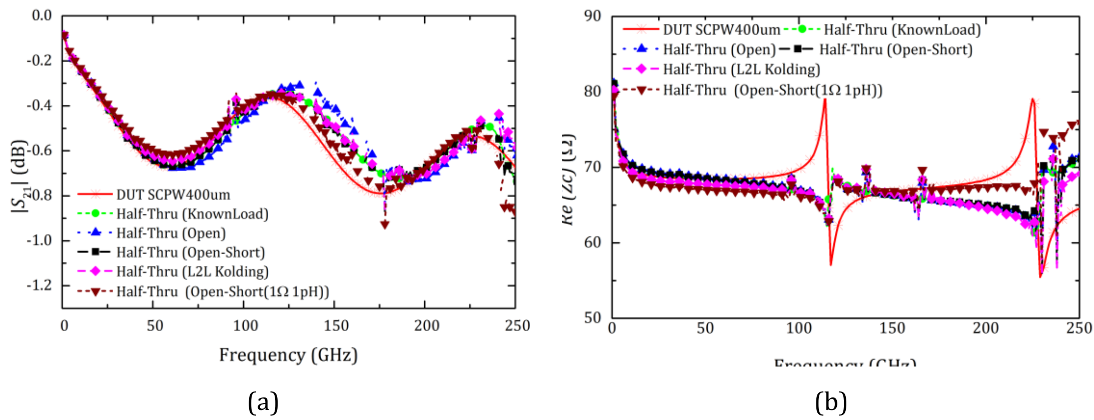


Figure 3.22. Open-Short de-embedding with non –perfect short (a) Z_{Load} (Real) (b) Z_{Load} (imag)

By concluding the accuracy of the method, the Open-Short de-embedding with perfect short gives performant results (Figure 3.21).

3.5.5 Half-Thru De-embedding with Different Load Extraction Methods

S-CPW transmission line with pitch of 50 μm is considered as DUT to de-embed and compare the load extraction methods. Half-Thru de-embedding method with the known load value and the load value extracted by using different load extraction methods are compared to simulated S-CPW transmission line (see Figure 3.23). Considering the de-embedded results (Figure 3.23(a) and Figure 3.23 (b)), load value extracted using open-short de-embedding with non-perfect short value shows greater accuracy with respect to DUT. Load value extracted using other de-embedding methods and the known load value (green line) show 2% to 4% variation in the band of 200 GHz to 250 GHz, which is negligible. Also these methods do not take more wafer place, compared to TRL.



(a) (b)

Figure 3.23. Half-Thru de-embedding with load extraction methods (a) Transmission coefficient (S_{21}) (b) Characteristic impedance (Zc)

3.5.6 Conclusion of Extraction of Load Value for Half-Thru De-embedding

Different de-embedding methods are analysed to extract the load value. Considering the methods for load value extraction open-short de-embedding shows greater accuracy than all the methods. In addition, Half-Thru de-embedding with different load value extraction methods are performed.

3.6 Simplified Half-Thru De-embedding: Thru-Load De-embedding

Thru-Load de-embedding [8] is a simplified Half-Thru de-embedding method. All the principles of the Half-Thru method are applicable for this method. The pad- interconnects parasitics are modeled as Half-Thru sections. The aim of the method is to reduce the number of de-embedding structures and keep the features of the Half-Thru de-embedding method. Since the accessline is enough long to make a direct *Thru*, we can eliminate the two transmission lines, needed to make the Thru. This will save a space on-wafer as well as the cost. This method requires only *Thru* and *Load* de-embedding structures with, load extraction de-embedding methods.

3.6.1 Simulation and Comparison with Half-Thru De-embedding

The de-embedding structures used for Thru-Load de-embedding are the *Thru* with S-CPW accessline and the *Load* (Z_{Load}) of 100 Ω which is loaded at "Half-Thru". The de-embedding structures *Thru* and Load at Half-Thru are shown in Figure 3.24(a) and Figure 3.24 (b) respectively. The "Half-Thru", can be obtained from the *Thru*, and the Load (Z_{Load}) of 100 Ω by using the same equations (3.5), (3.6) and (3.7) of the Half-Thru de-embedding.

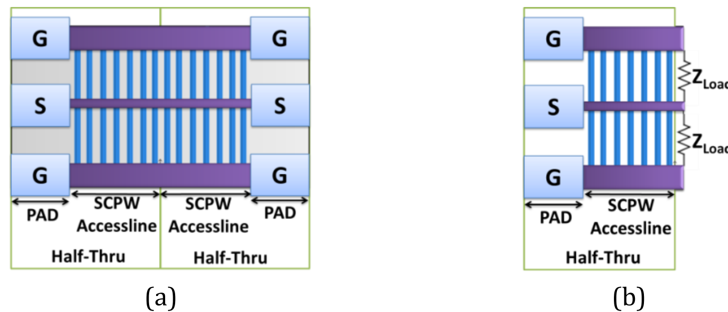


Figure 3.24. Thru –Load de-embedding (a) Thru, (b) Load at Half-Thru

The comparison between the DUT alone (simulated without any parasitics: S-CPW transmission line) and the de-embedded result of S-CPW Transmission line using the Thru-Load de-embedding method and the Half-Thru de-embedding and is plotted (see Figure 3.25). The plots S_{21} and the Zc vs frequency is shown in Figure 3.25(a) and Figure 3.25 (b) respectively. The de-embedded results are compared with the DUT alone, both the Half-Thru de-embedding and Thru-Load de-embedding have good accuracy over >100 GHz until 250 GHz by considering the magnitude of the S_{21} and Zc of the S-CPW transmission line.

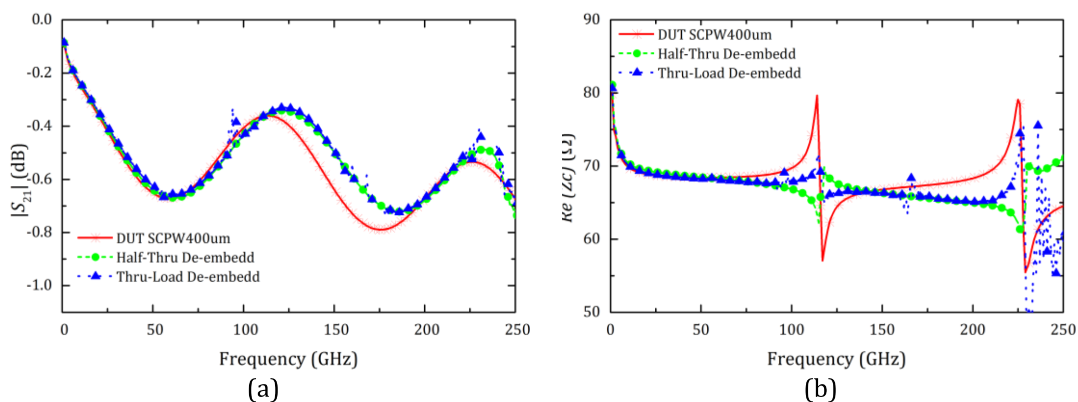


Figure 3.25. Thru-Load De-embedding (a) Transmission coefficient (S_{21}) (b) Characteristic impedance (Zc)

Considering the de-embedded results of Thru-Load de-embedding (blue colour line) and Half-Thru De-embedding (green colour line) have similar/agreeable results entire frequency spectrum. These results show that if the accesslines are enough long to avoid the coupling between the probes/pads, Half-Thru de-embedding can be replace with Thru-Load de-embedding. Thru-Load de-embedding uses one less de-embedding structure than Half-Thru de-embedding. Since we use only one *Thru* instead of lines there is a great achievement in the space on the wafer and cost compared to the Half-Thru de-embedding. In this case, both the methods are suitable for millimeter wave and sub-millimeter wave device characterization.

3.7 Conclusion

An effective de-embedding method (Half-Thru De-embedding) for SCPW Transmission line de-embedding at millimeter and sub-millimeter wave frequencies in the integrated technology is

proposed. Half-Thru de-embedding is compared and benchmarked with TRL; considering TRL is the best and standard method, which is working until millimeter wave and sub-millimeter wave.

The major advantages of this method are,

- High accuracy above >100 GHz, evaluated until 250 GHz; suitable for millimeter wave and sub-millimeter wave applications
- All the parasitics are compromised into "Half-Thru"
- No lumped equivalent models and no assumptions of symmetry
- Well take into account the transition between the pad and the accesslines
- Low cost, considering the very broadband operation

Half-Thru de-embedding method is performed for different accesslines. The studies explain that, **we need a good propagation in front of the device; any discontinuity in this case will affect the accuracy of de-embedding, at higher frequencies.** Therefore, for a transmission line de-embedding, it is better to have the same transmission line as accessline. This proves that **the measurement model of the device under test is also highly important in millimeter wave and sub-millimeter wave device characterization.**

The major challenge of this method is to find the load value of the load de-embedding structure used for Half-Thru de-embedding. We have evaluated different methods to extract the load value for the Half-Thru de-embedding. We have proposed a new S-parameter based method**; load extraction with Kolding's method**. Effectively Half-Thru de-embedding is comparable with the TRL and the number of de-embedding structures is very less. The unknown parameter for the Half-Thru de-embedding is zero, but for the TRL it is important to know the characteristic impedance of the transmission line.

Further, to minimize the size or area of the wafer, we propose a simplified Half-Thru de-embedding method called **Thru-Load de-embedding method**. This helps to reduce the number and the space of the de-embedding structures.

Next chapter compares both simulated and actual de-embedding results of the DUT S-CPW. The DUT and the de-embedding structures fabricated in the AMS 0.35 µm C-MOS technology and BiCMOS 55 nm technology. The chapter includes the study of the variation in the de-embedding results, various on-wafer measurement problems and the possible explanations, which are done by using EM simulation tool Ansys HFSS. In addition, the chapter includes the study of both Half-Thru de-embedding and Thru-Load de-embedding for millimeter wave frequencies with different parameters. Comparison and benchmarking with different methods also included in the chapter.

3.8 References

[1] V. Velayudhan, E. Pistono, and J.-D. Arnould, "Half-Thru de-embedding method for millimeter-wave and sub-millimeter-wave integrated circuits," in *Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph.D. Research in*, pp. 1–4, Jul. 2014.

[2] V. Velayudhan, E. Pistono, and J.-D. Arnould, "Comparison of De-embedding Methods for Long Millimeter and Sub-Millimeter-Wave Integrated Circuits," presented at the *JCMM 2014, 13èmes Journées de Caractérisation Microondes et Matériaux*, Nantes, 24-26 March, 2014.

[3] David M. Pozar, Microwave Engineering, 4th Edition Dec. 2011.

[4] S. J. Orfanidis, Electromagnetic Waves and Antennas, 1st Edition, 2010.

[5] R. E. Collin, "Foundations for Microwave Engineering", 2nd Edition . 1992.

[6] S. J. Mason, "Feedback Theory-Further Properties of Signal Flow Graphs," *Proc. IRE*, vol. 44, no. 7, pp. 920–926, Jul. 1956.

[7] J. M. Song, F. Ling, W. Blood, E. Demircan, K. Sriram, G. Flynn, K.-H. To, R. Tsai, Q. Li, T. Myers, M. Petras, and A. Dengi, "De-embedding techniques for embedded microstrips," *Microw. Opt. Technol. Lett.*, vol. 42, no. 1, pp. *50*–54, Jul. 2004.

[8] Z. Deng and A. M. Niknejad, "The 'Load-Thru'(LT) de-embedding; (LT) de-embedding technique for the measurements of mm-wave balanced 4-port devices," *in 2010 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 207–210, 2010.

[9] Advanced Design System (ADS), ADS 2014.01, Keysight EEsof EDA, Keysight Technologies.

[10] ANSYS® HFSS, Release 14.0, ANSYS, Inc.

[11] G. F. Engen and C. A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 12, pp. 987–993, Dec.1979.

[12] B. Zhang, Y.-Z. Xiong, L. Wang, S. Hu, and J. L.-W. Li, "On the De-Embedding Issue of Millimeter-Wave and Sub-Millimeter-Wave Measurement and Circuit Design," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 2, no. 8, pp. 1361–1369, Aug. 2012.

[13] A. Hamidipour, M. Jahn, F. Starzer, X. Wang, and A. Stelzer, "On-wafer passives de-embedding based on open-pad and Transmission Line measurement," in *2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 102–105, 2010.

[14] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," *in Proceedings of the Bipolar Circuits and Technology Meeting,* pp. 188–191, 1991.

[15] E. P. Vandamme, D. M. M. Schreurs, and C. van Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 737–742, Apr. 2001.

[16] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," IEEE Trans. Electron Devices, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[17] T. E. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," *in Proceedings of the 1999 International Conference on Microelectronic Test Structure. ICMTS 1999,* pp. 105–110, 1999.

[18] Y. Lin, H.-T. Yen, H.-H. Chen, C.-P. Jou, C.-W. Kuo, M.-C. Jeng, F.-L. Hsuch, C.-H. Hsiao, and G.-W. Huang, "An extended de-embedding method for on-wafer components," in *2012 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, pp. 166–168, 2012

[19] Y. N. Yosuke Goto, "New On-Chip De-Embedding for Accurate Evaluation of Symmetric Devices," *Jpn. J. Appl. Phys.,* vol. 47, pp. 2812–2816, 2008.

[20] N. Li, K. Matsushita, N. Takayama, S. Ito, K. Okada, and A. Matsuzawa, "Evaluation of a Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design," *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.,* vol. E93-A, no. 2, pp. 431–439, Feb. 2010.

[21] A.-L. Franc, E. Pistono, N. Corrao, D. Gloria, and P. Ferrari, "Compact high-Q, low-loss millimeter wave transmission lines and power splitters in RF CMOS technology," *in Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International,* pp. 1–4, 2011.

[22] A.-L. Franc, E. Pistono, D. Gloria, and P. Ferrari, "High-Performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Band pass Filters," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1219–1226, May. 2012.

[23] N. Erickson, J. Fan, X. Gao, B. Achkir, and S. Pan, "De-embedding techniques for transmission lines: An application to measurements of on-chip coplanar traces," in *2014 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, pp. 660–666, 2014.

[24] R. Torres-Torres, G. Hernandez-Sosa, G. Romo, and A. Sanchez, "Characterization of Electrical Transitions Using Transmission Line Measurements," *IEEE Trans. Adv. Packag.*, vol. 32, no. 1, pp. 45–52, Feb. 2009.

[25] W. Shu, S. Shichijo, and R. M. Henderson, "Investigation of the de-embedding issue of CPWs on silicon substrates at high frequency," in *2013 Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS)*, pp. 1–4, 2013.

[26] T. Hirano, K. Okada, J. Hirokawa, and M. Ando, "Accuracy investigation of the de-embedding technique using open and short patterns for on-wafer RF characterization," in *Microwave Conference Proceedings (APMC), Asia-Pacific*, 2010, pp. 1436–1439, *2010*.

4. Measurements and Electromagnetic Modeling Analysis of De-embedding Methods

This chapter analyses and explains the measurement results with the electromagnetic model. We are using **S-CPW** transmission line as DUT (Device Under Test) to analyse the methods. The fabrication of the DUT and the de-embedding structures are done in AMS 0.35 µm CMOS technology and BiCMOS 55 nm technology. We compare and benchmark the de-embed results using Half-Thru de-embedding and TRL with the S-CPW transmission line which is simulated using 3D electromagnetic simulation tool Ansys HFSS. In general, uncertainties make the de-embedding results different from the device alone. These uncertainties in the de-embedding results and the excessive loss happening beyond millimeter wave frequencies are explained based on a new realistic EM simulation model by taking of all possible parasitics from the on-wafer measurement into account. Finally, comparison and benchmarking of the different de-embedding methods with Half-Thru de-embedding and the Thru-Load de-embedding method are performed.

4.1 AMS 0.35 µm CMOS Technology

The technology used to fabricate the devices and the de-embedding structures is 0.35 µm CMOS from Austriamicrosystems (AMS) [1]. This technology is relatively low cost (890 Euro/mm^2). The Back End of Lines (BEOL) of AMS 0.35 µm CMOS Technology is shown in Figure 4.1.

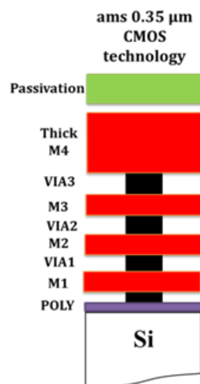


Figure 4.1. Back End of Lines (BEOL) of AMS 0.35 µm CMOS Technology

As shown in Figure 4.1, this technology uses four metal layers of aluminium metallization with a thick metal, in the layer M4, about ~2.8 µm thick. The other three metal layers have a thickness of ~0.64 µm

and each layer of Silicon di-Oxide (SiO_2) dielectric is present in between two metal layers, has a thickness of ~1 µm. The top metal layer is covered with a passivation layer of ~2 µm of silicon nitride Si_3N_4 to protect devices from corrosion.

4.2 Fabrication Map

To benchmark the de-embedding methods, we fabricated S-CPW transmission line as DUT and associated de-embedding structures in AMS 0.35 µm CMOS technology. We de-embed the S-CPW transmission line with different parameters and different ways, to compare and benchmark the Half-Thru de-embedding [2], [3] and Thru-Load de-embedding (see Figure 4.2).

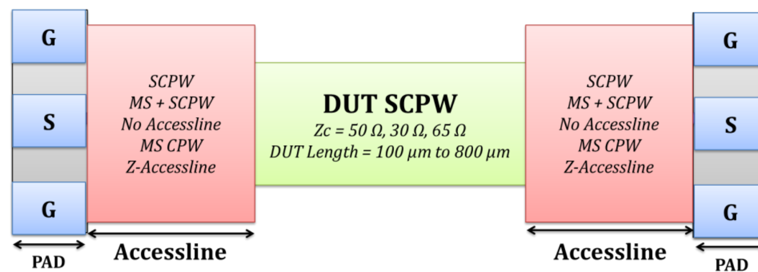


Figure 4.2. Different de-embedding models: S-CPW Transmission Line as DUT

Concerning the S-CPW transmission line, we considered several parameter considerations,

1. Lengths of S-CPW transmission line DUT is varying from 200 µm to 800 µm.
2. Characteristic impedance is varying from 30 Ω to 65 Ω.

For extensive validation of Half-Thru de-embedding method and Thru-Load de-embedding method, we fabricated **different values of *Load* (100 Ω and 200 Ω)** de-embedding structures. In the Chapter 3, section 3.4.3, we discussed about "accessline" which is one of the important parameters in de-embedding model. To study this case, the Half-Thru de-embedding method and Thru-Load de-embedding method have to be performed by **different accesslines** used to connect pad and DUT. **Bended-accessline** configuration is fabricated to test Half-Thru de-embedding and Thru-Load de-embedding, which can de-embed any kind of parasitics.

4.3 Comparison of Half-Thru De-embedding and TRL

In the previous chapter, we evaluated Half-Thru de-embedding [2], [3] and Thru-Load de-embedding and concluded that these methods are comparable with the TRL [4] in simulation. Here we are analysing these methods with measured data.

4.3.1 DUTs and De-embedding Structures

As shown in Figure 4.3, S-CPW transmission line with three different characteristic impedance (*Zc*) of 50 Ω, 65 Ω and 30 Ω are used to evaluate the Half-Thru de-embedding and TRL [4]. All the DUT and de-embedding structures are measured until 110 GHz at IMEP-LAHC.

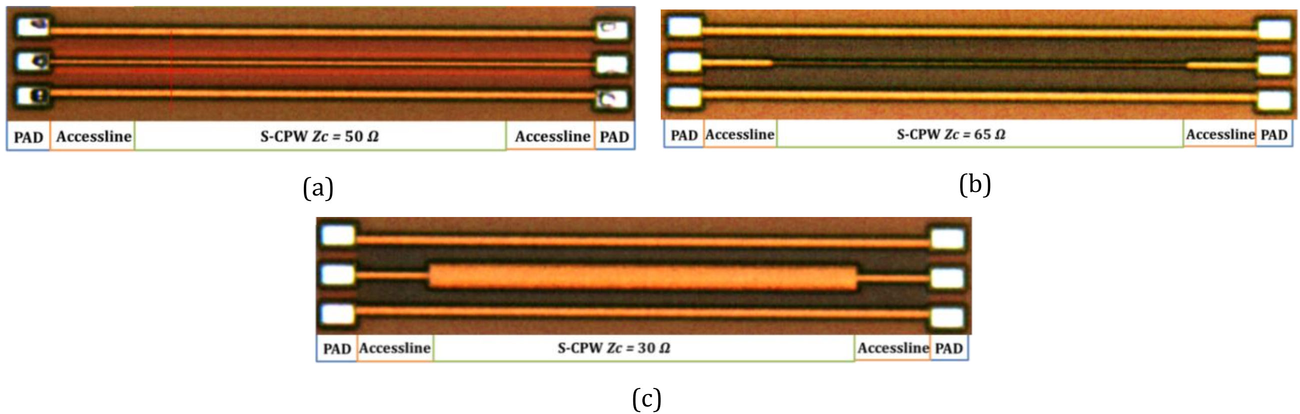


Figure 4.3. S-CPW (a) *Zc* = 50 Ω (b) *Zc* = 65 Ω (c) *Zc* = 30 Ω

Different de-embedding structures are fabricated to de-embed the device (see Figure 4.4). As shown in Figure 4.4, the *Thru, Open, and Line(s)* (TL_1, and TL_2: different lengths) are used for TRL method. Half-Thru de-embedding method utilizes TL_1, TL_2 (L_2= 2.TL_1), and the *Half-Thru Load.*

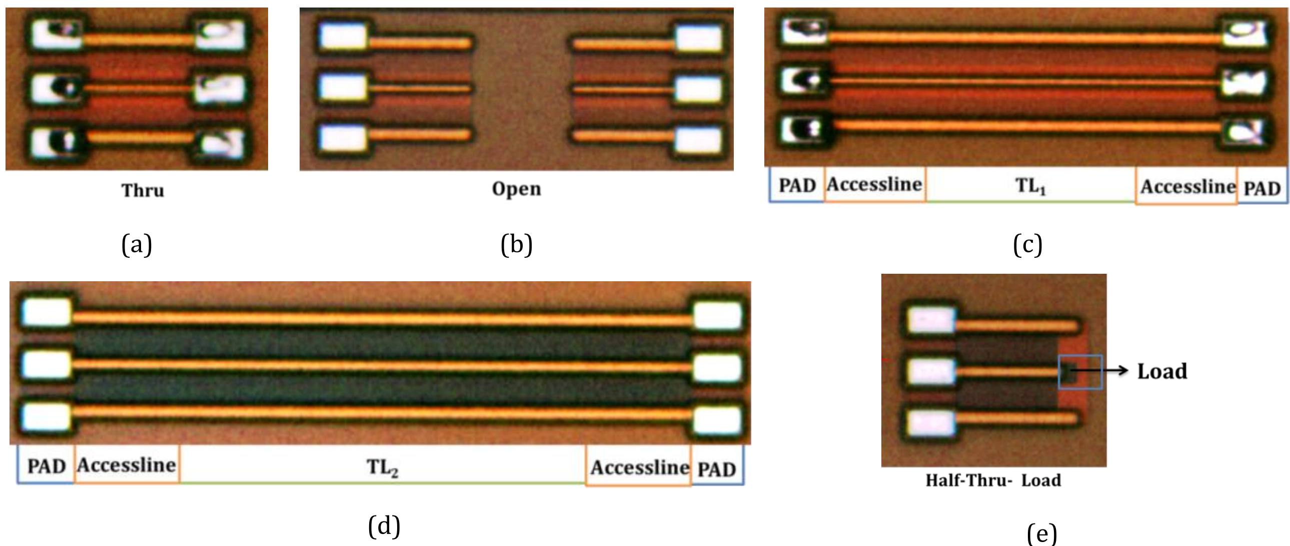


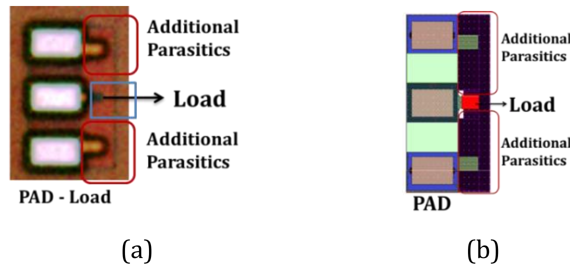
Figure 4.4. De-embedding structures (a) *Thru* (b) *Open* (c) TL_1 (d) TL_2 (L_2= 2.TL_1) (e) *Half-Thru Load*

4.3.2 Load value Extraction

To test the Half-Thru de-embedding and Thru-Load de-embedding method, we need to know the value of the *Load* (Z_{Load}) loaded in the *Half-Thu Load*. This value of the *Load* can be de-embedded using different methods. We compare three methods (see Chapter 3, section 3.5) such as,

1. Open de-embedding [5], [6], [8], [9]
2. Open-Short de-embedding [5], [6], [8], [9]
3. Kolding's Method for Load value extraction [7]

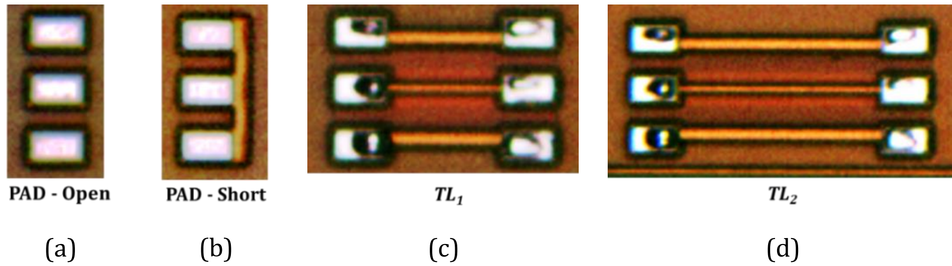
To utilize these methods the *"Load"* should be considered as a DUT and implemented on the wafer. Considering the open de-embedding, open-short de-embedding and load value extraction with Kolding's method, the *Load* is implemented in a pad, which is shown in Figure 4.5(a).



(a) (b)

Figure 4.5. DUT: Load (a) *PAD- Load* (b) PAD- Load Simulated Model

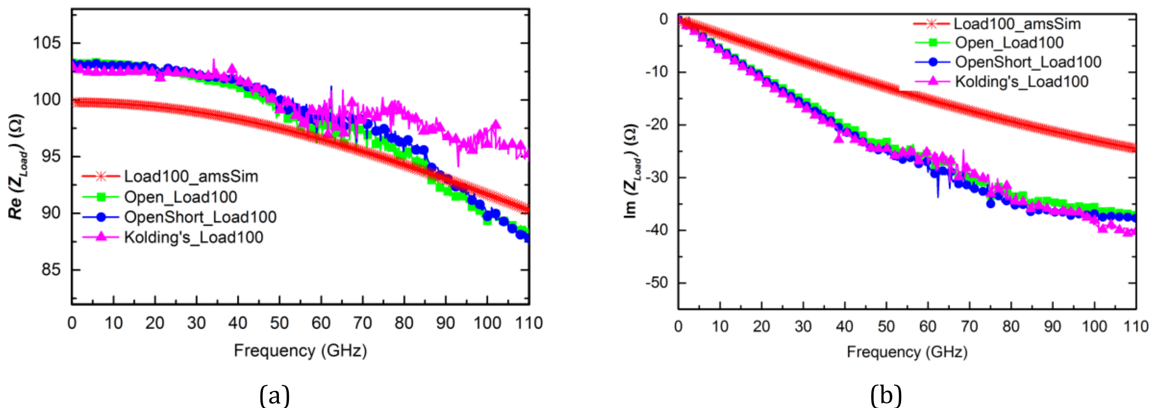
To de-embed the *load* and get the value, we need to use the different de-embedding structures, which are shown in Figure 4.6.



(a) (b) (c) (d)

Figure 4.6. De-embedding structures for Load Extraction (a) *Pad-Open* (b) *Pad-Short* (c) TL_1 (d) TL_2=2.TL_1

The simulation and the measurement are performed until 110 GHz for the study of load value extraction methods. De-embedded results of *Load* value (the real part of the *Load* (Z_{Load}) and the imaginary part of the *Load* (Z_{Load})) using different de-embedding methods are shown Figure 4.7(a) and Figure 4.7(b) respectively.



(a) (b)

Figure 4.7. Load value Extraction using different methods (a) Z_{Load} (Real) (b) Z_{Load} (imag)

Load of 100 Ω is used to test the Half-Thru de-embedding method. This *Load* (Load100_amsSim) is simulated without additional parasitics using an EDA Software and Verification Tool – Cadence Design. The *load* is not constant for the entire range of frequencies; it can have its own additional parasitics due to the dimensions of the metal/resistive element used. Here the *load* has an additional inductive parasitics due to its own length, which is shown in the imaginary part of Z_{Load} in Figure 4.7(b). All the de-embedding methods are compared with the real and imaginary part of the DUT Z_{Load}.

As shown in Figure 4.7, the open de-embedding and open-short de-embedding (green and blue lines) show good agreement with real part (< 3% error with respective to the Load100_amsSim) of the de-embed results. The pad capacitance can be de-embedded using an Open de-embedding structure. As shown in Figure 4.7(b), the inductive parasitics of pad are negligible, since open de-embedding and open-short de-embedding has the same imaginary part. There is an additional parasitics compared to the load alone (Load100_amsSim) in the imaginary part. This is due to the additional connecting lines/ metal layers which cause additional capacitive parasitics, in the de-embedding model to connect the GSG pad to the *load*, which is shown in Figure 4.5(b).

Load value extraction with Kolding's method shows comparable results as open de-embedding and open-short de-embedding until 70 GHz. Beyond, 70 GHz these methods have about 5 % of variation from the simulated result. The accuracy of the method depends on the symmetry of the pad. Since we use the rectangular pad for the measurement, this method is effective. In conclusion, comparing all the methods, open de-embedding and open-short de-embedding shows similar results in both real and imaginary part of Z_{Load}.

4.3.3 Comparison of Half-Thru De-embedding and TRL

We compare the de-embed results of Half-Thru de-embedding method [2], [3] and TRL [4] from the measured data and the simulated S-CPW transmission line to evaluate the de-embedding method. S-CPW of characteristic impedance 50 Ω with a length of 200 μm is chosen to evaluate the methods. To analyse the results, the characteristic impedance and the attenuation coefficient of de-embedded S-CPW are calculated and shown in Figure 4.8(a) and Figure 4.8(b) respectively. The DUT SCPW *Zc* 50Ω (red curve) represents the attenuation coefficient and characteristic impedance of the S-CPW transmission line, which was simulated using Ansys HFSS [11].

As shown in Figure 4.8(a), the characteristic Impedance of DUT S-CPW *Zc* 50 Ω using TRL and Half-Thru de-embedding are close to the DUT S-CPW. TRL uses the characteristic impedance of the line to the set reference impedance, here the DUT and the lines has same impedance of 50 Ω, hence the de-embed results using TRL show closest result to the DUT S-CPW *Zc* 50 Ω. Half-Thru de-embedding is performed using the value of the *Load* from the open-short de-embedding method shown in Figure 4.7,

since it gives performant results even in simulations. The characteristic impedance de-embedded using Half-Thru de-embedding is ~48 Ω. This variation is negligible; this can be due to the actual process variation of the transmission line.

As shown in Figure 4.8(b), the attenuation coefficient of DUT S-CPW *Zc* 50 Ω and the de-embed results using both methods show an excessive loss or discontinuity beyond ~60 GHz. While comparing both methods the results follow same trend with good agreement. These discontinuities do not appear on the simulated S-CPW transmission line (DUT S-CPW *Zc* 50 Ω).

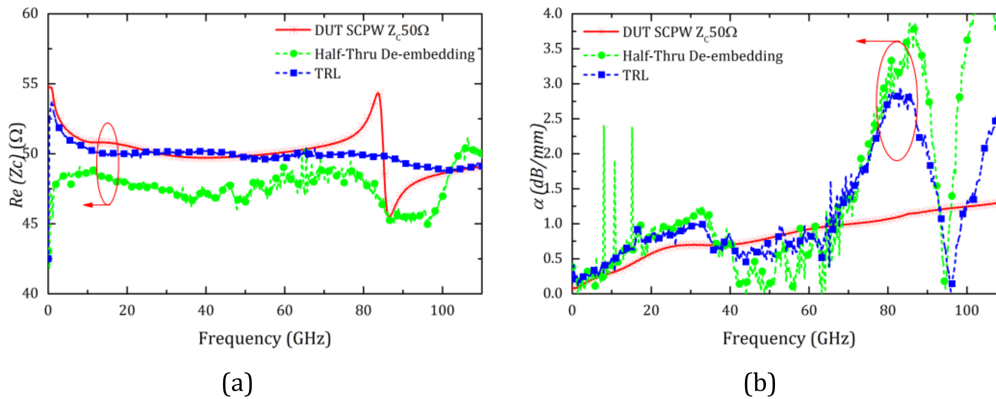


Figure 4.8. TRL and Half-Thru De-embedding (a) Characteristic Impedance (b) Attenuation Coefficient

4.3.4 Analysis of Excessive loss in S-CPW of 65 Ω and 30 Ω

We perform the de-embedding with the characteristic impedance which is different from *Zc* =50 Ω, *Zc*= 65 Ω (DUT S-CPW *Zc* =65 Ω) and *Zc*= 30 Ω (DUT S-CPW *Zc*= 30 Ω)) to confirm that the discontinuity problems in attenuation coefficient does not depend on the impedance of the line (different type of DUT). From the results, the attenuation coefficient of the S-CPW transmission lines (DUT S-CPW *Zc* 65 Ω and DUT S-CPW *Zc* 30 Ω) (see Figure 4.9(a) and Figure 4.9(b)) follow similar trend as S-CPW of *Zc* 50 Ω (see Figure 4.8(b)). The attenuation coefficient of S-CPW *Zc*= 30 Ω is slightly higher from the low frequency itself. However, de-embed results using both methods show an excessive loss or discontinuity beyond ~60 GHz irrespective to the different S-CPW transmission lines.

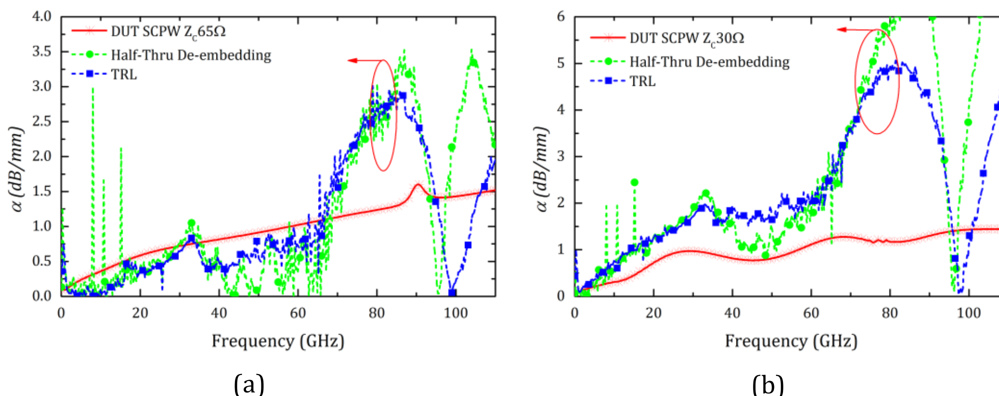


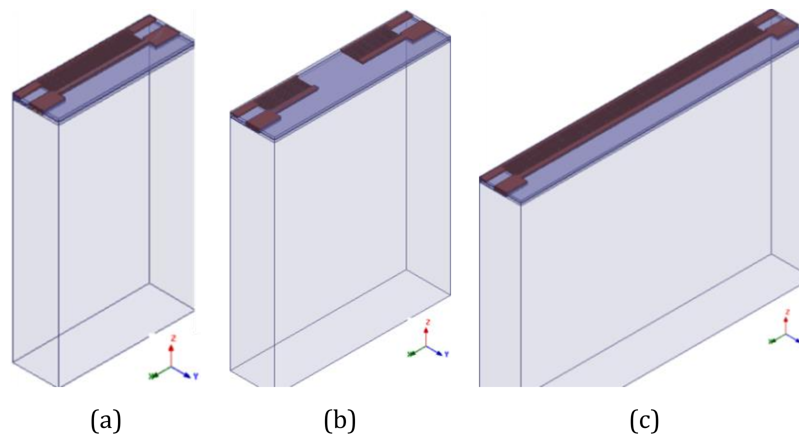
Figure 4.9. TRL and Half-Thru De-embedding: Attenuation Coefficient (a) Zc 65 Ω (b) *Zc* 30 Ω

To evaluate these factors and explain this phenomenon, we performed the simulations with all the de-embedding structures modeled in an EM model simulator, Ansys HFSS [11].

4.3.5 Impact of EM-Model in De-embedding

Since the simulated S-CPW transmission line cannot provide any explanations about the excessive loss happening at measurement, an electromagnetic model of the fabricated de-embedding structures are simulated using Ansys HFSS to perform de-embedding. This will help us to understand if the pad parasitics or any other EM modeling factors are affecting the excessive loss or not. In the preliminary step, the goal is to test the TRL, since the Half-Thru de-embedding and TRL are comparable. The de-embedding structures *Thru, Open, Line*(*s*) for TRL are modeled in Ansys HFSS and are shown in Figure 4.10(a), Figure 4.10(b), and Figure 4.10(c) respectively. All the simulations are performed by using Half-Symmetry of the EM models and performed de-embedding using these de-embedding structures. The results are shown as "TRL_DUT-HFSS S-CPW Zc ".

The de-embedded attenuation coefficient from the measure and the EM model for different S-CPW transmission lines are shown in Figure 4.11. The attenuation coefficient of S-CPW Zc 50 Ω, S-CPW Zc 65 Ω and S-CPW Zc 30 Ω are shown in Figure 4.11(a), Figure 4.11(b) and Figure 4.11(c) respectively.



(a) (b) (c)

Figure 4.10. De-embedding structures (Half-Symmetry) (a) *Thru* (*non-Zero*) (b) *Open* (c) *Line*

Even the EM model de-embedding results (TRL DUT- HFSS S-CPW *Zc*) are not matched with the measured de-embedded results (TRL DUT- Measure S-CPW *Zc*). **This shows that de-embedding has the effect of additional on-wafer measurement issues.** The literature shows that this excessive loss can be due to the adjacent cells nearby or coupling due to probe to probe or probe to the substrate or the higher order modes [12]-[20]. To evaluate these factors we need to identify a better EM model, which can explain all these phenomena.

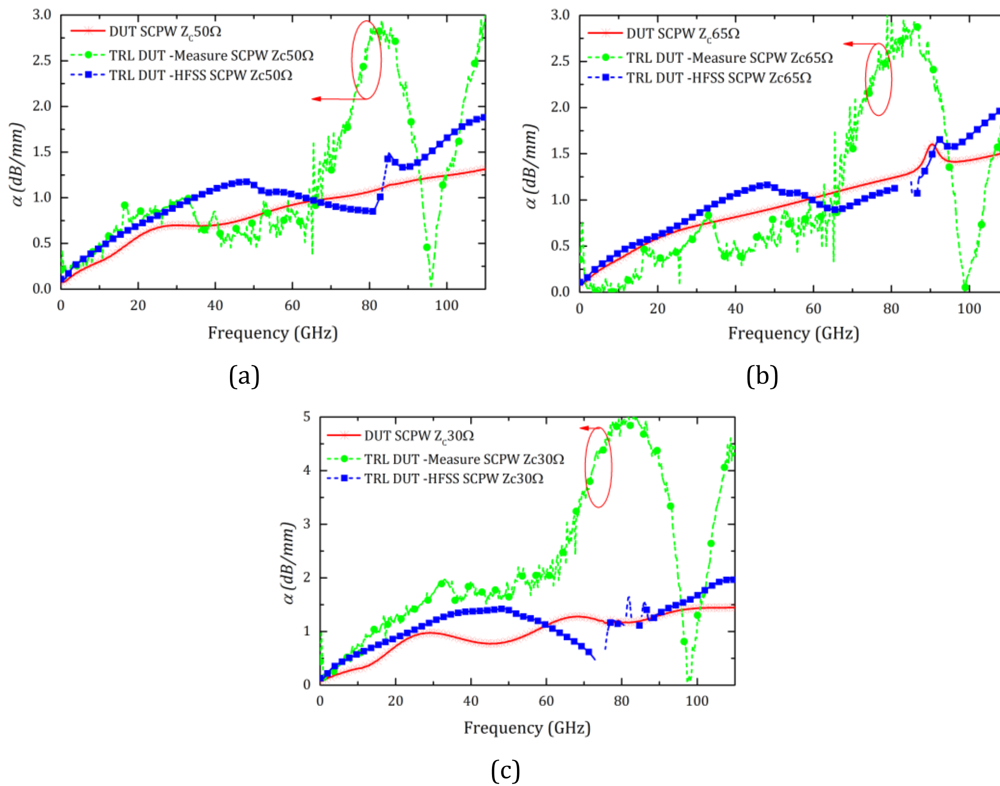


Figure 4.11. TRL: Measure vs HFSS Model: Attenuation coefficient (a) Zc=50 Ω (b) Zc=65 Ω (b) Zc=30 Ω

4.3.6 De-embedding: CPW Transmission Line as DUT

Previously, we tested the S-CPW transmission line as DUT. Considering S-CPW is a new topology, it can be difficult to explain that, the excessive loss or discontinuity happening are from measurement, or it can be a special phenomenon of S-CPW. To prove this ambiguity, we use CPW transmission line as DUT. CPW of characteristic impedance (Zc) 50 Ω (shown in Figure 4.12(a)) is fabricated and chosen to evaluate the phenomena of discontinuity in attenuation coefficient.

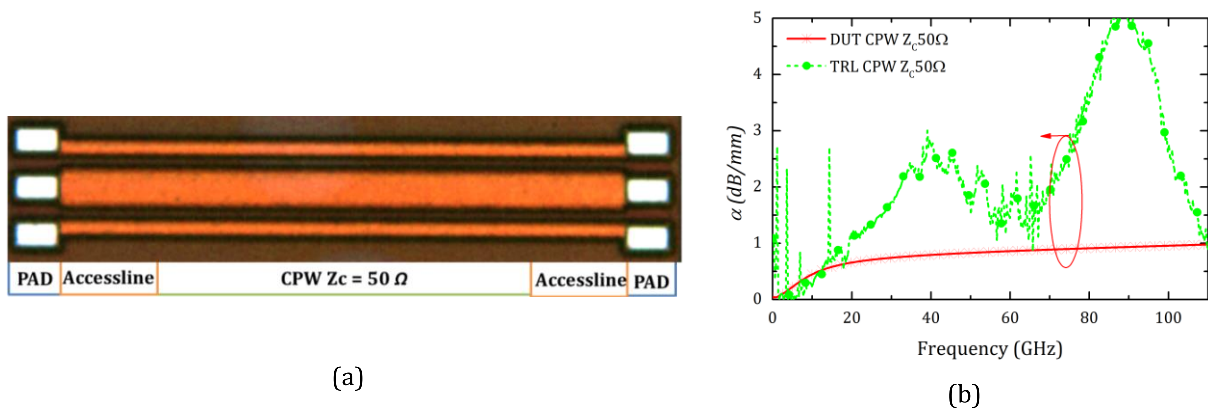


Figure 4.12. (a) DUT CPW Zc=50 Ω, with the length of 400 μm (b) Attenuation co-efficient

The attenuation coefficient (α) calculated using TRL is shown in Figure 4.12(b). The DUT CPW Zc 50 Ω (red curve) represents the homogeneous CPW transmission line, which is simulated using Ansys HFSS. The de-embed results using TRL method (TRL CPW Zc50Ω) and the homogenous CPW line have high

ambiguity in the case of attenuation coefficient. **The excessive loss or discontinuity (> 20 GHz) in CPW confirms that, this phenomenon can occur from the other on-wafer measurement issues** [12]-[19]. This need to be analysed properly and find out the parameters that are affecting the measurement.

4.3.7 Conclusion of Comparison of Half-Thru De-embedding and TRL

Half-Thru de-embedding and TRL [4] method are chosen to de-embed the DUT (S-CPW transmission line and CPW). The characteristic impedance of the de-embed results are comparable to the simulated S-CPW transmission line, but the attenuation coefficient shows, an excessive loss or discontinuity over ~60 GHz, (see Figure 4.8(b), Figure 4.9(a) and Figure 4.9(b)). From the results of the transmission lines, it is clear that the discontinuity in attenuation coefficient is not due to the different DUTs. The only conclusion we can make from these results is that **Half-Thru de-embedding method and TRL are comparable.**

Since the simulated S-CPW transmission line cannot provide any additional information about the excessive loss in the measured results, in the preliminary step TRL de-embedding is performed with all the de-embedding structures that modeled in EM simulator, Ansys HFSS. Even the de-embedding with EM model does not give excessive loss in the attenuation (see Figure 4.11). To prove these are not the special phenomena of S-CPW, we de-embed a CPW transmission line of Zc 50 Ω (see Figure 4.12(b)). Even the CPW transmission line results show the similar trend as S-CPW. Hence, **the excessive loss or discontinuity in the attenuation co-efficient can be due to the other on-wafer measurement problems.**

To study these phenomena we need an extensive EM modeling and Analysis. Following sections are focused on to explain this phenomenon.

4.4 EM-Model Issues and Analysis

The literature shows the measurement can be affected by many on-wafer measurement problems. The major problems that can create the problems are:

1. **Adjacent devices close to the measurement device (**[12]-[15]**)**
2. **Coupling between probe to probe or probe to substrate (**[12]-[19])
3. **Higher order modes (**[16]-[20]**)**

Here we are trying to analyse the phenomena and develop an "EM model" including all the possible factors, which can explain the excessive loss or discontinuity happening in the measurement. The analysis is done with a strategic way of adding the on-wafer parasitics such as adjacent cells (step by

step) and probe parasitics. In the preliminary step is to develop a realistic EM model that matches the results of a measured transmission line with pad-accessline parasitics. So all the EM simulations are performed for the measured transmission line with pad-accessline parasitics. Once we identify the right EM model, we perform the de-embedding and analyse the results.

4.4.1 On-wafer: Fabricated Transmission Lines

In the primary step we need to compare the results of measured transmission line with pad-accessline parasitics and EM model of the measured transmission line pad-accessline parasitics simulated in Ansys HFSS [11]. The EM model is simulated with different configuration of adjacent structures with the specified distance. In the reality, the transmission lines are fabricated on-wafer separated with a distance of 50 µm, from both sides (see Figure 4.13).

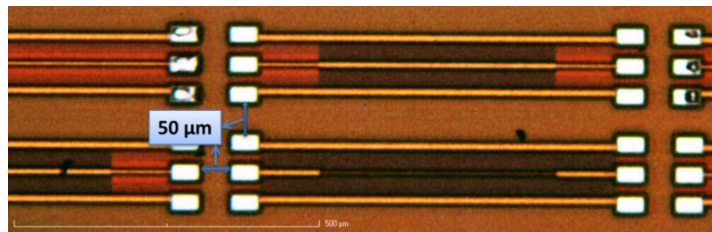


Figure 4.13. Fabricated wafer: Transmission Lines/other structures separated with a distance of 50 µm

4.4.2 EM – Model of Measured CPW transmission line

To analyse the EM model vs measurement, we have chosen a CPW transmission line, length of 400 µm. The EM model of the CPW transmission line with pad /accessline parasitics (half-symmetry) is shown in Figure 4.14. The line is simulated without any adjacent devices. All the simulations are performed for half-symmetry of the EM models.

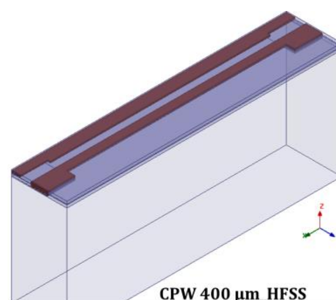


Figure 4.14. HFSS Model of CPW 400 µm Line with pad/accessline Parasitics (Half-Symmetry)

The magnitude of S_{11} and S_{21} of the EM model results compared with the measured results are shown in Figure 4.15. Considering the S_{11}, the measurement (CPW 400 µm_Measure) and EM model (CPW 400 µm_HFSS) has good agreement until ~80 GHz, but considering the S_{21} the measurement and the EM Model has discrepancy above 30 GHz. Since the S-parameter results are not matched with the measurement results or not following the similar trend, this EM model is not valid to explain the

excessive losses happening in the measurement. **Therefore, we have to analyse the EM model with other parasitics such as adjacent cells/devices to try to explain the phenomena of excessive loss or discontinuity.**

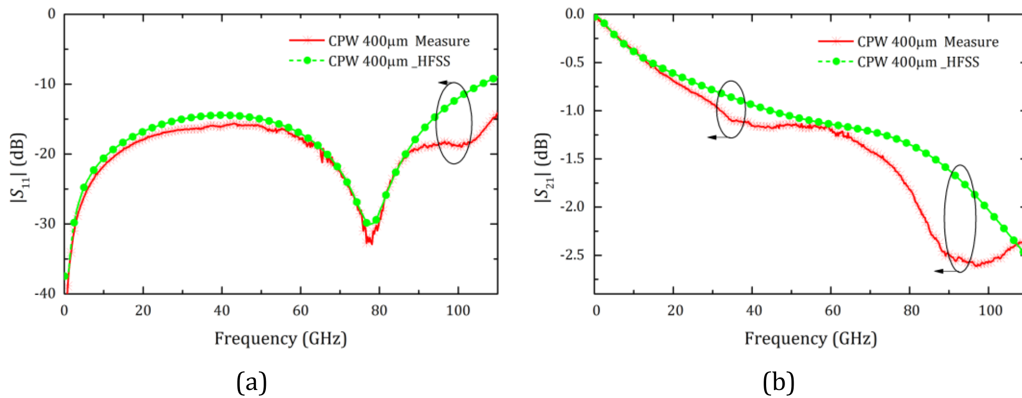


Figure 4.15. Measurement vs HFSS Model: CPW 400 μm Line with Parasitics (a) $|S_{11}|$ (b) $|S_{21}|$

4.4.3 EM – Model of Measured CPW transmission line with adjacent cells

Here, we study the second possibility to have a better agreeable result with the actual measurement. Here we model the CPW transmission line with pad /accessline parasitics (measured CPW transmission line: DUT) with different configurations of adjacent cells, which are shown in Figure 4.16.

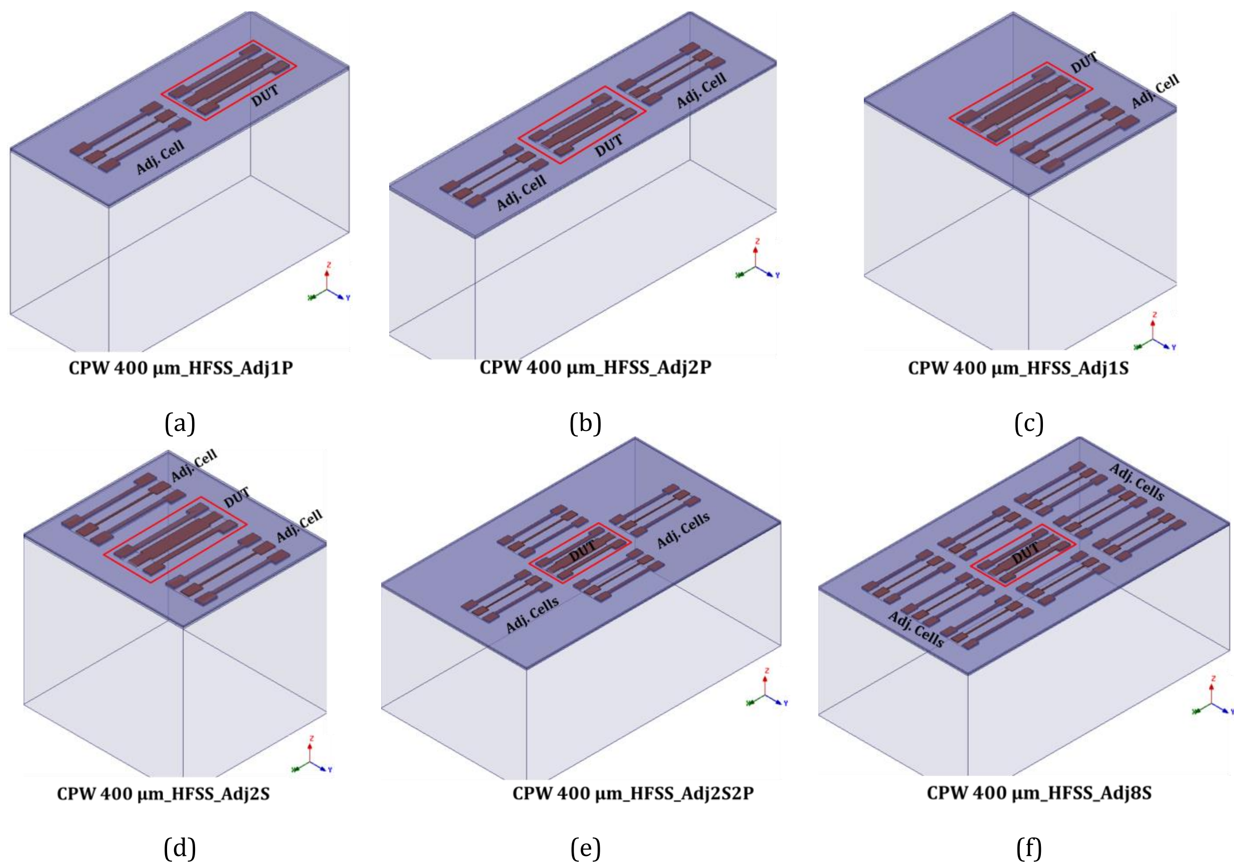


Figure 4.16. DUT with adjacent cells: (a) One adj. cell on the same direction of DUT (b) Two adj. cells on the same direction of DUT (c) One adj. cell on the side (d) Two adj. cells on the sides (e) Four adj. cells (f) Eight adj. cells

This gives a step-by-step analysis of the effect of adjacent cells. The EM model of measured CPW transmission line (DUT) with a single adjacent cell to EM model of measured CPW transmission line (DUT) with eight adjacent cells are shown from Figure 4.16(a) to Figure 4.16(f) respectively. The adjacent cells are separate with the distance of 50 μm. In this case, the EM model of DUT excited with internal or lumped port of 50 Ω.

The S_{11} and the S_{21} of EM model of the DUT with adjacent cells are shown in Figure 4.17 and Figure 4.18. As shown in Figure 4.17 and Figure 4.18, both the S_{11} and S_{21} of the EM model of the DUT with adjacent cells have an impact compared to the EM model without adjacent cells. When comparing Figure 4.17 and Figure 4.18, it is noticed that a better agreement between measurement and simulation is obtained when two adjacent cells are added on the sides of the DUT (CPW 400μm_HFSS_Adj2S) as well as four adjacent cells model (CPW 400 μm_HFSS_Adj2S2P) that are shown in Figure 4.18. Nevertheless, the measured peak resonance of S_{11} at about 80 GHz and the additional resonance appearing nearly at 90 GHz in S-parameters are not well predicted in any of these EM model simulations. **Since the results of the EM Model with adjacent cells are not able to match with the results of measured device, the next step is to include the other parasitics from the on-wafer measurement, which is the probe parasitics.**

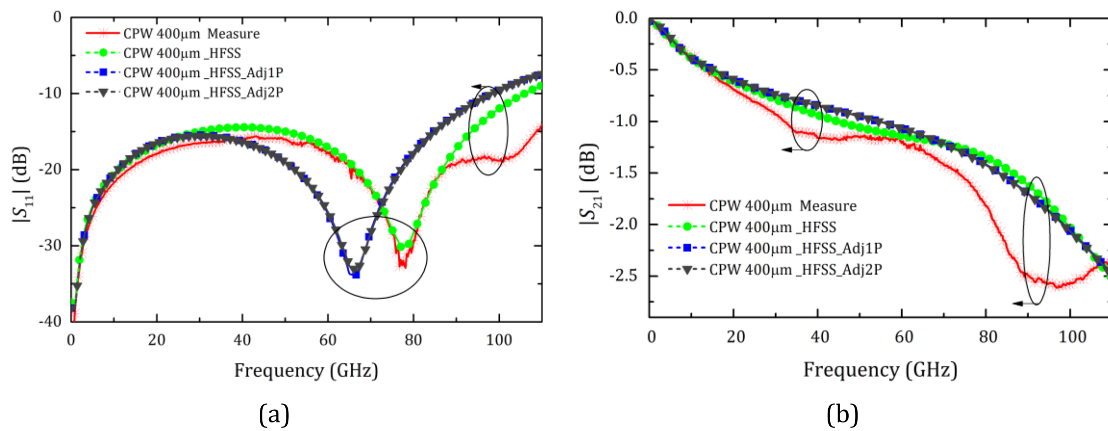


Figure 4.17. Measurement vs HFSS Model: CPW 400 μm Line with Parasitics (a) $|S_{11}|$ (b) $|S_{21}|$

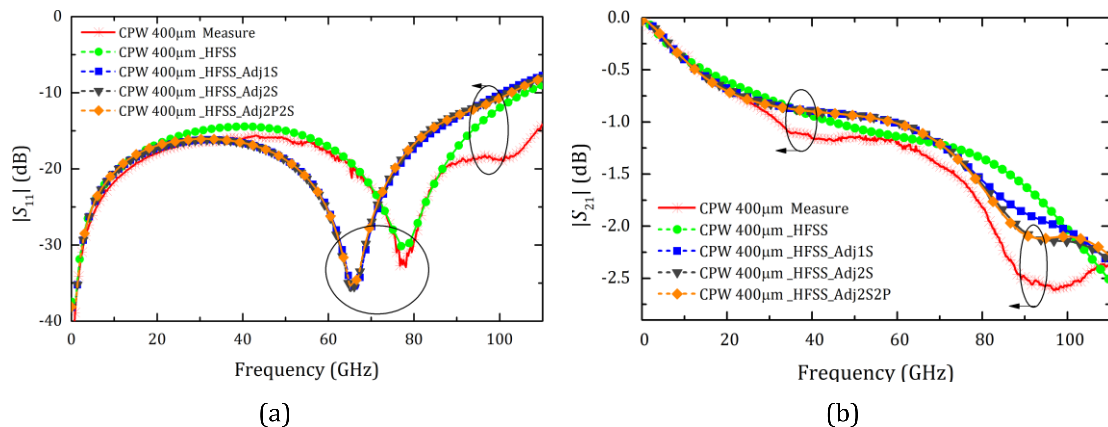


Figure 4.18. Measurement vs HFSS Model: CPW 400 μm Line with Parasitics (a) $|S_{11}|$ (b) $|S_{21}|$

Note: The results of EM model of the DUT with eight adjacent cells "CPW 400 µm_HFSS_Adj8S" surrounded to device shows the same results as "CPW 400 µm_HFSS_Adj2S", so these results are eliminated from the plots.

4.4.4 EM - Model of Millimeter Wave Probe

Apart from the adjacent cells influence, the next parasitics problems can arise from the measurement probe. The probe in the measurement system can creates extra coupling or loss. In the measurement, there can be two ways of probe coupling:

1. Probe to probe : If the device is small, there can be a possibility to have coupling between probe to probe
2. Probe to substrate: In this case, the probe can be coupled to the substrate and that can creates some special modes and extra losses.

For example, these phenomena are illustrated in Figure 4.19. $C_{Probe\text{-}Probe}$ is the possible probe to probe coupling and $C_{Probe\text{-}Substrate}$ is possible probe to substrate coupling.

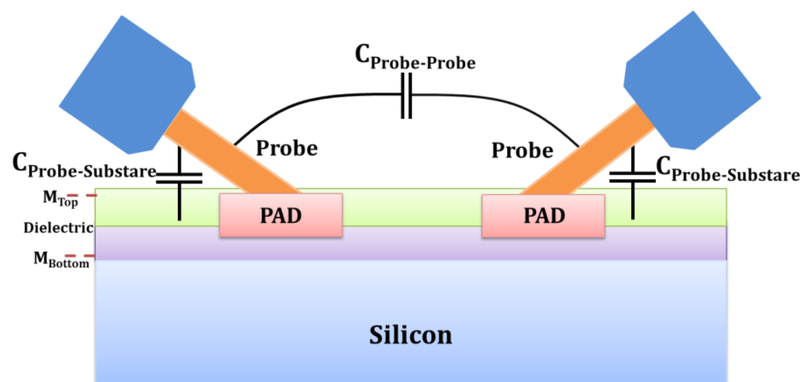
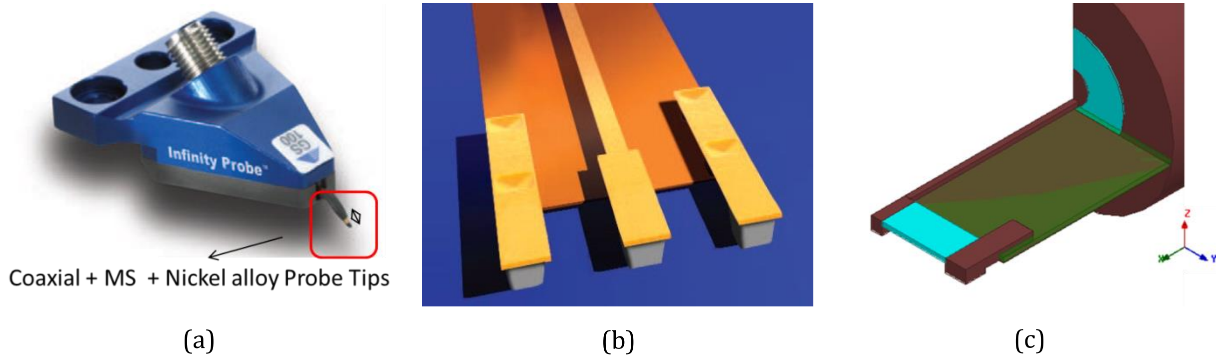


Figure 4.19.Possible effects of Probe in on-wafer measurement

Normally, the measurement depends also on the probe type. Here we use Infinity probe from Cascade Microtech, which is specifically for working in millimeter wave band [21]**. Most of the literature uses CPW probe to study the on-wafer effects** [12]-[17]. **CPW probes provide high impact on probe-to-probe and probe to substrate coupling compared to infinity probe.**

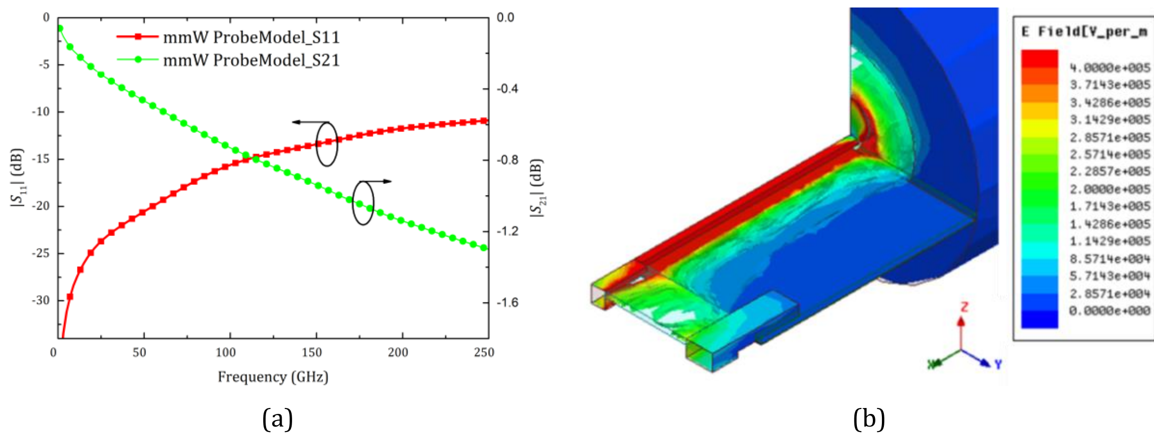
The model of the Infinity probe is shown in Figure 4.20(a). Infinity probe is developed for high frequency characterizations of the RF devices. Infinity probe uses microstrip transmission lines to carry the signal between the co-axial connector to the probe tips, shown in Figure 4.20(b). It uses non-oxidizing nickel alloy for probe tips. The advantages of infinity probe includes less unwanted coupling to nearby devices or other probe tips compared to the CPW probes and it has higher RF measurement accuracy.



(a) (b) (c)

Figure 4.20. Infinity Probe Model (a) Infinity probe (b) MS transmission line for Infinity probe (c) EM Model

An EM model of millimeter wave probe (Half-Symmetry) (Infinity probe) is modeled in Ansys HFSS according to the Cascade Microtech Application Notes [21], which is shown in Figure 4.20(c). The EM model of the infinity probe is modeled with the available data. The substrates used and the other design and technology parameters of the infinity probe is not available (confidential), but for the potential study this model can be used. The co-axial and microstrip sections are designed separately for 50 Ω. The S_{11} and the S_{21} are shown in Figure 4.21(a). As shown in Figure 4.21(a), the S_{11} shows good adaptation (-10 dB) until 250 GHz. The E-field plot is shown in Figure 4.21(b). Since the probe is de-embedding until the probe tip (in HFSS) the propagation losses are eliminated.



(a) (b)

Figure 4.21. Infinity Probe Model (a) $|S_{11}|$ and $|S_{21}|$ (b) E-field

4.4.5 EM - Model of measured CPW transmission line with Millimeter Wave Probe Model and Adjacent Cells

In this case, we study the possibility to have a better agreeable result for EM model of measured CPW transmission line (DUT) with the actual measurement, by adding the EM model of millimeter wave infinity probe and with the adjacent cells. The EM model of the measured CPW transmission line (DUT) with different configurations of adjacent cells separated with the distance of 50 μm and the millimeter wave probe model are shown in Figure 4.22. The EM model of the DUT with no adjacent cells and millimeter wave probe model to EM model of the DUT with four adjacent cells are shown in Figure 4.22. In this case, the EM model of the DUT is excited with wave port at the microstrip

transition of the millimeter wave probe. The co-axial part of the probe is removed, since it is insulated, thus there would not be any impact. This EM millimeter wave probe is de-embedding until the probe tip in Ansys HFSS. This creates a similar environment as the real measurement system.

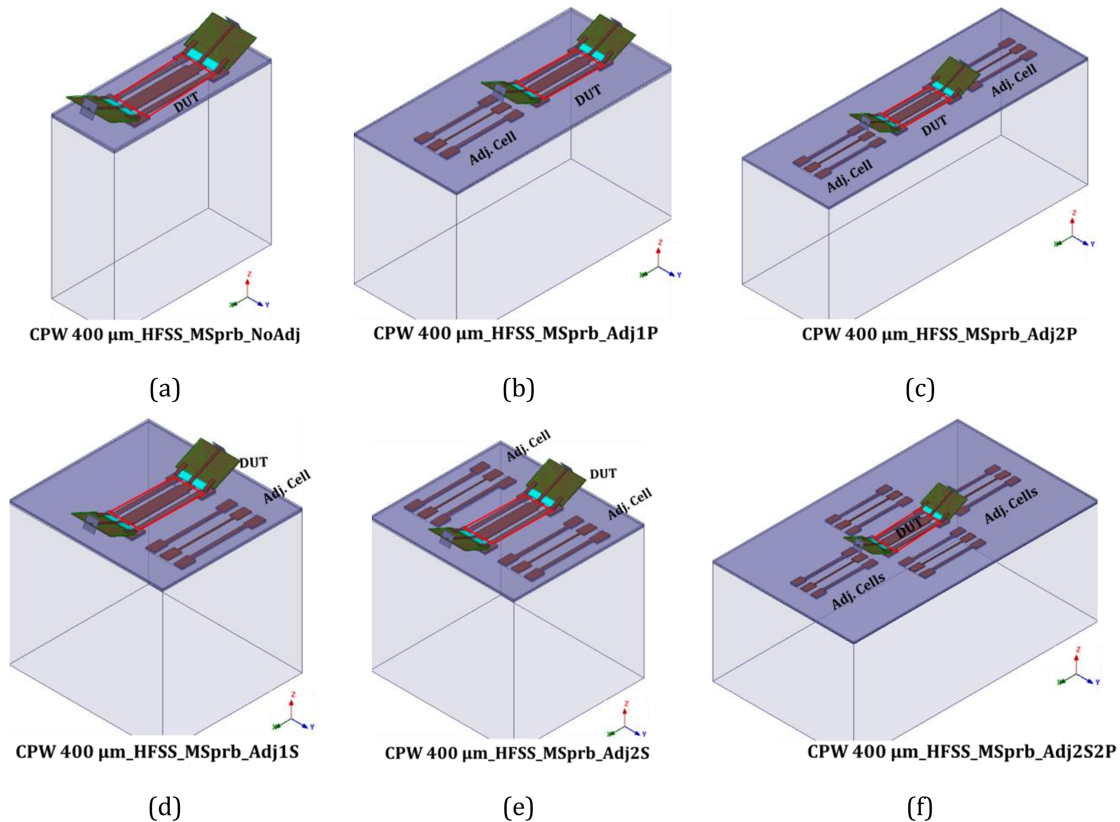


Figure 4.22. DUT with adjacent cells and millimeter wave probe model: (a) No adj. cell (b) One adj. cell in the same direction of the DUT (c) Two adj. cells in the same direction of the DUT (d) One adj. cell on the side of DUT (e) Two adj. cells on the sides of DUT (f) Four adj. cells on the sides of DUT

The S_{11} and the S_{21} of the EM model of the DUT with adjacent cells and millimeter wave probe is shown in Figure 4.23 and Figure 4.24. **While comparing Figure 4.23 and Figure 4.24, it is clear that both the S_{11} and the S_{21} of the EM model of DUT with two and four adjacent cells with millimeter wave probe model (CPW 400 µm_HFSS_MSprb_Adj2S and CPW 400 µm_HFSS_MSprb_Adj2S2P) show an agreeable result and similar trend with respect to measurement that is shown in Figure 4.24.** Even both the resonances (~ 80 GHz and further) in the S_{11} and the S_{21} of the measured transmission line are able to reproduce in these EM models. Considering Figure 4.23, we are not able match the EM model results with the measurement result. **This shows adjacent cells in the same direction does not have a big effect on the device measurement. This proves that the minimal additive parasitics appearing in the measurement is from the adjacent cells from the side of the device, not from the same direction as DUT or port.** As shown in Figure 4.24, we compared the results of **EM model of the DUT with adjacent cells without probe (see model: Figure 4.16(d)-CPW 400 µm_HFSS_w/oPrb_Adj2S). This shows the impact of the millimeter wave probe model is important in the EM model de-embedding.**

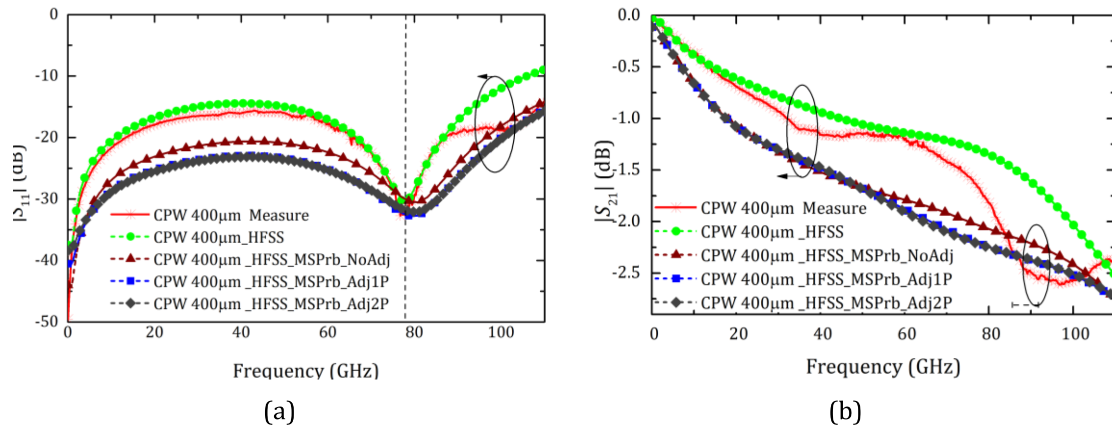


Figure 4.23. Measurement vs HFSS Model with MSprobe Model: CPW400µm Line with Parasitics (a) $|S_{11}|$ (b) $|S_{21}|$

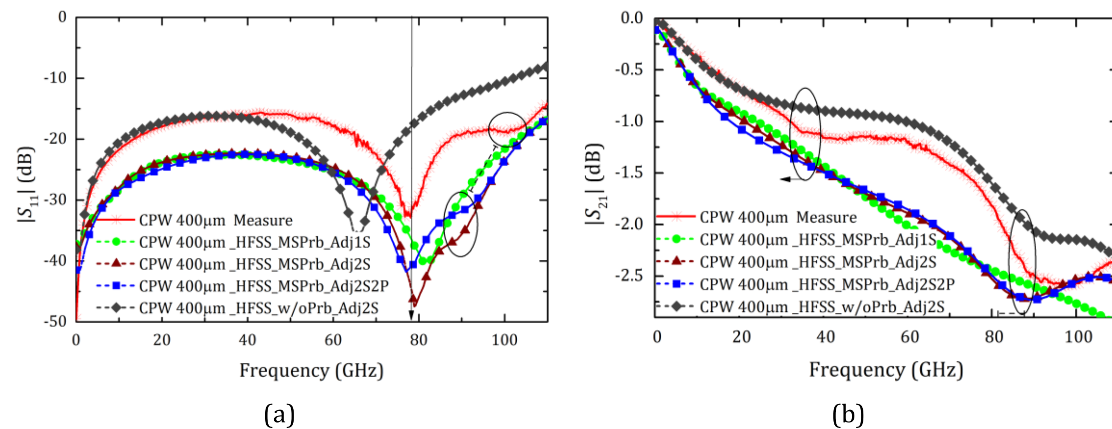


Figure 4.24. Measurement vs HFSS Model with millimeter wave probe: CPW 400 µm Line with Parasitics (a) $|S_{11}|$ (b) $|S_{21}|$

In conclusion, CPW measurement with two adjacent cells (CPW 400 µm_HFSS_MSprb_Adj2S) with millimeter wave probe model, which is placed on the sides of the DUT (Figure 4.22(e)) model can be considered as a (closest) realistic model and used for the evaluation of the de-embedding methods. The further section explains the studies with the realistic EM model.

4.4.6 De-embedding with the realistic EM- Model

To evaluate the realistic EM model, CPW transmission lines with its de-embedding structures are modeled with adjacent cells on the sides with millimeter wave probe model. We consider CPW 200 µm with *Zc* of 50 Ω as DUT. EM model of the DUT with two adjacent cells on the sides of DUT (Figure 4.22(e)) and four adjacent cells (Figure 4.22(f)) with millimeter wave probe model, separated with distance of 50 µm, chosen to analyse the de-embedding. TRL method is used to analyse the results in the preliminary stage.

The de-embed attenuation coefficient using TRL is shown in Figure 4.25(a). De-embed results of EM model of CPW with two adjacent cells on the sides of DUT (Figure 4.22(e)) and four adjacent cells (Figure 4.22(f)) with millimeter wave probe model are shown as “TRL_HFSS_MSPrb_Adj2S” and

"TRL_HFSS_MSPrb_Adj2S2P" respectively. **The results show that, both the models have similar results and trend with the measured de-embed results until 110 GHz. This again proves that the adjacent cells in the same direction of the DUT or port have less impact compared to the side of the DUT measure.** Hence, device with two adjacent cells on the sides of DUT with millimeter wave probe model is chosen for further analysis.

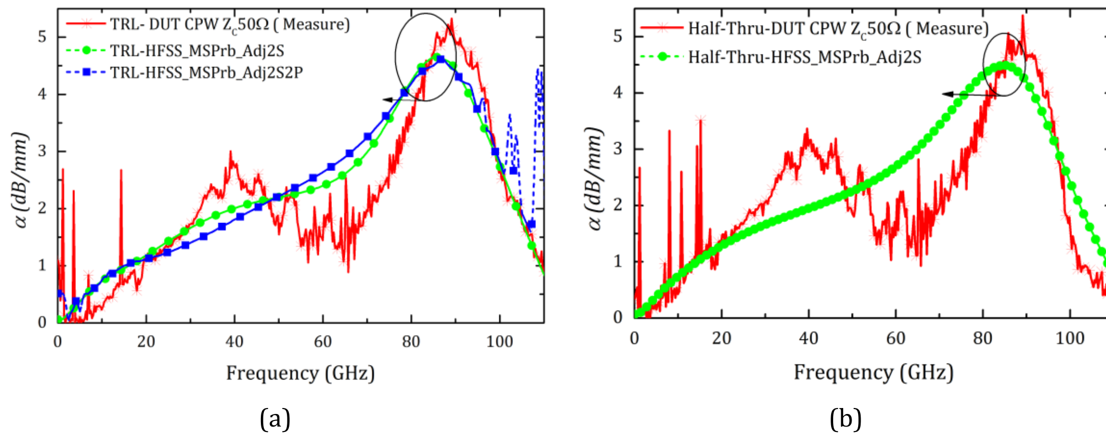


Figure 4.25. Measure vs HFSS Model with millimeter wave probe: DUT CPW Zc=50 Ω Attenuation coefficient (a) TRL (b) Half-Thru de-embedding

The next step is to evaluate the Half-Thru de-embedding method with this model. The de-embed attenuation coefficient using Half-Thru de-embedding is shown in Figure 4.25(b). The de-embed results from the measurement and the two adjacent cells on the sides of DUT with millimeter wave probe model (Half-Thru HFSS_MSPrb_Adj2S), gives the similar results and trend as TRL, Since Half-thru de-embedding is comparable with TRL until 110 GHz in measurements. **In conclusion, The variation in the results of the realistic EM model is because the millimeter wave probe, since it is just an EM model, in actual scenario it can be different, also the radiation characteristics of the actual infinity probe is difficult to model.**

4.4.7 Reasons of Excessive Loss

Considering the excessive loss, the conclusions made from the previous analysis are,

- Impact of the millimeter wave probe
- Adjacent cells on the sides of the DUT affecting the measurement

To understand it briefly, we analyse the de-embed results of CPW transmission line with different adjacent cell parasitics and with millimeter wave probe model. As shown in Figure 4.26, we can see that the attenuation coefficient of the homogeneous line differs from the other de-embed results. The realistic EM model (two adjacent cells on the sides of DUT with millimeter wave probe model: TRL-HFSS_MSPrb_Adj2S) has the comparable results with the de-embed results of measurement.

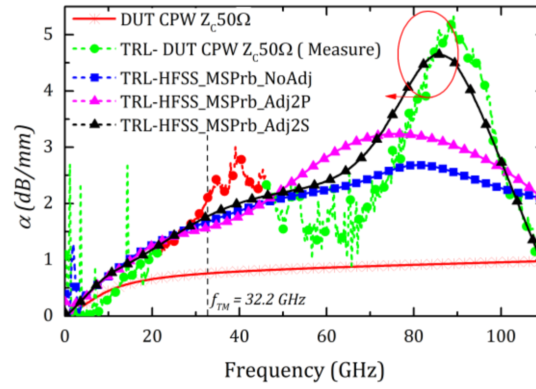


Figure 4.26. Attenuation coefficient of DUT CPW *Zc*=50 Ω: Measure vs HFSS Model with MSprobe

Comparing the attenuation coefficient of the homogeneous CPW transmission line and de-embed results (see Figure 4.26) from the EM model of the measured CPW transmission line with no adjacent cells with millimeter wave probe (TRL HFSS NoAdj), it is clear that the **impact of the millimeter wave probe** is quite important in case of de-embedding. This is due to **additive wave propagation in the edges of the metal planes (grounds of CPW), called parallel plate propagation**. This propagation is introduced by the metal planes/tips of the millimeter wave probe and the pads/substrate. Since the metal planes/tips of millimeter wave probes are open, the EM wave propagates through the edges of the transmission line [16]. This can cause additional losses. **Generally, in all the literature the studies of the excessive loss are explained with CPW probe. In addition, the literatures explain that the adjacent cells near to the ports have more impact. The adjacent cells on the sides of the DUT are not relatively taken until now. The realistic EM model (device with two adjacent cells on the sides of DUT and millimeter wave probe model) shows that the impact of the adjacent cells on the sides of the DUT.**

4.4.8 Other Possible Losses

Apart from effect of adjacent cell phenomena, there is a possibility to have non-TEM mode propagation, which may induce extra losses. The cut-off frequency of Transverse Electric (TE) and Transverse Magnetic (TM) modes [20] for a CPW on a silicon substrate of height h_{si} (540 µm) and the permittivity of the silicon ε_{Si} (11.9) can be expressed as,

$$f_{TE} = \sqrt{\frac{2}{\varepsilon_{si} - 1}}\frac{c}{2\pi . h_{si}}\left(arctan\,(1) + \frac{\pi}{2}\right) \quad =51.3\text{ GHz} \tag{4.1}$$

$$f_{TM} = \sqrt{\frac{2}{\varepsilon_{si} - 1}}\frac{c}{2\pi . h_{si}}(arctan\,(\varepsilon_{si})) \quad =32.26\text{ GHz} \tag{4.2}$$

These TE and TM modes can be mixed with TEM modes and have excessive loss. From the above equations ((4.1) and (4.2)), it is clear that both modes appear within the millimeter wave frequency. It

is clear that the TM mode will start to interact with the TEM mode above 32.2 GHz, and TE mode will start to interact with the TEM mode above 51.3 GHz. So the CPW above these frequencies is less preferred. The cut-off frequency of first TM mode is marked in Figure 4.26. In addition, the TE or TM frequencies are proportional to $1/h_{si}$, so decreasing the substrate thickness will increase the mode frequency (f_{TE} and f_{TM}). Beyond these frequencies, there will be interaction of the non-TEM modes, which can mixed with quasi-TEM mode and can have extra losses.

4.4.9 Conclusion of EM-Model Issues and Analysis

The analysis of the excessive loss happening in the on-wafer measurement is analysed by considering the EM model. Fabricated CPW transmission line is used to analyse the excessive loss or the discontinuity in the attenuation coefficient. This phenomena is analysed step by step using the EM model of the measurement scenario. That follows,

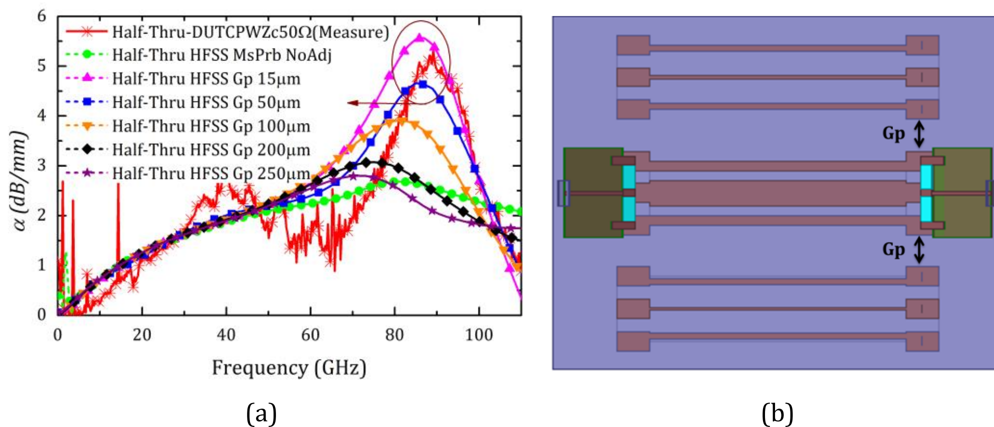
1. The results of measured CPW transmission are compared with the basic EM model of measured CPW, without any extra parasitics.
2. The result of measured CPW transmission is compared with the EM model of measured CPW, with extra parasitics, which are adjacent cells/devices. A step by step evaluation is performed to match the result of EM model with measured device. Concluded that the adjacent cells which are on the sides of the device (Figure 4.16(b)) is affecting the measurement rather than the adjacent cells near the ports (Figure 4.16(b)). With the adjacent cell parasitics, the results are not matched (similar trend and resonances) with the results in case of both reflection and transmission characteristics (Figure 4.17 and Figure 4.18). So we consider the next parasitics as millimeter wave probe used in the measurement.
3. An EM model of millimeter wave probe is developed and used the same strategic way to match with measured results. We are able to match the EM model results (same trend and resonances) with the measured results (Figure 4.24). **The total parasitics includes the device under test with adjacent cells on the sides of DUT and millimeter wave probe model** (Figure 4.22(d)). In addition, **we concluded the additive parasitics from the same direction as port is negligible and there is an impact of the millimeter wave probe model in the EM model de-embedding.**

Finally, we used the realistic EM model to test the de-embedding using TRL and Half-Thru de-embedding. The excessive losses appear in the de-embed results, as similar as the de-embed results of measurement (Figure 4.25). The variation in the results of the realistic EM model is because of the millimeter wave probe, since it is just an EM model in actual scenario, it can be different and all the characteristics of the probe is difficult to model. Finally, we presented the reasons for excessive loss happening at on-wafer measurement. The evaluated solutions will be explained in the further section.

4.5 Solutions

Here we discuss the possible solutions to eliminate the excessive losses in the measurement. Apart from the millimeter wave probe, the adjacent cells are the major reason. Therefore, to avoid the excessive loss the adjacent cells/devices can be separated from the device under measure. Here we evaluate the gap, Gp between the adjacent cell and measurement is shown in Figure 4.27(b). The gap, Gp is evaluated from 15 µm to 250 µm. In the reality, the transmission lines are separated by 50 µm. The de-embed results of CPW transmission lines which is simulated with different gap Gp 15 µm to 250 µm is shown in Figure 4.27(a).

The simulated results are compared with the measured results (Half-Thru- DUT CPW Zc 50Ω) and the de-embed results with no adjacent cells (Half-Thru- HFSS MsPrb NoAdj). From the results, we can observe that, when the gap between the adjacent cell decreases, the α increases. The discontinuity in the α decreases, when the gap between adjacent cell and the device under measure increases. When the gap is above 200 µm, the α of the line is closest (0.2 dB at 70 GHz) to the α of the line without adjacent cells. Therefore, for a **good on-wafer measurement without having an excessive loss in the attenuation need the adjacent cells to be separated by > 200 µm especially on the sides of the DUT.**



(a) (b)

Figure 4.27. (a) Attenuation coefficient with different Gap for Adj.Cells in sides (b) Adj.Cell Gap (Gp)

4.5.1 Conclusion of On-wafer Measurement Issues and Possible Solutions

The reasons for the excessive are due to,

1. Parallel plate propagation due to millimeter wave probe
2. Extended propagation towards the adjacent cells on the sides of the DUT
3. Possibility of TE and TM modes, which are interacting with the dominant mode of the DUT

The possible solutions to reduce this ambiguity in the attenuation coefficient is to separate the adjacent cells by >200 µm. This will reduce the second reason, which is extended propagation due to

adjacent cells. The parallel plate propagation due to millimeter wave probe depends on the probe used for the measurement. Therefore, it is better to use a probe, which has less probe to substrate coupling. We are not able to model the radiation phenomena of the probe, since the restrictions of the available data. The substrate has to make as thin as possible to increase the critical frequency of the TE and TM mode interaction.

4.6 Half-Thru De-embedding and Thru-Load De-embedding Analysis

Various properties of the S-CPW transmission line is considered to evaluate the Half-Thru de-embedding [2]-[3] and Thru-Load de-embedding method, which is developed to characterize the device until 250 GHz. Here we compare the de-embed results from the actual measurement using Half-Thru de-embedding method and Thru-Load de-embedding method, with the realistic EM model. The measurement results are shown until 110 GHz.

4.6.1 De-embedding with Different Length of the DUT

The Half-Thru de-embedding and Thru-Load de-embedding is performed by different length of the DUT (S-CPW Transmission line) to prove these methods have good accuracy over millimeter wave and sub-millimeter wave frequencies for different lengths of DUT. With the increasing or decreasing size of the DUT, the attenuation and phase of the propagation is going to affect the de-embedding of the DUT. Therefore, it is important to de-embed the different lengths of DUT's in order to prove that the Half-Thru de-embedding and Thru-Load de-embedding can work well in all cases. The DUT are S-CPW transmission lines with a length of 200 µm and 800 µm with constant *Zc* of 50 Ω. S-CPW accesslines of 100 µm are used to connect the DUT and the pad. The *Load* value is taken from the open-short de-embedding load value extraction. In addition, the de-embedding structures are modeled with the realistic EM model (two adjacent cells on the sides of DUT with millimeter wave probe model) for the comparison. To analyse the results, the characteristic impedance and attenuation coefficient of the S-CPW transmission lines are calculated and plotted.

The characteristic impedance (*Zc*) for the S-CPW transmission line of 200 µm is already evaluated in the beginning of this chapter (see Figure 4.8(a)). It shows good accuracy (<3% error) and comparable results with TRL. Since Thru-Load de-embedding is a simplified method of Half-Thru de-embedding, the results will be similar. The attenuation constant of S-CPW is also plotted (see Figure 4.8(b)) and the reasons for the excessive loss are explained in the section 4.4.7.

The characteristic impedance of de-embedded S-CPW transmission line of 800 µm is shown in Figure 4.28(a). The de-embed results of the measured line using Half-Thru de-embedding (Half-Thru-DUT SCPW 800 µm*)* and Thru-Load de-embedding (Thru-Load-DUT SCPW 800 µm*)* is compared with the

de-embed results of realistic EM model (Half-Thru-HFSS_MSPrb_Adj2S). However, there is a variation of 4 Ω in EM model in characteristic impedance value, this can be due to the process variation factors in the technology. Nevertheless, the trend of the EM model de-embedding follows similar as measured de-embedded results, so the model is valid for the analysis of on-wafer measurement issues. As shown in Figure 4.28(b), the attenuation coefficient of the realistic EM model follows the same trend as the measured results. The dominant TM mode appears at 32.2GHz; beyond this frequency the attenuation have large noise. This confirms that, we can apply the same reasons (see 4.4.7) to explain the discontinuities in the attenuation coefficient.

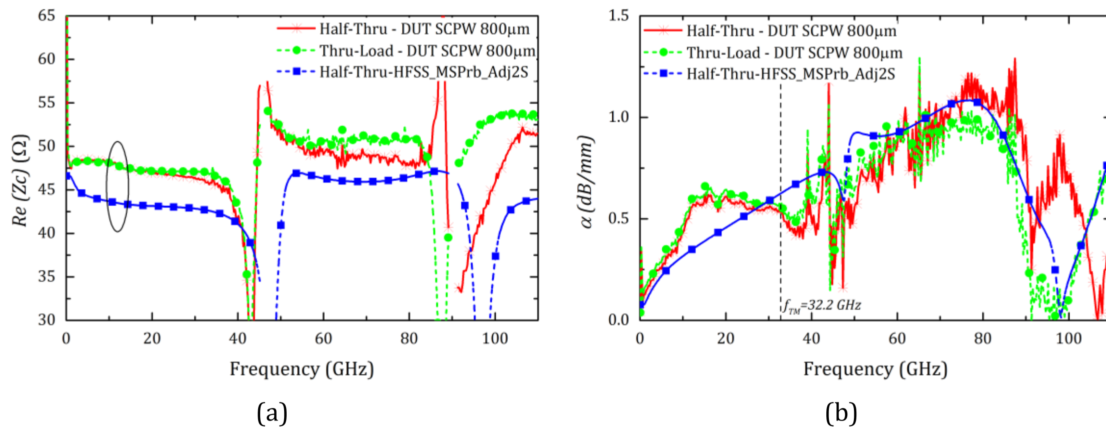


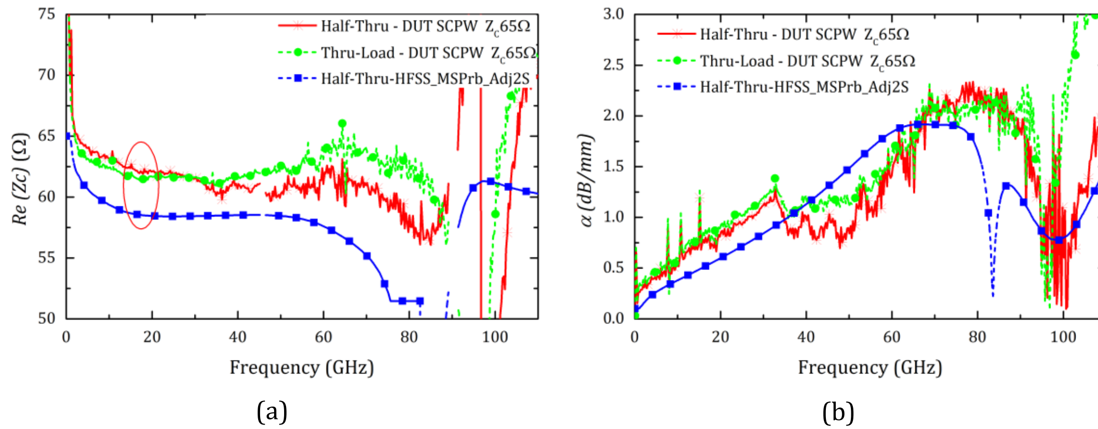
Figure 4.28. Half-Thru and Thru-Load de-embedding: DUT SCPW 800 μm, Zc=50 Ω (a) Characteristic Impedance (b) Attenuation coefficient

4.6.2 De-embedding with Different Characteristic Impedance of DUT

The Half-Thru de-embedding and Thru-Load de-embedding has to be performed by different impedance characteristics Zc of the DUT. This proves the de-embedding method can be performed with different DUTs. In addition, this proves the impedance change from accessline to DUT can be effectively taken into account for the de-embedding. For proving this concept we tested DUT S-CPW transmission line with different characteristic impedance, Zc=65 Ω (50 Ω: already exists) with length of the S-CPW transmission lines 400 μm. S-CPW accessline of 100 μm used to connect the DUT and the pad.

The characteristic impedance (Zc) and attenuation coefficient (α) of S-CPW transmission line of Zc 65 Ω is shown in Figure 4.29(a) and Figure 4.29(b) respectively. The characteristic impedance of Half-Thru de-embedding and Thru-Load de-embedding has comparable results and it is also comparable with the realistic EM model results. However, the variation of 4 Ω in EM model can be due to the process variation factors in the technology, but the trend of the EM model de-embedding follows similar as measured de-embedded results. This proves the Half-Thru de-embedding and Thru-Load de-embedding can work well with the different characteristic impedance/DUT. The attenuation coefficient (α) (see Figure 4.29(a)) shows the similar trend with a resonance shift. The resonance shift

can be a problem of an improper millimeter wave probe model or the process parameters of the technology.



(a) (b)

Figure 4.29. Half-Thru and Thru-Load de-embedding: DUT SCPW *Zc*=65 Ω (a) Characteristic Impedance (b) Attenuation coefficient

4.6.3 Half-Thru De-embedding with Different Load Extraction Methods and with Different Load Values

The key idea of the Half-Thru is to know the value of the *Load* and which should be different from the impedance value of the pad or interconnect. If we are able to determine the value, we can de-embed the device for entire band of frequency with high accuracy. The extraction of the *Load* value and the comparison of the methods are explained in the section 4.3.2. These Load values are used to perform the Half-Thru de-embedding. S-CPW transmission line of *Zc* 65 Ω with a length of 400 μm is used to perform the method. We used the *Load* value of Z_{Load} 100 Ω loaded at the Half-Thru.

To analyse the results, the characteristic impedance (*Zc*) of the S-CPW transmission lines are calculated and shown in Figure 4.30(a). The de-embed results of the measured line using Half-Thru de-embedding with different load extraction methods are shown as “Half-Thru: Load(Open)”for the load extraction using Open de-embedding, “Half-Thru: Load(Open-Short)”for the load extraction using Open-Short de-embedding, “Half-Thru:Load(Kolding)” for and the load extraction with Kolding’s method. De-embed results of the realistic EM model is shown as “Half-Thru-HFSS_MSPrb_Adj2S”. As shown in Figure 4.30(a) the characteristic Impedance of DUT S-CPW *Zc 65* Ω using different load extraction methods (Open de-embedding, Open-Short de-embedding and load extraction with Kolding’s method) show great agreement with each other. Similarly the de-embed results with the EM model follows same trend as the measured results.

Note: The Thru-Load de-embedding method is not included, since the method is comparable with Half-Thru de-embedding method.

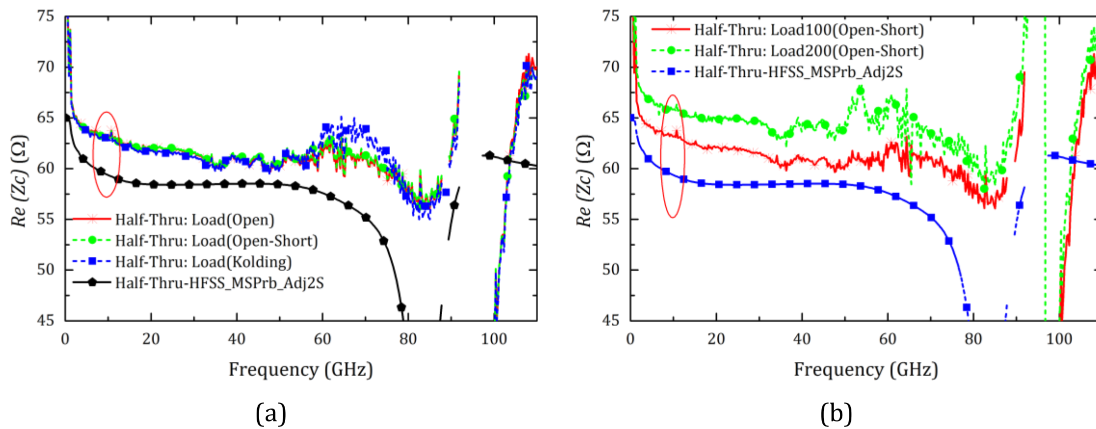


Figure 4.30. Half-Thru de-embedding: Characteristic Impedance (a) Different Load Extraction methods (b) Different Load Values

The Half-thru de-embedding has to be performed by different *Load* values, which is loaded at the Half-Thru. This is to test the method can work with different load values, which is available according to the device technology. S-CPW transmission line of *Zc* 65 Ω with a length of 400 µm is used to perform the method. The different Load values of Z_{Load} of 100 Ω and 200 Ω are used to de-embed the DUT. Open-Short de-embedding method is used to extract the Load value.

Characteristic impedance (*Zc*) of the S-CPW transmission lines are calculated and shown in Figure 4.30(b). The de-embed results of the measured line using Half-Thru de-embedding with different load values are shown as "Half-Thru: Load100(Open-Short)" and "Half-Thru: Load200(Open-Short)" for the load value of Z_{Load} of 100 Ω and 200 Ω. De-embed results realistic EM model is shown as "Half-Thru-HFSS Model". The characteristic impedance of DUT S-CPW *Zc* 65 Ω using Half-thru de-embedding with different load values are sensitive to the value of the load value about 4 Ω. This variation can be due to the process variation in the chip, which is not constant throughout the fabrication, also there will be effects of adjacent devices and other measurement parameters. Thee EM model follows the similar trend as the measured results.

4.6.4 De-embedding with Different Accessline Topology

De-embedding is performed with different accessline models. Considering the accessline, we should have a good propagation in front of the DUT to have a good de-embedding [2]. To prove this concept we fabricated S-CPW transmission line as DUT with different accesslines, such as S-CPW, combination of microstrip with S-CPW, microstrip accessline only, directly connected to the S-CPW transmission line (no accessline) DUT and CPW accessline.

The characteristic impedance and attenuation coefficient are calculated from de-embed results and shown in Figure 4.31(a) and Figure 4.31(b) respectively. From the attenuation results, it is difficult to analyse the accuracy of the de-embedding with different accesslines. **Nevertheless, from the**

observed results show that the microstrip accessline and combination of microstrip with S-CPW creates higher loss in the DUT compared to the other accesslines. In addition, the characteristic impedance is the dropping off above 60 GHz for both microstrip accessline and combination of microstrip with S-CPW compared to other accessline topology. This proves microstrip accessline and microstrip with S-CPW accessline overestimates the loss in DUT. According to the simulated results present in the previous chapter (Chapter 3, Section 3.4.3), we recommend to use S-CPW accesslines for S-CPW DUT.

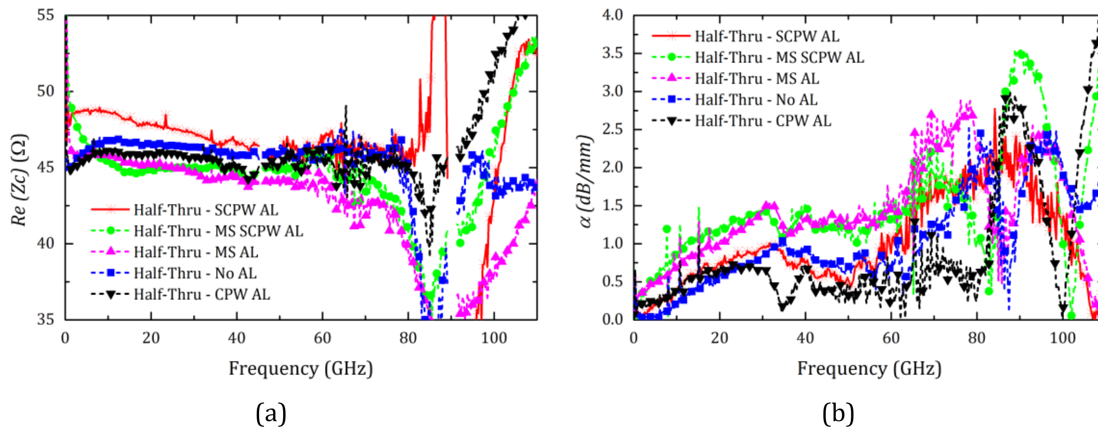


Figure 4.31. Half-Thru de-embedding: Different Accessline (a) Characteristic Impedance (b) Attenuation Coefficient

4.6.5 Comparison and Benchmarking of de-embedding methods

Comparison and Benchmarking for Half-thru de-embedding and Thru-Load de-embedding is tested with other de-embedding methods from lumped circuit equivalent model to cascaded matrix with lumped equivalent models. Vandamme method [22] is chosen to test the Lumped Circuit Equivalent model. L-2L Kolding [7], Hernandez method [25] and TRL [4] are used to test the Cascaded Matrix based de-embedding methods. For cascaded matrix with lumped circuit equivalent models, Mangan method [23] and Thru-only de-embedding [24] were chosen. S-CPW transmission line with Zc 65 Ω is used to evaluate the de-embedding methods. The de-embed results (characteristic impedance) of Cascaded matrix model with Half-Thru de-embedding and Thru-Load de-embedding are shown in Figure 4.32(a). The de-embed results of Lumped Circuit Equivalent model and Cascaded Matrix with Lumped Circuit equivalent model with Half-Thru de-embedding and Thru-Load de-embedding are shown in Figure 4.32(b).

As shown in Figure 4.32(a), the Half-Thru de-embedding and Thru-Load de-embedding are comparable with TRL in the entire band. Considering the L-2L Kolding method, it has good accuracy until 110 GHz about < 5 % error compared to Half-Thru de-embedding, Thru-Load de-embedding and TRL. L-2L Kolding gives good results until 100 GHz, even in simulations. So potentially, L2-L Kolding can use to de-embed the transmission line ~ 100 GHz with a symmetrical pad. Hernandez method is

accurate to de-embed a transmission line nearly ~ 60 GHz. Even the Hernandez method utilizes symmetrical assumption of the pad, so the accuracy is limited.

Considering the Vandamme method (Lumped Circuit Equivalent model) the accuracy drops above 30 GHz , because of lumped circuit assumptions. Considering the cascaded with lumped methods such as Mangan and Thru-only de-embedding (Figure 4.32(b)), the impedance start to drop drastically beyond 30 GHz. However Mangan and Thru-only de-embedding methods cannot accumulate the series parasitics that are present in the pad and accessline, hence the accuracy for the impedance drops off at higher frequencies.

With the restriction of the VNA, we tested all the methods until 110 GHz only. The actual aim is to measure and prove Half-Thru de-embedding and Thru-Load de-embedding is working until 250 GHz , that will be our first perspective.

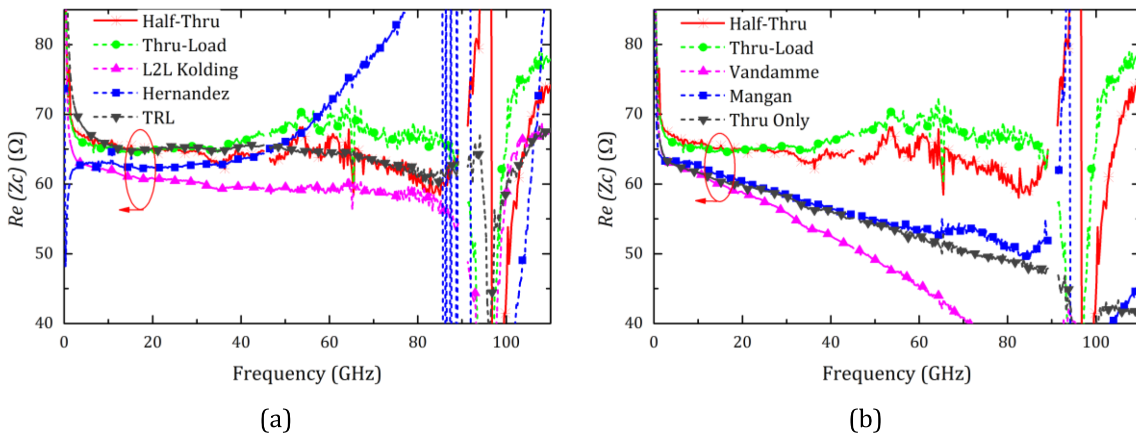


Figure 4.32. Comparison and Benchmarking: Half-Thru and Thru- Load de-embedding (a) Cascaded matrix Based methods (b) Lumped Circuit Equivalent and Cascaded with Lumped Circuit Equivalent methods

4.6.6 De-embedding with Bended-Accessline Model

De-embedding is performed with bended-accessline model to prove Half-Thru de-embedding and Thru-Load de-embedding will work with any kind of parasitics. S-CPW of Zc 50 Ω with bended-accessline shown in Figure 4.33(a). The Bended-accessline is modeled with a combination of microstrip and S-CPW accessline, shown in Figure 4.33(b). For a good propagation, we used S-CPW accessline in front of the DUT.

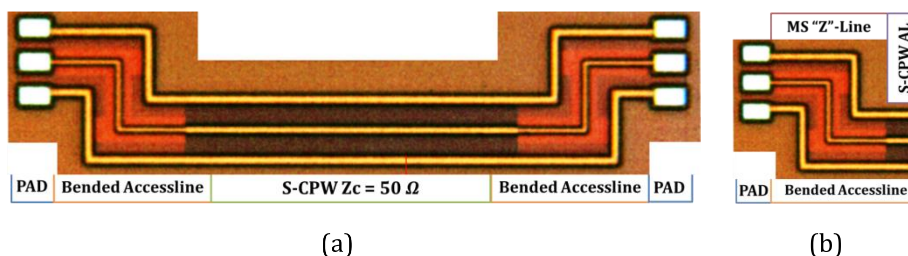


Figure 4.33. (a) S-CPW DUT with Bended-Accessline (b) Bended-Accessline

The characteristic impedance (Zc) and attenuation coefficient (α) are calculated from de-embed results are shown in Figure 4.34(a) and Figure 4.34(b) respectively. TRL is performed to compare with the Half-Thru de-embedding and Thru-Load de-embedding. The other de-embedding methods are not presented due to its accuracy. Apart from L-2 L Kolding method, all other methods are limited below 60 GHz in our case (see Figure 4.32). Nevertheless, L-2L Kolding method will only work with symmetrical pad/accessline parasitics, so it is not valid for bended-accesslines with the combination of microstrip and S-CPW accessline.

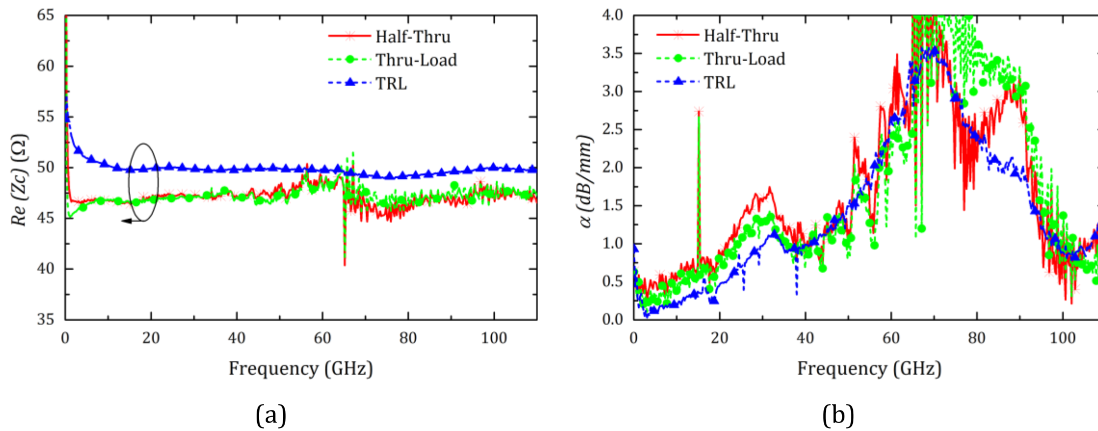


Figure 4.34. Bended-Accessline (a) Characteristic Impedance (b) Attenuation coefficient

Considering the characteristic impedance of the line, Half-Thru de-embedding and Thru-Load de-embedding shows comparable and performant results with respect to TRL (<3% error) until 110 GHz. This proves both the methods are highly comparable and recommended for any kind of parasitics de-embedding. Compared to TRL, the number of de-embedding structures are less and hence the cost reduction. In addition, there is no unknown parameter in Half-Thru de-embedding and Thru-Load de-embedding. It is difficult to analyse the accuracy from the attenuation coefficient results, but all the methods follows the similar trend. The excessive loss or the discontinuity in the attenuation coefficient is explained in the section 4.4.7.

4.6.7 Conclusion of Half-Thru De-embedding and Thru-Load De-embedding Analysis

Half-thru de-embedding and Thru-Load de-embedding are analysed for different parameters of the transmission lines such as different length and different characteristic impedance. Both the methods show similar/comparable results with each other. In addition, Half-Thru de-embedding is verified for different load extraction method to extract the load value that is loaded in the Half-Thru. Half-Thru de-embedding and Thru-Load de-embedding can be implemented with different load extraction methods. Even comparing the other de-embedding structures, it will not take much wafer size. Further we presented the comparison and benchmarking with other de-embedding methods and de-embedding with bended–accessline.

4.7 Half-Thru de-embedding and Thru-Load de-embedding in B55 nm Technology

Half-Thru de-embedding and Thru-Load de-embedding is implemented for S-CPW transmission line in the new technology BiCMOS 55 nm [26]. The measurement model of S-CPW transmission line with *Zc* 50 Ω with the de-embedding structures are shown in Figure 4.35. The S-CPW is measured until 150 GHz with new measurement system implemented in IMEP-LAHC.

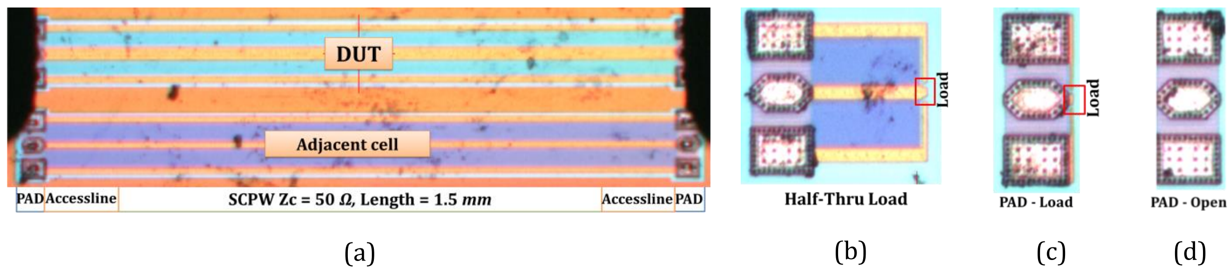


Figure 4.35. BiCMOS 55 nm Technology (a) S-CPW *Zc* 50 Ω Measure (b) *Half-Thru Load* (c) DUT Load (d) *Open*

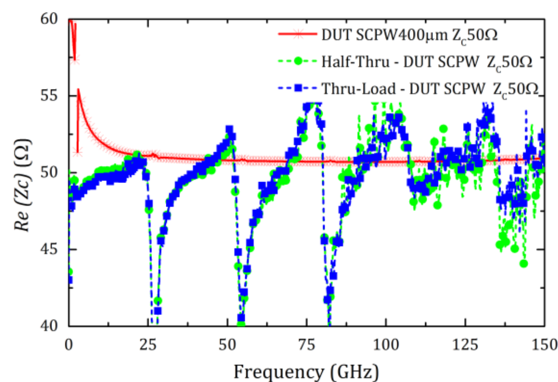


Figure 4.36. Half-Thru and Thru-Load de-embedding: Characteristic Impedance

The de-embed results of characteristic impedance (*Zc*) is shown in Figure 4.36. As shown in Figure 4.36, the Half-Thru de-embedding and Thru-Load de-embedding have comparable results and good agreement with the simulated S-CPW line (<5% error) until 150 GHz . This shows that Half-Thru de-embedding and the Thru-load de-embedding have accurate results for different technologies. However, the S-CPW line is very long, simulation with adjacent cells are not performed to evaluate the attenuation coefficient results.

4.8 Conclusion

Half-Thru de-embedding and Thru-Load de-embedding are performed for the measured transmission lines which are fabricated in AMS 0.35 µm CMOS technology and BiCMOS 55 nm technology. We compared the Half-Thru de-embedding and TRL method for DUT (S-CPW transmission line and CPW). Half-Thru de-embedding and TRL are comparable and accurate until 110 GHz, but the attenuation

coefficient shows an excessive loss or discontinuity over ~60 GHz, (see Figure 4.8(b)). This discontinuity in the attenuation coefficient is an on-wafer problem.

To analyse facts and solutions, we performed different EM model analysis step by step . Finally, we obtain a realistic EM model, which gives comparable results with the measurement. This realistic EM model includes device under test with adjacent cells on the sides and millimeter wave probe model (Figure 4.22(d)). Further, we explain the on-wafer problems and the solutions. The major facts for the excessive loss or discontinuity in the attenuation coefficient are due to,

1. Parallel plate propagation due to millimeter wave probe
2. Extended propagation towards adjacent cells on the sides.
3. Possibility of TE and TM modes, which are interacting with the dominant mode of the DUT.

The possible solutions to reduce this ambiguity in the attenuation coefficient are to separate the adjacent cells by >200 µm to avoid the adjacent cell effects. Also, the substrate has to make thin as possible to avoid the higher order modes.

The Half-Thru de-embedding and Thru-Load de-embedding are tested with different length of the DUT and different impedance of the DUT to prove the method works for different parameters. Also, different load extraction methods and different load values loaded at the Half-Thru are used to determine the accuracy of the Half-Thru de-embedding and Thru-Load de-embedding. Both methods are comparable until 110 GHz from the measured data. The accessline problem shows that the microstrip accessline and microstrip with S-CPW accessline has higher loss compared to the other accesslines for S-CPW transmission line DUT. Finally, de-embedding with Bended-accessline is performed. Both Half-Thru de-embedding and Thru-Load de-embedding have accurate and comparable results with TRL.

We compared and benchmarked these methods with other de-embedding methods. Half-Thru de-embedding and Thru-Load de-embedding have comparable results with TRL, but the TRL used simulated transmission line impedance as reference impedance. L-2L Kolding method is the only one method that has good results until 110 GHz apart from the other methods. Nevertheless, the limitations are not tested beyond 110 GHz. In the simulation, the limitations of L-2L Kolding appear after 100 GHz (see Figure 2.33). Due to the restrictions of the system we are not able to measure beyond until 250 GHz, which is a perspective of the thesis.

4.9 References

[1] AMS 0.35µm CMOS Technology, austriamicrosystems AG, http://ams.com/eng/Products/Full-Service-Foundry/Process-Technology/CMOS/0.35-m-CMOS-Technology-Selection-Guide

[2] V. Velayudhan, E. Pistono, and J.-D. Arnould, "Half-Thru de-embedding method for millimeter wave and sub-millimeter wave integrated circuits," *in Microelectronics and Electronics (PRIME), 2014 10th Conference on Ph.D. Research in*, pp. 1–4, Jul. 2014.

[3] V. Velayudhan, E. Pistono, and J.-D. Arnould, "Comparison of de-embedding Methods for Long Millimeter and Sub-Millimeter wave Integrated Circuits," presented at the *JCMM 2014, 13èmes Journées de Caractérisation Microondes et Matériaux,* Nantes, 24-26 March, 2014.

[4] G. F. Engen and C. A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Trans. Microw. Theory Tech.,* vol. 27, no. 12, pp. 987–993, Dec. 1979.

[5] B. Zhang, Y.-Z. Xiong, L. Wang, S. Hu, and J. L.-W. Li, "On the De-Embedding Issue of Millimeter wave and Sub-Millimeter wave Measurement and Circuit Design," *IEEE Trans. Compon. Packag. Manuf. Technol.,* vol. 2, no. 8, pp. 1361–1369, Aug. 2012.

[6] A. Hamidipour, M. Jahn, F. Starzer, X. Wang, and A. Stelzer, "On-Wafer Passives De-Embedding Based on Open-Pad and Transmission Line Measurement," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM),* pp. 102–105, 2010.

[7] T. E. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," in *Proceedings of International Conference on Microelectronic Test Structure. (ICMTS),* pp. 105–110, 1999.

[8] T. Hirano, K. Okada, J. Hirokawa, and M. Ando, "Accuracy investigation of the de-embedding technique using open and short patterns for on-wafer RF characterization," in *Asia-Pacific MicrowaveConference Proceedings (APMC), „* pp. 1436–1439, *2010*.

[9] W. Shu, S. Shichijo, and R. M. Henderson, "Investigation of the de-embedding issue of CPWs on silicon substrates at high frequency," in *2013 Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS)*, pp. 1–4, 2013.

[10] A.L. Franc "Lignes de propagation intégrées à fort facteur de qualité en technologie CMOS - Application à la synthèse de circuits passifs millimétriques", Thèse de doctorat, Université de Grenoble, 2011.

[11] ANSYS® HFSS, Release 14.0, ANSYS, Inc.

[12] J. Bazzi, "Caractérisation des transistors bipolaires à hétérojonction SiGe à très hautes fréquenc-es," Thèse de doctorat, Université Bordeaux , France, 2011.

[13] C. Raya, Modélisation et optimisation de transistors bipolaires à hétérojonction Si/SiGeC ultra rapides pour applications millimétriques, Thèse de doctorat, L'Université Bordeaux, 2008.

[14] M. Potereau, C. Raya, M. D. Matos, S. Fregonese, A. Curutchet, M. Zhang, B. Ardouin, and T. Zimmer, "Limitations of On-Wafer Calibration and De-Embedding Methods in the Sub-THz Range," *Comput. Commun.*, vol. 01, no. 06, pp. 25–29, 2013.

[15] J. Bazzi, C. Raya, A. Curutchet, and T. Zimmer, "Investigation of high frequency coupling between probe tips and wafer surface," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 87–90, 2009.

[16] Schmiickle, F.J., R. Doerner, G.N. Phung, W. Heinrich, D. Williams, and U. Arz. "Radiation, Multi-mode Propagation, and Substrate Modes in W-Band CPW Calibrations." In *41st European Microwave Conference (EuMC),* 297–300, 2011.

[17] G. N. Phung, F. J. Schmuckle, and W. Heinrich, "Parasitic effects and measurement uncertainties in multi-layer thin-film structures," in *European Microwave Conference (EuMC),* pp. 318–321, 2013.

[18] M. Spirito, G. Gentile, and A. Akhnoukh, "Multimode analysis of transmission lines and substrates for (sub)mm-wave calibration," in *82nd Microwave Measurement Conference (ARFTG),* pp. 1–6, 2013.

[19] L. Galatro and M. Spirito, "Calibration and characterization techniques for on-wafer device characterization," in *IEEE 13th International New Circuits and Systems Conference (NEWCAS),* pp. 1–4, 2015.

[20] Ø. Bjørndal, "Millimeter wave interconnect and slow wave transmission lines in CMOS," Masters thesis, Universitetet i Oslo, 2013.

[21] Cascade Microtech, "Mechanical Layout Rules for Infinity Probes.", Application note,2006

[22] E. P. Vandamme, D. M. M. Schreurs, and C. van Dinther, "Improved Three-Step De-Embedding Method to Accurately Account for the Influence of Pad Parasitics in Silicon On-Wafer RF Test-Structures," *IEEE Trans. Electron Devices,* vol. 48, no. 4, pp. 737–742, Apr. 2001.

[23] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An Improved De-Embedding Technique for On-Wafer High-Frequency Characterization," in *Proceedings of the Bipolar Circuits and Technology Meeting,* pp. 188–191, 1991.

[24] Y. N. Yosuke Goto, "New On-Chip De-Embedding for Accurate Evaluation of Symmetric Devices," *Jpn. J. Appl. Phys.,* vol. 47, pp. 2812–2816, 2008.

[25] J. E. Zúñiga-Juárez, J. A. Reynoso-Hernández, J. R. Loo-Yau, and M. C. Maya-Sánchez, "An improved two-tier L-L method for characterizing symmetrical microwave test fixtures," *Measurement* , vol. 44, no. 9, pp. 1491–1498, Nov. 2011.

[26] Chevalier, P.; Meister, T.F.; Heinemann, B.; Van Huylenbroeck, S.; Liebl, W.; Fox, A.; Sibaja-Hernandez, A.; Chantre, A., "Towards THz SiGe HBTs," *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011 IEEE* , vol., no., pp.57,65, 9-11 Oct. 2011.

Conclusion and Perspective

Nowadays, numerous millimeter and sub-millimeter wave applications are investigated and studied in many domains such as telecommunications (video-streaming (57-66 GHz), automotive radar (76-81 GHz)), imaging (around 140 GHz, 220 GHz)), security, medicine, environmental, etc. The rapid growth and developments in the silicon technology caused miniaturization of components and circuits, especially in millimeter wave integrated circuits. To ensure the best performance of a device we need to measure and de-embed it to obtain its actual characteristics. Currently, most of the de-embedding methods are investigated for frequencies up to 170 GHz. In this thesis, we evaluated several de-embedding methods for millimeter and sub-millimeter wave frequencies and we proposed two new methods. The electromagnetic studies are performed until 250 GHz using Ansys HFSS by considering mainly S-CPW transmission line as DUT. In addition, the measurements are performed until 110 GHz and 150 GHz in IMEP-LAHC for the fabricated devices in two different technologies: AMS 0.35 µm CMOS technology and STMicroelectronics BiCMOS 55 nm.

The initial motivations of this thesis were to,

- Study and analysis the different de-embedding methods for millimeter wave and sub-millimeter wave frequencies by considering S-CPW transmission line and analyses the excessive loss or uncertainties happening at the measurement.
- Benchmark the current de-embedding methods and find out methods works for millimeter wave and sub-millimeter wave frequencies.
- Develop new methods called *Half-Thru De-embedding* and *Thru-Load De-embedding* and compare them to TRL one since this latter remains one of the best methods beyond 110 GHz.

Finally, after having done these tasks, we evaluated and tried to explain the excessive losses measured in S-CPW transmission lines with EM modeling by considering all the parasitics from the on-wafer measurement.

IMEP-LAHC is developing mm-wave circuits based on high-quality factor transmission lines called S-CPW. Therefore, it is important to de-embed the S-CPW transmission line in a wide frequency band to get its original characteristics. Also, analyse the excessive loss or the uncertainties happening in the measurement. In this thesis, we categorized different de-embedding methods into three different types. (1) Lumped Equivalent Circuit Model (2) Cascaded Matrix Based Model and (3) Cascaded Matrix with Lumped Equivalent Models. All these methods are evaluated using both electrical and 3D

electromagnetic simulations. The benchmarking and comparisons for several de-embedding methods with TRL have been performed for S-CPW transmission line as DUT. The lumped-circuit-equivalent methods and cascaded-matrix-with-lumped-equivalent methods are not suitable for the millimeter wave band, because of their lumped-element approximations. Concerning cascaded-matrix-based methods, most of them consider a theoretical assumption of the symmetry topology ($S_{11} = S_{22}$) for each access, which forbid to consider asymmetrical parasitics (either pad or accesslines). In reality, it is not sure that we can have good symmetrical parasitics (either pad or accesslines) assumptions beyond 100 GHz. In addition, these methods are not suitable for bended-accessline parasitics; those are used for different passive devices/circuits. From the electromagnetic analysis, **TRL is the high accurate method for a wide band of frequency.** Theoretically, there is no limitation for TRL in the case of frequency, but there are limitations for the practical use of TRL. TRL gives results referenced to the characteristic impedance of the line, which is unknown a *priori.* In addition, TRL is band limited, to cover the entire frequency range; we required multiple lines, thus the area of wafer and cost increases. These limitations of the current methods give an additional space for developing other de-embedding methods. A new method was proposed here, without any lumped approximations, or symmetrical one. It should be able to take care all the effects of contact pads, interconnects and substrate and less costly since de-embedding structures are lesser than TRL.

Here, we are proposing two new de-embedding methods (Half-Thru de-embedding and Thru-Load de-embedding) to de-embed the S-CPW transmission lines. It can be implemented for one port or two port devices. Thru-Load de-embedding method is an simplified method of Half-Thru de-embedding by eliminating the two line de-embedding structures into a single "Thru" de-embedding structure. In this method, all the parasitics such as pad parasitics or pad-interconnects parasitics are modeled as "Half-Thru" sections. So that all the pad or pad-interconnect parasitics can be well taken into account. This method does not have any lumped model assumptions, symmetry assumptions. This method uses the scattering parameter based calculations. So theoretically, there are no frequency limitations. The major challenge for both new de-embedding methods is to find precisely the value of the load connected at the "Half-Thru". To find out the load value, we de-embed the load fabricated by considering another de-embedding method such as open de-embedding and open-short de-embedding methods and developed a new method based on *S*-parameters called load extraction with Kolding's method. In comparison with TRL, Half-Thru de-embedding and Thru-Load de-embedding methods have no unknown parameter, since the value of load can be obtained by considering the load extraction methods. In addition, these de-embedding methods use less number of de-embedding structures than TRL, thus these methods are cheaper.

Then, an EM simulation study considering or not accesslines to connect the DUT to the pads was done. It allows explaining the proper continuity of propagated waves in front of the device must be

considered to do not affect the accuracy of de-embedding at higher frequencies. Comparison and benchmarking with TRL and other de-embedding methods are performed by considering S-CPW transmission line as DUT. Half-Thru de-embedding method and Thru-Load de-embedding show agreeable results with TRL in both EM simulation (until 250 GHz) and measurement (110 GHz and 150 GHz) for different technologies (AMS 0.35 µm CMOS and BiCMOS 55 nm). Half-Thru de-embedding and Thru-Load de-embedding can work with any kind of parasitics (e.g. bended-accessline).

Finally, we analysed the de-embedding methods with the measured circuits in AMS 0.35 µm CMOS technology. As we mentioned in the introduction, the attenuation coefficient has an excessive loss or discontinuity over ~60 GHz. This phenomenon appears in both S-CPW and CPW transmission lines, so this is an on-wafer measurement problem. We analysed of the excessive loss happening in the on-wafer measurement by considering the EM model. Instead of S-CPW transmission lines, we used CPW transmission line to analyse this phenomena. This phenomenon is analysed by adding the on-wafer parasitics step by step by using the EM model of the measurement scenario. That follows,

1. Comparison of measured CPW line with a basic EM model of measured CPW line, without any extra parasitics
2. Comparison of measured CPW line with a EM model of measured CPW line, with different combination of adjacent cells
3. Comparison of measured CPW line with an EM model of measured CPW line with different combination of adjacent cells and a millimeter wave probe based on infinity probe modeled in EM simulation

Finally, we obtained the realistic EM model for our measured devices. This realistic EM model includes device under test with adjacent cells on the sides and millimeter-wave probe model. Both TRL and Half-Thru de-embedding are performed devices and de-embedding structures based on this realistic EM model. This realistic model works well for both S-CPW and CPW transmission lines. The excessive loss or the discontinuity in the attenuation coefficient is explained by using a realistic EM model. The major facts for the excessive loss or discontinuity in the attenuation coefficient are due to,

1. Parallel plate propagation due to millimeter-wave probe
2. Extended propagation towards the adjacent cells on the sides of the DUT
3. Possibility of TE and TM modes, which are interacting with the dominant mode of the DUT

The possible solutions to reduce this ambiguity in the attenuation coefficient is to separate the adjacent cells by more than 200 µm to avoid the adjacent cell effects. In addition, the substrate has to make thin as possible to avoid the higher order modes. Otherwise, these problems will appear in all de-embedding methods including TRL.

Perspectives

In the thesis, all the simulations are performed for the devices and de-embedding structures until 250 GHz. Due to the restrictions and the availability of the measurement system we are not able to measure the circuits until 250 GHz, which is considered as a first perspective for the thesis. This includes the measurement of the passive load fabricated at Half-Thru until 250GHz to check whether it is possible to implement load for sub-millimeter wave frequencies, currently it is working until 150GHz. Another key idea is to develop multiport de-embedding such as 3 ports and 4 ports de-embedding based on Thru-Load De-embedding [1]-[3]. Another objective is to test these de-embedding methods for other devices: two port and multiport devices developing for RF/millimeter wave applications. In the future it will be interesting to implement an "active load" which can give a given load value at a particular frequency with a DC controlled voltage. Finally, it will be interesting to integrate the other measurement devices as close to the DUT. This is the goal of and objective of the ANR project BISCIG (Build n Self Characterization in G Band) [4]. There is a large possibility to perform measurement and characterisation even in the field of technologies/materials (e.g. 3D integration technologies, TSV characterizations) which are developing for the high frequency applications and packaging [5].

References

[1] M. Wojnowski, V. Issakov, G. Sommer, and R. Weigel, “Multimode TRL Calibration Technique for Characterization of Differential Devices,” *IEEE Trans. Microw. Theory Tech.,* vol. 60, no. 7, pp. 2220–2247, Jul. 2012.

[2] J. Lugo-Alvarez, A. Bautista, F. Podevin, and P. Ferrari, “High-directivity compact slow-wave CoPlanar waveguide couplers for millimeter-wave applications,” in *Microwave Conference (EuMC), 2014 44th European,* pp. 1072–1075, 2014.

[3] A. Serhan, “Conception et réalisation de fonctions millimétriques en technologie BiCMOS 55nm,” phdthesis, Université Grenoble Alpes, 2015.

[4] J-D. Arnould, “Build In Self Characterization In G Band (BISCIG)”- ANR-14-CE26-0027, 2014.

[5] O. E. Bouayadi, “ Module wireless 60 GHz intégré en 3D sur silicium,” phdthesis, Université Grenoble Alpes, 2015.

APPENDIX - A

TRL Algorithm

TRL Calibration is developed by Engen and Hoer [1] in 1979. TRL uses de-embedding structures Thru, Reflect (Open or Short) and Line(s). The measurement model of a DUT test is shown in the Figure 2.5 (see Chapter 2 section 2.1.2.(b)). The Error Box A and the Error Box B is the pad/interconnect parasitics, which has to be de-embedded. The procedure is to find out the error matrices. Consider "*R*" is known as the wave cascading matrix. Consider the Error box A matrix and Error box B matrix are dented by R_a and R_b.

$$R_t = R_a R_b \tag{3}$$

Similarly, the cascaded matrix of the line can be written as,

$$R_d = R_a R_l R_b \tag{4}$$

From (3),

$$R_b = R_a^{-1} R_t \tag{5}$$

So, R_b is obtained from R_a and R_t. Eliminate the R_b from (4), then

$$TR_a = R_a R_l \tag{6}$$

Where,

$$T = R_d R_t^{-1} \tag{7}$$

Where γ represents the propagation constant and l represent the length of the line, which is no-reflecting,

$$R_l = \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{\gamma l} \end{bmatrix} \tag{8}$$

Finally, the elements of R_a and T will be represented by r_{ij} and t_{ij}. Then (6) can expanded as,

$$t_{11}r_{11} + t_{12}r_{21} = r_{11}e^{-\gamma l} \tag{9}$$

$$t_{21}r_{11} + t_{22}r_{21} = r_{21}e^{-\gamma l} \tag{10}$$

$$t_{11}r_{12} + t_{12}r_{22} = r_{12}e^{\gamma l} \tag{11}$$

$$t_{21}r_{12} + t_{22}r_{22} = r_{22}e^{\gamma l} \tag{12}$$

Taking the ratio of (9)to (10) and (11)to (12) gives,

$$t_{21}(r_{11}/r_{21})^2 + (t_{22} - t_{11})(r_{11}/r_{21}) - t_{12} = 0 \tag{13}$$

$$t_{21}(r_{12}/r_{22})^2 + (t_{22} - t_{11})(r_{12}/r_{22}) - t_{12} = 0 \tag{14}$$

Taking the ratio of (12) to (10)gives,

$$e^{2\gamma l} = \frac{t_{21}(r_{12}/r_{22}) + t_{22}}{t_{12}(r_{21}/r_{11}) + t_{11}} \tag{15}$$

Generally, a system of four equations (9) to (12), can be yield four unknowns, where, there unknowns are already obtained.

$$a/c = (r_{11a}/r_{21a}) \tag{16}$$

$$b = (r_{12a}/r_{22a}) \tag{17}$$

And $e^{2\gamma l}$.

The reflection coefficient w_1 obtained at the fictitious port for the two port error A is related to the reflection coefficient of the load by,

$$w_1 = \frac{a\Gamma_l + b}{c\Gamma_l + l} \tag{18}$$

Or

$$a = \frac{w_1 - b}{\Gamma_l(1 - w_1\, c/a)} \tag{19}$$

Similarly, error B yields,

$$\alpha = \frac{w_2 + \gamma}{\Gamma_l (1 + w_2 \, \beta/\alpha)} \tag{20}$$

The unknown reflection coefficient is Γ_l eliminated from (19)and (20),

$$a = \pm \sqrt{\frac{(w_1 - b)(1 + w_2 \, \beta/\alpha)(d - bf)}{(w_2 + \gamma)(1 - w_1 \, c/a)(1 - ec/a)}} \tag{21}$$

Once the value for 'a' for two-port error matrix A is found, the remaining parameters of the error matrix A and B can be easily found. From the '*Thru'* and *'Line'* measurements (15)the values for b and a/c have already been obtained. Then from (3) substituting the matrix we get,

$$r_{22}\rho_{22}\begin{pmatrix} a & b \\ c & 1 \end{pmatrix} \cdot \begin{pmatrix} \alpha & \beta \\ \gamma & 1 \end{pmatrix} = g\begin{pmatrix} d & e \\ f & 1 \end{pmatrix} \tag{22}$$

From (22) the following parameters can be easily obtained,

$$\gamma = \frac{f - dc/a}{1 - ec/a} \tag{23}$$

$$\beta/\alpha = \frac{e - b}{d - bf} \tag{24}$$

$$a\alpha = \frac{d - bf}{1 - ec/a} \tag{25}$$

Hence from the above set of equations all the parameters of the error matrices are found out.

Reference

[1] G. F. Engen and C. A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 12, pp. 987–993, dec. 1979.

APPENDIX - B

Pad parasitics model

The DUT is modeled in BiCMOS 55 nm, and the pad and interconnects are modeled to connect the DUT. The pad parasitics are always in the measurement model and interconnects is optional, depending on the de-embedding methods. The pad is modeled as a microstrip pad in BiCMOS 55 nm as shown in Figure 1(a). To know the approximate or realistic parasitics in the measurement model, the pad is modeled in Ansys HFSS and matched with a lumped electrical model (Pi-model) using Agilent ADS. The parasitic equivalent of a microstrip pad is shown in Figure 1(b). The parasitics of the pad is modeled as a *Pi-model*. This includes the pad capacitance C_P of 18 fF in parallel, series inductance (pad length) L_S of 3.95 pH and with a series resistance is R_S of 0.18 Ω, which is very small and can be neglected.

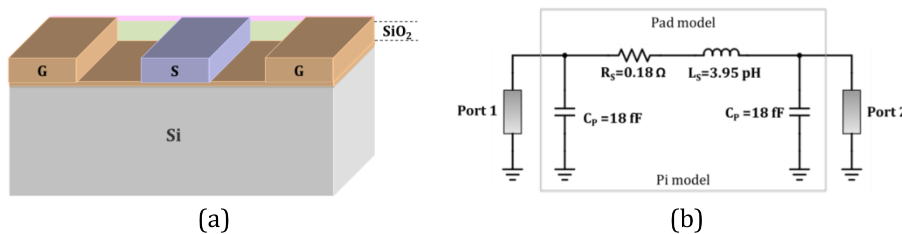


Figure 1. (a) Microstrip Pad model in B55 nm Technology, (b) Equivalent Parasitic Model of the Microstrip Pad

The magnitude of the reflection coefficient (S_{11}) and the transmission coefficient (S_{21}) of the microstrip pad using HFSS and the lumped Pi- model using ADS model is shown in Figure 2(a) and Figure 2(b) respectively. The results show good agreement between the EM model and the lumped Pi-model. This lumped model used to study the known electrical parasitics (lumped parasitics) and benchmark the different de-embedding methods using Agilent ADS.

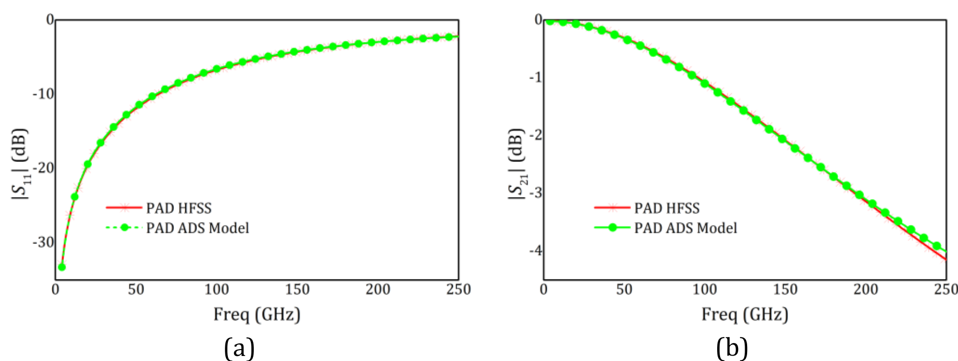


Figure 2. (a) Reflection coefficient of Microstrip Pad (b) Transmission coefficient of Microstrip Pad.

APPENDIX - C

Load Extraction with Thru De-embedding Method

Thru de-embedding Method is based on the direct *S*-parameters de-embedding. The pad parasitics is extracted from the *Thru* (Figure 1(d)), which is obtained from the two lines (see Figure 1(b) and Figure 1(c)) by considering *ABCD* matrix.

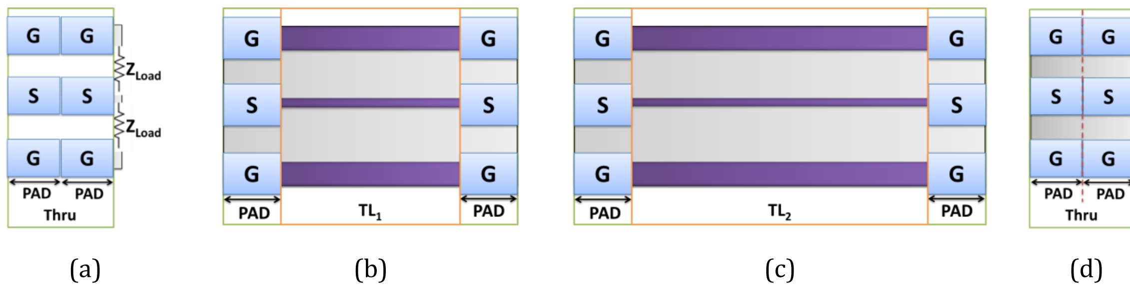


Figure 1. (a) *Load* as DUT with Thru (pad-pad) (b) TL_1 (c) TL_2 (L_2= 2. TL_1) (d) *Thru*

Consider the load as DUT implemented in a zero-thru, which is shown in Figure 1(a). The transfer function of the *Load* can be written by considering the signal flow graph,

$$S_{11L} = S_{11} + \frac{S_{21}S_{12}\Gamma_{Load}}{1 - S_{22}\Gamma_{Load}} \tag{1}$$

By considering the equation (3.12), we can extract the Γ_{Load}, shown in equation (4). Further, we extract load value, using the equation (3.14).

$$\Gamma_{Load} = \frac{S_{11Load} - S_{11Thru}}{S_{21Thru}^2 + S_{11Load}.S_{22Thru} - S_{11Thru}.S_{22Thru}} \tag{2}$$

$$Z_{Load} = Z_O \frac{1 + \Gamma_{Load}}{1 - \Gamma_{Load}} \tag{3}$$

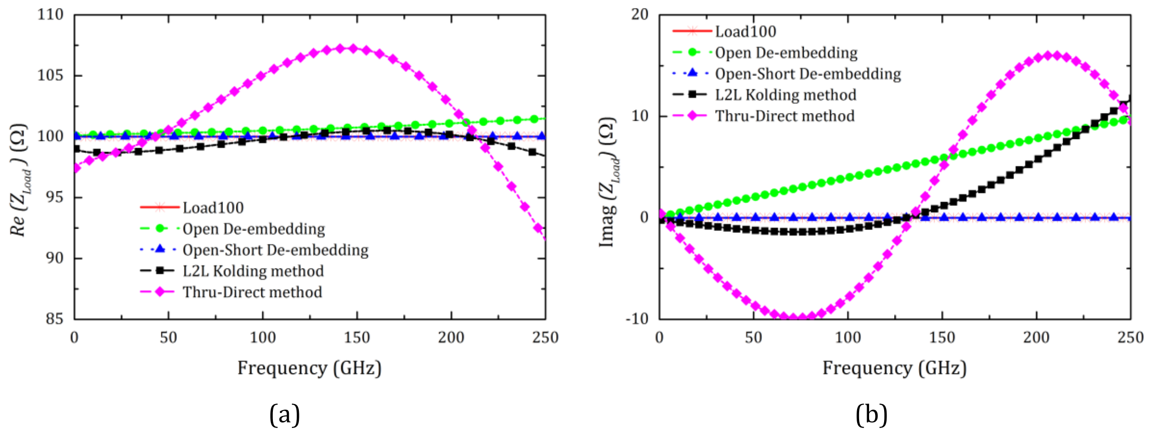
Where, $S_{11\text{Load}}$ is the one port measurement from the DUT implemented in the pad. $S_{11\text{Thru}}$, $S_{22\text{Thru}}$ and S_{21Thru} are from the *Thru*. *Zo* is the port impedance (50 Ω).

Simulation and Results of Load Extraction Methods

The de-embedding structures and *load* are modeled using 3D electromagnetic modeling tool Ansys HFSS and explained in section 3.5.4. The result of the extracted load value with thru

de-embedding method and comparison with other methods are shown in Figure 2. Figure 2(a) shows the real part of the load value and the Figure 2(b) shows the imaginary part of the load value.

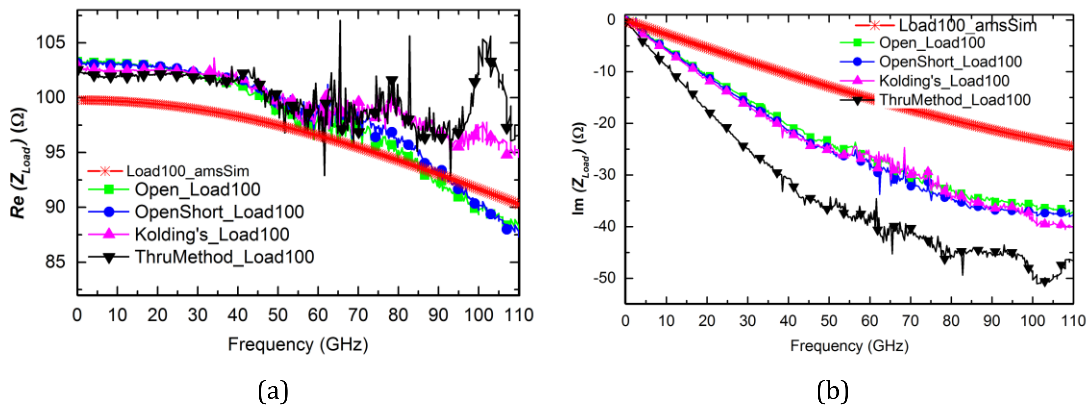
The *"Load* 100*"* (red line) shows the DUT alone, which is loaded by 100 Ω. **The real part of the de-embed load value with Thru de-embedding method shows about 5% error until 100GHz and less than 8 % error in the band 100GHz to 250 GHz.** This method is a more empirical mathematical model, but the error is high compared to the Kolding's method. It is because of long series parasitics (PAD-PAD) [1] present in the load measurement model. The open de-embedding and open-short de-embedding show the good accuracy with respect to the real part of "Load 100" over 250 GHz [2]. Also the load value extraction with Kolding's method [3] shows about <2 % ~250 GHz in the real part of load value. The real part of the *Load* value is more important than the imaginary part, because, error in the real part makes more impact in the reflection coefficient (*Γ*), than the imaginary part.



(a) (b)

Figure 2. Load Value Extraction (a) Z_{Load} (Real) (b) Z_{Load} (imag)

The measurement and load value extraction methods are performed for fabricated *load* until 110 GHz. De-embedded results of *Load* value (the real part of the *Load* (Z_{Load}) and the imaginary part of the *Load* (Z_{Load})) using different de-embedding methods are shown Figure 3(a) and Figure 3(b) respectively.



(a) (b)

Figure 3. Load Value Extraction (a) Z_{Load} (Real) (b) Z_{Load} (imag)

Considering the load value extraction with thru de-embedding method in *Zero-Thru* parasitics gives comparable results with open de-embedding, open-short de-embedding and the Load extraction with Kolding's method until 70 GHz (also, see section 4.3.2). In fact, this method creates an additional parasitics in imaginary part, since the *Zero-Thru* (PAD-PAD) has higher inductive parasitics compared to the single pad. Beyond 70 GHz these methods have about 5 % of variation until 90 GHz from the simulated result and further it increases.

Reference

[1] T. Hirano, K. Okada, J. Hirokawa, and M. Ando, "Accuracy investigation of the de-embedding technique using open and short patterns for on-wafer RF characterization," in *Microwave Conference Proceedings (APMC), Asia-Pacific*, 2010, pp. 1436–1439, 2010.

[2] B. Zhang, Y.-Z. Xiong, L. Wang, S. Hu, and J. L.-W. Li, "On the De-Embedding Issue of Millimeter wave and Sub-Millimeter wave Measurement and Circuit Design," *IEEE Trans. Compon. Packag. Manuf. Technol.,* vol. 2, no. 8, pp. 1361–1369, Aug. 2012.

[3] T. E. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," in *Proceedings of International Conference on Microelectronic Test Structure. (ICMTS),* pp. 105–110, 1999.