UNDERSTANDING ORGANIC THIN FILM PROPERTIES FOR MICROELECTRONIC ORGANIC FIELD-EFFECT TRANSISTORS AND SOLAR CELLS

A Thesis
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctorate of Philosophy in Chemistry

Georgia Institute of Technology
December, 2005

UNDERSTANDING ORGANIC THIN FILM PROPERTIES FOR

MICROELECTRONIC ORGANIC FIELD-EFFECT TRANSISTORS

AND SOLAR CELLS

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I would like to dedicate this work to my lovely wife, Jackie, and our daughter, Brianna. Without their support and love, I would not be the man I am today.

PREFACE

Prior to arriving at the Georgia Tech School of Chemistry and joining the research group of Professor Laren M. Tolbert, little work had been done in the field of conductive polymer chemistry in our group. More specifically, no work in our group had been conducted on organic field-effect transistors, in either the single crystal or thin film state. Therefore, all the work and ideas concerning the OFET project described within this document were newly generated. However, there was sufficient work in this field outside our group, most notably the research groups at Lucent Technologies (Howard Katz and Zhenan Bao, now an associate Professor at Stanford), IBM (Christos Dimitrakopoulos), and Xerox (Beng Ong). Their research has been described in more detail within the Introduction and Chapter 3.

The organic solar cell project has been ongoing in the Tolbert group since 1995 when collaborations began with Greg Smestad, Ph.D. of SolIdeas, Inc. to develop new materials to improve organic cell efficiency. Dr. Smestad's Ph.D. work involved the design and manufacture of liquid photoelectrochemical (PE) cells using titanium dioxide electrodes in an iodine/triiodine redox electrolyte (Figure 1) [1]. Dyes were employed to capture light and enhance electron injection into the electrolyte by improving charge separation. The authors were able to achieve milliamp currents, V_{OC} between 0.4-0.5 V, and approximate 19% photon-to-current efficiency.

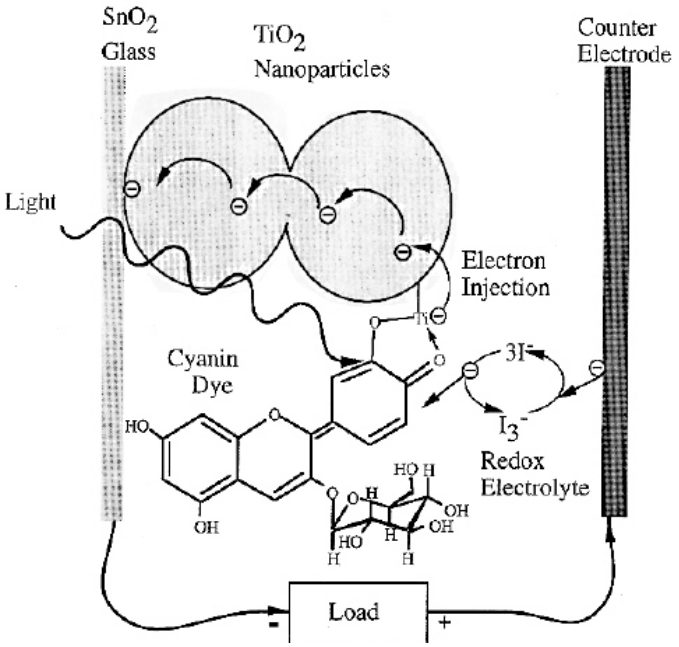

Figure 1 Photoelectrochemical cell using an I/I_3 electrolyte and TiO_2 electrode [1].

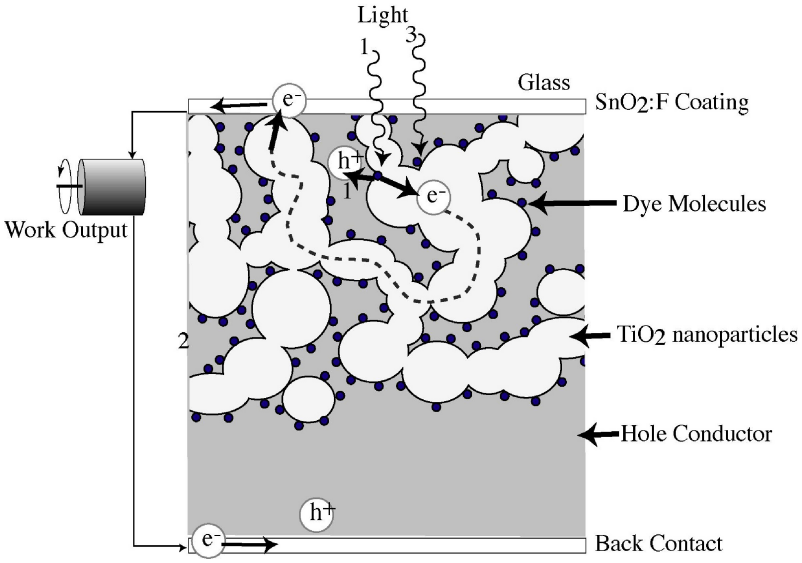

Figure 2 Solid state TiO_2 PV cell with nanoporus TiO_2 [6].

Although the PE cell showed good potential towards a high efficiency cell, the liquid electrolyte had its disadvantages. For one, the cell must be sealed completely to prevent the electrolyte from leaking or drying out. The lifetime of the electrolyte was also an issue, such that there was an observed decrease in efficiency over time. This led our group to propose new research for a solid state device that worked on similar principles to Dr. Smestad's devices. In 2001, our group published a reports doing just that; constructing dye-sensitized solid state titanium dioxide solar cells (Figure 2) [2,6] using previously synthesized poly(4-undecyl-2,2'-bithiopehene) (P4UBT) and P3UBT (Figure 3) [3]. Average J-V values of 60 μA and V_{OC} of 0.65V were comparable to that of the liquid devices using similar device configurations.

Next, the TiO_2 layer was examined to determine the dependence of the PV performance based on the TiO_2 morphology [4]. It was discovered that there was a significant dependence, such that current levels of nanoporus TiO_2 were 5 to 8 times larger than current levels of the flat TiO_2 previously reported. They proposed the increase in current was based on an increase in surface area between the polymer filling the nanopores, thus improving electron injection at the polythiophene-TiO_2 interface. The energy level diagram, shown in Figure B4, was calculated using standard electrochemical cell potentials for HOMO/LUMO estimations and determination of polymer feasibility as both a sensitizer and hole conductor.

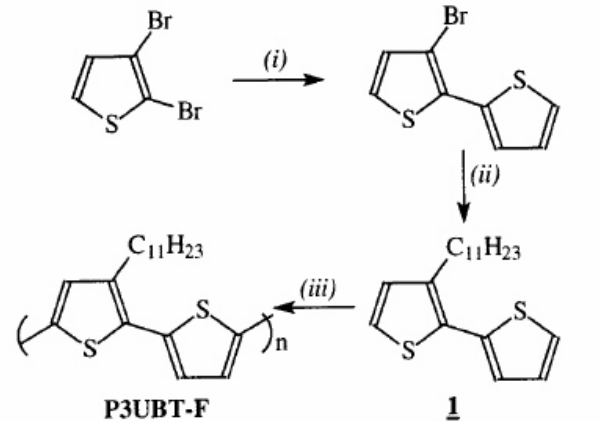

Figure 3 Synthesis of P3UBT [3].

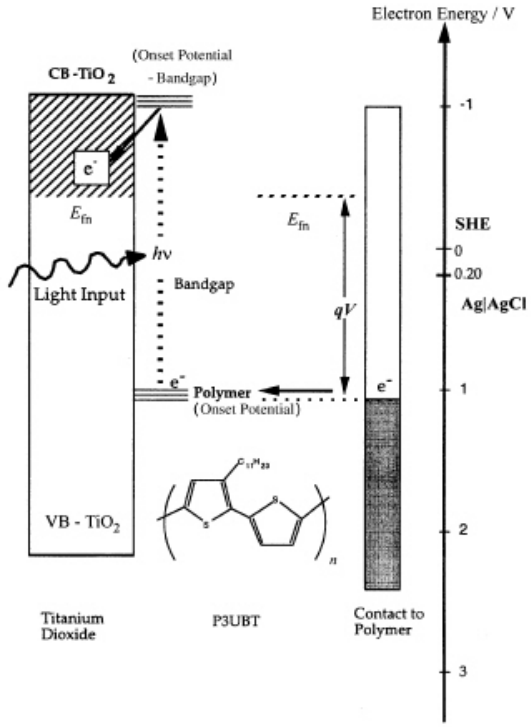

Figure 4 Energy level diagram for the solid state P3UBT-TiO_2 PV cell [4].

Finally, the optical and electrochemical characterization was performed on the P3UBT solid state PV cells [5]. Absorption of the P3UBT thin films were measured for bandgap calculation. CV of the P3UBT was performed to determine the onset of oxidation (0.8V) which provided an estimation of the HOMO level.

With the P3UBT cell almost fully characterized, it was important that we know how the polymer layer was affected upon deposition atop the flat TiO_2. The ability of the polymer to orient on the surface of the TiO_2 would be of importance to hole transport and cell efficiency.

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ACKNOWLEDGEMENTS

I would like to thank all those who help me in my scientific adventure, specifically Dr. Laren Tolbert and Dr. Janusz Kowalik. You provided me with the opportunity, support, and guidance, that without, none of this work would have been possible. I would like to thank my graduate committee, Dr. David Collard, Dr. Art Janata, Dr. Marcus Weck, and Dr. Mohan Srinivasarao for their insight and patience. I would also like to express my deep appreciation for the help of Dr. Christian Kloc at Lucent Technologies for his expertise and collaboration with the fabrication of the single crystal OFET devices. I would like to also thank: Professor Bernard Kippelen and Josh Haddock for the use of their transistor testing equipment, Dr. Victor DeJesus of the Georgia Tech Research Institute for their help with HPLC-EIMS, and Professor Lawrence Bottomley and Dr. Mark Poggi for providing their AFM expertise. Finally, I would like to acknowledge the Department of Energy and the Intel Foundation Fellowship for funding of the work described herein.

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LIST OF SYMBOLS AND ABBREVIATIONS

AAS	Atomic absorption spectroscopy
AFM	Atomic force microscopy
AN	Anthracene
BOE	Buffered oxide etchant
BPP	Bisperipentacene
CI or CIMS	Chemical ionization mass spectrometry
CMOS	Complimentary P-type and N-type metal-oxide-semiconductor transistors
C_{ox}	Internal capacitance per unit area of the insulating layer
CTO	Conductive tin oxide
CVD	Chemical vapor deposition
DHP	6,13-Dihydropentacene
DFT	Density functional theory
DSC	Differential scanning calorimetry
DSSC	Dye-sensitized solar cell
EDX	Electron dispersion X-ray spectroscopy
EI or EIMS	Electron ionization mass spectrometry
F1	Sharp flow profile
F2	Broad flow profile
FEM	Field-effect mobility
FTIR	Fourier transform infrared spectroscopy
FTMS	Fourier transform mass spectrometry
HMDS	Hexamethyldisilizane
^{1}HNMR	Proton nuclear magnetic spectroscopy
HOMO	Highest occupied molecular orbital
HPB	Hexaphenylbenzene
HPLC	High pressure liquid chromatography
IC	Integrated circuit
ICP	Inductively coupled plasma
I_{DS}	Current traveling between drain and source electrodes
I_{DG}	Current traveling between drain and gate electrodes
IV	Current-voltage measurement
J_{SC}	Solar cell current
L	Channel length
LCD	Liquid crystal display
LCMS	Liquid chromatography mass spectrometry
LPCVD	Low pressure chemical vapor deposition
MA6	Karl Seuss mask aligner
MIRC	Georgia Tech Microelectronics Research Center
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	N-type metal-oxide-semiconductor transistor

OFET	Organic field-effect transistor
OLED	Organic light emitting diode
OTS	Octadecyltrichlorosilane
P3HT	Poly-3-hexylthiophene
P3OT	Poly-3-octylthiophene
P3UBT	Poly-3-undecylbithiophene
PAH	Polyaromatic hydrocarbon
PE	Photoelectrochemical solar cell
PECVD	Plasma enhanced chemical vapor deposition
PEEK	Poly(ethyl-ethylketone)
PEN	Pentacene
PMOS	P-type metal-oxide-semiconductor transistor
PPMS	Physical Properties Measurement System
PQ	6,13-Pentacenequinone
PTFE	Poly(tetrafluoroethylene)
PV	Photovoltaic cell
Q_{ox_inv}	Native charge level of oxide
RID	Reactive ion detector
RF	Radio frequency
RMS	Root mean square roughness
SCA	Surface charge analyzer
SCFH	Square cubic feet per hour
SEM	Scanning electron microscope
SRD	Spin-rinse-dryer
T	Thickness
TCB	1,2,4-Trichlorobenzene
TFT	Thin-film transistor
THC	Total hydrogen content
UHP	Ultra-high purity
UHV	Ultra-high vacuum
V_0	Threshold voltage
V_{DS}	Source-drain voltage
V_G	Gate voltage
W	Channel width
XRD	X-ray Defractometer(y)
XPS	X-ray photoelectron spectroscopy
ε	Permissivity of the gate dielectric
μ	Field-effect mobility

SUMMARY

The objective of this work was to understand how the thin film characteristics of p-type organic and polymer semiconductors affect their electronic properties in microelectronic applications. To achieve this goal, three main objectives were drawn out: (1) to create single-crystal organic field-effect transistors and measure the intrinsic charge carrier mobility, (2) to develop a platform for measuring and depositing polymer thin films for organic field-effect transistors, and (3) to deposit polythiophene thin films for inorganic-organic hybrid solar cells and determine how thin film properties effect device performance.

Pentacene single-crystal field-effect transistors (OFETs) were successfully manufactured on crystals grown via horizontal vapor-phase reactors designed for simultaneous ultrapurification and crystal growth. These OFETs led to calculated pentacene field-effect mobility of 2.2 cm^2/Vs. During the sublimation of pentacene at atmospheric pressure, a pentacene disporportionation reaction was observed whereby pentacene reacted with itself to form a peripentacene, a 2:1 cocrystal of pentacene:6,13-dihydropentacene and 6,13-dihydropentacene. This has led to the proposal of a possible mechanism for the observed disproportionation reaction similar to other polyaromatic hydrocarbons, which may be a precursor for explaining the formation of graphite.

Several silicon-based and PET-based field-effect transistor platforms were developed for the measurement of mobility of materials in the thin film state. These platforms were critically examined against one another and the single-crystal devices in order to determine the optimal device design for highest possible mobility data, both

theoretically based on silicon technology and commercially based on individual devices on flexible substrates. Novel FET device designs were constructed with a single gate per device on silicon and PET as well as the commonly used common-gate device. It was found that the deplanarization effects and poor gate insulator quality of the individual gate devices led to lower overall performance when compared to the common gate approach; however, good transistor behavior was observed with field modulation.

Additionally, these thin films were implemented into inorganic-organic hybrid and purely organic solid-state photovoltaic cells. A correlation was drawn between the thin film properties of the device materials and the overall performance of the device. It was determined that each subsequent layer deposited on the device led to a planarization effect, and that the more pristine the individual layer, the better device performance. The hybrid cells performed at $V_{OC} = 0.8V$ and $J_{SC} = 55\mu A/cm^2$.

CHAPTER 1:

GENERAL INTRODUCTION TO POLYMER MICROELECTRONICS

1.1 Historical Prospective

The world of organic electronics has exploded during my tenure as a graduate student, from several large players including IBM, Lucent, and Kodak to nearly 75 research groups across the world racing to find the perfect materials for their organic field effect transistors (OFETs), organic light emitting diodes (OLEDs), and organic photovoltaics (PVs). This influx of new population has resulted in the rapid generation of novel ideas, designs, and results that has launched this field into a new era. Yet, as we embark and attempt to expand this new era of carbon-based electronic materials, we must first understand the field and its evolution. This dissertation begins by explaining the history of inorganic electronics and how the field of organic electronics has evolved from them. It then examines the fundamental transfer of single crystal silicon electronics to single crystal OFETs, specifically pentacene. It then moves into thin film OFETs and attempts to correlate the findings from the single crystal to that of the thin film properties, by examining the 2 key aspects: (1) the device architecture itself, from a common gate to an individual gate platform, and (2) the mobility as it relates in the bulk single crystal and at the interface of the MOSFET device. Finally the materials for which we have studied charge mobility, specifically P3UBT, are then applied towards the manufacture of organic-inorganic hybrid solid-state photovoltaic devices.

1.2 The Transistor

The first transistor was invented in 1947 at Bell Laboritories [1], and the first silicon transistor followed suit in 1954. These rudimentary transistors allowed for base switching; however, it wasn't until the discovery of the integrated circuit (IC, 1958) [2] and metal-oxide-semiconductor (MOS) integrated circuits (1964) that complex, high density, fast switching devices were possible. These MOS transistors led to the development of the transistor radio, calculators and digital wrist watches of the late 1960's and early 1970s.

Today, the MOS transistor (Figure 1.1) is the basis for modern silicon IC fabrication. It rose to this stature not only because of the high electron and hole mobilities of doped silicon, but mainly because of the ease in growing a good dielectric layer on top of the wafer surface. There are two types of MOS transistors: positively charged metal-oxide semiconductors (PMOS, Figure 1.1A) and negatively charged metal-oxide semiconductors (NMOS, Figure 1.1B). The combination of PMOS and NMOS devices on a single wafer is referred to as a complimentary metal-oxide semiconductor (CMOS). Both device types work on the fundamental basis of a p-n junction, whereby a localized area of p-doped silicon adjoins an area of n-doped silicon. In the off state, the holes located within the p-doped area remain, as do the free electrons in the n-doped area.

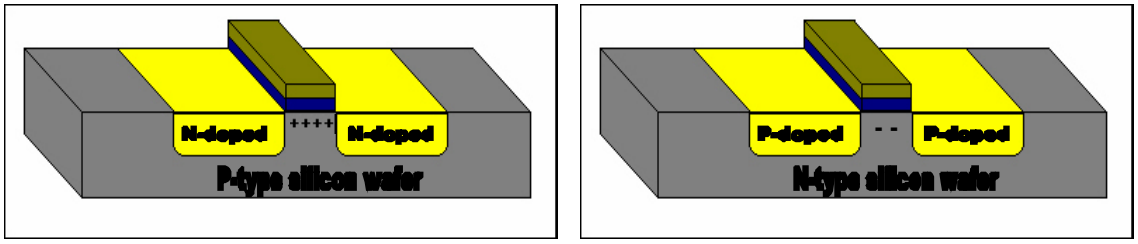
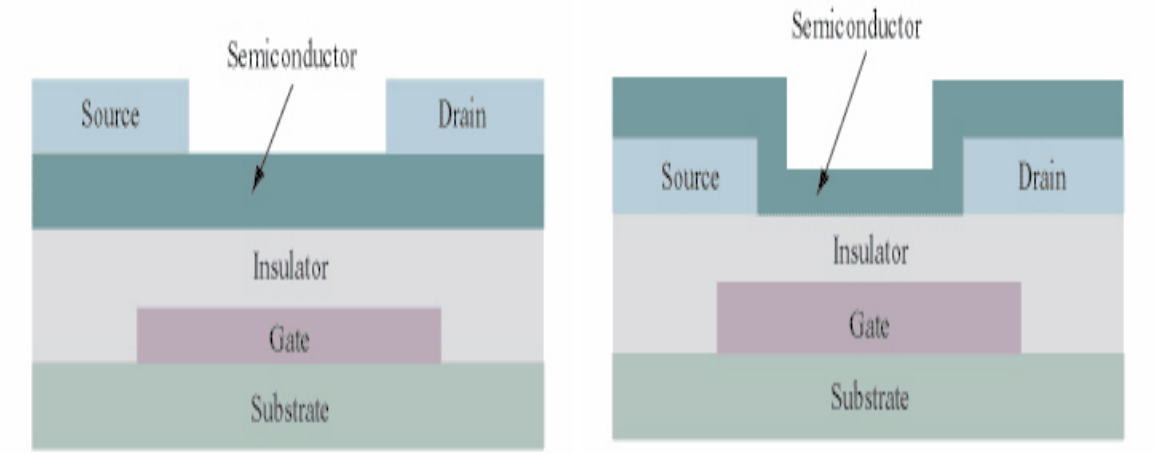


Figure 1.1 PMOS (A) and NMOS (B) silicon device architectures

However, when an electrical field is applied to the junction, the energy levels are decreased, permitting the flow of electrons across the junction. The change in electron flow in the applied electrical field is termed a "field-effect" and thus the transistor is termed a field-effect transistor (FET). Therefore the combination of metal-oxide semiconductors containing p-n junctions with an applied electrical field is a MOSFET.

Organic devices, first described in 1986 [3], were developed using a similar platform. The IC design of an OFET varies between applications; however, there are two main layouts commonly used for developing OFETS based on a common gate approach. Figure 1.2 diagrams the landscape of a top-contact (A) and bottom contact (B) OFET. The substrate acts as the support for the device and is commonly composed of glass, silicon, gold coated or silicon dioxide coated silicon. The gate electrode, which is responsible for turning on and off the applied electrical field, is either the entire wafer or is positioned along one central axis of the substrate. Above the gate electrode is the



Top Contact Bottom Contact

Dimitrakopoulos, C. D. IBM J. Res. & Dev. 2001, 45(1), 11-27

Figure 1.2 Top contact (A) and bottom contact (B) OFET device architectures

dielectric or insulating layer. The function of the layer is to prevent electron transfer between the semiconducting layer and gate electrode. For top-contact thin-film transistors (TFTs), the organic or polymer semiconducting layer is deposited on top of insulator, with source and drain electrodes, composed of gold, resting over-top the semiconducting layer. In bottom-contact TFTs, the source and drain electrodes are positioned over the insulating layer, with the semiconducting layer deposited on top of the electrodes [4].

The applied gate voltage (V_G) regulates the transport of electrons between the source and drain electrodes by reducing the energy barrier of the p-n junction. Once the gate voltage is applied, electron transport can proceed via one of two mechanisms: electrons (n-type) or holes (p-type semiconductor). The transport mechanism and speed are completely determined by V_G and the mobility of the semiconducting material. V_G can then be used as a switch to regulate the flow of electrons. Therefore, there is a great need for the semiconducting layer to respond promptly and efficiently to the switch in V_G [5], as well as have a distinct p-n junction prohibiting the free-flow of electrons between electrodes.

Two key parameters are used to characterize OFETs: field-effect mobility and on/off ratios [6]. Field-effect mobility (FEM) is defined as the average charge carrier drift velocity per unit electric field. FEM can be calculated using Equation 1, where μ represents FEM, V_0 is the extrapolated threshold voltage, W is the channel width, L is the

$$I_{DS} = (WC_{ox}/2L)\mu(V_G-V_0)^2 \qquad \text{Equation 1.1}$$

channel length, and C_{ox} is the internal capacitance per unit area of the insulating layer, in this case the metal oxide. C_{ox} is equal to a factor of the permissivity, ε, of the gate dielectric divided by its thickness (Equation 2). For 1000 Å of thermally grown silicon

dioxide, as seen in Figures 1.1 and 1.2, C_{ox} = 4(8.85E-14)/(1E-7) or 3E-8. Plotting $I_{DS}^{1/2}$ vs. V_G produces a slope equal to $(WC_{ox}/2L)^{1/2}$, from which μ can be calculated [7]. The

$$C_{ox} = n\ \varepsilon_{ox}/\ t_{ox} \qquad \text{Equation 1.2}$$

ratio between the source-drain current in the on and off states is referred to as the on/off ratio. The on/off ratio is strongly dependant on the insulating properties of the gate dielectric and the applied V_G; therefore comparisons should only be made between identical V_G trials and similar device layouts. For device applications, such as driving circuits in LCDs, FEM greater than 0.1 cm^2/Vs and on/off ratio greater than 10^6 are needed [6].

To date only a select few organic semiconductors possess a field-effect mobility similar to silicon [5]. Most p-type organic semiconductors are based on thiophene derivatives [8], while several other systems have been explored based on aromatic macrocyclics, such as metallophthalocyanines [8,9], and fused aromatic rings, such as pentacene [8,10] and tetracene [8,10,11]. In addition, these p-channel semiconductors have reported degradation of the electrodes due to the photo oxidation of the semiconducting layer resulting from their relatively low band gaps and high HOMO levels [12]. Because of the polycrystalline nature of these materials, the charge carrier transport is dominated by the hopping mechanism between crystal grains at room temperature [12-13]. This transport regulates the field-effect mobility; therefore, it is beneficial for the semiconducting layer to be highly ordered thin films with large interconnected polycrystalline grains [14].

1.3 The organic-inorganic hybrid solar cell

The electronics generation has created an ever-increasing demand for energy to fuel the new technologies of the 21st century; therefore, the need for new forms of energy conversion to meet this demand is imperative. Traditional fossil fuel energy sources are finite and their release of waste products into the atmosphere is detrimental to the earth's global environment. As an alternative, methods for efficient conversion of wind, hydroelectric, and solar energy into electrical energy are being explored to solve the world's energy dilemma [15]. Solar power is attractive due to the abundance and consistency of sunlight; therefore, inorganic semiconductors and, more recently, organic-based solar cells have been explored to develop an inexpensive yet efficient method for the conversion of solar light into energy. The first recorded development of standard silicon solar cells occurred in the 1950's when Chapin et al. reported the first crystalline solar cell with a power conversion efficiency of 6% [16]. To date, modern solar energy conversion is still only between 15 and 20% efficient, yet they remain expensive both in development and commercialization [17,18].

Organic materials are being investigated to determine the effectiveness of charge carrier mobilities and charge injection mechanisms in polymer-based solar cells [19], light emitting diodes (LEDs) [20], and field effect transistors (FETs) [21,22]. One approach to low cost organic PV devices is based on the sensitization of a high bandgap material, such as TiO_2 with organic dyes such as cis-$(SCN)_2$ bis(2, 2' bipyridyl-4,4'-dicarboxylate) ruthenium(II) [23]. This dye coordinates to the TiO_2 surface at the interface between the two materials and forms a new light absorbing composite with unique photophysical properties. This dye-sensitized solar cell (DSSC) approach was

pioneered by Michael Grätzel and co-workers at the Swiss Federal Institute of Technology in Lausanne. It has yielded PV devices with efficiencies that are comparable to commercially viable inorganic thin film solar cells (AM1.5 J_{SC} = 16 mA/cm^2 and in sunlight to electrical energy conversion efficiency of 7-10%, as well as quantum efficiencies of 80-90% from 400 to 700 nm) [23]. Only a monolayer of the dye is utilized as the light absorber on the high surface area semiconductor support. The high surface area multiplies light absorption while allowing for efficient charge collection at the dye – TiO_2 interface. Photon-induced charge carrier production and transport are carried out by two different types of materials, the dye, and electron and hole conductors, respectively.

The inorganic layer plays two important roles in an inorganic-organic hybrid DSSC. The main purpose of the inorganic semiconductor is to accept the electron from the excited state of the dye, formed upon absorption of light, while, at the same time preventing recombination of the newly formed electron-hole pair. The better optimized the bandgap of the inorganic material is, vis-à-vis organic sensitizer, the more efficient the charge separation and PV device performance. An astute approach to controlling the interfacial charge recombination dynamics has been recently reported by Durrant et al. [24]. The inorganic layer also acts as a blocking layer by preventing direct, physical contact, and thus avoiding an electrical short between the SnO_2:F electrode and a hole conductor. Inorganic oxides with appropriate bandgaps are typically chosen as inorganic layers in DSSC applications. We have chosen TiO_2 because of its optical and physical properties and our familiarity with synthesis.

The originally developed DSSC PV device utilizes an iodine-iodide redox mediator dissolved in acetonitrile to transport holes [25]. Although the efficiency of

obtained light conversion was spectacular, one limitation of this liquid electrolyte-based DSSC approach is that the use of low viscosity volatile solvents introduces practical limitations when approaching commercialization. A number of solutions have been proposed to solve these problems. One includes replacement of the liquid junction with a gel electrolyte [28-30]. Previous reports have shown that the liquid electrolyte in the DSSC can be replaced with suitable substituted polythiophenes [15,29,30] using a flat (simplified) interface in order to carry out basic studies without the complicating effects of pore filling and light absorption by hole conductors. In these initial studies it was found that one needs to completely understand and control the interface between the organic and inorganic portion of the PV cell in order to facilitate events occurring at that interface. As part of our continuing interest in the development of organic-inorganic hybrid solar cells, we initiated an investigation of the relationship between surface morphology and solar cell performance [15]. The continuation of this work is explained within Chapter 4, where we examine how the multiple layers and their interfacial boundaries affect the overall device's performance.

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CHAPTER 2

ULTRAPURIFICATION, CRYSTAL GROWTH, AND DEPOSITION OF POLYACENES FOR SINGLE-CRYSTAL ORGANIC FIELD-EFFECT TRANSISTORS

2.1 Rationale

Organic and polymer-based semiconductor field-effect transistors (OFETs) are of great interest for low-cost, high production applications including transistors, display circuits, storage devices, and light emitting diodes (LEDs). Across the globe, current research in this field has been devoted to discovering the best materials for these applications; however, it has been shown that in device applications, the semiconductor's environment affects the overall charge mobility within the semiconducting layer [1]. These effects, such as material impurities, contact resistance, device structure, and environmental conditions variably alter the measured intrinsic mobility of the organic semiconductor. It was hypothesized that ultrapurification of these materials would increase their physical and electron mobility characteristics while improving processing conditions. Current methods for transistor production did not incorporate an ultrapurification step, which opens up the possibility of modifying and enhancing these protocols to increase the material's FEM and overall transistor performance. Therefore, we set out to build transistors on top of pure, single crystalline organic materials. This chapter will briefly describe our efforts to ultrapurify pentacene and build transistors using the single-crystalline pentacene. Additionally, described herein is an account and discussion of the observed hydrogen transfer pentacene undergoes at elevated temperatures at atmospheric pressure.

2.2 Development of the HPVD Chamber

Several deposition techniques have been investigated and well published for the deposition of organics and polymers on a variety of substrates [2]. The most common method for the deposition of these materials is solution deposition: a technique for which the material is dissolved in a solvent, added on the substrate, and spin-coated, dip-coated, or microprinted to achieve uniform thickness across the entire substrate. These methods have been found effective for making nanometer thin films; however, due to the poor solubility of some materials such as pentacene in organic solvents, solution deposition techniques have been difficult to consistently yield uniform thin films. Deposition of pentacene thin films is most often prepared by thermal evaporation at approximately 240°C in an ultra-high vacuum (UHV) chamber, with pressures between 10^{-6} and 10^{-9} torr [3]. The equipment required to maintain and operate at UHV is very expensive. Therefore, a deposition method to purify and deposit pentacene and other sublimeable organic materials without the need for solvents or UHV could greatly enhance the commercialization of OFETs.

In 1997, Laudise et al published a report for the purification and crystal growth of sublimable organic materials using a zone heating furnace [4]. This unique apparatus worked by heating the organic starting materials to their sublimation point under a stream of flowing gas at atmospheric pressure. The purified gaseous material deposited further down the furnace where temperatures were controlled at the material's crystallization temperature, whereby any impurities contained within the starting material would continue flowing down the furnace and deposit in the unheated region of the furnace or

within a trap or remained in the furnace. To date, no other method had been developed that incorporated ultrapurification, crystallization, and deposition of sublimable organic semiconductors in a single step without requiring UHV or solvents. Francis Garnier demonstrated that vapor-phase deposition resulted in increased charge carrier properties of OFETs [5]; therefore, we believed that ultrapurification during vapor-phase crystal growth of these materials would increase their physical and electronic properties while simplifying processing conditions and that building transistors onto single crystalline material would allow for intrinsic mobility measurements of organic materials for direct comparison to that of single crystal and amorphous silicon devices.

2.2.1 Experimental Setup

The zone heating furnace shown in Figure 2.1 was built using a similar approach to Laudise et al [4]. Borosilicate glass source and crystallization tubes (Sandy Industrial Glass) were cut and inset within the reactor tube as shown. The exterior diameter of each tube was approximately 20, 17, and 15 mm respectively. The matching of inner and outer diameters was key to prevent gas flow and material loss between tubes. To each end of the reactor tube, Ace 24/40 female ground glass joints were fused using a torch. The corresponding male adaptor was attached to either the regulator of the carrier gas or a bubbler containing mineral oil using Tygon tubing. The purpose of the bubbler was to collect any material not deposited within the tube and to prevent a backflow of air into the system. In alternate experiments, metal connectors were used to connect PTFE tubing to the reactor tube.

The furnace was wrapped in an Omega heating tape Model FGH051-100 (522W, 120V, 0.5"X 10', heavy insulated) at different thicknesses to obtain an exact heating profile (Figure 2.1 inset) and create four distinct heating zones: gas preheat, sublimation, crystallization, and impurity deposition. The temperature of each zone was measured by an Omega HH-12 Digital Thermometer with industry calibrated thermocouples. Accuracy with this thermometer was stated to be within ±2°C and resolution within

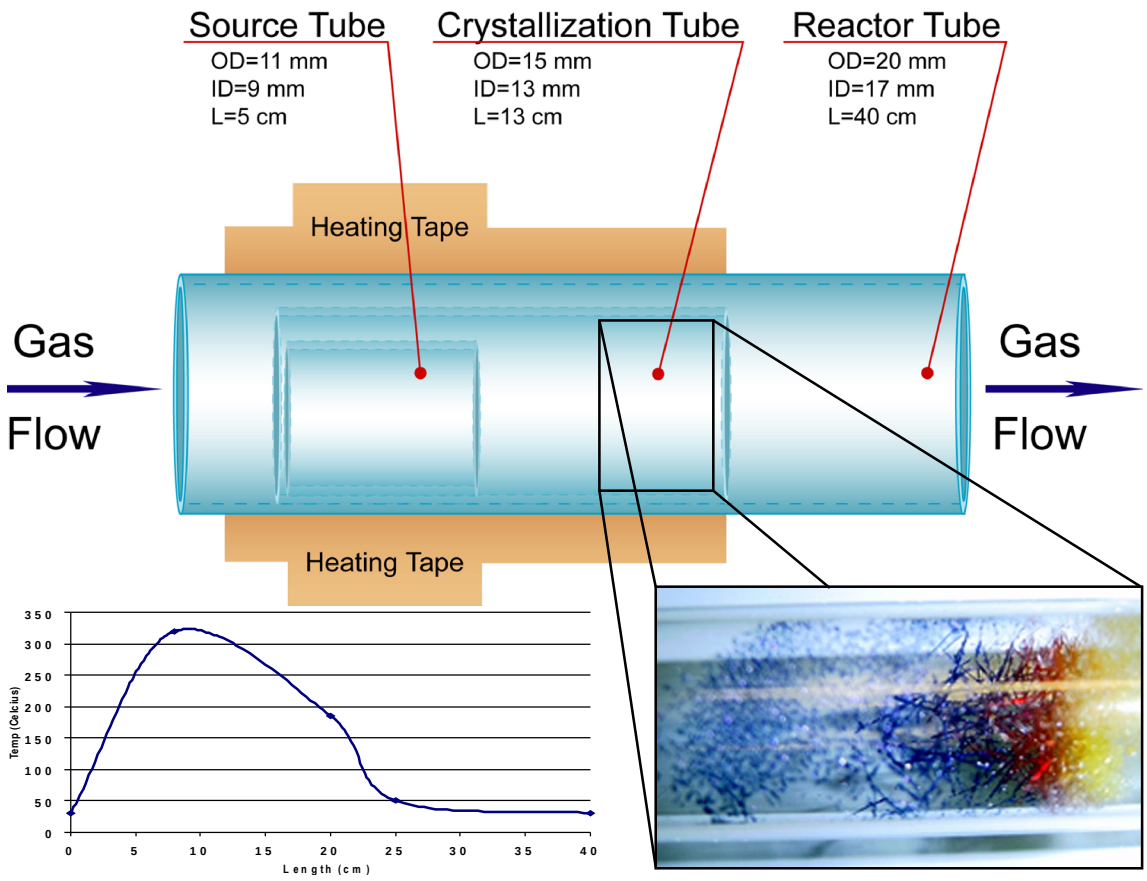


Figure 2.1 Diagram of the Horizontal Physical Vapor Deposition (HPVD) chamber used for the sublimation and crystal growth of pentacene. The temperature profile shows the temperatures measured for the sublimation process along with an aid-to-the-eye line. The inset depicts the overlapping crystal boundaries of purple pentacene crystals with the red and yellow 2:1 **DHP**:pentacene co-crystals.

0.1°C. Heat dissipation through the glass layers was found to be negligible (2-4°C difference) when compared to a calibrated thermometer placed inside the source tube. Several of these glass furnaces were built over the course of the project, and these apparati varied less than 1 mm in wall thickness and each showed identical temperature dissipation through the glass.

A carrier gas was employed to transport the sublimed organic semiconductors between heating zones. The behavior of gas transport has been previously reported for horizontal heating furnaces [4], therefore it was speculated that the velocity and apature of the inlet would affect crystallization and crystal growth. Gas flow was achieved using one of two different methods. The first method, F1, involved connecting the gas inlet tube to a disposable Pasteur pipette and attaching both to an Ace 5028-30 (male 24/40-mini #7 Ace-thread). The resulting setup was attached to a female 24/40 joint fused to the reactor tube. This method resulted in the proposed initial gas flow forced convection pattern [4] shown pictorially in Figure 2.2A. The second method, F2, involved the gas inlet tube connected to an Ace 5216 adapter (male 24/40 joint with hose connector or the metal connector with PTFE tubing). This method of carrier gas introduction resulted in the proposed broader flow pattern shown in Figure 2.2B. This adaptation provided an intermediate between the buoyancy driven convection pattern, as seen in a closed ampule, and the forced convection pattern of F1. Carrier gas flow was measured using standard methods (ie. water displacement) and with an Omega Flow Meter. Gas flow was maintained between 10 and 70 ml/min for all experiments. Carrier gases, purchased from

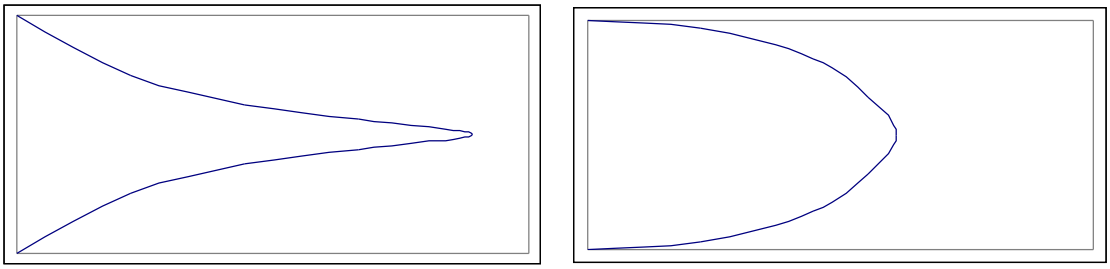


Figure 2.2 Approximated gas flow patterns for the HVPD chamber shown in Figure 2.1: Sharp (A) and Broad (B)

Air Products, used were either Ultra-high purity (UHP) grade argon (99.97% pure, 4 ppm O_2, 1 ppm total hydrogen content (THC)), Mega BIP grade argon (99.9999% pure, ≤0.2 ppm O_2, ≤0.1 ppm THC), or a mixture of 10% hydrogen in nitrogen.

In the gas preheat zone, the carrier gas was heated to improve transport properties and prevent the gas from reducing or destabilizing the sublimation temperature. In the sublimation zone, the starting material was heated to the material's sublimation point. In the crystallization zone the temperature was gradually decreased to stimulate crystallization and slow crystal growth. The impurity deposition zone was kept at room temperature to induce crystallization or deposition of any impurities or byproducts in the system.

2.2.2 Materials

Anthracene (97%), benzene, chlorobenze, 1,2,4-trichlorobenzene, hexaphenylbenzene (98%), pentacene (99+%) and 6,13-pentacenequinone were purchased from Aldrich. Additional penacene was purchased from TCI America. Benzene-d_6 and perdeuterated pentacene (pentacene-d_{14} D, 98%) were purchased from Icon Isotopes.

2.2.3 Characterization Methods

Elemental Analyses were performed by Atlantic Microlabs, Inc. or using a Perkin Elmer Series II CHN analyzer 2400. ^{1}HNMR spectra were acquired in deuterated solvents using a 300 MHz Varian Gemini ^{1}HNMR spectrometer. FTIR samples were pressed in dried KBr and spectra were taken using a Nicolet 520 spectrometer. A Siemens SMART CCD X-ray diffractometer was used for X-ray analysis of single crystals. Solid-state mass spectrometry analyses were performed in both EI (70 and 20 eV) and CI (isobutene) modes on a VG Instruments 70SE. Fourier transform mass spectrometry (FTMS) was performed by Professor Charles Wilkins at the University of Arkansas using a 9.4 T FTMS instrument (IonSpec, Lake Forest, CA). FTMS spectra were obtained by using direct laser desorption using a Nd-YAG laser (New Wave, Sunnyvale, CA) operating at 355 nm. Samples were dissolved in toluene and deposited on a stainless steel target and the toluene evaporated to form the laser desorption sample. UV-Visible spectroscopy was performed on a Perkin-Elmer Lambda 19 UV-Vis-NIR spectrometer. High-pressure liquid chromatography (HPLC) was performed using a ChromegaBond C18 reverse-phase column (25cm x 4.0 mm, 5 μm particle diameter) at 40°C and 1.0 mL/min flow rate in a 75/25 or 70/30 vol/vol HPLC grade acetonitrile:water mobile phase on a Shimadzu VP series chromatograph equipped with refractive index and UV-Vis detectors (210 nm). HPLC-EIMS was performed on a HP 1050 series chromatography using the same column and conditions. Attached to the HPLC was a HP 59980B particle beam/LCMS interface equipped with a HP 5989B electron-ionization mass spectrometer (70 eV). Concentrations of all HPLC samples were 1.0 mg/mL dissolved in mobile phase. X-ray photoelectron spectroscopy (XPS) was used

for comparison of elemental composition. All angle-resolved spectra were collected using a Physical Electronics (PHI) 1600 XPS system equipped with an Al Kα X-ray source. The chamber base pressure during all XPS analyses was at or below 5 x 10^{-9} torr. Flame atomic absorption spectroscopy (AAS) was performed by Galbraith Laboratories, Inc., of Knoxville, TN. A Brooker 1KCCD Area Detector X-ray defractometer (XRD) was used to obtain unit cell parameters for single-crystal structures. Scanning Electron Microscopy (SEM) pictures were taken using a Hitachi 3500H. Melting points were measured on an Electrothermal® Melting Point Apparatus with max temperature of 300°C.

2.2.4 Typical Experimental Procedure

Initially, the reactor tube was wrapped with heating tape and purged with Mega BIP grade argon at a flow rate of 30 ml/min. Heat was applied to the tube to remove any residual water adhering to the glass surface. 100 mg of Aldrich pentacene was placed within the source tube, which was then placed into the deposition tube, and both were placed into the reactor tube from the end with gas exiting from the chamber. A source temperature of 330°C and deposition temperature of 210°C were kept constant during the 4 hour procedure.

2.2.5 Optimization of Test Variables

Test variables described above were standardized for anthracene and pentacene to determine the ability of the multi-stage furnace for the ultrapurification and crystal growth of polyacenes. The amount of starting material consumed was tested at 25, 50, 75 and 100 mg. It was observed that increasing the amount of starting material

gradually increased the crystal size up to a maximum size equaling the diameter of the deposition tube. From this finding, it was only necessary to use 50 mg of anthracene to achieve large single crystals; however for pentacene, 100 mg was necessary to larger crystal growth.

The sublimation temperature of anthracene was varied between 100 and 215°C, and it was determined that a sublimation temperature of 180°C and deposition temperature of 150°C were optimal for this furnace. These trials were repeated for pentacene, and optimal conditions for sublimation were established at 310°C with 185-210°C deposition temperature.

The carrier gas showed very little effect on crystal growth and purification between UHP argon and a mixture of 10% hydrogen in nitrogen. However, the flow rate was crucial to the deposition rate and product formation. A flow rate of 10 mL/min was found to be insufficient for transport of the sublimed material into the crystallization zone, while a flow rate of 70 mL/min resulted in a decrease in crystal size and observations of the material depositing in the impurity zone and bubbler. The optimal flow rate was determined to be 30 mL/min and be kept constant throughout the experiment. The flow profiles were examined, and it was found that the sharper flow profile F1 improved crystallization of products when compared with profile F2. The increase in convection of carrier gas in the center of the furnace helped transport the material between zones more rapidly, decreasing the experimental time. When using the forced convection profile, the experimental time was also dependant on sublimation temperature and amount of starting material. For experimental purposes, the time was varied between 4 and 48 hours, and it

was found that only 4 hours was necessary to effectively sublime 90 percent of the anthracene, HPB, and pentacene starting material for crystallization.

2.3 Purification Results

2.3.1 Anthracene and Hexaphenylbenzene

The purification of anthracene produced large, single-crystalline plates approximately 2 cm in diameter under the optimized conditions. These crystals, shown in Figure 2.3, were further characterized by ^{1}HNMR and EIMS to verify their purity (Appendix 2.1). Complete consumption of starting material was observed at source temperatures above 170°C. These observations concurred with Laudise's results, supporting the accuracy and reproducibility for this method of ultrapurification [4].

Hexaphenylbenzene (HPB) was ultrapurified using operating conditions similar to those for pentacne. Needle-shaped HPB crystals were grown measuring in size up to 1 cm long with complete consumption of starting material. ^{1}HNMR and EIMS spectra showed no evidence of impurities or byproducts in either the ultrapure material or the original material (Appendix 2.2).

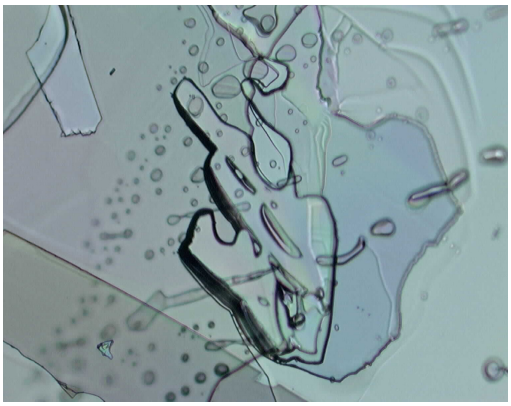


Figure 2.3 Optical microscopy at 10x normal magnification of anthracene crystals grown using the HPVD.

2.3.2 Pentacene

The purification of pentacene produced the unique deposition profile observed at sublimation temperatures exceeding 320°C (Figure 2.1 inset). As the material sublimed, it was transported by the carrier gas to the crystal growth zone, where dark large plate and needle-shaped, dark blue-violet colored pentacene crystals as large as the diameter of the deposition tube were deposited. It was possible to manipulate the structure of the pentacene crystals by adjusting the source and crystallization zone temperatures. At source temperatures between 265 and 285°C and deposition temperatures around 165°C, needle-shaped crystals were produced. Increasing the source temperature to 310°C and deposition temperature of 185°C resulted in single-crystal pentacene plates slightly larger than 2 cm by 1 cm, bigger than previously reported (Figure 2.4). Elemental analysis of the needle and plate-shaped pentacene crystals showed a 100% composition of only carbon and hydrogen and an exact C:H ratio of 22:14 (Table 2.1). FTIR showed presence of only pentacene. X-Ray Diffraction (XRD) lattice structures obtained from the needle and plate single-crystals were identical to other lattice dimensions for vapor-phase grown pentacene recently reported by Anthony et al [6]. Lattice dynamic calculations and lattice dimensions matched those published by Venuit et al for vapor-phase grown pentacene [7].

In addition to the purified pentacene product, yellow and red, needle-shaped crystals, previously identified as a 2:1 6,13-dihydropentacene:pentacene co-crystal [8], were deposited in the impurity deposition zone concomitantly with 6,13-dihydropentacene (yellow powder), 6-pentacenone and 6,13-pentacenequinone (also a yellow powder) (Appendix 2.3) . The color difference between the yellow and red co-

crystals was associated with a slight difference in impurity concentration within the crystal. Pentacene impurities led to the red color, while 6,13-dihydropentacene impurities produced yellow crystals. Removal of impurities led to colorless crystals. Independent of the amount of starting material used, the ratio of residue to pentacene to dihydropentacene was nearly always 25/50/25 percent at source temperatures above 350°C. After purification, a black, glassy residue remained in the source zone (Section 2.4). However, sublimations over extended periods of time at source temperatures below 300°C resulted in no observable formation of any residue or byproducts**.**

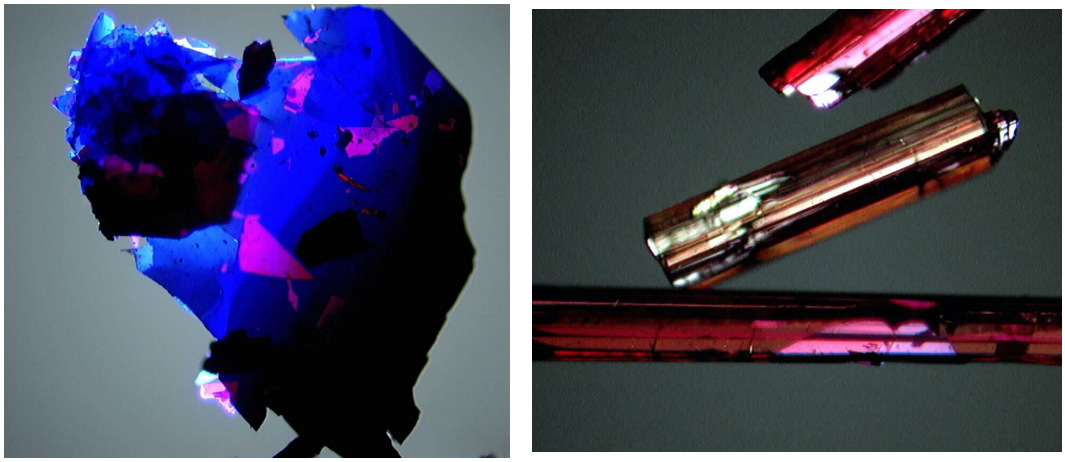


Figure 2.4 Optical microscopy at 10x normal magnification of (A) pentacene crystals and (B) 2:1 6,13-dihydropentacene:pentacene co-crystals grown using the HPVD.

Table 2.1. Elemental analysis and AAS data for pentacene starting material and sublimation products. Theoretical values in parenthesis, including bisperipentacene for the "residue".

Sample	Aldrich Pentacene	Purified Pentacene	Residue	DHP
Element				
% C	95.01 (94.96)	95.00 (94.96)	94.15 (96.70)	93.82 (94.29)
% H	5.10 (5.04)	5.22 (5.04)	4.83 (3.30)	5.82 (5.71)
% O	0.00	0.00	0.00	
% N	0.00	0.00	0.00	0.00
% Fe	114 ppm		719 ppm	
% Al	593 ppm		1.76	

The identity of the carrier gas played little apparent role in the distribution of byproducts formed during sublimation. Using any of the three carrier gases, the production and deposition of dihydropentacene and co-crystal remained relatively unchanged. The use of 10% H_2 in N_2 at these temperatures did not affect the yield of hydrogenated byproducts versus UHP or Mega BIP grade argon. Oxygenated byproducts (6-pentaceneone and pentacenequinone) were observed when UHP grade argon was employed. Oxygen in excess of 2 ppm resulted in the oxygenated products, whereas with Mega BIP grade argon with oxygen concentrations less than 0.2 ppm we were unable to detect any oxygenated products. Due to the formation of 6-pentacenone, pentacenequinone, and 6,13-pentacenequinone-d_{12} (observed by EI/CIMS) using UHP argon, the purification process was examined to determine the source of oxygen. Ridox® and Drierite© ($CaSO_4$) columns installed to remove oxygen and water from the carrier gas failed to hinder the formation of pentacenequinone. Experiments using Mega BIP argon or a vacuum-sealed ampoule at 10^{-3} torr avoided the formation of the corresponding

quinone, yet still produced dihydropentacene and co-crystal with no observable change in yield.

The vapor-phase deposition apparatus provided us the means to obtain ultrapure single crystals of anthracene, pentacene, and hexaphenylbenzene. Although byproducts of a potential disproportionation reaction were observed for pentacene at temperatures above 320°C, single crystals have been produced larger than previously reported with future implementation for organic transistors [9-10].

2.3.3 Identification of Residue

The appearance of the residue within the source tube following the sublimation of pentacene varied based on the source temperatures used during sublimation. At source temperatures between 320 and 375°C, the residue appeared as a black powder; however, at temperatures exceeding 380°C, the residue melted into a glassy state. The identity of the residue was established based on the FTMS spectrum shown in Figure 2.5. As seen in the figure, the mass peak at 546 m/z, measured with resolving power of 100,000, corresponded within 7 ppm to the composition of the previously unknown bisperipentacene (BPP). The distribution pattern of the peaks around 546 m/z could be explained by the positioning of the two pentacene rings relative to one another. A slight off-set in ring fusion or an unfused position would result in an increase in molecular mass by 2, 4, or 6. The peak with m/z 818 corresponded to trisperipentacene with 2 unfused positions (i.e. $C_{66}H_{26}^{+}$). The totally fused trisperipentacene appearing at m/z 814 was less likely to form either due to torsional ring strain of the molecule or statistical mismatches between rings.

The initial FTIR spectrum of the residue exhibited both aromatic and aliphatic C-H stretching [11]. However, further analysis revealed the presence of dihydropentacene in the residue, requiring further purification. Electrical conductivity measurements performed using a Quantum Design Physical Properties Measurement System (PPMS) run with Lab View showed the material to be more conductive than pentacene, with a linear I-V dependence similar to graphite. Single crystal X-ray diffraction could not be obtained because of the high reflectivity of the glassy samples. Powder X-ray diffraction revealed a d-spacing of 7.43Å, almost half of the 14-15Å d-spacing of the different pentacene polymorphs [9,10] and twice that of the 3-4 Å d-spacing of graphite and single-walled carbon nanotubes [12].

2.4 Observations of Hydrogen Transfer

2.4.1 Introduction

The appearance of a substantial amount of dihydropentacene and pentacenequinone in the impurity zone after ultrapurification was examined in order to determine its origin as an impurity in the system or a byproduct of the purification process. Other research using the pentacene material for deposition by UHV [2,13,14] and in solution [15] did not report the observation of the formation or appearance of dihydropentacene. Hydrogen transfer has been observed for polyaromatic hydrocarbons resulting in the formation of the tetrahydrogenated or dihydrogenated species along with graphite [16,17]. As stated previously, pentacene sublimations carried out at source temperatures below 320°C did not lead to the observation of dihydropentacene or quinone. Although these remarks provide strong evidence towards a reaction during the

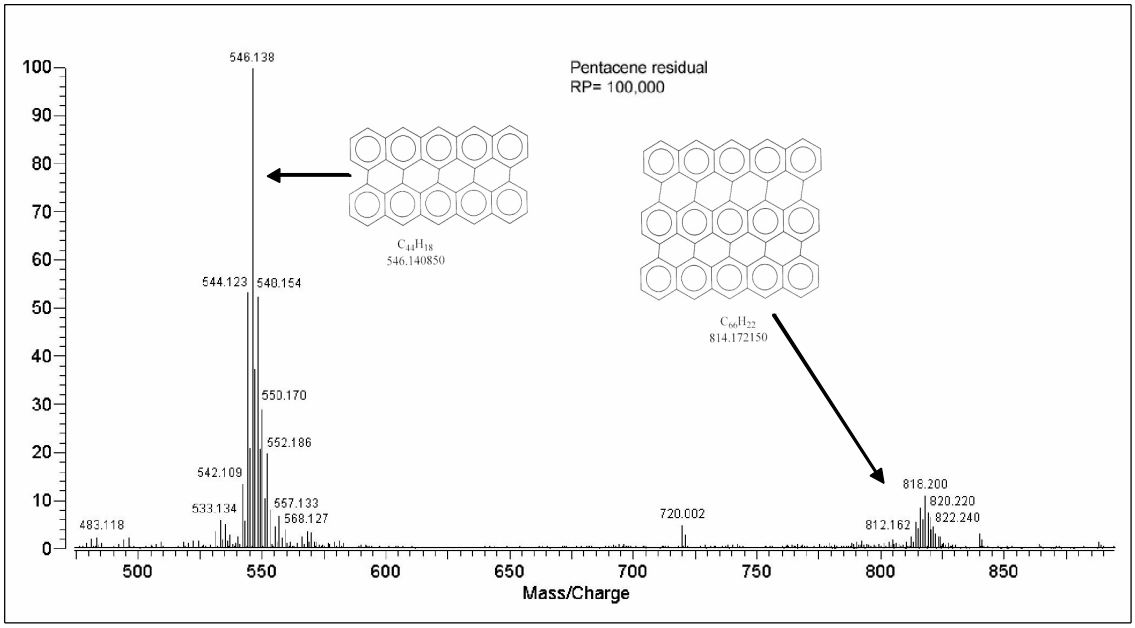


Figure 2.5 Direct 355 nm Laser Desorption FTMS of the pentacene residue.

purification process, it was necessary to carry out a series of tests to validate this hypothesis.

2.4.2 Elemental Analysis and FTIR

A series of elemental analyses were completed to illustrate a direct trend in hydrogen content between sublimation products. The results showed a 5 percent decrease in hydrogen content between the Aldrich pentacene starting material and the black, glassy residue containing BPP (Table 2.1). As expected, the dihydropentacene and co-crystal showed an increase in hydrogen when compared to the starting material. The differences are presumably due to the difficulty associated with separating the overlapping of materials within the impurity zone. The elemental analysis also showed a slight oxygen content within the dihydropentacene formed under the UHP argon atmosphere. This

oxygen was in the form of 6-pentacenone and 6,13-pentacenequinone and was not observed when Mega BIP grade argon was employed. This led us to speculate and later confirm that the carrier gas was the main source of oxygen leading to the oxygenated products.

The infrared spectrum of the pentacene starting material duplicated previous results and did not show aliphatic C:H bond stretching. The presence of the large aliphatic C:H stretch observed in the dihydropentacene and co-crystal spectra demonstrate a trend in the loss of aromaticity from the starting material. The FTIR spectrum of the unpurified residue contained protons that absorb similarly to pentacene and dihydropentacene; however, the residue also contained additional vibrations above 3000 and at 2925 cm^{-1} (Figure 2.6).

2.4.3 Solubility and Absorption Spectra

A 5.6 mg of sample of glassy residue prepared using Mega BIP argon as the carrier gas was ground with a glass rod and dissolved in 2 mL of 1,2,4-trichlorobenzene (TCB), resulting in a black homogenous solution. UV-Vis absorption spectroscopy of this solution revealed an unstructured absorption with significant oscillator strength at 800 nm. However, 4.8 mg of Aldrich pentacene treated similarly at room temperature did not dissolve, but rather remained at the surface of the TCB. Heating the mixture to 60°C resulted in a purple solution. Upon cooling, the solution remained a light purple color with considerable reprecipitation. After 30 minutes, the color disappeared to leave crystals floating on the surface, and after 12 hours the supernatant turned yellow, consistent with the appearance of DHP dissolved in TCB.

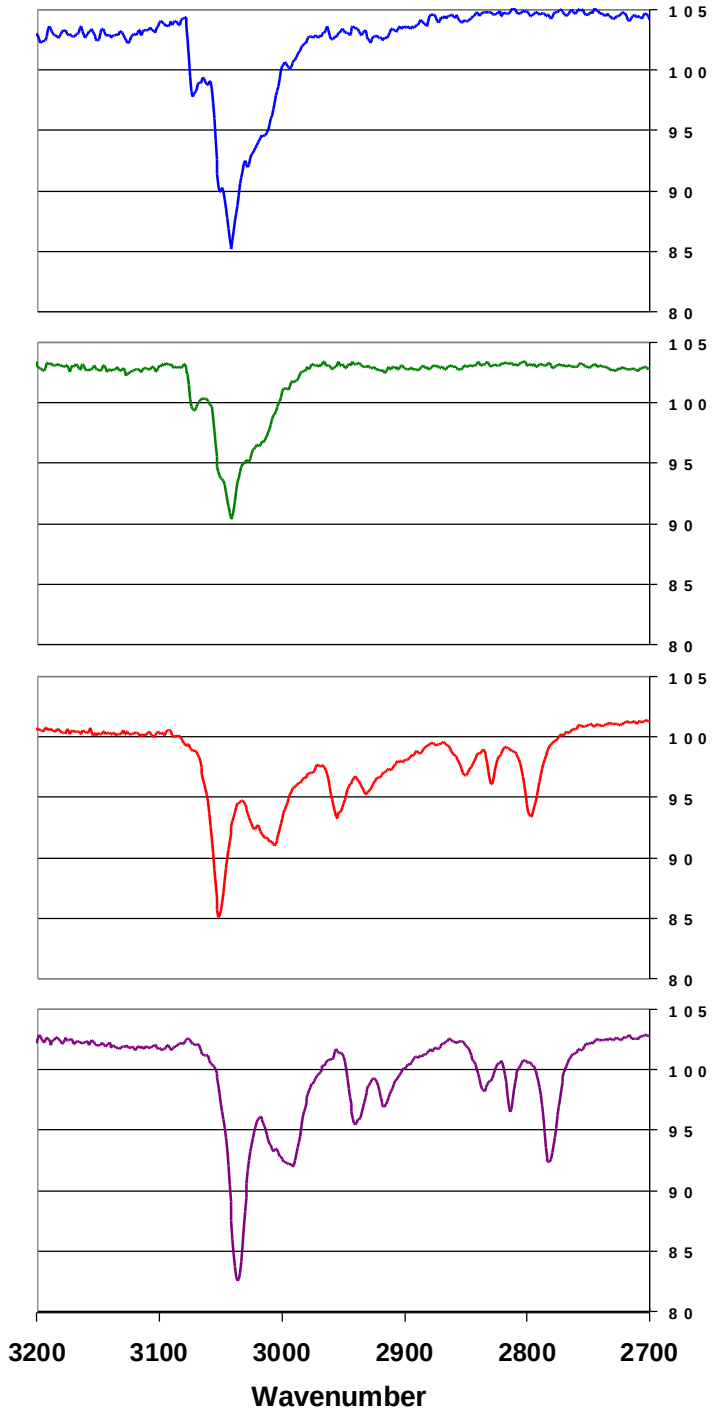


Figure 2.6 Selected region of the FTIR spectra of (A) Aldrich pentacene, (B) purified pentacene, (C) **DHP**, and (D) co-crystal.

UV-Vis absorption spectra were taken of solutions containing the residue, pentacene, and DHP in TCB at room temperature and heated to 60°C (Figure 2.7). As can be seen from the figure, it appeared that the residue contained pentacene, which was verified by EIMS, but may also possibly contain other compounds such as DHP, an unsaturated dimer, or a tetracene subunit [18].

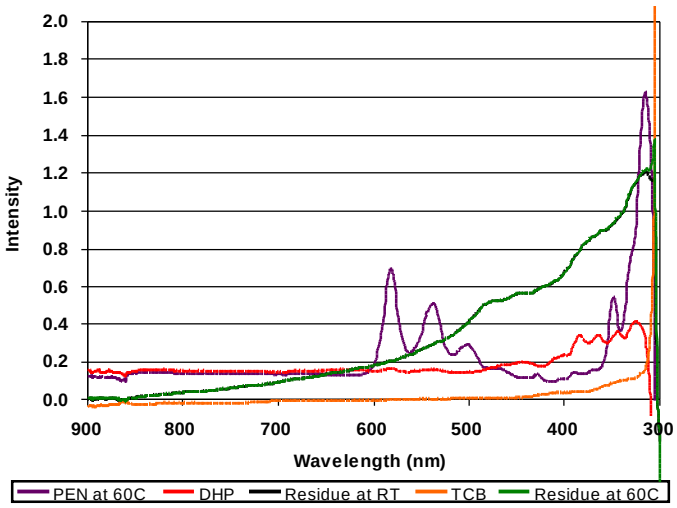


Figure 2.7 UV-vis spectra of pentacene starting material and hydrogen transfer products taken in **TCB**.

2.4.4 High Pressure Liquid Chromatography

High-pressure liquid chromatography (HPLC) was carried out based on the work of Baweja, who separated hydrogen and deuterium analogues of polyaromatic hydrocarbons (PAH) using various mixtures of ACN/H_2O mobile phase and a C18 reverse phase column [19,20]. The experimental conditions can be found in Section 2.2.3. In addition to the HPLC-RID (reactive ion detector), a UV-vis and a particle beam interface Electron ionization mass spectrometer (EIMS) detector were used to accurately identify the separated compounds. The separation of peaks varied as a function of mobile

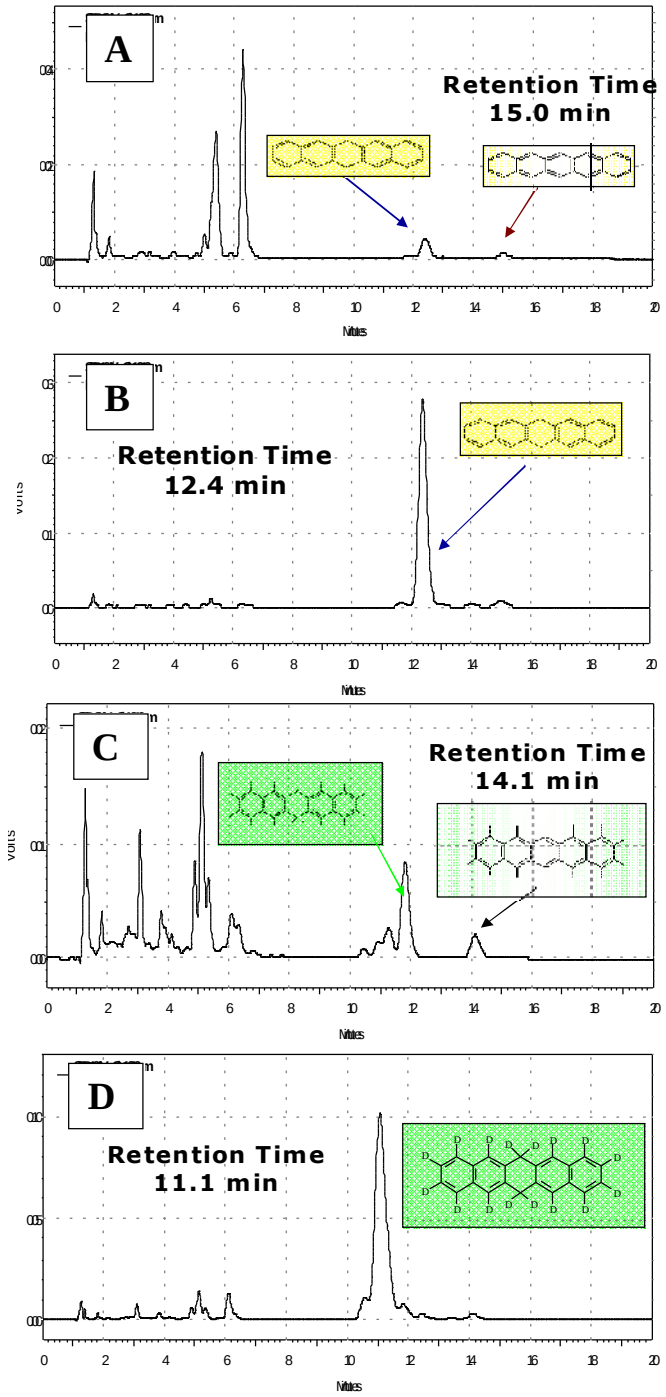


Figure 2.8 HPLC chromatogram traces for (A) Aldrich pentacene, (B) **DHP**, (C) Icon pentacene-$_{d14}$, and (D) **DHP-$_{D16}$** in 75:25 ACN:H_2O mobile phase at a flow rate of 1 mL/min. Traces show dissolved products only; therefore, it should be noted that a large portion of pentacene analogues would not dissolve.

phase concentration and aromatic hydrocarbon; however, the separation of hydrogen and deuterium analogs was typically greater than 1 mL. We were able to reproduce Baweja's results with a small difference in retention times between standard PAHs such as benzene and anthracene. Using this separation technique, we were able to separate and identify hydrogen and deuterium analogues of the pentacene products as shown in Figure 2.8. The solubility of pentacene within this mobile phase was very poor, as can be seen in Figure 2.9A, yet certain impurities were identified via EIMS such as dihydropentacene and pentacenequinone. As expected, the dihydropentacene (12.3 mL) eluted more rapidly than pentacene (15.0 mL). This was the same for the deuterium analogs 6,13-dihydropentacene-d_{16} and pentacene-d_{14} that eluted at 11.0 and 14.3 mL respectively. Similarly to Baweja, we observed that the deuterium analog eluted before the hydrogen analog in both cases.

2.4.5 Mass Spectrometry

The solid-state EIMS at 70 eV of the Aldrich pentacene, dihydropentacene, co-crystal, and purified pentacene samples are shown in Figure 2.10. The Aldrich pentacene and purified pentacene spectra were identical, with M^+ peaks at 278 m/z at column temperatures at 452°C. The dihydropentacene, M^+ peak at 280 m/z, came off at a column temperature at 265°C. The FTMS of the residue was described previously; however, EIMS of the residue in TCB resulted in a spectrum containing an M^+ peak at 556 m/z at a column temperature of 453°C; showing the presence of a single-bonded bipentacene, as well as the observed dihydropentacene and pentacene fractions isolated at their respective column temperatures. Perdeuterated samples were also tested for comparison (Figure

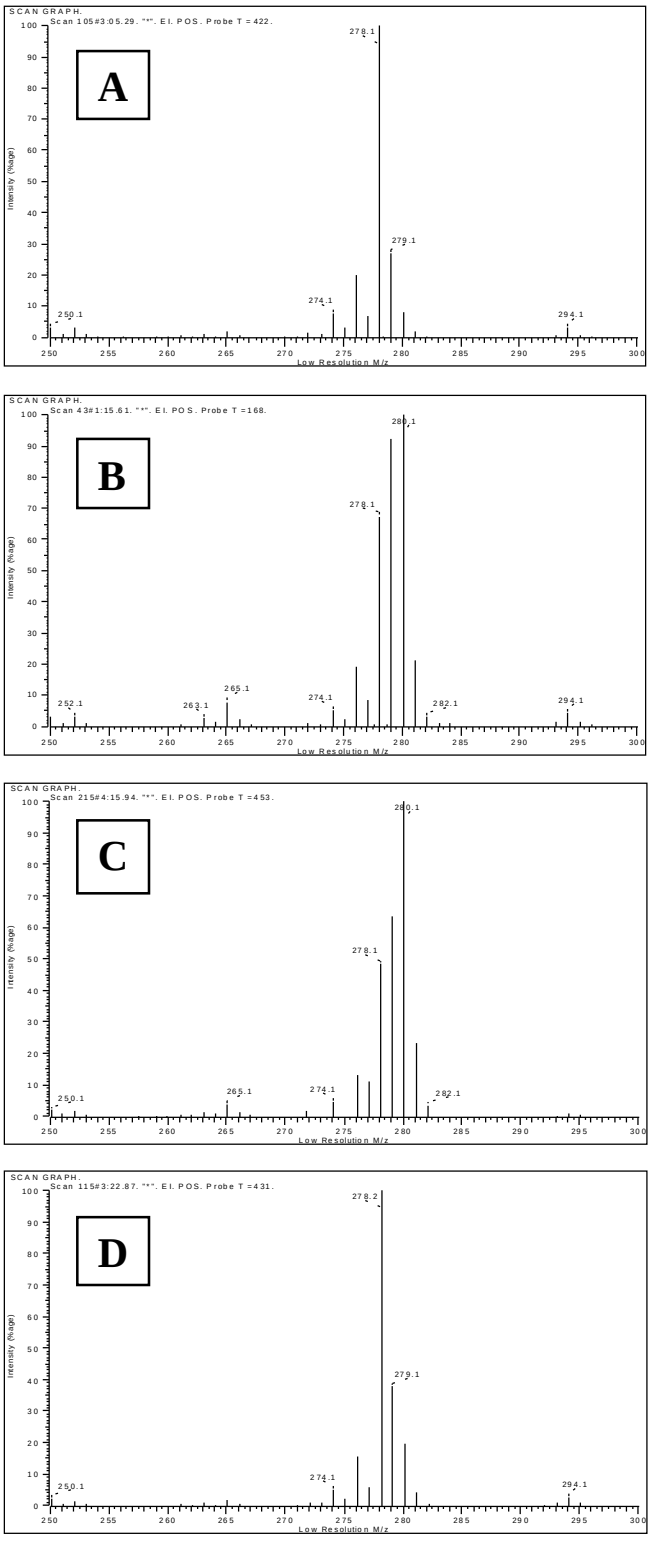


Figure 2.9 Solid-state EIMS of (A) pentacene, (B) 6,13-dihydropentacene, (C) co-crystal, and (D) purified pentacene from 250-300 m/z.

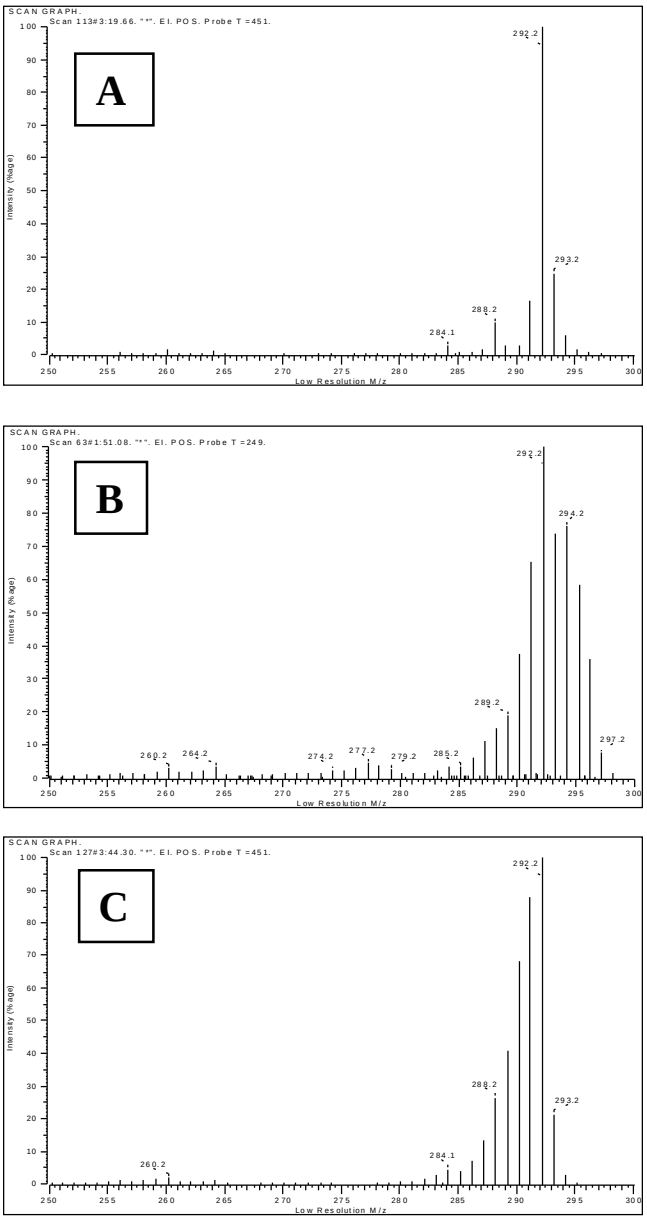


Figure 2.10 Solid-state EIMS of (A) pentacene-d_{14}, (B) 6,13-dihydropentacene-d_{16}, and (C) purified pentacene-d_{14}.

2.11). The observed fractionation patterns between the hydrogenated and deuterated products were nearly identical.

2.4.6 Crossover Experiment

In order to determine the extent of intramolecular hydrogen transfer reactions, 17.9 mg (6.44×10^{-5} mol) of Aldrich pentacene was mixed with 12.5 mg (4.28×10^{-5} mol) of pentacene-d_{14} (ICON) and heated in the HPVD chamber at a source temperature of 380°C for 4 hours. The mixed reaction products were isolated and collected. EIMS of the mixed dihydropentacene (Figure 2.12A) and mixed pentacene (Figure 2.12B) samples were analyzed. Upon comparison with the purely hydrogenated and deuterated 6,13-dihydropentacenes and pentacenes described in Section 2.4.5, there was a very good mixed distribution of hydrogen and deuterium products within the mixed samples. Overlap of the original respective hydrogenated and deuterated EIMS spectra would not have resulted in the spectrum obtained for the mixed samples. HPLC of the mixed dihydropentacene (Figure 2.13A) was run against the dihydropentacene and dihydropentacene-d_{16} compounds. The result was a broad chromatogram with four local maxima between the dihydropentacene maximum at 13.5 minutes and the dihydropentacene-d_{16} maximum at 12.5 minutes. The local maxima are attributed to the mixed and original samples. These results demonstrated a proficient transfer of hydrogen and deuterium between the two species.

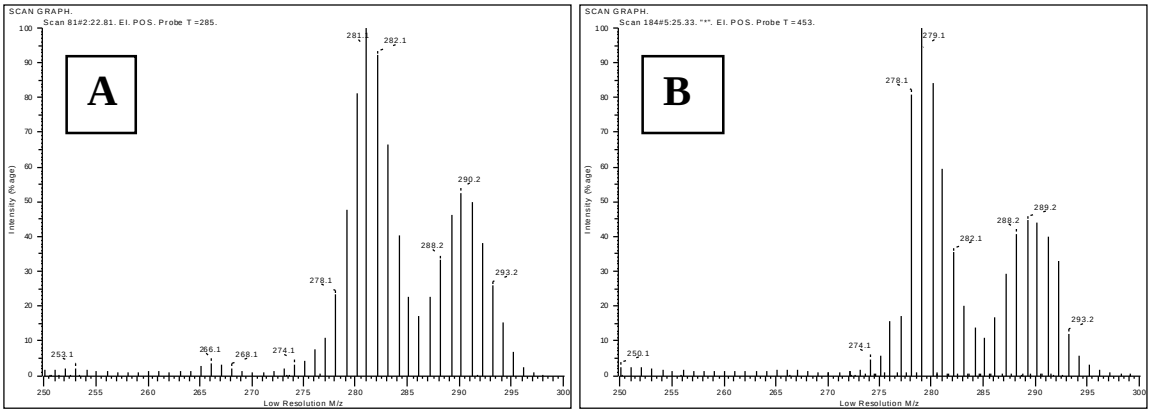


Figure 2.11 Solid-state EIMS of (A) mixed H/D 6,13-dihydropentacenes (B) mixed H/D pentacenes.

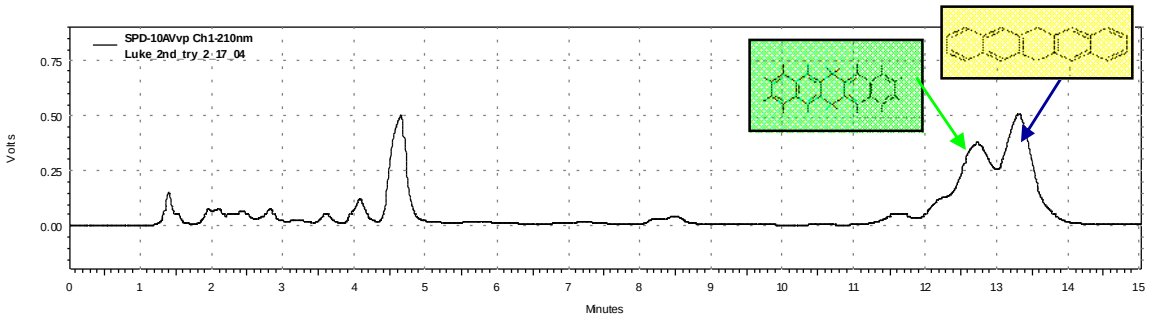
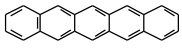
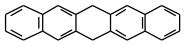
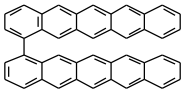
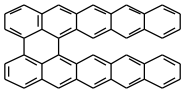
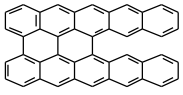
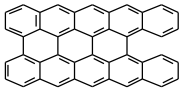


Figure 2.12 HPLC chromatogram traces for mixed 6,13-dihydropentacenes in a 70:30 ACN:H_2O mobile phase at a flow rate of 1 mL/min.

2.4.7 Theoretical Calculations

Ab initio (3-21G*) and semiempirical (AM1) calculations for the hydrogenation of pentacene to dihydropentacene and from pentacene to BPP were performed to rationalize the observed hydrogen transfer (Table 2.2). These results showed the heat of hydrogenation of pentacene to be 36.1 kcal/mole, while the heat of dehydrogenation of pentacene to 1,1'-bipentacene is 7.3 kcal/mol, providing an overall enthalpy for the reaction of -28.8 kcal/mol. In that regard, it is interesting to consider the individual steps of the "zipper" reaction which converts 1,1'-bipentacene into peribipentacene. Of course, the actual mechanism may involve a number of different intermediates with differing

Table 2.2 *Ab initio* and AM1 heats of formation and reaction for the proposed "zipper-effect" for the formation of bisperipentacene and 6,13-dihydropentacene from pentacene.

Hydrocarbon	Structure	ΔH_f (a.u.)	ΔH_r (kcal/mol)	ΔH_f (kcal/mol)	ΔH_r (kcal/mol)
		ab initio		AM1	
Pentacene		-836.57		111.85	
Dihydropentacene		-837.77		75.75	-36.1
Bipentacenyl		-1671.98	-25.1	230.99	-28.8
Didehydrobipentacene		-1670.8	-37.65	246.74	-49.14
Trisdehydrobipentacene		-1669.68	-87.85	243.27	-88.7
Tetradehydrobipentacene		-1668.54	-124.25	243.33	-124.74
Peribipentacene		-1667.42	-175.7	231.23	-172.93

fusion points, although initial reaction at C-6 represents a plausible starting point (Figure 2.14). We would also expect at these temperatures that considerable redistribution among various connectivities would obtain to lead to intermediates allowing for final ring fusion. Nevertheless, assuming a symmetrical order of bond formation, we see that each successive bond after the second delivers a greater enthalpy. This observation may represent a general mechanism for graphitization reactions, since there is apparently a kinetic driving force for planarization once the aryl-aryl bonds begin to form.

2.4.8 Proposed Mechanism

Studies of the thermal reactivity of polyaromatic hydrocarbons (PAH) have been reported since the 1960s, for which the carbonization of PAH via hydrogen transfer is monitored by differential thermal analysis [16]. Additionally, high mechanical pressures have been shown to produce graphitic species and dihydrogenated and tetrahydrogenated byproducts from polyacenes via hydrogen transfer [17]. The mechanism of the hydrogen transfer reaction itself is still unclear. Polyacenes are well known to undergo radical reactions, and the possibility of a catalytic reaction involving the formation of radicals was considered. The source of a radical initiator was explored to determine the initiation step of the mechanism. Flame AAS was used to see if Fe or Al was present in the Aldrich or ICON starting materials. Iron is known to be a catalyst for radical reactions [21,22]; whereas Al is commonly used as a catalyst in the synthesis of pentacene from pentacenequinone [23]. AAS results showed a small concentration of both Fe (114 ppm, 719 ppm) and Al (593 ppm, 1.76%) in the Aldrich and sublimed residue samples respectively. As expected, the concentration of the metals in the residue was greater than

that in the Aldrich material, since the metals do not sublime. Ruchardt's hydrogen transfer experiments using 9,10-dihydroanthracene as the radical initiator have led us to believe that small concentrations of dihydropentacene are acting similarly in our experiments [24,25]. We note that HLPC trace chromatograms showed the presence of small amounts of dihydropentacene in pentacene, and it is possible that this is an autocatalytic reaction, with dihydropentacene acting as the radical initiator with the loss of hydrogen at the 6 position at temperatures exceeding 320°C (Figure 2.13). This mechanism is consistent with Rüchardt's observations on the hydrogen transfer reduction of styrene [26,27]. We note that the crossover experiments, indicating scrambling of hydrogen and deuterium in the DHP products, are permissive of such a mechanism but not exclusive to it. Moreover, the temperature of the transformation is similar to that required under Rüchardt's conditions using dihydroanthracene as the hydrogen donor. Although we see no evidence for this process, it has been suggested to us that the butterfly photodimer [28] present in some preparations of pentacene could also lead to pentacenyl radicals through bond scission at high temperature, which would obviate the formation of slip isomers of the pentacene dimers and trimers. Conversely, formation of peripentacene and its higher homologues may occur via isomerization of such intermediate slip isomers of bipentacenes formed under these conditions.

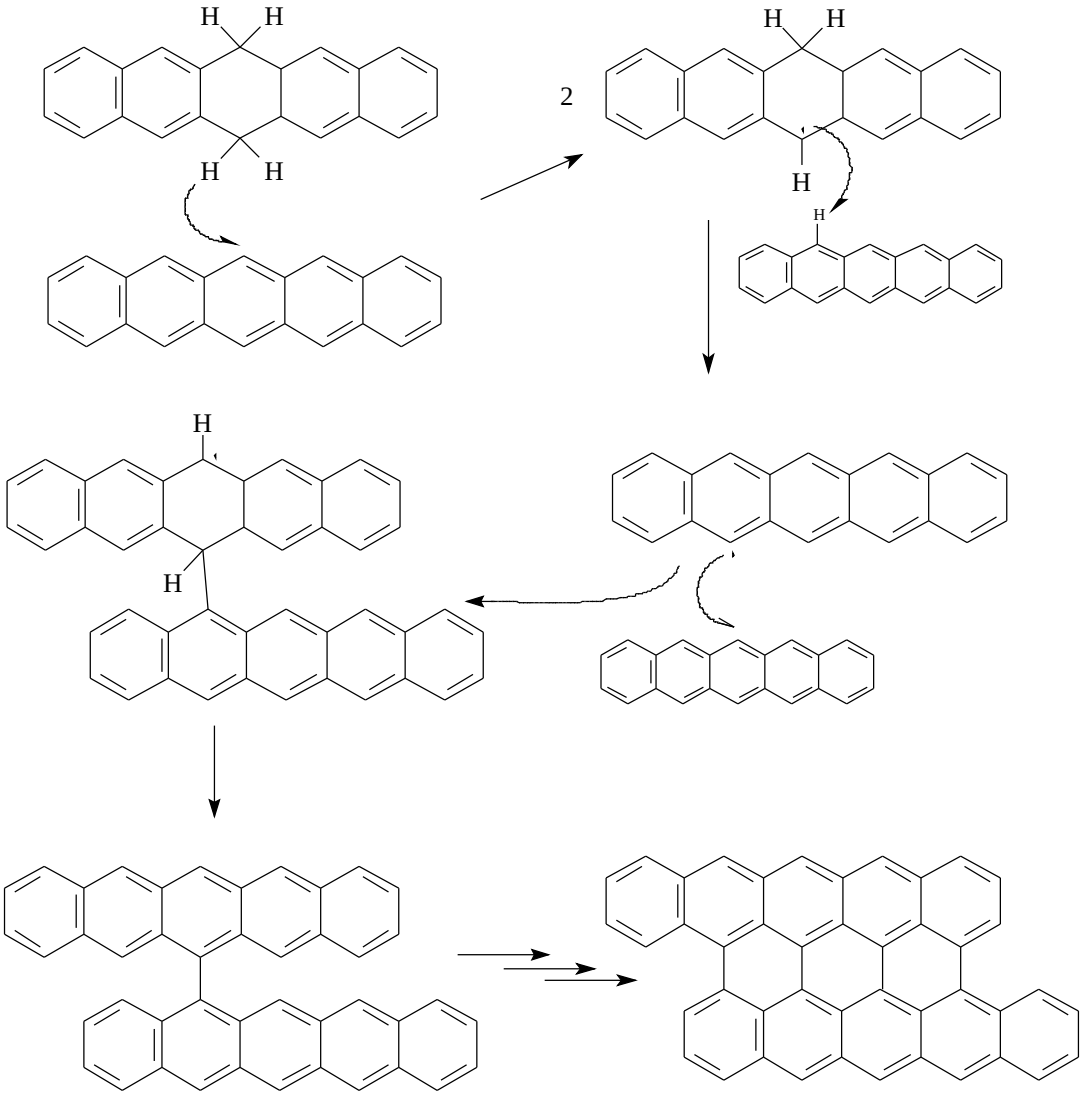


Figure 2.13 Proposed reaction mechanism for the hydrogen transfer of pentacene during sublimation at 1 atmosphere pressure.

2.5 Ultrapure Single Crystal OFETs

Taking into account the above described formation of pentacenequinones, dihydropentacene and peripentacenes during the purification of pentacene at elevated temperatures, the following procedure was used for preparation of ultrapure single crystals. First, commercial pentacene was sublimed in a 30 ml/min flow of argon at 200–320^{o}C temperature gradient. The pentacene crystals were accompanied by black residue

in evaporation source and a violet-blue deposit in low temperature. Pentacene crystals separated from residues were used for subsequent crystal growth in a sealed ampoule. The absence of inert gas provided for sublimation at a slightly lower temperature thereby producing thicker crystals.

Having achieved high-purity pentacene, we were able to build transistors on these crystals and perform mobility measurements. All transistors constructed and measured in this manner were built at Lucent Technologies at Murray Hills, NJ under the direction of Dr. Christian Kloc. Single-crystal field-effect transistors were constructed on by RF sputtering of aluminum oxide onto the crystal, followed by evaporation of gold source, drain, and gate electrodes through a shadow mask in a RF metal evaporator at 10^{-6} torr. Hole mobilites up to 2.2 cm^2/Vs were measured using an HP4155A semiconductor parameter analyzer at Lucent Technologies. The transistor I_D vs. V_D and I_D vs. V_G curves are shown in Figure 2.14. This high value was possible to achieve because the two-step crystal growth and purification process was applied. OFETs have been prepared using low temperature electrodes and dielectric deposition processes, which limited defect formation in the FET channel and in source gate electrodes areas.

2.6 Conclusions

The preparation and purification of organic materials for electronic devices continues to be a challenge to the field of organic electronics [29]. Even well-characterized materials such as pentacene are capable of significant impurity-forming reactions at relatively low temperatures. Such results serve as a caution to overinterpretation of results based upon materials that may have defects at extremely low

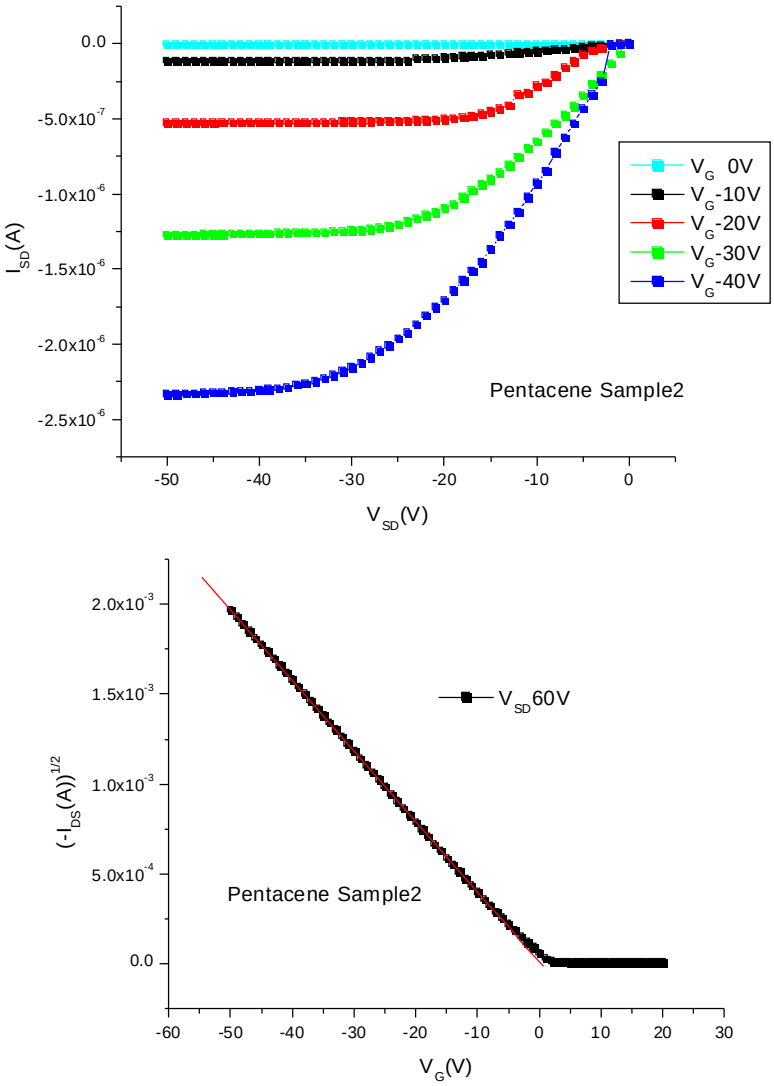


Figure 2.14 I-V curves for pentacene single crystal field-effect transistors a) source-drain current vs. source-drain voltage for various gate voltages, b) source-drain current vs. gate voltage for the saturation region at V_{SD} = -60 V leading to a calculated hole mobility of 2.2 cm^2/Vs.

concentrations, which nevertheless impact device performance. Fortunately, it is possible to limit the concentration of impurities and defects and produce single-crystal field-effect transistors with relatively high hole mobility. Such careful analysis and purification, when applied to thin film transistors, can improve pentacene thin film field-effect transistors and can be widely applicable into industry scale organic microelectronic devices.

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CHAPTER 3:

FROM COMMON TO INDIVIDUAL GATE MOS OFETS: A PLATFORM FOR HIGH-THROUGHPUT ORGANIC SEMICONDUCTOR MOBILITY SCREENING

3.1 Introduction

As explained in Chapter 1, the silicon transistor will remain as the workhorse for data switching devices requiring high throughput data transfer for the next 20 to 30 years. Moore's Law defines the productivity of these devices based on the number of devices required to double processor speed over time [1]. However, this theory takes into account only silicon processing and does not extend beyond 30 years from now. Smaller transistor sizes increase performance by diminishing switching times; however, there is a fundamental size limit to the transistor where short channel effects disrupt output performance. As the number of devices per wafer increases to supply an increase in desired performance, many new problems have appeared that limit the overall productivity such as increased power consumption, increased heat generation, and decreased output yield of working devices. These factors exponentially increase the cost of production which is then passed to the consumer as higher prices. This has led to the need for low cost, disposable devices with similar output performance to that of amorphous silicon. The exploration of polymer thin films to solve this dilemma was an obvious choice as most polymers are solution processable, readily available, inexpensive, generate little to no heat, and consume less power.

Our work in this field followed that of many published reports from research groups across the world [2]. All of these publications varied from device structure to

semiconducting polymer material used to deposition method; however, the one reoccurring theme to these devices was that they all implement a common gate approach, whereby the substrate, typically a heavily doped silicon wafer, was used as the gate electrode. This method of device manufacture provided a good way for testing material mobility based on the geometry of the source-drain electrodes deposited, because the method employed a generic five to seven-step manufacture process in either a top contact or bottom contact device structure. The main advantage to this approach was that a pristine gate dielectric material, silicon dioxide, was thermally grown from the single crystal substrate. The pristine dielectric enabled the devices to be taken to higher voltages, thereby resulting in higher source-drain currents and larger on-off ratios. The glaring problem with this method was that each different semiconducting polymer material was tested on a different silicon wafer (gate electrode) and that these wafers could have varied in resistance based on doping concentration, crystal structure, and surface roughness; therefore, reproducibility and direct semiconductor comparisons may have been compromised. Another disadvantage was that the wafer must be diced before testing. Dicing was required because the substrate acting as the gate turns on all devices simultaneously, causing device to device leakage. It is also known that device structure greatly influenced the performance of the transistor [3]. Thus when a common gate approach was used to test material performance it must be recognized that their performance was based on a methodology whereby all devices were turned on simultaneously. This tactic can not be utilized for high throughput material testing or in commercial applications or for flexible substrates; therefore, we developed a new method for testing the electronic properties of the polymer semiconductor that addressed these

concerns by implementing an individual gate OFET design. This design allowed for subsequent multiple semiconductor material testing on the same substrate with the consequence of some additional processing steps.

In this Chapter we discuss the design of our individual gate OFETs, how the same design was implemented into a common gate device, and how the design can be transferred seamlessly to a flexible substrate for future research. We will compare the device performance based on the different architectures with a few different polymers, both reported in literature and newly developed, doped and undoped. It is noteworthy to mention that all work described within this chapter was performed within the cleanroom of the Microelectronics Research Center (MIRC) at the Georgia Institute of Technology, and that funding of this work was provided by the Intel Foundation Fellowship and by a grant from the Department of Energy.

3.2 The MOSFET

The organic transistor was developed on the basis of the silicon transistor, as briefly explained in Chapter 1. The name metal-oxide-silicon field-effect transistor (MOSFET) arises from the architecture of the device itself, whereby silicon dioxide is thermally grown or chemically deposited on a doped silicon wafer surface and used as the "skeleton" for field-effect transistors. The thermal growth of the gate oxide from the surface of the wafer provides a direct continuation of the underlying silicon crystal structure, preventing the formation of defects, including crystal mismatches, incorporation of impurities, and creation of current trap sites. Formation of these defects and traps leads to a decrease in source-drain current as well as gate oxide breakdown at

higher gate voltages. Chemically vapor deposited (CVD) oxides are commonly used as gate dielectrics; however, their lower density results in higher resistance, pinholes, and increased traps; therefore, it is common to see leakage currents and oxide breakdowns at higher gate voltages. Additionally, CVD oxides can be brittle if they are too thick, therefore their use in flexible substrates should be minimized to prevent cracking when flexed.

MOSFET device architectures are either n-type or p-type. The combination of n-type and p-type devices arranged on the same wafer is referred to as a complimentary metal-oxide-semiconductor (CMOS). The manufacturing process for silicon CMOS devices is very complex, requiring over 50 processing steps using 13 different photolithography masks. Because the focus of this work does not involve a direct manufacture of either silicon or organic CMOS devices, the procedure will not be explained here. However, a reference for this procedure can be found at the CMOS group webpage [4]. What is of importance is the ability to effectively transfer the fundamentals of this technology into the field of p-type organic electronics. Although the ability to have both p-type and n-type devices on the same chip is a great advantage to minimize cross-talk between silicon devices on a very small scale, it is not yet of significance to the field of organic electronics. Therefore, we did not attempt to design CMOS architectures, but rather use CMOS protocols to design high quality p-type MOSFET using an organic semiconductor.

3.3 From Silicon to Organics

This transfer of CMOS technology and silicon theory has been the topic of debate for several years now as the basis for silicon technology was conveniently applied to the world of organic chemistry. As mentioned in Chapter 1, the standard for determining the electron or hole mobility within a conductive organic or polymer material has been accepted in the literature. However, it is worth mentioning that the methodology for determining the charge mobility in a material under an applied electrical field is strictly based on that of silicon, and that the charge mobility in silicon in an applied electrical field is independent of that applied field (field modulation). This may or may not be the case for organic materials. We will attempt to address this concern and add to those ongoing debates.

In the current literature, one can find numerous accounts of the mobility of organic semiconductors in different device configurations, with different surface modifiers, deposited by different methods [2]. For silicon MOSFETs, the transistor was built directly into the doped silicon acting as the semiconductor, source and drain electrodes. As shown in Chapter 2, we were successful in building transistors on the surface of single crystals of organic semiconductors. Nevertheless, not all organic and polymer materials have crystal structures; therefore, it was necessary to develop alternative methods for measuring semiconductor mobility within thin films. To do this, researchers inverted the silicon MOSFET devices, where the silicon wafer now acted as both the gate electrode and the substrate for which the remaining transistor was built [5]. Schematics of these common gate top and bottom contact devices are shown in Figures 1.1 and 1.2. The inversion was crucial for the theory of the field, as the heavily doped

silicon substrate functioned concomitantly as the substrate and gate electrode, thus permitting thermal growth of pristine oxide from its surface. This enabled the device to mimic CMOS device architecture and follow similar transistor behavior and equations.

3.4 Mask Making

Before diving into the manufacture process for the OFETS, it is important that the tools necessary for successful replication of these experiments be explained. One of the key tools for IC fabrication is the mask, essential for creating patterned features on a substrate surface. The most important and common mask type is the photolithography mask, whereby a glass substrate with a generated pattern made of nontransparent metal (chrome) is placed between the light source and a photo-active polymer layer. Upon exposure to light, the photoresist chemically changes. When developed the exposed (negative resist) or unexposed (positive resist) areas of the resist generate the desired pattern. A series of four 5" photolithography masks, labeled OFET 1-4, were drawn in CADence® and converted to autoCAD®. The drawings (see data supplement) were submitted to the mask department at the MIRC and were constructed by them in 1-2 weeks. The masks were specifically designed to work in the Karl Suss MA6 mask aligner.

A shadow mask is a physical mask for metal evaporation through patterned holes. Shadow masks are more difficult to make compared to the photolithography masks, yet they can be purchased for $600-2000 from a few US manufacturers. To make a shadow mask it was first necessary to generate a new pattern using CADence/AutoCAD and have a photolithography mask made. The photolithography mask was a 4-inch mask; however,

if I had to repeat this experiment again, the mask needed to have been 5 inches to accommodate more devices on a 4-inch wafer. The manufacturing process was as follows: silicon <100> test grade wafers were cleaned in a piranha bath at 120°C. Shipley 1813 photoresist was spun at 5000 rpm for 30 sec using a spin coater, followed by a 75 second softbake at 115°C. Exposure using the photomask in the MA6 mask aligner at CI2 wavelength (435 nm, intensity of 15 mW/cm^2, dosage: 45 mWs/cm^2) for 3.1 seconds was sufficient to expose the photoresist. Development using MF319 for 45 seconds in the Solitec developer removed the exposed area. To etch trough the wafer, two wafers were sandwiched together using Shipley 1813. The wafer sandwich was placed into the STS ICP for approximately 15 minutes at 300 W. The 70:1 selectivity of the CH_4 plasma for silicon versus the photoresist proved to be enough to etch through the wafer with 2 depositions with photoresist. Early trials at higher power (600 W) ended up etching the entire top wafer away. Attempts were made to deposit CVD oxide and pattern using the photomask and a BOE etch; however, the extra layer and improved selectivity (100:1) were not necessary to achieve the desired shadow mask.

3.5 Common Gate OFETs

3.5.1 Experimental

The manufacturing process for each individual batch run of common gate OFETs is outlined within Appendix 3.5, 3.6, 3.12-15. As mentioned, the literature demonstrates different methods for developing and making common gate OFETs; therefore, we repeated two of the most common experimental procedures, the lithographically

patterned source/drain electrodes using our generated mask set and the shadow masked source/drain electrodes.

3.5.1.1. Liftoff Common Gate OFETS

Heavily Sb-doped silicon <111> wafers were purchased from WaferNet, Inc. with a resistivity between 0.01-0.02 ohms/cm and a thickness between 470-500 μm. Typically, silicon wafers have a polymer backing to increase their durability. An etched back was necessary because the substrate acted as the gate electrode and would be in contact with the probe station. Polymer-backed wafers would prevent the backside of the wafer from being used as the gate electrode. For the wafer to have an etched back and be durable enough for processing, <111> orientations were preferred. In the future, resistivity levels should be between 0.1-0.2 for a proper surface charge analyzer (SCA) test, since the current was too high at 0.01 ohm/cm resistivity for the SCA test and silicon mobility was not necessary for device performance.

Silicon substrates were cleaned in a piranha bath of 4:1 sulfuric acid and hydrogen peroxide at 120°C to remove any residual organic materials. A RCA clean (4:1:1 H_2O:HCl:H_2O_2 at 70°C) was performed to remove metal contamination from the surface of the wafer. Following the RCA clean, the wafers were dipped into a buffered oxide etch (BOE, 6:1 HF in NH_4F) bath for 30 seconds to remove oxide growth from the reaction. After a thorough cleaning process, the wafers are rinsed with deionized water and dried using a SemiTool Spin-Rinse-Dryer (SRD). The wafers were then placed into nitride furnace 3 where silane (SH_4) and oxygen are pumped in at 950°C to thermally grow oxide over the entire wafer in a dry growth process. Growth rates of the oxide

dielectric were taken and it was found that 4 hours and 40 minutes of growth led to 200 nm of oxide on the surface of the wafer, following the calculations provided at http://www.lelandstanfordjunior.com. The disadvantage of dry growth versus a wet growth, where water was used to thermally grow oxide at twice the growth rate, was that wet growth would lead to chlorine contamination within the oxide layer. The effects from contamination are described in detail within Section 3.5.2. The oxide quality was then determined using SCA by measuring the amount of charging and the lifetimes of charge accumulation on the oxide surface. Areas of the oxide surface were then photolithographically patterned by spinning Shipley 1813 photoresist at 5000 rpm for 30 seconds at an acceleration of 2500 rps. This was followed by a soft bake at 115°C for 75 seconds. The oxide on the backside of the wafer was etched, either as a wet etch in BOE or as a dry etch in a CF_4 plasma. Wet etching was easier and produced similar results to dry etching. To make patterned source and drain electrodes, a liftoff method was employed. Shipley 1813 was spun onto the oxide using the same procedure. Exposure was done using OFET mask 3 in the Karl Suss MA6 mask aligner in hard contact mode for 8 seconds at CI2 (435 nm wavelength with an approximate 16.5 mW/cm^2 intensity level). The photoresist was developed in a Solitec developer for 45-60 seconds using MF319 and rinsed with deionized water and spin dried. Deposition of the metals, 5 nm titanium and 200 nm gold, were performed on a CVC E-beam evaporator at 10^{-6} torr with deposition rates at 1.5 Å/s. The titanium was necessary to produce an ohmic contact between the dielectric layer and the gold electrodes as well as act as an adhesion layer. Liftoff of the metal and remaining photoresist was carried out by placing the wafers into a glass bowl containing acetone and left for an extended period of time, typically

overnight. The unexposed areas then lifted off of the oxide surface leaving the exposed areas now containing metal. The semiconducting organic material was deposited onto the wafer either by spin coating, drop casting, or evaporation. Depending on the semiconductor, the wafer was annealed on a hotplate above the polymer glass transition temperature. At this point, the devices could have been tested. However, to individualize the devices, Shipley 1813 was spun onto the organic surface. Lithography was performed using OFET mask 4 in the MA6, exposed for 3.1 seconds at CI2, and developed with MF-319 for 45-60 seconds depending on intensity. Etching of the organic material was done in an appropriate solvent that would dissolve the semiconductor without effecting the photoresist, while etch times were short to minimize undercutting of the photoresist. The solvent of choice was a derivative of chlorobenzene because it would not strip the protective photoresist.

Device testing was performed using Professor Bernard Kippelen's (Georgia Institute of Technology, School of Electrical Engineering) custom made LabView program and an Agilent Technologies E5272A source/monitor unit connected to a Signatone H100 series probe station contained within a Siemens LabMaster 130 glovebox with a nitrogen atmosphere. While measuring source-drain currents, the program allowed for altering variables, such as applied drain and gate voltages as well as the magnitude of the voltage steps. Transfer curves, I_D-V_G and $\sqrt{I_D}$-V_G, were taken in the same manner using a different LabView program.

3.5.1.2. Shadowmask Common Gate OFETS

The process for making a shadow mask followed that of the e-beam deposited metal; however, rather than using lithography and lift-off methods to pattern the gold source-drain electrodes, here a physical mask was employed to create features on the wafer surface. The advantage of a physical mask was that the lithography, patterning, and etching steps were removed, which reduced the possibility for contamination by solvents and photoresists. The disadvantage to the shadow mask was that distinct feature profiles were compromised, such that the walls of the electrodes were no longer vertical but angled and the channel length has a higher percent deviation. Therefore, shadow mask devices were typically larger than the photolithography devices so that the percent deviation was not of a concern.

3.5.2. Common Gate Results

Common gate device manufacture with pristine oxide layers was successfully accomplished using liftoff procedures with photolithography masks; however, due to contamination issues, the few attempts to make shadowmask devices reproducibly failed. Metal and water contamination within the gate oxide layer was a big problem. The SCA data shown in Figure 3.1 was for wafer batch 15, a common gate liftoff batch. The native charge level of the oxide, Q_{ox_inv}, was comparatively low for oxide growth, and the charge lifetime generated on the oxide, Ts, was long, approximately 140 seconds. However, you can see in the SCA of batch 12 (Figure 3.2), which had the same procedure of batch 14, Q_{ox_inv} levels were twice as high and lifetimes were less than half. The oxide layer was contaminated with water produced from a previous wetox.003 recipe where the

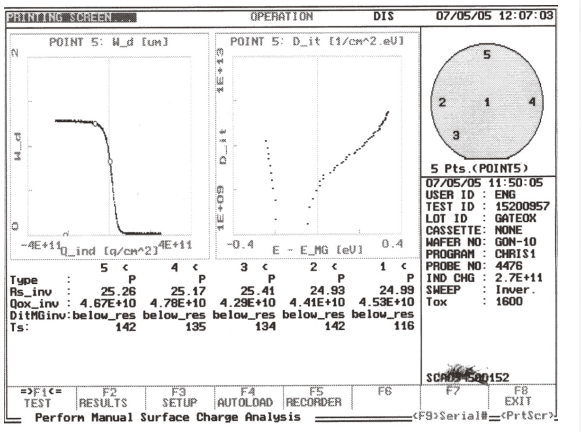

Figure 3.1 SCA data for batch 15.

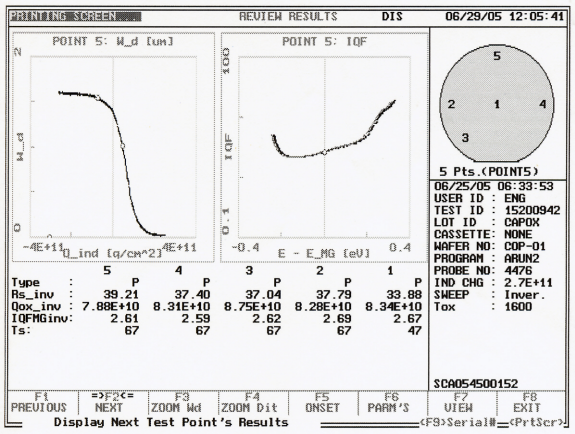

Figure 3.2 SCA data for batch 12.

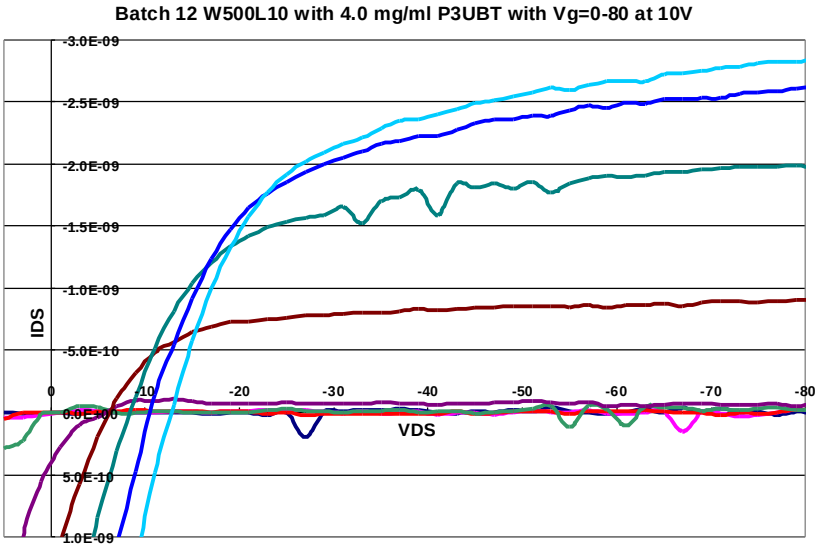

Figure 3.3 IV Curve for batch 12 W500L10 device with 4.0 mg/ml P3UBT.

user had failed to clean the tube following oxide growth. The contamination can be seen in the IV curve traces of batch 12, where they displayed a large amount of leakage current, as shown in Figure 3.3 for patterned 40 nm P3UBT. The large leakage currents were contributed to the high charge levels on the oxide acting as traps by absorbing the induced charges, now with shorter lifetimes, from the source electrode.

Once the contamination issue was addressed, IV curve traces from batch 14 and 15 with different materials were tested. To ensure the accuracy of our results, our common gate devices were run against Kippelen's common gate diced devices. Kipplean's devices have been reported in literature for various materials including pentacene [6]. For the comparison, we first used P3UBT without adhesion promoters, as seen in the batch 15 IV curves (Figure 3.4). When compared to Kippelan's results shown in Figure 3.5, both current maximums are in the nanoampere range, mobilitites are 10^{-5}, and V_{th} were between -10 and -20 V at -40 V drain voltages. These tests helped to verify that a material can be reproducibly examined on different platforms and obtain similar device characteristics.

We then tested the widely reported pentacene OFET by thermally evaporating 40 nm of purified pentacene onto batch 14 without the use of surface promoters. The process was conducted so that measurements were taken prior to lithography, after lithography, and then after etching. The purpose was to examine the effect of lithography and etching on the pentacene's hole mobility and compare all three results to literature common gates and individual gates explained in the next section. The IV curve trace shown in Figure 3.6 was for pentacene prior to lithography. As seen in the trace, there was a substantial amount of leakage current and contact resistance. This was expected because devices

were now interconnected by means of the polymer layer, and that the gate electrode, the silicon substrate, was inducing an electric field over the entire 2100 devices allowing for charge migration in any direction even though holes were biased by the applied drain voltage. Hole mobilities obtained in the saturation region were 0.01 cm^2/Vs at V_D = -20 V as determined by the transfer curves in Figure 3.7. The on/off ratio was $3x10^2$; however, increasing the gate and drain voltage maxima, the on/off ratio increased to 10^4. Patterning the pentacene with Shipley 1813 led to similar IV curves with contact resistance and leakage current shown in Figure 3.8. Mobility of the pentacene in the saturation region dropped by an order of magnitude to 0.002 cm^2/Vs at V_D = -20 V as did the on/off ratio to 20. It was believed that solvent incorporation led to the decrease in current, and that vacuum baking after etch would remove solvent and increase mobility. However, this wasn't the case. After etching the pentacene in low wattage oxygen plasma for 90 seconds, testing revealed little change between the devices, as shown in Figure 3.9. The reduced mobility induced after the incorporation of photoresist was a concern that needs to be addressed in future work.

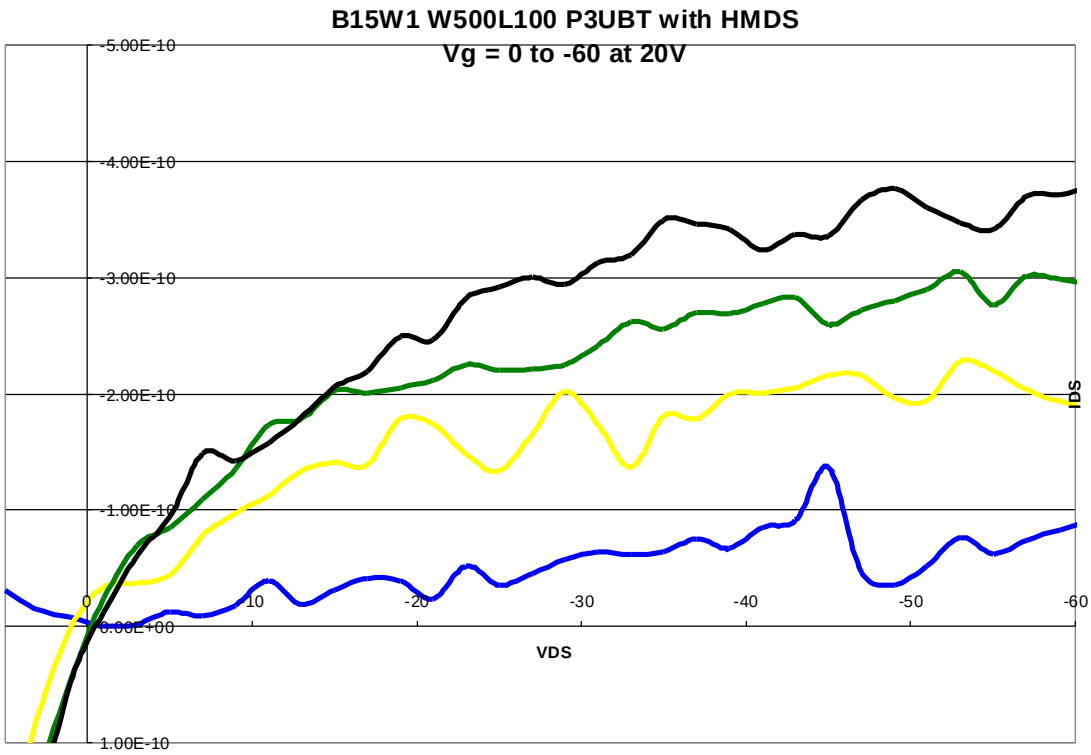

Figure 3.4 IV Curve for batch 15 W500L100 device with 4.0 mg/ml P3UBT and HMDS.

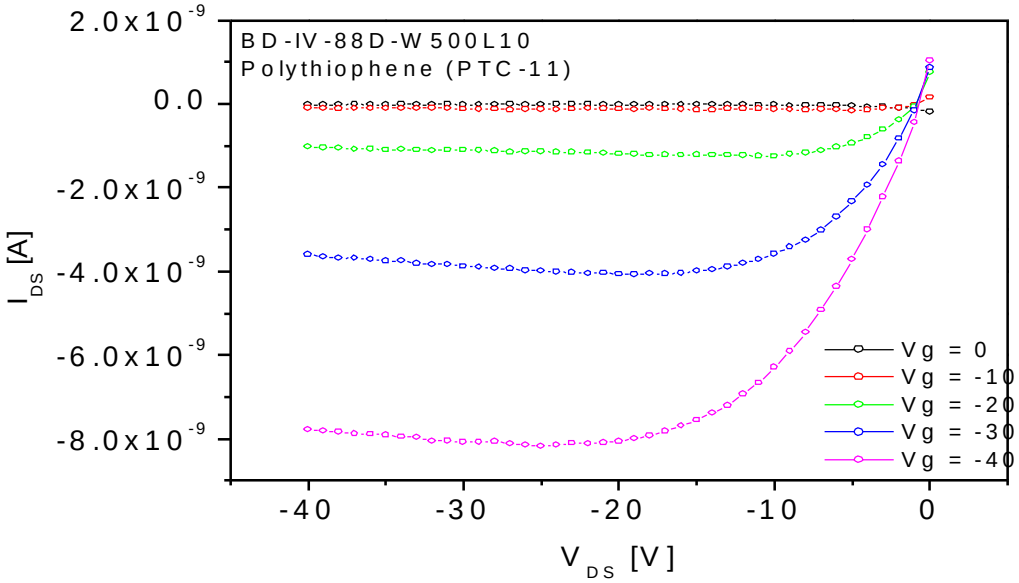

Figure 3.5 Kippelen's IV Curve for W500L10 device with 4.0 mg/ml P3UBT.

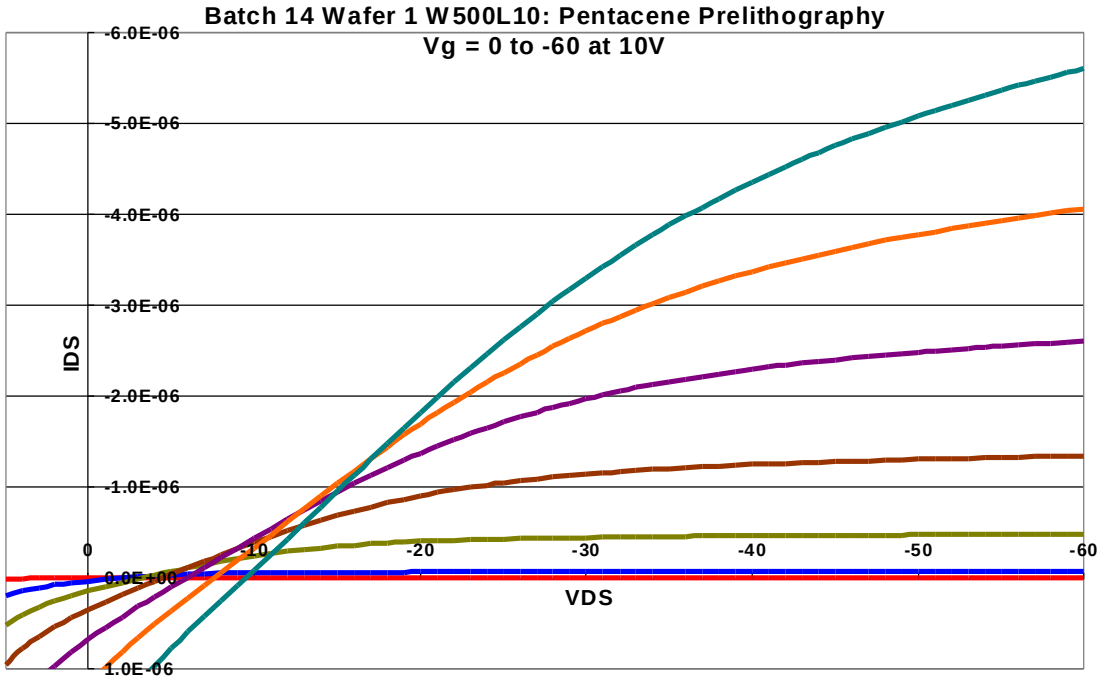

Figure 3.6 Batch 14IV Curve for W500L10 device with 40 nm thermally evaporated pentacene prior to lithography.

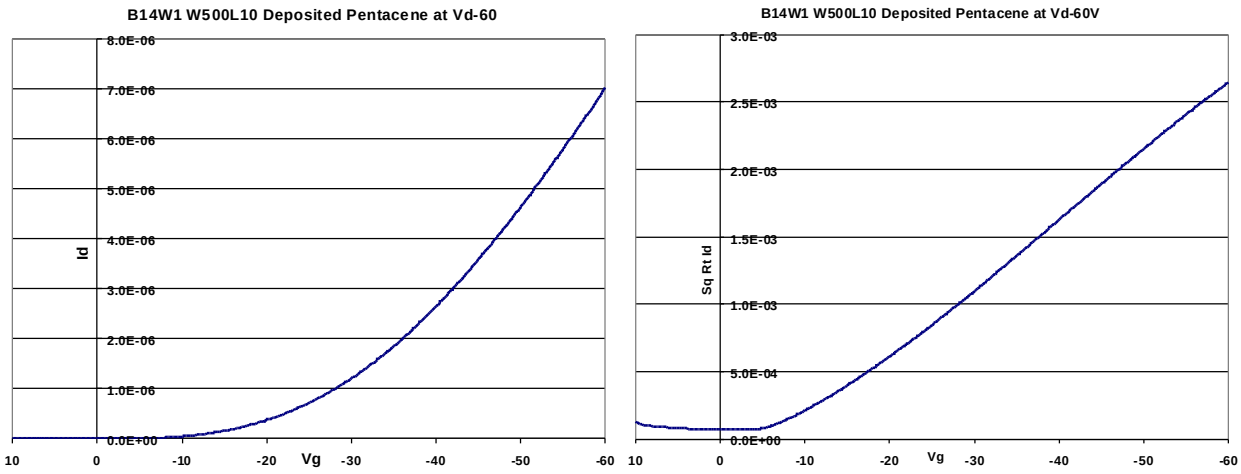

Figure 3.7 Batch 14 transfer curves (A) I_D-V_G and (B) $I_D^{½}$ vs. V_G for W500L10 device with 40 nm thermally evaporated pentacene prior to lithography.

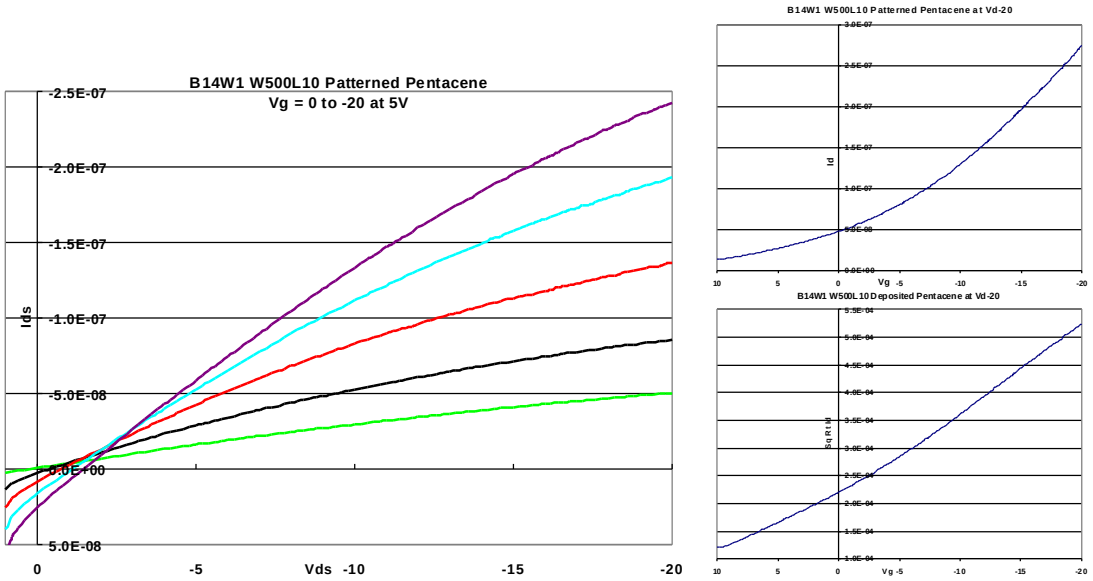

Figure 3.8 Batch 14 IV and transfer curves (I_D vs. V_G and $I_D^{1/2}$ vs. V_G) for W500L10 device with 40 nm thermally evaporated pentacene after photolithography.

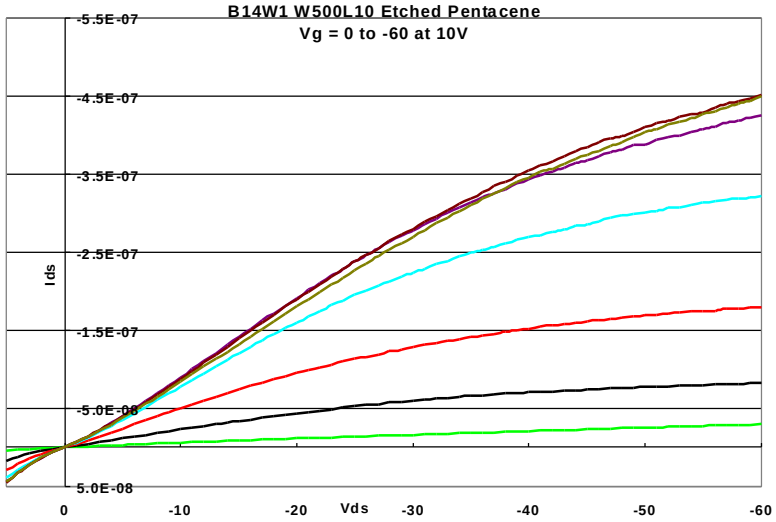

Figure 3.9 Batch 14 IV curve for W500L10 device with 40 nm thermally evaporated pentacene following one minute oxygen plasma etch.

3.6 Individual Gate OFETs

The idea of an individual gate OFET was not new, but the idea of having a reusable platform for testing field-effect mobilities in patterned organic semiconductors at low voltages was. In order to make this happen, new transistors were designed as shown in Figure 3.10. Here a 4 mask set would be utilized to isolate 5 distinct layers within the device: (1) an underlying substrate that is non-conductive, either thermally grown oxide on single crystal silicon or a plastic flexible substrate; (2) a layer of metal, either high temperature LPCVD polysilicon or gold, patterned for the gate electrode; (3) a dielectric layer; (4) a layer of patterned gold source and drain electrodes; and (5) a layer of organic semiconductor patterned with photoresist to prevent interference from other devices and from exposure to the atmosphere. The added layers increased the amount of processing steps from 10 to 30 as shown in process flow run sheets (Appendix 3.1 through 3.16). The flow sheets portrayed a quick, general outline of the manufacture

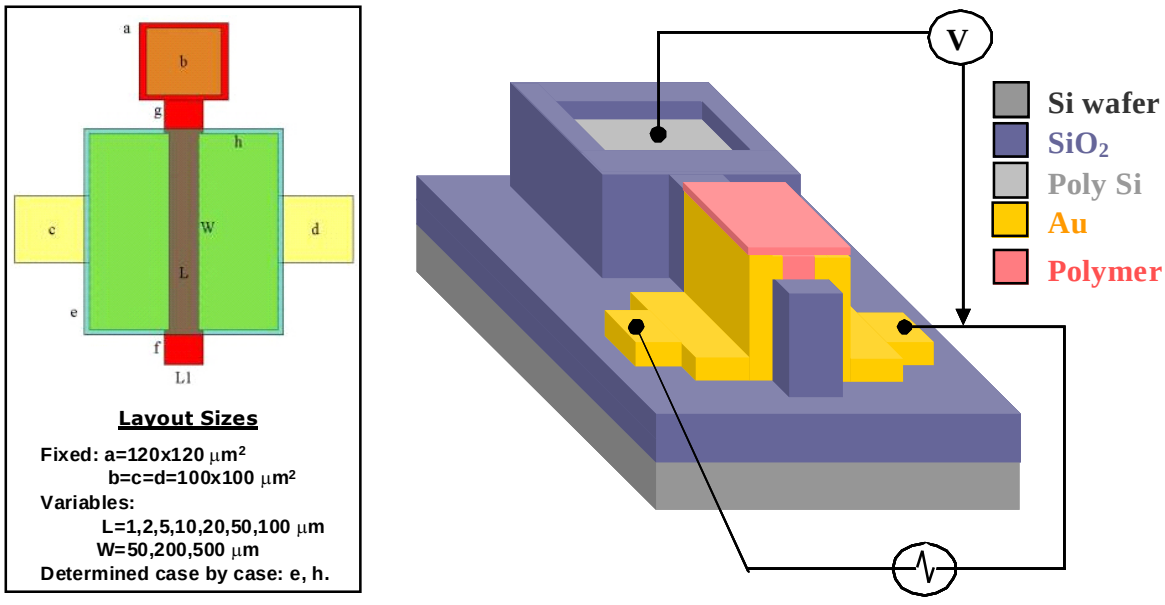

Figure 3.10 Individual gate OFET design in top view (left) and angled view (right).

process and were handy during manufacture; however, a thorough explanation of each step was important to grasp the overall idea and feasibility of the project.

3.6.1. Experimental

Silicon wafers were purchased from WaferNet, Inc. For individual gates, it was not important for the wafer to have an etched back, because the wafer was not acting as the gate electrode. Therefore, Si <100> test grade wafers were used in most cases; however, silicon <111> wafers from the common gate devices were used occasionally due to their availability. The wafers were cleaned in a piranha bath heated to 120°C for 10 min in the CMOS cleaning station. After the 10 minutes, the wafers were removed, dipped in BOE for 1 min, and rinsed in the dump rinser for 5 cycles. The wafers were then placed into a RCA clean at 70°C for 5 minutes. Removing the wafers from the metal clean, they were rinsed in the dump rinser for 5 cycles, and rinse again in the SRD. The wafers were then placed into nitride furnace 3 for an initial oxide growth using gateoxHH.003 recipe at 950°C with a 90 min growth time. The initial oxidation was necessary to prevent device to device contact through the substrate, since we're using a conductive silicon substrate. Initial oxide thicknesses were targeted at 800 Å, and thicknesses were verified using the Nanospec profilometer. From here it was possible to make devices with different gate materials and different dielectrics; therefore, the manufacture process for polysilicon and gold gates was explained separately.

3.6.1.1. Polysilicon Individual Gate Devices

For the polysilicon individual gate devices, the wafers containing the initial oxide layer were placed into poly furnace 4 where the LPCVD process deposited polycrystalline silicon at 1000°C for 7 min. Depositions were targeted at 1000 Å, 2200 Å, and 4500 Å for different batches to determine if the vertical profile affected the overall performance. Because polysilicon was not conductive, the metal was n-doped with phosphorus using recipe pypredop.001 in nitride furnace 1 for 15 min doping times for 2200 Å polysilicon. The wafers were then annealed for 8 min at 900°C in nitride furnace 1 to provide a good junction depth for doping. Phosphorus glass produced from the doping/annealing was removed with BOE until the wafer was uniform in color and dewet, typically 30 seconds. The wafers were rinsed using the dump rinser for 3 cycles and SRD. Target sheet resistivity was 50 Ω/sq and data was collected on a 4 point probe.

In order to convert the polysilicon layer into individual gates, the doped metal needed to be patterned. To do this, Futurrex 3000NP was spun at 4000 rpm for 30 seconds using a spin coater. Futurrex 1500NP could be supplemented for 3000NP-7, but deposition required spinning at 3000 rpm for 30 seconds. The photoresist was soft baked at 150°C for 90 seconds. Level one lithography was performed using OFET mask 1 on the MA6 mask aligner with an exposure at CI1 (405 nm, 18 mW/cm^2 intensity) for 7 seconds. A hard bake at 115°C for 90 seconds was followed by development in the Solitec developer for 45 seconds with MF319. The STS ICP was used to etch the polysilicon. Etch rates for the ICP using a SF_6 plasma were set at approximately 1000 Å/min using recipe *lukepoly*, which for 200 W power 4 cycles of 48 sec/cycle was enough to etch 2200 Å polysilicon in the unprotected areas. A one minute oxygen plasma

etch in the Gasonics Asher stripped the remaining photoresist. The wafers were then cleaned in piranha solution at 120°C, rinsed in the dump rinse, and dried in SRD.

The gate dielectric, silicon dioxide, was thermally grown in nitride furnace 3 using gateoxHH.003 for 11 hours and 30 minutes. This produced 200 nm of oxide, similar to that for the common gate devices, as measured using the nanospec. The gate, now fully covered in oxide, needed to be exposed for testing purposes; therefore, a gate cut (level two photolithography) was orchestrated by spinning Shipley 1813 at 5000 rpm for 60 seconds on the Karl Suss RC8 spinner, soft baked at 115°C for 75 seconds, and placed into the MA6 mask aligner. The features were aligned according to the alignment marks so that the gate cut would not overlap the gate. Exposure at CI2 for 3.4 seconds using OFET mask 2 was followed by development using MF319 for 45 seconds in the Solitec developer. The wafers were then rinsed with water and dried using a nitrogen gun. Etching of the oxide was performed at the CMOS wet bench in a bowl or tank containing BOE. Oxide etch rates were typically 1000 Å/min, so that 2 minutes of wet etch in BOE was enough to remove the exposed oxide. However, it was more important to remove all of the oxide from the gate pad rather than have perfectly vertical oxide walls for the gate cut, so etching was typically extended to 3 min for 200 nm thicknesses. Finally the photoresist was stripped either in the Gasonics asher for 1 min in an oxygen plasma or by washing with acetone.

To create source and drain electrodes, Shipley 1813 was spun onto the gate oxide at 4000 or 5000 rpm for 30 seconds at an acceleration of 2500 and then soft baked at 115°C for 75 seconds. Level three photolithography was performed on the MA6 at CI2 for 8 seconds using OFET mask 3. The wafers were place in a glass bowl containing

chlorobenzene for 20-25 minutes. The purpose of the chlorobenzene was to harden the photoresist for the liftoff process. The photoresist was developed for 75-90 seconds in the Solitec developer, rinsed with water, and dried with a nitrogen gun. Using the CVC E-beam evaporator, 50 Å of titanium and 2000 Å of gold were evaporated onto the wafer's surface at a rate of 3 Å/second. To liftoff the photoresist, the wafers were placed into glass bowls containing acetone and left overnight. This process removed all of the remaining photoresist that had Ti/Au on top. Additional washing with acetone removed any residual photoresist or metal. Tenkor-KLA or AlphaStep profilometers were used to measure source and drain height.

3.6.1.2. Gold Individual Gate Devices

For gold individual gates, Shipley 1813 was spun onto the initial oxide layer at 4000 or 5000 rpm for 30 seconds with an acceleration of 2500 using the RC8 spinner. The resist was soft baked at 115°C for 75 seconds. Level one lithography was performed using OFET mask 1 in the MA6 mask aligner with a 40 nm alignment gap and CI2 exposure for 8-9 seconds. The wafers were placed into a glass bowl containing chlorobenzene for 20 min. The chlorobenzene penetrated the resist, hardening it for development and liftoff. Development took place in the Solitec developer for 75-90 seconds or until the features fully developed. 50 Å of titanium and 2000 Å of gold were deposited using the CVC E-beam evaporators at 10^{-6} torr at rates of 3 Å/sec. Liftoff of the photoresist and metal were done in a covered glass bowl containing acetone left overnight. The wafers were washed with acetone the next morning to remove any

residual photoresist and metal that had not lifted off. Gate height and channel lengths were measured using profilometry.

Because we have implemented a gold gate architecture, silicon dioxide and silicon nitride could not be grown thermally; therefore, we deposited 3000 Å of PECVD silicon dioxide using the *CMOS3000* recipe on the STS PECVD at a growth rate of approximately 80 Å/second. Level two lithography for the gate cut and level 3 for the source-drain deposition were both done exactly the same as for the polysilicon gate.

3.6.1.3. Polymer Deposition and Patterning

Polymer depositions were done based on the property of the organic material. For polyacenes, thermal evaporation at 10^{-8} torr produced 40 nm organic layers. Polythiophenes, typically 1 ml of a 4.0 mg/ml concentration solution, were spin coated at 3000 rpm for 60 seconds, leading to 30-60 nm thick polymer layers. Current-voltage measurements were taken after deposition; however, to individualize the devices, level four lithography was performed by spinning Shipley 1813 at 4000 or 5000 rpm for 30 seconds with an acceleration of 2500. The resist was soft baked at 115°C for 75 seconds. Exposure was done at CI2 for 3.4 seconds using OFET mask 4 in the MA6. The resist was developed in the Solitec developer with MF319 for 45 seconds and then rinsed with water. Polymer etching was performed based on the organic material. Polythiophenes were etched for 5-15 seconds in a glass bowl containing chlorobenzene, washed with water, and dried with a nitrogen gun. Pentacene was etched in an oxygen plasma. The wafers were then vacuum baked at 60°C and 10^{-3} torr overnight. Current-voltage measurements were repeated.

3.6.2. Individual Gate Results

In our first approach to individual gates, a series of experiments were performed to examine their feasibility. First it was important to measure the devices without a semiconductor layer to prove that there was no current flow between the source-drain electrodes and no leakage currents between the source and gate electrodes. The IV and transfer curves shown in Figure 3.11 were from a W500L10 Batch 1 device wafer. The curves showed only noise at the minimum resolution of the machine, 10^{-13} amps. The tests were repeated for different device sizes and they all reproduced similar noise levels for source-drain currents. However, this result only accounted for the possible leakage though the dielectric at the point of overlap between the source and gate electrodes, and most leakage current occurs between the organic and the gate electrode. Therefore, measuring the source-gate current with the organic semiconductor present was key to determining the presence of leakage currents. A compilation of IV and transfer curves were performed on batch 1 with 40 nm P3UBT (Figure 3.12 and Appendix 3.17). As can

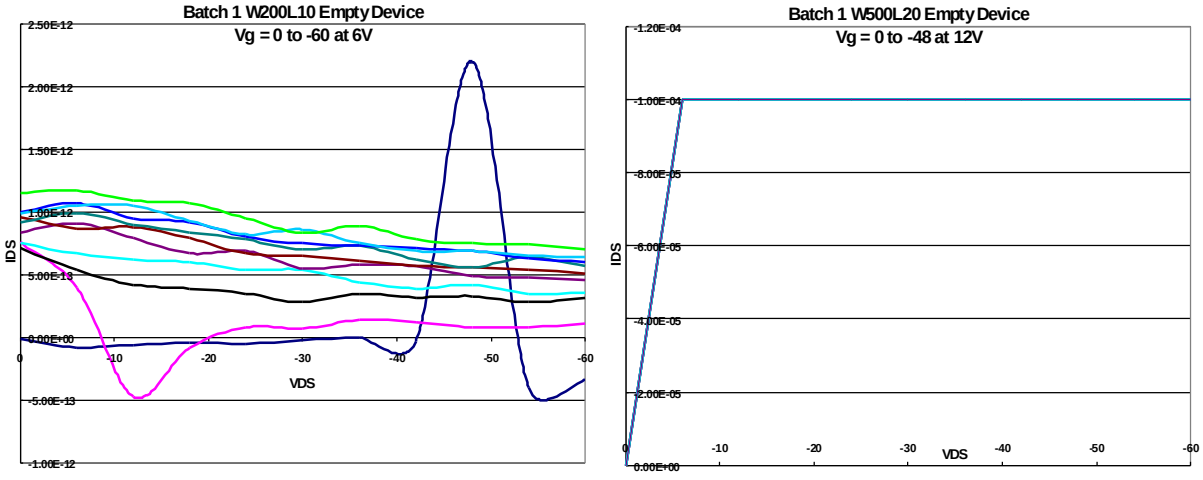

Figure 3.11 Batch 1 IV curve for (A) W200L10 empty device and (B) a W500L20 shorted device.

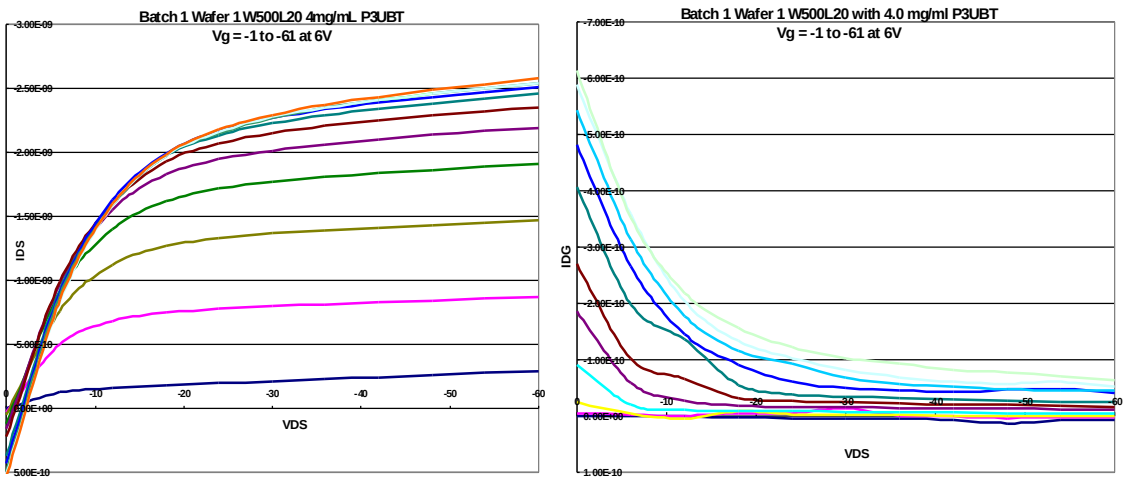

Figure 3.12 Batch 1 W500L20 with 4.0 mg/ml P3UBT (A) I_{DS}-V_{DS} curve and (B) I_{DG}-V_{DS} curve.

be seen in the inset, the I_{SG} vs V_{DS} curve shows a substantial amount of leakage current for batch 1. This was common throughout the entire batch, and it was later discovered that the oxide layer was contaminated with gold, thus leading to source-gate leakage through the dielectric at the semiconductor overlap. Later trials with non-contaminated oxide reduced or eliminated the leakage currents to noise levels.

The next step was to observe the effect of photoresist (Shipley 1813) on the source-drain current of a device without semiconductor to see if the photoresist by itself provided a means of charge transfer. Photoresist devices from batch 1 failed to show substantial source-drain or source-gate currents above the detection limit of the analyzer (Appendix 3.18).

Finally, we wanted to make P3UBT and pentacene devices for a direct comparison to our common gate devices and Kippelen's interdigitated common gate devices, while ensuring that our individual devices worked properly. The aforementioned compilation of IV and transfer curves for batch 1 with 40 nm P3UBT exhibited an average charge mobility of $7x10^{-6}$ cm^2/Vs, with a maximum FEM of $1.8x10^{-5}$ cm^2/Vs. As

stated earlier, leakage currents were observed between the source and gate due to oxide contamination. The data set was repeated with P3UBT devices from batches 5 and 9 produced molilities for P3UBT $\mu = 6.4x10^{-5}$ with on/off = $5.0x10^{4}$ and $\mu = 3.6x10^{-5}$ with on/off = $1.3x10^{3}$ and V_{th} = -3.7V (Figure 3.13 and Appendix 3.19). These values were very competitive with Kippelen's interdigitated common gate results and with our common gate devices. Therefore, it was determined that these individual devices, with pristine gate oxide, would function just as well as common gate devices with the benefit of testing multiple device sizes on the same wafer. However, we needed to determine if higher mobility materials experienced the same effects as did the low mobility P3UBT.

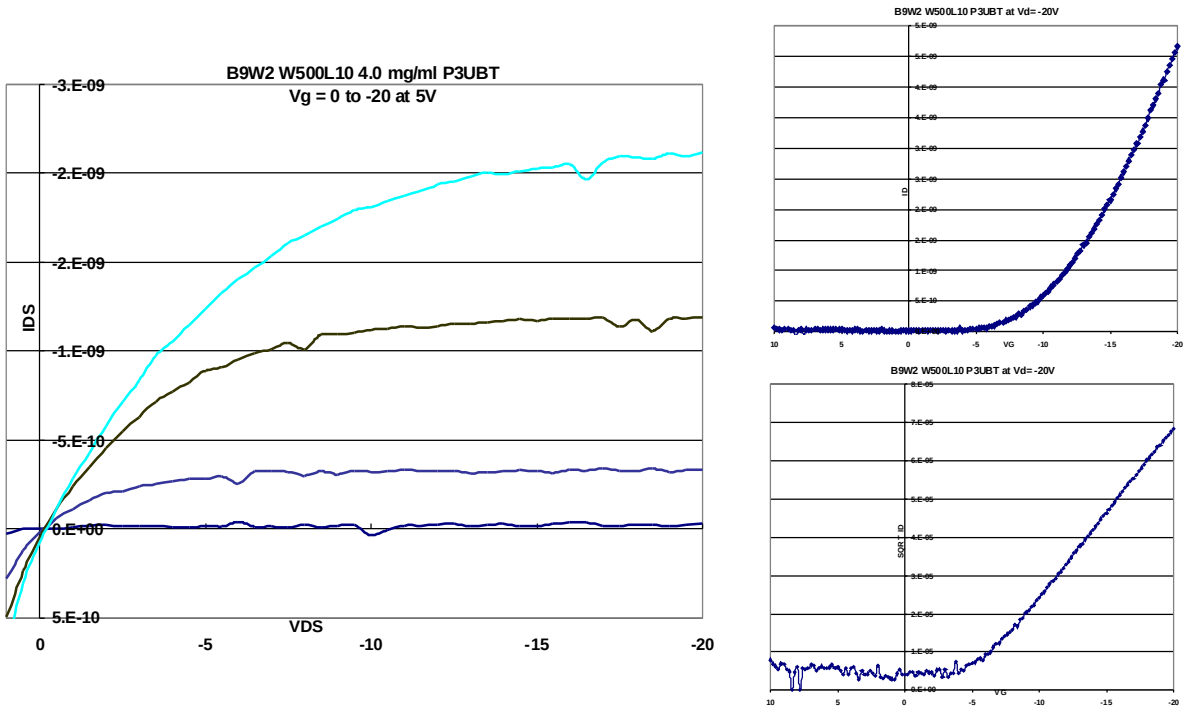

Figure 3.13 Batch 9 Wafer 2 W500L10 with 4.0 mg/ml P3UBT (A) I_{DS}-V_{DS} curve, (B) I_D-V_G curve, and (C) $I_D^{½}$-V_G curve.

3.6.2.1. Pentacene Comparison

As stated previously, pentacene is the most promising of the organic materials because of its high mobility, at 2.2 cm^2/Vs as shown in Chapter 2, and easy deposition through evaporation. Therefore pentacene was a good platform for comparing the effects of lithography on the polymer semiconducting layer and the overall performance of the individual gates. Both the individual gate and the common gate architecture were placed into an ultra-high vacuum chamber at 10^{-8} torr where 40 nm of pentacene was evaporated onto the surface of the wafers. The evaporation process was previously described in literature [6]. The devices were tested following deposition and before patterning. As seen in Figure 3.6 and 3.14, the common and individual gate devices exhibited large amounts of contact resistance and leakage currents. This was expected due to the interconnection of devices by the organic layer. Currents less than 1 μA, V_{th} = -6 V, and on/off ratios between 10^2 and 10^3 were observed. The apparent FEM of the pentacene was 0.045 ± 0.005 cm^2/Vs; however, this value is not a true value because of the

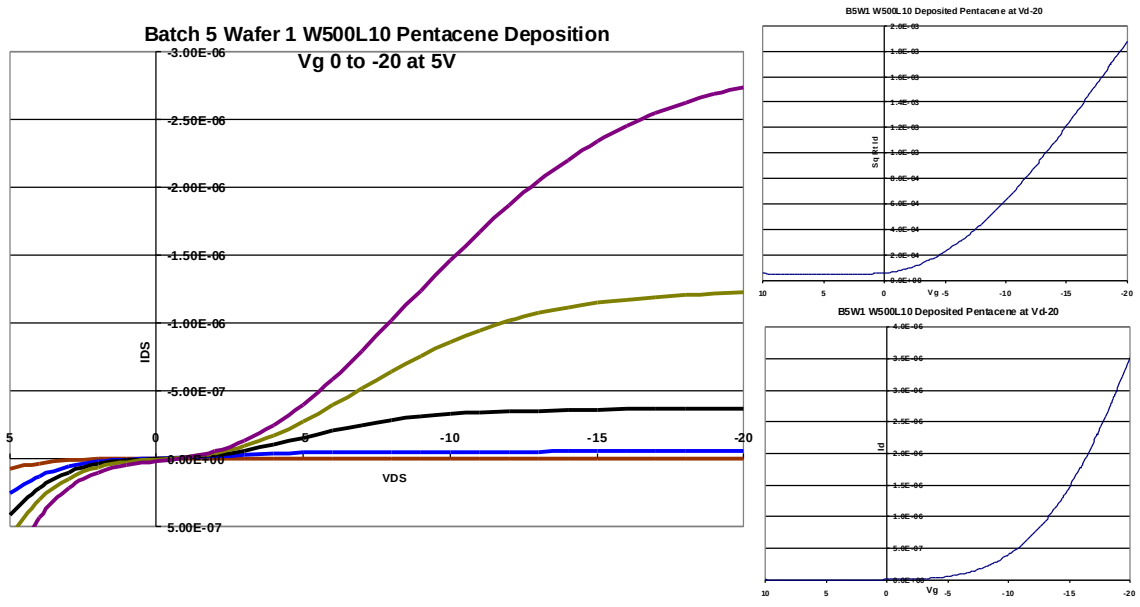

Figure 3.14 Batch 5 Wafer 1 W500L10 with 40 nm deposited pentacene (A) I_{DS}-V_{DS} curve, (B) I_D-V_G curve, and (C) $I_D^{½}$-V_G curve.

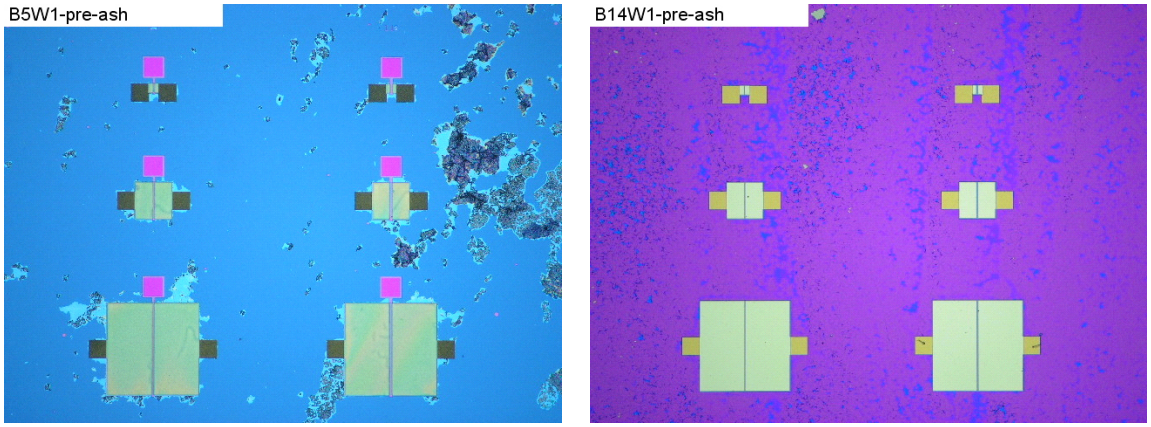

Figure 3.15 Optical microscopy of batch 5 (A) and batch 14 (B) L5 and L10 devices after lithography.

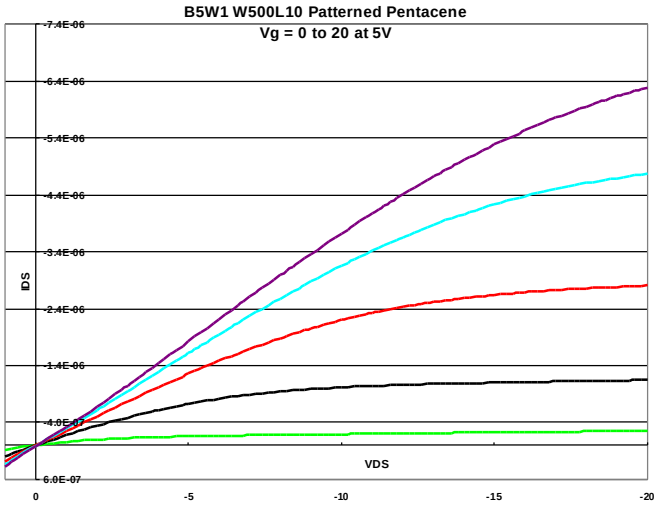

Figure 3.16 IV Data for batch 5 W500L10 device after lithography.

aforementioned artifacts.

Shipley 1813 was spun on the both gate architectures at 5000 rpm for 30 seconds, soft baked at 115°C for 75 seconds, then aligned and exposed in the MA6 for 3.4 seconds at CI2 wavelength. The individual gates were developed in the Solitec developer with MF319 fro 45 seconds; however, the developer physically washed off both the exposed photoresist and the underlying pentacene. The physical etching of the pentacene can be seen in the optical microscopy in Figure 3.15A. The lithography and etching of the devices led to the observed IV curves shown in Figure 3.16. The curve traces still showed

a small amount of contact resistance, yet the leakage currents and a majority of the contact resistance was removed from lithography and etching. The new FEM data for various device sizes was 0.035 ± 0.003 cm^2/Vs, the on/off ratio increased to 10^4, and the new threshold voltage was around 4 V. The decrease in current and change in threshold voltage was believed to be caused by strain induced by the encapsulation by the photoresist.

The observed improvement in the curve traces, the idea that the lithography was acting as the patterning and etching of the devices was not desired. Therefore, the common gate devices were developed in a glass bowl slightly agitated by hand. The development of the photoresist was maintained at 45 seconds, and the pattern was generated sufficiently without etching the underlying pentacene, as shown in Figure 3.15B. The curve traces of the common gate patterned pentacene were shown in Figure 3.8. Identical contact resistance and leakage currents were observed prior to patterning. This was expected based on the belief that the leakage was due to the organic layer rather than through the dielectric layer. However, the mobility took a large hit, falling to 5×10^{-4} cm^2/Vs and, as seen with the individual devices, an inversion of the threshold voltage from -5 V to 12 V was observed from Vg = 0 to 20 V. Mobility measurements were not taken literally since too many artifacts were observed.

Next, both device architectures were placed into a one minute oxygen plasma using a PlasmaPreen II-862 with 2 SCFH oxygen flow. The low wattage ashing provided improved selectivity of the pentacene versus the photoresist. Optical microscopy (Figure 3.17A&B) taken of the etched devices showed a big difference between pentacene

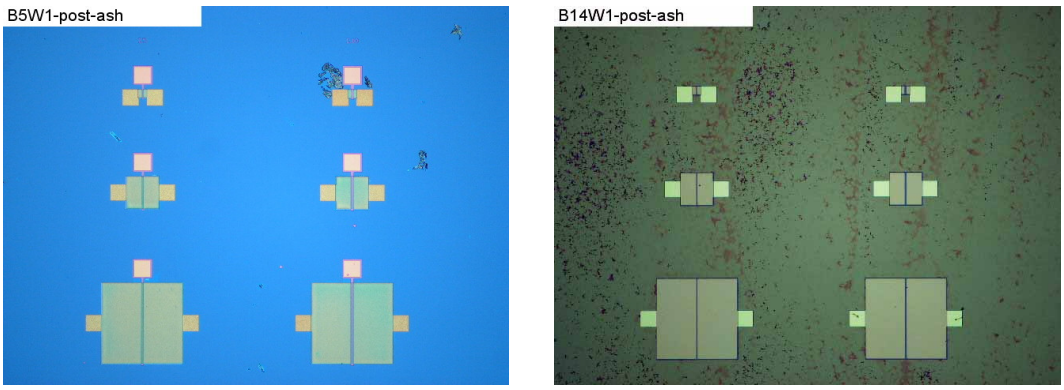

Figure 3.17 Optical microscopy of batch 5 (A) and batch 14 (B) L5 and L10 devices after 1 minute oxygen plasma etch.

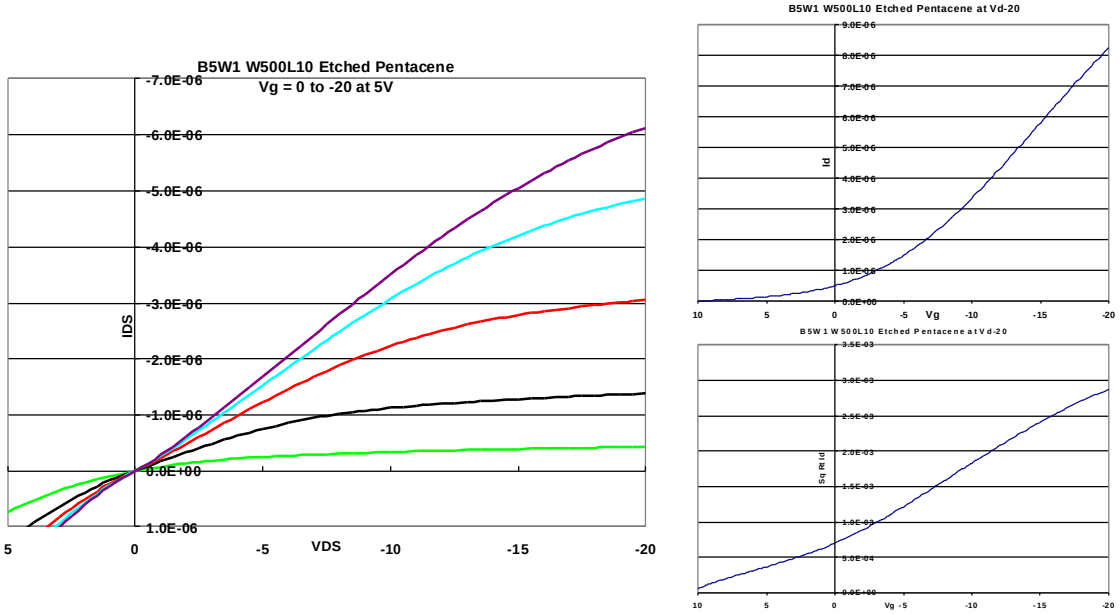

Figure 3.18 Batch 5 Wafer 1 W500L10 with 40 nm Pentacene after etching (A) I_{DS}-V_{DS} curve, (B) I_D-V_G curve, and (C) $I_D^{½}$ -V_G curve.

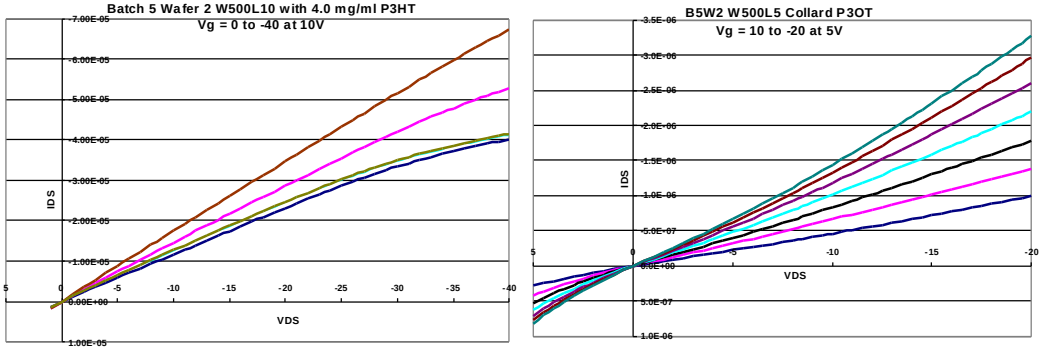

Figure 3.19 IV curve for batch 5 wafer 2 (A) W500L10 with 4.0 mg/ml P3HT and (B) W500L5 with 4.0 mg/ml P3OT.

coverage before and after ashing. Both wafers were placed into a 10^{-3} torr vacuum oven at 70°C for 20 hours. The devices were then tested, and the curve traces shown in Figure 3.18 and 3.9 for both the individual and common gates displayed proper transistor characteristics with minimal leakage and contact resistance. Mobility data for the individual approximately 5 V, while the common gate devices maintained the low mobilities observed after patterning. For the common gate devices, etching removed the pentacene between devices, thus improving the transistor behavior of the devices such that the leakage currents and contact resistance were greatly diminished. Mobilities improved to 3 x 10^{-3} cm^2/Vs and on/off ratios increase to 10^4 based on the ability to increased applied voltages based on the improved dielectric properties of the single crystalline silicon dioxide layer.

The change in transistor behavior from unpatterned to patterned devices demonstrated the strong need for separation of devices when testing. These results demonstrated the strong need for device separation when testing, either by dicing or by patterning and etching.

3.6.2.2. Polyalkylthiophenes and Surface Modifications

Now that the need for device separation was confirmed, we repeated the aforementioned procedure for different materials, including several polyalkylthiophenes, such as poly-3-hexylthiophene (P3HT), P3UBT, and poly-3-octylthiophene (P3OT). The mobility data for P3HT has been well published over the last 5 years in different device architectures with different surface modifiers [7]. We found that the low mobility P3UBT material worked well in our devices with a pristine oxide layer. IV and transfer curves

reached charge saturation and displayed little evidence of artifacts. Mobility results of $5x10^{-5}$ cm2/Vs and of/off ratios of 10^3 corresponded to that of Kippelan's interdigitated devices. However, moving to the higher mobility P3HT and P3OT produced the resistance curves shown in Figure 3.19A&B. Field modulation was observed in the IV curve, but charge saturation was not evident, even for common gate devices with and applied gate voltage of 80V. It was thought that surface modifiers, such as hexamethyldisilizane (HMDS), octyltrichlorosilane (OTS-8), and octadecyl-trichlorosilane (OTS-18) [8] would help the device characteristics and improve charge mobility, even though currents were in the microampere range. HMDS was applied to the native surface of the devices following literature procedures [9] followed by polymer deposition and etching. Etching failed to remove the HMDS between devices; however, this was not initially perceived as a problem since the HMDS was not conductive. IV curves from the P3HT and the P3OT with HMDS now showed proper field modulation and charge saturation with a slight change in inflection point from a small contact resistance (Figure 3.20). This may have been due to the thick titanium adhesion layer (30 nm) used in batch 5, which would also help to explain the high threshold voltage. Later batches were made with 3 nm of titanium to minimize the observed contact resistance while maintaining an ohmic contact. Both the P3HT and P3OT FEM were calculated to be 10^{-3} cm^2/Vs, on/off ratios of 10^3, and threshold voltages of -25 V. Mobility data from these curves was consistent from reports a few years back but not as high as recent reports. This was due in part to a non-optimized method of polymer application. This will need to be done in future work, as would the need for improving and studying the adhesion layer's effects.

One concern with the use of the HMDS was in the two orders of magnitude decrease in total source-drain current form 10^{-6} to 10^{-8} amps. Some literature called for the washing of the HMDS following application and baking [10], while others called for simple spinning at medium speeds [9]. If the HMDS layer was too thick, this would cause interference in the applied field and decrease the overall current. Therefore, we believed that this was the case and that the latter reference failed to wash and bake the HMDS or failed to mention it in their experimental procedure. Nonetheless, this topic of research will be of future interest in our group.

3.6.2.3. Gate Material and Dielectric Comparison

The main benefit of having thermally grown oxide as the dielectric layer was that it was easy to produce a robust, defect-free dielectric layer with a good dielectric constant. Thus we chose polysilicon as one of the individual gate materials since oxide

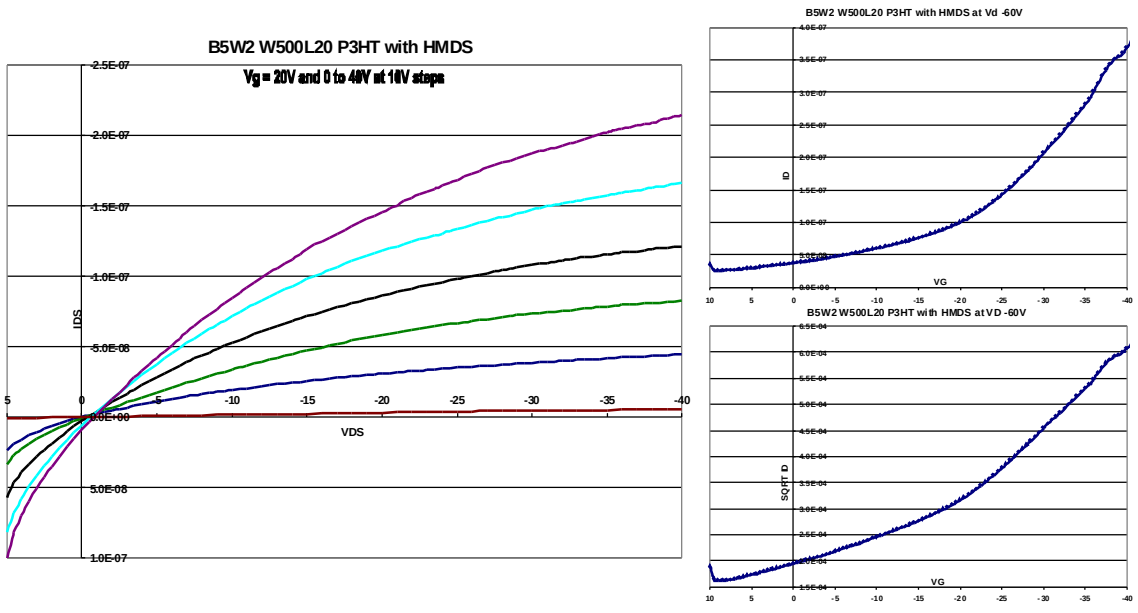

Figure 3.20 Batch 5 Wafer 1 W500L20 with 4.0 mg/ml P3HT with HMDS (A) I_{DS}-V_{DS} curve, (B) I_D-V_G curve, and (C) $I_D^{½}$-V_G curve.

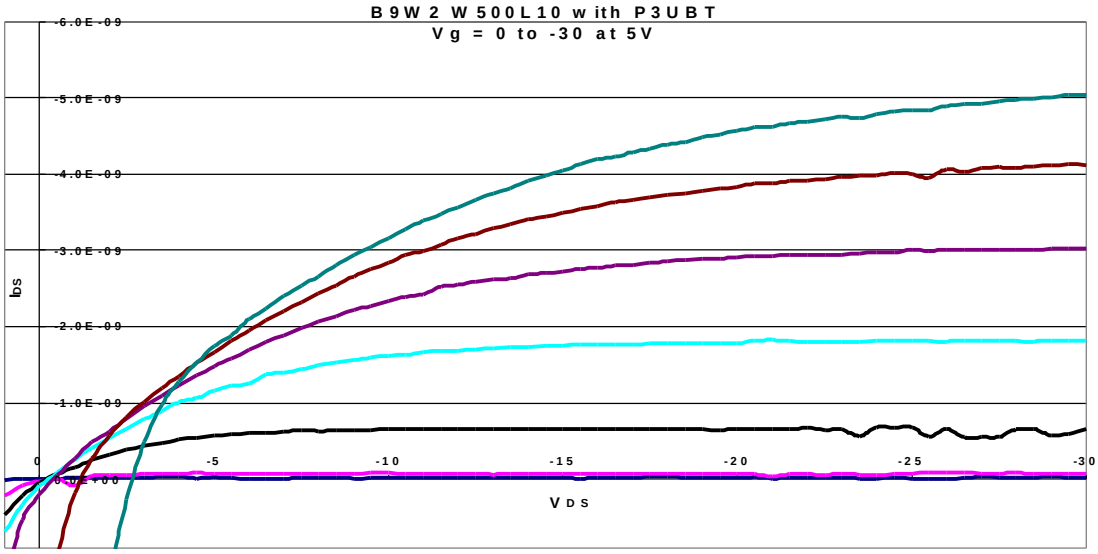

Figure 3.21 Batch 9 Wafer 2 W500L10 with 4.0 mg/ml P3UBT. Increasing the gate voltage above the critical voltage of the gate dielectric causes sever breakdown, as can been seen from the IV curves pulling away from the origin.

could be thermally grown from its surface. However, thermally grown oxide on polysilicon was not as robust as its single crystal counterpart. As can be seen in the IV curves from batch 9, increasing the gate voltage to 30 V for materials such as P3UBT (shown in Figure 3.21) led to substantial breakdown and leakage currents. When compared to the common gate with pristine oxide, gate voltages exceeded 80 V before leakages from the oxide breakdown were present. This was not perceived as a problem because low operating voltages were desired for OFETs. However, increasing the gate voltage lead to increased mobility and on/off ratios; therefore, our device characteristics would be noticeably lower for individual gates. The same went for the gold gates with CVD oxide. Operating voltages could not exceed 20 V before breakdown was observed, however, the oxide provided a good means of dielectric strength between 0 and 15 V, i.e. good field modulation with few artifacts. The gold, on the other hand, was not as resilient to silicon processing as expected. Gold decomposition was observed following treatment

in oxygen plasma. Sections of the source and drain electrodes, as well as the exposed gate pad, were 'eaten-away' during each subsequent plasma cleaning of the organic material. This observation caused the loss of several device wafers, yet the problem itself could be avoided by using alternative cleaning methods such as solvents though vigorous spray washing. For materials such as pentacene that has poor solubility in most organic solvents, high velocity spray washing and low wattage oxygen plasma still removed most of the organic material without damaging the gold. Since most of the preferred organic semiconductors are solution processable, individual gold electrodes could be used with CVD oxide. However, concern should be taken when using gold electrodes for reusability. In the future, replacement of gold with doped polysilicon would eliminate the need for this caution.

3.6.3. Flexible Substrates

Although the main purpose of this work was to develop a platform for reproducible high-throughput testing of numerous organic semiconductors, the individual gate design allowed us to step aside and look at flexible substrates as platforms for our devices. 500 micron-thick PEEK substrates were used to fabricate a 4 inch diameter flexible wafer containing 2100 OFETs using the gold individual gate process described for batch 7 (Appendix 3.7). The flexible process flow sheet was outlined in Appendix 3.13. PEEK substrates were chosen due to their ability to withstand the 300°C processing temperature of the STS PECVD furnace and the solution processing required for liftoff patterning of the gold electrodes and organic semiconductor. Additionally, 500 micron thicknesses were required for mask alignment. 100 micron thick PET substrates were

initially used; however, they were too flexible to achieve a uniform alignment across the entire substrate. Unfortunately, device testing was not completed due to a lack of time. However, devices were constructed. These devices should behave similarly to those built on the silicon substrate. This would be a point of interest for future work.

3.7. Conclusion

We have successful designed and constructed both common and individual gate organic field-effect transistors based on a few well-reported and new organic semiconductors. Device architectures were designed and constructed to determine if they had an effect on device performance. Not only did the device architecture have a bearing on the device performance, but more importantly each individual step of the manufacture process played an important role in the device's operation. Any deviation to the process conditions could have led to contamination, loss of ohmic contact, or misalignment which consequently led to device failure. Mobility data comparisons fell within the literature reports for commonly published organic semiconductors such as P3HT and pentacene, but more importantly, the individual gate approach was successful in creating a platform for high throughput screening for large amounts of organic materials on a single wafer.

3.8 Future Work

The purpose of the work described within this chapter was to develop a platform for reproducible, high-throughput testing of numerous organic semiconductors. We have been able to achieve this though patterning of the organic semiconductor, both in a

common gate and an individual gate format. OFET architectures were designed so that seamless transition could be made if the need arose to move to flexible substrates.

Future work in this area would need to follow along these lines as a test platform for high screening of organic semiconductors. Surface modifications need to be addressed, more specifically; the interaction and role the modifier plays would be an important addition to the field of organic electronics. Improved functionality of the surface modifier may lead to increased mobility as seen in the bulk mobility of the single crystal. Also, the affect the modifier has on the dielectric constant needs to be addressed. If the modifier acts as an additional dielectric layer, then the dielectric constant needs to be altered to reflect a more accurate FEM.

3.9 References

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CHAPTER 4:

CORRELATION OF MORPHOLOGY AND DEVICE PERFORMANCE IN INORGANIC-ORGANIC TIO2-POLYTHIOPHENE HYBRID SOLID-STATE SOLAR CELLS[1]

4.1 Introduction

The main introductory points for this Chapter can be found in the Background and in Section 1.4.

4.2. Experimental

4.2.1 Sol-Gel TiO_2 Electrode Preparation

Nanoporous TiO_2 films were prepared using the sol-gel methods previously reported by several groups [1-3]. A 500 µl aliquot of titanium (IV) isopropoxide [$Ti(^iPrO)_4$] was added to a solution containing 10 ml of dry ethanol, 250 µl of nanopure water (water purified using a NanoPure water filtration system), and 2-5 drops of nitric acid so that the pH was between 1-2. The reaction was carried out using Schlenk techniques under an argon atmosphere. $Ti(^iPrO)_4$ was added dropwise at a slow rate. The solution was stirred vigorously for 24-48 hours before application to the substrate. Fluorine-doped conductive tin oxide (SnO_2:F or CTO-1.0x1.0 cm^2 and 1.0x1.5 cm^2, sheet resistance ~15 Ω/cm^2) glass plates purchased from Hartford Glass were used as electrode substrates. The conductive glass substrates were cleaned in triplicate using deionized water and either acetone or isopropanol. An approximate 2 mm section of glass was covered using Kapton tape to create an electrode contact (further referred to as the

[1] The ideas, context, and images described within this chapter were published in the April 2004 issue of Coordination Chemistry Reviews, volume 248, pages 1491-1499.

contact tab) and care was taken to prevent underflow of sol-gel during deposition. The sol-gel solution was spin-coated onto the substrates at spinning speeds of 1000, 2000, 3000, and 5000 rpm using a Laurel Technologies WS-400A-6NPP-LITE spin coater. Samples were dried under ambient conditions for several minutes. They were then placed in a Lindberg furnace and sintered at 450°C from 30 to 60 min. The temperature of the furnace was ramped to 450°C at 25°C/min and, following sintering at the desired time period, ramped down to 120°C at 50°C/min with an air flow rate of 10 ml/min. Upon cooling to 120°C, TiO_2 samples were immediately removed from the furnace and placed into dry chloroform to prevent them from interacting with moisture.

4.2.2 Polymer Synthesis and Deposition

P3UBT was synthesized using Sugimoto-type oxidation methods previously reported [4,5]. Sintered TiO_2 samples to be coated with P3UBT were initially placed in a protecting solution containing 0.04, 0.40 and 4.0 mg/ml P3UBT in chloroform; however, due to aggregate formation upon drying, this procedure was abandoned and dried chloroform was used instead. The samples were then placed onto the spin coater where two subsequent 100 µl applications of warm 0.4 or 4.0 mg/ml P3UBT in chloroform were spun at 1000, 2000, or 3000 rpm. It was necessary to filter and heat the polymer solution prior to deposition to promote a uniform polymer film and reduce aggregate formation. Polymer solutions were filtered using a 0.2 µm PTFE Aerodisc syringe filter. The polymer films were dried upon completion of spinning. Chloroform (Fisher) was used to clean residual polymer on the contact tab, edges, and underside of the conductive glass and were then stored in a desiccator until they were analyzed or made into PV cells.

4.2.3 PV Cell Construction

The edges of the remaining polymer layer were masked with Kapton tape to create a well 0.20 or 0.25 cm^2 in area. Two to six drops of hot 4.0 mg/ml solution of P3UBT in chloroform were deposited into the well and dried slowly to create a thick, uniform film resistant enough to prevent the carbon particles from punching through the polythiophene layer. A hole-punch was used to remove a circular area in a piece of electrical tape. The tape was then positioned over the top of the polymer as a contact mask. Carbon powder (Merck 4206) dried at 110°C [6-8] was applied into the contact mask and formed a thin contact to the polymer. Lastly, the copper tape (3M, 1181) was used as the positive electrode and was pressed against the carbon powder. Devices were illuminated through the TiO_2 side using a solar lamp (AM1.5) and current-voltage measurements were taken on a Keithley model 196 digital multimeter. Measurements were taken at the PV Center of Excellence at the Georgia Institute of Technology Electrical Engineering department.

4.2.4 Thin Film Characterization

All AFM measurements were performed using a Multimode™ NanoScope IIIa (Veeco Metrology). The "J" piezo scanner was calibrated in x, y and z using NIST certified calibration gratings (MikroMasch). Microlever™ AFM probes (Part # MLCT-AUHW, Veeco Metrology) possessing spring constants of approximately 0.03 N/m were used for most imaging conditions. For moisture-sensitive samples, a custom-built nitrogen sleeve enclosed the AFM and was held at a relative humidity of less than 10%. All contact mode AFM images were obtained under a minimal load via minimization of

the setpoint to maintain contact with the substrate. All images were composed of 512 data points per line at 512 lines per image. Tracking of the torsional movement of the cantilever (friction mapping) was also done to interpret the degree of surface coverage of all chemical layers used in creating the solar cell. This mode of data collection can discriminate hydrophilic and hydrophobic regions of a substrate at the sub-micron level. In some instances it was necessary to image the samples of interest utilizing Tapping Mode™ AFM. In these instances, cantilevers possessing resonant frequencies around 280 kHz were used (Model CSC 12, MikroMasch).

All AFM roughness values reported herein are root mean square (RMS) roughness. These values were calculated via the standard equation:

$$R_q = \sqrt{\frac{\sum (Z_i - Z_{ave})^2}{N-1}}$$

where Z_i is the z-height of the i-th pixel, Z_{ave} is the average of all z-heights in a single image and N is the number of pixels. AFM topographical images were acquired at 10 different, non-overlapping domains on the surface. The RMS roughness for each image was determined following a first order plane fit. Samples for scanning electron microscopy (SEM) analysis were prepared by placing small amounts of Aquadag colloidal graphite (Ted Pella) onto standard aluminum specimen mounts (Ted Pella) and then immobilizing the sample of interest on the colloidal graphite. Since some of the samples were moisture sensitive, following immobilization, the samples were stored overnight under a nitrogen atmosphere. All samples were analyzed using an S-800 SEM (Hitachi) equipped with energy-dispersive x-ray (EDX) microanalysis (Thermo Kevex X-ray, Model 3600-0398). All spectroscopic measurements were made using a driving voltage of 7-9 kV.

A Surface Science Laboratories, Inc. SSX-100 X-ray photoelectron spectrometer with an Al Kα X-ray source (1486.6 eV) was used for angle resolved XPS studies. The base pressure was around $5x10^{-9}$ torr. Film thicknesses were measured using a Tencor Alpha-Step 500 profilometer. Optical micrographs were obtained with an Olympus BX51 microscope operated in reflectance mode.

4.3. Results and Discussion

4.3.1 TiO_2 Electrode Characterization

The CTO glass and TiO_2 electrodes were characterized using AFM, SEM-EDX, XPS and optical microscopy to determine the effect of the morphology of the underlying substrate upon subsequential layer depositions as well as on the overall device performance. Kapton tape was used to mask the CTO underlayer from sol-gel deposition. The adhesive of the tape was chemically-resistant to the solvents used in these experiments. Application of the sol-gel through spin-coating at 1000, 1500, 2000, and 3000 rpm produced 100, 70, 40, and 12 nm films, respectively. The tape, however, is not a perfect mask. At the rotation speeds used, the sol gel seeps under portions of the tape leaving an irregular interface. As a result, film thickness had to be measured using profilometry rather than AFM. Optical microscopic images obtained after sintering of the TiO_2 film deposited at spin-speeds of 1000 rpm (Figure 4.1a) and 2000 rpm (Figure 4.1b) reveal significant differences in surface morphologies. The thicker film (Figure 4.1a) was highly fractured during the sintering process whereas the thinner film (Figure 4.1b) was uniform.

Two concerns with using Kapton tape as a mask were: (1) removal of the tape leaves behind an adhesive residue or (2) the adhesive (or its removal) modifies the surface morphology of the underlayer. To alleviate these concerns, native fluorinated tin oxide glass was half-covered with Kapton tape and then removed. Ten contact mode images were acquired at randomly chosen locations on the unmasked portion of the slide. The average RMS roughness for the fluorinated tin oxide glass was 10.3 ± 1.1 nm. The tape was removed from the masked portion and ten additional contact mode images were acquired. The average RMS roughness for the tape-treated surface of the fluorinated tin oxide was 10.8 ± 1.4 nm. This value is statistically equivalent to that found for the unmasked side. This result leads us to conclude that the tape adhesive does not modify the surface morphology of the CTO surface. Force curves were also acquired at various positions on the surface of both the masked and unmasked portions of the CTO surface. Equivalent rupture forces were obtained. This finding supports the hypothesis that no tape residue was left behind by the Kapton adhesive.

Next, a native fluorinated tin oxide glass substrate with Kapton tape covering half of the glass was treated and spun at 1000 rpm with a low viscosity sol-gel. Contact mode AFM and friction mapping were carried out to determine the average surface roughness and the degree of coverage (Figure 4.2). The average RMS roughness of this film was 9.1 ± 0.5 nm. It is important to note that the friction map (Figure 4.2b) demonstrates that the cantilever experiences a high amount of torque. This can be attributed to the high degree of hydrophilicity of the TiO_2 [9] as well as the thicker film having a higher degree of

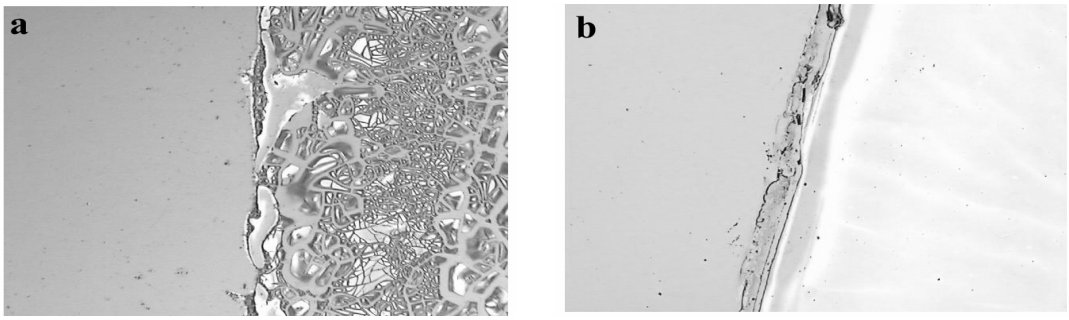

Figure 4.1 Optical micrographs depicting the interface between SnO_2:F and the TiO_2 thin film spin-cast at (a) 1000 rpm and (b) 2000 rpm. The images were acquired after sintering at 450°C for 30 min. As seen in these photographs, the severe cracking observed in (a) was caused from the thickness of the TiO_2 layer under a considerable amount of stress, whereas the thinner TiO_2 layer shown in (b) does not crack under the same sintering conditions.

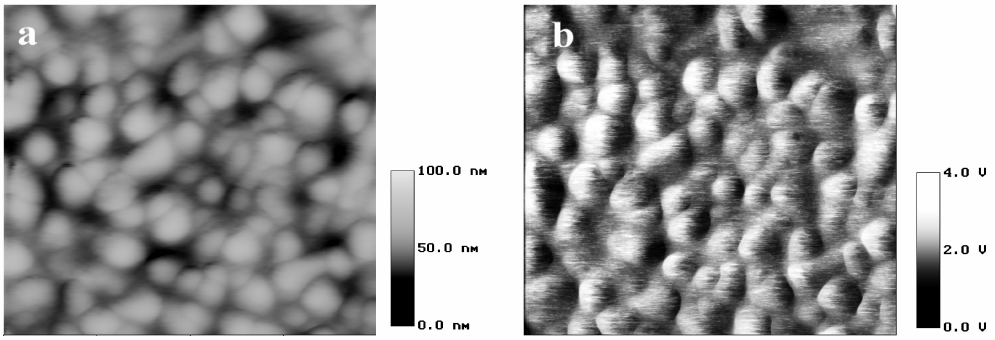

Figure 4.2 Contact mode AFM image of the surface of a low viscosity TiO_2 thin film spun at 1000 rpm and sintered at 450°C for 30 min. (a) topographical image of a 1 μm x 1 μm domain; (b) friction map of the same region.

residual solvent present. On the other hand, if a high viscosity sol-gel was deposited at 1000 rpm and sintered for over 1 hour at 450°C, we observe a drastically different looking surface. First, the film itself fractures (as depicted optically in Figure 4.1). It was of interest to determine whether the film had totally fractured or had simply blistered at the surface of the film. SEM was used to characterize the bulk morphology of the fractured film in parallel, EDX spectroscopy was used to determine elemental composition of the film. Figure 4.3 presents SEM images of a highly fractured TiO_2 film. Close inspection of the image reveals that each of the fractured parts of the film were still

under a considerable amount of stress. This is based on the observation that the middle of each TiO_2 fragment contains a darker region, which most likely represents the portion of the TiO_2 that remains in contact with the native glass. EDX spectra of the cracked TiO_2 (Figure 4.4a) confirmed that the fracturing led to the exposure of the underlying SnO_2:F substrate (Figure 4.4b). This explains why solar cell devices fabricated from films prepared in this manner always failed. This will be discussed shortly. Next, using AFM we investigated the surface morphology of the individual islands composing this fractured film. Circular voids were found in the islands that ranged from 150–400 nm in diameter (Figure 4.5a). These voids could have potentially been generated during the out-gassing of the solvent in the sol-gel. It was also found that the areas between these nanometer-size voids possess surface morphologies that were significantly different (Figure 4.5b) than the morphology of the unstressed film that was cast under optimal conditions (image on the right of Figure 4.2). The morphology that was observed in Figure 4.5b was a highly crystalline lattice that has an average RMS roughness of 0.42 ± 0.22 nm. Others have observed the enhancement of all PV solar cell parameters with an increase in sintering temperature, best results obtained for TiO_2 electrodes sintered at 450^{o}C for 12 hours [10].

Solvent-cast TiO_2 that was spun at 2000 rpm yielded slightly smoother and uniform films (RMS roughness = 7.9 ± 0.8 nm) (Figure 4.6a). The friction map illustrates that a uniform torque is induced on the cantilever (Figure 4.6b). The friction map also demonstrates another interesting point: the cantilever is torqued less when probing this film as opposed to the TiO_2 that was cast at 1000 rpm. A potential explanation for this

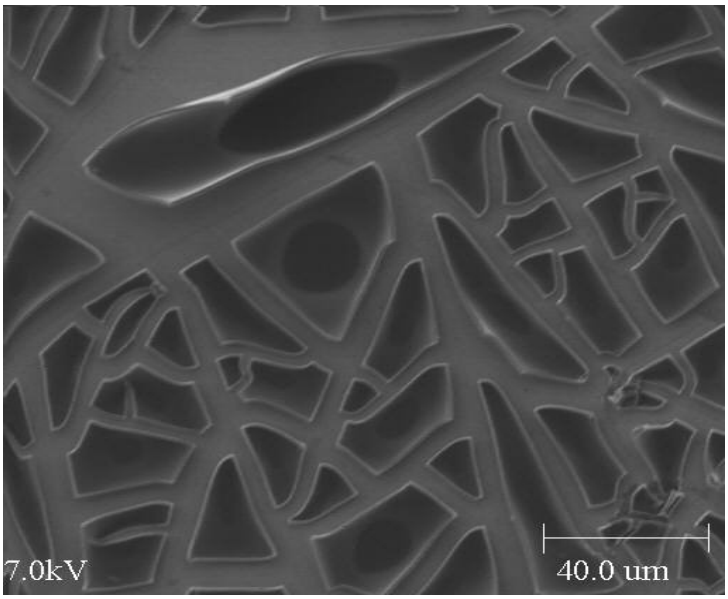

Figure 4.3 SEM image of high viscosity TiO_2 spun at 1000 rpm and sintered for over 1 hour at 450°C. We have concluded that these "islands" of TiO_2 are also stressed and only attached to the underlying glass at the dark regions located near the center of each TiO_2 fragment.

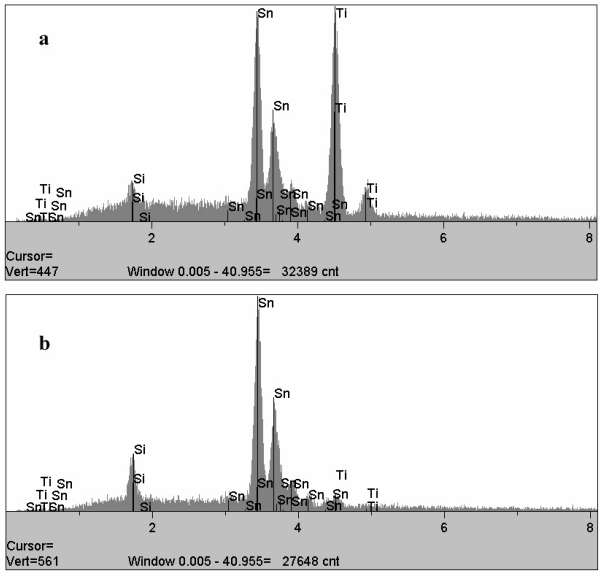

Figure 4.4 EDX spectra of a high viscosity TiO_2 spun at 1000 rpm and sintered for over 1 hour at 450°C. Spectrum (a) was acquired on a TiO_2 island whereas spectrum (b) was acquired between TiO_2 islands.

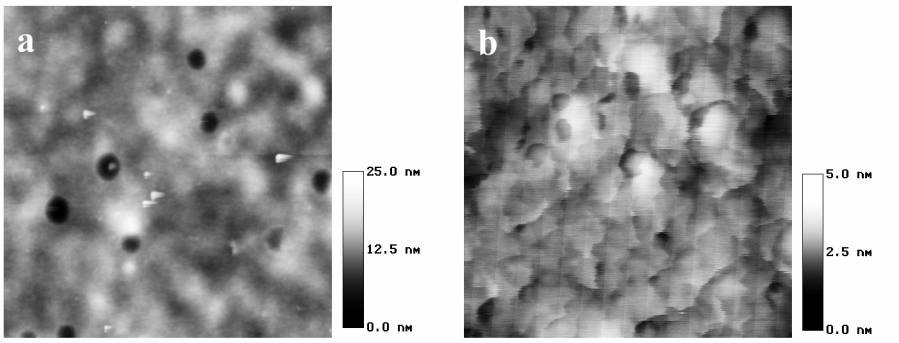

Figure 4.5 Tapping Mode™ AFM images of crystalline TiO_2 islands. (a) 6 μm X 6 μm micrograph that demonstrates the presence of nanoscale pits in the TiO_2 islands. (b) 300 nm x 300 nm micrograph of the smooth area between the circular pits.

could be that since the 1000 rpm film is thicker, it can absorb a higher amount of water than the thinner (2000 rpm) film.

Reduction of the sintering time to 30 minutes produced uniform, flat TiO_2 films without cracking for films with thicknesses less than 70 nm (Figure 4.1b). High-resolution XPS data shown in Figure 4.7 matched those previously reported for anatase TiO_2 [2]. Best device performances (80.0 μA/cm^2, V= 0.693 V) were found with 40 nm TiO_2 films sintered for 30 min; therefore, a defect-free TiO_2 layer acted as an efficient blocking layer. Current-voltage curves acquired with cells made by these procedures have already been published [11]. Additionally, performance versus time measurements have been reported on cells produced in the same manner which have shown that current and voltage measurements improved over time [11].

4.3.2 Polymer Layer Characterization

Sintered TiO_2 films removed from the furnace at 120°C were quickly placed in a P3UBT-chloroform solution to protect the TiO_2 by preventing water absorption onto the film. Devices constructed without protecting the TiO_2 layer failed to produce measurable current or voltage. Sintered TiO_2 films were rapidly placed into heated solutions containing either 0.4 or 4.0 mg/ml P3UBT in chloroform in order to protect the TiO_2 while absorbing the polythiophene into the nanoporous surface. Although the thin P3UBT films absorbed onto the TiO_2 surface were of the desired thickness, they contained polymer aggregates measuring several microns in diameter as seen in the optical microscopy pictures in Figure 4.8.

Next it was necessary to characterize the surface morphology of the P3UBT adsorbed layer. Initially we found that this layer possessed particles that were embedded in the film (Figure 4.9a). AFM topological measurements of the areas between the aggregates (Figure 4.9b) yielded an average RMS roughness of 6.70 ± 0.65 nm. Devices fabricated from polymer films that exhibited these aggregate structures yielded working devices of low efficiencies (2.0 $\mu A/cm^2$, V= 0.25 ± 0.05 V). It is postulated that these aggregates could be penetrating to the TiO_2, which could create a short in the final solar cell device.

Due to the formation of these large aggregates, the P3UBT-chloroform protecting solution was not used to prevent moisture absorption by the TiO_2. Instead, dried chloroform was used as the protecting solvent, while solutions of warm 0.4 and 4.0 mg/ml P3UBT-chloroform were spin-cast at speeds between 1000 and 3000 rpm. It was

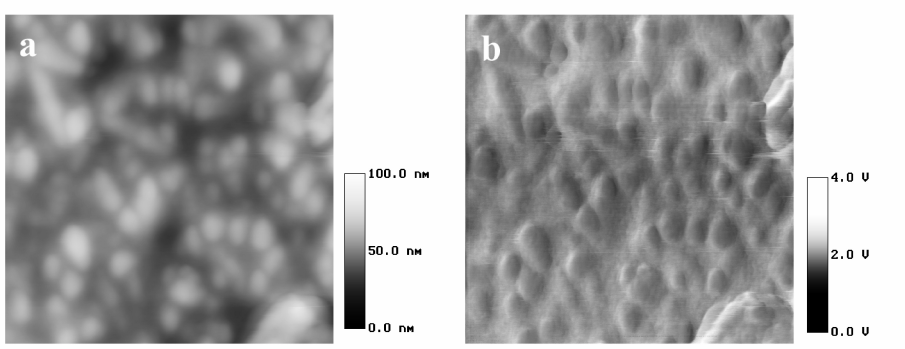

Figure 4.6 AFM images of solvent-cast TiO_2 spun at 2000 rpm and sintered for 30 min. (a) topographical and (b) friction images of the same 1 μm x 1 μm domain.

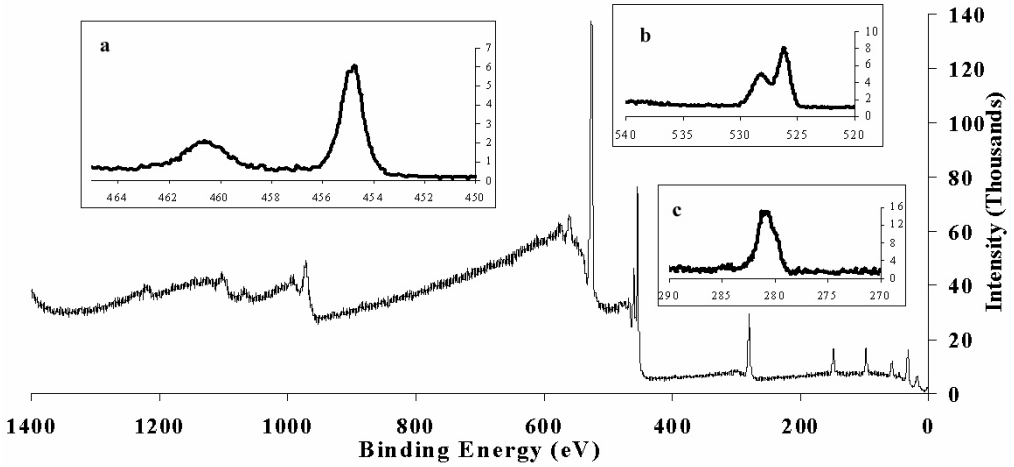

Figure 4.7 XPS survey scan of TiO_2 including (inset): (a) High Res Ti-2p. (b) High Res O-1s. (c) High-Res C-1s.

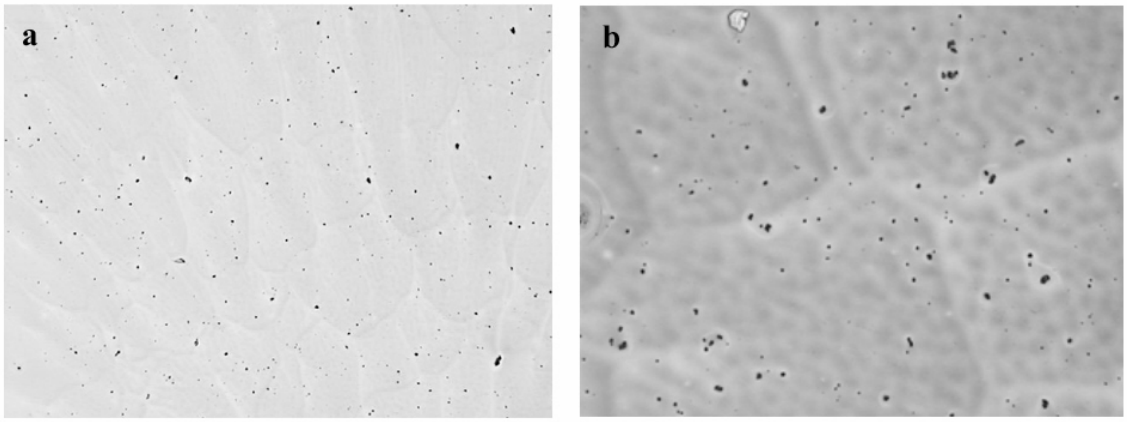

Figure 4.8 Optical microscopy of P3UBT film containing aggregates. The larger image is 5 times the normal magnification, while the smaller image is 20.

found that speeds less than 2000 rpm resulted in films similar to those described for the absorption layers. However, spin speeds of 2000 rpm or greater led to uniform, aggregate-free films able to protect the hydrophilic TiO_2 layer. When uniform spin-cast P3UBT films were achieved, AFM surface analysis yielded an average RMS roughness of 5.26 ± 0.45 nm (Figure 4.10a) and coating of samples was extremely uniform as depicted by the friction image (Figure 4.10b).

P3UBT cast layers were prepared as described in the experimental section. UV-Vis of the polythiophene cast layer exhibited an absorbance of 0.33 ± 0.02 at λ_{max}= 525 nm, while the underlying spin-cast layers displayed an absorbance of only 0.04 at the same wavelength. The data confirms that of previous reports for the P3UBT [10]. It was apparent from this data that the PV device has a sufficient light absorption ability to roughnesses below 3 nm but also possessed areas that were slightly more corrugated and possessed roughnesses of approximately 7 nm. The EDX spectra that were acquired on this final polymer layer (Figure 4.11b) showed a strong sulfur signature which is indicative of the P3UBT layer. PV devices designed from the combination of the best P3UBT and TiO_2 layers resulted in devices that facilitated maximum light absorption by the polymer to create flat solid-state photovoltaic cells with J_{sc}= 55 μA/cm^2 and V_{oc}= 0.8 V.

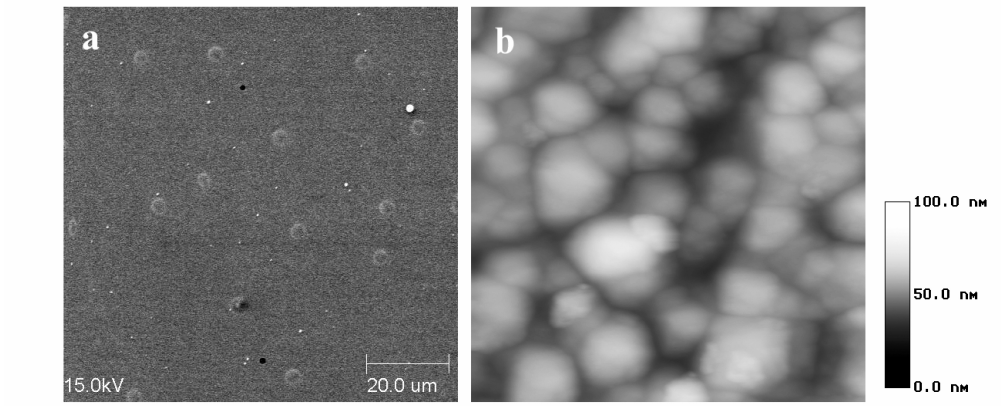

Figure 4.9 (a) SEM image of the P3UBT spin-cast layer spun at 1000 rpm. (b) Tapping Mode^{TM} AFM topographic image of the area between the aggregates (1 μm x 1 μm).

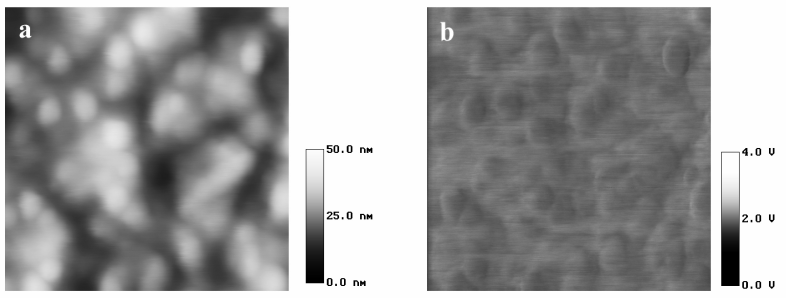

Figure 4.10 AFM Image of a uniform spin-cast P3UBT film. (a) 1 μm x 1 μm topographical image. (b) corresponding friction map (note that there is less frictional contrast than either of the TiO_2 layers).

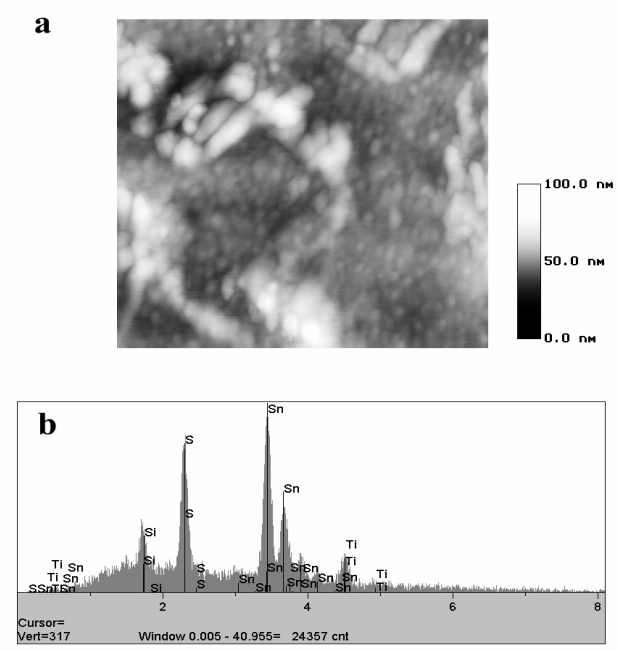

Figure 4.11 (a) 2 μm x 2 μm Tapping Mode^{TM} AFM image of a typical solvent cast P3UBT layer. (b) EDX spectrum of the cast layer.

4.4. Summary, Conclusions, and Future Work

It has been demonstrated that the morphological properties of each layer in an inorganic-organic hybrid solar device strongly influences the overall efficiency of the photovoltaic cell. Each additional layer exhibits a planarizing effect which can only enhance the contact of subsequent layers. Fracture planes and inhomogeneities in the TiO_2 and aggregates in the P3UBT layers lead to PV devices of low efficiency or a total destruction of the electrical output of the PV cell. Surface morphologies can be determined rapidly and easily, although only qualitatively, through optical microscopy in reflection mode at 5 to 20 times magnification, while for quantitative analyses, SEM-EDX and AFM need to be employed. There is still much room left for optimizing the sol-gel and polymer coating processes by systematically and narrowly changing the parameters, such as solution viscosity, spin-rate, and sintering process.

More research is currently being carried out to further elucidate the mechanism(s) that limit the efficiency and electrical output of inorganic-organic hybrid solid-state PV solar cell devices. We have previously explored functionalizing polythiophenes with phosphonate end-groups to achieve better intimate contact between TiO_2 and the polymer [11], while others have recently explored the effect of carboxyl-functionalized polythiophenes in PV devices [14,15]. The functionalized end-groups have led to an improvement in the performance of inorganic-organic hybrid solar cells; therefore, studying the surface morphologies created through the use of such functionalizations has become the focus of our future work.

4.5 References

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CONCLUSION

Our work in the field of polymer and organic semiconductors has taken a look deeper into what drives conductivity through applications in different device structures. We have shown that hole mobility in single crystal pentacene applications can be 2-3 orders of magnitude greater than in the thin film state. This was largely due to the intense purification process of the material to remove defects and grain boundaries, which was leading to decreased charge transport. Through the purification process, we observed the reaction between pentacene and its impurities that produced 2 new polyaromatic hydrocarbons: bisperipentacene and trisperipentacene. The establishment of these compounds enabled us to help explain the mechanism for hydrogen transfer at elevated temperatures, which may help to explain the formation of graphite and other larger polyaromatic hydrocarbons.

While constructing thin film devices for comparison to single crystal devices, we envisioned designing these devices to have the ability for reusable platform for high throughput screening of organic materials. Our goal led us to develop a reusable silicon wafer platform containing 2100 individual gate field-effect transistors of various channel widths and lengths. The devices operated at gate voltages much less than the operating voltage of typical silicon common gate devices. Hole mobilities of the organic and polymer semiconductors were similar to earlier reported common gate devices, but were not the highest values reported. This design structure allows for the ability to measure numerous new organic and polymer semiconductors quickly and easily as well as move into flexible substrates. Future concerns using surface modifications should increase the FEM to that of amorphous silicon, both in pentacene and polythiophenes.

Knowing the mobility of our organic semiconductors, we were able to employee these materials, specifically P3UBT, into an inorganic-organic hybrid solid-state solar cell and measure its efficiency. A correlation was drawn between the thin film properties of the device materials and performance. It was determined that each subsequent layer deposited on the device led to a planarization effect, and that the more planar and pristine the individual layer, the better device performance. P3UBT devices measured 55 μA and V_{OC} of 0.8V.

APPENDIX

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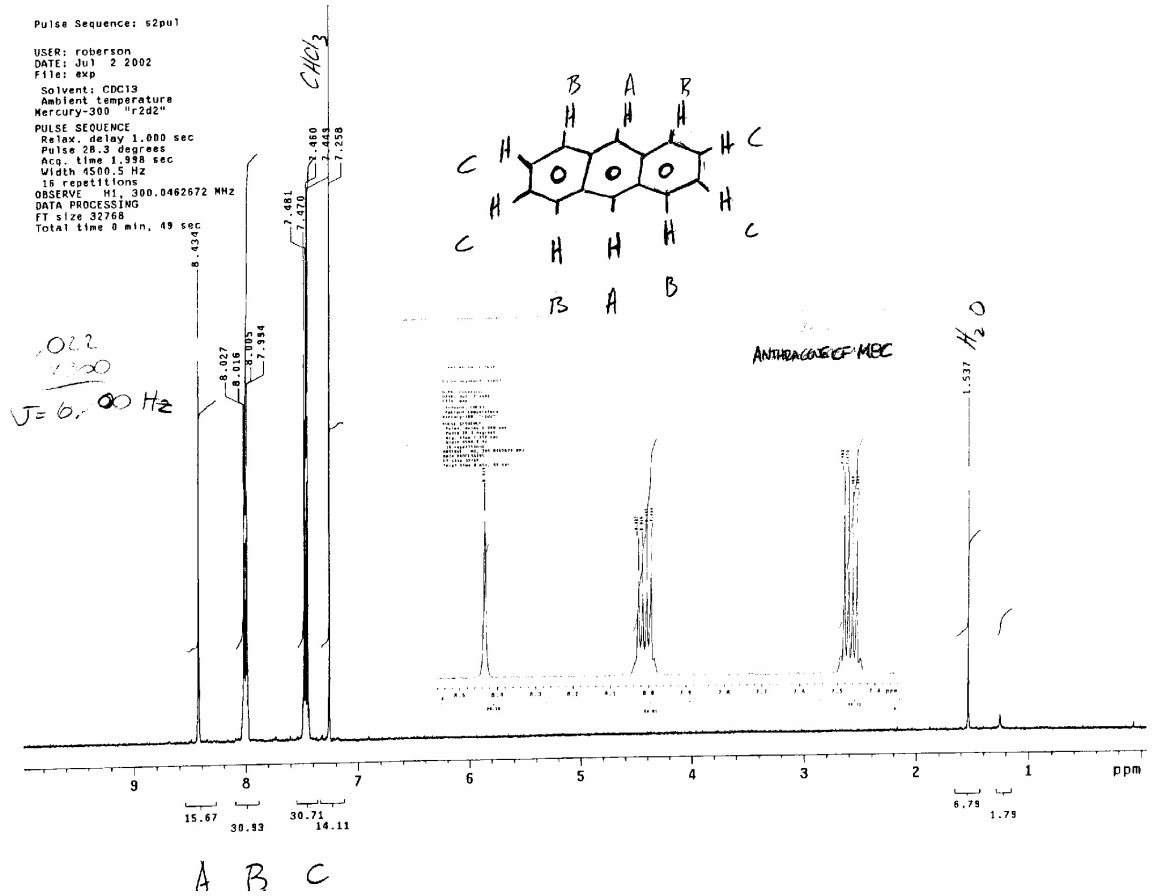
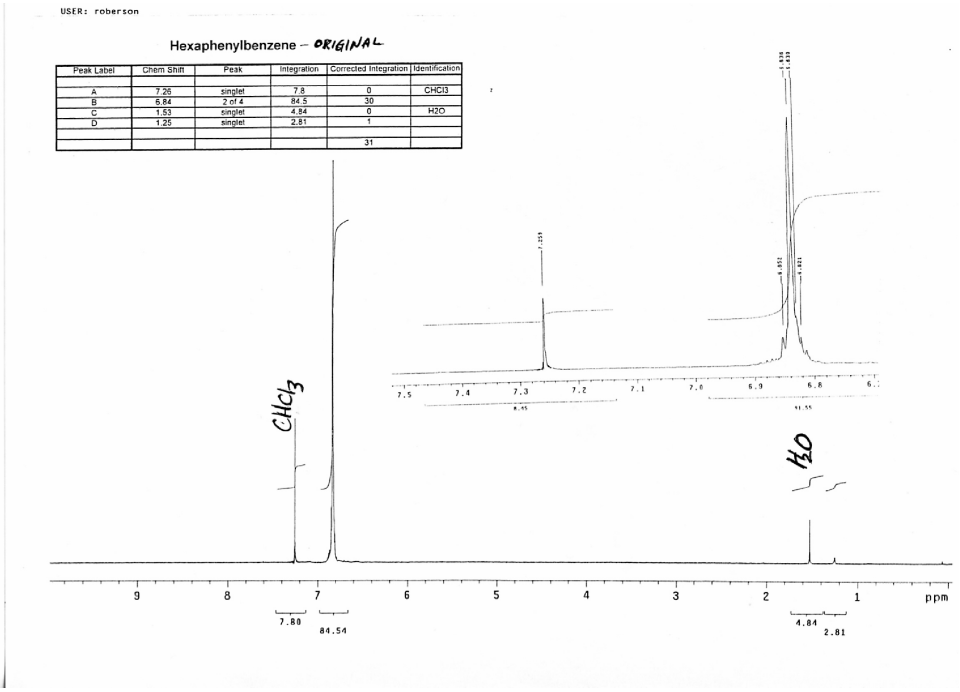
Appendix 2.1 NMR of Purified Anthracene

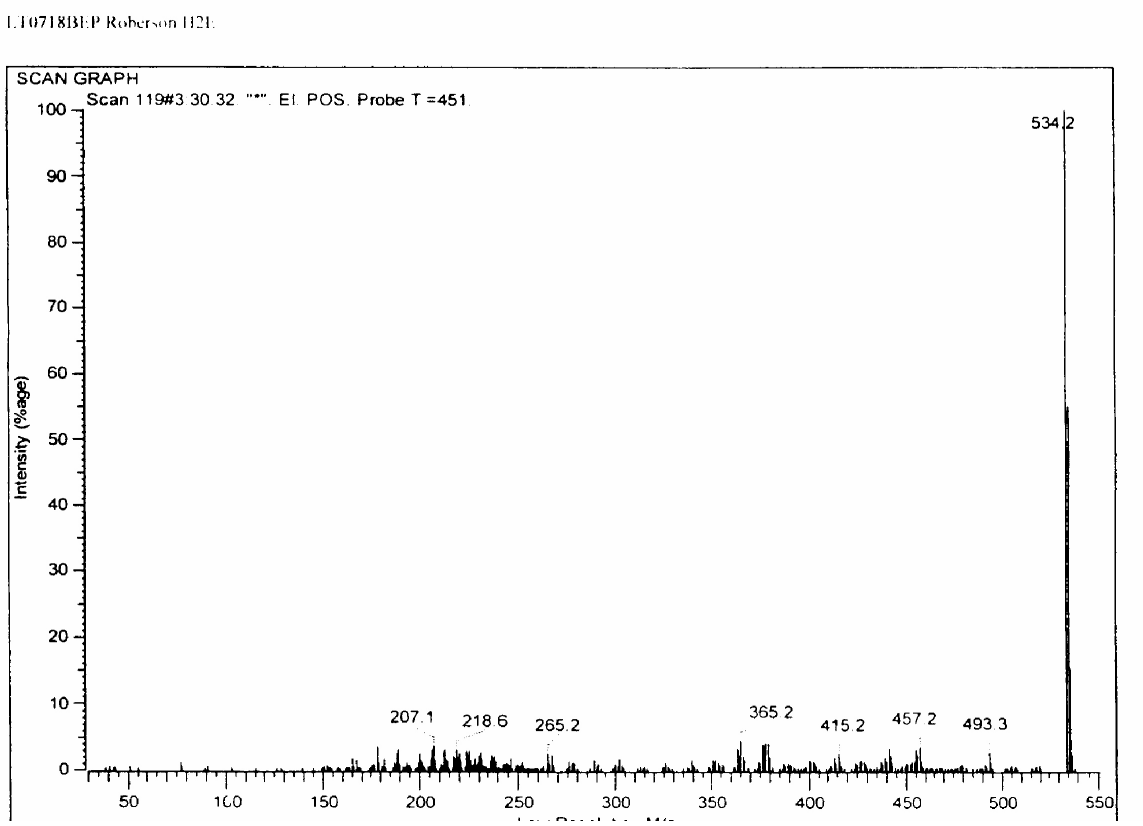


Appendix 2.2 Hexaphenylbenzene characterization data

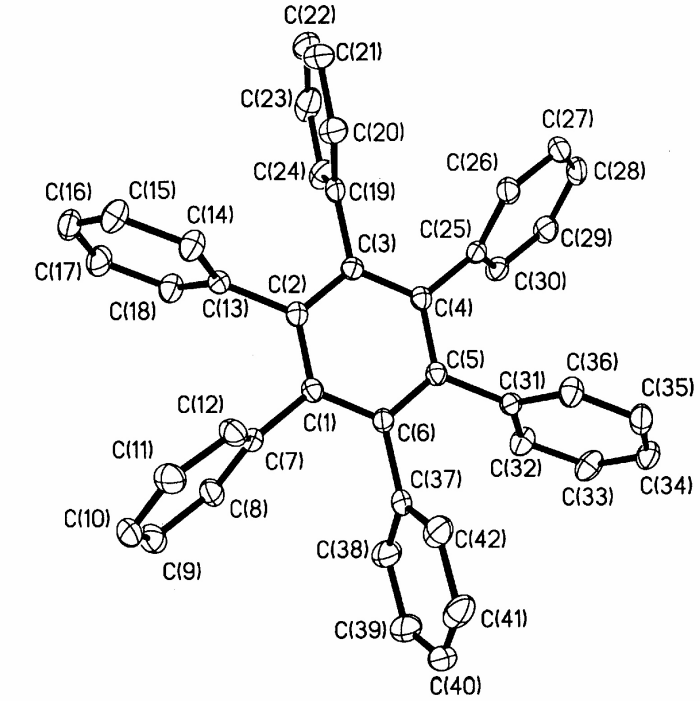
(A) HNMR



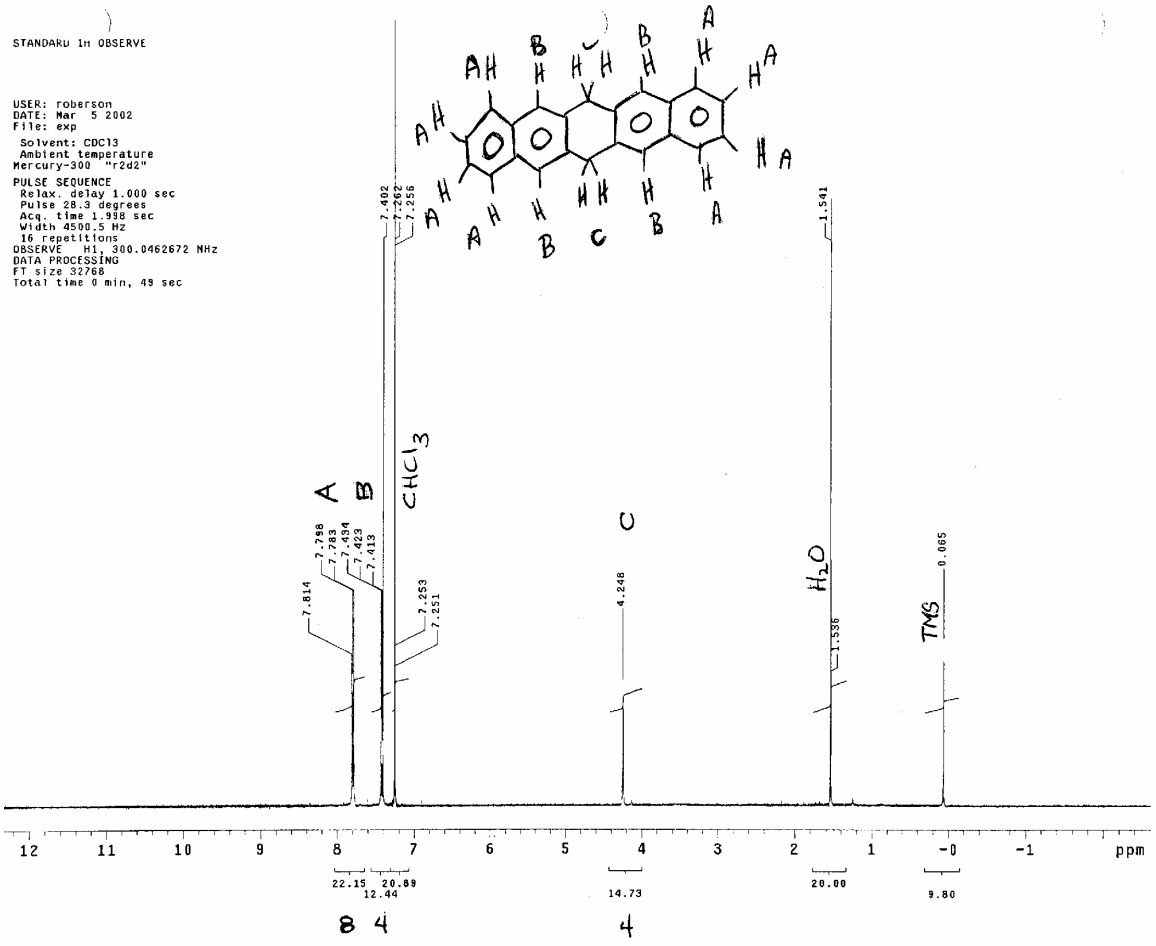
(B) EIMS



(C) Unit cell crystal structure



Appendix 2.3 [1]HNMR data for 6,13-dihydropentacene



Appendix 3.1 Initial Individual Gold Gate OFETs

GT MiRC CMOS Process Run Sheet						
Batch 1: Initial Individual Au Gate OFET						
(um p-type OFET, 4 wafers)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Prime grade Si [100], 500 um thickness, 5.4-6.7 ohm/cm supplied by cleanroom					
2	Piranha clean			CMOS wet bench, SRD	CMOS clean	4/7/2003
3	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, CMOS hotplate	CMOS clean	4/7/2003
4	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 CI2 9s			MA-6, CMOS hotplate	general use	4/7/2003
5	Chlorobenzene soak 20 min, develop w/ MF319 75-90s			glass bowl	general use	4/7/2003
6	Ti/Au deposition	300A Ti / 2000A Au		Ebeam 1, alpha step profilometer	general use	4/7/2003
7	Au liftoff			Bowl of acetone		4/7/2003
8	Gate height measurement	t=2100A		Alpha Step Profilometer	general use	4/15/2003
9	Gate oxidation (cmos3000)	tox ~ 3000A	thickness	STS PECVD	general use	4/23/2003
10	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate	general use	4/24/2003
11	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s CI2			MA-6	general use	5/14/2003
12	Develop with MF319 for 45s			glass bowl		5/14/2003
13	SiO_2 etch	75 sec BOE dip	gate well height	glass bowl	general use	5/14/2003
14	PR strip			Gastonics Asher	general use	5/14/2003
15	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate		5/21/2003
16	Level 3 Photolithography: OFET MASK 3, expose MA-6 9s CI2			MA-6	general use	5/21/2003
17	Chlorobenzene soak 25 min, develop w/ MF319 75-90s			glass bowl	general use	5/21/2003
18	Ti/Au deposition	300A Ti / 2000A Au / 300A Ti		Ebeam 1, alpha step profilometer	general use	5/21/2003
19	Au liftoff			Bowl of acetone		5/21/2003
20	S/D height measurement	t=2600A		Alpha Step Profilometer	general use	6/9/2003
21	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	6/9/2003
22	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8 Spinner, hotplate	general use	6/9/2003
23	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	6/9/2003
24	Develop with MF319 for 45s			glass bowl		6/9/2003
25	Polymer etch in Chlorobenzene	40nm polythiophene		glass bowl	general use	6/9/2003
	Polymer Depositions					
	1-1 P3UBT 5000 rpm, 2500 acc, 30 sec (6/9/2003)					
	1-2 P3UBT 4.0 mg/ml 3000 rpm, 2500 acc, 60 sec (6/17/2003)					
	1-3 P3UBT 4.0 mg/ml cast coated and dried at room temperature (6/17/2003)					
	1-2 Empty device (12/7/2004)					

Appendix 3.2 Initial Individual Poly Gate OFETs

	GT MiRC CMOS Process Run Sheet					
	Batch 2C: Initial Individual Poly Gate OFET					
	(um p-type OFET, 4 Wafers)					
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Prime grade Si [100] wafers supplied by CMOS	4-pt probe measurement	resistivity	4-pt probe	general use	8/30/2004
2	Piranha clean			CMOS wet bench, SRD	CMOS clean	8/30/2004
3	Initial Oxidation (gateox.001) 3 hr 15 min dry ox	tox=985A	thickness	Nitride furnace tube 3, wyko	CMOS clean	8/30/2004
4	Poly-Si deposition	tg = 4500A	thickness	Poly furnace 4, nanospec	CMOS clean	9/3/2004
5	PR deposition (Futurex 3000NP, 4000rpm, 30s) and softbake 150C 90s			RC8, CMOS hotplate	CMOS clean	9/8/2004
6	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 Cl2 3.4s			MA-6, CMOS hotplate	general use	9/8/2004
7	Hardbake 115C 90s, Develop with MF319 45s			CMOS hotplate. Solitek developer	CMOS clean	9/8/2004
8	Poly-Si etch	receipe: Epoly3	etch time = 3 min	STS ICP	CMOS clean	9/20/2004
9	PR strip	overnight		acetone bath	general use	9/20/2004
10	Gate height measurement	t=4500A		Alpha Step Profilometer	general use	10/4/2004
11	Gate oxidation (gateox.001) 950C, 2 hr 45 min dryox	tox = 997A	thickness	Nitride furnace tube 2, nanospec	COMOS clean	10/28/2004
12	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate	general use	8/4/2004
13	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s Cl2			MA-6	general use	8/4/2004
14	Develop with MF319 for 45s			Solitek developer	CMOS clean	8/4/2004
15	SiO_2 etch	90 sec BOE dip	gate well height	CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	11/1/2004
16	PR strip	90 sec O2 plasma		Gastonics Asher	general use	11/1/2004
17	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, CMOS hotplate	general use	11/4/2004
18	Level 3 Photolithography: OFET MASK 3, expose MA-6 9s Cl2			MA-6	general use	11/4/2004
19	Chlorobenzene soak 20 min, develop w/ MF319 75-90s			Solitek developer	general use	11/4/2004
20	Ti/Au/Ti S/D deposition, liftoff in acetone	300A Ti / 2000A Au/300A Ti	thickness	Ebeam 1, alpha step profilometer	general use	11/4/2004
21	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	11/10/2004
22	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8 Spinner, hotplate	general use	11/10/2004
23	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s Cl2			MA-6	general use	11/10/2004
24	Develop with MF319 for 45s			glass bowl		11/10/2004
25	Polymer etch in Chlorobenzene			glass bowl, 20 sec	general use	11/10/2004

Appendix 3.3 Shadowmask devices

	GT MiRC CMOS Process Run Sheet					
	Batch 3: Common Gate Shadowmask OFETs					
	(mm p-type OFET, 2 wafers)					
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Sb-doped n-type Si [111], 470 um thickness, 5.4-6.7 ohm/cm purchased from WaferNet	4-pt probe measurement	resistivity	4-pt probe	general use	3/1/2005
2	Piranha clean			CMOS wet bench, SRD	CMOS clean	3/1/2005
3	Initial Oxidation (dryoxcon) 950C 46 min	tox=975A	thickness	Nitride furnace tube 3, nanospec, SCA	CMOS clean	3/1/2005
4	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	3/3/2005
5	Backside SiO_2 etch	1 min BOE dip		CMOS wet bench, SRD, alpha step profilometer	CMOS clean	3/3/2005
6	PR strip	Gastonics Asher	1 min	Gastonic Asher	general use	3/3/2005
7	Polymer deposition (1000 rpm 60 sec)	40nm polythiophene		RC-8 spinner	general use	3/3/2005
8	Ti/Au deposition	30A Ti/ 1000A Au	s/d height	Ebeam 1	general use	3/3/2005

Appendix 3.4 Individual Poly Gate OFETs

	GT MiRC CMOS Process Run Sheet					
	Batch 4: CMOS Individual Poly Gate OFET					
	(um p-type OFET, 2 Wafers)					
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Sb-doped n-type Si [111], 470 um thickness, 5.4-6.7 ohm/cm purchased from WaferNet	4-pt probe measurement	resistivity	4-pt probe	general use	
2	Initial Oxidation (iniwetox.003) 1100C	tox=1000A	thickness	Nitride furnace tube 3, nanospec	CMOS clean	
3	Poly-Si deposition	tg=1184A	thickness	Poly furnace 4, nanospec	CMOS clean	
4	Doping (ndopcom.001) for 8 min then anneal for 15 min at 900C	Targeting Rs = 100ohm	resistivity	Nitride furnace tube 1, 4-pt probe	CMOS clean	3/2/2005-3/4/2005
5	Phosphorus glass removal (BOE dip)	wafer surface uniform in color	color: light yellow	CMOS wet bench, SRD	CMOS clean	3/4/2005
6	PR deposition (Futurex 3000NP, 4000rpm, 30s) and softbake 150C 90s			RC8, CMOS hotplate	CMOS clean	3/8/2005
7	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 Cl2 3.4sec			MA-6, CMOS hotplate	general use	3/8/2005
8	Hardbake 115C 90s, Develop with MF319 45s			CMOS hotplate. Solitek developer	CMOS clean	3/8/2005
9	Poly-Si etch		etch time = 1 min	STS ICP	CMOS clean	3/8/2005
10	PR strip		etch time = 1 min	Gastonics Asher	general use	3/8/2005
11	Gate height measurement	t=1900A		Alpha Step Profilometer	general use	3/24/2005
12	Piranha clean and RCA clean			CMOS wet bench, SRD		3/24/2005
13	Gate oxidation (gateoxHH.003) 950C, 90 min dryox	tox=800A	thickness	Nitride furnace tube 3, nanospec	COMOS clean	3/24/2005
14	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, CMOS hotplate	CMOS clean	3/28/2005
15	Level 3 Photolithography: OFET MASK 3, expose MA-6 3.4s Cl2			MA-6	general use	3/28/2005
16	Chlorobenzene soak 25 min, develop in MF319			Solitek developer	CMOS clean	3/28/2005
17	Ti/Au S/D deposition, liftoff in acetone	300A Ti / 2000A Au	thickness	Ebeam 1, alpha step profilometer	general use	3/28/2005
18	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate	general use	4/4/2005
19	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s Cl2			MA-6	general use	4/4/2005
20	Develop with MF319 for 45s			glass bowl		4/4/2005
21	SiO_2 etch	75 sec BOE dip	gate well height	quartz tank, profilometer	general use	4/5/2005
22	PR strip	112A stripper, 60C overnight		plastic bowl	general use	4/5/2005
23	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	
24	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8 Spinner, hotplate	general use	
25	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s Cl2			MA-6	general use	
26	Develop with MF319 for 45s			Solitek developer		
27	Polymer etch in Chlorobenzene	40nm polythiophene		glass bowl	general use	

Appendix 3.5 Individual Poly Gate OFETs

	GT MiRC CMOS Process Run Sheet					
	Batch 5: Super Clean CMOS Individual Poly Gate OFET					
	(um p-type OFET, 3 Wafers)					
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	New green boat			SRD (2)		3/24/2005
2	Sb-doped n-type Si [111], 470 um thickness, 5.4-6.7 ohm/cm purchased from WaferNet	4-pt probe measurement	resistivity	4-pt probe	general use	3/24/2005
3	Piranha clean			CMOS wet bench, SRD	CMOS clean	3/24/2005
4	Initial Oxidation (gateoxHH.003) 950C, 90 min run time	tox=700A	thickness	Nitride furnace tube 3, nanospec	CMOS clean	3/24/2005
5	Poly-Si deposition	tg ~ 1000A	thickness	Poly furnace 4, nanospec	CMOS clean	3/28/2005
6	Doping (ndopcom.001) for 8 min then anneal for 15 min at 900C	Targeting Rs = 100ohm	resistivity	Nitride furnace tube 1, 4-pt probe	CMOS clean	3/28/2005-3/30/2005
7	Phosphorus glass removal (BOE dip)	wafer surface uniform in color	color: light yellow	CMOS wet bench, SRD	CMOS clean	3/31/2005
8	PR deposition (Futurex 3000NP, 4000rpm, 30s) and softbake 150C 90s			RC8, CMOS hotplate	CMOS clean	3/31/2005
9	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 Cl2 3.4s			MA-6, CMOS hotplate	general use	3/31/2005
10	Hardbake 115C 90s, Develop with MF319 45s			CMOS hotplate. Solitek developer	CMOS clean	3/31/2005
11	Poly-Si etch		etch time = 1 min	STS ICP	CMOS clean	3/31/2005
12	PR strip			acetone bath	general use	3/31/2005
13	Gate height measurement	t=1900A		Alpha Step Profilometer	general use	3/31/2005
14	Piranha clean and RCA clean			CMOS wet bench, SRD	CMOS clean	3/31/2005
15	Gate oxidation (gateoxHH.003) 950C, 90 min dryox	tox ~ 1000A	thickness	Nitride furnace tube 3, nanospec	COMOS clean	4/1/2005
16	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate	general use	4/4/2005
17	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s Cl2			MA-6	general use	4/4/2005
18	Develop with MF319 for 45s			Solitek developer	CMOS clean	4/4/2005
19	SiO_2 etch	75 sec BOE dip	gate well height	CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	4/5/2005
20	PR strip	1112A Stripper, 60C overnight		plastic bowl	general use	4/5/2005
21	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, CMOS hotplate	general use	4/7/2005
22	Level 3 Photolithography: OFET MASK 3, expose MA-6 3.4s Cl2			MA-6	general use	4/7/2005
23	Chlorobenzene soak 25 min, develop w/ MF319 75-90s			Solitek developer	general use	4/7/2005
24	Ti/Au/Ti S/D deposition, liftoff in acetone	300A Ti / 2000A Au/300A Ti	thickness	Ebeam 1, alpha step profilometer	general use	4/7/2005
25	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	4/19/2005
26	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8 Spinner, hotplate	general use	4/19/2005
27	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s Cl2			MA-6	general use	4/19/2005
28	Develop with MF319 for 45s			glass bowl		4/19/2005
29	Polymer etch in Chlorobenzene			glass bowl, 20 sec	general use	4/19/2005
	Polymer Depositions					
	Batch 5 Wafer 1 Deposision A : Spin 4.0 mg/ml P3HT in HPLC grade 1,2-dichlorobenzene at 3000 rpm at 500 rpm acc for 60 sec, baked at 110C for 5 min (4/19/05)					
	Batch 5 Wafer 2 Deposision A : Cast 2ml of 4.0 mg/ml P3HT in HPLC grade 1,2-dichlorobenzene and dried on a hotplate at 110C for 10 min					
	Batch 5 Wafer 1 Deposision B : Spin 2ml of 4.0 mg/ml P3UBT in HPLC grade 1,2-dichlorobenzene and dried on a hotplate at 110C for 10 min followed by a 24 hr bake in vac oven at 60C and 10-3 torr					
	Batch 5 Wafer 1 and 2 Deposision C: Spin 2ml of 4.0 mg/ml P3HT in HPLC grade 1,2-dichlorobenzene and dried on a hotplate at 110C for 2 min followed by a 24 hr bake in vac oven at 60C and 10-3 torr (6/10/05)					

Appendix 3.6 Common gate OFETs

GT MiRC CMOS Process Run Sheet						
Batch 6: CMOS Common Gate OFET						
(mm p-type OFET, 1 wafer)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Sb-doped n-type Si [111], 470 um thickness, 5.4-6.7 ohm/cm purchased from WaferNet	4-pt probe measurement	resistivity	4-pt probe	general use	3/28/2005
2	Piranha clean			CMOS wet bench, SRD	CMOS clean	3/28/2005
3	Initial Oxidation (gateoxHH.003) 950C 90 min	tox=800A	thickness	Nitride furnace tube 3, nanospec, SCA	CMOS clean	3/28/2005
4	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	4/13/2005
5	Ti/Au deposition	300A Ti/ 3000A Au	s/d height	Ebeam 1	general use	4/13/2005
6	Dicing				MIRC staff	4/14/2005

Appendix 3.7 Individual Gold Gate OFETs

GT MiRC CMOS Process Run Sheet						
Batch 7: CMOS Individual Au Gate OFET						
(um p-type OFET, 2 wafers)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Prime grade Si [100], 500 um thickness, 5.4-6.7 ohm/cm supplied by cleanroom (Chris)	4-pt probe measurement	resistivity	4-pt probe, SCA	general use	3/24/2005
2	Initial Oxidation (gateoxHH.003) 950C, 90 min run time	tox=700A	thickness	Nitride furnace tube 3, nanospec, SCA	CMOS clean	3/24/2005
3	Piranha clean			CMOS wet bench, SRD	CMOS clean	3/28/2005
4	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, CMOS hotplate	CMOS clean	3/28/2005
5	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 Cl2 9s			MA-6, CMOS hotplate	general use	3/28/2005
6	Chlorobenzene soak 20 min, develop w/ MF319 75-90s			glass bowl	general use	3/28/2005
7	Ti/Au deposition	300A Ti / 2000A Au		Ebeam 1, alpha step profilometer	general use	3/28/2005
8	Au liftoff			Bowl of acetone		3/28/2005
9	Gate height measurement	t=2300A		Alpha Step Profilometer	general use	3/28/2005
10	Gate oxidation (cmos3000)	tox ~ 3000A	thickness	STS PECVD	general use	3/28/2005
11	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate	general use	4/5/2005
12	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s Cl2			MA-6	general use	4/5/2005
13	Develop with MF319 for 45s			glass bowl		4/5/2005
14	SiO_2 etch	75 sec BOE dip	gate well height	glass bowl	general use	4/5/2005
15	PR strip	1112A stripper, 60C overnight		plastic bowl	general use	4/5/2005
16	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate		4/7/2005
17	Level 3 Photolithography: OFET MASK 3, expose MA-6 9s Cl2			MA-6	general use	4/7/2005
18	Chlorobenzene soak 25 min, develop w/ MF319 75-90s			glass bowl	general use	4/7/2005
19	Ti/Au deposition	300A Ti / 2000A Au / 300A Ti		Ebeam 1, alpha step profilometer	general use	4/7/2005
20	Au liftoff			Bowl of acetone		4/7/2005
21	S/D height measurement	t=2600A		Alpha Step Profilometer	general use	
22	Polymer deposition*	40nm polythiophene		RC-8 spinner	general use	4/19/2005
23	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8 Spinner, hotplate	general use	4/19/2005
24	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s Cl2			MA-6	general use	4/19/2005
25	Develop with MF319 for 45s			glass bowl		4/19/2005
26	Polymer etch in Chlorobenzene	40nm polythiophene		glass bowl	general use	4/19/2005
*	Batch 7 Wafer 1 Deposision A : Spin 0.8 ml 4.0 mg/ml P3HT in HPLC grade 1,2-dichlorobenzene at 3000 rpm at 500 rpm acc for 60 sec, baked at 110C for 5 min					

Appendix 3.8 Individual Poly Gate OFETs

GT MiRC CMOS Process Run Sheet						
Batch 8: Super Clean CMOS Individual Poly Gate OFET						
(um p-type OFET, 6 Wafers, 3000A gate ox)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	New green boat			SRD (2)		5/16/2005
2	Prime grade Si [100] wafers supplied by CMOS	4-pt probe measurement	resistivity	4-pt probe	general use	5/16/2005
3	Piranha clean			CMOS wet bench, SRD	CMOS clean	5/16/2005
4	Initial Oxidation (gateoxHH.003) 950C, 90 min run time	tox=800A	thickness	Nitride furnace tube 3, nanospec	CMOS clean	5/16/2005
5	Poly-Si deposition	tg ~ 1900A	thickness	Poly furnace 4, nanospec	CMOS clean	5/18/2005
6	Doping (ndopcom.001) for 15 min then anneal for 15 min at 900C	Targeting Rs = 100ohm	resistivity	Nitride furnace tube 1, 4-pt probe	CMOS clean	5/19/2005
7	Phosphorus glass removal (BOE dip)	wafer surface not uniform in color	color: green to light yellow	CMOS wet bench, SRD	CMOS clean	5/24/2005
8	PR deposition (Futurrex 3000NP, 4000rpm, 30s) and softbake 150C 90s			RC8, CMOS hotplate	CMOS clean	5/24/2005
9	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 Cl2 3.4s			MA-6, CMOS hotplate	general use	5/24/2005
10	Hardbake 115C 90s, Develop with MF319 45s			CMOS hotplate. Solitek developer	CMOS clean	5/24/2005
11	Poly-Si etch		etch time = 2 min	STS ICP	CMOS clean	5/24/2005
12	PR strip			acetone bath	general use	5/24/2005
13	Gate height measurement	t=1900A		Alpha Step Profilometer	general use	5/24/2005
14	Piranha clean and RCA clean			CMOS wet bench, SRD	CMOS clean	5/25/2005
15	Gate oxidation (gateoxHH.003) 950C, 7 hr 42 min dryox	tox ~ 3000A	thickness	Nitride furnace tube 3, nanospec	COMOS clean	5/25/2005
16	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, hotplate	general use	5/28/2005
17	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s Cl2			MA-6	general use	5/28/2005
18	Develop with MF319 for 45s			Solitek developer	CMOS clean	5/28/2005
19*	SiO_2 etch	3 min BOE dip	gate well height	CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	5/28/2005
20	PR strip	Gastonics Asher	1 min	Gastonic Asher	general use	5/28/2005
21	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8, CMOS hotplate	general use	5/30/2005
22	Level 3 Photolithography: OFET MASK 3, expose MA-6 3.4s Cl2			MA-6	general use	5/30/2005
23	Chlorobenzene soak 20 min, develop w/ MF319 30-45s			Solitek developer	general use	5/30/2005
24	Ti/Au/Ti S/D deposition, liftoff in acetone	50A Ti / 2000A Au	thickness	Ebeam 1, alpha step profilometer	general use	5/30/2005
25	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	5/31/2005
26	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 90s			RC8 Spinner, hotplate	general use	5/31/2005
27	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s Cl2			MA-6	general use	5/31/2005
28	Develop with MF319 for 45s			glass bowl		5/31/2005
29	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	5/31/2005
30	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	6/1/2005
	Batch 8 Wafer 1 Deposision A : Spin 4.0 mg/ml P3UBT in HPLC grade 1,2-dichlorobenzene at 3000 rpm at 500 rpm acc for 60 sec					
	Batch 8 Wafer 2 Deposision A : Spin 4.0 mg/ml P3UBT in HPLC grade 1,2-dichlorobenzene at 3000 rpm at 500 rpm acc for 60 sec					
	19*	8-1 has 3000A gate ox				
		8-2 has 2000A gate ox, 1000A blanket etch with BOE then dump rinse and SRD				
	Note: Both 8-1 and 8-2 failed testing. This was due to chlorine contamination causing charging in the gateox layer. The chlorine came from running a wetox prior to the dryox run without performing a tubeclean. For all following batches, a new Tubeclean step was added which is mandatory for metal and chlorine removal.					

Appendix 3.9 Individual Poly Gate OFETs

GT MiRC CMOS Process Run Sheet Batch 9: Super Clean CMOS Individual Poly Gate OFET (um p-type OFET, 2 Wafers, 2000A gate ox)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Same green boat			SRD (2)		6/3/2005
2	Prime grade Si [100] wafers supplied by CMOS	4-pt probe measurement	resistivity	4-pt probe	general use	6/3/2005
3	Piranha clean			CMOS wet bench, SRD	CMOS clean	6/4/2005
4	Initial Oxidation (gateoxHH.00) 950C, 90 min run time	tox=800A	thickness	Nitride furnace tube 3, nanospec	CMOS clean	6/4/2005
5	Poly-Si deposition (run twice due to machine error)	tg ~ 2000A	thickness	Poly furnace 4, nanospec	CMOS clean	6/5/2005
6	Doping (PYPREDOP.001) for 60 min then anneal for 15 min at 900C	Rs = 47ohm/sq	resistivity	Nitride furnace tube 1, 4-pt probe	CMOS clean	6/7/2005
7	Phosphorus glass removal (BOE dip)	wafer surface uniform in color	color: light yellow	CMOS wet bench, SRD	CMOS clean	6/8/2005
8	PR deposition (Futurrex NR7-1500P, 3000rpm, 30s, acc=1000) and softbake 100C 60s			RC8, CMOS hotplate	CMOS clean	6/8/2005
9	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 CI1 7s (intensity=4.5)			MA-6, CMOS hotplate	general use	6/8/2005
10	Hardbake 115C 75s, Develop with MF319 30s			CMOS hotplate. Solitek developer	CMOS clean	6/8/2005
11	Poly-Si etch		etch time = 8 cycles of 48s/cycle	STS ICP	CMOS clean	6/8/2005
12	PR strip		1 min	Gastonic Asher	general use	6/9/2005
13	Gate height measurement	t=4300A		Alpha Step Profilometer, Woolam Elipsometer	general use	6/9/2005
14	Furnace Tube Clean (tubeclean.00)	9 hr tube clean		Nitride Furnace 3	CMOS clean	6/9/2005
15	Piranha clean and RCA clean			CMOS wet bench, SRD	CMOS clean	6/10/2005
16	Gate oxidation (gateoxHH.00) 950C, 4 hr 40 min hr dryox	tox ~ 2000A	thickness	Nitride furnace tube 3, nanospec, SCA	CMOS clean	6/10/2005
17	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, hotplate	general use	6/15/2005
18	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s CI2			MA-6	general use	6/15/2005
19	Develop with MF319 for 45s			Solitek developer	CMOS clean	6/15/2005
20	SiO_2 etch	2 min BOE dip then 3 min BOE dip	gate well height	CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	6/15/2005-6/16/2005
21	PR strip	Gastonics Asher	1 min	Gastonic Asher	general use	6/15/2005
22	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	6/16/2005
23	Level 3 Photolithography: OFET MASK 3, expose MA-6 8.0s CI2			MA-6	general use	6/16/2005
24	Chlorobenzene soak 20 min, develop w/ MF319 30-45s			Solitek developer	general use	6/16/2005
25	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 5000A Au	thickness	Ebeam 1, alpha step profilometer	general use	6/16/2005
26	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	6/17/2005
27	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	6/17/2005
28	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	6/17/2005
29	Develop with MF319 for 45s			glass bowl		6/17/2005
30	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	6/17/2005
31	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	6/20/2005
	Polymer Depositions					
	Batch 9 Wafer 1 Deposision A: Spin 2ml of 4.0 mg/ml P3UBT in HPLC grade 1,2-dichlorobenzene and dried on a hotplate at 110C for 10 min followed by a 24 hr bake in vac oven at 60C and 10-3 torr					
	Batch 9 Wafer 2 Deposision A: Spin 2ml of 4.0 mg/ml P3HT in HPLC grade 1,2-dichlorobenzene and dried on a hotplate at 110C for 10 min followed by a 24 hr bake in vac oven at 60C and 10-3 torr					

Appendix 3.10 Individual Poly Gate OFETs

GT MiRC CMOS Process Run Sheet						
Batch 10: Super Clean CMOS Individual Poly Gate OFET						
(um p-type OFET, 4 Wafers, 2000A gate ox)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Same green boat			SRD (2)		6/12/2005
2	Prime grade Si [100] wafers supplied by CMOS	4-pt probe measurement	resistivity	4-pt probe	general use	6/12/2005
3	Piranha clean			CMOS wet bench, SRD	CMOS clean	6/12/2005
4	Initial Oxidation (gateoxHH.00) 950C, 90 min run time	tox=900A	thickness	Nitride furnace tube 3, nanospec	CMOS clean	6/12/2005
5	Poly-Si deposition	tg ~ 2000A	thickness	Poly furnace 4, nanospec	CMOS clean	6/14/2005
6	Doping (PYPREDOP.001) for 30 min then anneal for 30 min at 900C	Rs = 39 ohm/sq	resistivity	Nitride furnace tube 1, 4-pt probe	CMOS clean	6/16/2005
7	Phosphorus glass removal (BOE dip)	wafer surface= uneven color	color: fades pink to green	CMOS wet bench, SRD	CMOS clean	6/17/2005
8	PR deposition (Futurrex NR7-1500P, 3000rpm, 30s, acc=1000) and softbake 100C 60s			RC8, CMOS hotplate	CMOS clean	6/17/2005
9	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 CI1 7s (intensity=4.5)			MA-6, CMOS hotplate	general use	6/17/2005
10	Hardbake 115C 75s, Develop with MF319 30s			CMOS hotplate. Solitek developer	CMOS clean	6/17/2005
11	Poly-Si etch		etch time = 2 cycles of EricPoly @ 200W	STS ICP	CMOS clean	6/17/2005
12	PR strip		1 min	Gastonic Asher	general use	6/17/2005
13	Gate height measurement	t= 2000 A		Alpha Step Profilometer, Woolam Elipsometer	general use	6/20/2005
14	Piranha clean and RCA clean			CMOS wet bench, SRD	CMOS clean	6/20/2005
15	Gate oxidation (gateoxHH.00) 950C, 4 hr 40 min hr dryox	tox ~ 2000A	thickness	Poly furnace tube, nanospec, SCA	CMOS clean	6/20/2005
16	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, hotplate	general use	6/21/2005
17	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s CI2			MA-6	general use	6/21/2005
18	Develop with MF319 for 45s			Solitek developer	CMOS clean	6/21/2005
19	SiO_2 etch	2 min BOE dip	gate well height	CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	6/21/2005
20	PR strip	Gastonics Asher	1 min	Gastonic Asher	general use	6/21/2005
21	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	
22	Level 3 Photolithography: OFET MASK 3, expose MA-6 3.4s CI2			MA-6	general use	
23	Chlorobenzene soak 20 min, develop w/ MF319 30-45s			Solitek developer	general use	
24	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 4000A Au	thickness	Ebeam 1, alpha step profilometer	general use	
25	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	
26	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	
27	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	
28	Develop with MF319 for 45s			glass bowl		
29	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	
30	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	
	Note: Batch 10 was not completed, but was still good.					

Appendix 3.11 Individual Au Gate OFETs on PET substrate

GT MiRC CMOS Process Run Sheet						
Batch 11: Individual Au Gate OFET on PET						
(um p-type OFET, 2 Wafers, 2000A SiN dielectric)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Coated PET substrate	4-pt probe measurement	resistivity	4-pt probe	general use	6/1/2005
2	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	6/20/2005
3	Level 1 Lithography: Au gate: OFET MASK 1, expose MA-6 CI2 8.0s			MA-6, CMOS hotplate	general use	6/20/2005
4	Chlorobenzene soak 20 min, develop w/ MF319 30-45s			Solitek developer	general use	6/20/2005
5	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 2000A Au	thickness	Ebeam 1, alpha step profilometer	general use	6/20/2005
6	Gate oxidation SiN PECVD	tox ~ 2000A	thickness	Uniaxis PECVD	general use	6/22/2005
7	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, hotplate	general use	6/23/2005
8	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s CI2			MA-6	general use	6/23/2005
9	Develop with MF319 for 45s			Solitek developer	general use	6/23/2005
10	SiN etch	RIE CHF3 45 sccm/O2 5 sccm	gate well height	RIE, alpha step profilometer	general use	6/23/2005
11	PR strip	Acetone wash		wet bench	general use	6/23/2005
12	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	6/27/2005
13	Level 3 Photolithography: OFET MASK 3, expose MA-6 3.4s CI2			MA-6	general use	6/27/2005
14	Chlorobenzene soak 20 min, develop w/ MF319 30-45s			Solitek developer	general use	
15	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 2000A Au	thickness	Ebeam 1, alpha step profilometer	general use	
16	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	
17	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	
18	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	
19	Develop with MF319 for 45s			glass bowl	general use	
20	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	
21	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	

Appendix 3.12 Common Gate OFETs with level 2 lithography

GT MiRC CMOS Process Run Sheet						
Batch 12: Super Clean CMOS Common Gate OFET						
(um p-type OFET, 2 Wafers, 2000A gate ox)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Same green boat			SRD (2)		6/23/2005
2	Sb-doped n-type Si [111], 470 um thickness, 5.4-6.7 ohm/cm purchased from WaferNet	4-pt probe measurement	resistivity	4-pt probe	general use	6/23/2005
3	Piranha clean and RCA clean			CMOS wet bench, SRD	CMOS clean	6/23/2005
4	Gate oxidation (PADOX.001) 950C, 11 hr 30 min hr dryox	tox ~ 2000A	thickness	Poly furnace tube 2, nanospec, SCA	CMOS clean	6/23/2005
5	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, hotplate	general use	6/25/2005
6	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s CI2			MA-6	general use	6/25/2005
7	Develop with MF319 for 45s			Solitek developer	CMOS clean	6/25/2005
8	SiO_2 etch	2 min BOE dip then 3 min BOE dip	gate well height	CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	6/25/2005
9	PR strip	Gastonics Asher	1 min	Gastonic Asher	general use	6/25/2005
10	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	6/25/2005
11	Level 3 Photolithography: OFET MASK 3, expose MA-6 8.0s CI2			MA-6	general use	6/25/2005
12	Chlorobenzene soak 20 min, develop w/ MF319 30-45s			Solitek developer	general use	6/25/2005
13	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 5000A Au	thickness	Ebeam 1, alpha step profilometer	general use	6/25/2005
14	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	6/25/2005
15	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	6/27/2005
16	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	6/27/2005
17	Develop with MF319 for 45s			glass bowl		6/27/2005
18	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	6/27/2005
19	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	6/27/2005
	Polymer Depositions					
	12-1 P3UBT at 3000 rpm, 1500 acc, 60 s					

Appendix 3.13 Common Gate OFETs with SiN gate dielectric

GT MiRC CMOS Process Run Sheet						
Batch 13: Common Gate OFET						
(um p-type OFET, 2 Wafers, 2000A SiN)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Sb-doped n-type Si [111], 470 um thickness, 5.4-6.7 ohm/cm purchased from WaferNet	4-pt probe measurement	resistivity	4-pt probe	general use	6/28/2005
2	Piranha clean and RCA clean			CMOS wet bench, SRD	CMOS clean	6/28/2005
3	Gate oxidation: LPCVD SiN deposition	t_{SiN} ~ 2000A	thickness	Nitride furnace tube 4, nanospec	CMOS clean	6/28/2005
4	PR deposition (Shipley 1813, 5000rpm, 30s) and softbake 115C 75s			RC8, hotplate	general use	7/1/2005
5	SiN Etch (5 min etch in 45sccm CH4 and 5 sccm O2)	remove SiN from wafer back		RIE	general use	7/1/2005
6	PR strip	Gastonics Asher	1 min	Gastonic Asher	general use	7/1/2005
7	PR deposition (Shipley 1813, 5000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	7/1/2005
8	Level 3 Photolithography: OFET MASK 3, expose MA-6 8.0s CI2			MA-6	general use	7/1/2005
9	Chlorobenzene soak 20 min, develop w/ MF319 30-45s			glass bowl	general use	7/1/2005
10	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 2000A Au	thickness	Ebeam 1, alpha step profilometer	general use	7/2/2005
11	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	7/5/2005
12	PR deposition (Shipley 1813, 5000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	7/5/2005
13	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	7/5/2005
14	Develop with MF319 for 45s			glass bowl		7/5/2005
15	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	7/5/2005
16	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	7/5/2005

Appendix 3.14 and 3.15 Super Clean Common Gate OFETs

GT MiRC CMOS Process Run Sheet						
Batch 14: Super Clean CMOS Common Gate OFET						
(um p-type OFET, 2 Wafers, 2000A gate ox)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Same green boat			SRD (2)		
2	Sb-doped n-type Si [111], 500 um thickness, 0.01 ohm/cm purchased from WaferNet	4-pt probe measurement	resistivity	4-pt probe	general use	7/2/2005
3	Furnace Tube Clean (tubeclean.00)	9 hr tube clean		Nitride Furnace 3	CMOS clean	7/2/2005
4	Piranha clean and RCA clean			CMOS wet bench, SRD	CMOS clean	7/2/2005
5	Gate oxidation (gateoxHH.00) 950C, 4 hr 40 min hr dryox	tox ~ 2100A	thickness	Nitride furnace tube 3, nanospec, SCA	CMOS clean	7/2/2005
6	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 3min			RC8, hotplate	general use	7/5/2005
7	SiO_2 etch (4 min BOE dip)	Etch SiO2 from backside of wafer		CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	7/5/2005
8	PR strip	Gastonics Asher	1 min	Gastonic Asher	general use	7/5/2005
9	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	7/5/2005
10	Level 3 Photolithography: OFET MASK 3, expose MA-6 8.0s CI2			MA-6	general use	7/5/2005
11	Chlorobenzene soak 20 min, develop w/ MF319 60-75s			Solitek developer	general use	7/5/2005
12	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 2000A Au	thickness	Ebeam 1, alpha step profilometer	general use	7/5/2005
13	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	7/6/2005
14	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	7/6/2005
15	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	7/6/2005
16	Develop with MF319 for 45s			glass bowl		7/6/2005
17	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	7/6/2005
18	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	7/6/2005

Appendix 3.16 Individual Poly Gate OFETs

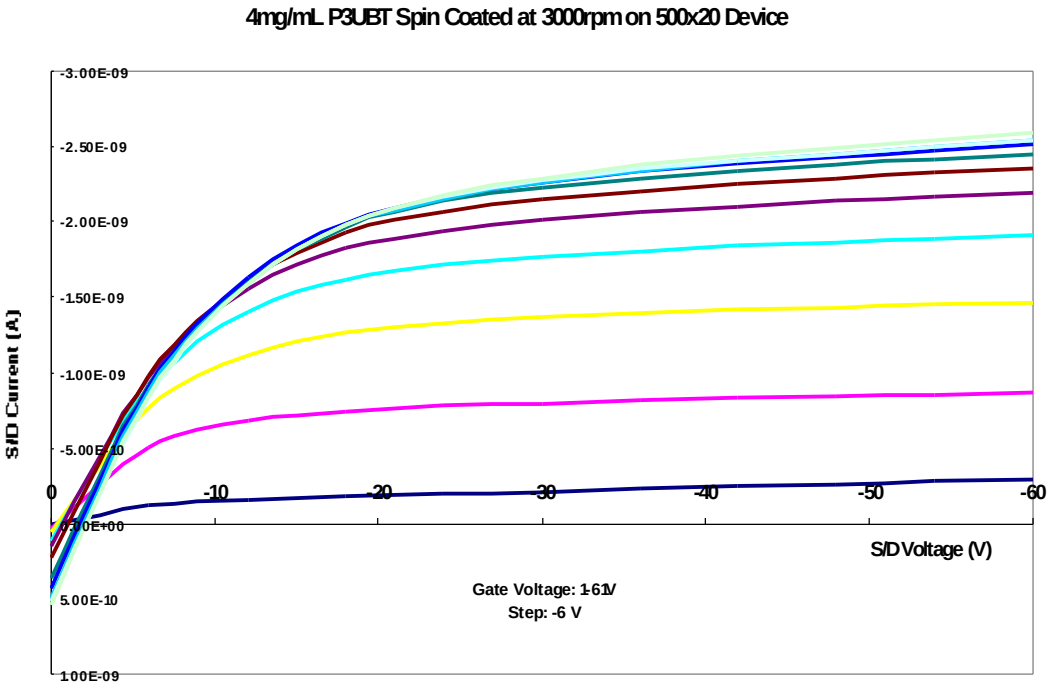
GT MiRC CMOS Process Run Sheet						
Batch 16: Super Clean CMOS Individual Poly Gate OFET						
(um p-type OFET, 6 Wafers, 2000A gate ox)						
	Steps & Recipes	**Expectations**	**Measurements**	**Equipment**	**Comments**	**Date Completed**
1	Same green boat			SRD (2)		8/8/2005
2	Prime grade Si [100] wafers supplied by CMOS	4-pt probe measurement	resistivity	4-pt probe	general use	8/8/2005
3	Piranha clean/RCA Clean/Boe Dip/SRD	Wafer cleaning		CMOS wet bench, SRD	CMOS clean	8/8/2005
4	Initial Oxidation (gateoxHH.00) 950C, 90 min run time	tox=930A	thickness	Nitride furnace tube 3, nanospec	CMOS clean	8/8/2005
5	Poly-Si deposition (run twice due to machine error)	tg = 2200A	thickness	Poly furnace 4, nanospec	CMOS clean	8/9/2005
6	Doping (PYPREDOP.001) for 15 min then anneal for 8 min at 900C	Rs =50 ohm/sq (0.13Ω/cm)	resistivity	Nitride furnace tube 1, 4-pt probe	CMOS clean	8/10/2005
7	Phosphorus glass removal (BOE dip)	wafer surface uniform in color	color: lt yellow	CMOS wet bench, SRD	CMOS clean	8/11/2005
8	PR deposition (Futurrex NR7-1500P, 3000rpm, 30s, acc=1000) and softbake 100C 60s			RC8, CMOS hotplate	CMOS clean	8/11/2005
9	Level 1 Lithography: Poly gate: OFET MASK 1, expose MA-6 CI1 7s (intensity=4.5)			MA-6, CMOS hotplate	general use	8/11/2005
10	Hardbake 115C 75s, Develop with MF319 30s			CMOS hotplate. Solitek developer	CMOS clean	8/11/2005
11	Poly-Si etch (lukepoly.set)		etch time = 2 cycles of 48s/cycle at 300W	STS ICP	CMOS clean	8/11/2005
12	PR strip		1 min	Gastonic Asher	general use	8/12/2005
13	Gate height measurement	t=1800A		Alpha Step Profilometer, Woolam Elipsometer	general use	8/12/2005
14	Furnace Tube Clean (tubeclean.00)	9 hr tube clean		Nitride Furnace 3	CMOS clean	8/10/2005
15	Piranha clean/RCA clean/SRD			CMOS wet bench, SRD	CMOS clean	8/12/2005
16	Gate oxidation (gateoxHH.00) 950C, 4 hr 40 min hr dryox	tox = 2000A	thickness	Nitride furnace tube 3, nanospec, SCA	CMOS clean	8/12/2005
17	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8, hotplate	general use	8/23/2005
18	Level 2 Photolithography: Gate cut, OFET MASK 2, expose MA-6 3.4s CI2			MA-6	general use	8/23/2005
19	Develop with MF319 for 45s			Solitek developer	CMOS clean	8/23/2005
20	SiO_2 etch	2 min BOE dip	gate well height	CMOS wet bench, SRD, alpha step profilometer	CMOS clean / general use	8/23/2005
21	PR strip	acetone bath	1 min	Gastonic Asher	general use	8/23/2005
22	PR deposition (Shipley 1813, 5000rpm, 30s) and softbake 115C 75s			RC8, CMOS hotplate	general use	8/23/2005
23	Level 3 Photolithography: OFET MASK 3, expose MA-6 8.0s CI2			MA-6	general use	8/23/2005
24	Chlorobenzene soak 20 min, develop w/ MF319 60s			Solitek developer	general use	8/23/2005
25	Ti/Au S/D deposition, liftoff in acetone	50A Ti / 5000A Au	thickness	Ebeam 1, alpha step profilometer	general use	8/24/2005
26	Polymer deposition	40nm polythiophene		RC-8 spinner	general use	8/30/2005
27	PR deposition (Shipley 1813, 4000rpm, 30s) and softbake 115C 75s			RC8 Spinner, hotplate	general use	8/30/2005
28	Level 4 Photolithography: OFET MASK 4, expose MA-6 3.4s CI2			MA-6	general use	8/30/2005
29	Develop with MF319 for 45s			glass bowl		8/30/2005
30	Polymer etch in Chlorobenzene			glass bowl, ~15s	general use	8/30/2005
31	Post Bake (60C @10-3 torr)		24 hrs	vac oven	general use	8/30/2005
	Polymer Depositions					
	16-1 HMDS (3000rpm, 1500 acc, 60 sec) then P3UBT (same)					
	16-2 HMDS (3000rpm, 1500 acc, 60 sec) then P3OT (same)					

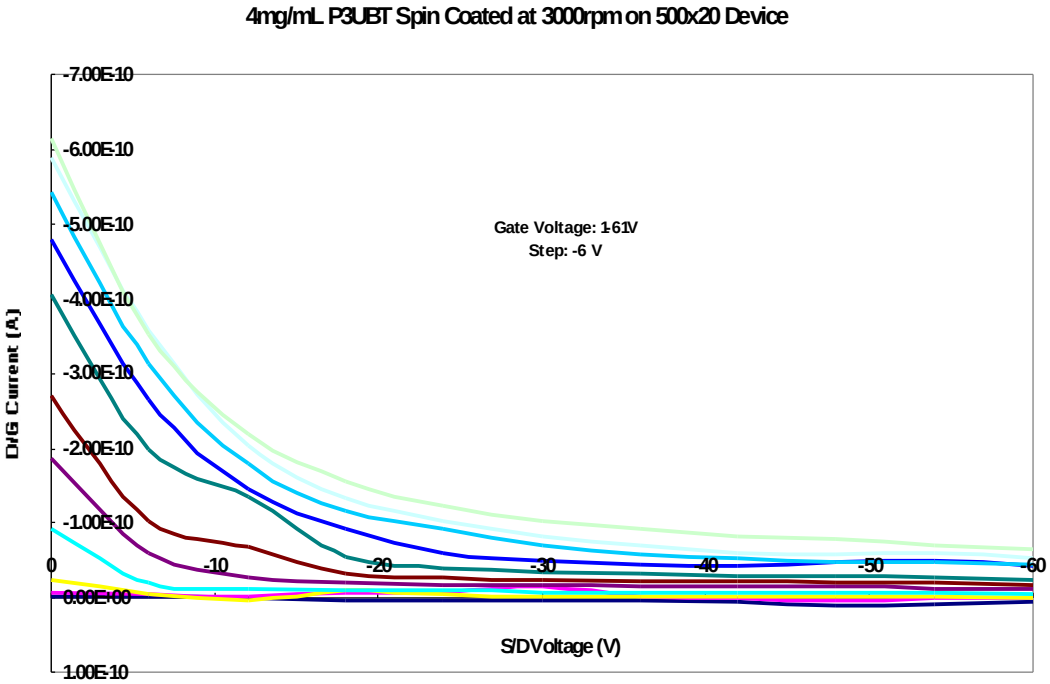
Appendix 3.17A Representative IV FEM data for batch 1 with 4.0 mg/ml spin coated P3UBT

	Length	Width	FEM	FEM (from SPA)
CAST				
	50	5	6.50E-07	
	50	20	5.16E-07	
	50	50		
	200	20		
	200	50		7.36E-06
	200	100		1.14E-05
	500	20		3.84E-06
	500	50	1.75E-05	5.51E-06
	500	100	7.33E-06	7.62E-06
SPIN (3000)				
	50	20		
	50	50	6.27E-07	8.00E-06
	200	20	1.50E-06	6.73E-06
	200	50	8.78E-07	4.94E-06
	200	100	7.40E-07	6.05E-06
(A)	500	20	1.21E-06	8.57E-06
	500	50	1.27E-06	8.57E-06
	500	100	1.33E-06	6.65E-06

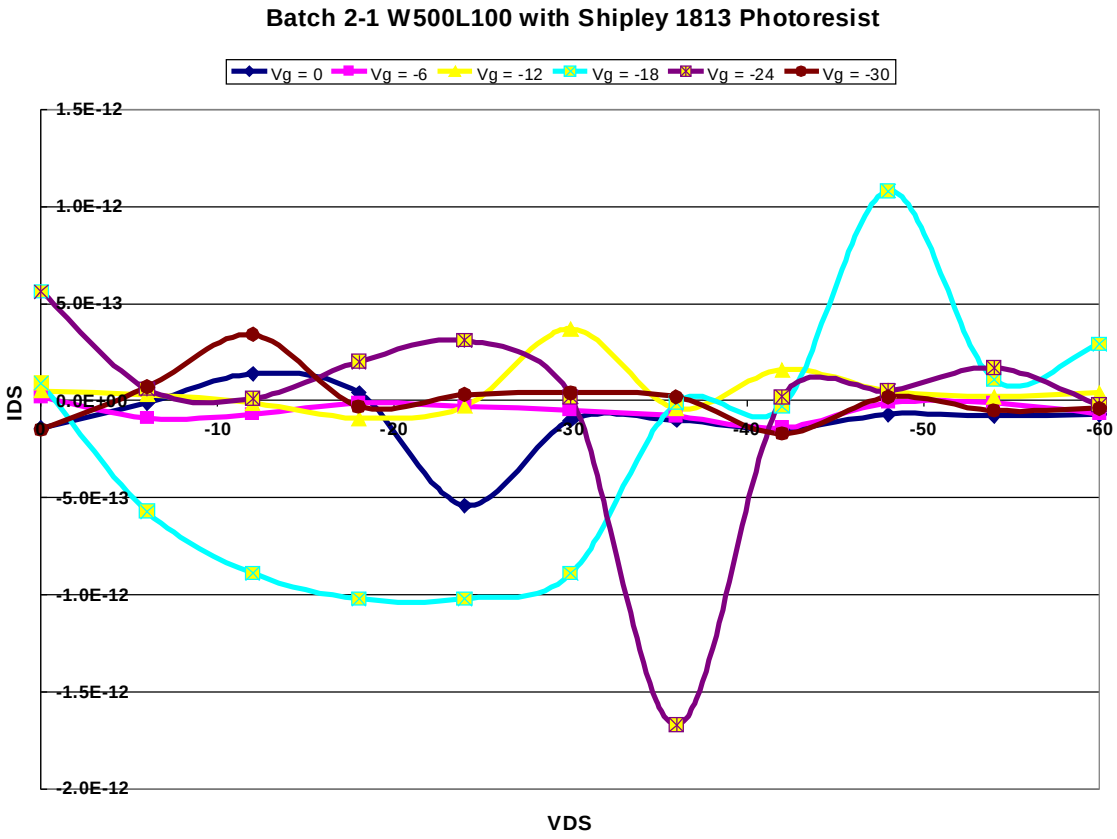
CAST	average	6.50E-06	7.15E-06
	standard deviation	7.99E-06	2.83E-06
SPIN	average	1.08E-06	7.07E-06
	standard deviation	3.30E-07	1.43E-06

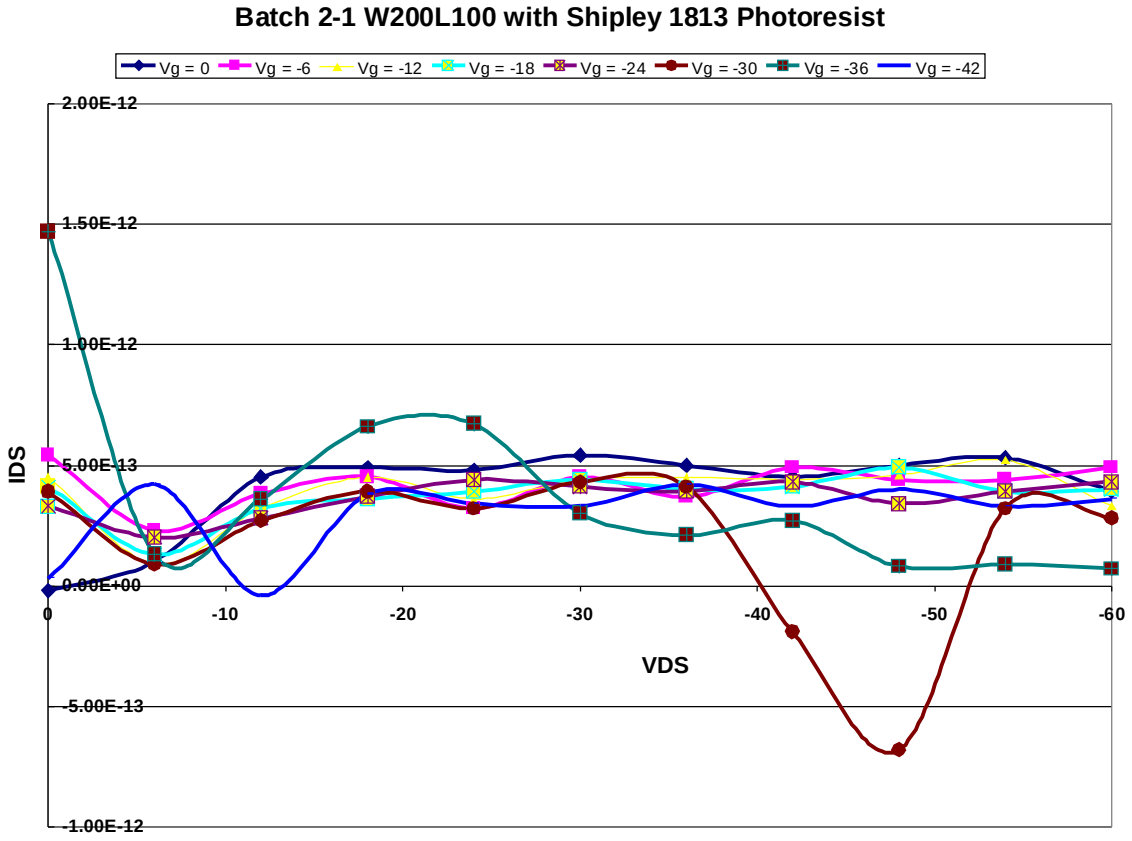
Appendix 3.17B IV curves corresponding to the FEM data.



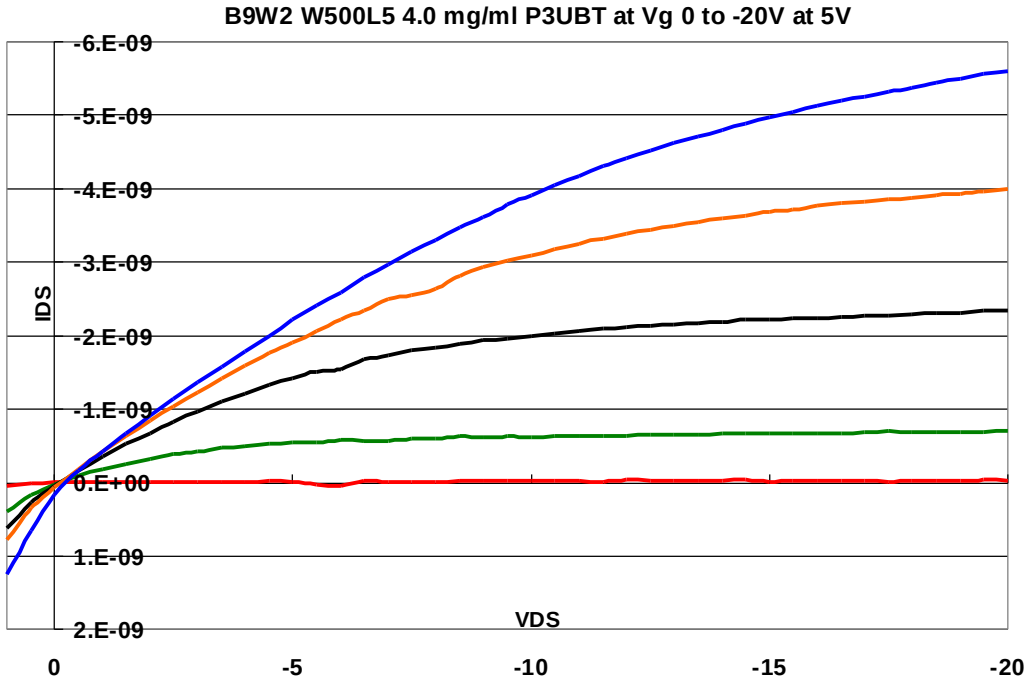


Appendix 3.18 Representative IV curves for batch 2 with Shipley 1813 spun at 5000 rpm

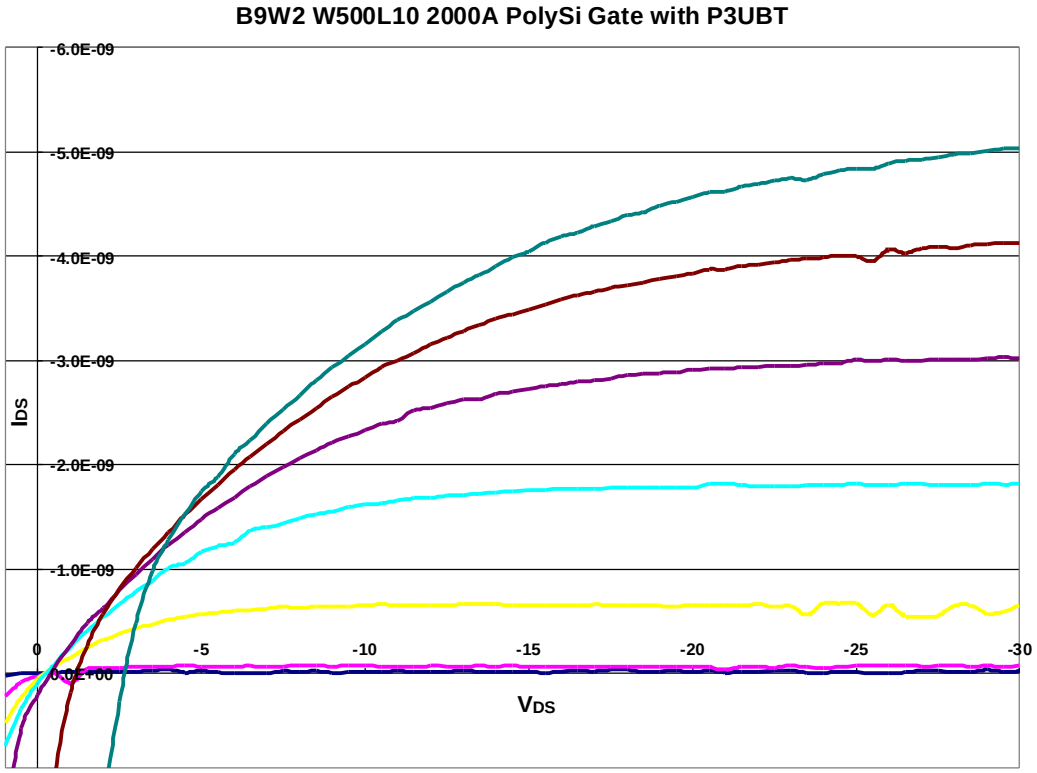




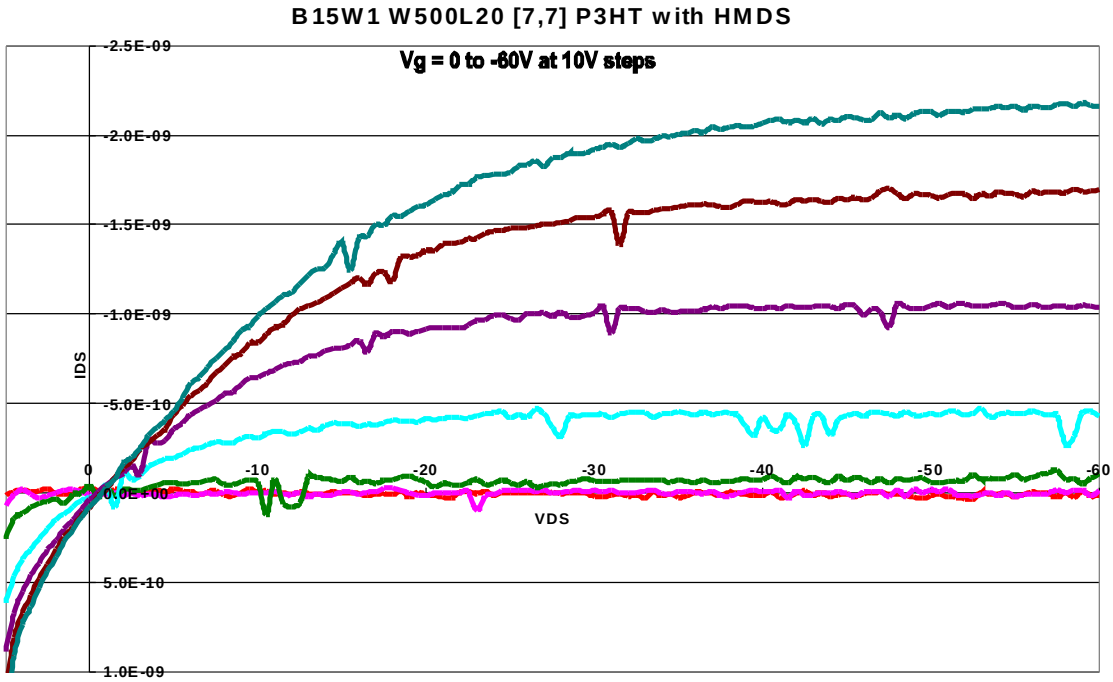
Appendix 3.19A Batch 9 W500L5 P3UBT individual gate device.



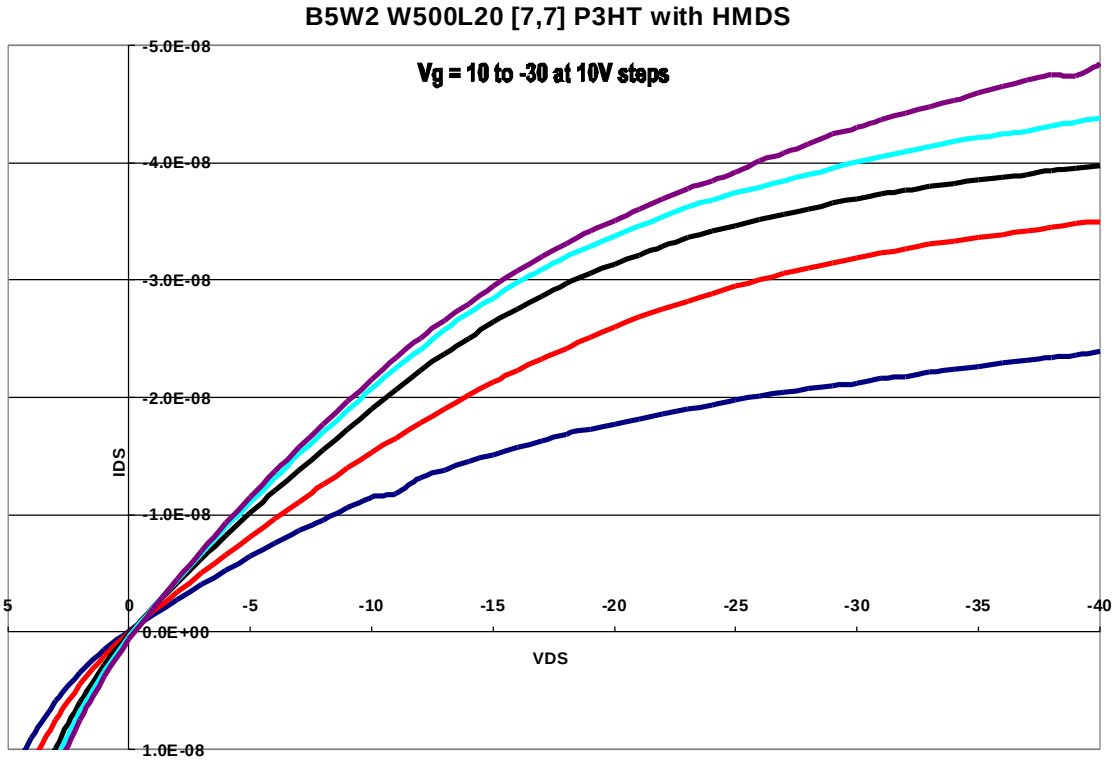
Appendix 3.19B Batch 5 W500L10 P3UBT individual gate device with Vg from 0 to -40V at -5V steps



Appendix 3.19C Batch 15 Common gate P3HT with HMDS



Appendix 3.19D Batch 5 Individual gate P3HT with HMDS



CIRICULUM VITA

Overview:

Extensive polymer characterization experience
Organic and polymer synthesis and purification experience
Microelectronic fabrication design and manufacture
Transistor design fabrication in cleanroom environments
Effective problem solving, presentation, and leadership skills

Academic Education:

Georgia Institute of Technology, Atlanta, GA (Graduation Date: 12/2005)
Ph.D., Major: Polymer Chemistry, Minor: Polymer and Textile Fiber Engineering.
September 2000-Present, Total GPA 3.4/4.0: Chemistry GPA 3.6/4.0, MSE GPA 3.2/4.0, MBA GPA 3.0.

Georgia Institute of Technology, Atlanta, GA, 12/2002
Masters of Science: Polymer Chemistry

Georgia Institute of Technology, Atlanta, GA, 8/1999
Bachelors of Science: Major: Polymer Chemistry, Minor: Organic Synthesis

Research Experience:

Georgia Institute of Technology, Atlanta, GA (1995-present)

- Graduate Research Assistant for Dr. Laren Tolbert (2000-present)
    - Research Projects:
        - Fabrication of physical and chemical vapor deposition chambers for organic thin-film depositions
        - Design and manufacture of organic field-effect transistors
        - Manufacture of organic-inorganic hybrid solid-state solar cells
        - Thin-film analysis within solid-state solar cells
        - Maintenance of PVD, glovebox, and spin processors
    - Other duties
        - Computer network administrator for 10 lab computers
- Teaching Assistant for Undergraduate Advanced Organic Synthesis Lab II (2000-2001)
    - Responsibilities: Teaching advanced organic synthesis and characterization techniques to undergraduate seniors
- Undergraduate Research Assistant for Dr. David Collard (1998-1999)
    - Research Project: To explore the thermal effects from additives on PET blends
    - Extensive polymer characterization using TGA, DSC, FTIR, and HNMR

Honors and Awards:

- Intel Foundation Ph.D. Fellowship Award (2004-2005)
- Research Assistantship, Georgia Institute of Technology (2001-present)
- Teaching Assistantship, Georgia Institute of Technology (2001-2002)
- GAANN Teaching Fellowship (2001-2002)

Certification and Memberships:

- American Chemical Society, ACS (Member since 2002)
- University Center of Excellence in Photovoltaic Research, UCEP (2001-2005)
- Vice President of External Affairs for the Georgia Beta Housing Corporation of Phi Kappa Psi (2000-present)
- Phi Kappa Psi Atlanta Alumni Association
- Member Association of Volleyball Professionals (AVP)

Other Work Experience:

Lucent Technologies, Murray Hills, NJ; Graduate Internship (2003)
- Developed methods for crystal growth and purification
- Manufactured and tested polyacene thin-film and single-crystal OFETs

Lucent Technologies, Atlanta, GA; Assistant Research Chemist (5/2000-8/2001)
- Polymer characterization for the production of optical fibers and optical fiber coatings
- Die-cast and spinning application of polymer and Kevlar coatings to optical fibers
- Development of company standards for loss performance in optical fibers

Hess Polyurethanes, Undergraduate Summer Internship (1999)
- Designed and formulated urethanes including elastomers, flexible and rigid foams
- Met with clients to develop custom urethanes

Ecosys Laboratories, Undergraduate Summer Internship (1996)
- Environmental chemist testing samples for toxic contamination

LIST OF PUBLICATIONS AND PRESENTATIONS

Publications:

Roberson, Luke; Patel, Biren; Kowalik, Janusz; Tolbert, Laren; Janata, Jiri. "From common to individual Gate MOS OFETs: A platform for high-throughput, reuseable organic/polymer semiconductor mobility screening." *Polymeric Materials Science and Engineering* **2006**, accepted.

Roberson, Luke; Kowalik, Janusz; Tolbert, Laren; Kloc, Christian. "Pentacene Disproportionation during Sublimation for Field-Effect Transistors. *J. Amer. Chem. Soc*. **2005**, 127, 3069-3075.

Luke B. Roberson, Mark A. Poggi, Janusz Kowalik, Greg P. Smestad, Lawrence A. Bottomley, and Laren M. Tolbert. "Correlation of Morphology and Device Performance in Inorganic-Organic TiO_2-Polythiophene Hybrid Solid-State Solar Cells." *Coordination Chemistry Reviews* **2004**, 248(13/14) 1491-1499.

Roberson, Luke; Kowalik, Janusz; Tolbert, Laren; Kloc, Christian. "Hydrogen transfer during pentacene sublimation at atmospheric pressure." *Polymeric Materials Science and Engineering* **2003**, 89, 410-411.

Presentations:

"Correlating Morphology and Device Performance in Inorganic-Organic TiO2-Polythiophene Hybrid Solid-State Solar Cells". **Poggi, Mark A**.; Roberson, Luke B.; Kowalik, Janusz.; Smested, Greg P.; Bottomley, Lawrence A.; Tolbert, Laren M.; ECS Symposium on Electrochemical Systems, Sensors and MEMS. Atlanta, GA, **2004**.

"Hydrogen Transfer During Pentacene Sublimation at Atmospheric Pressure." **Roberson, Luke**; Kowalik, Janusz; Tolbert, Laren; Kloc, Christian. 226th National American Chemical Society Conference, **2003**.

"Hydrogen Transfer During Pentacene Sublimation at Atmospheric Pressure." **Roberson, Luke**; Kowalik, Janusz; Tolbert, Laren; Kloc, Christian. 5th Annual Harold Nations Symposium at Georgia Tech. **2003**.