Alternate Testing of Analog and RF Systems Using Extracted Test Response Features

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Alternate Testing of Analog and RF Systems using Extracted Test Response Features

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"We make a living by what we get, but we make a life by what we give."

— *Norman McEwan.*

... to my parents, Purnendu and Sampriti Bhattacharya and my wife, Ananya, without whom I would have never achieved my dreams ...

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As Lord Krishna narrated to Arjuna, "*karmanyebadhikaraste, maa faleshu kadachana; maa karmafalahetur bhur, maa te sadgostaba akarmani* (One has only the ability to perform the work, but has no control over the outcome; so, do not get tempted in the consequences of your work, nor should one leave work as well)", he gave him as well as the mankind the greatest lessons of all. This has always inspired me to do something in my life. I thank God, The Almighty for his blessings and pray to him for his continued benevolence throughout the rest of my life.

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Summary

Testing is an integral part of modern semiconductor industry. The necessity of test is evident, especially for low-yielding processes, to ensure Quality of Service (QoS) to the customers. Testing is a major contributing factor to the total manufacturing cost of analog/RF systems, with test cost estimated to be up to 40% of the overall cost. Due to the lack of low-cost, high-speed testers and other test instrumentation that can be used in a production line, low-cost testing of high-frequency devices/systems is a tremendous challenge to semiconductor test community. Also, simulation times being very high for such systems, the only possible way to generate reliable tests for RF systems is by performing direct measurements on hardware. At the same time, inserting test points for such circuits while maintaining signal integrity is a difficult task to achieve.

The proposed research develops a test strategy to reduce overall test cost for RF circuits. A built-in-test (BIT) approach using sensors is proposed for this purpose, which are designed into high-frequency circuits. The work develops algorithms for selecting optimal test access points, and the stimulus for testing the DUT. The test stimulus can be generated on-chip, through efficient design reuse or using custom built circuits. The test responses are captured and analyzed by on-chip sensors, which are custom designed to extract test response features. The sensors, which have low silicon area overhead, output either DC or low frequency test response signals and are compatible to low-speed testers; hence are low-cost. The specifications of the system are computed using a set of nonlinear models developed using the *alternate test* methodology. The whole approach has been applied to a RF receiver at 1 GHz, used

as a test vehicle to prove the feasibility of the proposed approach. Finally, the method is verified through measurements made on a large number of devices, similar to an industrial production test situation. The proposed method using sensors estimated system-level as well as device-level specifications very accurately in the emulated production test environment with a significantly smaller test cost than existing production tests.

Chapter I
Introduction

1.1. Standard Industry testing approach

The standard industrial test development flow for any commercial product is shown in Figure 1.1.

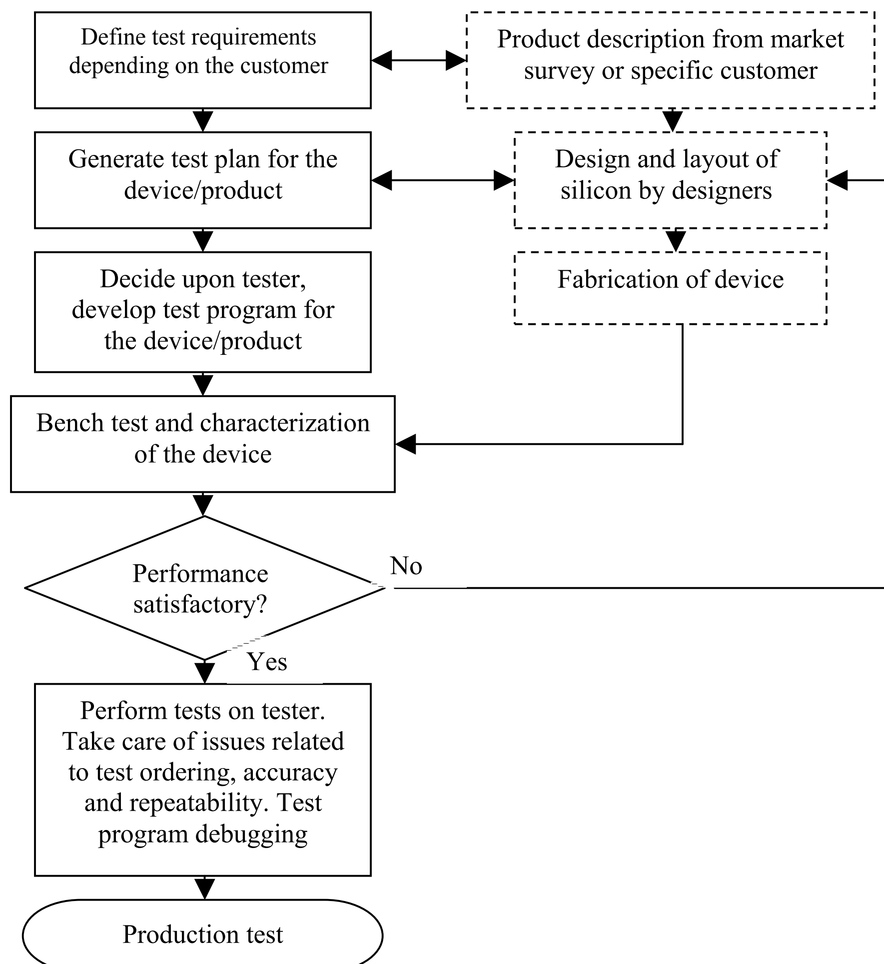


Figure 1.1. Industrial test development flow.

First, after the market demand has been studied and customers of the specific product have been well identified, the test development process is started. Usually, there are two different types of test requirements. For any product specially requested by a specific customer, the stringent specification requirements depending on application targeted by the customer, decides the tests that need to be performed to meet these necessities. For other types of products, where the manufacturer targets a new segment of the market with a solution to the needs of the consumers, the manufacturers themselves usually set the test requirements. Once the test requirements are identified, the test engineers work with the designers to generate the test plan for the device or product. As the device goes into production manufacturing, test engineers decide upon the tester to use depending on the test requirements and the resources available from different testers. In addition, the test program for production test is also developed. In addition, the device load board is designed and simulated during this time.

As soon as the fabricated devices come back from fabrication, first, a bench test is performed to characterize the product, understanding the silicon behavior, as well as detecting any unforeseen problems that might be associated with the fabrication and design. Once the device performs satisfactorily in the bench test, the load board is sent for manufacturing by the test engineer. Next, the challenge for the test engineers is to make the test program functional for production test, which involves debugging and restructuring the tests to obtain similar performance as obtained in the bench or close to it. In addition, issues related to loss in accuracy and errors from the tester and its associated accessories need to be considered here, and it is desired to have no loss of accuracy between tester results and the bench test results. The final set of tests performed

determines the issues related to repeatability and the handlers/ wafer probers. Once the program is debugged and the device specifications can be measured with a very small error margin, the test programs are released for production testing.

1.2. Problems and possible solutions

In general, for any device, there exist tests that are similar in nature, exercising the same behavior of the device under test. Tests, viz. IIP3, and 3rd Harmonic measurements are similar in nature, but usually to ensure uncompromised performance of the device, in some cases, these tests are performed separately. Moreover, the test procedure in industry is essentially sequential. With this approach, the test time is undoubtedly longer than it should be. Several approaches, as discussed below, are taken to reduce the number of tests, as well as the overall test cost.

1.2.1. Test compaction

In this approach, the tests are usually combined together to perform multiple tests with a single data capture operation. This method is applied to cases where the specifications of the devices need not be measured very accurately. In such cases, reduction of the overall test time to reduce the manufacturing cost plays a vital role, while the loss of accuracy in measurements up to certain limits is not critical to ensure device performance. The results of all the associated tests are calculated from the acquired data with the aid of mathematical equations that relate the results of the different tests to the measurements made. Usually, these equations are incorporated within the test program to obtain the specifications directly during production testing.

1.2.2. Test parallelization

While test compaction is performed with the aid of equations relating different specifications to a single measurement, test parallelization incorporates the technique where many parts of a large circuit can be tested in parallel, at the same time. This method, contrary to the method described above, uses multiple measurements to test individual specifications and is thus more accurate. Tests, viz. PSRR and Gain for OpAMP, can be performed in parallel using this approach.

1.2.3. An overview of alternate test

In the alternate testing approach, the test specifications of the circuit-under-test are not measured directly using conventional methods (such as circuitry and stimulus to measure CMRR, for example). Instead, a specially crafted stimulus is applied to the circuit-under-test and the (conventional) test specification values are computed (predicted) directly from the observed test response. Test generation for this approach starts with the standard test plan for any product and the test generation algorithm. Usually, sample sets of devices are chosen from different lots and are then used in test generation, as shown in Figure 1.2. The final output from the test generation approach is the optimized test stimulus, which potentially replaces all the specification tests for which the test generation was performed. During test, this optimized test stimulus is applied to the DUT and from the response of the DUT, the specifications are estimated directly with a very small margin of error. In general, all the test specifications can be computed from the response to a single applied test stimulus or a set of stimuli applied to the different ports of the device under test.

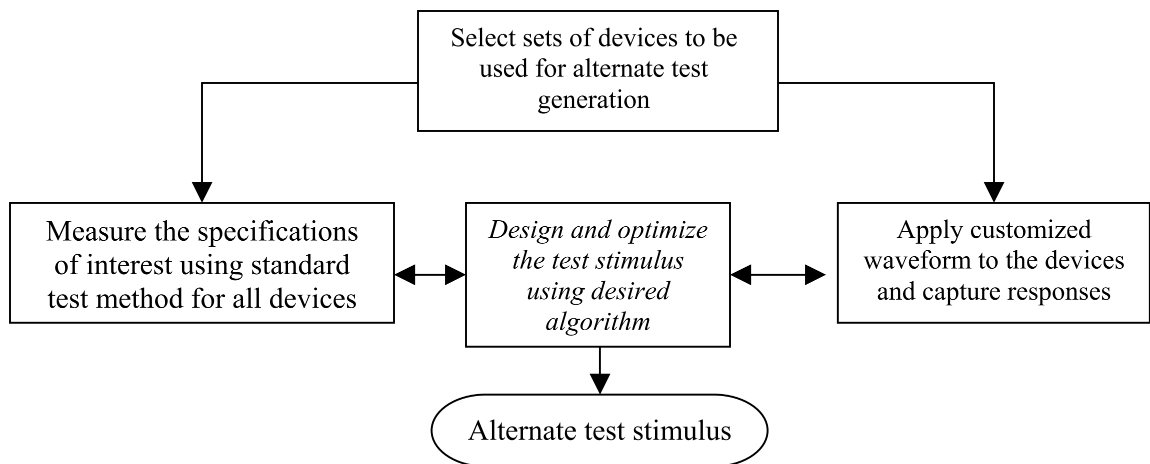


Figure 1.2. Alternate test generation framework.

1.3. Alternate test fundamentals

Alternate test has been around for a long time since Variyam and Chatterjee proposed it in 1998 [42]. Alternate test, as of today, seems to be the only viable solution to the problem associated with testing high-frequency devices. As described in section 1.2.3, alternate test makes use of the variations in the response of the DUT to estimate the specifications, even without performing any standard test procedure. It is a manifestation of test compaction, test ordering and use of inherent statistical correlation between the process parameters and the specifications. Though, today the concept has been extended to different directions [15],[44],[102],[103],[47],[48],[119],[120], the core idea remains the same.

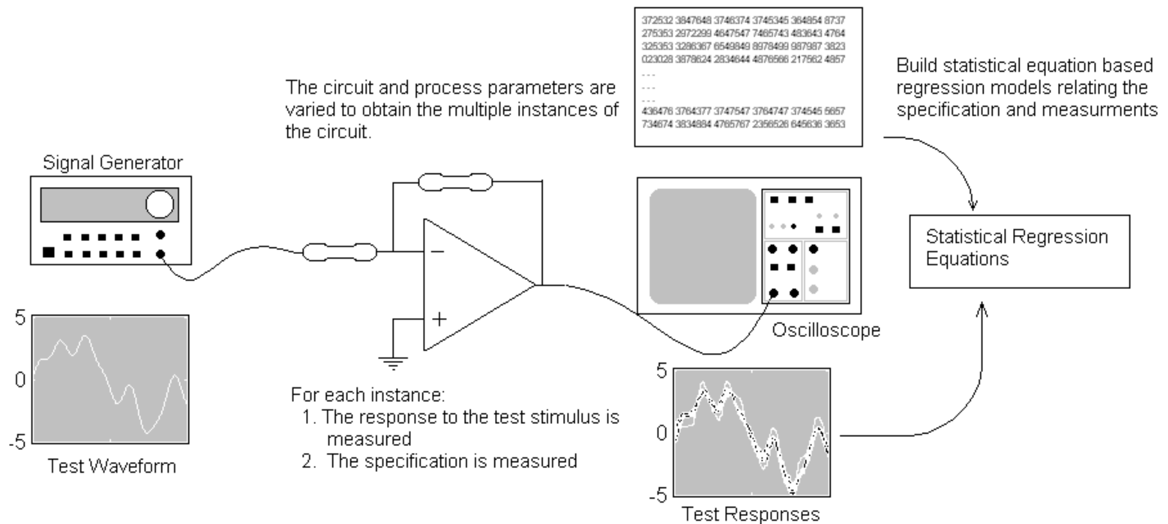


Figure 1.3. Alternate test generation.

Figure 1.3 shows the idea behind generation of alternate test. During test generation, various waveforms, generated using sinusoids, pulses, piecewise linear and a combination of some or all of those, are considered. Each of the waveforms is considered individually. For each waveform, as shown in Figure 1.3, multiple instances are generated for the device-under-test. For each instance, the response to the input waveform is captured and stored, and, at the same time, the specifications of interest are measured using the standard specification measurement technique. After this procedure is finished for all the instances, the responses and the measured specifications are related using non-linear regression equation, which is referred as model. Thus, models are constructed for all the candidate waveforms. Next, the accuracy of the models is evaluated using a set of test inputs. In some cases, the candidate waveform is picked directly depending on accuracy of the models, or the waveforms are further optimized to obtain better accuracy. Finally, the optimized test waveform is produced. This optimized waveform and the model corresponding to it together, constitutes the alternate test.

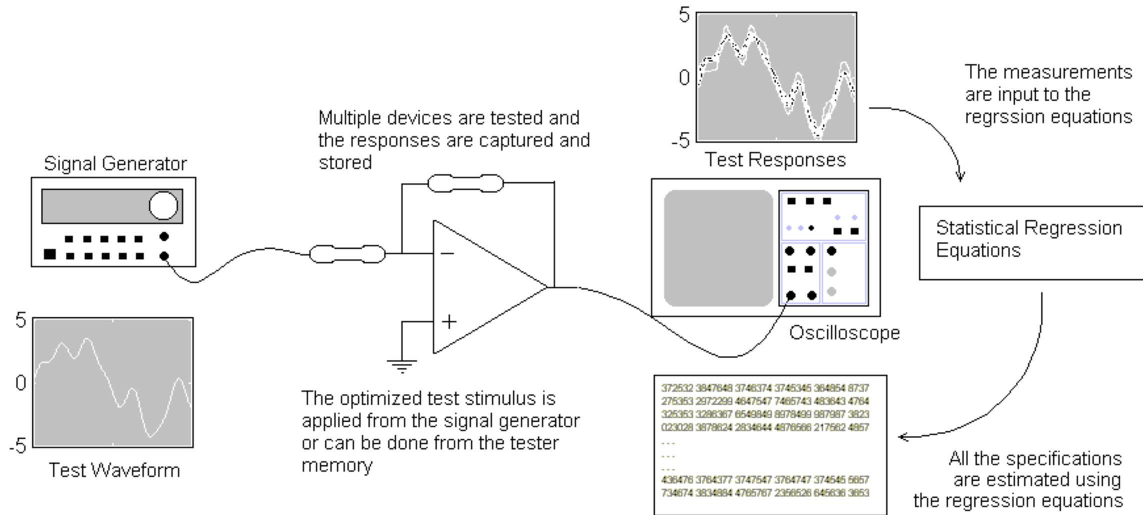


Figure 1.4. Application of alternate test to estimate specifications.

After the test is generated, the test is applied to the devices to be tested. The optimized test waveform is applied to each device and the output response is captured. The measured response is then put into the model that was generated, as shown in Figure 1.4, and the model outputs the specifications of the circuit. This procedure does not require any other tests to be made on the circuit and all the specifications can be obtained directly from the model.

1.3.1. Use of alternate test

The alternate test approach, described above, is compact and easy to use with any device. With the test times for different complex devices being very high and with a very little possibility of test compaction or parallelization, alternate test can use a single test stimulus to test all the specifications, thereby simplifying load-board designs considerably. Moreover, test time is very less compared to standard specification tests. To prove the viability of alternate test, in the work described next, test procedures at

assembled-package and wafer-probe are co-optimized using alternate test to reduce test cost.

1.4. Contributions

This section briefly summarizes the contributions and the novelty of this thesis. Figure 1.5 summarizes the contributions in different classes of electronic devices. It can be broadly divided into three classes. Initial part of the thesis focuses on co-optimizing tests for wafer probe and assembled package devices. This method has been validated on OpAMPs, high-speed comparators and a RF mixer. In addition, this was validated through hardware measurements performed on OpAMPs.

Next part focuses on test development of RF devices. Initially, to ease simulation constraints, behavioral models were built for devices, viz. LNA, mixer as well as front-end RF sub-systems. After the initial learning phase, a loop-back test methodology was proposed with the objective of built-in-test of RF systems. A hardware validation of the proposed approach was performed. However, limitations of the loop-back test were later understood and a built-in-test approach using sensors was proposed as the thesis topic. A receiver system with sensors was built to validate the method.

The other class of devices investigated was ultra-wide band (UWB). For this class, test methodologies to reduce test time and test cost for both pulsed and MB-OFDM devices were proposed.

The following chapters elaborate the different methods developed for enhancing production test of electronic devices by reducing test cost and test time using alternate test method.

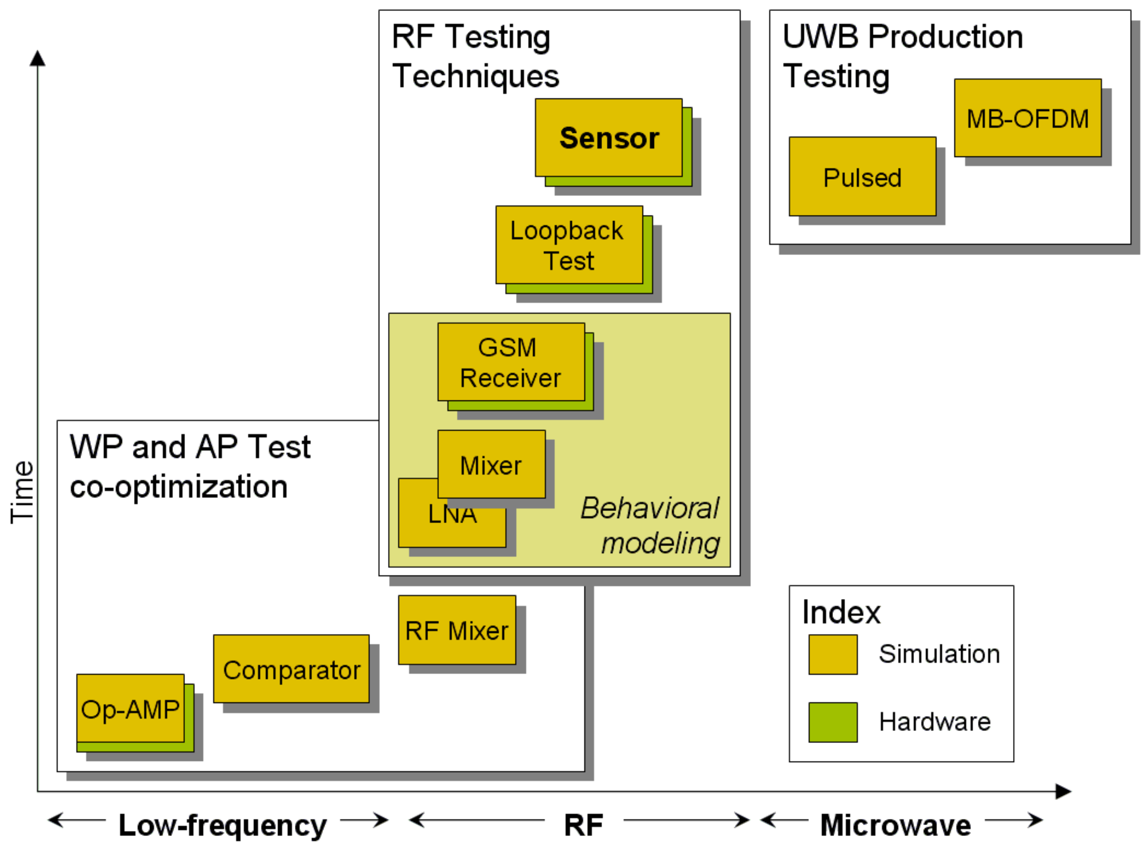


Figure 1.5. Contributions of the thesis.

Chapter II
Wafer-Probe and Assembled-Package Co-optimization to Minimize Overall Test Cost

Because of the increasing complexity and speed of analog, mixed-signal, and RF ICs, test engineers are often faced with characterization and new production testing challenges to ensure high product quality without incurring excessive testing costs. In a typical IC manufacturing process, first the bare die on each silicon wafer are tested using a wafer-probe tester. This procedure is called the wafer-probe (WP) test. Subsequently, the *"good"* die are diced, packaged and tested again; a procedure, known as the assembled package (AP) test, is performed to eliminate any bad ICs passed by the wafer-probe test procedure. In this work, the objective is to reduce the overhead of the AP test to bring down the overall test cost.

2.1. Previous work

In the past, there has been significant effort in the area of reducing specification testing time by eliminating unnecessary tests and ordering them in an optimal way [1]. However, these tests are still time consuming and expensive. In [2], the authors propose using extra tests during wafer-probe testing to eliminate faulty packaged circuits. In [3], the authors proposed a way to generate tests for analog circuits using fault models. Nagi et al, presented a test frequency selection algorithm in [4] for AC testing using behavioral-level fault modeling. In [5], a test-generation algorithm for detecting single and multiple faults based on circuit sensitivity computation was presented. In [6], the authors solved the test frequency selection problem through optimization techniques. Zheng et al. [7] use a

digital test generator tool to obtain test stimuli for analog circuits. In [8], Tsai showed that the difference between faulty and fault-free circuits could be maximized using a quadratic programming-based transient test optimization procedure. Abraham, Chen, and Balivada [9] used a ramp as the primary test stimulus for analog circuits.

The process of alternate testing consists of applying a short transient test stimulus to the circuit under test (CUT) and analyzing the corresponding (sampled) test response to predict the circuit's specifications. In the alternate testing approach, the test specifications of the CUT are not measured directly using conventional methods (such as circuitry and stimulus to measure CMRR, for example). Instead, a specially crafted stimulus is applied to the CUT and the (conventional) test specification values are computed (predicted) from the observed test response. In general, all the test specifications can be computed from the response to a single applied test stimulus.

In [10], [11], and [12], the authors presented an assembled package test method that relies on the application of a carefully designed transient test stimulus for implicit specification testing of analog ICs. In this approach, the specification values of the device under test (DUT) are predicted from the response of the DUT to the applied test stimulus.

This approach is not directly applicable to wafer-probe testing, as the signal drive and response observation capabilities during wafer-probe testing are limited because of parasitics from long cables and probes used in the procedure. Moreover, the various test cost components of wafer-probe and assembled-package testing need to be considered concurrently to get the maximum benefits from both tests and to construct an optimal wafer-probe and corresponding assembled-package test program that minimizes overall test cost. In [13], the authors incorporated bandwidth constraints for wafer-probe testing

during test generation. Later, in [14], they used nonlinear regression models to predict the specifications from the responses for both assembled-package and wafer-probe testing and co-optimized the tests for wafer-probe and assembled-package testing. In [15] and [16], the authors showed that this method can be applied to high-speed devices as well and excellent accuracy can be achieved using the proposed test methodology.

2.2. Predicaments in wafer-probe testing

During wafer-probe testing, the tester makes an electrical contact with each die on the wafer through traveling probes that touch down on the die pads. Because of the long cable lengths and Schottky contacts formed by the probes at the die surfaces, huge parasitics are introduced in the signal path. For this reason, typically for analog circuits, DC tests and power supply current tests are performed during the WP test. All other specifications are measured during AP test, i.e., slew rate, gain, noise figure, etc. The electrical performance (parasitics) of the probe is modeled using a passive network and is referred to as the "*wafer-probe model*" in Figure 2.1. Such a passive network for an industrial wafer-probe tester is shown in the next section. The parasitics added to the input of the DUT in Figure 2.1 by the probe contact limit the signal that can be applied to the DUT. The same parasitics connected to the output of the DUT limit the external tester observation capability of the response to the applied stimulus. Similarly, during AP testing, the signals that can be seen by the CUT are limited by the package parasitics, while the small amount of parasitics introduced by the load board and the signal traces can be ignored. Package models associated with the inputs and outputs of the CUT are used to model the constraints as a result of test signal application and device response observation during the AP test (Figure 2.1).

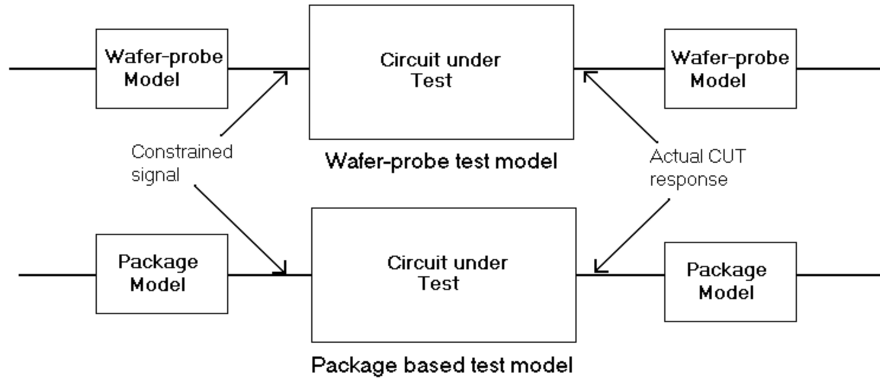


Figure 2.1. Models used for WP and AP test setups.

2.2.1. Solutions

In this approach, instead of finding a way to overcome the above problems associated with the parasitics, the parasitics are modeled very carefully and accurately. Thus, their effects are taken into account during test generation, and optimization is performed.

2.3. Co-optimization framework

During test stimulus generation, the suitability of a candidate test stimulus for a WP or AP test is evaluated by simulating the circuit under test using the associated end-to-end models, as shown in Figure 2.1. The objective is to be able to evaluate the performance of the embedded circuit under test by observing the output of the corresponding model of Figure 2.1 (these are the signals seen by an external tester). Furthermore, the goal is to *detect as many bad die as possible during WP testing, even when the signal drive limitations imposed by the WP model are significant*. As an extreme example, the circuit under test may be a 1 GHz device, while the wafer probe may be "good" only up to 300-400 MHz. WP and AP parasitic models for the HPL-94-18 Tester and a DIP40 ceramic package are used in this work for WP and AP models, respectively. These are shown in figures Figure 2.2 and Figure 2.3, respectively.

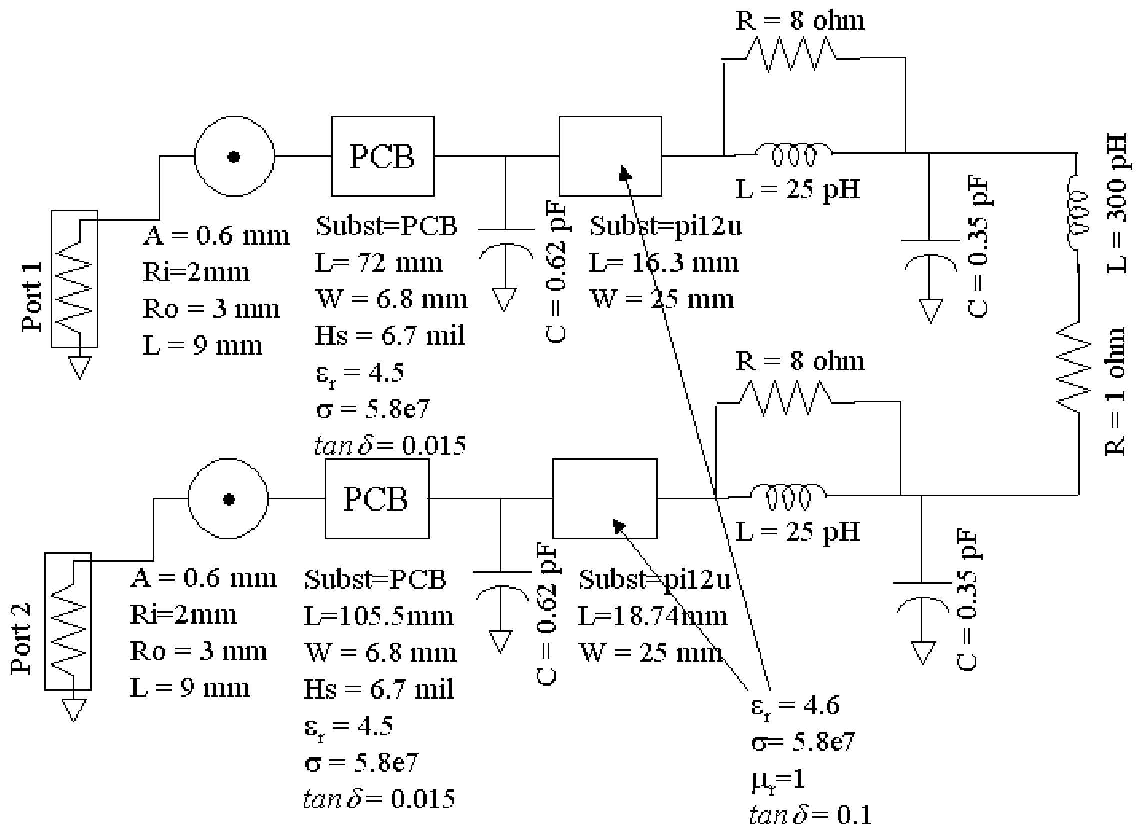


Figure 2.2. Wafer-probe model.

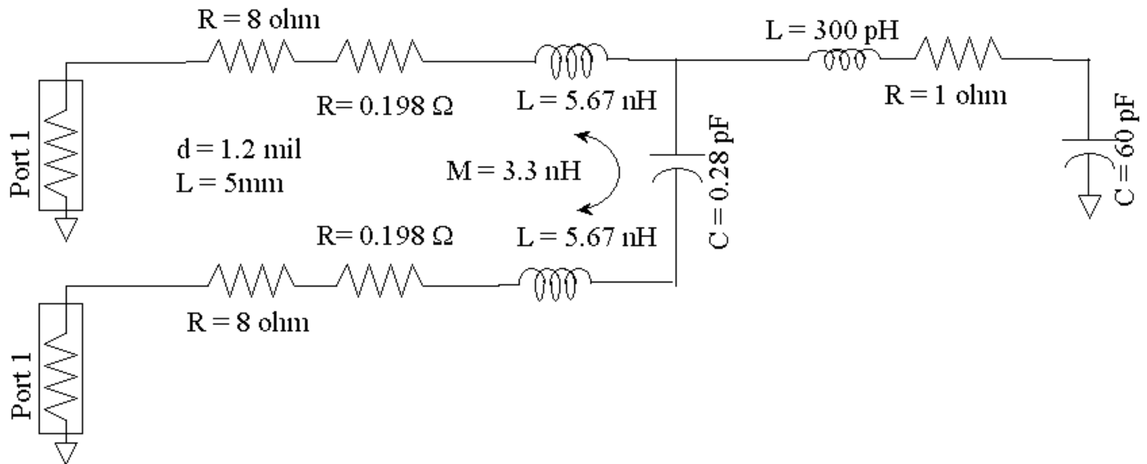


Figure 2.3. Assembled package parasitic model.

Transient tests are used during production testing for both WP and AP methods. Transient tests can be designed to extract a maximum amount of information about the DUT even when WP performance is not as accurate as compared to that of the circuit under test. In this way, a significant number of bad ICs can be detected during wafer-probe testing. Further, given the test cost components of the wafer-probe and assembled package test procedure, new algorithms can be developed for co-optimizing wafer-probe and assembled package tests to minimize test cost and test time, while ensuring high coverage and improving yield. Figure 2.4 shows the test framework used in industry for pass/fail binning of the circuits/devices.

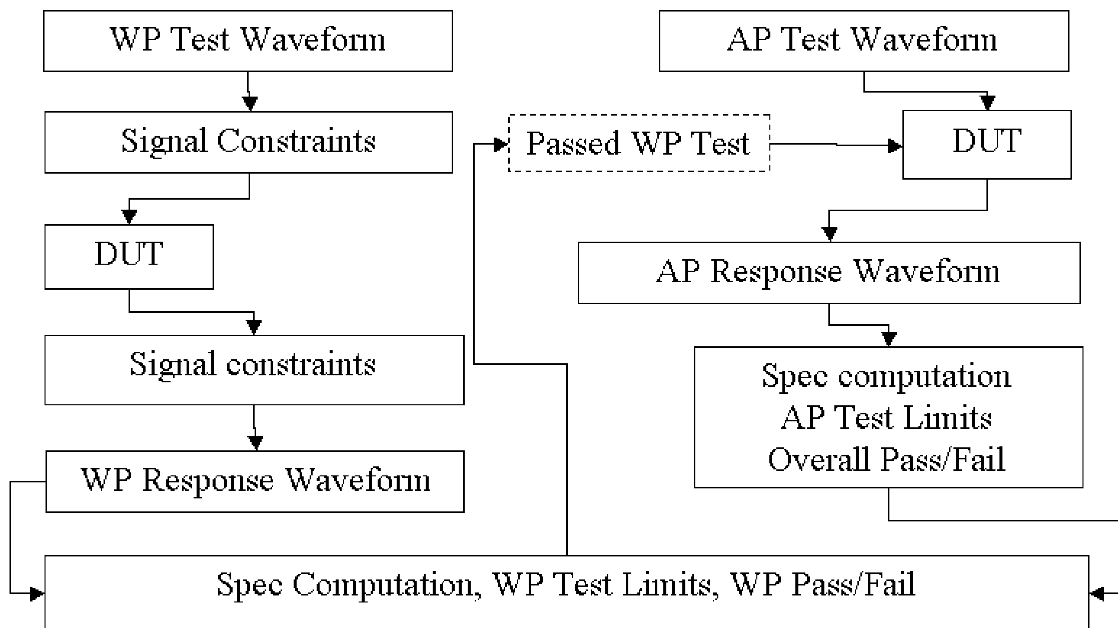


Figure 2.4. WP and AP test framework.

In the proposed approach, given the WP test cost/sec, AP test cost/sec, process statistics, yield, and packaging cost, the optimal WP and AP test stimuli are found that

minimize the overall test cost. For WP test stimulus evaluation, WP parasitic models are used and for AP test stimulus evaluation, AP parasitic models are used. The optimal tests are obtained by *co-optimizing* the WP and AP test stimuli. Moreover, the proposed algorithm can be configured to accommodate any relation between WP and AP test costs. Using different test cost values for a specific device might result in a different waveform with different duration, but the proposed method of co-optimization remains the same. As already explained, the WP test cost/time is usually less than the AP test cost/time.

2.4. <u>Test approach</u>

In the case of WP testing, traveling probes test the whole die, and there is very little mechanical movement involved (stepping time is approximately 120 ms) [17]. In AP testing, every time a new chip needs to be tested, it is put into the test site by a handler, followed by sorting and putting it into the correct bin, depending on the outcome of the test (total time required for handling is 300 ms, indexing time being 150 ms) [18]. This involves a lot of extra mechanical movement and causes an increase in the test cost/second for AP. Thus, the WP test cost per second (*approximately 1.5¢/s*) is significantly less than the AP test cost per second (*approximately 5¢/s*). Therefore, bad ICs detected during wafer-probe testing can help reduce the overall test cost dramatically. During production testing, all bad ICs that pass the WP test are packaged for AP testing and are eventually discarded after the AP test. A good WP test procedure minimizes the number of such bad ICs that are packaged and retested. On the other hand, WP test times that are too long (~5× AP test time) can offset the advantages of WP testing.

In our proposed test-generation approach, one-time establishment costs for wafer probe stations or handlers were not considered; a generalized methodology was provided to

bring down the production test cost. Several studies concerning the cost of probes and handlers to reduce overall test cost have been performed by various researchers, but in this work, the focus is on reducing the overall manufacturing cost by minimizing the functional test costs by reducing test times and packaging costs by eliminating bad devices at an early stage of production test.

The results of the WP (transient) test and AP (transient) test are mapped to the test specifications of the packaged ICs for pass-fail decision. Test guard bands are set so that all good ICs pass the WP test. A few bad ICs that pass the WP test are eventually detected during the AP test. The guard bands for the assembled package testing are set in such a way that all bad ICs are detected by the test. Some yield loss may occur by using the proposed test procedure because of a few good ICs being classified as bad, but this ensures that the test coverage remains very high and is able to detect all the faulty ICs.

2.5. Fault model

In our approach, the process parameters (i.e., device width, length, oxide thickness, zero-bias threshold voltage, etc.) are varied to generate different instances of the DUT. The process parameters are varied according to a statistical distribution (assuming a Gaussian distribution) to mimic the actual manufacturing process using the mean and the standard deviation values. The parametric variations are modeled as shown in Figure 2.5. For each such combination of process parameters, the specification value is computed and thus the specification space is computed.

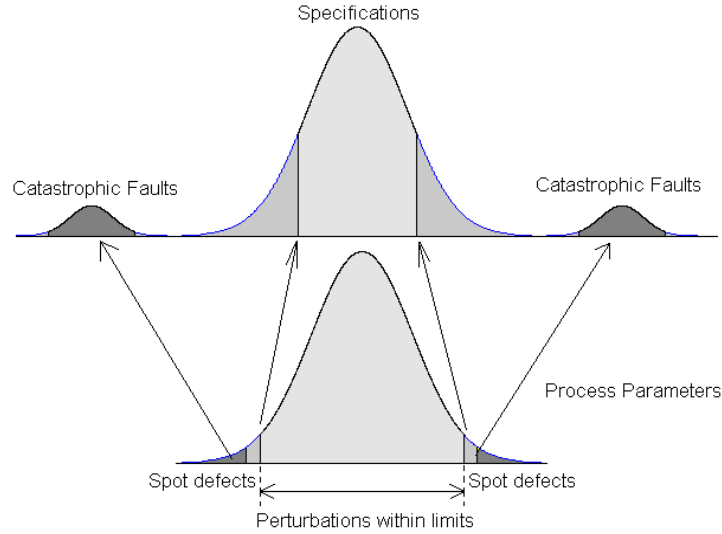


Figure 2.5. Parametric fault modeling.

This work focuses on functional test generation for the DUT. Random or spot defects, which are manifestations of catastrophic faults, i.e., open, short, or bridging faults, cause large deviations from the nominal specification values (Figure 2.5). Therefore, any spot defect present in the DUT will affect the response to the optimized input waveform considerably, resulting in a grossly inaccurate estimation of specification(s). In such a case, the DUT will lie outside the test limits imposed by the test engineer. Thus, using the proposed algorithm, any DUT with spot defects will definitely be eliminated. In another case, there might be some spot defects present that do not affect the specifications or the test response at all (or affect it by a very small amount). This essentially means that the specific spot defect is not affecting the DUT performance in any way. Thus, the proposed algorithm can handle the effect of spot defects although they are not generated as a part of the parametric variation of process parameters.

2.6. Test algorithm

The DUT performance parameters are directly related to the process parameters. While all the process parameters affect the DUT performance in some way or other, considering a smaller "critical" set of process parameters that bears high correlations to the specification values can perform accurate test generation. Identifying this set of "critical" parameters is necessary to reduce the simulation complexity of the test generation algorithm. So, before the test-generation process starts, a search algorithm is used to find the critical process parameters. Section 2.6.1 describes the algorithm for identifying these process parameters.

2.6.1. Computing critical process perturbations

For given process statistics, N process vectors, each consisting of different assignments of the n process parameters, $[p_1, p_2, \ldots p_n]$, can be generated using statistical sampling. For this purpose, the process parameters are varied around a mean value, with a specific standard deviation, and the process and circuit parameter vectors are generated in such a way that they cover the whole process space within the standard deviation limits. These process vectors (that impact the DUT's performance) are applied to the DUT, and corresponding sets of m specification values of interest constituting the specification vector $[s_1, s_2 \ldots s_m]$ are measured. Hence, N specification vectors are generated, corresponding to each of the N process vectors.

Once the process parameter and specification vectors are generated, nonlinear modeling using multivariate adaptive regression splines (MARS) [19], explained in Section 2.6.1.1, is used to relate the process parameters to the specifications. Using the

models generated, critical process parameters are identified following a greedy search algorithm, as explained in Section 2.6.1.2.

The relation between the responses of the DUT and the specifications is nonlinear. Using a simpler modeling option, e.g., Taylor series expansion, for constructing the models may not capture all the nonlinear relationships between the responses and the specifications. For the above-mentioned reason, MARS was used for modeling.

2.6.1.1. MARS model generation

MARS are used for developing the nonlinear model that relates the process parameters to the DUT's test specifications. The MARS algorithm mainly depends on the selection of a set of basis functions and a set of coefficient values corresponding to each basis function to construct the nonlinear model. The model can also be visualized as a weighted sum of basis functions from the set of basis functions that spans all values of each of the independent variables. MARS use two-sided truncated functions of the form *(t-x)+* and *(x-t)+* as basis functions for linear and nonlinear relationships between the dependent and independent variables, *t* being the knot positions. The basis function has the form as shown in (1).

$$(x-t) = \begin{Bmatrix} x-t & x>t \\ 0 & otherwise \end{Bmatrix} \quad (1)$$

The basis functions together with the model parameters are combined to generate the model, which can predict the dependent variables from the independent variable values. The MARS model for a dependent variable *y,* independent variable *x*, and *M* basis functions, is summarized in (2).

$$y = f(x) = \beta_0 + \sum_{m=1}^{M} \beta_m H_{km}(x_{v(k,m)}) \quad (2)$$

where the summation is over the M independent variables, and β_0 and β_m are parameters of the model (along with the knots *t* for each basis function, which are also estimated from the independent data). The function H is defined as

$$H_{km}(x_{v(k,m)}) = \prod_{k=1}^{K} h_{km} \qquad (3)$$

where $x_{v(k,m)}$ is the kth independent variable of the mth product. During the forward stepwise placement, basis functions are constantly added to the model. After this implementation, a backward procedure is applied when the basis functions associated with the smallest increase in the least squares fit are removed, producing the final model. At the same time, the generalized cross validation error (GCVE), which is a measure of goodness of fit, is computed to take into account the residual error and the model complexity. The above equation can be further decomposed into the sum of linear, square products, cubic products, and so forth. Introducing a larger or smaller number of basis functions can also change the accuracy. Changing the order of products can change the degree of nonlinearity of the model.

2.6.1.2. Selection of critical process parameters

As described above, a nonlinear mapping from the *n-dimensional* process vector space (Δp) to the *m-dimensional* specification vector space (Δs) is constructed using MARS, as shown in (4).

$$\overline{\Delta s} = \Psi\left(\Delta p\right) \cdot \left(\Delta p\right) \qquad (4)$$

A set of critical process parameters is identified using a greedy algorithm-based search method. First, one set process vector and the corresponding specification vector is eliminated from the observation set. The reduced process parameter set, ($\Delta p'$), is then related to the reduced specification space ($\Delta s'$) using a MARS model, as described in (5).

$$\left(\overline{\Delta s}\right)' = \Psi'(\Delta p')\cdot(\Delta p)' \quad (5)$$

N such models are created, each time eliminating one process vector and the corresponding specification vector. Each model is then used to predict the eliminated specification vector by using the corresponding eliminated process vector, used as the input to the model. Next, the error between the estimated and the actual specification vector is computed. The process vector, the exclusion of which produces the largest error, is considered the most critical process parameter vector. The eliminated process vectors, for which the corresponding model produces error values above a certain threshold, are selected as "*critical vectors.*" The algorithm is shown in Figure 2.6.

```
function Selection(P,S,k)
P = Process matrix (N X p);
S = Specification matrix (N X s);
p = Number of process and circuit parameters;
s = Number of specifications;
N = Total number of process vectors;
k = Number of critical process vectors;
for i = 1,2 … s
{
 S_validation = S(i,:);
 P_temp = P; S_temp = S;
 for x = N, (N-1) … (N-k+1)
 {
    for j = 1,2 … x
      {
       P_validation = P_temp(j,:);
       S_validation = S(j,:);
       P_reduced    = P_temp - P_validation;
       S_reduced    = S_temp - S_validation;
       M_j = BuildMARSModel(P_reduced, S_reduced);
       Error(j) = S_validation - EvalMARSModel(M_j,P_validation);
       }
     Index = maxIndex(Error); /*returns index for maximum
   error */
     Append(CriticalProc(i), P_temp(Index));
     P_temp = P_temp - CriticalProc(i);
   }
 }
 return CriticalProc;
```

Figure 2.6. Selecting critical process parameters.

2.6.2. Core algorithm

During the manufacturing process, as devices are fabricated, there is no way to get access to the process data unless measurements are made on the device after manufacturing. Thus, after manufacturing, one does not know the process data and hence there is no knowledge about the process and circuit parameters. Therefore, we cannot use a methodology to get the specifications directly from the process and circuit parameters.

The process parameters were varied to generate different instances of the DUT to mimic the actual manufacturing process. However, in an actual manufacturing process, all the process parameters vary around the nominal value, with a specific statistical distribution. In simulation, it is nearly impossible to vary all the process parameters. So, first a set of critical process parameters was selected. For example, the selected process parameters included oxide thickness, width, and length of the MOS devices. Initially, k critical process perturbations are computed for all the specifications, as described in Section 2.6.1. The algorithm starts with a set of N waveforms and a set of k critical process vectors. The initial choice of waveforms is random, where several candidate waveforms, i.e., sine waves, pulses, and piecewise linear waveforms, or a combination of those, are used as a preliminary guess for both WP and AP tests. These are successively co-optimized to generate the final test waveform.

First, the test waveforms for the WP test and AP test are constructed independently, depending on the frequency and current limitations of each test setup. N such pairs of waveforms, for WP and AP, are constructed, which are treated as the initial population space for co-optimizing. All the test waveforms are applied to the DUT while the circuit is perturbed with the critical process perturbation vectors (obtained by using the algorithm in Section 2.6.1). Each of the N pairs of waveforms is simulated for all the k

critical process variations to obtain the corresponding *k* response waveforms. The specifications of the DUT under each of the *k* process variations are already computed while calculating the critical process vectors. From the data, a MARS model relating the sampled response waveform to the DUT's specifications is constructed (given the response waveform, the model computes the DUT's specification values). This is done separately for the WP and AP test waveforms. Let us denote the model relating the WP responses to the specifications by M_{WP} and the model relating the combined WP and AP responses to the specifications by M_{comb}. For each WP and AP test waveform set, two such models are created. The process is described in Figure 2.7.

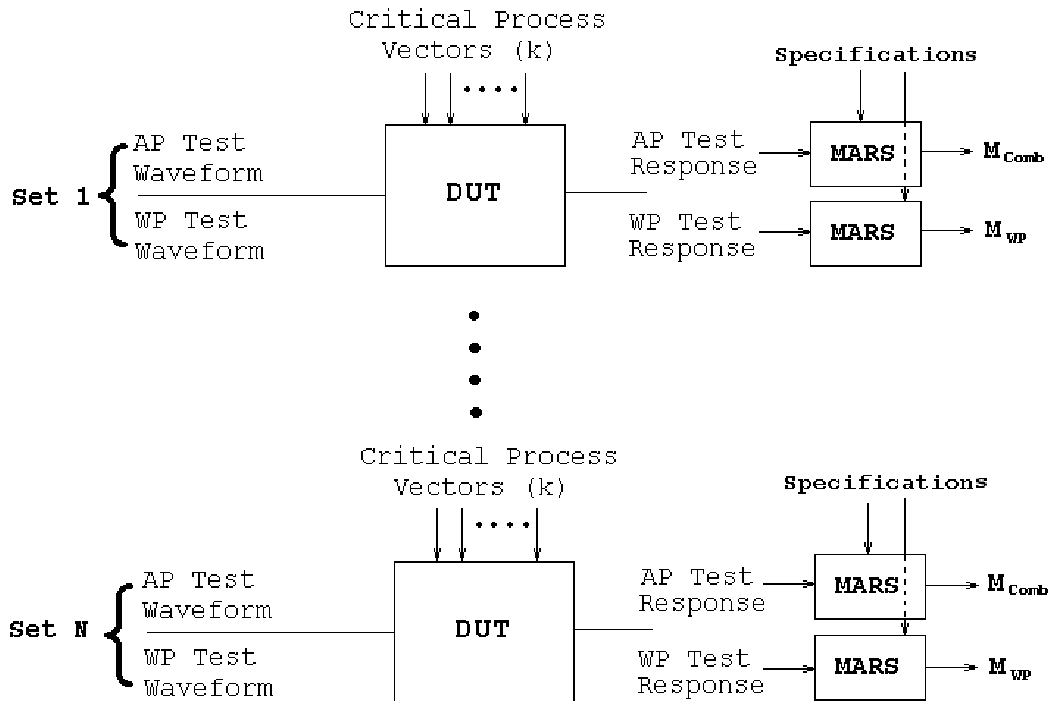


Figure 2.7. Test generation algorithm.

Now, the fitness of each of the models (M_{WP} and M_{comb}) is found from a set of reference process vectors and their corresponding specification values, which are also computed beforehand. By using these process vectors to perturb the DUT instances, the test waveforms are applied to the DUT and the response obtained is used as the input to the model. From the response and the model, estimates of the specifications are obtained. These are then compared to the actual values, and errors are computed for each model. The error between the specifications predicted from the model and the actual specifications obtained from the circuit measurements serve as the fitness of the model. The error can be obtained as shown in (6).

$$Spec^{NN}(k) = \frac{1}{S}\sum_{j=1}^{S} Spec^{N}_{actual}(j) - Spec^{N}_{predicted}(k,j) \text{ for } \forall k \in \{1,\ldots,N\} \quad (6)$$

where, k indicates the stimulus currently being considered, $Spec^{N}_{actual}(j)$ is the normalized specification computed for the reference process vectors, and $Spec^{N}_{predicted}(k,j)$ is the normalized specification predicted by the model made from the circuit output response measurements with all the process variations applied for the same stimulus. j represents the index for normalized specification value, which is computed as shown in (7). With those error values, the cost is computed, which is described in Section 2.7.

$$Spec^{N}(j) = \frac{1}{P}\sum_{i=1}^{P} Spec(i,j) \quad (7)$$

After the cost for all the waveforms is computed, the waveform that gives the least cost is chosen and is used to evolve the next set of waveforms using a genetic algorithm. Genetic algorithm comes in handy for optimization [20], [21]. It generates the optimized waveform for specification prediction and searches the solution space of a function using simulated evolution, i.e., survival-of-the-fittest strategy. In general, the fittest individuals of any population tend to reproduce and survive to the next generation, thereby

improving successive generations through mutation, crossover, and selection operations applied to individuals in the population. An outline for a generalized genetic algorithm is shown in Figure 2.8.

```
a)  Supply a population P0 of N individuals and respective
    function values.
b)  i ← 1.
c)  Pi' ← selection_function (Pi-1)
d)  Pi  ← reproduction_function (Pi' -1)
e)  evaluate(Pi)
f)  i=i+1
g)  Repeat step 3 until termination
h)  Output the best solution
```

Figure 2.8. Genetic algorithm framework.

To keep track of the test generation procedure and the fitness of the test, a few past cost values are stored. More and more time points are added according to the changes in the cost as the test progresses. The algorithm for modifying the test waveforms is shown in the following pseudo-code in Figure 2.9.

```
Backtrack (CostHistory, Cost) /* change the waveforms */
/* Cost is the present cost value */
/* CostHistory is a FIFO vector of k past cost values */
/* CostHistory (1) contains the most recent cost value */
{
if CostHistory(1) > Cost & … & CostHistory(k) > Cost
Increment wafer-probe waveform by one time step;
else
 /*Cost is not improving by increasing the WP test waveform */
  Backtrack 'k' time steps in WP test waveforms;
  Increment the AP waveforms by one time step;
end if
Shift CostHistory by one position by discarding the oldest
value
CostHistory(1) ← Cost;
}
return;
```

Figure 2.9. Waveform modification procedure.

2.7. Optimization cost function

In the proposed algorithm, shown in Figure 2.10, the test engineer provides these specification limits before the test generation is started. During testing, these specification limits are used to make a pass/fail decision about the circuit-under-test. Before describing the cost function and its various parts, different features that constitute the cost function and that must be taken into account, are described. The test cost has the following components:

- Wafer-Probe Test Time (WPTT) × Wafer-Probe Test Cost/time (WPTC).
- Assembled-Package Test Time (APTT) × Assembled-Package Test Cost/time (APTC).
- Cost incurred because of the packaging of bad ICs after wafer-probe test, but which are actually detected by assembled-package test and eventually rejected.
- Cost incurred because of good ICs being considered as bad after final tests.

As described in Section 2.6.2, the DUT is simulated in the presence of critical process vectors and testing is performed for both WP and AP. The measured specifications of the DUT and the test responses from WP and AP are used to build models, M_{WP} and M_{comb}, respectively. Let us define the errors obtained from the models M_{WP} and M_{comb} as *Error* and *WPError*, respectively. These errors are used to compute the areas, designated as α,β and γ in Figure 2.11, each of which is described in the next few paragraphs. *'N'* denotes the total number of ICs tested. The picture shown in Figure 2.11 shows the distribution (Gaussian) of specifications for any typical manufacturing process. The total area under the graph represents the total number of ICs that are considered for test purposes. During cost computation, the area considered is normalized with respect to the total area and

multiplied by the total number of ICs tested, as shown in (8), to obtain the number of ICs that fall within that category.

$$NumICs = TotalICs \times \frac{Area_{Type}}{Area_{Total}} \tag{8}$$

The first part of the test cost is the cost incurred because of the test time involved in wafer-probe testing. The total test time for wafer-probe testing multiplied the wafer-probe test cost per unit time gives the wafer-probe test cost. All ICs with specifications outside the specification limits are considered bad. However, in this case, a certain uncertainty is introduced because of the errors in the models, as described in Section 2.6.2. The errors, *Error* and *WPError*, indicate the relative error present in the prediction process. Therefore, any IC with a predicted specification value exactly at the *specification limit* can have the predicted specification anywhere between ±*WPError* around the *specification limit*.

Hence, there is an equal chance of that IC being good or bad and therefore it cannot be classified completely. However, if the predicted value itself is at *Specification limit* + *WPError*, then definitely the IC is bad. Therefore, all ICs with predicted values equal to and above *Specification limit* + *WPError* are considered bad. This area in Figure 2.11 represents the ICs eliminated during wafer-probe testing and the number of bad ICs is computed using (8). The ICs that have their specification values within the *Specification limit* and the value *Specification limit* + *WPError* are actually bad ICs, but they are packaged and passed on for assembled-package testing. Thus, the cost of packaging these ICs is an unwanted cost brought on by test inaccuracy, i.e. the error in prediction of M_{WP}. This cost is included in the overall test cost. The area β in Figure 2.11 allows us to calculate the number of bad ICs that are packaged.

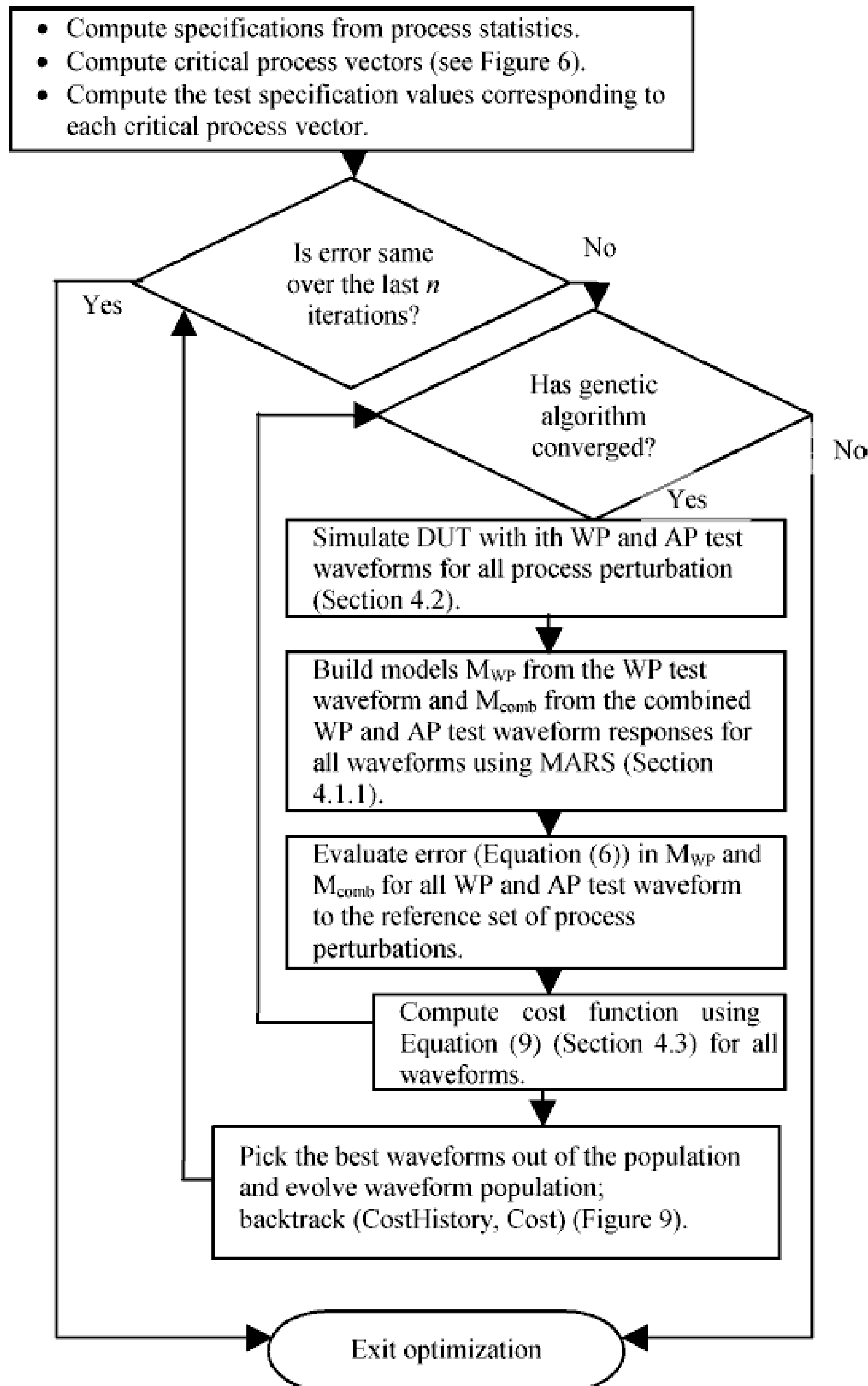


Figure 2.10. Core algorithm flowchart.

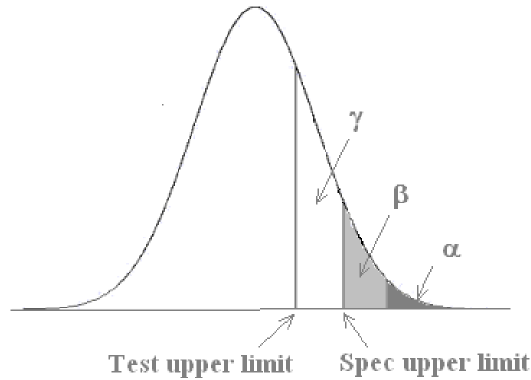


Figure 2.11. Distribution of specification used to compute test cost.

Finally, because of inherent errors in the test procedures, generally, test engineers set the specification limits tighter than the ones set by the designers. This is to ensure that despite the inaccuracies in measurements during testing, all bad ICs are definitely eliminated. However, at the same time, some good ICs are eliminated because of the tighter limits. This adds to the overall test cost. In this case, the test limit is determined from the overall *Error*. The test limit is set to *Specification Limit – Error*. Using the area γ in Figure 2.11, the number of good ICs that are rejected can be found. From the above discussion, the total test cost is obtained using (9).

$$\text{Cost} = \text{WPTT X WPTC X N} + \text{Packaging Cost per IC X } \beta\text{N} + APTT \text{ X } APTC \text{ X } (1 - \alpha) \text{ X } N + \textit{Cost Of Individual IC} \text{ X } \gamma N \quad (9)$$

2.8. <u>Results</u>

In the following, results obtained from the developed prototype are presented using the cost function and the optimization [22] approach as per the algorithm of Figure 2.10 [23]. The designs made for this work were developed with references from [24] and [25]. Also, [26] was used to develop the required statistical background for this work.

Results obtained from simulations for three circuits are presented below. The first example (Case Study I) shows an experiment to demonstrate that a significant number of bad ICs can be detected even when the cut-off frequency of the wafer probe is less than the bandwidth of the DUT. The second example (Case Study II) shows results for a high-frequency amplifier. The final example is a RF mixer (Case Study III). The DUT cost and the packaging cost for each IC and the test time for each of the ICs using standard specification testing are shown in Table 2.1. The test cost for the WP test was 1¢/s and 3¢/s for the AP test. Using these values, the test cost for standard specification testing was computed.

Altogether, 500 ICs of each type were considered for test generation and validation purposes. A large number of devices are used to ensure a proper statistical sampling. The test cost data was obtained from industry members of the Semiconductor Research Corporation (SRC) [27]. Case Study IV involved the validation of the proposed WP and AP test methodologies using hardware measurements made on the National Semiconductor LM318 operational amplifier [28].

Table 2.1. Different components used for cost computation.

	Cost component	**Value used**
Case Study I	Final product cost	$0.50
	Packaging cost	$0.20
	WP test time	150ms
	AP test time	500ms
Case Study II	Final product cost	$0.50
	Packaging cost	$0.35
	WP test time	350ms
	AP test time	750ms
Case Study III	Final product cost	$1.50
	Packaging cost	$0.50
	WP test time	1.8s
	AP test time	4s

Table 2.2 shows the different operating frequencies of the devices and the frequency at which they are tested using the proposed methodology. The wafer-probe cut-off frequency is the frequency up to which the signals applied to the probe station are not distorted. This is caused by the parasitics introduced by long cables and sharp contact probes used during WP testing. These introduce current and frequency limitations on the signals and distort high-frequency signals considerably before they reach the device. The input corner frequency is the maximum frequency at which the device can operate without any introduction of nonlinearity into the signal.

Table 2.2. Operating frequency and WP frequency limits for different devices.

	Operating frequency	**Test frequency**
OpAMP	500 kHz	200 kHz
Comparator	250 MHz	50 MHz
Mixer	900 MHz	100 MHz
Hardware measurement	10 kHz	2.5 kHz

2.8.1. Case Study I

This circuit was designed and used as the circuit-under-test. The bandwidth of the amplifier was close to 500 kHz. The wafer-probe test waveforms were limited to 200 kHz because of the package parasitics. This limit was imposed by a Tow-Thomas filter connected in front of the CUT. Changing the cutoff frequency of the filter would change the frequency limitations imposed in the case of the wafer-probe test. While determining the number of bad ICs, the total number of bad ICs found for all the specifications were added and divided by the number of specifications. In this example, the individual bad ICs were not tracked. This was done as the correlation between the specifications was not computed and hence the assumption was made that the bad ICs are equally distributed

over all the specifications. Table 2.3 shows the nominal specification values for the amplifier and the best accuracy achieved for each of the specifications. Table 2.4 shows test cost/IC and total ICs rejected at the wafer probe for different yielding processes.

Table 2.3. Accuracies achieved for different specifications (Case Study I).

Specifications	Nominal Value	Minimum error in prediction (AP test)
Gain Bandwidth	55 MHz	1.09%
Low Freq. Gain	76dB	0.94%
CMRR	-93 dB	2.42%
DC Offset	2.5 mV	4.33%
Overshoot	3.4mV	2.89%

Table 2.4. Comparison of test cost and ICs eliminated at WP test for different yield values.

Yield	99.0%		91.60%		88.40%	
Good and bad ICs	495	5	458	42	442	58
Bad ICs detected at WP test	3		20		29	
Bad ICs eliminated after AP test	2		22		29	
Savings in packaging cost	$0.60		$4.40		$5.80	
Test Cost/IC	$0.017		$0.0267		$0.0311	

In addition, a study was performed to see how the error in prediction changes as the frequency limitation imposed by the prober at WP test is changed. Table 2.5 shows that the error in prediction increases as the frequency limit is increased. This shows a limitation of the proposed approach, as the test stimulus needs to be within the frequency limits of the WP test instrumentation to achieve high degree of prediction accuracy for specifications.

Table 2.5. Change in error in prediction with change in frequency limit of WP.

Frequency limit	Error in prediction (%)
200KHz	1.5
170KHz	2.7
130Khz	6.7
100KHz	9.5

Figure 2.12 shows a convergence curve for test generation and the changes in cost as the test is optimized. Figure 2.13 shows a comparison of the number of bad ICs eliminated in the wafer-probe testing procedure compared to the total number of bad ICs using the test generated by the algorithm described above. Figure 2.14 and Figure 2.15 show the optimized test waveforms for assembled package testing and wafer-probe testing, respectively.

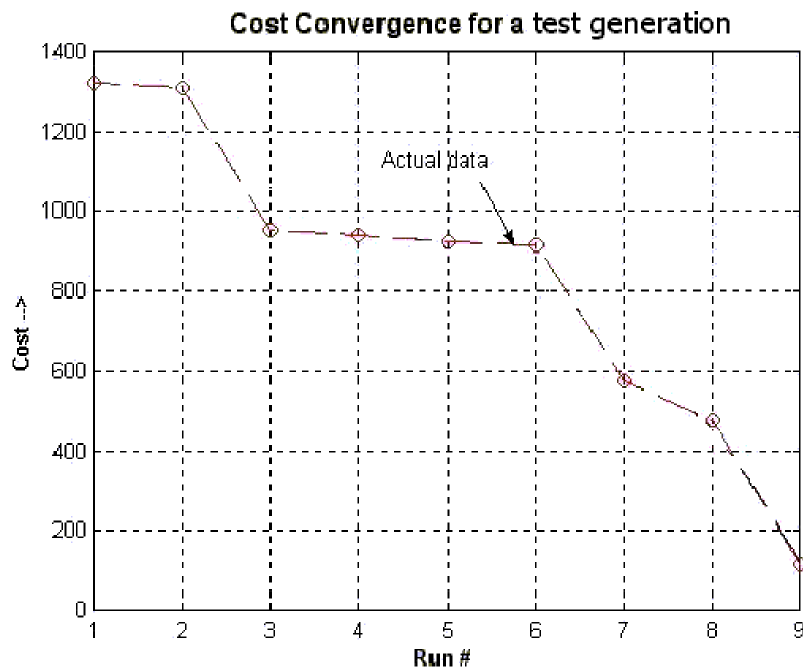


Figure 2.12. Cost convergence curve.

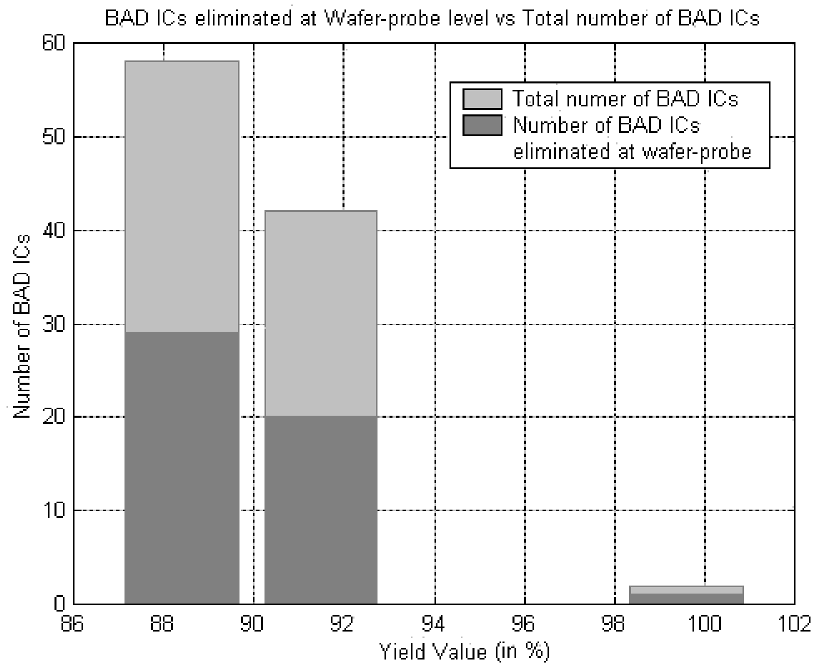


Figure 2.13. Comparison of bad ICs eliminated at WP vs. the total bad ICs.

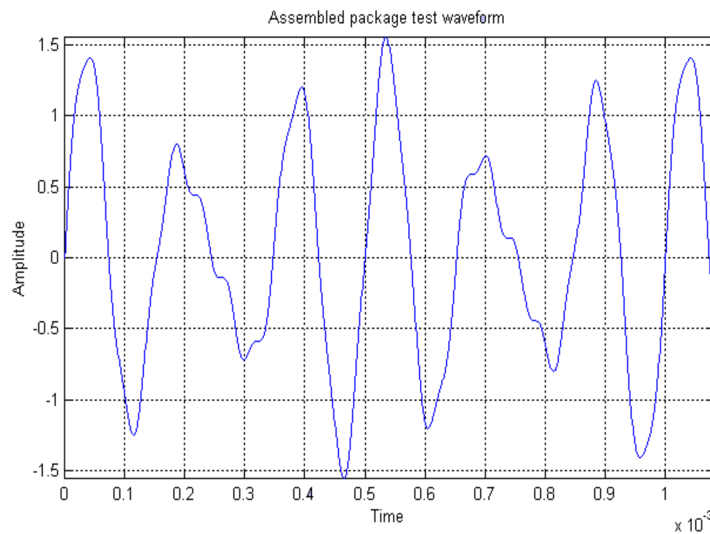


Figure 2.14. Assembled package test waveform for Case Study I.

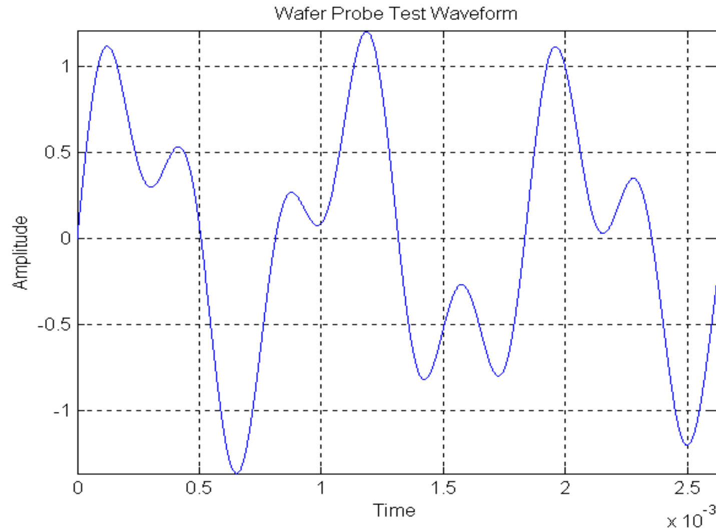


Figure 2.15. Wafer-probe test waveform for Case Study I.

2.8.2. Case Study II

The DUT was a high frequency, low-offset operational amplifier, the frequency response of which is shown in Figure 2.16. Table 2.6 shows the specifications of the device. This bandwidth limitation for WP and AP tests was imposed by the parasitic models shown in Figure 2.2 and Figure 2.3, respectively. The bandwidths of the parasitic models are ~50 MHz and 600 MHz, respectively, for WP and AP models. As shown in Table 2.6, specifications that far exceed the cutoff frequencies of the models, could be predicted very accurately. Table 2.6 shows the nominal specification values for the amplifier and the best accuracy achieved for each of the specifications. The specifications of the circuits were individually tracked and the ICs, for which any one of the specifications was out of limits, were rejected as bad ICs.

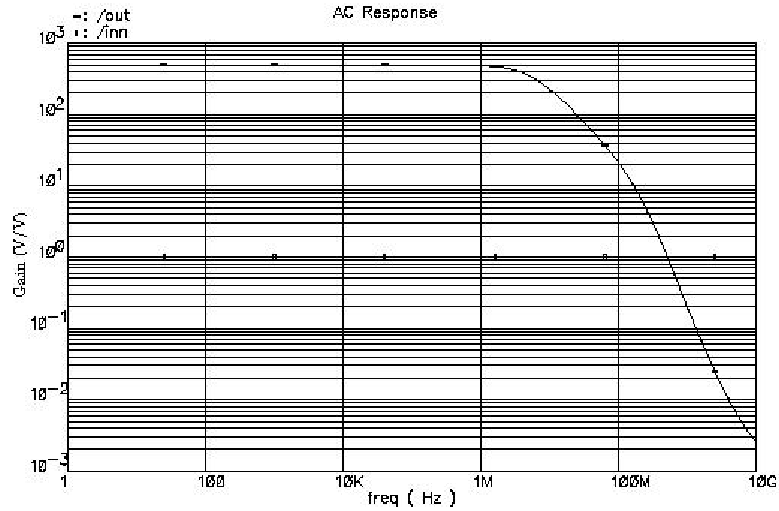


Figure 2.16. AC Response of the DUT.

Table 2.6 and Table 2.7 show the minimum error values obtained, test cost/IC, and total ICs rejected at wafer-probe testing for different yielding processes. Table 2.7 shows that all the bad ICs were detected after the AP test; hence, the coverage of the test was 100%. In addition, a significant number of bad ICs were detected at the WP test level.

Table 2.6. Accuracies achieved for specifications.

Specifications	Nominal Value	Minimum error in prediction (AP test)
Gain Bandwidth	1.1 GHz	0.73%
Phase Margin	37°	1.28%
Low Freq. Gain	53dB	0.18%
CMRR	79 dB	0.52%
DC Offset	235 μV	3.76%

Table 2.7. Comparison of test cost and ICs eliminated at WP test for different yield.

Yield	98.60%		88.40%	
Good and bad ICs	493	7	431	69
Bad ICs detected at WP test	6		53	
Bad ICs eliminated after AP test	1		16	
Savings in packaging cost	$2.10		$18.55	
Test Cost/IC	$0.018		$0.0271	

The next figures (Figure 2.17 and Figure 2.18) show the optimized test waveforms for AP and WP test.

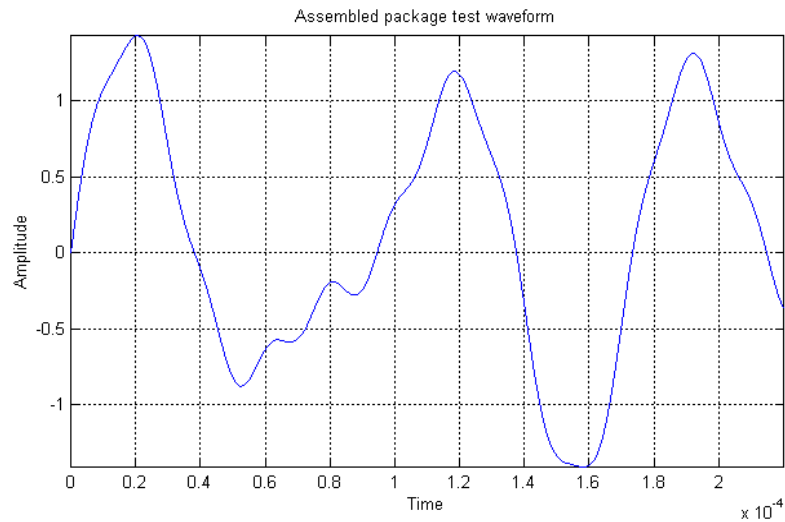


Figure 2.17. Assembled package test waveform for Case Study II.

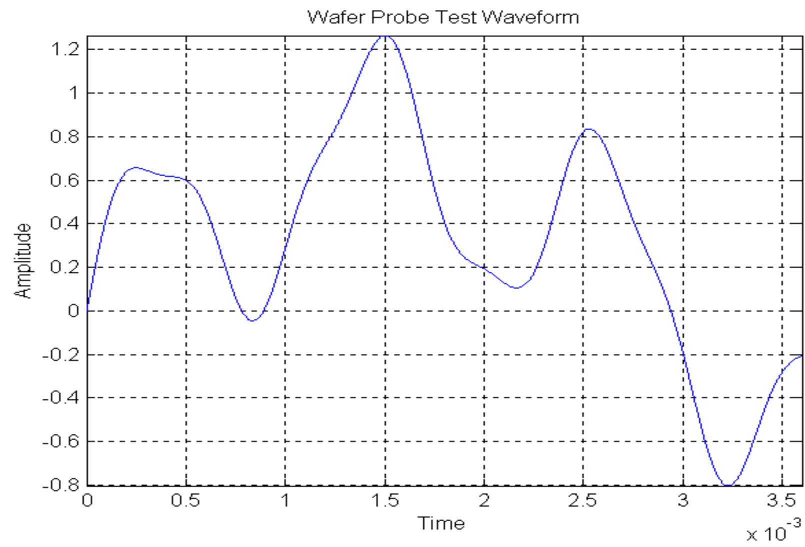


Figure 2.18. Wafer probe test waveform for Case Study II.

2.8.3. Case Study III

This example was worked out using a down-conversion mixer. The operating frequency of the mixer is 900 MHz. This example is intended to show that this methodology can be applied to RF circuits also. While accurately tracking all the specifications, large numbers of bad ICs were eliminated after WP testing. Table 2.8 and Table 2.9 show the minimum prediction error values obtained for predicting different specifications, test cost/IC, and total ICs rejected after wafer-probe testing for different yielding processes. In this case, the specifications of the individual ICs were also tracked.

Table 2.8. Accuracies achieved for specifications.

Specifications	Nominal Value	Minimum error in prediction (AP test)
THD	-64.87 dB	1.11%
Conversion Gain	-7.56 dB	0.52%
PSRR	-67.39 dB	0.94%
Noise Figure	4.53 dB	0.63%
IIP3	3.62 dBm	5.50%

Table 2.9. Test cost and ICs eliminated at WP test.

Yield	89.4%	
Good and bad ICs	447	53
Bad ICs detected at WP test	42	
Bad ICs eliminated after AP test	11	
Savings in packaging cost	$21	
Test Cost/IC	$0.0419	

The next two figures (Figure 2.19 and Figure 2.20) show the optimized test waveforms for the assembled package testing and wafer probe testing. In contrast to the previous two case studies, the assembled package test waveform duration was longer compared to the wafer-probe test waveform. The device considered here was a RF mixer, and thus the

wafer-probe test was not able to capture all the characteristics of the device under the signal limitations of the wafer-probe test.

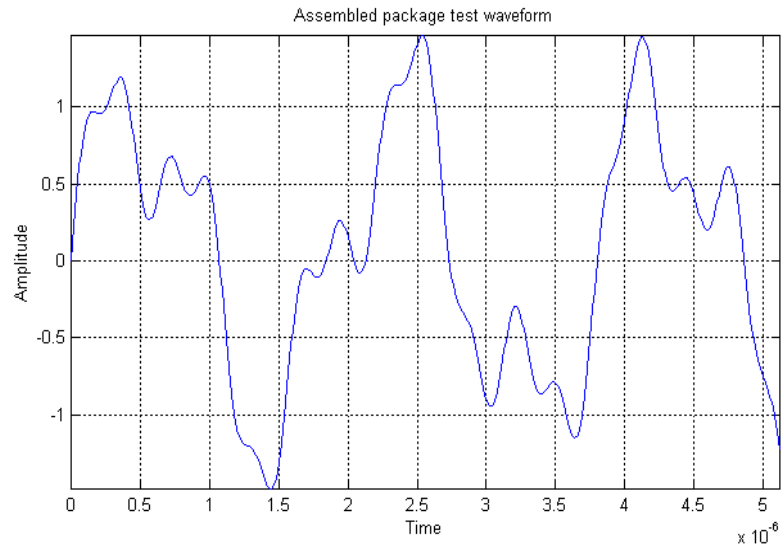


Figure 2.19. Assembled package test waveform for Case Study III.

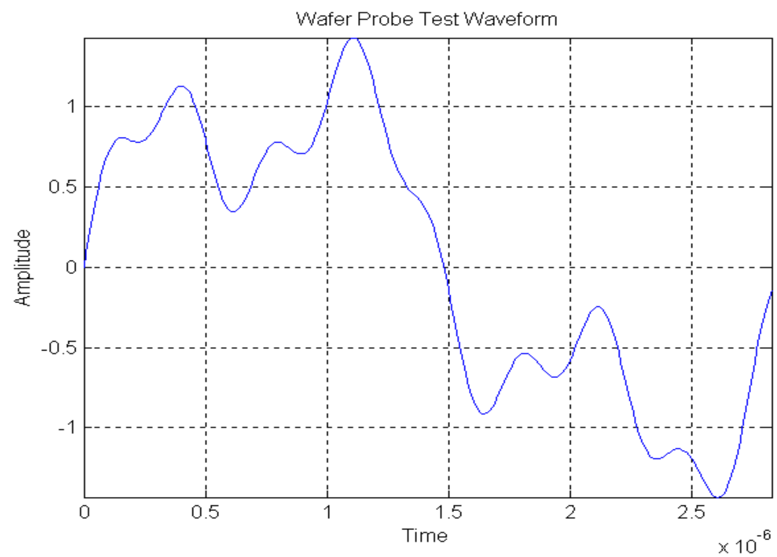


Figure 2.20. Wafer probe test waveform for Case Study III.

2.8.4. Case study IV (hardware test)

Case Study IV shows hardware test measurement data for a National Semiconductor LM318 operational amplifier. Test generation was performed for the LM318 operational amplifier based on circuit netlist and model parameter data obtained from the LM318 product datasheet [28], using the Cadence Spectre simulation. Altogether, 100 ICs were used in this experiment; 50 for test calibration and 50 for test validation. The test stimulus was applied to the circuit and captured using the PCI 6110E Data Acquisition Card [29] from National Instruments. The test calibration involves the following steps:

Apply test waveforms to the CUT and measure responses using the right printed wiring board (PWB), shown in Figure 2.23.

- Compute specifications using the left PWB, shown in Figure 2.23.
- Build regression model *"M"* relating specifications and responses from the circuit.

For validation, the obtained response was digitized using the same data acquisition card, and the test specifications of the LM318 were predicted from the data so obtained using the regression model *"M"*, as discussed above in step 3. Figure 2.21 and Figure 2.22 show the input as well as the output waveforms for both WP and AP tests. The band-limited signals for the WP test can be seen in Figure 2.22. The test waveforms show accurate tracking of the specifications.

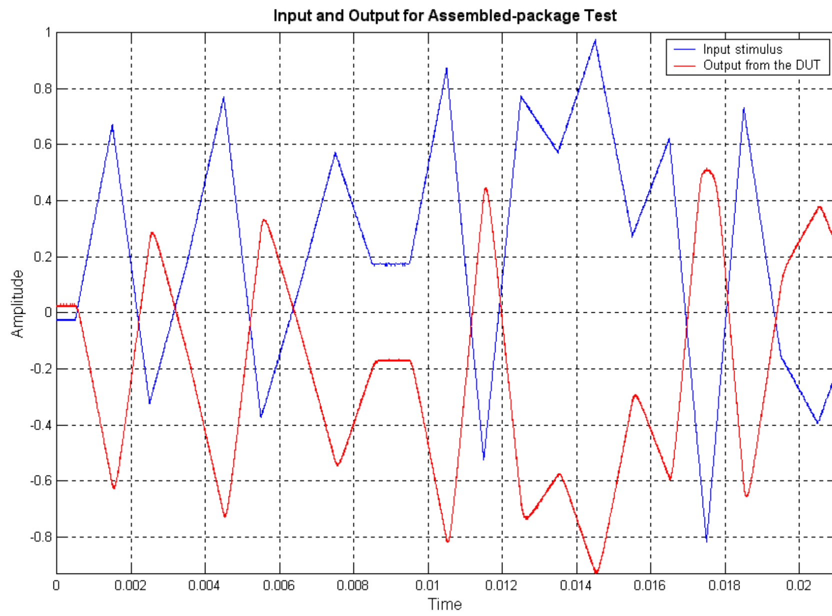


Figure 2.21. Assembled package test waveforms from hardware measurement.

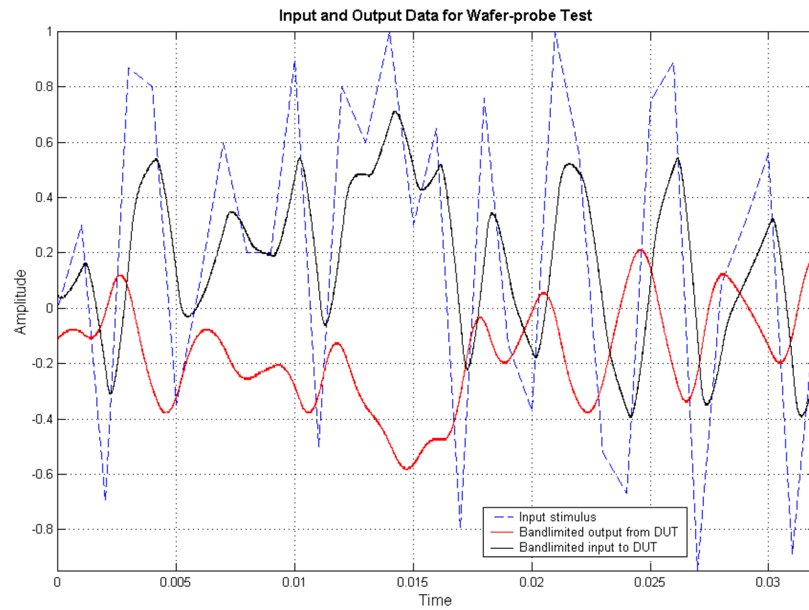


Figure 2.22. Wafer probe test measurements made on the prototype.

Figure 2.23 show the prototypes that were built for specification measurement and response acquisition purposes.

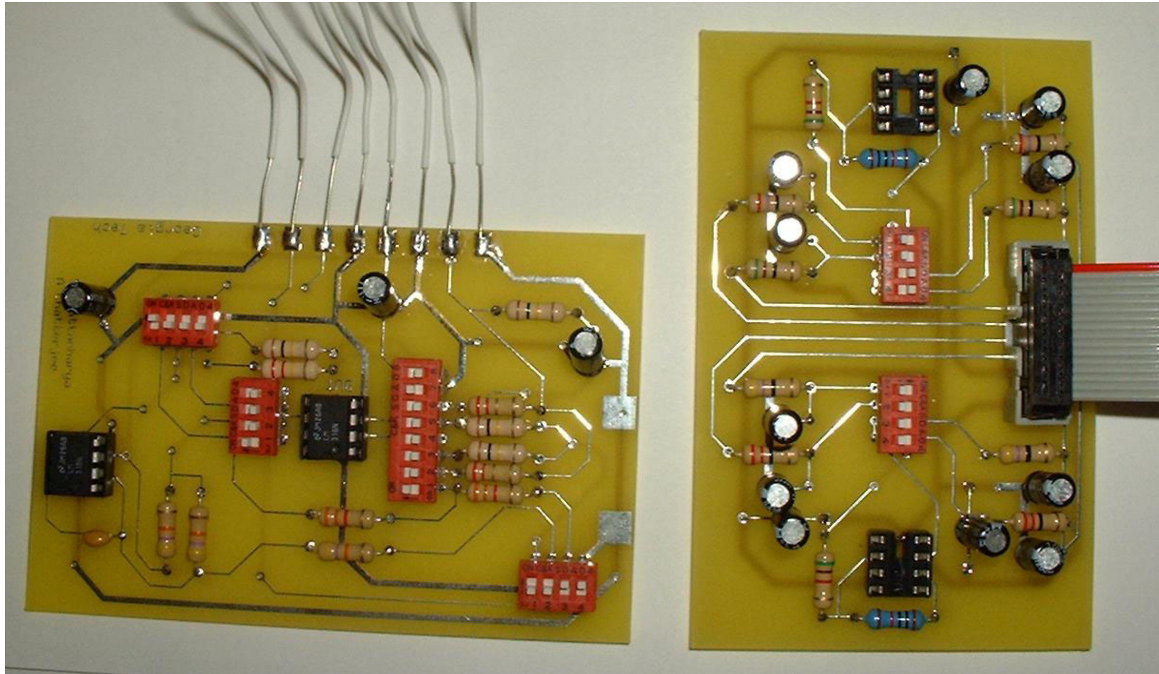


Figure 2.23. Hardware prototype used for validation purpose.

The following two tables (Table 2.10 and Table 2.11) show the specification values, error in prediction of the specifications, and the test cost.

Table 2.10. Accuracies achieved for specifications.

Specifications	Nominal Value	Minimum error in prediction (AP test)
Offset Voltage	5mV	3.68%
Open Loop Gain	84.7 dB	2.64%
CMRR	-65.56 dB	3.1%

Table 2.11. Test cost and ICs eliminated at WP test

Yield	100%	
Good and bad ICs	100	0
Bad ICs detected at WP test	0	
Bad ICs eliminated after AP test	0	
Savings in packaging cost	$0.0	
Test Cost/IC	$0.0019	

2.8.5. Cost comparison with standard specification test

Tables Table 2.12, Table 2.13, Table 2.14, and Table 2.15 show the test times, test costs and a comparison of test costs for the circuits. In some cases, test cost for the proposed method is almost 3.5 times less than the standard specification test method.

Table 2.12. Cost comparisons for proposed algorithm and standard test (Case Study I).

Yield	99%	91.6%	88.4%
WPTT (μs)	2080	2620	3710
APTT (μs)	1370	1080	2110
Test Cost/IC[1]	$0.017	$0.027	$0.031
Test Cost/IC[2]	$0.035	$0.049	$0.056
Saving[†] in Test Cost	2.04	1.853	1.797

Table 2.13. Cost comparisons for proposed algorithm and standard test (Case Study II).

Yield	98.6%	86.2%
WPTT (μs)	3600	4200
APTT (μs)	2200	3000
Test Cost/IC[1]	$0.018	$0.027
Test Cost/IC[2]	$0.047	$0.090
Saving[†] in Test Cost	2.640	3.340

Table 2.14. Cost comparisons for proposed algorithm and standard test (Case Study III).

Yield	99.8%
WPTT (ns)	2830
APTT (ns)	5120
Test Cost/IC[1]	$0.042
Test Cost/IC[2]	$0.147
Saving[†] in Test Cost	3.513

Table 2.15. Cost comparisons for proposed algorithm and standard test (Case Study IV).

Yield	100%
WPTT (ms)	22
APTT (ms)	31
Test Cost/IC[1]	$0.019
Test Cost/IC[2]	$0.07
Saving[†] in Test Cost	3.68

[1] Test Cost using proposed approach
[2] Test Cost using standard specification test method
[†] Savings is unit less, it represents the ratio of Test Cost/IC using standard specification test to Test Cost/IC using proposed approach

Chapter III
Extending Alternate Test Approach to RF Circuits and Systems

In the previous chapter, it was described how the concept of alternate test can be applied to mixed-signal circuits and systems and efficiently used to estimate the specifications of the DUT. In this chapter, the same concept has been extended to RF (0.300 GHz – 3.000 GHz) circuits and systems.

3.1. Impediments posed by RF Circuits

Before the concept of alternate test is applied to RF circuits, a feasibility study was performed to identify the impediments presented by this category of devices. In this section, the different problems that arise with testing of RF circuits are discussed and their possible solutions are presented.

3.1.1. Test generation limitation: simulation issues

Any test-generation or test-optimization approach involves multiple simulations of the netlist level description of the DUT. For alternate test-generation, multiple instances of the device are simulated with the test waveform and using a feedback procedure, the waveform is optimized to provide best estimation of specifications. Usually, for RF devices, the simulation of the DUT netlist takes longer than that compared to low-frequency devices. This is because of the small simulation time steps involved in simulating high-frequency devices. In addition, the results obtained from the RF devices are not the transient output waveforms. The previous discussion in Chapter 2 used sampled amplitude points of transient response waveform from the DUT to estimate the

specifications of the DUT. In most of the cases for RF devices, the scattering parameters, the output spectrum and many such frequency domain results may be available and are desired. To extract the transient response from frequency domain responses of the DUT via post-processing will add an extra overhead to the overall simulation time. To address these issues, many simulation techniques, viz., periodic steady state (PSS), harmonic balance (HB), have been developed to speed up the simulations, and directly obtain the results in simultaneously frequency domain and time domain.

Yet, these techniques are not adequate to reduce the overall simulation time. In cases, where the DUT is a large system, or a part of a bigger system, the simulations usually take multiple hours, sometimes days. In the proposed approach, the objective is to reduce the test time, but at the same time, the simulation time should be kept in mind so that it does not increase exponentially. To address this issue, it has been proposed to use behavioral models to simulate the DUT for test generation. This will not only reduce the overall complexity of the system or DUT, but also reduce the simulation time considerably.

The problem associated with behavioral models is that they are less accurate than the actual transistor level description of the circuit. Therefore, any simulation that are performed, will give us less accurate results. However, in this work, it has been verified that even with less accurate simulations, it is possible to generate tests that provide excellent estimations of the specifications of the circuit, when applied on the actual circuits. A comparison has been also made between the behavioral simulations and netlist simulations to verify correctness and accuracy of the method (this work is a part of Achintya Halder’s thesis).

3.1.2. Test point insertion: minimal access

In this approach, where the signals are of very high frequency, any probing of internal circuit nodes might disrupt the overall signal integrity. In RF devices, matching is a big issue for efficient power transfers from node to node. Moreover, insertion of a small parasitic might prove to be fatal, as the parasitics for these circuits are designed to be very low and the probe parasitics incurs a larger percentage error, causing a loss in signal or in some cases, creating oscillation. Therefore, in our approach, the test point insertion is kept to a minimum.

3.1.3. Waveform capture and sampling issues

The final and toughest problem posed by RF circuits is the high operating frequency of the circuit. In the alternate test framework presented earlier, the output waveform was sampled and captured. In this case, this is not practically possible. Therefore, in this approach, the alternate test framework is revised and all simulations and waveform captures are done in the frequency domain.

3.2. Remodeling alternate test approach

In the domain of wireless communication systems, there is increased impetus among system manufacturers towards integrating the base-band, IF and RF functionalities into as fewer numbers of ICs as possible. Although, this trend in general reduces form factor and improves system performance, the production test cost of these systems has been increasing as a proportion of the total manufacturing cost. This is due to the high cost of RF test instrumentation and the fact that many complex test specifications need to be determined during production test [35]-[39].

The key problems with testing RF subsystems are the following:

- The cost of testing complex RF test specifications is high and at high frequencies, the costs increase further.
- Any viable test-generation algorithm requires repeated simulation of the device under test. The cost of such repeated simulations is prohibitive for complex RF subsystems.

3.2.1. Simulation bottlenecks

Note that in alternate test, the test limits can be set so that a small number of marginal circuits are subjected to the conventional specification tests. In this way, there is no loss in fault coverage and yield due to the use of the alternate test itself. The issue of high simulation cost of RF subsystems is addressed in the following manner:

Behavioral models [40], [41] are used to simulate the RF subsystem. By perturbing the behavioral model parameters, the correlation between the perturbation in the test response due to an applied multi-tone stimulus and the corresponding perturbation in the test specifications can be monitored. In this way, it is possible to determine how accurately all the test specifications can be computed (predicted) from the observed test response.

After the tests are generated, the quality of the tests can be determined by studying how the test specifications of an RF subsystem as well as the response to the computed multi-tone AC test stimulus are affected in the presence of actual process/circuit parameter variations. From this, the quality of the computed test (discussed later) can be determined. This is a one-time simulation study as opposed to the many simulations needed during test-generation.

As shown in the literature [42], [43], variation of any process or circuit parameter, such as width of a FET, value of a resistor, etc., in the process or circuit parameter space ***P***

affects the circuit specification ***S*** by a corresponding sensitivity factor. Let ***M*** be the space of measurements (amplitudes values of subsystem output spectrum, for example) made on the circuit under test. The variations in the process or circuit parameters also affect the measurement data in the measurement space ***M*** of the circuit by a corresponding sensitivity factor. Figure 3.1 illustrates the effect of variation of process or circuit parameter space ***P*** on the specification space ***S*** and the corresponding variation of a particular measurement data space in ***M***.

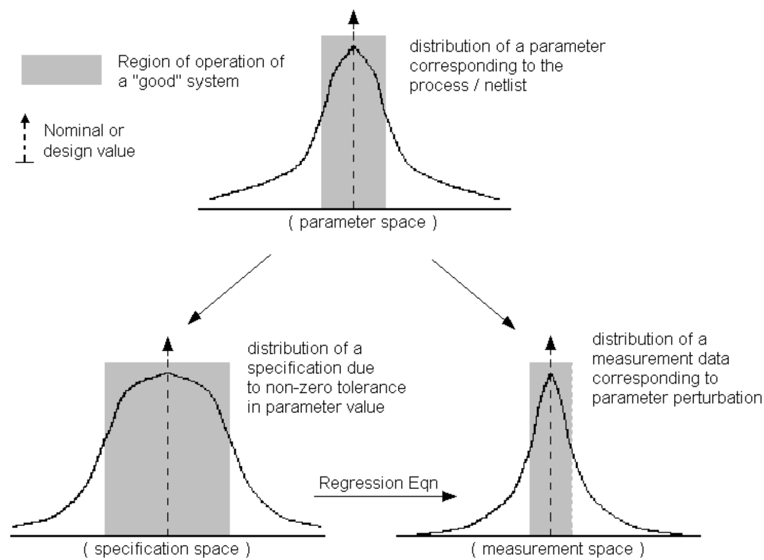


Figure 3.1. Variation in process or circuit parameter and its effect on specification and measurement.

Given the process parameter space ***P***, for the points in ***P***, a mapping function (nonlinear) onto the specification space ***S***, *f*: ***P→S,*** can be computed. Similarly, for the same points, another mapping function (nonlinear) onto the measurement space in ***M***, *f*: ***P→M****,* can be computed. Therefore, for a region of acceptance in the circuit specification space, there exists a corresponding allowable *"acceptable"* region of variation of

parameters in the parameter space. This in turn defines a region of acceptance of the measurement data in the space ***M***. A circuit can be declared faulty if the measurement data lies outside the acceptance region in ***M***.

Alternatively, as shown in [42]-[44], a mapping function f: ***M***→***S*** can be constructed for the circuit specifications ***S*** from all the measurements in the measurement space ***M*** using nonlinear statistical multivariate regression. Given the existence of the regression model for ***S***, an unknown specification of a system under test can be predicted from the measured data. In the proposed approach, MARS are used to construct the regression models and estimate the test specifications of the subsystem from the frequency spectrum of the test response waveforms. The objective of the proposed test methodology is:

- To find a simple test stimulus (e.g. the multi-tone sinusoid),
- To predict circuit specifications accurately from alternate test response.

3.3. Test Generation

Periodic bit sequences are used as test stimuli that are generated and modulated by the baseband communication subsystem of the transmitter and sent to the RF transmit subsystem under test. A random search based selection technique is used to generate the required test bitstreams. The objective of the test selection procedure is to achieve prediction error in the mapping function lower than a given error threshold. The inputs to the algorithm are:

- The packet size of the communication protocol (N)
- An error vector that corresponds to acceptable error in prediction values of different transmit and receive sub-system specifications (Δ_{ERR}).

The random search based test selection algorithm is as follows:

```
a)   Set N and Δ_ERR
b)   Select at random a new bit pattern of size N
c)   Apply the candidate pattern to multiple transceiver
     instances (generated by perturbing its behavioral
     parameters) and capture the response at the baseband of
     the receiver
d)   In parallel, measure the specifications of the transmitter
     and receiver subsystems using conventional test set up
e)   Compute nonlinear regression models (using MARS) from the
     captured baseband receiver spectrum onto the subsystem
     specifications
f)   Apply the bitstreams to a different set of transceiver
     instances and predict the specifications using previously
     computed regression models
g)   If for any specification, the maximum error in predicted
     specifications is greater than the corresponding threshold
     Δ_ERR, go to step 4
h)   Set test stimulus ← Selected bit sequence
```

Figure 3.2. Test selection algorithm.

Using the above random search based test selection method; it is never guaranteed the most optimal stimulus is selected each time. Moreover, for a very low Δ_{ERR} values, no unique test bit sequence may exist. Ideally, it is desired to have a deterministic selection process for satisfying the Δ_{ERR} error thresholds for all specifications. However, any deterministic test stimulus search method using iterative optimization over continuous search parameters, such as gradient search technique used in [44]-[46], may not be used in this problem; the test search space consists of discrete and discontinuous values. Other test ranking based approaches proposed by in [47] may be used for guaranteeing of selection of a near-optimal test stimulus. The objective of the presented algorithm is to test for the existence of such bit sequences and to show the feasibility of loop back test using these periodic bit patterns (Section 3.4).

3.4. Hardware validation

The proposed test generation methodology was validated using hardware measurements. The different modules constituting the transceiver were first characterized individually. From the data obtained, a third order polynomial curve was fitted to the transfer curves of each of the individual module to construct the behavioral models. The coefficients of the polynomial were then used as the behavioral component parameters, as described in Section 3.3. The different components and their corresponding characterization data are presented in Table 3.1. In addition, the figures below show the frequency characteristics of the different modules used to build the transmitter.

Table 3.1. Module characterization data from hardware.

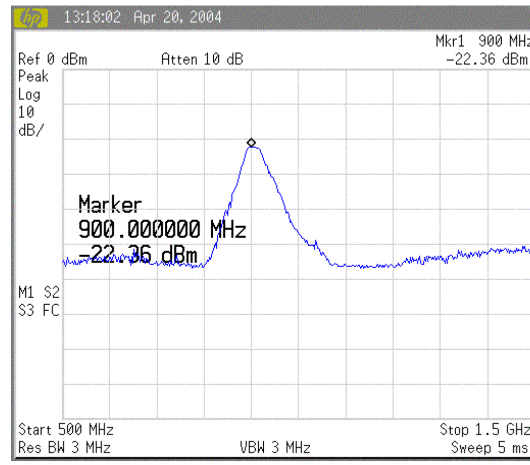
	Gain (dB)	**P-1dB (dBm)**	**IIP3 (dBm)**
Transmit Mixer	-33	2.8	15.9
Transmit Amplifier	13	3.5	16.47
Receive LNA	10	-5.1	4.6
Receive Mixer	5.8	-5.2	11
Band Pass Filter	-2.7	--	--

Using the data, test generation was performed on the behavioral models described in the Section 3.3 and the optimal test was found. The transmission system used GMSK modulation scheme with BT = 0.3. Next, transmit and receive chains were characterized separately. The characterization data for the receiver and the transmitter are presented in Table 3.2.

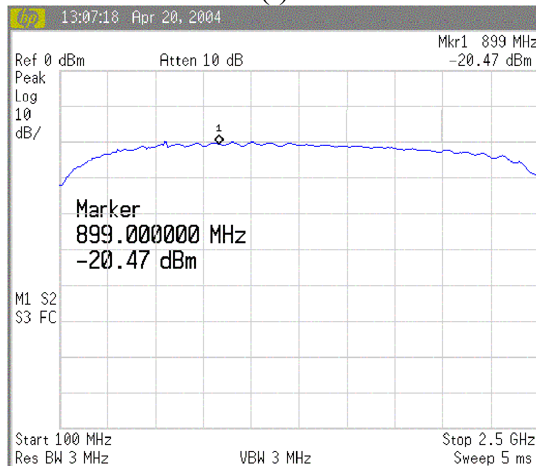
Table 3.2. Receiver and transmitter characterization data.

	Gain (dB)	**IIP3 (dBm)**
Transmitter	-1.6	15.9
Receiver	20	-1.26

As per the characterization data, first the transceiver loop was tested by transmitting a single tone (200 KHz, -16dBm) from the signal generator. The received baseband spectrum is shown in Figure 3.4. From the figure and the figures presented in Table 3.2, the channel attenuation was found to be close to -38dB.

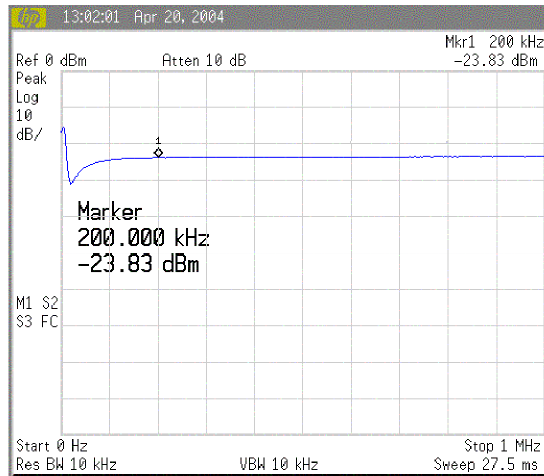


(i)



(ii)

Figure 3.3. (i) Band Pass Filter characteristics with input power = -20 dBm (ii) LNA Gain for input power = -30 dBm (iii) Receive mixer conversion gain with input power = -30 dBm.



(iii)

Figure 3.3. continued. (i) Band Pass Filter characteristics with input power = -20 dBm (ii) LNA Gain for input power = -30 dBm (iii) Receive mixer conversion gain with input power = -30 dBm.

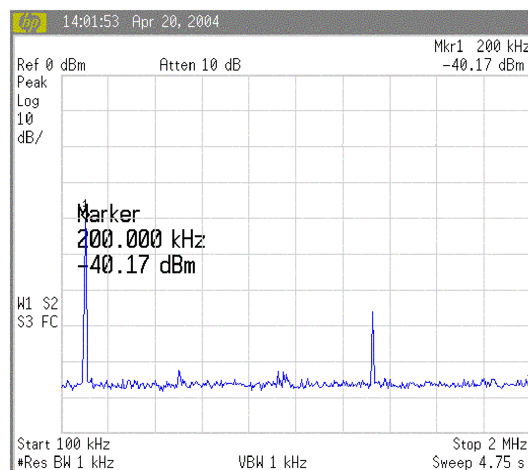


Figure 3.4. Single tone (200 KHz) spectrum received
(Note the Intermodulation tones created due to system nonlinearity).

After the characterization of the modules and the system were complete, the loop back mode was performed at the baseband level to determine the validity and spectral purity of the data acquisition card. Figure 3.5 shows the loopback test setup. The output of the setup was stabilized by controlling the power levels of the input from baseband and the LO signal power level.

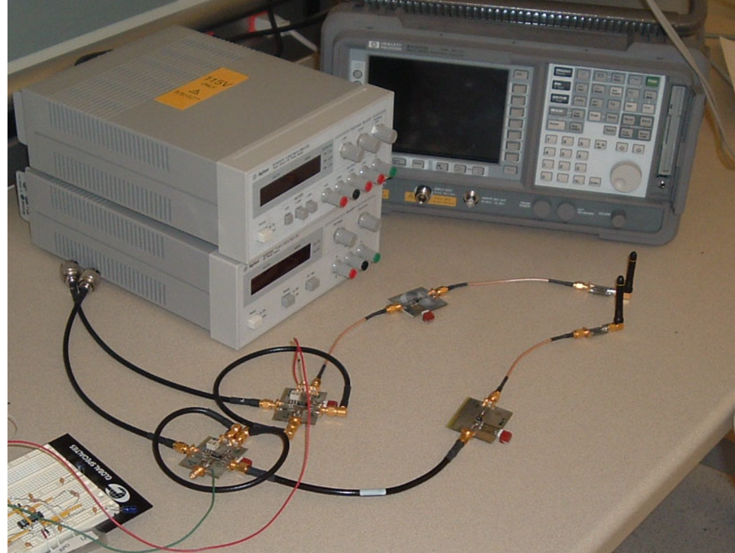
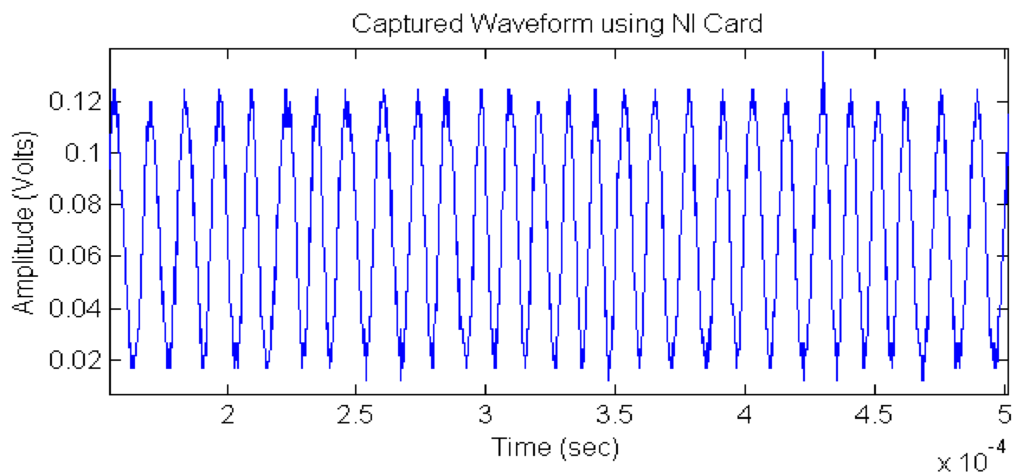


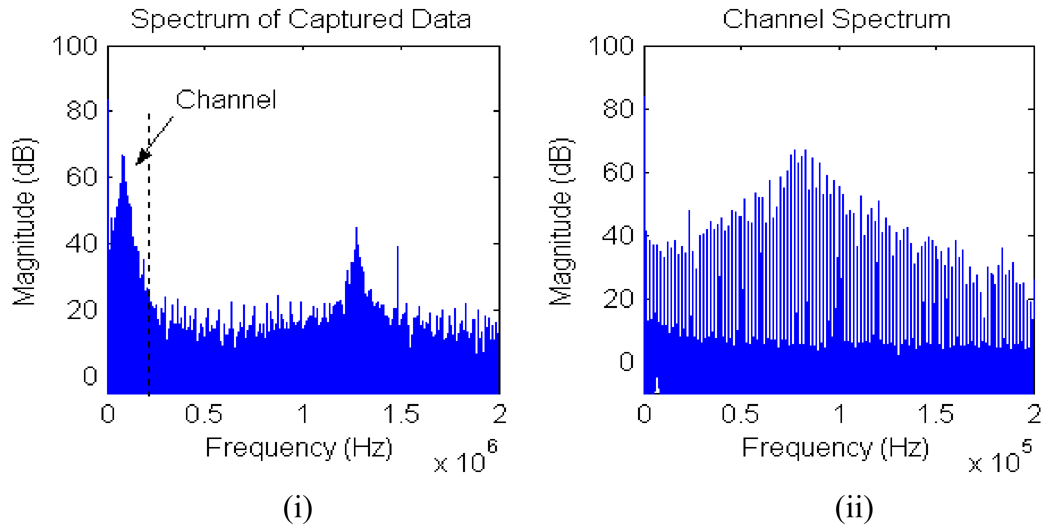
Figure 3.5. Loopback test setup for testing the transceiver.

Figure 3.6 (i) shows the captured waveform using the National Instruments (NI) data acquisition card. The spectrum of the acquired data is shown in Figure 3.6 (ii). The 0-200 KHz channel in shown in the left half figure is shown in the right half figure in Figure 3.6 (iii). (The amplitudes of the spectral components were not normalized by the sample size before converting to decibels)



(i)

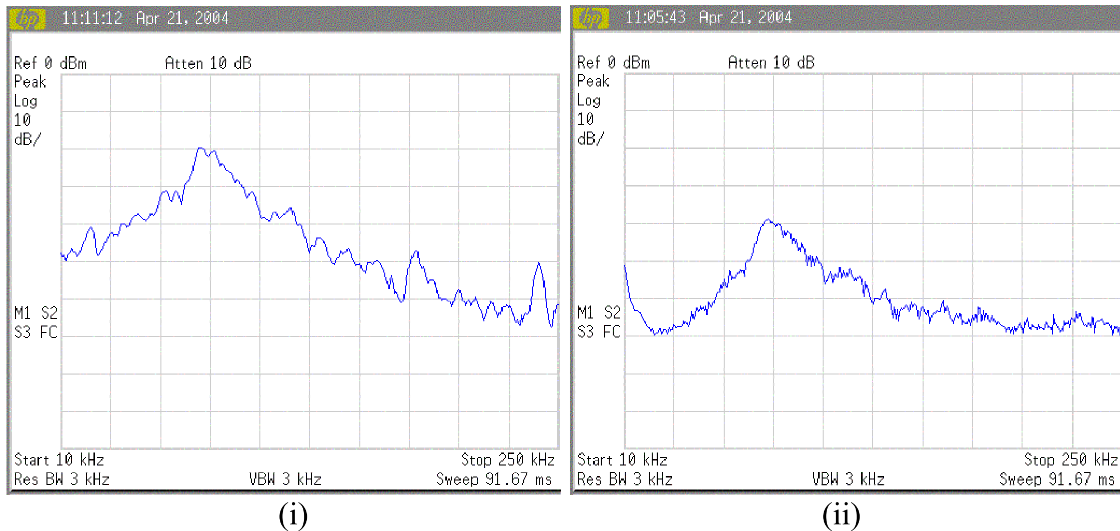
Figure 3.6. (i) Modulated waveform captured by NI Card (ii) Spectrum of the captured waveform and (iii) zoomed in spectrum for the baseband



(i) (ii)

Figure 3.4. continued. (i) Modulated waveform captured by NI Card (ii) Spectrum of the captured waveform and (iii) zoomed in spectrum for the baseband

The test stimulus obtained (explained in Section 3.3) was then GMSK modulated and propagated through the transceiver. The transmitted and the received spectrum are presented in Figure 3.7(i) and Figure 3.7(ii).



(i) (ii)

Figure 3.7. GMSK modulated spectrum at baseband (i) transmitted (ii) received.

As described in the test generation algorithm, the nonlinear model was built from the behavioral simulations. After performing the hardware experiments, the spectrum was captured and was used as the input to the model. The predicted specifications and the corresponding errors in predictions are presented in Table 3.3.

Table 3.3. Specification predicted from hardware data.

	Actual Specification	**Predicted Specification**
Receiver Gain	20 dB	19.0 dB
Receiver IIP3	-1.26 dBm	0.8 dBm
Transmitter Gain	-1.6 dB	-3.3 dB
Transmitter IIP3	15.9 dBm	20.3 dBm

Chapter IV
Impact of process variations on test generation

The necessity of on-line process monitoring was realized many years ago and people have developed numerous techniques for this purpose. In-situ sensors have been used [50] to monitor and process single wafers, which is a very standard procedure practiced in industry. In most cases, small test structures are incorporated into the device-under-test (DUT) or the wafer to gather test data. Electrical test data from these are processed on a real-time basis and rapid feedback is given to the fabrication process [51]. Failures in production are often due to small deviations or malfunctions in the equipments. Rapid diagnosis systems using response surface models for detecting small deviations and equipment models for detecting equipment failures has been widely used in semiconductor manufacturing industry [54]. Other techniques involve data accumulation from on-line test of zero-yield wafers and off-line processing of the data for process diagnosis [53].

Off-line fabrication data processing for yield improvement is also a standard technique. Earlier, patterns of parametric faults, which are specific to process defects, were used as a signature to detect bad parts [49]. Researchers have used parametric test measurements for zero-yield wafers to predict circuit as well as process parameters. Research has also shown that based on a knowledge base, using fuzzy modeling and inference engine, a set of prioritized causes for further investigation can be produced from abnormal electrical test data [51]. Diagnosis of process integration errors and process integration problems has been studied using statistical [58] as well as neural-

network techniques [59], [60]. Some other techniques involve grouping of wafers according to spatial distribution of test data and generation of a directed graph using a partitioning algorithm. Later, this directed graph can be used to put a new wafer into one of the groups and processed to figure out about the process [52]. In [53], authors developed a knowledge-based tool through simulation, called AESOP, for process diagnosis purposes. Further, a technique to reduce the dimensionality of the overall process space and later using regression and function approximation to perform spatial characterization is described in [55].

The usual problems associated with both on-line as well as off-line data analysis for process monitoring/diagnosis is that a huge amount of data needs to be stored. The software processes this data and most of the time, provides the fabrication engineers multiple reasons about the possible problems causing the process drift. This feedback cycle is usually long and it could take from weeks to some cases even months.

In this work, a new technique is proposed using a *diagnosis core* to infer about the process and circuit parameters from simple measurements made on the diagnosis core. The assumption is that within each part that is produced, the process variations are same across the whole of it, while it might be different from another part from the same wafer lot. The benefits of using this diagnosis core are:

- There is no need to store huge amounts of data for analysis and feedback purposes.
- The processing time is much less compared to standard procedures, as the data set to be handled is very small.
- The process monitoring can be implemented as real-time.

By the use of Principal Components Analysis (PCA), the length of data set to be monitored is reduced to a minimal size.

4.1. Process diagnosis

In any circuit or system, the specifications as well as the responses are a function of its process and circuit parameters. As long as the parameters are within a tolerable range, the circuit behaves as desired. However, deviations in the parameters exceeding the limits results in some or all of the specifications to go out of range and this might cause the circuit to perform poorly. Thus the process and circuit parameter space, denoted by ***P***, affects the circuit specification space ***S*** by a corresponding sensitivity factor. Let ***M*** be the space of measurements made on the circuit under test. The variation in the process parameters also affects the measurement data in the measurement space ***M*** of the circuit by a corresponding sensitivity factor. Figure 4.1 illustrates the effect of variation of one such parameter in ***P*** on the specification ***S*** and the corresponding variation of a particular measurement data in ***M***. Given the parameter space ***P***, for any point in ***P***, a mapping function (nonlinear) onto the specification space ***S***, f:***P→S,*** can be computed directly.

Using an iterative algorithm, a mapping similar to the one shown above, can be constructed from the measurement space ***M*** to the process parameter space ***P***. This will obviate the requirement to measure the specifications of a circuit and the process data can be directly be monitored by observing the changes in the response of the circuit, with certain degree of accuracy. So, we aim to construct a function ***f:M→S,*** which will directly provide us the process parameters from the measurements. Now, as the number of process parameters is numerous, PCA is used to reduce the dimensionality of the

process parameter space. Using PCA, the number of process parameters that need to be monitored is brought down to a minimal.

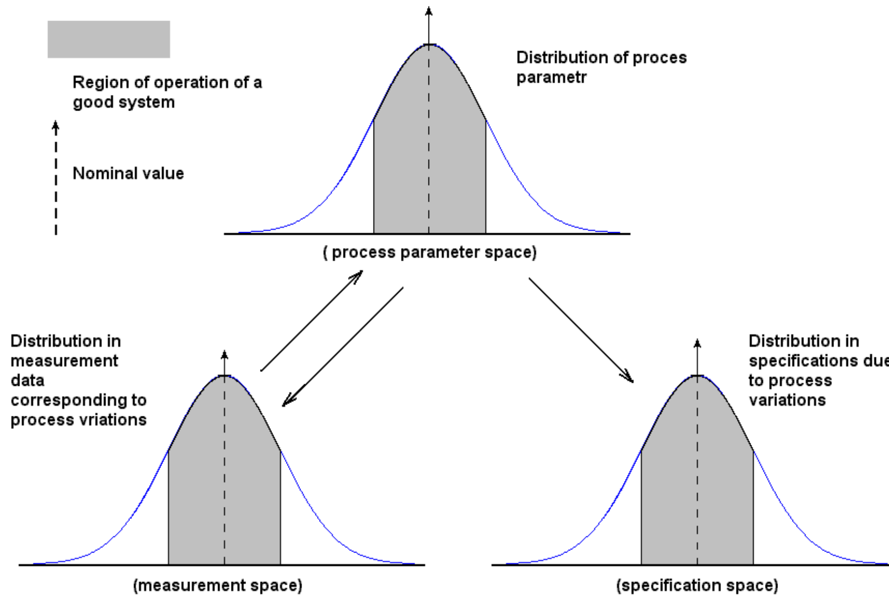


Figure 4.1. Relation between the process, specification and measurement space.

In a fabrication line, the good circuits that come out of production are not all identical and although they have specifications within the tolerable limit; the individual parts might have different specifications as well. These variations are tolerable, as long as they are within the desired limits, which in turn imply that the process parameters are under control. At the same time, for nominal or within the limits process parameter values, the measurements do not vary considerably. Now, if the process parameters start migrating beyond the allowable limits, their effects start showing up on the specification values and the measurements.

Our approach is to find a waveform, which will be sensitive to the process parameters and will give significant changes in the measurement space for small, out of the limit

parameter values. Using this carefully crafted waveform, obtained through an iterative algorithm, the process parameter values can be directly predicted from the response measurement of the diagnosis core. This will help the fabrication engineers to monitor the process closely and pinpoint any possible fault that occurs in the manufacturing line.

4.1.1. Principle components analysis

Semiconductor manufacturing typically consists of several process parameters to be monitored simultaneously. Measurement and analysis of such a large number of process parameters can be difficult. Principal component analysis (PCA) [56], [57] has emerged as an extremely useful tool for data reduction and analysis. PCA enables the reduction of a large set of correlated measurements to that which can be more easily interpreted, while retaining the important covariance information contained within the data. A graphical interpretation of principal component analysis is provided in Figure 4.2(a). Coordinates x_1 and x_2 indicate two zero-centered measurement variables with sample data represented by the black points. The projections of the standard deviations σ_1 and σ_2 onto vectors v_1 and v_2 provide information regarding the "natural" coordinates of the data. By rotating the original axes x_1 and x_2 onto the more natural coordinates v_1 and v_2, an orthogonal space is found where the primary axes align along the directions of maximum variance. In Figure 4.2(b), the experimental data indicates a linear relationship between the two measured variables x_1 and x_2. By rotating the coordinate system along the direction of maximum variance in the data, the two measured variables can be well represented by only one variable v_1. PCA provides the direction of maximum variance in the data; in this case, the projection of x_1 and x_2 onto the first principal component direction changes the dimensionality of the data from 2 to 1. Once the principal components are determined,

subsequent measurements can be projected onto the natural coordinates or principal component directions to reduce the overall dimensionality and these projections can be plotted to determine linear or nonlinear correlations in the data or to indicate variables, which may be omitted.

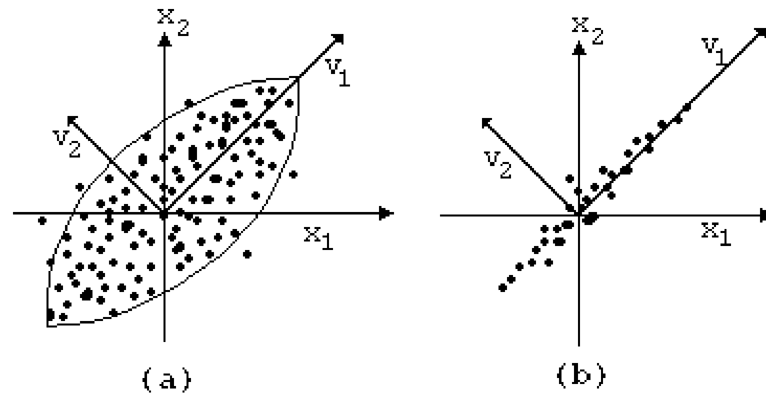


Figure 4.2. Reduction of dimensionality of data using Principal Component Analysis (PCA).

4.1.2. Test generation for process diagnosis

The test generation procedure finds a waveform, the response of the diagnosis core to which is sensitive to the perturbations in the process parameters. The sampled response of the diagnosis core is mapped to the process parameters using regression models and the process parameter values are obtained.

4.1.2.1. Test generation algorithm

The test generation is started with a set of piece-wise linear waveforms. For each waveform, a statistically generated set of process parameter values, around the nominal values are applied to the circuit and the response is sampled and stored. Each set of process parameters is called a process vector. Thus, for *N* such process parameter vectors,

N sets of vectors consisting of sampled response are obtained. This is repeated for each of the waveforms. For each such waveform, a non-linear regression model is built relating the responses and the corresponding process parameters.

The models constructed for all the waveforms are then evaluated using a new set of process parameters. The fitness of a model is determined by how well it is able to predict the process parameters from the response of the circuit. This metric is used as a measure to choose the waveform and thus, the waveform that delivered maximum accuracy is chosen as the optimum waveform for process diagnosis. Using genetic algorithm, the next population of waveforms are generated from the selected one, through the process of mutation and crossover. This procedure was continued until the desired accuracy is achieved. The algorithm is shown in Figure 4.3.

For the response of the circuit, DC operating point, its output transient current as well as the transient voltage was considered. It was observed that, by considering the transient current values with voltage values, greater accuracy could be achieved compared to when only transient voltage was considered.

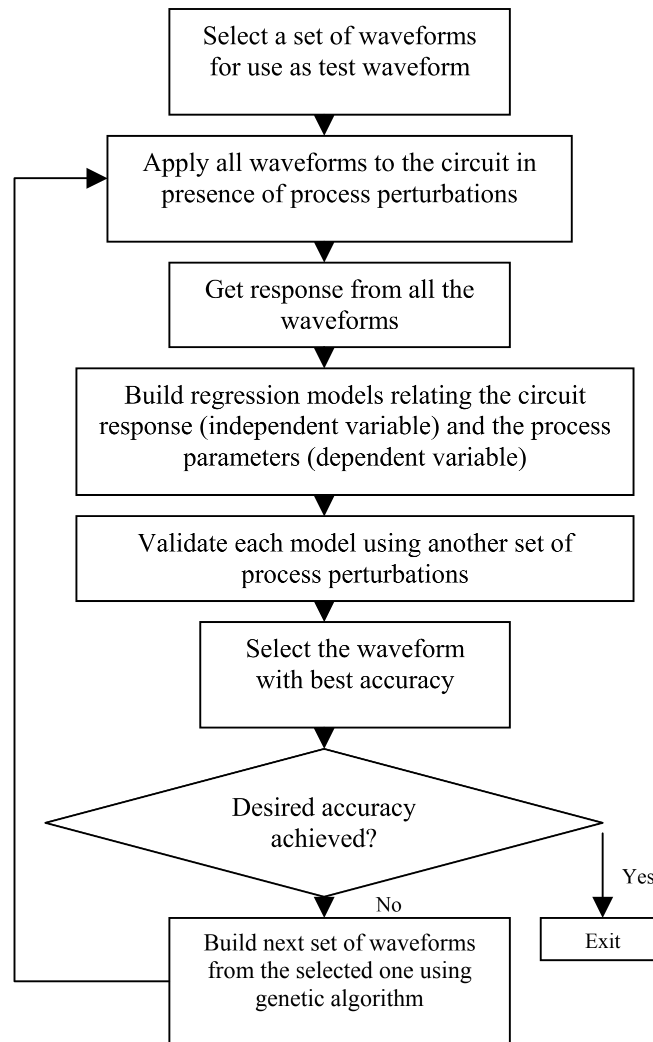


Figure 4.3. Flowchart showing test generation algorithm for process diagnosis.

4.1.2.2. Using PCA to reduce the data set

After the best waveform was found and the desired accuracy was achieved, the process parameter set was reduced using PCA. Initially, a number of process and circuit parameters were considered for building and validating the models. After reduction, the final data set was generated for the first few principal components. After the data dimension was reduced for the process parameters; the parameters causing the most variation in the measurement data set were retained, while the others were dropped.

Using this new parameter space, the model was reconstructed for the chosen waveform. This final model can be used to predict the process parameters from the measurements directly.

4.1.3. The diagnosis core

The diagnosis core was designed to respond to process variations. The measurements made on the *diagnosis core* are sensitive to process perturbations. It can easily be incorporated on-chip, with a bigger system. By doing this, the bigger system, which is often difficult to test, need not be tested at all. By making very simple measurements on the circuit, inference can be drawn about the state of the fabrication process. As shown in Figure 4.4, the input and output signals of the diagnosis core do not interfere with the main circuit. Therefore, measurements made on the diagnosis core are not going to affect the main circuit in any way. In addition, the space occupied by the core is very small compared to the main circuit area. Thus, it will not be a problem to put this circuit in any bigger system. The circuit consists of approximately 40 transistors, a bandgap reference circuit, load and bias resistors.

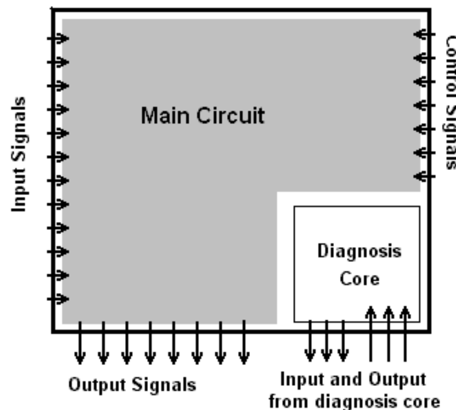


Figure 4.4. Diagnosis core embedded in a bigger circuit.

This circuit can be perturbed at wafer probe as well as assembled package test to collect the test data for process diagnosis. At the wafer-probe test, bandwidth and current drive limitations are presented by the wafer-probe test instrumentation. So, if tested at wafer probe, the test waveform might get modified considerably during input and also the response of the circuit to the test waveform might also get attenuated due to the probe parasitics. Therefore, special care needs to be taken if this is tested at wafer probe test. Figure 4.5 shows a part of the diagnosis core that was used in this work. The circuit consists mainly of mixer, oscillator and operational amplifiers. The choice of the different devices was made based on the capabilities of these circuits to respond to the process variations of interest to us. The different parts were specifically designed to get insight about the different parameters of the circuit as well as the process itself. The oscillator, which is a tunable VCO, is used to drive the mixer. The oscillation frequency is 50 MHz. The mixer has a conversion gain of –2.3dB at 50MHz. The mixer IIP3 is -20 dBm. The operational amplifiers used were differential input, single-ended output devices, with gain of 55dB and unity-gain bandwidth of 750MHz.

The circuit also uses a constant DC current mirror circuit, designed using MOS devices. The supply current for the circuit was 1.2mA, with power dissipation being 5.5mW. Pad models were used for all input and output pins. The transient outputs of the circuit were sampled and the transient and DC currents were noted for building the regression model. The circuit was designed with TSMC 0.35um technology. The next section presents the results obtained from the measurements made on the circuit.

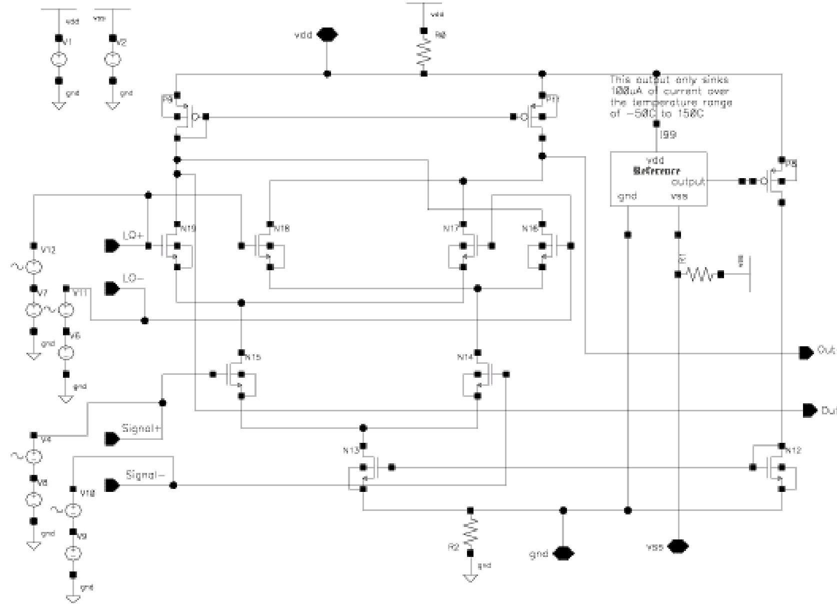


Figure 4.5. Part of diagnosis core (mixer).

4.1.4. Results

This section presents the results obtained from simulations performed on the diagnosis core for process perturbations. The circuit process and circuit parameters were perturbed for the netlist, and measurements were made on the circuit, while the test-waveform obtained was applied to the circuit. Initially, 51 process and circuit parameters were considered. The test generation was performed with all the process parameters and the response of the circuit for these parameters perturbations was noted. The response measurements showed noticeable variation in the response space. The model was able to predict the process parameters very closely in some cases, with very little variation in the standard deviation.

Next, the data set for the process parameter was reduced using PCA from the data obtained from the model. Only the first 10 parameters were chosen for the final model generation purpose and they explained 98.6% of the total variability for the process

perturbation space. Figure 4.6 shows the percentage of variability explained by the first 10 principal components. The top 10 components were as listed below in Table 4.1 and their corresponding accuracy values, as predicted by the model.

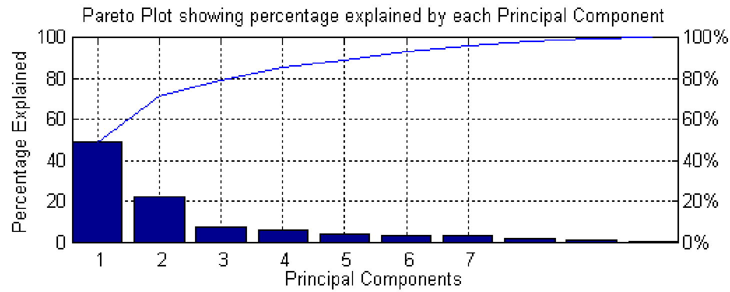


Figure 4.6. Pareto plot showing contributions by each principal component

Table 4.1. Process parameters and their accuracies.

Component	**Error in Prediction (%)**
Oxide thickness	5.81
Length variation due to etching and masking	1.30
Width variation due to etching and masking	2.46
Coupling capacitor	4.88
Feedback resistor	0.75
Substrate doping	2.14
Lateral diffusion length	5.74
Fast surface states	1.51
Junction depth	6.67
Gate-source capacitor	4.15

The new data sets, i.e. the principal components are a weighted combination of the different process and circuit parameters. Figure 4.7 shows a plot showing the data after transformed into the new data sets. Here, principal component 2 is plotted against principal component 1. From the figure, it can be seen that the outlier ICs, i.e. the bad ones, can be easily detected.

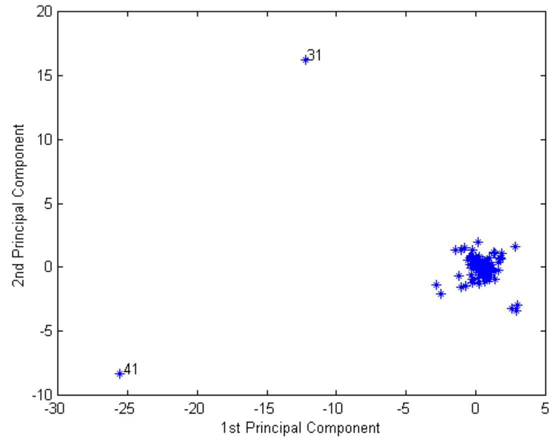


Figure 4.7. The first two principal components on the new set of axes.

Chapter V
Production Test Techniques for UWB Devices

Recently, Ultra-wide Band (UWB) has emerged as the standard of choice for short-range, high data rate communication (for WPAN environments), replacing existing standards viz. Bluetooth. UWB devices can operate from 3.1 GHz to 10.6 GHz, with a maximum PSD of –41.3 dBm/MHz. UWB is based on overlay technology, as it can coexist with other standards by sharing the spectrum [62]-[64]. UWB uses two transmission modes: pulse based and OFDM. While the pulse-based mode uses the entire frequency spectrum available to UWB, OFDM divides the frequency range into multiple bands, giving it the name Multi-band OFDM (MB-OFDM) [65].

5.1. Production testing of UWB devices

Production testing of UWB transceivers involves testing for interference immunity, error vector magnitude (EVM), complementary CDF (CCDF), bit error rate (BER), etc. The different specifications and their significance to production testing are described in the following subsections.

5.1.1. "In-band" interference

The UWB standard is proposed as an overlay technology due to its ability to co-exist with existing standards. Although, sharing the spectrum with UWB does not hamper the functionality of other standards considerably, the operation of a UWB device can be significantly affected by interference from other wireless data transfer protocols. This is known as *"in-band"* interference and it affects the sensitivity of the UWB receiver

significantly. To ensure proper operation, a UWB device needs to maintain a very low BER even in the presence of an interference signal. In this paper, we study the effect of IEEE 802.11a (WLAN) signals (5.15-5.35 GHz and 5.725-5.825 GHz) and various other interference sources on the BER of pulsed and OFDM UWB devices.

5.1.2. "Out-of-band" interference

As UWB devices have a wide bandwidth, during operation, it is possible for the energy to be transmitted beyond the allowed spectrum limits. The energy that spills outside the frequency band acts as an interfering signal for other standards, known as *"out-of-band"* interference. In production test, it is thus necessary to test UWB transmitters for spectral energy leakage out of its frequency band of operation.

5.1.3. EVM and CCDF

The EVM test is performed to measure the amount of nonlinearity introduced by the transmitter. For UWB devices, the sources of non-linearity include the phase noise of oscillator, nonlinearities from D/A converter and transmit mixer. On the other hand, CCDF test determines the peak to average ratio of the transmitted signal. In addition, it provides a design guideline for the required dynamic range of the RF front-end.

5.1.4. BER test

BER is a system level specification that measures the number of erroneous bits received in a fixed number of transmitted bits (usually large). It is a fundamental measure of system performance, as it is sensitive to system non-idealities as well as signal-to-noise ratio, distortion. BER testing quantifies the ability of the system to receive information error-free. This determines the quality of the communication link.

5.2. Production test of UWB devices: pulsed and OFDM

5.2.1. Pulsed-UWB

5.2.1.1. Transmitter tests

Pulsed-UWB systems use a train of modulated pulses to transmit the data. Due to the high-occupied bandwidth of these devices, the spectral co-existence properties of UWB devices need to be carefully characterized and measured during production test. Therefore, "out-of-band" interference test is very important for pulsed-UWB transmitters and we develop a methodology to test this specification efficiently during production test.

5.2.1.2. Receiver tests

Pulsed-UWB receivers use a correlator and a sample and hold circuit to decode the transmitted bits [66]. Any interfering signal affects the error sensitivity of the receiver and increases the probability of error for bit '0' and bit '1'. In this paper, we consider narrowband interference sources (viz. WLAN) affecting the error probability in UWB receivers. Production testing of the UWB devices for BER/*error probability* (P_e) in the presence of interference requires a minimum number of bits to be transmitted and decoded at the receiver to compute the P_e. The number of bits transmitted during the production test procedure is inversely proportional to the target P_e of the device. For low interference levels, P_e is small, indicating a large number of bits required for testing. The results in a long production test time. Increasing the level of interference increases the error probability of the received UWB data.

5.2.2. OFDM UWB

During high-volume manufacturing (HVM), production testing of wireless systems includes testing for specifications related to gain, output power, nonlinearity, clock jitter/phase noise, BER etc., for regulatory transmission mode compliance.

5.2.2.1. Transmitter tests

Production test of UWB transmitters includes measurement of specifications viz. output power level/power spectral density (PSD), spectral mask compliance test, complimentary cumulative distribution function (CCDF) [67]-[68] and error vector magnitude (EVM) [68]. As UWB transmitters are low-power devices, ACPR and other nonlinearity-related specification tests are not performed during production test. Among all the specification tests performed on UWB transmitters, EVM and CCDF are inherently complex in nature [69]. EVM is the RMS value of the magnitudes of all the error vectors between the transmitted (desired) and received (actual) constellation points. CCDF is used to analyze the power statistics and is defined as the peak-to-average ratio of the transmitted signal.

5.2.2.2. Receiver tests

For UWB receivers, BER test and its tolerance to "in-band" interference is a very important specification that is tested during manufacturing test. Other specifications that are tested during production test include sensitivity, "in-band" interference and synchronization related specifications. In this paper, we concentrate on BER testing of UWB devices.

5.3. Significance of proposed research

Direct measurement of the UWB test specifications described above are time-consuming and places stringent requirements on the test equipment/ATE, resulting in increased test cost of UWB devices.

Earlier work [70]-[75] on the coexistence capabilities of pulsed-UWB with other standards focused mainly on characterizing the standard and developing an accurate model for the indoor channel [76]-[78]. We study the effect of interference on BER of a UWB receiver system and develop a test methodology for the same. The purpose of this work is to study the effect of narrowband interference signals on UWB receiver performance and devise a method for estimating the probability of error at very low interference levels using an *alternate test stimulus*, suitable for production test environment. In addition, test of pulsed-UWB devices for "out-of-band" interference is studied and test methods are developed that provides fast and highly repeatable results in a production test environment.

In the past, different design and performance aspects of OFDM-based UWB systems for various specifications have been studied [79]-[80], to help reduce the manufacturing cost of these devices. However, production test scenarios for minimizing overall test cost of these devices have not been fully explored. Test cost has been increasing over the last few years and constitutes a significant portion (up to 40%) of the total manufacturing cost for present-day wireless products [81]. Since UWB devices have a large market, it is necessary to manage their test costs carefully. We study the MB-OFDM UWB transceiver systems and propose techniques to enhance production test for EVM, CCDF and BER specifications. The significance of the proposed work is due to its potential to

perform production test MB-OFDM UWB devices by applying simple test stimulus using low-cost ATE.

5.3.1. Key contributions

Test time and equipment costs are major contributors to the overall test cost in a production test environment. To address the issues related to test, innovative production test techniques that optimize the test cost and coverage are therefore necessary. The key contributions of this work are to:

- Develop '*alternate*' test [82] techniques for MB-OFDM UWB devices that reduce test time significantly
- Allow production testing of UWB devices using low cost test hardware/ATE

5.4. Pulsed-UWB devices

5.4.1. Pulsed-UWB basics

A UWB transceiver uses very short duration pulses, typically of the order of nanoseconds to transmit data. In most cases, the pulses used for transmission correspond to the second derivative of a gaussian pulse, as it provides the desired spectral shape, conforming to FCC standards. The equations for both gaussian pulse and its 2nd derivative are shown in (10) and (11), respectively.

$$w(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(t-\mu)^2 / 2\sigma^2} \quad (10)$$

$$w''(t) = p(t) = \frac{1}{\sigma^3\sqrt{2\pi}} \left[\left(\frac{t-\mu}{\sigma} \right)^2 - 1 \right] e^{-(t-\mu)^2 / 2\sigma^2} \quad (11)$$

There are two possible modulation schemes used to transmit the pulses – Bi-phase modulation (DS-UWB) and Pulse position modulation (PPM), also known as TH-UWB, where DS and TH stand for *direct sequence* and *time hopping*, respectively. DS-UWB

employs a transmission scheme where each bit is encoded using a *spreading code* that determines the time slot when the pulse is transmitted. The spreading code is kept the same for all bits during DS-UWB transmission, and a pulse is transmitted in the time slot corresponding to the value of the spreading code. If the width of each time pulse is t_p, the time gap between two pulses is given by t_p*2^D, where '*D'* denotes the number of bits used in the spreading code. If *N* pulses are transmitted for every bit, then the bit duration is given by $Tb = N X t_p X 2^D$.

Before transmission, the generated pulses are passed through a band pass filter, which shapes the pulses and limits any out-of-band emissions to satisfy FCC limits. TH-UWB uses a more complex modulation scheme in which each monocycle is given a distinct extra delay and the spreading code is different for each bit. The spreading code, also called the hopping sequence is a pseudorandom sequence. TH-UWB is not considered here and we shall confine our analysis to DS-UWB.

5.4.1.1. Transmitter architecture

The pulse-based UWB transmitter includes a pulse position (TH-UWB)/pulse polarity (DS-UWB) modulator, followed by a pulse generation unit and finally, a spectrum shaper to reduce the "out-of-band" interference. The transmitter architecture is shown in Figure 5.1.

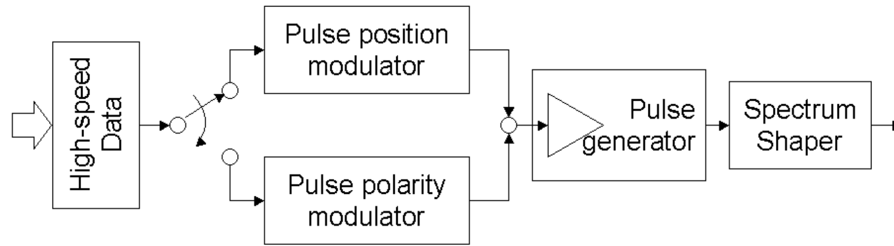


Figure 5.1. Pulsed-UWB Transmitter.

5.4.1.2. Receiver architecture

The UWB receiver consists of a correlator, which is composed of an integrator, followed by a Sample and Hold (S/H) block, as shown in Figure 5.2.

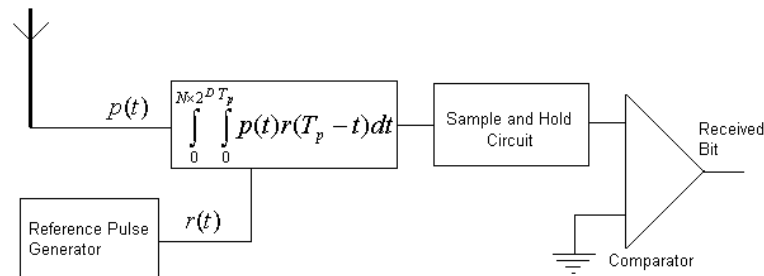


Figure 5.2. UWB receiver architecture.

The receiver has a reference pulse generator (also called *reference pulse generator*) unit, which creates the transmitted pulses for bit '1'. The received waveform is correlated with the *reference pulse generator* output over a one-bit duration (T_b) and the correlator output is sampled at the end of the bit duration. The S/H output is reset after every bit is received. Thus, each received bit is *independent* of the previous bits. It should be noted here that the reference pulses generated correspond to a '1' bit. Thus, if a '1' is received at the correlator input, the output at the end of one bit period is a positive value, which is

then sampled as a ‘1’ by the receiver. If the received bit is a ‘0’, the corresponding correlator output at the end of one bit period is negative, which is detected as a ‘0’.

5.4.2. Standard production test methods for pulsed-UWB devices

5.4.2.1. “Out-of-band” Interference

The standard production test method for “out-of-band” interference uses two separate tester load boards. The first load board contains the UWB transmitter, and the second one contains antenna/multiple antennae for capturing the signal within the band of interest (Figure 5.3).

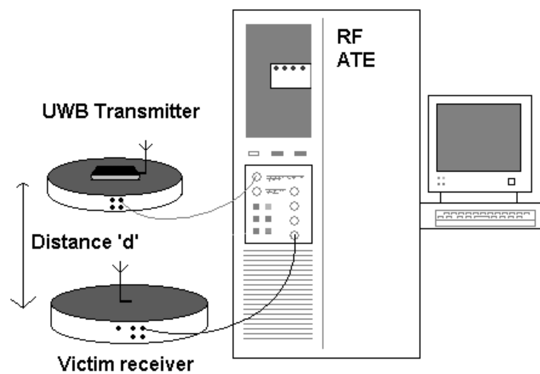


Figure 5.3. Test setup for standard production test of UWB devices.

There are some issues to consider with this test setup. First, as the test signal propagates through the air medium, the tests may not be perfectly repeatable. Second, the cost associated with this test is larger, as two separate load boards must be used (to test the amount of interference with varying distance between the transmitter and the receiver).

5.4.2.2. "In-band" interference: effect on receiver sensitivity

In production test, a UWB transmitter is used to generate the test waveform. The interfering signal is generated from a RF signal generator, which is interfaced with the ATE through GPIB. The interference signal is combined with the test waveform from the UWB transmitter and input to the receiver. The receiver decodes the data and sends it back to ATE. By comparing the transmitted and received data, error probability values and degradation due to presence of interfering signals can be measured.

We model the interference signal with a single tone, as the UWB signal bandwidth is much larger compared to the bandwidth of the WLAN signal. The WLAN signal frequency is chosen as 5.1GHZ, with an associated random phase $\theta(t)$. The phase noise component of the signal is assumed to have a peak phase deviation θ_{pk} = 10°, with a periodically varying phase term. The signal can be modeled as shown in (12),

$$I(t) = A\sin[2\pi f_c t + \theta(t) + \theta_{pk}\sin(2\pi f_m t)] \tag{12}$$

where, A=amplitude of the interference signal, f_c = 5.25GHz, and $f_m = f_c/1000$.

In the following discussion, all the analysis presented is for a bit '1'. The methods, proposed solution and the results for bit '0' are the same. Thus, in presence of interference and channel noise (which we assumed to be AWGN), the received signal is

$$r(t) = p(t) + I(t) + n(t) \tag{13}$$

The reference pulse generator generates a waveform similar to the one transmitted, which is correlated with the received signal, $r(t)$. Thus, the correlator output is given by,

$$\begin{aligned} c(t) &= \int_0^{N\times 2^D}\int_0^{t_p} r(t)R(t_p - t)dt \\ &= \int_0^{N\times 2^D}\int_0^{t_p} p^2(t)dt + \int_0^{N\times 2^D}\int_0^{t_p} I(t).p(t)dt \end{aligned} \tag{14}$$

[Note: $R(t_p\text{-}t)=R(t)$ and $p(t) = R(t)$ for $0 \le t \le t_p$]

Notice the noise component has been ignored in the above equations, but was included in the simulations performed. Close observation of the above equation reveals that the first term is always positive for a bit ‘1’ (negative for a bit ‘0’), irrespective of the pulse waveform used for transmission. Thus, for an error to occur for bit ‘1’, the second term needs to be more negative than the first term (more positive for a bit ‘0’). If no interference is present ($I(t) = 0$), all the bits are correctly detected, and the error probability is 0.

The probability of correct detection of ‘1’ can be formulated as $p(1) = p[c(t)|_{t=Tb} > 0]$. To obtain a closed form equation to estimate the probability of error for a bit in the presence of interference, we need to integrate (14) to find $c(t)$. While the first term of (14) can be evaluated, the second term, which has the form,

$$f(x) = \iint x^2 \sin(x) e^{-x^2} dx \qquad (15)$$

is not integrable. Thus, the only way to obtain an estimate of the error probability is to use numerical methods for integration. The S/H circuit samples $c(t)$ at $t=T_b$ to determine the value of the received bit. The random phase $\theta(t)$ in (12), is uniformly distributed and can take any value in $(0,2\pi)$. The variation in the sampled value at the instant $t=T_b$ due to variations in $\theta(t)$ is shown in Figure 5.4.

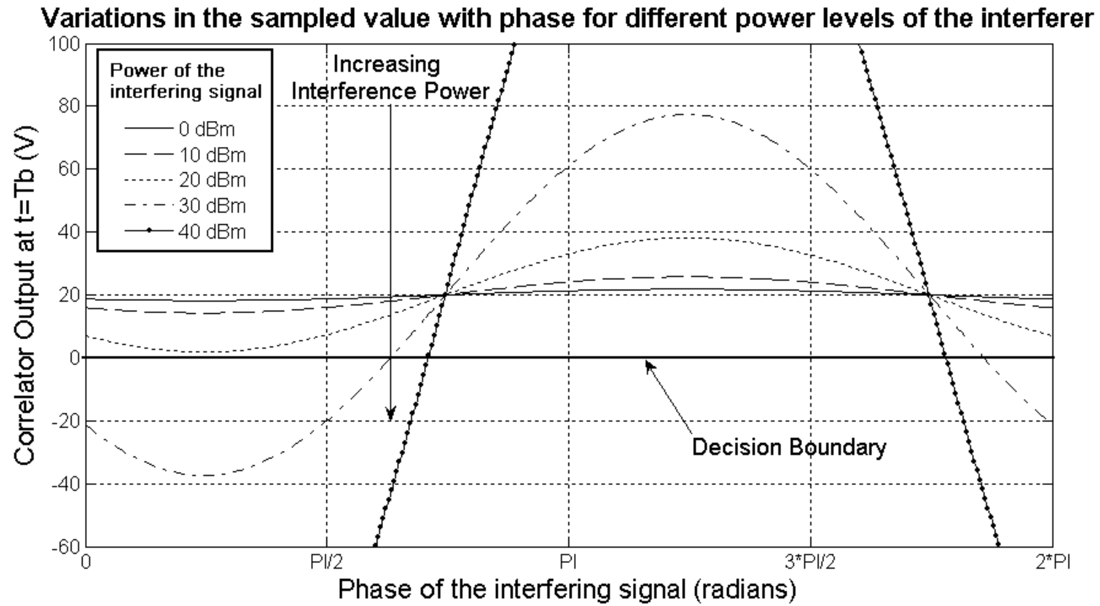


Figure 5.4. Variation in sampled value with change in phase of the interferer signal (for multiple power levels of the interferer).

In Figure 5.4, the decision boundary for detecting bits is shown by a solid horizontal line. From the figure, the positive offset due to the first part of the integral in (14) can be easily seen. It is evident from the figure that the higher levels of interference start causing bit errors as the sampled value starts taking negative values at certain phase values, thus increasing the error probability. But, due to the unknown variables associated in (12) and highly nonlinear nature of (14), it is not possible to construct a direct linear relationship between *p(1)* and the interfering signal.

5.4.3. Proposed test methods

5.4.3.1. Proposed “out-of-band” interference test

We study the effect of interference on the GSM900, DCS and PCS bands due to UWB transmission. The presented methodology can be easily extended to other standards (e.g. RAST, UNII). The proposed method uses a different approach and eliminates the above-

mentioned problems with very little test overhead added. However, additional analysis is required to properly interpret the test results.

The first step involved in the production test plan is to develop an accurate channel model and to characterize the channel in which the UWB device will operate in the target environment. Once the 'worst case' environment (channel) model in which the UWB device will operate is determined, a production test sequence can be designed to ensure that the UWB device interference to other standards will be insignificant during normal operation. With an accurate channel model, the overall channel attenuation and the associated path delay can be estimated for a specific position of the victim receiver with respect to the UWB transmitter. In the proposed approach, using a programmable attenuator and a delay unit, the UWB transmitter and the victim receiver's input filters (antenna is no longer required, as this uses a wired connection between the transmitter and the receiver) are placed on a single load board (Figure 5.5). Thus, test reliability and repeatability is highly improved. Also, the problem associated with crosstalk and isolation is mitigated as:

- The UWB transmitter is the only active signal source on the load board.
- The RF response measurements are targeted at frequency bands outside the UWB frequency band of operation.

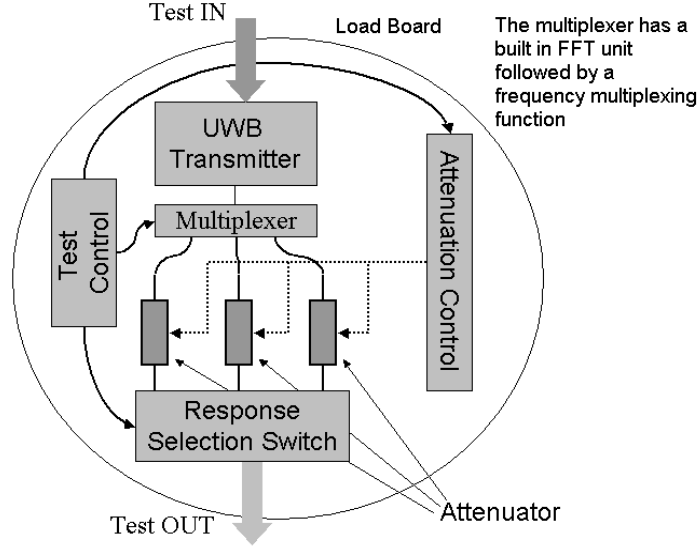


Figure 5.5. Proposed production test setup.

In this work, the channel is modeled using the Saleh-Valenzuela (S-V) model as proposed in [77]. As proposed in the S-V model, we assume the rays arrive in clusters. The cluster arrival times and ray arrival times within a cluster follow exponential distributions as shown in (16) and (17).

$$p(T_L \mid T_{L-1}) = \Lambda e^{-\Lambda(T_L - T_{L-1})} \tag{16}$$

$$p(\tau_L \mid \tau_{L-1}) = \lambda e^{-\lambda(\tau_L - \tau_{L-1})} \tag{17}$$

where the constants Λ and λ values depend on the room geometry. We assumed these constants to be 1/35e-9 and 1/5e-9, respectively. For determining the amplitudes of the rays, the amplitude of the first ray of the first cluster is determined as shown in (18).

$$\overline{\beta_{00}^2} = \frac{1}{\gamma\lambda} G(1m) r^{-\alpha} \tag{18}$$

G(1m) denotes the loss at a distance of 1m from the source, *r* being the actual distance between the transmitter and the receiver, γ is a constant equal to 50e-9. Using (18), the amplitude of the kth ray of the lth cluster is determined using the following equation (19) (Γ is a constant, whose value is 100e-9).

$$\overline{\beta_{kl}^2} = \overline{\beta_{00}^2} e^{-T_L/\Gamma} e^{-\tau_{kl}/\gamma} \quad (19)$$

Finally, the amplitudes follow the exponential distribution described in (20).

$$p\left(\beta_{kl}/\overline{\beta_{kl}^2}\right) = \frac{2\beta_{kl}}{\overline{\beta_{kl}^2}} e^{-\beta_{kl}^2/\overline{\beta_{kl}^2}} \quad (20)$$

It is assumed that production test is used to qualify interference parameters for direct Line of sight (LOS) transmission between the UWB transmitter and the victim receiver and thus, the subsequent clusters after the first cluster have very little effect on the victim. We have studied the effects of interference for two different positions, viz. 1 inch and 3m from the UWB transmitter. Figure 5.6 shows simulation data for a single pulse transmitted and received by a receiver located 3m from the transmitter. Only the first cluster was considered during analysis. Note the spreading effect due to the channel (input and output data amplitudes were scaled to fit in the same window) and the exponential distribution followed by the amplitudes of the rays in different clusters.

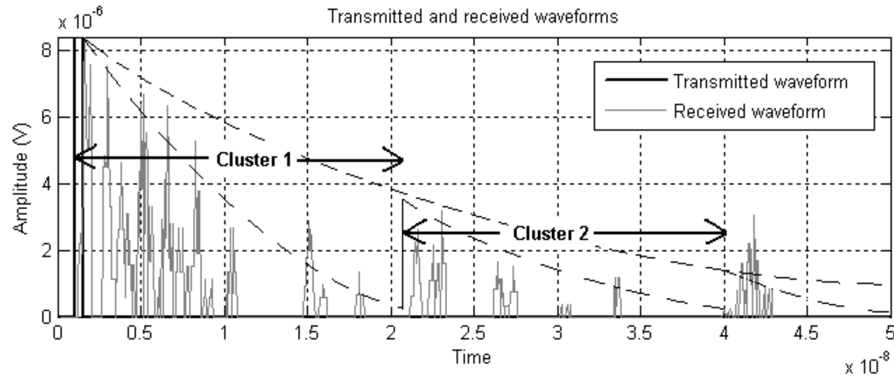


Figure 5.6. Waveform of transmitted and received pulse.

5.4.3.2. Proposed "in-band" interference test

To test the UWB receivers for error probability at low interference levels using the standard test procedure would require a large number of bits, and thereby long time. An *alternate test stimulus* that increases the error probability for low level of interference can reduce the test time significantly.

It has been observed that using sinusoidal pulses instead of gaussian pulses increases the overall error probability significantly even at low interference levels. Therefore, we choose sinusoidal pulses as the *alternate test* stimulus for testing error probability. Moreover, it is easy to generate sinusoidal pulses using a pulsed RF signal generator. Thus, (13) changes to

$$r(t) = s(t) + I(t) + n(t) \qquad (21)$$

where, $s(t) = A\sin(2\pi f_p t + \phi)$. The sinusoidal pulse has the same amplitude as the interfering signal (at which the production test is performed), f_p is the frequency of the sinusoid, and ϕ is the fixed phase of the sinusoid (set to 0). This changes (14) to (22) (again, we ignore the noise effects here).

$$\begin{aligned} c(t) &= \int_0^{N\times 2^D} \int_0^{t_p} [s(t) + I(t)]p(t)dt \\ &= A \int_0^{N\times 2^D} \int_0^{t_p} 2\cos[(\omega_c - \omega_p)t + \theta(t)]\sin[(\omega_c + \omega_p)t + \theta(t)]p(t)dt \qquad (22) \end{aligned}$$

If the frequency of the sinusoidal pulse *s(t)* is chosen close to the interferer, then the cosine term will be almost equal to unity during the pulse duration, giving a probability of error of ~0.5 for all levels of interference, which is not desired. Thus f_p is chosen such that the variation in correlator output value due to change in phase has maximum peak-to-peak variation at $t = T_b$. The test setup looks as shown in Figure 5.7. The results show that the proposed method can estimate P_e very accurately.

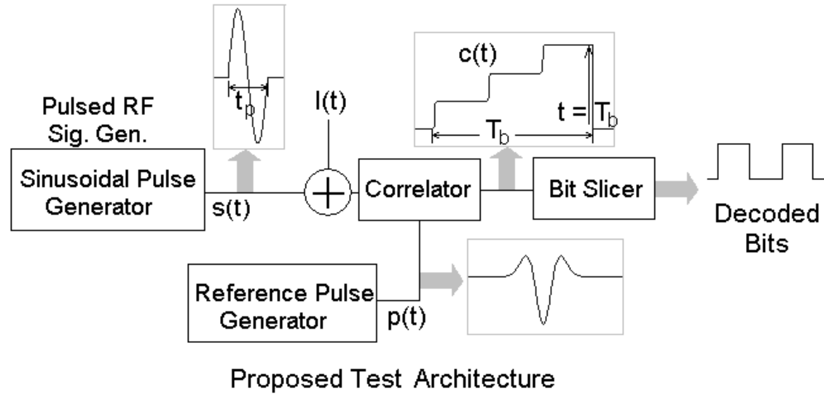


Figure 5.7. Proposed test architecture using a pulsed RF signal generator.

5.5. MB-OFDM UWB devices

5.5.1. OFDM basics

OFDM is a wireless data modulation scheme that multiplexes data over several orthogonal frequency components. It is currently used in standards such as Asymmetric Digital Subscriber Loop (ADSL), IEEE 802.11a/g, IEEE 802.16a and, Digital Audio Broadcast (DAB). In traditional frequency division multiplexing systems (FDM), the channel spacing is more than the encoded data rate to avoid spectrum overlapping between channels. In OFDM, the carriers have a spectral null at all other carrier frequency peak values, making the individual carrier frequencies independent of each other, thereby reducing the required bandwidth (by bringing the individual carrier frequencies closer to each other) and a more efficient use of the available spectrum. The other advantages of OFDM include robustness to narrowband interference and immunity to multi-path effects [83].

The MB-OFDM PHY standard has emerged as the leading contender for adoption by the UWB community. MB-OFDM proposed for use by UWB systems is a variation of OFDM. The UWB spectrum is divided into 4 band groups with each band further divided

into 2 or 3 sub-bands, altogether yielding 14 bands, as shown in Figure 5.8 [80],[84]. MB-OFDM uses a Time-Frequency code (TFC) to interleave data between the sub-bands in a band group. Transmitting data over this wide frequency range further helps in increasing the robustness of the transmission to frequency-selective fading and interference from other sources.

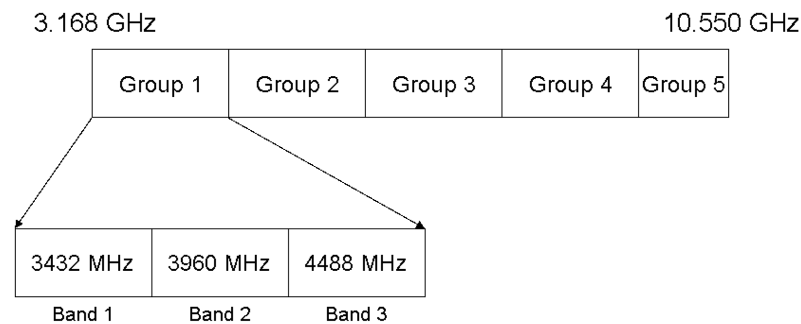


Figure 5.8. MB-OFDM Frequency allocation.

5.5.2. OFDM transmitter and receiver architecture

5.5.2.1. UWB transmitter

There are two main modules constituting the UWB transmitter: the *digital module*, which is usually a digital signal processor (DSP) and the *RF module*. The DSP takes the digital data bits as input, encodes and modulates them and passes on to the RF section through a digital-to-analog converter (DAC). The modulation used in MB-OFDM is Quadrature Phase shift Keying (QPSK). The *RF module* consists of a mixer and a time-frequency (TF) kernel that up-converts and transmits the data through the antenna. The UWB transmitter architecture is shown in Figure 5.9 [70] (The gray shaded blocks in the figure are modeled for test generation and validation purposes). The TF kernel generates the LO frequencies to hop the transmitted signal from one band to the other. The hopping

sequence is controlled by the *digital block;* every OFDM frame transmitted is up-converted using a different LO frequency in a different band. In Figure 5.9, the RF modules under test are shaded in gray.

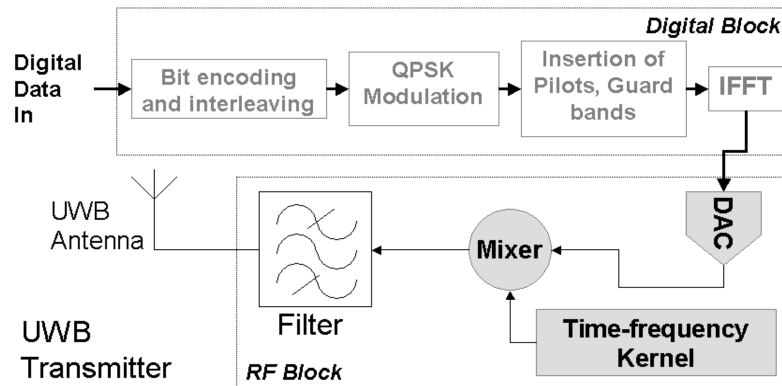


Figure 5.9. UWB transmitter architecture.

5.5.2.2. UWB receiver

The UWB receiver has a similar time-frequency (TF) kernel to down-convert the received signal. The hopping sequence is synchronized with the transmitter, based on the header and the preamble in each frame. After down-conversion, the signal is digitized and processed by the DSP block to recover the transmitted bits. The block diagram of a typical UWB receiver is shown in Figure 5.10.

In reality, a pair of mixers with LO signals in quadrature are used and the signals are combined to generate the desired output. The figure here is not elaborated for simplification purposes.

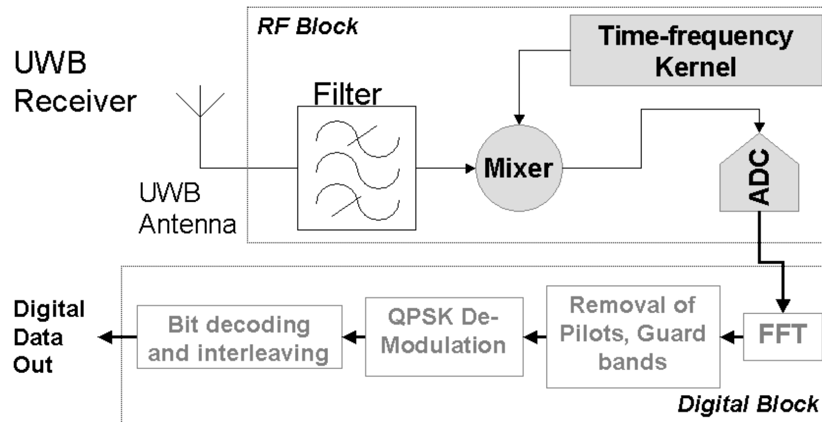


Figure 5.10. UWB receiver architecture.

5.5.3. Standard production test methods for MB-OFDM UWB devices

5.5.3.1. EVM test

EVM test is common among all wireless transmitter systems. For EVM test, the received signal needs to be compared with the actual transmitted data to determine the EVM value. Typically, a large number of QPSK modulated symbols needs to be transmitted to get a good estimate of the EVM value. The test setup used for production testing of EVM is shown in Figure 5.11.

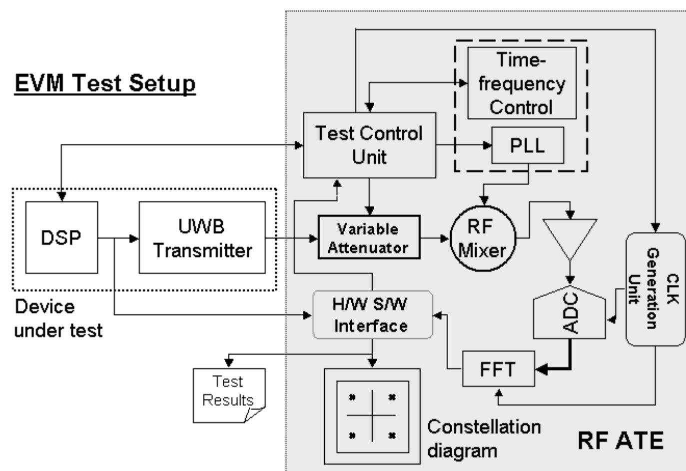


Figure 5.11. Standard EVM test setup.

EVM helps in characterizing the nonlinearities added to the digital data by the RF front-end. The nonlinearities arise from the DAC INL/DNL and sampling clock jitter, PA and mixer nonlinearities and antenna imperfections. Although, UWB transmitters do not use a PA, errors are introduced in the transmitted signal by the *phase noise* of the time-frequency kernel and the *nonlinearity/jitter* of the DAC (shown in Figure 5.9). The phase noise of the device is modeled using (12), which accounts for both random and deterministic jitter. We do not consider the antenna effects in our study.

For EVM test, the tester provides a set of digital data bits to the DSP processor of the DUT. The DSP generates complex QPSK modulated symbols from the data using Table 5.1 and (23) [80]. The complex symbols are then passed through an IFFT block, generating the complex time domain waveform. Finally, the real part of the waveform is up-converted and transmitted.

Table 5.1. QPSK Modulation (generating I and Q values).

QPSK Modulation		
Input bits (D0, D1)	I	Q
00	-1	-1
01	-1	1
10	1	-1
11	1	1

$$d = (I + jQ) \times \frac{1}{\sqrt{2}} \tag{23}$$

As shown in Figure 5.11, the tester needs a TF kernel similar to the *UWB transmitter* to down-convert the transmitted signal before comparing the QPSK symbols to determine the EVM value. The tester down-converts the received data from the transmitter,

performs a FFT operation to determine the frequency information and compares it with the transmitted data to determine the EVM value.

5.5.3.2. CCDF test

Present day digital communication systems combine multiple data channels together in the baseband, yielding a high peak-to-average ratio of the transmitted signal. The peak-to-average ratio is dependent on the number of channels combined and the specific channels that are combined. Thus, the peak power of the baseband signal needs to be accounted for while designing the RF front-end. For this purpose, CCDF curves are used to specify the power characteristics of a digital modulated signal at the baseband, to visualize the effect of modulation, helping in design and test of the transmitter. Figure 5.12 shows a portion of the transmitted signal and its corresponding CCDF plot is shown in Figure 5.13. The y-axis values represent the percentage of time the signal instantaneous power is above the RMS power by an amount equal to the x-axis value.

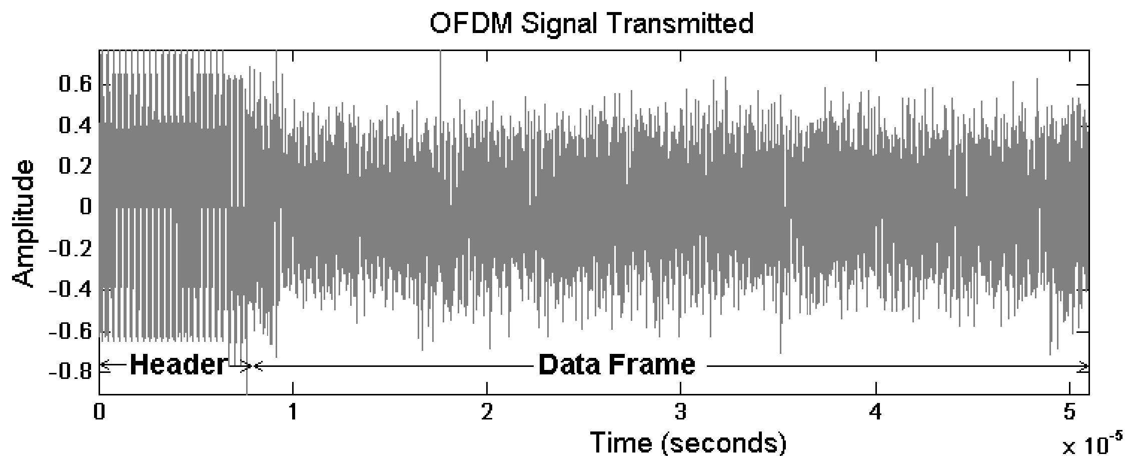


Figure 5.12. Time domain OFDM signal transmitted.

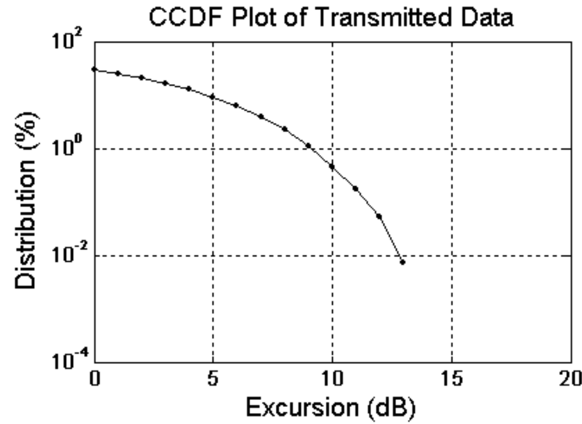


Figure 5.13. CCDF plot of OFDM signal.

To generate an accurate CCDF curve, a large number of OFDM symbols are transmitted from the UWB transmitter to accurately capture the signal characteristics. A smaller test sequence might not be able to capture all the peaks and thus a very long pseudo-random bitstream (>10,000 bits) is used. To test for CCDF, the tester needs to only sample the transmitted data and process the sampled data points to generate the CCDF plot. The test setup for CCDF is shown in Figure 5.14.

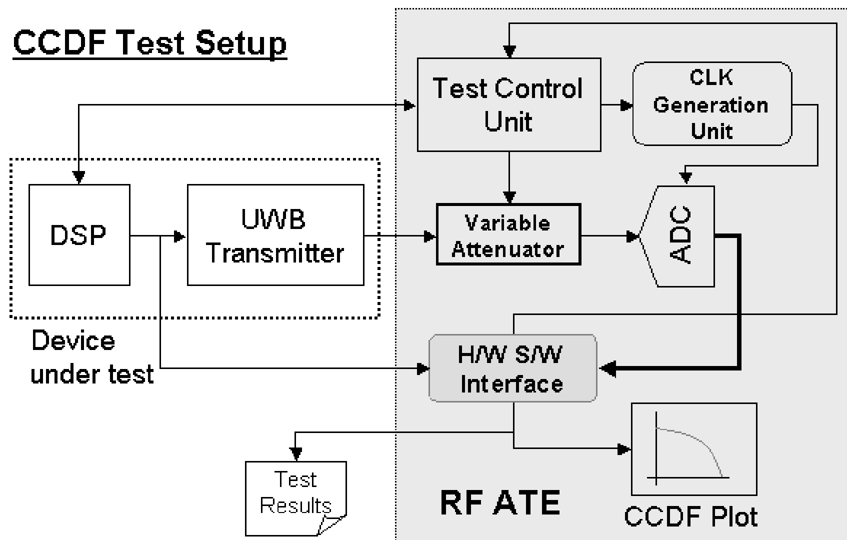


Figure 5.14. Standard CCDF test setup.

5.5.3.3. BER test

BER is a system specification, which denotes the probability of a received bit being incorrect in presence of system non-idealities. Channel effects viz. multi-path, frequency selective fading, etc. are not considered for BER test. This increases repeatability in the obtained results. In addition, this ensures characterization of the system under test, excluding environment effects and the effect of system non-idealities on BER. The BER can be formulated as:

$$BER = \frac{N_e}{N_{tx}} = \frac{e(t_p)}{R \times t_p} \tag{24}$$

(t_p is the measurement period, R is bit rate, N_e is the number of error bits, N_{tx} is the bits transmitted)

BER testing of UWB devices in production test involves transmitting a large number of bits from the BER Tester (BERT), transmitting the bits through the RF front-end system and receive the bits in the BERT. Finally, analysis is performed using (24) to obtain BER for the system. The BERT can transmit different patterns, introduce various errors (delay and jitter) and compensate for cable effects. A typical BER test setup using a BERT is shown in Figure 5.15.

Typically, to test for BER, the number of bits chosen is inversely proportional to the actual BER value. As an example, for Bluetooth, the specification for BER is less than 0.001. Thus, if the number of bits transmitted is 10,000, then the number of error bits must be less than 10. The more number of bits are transmitted, the more number of error bits are allowed, while still having a passing device. Typically, 40,880 bits are used which means there must be less than 41 error bits for the device to pass. The data rate for Bluetooth is 1Mbps. If 40,880 bits are used for a BER measurement, it takes 41 ms for

the tester to receive the data from the DUT before the measurement is performed. Typically, UWB devices have a lower BER value, thereby requiring a larger number of bits to test. Thus, with long measurements necessary for high-speed wireless ICs, it is imperative that the time it takes to perform BER measurements is minimized.

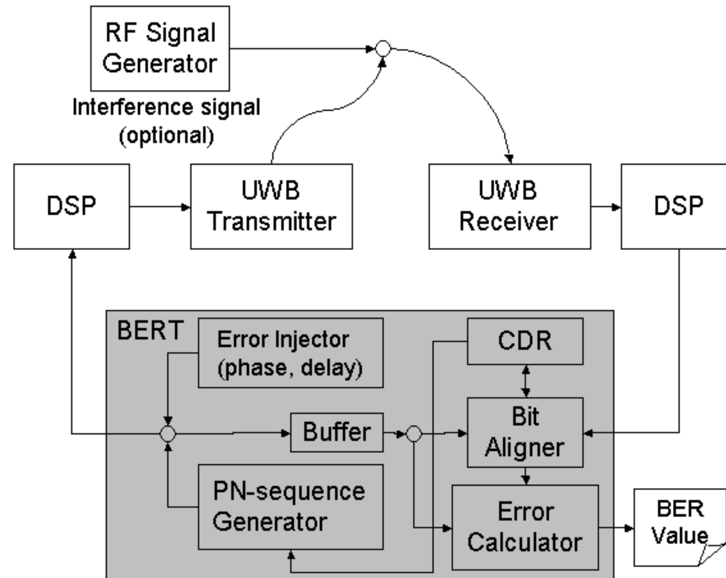


Figure 5.15. Standard BER test setup using a BERT.

Here, we also investigate how BER changes in presence of *"in-band"* interference. Usually, many different interfering signals may be present at the same time, but we consider cases where a single, strong interferer signal is present.

5.5.4. Test cost model

As evident from the previous sections, test time for EVM and CCDF specifications is large, adding directly to the overall test cost. In addition, these specifications require superior tester capabilities, as the tester needs to operate over a wider range of

frequencies. To clearly understand the effects of different components and their contributions to the overall test cost, a test cost model is developed.

The manufacturing test cost can be divided into two major categories [85],

- Fixed test cost (test setup, equipment etc.)
- Variable test cost (test time, labor involved)

Fixed test cost includes test setup cost; cost of test development and the cost of test equipment needed for testing, viz. the tester. The tester cost constitutes a major portion of the fixed test cost. On the other hand, the variable test cost depends on the time required to test the DUT and the test labor involved in testing. All the components of variable test cost contribute almost equally towards the total variable test cost. Figure 5.16 shows a graphic illustration of the test cost model.

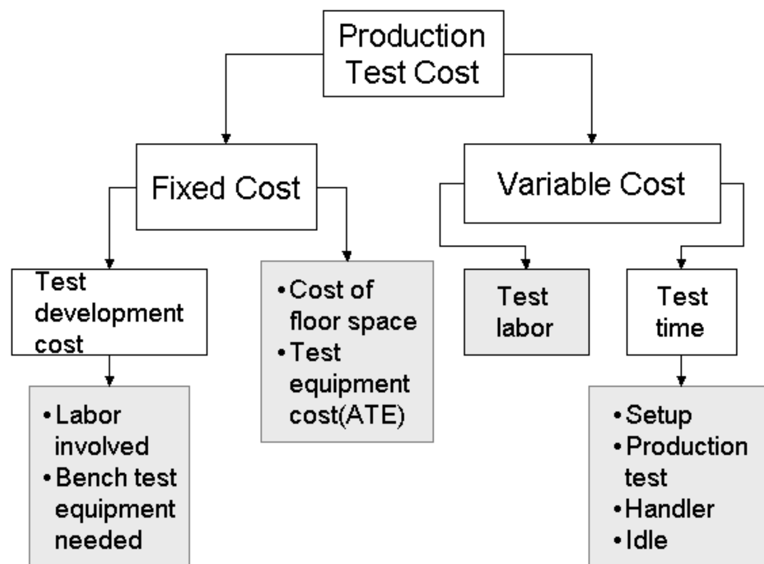


Figure 5.16. Test cost model.

In order to make an informed decision, we need to quantify the test costs for both the standard and proposed tests. We quantify the test cost using the standard test approach as follows.

Apart from EVM and CCDF test, many other tests that are performed on UWB devices include spectral mask compliance test, PSD, etc. To use a single tester to perform all the tests, the following minimum features are needed in the tester, as listed below in Table 5.2. For production test, we assume the following test costs, as indicated in Table 5.3 [86]-[87].

Table 5.2. Required tester specifications for UWB devices

Tester Specifications	
Digitizer Speed	~ 21 GSPS
Digitizer Bits	> 6
RF Frequency Range	3.1-10.6 GHz
RF Channels	> 4
Noise Level	-110 dBm
Clock inaccuracy	<±10ppm
Sensitivity	-100 dBm

Table 5.3. Test cost values considered for analyzing standard test method.

Tester costs in standard test approach	
Equipment	Price ($)
Fixed Test Cost:	
Tester	1,000,000
Floor Space	10,000
Test development labor	2,000
Bench test equipment	40,000
Variable Test Cost/time	
Setup	0.15
Production test	0.05
Idle	0.01
Handler	0.05

For HVM, the fixed cost of testing remains the same, and the variable test cost increases with the number of devices produced, assuming the test plan remains the same. The test cost/device at any point of time during production can be derived by dividing the total cost of manufacturing test by the number of devices produced until that point of time. In our work, as indicated earlier, we propose to reduce the test cost/device by using simpler instruments (i.e. testers) and reducing test time.

5.5.5. Proposed test method

The proposed test methods for EVM and CCDF minimize the overall test cost by reducing:

- Test time
- Test instrumentation cost

The following sub-sections describe test setups for CCDF and EVM, compare each of the methods to the standard test setups and finally determine the tester capabilities needed to perform production test.

5.5.5.1. Proposed EVM test method

Before discussing the alternate test method used for EVM test, a brief introduction on the EVM test setup is offered in this section.

A closer look at the transmit-receive scheme used in MB-OFDM systems reveals that the QPSK symbols at the baseband processor represent information in the frequency domain. This helps in formulating the following guiding principles for test generation:

As the digital data bits used for EVM test are random in nature, the QPSK symbols can appear at one of the four constellation points with equal probability.

Each complex symbol generated after QPSK modulation in the baseband corresponds to a single sinusoid in the complex time domain waveform that is transmitted and all such sinusoids have the same peak amplitude.

As evident from the FFT algorithm, each time-domain sinusoid with properly adjusted phase value generates two symbols in the frequency domain corresponding to each QPSK constellation point (refer to Figure 5.17a) [88]. By inverting the sinusoid waveform, symbols corresponding to the other two constellation points can be generated. In each case, the complex part of the FFT input is set to zero (Figure 5.17b).

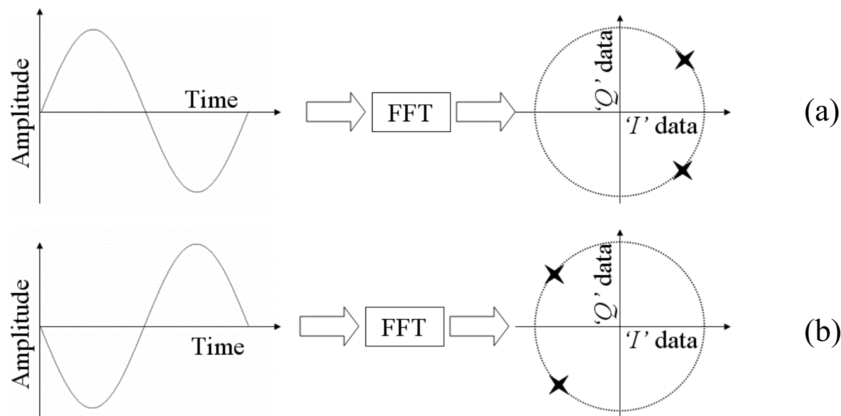


Figure 5.17. Relation between time domain input and FFT output.

We propose to use a *time domain waveform generated by adding multiple sinusoids*, whose frequencies are spaced as per the OFDM frequency spacing. For a MB-OFDM UWB system, within each band of 528 MHz, 128 equally spaced tones are present, resulting in a frequency spacing of 4.125 MHz (528 MHz/128). If multiple tones with properly adjusted phase and amplitude values are added together, the FFT output will have more symbols falling onto one of the four constellation points. Thus, by using this

multi-sinusoid time domain waveform, which is easy to generate, similar EVM characteristics can be obtained, bypassing the DSP module of the transmitter altogether. Moreover, the test waveform can generated easily using simpler test hardware.

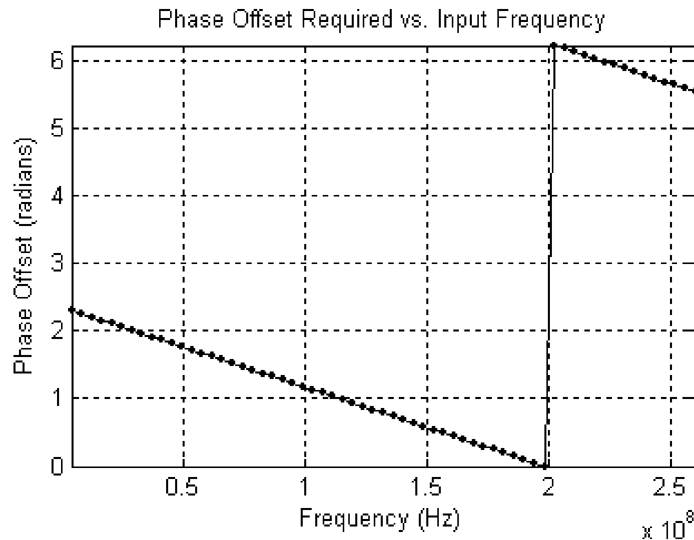


Figure 5.18. Phase offset required vs. frequency of input stimulus.

Determining the relationship between the phase and the frequency of the input stimulus is critical in generating the correct input stimulus. The phase vs. frequency plot shown in Figure 5.18 indicates the amount of phase shift needed for a specific frequency to have the symbols generated coincide with the QPSK constellation points. This can be stored as a lookup-table in the tester for use during production test.

At most 64 sinusoids ($^{128}/_{2}$) can be added to form the time domain waveform, giving rise to 128 QPSK symbols for each OFDM symbol. These will fall into two QPSK constellation points, as shown in Figure 5.17. By inverting the time domain waveform during the next OFDM symbol duration, the QPSK symbols will fall on to the other two constellation points. The maximum possible frequency for the sinusoid is 264 MHz

(4.125 MHz X 64). Therefore, a digitizer operating at 528 MSPS would be sufficient to capture the transmitted waveform.

The above-mentioned method has several advantages over the standard test. They are summarized below:

- The symbols are equally probable over all the QPSK constellation points. In the standard test, a large number of OFDM symbols are required to be transmitted to ensure that the symbols appearing at all four constellation points are equally probable.
- The test hardware used is much simpler in this case. We can use a simple Vector Network analyzer (VNA) connected with the tester through GPIB to generate the LO signal for the mixer (Figure 5.20).
- The digitizer requirements are relaxed considerably using this method when compared to the standard test method.

Figure 5.20 shows the proposed EVM test setup. The time-frequency control unit has been replaced by a VNA. In addition, to generate the desired time domain waveform, 128 amplitude points over a single period of a sinusoid can be stored and higher frequency waveforms can be easily generated by sub-sampling and concatenating the sample value. The pseudo-code for function **`CreateWaveform`** indicated below in Figure 5.19 shows how a time domain waveform consisting of *'N'* consecutive tones can be generated.

```
function [data] = CreateWaveform (N)
Amplitude = read (128 data points)
Data      = 1 X 128 vector with all zeros;
for i =1:N,
   d = Amplitude (1:i:end)
   D = repeat_data (d, 1 X i)
   Data = Data + d;
end
output (data)
```

Figure 5.19. Pseudo-code for generating test waveform.

The amplitude values of the sinusoidal waveform can be stored on the on-board EEPROM or the tester itself. The final test configuration is shown in Figure 5.20.

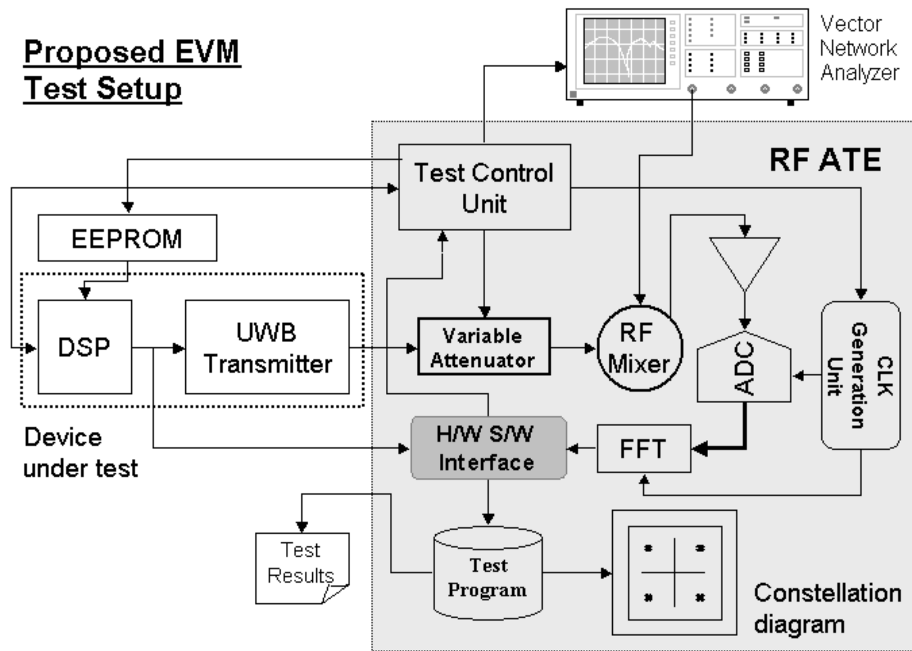


Figure 5.20. Proposed EVM test setup.

Figure 5.21 shows a simulation of EVM using the proposed test approach. This test setup uses only 20 sinusoids for generating the test stimulus shown in Figure 5.22. Thus,

as described above, out of 128 QPSK symbols, only 40 symbols coincide with the constellation points for each OFDM symbol, and the rest of the QPSK symbols appear at the origin. The symbols that appear at the center are not used for EVM calculation. The test is repeated for 44 OFDM symbols.

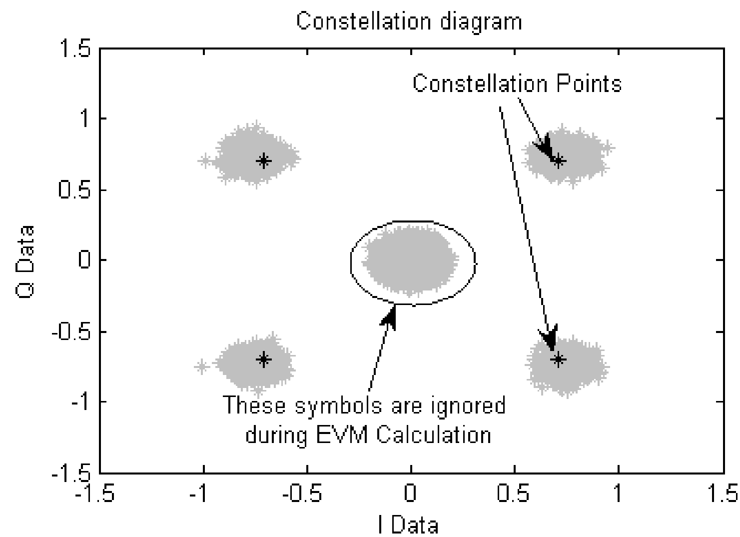


Figure 5.21. Constellation diagram using proposed approach.

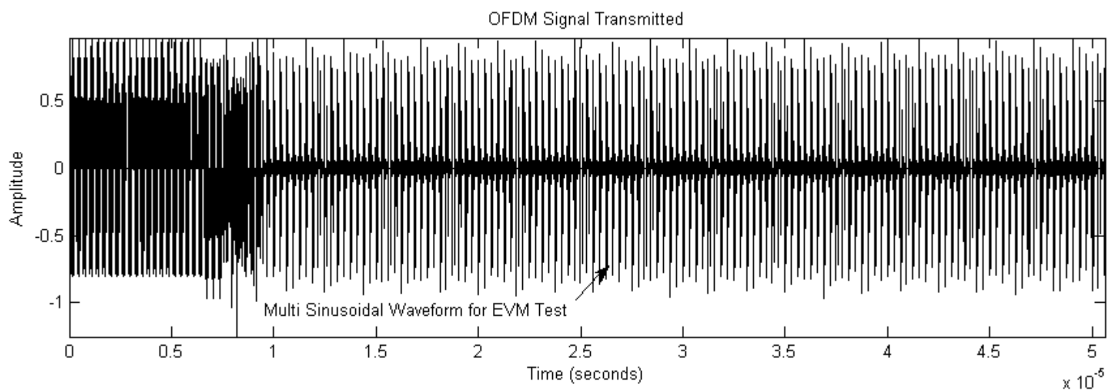


Figure 5.22. OFDM signal transmitted for proposed approach.

5.5.5.2. Proposed CCDF test method

To reduce the test time for CCDF, we propose to use a shorter bitstream that has the same CCDF characteristics of a longer bitstream used during standard CCDF test, under normal manufacturing process variations. The test setup is shown in Figure 5.23.

Figure 5.23. Proposed CCDF test setup.

Test generation for CCDF uses a genetic algorithm based optimization to determine the bitstream to be used during production test. The flowchart of the algorithm is shown in Figure 5.24.

Initially, 1000 device instances are generated by perturbing the process parameters of the DUT (viz. Phase Noise, INL/DNL of DAC, Mixer Conversion Gain etc.) around their nominal values. Simulations are performed using the standard test setup (*'K'* OFDM symbols, usually > 150) and all the CCDF curves are generated. The mean of the CCDF curves from all the device instances is computed and used as the *"Golden CCDF Curve"*.

The genetic algorithm starts by generating random bitstreams with *'k'* ($k < 40$) OFDM symbols ($k << K$). Altogether, *'N'* such bitstreams are generated (we used $N = 10$ in our algorithm). Each of the bitstreams is then passed through the UWB transmitter and the CCDF curves are computed. Next, a selection procedure computes the error between the '*golden CCDF curve*' and each of the computed CCDF curves, selecting the top *'n'* bitstreams with least error ($n = 2$ is used in this work). If the error values computed are less than the error threshold, the bitstream with least error is returned. Otherwise, these best *'n'* parent bitstreams generate *'N'* sibling bitstreams through mutation and crossover and the algorithm continues.

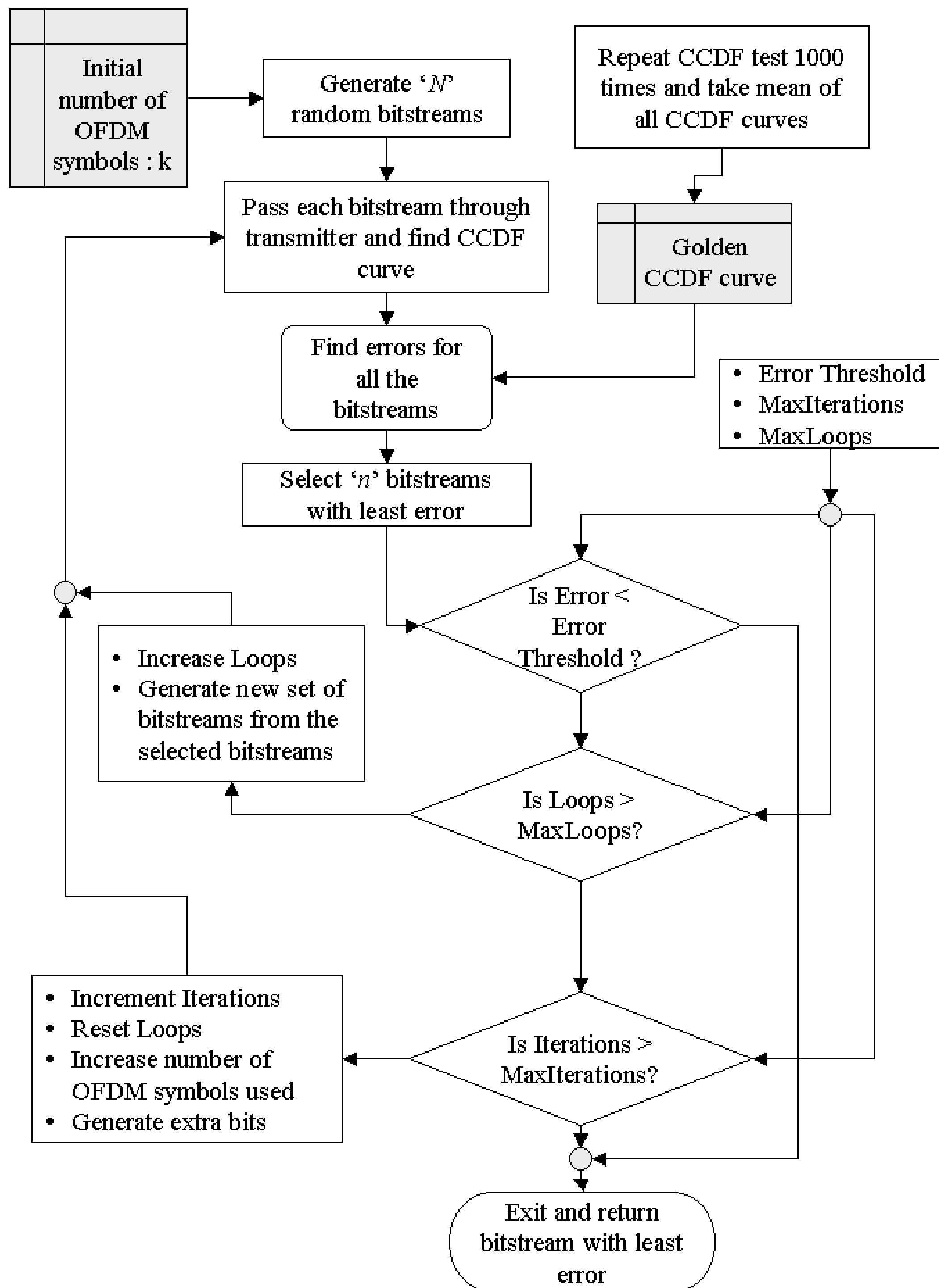


Figure 5.24. Flowchart of genetic algorithm used for test generation for CCDF.

In addition, if repeating the above steps does not reduce the error considerably, the length of the bitstream (*'k'*) is increased and the algorithm is continued. Finally, the algorithm exits when $k < 40$ no longer holds true.

Once such a bitstream is obtained, it is stored in the tester memory or the device on-board memory (Figure 5.23). During test, the Test Control Unit (TCU) of the ATE enables the DSP of the UWB device to read the bitstream from the stored location. This results in direct savings in test time, thereby reducing overall test cost.

The proposed test setup for CCDF do not relax any requirements for the tester, but attempts to reduce the overall test time. The test time saving obtained using the proposed test method is presented in the Results and Analysis section.

5.5.5.3. Proposed BER test method

A bit error is caused when a received QPSK symbol leaves the original quadrant's decision boundary and moves to a different quadrant. The proposed BER test method modifies the phase relations between the QPSK symbols transmitted to increase the number of bit errors. By rotating the different symbols by different amount, the symbols are brought close to the decision boundary, thereby increasing the chances of bit errors. This method, as shown in Figure 5.25, can be also applied in the opposite manner, where the symbols are rotated in opposite directions.

This phase rotation does not change the EVM specification significantly, as the transmitted and received vectors are both rotated by the same amount. In addition, the transmitted signal changes due to the phase rotation, but CCDF remains the same as the signal statistics, which is obtained from a set of pseudo-random bits, remains same. Thus, with large number of bits used for testing BER, CCDF is not affected significantly.

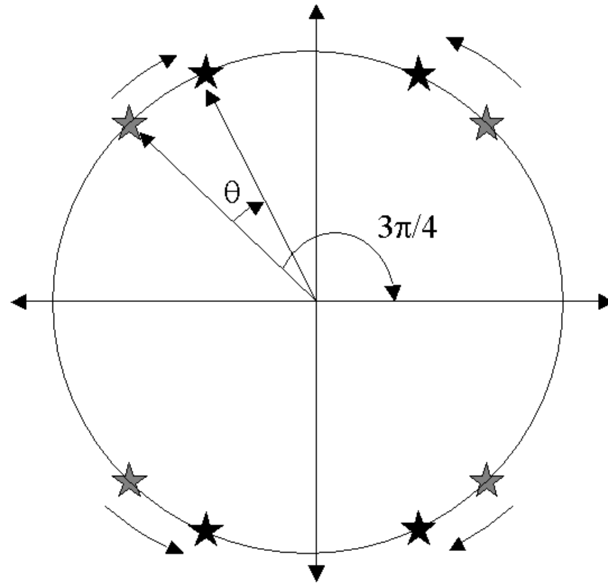


Figure 5.25. QPSK symbols for BER test.

The analysis for BER also includes effects of "in-band" interference. The phase angle θ can be adjusted to reduce BER in this case.

The proposed method uses smaller number of bits to test for BER, as rotating the QPSK symbols increases the number of error bits. To determine the BER at low SNR levels, first tests are performed using the proposed test method. This BER value can be used to estimate the actual BER value (i.e. without phase rotations), which is very small in magnitude. In addition, standard tests are performed to measure the actual BER value. Next, a regression function is built to and actual BER values are predicted. Actually testing for the small BER value would require a large test time. The results indicate that test time reduces by 10 times by using the proposed approach.

5.5.6. Test cost analysis

Based on the test setups mentioned and the test plans presented, the requirements of the tester needed are listed below in Table 5.4.

Table 5.4. Required tester specifications for UWB devices.

Tester Specifications	
Digitizer Speed	> 528 MSPS
Digitizer Bits	> 6
RF Frequency Range	< 3 GHz
RF Channels	2 or 4
Noise Level	-110 dBm
Clock inaccuracy	<±1ppm
Sensitivity	-100 dBm

Based on the tester requirement and test development overhead [86]-[87], test costs are estimated for the different components of the production test cost. The following test costs are used with the test cost model for the proposed test method, as indicated in Table 5.5. Note that, due to simplicity of the proposed test method, tester requirements and hence, the tester cost has come down considerably compared to the standard test method.

Table 5.5. Test cost values considered for analyzing the proposed test method.

Tester costs in proposed test approach	
Equipment	Price ($)
Fixed Test Cost:	
Tester	300,000
Floor Space	10,000
Test development labor	20,000
Bench test equipment	40,000
Variable Test Cost/time	
Setup	0.15
Production test	0.05
Idle	0.01
Handler	0.05

5.6. Results and analysis

5.6.1. Pulsed-UWB: "out-of-band" interference testing

The test waveform selected is a 3rd order derivative of a gaussian pulse, DS-UWB encoded with codeword [0 1 0 0] and pulse duration of 1 ns (data rate of 250 Mbps).

While performing tests, we considered parametric variations in the manufactured devices. The variations are modeled as variations in pulse amplitudes, pulse width and timing jitter. The amplitude variation is considered to be ±5% and ±2% variations in period, both uniformly distributed within the range of variation. The following figure (Figure 5.26) shows the amount of interference at the transmitter antenna for the different bands (for 100 devices under parametric variations).

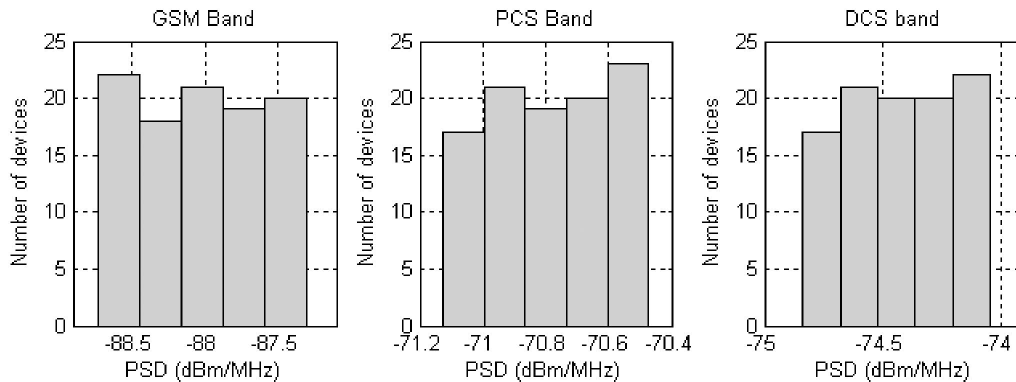


Figure 5.26. Variations in interference PSD for different bands at the transmitter antenna.

As evident from the figure, the variation is uniform with very little spread. Thus, the channel is the major factor affecting the variations of the receiver performance. Consequently, the next step is to use the attenuator and delay units to obtain the interference at the victim receiver's antenna and compare with the standard production test approach.

Now, using the proposed test setup shown in Figure 5.5, the interference PSD is measured at each of the victim receiver's antenna and compared to the actual interference PSD value obtained by performing a complete channel simulation. Table 5.6 shows the interference PSD values for the victim receivers.

Table 5.6. Interference PSD at different bands (victim I and victim II).

Victim I (1 inch)	**Interference PSD (dBm/MHz)**		
	GSM	DCS	PCS
Proposed approach	-109.45	-100.61	-100.15
Channel simulation	-105.17	-99.53	-98.93
Error	4.28	1.08	1.22

Victim II (3m)	**Interference PSD (dBm/MHz)**		
	GSM	DCS	PCS
Proposed approach	-155.58	-144.56	-145.02
Channel simulation	-155.60	-146.48	-144.84
Error	-0.02	-1.92	0.18

The final step of the analysis is to perform a repeatability test for the victim's receiver antenna (Figure 5.27 and Figure 5.28). For each band of interest, using the obtained attenuator and delay settings, the test is repeated 100 times, under parametric variations. The variations in PSD for both the victim receivers are shown for the different bands considered, viz. GSM900, DCS and PCS. The dotted lines show the actual interference PSD values obtained from channel simulations. We set this as the specification limit. The difference between the spectral responses from channel simulation and the attenuator settings obtained for different frequencies introduces a level of uncertainty on the results obtained using the proposed approach. The maximum deviation between the channel simulation and the response obtained from attenuator is denoted by *'d'*. Thus, the test limit is set at *'d'* units away from the specification limit. The thick line in the receiver

PSD diagrams shows the test limit. From the receiver PSD, all devices having PSD more than the test limit can be considered bad (devices lying on the right side of the test limit). The devices within the specification limit and the test limit need to be re-tested to determine pass/fail. Such devices are less than 12% of the total number of devices.

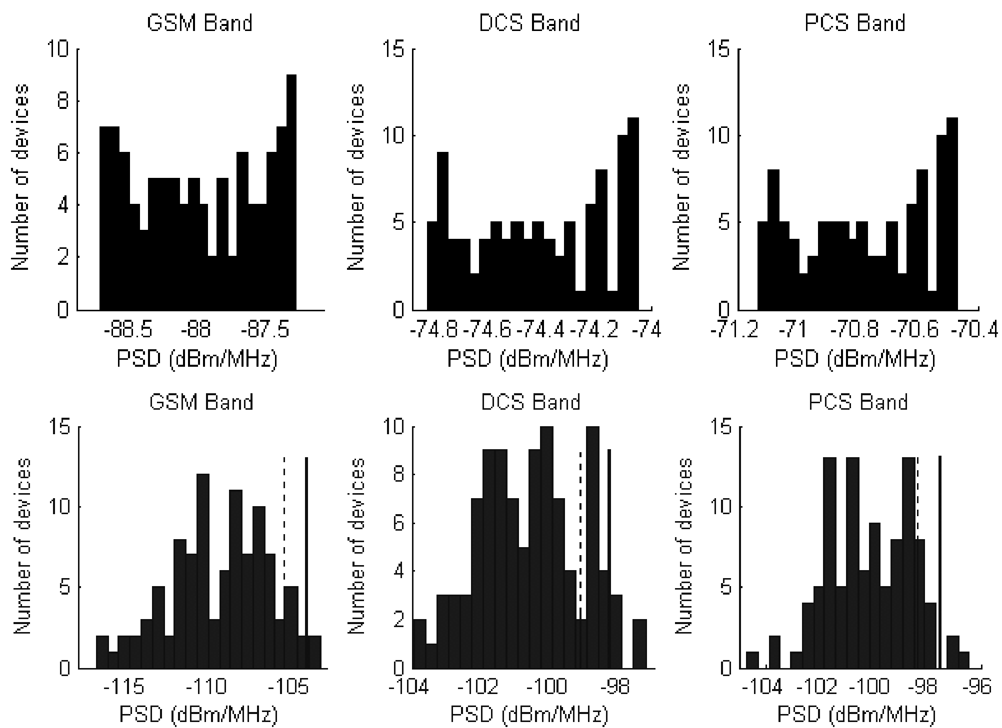


Figure 5.27. Repeatability test for victim I at UWB transmitter and victim receiver.

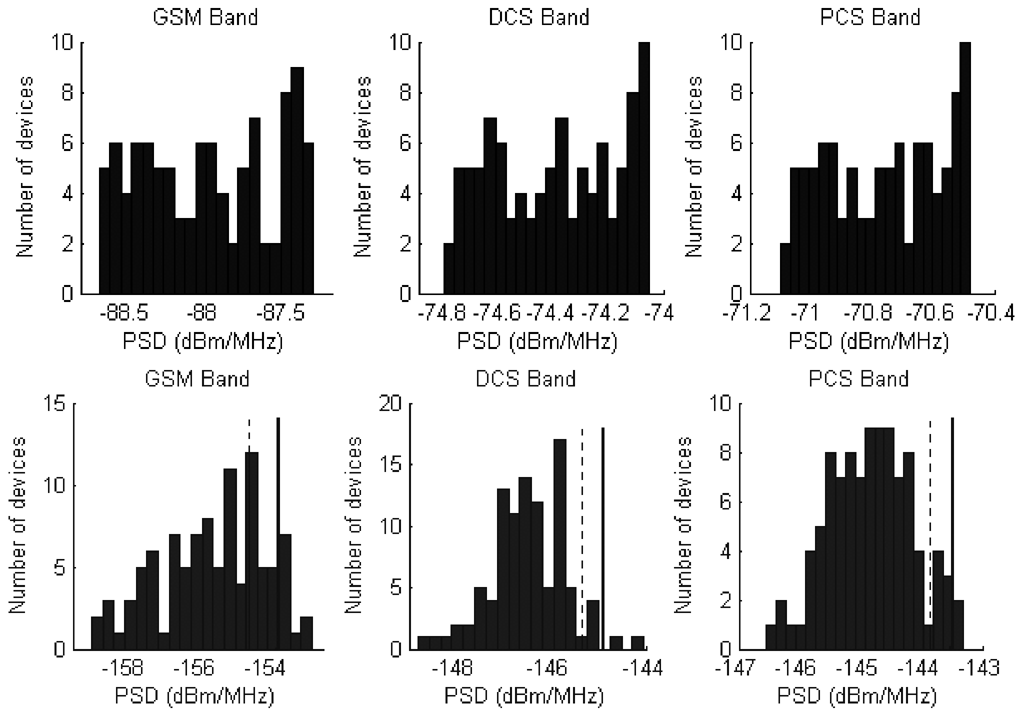


Figure 5.28. Repeatability test for victim II at UWB transmitter and victim receiver.

5.6.2. Pulsed-UWB: error probability testing (in presence of "in-band" interference)

To demonstrate the new method for error sensitivity analysis of a UWB receiver, first, transmitter and a receiver models were developed. We assumed perfect synchronization between the transmitter and the receiver. In addition, assuming a production test environment, we ignored the multi-path components for the channel and modeled transmit and receive antennae as differentiators. An example of the simulation environment is shown below in Figure 5.29, without any interference added (data rate 83.33 Mbps, pulse width = 500 ns). All the bits are correctly decoded.

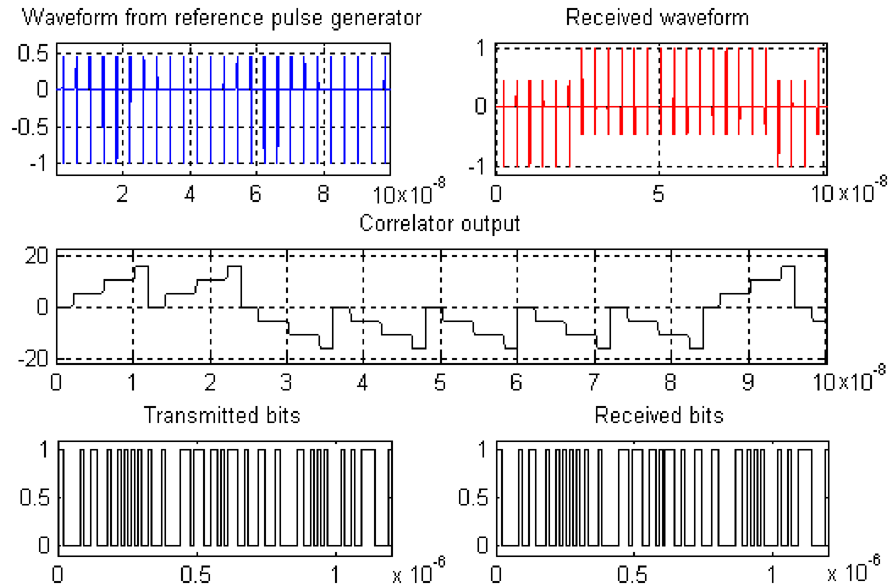


Figure 5.29. Simulation example: the transmitted and the received bits.

If an interferer of sufficient power is added to the signal, bit errors show up, and increase as the interferer power is increased. Figure 5.30 shows the simulation results with interference signal added (data rate 83.33 Mbps, interference power 22 dBm). Few bit errors are present in this case.

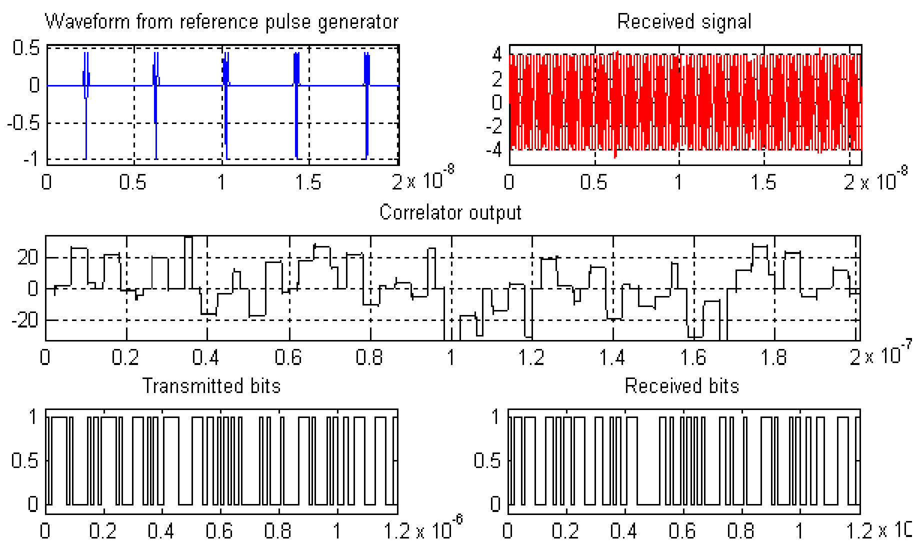


Figure 5.30. Simulation results with interference added.

Next, we performed simulations at various interference levels to find out how the P_e changes with E_b/N_0, E_b is the energy per bit; N_0 is the total noise energy, including interference. Figure 5.31 shows the performance of an UWB transceiver in presence of AWGN noise and varying powers of interfering WLAN signal (graph A). Also shown in is the error probability (graph B) for the proposed approach using sinusoidal pulses.

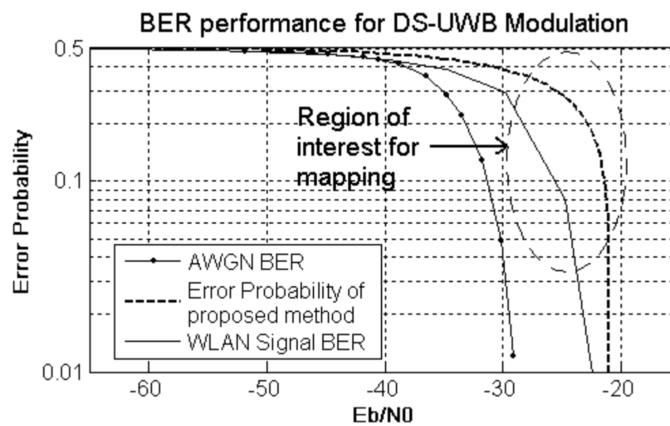


Figure 5.31. BER performance of a UWB transceiver in presence on interference.

Next, the measured error probability value using the alternate test stimulus (sinusoidal pulses) at low interference levels is mapped to the actual error probability value. The mapping function used is multivariate adaptive regression splines (MARS) [19], which uses piecewise linear basis functions to create a mapping between two nonlinear functions. We build a mapping function from graph 'B' to graph 'A'. The mapping function takes the error probability value measured using the proposed technique as input and outputs the actual error probability, for a fixed E_b/N_0 value.

To develop the mapping function, first, the error probability for the UWB receiver is measured using the proposed technique (using sinusoidal pulses, as shown in Figure 5.7). At the same time, the test is performed using a complete UWB transmitter and receiver,

with sufficient number of bits (>50/*P(e)*) to find out the exact error probability value (which requires a large number of bits and hence, longer test time). This is repeated for different power levels of interference we desire to test for. Finally, a mapping function is developed for the region of interest, as shown in Figure 5.31.

Using the mapping function developed, the results are mapped back to the graph 'A' to obtain the actual error probability. This is shown in Figure 5.32.

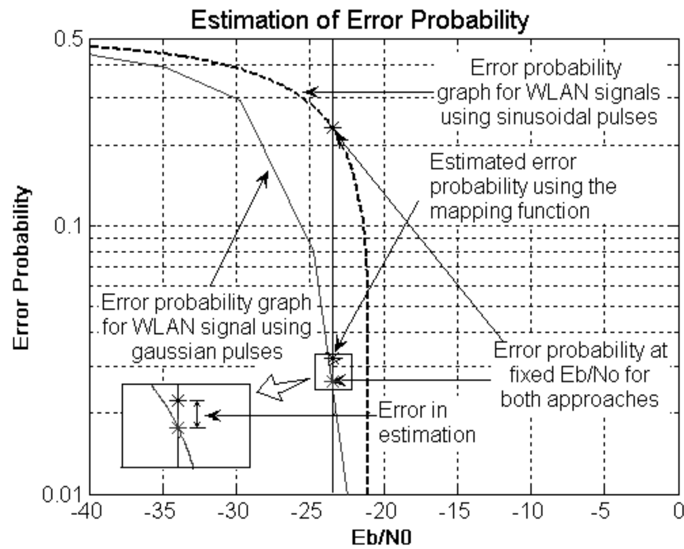


Figure 5.32. Estimating the error probability.

Using this technique, the error probabilities for low interference levels are estimated. Table 5.7 lists the error probability values for various interference power levels, for the standard test method and the proposed test method, while Table 5.8 shows the test-time savings using the proposed method.

Table 5.7. Comparison of standard and proposed test methods.

Interference Level (dBm)	Error Probability (P_e)		Error
	Standard Test Method	Proposed Test Method	
0	0.0016	0.0015	0.0001
10	0.0081	0.0079	0.0002
20	0.03	0.0301	0.0001

Table 5.8. Test-time savings.

Interference Level (dBm)	Test Length		Test Ratio
	Standard Test Method	Proposed Test Method	
0	62500	3000	~21
10	12300	1200	~10
20	3300	500	6.6

5.6.3. MB-OFDM UWB: EVM test results

The proposed EVM test setup combines 32 tones to generate the test waveform. The measured EVM value under manufacturing process perturbations using the standard test method is 9.9. Using the same test setup, the test is repeated 200 times using the standard test and the proposed test to find out the repeatability of each test and the correlation between the two tests. Figure 5.33 shows the results from both the tests.

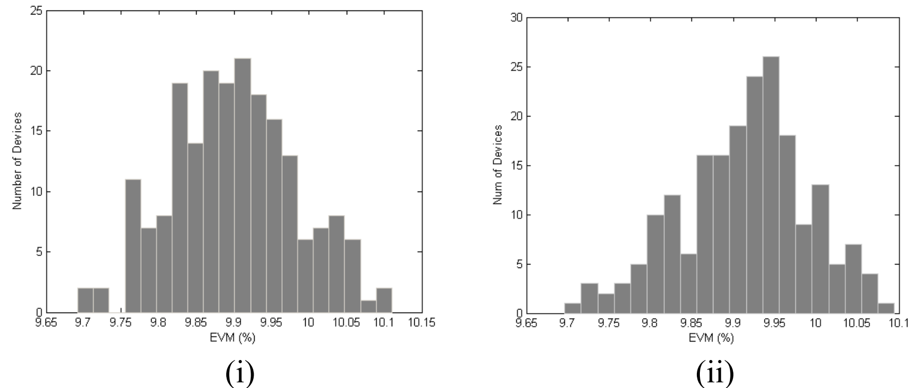
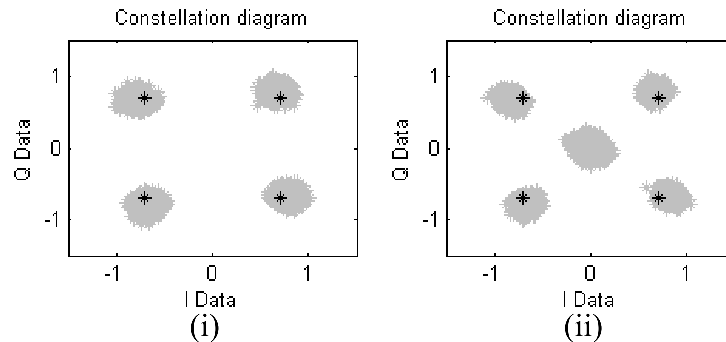


Figure 5.33. Comparison of repeatability for (i) standard and (ii) proposed test.

The following analysis finds out how the two tests correlate for a defective device. The device tested has an EVM of 13.3872 with a variance of 0.0093 (0.0695 %). When tested using the proposed method, the EVM turned out to be 13.4132 with variance of 0.0046 (0.0341%). Figure 5.34 shows the constellation diagrams obtained for the defective device using both test methods. Again, as mentioned before, the symbols appearing near the origin for the proposed test method were ignored during the EVM calculation.



(i) (ii)

Figure 5.34. EVM constellation diagrams for a defective device using (i) standard and (ii) proposed test methods.

5.6.4. MB-OFDM UWB: CCDF test results

For CCDF test, the *'golden CCDF curve'* is first generated by simulating 1000 devices. The CCDF curves from all the devices and the corresponding *'golden CCDF curve'* is shown in Figure 5.35.

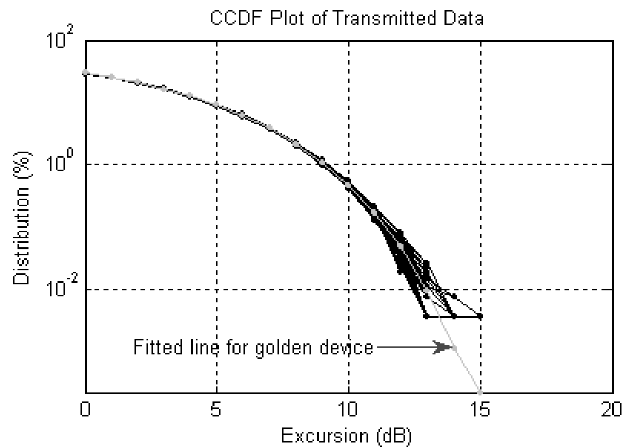


Figure 5.35. *'Golden CCDF curve'* generated from testing 1000 devices.

The bitstream obtained from the genetic algorithm based optimization has the same CCDF characteristics as the *'golden CCDF curve'*. Figure 5.36 shows a comparison between the CCDF curves generated using the optimized bitstream and the '*golden CCDF curve'*. Using the optimized bitstream (275 bytes), test time is reduced by 9X compared to the standard specification test (2048 bytes).

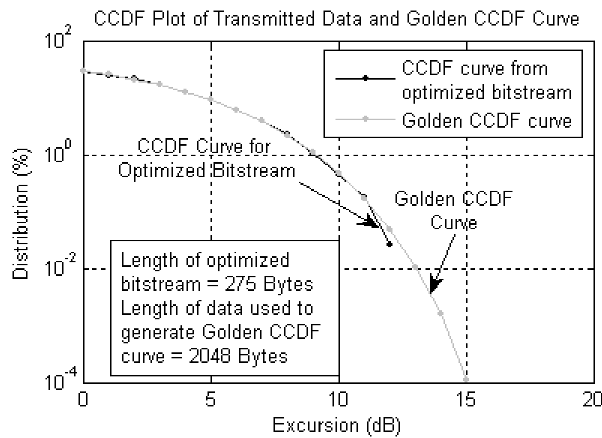


Figure 5.36. Comparison of the *'golden CCDF curve'* and the CCDF curve from the optimized bitstream, obtained from genetic algorithm.

Next, a repeatability test is performed using the optimized bitstream. Figure 5.37 shows the results for the test repeated 100 times.

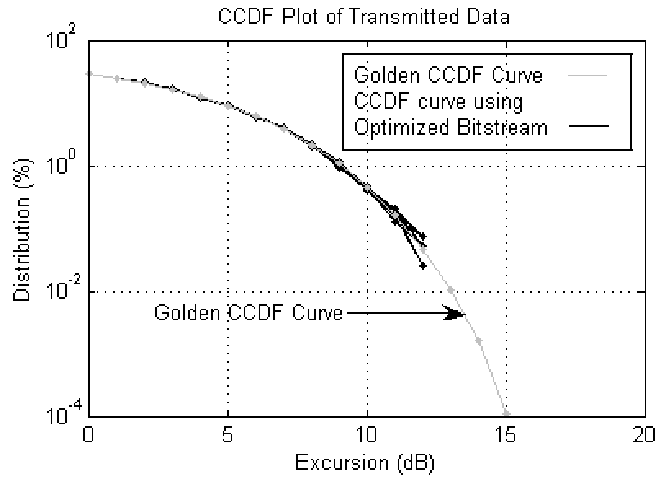


Figure 5.37. Repeatability of CCDF curve using optimized bitstream as input stimulus.

Finally, a comparison of the proposed test and the standard test for a defective device is performed. The proposed test was repeated 10 times for the defective device, but every time the CCDF curve obtained was considerably different from the *'golden CCDF curve'* (Figure 5.38) and aligned with the CCDF curve obtained from the standard test.

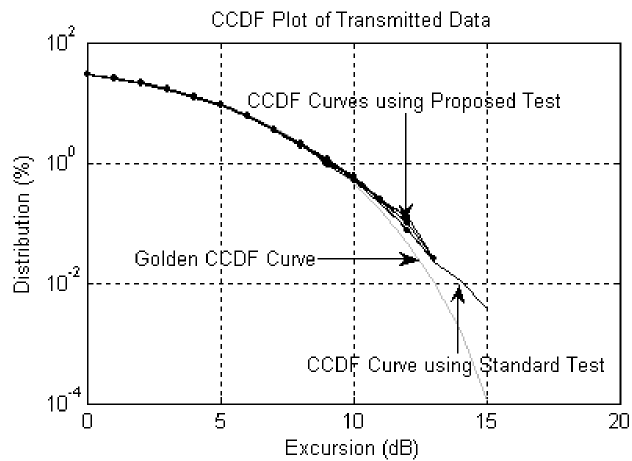


Figure 5.38. Detecting a faulty device using standard and proposed tests.

5.6.5. MB-OFDM UWB: BER test results

For BER test, we first determine the phase offset, which was set to 25°. The BER tests were performed for three different interference signals: Bluetooth (2.4835 GHz), IEEE 802.11a (5.35 GHz) and IEEE 802.15.4 (915 MHz). As mentioned earlier, the results show that EVM does not change by adding the phase offset to the transmitted data.

5.6.5.1. Bluetooth interferer

The BER for MB-OFDM devices in presence of Bluetooth interfering signals does not reach a significant level due to the inherent low power levels of Bluetooth signals (Figure 5.39). As the maximum power level of Bluetooth signals transmitted is 0dBm, the interference signal power is varied from –40 dBm to –10 dBm.

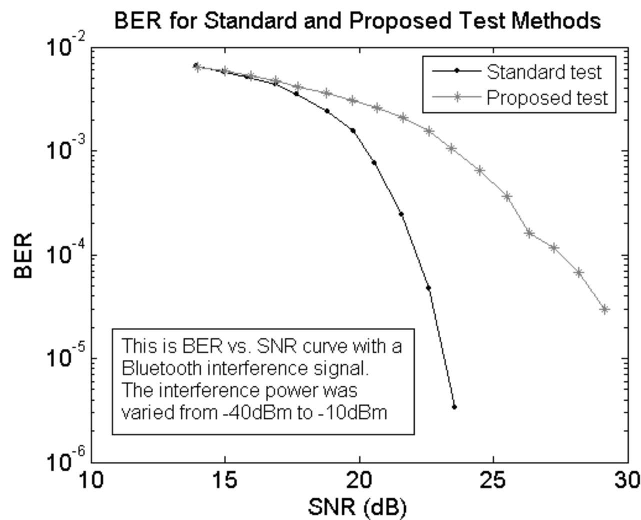


Figure 5.39. BER comparison for standard and proposed test for a Bluetooth interferer.

The EVM does not change considerably, as shown in Figure 5.40. The CCDF changes by 0.3% due to the phase offset.

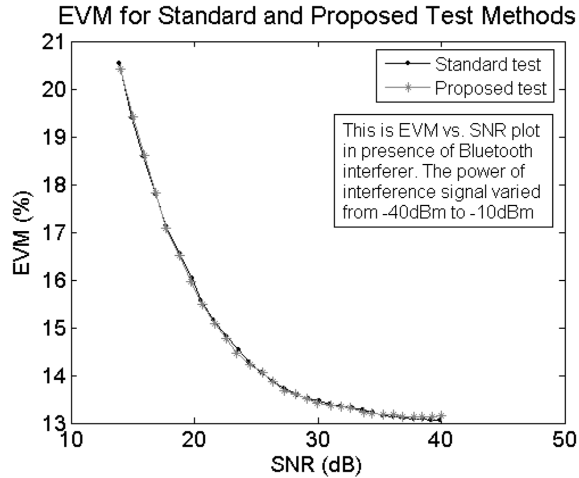


Figure 5.40. EVM with varying SNR for standard and proposed test methods.

5.6.5.2. IEEE 802.11a interferer

The IEEE 802.11a interferer is a stronger signal, thus resulting in a larger BER compared to Bluetooth. The plot of BER for increasing levels of interference signal power is shown in Figure 5.41. For IEEE 802.11a, the maximum allowable signal power for transmission is 15 dBm. In this work, the interference signal power is varied from –35 dBm to 5 dBm.

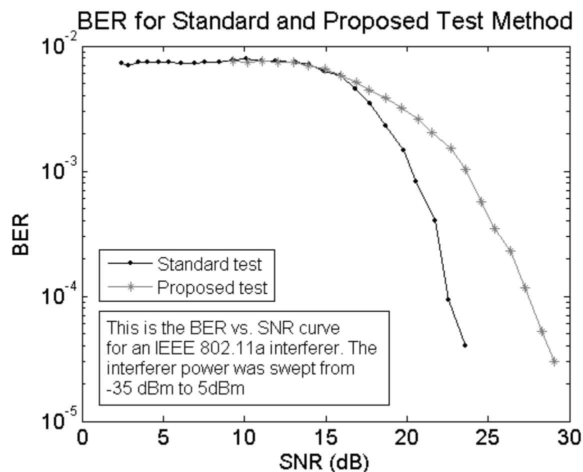


Figure 5.41. BER comparison for standard and proposed test for IEEE 802.11a interferer.

The difference between the BER curves obtained using the standard test method for Bluetooth (Figure 5.39) and IEEE 802.11a (Figure 5.41) is evident from the figures. However, a closer look at the BER curves obtained using the proposed test approach shows that the curves have a similar nature. This is because the BER for both the systems is much larger (factor of 10 to 100) than the actual BER value. If we keep increasing the phase offset, at one point of time, the curves will be the same for different interference signals and the slope will be considerably low. This is intuitively true, because in such a case, all BER values will be in the close proximity of 0.5 at different SNR values.

The variation of EVM for different SNR values for an IEEE 802.11a interferer is shown in Figure 5.42.

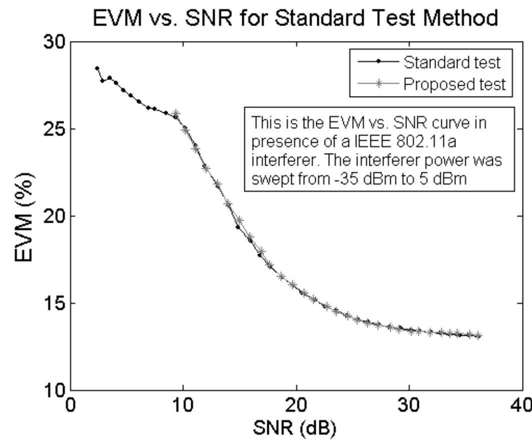


Figure 5.42. EVM with varying SNR for standard and proposed test methods.

5.6.5.3. <u>IEEE 802.15.4 interferer</u>

For IEEE 802.11a, the maximum allowable signal power for transmission is -3 dBm. In this work, the interference signal power is varied from –40 dBm to -15 dBm. The plot of BER for increasing levels of interference signal power is shown in Figure 5.43.

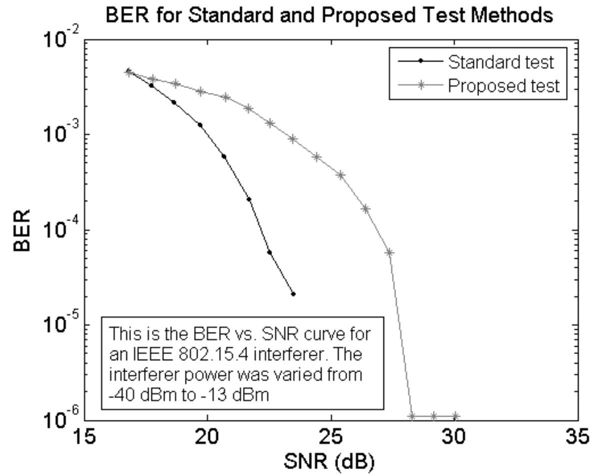


Figure 5.43. BER comparison for standard and proposed test for IEEE 802.15.4 interferer.

For the proposed test method, the IEEE 802.15.4 interferer shows a different behavior compared to Bluetooth and IEEE 802.11a. This can be attributed to the fact that the signal frequency for this interferer is much lower than the actual operating frequency of the UWB OFDM system. This shows that OFDM modulation is resilient to low frequency signals. Figure 5.44 shows the variation of EVM for standard and proposed test approaches with varying SNR values.

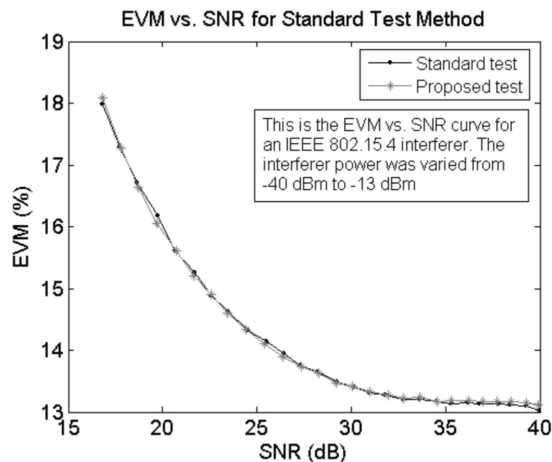


Figure 5.44. EVM with varying SNR for standard and proposed test methods.

Table 5.9 and Table 5.10 shows the test-time savings obtained for different standards at different BER levels. Up to 40X savings in actual test time can be obtained using the proposed test method.

Table 5.9. Test-time savings for BER = 0.001.

Interference signal	Test length		Test Ratio
	Standard Test Method	Proposed Test Method	
Bluetooth	40000	500	80
IEEE 802.11a	35000	700	50
IEEE 802.15.4	22000	1000	22

Table 5.10. Test-time savings for BER = 0.0001.

Interference signal	Test length		Test Ratio
	Standard Test Method	Proposed Test Method	
Bluetooth	400000	1500	267
IEEE 802.11a	350000	2500	140
IEEE 802.15.4	220000	3300	67

5.7. Test cost comparisons

As UWB devices enter the consumer market in 2005, the sales volume can broadly follow three different trends, soaring, steady and sluggish, as shown in Figure 5.45 (there could be other trends, but we are considering the monotonic ones only).

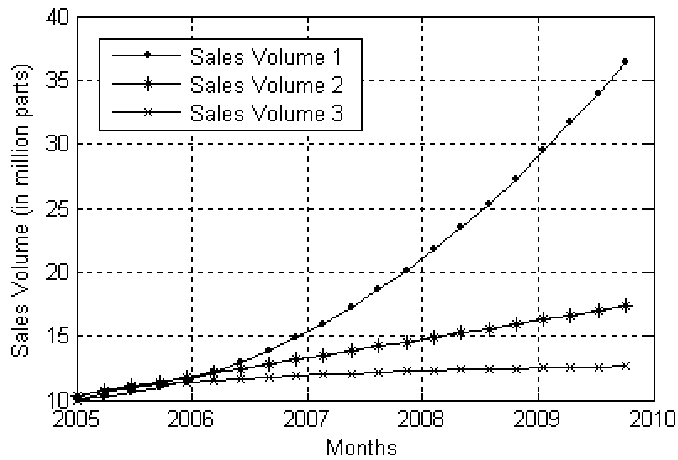


Figure 5.45. Sales volume over five years: three possible trends.

For each of the three cases, the test cost per device for both standard and the proposed test approaches are computed over a period of five years using the test cost model developed (Figure 5.46).

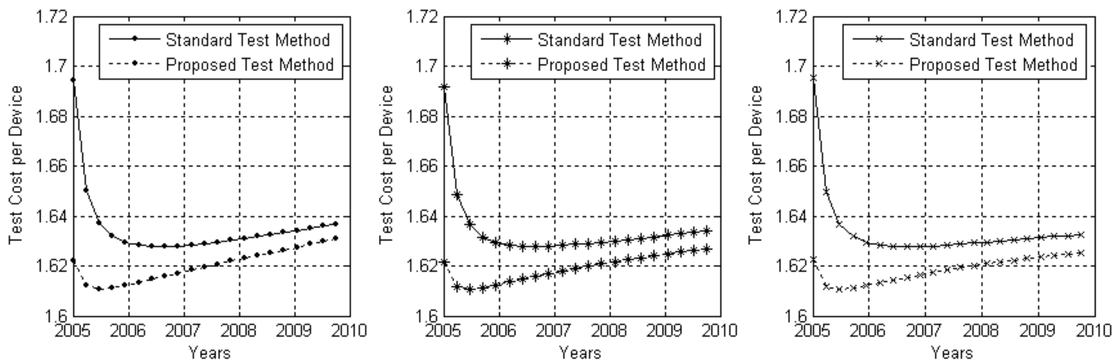


Figure 5.46. Test cost/device for different sales trends.

As shown in Figure 5.46, the y-axis values in are indicated in $. Initially, the test cost per device remains high due to the fixed cost factors, but slowly decreases as more devices are produced. In all three cases, the test cost/device using proposed test method

remains lesser than the standard test method, for the whole duration of the time considered.

Regardless of the sales trend, considerable savings can be achieved using the proposed test method over the five-year period, as indicated in Figure 5.47, compared to the standard test method. As evident from the figure, the total savings after five years, even for a sluggish market is more than 3.5 million dollars.

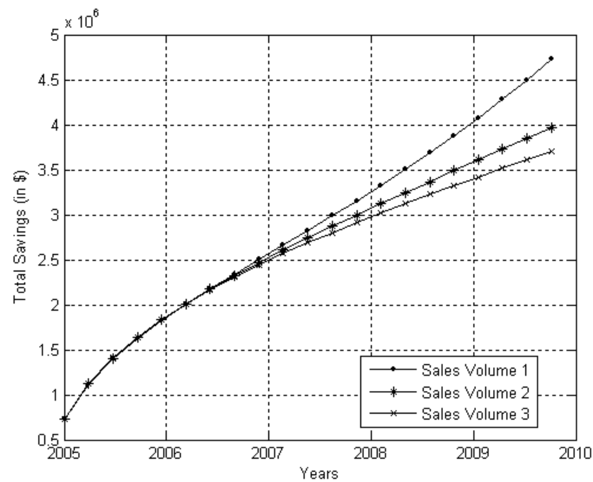


Figure 5.47. Saving per quarter and overall savings using proposed test approach for three different sales trends

Chapter VI
Built-in-test Techniques for RF and High-speed Devices

In the discussions presented in the last few chapters, the problem of test generation and optimization has been addressed and various techniques have been proposed as solutions. In this chapter, first, all the techniques are summarized and the possible shortcomings of the different techniques have been described. Next, the proposed research, which is a possible solution of the problem and takes care of the limitations of the previously described techniques, is presented.

The preliminary concept used alternate test methodology for test generation and test co-optimization. Initially, this method was applied for co-optimizing wafer-probe and assembled-package tests to obtain minimum test cost. While optimizing, the loss in test cost for packaging of bad dies and due to rejection of good devices, both were considered. At the same time, the savings in packaging cost due to rejection of bad dies at wafer-probe was also taken into account. As a limitation of this method, it has to be applied to every individual device-under-test for generating test, as well as the tests need to recalibrated if there is a change in process parameters (process drift).

Even with the limitations present and well identified, this concept was extended next to RF devices. For the previous work, the test generation and application of the test for data capture was done for transient waveforms. For RF and microwave devices, the simulation techniques used in this case are either S-parameter or Harmonic Balance techniques. Moreover, the measurement instruments, viz. Spectrum Analyzers, Network Analyzers etc. work on the same principle as the simulations. So, the alternate test generation and

application method was modified. Instead of sampling the transient output response, the output spectrum (i.e. amplitudes at different frequencies) was used as the test response. Moreover, the simulation bottleneck due to long simulation time required for RF circuits was taken into account by using behavioral models for test generation. With promising results obtained from this approach, the idea was then extended to complete transceiver system. The simulations were performed in behavioral domain to reduce test generation complexity. Finally, the generated tests were verified with hardware measurements, with satisfactory results. The limitations in this case were long simulation times and the requirement for calibration of the test stimulus for process drifts.

As observed in both cases, the process drift causes a big problem for the alternate test approach. Therefore, the attention was shifted to monitoring the process and giving feedback to alternate test method when it is necessary to recalibrate the test. For this purpose, a dedicated circuit was designed that can be put on-chip. This circuit, called *diagnosis core*, has dedicated input and output pins. As described in section 4.1.4, the process variations could be detected with considerable accuracy from the responses of the diagnosis core and be used to provide feedback to the alternate test for recalibration of test.

Seemingly, it might also be possible to extract the specifications of the DUT, like the process parameters of the circuits using the responses of the diagnosis core. This gave rise to two different approaches as described below.

The DUT will have a diagnosis core embedded within it, with dedicated input and output pins to put in customized waveforms and capture the responses. From the

responses, apart from obtaining an estimate about the process, it might also be possible to estimate the specifications of the DUT.

The other approach is to have a dedicated built-in-test (BIT) circuitry on-chip, which will generate the test stimulus to test the DUT directly and the responses will be captured to process and estimate the specifications of the DUT.

Upon close inspection of both methods, the second one seemed to be a more practical solution compared to the previous one. In the first approach, the circuit-under-test is not subjected to any test, estimation of its specifications, i.e. the performance, is made by merely observing the diagnosis core. Thus, catastrophic faults in the DUT, if any, will not be detected at all. The second method (BIT) is more favorable, as it actually tests the DUT using the test waveforms, which are generated on-chip. Therefore, this technique would be able to find the catastrophic faults in circuits along with failures due to parametric variations. The BIT approach can be described as shown in Figure 6.1.

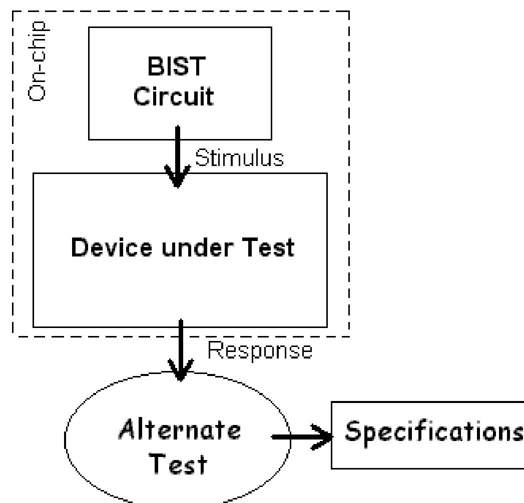


Figure 6.1. BIT approach.

6.1. Built-in-test (BIT) approach: a possible solution?

The BIT approach can solve the problem of calibration for alternate test, but brings in a new limitation. As the process drifts, it will also change the characteristics of the BIT circuitry, thereby modifying the test applied to the CUT. To study the amenability of the BIT scheme, a study was performed to see the effect of process variations on the CUT and the BIT circuit. A LNA was designed and tested with a single sinusoidal input. First, an external source was used to provide the stimulus to the LNA and using the alternate test approach, the specifications were estimated under process perturbations. Next, a VCO was designed and the output of the VCO was used as the test stimulus for the LNA (Figure 6.2). In this approach, it was assumed that both the devices were part of the same die and thus, both were subjected to process perturbations. The specifications of the LNA were estimated from its response, following the alternate test methodology. The results obtained are presented in Figure 6.3 and Figure 6.4.

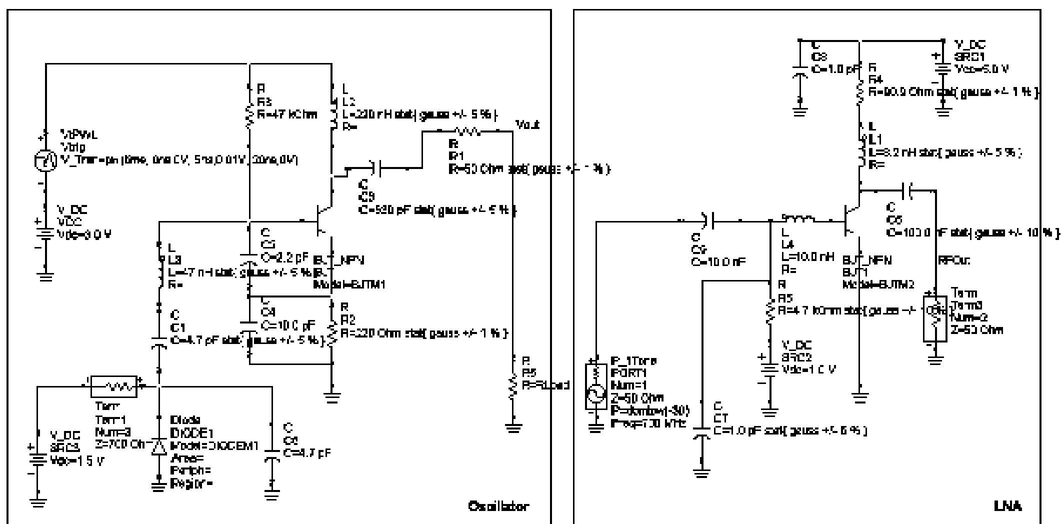


Figure 6.2. Schematic of LNA and VCO circuits.

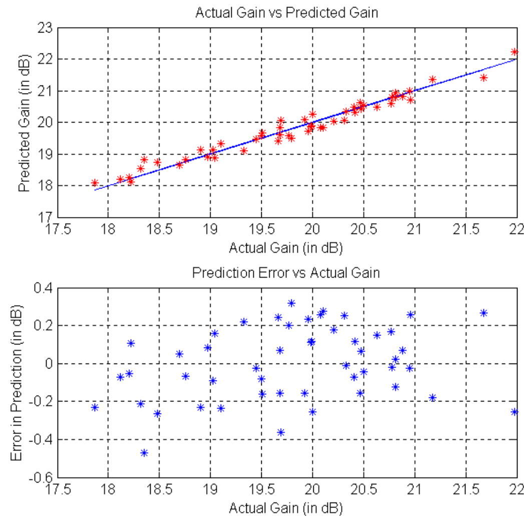


Figure 6.3. LNA specifications estimated by using an external sinusoidal source

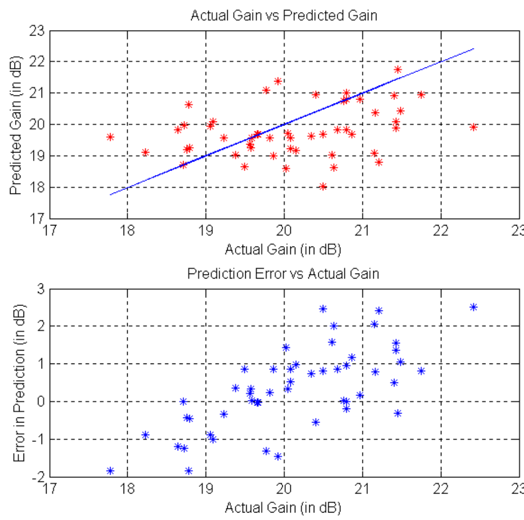


Figure 6.4. LNA specifications estimated using VCO output as test stimulus.

Table 6.1. LNA specification prediction.

LNA specification	Nominal Value	Error in prediction (with external source)	Error in prediction (with VCO)
Gain	20dB	+0.4/-0.6 dB	+3/-2 dB

As presented in Table 6.1, the nominal LNA gain, which was 20dB, was predicted within +0.4/-0.6dB when it was stimulated by the external sinusoidal source; the error increased to +3/-2dB when the VCO was used to estimate the specification of the LNA.

With the above study, it seemed that the possible way to solve the issues related to built-in test waveform generation requires some form of calibration for process variations of the BIT circuitry as well. But in this case, there would be a need to monitor the test waveform generated and for on-chip solutions. This would result in an increase in pin count for the device, which is not a very cost-effective solution. Therefore, the other seemingly alternative would be to perform the test waveform analysis on-chip. In such a case, both the test generation and the test analysis circuitry would experience the same process perturbations as the DUT, and the need for calibration would be obviated. This would be possible by using the test analysis circuits, which would be called as *sensors* from now on.

6.2. Generating test stimulus: using the baseband processor for BIT

Presently, RF front-end devices are usually tested and characterized for linear as well as non-linear end-to-end specifications. While few tests, viz. gain and isolation tests can be classified as the linearity tests, most of the tests, viz. IIP3, ACPR, sensitivity, SNR, focus on characterizing the nonlinearities and noise performance of the system-under-test. By using the baseband DSP processor as the BIT circuit to generate a customized bitstream to test for the linearity as well as non-linearity test specifications of interest addresses the limited test access problem associated with SoCs and SoPs.

6.2.1. Standard test methods

Standard test procedures for ACPR measurement in industry employ a pseudo-random bitstream as the test stimulus. Consequently, the output power from the receiver is spread over a large number of FFT "bins", where each "bin" corresponds to a small range of frequencies. Figure 6.5 shows the spectrum of both a periodic bitstream and a random bitstream of the same length. For ACPR measurement, it is required that the discrete amplitudes of all the frequency components in the main and adjacent channels be measured, and the ratio calculated. Due to the large number of output bins in the case of pseudo-random bitstreams this computation is time consuming [92], [93]. In addition, a lot of time is required to perform averaging in case of lower energy frequency components, which are close to the noise floor. In case of a periodic bitstream, as shown in Figure 6.5, *the energy is contained in a fewer number of frequency components*. Hence, if the pseudo-random bitstream is replaced with a periodic bitstream, the output spectrum of the transmitter will have a fewer number of bins to be measured. This can directly result in test time savings. Moreover, by choosing a bitstream with sufficient energy in its passband, IIP3 measurement can also be performed using the same bitstream.

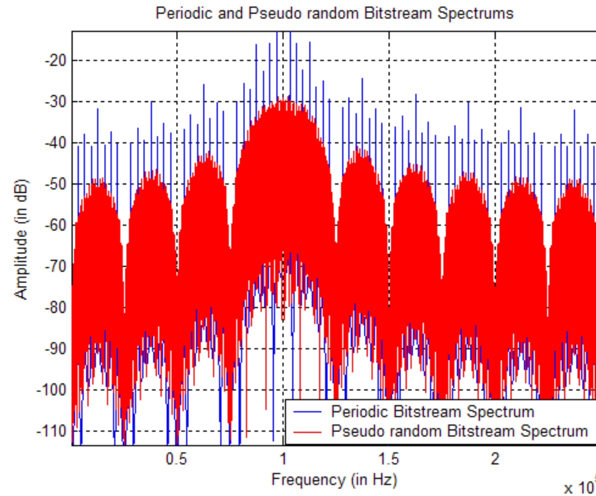


Figure 6.5. Spectrum of periodic and random bitstream.

Finally, for linear measurements such as gain, during production testing, a single tone test is performed. We propose to combine the linear and non-linear measurements by selecting a single bitstream that efficiently tests for the above-mentioned specifications, to obtain a significant overall reduction in test time.

The proposed concept has been demonstrated on a transmitter system. Different modulation schemes, viz. Frequency Shift Keying (FSK), Gaussian Mean Shift Keying (GMSK) were employed at the baseband, while the transmitter was tested for linear and non-linear specifications for each case. IIP3, Gain and ACPR tests were performed on a transmitter employing FSK in the baseband. In addition, GMSK was used in the baseband to show the versatility of the proposed algorithm. The algorithm can be applied to other modulation schemes such as OQPSK, 8PSK as well. In addition, it can be used to estimate other specifications of interest, viz. SNR, and sensitivity.

6.2.2. Selection of bitstream

To determine the optimal bitstream or the bitstreams, two measures were considered. In the first approach, the selection of the bitstream was based on the inferences made on the input itself, without evaluation of the response of the system to the bitstreams. The autocorrelation function $R_f(t)$ of a real continuous time function $f(t)$ is given by:

$$R_f(t) = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} f(\tau) f(t+\tau) d\tau \qquad (25)$$

As per the Wiener-Khinchin theorem [94],[95], there is also a somewhat surprising and extremely important relationship between the autocorrelation and the Fourier transform.. According to the theorem, for a continuous real time function $f(x)$, let the fourier transform $F(k)$ be $F_x[f(x)](k) = F(k)$, and $\overline{F}$ denote the complex conjugate of F, then the Fourier transform of the absolute square of $F(k)$ is given by

$$F_k[|F(k)|^2](x) = \int_{-\infty}^{\infty} \bar{f}(\tau) f(\tau + x) d\tau \qquad (26)$$

Thus, the *power spectral density* in the frequency domain forms a Fourier transform pair with the *autocorrelation* function in the time domain. Hence, for the initial choice of the bitstream, autocorrelation values of the bitstreams are used to selectively pick a few periodic bitstreams with highest autocorrelation values from all possible bitstreams of the specified length. A high autocorrelation value ensures that the power in the spectrum is high enough to force the system-under-test to work in the nonlinear region of the transfer curve and hence the corresponding bitstream will exercise the nonlinearities of the system-under-test. Since some of the bitstreams have very close autocorrelation values,

‘k’ of these bitstreams, which have the highest autocorrelation values, was selected from all possible periodic bitstreams. For this work, *‘k’* was chosen as 10.

6.2.3. Results

The results summarized below are divided into four case studies, first for the ACPR measurement of a transmitter that employs GMSK modulation scheme, next for ACPR measurement using FSK modulation scheme. The third case study estimates gain and IIP3 using FSK modulation at baseband. The final case study uses the other ranking scheme as described in Section 6.2.2, and the modulation scheme used was GMSK.

The 10 bitstreams chosen by the first few steps of the algorithm, as explained in Section 6.2.2, has highest autocorrelation and thus were most suitable for ACPR measurement. The optimum bitstream was chosen from the selected ones.

6.2.3.1. Case study I: ACPR measurement using GMSK modulation

The optimum bitstream obtained using the above-mentioned algorithm was [0 0 0 1 1 1 0 0]. This can be stored in the on-chip memory and repetitively transmitted using the baseband DSP to measure the ACPR of the transmitter chain. The modulation scheme used in this case was Gaussian Mean Shift Keying. Table 6.2 presents the comparison of the number of times the bitstream was repeated and the prediction accuracy.

Table 6.2. Comparison of bit-sequence length and accuracy (GMSK).

Bitstream repeated	Predicted ACPR (dB)	Error (dB)	% Error
10	31.6615	0.654	2.1%
100	31.5444	0.5369	1.73 %
1000	31.4127	0.4052	1.3 %

As it seems from Table 6.2, by repeating the bitstream larger number of times, better prediction accuracy is obtained; but at the same time, the test time increases considerably. For all general purposes, repeating the bitstream 10 times gives acceptable accuracy (2% error) in prediction. In addition, in this case the total test time is considerably less than the pseudo-random bitstream duration. Considering an internal clock of 25 KHz, the test time using the pseudo-random bitstream of length 1000 is *40ms*, whereas for the periodic bitstream, the test duration is only *3.2ms*. This shows that a direct *12.5 times* reduction in test time was achieved. In Figure 6.6, the spectrum for GMSK modulated signal at baseband and the output of the PA is shown. The energy is mostly concentrated around the baseband carrier frequency.

The other factor that plays a vital role in terms of test time is the number of FFT bins that needs to be measured for both cases. For a pseudo-random bitstream, the number of frequency components are much larger in number than the periodic bitstream. In this case, both the bit sequences are passed through the transmitter chain and finally, the measurements are made on the spectrum obtained at the PA output after performing FFT on the output signal. In case of the pseudo-random bitstream, the number of frequency bins to be measured is 162 for ACPR measurement; while for the periodic bitstream it is equal to 74 only. For measurement purposes, that gives a saving of approximately *2.2 times*.

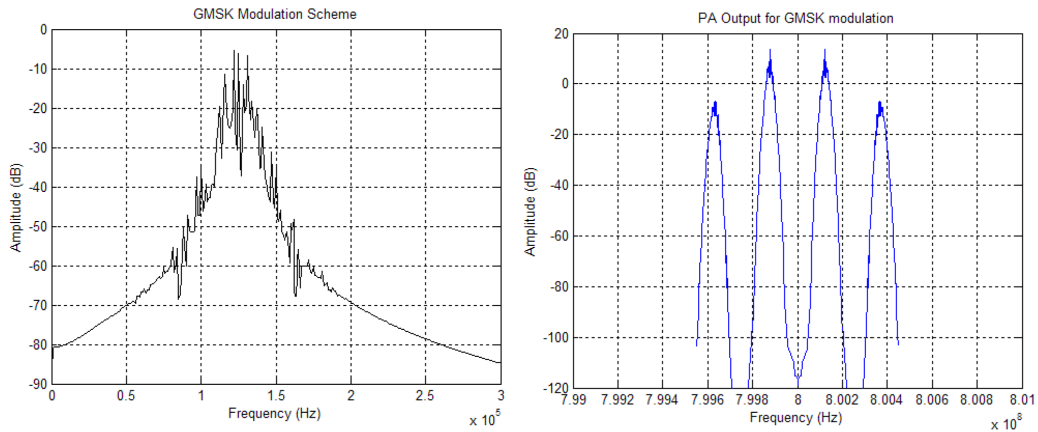


Figure 6.6. GMSK baseband spectrum and PA output spectrum.

6.2.3.2. Case study II: ACPR measurement for FSK

The optimum bitstream obtained using the above-mentioned algorithm was [0 0 0 0 1 1 1 1 0]. The modulation scheme used in this case was Frequency Shift Keying (FSK). The bitstream was repeated for finite number of times and a study was made on the effect of the prediction accuracy as the number of repetitions was changed. Table 6.3 presents the comparison of the times the bitstream was repeated and the prediction accuracy.

Table 6.3. Comparison of bit-sequence length and accuracy (FSK).

Bitstream repeated	Predicted ACPR (dB)	Error (dB)	% Error
10	37.8681	0.0698	0.18%
100	37.8116	0.1263	0.33%
1000	38.0154	0.4052	0.20%

As it seems from Table 6.3, for all general purposes, repeating the bitstream 10 times gives acceptable accuracy (0.18% error) in prediction. In addition, in this case the total test time is considerably less than the pseudo-random bitstream duration. Considering an internal clock of 25 KHz, the test time using the pseudo-random bitstream of length 1000

is 40ms, whereas for the periodic bitstream, the test duration is only 3.6 ms. This shows that an *11.12 times* reduction in test time is achieved. The baseband signal and the PA output for FSK modulation is shown in Figure 6.7. As evident from the figure, FSK introduces more energy in the passband compared to GMSK modulation. This explains the higher accuracy obtained with FSK modulation for ACPR prediction compared to GMSK.

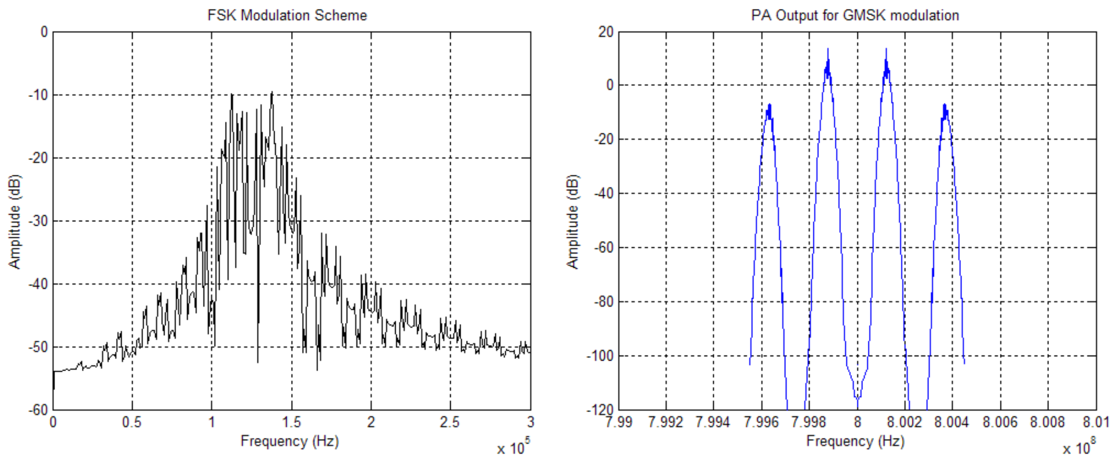


Figure 6.7. FSK baseband spectrum and PA output spectrum.

In case of the standard testing using 1000-length pseudo-random bitstream, the number of frequency bins to be measured is 161 for ACPR measurement; while for the periodic bitstream it is equal to 101 only. For measurement purposes, that gives a direct saving of approximately *1.6 times* in time.

6.2.3.3. Case study III: gain and IIP3 measurement

The optimum bitstream obtained using the above-mentioned algorithm was [1 0 0 1 1 1 0 0] for gain estimation. The modulation scheme used in this case was Frequency Shift Keying (FSK). The bitstream was repeated for finite number of times and a study was

made on the effect of the prediction accuracy as the number of repetitions was changed. Table 6.4 presents the comparison of times the bitstream was repeated and the prediction accuracy.

Table 6.4. Comparison of bit-sequence length and accuracy (FSK).

Bitstream repeated	Predicted Gain (dB)	Error (dB)	% Error
10	39.6138	0.3862	0.9655%
100	39.6882	0.318	0.795%
1000	39.6225	0.3775	0.94375%

For IIP3 estimation, the optimum bitstream was found to be [0 0 0 1 1 1 0 0]. Using this bitstream and repeating it finite numbers of times, different errors were obtained by using the same model for estimation.

Table 6.5. Comparison of bit-sequence length and accuracy (FSK).

Bitstream repeated	Predicted IIP3 (dB)	Error (dB)	% Error
10	-5.5449	0.1954	3.404 %
100	-5.5246	0.2157	3.757 %
1000	-5.5538	0.1865	3.24 %

6.3. Using sensors for test response analysis

In this work, the objective is to predict the specifications or the performance metrics of the DUT by observing the sensor outputs, assuming the test is generated on-chip. Instead of performing the standard tests on the DUT, the sensor outputs will be captured and used to predict the specifications of the DUT. In the proposed test methodology, the focus is on using sensors effectively for a previously determined test stimulus (as explained in

Section 6.2) applied to the DUT. The test framework would also use the available measurements to place the sensors at specific points to get the best estimate of the performance metrics of the DUT.

6.3.1. Why use sensors?

Until recently, test procedure was mostly based on applying a test waveform, capturing the response of the DUT accurately and finally analyzing the captured waveform to obtain the specifications of the device. With increasing device speed and shrinkage in device dimensions, the speed of operation of silicon and other associated semiconductor devices has increased manifold during the last decade. As described before, test response sampling for RF devices is no longer feasible for alternate test. Moreover, test access is very difficult for RF devices, as *impedance matching* for maximum power or minimum noise match is required for any RF device. Therefore, it is no longer possible to probe into the DUT, as it was possible for low-frequency analog and mixed-signal devices. Test point selection is an integral part of design, and insertion of an extra test access point not only complicates the design, but also it increases the Time-to-Market and raises the cost of the device as the pin count of the device increases. Although various BIST schemes has been proposed in the past [107],[111]-[113],[118], both for analog [105],[106],[108]-[110],[114]-[116] as well as digital [104],[117]circuits, until now, there is no concrete way to test RF devices. To overcome these hindrances, we propose a new test methodology for RF and microwave circuits.

In the method described, putting the test on-chip eliminates these problems. The tests are put in the form of sensors in the critical signal paths that need to be observed to determine the DUT performance. The output of the sensors is usually a DC or a very low

frequency signal. This is a means to bring the expertise of designers and test engineers together and developing the *test-plan* at an early phase of production, i.e. design. This scheme has many advantages compared to the standard test approach:

As the tests are put on-chip, the signal is captured by the circuit on-chip and hence the problems related to matching of the signal paths outside the IC are not present any more.

There is no need to sample the waveform to capture it; rather the signal characteristics can be directly extracted on-chip and output by the sensors. This need not be a very high speed output as in most cases, the output signal of the DUT is periodic.

The sensor outputs can also be used for on-line test of the device. In cases where many devices are present with very limited test access, the outputs of the sensors can provide a quick estimate of the performance of any specific IC. This can be further extended as a BIT solution for larger systems, viz. SoCs and SoPs.

Finally, this method can be combined with alternate test approach to predict the specifications of interest without even performing specification tests. As the sensors, which are also on-chip, experience the process perturbations in the same way as the CUT, there is no need to perform calibration.

6.3.2. Test architecture

The sensors are used within the DUT, in the critical signal paths. The sensors tap onto the signal path and provide separate outputs, as shown in Figure 6.8.

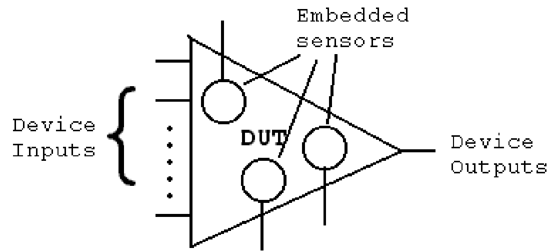


Figure 6.8. Sensors embedded in the DUT.

In case of a typical RF receiver, the front-end usually consists of a LNA followed by a Mixer/Local Oscillator and finally a VGA, before the signal is fed to the baseband DSP processor. In most cases, viz. cellular telephone systems, the different parts of the circuit are on a single chip, except for the bulky passive components and filters (mostly SAW filters), which are put off-chip (Figure 6.9). Therefore, for such systems, there are only a few access points available, as indicated in Figure 6.9. Here we have limited our observability to such access points only.

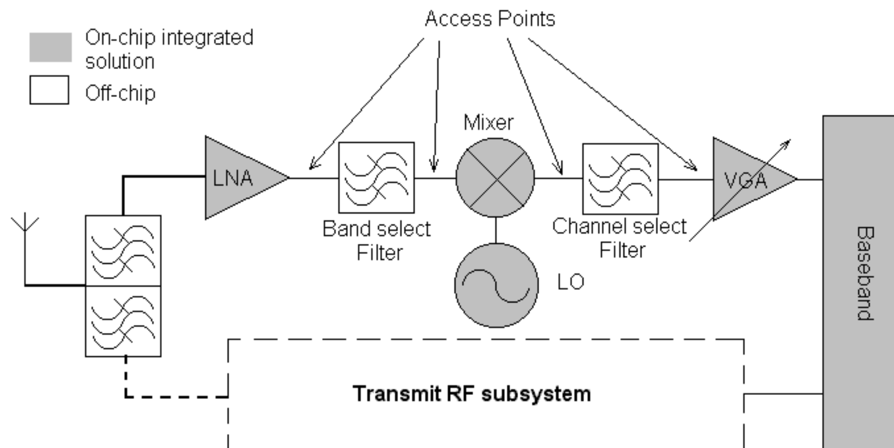


Figure 6.9. System test overview.

As shown above, so far our scope is limited to placing the sensors at the available access points only. While more than one sensor can be put at any one of these access points, the issue of signal integrity and purity in terms of matching has to be kept in mind. As shown in Figure 6.10, the sensors are placed these points and the *sensor outputs are captured to predict the specifications of the individual blocks and the system as well*. Moreover, as system integration gets more mature, these access points will not be available any more, as filters and other components will also be implemented on-chip. In such cases, there will be a definite need to put the sensors on-chip.

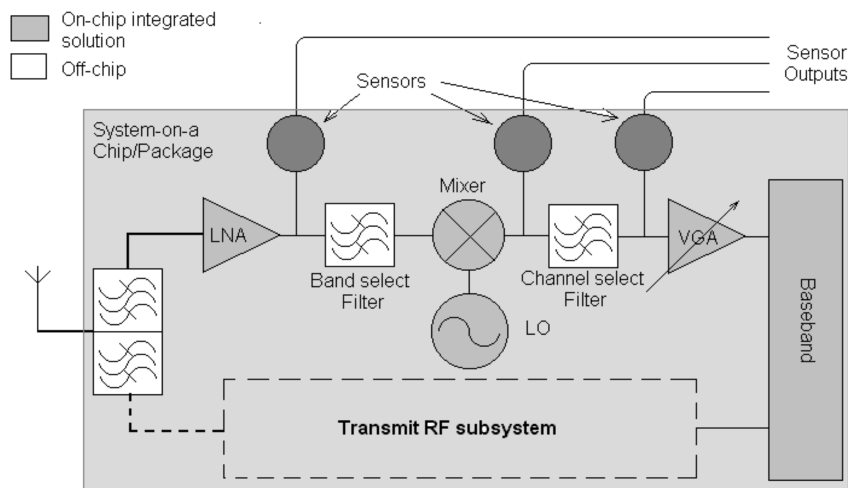


Figure 6.10. Sensors placed for system specification test.

6.3.3. Algorithm for optimal placement of sensors

In this proposed work, an algorithm has been proposed to determine the optimal placement of a set of available sensors, and achieve the best prediction of specifications from the sensor measurements.

The algorithm shown in Figure 6.11, starts with all the sensors put at the access nodes of the system-under-test. For a fixed, pre-determined test stimulus, the strategy is to use minimum number of sensors in such a way that the prediction accuracy does not reduce considerably, or increases compared to the accuracy obtained with all sensors used. Assuming the sensors to be on-chip, they experience the process variations in the same way, as does the DUT. Thus, perturbing the process parameters creates multiple instances of the DUT and the sensors, and the responses for each instance are captured. A preliminary analysis is performed to find out which of the specifications cannot be predicted with reasonable accuracy even with all the sensors present. After eliminating such specifications, a *nonlinear model* relating the reduced set of specifications and measurements is constructed. To reduce the measurement set, i.e. the number of sensors required, the measurements are checked if they bear sufficient linear correlation with the remaining specifications. The assumption here is that even though the relation between a measurement and a specification is nonlinear, there exists a strong linear relationship between them. In case where there is not a strong correlation between the specification and a sensor measurement, the likelihood of predicting the specification using the specific measurement is low. So, the measurement having lowest correlation with all the specifications is eliminated from the list of measurements. Next, a nonlinear model relating the rest of the measurements and specifications is built. The model is compared to the previous one to see if the prediction accuracy has improved or not, and accordingly the measurement is retained or removed from the measurement set. Proceeding in this way, the measurement set is reduced until no further gain in accuracy can be achieved.

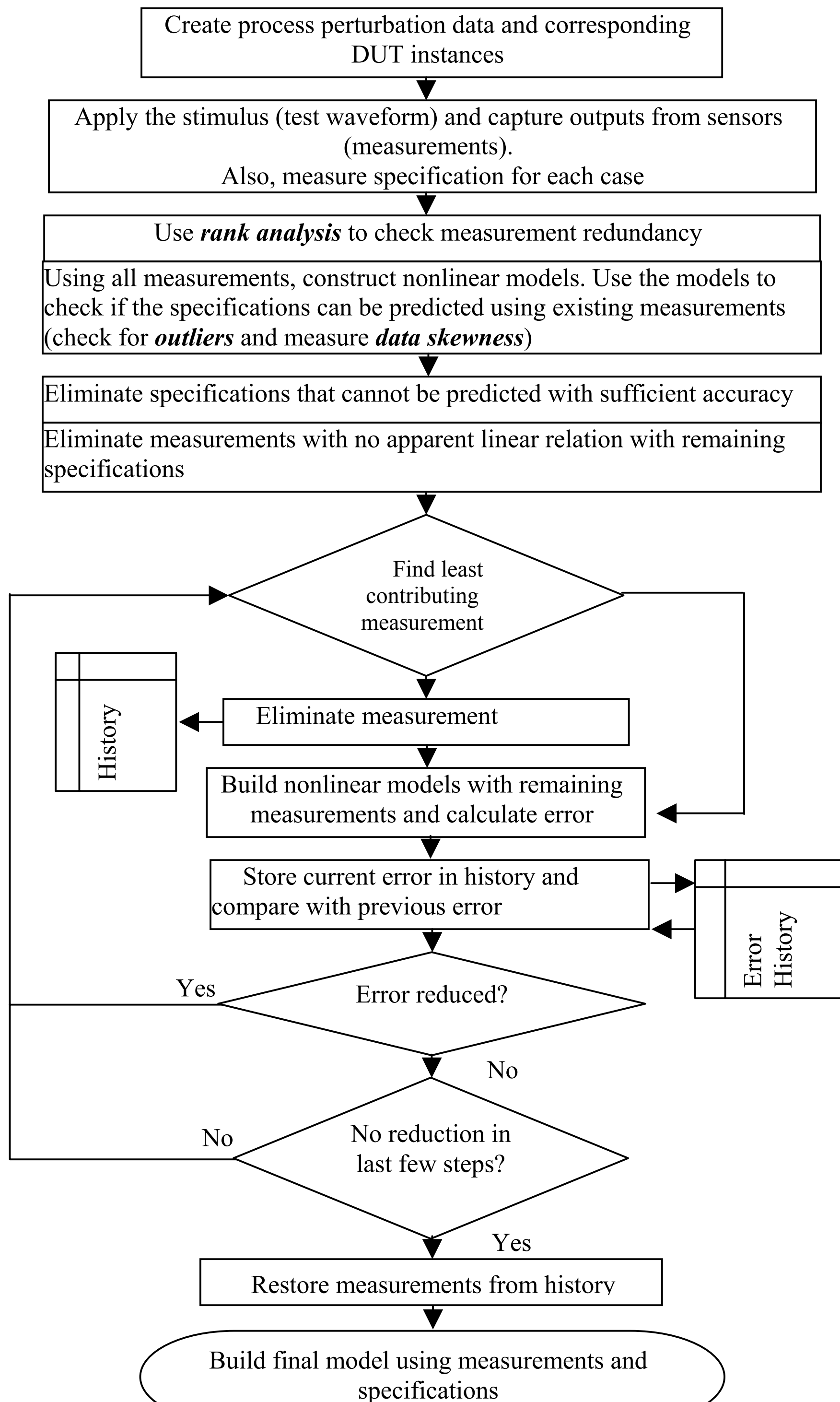


Figure 6.11. Flowchart of core algorithm.

6.4. Results

The results section comprises of two case studies. In the first case, the DUT was a filter and in the second case, the DUT was a RF front-end system comprising of a LNA and a mixer. Each of these studies is described in detail in the following sections.

6.4.1. Case study I

The above algorithm was first applied in case of a state-variable filter and three sensors, which were ideal in behavior, were used at all the outputs of the filter. The sensors used were peak detector, RMS detector and a sensor providing a DC output proportional to the periodicity of the output signal. As described in the algorithm described in Section 6.3.3, the band pass filter gain could not be predicted with sufficient accuracy for normal process perturbations (5%) and hence was eliminated, as is evident from Figure 6.12 and Figure 6.13.In Figure 6.12, the percentage error in prediction for different filter specifications with change in process perturbations is presented. In the algorithm, it was assumed that the test stimulus is known and remains unaltered. In this case, it was a two-tone test, well within the limits of the lowpass filter. As is evident from Figure 6.12, the lowpass filter specifications were predicted with considerable accuracy, but not the bandpass and highpass filter specifications. As tones with higher frequencies were added to the test stimulus, the error in prediction for bandwidth specification of bandpass and highpass filters reduced (Figure 6.13). This indeed tells us that apart from placement of sensors at specific nodes, optimizing the test stimulus is also required for increasing prediction accuracy.

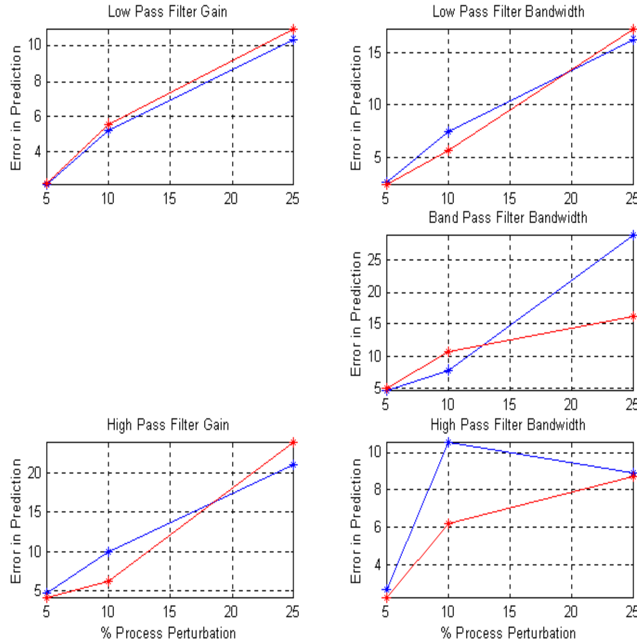


Figure 6.12. Percentage error in prediction of filter specification for different process perturbations.

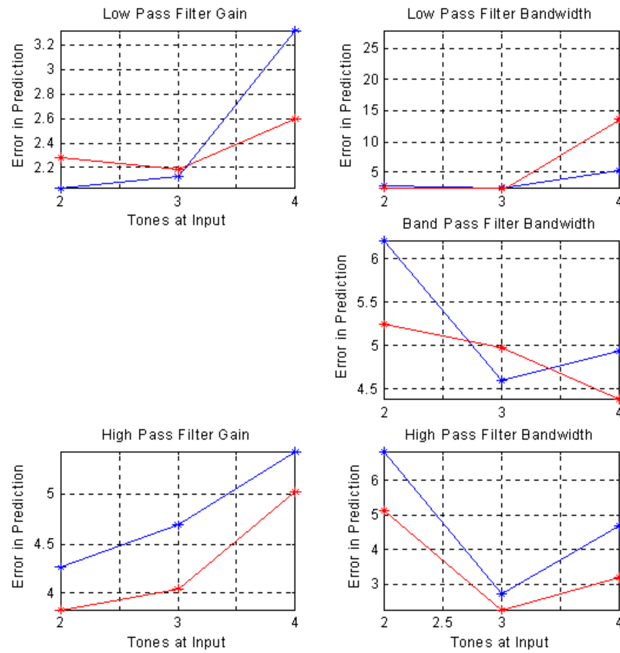


Figure 6.13. Percentage error in prediction of filter specifications for different input test stimuli.

6.4.2. Case study II

In order to determine which sensors can be used for a RF system, first a behavioral model is developed for a receiver subsystem. Behavioral models for the sensors are also developed. This case study considers a LNA and mixer together, operating at 900 MHz, as a RF subsystem under test. Multi-tone sinusoids are used as test stimulus.

First, the test is determined so that the useful part of information propagates unaltered through the system. Next, sensors are placed at the outputs of the LNA and the mixer. The sensors used are peak and RMS detectors, and a tunable sensor used to find out the amplitude of a specific tone of interest. A separate sensor takes the test stimulus as input; phase shifts the input and down-converts to baseband with sufficient amplification. The sensor is linear, so it does not generate intermodulation components. The output of the sensor is then added to the output of the receiver, which essentially eliminates the main tones that are input to the system at baseband. The system architecture is shown in Figure 6.14.

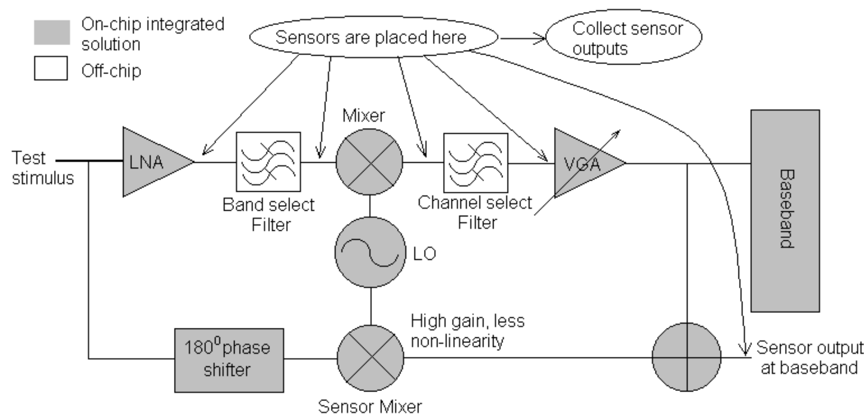


Figure 6.14. Test architecture for Case Study II.

Figure 6.15 and Figure 6.16 show the change in prediction accuracy as number of tones in the input stimulus is changed. Increasing the number of tones has almost little or no effect on Gain prediction, whereas IIP3 prediction improves considerably. Increasing the number of tones increases the intermodulation terms, and thus, prediction of IIP3 is better with larger number of tones present in the test stimulus. The following table shows the error in prediction for the test architecture described above.

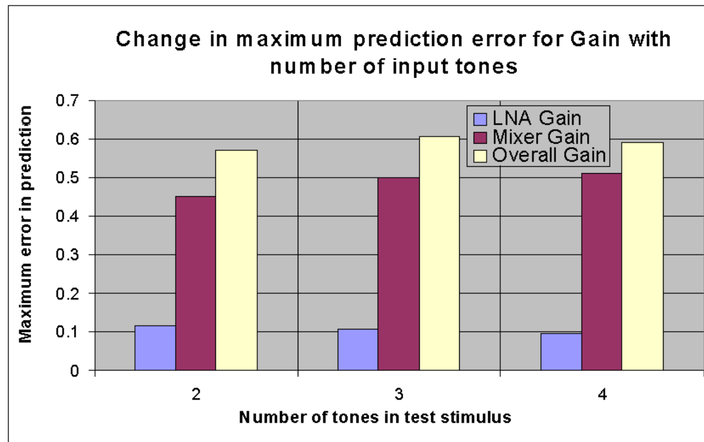


Figure 6.15. Change in maximum error for Gain with number of input tones.

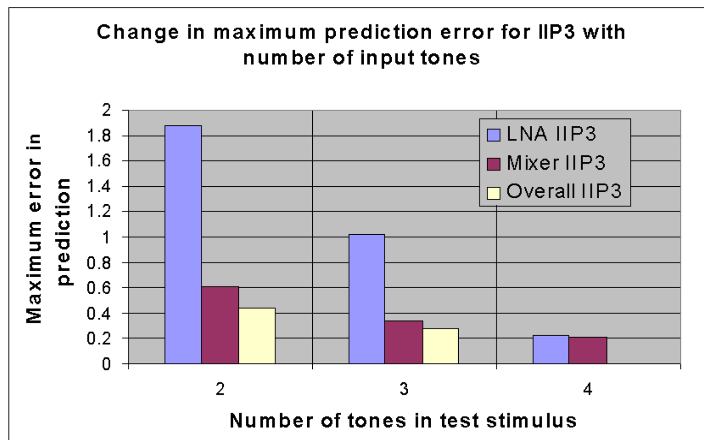


Figure 6.16. Change in maximum error for IIP3 with number of input tones.

The above experiments were conducted for two different sets of 3-tone input. The results presented in Table 6.6, has tones at 899.8MHz, 900.3MHz and 900.7MHz. This test stimulus ensures that the intermodulation terms do not overlap with the fundamental tones. Another experiment was conducted with three tones, with tones occurring at 900.1MHz, 900.2MHz, and 900.3MHz. The intermodulations generated due to the nonlinearities of the blocks overlap with the fundamentals and thus could not be distinguished separately. The modeling algorithm does not get enough visibility of the variations occurring in the sensor measurements and thus the nonlinear effects of the modules as well as the system are masked. Table 6.7 supports the above argument, showing that prediction errors have increased compared to Table 6.6.

Table 6.6. Error in prediction of system as well as module specifications using sensors (3-tone test, 20% process variation).

	LNA Gain	Mixer Gain	System Gain	LNA IIP3	Mixer IIP3	System IIP3
Error	0.3%	3.8%	0.1%	0.9%	0.2%	0.3%
Max Error	0.55	0.43	0.33	0.50	0.11	0.22

Table 6.7. Error in prediction of system as well as module specifications using sensors (3-tone test, 20% process variation).

	LNA Gain	Mixer Gain	System Gain	LNA IIP3	Mixer IIP3	System IIP3
Error	0.68%	4.8%	0.1%	3.62%	0.36%	0.22%
Max Error	0.125	0.459	0.23	0.48	0.09	0.11

Figure 6.17 shows the prediction of system specifications using sensor measurements for a 3-tone input test stimulus.

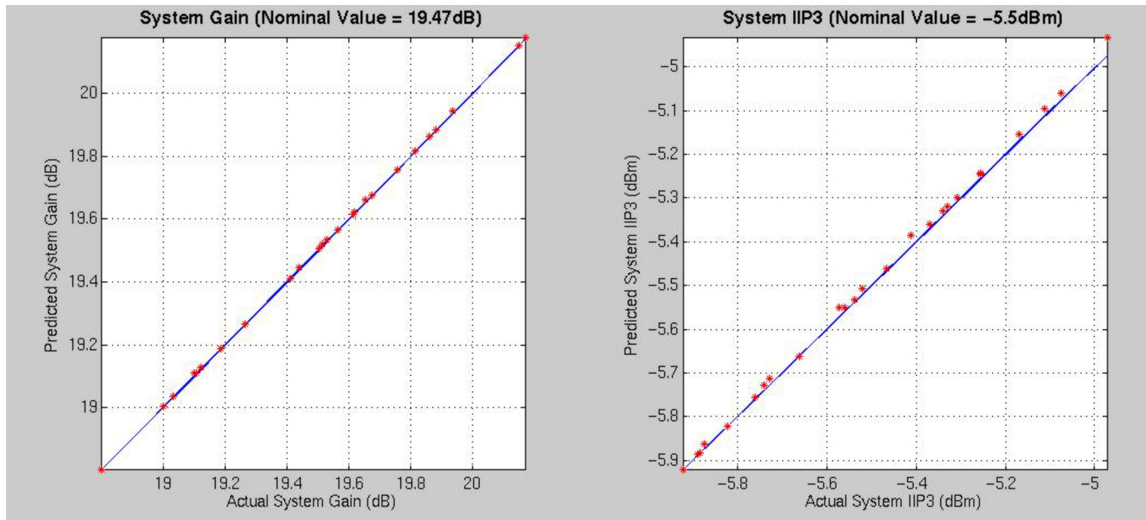


Figure 6.17. Prediction of system specifications using sensor measurements.

6.4.3. Test case: wireless receiver

Next, the actual design for the RF front-end is performed. The test vehicle for this case study was a GSM receiver. The test architecture is shown in Figure 6.18.

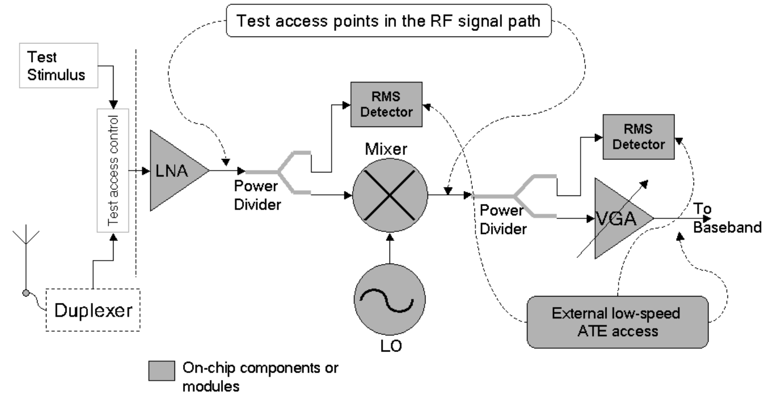


Figure 6.18. Test architecture.

6.4.3.1. Design of individual components

The system comprised of a LNA and a mixer, as shown in Figure 6.19. The individual system components were designed in HPADS. The system operates at 900 MHz, with the

LO at 850 MHz. The system was designed using NEC transistors. The LNA design used NE68530 and the mixer used NE68019 [123].

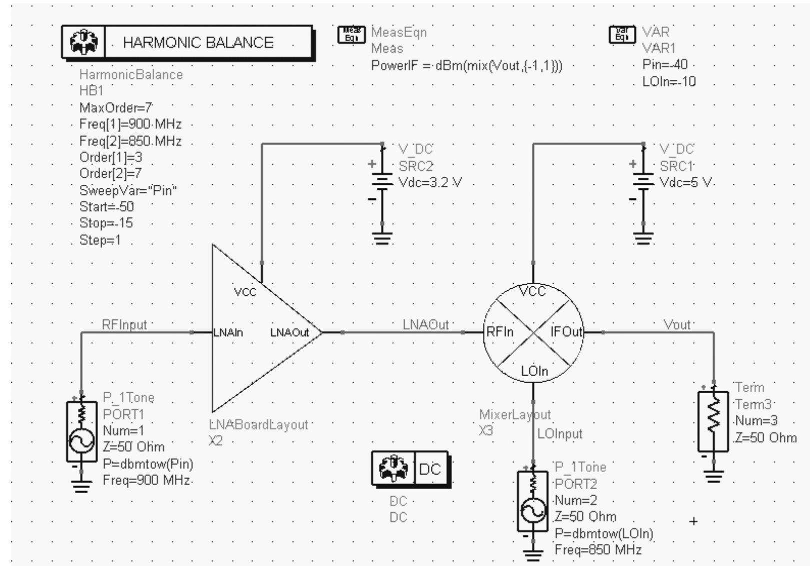


Figure 6.19. Receiver system with LNA and mixer.

Table 6.8 shows the specifications of the individual modules, viz. LNA and mixer that constitute the receiver.

Table 6.8. Individual module specifications.

LNA			**Mixer**	
Gain	NF	Stability Factor*	Conversion Gain	P_{-1dB}
10.5 dB	1.35 dB	K>1	12.3 dB	-15 dBm

The LNA and the mixer were first fabricated and characterized. Figure 6.20 and Figure 6.21 shows the characterization graphs for LNA and mixer, respectively. When both components are connected in series, they need to satisfy the stability conditions

individually to make the chain stable. For this reason, the LNA and mixer designs were carefully considered for stability during the design process.

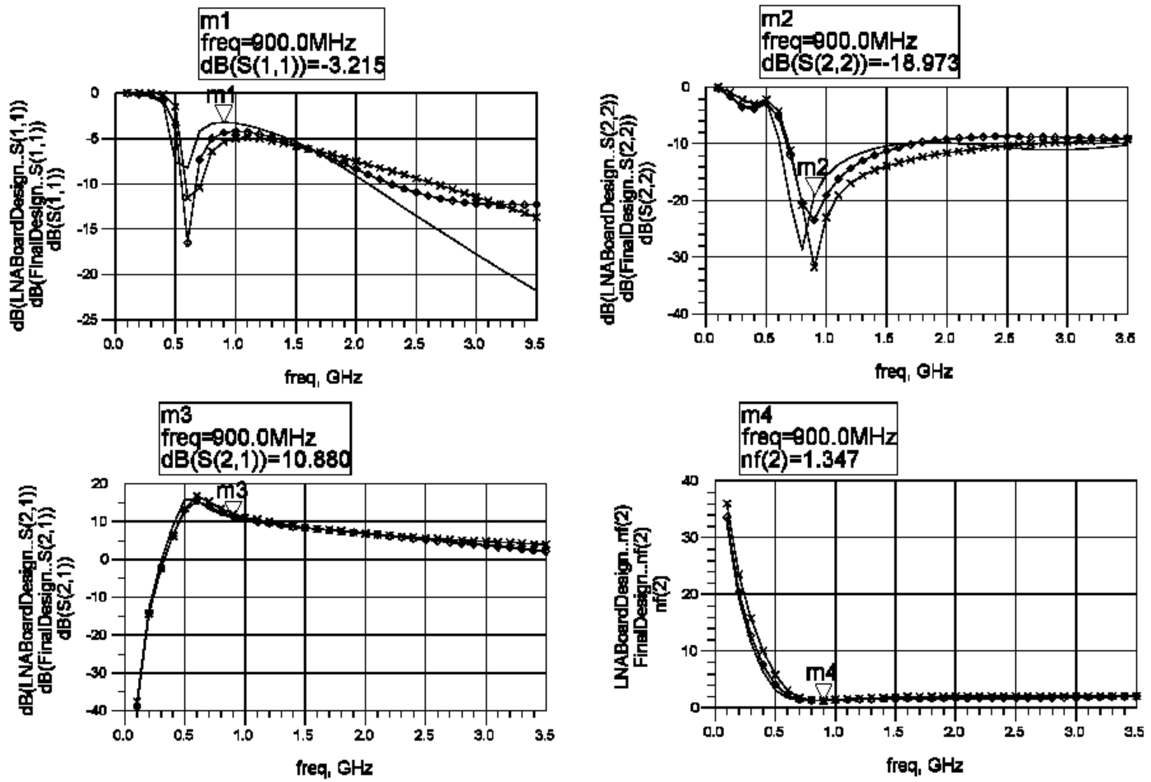


Figure 6.20. Comparison of LNA results from netlist simulation and hardware measurements.

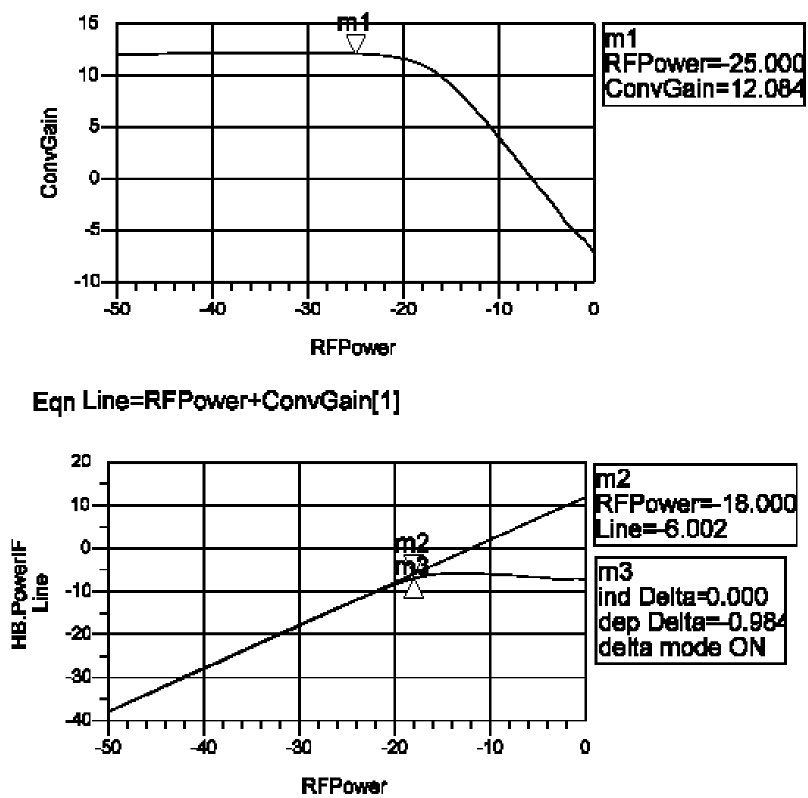


Figure 6.21. Mixer hardware measurement results.

An RMS detector was used as the sensor for this work. The sensor design was kept very simple, as shown in Figure 6.22, using diodes from Agilent (HSMS-2865)[122]. The sensor performance metrics are presented in Figure 6.23.

The sensitivity of the RMS detector is 2mV/μW. The Smith Chart shows the input matching of the RMS detector at 900 MHz. The marker "m1" indicates the design with ideal components in the schematic, and the marker "m2" indicates the changes in S11 and input matching when simulated from the final layout. As sensors were part of the circuit, they experienced process perturbations the same way as the main circuit. Therefore, separate calibration will not be required for the sensor designs.

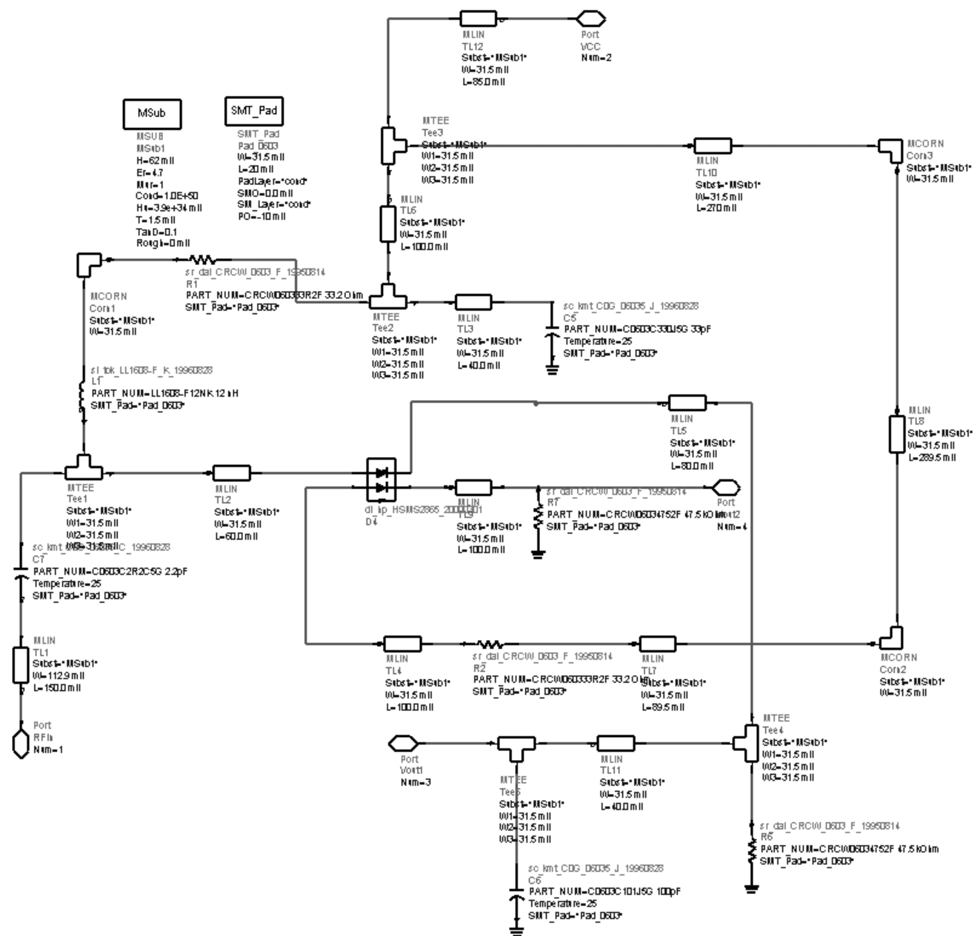


Figure 6.22. RMS detector schematic.

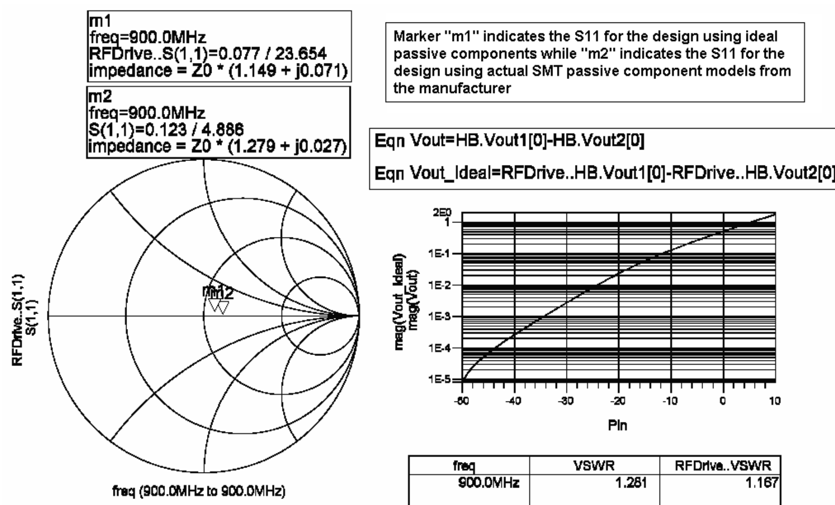


Figure 6.23. RMS detector results.

The RMS detector was designed and characterized on a printed circuit board. The designed and manufactured PCB for the RMS detector is shown in Figure 6.24. Figure 6.25 shows a comparison between the simulation and hardware measurement results.

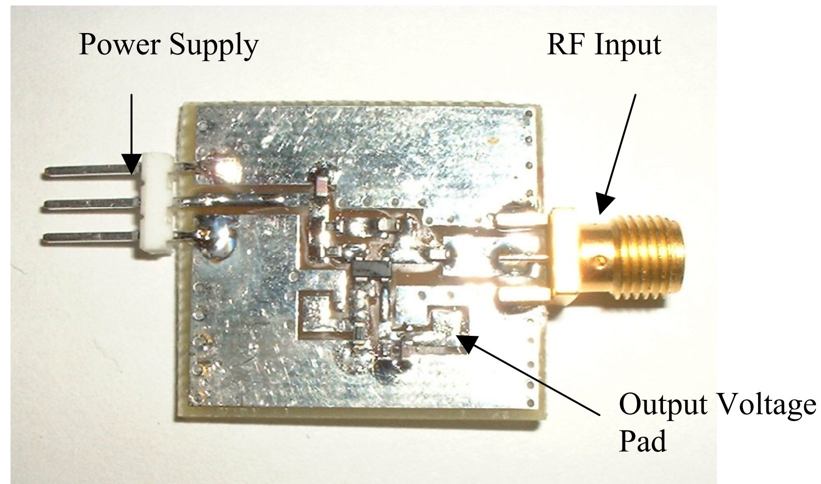


Figure 6.24 RMS detector circuit board.

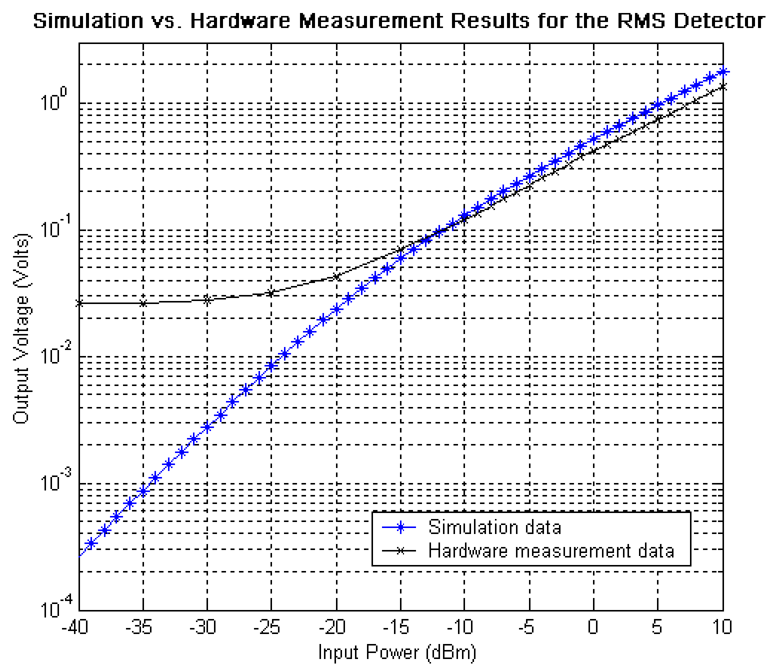


Figure 6.25 Comparison between simulation and hardware results.

Note that, for low levels of input power, the output voltage (below 25 mV, -15 dBm of input power) could not be measured accurately using the current technique (NI-DAQ card). More sophisticated methods need to be developed for this purpose.

6.4.3.2. Integration of complete system

The following figure (Figure 6.26) shows the receiver netlist with the sensors placed in the design. Note the power dividers added to the circuit to ensure that proper signal integrity is maintained for the RF signal path.

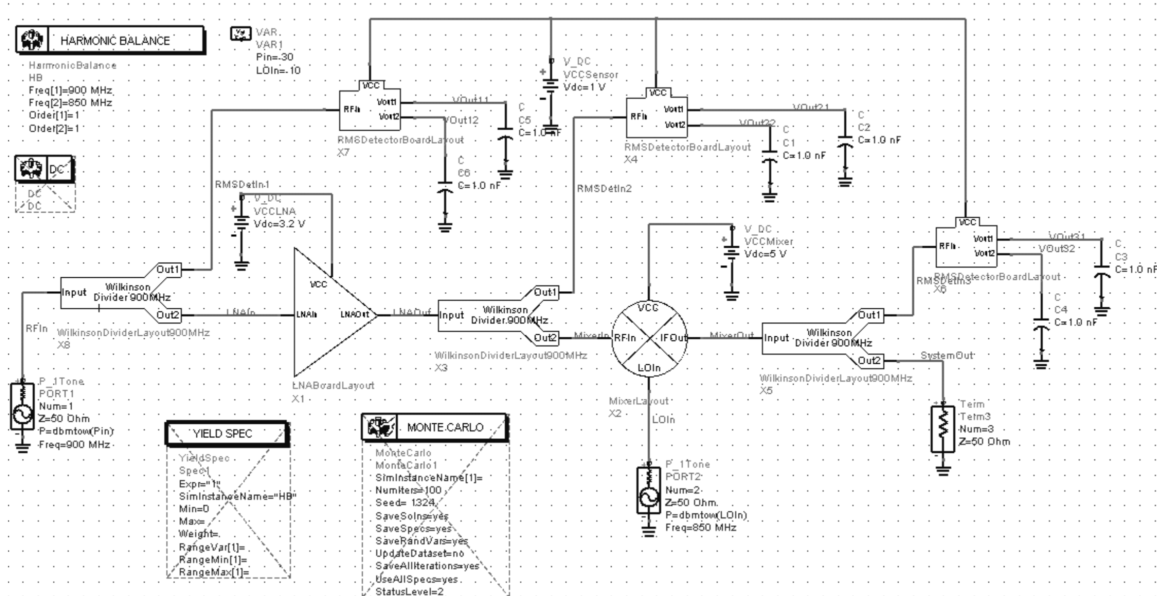


Figure 6.26. Receiver front-end with the sensors placed in the design.

A performance comparison was made between the two designs, i.e. with and without sensors and is presented in Table 6.9.

Table 6.9. Performance comparison of the receiver with and without sensors.

	Gain (dB)			IIP3 (dBm)		
	System	LNA	Mixer	System	LNA	Mixer
Without sensors	22.3	10	12.3	-14.7	-5.2	-10.8
With sensors	20.8	9.6	11.2	-15.1	-3.4	-11.2

As evident from the table, none of the specifications was affected significantly after sensors were added to the design. Therefore, sensors can be used for built-in-test purposes. The boards for the individual modules were designed. The area overhead for the sensor was less than 16% of the total board size. The board layout for the complete receiver was performed and the simulation results presented were obtained by simulating the layout. While designing the receiver, packaged component models from manufacturers were used for all active and passive SMT devices used in the DUT. Using the variations in the components, multiple instances were generated using a Monte Carlo analysis. Altogether three sensors were finally needed to predict the system and individual module specifications as presented. The sensors were put at the LNA output (RMS and peak detector) and the mixer output (RMS detector).

In the following tables, the maximum prediction errors for the specifications of interest are presented. The prediction error using just sensors to predict the test specification values and using sensors combined with the response of the receiver at the IF stage is shown in Table 6.10 and Table 6.11. The maximum loss in prediction accuracy for gain specifications was approx. 0.5 dB; for IIP3, the loss in prediction was approx. 0.65 dBm. For gain specifications, a single tone test was performed, while a 2-tone test (900 MHz and 890 MHz) was used for predicting IIP3 specifications.

Table 6.10. Gain prediction using single-tone test for the receiver.

	Prediction error using sensors	Prediction error using sensors and IF output
System Gain	0.47 dB	0.36 dB
LNA Gain	0.84 dB	0.72 dB
Mixer Gain	0.65 dB	0.48 dB

Table 6.11. IIP3 prediction using 2-tone test for the receiver.

	Prediction error using sensors	Prediction error using sensors and IF output
System IIP3	0.39 dBm	0.43 dBm
LNA IIP3	1.14 dBm	1.09 dBm
Mixer IIP3	0.46 dBm	0.33 dBm

The next two figures, one using the sensors outputs to predict the specifications (Figure 6.27) and the other with sensor and IF output combined to predict the specifications (Figure 6.28), show the predicted test specifications along with the actual test specification values.

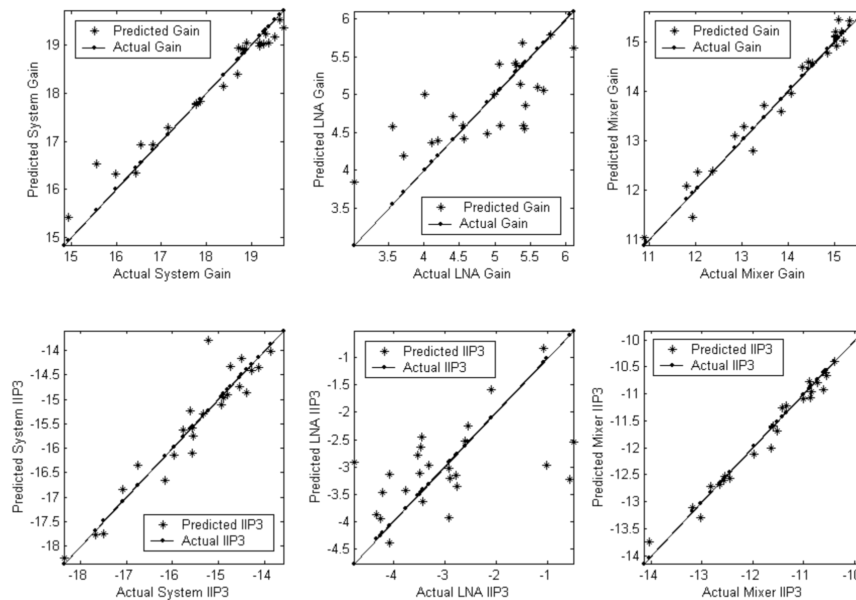


Figure 6.27. Specification prediction using sensor outputs only.

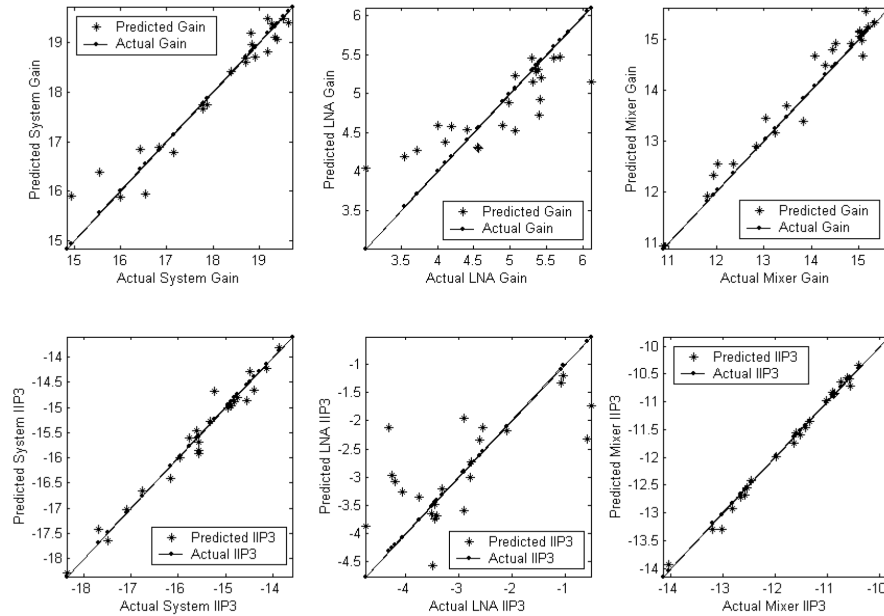


Figure 6.28. Specification prediction using sensor outputs and IF output waveform.

6.4.3.3. Hardware validation

The complete receiver board with the sensors and the front-end circuitry was designed, fabricated and characterized. First, a Monte Carlo simulation was performed on the design to generate multiple circuit instances. Using the instances, a MARS model was generated. This model was used to predict the specifications of the fabricated board using the sensor output response measurements. Table 6.12 shows the predicted and the actual specification values of the fabricated board shown in Figure 6.29 using the model built using the measurement data from simulation.

Table 6.12. Specification prediction results from the receiver board from the sensor output response measurements. *(In addition, actual specifications were measured using standard specification test methods, with sensors built-into the circuit.)*

	Gain (dB)			IIP3 (dBm)		
	System	LNA	Mixer	System	LNA	Mixer
Specifications from simulation (with sensors)	20.8	9.6	11.2	-15.1	-3.4	-11.2
Actual specifications (from hardware measurement)*	19.6	8.7	10.9	-16.8	-5.7	-13.2
Predicted specifications (from sensor output response measurements)*	20.23	9.07	11.02	-17.52	-2.27	-15.09

*measurements were performed on the fabricated board shown in Figure 6.29.

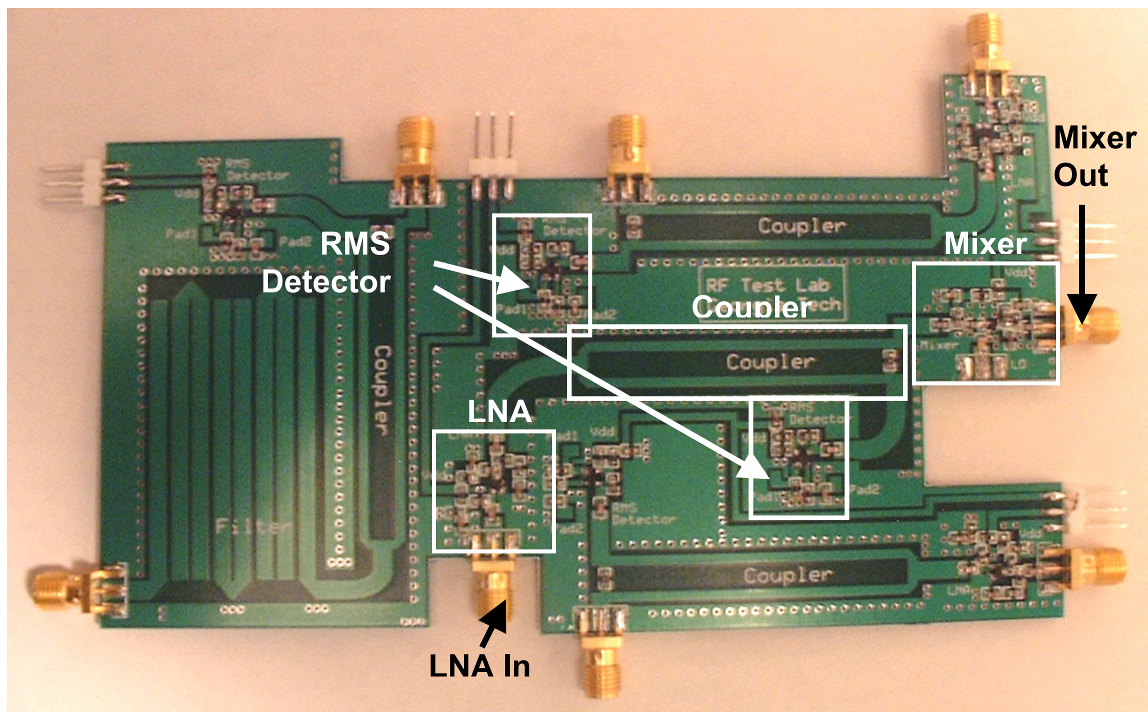


Figure 6.29. Fabricated receiver board for test purpose.

The system was applied a test stimulus of 900 MHz, -33 dBm, as shown in Figure 6.30. Figure 6.31 shows the IF output spectrum (50 MHz, -12.5 dBm) and the different leakage components (LO @ 850 MHz, -52 dBm and RF @ 900 MHz, -61 dBm).

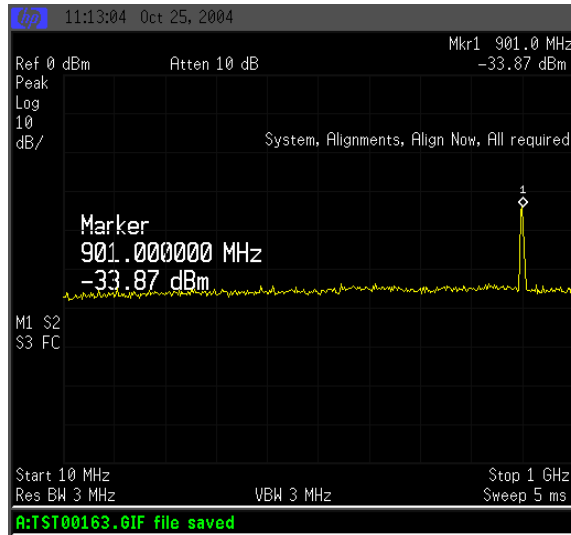


Figure 6.30. Input test stimulus to the receiver.

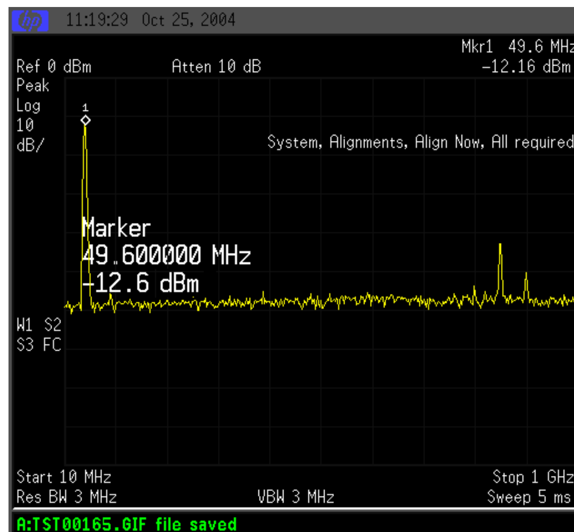


Figure 6.31. Output IF waveform from the receiver.

6.4.3.4. Production test emulation

Production testing of wireless systems involves testing large number of parts. In the above experiment performed, the model for specification prediction was built from simulation data and the validation was performed from hardware measurement. However, this is not the case in a production test environment. In production test environment, the

model will be built from measurements performed on actual devices and then it will be used to predict specifications using the measurements from other set of devices.

For this reason, a separate board was built with sockets and a large number of commercial, off-the-shelf devices were purchased to mimic the actual production test environment. Altogether, 100 LNAs (RF2304) and mixers (RF2411) were used to generate 100 instances of a RF receiver. This receiver block used two RMS detectors as sensors for test response measurement purposes. The sensor outputs for 75 devices were used to build the model and the model was validated on the other set of 25 devices. The following figures and the table summarize the results.

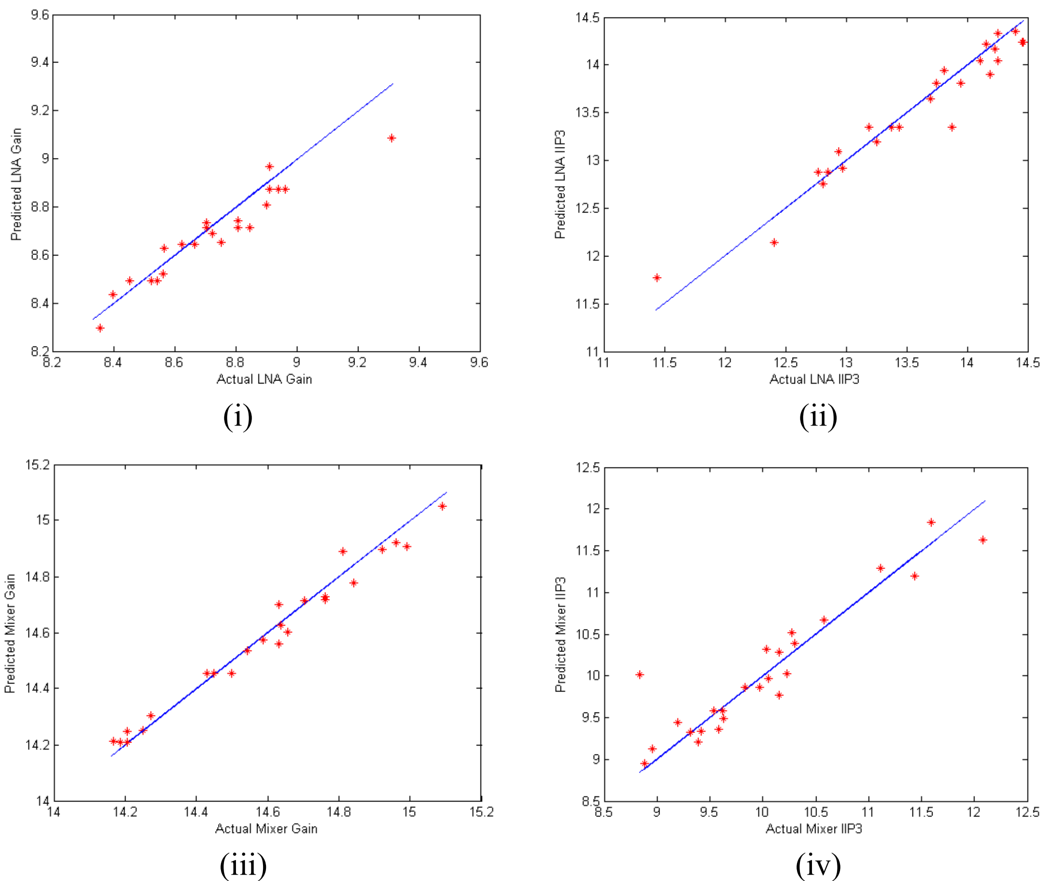


Figure 6.32. Comparison of actual specification values and the predicted specifications (i) LNA gain (ii) LNA IIP3 (iii) Mixer gain and (iv) Mixer IIP3

Table 6.13. Mean, maximum and minimum error values in prediction using the model from the response measurements of the sensors

	Prediction error using sensors		
	Mean error	Max error	Min error
System Gain	0.37 dB	1.01 dB	0.06 dB
LNA Gain	0.24 dB	0.72 dB	0.02dB
Mixer Gain	0.15 dB	0.39 dB	0.01 dB
System IIP3	1.45 dBm	2.32 dBm	0.09 dBm
LNA IIP3	0.67 dBm	1.92 dBm	0.02 dBm
Mixer IIP3	1.01 dBm	2.17 dBm	0.06 dBm

The following figure (Figure 6.33) shows the test setup for this experiment performed.

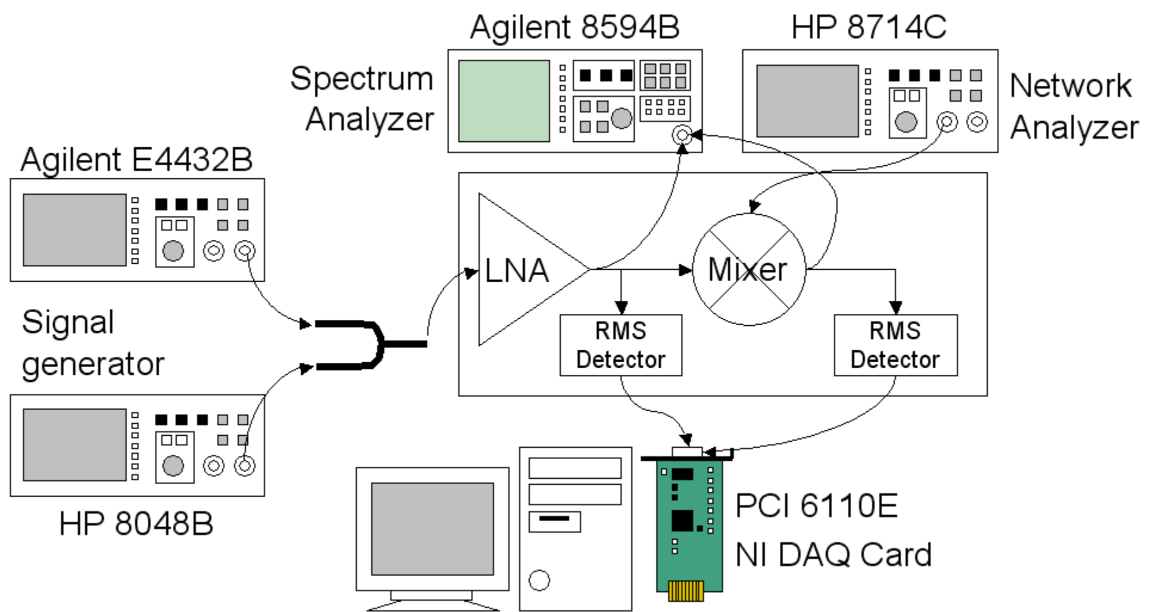


Figure 6.33. Test setup used to emulate production testing

As it seems from the above data, the specifications of the individual modules cannot be computed (estimated) from the sensor response measurements. This can be attributed to the following:

- The devices used to perform the experiment were obtained from different lots of production of the manufacturer. This was to ensure that there were enough variations among the devices. Yet, the amount of variation between the devices was not significant enough to build a highly correlated model between the specification values and the response measurements from sensors.
- The devices tested were robust against power supply variations. The nominal supply voltage is around 5V (8.5 dB gain), but to diminish the performance of the devices, the power supply was brought down to 1V. Still, the gain was in the order of 5.7 dB. Thus, it was not possible to generate bad instances of the device by reducing the supply voltage.
- The sensor output is captured by a digitizer (NI-DAQ card PCI 6110-E). The inherent noise in the data capture card is in the order of 2.5 mV (obtained by free running of the DAQ channel and averaging over a long duration, i.e. large number of samples). The sensor outputs are in the order of 130-150 mV. Therefore the DAQ itself poses an error of ~2% in the data.
- Noise contributions from spectrum analyzers, phase noise of RF signal generators and DC power supplies contribute to the prediction accuracy as well.

6.5. Concluding remarks

During the last decade, advances in wireless design techniques and migration to smaller feature sizes in silicon manufacturing has significantly reduced the cost of RF and high-speed wireless devices. However, opposing the trends in other sectors of the semiconductor industry, production test cost has increased manifold due to various limitations in the test industry. The increase in production test cost can be attributed to

two factors: time required for performing production tests and the cost of test instrumentation, including ATEs, used during production test.

In order to reduce the overall test cost for high-speed devices, we propose to use built-in sensors in the device or the system under test. Instead of using complex test instruments at the device response outputs, the sensor outputs are used to compute the system level as well as device level specifications. The sensor outputs are usually low frequency or DC signals and they compute various features of the signals, internal to the complete system. These nodes are not visible to the outside world and hence, the sensors provide a better understanding of the system's operation through the observation of its output responses. These responses from the sensors are related to the specifications of the system using a model, composed of a set of nonlinear equations. During production test, the sensor output responses are input to the model and the specifications are computed directly with a high degree of accuracy, without performing any explicit measurements for the specifications.

Mainly, RMS detectors and peak detectors were used as sensors in this work. The choice of sensors was kept simple for easy designs and low area overhead during silicon implementation. The sensors are placed at strategic nodes of the complex device under test using a sensor placement algorithm to maximize the specification prediction accuracy from the output responses of the sensors. At the same time, a test generation algorithm was also developed and specific tests were tailored to achieve high degree of accuracy in specification prediction. The target tests were for measuring gain and nonlinearities of the system as well as the devices constituting the system. The results from the simulation

studies performed showed very high degree of accuracy in system level specification prediction.

This method was also verified through hardware measurements. A receiver was designed with all the sensors added at specific nodes, obtained from the sensor placement algorithm. Next, test stimuli were determined to maximize the prediction accuracy using the sensors. A Monte-Carlo simulation was performed on the netlist and the nonlinear model relating the specifications to the output responses of the sensors was calculated. The receiver board was next fabricated and measurements were made at the sensor outputs. Using these responses and the model developed earlier, specifications of the fabricated receiver board were measured. All the specifications were predicted very accurately from the measurements.

The final step of this work was to emulate a production test environment. For this purpose, a PCB with sockets was built, where devices may be inserted, tested and binned based on its performance. In addition, sensors were built into the board and sensor output responses were measured for specification prediction. Initially, 75 devices were tested, and the model relating the specifications to the sensor responses were built. Next, this model was used to predict the specifications of 25 other devices. From the sensor response measurement, gain and nonlinearity related specifications could be predicted very accurately (3% error in measurement).

6.5.1. Novelties of the work performed

The various aspects of the proposed method make it amenable to application in an industrial environment. The features of this method include:

- Using built-in sensors, system level as well as device level specifications can to predicted with a high degree of accuracy.
- Test time is reduced significantly. In addition, the sensor outputs are usually low frequency or DC. Therefore, low-cost ATEs can be used to capture sensor output responses. This reduces the overall production test cost significantly.
- The device interface board (DIB) is simplified significantly during production testing.
- The sensors can be used for on-line testing of the devices and the system.

6.5.2. Shortcomings

In the proposed method, the sensors are designed into the system. The shortcomings of this method are as follows:

- The inclusion of the sensors into the system may cause the system to perform worse than the original design. Thus, extra design iterations may be needed in such cases to compensate for the effects of the sensors on the overall system performance.
- The sensors occupy a portion of the overall silicon space. Therefore, sensor designs need to be simple to reduce the silicon area overhead.
- As this method relies heavily on the sensors for estimating the system performance, there needs to be a initial step during production test where the sensors are tested and characterized before they are used to perform system-level testing. In case where a sensor fails to meet its own specifications, standard tests can be performed on the system.

6.5.3. Future trends: Integration of sensors in high-speed systems

The proposed method shows immense potential in predicting the specifications of a system as well as its internal modules by migrating the test resources on-chip. The method proposed, combined with the sensor placement and test generation algorithm, can reduce the overall test complexity and the cost of testing RF and other high-speed devices significantly in a production test environment. The future work in this direction will be to integrate sensors within a complete high-speed or RF system, where sensors will be an integral part of the system and will be used in estimating system performance by measuring the specifications of interest. Apart from specifications, this information can be intelligently used to diagnose the reasons of failure of a device and correct it through efficient use of redundancy or by rerouting the signals for an adaptive system level design approach.

Chapter VII
References

[1] J.B.Brockman and S.W.Director, "Predictive Subset Testing: optimizing IC parametric performance for quality, cost and yield," *IEEE Tran. on Semiconductor Manufacturing,* vol. 2, no. 3, 1989, pp. 104-113.

[2] L.Milor and V.Viswananathan, "Detection of catastrophic faults in analog integrated circuits," *IEEE Tran. on Computer Aided Design of Integrated circuits and Systems,* vol. 8, no. 2, 1989, pp. 114-130.

[3] M.Soma and G.Devarayanadurg, "Analytical fault modeling and static test generation for analog ICs," *Proc., IEEE International conference on computer-aided design,* Nov. 1994, pp. 44-47.

[4] N.Nagi, A.Chatterjee, A.Balivada and J.A.Abraham, "Fault based automatic test generator for linear analog devices," *Proc., Intl. Conf. on Computer-Aided Design,* Nov. 1993, pp. 88-91.

[5] M.Salamani, B.Kaminska and G.Quesnel, "An integrated approach for analog circuit testing with minimum number of detected parameters," *Proc., IEEE Intl. Test Conf.,* 1994, pp. 631-640.

[6] A.Abderrahaman, E.Cerny and B.Kaminska, "CLP-based multi-frequency test generation for analog circuits," *Journal of Electronic Testing Theory and Applications,* vol. 9. 1996, pp. 59-73.

[7] H.H.Zheng, A.Balivada, and J.A.Abraham, "A novel test generation approach for parametric faults in linear analog circuits," *Proc., IEEE VLSI Test Symposium*, 1996, pp. 470-475.

[8] Sheng-Jen Tsai. "Test vector generation for linear analog devices," *Proc., IEEE Intl. Test Conf.* 1991, pp. 592-597.

[9] A.Balivada, J.Chen and J.A.Abraham, "Analog testing with time response parameters," *IEEE Design and Test of Computers,* vol. 13, no. 2, 1996, pp. 18-25.

[10] P.N.Variyam and A.Chatterjee, "Test generation for comprehensive testing of linear analog circuits using transient response sampling," *Proc., IEEE Intl. Conf. on Computer Aided Design,* 1997, 382-385.

[11] P.N.Variyam and A.Chatterjee, "Enhancing test effectiveness for analog circuits using synthesized measurements," *Proc., IEEE VLSI Test Symp.,* 1998, 132-137.

[12] R.Voorakaranam and A.Chatterjee, "Test Generation for Accurate Prediction of Analog Specifications," *Proc., IEEE VLSI Test Symp.,* 2000, 137-142.

[13] S.Bhattacharya and A.Chatterjee, "Constrained Specification-Based Test Stimulus Generation for Analog Circuits Using Nonlinear Performance Prediction Models," *DELTA,* 2002, pp. 25-29.

[14] S.Bhattacharya and A.Chatterjee, "Wafer Probe and Assembled Package Test Co-Optimization for Minimal Test Cost," *Intl. Mixed Signal Test Workshop,* 2002, pp. 15-20.

[15] S.Bhattacharya and A.Chatterjee, "High Coverage Analog Wafer-Probe Test Design and Co-optimization with Assembled-Package Test to Minimize Overall Test Cost," *Proc., IEEE VLSI Test Symposium*. 2003.

[16] S.Bhattacharya and A.Chatterjee, "Wafer-probe and Assembled-Package Test Co-optimization to Minimize Overall Test Cost," *ACM Transactions on Design Automation of Electronic Systems,* vol. 10, no.2, 2005, pp. 303-329.

[17] Electroglas 4090 Fast Prober Data Sheet (http://www.electroglas.com).

[18] Aetrium 55v6 Test Handler Data Sheet (http://www.aetrium.com).

[19] J.H.Friedman, "Multivariate Adaptive Regression Splines" *The Annals of Statistics*, vol. 19, no. 1, pp. 1-141.

[20] D.E.Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning," Addison-Wesley Publishing Company, January 1989.

[21] N.Chaiyaratana, and A.M.S.Zalzala, "Recent developments in evolutionary and genetic algorithms: theory and applications," *IEE Genetic Algorithms in Engineering Systems: Innovations and Applications.* Pub. No. 446, 1997, pp. 270-277.

[22] MATLAB Optimization Toolbox User's Guide and MATLAB Statistics Toolbox User's Guide.

[23] W.H.Press, S.A.Teukolsky, W.T.Vellerling, and B.P.Flannery, "Numerical Recipes in C: The Art of Scientific Computing," Cambridge University Press, 2nd Edition, 1998.

[24] P.E.Allen, and D.R.Holberg, "CMOS Analog Circuit Design." Oxford University Press, 2nd Edition, 2002.

[25] P.R.Gray, P.J.Hurst, S.H.Lewis, and R.G.Meyer, 2001. "Analysis and Design of Analog Integrated Circuits" John Wiley and Sons, 4th Edition, 2001.

[26] J.Neter, M.H.Kutner, C.J.Nachtfheim, and W.Wasserman, "Applied Linear Statistical Models," WCB/McGraw-Hill, 4th Edition, 1996.

[27] Semiconductor Research Corporation (http://www.src.org).

[28] National Semiconductor LM318 Data Sheet.

[29] National Instruments Data Acquisition Card (NI PCI-6110) User Manual.

[30] B.Razavi, "RF Microelectronics," Prentice Hall, NJ, 2nd Editions, 1998, ch. 1-2, pp. 1-53.

[31] T.H.Lee, "The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge University Press, 2002, ch. 11-12, ch. 16, pp. 272-340.

[32] Openbook Cadence Spectre Simulation Handbook, December 1999.

[33] J.E.Dennis, Jr., and Robert B.Schnabel, "Numerical Methods for Unconstrained Optimization and Nonlinear Equations," Society for Industrial & Applied Mathematics, Feb 1996.

[34] "Agilent 84000 RFIC Series Test Systems – Product Overview", Agilent Technologies.

[35] M.Jarwala, D.Le, M.S.Heutmaker, "End-to-end test strategy for Wireless Systems," *Proc., IEEE Intl. Test Conference*, 1995, pp. 940-946.

[36] S.Ozev, C.Olgaard and A.Orailoglu, "Testability implications in low-cost integrated radio transceivers: A Bluetooth case study," *Proc., IEEE Int'l Test Conf.*, 2001, pp. 965-974.

[37] S.Ozev, A.Orailoglu and H.Haggag, "Automated test development and test time reduction for RF subsystems," *Proc., IEEE Intl. Symp. on Circuits and Systems,* vol. 1, 2002, pp.I-581 – I-584.

[38] J.Lukez, "Novel techniques for wideband RF test," *Proc., IEEE Electronics Manufacturing Tech. Symp.*, 2002, pp. 423-425.

[39] B.R.Veillette and G.W.Roberts, "A built-in self-test strategy for wireless communication systems," *Proc., IEEE Int'l Test Conf.*, 1995, pp. 930-939.

[40] K.S.Kundert, "Introduction to RF simulation and its Application," *IEEE Journal of Solid-state Circuits*, vol.34, no. 9, 1999, pp. 1298-1319.

[41] J.Zhao, " Behavioral Modeling of RF Circuits in Spectre," *Cadence white paper*, March 5, 1999

[42] P.N.Variyam, S.Cherubal and A.Chatterjee, "Prediction of Analog Performance Parameters Using Fast Transient Testing", *IEEE Trans. CAD of Integrated Circuits and Sys.,* vol. 21, no. 3, 1992, pp. 349-361.

[43] P.N.Variyam and A.Chatterjee, "Enhancing test effectiveness for analog circuits using synthesized measurements", *Proc., IEEE VLSI Test Symp.*, 1998, pp. 132–137.

[44] R.Voorakaranam and A.Chatterjee, "Test Generation for Accurate Prediction of Analog Specifications," *Proc., IEEE VLSI Test Symp.*, 2000, pp. 137-142.

[45] A.Halder, S. Bhattacharya and A. Chatterjee, "Automatic Multitone Alternate Test Generation for RF Circuits Using Behavioral Models", *Proc., IEEE Intl. Test Conf.,* 2003, pp. 665-573.

[46] S.Bhattacharya, A. Halder, A.Chatterjee, "Automatic Alternate Test Generation for RF Circuits Using Behavioral Models," *TECHCON* 2003.

[47] S. Bhattacharya, G. Srinivasan, S. Cherubal, A. Halder and A. Chatterjee, "System-level Testing of RF Transmitter Specifications using Optimized periodic Bitstreams," *Proc., IEEE VLSI Test Symp.,* 2004, pp. 229-234.

[48] G.Srinivasan, A.Halder, S.Bhattacharya and A.Chatterjee, "Loopback Test of RF Transceivers Using Periodic Bit Sequences: an Alternate Test Approach", *International Mixed-Signal Test Workshop,* 2004, pp. 69-75.

[49] Andrew Hamilton, Richard Schofield, "An Expert System for Process Diagnosis," *Proc. IEEE Intl. Conf. On Microelectronics Test Structures*, vol. 2, no. 1,1989, pp. 55-57.

[50] M.M.Moslehi, L.Velo, H.Nazm, T.Breedijk and B.Dostalik, "Sensor Fusion for ULSI Manufacturing Process Control," *Symp. on VLSI Technology Digest of Technical Papers,* 1992, pp. 50-51.

[51] R.Guo, C.Tsai, J.Lee and S.Chang, "Intelligent Process Diagnosis Based on End-of-line Electrical Test Data," *Intl. Electronics Manufacturing Technology Symp.,* 1996, pp. 347-354.

[52] M.W.Cresswell, D.Khera, L.W.Linholm and C.E.Schuster, "A Directed-graph Classifier of Semiconductor Wafer-test Patterns," *IEEE Trans. on Semiconductor Manufacturing*, vol. 5, no. 3, 1992, pp. 255-263.

[53] J.Dishaw and J.Y.Pan, "AESOP: A Simulation-based Knowledge System for CMOS Process Diagnosis," *IEEE Trans. on Semiconductor Manufacturing*, vol. 2, no. 3, 1989, pp. 94-103.

[54] S.Saxena and A.Umruh, "Diagnosis of Semiconductor Manufacturing Equipments and Processes," *IEEE Trans. on Semiconductor Manufacturing*, vol. 7, no. 2, 1994, pp. 220-232.

[55] D.A.White, D.Boning, S.W.Butler and G.G.Barna, "Spatial Characterization of Wafer State Using Principal Component Analysis of Optical Emission Spectra in

Plasma Etch," *IEEE Trans. on Semiconductor Manufacturing*, 1997, vol. 10, no.1, pp. 52-61.

[56] I.Jolliffe, "Principal Component Analysis," New York: Springer-Verlag, 2nd Edition, 2002.

[57] B.Wise, N.Ricker, D.Veltkamp, and B.Kowalski, "A theoretical basis for the use of principal component models for monitoring multivariate processes," *Process Control and Quality*, 1990, pp. 41–51.

[58] K.Saito, M.Sakaue, T.Okubo and K.Minegishi, "Application of Statistical Analysis to Determine the Priority for Improving LSI Technology," *IEEE Trans. on Semiconductor Manufacturing*, vol. 5, no. 1, 1992, pp. 47-54.

[59] H.C.Fu and J.J.J.Shann, " A Fuzzy Neural Network for Knowledge Learning," *Int. Journal on Neural Systems*, vol. 5, no. 1, 1994, pp. 13-22.

[60] R.Ramamurthi, "Self-learning Fuzzy Logic System for In Situ, In-process Diagnostics of Mass Flow Controller" *IEEE Trans. on Semiconductor Manufacturing*, vol.7, no. 1, 1994, pp. 42-52.

[61] S.Bhattacharya and A.Chatterjee, "A Fast Process Diagnosis Method Using Diagnosis Core", *International Mixed-Signal Test Workshop*, 2003.

[62] D.Porcino, W.Hirt, "Ultra-wideband radio technology: potential and challenges ahead," *Communications Magazine, IEEE*, vol. 41, no. 7, July 2003, pp. 66 – 74.

[63] L.D.Paulson, "Will ultrawideband technology connect in the marketplace?" *Computer*, vol. 36,no. 12, Dec. 2003, pp. 15 – 17.

[64] G.R.Aiello, G.D.Rogerson, "Ultra-wideband wireless systems," *IEEE Microwave Magazine*, vol. 4, no. 2, June 2003, pp. 36 – 47.

[65] Multiband OFDM Alliance: http://www.multibandofdm.org/

[66] S.Roy, J.R.Foerster, V.S.Somayazulu, D.G.Leeper, "Ultrawideband Radio Design: The Promise of High-Speed, Short-Range Wireless Connectivity," *Proceedings of the IEEE*, vol. 92, no. 2, Feb 2004, pp. 295 – 311.

[67] Agilent application note "Agilent Ultra-Wideband Communication RF Measurements," Application note AN1488.

[68] Agilent application note "Characterizing Digitally Modulated Signals with CCDF Curves".

[69] Agilent application note "Agilent Technologies Wireless Test Solutions," Application note AN1313.

[70] M.Hamalainen, V.Hovinen, R.Tesi, J.H.J.Iinatti, M.Latva-aho, "On the UWB system coexistence with GSM900, UMTS/WCDMA, and GPS," *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 9, Dec. 2002, pp. 1712 – 1721,

[71] L.Zhao, A.M.Haimovich, "Performance of ultra-wideband communications in the presence of interference," *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 9, Dec. 2002, pp. 1684 – 1691,

[72] J.Bellorado, S.S.Ghassemzadeh, L.J.Greenstein, T.Sveinsson, V.Tarokh, "Coexistence of Ultra-Wideband Systems with IEEE-802.11a Wireless LANs", *Proc., IEEE Global Telecommunications Conference*, 2003, vol. 1, pp. 410 – 414.

[73] A.Swami, B.Sadler, J.Turner, "On the coexistence of ultra-wideband and narrowband radio systems", *Proc., IEEE Military Communications Conference, Communications for Network-Centric Operations: Creating the Information Force*, vol. 1, Oct. 2001, pp. 16 – 19.

[74] M.Schmidt, F.Jondral, "Ultra Wideband Transmission based on MC-CDMA," *Proc., IEEE Global Telecommunications Conference*, vol. 2, Dec 2003, pp. 749 – 753.

[75] D.K.Borah, R.Jana, A.Stamoulis, "Performance evaluation of IEEE 802.11a wireless LANs in the presence of ultra-wideband interference," *Proc., IEEE Wireless Communications and Networking,* vol. 1, March 2003, pp. 83 – 87.

[76] D.Cassioli, M.Z.Win, A.F.Molisch, "The ultra-wide bandwidth indoor channel: from statistical model to simulations," *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 6, Aug. 2002, pp. 1247 – 1257.

[77] A.Saleh, R.Valenzuela, "A Statistical Model for Indoor Multipath Propagation," *IEEE Journal on Selected Areas in Communications*, vol. 5, no. 2, Feb 1987, pp. 128 – 137.

[78] M.Z.Win, R.A.Scholtz, "Characterization of ultra-wide bandwidth wireless indoor channels: a communication-theoretic view," *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 9, Dec. 2002, pp. 1613 – 1627.

[79] A.Batra, "Achieving High Speed Wireless Communications Using a Multi-Band OFDM UWB System," Ultrawideband Radio Communications, ISCAS, May 2004.

[80] IEEE proposal "Multi-band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a," Document Number P802.15-03/268r3, March 2004.

[81] ITRS public document "International Technology Roadmap for Semiconductors - 2004 update – Test and Test Equipment".

[82] P.N. Variyam, S. Cherubal and A. Chatterjee, "Prediction of Analog Performance Parameters Using Fast Transient Testing," *IEEE Trans. CAD of Integrated Circuits and Sys.*, vol. 21, no. 3, 1992, pp. 349-361.

[83] The International Engineering Consortium (IEC) Web ProForum Tutorials, "OFDM for Mobile Data Communications," http://ww.iec.org.

[84] M.B.Showmake, "Multi-Band OFDM Update and Overview," *Multiband OFDM Alliance SIG*, September 2004.

[85] D.Williams, A.P.Ambler, "System manufacturing test cost model," *Proc., Intl. Test Conference*, Oct. 2002, pp. 482 – 490.

[86] Agilent website, http://www.agilent.com

[87] Tektronix website, http://www.tektronix.com

[88] E.W.Weisstein, "Fast Fourier Transform" from MathWorld (http://mathworld.wolfram.com/FastFourierTransform.html) -A Wolfram web resource.

[89] S.Bhattacharya and A.Chatterjee, "Production Test Methods for Measuring 'Out-of-band' Interference of Ultra Wide Band (UWB) Devices," *Proc., IEEE VLSI Test Symposium*, Palm Springs, CA, May 2005, pp. 137-142.

[90] S.Bhattacharya, R.Senguttuvan and A.Chatterjee, "Production Test Method for Evaluating the Effect of Narrow-band Interference on Data Errors in Ultra-Wide Band (UWB) Receivers," *Proc., IEEE MTT-S International Microwave Symposium*, Long Beach, CA, June 2005.

[91] S.Bhattacharya, R.Senguttuvan and A.Chatterjee, "Production Test Enhancement Techniques for MB-OFDM Ultra Wide Band (UWB) Devices: EVM and CCDF," *Proc., IEEE Intl. Test Conference*, Nov. 2005 (to appear).

[92] J.E.Padgett, et al, "Overview of Wireless Personal Communication," *IEEE Communications Magazine*, January 1995, pp. 28-41.

[93] J.F.Sevic and J.Staudinger, "Simulation Of Power Amplifier Adjacent-Channel Power Ratio for Digital Wireless communication Systems," *Proc., IEEE 47th Vehicular Technology Conference*, vol. 2, May 1997, pp. 681 -685.

[94] N.Despande, et al, "ACPR Specs Place Demands on WCDMA Base-Station Amplifiers," *Wireless Systems Design Magazine*, August 1999, pp. 15-22.

[95] Autocorrelation – from Mathworld, A Wolfram web resource, website: http://mathworld.wolfram.com/Autocorrelation.html

[96] J.Neter, et al, "Applied Linear Statistical Models," Mc-Graw Hill/Irwin, 4th Edition, 1996.

[97] A.V.Oppenheim and R.W.Schafer, "Discrete-Time Signal Processing", Prentice Hall, 2nd Edition, 1999.

[98] W.Struble, et al, "Understanding Linearity in Wireless Communication Amplifiers," *GaAs IC Symposium*, 1996, pp. 295-298.

[99] S.C.Cripps, "RF Power Amplifiers for Wireless Communications", Artech House, 1999.

[100] A.Raghavan, et al, "A 2.4 GHz high efficiency SiGe HBT power amplifier with high-Q LTCC harmonic suppression filter," *IEEE MTT-S International Microwave Symposium Digest*, vol.2, 2002, pp. 1019-1022.

[101] B.Kruseman, et al, "Transient current testing of 0.25µm CMOS devices," *Proc., IEEE Intl. Test Conference*, September 1999, pp. 47-56.

[102] S.Bhattacharya, G.Srinivasan, S.Cherubal and A.Chatterjee, "Test Time Reduction for ACPR Measurement of Wireless Transceivers Using Periodic Bit-Stream Sequences," *DELTA*, Jan 2004, pp. 372-377.

[103] G.Srinivasan, S.Bhattacharya and A.Chatterjee, "Efficient Test Strategy for TMDA Power Amplifiers Using Transient Current Measurements: Uses and Benefits," *Design and Test in Europe*, vol. 1, Feb 2004, pp. 280-285.

[104] M.Ehsanian, B.Kaminska, K.Arabi, "A new digital test approach for analog-to-digital converter testing," *Proc., VLSI Test Symposium*, 1996, pp. 60 – 65.

[105] C.L.Wey, "Built-in self-test (BIST) structure for analog circuit fault diagnosis," *IEEE Transactions on Instrumentation and Measurement*, vol. 39, no. 3, June 1990, pp. 517 – 521.

[106] L.Carro, E.Cota, M.Lubaszewski, Y.Bertrand, F.Azais, M.Renovell, "TI-BIST: a temperature independent analog BIST for switched-capacitor filters," *Proc., Asian Test Symposium*, 2000, pp. 78 – 83.

[107] M.F.Toner, G.W.Roberts, "A BIST scheme for a SNR, gain tracking, and frequency response test of a sigma-delta ADC," *IEEE Transactions on Analog and Digital Signal Processing: Circuits and Systems II*, [see also IEEE Transactions on Circuits and Systems II: Express Briefs], vol. 42, no. 1, Jan. 1995, pp. 1-15.

[108] A.A.Hatzopoulos, S.Siskos, J.M.Kontoleon, "A complete scheme of built-in self-tests (BIST) structure for fault diagnosis in analog circuits and systems," *IEEE Transactions on Instrumentation and Measurement*, vol. 42, no. 3, June 1993, pp. 689 – 694.

[109] A.Walker, P.K.Lala, “A dual edge transition based BIST approach for passive analog circuits,” *Southwest Symposium on Mixed-Signal Design*, 2000, pp. 179 – 181.

[110] J.Velasco-Medina, I.Rayane, M.Nicolaidis, “AC/DC BIST for testing analog circuits,” *12th Annual IEEE ASIC/SOC International Conference*, 1999, pp. 223 – 227.

[111] M.F.Toner, G.W.Roberts, “A frequency response, harmonic distortion, and intermodulation distortion test for BIST of a sigma-delta ADC,” *IEEE Transactions on Analog and Digital Signal Processing: Circuits and Systems II*, [see also: IEEE Transactions on Express Briefs: Circuits and Systems II], vol. 43, no. 8, Aug. 1996, pp. 608 – 613.

[112] P.N.Variyam, A.Chatterjee, “Digital-compatible BIST for analog circuits using transient response sampling,” *IEEE Design & Test of Computers*, vol. 17, no. 3, July-Sept. 2000, pp. 106 – 115.

[113] A.C.Nacul, L.Carro, D.Janner, M.A.Lubaszewski, “BIST procedure for analog mixers in software radio,” *14th Symposium on Integrated Circuits and Systems Design*, Sept. 2001, pp. 103 – 108.

[114] J.Velasco-Medina, I.Rayane, M.Nicolaidis, “On-line BIST for testing analog circuits,” *Proc., International Conference on Computer Design (ICCD)*, Oct. 1999, pp. 330 – 332.

[115] S.Khaled, B.Kaminska, B.Courtois, M.Lubaszewski, “Frequency-based BIST for analog circuit testing” *VLSI Test Symposium*, pp. 54 - 59, 1995

[116] C.L.Wey, S.Krishman, “Built-in self-test (BIST) structures for analog circuit fault diagnosis with current test data,” *IEEE Transactions on Instrumentation and Measurement*, vol. 41, no. 4, Aug. 1992, pp. 535 – 539.

[117] M.Negreiros, L.Carro, A.A.Susin, “Ultra low cost analog BIST using spectral analysis,” *Proc., VLSI Test Symposium*, 2003, pp. 77 – 82.

[118] S.Dragic, I.Filanovsky, M.Margala, “Low-voltage analog current detector supporting at-speed BIST,” *International Symposium on Circuits and Systems (ISCAS)*, vol. 1, May 2002, pp. I-593 - I-596.

[119] S.Bhattacharya and A.Chatterjee, “Built-In-Test of Analog and RF Circuits using Embedded Sensors,” *Test Resource Partitioning Workshop*, 2004.

[120] S.Bhattacharya and A.Chatterjee, “Use of Embedded Sensors for Built-In-Test of RF Circuits,” *Intl. Test Conference*, 2004, pp. 801-809.

[121] S.Bhattacharya and A.Chatterjee, “A Built-In Loopback Test Methodology for RF Transceiver Circuits using Embedded Sensor Circuits,” *Proc., Asian Test Symposium*, Nov. 2004, pp. 68-73.

[122] Data sheet from http://semiconductors.agilent.com for HSMS-286x series Schottky diodes

[123] Data sheet from http://www.cel.com for NE68019 and NE68530.

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