Bus Interconnect Structure for a System-On-a-Chip Multiprocessor System

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1.0 Introduction

This report describes two possible implementations for a bus interconnect structure which would be used in a multiprocessor System-On-a-Chip. The bus architecture is called the GGBA (General Global Bus Architecture.) The research findings presented in this report show that from two possible implementations for a system bus for this bus architecture, one of those would be the most advantageous based on factors such as bus latency, crosstalk, and bus area.

2.0 System Floorplan

This section describes the floorplan for a 4 processor System-On-a-Chip. The bus which will be discussed throughout this report connects the 4 processors to a shared memory module. Figure 1 shows the floorplan for this multiprocessor system. The interconnect line (shown as a dark line traveling between the MPC755 elements and the memory represents the bus interconnect structure. The longest path (the path on which the delay in this report will be measured) is between the MPC755 module at the lower left in Figure 1 and the MBI module which connects to the SRAM memory module.

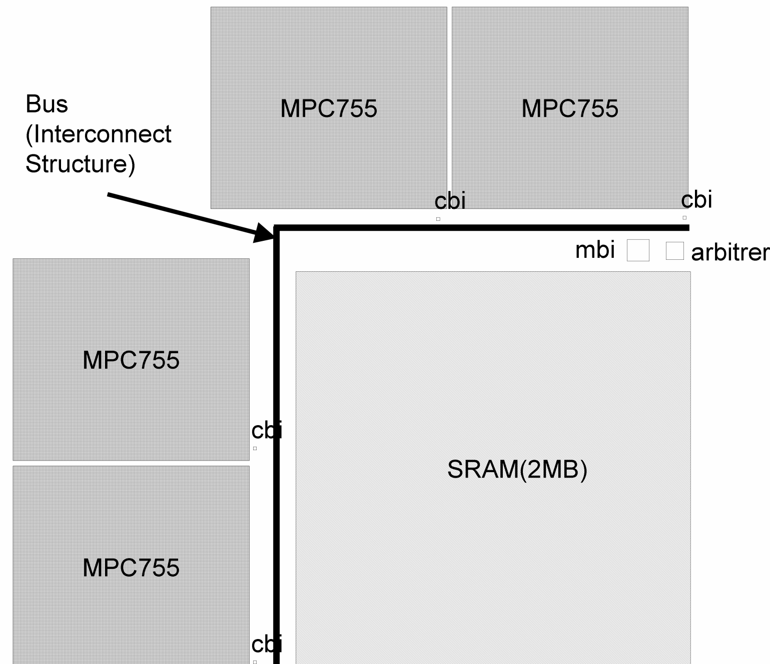

Figure 1. Multiprocessor System with Interconnect Structure. (Area measurements for the MPC755 [3] and SRAM memory [4] available online)

The processing elements connected to the central bus are Motorola Power PC modules (MPC755). In order to communicate on a central bus, arbitration modules are placed between the bus and the different processing elements as well as memory. These arbitration modules control which processor has control over the bus to fetch or write data to and from a shared memory. With a die size of each MPC755 element equal to 0.51cm^2 and that of the main memory equal to 1.66cm^2 the total interconnect length for the system shown in Figure 1 was 2.55 for a version using repeaters and 1.99cm for a

structure without repeaters. Both interconnect structures were designed using TSMC 0.25um technology [1].

3.0 Bus Interconnect Structures

The first interconnect structure for a 64 bit bi-directional bus connects four processors to a shared memory structure. This is considered a basic bus interconnect structure since it does not include elements such as repeaters which might make the bus faster. The technology used to model this bus structure in order to find the delay through the bus was TSMC 0.25um [1]. Capacitance [2][6], resistance [5], and inductance values for the interconnect structure were derived from capacitance per unit length and resistance per unit length values from a MOSIS run for this TSMC 0.25um technology [1]. The interconnect structure for a system bus without repeaters is shown in Figure 2.

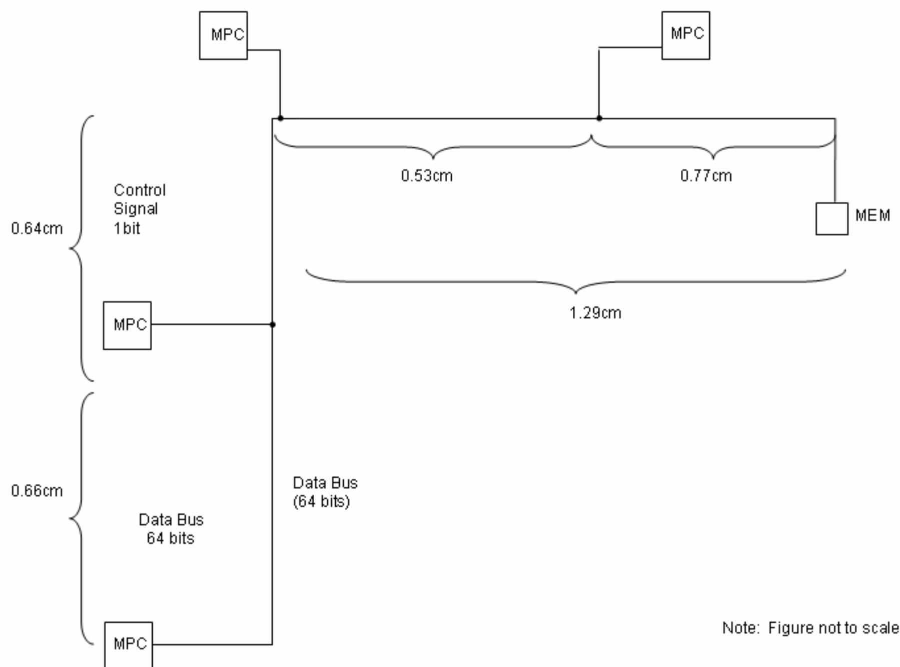

Figure 2. Interconnect for a Bus with No Repeaters.

In this figure, there are four interconnect stages which comprise the entire system bus. This bus interconnect structure was simulated using HSPICE and the delay across the bus interconnect was 4.29ns with an interconnect length of 1.99cm.

The second bus structure considered is shown in Figure 3. This bus structure includes repeaters for the possibility of decreasing the delay on the bus. Repeater insertion on this 64 bit bus required two lines to be included for each bi-directional line. This is due to the one-directional repeaters being inserted along the interconnect.

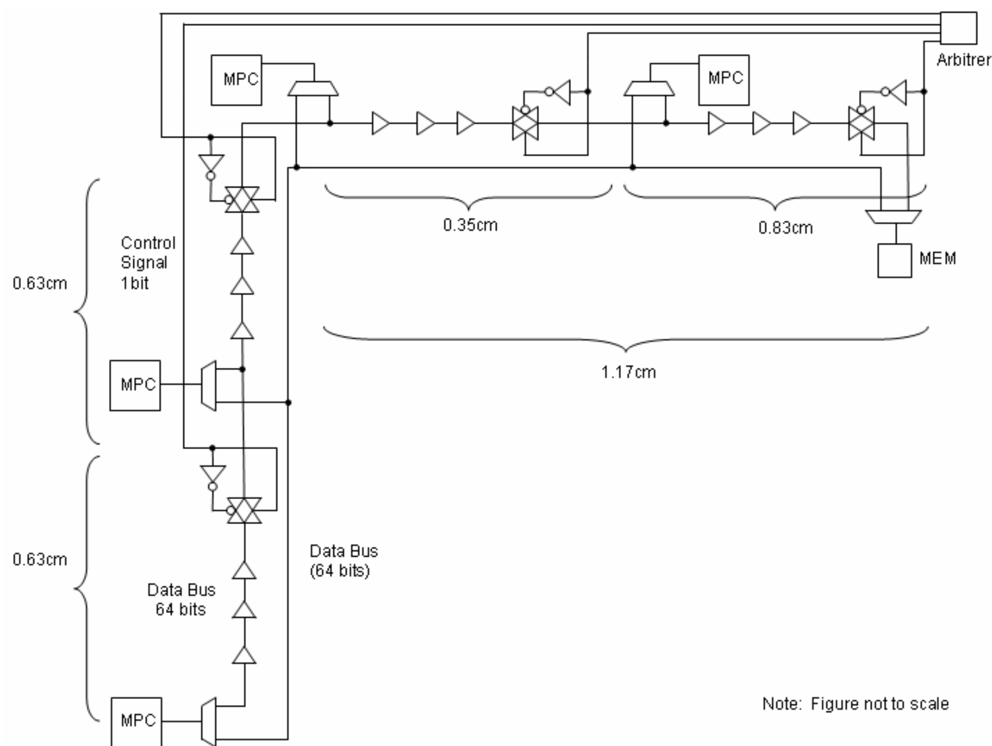

Figure 3. 64 bit bi-directional Interconnect with Repeaters.

In order to remove the possibility of contention on the bus, the bus was segmented into four different segments. Each segment would be turned on or off through specific t-

gates placed before the connection of the bus to each processing element. These t-gates are called control gates, since they control whether or not a section of the bus is connected to the rest of the bus. The control logic for the control gates is embedded into the arbitrer as shown in Figure 3.

After HSPICE simulation with transistor decks from MOSIS and wire capacitance and resistance values from a specific run [1], the resulting delay across the bus for the second implementation was 6.98ns. The total length of the bus interconnect was 2.55cm.

4.0 Crosstalk and Area Comparisons

Crosstalk between a specific line and another neighboring line was analyzed using a published capacitance model [2]. The coupling capacitance was introduced between an interconnect line which was stimulated with a square wave pulse and a line which did not have any stimuli (called the crosstalk line). The resulting wave on the line without stimuli was analyzed for the two interconnect structures presented in Section 3.0. For the first interconnect structure (without repeaters), the waveform observed on the crosstalk line is shown in Figure 4.

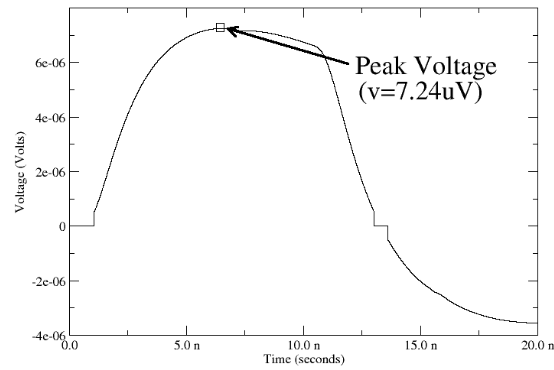

Figure 4. Induced Voltage on Crosstalk Line for an Interconnect Structure without Repeaters.

As can be observed in Figure 4, the peak crosstalk voltage for this line is 7.24uV. Similar simulations were run on the second interconnect structure. The results on the crosstalk line for this implementation is shown in Figure 5. The peak induced voltage for this structure was 3.41uV.

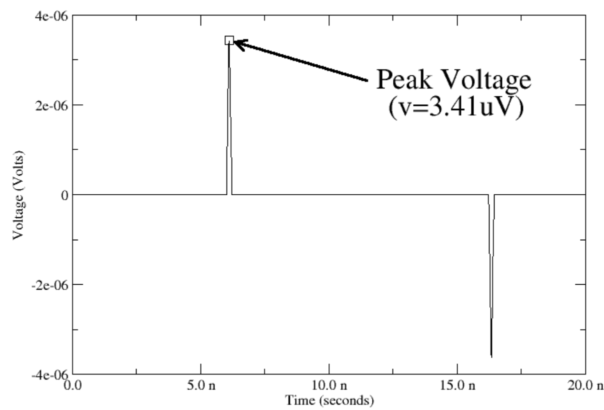

Figure 5. Interconnect Structure With Repeaters, Crosstalk Line.

Comparing the resulting peak voltage on the crosstalk line between the interconnect structure with repeaters and the one without repeaters, it can be observed that the structure with repeaters has a smaller peak voltage. The peak voltage on the line without repeaters, however, is not large enough to cause false switching, since the value of Vdd/2 (1.25V) for this line is not met [1].

The area for the interconnect structure with repeaters would be more than twice as large as the area for the structure without repeaters. This would be due to the presence of two bus lines for the repeater structure since the repeaters are uni-directional and thus there is a need for a forward and return path between the source and destination. The difference in areas is because the repeater version requires two sets of lines, in total 128 bus lines since the repeaters are uni-directional. The interconnect structure with repeaters is more than twice as much as the other structure since it includes the areas for the repeaters and control gates for the four sections of the bus.

Possible Improvements

One possible improvement that could be made in the modeling of the two interconnect structures is to change the placement of the locations where different MPC elements connect to the main bus. The assumption was that the place where this connection is made is close to one of the corners of each MPC module (as shown in Figure 1.) This assumption was made because the layout of the MPC modules was not available. Thus, the worst case connection assumption was made. A better assumption could be to connect the bus in the middle of the MPC modules, since this would reduce to total length of interconnect on the worst path between an MPC element and the memory.

Another improvement which could be made to the modeling presented in this report has to do with a possible discrepancy between expected peak crosstalk voltage values and the simulated peak crosstalk voltage value. The expected peak voltage value for crosstalk on the interconnect structure without repeaters is around 1624.9uV while the actual value based on HSPICE simulation results was 7.24uV. The equation used for the expected peak crosstalk value was (Vpeak=0.5*C_mutual/(C_mutual+C_total)). This discrepancy could be due to capacitance factors which might not have been accounted for in the HSPICE simulation.

Conclusion

The first implementation which was considered was a 64 bit bus with no repeaters, while the second implementation contained repeaters. It was found that although the repeater implementation offered less crosstalk for a 64 bit bi-directional bus interconnect structure, the delay through it was more than the delay through a bus without repeaters. Also, since the repeater implementation would take up more silicon area and would not offer a delay improvement over the bus without repeaters, the bus without repeaters was chosen as the most viable bus interconnect solution for a GGBA bus architecture.

References:

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