## Development of Measurement-based Time-domain Models

## and its application to Wafer Level Packaging

A Thesis Presented to The Academic Faculty

by

Woopoung Kim

In Partial Fulfillment of the Requirements for the Degree Doctor of Philosophy in Electrical Engineering

Georgia Institute of Technology June 2004

# Development of Measurement-based Time-domain Models

and its application to Wafer Level Packaging

Approved by:

Dr. Madhavan Swaminathan, Advisor

Dr. Andrew F. Peterson

Dr. Rao R. Tummala

Dr. C. P. Wong

Dr. J. Stevenson Kenney

Date Approved 06/28/2004

Dedicated to

My loving parents and family

#### ACKNOWELEDGEMENTS

I would like to thank many friends and supporters who have made this happen. First of all, I would like to thank professor Madhavan Swaminathan at Georgia Institute of Technology who advised me. Without his help and guidance, I could not achieve the good work in this dissertation. I also received a lot of help from the Packaging Research Center (PRC) staffs to fabricate the test samples. Thanks. The professor I cannot forget is Prof. Joungho Kim at Korea Advanced Institute of Science and Technology (KAIST) who advised my master degree. Without him, I could not study at Georgia Institute of Technology. As committee members for my master degree at KAIST, I would like to thank professor Jung-Woong Ra and Young-Se Kwon at Korea Advanced Institute of Science and Technology. They kindly wrote the recommendation letters enabling me to study at Georgia Tech. Also, I would like to thank committee members for my Ph.D at Georgia Tech. I should not omit the unconditional help from my parents and family in South Korea. Please God, God bless them! I had also received a lot of help from my labmates at Georgia Tech. Thank you, everyone. I really appreciate your help.

## TABLE OF CONTENTS

Acknowledgements		iv
Table of Contents		v
List of Figures		viii
Summary		xviii
Chapter 1	Introduction	1
1.1	Wafer level Packaging (WLP)	3
1.2	Driving force for wafer level packaging	4
1.3	Integrated board	9
1.4	Driving force for integrated board	9
1.5	Test vehicle	10
1.6	Development of accurate time-domain models	13
1.7	Time-Domain Reflectometry (TDR) measurements	16
1.8	Outline of the dissertation	33
Chapter 2	Calibration and error analysis in TDR/TDT measurements	37
2.1	Block Diagram of TDR equipment	37
2.2	Error in TDR measurements	38
2.3	Short-Open-Load (SOL) calibration for TDR measurements	41
2.4	Error analysis for SOL calibration	43
2.5	Short-Open-Load-Line (SOLL) calibration for TDR	51
2.6	TDR/TDT calibration	54
2.7	TDR characterization examples	56
2.8	Summary	64

Chapter 3	Characterization of package transmission lines	65
3.1	Previous research on transmission line parameter extraction	66
3.2	Transient behavior of transmission lines	67
3.3	Extraction of the frequency-dependent characteristic impedance	69
	and propagation constant using TDR measurements	
3.4	Non-physical transmission line models: Theory and extraction	82
3.5	Time-domain model-to-hardware correlation	85
3.6	Eye-diagram simulation	90
3.7	Effect of frequency-dependent parameters on digital signals	94
3.8	In-situ characterization of transmission lines	96
3.9	Characterization of striplines	108
3.10	Characterization of package transmission lines	109
3.11	Summary	119
Chapter 4	Characterization of silicon transmission lines	120
Chapter 4 4.1	Characterization of silicon transmission lines Prior measurement methods for silicon transmission lines	120 120
4.1	Prior measurement methods for silicon transmission lines	120
4.1 4.2	Prior measurement methods for silicon transmission lines Co-planar lines on high resistivity silicon substrate	120 122
4.1 4.2 4.3	Prior measurement methods for silicon transmission lines Co-planar lines on high resistivity silicon substrate Co-planar lines on low resistivity silicon substrate	120 122 126
4.1 4.2 4.3	Prior measurement methods for silicon transmission lines Co-planar lines on high resistivity silicon substrate Co-planar lines on low resistivity silicon substrate Characterization of transmission lines on low-resistivity	120 122 126
4.1 4.2 4.3 4.4	Prior measurement methods for silicon transmission lines Co-planar lines on high resistivity silicon substrate Co-planar lines on low resistivity silicon substrate Characterization of transmission lines on low-resistivity silicon substrate using non-physical RLGC models	120 122 126 130
4.1 4.2 4.3 4.4 4.5	Prior measurement methods for silicon transmission lines Co-planar lines on high resistivity silicon substrate Co-planar lines on low resistivity silicon substrate Characterization of transmission lines on low-resistivity silicon substrate using non-physical RLGC models Selection and optimization of silicon transmission lines	120 122 126 130 139
4.1 4.2 4.3 4.4 4.5 4.6	Prior measurement methods for silicon transmission lines Co-planar lines on high resistivity silicon substrate Co-planar lines on low resistivity silicon substrate Characterization of transmission lines on low-resistivity silicon substrate using non-physical RLGC models Selection and optimization of silicon transmission lines Thermal, passivation and underfill effect on signal propagation	120 122 126 130 139 143
4.1 4.2 4.3 4.4 4.5 4.6 4.7	Prior measurement methods for silicon transmission lines Co-planar lines on high resistivity silicon substrate Co-planar lines on low resistivity silicon substrate Characterization of transmission lines on low-resistivity silicon substrate using non-physical RLGC models Selection and optimization of silicon transmission lines Thermal, passivation and underfill effect on signal propagation Summary	120 122 126 130 139 143 146
4.1 4.2 4.3 4.4 4.5 4.6 4.7 Chapter 5	<ul> <li>Prior measurement methods for silicon transmission lines</li> <li>Co-planar lines on high resistivity silicon substrate</li> <li>Co-planar lines on low resistivity silicon substrate</li> <li>Characterization of transmission lines on low-resistivity</li> <li>silicon substrate using non-physical RLGC models</li> <li>Selection and optimization of silicon transmission lines</li> <li>Thermal, passivation and underfill effect on signal propagation</li> <li>Summary</li> <li>Characterization of multi-conductor transmission lines</li> </ul>	120 122 126 130 139 143 146 147

5.4	Summary	189
Chapter 6	Wafer-level package on integrated board	190
6.1	Wafer-level package test vehicle	191
6.2	Modeling of solder bumps	192
6.3	Simulation of Test vehicle	199
6.4	Fabrication of Test vehicle	205
6.5	Design procedure for wafer-level package on integrated board	213
6.5	Summary	214
Chapter 7	Conclusion & Future work	215
Appendix A	A. Simulation of (64+1)-conductor transmission lines	219
Appendix B	8. VNA characterization of transmission lines	232
References		234
Publications Generated		243
Award/Patents		246

### LIST OF FIGURES

Figure 1.1	International Technology Roadmap for Semiconductors (ITRS)	2
	for on-chip and off-chip clock frequency	
Figure 1.2	Lead free solder 100um pitch bumps	3
Figure 1.3	Supply voltage, operating frequency, and power trends for Intel	5
	microprocessors	
Figure 1.4	Power integrity simulation using various wafer level interconnect	7
	inductance for 5GHz chip operation [A6].	
Figure 1.5	Integrated boards.	9
Figure 1.6	Wafer level packaging on integrated board.	11
Figure 1.7	Test vehicle for WLP on integrated board	12
Figure 1.8	Frequency spectrum of 5GHz digital clock signals	14
	and their step pulses.	
Figure 1.9	Another representation of a digital signal with a step pulse	14
	and delta functions.	
Figure 1.10	TDR measurement setup	16
Figure 1.11	Previous TDR measurements	18
Figure 1.12	(a) TDR measurement setup and (b) one-port error model.	21
Figure 1.13	(a) Uni-directional TDR/TDT setup and (b) its Error model.	22
Figure 1.14	Bidirectional two-port TDR/TDT measurement setup.	23
Figure 1.15	12-term error model for bidirectional TDR/TDT calibrations.	24
Figure 1.16	8-term error models for bidirectional TDR/TDT calibrations.	24
Figure 1.17	TDR/TDT response with time.	25
Figure 1.18	(1,0) excitation of coupled lines.	27

Figure 1.19	Schematic representation of the NA measurement procedure.	27
Figure 1.20	Extraction procedure of crosstalk parameters in [A55].	28
Figure 1.21	(a) Even and (b) odd- mode TDR measurements.	29
Figure 1.22	Transformation of port impedances.	31
Figure 2.1	Block Diagram of SD24 TDR head and 11801B oscilloscope.	38
Figure 2.2	Measured horizontal random noise of the TDR equipment.	39
Figure 2.3	(a) Measured vertical random noise and (b) its standard	40
	deviation as a function of number of averages.	
Figure 2.4	One-port error model for Short-Open-Load (SOL) calibration.	42
Figure 2.5	Maximum uncertainty on the Smith chart at 50MHz.	47
Figure 2.6	Maximum uncertainty on the Smith chart at 2GHz.	47
Figure 2.7	Maximum uncertainty on the Smith chart at 8GHz.	48
Figure 2.8	Maximum absolute uncertainty for the measured impedances	48
	along the imaginary axis of the Smith chart.	
Figure 2.9	Simulated TDR signals for repeatability analysis.	49
Figure 2.10	Exact frequency response of the DUT.	50
Figure 2.11	Simulated repeatability of TDR calibration.	51
Figure 2.12	Short-Open-Load-Line (SOLL) calibration procedure.	52
Figure 2.13	Simulated repeatability of SOLL calibration.	52
Figure 2.14	Measured repeatability of TDR system used.	53
Figure 2.15	Simulated TDR/TDT signals for a transmission line.	54
Figure 2.16	Extracted S-parameters of the transmission line	55
	in Figure 2.31 using SOLT calibration (DC~10GHz).	
Figure 2.17	Simulated repeatability of uni-directional TDR/TDT calibration	56
	with a drift of $\pm$ 1.5ps for the transmission line in Figure 2.15.	
Figure 2.18	Embedded inductors.	57

Figure 2.19	TDR measurement of the one-loop inductor in Figure 2.18.	57
Figure 2.20	S-parameter (S11) of the inductor (DC~4.3GHz).	58
Figure 2.21	Quality factor of the inductor.	59
Figure 2.22	Uncertainty of the extracted quality factor of the inductor	59
	from TDR measurement.	
Figure 2.23	Capacitors fabricated at PRC.	60
Figure 2.24	TDR measurement of a capacitor.	60
Figure 2.25	(a) Extracted capacitance and (b) quality factor of the capacitor.	61
Figure 2.26	Uncertainty of the extracted quality factor of the capacitor	62
	from TDR measurements.	
Figure 2.27	Lowpass filter circuits.	62
Figure 2.28	TDR measurement of the lowpass filters.	63
Figure 2.29	S-parameters (S11) of the lowpass filter (DC~10GHz)	63
Figure 3.1	Reflection diagram of lossy transmission line.	68
Figure 3.2	TDR measurements of lossy transmission lines.	69
Figure 3.3	Coplanar lines on organic Substrate.	70
Figure 3.4	Extracted frequency-dependent characteristic impedance	71
	of the coplanar line.	
Figure 3.5	Pad modeling. (a) physical structure (b) physical pad model.	72
Figure 3.6	Pad transition on Smith Chart.	73
Figure 3.7	Structure at the near end of Figure 3.1.	75
Figure 3.8	Error bound of the extracted characteristic impedance.	77
Figure 3.9	TDR measurements for extracting propagation constant.	78
Figure 3.10	Extracted propagation constant of the coplanar line.	79
Figure 3.11	Error/uncertainty bound of extracted propagation constant.	81
Figure 3.12	RLGC models for transmission lines.	83

Figure 3.13	Characteristic impedance of the coplanar line extracted	88
	from NA measurements.	
Figure 3.14	Propagation constant of the coplanar line extracted	89
	from VNA measurements.	
Figure 3.15	Measurements and simulations for the coplanar line.	90
Figure 3.16	Circuit for eye-diagram simulation.	91
Figure 3.17	Eye-diagram simulations with a periodic square wave.	92
Figure 3.18	Eye-diagram simulation with a random binary source.	93
Figure 3.19	TDR response for various frequency-dependent Z0.	95
Figure 3.20	TDR response with various frequency-dependent	96
	propagation constant.	
Figure 3.21	Step pulse response to exp(-a·f) and exp(-b· $\sqrt{f}$ ).	98
Figure 3.22	Step pulse response to exp(-b $\sqrt{f}$ ) and its approximation.	99
Figure 3.23	TDR measurement of a lossy transmission line.	101
Figure 3.24	Extraction of the frequency-dependent characteristic	102
	impedance from the first reflection in Figure 3.1.	
Figure 3.25	Finding the effective dielectric constant.	103
Figure 3.26	Optimized waveform using simulation for lossless	104
	transmission line.	
Figure 3.27	Finding $b \cdot i$ in the attenuation constant.	105
Figure 3.28	Finding <i>a f</i> in the attenuation constant.	106
Figure 3.29	Comparison between simulation and measurement	107
	for open termination.	
Figure 3.30	(a) Side view and (b) top view of the fabricated stripline.	108
Figure 3.31	TDR measurement and simulation for the stripline.	110

(a) Cross-section and (b) top view of fabricated coplanar lines.	111
TDR measurements and simulations for a FR4 line.	112
TDR measurements and simulations for a APPE line.	113
TDR measurements and simulations for a Ciba line.	114
TDR measurements and simulations for a Vialux line	115
TDR measurements and simulations for a Hitachi line.	116
TDR measurements and simulations for a Nelco line.	117
Comparison of propagation constant for board	118
transmission lines characterized.	
Silicon resistivity vs. frequency relationship [D6].	121
Cross-section of the fabricated co-planar lines on	123
silicon substrate with resistivity of 2000 $\Omega$ -cm.	
TDR measurement of the coplanar line on 2000 $\Omega\mbox{-}cm$	124
Resistivity silicon substrate.	
Time-domain correlation between simulation and measurement	125
for the coplanar line on 2000 $\Omega\mbox{-}cm$ resistivity silicon substrate.	
Frequency-domain correlation between simulation and	126
measurement for the coplanar line on 2000 $\Omega\mbox{-}cm$ resistivity silicon.	
Cross-section of the fabricated coplanar lines on silicon substrate	127
with 100 $\Omega$ -cm resistivity.	
TDR measurement of the coplanar line on 100 $\Omega$ -cm resistivity	128
silicon substrate.	
Loss induced by silicon substrate.	129
(a) 2000 $\Omega\text{-cm}$ resistivity and (b) 100 $\Omega\text{-cm}$ resistivity silicon.	
Transmission lines represented using Z0 and $\gamma$ .	130
	TDR measurements and simulations for a FR4 line.TDR measurements and simulations for a APPE line.TDR measurements and simulations for a Ciba line.TDR measurements and simulations for a Vialux lineTDR measurements and simulations for a Hitachi line.TDR measurements and simulations for a Nelco line.Comparison of propagation constant for boardtransmission lines characterized.Silicon resistivity vs. frequency relationship [D6].Cross-section of the fabricated co-planar lines onsilicon substrate with resistivity of 2000 Ω-cm.TDR measurement of the coplanar line on 2000 Ω-cmResistivity silicon substrate.Time-domain correlation between simulation and measurementfor the coplanar line on 2000 Ω-cm resistivity silicon substrate.Frequency-domain correlation between simulation andmeasurement for the coplanar line on 2000 Ω-cm resistivity silicon.Cross-section of the fabricated coplanar lines on silicon substrate.Frequency-domain correlation between simulation and measurementfor the coplanar line on 2000 Ω-cm resistivity silicon.Cross-section of the fabricated coplanar lines on silicon substratewith 100 Ω-cm resistivity.TDR measurement of the coplanar line on 100 Ω-cm resistivity siliconsilicon substrate.Loss induced by silicon substrate.Loss induced by silicon substrate.(a) 2000 Ω-cm resistivity and (b) 100 Ω-cm resistivity silicon.

Figure 4.10	Smith-chart behavior of S11 for board transmission lines.	132
Figure 4.11	VNA measurement of the coplanar line on 100 $\Omega\text{-cm}$	133
	Resistivity silicon substrate.	
Figure 4.12	Non-physical RLGC models for silicon substrate with	134
	slow-wave propagation effect.	
Figure 4.13	S-parameters of the coplanar line on 100 $\Omega\text{-cm}$ resistivity	137
	Silicon substrate with and without slow-wave propagation effect.	
Figure 4.14	Frequency-domain correlation between simulation and	138
	measurement for the coplanar line on 100 $\Omega\text{-cm}$ resistivity silicon.	
Figure 4.15	Time-domain correlation between simulation and measurement	139
	for the coplanar line on 100 $\Omega\text{-cm}$ resistivity silicon substrate.	
Figure 4.16	Fabricated silicon transmission lines.	141
Figure 4.17	TDR measurements for the co-planar line on four silicon wafers.	142
Figure 4.18	Network Analzyer measurements for the co-planar lines.	143
Figure 4.19	Effect of thermal cycling on S21 of silicon transmission lines.	144
Figure 4.20	Effect of polyimide and thermal cycling on S21 of silicon lines.	144
Figure 4.21	Electrical characteristics of an underfill used.	145
Figure 4.22	Effect of underfill on S21 of the silicon lines.	145
Figure 5.1	Dimensions of fabricated microstrip coupled line	148
	and measurement setup.	
Figure 5.2	TDR measurement of the even and odd mode waveforms	149
	for the coupled line	
Figure 5.3	(a) Lossless non-physical RLGC model and (b) lossy non-physical	151
	RLGC model for single transmission line.	
Figure 5.4	RLGC model for symmetric lossless coupled lines.	152

Figure 5.5	(a) Even-mode equivalent circuit and (b) odd-mode equivalent	153
	circuit for symmetric lossless coupled lines.	
Figure 5.6	General RLGC model of symmetric lossy coupled lines.	154
Figure 5.7	Comparison between simulation and TDR measurement	157
	for (a) even- mode and (b) odd-mode.	
Figure 5.8	Single-line excitation of microstrip coupled lines.	158
Figure 5.9	Comparison between simulations and TDR measurements	159
	for coupled line with single excitation. (a) ch1 and (b) ch2.	
Figure 5.10	Fabricated co-planar coupled lines.	159
Figure 5.11	Comparison between simulations and TDR measurements	161
	for (a) the even- mode and (b) odd-mode of the coupled line.	
Figure 5.12	Comparison between simulations and TDR measurements	162
	of single-line excitation for the coupled line.	
Figure 5.13	Non-physical RLGC models for symmetric lossy coupled lines	163
	on high-loss silicon substrates. $G_d$ is the substrate loss.	
Figure 5.14	General RLGC model for asymmetric lossy coupled lines.	164
Figure 5.15	Fabricated differential lines and measurement setup.	166
Figure 5.16	Comparison between the coupled line in Figure 5.1 and	167
	differential line in Figure 5.15 for the (a) even-mode and (b) odd-mod	de.
Figure 5.17	Symmetric (3+1)-conductor transmission lines.	169
Figure 5.18	Modes of (3+1)-conductor transmission lines.	170
Figure 5.19	Characteristic impedance and propagation constant	171
	of (3+1)-conductor transmission lines	
Figure 5.20	RLGC model of lossless (3+1)-conductor transmission lines.	172
Figure 5.21	Equivalent circuits of lossless (3+1)-conductor transmission lines.	172
Figure 5.22	Characteristic impedances and phase velocities	173

of lossless (3+1)-conductor transmission lines.

Figure 5.23	General RLGC model of (3+1)-conductor transmission lines.	173
Figure 5.24	Non-physical RLGC model for (3+1)-conductor silicon lines	177
	on high-loss silicon substrates. $G_d$ represents the substrate loss.	
Figure 5.25	Cross-section of the simulated (3+1)-conductor transmission line.	179
Figure 5.26	Simulated circuit for the (3+1)-conductor transmission line.	180
Figure 5.27	Simulated waveforms for the (3+1)-conductor transmission line.	181
Figure 5.28	Cross-section of simulated (64+1)-conductor transmission lines.	182
Figure 5.29	(64+1)-conductor transmission line with 3pF load capacitors.	183
Figure 5.30	Simulation results of the (64+1)-conductor transmission line	184
	with 3pF load capacitors in Figure 5.29.	
Figure 5.31	Simulated waveforms of the (3+1)-conductor transmission line	187
	by neglecting mutual inductance and capacitance except for adjacer	nt
	conductors.	
Figure 5.32	Impedance controllability (signal integrity) chart.	188
Figure 6.1	Test vehicle for wafer-level package on integrated board.	191
Figure 6.2	Solder bump models for (a) two parallel solder bumps	193
	and (b) ground-signal solder bumps.	
Figure 6.3	Solder bump model for the wafer-level package test vehicle.	193
Figure 6.4	Simplification of solder bumps to cylinders.	195
Figure 6.5	Analytical model for the solder bumps with 50um diameter	196
	and 100um pitch in the wafer-level package test vehicle.	
Figure 6.6	Measurement test vehicle for the characterization	197
	of solder bumps with 100um diameter and 200um pitch.	
Figure 6.7	Imaginary part of the measured input impedance	197
	of the solder bumps with 100um diameter and 200um pitch.	

Figure 6.8	Solder bumps inductance extracted from HFSS.	198
Figure 6.9	Equivalent model for FR4 and $100\Omega$ -cm resistivity silicon	200
	test vehicle.	
Figure 6.10	Simulated eye-diagram for FR4 and 100 $\Omega$ -cm resistivity	201
	silicon test vehicle.	
Figure 6.11	Equivalent model for the APPE and 2000 $\Omega$ -cm resistivity	201
	silicon test vehicle.	
Figure 6.12	Simulated eye-diagram for APPE and 2000 $\Omega$ -cm resistivity	203
	silicon test vehicle.	
Figure 6.13	(a) Solder bumps with 35um diameter and 100um pitch	204
	and (b) their analytical model.	
Figure 6.14	Simulated model for the APPE and 2000 $\Omega$ -cm resistivity	204
	silicon test vehicle containing solder bumps.	
Figure 6.15	Simulated eye-diagram of APPE and 2000 $\Omega$ -cm silicon	205
	test vehicle containing solder bumps.	
Figure 6.16	Assembled wafer level package test vehicle.	206
Figure 6.17	TDR measurements of the APPE line, Si-on-APPE line	207
	and Si line for the assembled test vehicle in Figure 6.16.	
Figure 6.18	Extracted model of the assembled test vehicle.	208
Figure 6.19	Model-to-hardware correlation for the assembled test vehicle.	209
Figure 6.20	Simulated eye-diagrams for the assembled wafer-level package	210
	test vehicle in Figure 6.16 at (a) 3Gbps and (b) 5Gbps data rates.	
Figure 6.21	Eye-diagram at 5Gbps data rate for the test vehicle	211
	with proper assembly process.	
Figure 6.22	Equivalent circuit for the re-designed test vehicle.	212

Figure 6.23	Simulated eye-diagram at 5Gbps data rate for the re-designed	212
	test vehicle.	
Figure 7.1	Microstrip-type wafer-level package test vehicle.	218
Figure 7.2	Wafer-level package test vehicle including integrated circuits.	218

Figure B.1Two transmission-line measurements for the characterization232of transmission lines using Network Analyzers.

#### SUMMARY

In today's semiconductor-based computer and communication technology, system performance is determined primarily by two factors, namely on-chip and off-chip operating frequency. In this dissertation, time-domain measurement-based methods that enable gigabit data transmission in both the IC and package have been proposed using Time-Domain Reflectometry (TDR) equipment. For the evaluation of the time-domain measurement-based method, a wafer level package test vehicle was designed, fabricated and characterized using the proposed measurement-based methods. Electrical issues associated with gigabit data transmission using the wafer-level package test vehicle were investigated. The test vehicle consisted of two board transmission lines, one silicon transmission line, and solder bumps with 50um diameter and 100um pitch. In this dissertation, 1) the frequency-dependent characteristic impedance and propagation constant of the transmission lines were extracted from TDR measurements. Non-physical RLGC models for transmission lines were developed from the transient behavior for the simulation of the extracted characteristic impedance and propagation constant. 3) the solder bumps with 50um diameter and 100um pitch were analytically modeled. Then, the effect of the assembled wafer-level package, silicon substrate and board material, and material interfaces on gigabit data transmission were discussed using the wafer-level package test vehicle. Finally, design recommendations for the wafer-level package on integrated board were proposed for gigabit data transmission in both the IC and package.

# **Chapter 1**

## Introduction

In today's semiconductor-based computer and communication technology, system performance is determined primarily by two factors, namely the on-chip and off-chip operating frequencies. The on-chip frequency is the signal frequency inside the silicon integrated circuit (IC), while the off-chip frequency is the signal frequency outside the silicon IC such as on the mother board or in the package. In current personal computers, high-performance CPUs have an on-chip clock frequency of 3.40 GHz and an off-chip clock frequency of 1GHz. Examples of such microprocessors are the Intel Pentium IV and the Apple G5.

According to the International Technology Roadmap for Semiconductors (ITRS) 2001 [A1], the on-chip and off-chip clock frequencies are expected to converge and reach 5GHz in high-performance computers in 2005, as shown in Figure 1.1. Figure 1.1 shows the three ITRS projections based on the years 1997, 1999 and 2001 for on-chip and off-chip clock frequencies. In ITRS 1997 and 1999, the off-chip interconnections were expected to operate at a speed slower than the on-chip interconnections. However, in ITRS 2001, there is a convergence in the two frequencies. This can be attributed to the global inteconnect problem faced by interconnections due to the excessive resistance and capacitance of the interconnections on silicon. Hence, a major goal of this dissertation is the demonstration of methods that enable gigabit data transmission in both the IC and package. This has been achieved through wafer level packaging and

new integrated board technologies, as described in this dissertation. Wafer-level packaging on an integrated board is expected to be one of the future technologies that maximize IC performance with minimum system size. In this dissertation, the electrical issues arising in the design of wafer level packaging, board and silicon transmission lines are discussed through a combination of design, modeling and measurements.

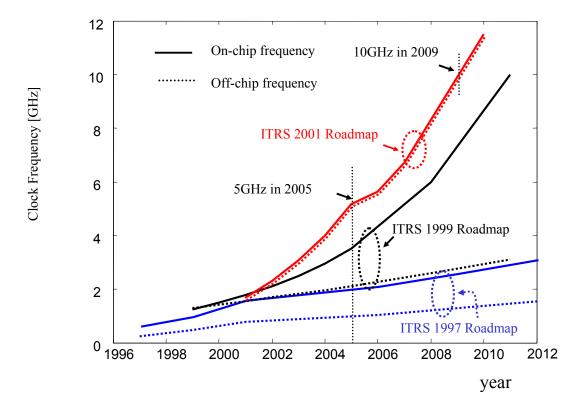


Figure 1.1 International Technology Roadmap for Semiconductors (ITRS) for on-chip and off-chip clock frequency

#### 1.1. Wafer level Packaging (WLP)

Wafer-level packaging can be defined as IC packaging formed at the wafer level in the wafer foundry [A2]. This is different from Chip-scale packaging (CSP) and Flip-chip where IC assembly onto the package is individually performed after dicing the wafer. CSPs are defined as packages with size up to 20% larger than the IC. Although the inductance of chip-scale packaging can be as small as that of wafer-level packaging, the price per I/O of chip-scale packaging is two times higher than wafer-level packaging [A2]. Figure 1.2 is an example of wafer level packaging fabricated at the Package Research Center (PRC).

Today, Amkor Technology's Ultra-CSP wafer process is a commercial wafer level packaging technology that has a minimum pitch of 500 um and diameter of 300 um for solder bumps with an inductance of ~80pH. National Semiconductor's microSMD has screen-printed solder balls with 170um diameter and 500um pitch with an inductance of ~50pH. Kulicke & Soffa Flip Chip technology can provide solder bumps with 120um diameter and 200um pitch. SuperCSP from Fujitsu has solder balls with 230 um diamater and 500 um pitch. Shellcase's ShellBGA has a minimum pitch of 250um. Unitive provides wafer level packaging solutions with a pitch of 150 um and a diameter of 75 um.

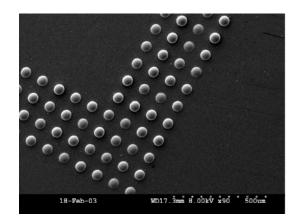


Figure 1.2 Lead free solder 100um pitch bumps

#### 1.2. Driving force for wafer level packaging

The driving force for wafer level packaging on an integrated board is microminiaturization and high performance through adequate management of signal and power integrity.

#### 1.2.1. Power Integrity

Managing power requires the purity of supply voltages to on-chip circuits from off-chip power supplies. In Intel's Pentium 4, the voltage tolerance on the IC is designed to be less than  $\pm$  5% of power supply voltage [A3]. Of the  $\pm$  5% voltage variation of the switching tolerance budget,  $\pm$  1.5% is reserved for settling the accuracy variation of the switching voltage regulator module. Therefore,  $\pm$  3.5% voltage variation is allocated for the design of the power delivery network from the power supply to the on-chip circuits. Since simultaneous switching noise (SSN) or delta-*I* noise induces noise on the voltage and ground rails of the on-chip circuits,  $\pm$  3.5% voltage tolerance limits the maximum impedance allowed in the power delivery network. Based on ITRS 2001 roadmap, the operating voltage and power for high-performance microprocessors is predicted to be 0.9V and 170W in 2005, and 0.6V and 218W in 2010, respectively. This limits the overall inductance of the power delivery network, which is difficult to satisfy using standard assembly technologies.

The current Intel Pentium 3 and 4 microprocessors have Organic Land Grid Arrary (OLGA) or Flip Chip Pin Grid Array (FCPGA) packages with a pin inductance of 1~2nH [A4]. Intel 486 and 386 microprocessors had Ceramic Pin Grid Array (CPGA) packages, and the Intel Pentium had Plastic Pin Grid Array (PPGA) packages with a pin inductance of ~10 nH [A5].

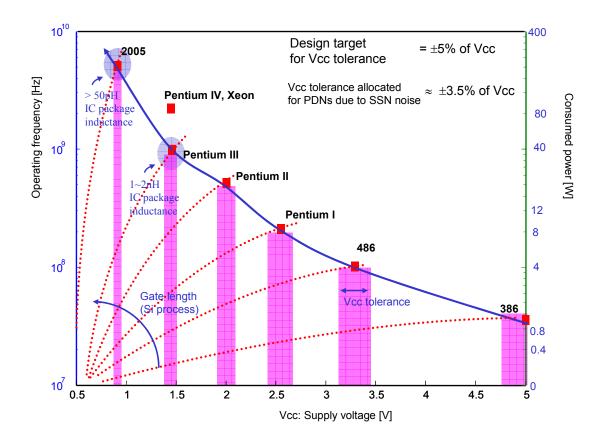


Figure 1.3 Supply voltage, operating frequency, and power trends for Intel microprocessors

As shown in Figure 1.3, as the performance of microprocessors increases, the supply voltage has been decreased. In addition, the voltage tolerance of the supply voltage has decreased. The smaller voltage tolerance and higher operating frequency have necessitated smaller inductance for microprocessor packages, which has motivated the transition of Intel microprocessor packages from CPGA in Intel 386 micro-processors to OLGA or FCPGA in Pentium 4 microprocessors.

In 2005, high-performance Integrated Circuits are expected to consume 170W of power at 0.9V, translating to a transient current of 189A. This translates to the pin inductance being smaller than 50pH based on simulations in [A6]. In [A6], the effect of wafer level packaging on power integrity was simulated using the Finite-Difference Time

Domain (FDTD) method for various interconnect (bump) inductances. The structure of the packaged microprocessor is shown in Figure 1.4. It consisted of an IC in wafer form assembled on a board with power and ground planes. Both the IC and board support decoupling capacitors. The IC was powered from one edge of the board. The transition between the IC and the board consisted of a number of rigid or compliant interconnects whose inductance can gate the performance of the microprocessor. Based on the simulations, the maximum inductance estimated for the interconnects was about 50pH assuming a noise tolerance on the power supply of 55mV, as shown in Figure 1.4. The simulation assumed that the number of stacked layers in silicon was 4, the size of the chip was 20.1mm by 27mm, the number of compliant interconnects was 400nF. The clock frequency assumed was 5GHz with the rise and fall time of the input signal 20ps, and period of 200ps.

Standard assembly technologies have large inductances. For example, wire-bonding and TAB have 1-6nH inductance per interconnection, while Ball Grid Arrays (BGA) can have ~0.5nH inductance [A2]. Dual in Line Packages (DIP) have an inductance from 3nH to 20nH per lead, Quad Flat Packages (QFP) have a lead inductance from 6nH to 8nH, Plastic Leader Chip Carriers (PLCC) have a lead inductance from 3nH to 7nH, Ceramic BGAs (CBGA) have a lead inductance from 0.5nH to 4nH , and Plastic BGAs (PBGA) have a lead inductance from 0.2nH to 5nH [A7]. Wafer-level packaging using solder balls of 300um diameter has an inductance of 80pH per solder ball. Similarly, 100um diameter solder balls have a 40pH inductance per solder ball and 50um diameter solder balls have a 20pH inductance per solder ball [A8]. The last two technologies satisfy the required inductance for the year 2005.

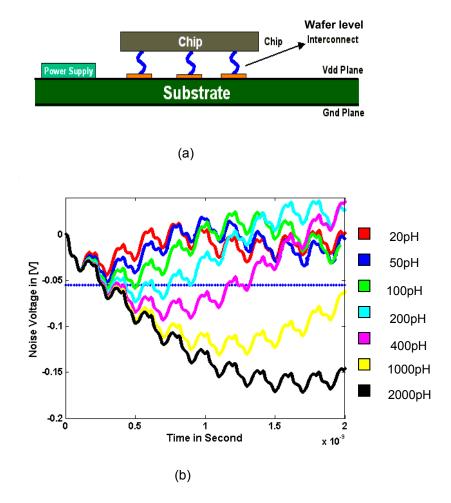


Figure 1.4 Power integrity simulation using various wafer level interconnect inductances for 5GHz chip operation [A6]. (a) Simulated wafer level packaging structure and
(b) Differential noise induced on the power supply with 40% of the circuits switching.

#### 1.2.2. Signal Integrity

Managing high speed signals requires seamless transitions through various interfaces in the system. Based on the ITRS 2001 roadmap, the on-chip and off-chip frequency is expected to be 5,173MHz in 2005, which translates to a signal bandwidth of 41.38GB/s for a 64-bit wide bus. The signals are expected to travel in both the IC and the package. Therefore, a seamless transition between the off-chip and on-chip circuits is critical for signal propagation.

In the previous section, power integrity in the IC package has been discussed in terms of inductance. Integrated circuits with higher operating frequencies and lower supply voltages require smaller inductance IC packages, which is the main reason for the need for wafer level packaging. In addition to the inductance, IC packages also contain parasitic capacitance. Since the parasitic capacitance helps the power integrity of IC packages, it is typically not included in the power integrity analysis. However, the parasitic capacitance degrades the signal integrity of IC packages. The parasitic capacitance of the IC package is more important for signal integrity than the inductance. Therefore, a smaller parasitic capacitance is important for power integrity.

Discontinuities in signal paths such as right angle bends induce parasitic capacitances [A9][A10][A11]. Hence, high-speed interconnections should be designed to have smaller number of discontinuities such as right angle bends and vias. Wafer level packaging has smaller parasitic capacitance than any other IC packages, which is another reason for the need for wafer level packaging. However, although wafer level packaging has small parasitic capacitance, the effect of small parasitic capacitance on propagating signals becomes larger as the operating frequency of ICs increases. The effect of parasitic capacitance in wafer level packaging on signal propagation is investigated in Chapter 6.

#### **1.3. Integrated Boards**

As integrated circuits contain a number of transistor circuits on a small wafer, integrated boards help reduce the size of systems through multi-layered high density interconnects and embedded passives. As shown in Figure 1.5, various functional blocks such as MEMS, digital circuits, analog circuits and RF circuits can be assembled onto an integrated board with embedded passives. Therefore, the integrated board can achieve micro-miniaturization and high-speed. The integration of both the IC and the board leads to the concept of a System on a Package (SOP).

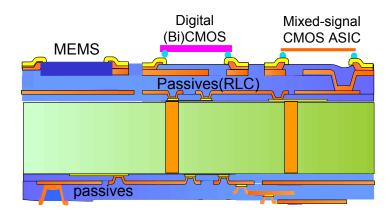


Figure 1.5 Integrated boards.

#### **1.4. Driving force for Integrated Boards**

There are two driving forces for integrated boards: namely, system miniaturization and high performance.

#### 1.4.1. Power Integrity

Power distribution networks designed with a thin film dielectric layer in integrated boards have better capability of managing power supply noise. Thin dielectrics suppress power-ground plane resonances, and high dielectric constant dielectrics shift the resonance pattern of power-ground plane pairs to lower frequencies, which also helps high-frequency bypassing [A12]. In [A13], SOP demonstrated improved performance over standard PWB technology, effectively suppressing simultaneous switching noise (SSN).

The parasitic inductance and resistance of power-ground decoupling capacitance also contribute to achieving better power integrity in integrated boards. Embedded decoupling capacitors have smaller parasitic inductance, increasing the effectiveness of the capacitance [A14]. In addition, embedded decoupling capacitors occupy a smaller area.

#### 1.4.2. Signal Integrity

Integrated boards can reduce a large system to a small board through high density. Therefore, the signal attenuation of interconnections in integrated boards becomes much smaller due to the reduced length of interconnections. The reduced signal attenuation leads to better signal integrity. In addition, embedded passives inside integrated boards contribute smaller discontinuities and parasitics than surface-mount discrete passives, improving signal integrity in integrated boards.

#### 1.5. Test vehicle

In the above discussion, better signal integrity and power integrity in high-speed packages requires less parasitic inductance and capacitance, which translates into the need for both wafer level packaging and integrated board technology. The wafer level packaging on an integrated board can be described as shown in Figure 1.6, with ICs on an integrated board assembled through wafer-level packaging (WLP). The integrated board can support gigahertz signals and have high-density interconnections.

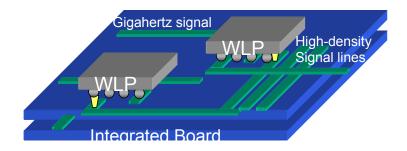


Figure 1.6 Wafer level packaging on integrated board.

For enabling gigabit data communication in WLP on an integrated board as shown in Figure 1.6, the effect of the following considerations on gigabit data signals have been investigated in this dissertation:

- Use of high-resistivity silicon wafer or SOI (silicon-on-insulator) wafer for reducing the signal propagation loss inside the integrated circuits.
- Use of low inductance solder bumps with 50um diameter and 100um pitch for satisfying the power integrity of the year 2005.
- Use of low-loss board materials for reducing the signal propagation loss over integrated boards.
- Implementation of seamless transitions between on-chip and off-chip circuits through low parasitic solder bumps for maintaining signal integrity.

The above strategy for gigabit data transmission has been investigated through the test vehicle in Figure 1.7. The test vehicle consisted of two Printing Wiring Board (PWB) transmission lines, a silicon transmission line, and solder balls with 50um diameter and 100um pitch.

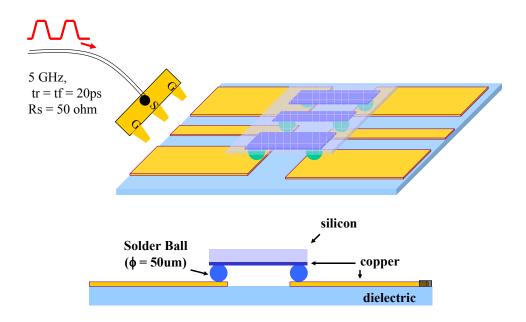


Figure 1.7 Test vehicle for WLP on integrated board

For the silicon transmission line in the test vehicle, a low-resistivity wafer with a resistivity of 100  $\Omega$ -cm and a high-resistivity wafer with a resistivity of 2000  $\Omega$ -cm have been compared. For the board transmission lines, various board materials have been investigated such as Ciba, Vialux, FR4, Hitachi MCL-LX67, N4000-13 and APPE. For assembling the WLP, solder bumps with 50um diameter and 100um pitch have been fabricated and modeled. Then, the possibilities for gigabit data transmission were evaluated using the test vehicle. Through the comparison between low- and high-resistivity silicon wafer, the rationale for choosing high-resistivity silicon wafers has been analytically modeled, resulting in an inductance of 26.8pH and capacitance of 0.32pF. The effect of the inductance and capacitance on gigabit data transmission has been quantified. The effect of board transmission lines on gigabit data transmission has been investigated through the characterization of various board transmission lines.

#### 1.6. Development of accurate time-domain models

While frequency-domain response is important in RF and Wireless systems, timedomain response is important in digital systems. Hence, accurate time-domain models are important for simulating high-speed digital systems. In this dissertation, time-domain models were extracted from Time Domain Reflectometry (TDR) measurements. In this section, the reason why TDR was used for characterizing digital systems is discussed using the frequency spectrum of digital signals. In Section 3.5, three kinds of transmission-line models are compared for correlation with time-domain measurements namely, 1) non-physical RLGC models extracted from TDR measurements, 2) RLGC models extracted from Vector Network Analyzer (VNA) measurements, and 3) physical RLGC models extracted using a 2D parameter extractor. The TDR based models showed better correlation with time-domain measurements than the models based on the VNA and the 2D parameter extractor which are being mainly used for frequencydomain applications.

#### 1.6.1. Frequency spectrum of digital signals

Since digital signals are trapezoidal pulses, the frequency spectrum of the signals is much wider in bandwidth than the corresponding sinusoidal signals. The frequency bandwidth of a digital signal is from DC to around  $1/(\pi^*Tr)$  which is around the third harmonic of the digital signal, where Tr is the risetime of the signal. For example, the clock signal with T = 200ps and Tr =20 ps has a bandwidth from DC to ~16GHz, where T is the clock period. In Figure 1.8, the frequency spectrum of a 5GHz digital signal with Tr=20ps is shown together with the frequency spectrum of its step pulse with Tr=20ps. The step pulse is shown in Figure 1.9. As shown in Figure 1.8, the digital signal has large intensity at low frequencies as well as at 5GHz and 15GHz. The step pulse of the digital signal has the low frequency spectrum shown in Figure 1.8. Therefore, for the

consideration of the low frequency spectrum, the step pulse can be used. Then, excluding the step pulse from the digital signal in Figure 1.8, delta functions are left based on the representation in Figure 1.9, which correspond to the 5GHz and 15GHz frequency components in Figure 1.8.

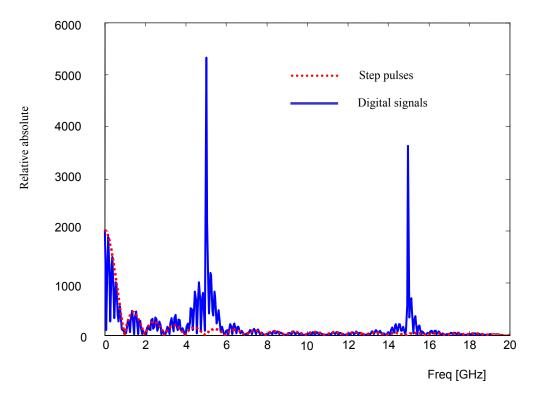


Figure 1.8 Frequency spectrum of 5GHz digital clock signals and their step pulses.

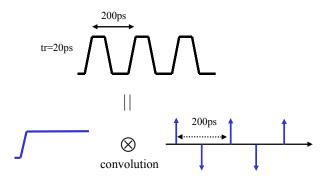


Figure 1.9 Another representation of a digital signal with a step pulse and delta functions.

#### 1.6.2. Measurement for digital systems

Next, consider that the digital signal is applied to a linear time-invariant system. Then, the output of the system is the convolution of the input digital signal and the impulse response of the system. Let x(t) be the input signal and let h(t) be the impulse response of the system. Based on Figure 1.9, the digital signal can be represented as the convolution between its step pulse and delta functions. Let p(t) be the step pulse and d(t) be the delta functions. Then, the output of the system y(t) can be represented as  $x(t) \otimes h(t)$  where  $\otimes$  is the convolution operator. Since  $x(t) = p(t) \otimes d(t)$  according to Figure 1.9,

$$\mathbf{y}(t) = \mathbf{x}(t) \otimes \mathbf{h}(t) = [\mathbf{p}(t) \otimes \mathbf{d}(t)] \otimes \mathbf{h}(t) = [\mathbf{p}(t) \otimes \mathbf{h}(t)] \otimes \mathbf{d}(t) \tag{1.1}$$

Since the delta functions d(t) introduce a series of delays with a period of 5GHz,  $p(t) \otimes h(t)$  is the fundamental response of the digital system. Then, the digital response of the system can be translated into the step pulse response of the system. The above discussion shows the importance of the step pulse response in digital systems.

Therefore, the frequency spectrum of digital systems can be thought of as the frequency spectrum of the step pulse, which has higher intensity at lower frequencies, as shown in Figure 1.8. This shows that the low frequency response including DC is very important in characterizing and simulating digital systems. The lowest frequency that most Network Analyzers can measure is 50Mhz. However, Time-Domain Reflectometry (TDR) can extract the frequency information from DC to  $1/(\pi \cdot Tr)$ , where Tr is the risetime of the step pulse of TDR. In this dissertation, along with VNA measurements, TDR measurements are used to develop accurate models.

#### 1.7. Time-Domain Reflectometry (TDR) measurements

In this dissertation, TDR is used to extract the frequency-dependent parameters of transmission lines both in silicon and on the board as well as passive components such as capacitors and inductors.

#### 1.7.1. TDR measurement setup

TDR represents the reflected time signature of an incident step waveform, as shown in Figure 1.10. TDR measurements display the reflection characteristics and round trip delay of the Device Under Test (DUT). The size of the discontinuity that can be measured is a function of the risetime of the step pulse.

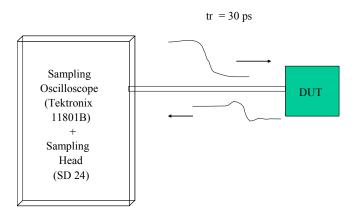


Figure 1.10 TDR measurement setup

Commercial TDR equipment such as that from Tektronix supports a risetime of 30ps with a pulse of amplitude 250mV. Though seldom used, TDR can be used to measure the frequency characteristics of a DUT by converting the time domain waveform to the frequency domain. Unlike the Vector Network Analyzer (VNA), TDR measures both the steady-state and transient response of the DUT. This capability of the TDR is exploited in this dissertation.

#### 1.7.2. Problems with TDR measurements

TDR measurements suffer from the difficulty in accurately extracting the frequency information of DUTs from transient waveforms (unlike VNA) since they do not have automated calibration algorithms. In this dissertation, a method has been proposed for the extraction of the frequency-dependent parameters of Device Under Tests (DUTs) using an Open-Short-Load-Line calibration that can be applied to transmission lines, inductors and capacitors. Theoretically, the results from TDR through calibration techniques should be the same as those of NA if there is no noise. However, while VNA generates sinusoidal signals with constant amplitude regardless of frequency, the step pulse of TDR has the frequency spectrum in Figure 1.8 whose amplitude decreases with frequency. Hence, at high frequencies, the signal-to-noise ratio of TDR is much lower than VNA, and the accuracy of TDR is much worse than VNA. However, at low frequencies, the signal-to-noise ratio of TDR can be larger than VNA. In this dissertation, the error bound of TDR calibrated results due to noise has been analyzed and compared to the error bound of common VNAs for one-port measurements. It has been shown that the error bound of TDR calibrated results is smaller than that of VNA results at frequencies below ~2Ghz, which means that TDR is more accurate than VNA at frequencies below ~2Ghz. As discussed in the previous section, the low frequency response of digital systems should be accurately characterized. Therefore, TDR measurements are more efficient than NA measurements for digital systems.

#### 1.7.3. Previous research in TDR measurements

The previous research in TDR measurements has been summarized and shown in Figure 1.11. Hewlett-Packard and Tektronix first provided commercial Time-Domain Reflectometry (TDR) equipment generating step pulses in the 1960s [A15][A16][A17]. By 1970, the TDR was primarily used for measuring the characteristic impedance of transmission lines. Up to the early 1990s, since a step pulse has a wide bandwidth

from DC to  $1/(\pi \cdot Tr)$  where Tr is the risetime, TDR was used for characterizing electronic systems over a large frequency bandwidth. A Fourier transform was used to obtain the frequency information from the TDR response [A18][A19]. Transistor parameters were obtained by fitting the model equations to the step response [A20]. In [A21], the frequency response of the DUT was directly computed from time-domain measurements using Prony's method. Comparing time-domain simulations to TDR measurements yielded wide-band models for circuits [A22][A23]. The characteristic impedance of transmission lines was calculated through an eigen-value method using TDR measurements [A24]. An extended method of characteristics was applied to simulate and extract frequency-dependent RLGC parameters [A25]. The complex permittivity of materials was extracted using TDR measurements in [A26][A27][A28].

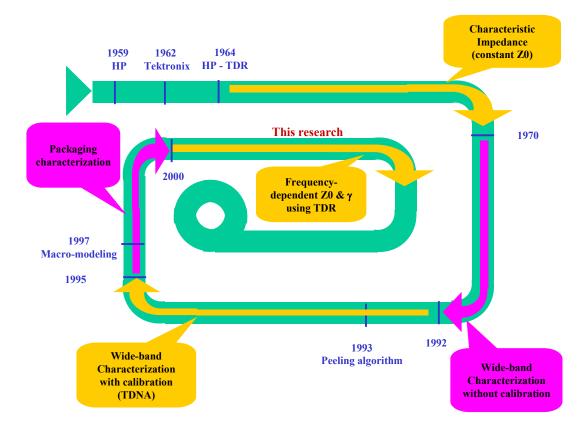


Figure 1.11 Previous TDR measurements

However, the frequency domain data extracted from time-domain measurements had error, especially at high frequencies, because no calibration techniques were used. In the mid 1990s, researchers began to use calibration techniques similar to those of Network analyzer measurements to improve the accuracy of the extracted frequency data. Similar to Network Analyzer measurements, the calibration techniques were called 'Time Domain Network Analysis (TDNA).' Since Network Analyzers were relatively expensive, TDNA provided an alternative method for characterization. A normalization algorithm was used in TDR equipment to improve the accuracy in the late 1980s [A29]. However, this algorithm was not a calibration method. Around the early 1990s, many calibration methods were developed for TDR or TDR/TDT (Time Domain Reflectometry/Time Domain Transmission) such as 1) calibration using a 50 ohm load and a short circuit standard for TDR [A30], 2) calibration using a short circuit standard for TDR and a thru standard for TDT using short-pulse sampling [A31], 3) SOL (Short-Open-Load) calibration for TDR and SOLT (Short-Open-Load-Thru) calibration for TDR/TDT [A32][A33], 4) TRL (Thru-Reflect-Line) calibration for TDR/TDT [A34][A35][A36], and 5) Multi-line TRL calibration for TDR/TDT [A37][A38]. Another interesting method developed in the mid 1990s was the layer peeling algorithm for extracting the spatial impedance distribution of packaging structures from TDR/TDT measurements [A39].

Based on the method developed, the TDNA system was used for package/board characterization to determine the complex permittivity and permeability in the late 1990s [A40][A41]. Also error analysis was performed to assess the accuracy of TDNA systems [A42][A43][A44][A45][A46]. The layer peeling algorithm was upgraded for characterizing packaging from TDR/TDT measurements [A47][A48][A49]. In addition, macro-modeling methods were developed that enabled the extraction of models directly from a time

domain waveform [A50][A51][A52]. Using this method, S-parameters of packaging structures could be extracted using Open and Short calibration standards [A51].

The calibration techniques, layer peeling algorithm and macro-modeling methods have been applied for characterizing two-conductor transmission lines. Multi-conductor transmission lines have been also characterized using TDR/TDT measurements, sometimes with the help of NA measurements. In [A53], the characteristic impedance matrix of multi-conductor uniform transmission lines was extracted from TDR/TDT measurements using single-line excitations. Lossy asymmetric coupled microstrip lines were characterized using Vector Network Analyzers (VNAs) in [A54]. In [A55], the mutual capacitance and mutual inductance of coupled lines were extracted using a hybrid method based on VNA and TDR measurements. In [A56], the self and mutual capacitance and inductance were extracted using even- and odd-mode TDR measurements, assuming that the coupled lines are lossless. In [A57][A58][A59], multi-conductor transmission lines were characterized using two-port Network Analyzers. In [A60], differential circuits were characterized using four-port Network Analyzer measurements.

#### 1.7.3.1. One-port TDR calibration using two standards

In [A30], two standards consisting of a 50 ohm load and a short-circuit standard were used to place the reference plane before the DUT and for compensating the imperfections in the measurement setup before the DUT. Using the measured information of the two reference standards, a frequency-domain filter was created as a calibration box. DUT measurement data was first converted to the frequency domain, and the frequency domain data was filtered using the developed filter based on the two reference standards. Then, the data was finally converted to the time domain, which was the calibrated measured data of the DUT in the time domain.

#### 1.7.3.2. One-port TDR calibration using three standards

Three standards consisting of Open, Short, and Load (SOL) calibration were applied to one-port TDR measurements as shown in Figure 1.12(a) [A33]. This is similar to one-port Network Analyzer calibration. The error model used is shown in Figure 1.12(b).

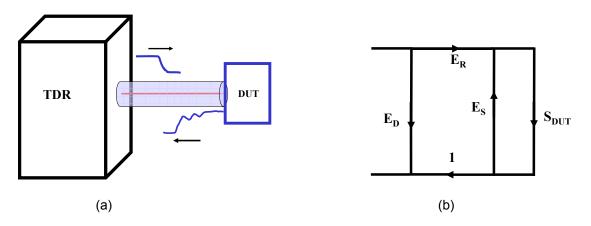


Figure 1.12 (a) TDR measurement setup and (b) one-port error model.

The directivity factor  $E_D$  represents systematic errors such as the crosstalk between different channels, the trigger coupling and the reflections of cables and connectors. The reflection frequency response factor  $E_R$  represents the unwanted filter characteristics of the measurement system such as losses in cables and connectors. The source impedance match factor  $E_S$  represents the impedance mismatch of the test set-up reflection return port. The three unknown parameters in Figure 1.12(b) were extracted from the measurements on the three standards measurements. Then, the model was applied to the DUT measurements. This method is more accurate than the two-standard calibration.

#### 1.7.3.3. Uni-directional two-port TDR/TDT calibration

The uni-directional TDR/TDT measurement setup shown in Figure 1.13(a) has a steppulse source and a sampler in port1 and has only a sampler in port2. This measurement setup is uni-directional since the step-pulse propagates only from port1 to port2. For calibration, four calibration standards consisting of Short-Open-Load-Thru (SOLT) are necessary since there are five unknown parameters in the error model in Figure 1.13(b) [A32].

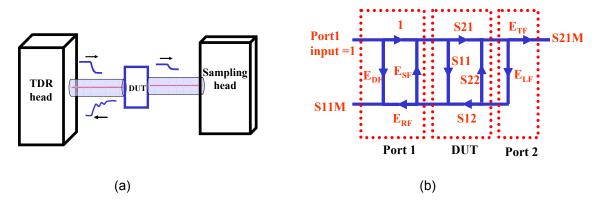


Figure 1.13 (a) Uni-directional TDR/TDT setup and (b) its Error model.

Since the thru measurement has both a reflection and transmission, there are a total of five measurements in the SOLT calibration. Open, Short, and Load have been applied for finding the error parameters  $E_{DF}$ ,  $E_{SF}$ , and  $E_{RF}$  in port1. Then, thru measurement has been used for extracting  $E_{LF}$  and  $E_{TF}$ . After extracting the five unknown parameters, the error model was applied to two-port TDR/TDT measurements.

The uni-directional two-port TDR/TDT calibration has a limitation. When measuring a two-port DUT, only two measurements, namely a reflection and transmission are obtained. However, a DUT has four unknown parameters: S11, S21, S12 and S22 in the error model as shown in Figure 1.13(b). Therefore, this calibration technique can only be applied to symmetric and reciprocal DUTs.

# 1.7.3.4. Bi-directional two-port TDR/TDT calibration

Bi-directional two-port TDR/TDT calibration uses both the forward and backward measurements, as shown in Figure 1.14. In the forward measurement, the pulse source is in port1, while the pulse source is in port2 in the backward measurement.

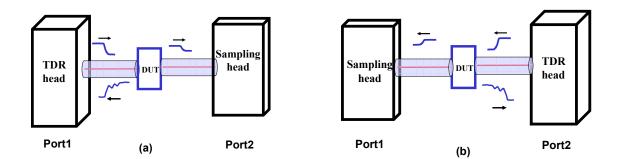


 Figure 1.14
 Bidirectional two-port TDR/TDT measurement setup.

 (a) forward measurement and (b) backward measurement.

Two-port calibration as used in Vector Network Analyzer (VNA) measurements can be directly applied for bi-directional two-port TDR/TDT calibrations. Examples of standards used are SOLT [A33], TRL (Thru-Reflect-Line) [A34][A35][A36], and Multiline TRL [A37][A38]. In VNA calibration, three kinds of two-port error models have been developed: 1) a 12-term error model as in Figure 1.15, 2) a 8-term error model as in Figure 1.16, which ignores the crosstalk from the 12-term error model, and 3) a 16-term (or 15-term) error model which includes all the crosstalk parameters. The 12-term error model is the most popular model whose parameters were extracted by using SOLT calibration. The 8-term error model can be derived from the 12-term error model by ignoring the crosstalk terms E<sub>XF</sub> and E<sub>RF</sub>. For calibrating the parameters in the 8-term error models; TRL (Thru-Reflect-Line), LRL (Line-Reflect-Line), LRM (Line-Reflect-Match), LRRM (Line-Reflect-Reflect-Match) and SOLR (Short-Open-Load-Reciprocal) calibrations can be used. According to a probe supplier (Cascade microtech), LRRM is the most accurate, LRM is the next and SOLT follows in terms of accuracy [A61]. Usually TRL is not generally recommended [A61]. The 16-term error model is the most complex model which includes all the crosstalk leakage at both ports. The 16-term error model is claimed to be the most proper calibration for lossy silicon wafer tests [A62].

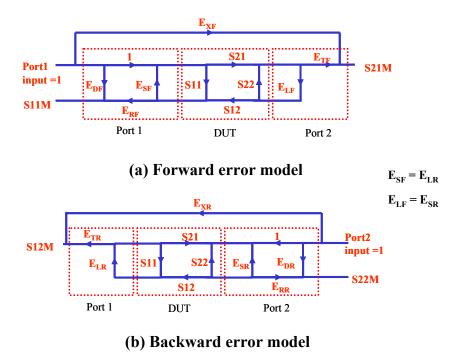


Figure 1.15 12-term error model for bidirectional TDR/TDT calibrations.

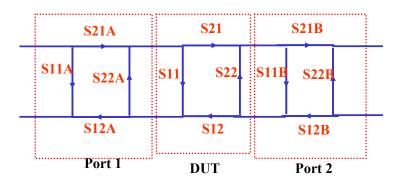


Figure 1.16 8-term error models for bidirectional TDR/TDT calibrations.

Using SOLT calibration, the 12-term error model in Figure 1.15 can be extracted. SOL measurements for each port have been used to obtain  $E_{DF}$ ,  $E_{RF}$ ,  $E_{SF}$ ,  $E_{DR}$ ,  $E_{RR}$ , and  $E_{SR}$ . Since  $E_{SF}=E_{LR}$  and  $E_{LF}=E_{SR}$ , four unknown parameters in the 12-term error model of Figure 1.15 can be extracted from a Thru measurement. The thru measurement consists of both forward and backward measurements, with each measurement having a

reflection and transmission. Therefore, there are a total of four measurements, which can be used for extracting the remaining four unknown parameters.

## 1.7.3.5. Layer peeling algorithm

The layer peeling algorithm has been used in [A39][A47] for computing the spatial impedance distribution from TDR/TDT measurements. The layer peeling algorithm begins with the assumption that a non-uniform structure can be expressed as summation of cascaded uniform transmission lines, as shown in Figure 1.17.

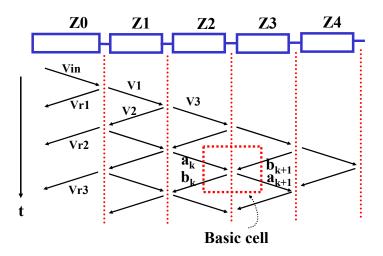


Figure 1.17 TDR/TDT response with time.

In Figure 1.7, the impedance of the first section Z1 can be found using the reflected voltage Vr1 using the equation.

$$\frac{Vr1}{Vin} = \frac{Z1 - Z0}{Z1 + Z0}$$
(1.2)

where  $Z0 = 50\Omega$  is the impedance of the TDR equipment. After finding Z1, Z2 can be calculated using the reflected voltages Vr2, Vr1 and impedance Z1. Using this procedure, the spatial impedance distribution Z1, Z2, Z3 and Z4 can be found.

Jong and Tripathi formulated an algorithm for peeling the impedance distribution using the concept of the basic cell in Figure 1.17 [A39][A47]. Although the layer peeling algorithm is very useful to characterize non-uniform transmission lines, it cannot be used to extract the frequency-dependent parameters of transmission lines.

#### 1.7.3.6. Macro-modeling approach

In [A51], a method for extracting the transmission line parameters directly from TDR/TDT measurements has been discussed using Short-Thru calibration. A short calibration measurement was used for setting the reference plane. Then, using the Generalized Pencil of Function Method, the poles of the system were captured. A thru calibration measurement was used to de-convolve the effect of the step source and for finding the residues of the system. The impulse response of the DUT was extracted in the form of a rational function, as given below:

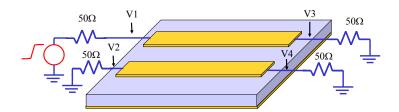
$$H(s) = \sum_{k=1}^{M} \frac{a_k}{s - s_k}$$
(1.3)

where  $s=j\omega$ ,  $a_k$  are the residues,  $s_k$  are the poles, M is the number of poles in the approximation, and  $\omega$  is the angular frequency. In Equation (1.3), H(s) is the transfer function of the DUT which can be used for simulation. From the transfer function of the transmission line, the frequency-dependent characteristic impedance and propagation constant were extracted in [A51].

# 1.7.3.7. Characteristic impedance matrix characterization using single-line excitations

In [A53], the characteristic impedance matrix of multi-conductor uniform transmission lines was extracted using TDR/TDT measurements. Using (1,0) excitation as shown in Figure 1.18, four measurements were used at ports V1, V2, V3 and V4. This was repeated for (0,1) excitation. Using the measurement data, the eigen-value and eigen-

vector of the characteristic impedance matrix of the coupled line was calculated, from which the characteristic impedance matrix was extracted.



**Figure 1.18** (1,0) excitation of coupled lines.

# 1.7.3.8. Asymmetric coupled line characterization using Network Analyzer

Lossy asymmetric coupled microstrip lines were characterized using Vector Network Analyzers (VNAs), using an electrical model for the multi-conductor transmission line under test [A54]. The characterization procedure consisted of three steps, as shown in Figure 1.19.

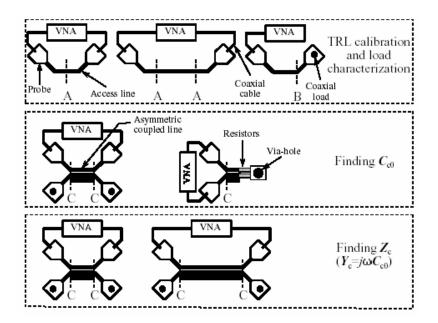


Figure 1.19 Schematic representation of the NA measurement procedure.

The first step was used to calibrate an over-determined set of two-port measurements using a two-port multiline thru-reflect-line (TRL) method. The second step was used to find the low-frequency limit of the line's per-unit-length capacitance matrix. The third step was based on the fact that the per-unit-length admittance matrix can be approximated from the per-unit-length capacitance matrix over the entire frequency range. This method resulted in a constant per-unit-length capacitance matrix and frequency-dependent resistance and inductance matrices for coupled lines.

#### 1.7.3.9. Hybrid method using TDR and VNA measurements

A hybrid method was used for characterizing coupled lines in [A55]. In [A55], the mutual capacitance and mutual inductance of coupled lines were extracted based on VNA and TDR measurements, as summarized in Figure 1.20.

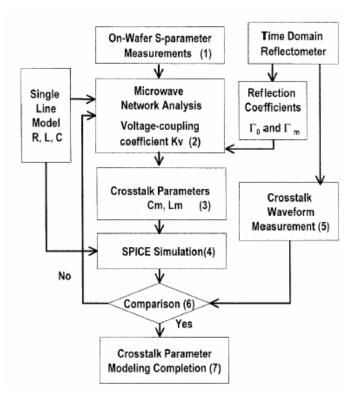
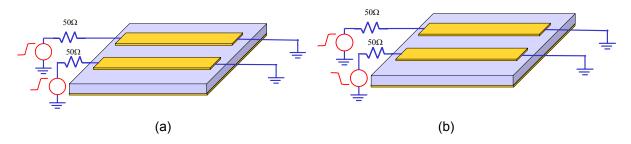


Figure 1.20 Extraction procedure of crosstalk parameters in [A55].

First, the voltage-coupling coefficient (Kv) is calculated from VNA measurements. Then, mutual capacitance (Cm) and mutual inductance (Lm) are calculated from the voltage-coupling coefficient, and the known single line self-capacitance and self-inductance parameters. Next, SPICE simulation is used for extracting the crosstalk parameters which are compared with TDT measurements. Finally, crosstalk parameters are optimized in SPICE such that the simulated waveforms match with TDT measurements. This extraction method is useful for characterizing homogeneous guiding structures, where the propagation of coupled transverse electromagnetic (TEM) modes are supported.

#### 1.7.3.10. Lossless coupled line characterization using TDR measurements

In [A56], the self and mutual capacitance and inductance were extracted using evenand odd-mode TDR measurements, assuming that the coupled lines are lossless. From the even- and odd-mode TDR measurements, the characteristic impedance  $Z_{even}$ ,  $Z_{odd}$ , and propagation delay  $t_{even}$ , and  $t_{odd}$  are extracted as shown in Figure 1.21



**Figure 1.21** (a) Even and (b) odd- mode TDR measurements.

where  $Z_{even}$  and  $Z_{odd}$  are the even and odd-mode characteristic impedances, and  $t_{even}$  and  $t_{odd}$  are even- and odd-mode delays, respectively. Then, using Equation (1.4), the self and mutual capacitance and inductance are extracted.

$$L_{self} = \frac{1}{2} \left( Z_{even} t_{even} + Z_{odd} t_{odd} \right) \qquad C_{total} = \frac{1}{2} \left( \frac{t_{odd}}{Z_{odd}} + \frac{t_{even}}{Z_{even}} \right)$$

$$L_{mutual} = \frac{1}{2} \left( Z_{even} t_{even} - Z_{odd} t_{odd} \right) \qquad C_{mutual} = \frac{1}{2} \left( \frac{t_{odd}}{Z_{odd}} - \frac{t_{even}}{Z_{even}} \right)$$

$$(1.4)$$

#### 1.7.3.11. Network Analyzer measurement of multi-conductor transmission lines

Since a Network Analyzer is basically a two-port measurement equipment, measurement of multi-port devices requires mathematical techniques for representing a multi-port device as summation of two-port devices [A57][A58][A59]. The techniques presented in [A57][A58] are based on the transformation of port impedances, as shown in Figure 1.22. In Figure 1.22(a), each port is terminated with impedance  $\zeta_i$  (i=1,2, ... n) and the scattering parameter measured with the port impedance  $\zeta_i$  is represented as [S], which is a n x n matrix. The port impedance represents the input impedance of the measurement port. In other words, the transmission line in Figure 1.22(a) is measured with an equivalent n-port Network Analyzer whose port impedances are  $\zeta_i$ . The measured result from the n-port Network Analyzer can be represented as a [S]<sub>nxn</sub> matrix. In Figure 1.22(b), each port is terminated with  $Z_i$  (i=1,2,... n) and the scattering parameter [S']<sub>nxn</sub> can be measured with n-port Network Analyzers whose port impedances are  $Z_i$  (i=1,2,... n).

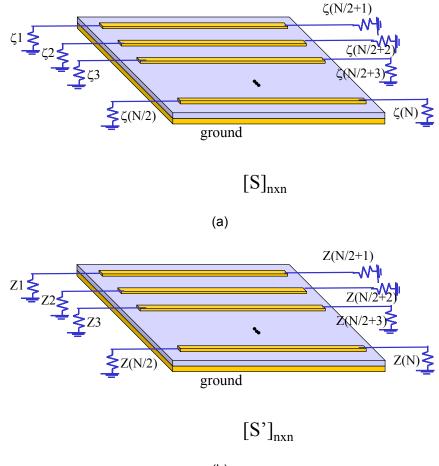
Based on the methods presented in [A57][A58], [S] and [S'] have the following relationship:

$$S' = (I - S)^{-1}(S - \Gamma)(1 - S \cdot \Gamma)^{-1}(I - S)$$

$$\Gamma = \begin{bmatrix} \Gamma_1 & 0 & 0 \dots & 0 \\ 0 & \Gamma_2 & 0 \dots & 0 \\ \vdots & & & \\ 0 & 0 & 0 \dots & \Gamma_n \end{bmatrix}, \quad \Gamma_i = \frac{Z_i - \zeta_i}{Z_i + \zeta_i}$$
(1.5)

where *S* is the original scattering matrix normalized to a given set of port impedances  $\zeta_i$  (i=1,2,..n), *S*' is the transformed scattering matrix normalized to a new set of port impedances  $Z_i$  (i=1,2,..n), and *I* is the nxn identity matrix. Then, using Equation (1.5),

multi-port devices can be measured using two-port Network Analyzers. As an example, a four-port hybrid coupler was measured in [A57]. Using this method, the scattering parameter of (n+1)-conductor transmission lines can be extracted. However, developing models for the (n+1)-conductor transmission lines from the measured scattering parameter can be a problem. The model development can be done using optimization [A63], or by using T- or  $\Pi$ - circuit models which are valid at frequencies below 1GHz [A64]. Hence, although Network Analyzer can accurately measure the scattering parameter of (n+1)-conductor transmission lines, modeling (n+1)-conductor transmission lines from the measured scattering parameters can be a problem.



(b)

Figure 1.22 Transformation of port impedances.

# 1.7.3.12. Mixed-mode characterization

In [A60], differential circuits were characterized from standard S-parameters using a transformation between standard S-parameters and mixed-mode S-parameters. Standard S-parameters are S-parameters obtained using single-ended Network Analyzers, which can be expressed as:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S \end{bmatrix}_{std} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}$$
(1.6)

where ai and bi are the waves measured at ports 1-4. On the other hand, mixed-mode S-parameters are S-parameters for differential and common-mode signals, which can be defined as:

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} S \end{bmatrix}_{mm} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \begin{bmatrix} S_{dd} & S_{dc} \\ S_{cd} & S_{cc} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix}$$
(1.7)

where

$$a_{d1} = \frac{1}{\sqrt{2}}(a1 - a2), \quad a_{d2} = \frac{1}{\sqrt{2}}(a3 - a4)$$
$$a_{c1} = \frac{1}{\sqrt{2}}(a1 + a2), \quad a_{c2} = \frac{1}{\sqrt{2}}(a3 + a4)$$
$$b_{d1} = \frac{1}{\sqrt{2}}(b1 - b2), \quad b_{d2} = \frac{1}{\sqrt{2}}(b3 - b4)$$
$$b_{c1} = \frac{1}{\sqrt{2}}(b1 + b2), \quad b_{c2} = \frac{1}{\sqrt{2}}(b3 + b4)$$

Then, the standard four-port S-parameters and mixed-mode S-parameters have the following relationship:

$$[S]_{mm} = M[S]_{std} M^{-1}$$
(1.8)

where

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0\\ 0 & 0 & 1 & -1\\ 1 & 1 & 0 & 0\\ 0 & 0 & 1 & 1 \end{bmatrix}$$

This transformation is useful for characterizing differential circuits from standard Sparameters. Currently, instead of using single-ended vector Network Analyzers, mixedmode S-parameters can be directly measured using mixed-mode (or pure-mode) vector Network Analyzers generating differential and common-mode signals.

#### 1.7.3.14. W-element models for transmission lines in Hspice

In this dissertation, transmission lines were simulated using W-element models in Hspice [A65]. There are three models for transmission lines in Hspice, namely, T models, U models and W-element models. W-element models are the most advanced models for simulating lossy transmission lines in the time domain, having been added to Hspice in 2000. There are three merits for using W-element models. First, W-element models include the causality condition of lossy transmission lines with finite length. Hence, the delay effect of lossy transmission lines can be accurately simulated in the time domain. Second, W-element models can simulate the frequency-dependent parameters of transmission lines such as frequency-dependent resistance, inductance, admittance and capacitance. Finally, W-element tabular models can simulate any frequency-dependent parameters associated with lossy transmission lines. Therefore, measurement results from VNA and TDR can be simulated using W-element tabular models.

# 1.8. Outline of the dissertation

This dissertation consists of 7 chapters with details provided in the following sections.

#### 1.8.1. Chapter 1: Introduction

The motivation, introduction and goal of this dissertation have been described. The goal of this dissertation is the demonstration of methods that enable gigabit data transmission in both the IC and package. In this dissertation, electrical issues associated with gigabit data transmission using a wafer-level package test vehicle have been discussed. The test vehicle consists of two board transmission lines, one silicon transmission line, and solder bumps with 50um diameter and 100um pitch. TDR characterization methods for transmission lines have been developed in this dissertation. The measurement need for Time-Domain Reflectometry (TDR) has been described for characterizing digital systems. The previous research on TDR has been reviewed.

## 1.8.2. Chapter 2: Calibration and Error Analysis in TDR/TDT measurements

In this chapter, the Short-Open-Load (SOL) calibration technique for TDR measurements is investigated for extracting frequency-domain information from TDR measurements. The uncertainty in the SOL calibration is quantified and compared to that of Network Analyzers. It has been shown that the error or uncertainty of SOL calibration for TDR with  $\pm 1.5$ ps drift is lower than Network Analyzer below 2GHz, but higher for frequencies greater than 2GHz. The maximum absolute uncertainty of SOL calibration for TDR is 0.0026 at 50MHz, 0.02 at 2GHz and 0.075 at 8GHz for  $|S_{11M}| = 1$ . Using similar analysis, it has been estimated that the Vector Network Analyzer has absolute uncertainty of 0.02 at 50MHz, 0.026 at 2GHz and 0.043 at 20GHz for  $|S_{11M}| = 1$ . For improving the accuracy of the SOL calibration, Open-Short-Load-Line (SOLL) calibration for TDR measurements are proposed and applied for characterizing transmission lines in the following chapters. For evaluating the accuracy of SOLL calibration, inductors, capacitors and microwave filters are characterized and compared to NA measurement results, showing good correlation. Two-port TDR/TDT calibrations are also discussed.

#### 1.8.3. Chapter 3: Characterization of Package Transmission Lines

The TDR calibration method developed in Chapter 2 is applied to transmission lines in Chapter 3. The frequency-dependent characteristic impedance and propagation constant of transmission lines are extracted with a pad de-embedding technique proposed for TDR measurements. Non-physical RLGC models for package transmission lines are developed for simulating the extracted data. Three transmission line models are discussed by comparing simulations to time-domain measurements, namely, the non-physical RLGC models based on TDR measurements, conventional physical RLGC models based on 2-D Maxwell equations' simulators, and Vector Network Analyzer (VNA)-based models. In addition, an in-situ characterization method for package transmission lines using TDR measurements is developed for extracting the frequencydependent characteristic impedance and propagation constant without the need for calibration. Various Printing Wiring Board (PWB) transmission lines are characterized using TDR measurements, simulated with non-physical RLGC models, and verified by correlating simulations to time-domain measurements. The optimum structure for the board transmission line in the wafer level package test vehicle is selected from the various PWB transmission lines characterized.

#### 1.8.4. Chapter 4: Characterization of Silicon Transmission Lines

The TDR characterization method in Chapter 3 is applied to silicon transmission lines in Chapter 4, and the limitation of the TDR characterization method is discussed. Coplanar lines on high-resistivity (2000  $\Omega$ -cm) and low-resistivity (100  $\Omega$ -cm) silicon substrate are fabricated and characterized using NA and TDR measurements. Non-physical RLGC models for silicon transmission lines including slow-wave propagation effect are developed for characterizing silicon transmission lines and simulating the extracted data from NA and TDR measurements. The accuracy of the non-physical RLGC models for silicon transmission lines with slow-wave propagation effect is verified results.

by showing the good correlation between simulations and measurements in the time and frequency domain. The optimum structure for the wafer level packaging test vehicle is selected from the various silicon transmission lines characterized.

#### **1.8.5.** Chapter 5: Characterization of Multi-conductor Transmission Lines

The TDR characterization methods for two-conductor transmission lines in Chapter 3 are extended to multi-conductor transmission lines in Chapter 5. Coupled line and differential lines are fabricated, characterized from TDR measurements, simulated with non-physical RLGC models, and verified by correlating simulations to time-domain measurements. Non-physical RLGC models for coupled lines, differential lines, (3+1)-conductor transmission lines and (n+1)-conductor transmission lines are developed for characterizing and simulating transmission lines. The stability of non-physical RLGC models for lossy (n+1)-conductor transmission lines is demonstrated by simulating (3+1) and (64+1)-conductor transmission lines.

# 1.8.6. Chapter 6: Wafer-level Package on Integrated Board

In Chapter 6, the effect of assembled wafer-level package, silicon substrate and board material, and material interfaces on gigabit data transmission is investigated using the wafer-level package test vehicle described in Chapter 1. The board and silicon transmission lines for the test vehicle are chosen based on the results in Chapter 3 and Chapter 4. The solder bumps with 50um diameter and 100um pitch are analytically modeled. The effect of the parasitic capacitance in the solder bumps on gigabit data transmission is discussed. It is concluded that better signal integrity cannot be achieved only by using lower loss material, but also requires low parasitic capacitance for signal transmission from the chip to the board.

## 1.8.7. Chapter 7: Conclusion and Future Work

Chapter 7 concludes the dissertation with the proposal for the continuing work of this dissertation.

# **Chapter 2**

# Calibration and Error Analysis in TDR/TDT Measurements

This chapter discusses the calibration and error analysis for Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) measurements. The purpose of TDR calibration is to accurately extract the frequency-domain response of interconnects from time-domain measurements. In this chapter, the calibration algorithm and error analysis of Short-Open-Load (SOL) calibration for TDR measurements are discussed in detail. A Short-Open-Load-Line (SOLL) calibration for TDR measurements is proposed for improving the accuracy. In this chapter, capacitors and inductors are characterized using TDR measurements.

#### 2.1. Block Diagram of TDR equipment

The TDR head consists of a step source, a sampler and an ADC converter, as shown in Figure 2.1. The step source generates a step pulse, which is supplied to the Device Under Test (DUT) through an SMA connector. The Tektronix instrument (SD24) has a pulse source with a risetime of 30ps and amplitude of 250mV. The reflected signals are detected by the sampler and converted to digital signals through the 8-bit ADC converter. The output impedance seen from the SMA connector is 50  $\Omega$  and the source impedance of the step source is also 50  $\Omega$ , which translates to the input impedance of the sampler being much higher than 50  $\Omega$ .

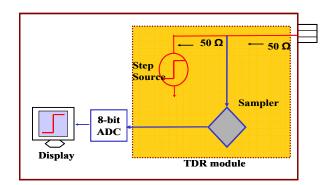


Figure 2.1 Block Diagram of SD24 TDR head and 11801B sampling oscilloscope.

# 2.2. Error in TDR measurements

TDR measurements have two kinds of errors, namely, systematic and random error [B1][B2].

# 2.2.1. Systematic error

Systematic error occurs in every measurement, is predictable, and can therefore be removed by calibration. The source of systematic error is the deviation from the ideal performance of every component in the TDR equipment. Since the sampling circuit, cable loss, characteristic impedance, calibration standards, and microprobes are not perfect, these imperfections are included in the measurement results. The calibration technique discussed in Chapter 1 can be used to eliminate the systematic error from measurements.

#### 2.2.2. Random error

Random error consists of vertical noise, jitter and drift. Vertical noise represents the amplitude of random noise. Jitter represents the random effect in the sampling circuit. Ideally, the sampling circuit must obtain samples at regular intervals. However, due to random noise, there is a variation in the sampling interval, which causes jitter. Jitter induces horizontal random noise causing variation along the time axis. Drift represents the random effect in the step source. The step source generates a very fast periodic step

pulse with a 30ps risetime using the internal clock of the sampling oscilloscope. However, since the internal clock and the step source circuit are not perfect, the generated step source has a small timing difference which is called drift. Drift causes horizontal random noise along the time axis.

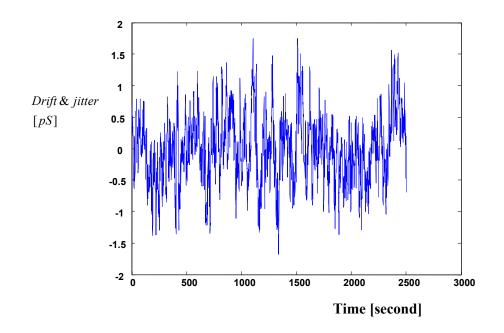
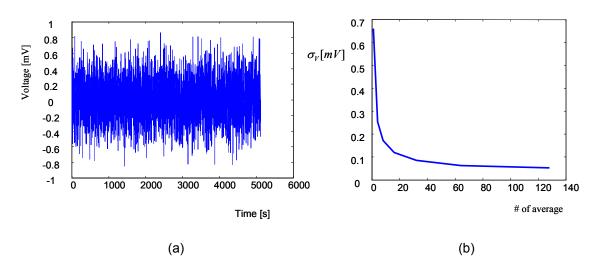


Figure 2.2 Measured horizontal random noise of the TDR equipment.

In Figure 2.2, the horizontal random noise caused by drift and jitter was measured using a Tektronix SD24 TDR head and 11801B sampling oscilloscope. The figure shows variation from the steady value. The median height of the step pulse was measured every second with the time recorded. In Figure 2.2, the TDR system used had  $\pm$  1.5 ps drift. Similarly, vertical random noise was measured, as shown in Figure 2.3. Assuming that the vertical random noise can be expressed as a normal distribution, its standard deviation has been plotted as a function of the number of averages in Figure 2.3(b). The vertical random noise has ~ 0.1 mV standard deviation using an averaging of 32.



**Figure 2.3** (a) Measured vertical random noise and (b) its standard deviation as a function of number of averages.

# 2.2.3. Effect of systematic and random error

The effect of systematic and random noise on extracted data from TDR can be explained in the following way. Let  $\mu$  be the true value of a parameter associated with a Device Under Test (DUT) measured using a TDR. Then, since there are random errors, the output result extracted from the TDR measurements has a normal distribution if the measurement is done repeatedly. The measurement can therefore be represented statistically as:

$$\overline{X} = N(\overline{\mu}, \sigma^2) \tag{2.1}$$

where the random variable  $\overline{X}$  is the measured waveform extracted from the TDR,  $\overline{\mu}$  is the average of the samples, and  $\sigma$  is the standard deviation. Based on Equation (2.1), systematic error is associated with  $\overline{\mu}$  causing error in  $\overline{\mu}$ , and random error affects  $\sigma$ thereby inducing error. Since calibration removes all the systematic errors, it corrects  $\overline{\mu}$ so that  $\overline{\mu} = \mu$ . However, there still exists random noise which causes uncertainty in the extracted results. In random noise, drift has the largest effect on the extracted frequency response after calibration. The effect of drift has been modeled and analyzed in Section 2.4.

# 2.3. Short-Open-Load (SOL) calibration for TDR measurements

Accurate one-port error models for calibration have three unknown parameters, as shown in Figure 2.4. Therefore, three known calibration standard measurements are required to find the three unknown parameters. Since Short-Open-Load calibration structures have high accuracy [B3], SOL calibration is often used for one-port calibration.

# 2.3.1. Time to Frequency domain Conversion

If a DUT is a linear time-invariant system, the incident signal p(t) and the reflected signal r(t) from the DUT can be related using the impulse response h(t) of the DUT in the form:

$$r(t) = p(t) \otimes h(t) \tag{2.2}$$

where  $\otimes$  is the convolution operator. Taking the derivative of Equation (2.2), (2.2) becomes

$$r'(t) = p'(t) \otimes h(t)$$
 (2.3)

where r'(t) and p'(t) are the derivatives of the reflected and incident waveforms, respectively. Using the Z-transform applied to Equation (2.3),

$$R'(Z) = P'(Z) H(Z)$$
 (2.4)

where the Z-transform of a discrete signal, X(Z), is defined as

$$X(Z) = \sum_{n=0}^{\infty} x(n) Z^{-n}$$
where  $Z = e^{j\omega T_s}$ 
(2.5)

In Equation (2.5),  $T_s$  is the sampling interval, x(n) are the discrete samples and  $\omega$  is the angular frequency. Since the Fourier transform of a finite length data stream x(n) is

performed with zeros patched outside x(n) from  $-\infty$  to  $\infty$ , the Fourier transform of a finite step pulse includes the frequency response of the abrupt transition at the end of the pulse if the final value for x(n) is not zero. However, the derivative of a step pulse has zero final value since the step pulse has a constant value in the steady state. Therefore, the Fourier transform of the derivative of the pulse does not include the abrupt transition. The sampling interval, Ts, determines the bandwidth that can be obtained using the calibration method discussed in this chapter. A sampling interval of 0.5ps was used in this dissertation, which results in a frequency bandwidth > 20GHz without aliasing error.

# 2.3.2. SOL Calibration

High Frequency measurements require the specification of reference planes. A DUT is always characterized at or between reference planes for a 1-port or 2-port measurement, respectively. Calibration structures are required to de-embed parasitics and discontinuities from the measurements at the reference planes. In this dissertation, Short-Open-Load calibration has been used for 1-port TDR measurements. As mentioned earlier, the parasitics and other discontinuities affect the accuracy of the measurements.

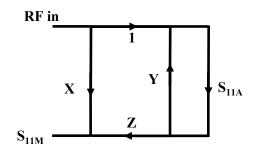


Figure 2.4 One-port error model for Short-Open-Load (SOL) calibration.

For a 1-port TDR measurement, an error model using a signal flow graph can be constructed, as shown in Figure 2.4 [B3]. In the Figure, x, y and z are the unknown

parameters which are calculated from the open, short and 50 ohm-load standard measurements. In Figure 2.4,  $S_{11A}$  is the actual response of the DUT and  $S_{11M}$  is the measured response which includes all the imperfections of the measurement setup used. From Figure 2.4, using the signal flow graph, the frequency response of the DUT can be derived as:

$$S_{11A} = \frac{S_{11M} - x}{yS_{11M} - xy + z}$$
(2.6)

If the open, short and load measurements are expressed as  $S_{11MO}$ ,  $S_{11MS}$  and  $S_{11ML}$  respectively, the variables x, y and z in Equation (2.6) can be expressed as:

$$x = S_{11ML}$$

$$y = \frac{S_{11MO} + S_{11MS} - 2S_{11ML}}{S_{11MO} - S_{11MS}}$$

$$z = \frac{2(S_{11ML} - S_{11MO}) (S_{11MS} - S_{11ML})}{S_{11MO} - S_{11MS}}$$
(2.7)

Once x, y and z parameters are computed, these parameters can be used to calibrate the DUT, similar to a network analyzer calibration.

An interesting point to note in Equation (2.6) and (2.7) is that the incident signal from TDR, p(t), need not be measured. Since S-parameters are expressed as the ratio (reflected signal/incident signal), the reference signal in Equation (2.6) and (2.7) is cancelled. In addition, linear operations on the four signals such as differentiation and integration do not change the results in the extraction procedure. Hence, derivatives of the signals have been used to compute S<sub>11A</sub>, using Equation (2.6) and (2.7).

# 2.4. Error Analysis for SOL calibration

#### 2.4.1. Drift error model

For the error analysis of the SOL calibration in Figure 2.4, the induced error due to random noise was modeled and used in the error analysis. From the previous section,

the test system used had a drift of  $\pm$  1.5ps. The step pulse had a risetime of 30ps and amplitude of 250mV. The normalized drift error model was extracted from the comparison between two pulses, namely, a step pulse with 30ps risetime and a step pulse with 1.5ps delay and 30ps risetime. The difference between the two pulses shows the maximum random variation of the incident pulse due to drift. After the Fourier transform of the two pulses, the difference was normalized. The normalized maximum difference can be represented as:

$$\Delta_{\max} = 1 - \exp(\pm j \cdot 2\pi \cdot f \cdot 1.5 \, ps) \tag{2.8}$$

where f is the frequency in Hertz. Equation (2.8) shows that the difference becomes larger as frequency increases, which means that the uncertainty of TDR measurements becomes larger with an increase in frequency. The random error in Equation (2.8) has been used to quantify the uncertainty of extracted data from TDR measurements using SOL calibration.

#### 2.4.2. Real error analysis

In this analysis, only the real axis of the Smith chart was considered for simplicity. The open, short and load measurements including random noise were modeled as:

$$S_{11MO} = 1 + \Delta S_O$$
  

$$S_{11ML} = \Delta S_L$$
  

$$S_{11MS} = -1 + \Delta S_S$$
  
(2.9)

where  $\Delta S_{O}$ ,  $\Delta S_{L}$ , and  $\Delta S_{S}$  are the normalized random variables of the open, short, and 50 $\Omega$ -load measurements, respectively. The mean of  $\Delta S_{O}$ ,  $\Delta S_{L}$ , and  $\Delta S_{S}$  are zero if the SOL calibration is perfect. Then using Equation (2.9), Equation (2.6) can be modified to include random error as:

$$S_{11A} = \frac{(S_{11M} - \Delta S_L)(2 + \Delta S_O - \Delta S_S)}{(\Delta S_O + \Delta S_S - 2\Delta S_L)S_{11M} + (\Delta S_O + \Delta S_S)\Delta S_L - 2(1 + \Delta S_O)(-1 + \Delta S_S)} \approx \frac{(S_{11M} - \Delta S_L)(2 + \Delta S_O - \Delta S_S)}{(\Delta S_O + \Delta S_S - 2\Delta S_L)S_{11M} + (\Delta S_O + \Delta S_S)\Delta S_L - 2(-1 + \frac{\Delta S_S - \Delta S_O}{2})} If x \approx 0, \quad \frac{1}{1 + x} \approx 1 - x$$

$$S_{11A} \approx S_{11M} - \Delta S_L + S_{11M} \frac{\Delta S_S - \Delta S_O}{2} - \frac{S_{11M}^2}{2}(\Delta S_O + \Delta S_S - 2\Delta S_L) S_{11A} \approx S_{11M} + (S_{11M}^2 - 1)\Delta S_L + \frac{1}{2}(S_{11M} - S_{11M}^2)\Delta S_S - \frac{1}{2}(S_{11M} + S_{11M}^2)\Delta S_O$$

$$(2.10)$$

Then, the error or uncertainty between  $S_{11A}$  and  $S_{11M}$  in Figure 2.4 can be calculated as:

$$(S_{11M}^2 - 1)\Delta S_L + \frac{1}{2}(S_{11M} - S_{11M}^2)\Delta S_S - \frac{1}{2}(S_{11M} + S_{11M}^2)\Delta S_O$$
(2.11)

The error or uncertainty in Equation (2.11) is random because  $\Delta S_{O}$ ,  $\Delta S_{L}$ , and  $\Delta S_{S}$  are random variables. Statistically, the mean of the error is zero since the mean of  $\Delta S_{O}$ ,  $\Delta S_{L}$ , and  $\Delta S_{S}$  are zero. However, if a TDR measurement is performed once, the TDR measurement result has the uncertainty in Equation (2.11). It is important to note that the error in Equation (2.11) depends on the measurement value  $S_{11M}$ . At around  $S_{11M} = 0$ ,  $\Delta S_{L}$  is the most important quantity. Around  $S_{11M}=1$ ,  $\Delta S_{O}$  is the most important quantity, while around  $S_{11M} = -1$ ,  $\Delta S_{S}$  is the most important quantity.

#### 2.4.3. Complex error analysis

In this section, the previous section has been extended to include a complex reflection coefficient to show the uncertainty on the entire Smith chart. There are two kinds of random noise in  $\Delta S_0$ ,  $\Delta S_L$ , and  $\Delta S_S$  in Equation (2.9), which are random vertical noise and drift noise. The random variables in Equation (2.9) have the following distributions, assuming that random noise has normal distributions with zero mean and is independent.

$$\Delta S_{o} \sim N(0, \sigma_{ov}^{2}) + N(0, \sigma_{odr}^{2}) + j \cdot [N(0, \sigma_{ov}^{2}) + N(0, \sigma_{odi}^{2})]$$
  

$$\Delta S_{L} \sim N(0, \sigma_{Lv}^{2}) + j \cdot [N(0, \sigma_{Lv}^{2}))]$$
  

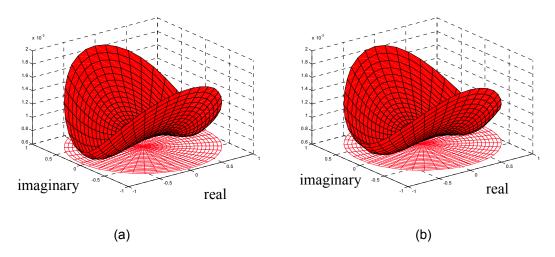
$$\Delta S_{S} \sim N(0, \sigma_{Sv}^{2}) + N(0, \sigma_{Sdr}^{2}) + j \cdot [N(0, \sigma_{Sv}^{2}) + N(0, \sigma_{Sdi}^{2})]$$
(2.12)

In Equation (2.12),  $\sigma_{Ov}, \sigma_{Lv}, \sigma_{Sv}$  are the standard deviations of normalized vertical random noise in the frequency domain for the open, load and short, respectively.  $\sigma_{Odr}, \sigma_{Ldr}, \sigma_{Sdr}$  are the real part of the standard deviations of normalized drift random noise in Equation (2.8),  $\sigma_{Odi}, \sigma_{Ldi}, \sigma_{Sdi}$  are the imaginary part of the standard deviations of normalized drift random noise in Equation (2.8),  $\sigma_{Odi}, \sigma_{Ldi}, \sigma_{Sdi}$  are the imaginary part of the standard deviations of normalized drift random noise in Equation (2.8), and *N()* represents a normal distribution. In Equation (2.12),  $\sigma_{Ov} = \sigma_{Lv} = \sigma_{Sv} = 0.4 mV$  since the normalized vertical noise for an averaging of 32 is 0.4mV (=0.1mV/0.25) in standard deviation from Figure 2.3. From Equation (2.8),

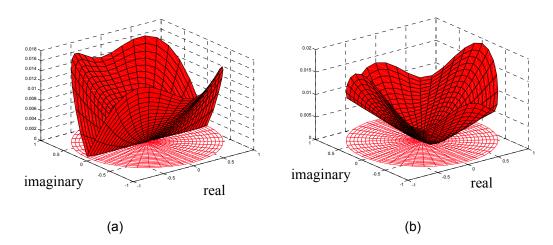
$$\sigma_{Odr} = \sigma_{Ldr} = \sigma_{Sdr} = \left|\frac{1}{2} [1 - \cos(2\pi \cdot f \cdot 1.5 \, ps)]\right|$$
(2.13)

$$\sigma_{Odi} = \sigma_{Ldi} = \sigma_{Sdi} = \left|\frac{1}{2} \cdot \sin(2\pi \cdot f \cdot 1.5 ps)\right|$$

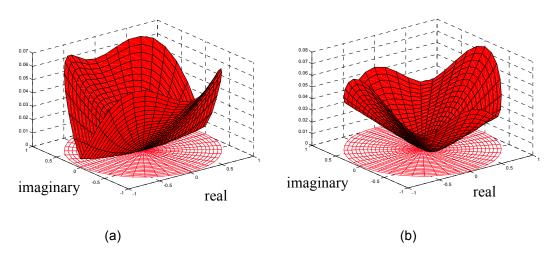
Then, the normalized vertical noise and the drift in Equation (2.13) can be generated and applied to Equation (2.6) and (2.7). The standard deviation of  $S_{11A}$  was statistically extracted, and the maximum uncertainty was assumed to be 2\*(the standard deviation of  $S_{11A}$ ). The maximum uncertainty at 50MHz, 2GHz, and 8GHz were statistically extracted with a drift of ± 1.5ps and a vertical random error of 0.1mV, and are shown in Figure 2.5, 2.6 and 2.7, respectively. From Figure 2.5, 2.6 and 2.7, the worst uncertainty occurs around the unit circle at each frequency. Based on Figure 2.5, 2.6 and 2.7, Figure 2.8 shows the absolute uncertainty of TDR measurements along the imaginary axis of the Smith chart. From Figure 2.8, the maximum absolute uncertainty of SOL calibration for TDR is 0.0026 at 50MHz, 0.02 at 2GHz and 0.075 at 8GHz for  $|S_{11M}| = 1$ . This uncertainty is lower than the uncertainty associated with a Vector Network Analyzer (VNA) at low frequencies, but higher at high frequencies. A Vector Network Analyzer has the absolute uncertainty of 0.02 at 50MHz, 0.026 at 2GHz and 0.043 at 20GHz for  $|S_{11M}|$  = 1 from [B4]. Below 2GHz, the uncertainty of TDR is lower than that of VNA. The uncertainty analysis shown was done for SOL calibration, with the uncertainty mainly caused by the drift in TDR measurements.



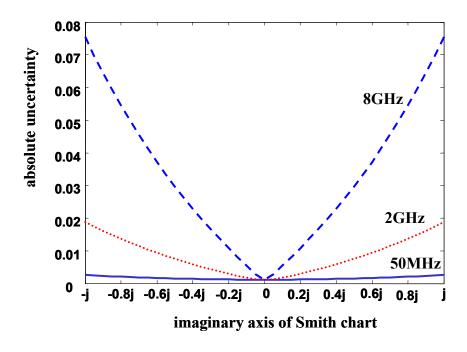
**Figure 2.5** Maximum uncertainty on the Smith chart at 50MHz for (a) the real part of measured impedance and (b) imaginary part of measured impedance.



**Figure 2.6** Maximum uncertainty on the Smith chart at 2GHz for (a) the real part of measured impedance and (b) imaginary part of measured impedance.



**Figure 2.7** Maximum uncertainty on the Smith chart at 8GHz for (a) the real part of measured impedance and (b) imaginary part of measured impedance.



**Figure 2.8** Maximum absolute uncertainty for the measured impedances along the imaginary axis of the Smith chart.

To reduce the uncertainty due to drift, an additional calibration structure (short or open transmission line) has been used in this dissertation. The additional structure reduces the uncertainty by  $\sim 15\%$  during TDR calibration.

#### 2.4.4. Repeatability and reproducibility

In the previous section, the effect of drift on the uncertainty of TDR measurements was discussed. However, there can be additional random error in the test system which arises from probe contacts. In order to ascertain the random variation of a measurement setup used, measuring the DUT many times provides statistical distribution due to random noise. There are two kinds of measurements for ascertaining the uncertainty of the test system used, which are repeatability and reproducibility. Repeatability is obtained by measuring a DUT many times over a short time period. Each measurement can be either done with a new calibration or with a previous calibration. The variation in the measurements shows the repeatability of the measurement setup used. Reproducibility shows the long-term variance of the test system used. For repeatability and reproducibility measurements, an open is the best structure to be measured [B5].

In this section, the repeatability of the TDR system used with a drift of  $\pm$  1.5ps was simulated using the signals shown in Figure 2.9.

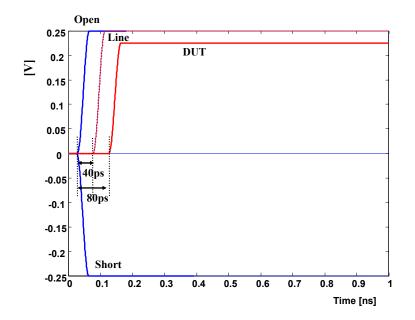


Figure 2.9 Simulated TDR signals for repeatability analysis of SOL calibration.

The DUT had a delay of 80ps compared to Open and Short calibration, and an exact frequency response from DC to 10GHz is plotted in Figure 2.10. After adding a random drift to each signal, the SOL calibration discussed above was applied to find the frequency response of the DUT. Then, the difference between the extracted results in the frequency domain is plotted in Figure 2.11. At 10GHz, the mean of the samples is 0.0502 and the standard deviation is 0.0283.

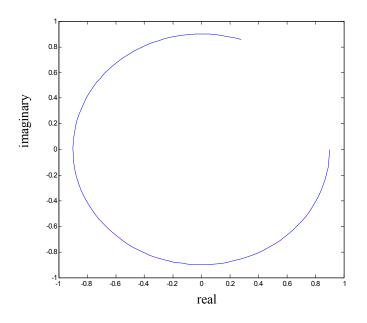


Figure 2.10 Exact frequency response of the DUT on Smith chart (DC~10GHz).

The random drift of TDR measurement induces two kinds of effect on the frequency response of the DUT. The first effect is the vertical movement of the calibrated frequency response on the Smith chart, which results in the response being outside the unit circle. The curves in Figure 2.11 show this effect. The second effect is an additional random delay to the DUT. The maximum uncertainty at each frequency in Figure 2.11 is determined by the maximum random delay since the uncertainty in Figure 2.11 represents the distance to the Smith chart response with random delay.

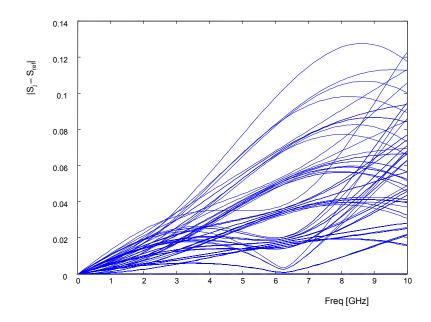


Figure 2.11 Simulated repeatability of TDR calibration for the DUT in Figure 2.9.

# 2.5. Short-Open-Load-Line (SOLL) Calibration for TDR

When TDR measurements are calibrated using SOL standards (Open-Short-Load), the reference planes of Open, Short and Load can be slightly different from each other due to the drift in TDR equipment. Hence, to reduce the error due to drift, an extra calibration structure is necessary in addition to SOL standards, as shown in Figure 2.12. The new calibration method in Figure 2.12 consists of Open-Short-Load-Line (SOLL) structures. The additional calibration structure, Line, is used to adjust the drift error between Open, Short and Load measurements, which can remove the vertical movement of the calibrated frequency response. Line can be a transmission line with 50 ohm characteristic impedance and finite length which is included in calibration standards for VNA. In Figure 2.12, after adjusting the delay of open, short and load using Line, the SOL calibration in Section 2.3.2 is applied to the DUT. However, the SOLL calibration still has a limitation. The random delay due to the drift in TDR measurements is still difficult to remove from the calibration response.

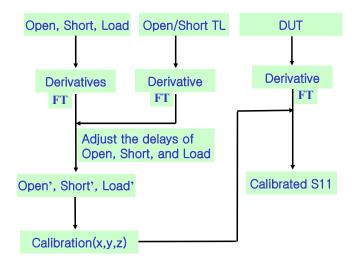


Figure 2.12 Short-Open-Load-Line (SOLL) calibration procedure.

The repeatability of the SOLL calibration was simulated using the signals in Figure 2.9 with an additional open-terminated line whose delay was 40ps compared to Open, as shown in Figure 2.13.

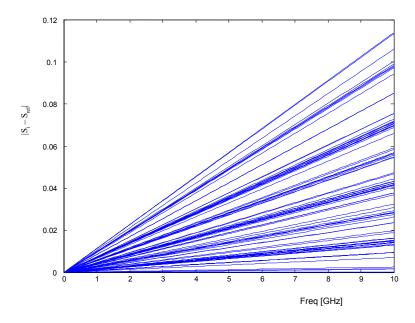


Figure 2.13 Simulated repeatability of SOLL calibration for the DUT in Figure 2.9.

Figure 2.13 shows that the vertical movement of the frequency response due to drift can be eliminated. At 10GHz, the mean of the samples was 0.0429, and the standard deviation was 0.0299. Using the SOLL calibration, ~15% of the uncertainty in Figure 2.11 was reduced.

The repeatability of the TDR system used was characterized by measuring a coplanar line with delay of 40ps on an Impedance Standard Substrate (101-190) from Cascade Microtech with the SOLL calibration. The frequency response is close to the response of the lossless line in Figure 2.10. Ten measurements for the coplanar line were performed at an interval of 5 minutes, and the difference between S-parameters were plotted, as shown in Figure 2.14. The curves in Figure 2.14 are similar to the curves in Figure 2.13, which implies that the main cause of the variance is drift in the TDR system.

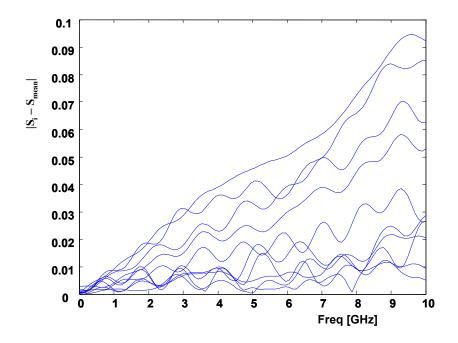
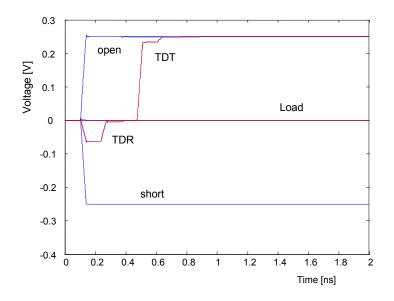


Figure 2.14 Measured repeatability of TDR system used for a 40ps delay line.

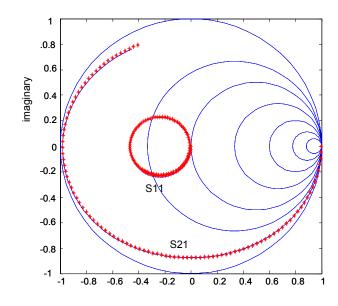
# 2.6. TDR/TDT calibration

In this section, the effect of drift in the TDR system on the uni-directional TDR/TDT calibration in Section 1.7.3.3 has been discussed [B6]. The drift of TDR used was  $\pm$  1.5 ps. TDR/TDT signals were first simulated using Hspice, as shown in Figure 2.15. The DUT is a transmission line with Z0=30 $\Omega$ ,  $\varepsilon r = 4$ ,  $\alpha = 2/(10*10^9)*f$  Np/m, and length = 0.01m, where  $\alpha$  is the attenuation constant and f is the frequency in Hertz. Using SOLT calibration explained in Section 1.7.3.3, the frequency response of the transmission line was extracted, as shown in Figure 2.16.

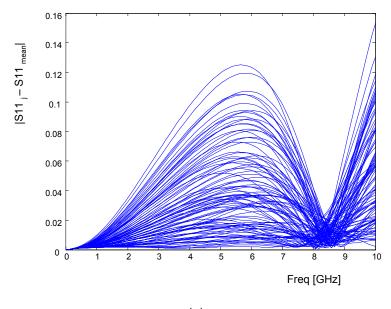
The repeatability of the TDR/TDT measurements due to a drift of  $\pm$  1.5ps is shown in Figure 2.17. Figure 2.17(a) shows the repeatability of S11 and Figure 2.17(b) shows the repeatability of S21. As shown in Figure 2.17, since S21 in Figure 2.16 is similar to Figure 2.10, the repeatability of S21 is similar to Figure 2.11. In addition, S11 and S21 have similar uncertainty.



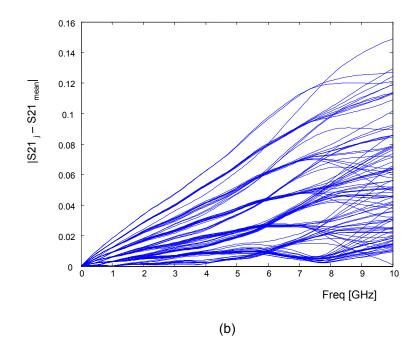
**Figure 2.15** Simulated TDR/TDT signals for a transmission line.



**Figure 2.16** Extracted S-parameters of the transmission line in Figure 2.31 using SOLT calibration (DC~10GHz).



(a)



**Figure 2.17** Simulated repeatability of uni-directional TDR/TDT calibration with a drift of  $\pm$  1.5ps for the transmission line in Figure 2.15. (a) S11 and (b) S21.

# 2.7. TDR characterization examples

In this section, the SOLL calibration has been applied for the characterization of inductors, capacitors and microwave filters to demonstrate the accuracy of the TDR measurements.

# 2.7.1. Inductors

The embedded one-loop inductor in Figure 2.18 was measured using the TDR, as shown in Figure 2.19. The inductor was patterned using a copper plane on a Dupont Vialux dielectric film with 1 mil thickness [B7]. The metal trace of the inductor had a width of 2 mils. In Figure 2.20, the extracted S-parameters from a Network Analyzer and TDR have been compared. The two results agree well with each other. The inductor had a resonant frequency of 3.6 GHz, Q of 80 at 2GHz and inductance of 10nH from NA measurements. Figure 2.21 shows the quality factor of the inductor. The quality factor is high from 1GHz to 2.5GHz, compared to on-chip inductors.

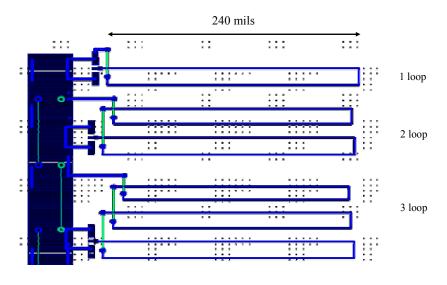


Figure 2.18 embedded inductors.

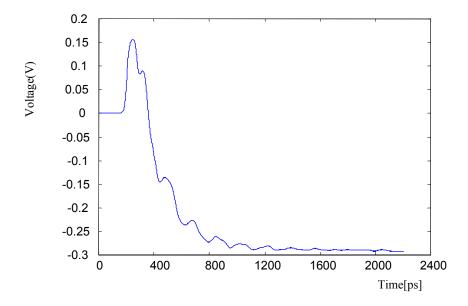


Figure 2.19 TDR measurement of the one-loop inductor in Figure 2.18.

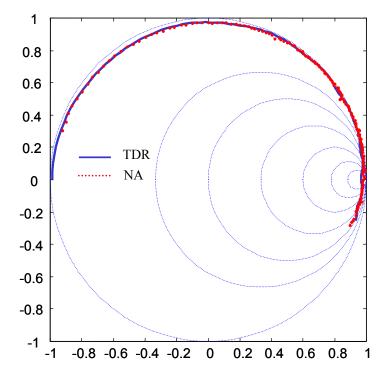


Figure 2.20 S-parameter (S11) of the inductor (DC~4.3GHz).

The following procedure was used for extracting the quality factor in Figure 2.21 from the TDR waveform in Figure 2.19. First, Open, Short, Load and Line standards were measured for SOLL calibration. Second, the inductor in Figure 2.18 was measured using the TDR, as shown in Figure 2.19. Then, the calibrated frequency-domain response in Figure 2.20 was extracted based on the TDR calibration in Figure 2.12. Finally, the quality factor was extracted using the rate of change of phase at resonance after attaching a known capacitance to the extracted inductor impedance [B8], as shown in Figure 2.21.

$$Q = \frac{\omega_0}{2} \frac{d\phi}{d\omega}$$
(2.14)

where  $\omega_0$  is a resonance frequency,  $\phi$  is the phase and Q is the quality factor. In Figure 2.22, the uncertainty of the extracted quality factor due to the random noise of the TDR equipment is shown. The extracted inductance was insensitive to random noise.

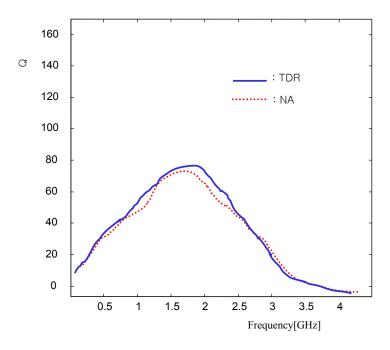


Figure 2.21 Quality factor of the inductor.

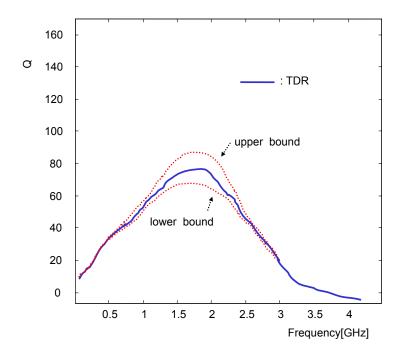


Figure 2.22 Uncertainty of the extracted quality factor of the inductor from TDR

measurement.

# 2.7.2. Capacitors

Figure 2.24 shows the TDR measurements of a capacitor. The capacitor was fabricated at the Packaging Research Center (PRC) using a high dielectric constant material developed at PRC [B9]. The thickness of the dielectric was 1mil and the diameter of the circular conductor was 0.6mm, as shown in Figure 2.23.



Figure 2.23 Capacitors fabricated at PRC.

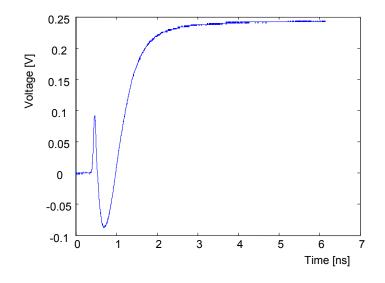


Figure 2.24 TDR measurement of a capacitor.

Figure 2.25 shows the extracted capacitance and quality factor of the capacitor from the TDR waveform in Figure 2.24. The following procedure was used for extracting the

capacitance and quality factor in Figure 2.25. First, Open, Short, Load and Line structures were measured for SOLL calibration. Second, the capacitor was measured using the TDR, as shown in Figure 2.24. Then, the calibrated frequency-domain response was extracted based on the TDR calibration in Figure 2.12. Finally, the capacitance and quality factor were extracted using the rate of change of phase at resonance, after attaching a known inductance to the extracted capacitor impedance [B8].

$$Q = \frac{\omega_0}{2} \frac{d\phi}{d\omega}\Big|_{\omega_0}$$
(2.15)

where  $\omega_0$  is the resonance frequency,  $\phi$  is the phase and Q is the quality factor. The effective capacitance was extracted from the resonance frequency since  $\omega_0=1/\sqrt{L\cdot C}$  where L is the known inductance. While the random noise of the TDR equipment did not induce any variation in the extracted capacitance, it caused a variation in the quality factor, as shown in Figure 2.25.

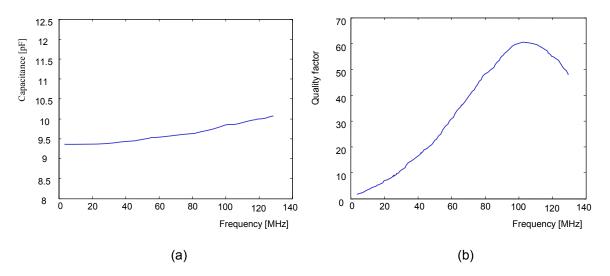


Figure 2.25 (a) Extracted capacitance and (b) quality factor of the capacitor.

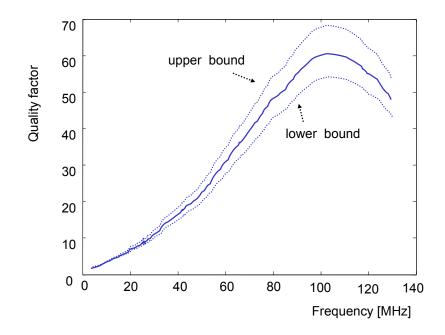


Figure 2.26 Uncertainty of the extracted quality factor of the capacitor from TDR measurements.

# 2.7.3. Microwave filters

A lowpass filter terminated with 50 ohm load, as shown in Figure 2.27, was measured using both TDR and a Network Analyzer (HP 8510C) up to 10GHz. The same calibration kit was used for both the measurements. Figure 2.28 shows the TDR measurements of the low pass filter. The sampling interval used was 0.4 ps with 5120 data points. Figure 2.29 compares the two results of NA and TDR for the lowpass filter showing good agreement. The random noise of the TDR equipment did not cause a significant variation on the Smith chart.



Figure 2.27 Lowpass filter circuits.

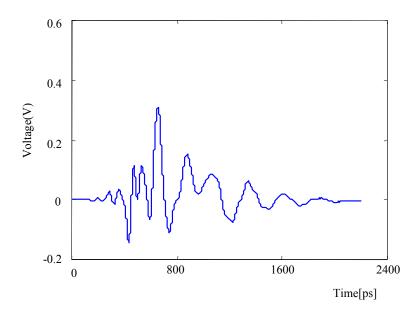


Figure 2.28 TDR measurement of the lowpass filters.

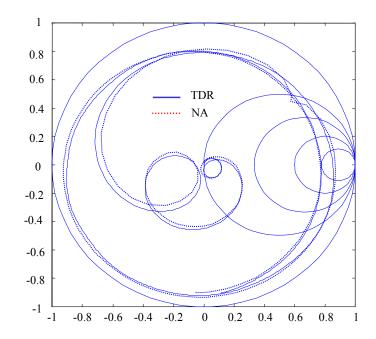


Figure 2.29 S-parameters (S11) of the lowpass filter (DC~10GHz)

# 2.8. Summary

In this chapter, the calibration method and error analysis of Short-Open-Load (SOL) calibration for TDR measurements was discussed. It was shown that the error or uncertainty of SOL calibration for TDR with  $\pm$ 1.5ps drift was lower than Network Analyzer uncertainty below 2GHz, but higher for frequencies greater than 2GHz. The maximum absolute uncertainty of SOL calibration for TDR was 0.0026 at 50MHz, 0.02 at 2GHz and 0.075 at 8GHz for  $|S_{11M}| = 1$ . Using a similar analysis, it was estimated that the Vector Network Analyzer has absolute uncertainty of 0.02 at 50MHz, 0.026 at 2GHz and 0.043 at 20GHz for  $|S_{11M}| = 1$ . To improve the accuracy, Short-Open-Load-Line (SOLL) calibration for TDR measurements was developed in this dissertation. The TDR calibration results were compared to Network Analyzer results for an inductor, capacitor and microwave filter. The results showed good agreement with network analyzer measurements. The TDR calibration method was applied for characterization of inductors and capacitors, yielding frequency-dependent capacitance, inductance and quality factor from TDR measurements.

# **Chapter 3**

# Characterization of Package Transmission Lines

In this chapter, a newly developed TDR characterization method for lossy transmission lines is discussed. The frequency-dependent characteristic impedance and propagation constant of lossy transmission lines are extracted from TDR measurements using the TDR calibration technique discussed in Chapter 2. For simulating the extracted characteristic impedance and propagation constant from TDR measurements, non-physical RLGC models for lossy transmission lines are derived from transient analysis. The results are evaluated through correlation with time-domain measurements. The effect of frequency-dependent characteristic impedance and propagation constant on digital signals is investigated. Based on the TDR characterization method and frequency-dependent effect, an in-situ characterization method for lossy transmission lines is proposed without requiring calibration, which is useful for practical applications. Package transmission lines fabricated on various dielectric materials at the Packaging Research Center (PRC) have been characterized using the methods discussed in this chapter.

# 3.1. Previous research on transmission line parameter extraction

Historically, William Thomson and Oliver Heaviside were the pioneers for transmission-line research in the 19<sup>th</sup> century. The first distributed analysis of transmission lines was performed by William Thomson in 1855 [C1]. Transatlantic cables from Ireland and Newfoundland were analyzed as distributed RC circuits. In the 1880s, Oliver Heaviside developed the transmission line theory using the distributed RLGC circuits [C2]. For extracting the RLGC parameters of transmission lines, William Thomson and Oliver Heaviside used the definition that 'R' is the per-unit-length loss due to conductor, 'L' is the per-unit-length inductance of transmission line, 'G' is the per-unit-length loss due to dielectric, and 'C' is the per-unit-length capacitance of transmission line [C3]. The parameters,' L' and 'C' were calculated using Maxwell's equations. In the early 1900s, considerable effort was expended in calculating 'R' [C4][C5], and the extraction of skin effect resistance was intensively studied.

From the 1950s, researchers have tried to solve Maxwell's equations for transmission line structures. The mathematical method used has been based on the conformal mapping technique for two-dimensional geometries [C6]. The conformal mapping technique that yields the characteristic impedance of transmission lines has been applied to striplines, microstrip-lines and coplanar-lines. Since the methods developed are based on the physical structure of the transmission lines, the extracted RLGC models have been categorized as 'physical RLGC models' in this dissertation.

In 1993, Y. Eo and W. R. Eisenstadt published a method for obtaining the frequencydependent characteristic impedance and propagation constant from the S-parameters of transmission lines using a simple pad de-embedding technique [C7]. Advanced techniques taking the more complex pad transitions into account were thereafter published for extracting the frequency-dependent characteristic impedance from Network Analyzer measurements using accurate de-embedding techniques [C8] ~ [C13].

66

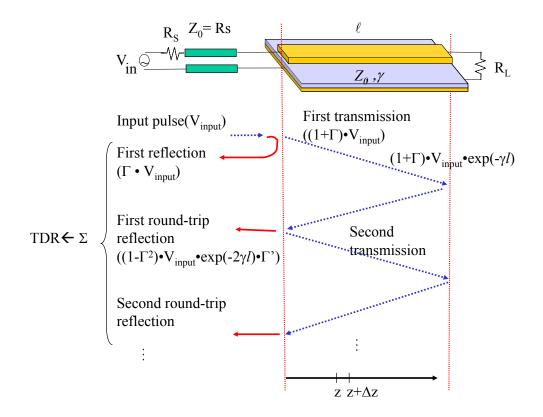
However, these methods still have limitations. These methods are applicable to pad transitions with small parasitics such as on-wafer measurements. While the extraction of characteristic impedance is possible only for small pad parasitics, the extraction of the propagation constant is mathematically possible for any pad transition from two-line measurements [C14]. Using the measured characteristic impedance and propagation constant from Network Analyzer measurements, frequency-dependent RLGC parameters have been obtained [C7].

Characterization of transmission lines using TDR/TDT measurements has been studied since the 1990s, using different calibration methods, the layer peeling algorithm and the macro-modeling technique explained in Chapter 1. Techniques using short pulses have been also studied since the 1990s for characterizing transmission lines [C15]. In this dissertation, a TDR characterization method for lossy transmission lines has been introduced, for extracting the frequency-dependent characteristic impedance and propagation constant.

# 3.2. Transient behavior of transmission lines

The new characterization method has been developed based on the transient behavior of transmission lines. The transient behavior of transmission lines is shown through a reflection diagram in Figure 3.1. In the figure, the first reflection from the near end of the transmission line provides information on the characteristic impedance, while the first round-trip reflection from the far end provides information on the propagation constant. Through time-windowing, these waveforms can be used to extract the frequency-dependent characteristic impedance and propagation constant of lossy transmission lines. In Figure 3.1, the Time Domain Reflectometry (TDR) waveform includes all the reflections from the near and far end. The various parameters used in the figure have been discussed in the relevant sections in this chapter.

67



**Figure 3.1** Reflection diagram of lossy transmission line. Rs is the source resistance, Z0 is the characteristic impedance,  $\gamma$  is the propagation constant, RL is the load resistance, *I* is the length,  $\Gamma$  is the near end reflection coefficient, and  $\Gamma$ ' is the far end reflection coefficient.

The measured TDR waveforms of lossy transmission lines with a short and open termination are shown in Figure 3.2. The measured transmission lines were coplanar lines with 5cm length, and the dimensions are as shown in Figure 3.3. As shown in the figure, the first reflection and round-trip reflection can be separated using time windowing if the length of the transmission line is long compared to the rise time and fall time of the signal. Through time windowing and signal processing methods, the characteristic impedance and propagation constant of the transmission lines are extracted in this chapter. The details are provided in the following sections.

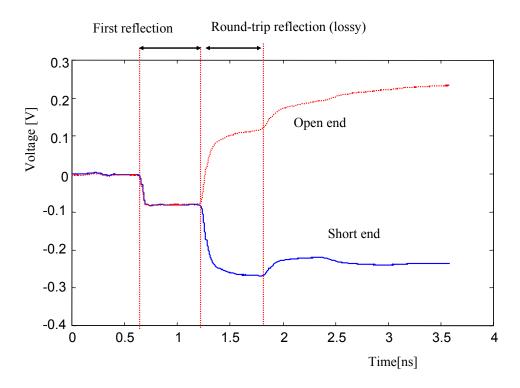


Figure 3.2 TDR measurements of lossy transmission lines.

# 3.3. Extraction of the frequency-dependent characteristic impedance and propagation constant using TDR measurements

In this section, using TDR measurements on a co-planar line, the frequencydependent characteristic impedance and propagation constant are extracted. Though the method has been applied to a co-planar line, the method is generic and can be applied to any transmission line structure.

# 3.3.1. Test structure: Co-planar Lines

The dimensions of a co-planar line fabricated on an organic substrate at the PRC are shown in Figure 3.3. The width and thickness of the center conductor are 5 mils and 1 mil, respectively. The gaps between the center conductor and ground conductors are 3 mils. The structure consists of a metal plane with 9 um thickness on the bottom layer with a dielectric of  $\varepsilon_r$  = 3.8, loss tangent = 0.02, and thickness of 1 mil. The ground conductor of the co-planar line were not connected to the bottom-side metal plane.

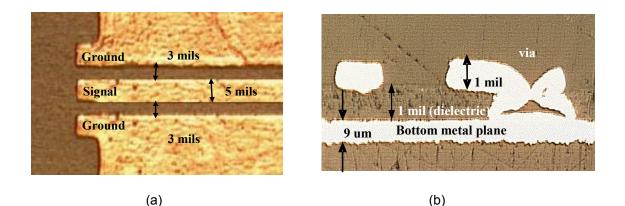


Figure 3.3 Coplanar lines on organic Substrate. (a) top view and (b) cross-section.

# 3.3.2. Extraction of frequency-dependent characteristic impedance

In TDR measurements, the first reflection in Figure 3.1 is caused by the characteristic impedance of the transmission line. Since the first reflection does not contain reflections from the far end, this measurement is equivalent to the response of a lossy transmission line of infinite length in the steady state. Hence, the input impedance calculated from the first reflection is the characteristic impedance of the transmission line. The characteristic impedance can therefore be calculated using the relation

$$\Gamma = \frac{Z_0 - R_s}{Z_0 + R_s} \tag{3.1}$$

where  $\Gamma$  is the measured near-end reflection coefficient, Z<sub>0</sub> is the characteristic impedance and R<sub>s</sub> is the source impedance of the TDR equipment. From Figure 3.2, only the first reflection is captured by using time windowing on the TDR waveform. Then, the first reflection is converted to the frequency domain using the TDR calibration method described in Chapter 2. This is the frequency-domain reflection coefficient which includes the pad parasitics of the transmission line. Using the de-embedding procedure described in Section 3.3.2.1 for removing pad parasitics, the frequency-dependent characteristic impedance of the co-planar line has been extracted, as shown in Figure 3.4.

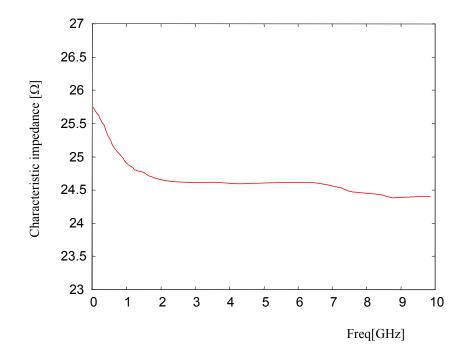


Figure 3.4 Extracted frequency-dependent characteristic impedance of the coplanar line.

# 3.3.2.1. Pad de-embedding for extracting the characteristic impedance

When SMA connectors or pads for probes are used to connect transmission lines to TDR equipment, parasitic inductances and capacitances in the transitions affect the extracted characteristic impedance in the RF frequency range. Hence, de-embedding of the pad transitions from the overall response is necessary. In this dissertation, a model based on the physical structure of the pads has been used. The advantage of this model is that the de-embedding problem becomes a one-variable optimization problem on the Smith Chart, which makes the method reliable.

Figure 3.5 shows the physical modeling of the pads and vias for a microstrip line. A capacitor between the two pads, a capacitor between the center pad and the ground plane, and an inductor for vias are the parasitic components in the transition. Since all these parasitic components are lumped in the model, the valid frequency range for this model is ~ 15GHz for typical pad dimensions. Above this frequency, the model is invalid due to the distributed transmission line effects. Since large pads and vias add large discontinuities, smaller pads and vias are preferred for obtaining a larger bandwidth in the frequency response. It is important to note that the extracted pad parasitics L, C1, and C2 in Figure 3.5(b) are frequency dependent parameters.

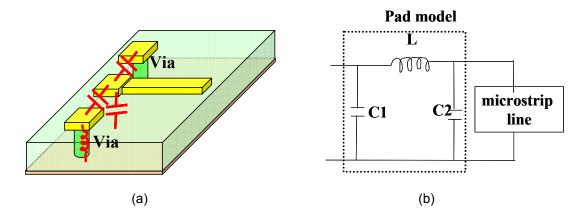


Figure 3.5 Pad modeling. (a) physical structure (b) physical pad model.

To extract the frequency dependent values for the pad parasitics, the behavior of the pad transition model on the Smith Chart was first investigated at a given frequency. The characteristic impedance of the transmission line is plotted as (P1) on the Smith Chart in Figure 3.6. The capacitance, C2 rotates the point (P1) downward to (P2) along the circle determined by the characteristic impedance. Inductance L rotates the point (P2) to (P3)

along the circle shown in Figure 3.6. If the point (P4) is on the left side of the point (P3), point (P3) is chosen as the lower point of the two points where the two circles, the L circle and C1 circle, meet. Finally, capacitance C1 rotates the point (P3) to the measurement point (P4) along the circle determined by the measurement impedance at the given frequency. On the Smith chart, the only unknown variable is the circle related to the inductance L that needs to be determined. Since this is a one-variable minimization problem, the results are repeatable.

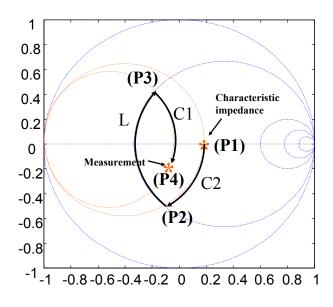


Figure 3.6 Pad transition on Smith Chart.

Since the characteristic impedance varies with frequency, the characteristic impedance at a frequency, for example 10MHz, can be assumed to be the same as the characteristic impedance at DC, which is displayed on the TDR instrument in the steady state. In addition, the parasitics, C1, L and C2 at low frequency also do not vary rapidly since the values are based on physical dimensions. From the characteristic impedance at 10MHz (P1) and the measurement at 10MHz (P4), the parasitics, C1, L, and C2 can be determined by minimizing the norm of the error between the measured and simulated

values at the next frequency. The simulated values are based on the C1, L, C2, and characteristic impedance values calculated at the previous frequency. The algorithm is based on a leap-frog scheme which leads to good results. To ensure that the extracted characteristic impedance and parasitics, C1, L, and C2 are repeatable, the same procedure was repeated with the simulated data generated from the extracted values. This produced the same values as the original results. For the co-planar line in Figure 3.3, the extracted values were L=0.1nH, C1 = 0.2pF and C2=0.2pF. The maximum frequency at which this physical de-embedding technique is valid depends on the physical dimensions of the pad transitions. As a rule of thumb, the maximum frequency is ~7 GHz and is >10GHz for 300 um length pad transitions [C16]. The pad transition in the transmission lines without pads makes the lumped pad model valid at frequencies greater than 20GHz.

#### 3.3.2.2. Real characteristic impedance

In [C17], the complex characteristic impedance of microstrip lines on silicon substrate has been extracted using VNA measurements. Unlike the results in [C17], the extracted characteristic impedance in Figure 3.4 is real. This difference has been explained through an example in Section 3.5 by comparing the results obtained from VNA measurements and TDR measurements. It is important to note that the primary goal of this dissertation is the simulation of digital signals propagating on lossy transmission lines using the extracted models.

The real characteristic impedance for package transmission lines can be explained through a physics based interpretation as well. Consider Figure 3.7 where the source impedance Rs in Figure 3.1 has been replaced by a lossless transmission line with characteristic impedance Rs and metal cross-section similar to the transmission line

74

being measured. Figure 3.7 represents the near end of the transmission line in Figure 3.1. In Figure 3.7, Z0 is the characteristic impedance of the transmission line to be measured which has a dielectric with permittivity  $\varepsilon$ 1, permeability  $\mu$ 1 and conductivity  $\sigma$ 1. The current and voltage just inside the transmission line at the interface are I1 and V1, as shown in the figure.

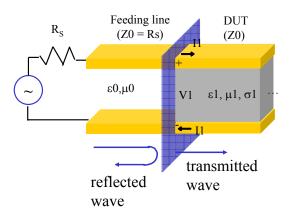


Figure 3.7 Structure at the near end of Figure 3.1.

If the length of the transmission line is infinite and attenuation constant is finite, the characteristic impedance of the DUT transmission line can be calculated as:

$$Z_0 = \frac{I1}{V1}$$
(3.2)

From Equation (3.2), if the phase of Z0 is zero, the transmission line has real characteristic impedance. In transmission lines, the current density  $\vec{j}$  and electric field  $\vec{E}$  are orthogonal to each other for Transverse Electromagnetic (TEM) waves. Since  $\vec{E} \cdot \vec{j} = 0$ , there is no energy dissipation by the electric field in the conductors. However, the currents induced by the coupled magnetic field dissipate energy due to the finite conductivity of the conductors. Since the first reflection in Figure 3.1 occurs at the

interface between the source and DUT transmission line, this signal is affected only by the dielectric loss because the conductor loss due to currents induced by the coupled magnetic field is zero. This can be attributed to the zero distance that the current travels along the vertical plane at the interface between the two transmission lines. Hence, the phase of the characteristic impedance can be related to the dielectric properties at the interface as:

$$phase(Z_{0}) = \pm phase(\eta_{1})$$

$$= \pm phase(\sqrt{\frac{\mu_{1}}{\varepsilon_{1}(1-j\tan\delta)}})$$

$$= \pm \frac{1}{2}\tan^{-1}(\tan\delta)$$
(3.3)

where  $\eta 1$  is the intrinsic impedance of the dielectric,  $\mu 1$  is the permeability,  $\epsilon 1$  is the permittivity,  $\sigma 1$  is the conductivity, and tan $\delta$  is the loss tangent of the dielectric. When the frequency variation of the real part of Z0 increases with frequency, the phase of Z0 has a positive sign. If the real part of Z0 decreases with frequency, the phase of Z0 has a negative sign.

Assuming a TEM mode for FR-4 with  $\varepsilon 1 = 4.0$  and  $\tan \delta = 0.02$ , the characteristic impedance has a phase angle of -0.572 degree. This is very small and hence for most package materials with  $\tan \delta \le 0.05$ , the phase of the characteristic impedance can be assumed zero without any loss in accuracy, especially for transmission lines supporting digital signals. Thus the characteristic impedance extracted in Figure 3.4 can be approximated as a real quantity.

# 3.2.2.3. Error/Uncertainty bound for the extracted characteristic impedance

The frequency-dependent characteristic impedance in Figure 3.4 extracted from TDR measurements has an uncertainty due to random noise, as explained in Chapter 2. The

error bound for the extracted characteristic impedance is shown in Figure 3.8 due to random noise. The uncertainty boundaries in the figure were extracted using the error analysis in Section 2.4 with a drift of  $\pm$  1.5ps for TDR equipment.

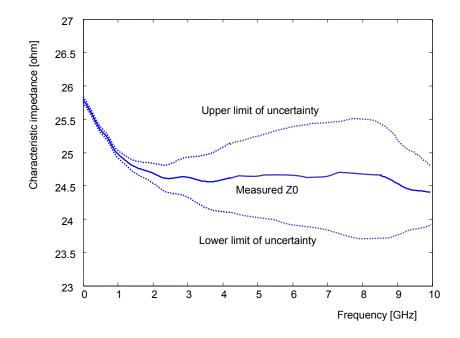


Figure 3.8 Error/Uncertainty bound of the extracted characteristic impedance.

As shown in Figure 3.8, at low frequencies below ~2GHz, the extracted characteristic impedance has a small uncertainty, while it has a large variation at frequencies above ~2GHz. From Figure 3.8, at 5Ghz, the measured characteristic impedance is 24.5  $\Omega$  with  $\pm 0.5 \Omega$  of uncertainty.

# 3.3.3. Extraction of frequency-dependent propagation constant

For measuring the propagation constant of the co-planar line, two co-planar lines with different lengths and the same cross-section were measured, as shown in Figure 3.9. The ends of the two lines were terminated to ground. The lengths of transmission lines were 1938 mils and 2242 mils. For extracting the propagation constant, the total

reflection coefficient of the two lines seen from the near end needs to be determined using the TDR calibration procedure discussed in Chapter 2. The total input reflection coefficient can be computed using the frequency-dependent characteristic impedance in Figure 3.4 after de-embedding the pad parasitics for the two lines in Figure 3.9.

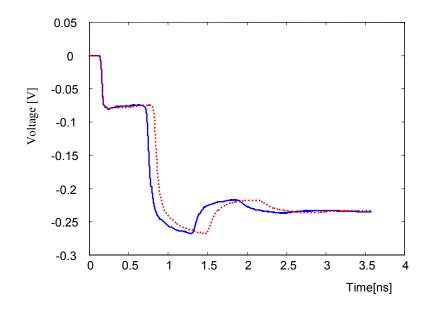


Figure 3.9 Two line TDR measurements for extracting propagation constant.

The total input reflection coefficient can be expressed as:

$$\Gamma_1 = \Gamma_L e^{-2\varkappa_1}$$

$$\Gamma_2 = \Gamma_L e^{-2\varkappa_2}$$
(3.4)

where  $\Gamma_1$  and  $\Gamma_2$  are the steady-state input reflection coefficients of the short and long lines, respectively. In the above equation,  $\Gamma_L$  is the reflection coefficient of the transmission line with the load,  $\gamma$  is the propagation constant and  $I_1$ ,  $I_2$  are the lengths of the transmission lines. Dividing the two input reflection coefficients, results in the propagation constant:

$$\gamma = \frac{1}{-2(l_2 - l_1)} \ln(\frac{\Gamma_2}{\Gamma_1})$$
(3.5)

Using Equation (3.5), the propagation constant of the transmission line can be extracted as shown in Figure 3.10 without de-embedding the termination at the far end of the transmission line. Although Equation (3.5) is not related to the termination, a short termination is preferable to an open termination. Since the Smith Chart is more sensitive around the short than the open, small differences in impedance around the short can be captured effectively using the TDR measurements.

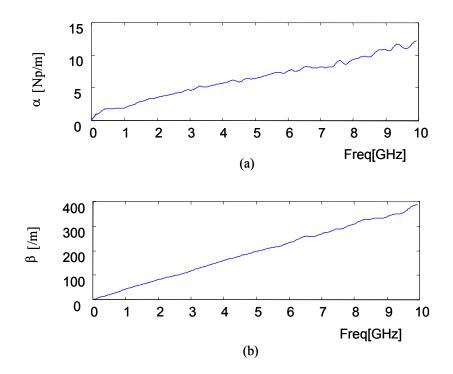


Figure 3.10 Extracted propagation constant of the coplanar line.

(a) attenuation constant and (b) propagation constant.

#### 3.3.3.1. Importance of the static resistance of transmission lines

When using the extracted data for simulating digital signals, the DC attenuation constant should be carefully handled. The steady-state input impedance seen from the near end of the DUT transmission line in Figure 3.1 can be expressed as:

$$Z_{in} = Z_0 \frac{R_L + Z_0 \tanh(\gamma \cdot l)}{Z_0 + R_L \tanh(\gamma \cdot l)}$$
(3.6)

where  $Z_0$  is the characteristic impedance,  $\gamma$  is the propagation constant,  $R_L$  is the load, and *I* is the length of the transmission line. Since the input impedance at DC should equal the static input resistance, Equation (3.6) becomes:

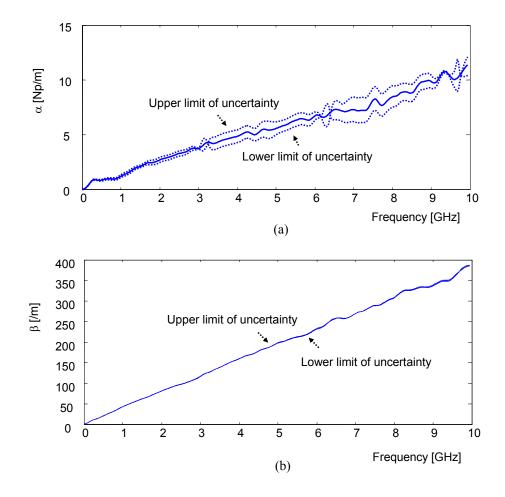
$$Z_{in}(DC) = Z_0(f \to 0) \cdot \frac{R_L + Z_0(f \to 0) \cdot \tanh(\alpha_{DC} \cdot l)}{Z_0(f \to 0) + R_L \cdot \tanh(\alpha_{DC} \cdot l)} = R_{DC} + R_L$$
(3.7)

where  $Z_{in}(DC)$  is the input impedance at DC,  $Z_0(f \rightarrow 0)$  is the low frequency characteristic impedance,  $\alpha_{DC}$  is the attenuation constant at DC, and  $R_{DC}$  is the DC resistance of the transmission line. If  $R_{DC} = 0$  in Equation (3.7), then  $\alpha_{DC} = 0$  independently of  $R_L$ . However, if  $R_{DC} \neq 0$ , then  $\alpha_{DC}$  needs to be approximated in Equation (3.6). To satisfy Equation (3.7) for any  $R_L$  and  $R_{DC}$ , a series resistance  $R_{DC}$  has been added at the far end of the transmission line after setting  $\alpha_{DC} = 0$  in this dissertation. Since the added resistance  $R_{DC}$  has a small value compared to the load resistance  $R_L$  in most of the applications, error induced by  $R_{DC}$  can be considered to be negligible.

# 3.3.3.2. Error/uncertainty bound of extracted propagation constant

The frequency-dependent propagation constant in Figure 3.10 extracted from TDR measurements also has an uncertainty due to random noise, as explained in Chapter 2. The error bound for the extracted propagation constant is shown in Figure 3.11 due to

random noise. At frequencies below ~2GHz, the extracted attenuation constant in Figure 3.11(a) has a small uncertainty, while it has a large variation at frequencies above ~2GHz. However, the uncertainty bound for the imaginary propagation constant in Figure 3.11(b) is small. Hence, the imaginary propagation constant is not prone to variations due to random noise. From Figure 3.11, the extracted attenuation constant at 5Ghz is 5.5 Np/m with an uncertainty of  $\pm$  0.5 Np/m. The uncertainty bounds were estimated using the error analysis for TDR in Section 2.4.



**Figure 3.11** Error/uncertainty bound of extracted propagation constant. (a) attenuation constant and (b) propagation constant.

# 3.4. Non-physical transmission line models-Theory and extraction

Non-physical RLGC models for transmission lines were developed to simulate the extracted characteristic impedance and propagation constant in the following sections. For the development of transmission line models from the extracted characteristic impedance and propagation constant, non-physical RLGC models for lossy transmission lines have been derived in this section. Non-physical RLGC models have been developed from the transient analysis of transmission lines, as shown in Figure 3.1.

Consider the reflection diagram in Figure 3.1. Summing all the signals propagating in the +z and -z direction at a point z along the transmission line yields the steady-state voltage V<sup>+</sup>(z) and V<sup>-</sup>(z), respectively, which can be expressed as :

$$V^{+}(z) = V_{0}^{+} e^{-\gamma z}$$

$$V^{-}(z) = V_{0}^{-} e^{\gamma z} = V_{0}^{+} \Gamma' e^{-2\gamma t} e^{\gamma z}$$
(3.8)

where  $V_0^+$  is the amplitude of V<sup>+</sup>(z),  $\Gamma'$  is the far-end reflection coefficient,  $\gamma$  is the propagation constant and *I* is the length of the transmission line. From Equation (3.8), the voltage and current at 'z' in the steady state are:

$$V(z) = V^{+}(z) + V^{-}(z) = V_{0}^{+} e^{-\gamma z} + V_{0}^{+} \Gamma' e^{-2\gamma t} e^{\gamma z}$$

$$I(z) = I^{+}(z) + I^{-}(z) = \frac{V_{0}^{+}}{Z_{0}} e^{-rz} - \frac{V_{0}^{+} \Gamma' e^{-2\gamma t}}{Z_{0}} e^{\gamma z}$$
(3.9)

For a small length  $\Delta z$  of the transmission line, let the voltage and current at 'z' be V1 and I1, respectively and the voltage and current at 'z+ $\Delta z$ ' be V2 and I2 respectively.

Then,

$$V_{1} = V_{0}^{+} e^{-\gamma z} + V_{0}^{+} \Gamma' e^{-2\gamma t} e^{\gamma z}$$

$$I_{1} = \frac{V_{0}^{+}}{Z_{0}} e^{-rz} - \frac{V_{0}^{+} \Gamma' e^{-2\gamma t}}{Z_{0}} e^{\gamma z}$$

$$V_{2} = V_{0}^{+} e^{-\gamma (z + \Delta z)} + V_{0}^{+} \Gamma' e^{-2\gamma t} e^{\gamma (z + \Delta z)}$$

$$I_{2} = \frac{V_{0}^{+}}{Z_{0}} e^{-r(z + \Delta z)} - \frac{V_{0}^{+} \Gamma' e^{-2\gamma t}}{Z_{0}} e^{\gamma (z + \Delta z)}$$
(3.10)

Based on Equation (3.10), the equivalent circuit for a length  $\Delta z$  can be constructed, as shown in Figure 3.12.

Using circuit theory, the voltages and currents in Figure 3.12(a) can be expressed as:

$$V_{2} = V_{1} - X * I_{1}$$

$$I_{2} = I_{1} - Y * V_{2} = (1 + X * Y) * I_{1} - Y * V_{1}$$
(3.11)

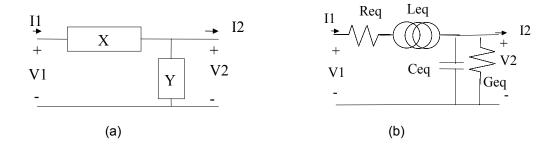


Figure 3.12 RLGC models for transmission lines.

Combining Equation (3.11) and (3.12) results in,

$$V_{2} = V_{1} - X * I_{1} = V_{0}^{+} (1 - \frac{X}{Z_{0}}) e^{-\gamma z} + V_{0}^{+} (1 + \frac{X}{Z_{0}}) \Gamma' e^{-2\gamma t} e^{\gamma z}$$

$$I_{2} = (1 + X * Y) * I_{1} - Y * V_{1} = (\frac{1 + X * Y}{Z_{0}} - Y) V_{0}^{+} e^{-\gamma z} - (\frac{1 + X * Y}{Z_{0}} + Y) V_{0}^{+} \Gamma' e^{-2\gamma t} e^{\gamma z}$$
(3.12)

Since Equation (3.12) and (3.10) should be identical, the conditions to be satisfied are:

$$e^{-\gamma\Delta z} = (1 - X / Z_0)$$

$$e^{\gamma\Delta z} = (1 + X / Z_0)$$
(3.13)
$$e^{-\gamma\Delta z} = (1 + X * Y - Z_0 * Y)$$

$$e^{\gamma\Delta z} = (1 + X * Y + Z_0 * Y)$$

Since there exists no unique solution for X and Y in Equation (3.13), an approximate solution can be obtained using the following approximation.

 $e^{-\gamma\Delta z} \approx 1 - \gamma\Delta z, \qquad e^{\gamma\Delta z} \approx 1 + \gamma\Delta z \qquad if \qquad \gamma\Delta z \approx 0$  (3.14)

Then, the per-unit-length parameters X and Y can be derived as:

$$X = Z_0 \gamma$$
(3.15)  
$$Y = \gamma / Z_0$$

From Equation (3.15), the non-physical RLGC parameters can now be derived as:

$$R eq = \operatorname{Re}(X)$$

$$Leq = \operatorname{Im}(X) / \omega \qquad (3.16)$$

$$Geq = \operatorname{Re}(Y)$$

$$Ceq = \operatorname{Im}(Y) / \omega$$

Since non-physical RLGC models represent the transient behavior of TEM waves on transmission lines, the inductance and capacitance of Equation (3.16) must be the same as the physical RLGC models, based on Maxwell's equations. Using the definition of phase velocity of transmission lines, the characteristic impedance can be derived as:

$$V_{p} = \frac{1}{\sqrt{L_{physical}C_{physical}}}, \quad Z_{0} = \sqrt{\frac{L_{physical}}{C_{physical}}}$$
(3.17)

where  $V_p$  is the phase velocity, and  $L_{physical}$  and  $C_{physical}$  are the physical inductance and capacitance of the transmission line, respectively. Combining Equation (3.16) and (3.17) yields:

$$R \ eq = Z_0 \alpha$$

$$Leq = L_{physical}$$

$$Geq = \frac{\alpha}{Z_0}$$

$$Ceq = C_{physical}$$
(3.18)

From Equation (3.18), it is important to note that  $R_{eq}$  and  $G_{eq}$  are dependent parameters, unlike the physical RLGC models. This is the primary difference between the models derived in this dissertation compared to the RLGC models used extensively in the literature. Hence, the RLGC models in Equation (3.18) are called 'non-physical RLGC models.' This difference can have a substantial effect for long lossy transmission lines used for digital applications.

#### 3.5. Time-domain model-to-hardware correlation

To verify the accuracy of the non-physical RLGC models and extracted data from TDR measurements, a comparison between simulation and measurement was conducted. Three kinds of transmission-line models were simulated for correlation with TDR measurements namely, 1) non-physical RLGC models extracted from TDR measurements, 2) RLGC models extracted from NA measurements, and 3) physical RLGC models extracted from a 2D parameter extractor.

# 3.5.1. Non-physical RLGC models

Using the extracted data for Z0 and  $\gamma$  in Figure 3.4 and 3.10, the coplanar line in Section 3.3 was simulated using the non-physical RLGC parameters in Equation (3.18). To minimize error due to noise, the characteristic impedance extracted in Figure 3.4 was approximated using an exponential function. Similarly, the real and imaginary values of the propagation constant in Figure 3.10 were approximated as a linear function of *f* 

85

and  $\sqrt{f}$ . The approximated characteristic impedance and propagation constant are as shown below:

Z0 = 1\*exp(-f/0.8e9)+24.7 ohms  

$$\alpha$$
 = 8/10e9\*f + 4/sqrt(10e9)\*sqrt(f) Np/m (3.19)  
 $\beta$  = 2 $\pi$  f/3e8\*sqrt(3.1611) /m

Since the step pulse response is dominated by the low frequency response after the rising part of the step pulse, the step pulse response should approach the DC resistance of the transmission line in the steady state. However, since  $\sqrt{f}$  behavior of the attenuation constant has a time-domain response with a long settling time, the step pulse response does not approach the DC resistance in the steady state with  $\sqrt{f}$  behavior. Hence, for improving the low-frequency behavior, the attenuation constant has been approximated using the following function:

$$\alpha = \frac{8}{10e9} \cdot f + \frac{4}{\sqrt{10e9}} \sqrt{f} \approx \frac{8}{10e9} \cdot f + 4 \cdot [0.3 \cdot erf(\frac{f}{0.6e9}) + \frac{0.8}{10e9} f]$$
(3.20)

where *erf* is the error function. These functions were then used to extract the nonphysical RLGC parameters as shown below:

$$R = 25.7 \cdot [8/10e9 \cdot f + 4/\sqrt{10e9} \cdot \sqrt{f}] \text{ ohm/m}$$

$$L = 152.3 \text{ nH /m}$$

$$G = [8/10e9 \cdot f + 4/\sqrt{10e9} \cdot \sqrt{f}]/25.7 \text{ S/m}$$

$$C = 230.6 \text{ pF/m}$$
(3.21)

The non-physical RLGC parameters were simulated in Hspice using the W-element tabular model for transmission lines [C18]. The static resistance of the transmission line

was  $0.1\Omega$ , the length of the transmission line was 5cm and the far end of the transmission line was connected to ground.

#### 3.5.2. Physical RLGC models

For comparison, RLGC parameters were also extracted from the physical crosssection of the line using a 2-D parameter extractor available in Hspice [C18]. The extracted RLGC parameters are as shown below:

 $R = 5.468 + 2.11263e-3 * \sqrt{f} \text{ ohm /m}$  L = 149.782 nH /m(3.22) G = 1.39453e-11 \* f S/m

C = 221.947 pF/m

As can be seen from the extracted parameters, this simulation assumes ' $\sqrt{f}$ , ' dependence for R and 'f' dependence for G, which are well known approximations for frequency-dependent conductor and dielectric loss, respectively. In addition, the conductance 'G' at DC approaches zero in Equation (3.22). Since non-physical RLGC models represent the transient behavior of TEM waves in transmission lines, the inductance and capacitance of Equation (3.21) are close to those of physical RLGC models in Equation (3.22).

#### 3.5.3. RLGC models extracted from NA measurements

Finally, the complex characteristic impedance and propagation constant in Figure 3.13 and 3.14 were extracted from Network Analyzer measurements using the two-line measurement method [C14][C17]. These were also simulated using the W-element Tabular model in Hspice [C18] after extracting the RLGC parameters. The RLGC parameter extraction was based on the method used in [C7] where the RLGC parameters were extracted using equations similar to Equation (3.15) and (3.16). The Network Analyzer measurements were done in the frequency range from 50MHz to

87

10GHz. As explained in Chapter 1, the low frequency behavior from DC to 50MHz is very important in digital simulations. In this example, the frequency range from DC to 50MHz was extrapolated using the slope at 50MHz for both the characteristic impedance and propagation constant. For the frequency range from 10GHz to  $\infty$ , the slope at 10GHz was extrapolated both for the characteristic impedance and propagation constant.

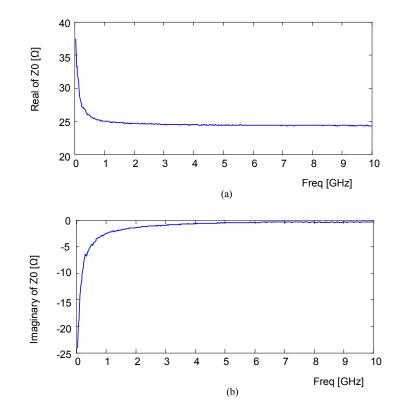


Figure 3.13 Characteristic impedance of the coplanar line extracted from NA measurements.

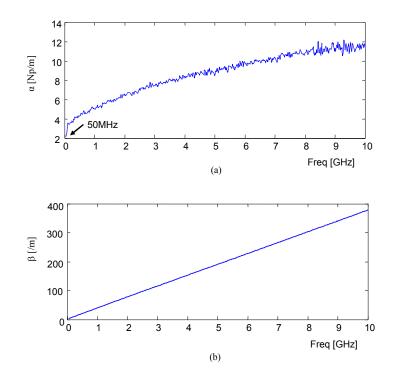


Figure 3.14 Propagation constant of the coplanar line extracted from VNA measurements.

# 3.5.4. Comparison between simulation and measurement

The time domain simulations using the three models have been compared with TDR measurements for the coplanar line discussed earlier. As can be seen in Figure 3.15, the non-physical RLGC model provides the best correlation with measurements. The physical RLGC model has some error, while the model extracted from VNA measurements shows the largest discrepancy. Since the propagation constant results are similar for TDR and VNA measurements, the primary reason for the discrepancy can be attributed to the difference in characteristic impedance at low frequencies.

Based on the results in Figure 3.15, the large variation in impedance at low frequency from VNA measurements results in an incorrect settling value for the voltage waveform. However, in the extraction of the characteristic impedance from TDR measurements, the impedance at low frequency is fixed by the value corresponding to the settled voltage level. Hence, for simulating digital signals, the finite value of impedance at low frequency is more critical than its complex representation.

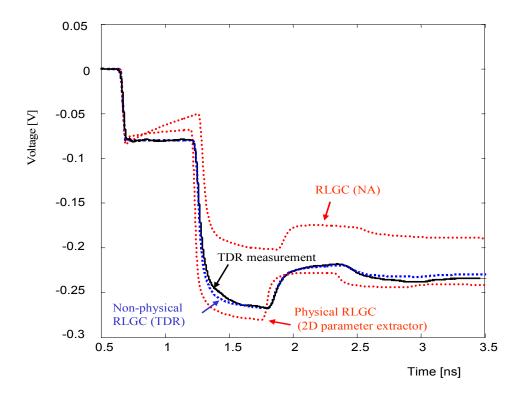


Figure 3.15 Measurements and simulations for the coplanar line.

# 3.6. Eye-diagram simulation

Eye diagrams are useful in characterizing high-speed digital circuits. The circuit used for the eye-diagram simulation of transmission lines was a simple long transmission line with a pulse source and a 50 ohm source resistance at the near end and a 50 ohm load resistance at the far end, as shown in Figure 3.16. Two kinds of voltage sources were used: 1) A periodic square wave similar to a clock signal and 2) a random binary signal. Eye diagrams were simulated at the far end of the transmission line. The non-physical RLGC model in Equation (3.21) and physical RLGC model in Equation (3.22) have been simulated for comparison.

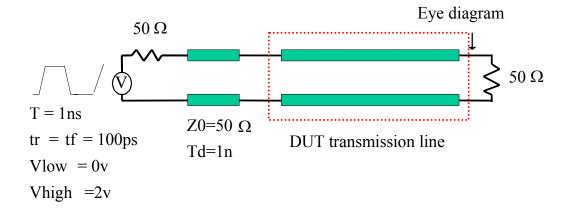


Figure 3.16 Circuit for eye-diagram simulation.

#### 3.6.1. Periodic square waves

A pulse source with a period of 1 ns and risetime/falltime of 100ps was used. The length of the lossy transmission line was 1m. The high and low voltage level of the pulse were 2V and 0V, respectively. The transient signal was measured at the 50  $\Omega$  load from 50ns to 200ns, as shown in Figure 3.17. Figure 3.17 shows the simulated eye-diagram of the long lossy transmission line using both the non-physical RLGC and physical RLGC models.

Since the non-physical RLGC model shows better agreement with TDR measurement in Figure 3.15, the eye diagram of the non-physical RLGC model is closer to the actual waveforms on the transmission line. The physical RLGC model shows unstable behavior causing fluctuations along the time axis, which is the reason for the substantial jitter in Figure 3.17. On the other hand, the non-physical RLGC model is stable and shows no voltage and time variation, which is expected of a periodic source.

The instability of the physical RLGC model depends on the length of transmission lines in the simulation. For example, a 6-inch long transmission line with the same physical RLGC parameters shows a clearer eye-diagram similar to that of the non-physical RLGC model. However, as the length of lossy transmission line increases, the unstable behavior appears in the physical RLGC model.

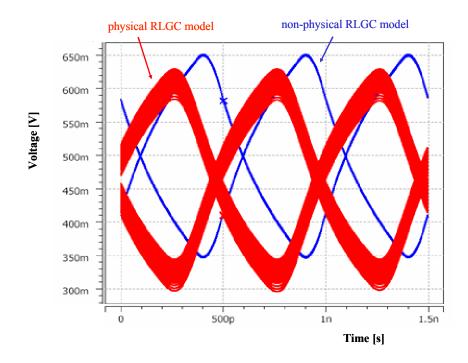
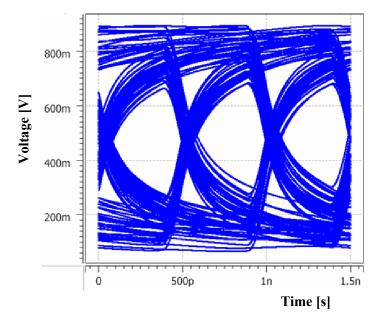


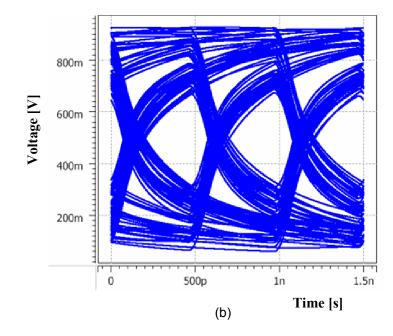
Figure 3.17 Eye-diagram simulations with a periodic square wave.

# 3.6.2. Random binary signals

Since signals are usually random rather than periodic, a random NRZ (Non-Returnto-Zero) signal of 2 Gbps was used to stimulate the long transmission line, with risetime and falltime of 100ps. The length of the transmission line was 0.5m. The high and low level voltage of the pulse were 2V and 0V, respectively. The eye-diagram was measured at the 50 ohm load from 50ns to 200ns. Figure 3.18 shows the simulated eye-diagrams of the long lossy transmission line with the random binary source. The non-physical RLGC model shows a smaller eye-opening than the physical RLGC model due to the higher loss.







**Figure 3.18** Eye-diagram simulation with a random binary source. (a) physical RLGC model and (b) non-physical RLGC model.

## 3.7. Effect of frequency-dependent parameters on digital signals

The effect of frequency-dependent characteristic impedance and propagation constant on digital signal are discussed in this section.

#### 3.7.1. Effect of frequency-dependent characteristic impedance

To investigate the effect of the frequency-dependent characteristic impedance on TDR waveforms using non-physical RLGC models, TDR simulations were performed using the parameters in Equation (3.23) with a short termination, where

Z01 = 25.7 ohms

 $Z02 = 1 \exp(-f/0.8e9) + 24.7 \text{ ohms}$  (3.23)

 $Z03 = 5^{exp}(-f/0.8e9) + 20.7$  ohms

with  $\alpha = 8/10e9^{*}f + 4/sqrt(10e9)^{*}sqrt(f)$  Np/m and  $\beta = 2\pi f/3e8^{*}sqrt(3.1611)$  /m

In Equation (3.23), the characteristic impedance is the same for all the examples at zero frequency. Figure 3.19 shows the TDR simulations for the three examples. The main difference occurs in the transition of the first reflection where high frequency components are dominant. With Z01, since it is constant with frequency, the high-frequency characteristic impedance is the same as the low-frequency characteristic impedance, resulting in the same shape as the input pulse. With Z02, the high-frequency characteristic impedance is ~24.7 ohms and the low-frequency characteristic impedance is 25.7 ohms, generating a dip in the falling transition. The dip for Z02 has the lower bound of 24.7 ohms. Finally, for Z03, the dip becomes deeper because the lower bound is 20.7 ohms. From this simulation, it can be seen that the effect of the frequency-dependent characteristic impedance on TDR waveforms is to create a null in the transition of the first reflection. The lower bound of the first reflection is the high-frequency characteristic impedance, which is the characteristic impedance around the 3dB bandwidth of the input pulse.

94

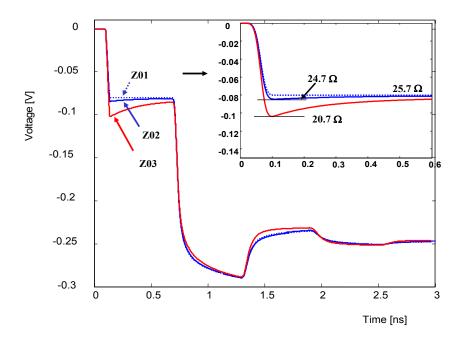


Figure 3.19 TDR response for various frequency-dependent Z0.

#### 3.7.2. Effect of frequency-dependent propagation constant

The attenuation constant of transmission lines is frequency-dependent due to skineffect and dielectric loss. In general, the attenuation constant increases monotonically with frequency. In this section, to investigate the effect of the frequency-dependent attenuation constant on TDR using non-physical RLGC models, the frequencydependent attenuation constant was modeled as a linear function as shown below:

$$\alpha 1 = 0 \text{ Np/m}$$
  
 $\alpha 2 = 1.2e-9 * f \text{ Np/m}$  (3.24)  
 $\alpha 3 = 2.4e-9 * f \text{ Np/m}$   
with  $\beta = 2^* \pi * f/3e8 * \sqrt{3.1611}$  /m and  $70 = 25.7 \text{ obms}$ 

The DC attenuation constant for the examples considered were assumed to be zero with  $R_{DC} = 0$ . As shown in Figure 3.20, there is no difference in the first reflection of the TDR waveform due to the constant characteristic impedance. However, the round-trip reflection suffers from the varying losses of the transmission line. As the high-frequency

loss increases, the fall time of the round-trip reflection increases. However, in all these cases, the steady-state level of the round-trip reflection remains constant, which is determined by the attenuation constant at DC.

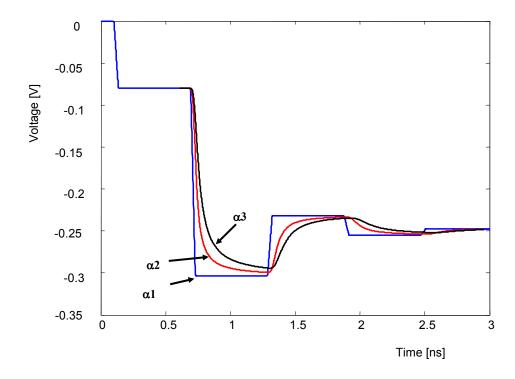


Figure 3.20 TDR response with various frequency-dependent propagation constant.

# 3.8. In-situ characterization of transmission lines

The TDR techniques proposed for characterizing transmission lines in this chapter require the measurement of Short, Open, Load and Line calibration structures. Although the calibration techniques are accurate, they are complex and require a priori knowledge for calibration. For practical applications, TDR techniques which are simple and easy to use are necessary in a manufacturing environment. Therefore, an in-situ characterization method without the need for calibration for characterizing transmission lines has been proposed in this section, based on the non-physical RLGC models and transient behavior of transmission lines.

# 3.8.1. Transient behavior of *f* and *sqrt(f*) in the attenuation constant

Consider the time domain response of  $exp(-a \cdot f)$  and  $exp(-b \cdot v \cdot f)$  to a step pulse. These functions have been chosen here since the loss of transmission lines can be modeled using *f* and  $v \cdot f$  behavior that captures the dielectric loss and conductor loss, respectively. In the exponential functions, *a* and *b* are constants and *f* is the frequency. As an example, consider the following functions.

$$F1(f) = \exp\{-5/10e9 \cdot f \cdot 0.1\}$$

$$F2(f) = \exp\{-10/10e9 \cdot f \cdot 0.1\}$$

$$F3(f) = \exp\{-5/sqrt(10e9) \cdot sqrt(f) \cdot 0.1\}$$

$$F4(f) = \exp\{-10/sqrt(10e9) \cdot sqrt(f) \cdot 0.1\}$$

The functions in Equation (3.25) can be used to represent the loss of materials such as FR4 and APPE. Assuming that the length of the transmission line *I* = 0.1m, the above functions are the transfer function of the attenuation constant  $\alpha$ , which is given by exp(- $\alpha \cdot I$ ), where *I* is the length of the transmission line. The time domain response of Equation (3.25) to a step pulse can be obtained through Hspice W-element tabular models [C18]. Using the circuit shown in Figure 3.1, let R<sub>s</sub> = 50, Z<sub>0</sub> = 50, R<sub>L</sub> = 50, *I* = 0.1m and

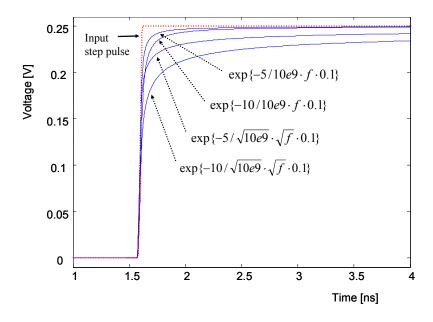
$$\alpha 1 = 5/10e9 \cdot f$$

$$\alpha 2 = 10/10e9 \cdot f$$

$$\alpha 3 = 5/sqrt(10e9) \cdot sqrt(f)$$

$$\alpha 4 = 10/sqrt(10e9) \cdot sqrt(f)$$
(3.26)

The time-domain waveform at the load RL for a step pulse is shown in Figure 3.24 after removing delay, which is the step pulse response of the functions in Equation (3.25).



**Figure 3.21** Step pulse response to  $exp(-a \cdot f)$  and  $exp(-b \cdot \sqrt{f})$ .

Since the response in Figure 3.21 is dominated by the low frequency behavior after the rising part of the step pulse, the response should approach the DC resistance of the transmission line in the steady state. As shown in Figure 3.21, functions F1 and F2 in Equation (3.25) approach the steady-state quickly, while functions F3 and F4 take a long time. To ensure that functions F3 and F4 reach the steady state faster, the following approximation has been used for representing  $\sqrt{f}$  in the attenuation constant.

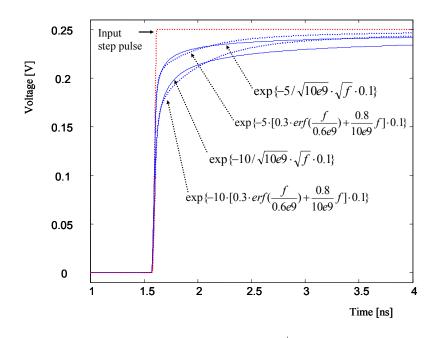
$$\frac{1}{\sqrt{10e9}}\sqrt{f} \approx 0.3 \cdot erf(\frac{f}{0.6e9}) + \frac{0.8}{10e9}f$$
(3.27)

where *erf* is the error function. Since  $erf(f/0.6e9) \approx 2/sqrt(\pi) \cdot f/0.6e9$  when f $\approx 0$ , the approximation in Equation (3.27) approaches the steady state faster. Then, the associated attenuation constant  $\alpha 3$  and  $\alpha 4$  in Equation (3.26) can be approximated as:

$$\alpha 3 = \frac{5}{\sqrt{10e9}} \sqrt{f} \approx 5 \cdot [0.3 \cdot erf(\frac{f}{0.6e9}) + \frac{0.8}{10e9}f]$$

$$\alpha 4 = \frac{10}{\sqrt{10e9}} \sqrt{f} \approx 10 \cdot [0.3 \cdot erf(\frac{f}{0.6e9}) + \frac{0.8}{10e9}f]$$
(3.28)

The step response using the attenuation constant  $\alpha$ 3 and  $\alpha$ 4 in Equation (3.28) are shown in Figure 3.22. The approximation in Equation (3.28) improves the low frequency behavior of  $\sqrt{f}$  while maintaining the high frequency response.



**Figure 3.22** Step pulse response to  $exp(-b \cdot \sqrt{f})$  and its approximation.

# 3.8.2. Procedure for in-situ characterization

#### 3.8.2.1. Assumptions

The in-situ characterization method for lossy transmission line using TDR measurements has been developed under the following assumptions:

- The transmission line length is long compared to the rise and fall time of the input pulse, such that the steady-state level of the round-trip reflection can be measured, as shown in Figure 3.2.
- 2) The transmission lines are terminated with a short circuit.

3) Based on the extracted characteristic impedance in Figure 3.4, the frequencydependent characteristic impedance of the transmission line can be modeled using an exponential function given by:

$$Z0(f) = (Z0_{DC} - Z0_{high}) * exp(-f / f1) + Z0_{high} \Omega$$
(3.29)

where  $ZO_{DC}$  and  $ZO_{high}$  are the DC characteristic impedance and high frequency characteristic impedance, respectively, f is the frequency in Hz, and f1 is a constant. Since Z0 is proportional to the inductance of the transmission line if the phase velocity is constant, f1 is mainly determined by the frequency behavior of the inductance of transmission lines, which does not change with the dielectric material. The behavior in Figure 3.4 has been validated using measurements of transmission lines on various dielectric materials.

4) The attenuation constant can be modeled as:

$$\alpha = a \cdot f + b \cdot \sqrt{f} \qquad \text{Np/m} \tag{3.30}$$

where *a* and *b* are constants. *a* f represents the dielectric loss and  $b \cdot \sqrt{f}$  represents the conductor loss.

5) The propagation constant can be modeled as a linear function for representing the group delay of the step pulse, given by:.

$$\beta = 2 * pi * f / C_0 * sqrt(\varepsilon_{eff}) \qquad rad/m \qquad (3.31)$$

where  $C_o$  is the speed of light in free space and  $\epsilon_{eff}$  is the effective dielectric constant.

Under the above assumptions, the unknowns in Equation (3.29), (3.30) and (3.31) are  $ZO_{DC}$ ,  $ZO_{high}$ , *f1*, *a*, *b*,  $\varepsilon$ r and the static resistance of the transmission line, which can be obtained directly from TDR measurements without knowing the physical dimension and material properties of the transmission line. All the simulations in this section were done using Hspcie W-element Tabular models [C18].

#### 3.8.2.2. Step 1: TDR measurement of a transmission line

The first step is the measurement of a transmission line using the TDR, as shown in Figure 3.23. The transmission line measured was a coplanar line fabricated on Ciba thin film dielectric material. The Ciba thin film substrate had a thickness of 1 mil and metal layers on both sides. Coplanar lines were fabricated on the metal layer with a thickness of 1mil. The center conductor had a width of 5 mils and the gap between metal lines was 3 mils. The ground conductor had a width of 10 mils.

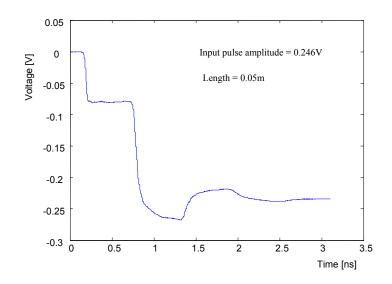
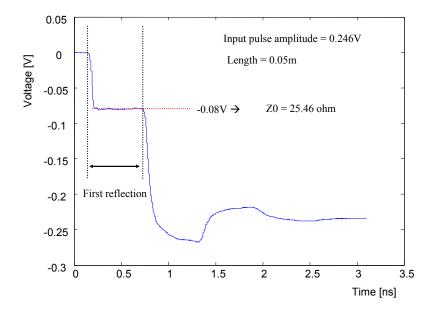


Figure 3.23 TDR measurement of a lossy transmission line.

#### 3.8.2.3. Step 2: extraction of the characteristic impedance

The second step is the extraction of the characteristic impedance. Since the first reflection in Figure 3.24 is only determined by the characteristic impedance, the simulation using the extracted characteristic impedance must match the waveform from the first reflection. Based on the effect of the frequency-dependent characteristic impedance on the step pulse response explained in Section 3.7.1, the characteristic impedance parameters  $ZO_{DC}$ ,  $ZO_{high}$ , and f1 can be determined from the TDR measurement. For example, the characteristic impedance in Figure 3.4 had  $ZO_{DC}$ = 25.7

 $\Omega$ , Z0<sub>high</sub>=24.7  $\Omega$  and f1 = 0.8GHz. In many package transmission lines, constant characteristic impedance can be assumed, as shown in Figure 3.24.



**Figure 3.24** Extraction of the frequency-dependent characteristic impedance from the first reflection in Figure 3.1.

Assuming constant characteristic impedance, the characteristic impedance can be extracted from the first reflection in Figure 3.24, as shown below:

$$Z_0 = 50 \cdot \frac{1 + \frac{-0.08}{0.25}}{1 - \frac{-0.08}{0.25}} = 25.46 \ \Omega \tag{3.32}$$

# 3.8.2.4. Step 3: Extraction of the effective dielectric constant

The third step is the extraction of the effective dielectric constant from the round-trip delay of the pulse. From the round-trip delay in Figure 3.25, the effective dielectric constant can be calculated as:

$$\varepsilon_{\text{eff}} = \{3e8/(2 \cdot l/0.63ns)\}^2 = 3.5721 \tag{3.33}$$

However, the effective dielectric constant in Equation (3.33) is not accurate due to the finite risetime of the input and reflected pulses, which needs optimization using H-spice simulation.

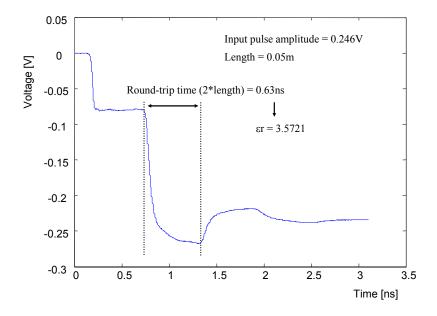


Figure 3.25 Finding the effective dielectric constant.

# 3.8.2.5. Step 4: Extraction of the DC resistance

The fourth step is the extraction of the DC resistance of the transmission line. From the measurement in Figure 3.25, the steady-state voltage at ~ 3ns approaches a DC resistance of 1.23  $\Omega$ . The steady-state voltage measured was -0.2342V, which corresponds to 1.23  $\Omega$  of resistance using the voltage divider. The calculated DC resistance from the physical dimensions of the transmission line is 1.2  $\Omega$  for a conductor conductivity of 2 x 10<sup>7</sup> S/m which correlates well with the measurement. For open termination, it is difficult to extract the static resistance of transmission lines from TDR measurements. Hence, a short termination is preferred during in-situ characterization.

# 3.8.2.6. Step 5: Adjustment of the effective dielectric constant

The fifth step is the adjustment of the extracted effective dielectric constant. Assuming that the line is lossless ( $\alpha = 0$ ), the extracted effective dielectric constant can be simulated using W-element Models in Hspice, as shown in Figure 3.26.

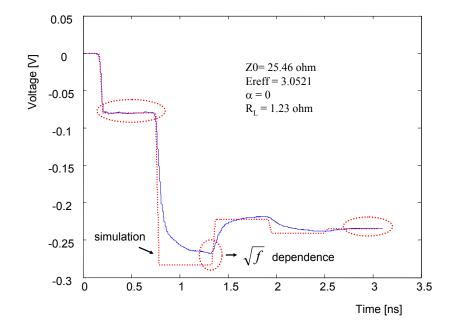
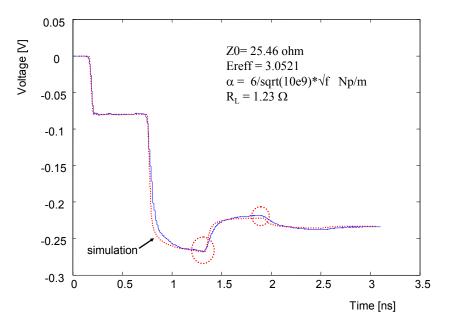


Figure 3.26 Optimized waveform using simulation for lossless transmission line.

In Figure 3.26, three points in the simulation must match the measurement. The first one is the first reflection determined only by the characteristic impedance. The second is the round-trip delay determined only by the effective dielectric constant. The final one is the steady-state voltage determined only by the load and DC resistance of the transmission line. Based on the comparison in Figure 3.26, the characteristic impedance, effective dielectric constant and DC resistance of the transmission line can be suitably adjusted and optimized.

# 3.8.2.7. Step 6: Extraction of $b \cdot \sqrt{f}$ in the attenuation constant

The sixth step is the extraction of  $b \cdot v^{\dagger}$  in Equation (3.30) for representing the attenuation constant of transmission lines. According to Figure 3.21,  $b \cdot v^{\dagger}$  in Equation (3.30) shows different behavior as compared to *a*  $\cdot$ f, leading to a difference between simulation and measurement, as shown in Figure 3.26. If the difference between the lossless simulation and measurement is negligible in Figure 3.26, the effect of  $b \cdot v^{\dagger}$  is negligible. However, as shown in Figure 3.26, if there is a difference, the difference is mainly due to the  $b \cdot v^{\dagger}$  behavior. Therefore, through Hspice simulation, *b* can be determined through optimization, as shown in Figure 3.27.



**Figure 3.27** Finding  $b \cdot \sqrt{f}$  in the attenuation constant.

## 3.8.2.8. Step 7: extraction of *a* f in the attenuation constant

The final step is the extraction of  $a \cdot f$  in the attenuation constant, as shown in Equation (3.30). From Figure 3.21, the effect of  $a \cdot f$  on the waveform leads to smooth curvature in

the round-trip reflection, for the same steady-state level. Hence, *a f* can be determined by matching the round trip reflections, as shown in Figure 3.28.

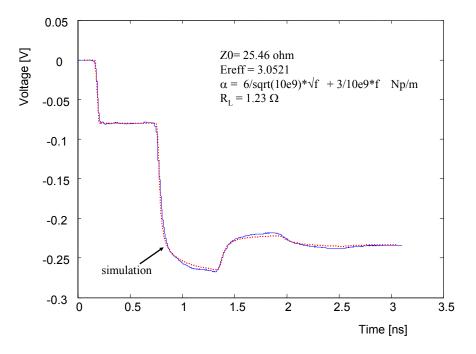


Figure 3.28 Finding *a* f in the attenuation constant.

Finally, the extracted parameters from the in-situ characterization method can be determined as:

Z0= 25.46 ohm  
εr = 3.0521 (3.34)  

$$\alpha$$
 = 6/sqrt(10e9)\* $\sqrt{f}$  + 3/10e9\*f Np/m  
R<sub>L</sub> = 1.23 Ω

These parameters can be simulated using the W-element model in Hspice.

# 3.8.2.9. Step 8: Verification of the extracted data

The extracted parameters can be used for simulating the transmission line with different terminations. For example, a transmission line with the same cross-section and same length was simulated with open termination, as shown in Figure 3.29, and compared with the time-domain measurement for verification. In Figure 3.29, the simulation and measurement shows good correlation, showing the accuracy of the extracted data. The small error in the first round-trip reflection of Figure 3.29 is probably due to the open termination, which is not a perfect open but has a capacitive effect.

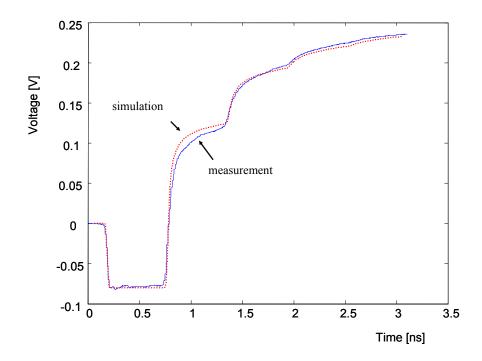


Figure 3.29 Comparison between simulation and measurement for open termination.

# 3.9. Characterization of Striplines

The extraction method using TDR measurements discussed earlier can also be applied to striplines. As an example, consider the structure shown in Figure 3.30. In Figure 3.30, the copper center conductor of the stripline has a width of 5 mils and thickness of 23.4um. The dielectric material surrounding the conductor is an organic material similar to FR4 with  $\varepsilon r = 3.9$  and  $\tan \delta = 0.02$ . The dielectric thickness from the conductor to both grounds is 6 mils. Both grounds were fabricated with copper and had thickness of 1 mil. The length of the stripline was 5 inches, and the pads for probing were located on the top surface and connected to the signal line and ground through vias. Ground-Signal probes from Cascade Microtech with 450um pitch were used to measure the TDR waveform, as shown in Figure 3.30.

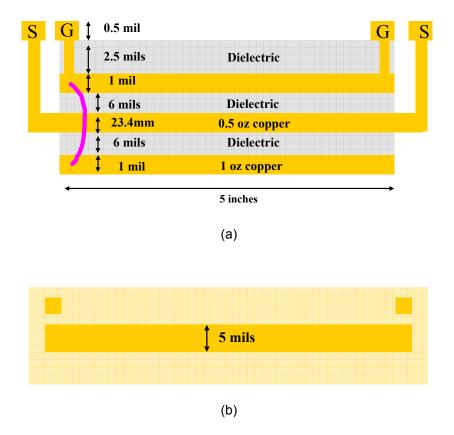


Figure 3.30 (a) Side view and (b) top view of the fabricated stripline.

Based on the cross-section of the stripline, physical RLGC models for the stripline were computed using Hspice 2D Parameter Extractor as:

R = 
$$5.842 + 1.1413e-3 * \sqrt{f}$$
 ohm /m  
L =  $329.36$  nH /m (3.35)  
G =  $1.6534e-11 * f$  S/m  
C =  $131.57$  pF/m

For non-physical RLGC models, the characteristic impedance and propagation constant of the stripline were measured using TDR. This resulted in the following parameters:

Z0 = 50.1 ohms  

$$\alpha = 1/10e9 * f + 3/\sqrt{10e9} * \sqrt{f}$$
 Np/m (3.36)  
 $\beta = 2*\pi * f/3e8 * \sqrt{3.9}$ 

For improving the low-frequency behavior, the attenuation constant was approximated using the following function:

$$\alpha = \frac{1}{10e9} \cdot f + \frac{3}{\sqrt{10e9}} \sqrt{f} \approx \frac{1}{10e9} \cdot f + 3 \cdot [0.3 \cdot erf(\frac{f}{0.6e9}) + \frac{0.8}{10e9} f]$$
(3.37)

where *erf* is the error function. The non-physical RLGC model for the stripline was computed as:

$$R = 50.1(1/10e9 * f + 3/\sqrt{10e9} * \sqrt{f}) \text{ ohm /m}$$

$$L = 329.8 \text{ nH /m}$$

$$G = (1/10e9 * f + 3/\sqrt{10e9} * \sqrt{f})/50.1 \text{ S/m}$$

$$C = 131.39 \text{ pF/m}$$
(3.38)

The two RLGC models were simulated using W-element models in Hspice and compared with the TDR measurement in Figure 3.31. The pad parasitics for the stripline was modeled as a capacitor with a capacitance of 0.35pF. As can be seen in Figure 3.31,

the non-physical RLGC models show good correlation with TDR measurements as compared to physical RLGC models.

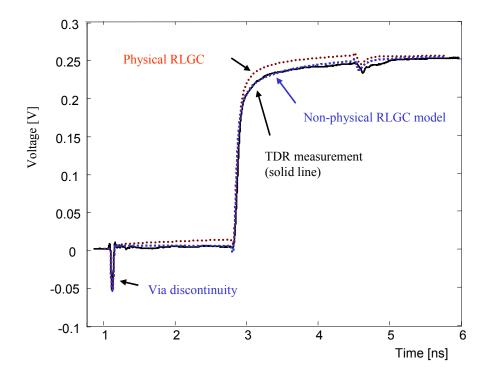


Figure 3.31 TDR measurement and simulation for the stripline.

# 3.10. Characterization of package transmission lines

Using the TDR based characterization methods described in this chapter, various package transmission lines were measured. The results were used for selecting the appropriate board material and geometry for the wafer level package (WLP) described in Chapter 1.

# 3.10.1. Co-planar transmission line test vehicle

Co-planar lines with the cross-section and layout in Figure 3.32 were fabricated at the PRC. For FR-4, APPE, Hitachi MCL-LX67 and Nelco N4000-13, the thickness of the dielectric material used was 1mm. For Ciba and Vialux thin films, the thickness of the

dielectric material used was 1mil. For FR-4, Ciba and Vialux, the center conductor had a width of 5 mils and the gap between metal lines was 3 mils. For APPE, Hitachi MCL-LX67 and Nelco N4000-13, the center conductor had a width of 2.5 mils and the gap between metal lines was 2.5 mils.

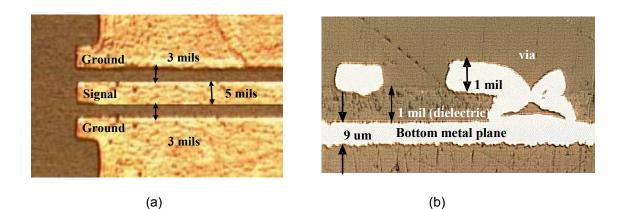


Figure 3.32 (a) Top view and (b) cross-section of fabricated coplanar lines.

# 3.10.2. Coplanar lines on FR-4

The FR-4 substrate used had a dielectric thickness of 1mm and metal layers on both sides. Coplanar lines were fabricated on the metal layer. The center conductor had a width of 5 mils and the gap between metal lines was 3 mils. Using the TDR measurements in Figure 3.33, the following parameters were extracted:

Z0 = 88 
$$\Omega$$
  
Effective  $\varepsilon r$  = 2.1 (3.39)  
 $\alpha = 7/10e9 \cdot f$  NP/m

The extracted data was used to simulate a coplanar line with length 5cm and compared to TDR measurements, as shown in Figure 3.33. The far end of the line was connected to ground.

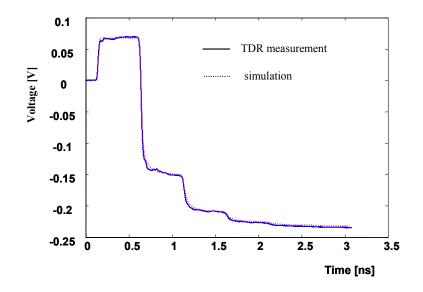


Figure 3.33 TDR measurements and simulations for a coplanar line on FR4.

## 3.10.3. Coplanar lines on APPE

The APPE substrate used had a dielectric thickness of 1mm and metal layers on both sides. Coplanar lines were fabricated on the metal layer. The center conductor had a width of 2.5 mils and the gap between metal lines was 2.5 mils. From TDR measurements, the following parameters were extracted:

Z0 = 107 
$$\Omega$$
  
Effective  $\varepsilon r$  = 1.95 (3.40)  
 $\alpha = 3/\sqrt{10e^9} \cdot \sqrt{f}$  NP/m

Then, the extracted data was simulated in Hspice for a coplanar line with length 1705 mils and compared to TDR measurements, as shown in Figure 3.34. The far end of the line was left un-terminated.

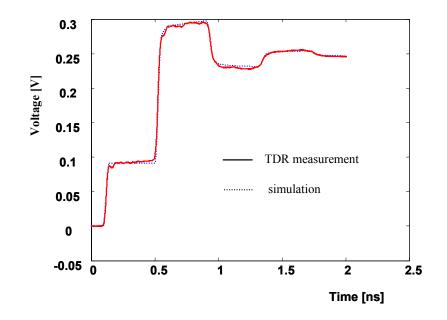


Figure 3.34 TDR measurements and simulations for a coplanar line on APPE.

# 3.10.4. Coplanar lines on Ciba thin film

The Ciba thin film substrate had a dielectric thickness of 1 mil and metal layers on both sides. Coplanar lines were fabricated on the metal layer. The center conductor had a width of 5 mils and the gap between metal was 3 mils. From TDR measurements, the following parameters were extracted:

Z0 = 25.5 
$$\Omega$$
  
Effective  $\varepsilon r$  = 3.05 (3.41)  
 $\alpha = 3/10e9 \cdot f + 6/\sqrt{10e9} \cdot \sqrt{f}$  NP/m

Then, the extracted data was simulated for a coplanar line with length 5cm and compared to TDR measurements, as shown in Figure 3.35. The far end of the line was short-circuited.

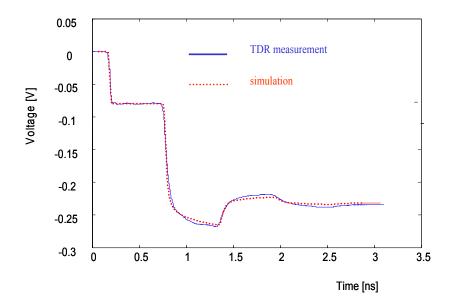


Figure 3.35 TDR measurements and simulations for a coplanar line on Ciba material.

# 3.10.5. Co-planar lines on Vialux thin fim

The Vialux thin film substrate had a thickness of 1 mil and metal layers on both sides. Co-planar lines were fabricated on the metal layer. The center conductor had a width of 5 mils and the gap between metal lines was 3 mils. From TDR measurements, the following parameters were extracted:

Z0 = 45.3 
$$\Omega$$
  
Effective  $\varepsilon r$  = 2.55 (3.42)  
 $\alpha = 4/10e9 \cdot f + 2/\sqrt{10e9} \cdot \sqrt{f}$  NP/m

Then, the extracted data was simulated for a coplanar line with length 5cm and compared to TDR measurements, as shown in Figure 3.36. The far end of the line was short-circuited.

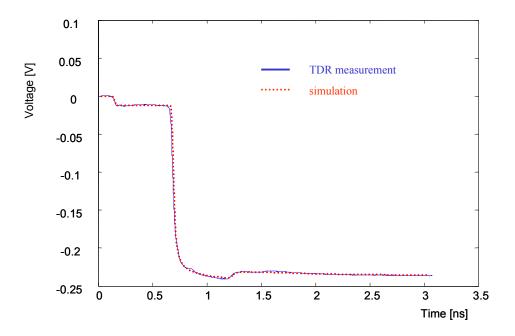


Figure 3.36 TDR measurements and simulations for a coplanar line on Vialux material.

# 3.10.6. Co-planar lines on Hitachi MCL-LX67

The Hitachi substrate had a dielectric thickness of 1mm and metal layers on both sides. Coplanar lines were manufactured on the metal layer with the other side metal removed. The center conductor had a width of 2.5 mils and the gap between metal was 2.5 mils. From TDR measurements, the following parameters were extracted:

Z0 = 95-11\*exp(-f/3e9)  $\Omega$ Effective  $\varepsilon r$  = 2.3 (3.43)  $\alpha = 1.5/10e9 \cdot f + 2.5/\sqrt{10e9} \cdot \sqrt{f}$  NP/m

Then, the extracted data was simulated for a coplanar line with length 1705 mils and compared to TDR measurements, as shown in Figure 3.37. The far end of the line was open-circuited.

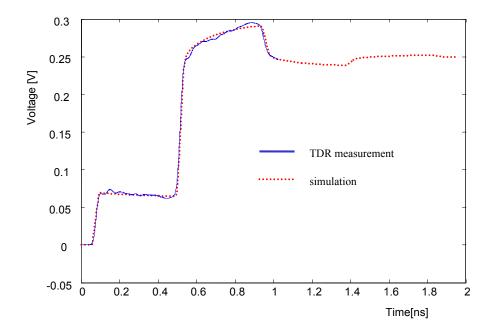


Figure 3.37 TDR measurements and simulations for a coplanar line on Hitachi MCL-LX67

material.

# 3.10.7. Co-planar lines on Nelco N4000-13

The Nelco substrate had a dielectric thickness of 1mm and metal layers on both sides. Co-planar lines were fabricated on the metal layer with the other side metal removed. The center conductor had a width of 2.5 mils and the gap between metal lines was 2.5 mils. From TDR measurements, the following parameters were extracted:

Z0 = 96.6 
$$\Omega$$
  
Effective  $\varepsilon r$  = 2.4 (3.44)  
 $\alpha = 3.2 / \sqrt{10e9} \cdot \sqrt{f}$  NP/m

Then, the extracted data was simulated for a co-planar line with length 1705 mils and compared to TDR measurements, as shown in Figure 3.38. The far end of the line was open-circuited.

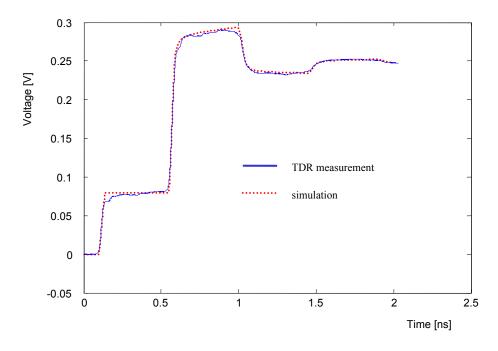
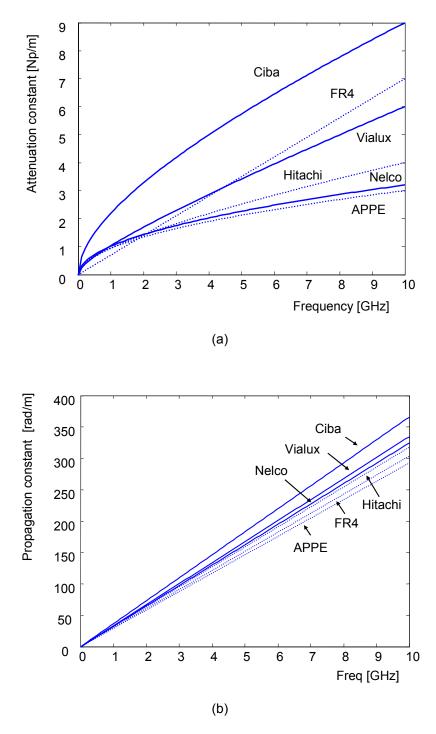


Figure 3.38 TDR measurements and simulations for a coplanar line on Nelco N4000-13 material.

# 3.10.8. Comparison of the fabricated transmission lines

For choosing the board material for the wafer-level test vehicle described in Chapter 1, the propagation constant of the board transmission lines fabricated using Ciba, Vialux, FR4, Hitachi MCL-LX67, Nelco N4000-13 and APPE are shown in Figure 3.39. Since loss is a measure of signal degradation, the attenuation constant is the most important factor for choosing the board material for the wafer-level test vehicle. The imaginary part of the propagation constant in Figure 4.39(b) shows the delay of those transmission lines. APPE has the lowest delay among them. From Figure 3.39, since APPE shows the lowest loss and delay, APPE was chosen for the wafer-level package test vehicle explained in Chapter 1.



**Figure 3.39** Comparison of propagation constant for board transmission lines characterized. (a) attenuation constant and (b) propagation constant.

# 3.11. Summary

In this chapter, a TDR characterization method was proposed for the characterization of lossy transmission lines. The method developed enables the extraction of the frequency-dependent characteristic impedance and propagation constant direcity from TDR measurements. Based on the results in Chapter 2, the uncertainty bound for the characteristic impedance and propagation constant was established. At frequencies below ~2GHz, the extracted data had small uncertainty bound, while the extracted data had a large bound for frequencies above ~2GHz. As explained in Chapter 1, digital simulation requires accurate measurements at low frequencies. The measurements, when simulated using W-element models in Hspice in the time-domain.

In this chapter, non-physical RLGC models were derived from the transient behavior of transmission lines and used for simulation using the extracted data from TDR measurements. Three transmission line models were compared in this chapter, namely, physical RLGC models, non-physical RLGC models and NA based RLGC models. Among these models, non-physical RLGC models showed the best agreement with measurements.

Using the non-physical RLGC models, the frequency-dependent effect of characteristic impedance and attenuation constant on digital signals was discussed. Based on these results, an in-situ characterization method for transmission lines was developed.

Various board transmission lines were measured and characterized using dielectric materials such as Ciba, Vialux, FR4, Hitachi MCL-LX67, Neclo N4000-13 and APPE. Among them, APPE had the lowest loss and was therefore chosen as the dielectric material for the wafe-level package test vehicle.

119

# **Chapter 4**

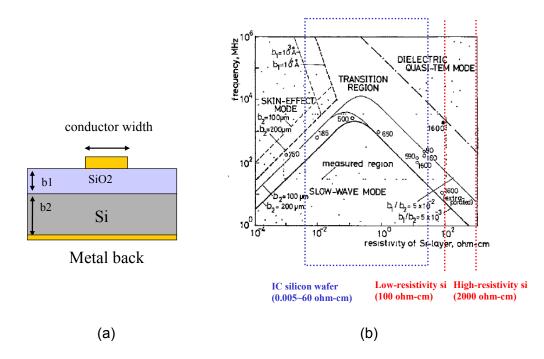
# Characterization of Silicon Transmission Lines

This chapter discusses the characterization of silicon transmission lines using Time-Domain Reflectometry (TDR) and Vector Network Analyzer (VNA) measurements. Coplanar transmission lines on two silicon substrates were fabricated and characterized. The silicon substrate with resistivity  $\rho = 100\Omega$ -cm included a slow-wave propagation effect, while the silicon substrate with resistivity  $\rho = 2000\Omega$ -cm did not contain slow-wave propagation effects. Co-planar lines on the silicon substrate with resistivity  $\rho = 2000\Omega$ cm were characterized using the TDR characterization method described in Chapter 3. However, co-planar lines on the silicon substrate with resistivity  $\rho = 100\Omega$ -cm could not be characterized using the TDR characterization method due to the slow-wave propagation effect, which is one major limitation of the TDR characterization method discussed in this dissertation. Instead, VNA measurements have been used along with non-physical RLGC models for the characterization of transmission lines with slow-wave propagation effects, as discussed in this chapter. Finally, the best silicon transmission line structure was chosen for the wafer-level test vehicle described in Chapter 1, for obtaining the best signal quality in the waveform.

# 4.1. Prior measurement methods for silicon transmission lines

In previous work available in the literature, characterization methods for package

transmission lines have been applied to silicon transmission lines under the assumption that the silicon transmission lines can be represented using the characteristic impedance and propagation constant. In [D1][D2][D3][D4][D5], the characteristic impedance and propagation constant of silicon transmission lines have been extracted using VNA measurements without the inclusion of slow-wave mode propagation. However, in Section 4.4, it has been shown that slow-wave effects of silicon transmission lines cannot be represented only by using the characteristic impedance and propagation constant. Since current integrated circuits are being fabricated on silicon substrates with resistivity range from ~0.005  $\Omega$ -cm to ~60  $\Omega$ -cm, most silicon-level interconnections include slow-wave propagation effects, based on the chart in Figure 4.1 [D6].



**Figure 4.1** Silicon resistivity vs. frequency relationship [D6]. (a) Line structure and (b)resistivityfrequency chart. b1 is the thickness of SiO2 and b2 is the thickness of Si. Numbers attached to the points are the conductor widths in um.

The chart in Figure 4.1(b) was obtained through a theoretical analysis of the line structure in Figure 4.1(a). Existence of three types of fundamental models was concluded in [D6]. In the quasi-TEM mode, the Si layer acts like a dielectric. In the skin-effect mode, the Si layer behaves like a lossy conductor wall, and the dispersion behavior is governed by the skin effect in the silicon substrate. In the slow-wave mode, the propagation velocity slows down due to the so-called "Maxwell-Wagner mechanism." However, surface wave propagation and radiation were not considered in [D6].

Since it is difficult to extract Z0,  $\gamma$  and the slow-wave mode propagation parameters from measurements, silicon transmission lines have often been represented using quasistatic equivalent circuit models instead of transmission-line RLGC models [D7][D8]. In [D9][D10], analytical models were developed using complex image theory and conformal mapping that include the slow-wave effect. In this dissertation, non-physical RLGC models for silicon transmission lines are developed that include the slow-wave effect for silicon substrates. The characteristic impedance, propagation constant and slow-wave effect are extracted from TDR and NA measurements based on the non-physical RLGC models for silicon transmission lines. Two kinds of silicon substrates were investigated based on the chart in Figure 4.1, namely, a wafer with resistivity  $\rho$ =100  $\Omega$ -cm and a wafer with resistivity  $\rho$ =2000  $\Omega$ -cm. While the silicon substrate with resistivity of 100  $\Omega$ cm includes slow-wave propagation effects, the silicon substrate with resistivity of 2000  $\Omega$ -cm does not include a slow-wave propagation effect.

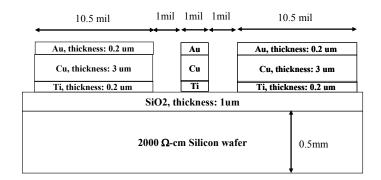
## 4.2. Co-planar lines on high resistivity silicon substrate

Co-planar silicon transmission lines were fabricated on silicon substrate with resistivity of 2000  $\Omega$ -cm. In this section, the co-planar silicon lines are characterized using the TDR characterization methods described in Chapter 3.

122

#### 4.2.1. Fabricated co-planar lines

Co-planar silicon transmission lines were patterned using Au-Cu-Ti layers on 2000  $\Omega$ cm resistivity silicon substrate, as shown in Figure 4.2. The cross-section of the fabricated co-planar lines consisted of 0.2um thickness Au, 3um thickness Cu, 0.2um thickness Ti and 1um thickness SiO<sub>2</sub> on 2000  $\Omega$ -cm silicon wafer. The fabricated coplanar lines had a center conductor width of 1 mil and spacing between conductors of 1 mil. The width of each ground conductor was 10.5 mils. The co-planar line measured using the VNA had a length of 60 mils, while the co-planar line measured using the TDR had a length of 960 mils.

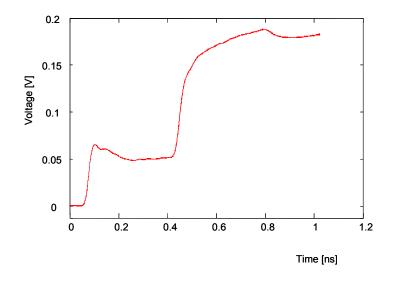


**Figure 4.2** Cross-section of the fabricated co-planar lines on silicon substrate with resistivity of 2000  $\Omega$ -cm.

#### 4.2.2. TDR measurement

Since the co-planar lines on the high resistivity silicon substrate only support the quasi-TEM mode from Figure 4.1, the co-planar lines can be represented by just a characteristic impedance and propagation constant, similar to the package transmission lines described in Chapter 3. The co-planar line with a length of 960 mils was measured using the TDR, as shown in Figure 4.3. The far end of the coplanar line was unterminated. The TDR waveform in Figure 4.3 shows the transient behavior of a

transmission line, as explained in Chapter 3, which contains both the first reflection and round-trip reflection. Hence, the TDR characterization methods described in Chapter 3 can be applied to characterize the co-planar lines on the high resistivity silicon substrate. From the first reflection, the characteristic impedance can be extracted, while the propagation constant can be extracted from the round-trip reflection.



**Figure 4.3** TDR measurement of the coplanar line on 2000  $\Omega$ -cm resistivity silicon substrate.

# 4.2.3. Extraction of characteristic impedance and propagation constant using TDR measurements

Using the TDR characterization methods described in Chapter 3, the co-planar line on the 2000  $\Omega$ -cm resistivity silicon substrate was characterized using the TDR waveform in Figure 4.3. From the measurement, the extracted characteristic impedance and propagation constant can be written as:

Z0 = 89 - 16·exp(-f/3e9) 
$$\Omega$$
  
Effective  $\varepsilon r = 4.9$  (4.1)  
 $\alpha = 18/10e9 \cdot f + 14 \cdot erf(f/0.4e9)$  NP/m

#### $\beta = 2\pi \cdot f/3e8^* \text{sqrt}(\text{Effective } \epsilon r)$ rad/m

where  $\gamma = \alpha + j \cdot \beta$ . *f* is the frequency in Hz, *erf* is the error function, Z0 is the characteristic impedance and  $\gamma$  is the propagation constant. Then, using Equation (3.19), the non-physical RLGC model for the transmission line can be extracted as:

$$R = [89 - 16 \cdot \exp(-f/3e9)] \cdot [18/10e9 \cdot f + 14 \cdot erf(f/0.4e9)] \text{ ohm/m}$$

$$L = [89 - 16 \cdot \exp(-f/3e9)]/3e8^* \operatorname{sqrt}(4.9) \text{ H/m}$$
(4.2)
$$G = [18/10e9 \cdot f + 14 \cdot erf(f/0.4e9)]/[89 - 16 \cdot \exp(-f/3e9)] \text{ S/m}$$

$$C = \operatorname{sqrt}(4.9) / \{3e8^* [89 - 16 \cdot \exp(-f/3e9)]\} \text{ F/m}$$

The non-physical RLGC model in Equation (4.2) was simulated in the time and frequency domains using the W-element tabular models for transmission lines in Hspice. The simulation results show good correlation with measurements in the time and frequency domains, as shown in Figures 4.4 and 4.5.

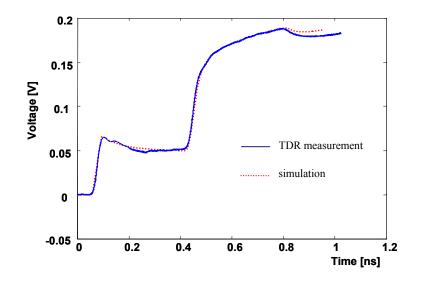
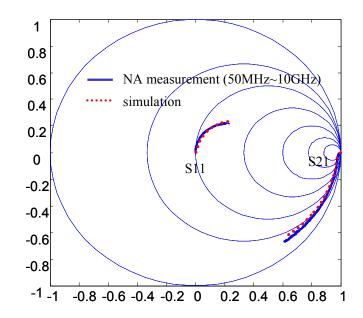


Figure 4.4 Time-domain correlation between simulation and measurement for the coplanar line on 2000  $\Omega$ -cm resistivity silicon substrate.



**Figure 4.5** Frequency-domain correlation between simulation and measurement for the coplanar line on 2000  $\Omega$ -cm resistivity silicon substrate.

In Figure 4.4, the length of the co-planar line used for TDR measurement and simulation was 960 mils, and the far end was unterminated. In Figure 4.5, the length of the coplanar line used for two-port NA measurement and simulation was 60 mils. In Figure 4.5, the parameters S11 and S21 of the VNA measurement and simulation are shown from 50MHz to 10GHz.

# 4.3. Co-planar lines on low resistivity silicon substrate

While the co-planar lines on the 2000  $\Omega$ -cm resistivity silicon substrate can be analyzed similar to board transmission lines, as described in the previous section, the co-planar lines on the low resistivity silicon substrate ( $\rho$ =100  $\Omega$ -cm) cannot be treated in the same way due to slow-wave propagation effects. In this section, silicon transmission lines with slow-wave propagation effects have been analyzed for extracting the characteristic impedance, propagation constant and slow-wave effect.

#### 4.3.1. Fabricated co-planar lines

The fabricated co-planar lines on the silicon substrate with  $\rho$ =100  $\Omega$ -cm are similar to the co-planar lines on the silicon substrate with  $\rho$ =2000  $\Omega$ -cm, as discussed in Section 4.2.1. The thickness of metal and SiO<sub>2</sub> is slightly different. The cross-section of the fabricated co-planar lines consisted of 0.2um thickness Au, 2um thickness Cu, 0.2um thickness Ti and 10nm thickness SiO<sub>2</sub> on a 100  $\Omega$ -cm silicon wafer, as shown in Figure 4.6. The co-planar lines had the same conductor width, gap and length as the highresistivity silicon lines in Section 4.2.1.

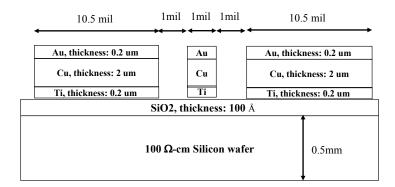
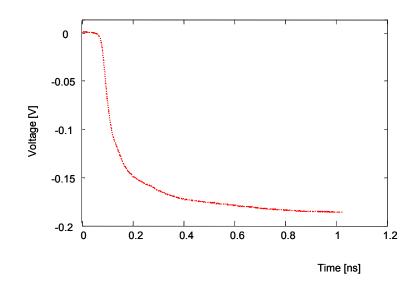


 Figure 4.6
 Cross-section of the fabricated coplanar lines on the silicon substrate

with 100  $\Omega$ -cm resistivity.

#### 4.3.2. TDR measurements

In Figure 4.7, the response of a coplanar line with a length of 960 mils on a silicon substrate with a resistivity of 100  $\Omega$ -cm is shown, which was measured using the TDR. The far end of the coplanar line was unterminated. However, unlike the co-planar line on the high-resistivity silicon substrate in Figure 4.3, the co-planar line on the low-resistivity silicon substrate does not show a transient response similar to Figure 4.3. This is due to the slow-wave propagation effect on the low-resistivity silicon substrate. Hence, the TDR characterization methods described in Chapter 3 cannot be directly applied to the co-planar line on the low-resistivity silicon substrate.

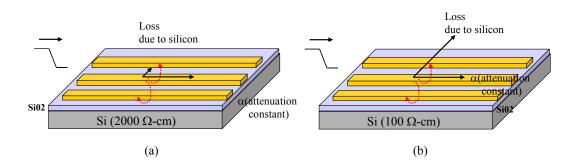


**Figure 4.7** TDR measurement of the coplanar line on 100  $\Omega$ -cm resistivity silicon substrate.

The measured TDR waveforms in Figures 4.3 and 4.7 for 2000  $\Omega$ -cm and 100  $\Omega$ -cm resistivity silicon substrates can be explained using the signal propagation diagram in Figure 4.8. When the step pulse of TDR propagates along coplanar transmission lines, the electric field around the conductor penetrates the silicon substrate, which induces loss by generating an electric current inside the silicon substrate. It is important to note that the direction of the induced current is in the direction orthogonal to the propagation direction. Since the loss caused by the electric field is in the orthogonal direction to the wave propagation direction, the induced loss is not included in the attenuation constant ( $\alpha$ ) of the transmission line. The attenuation constant represents the loss in the wave propagation direction.

In 2000  $\Omega$ -cm resistivity silicon substrate, the electric current induced by the electric field is so small that the orthogonal loss component is negligible. However, 100  $\Omega$ -cm resistivity silicon substrate induces an electric current yielding a large loss in the orthogonal direction. Hence, co-planar lines on a silicon substrate with a resistivity of 100  $\Omega$ -cm have two loss components, namely, the attenuation constant and orthogonal

ohmic loss in the silicon substrate. The orthogonal ohmic loss inside the silicon substrate is another representation of the slow-wave mode for co-planar silicon transmission lines. The TDR waveform in Figure 4.7 for the co-planar line on 100  $\Omega$ -cm resistivity silicon substrate includes the effect of the orthogonal ohmic loss, which attenuates the transient signals rapidly during wave propagation.



**Figure 4.8** Loss induced by silicon substrate. (a) 2000  $\Omega$ -cm and (b) 100  $\Omega$ -cm resistivity.

Metal planes and metal grids on silicon substrate can reduce the orthogonal ohmic loss due to the silicon substrate by blocking the electric field from penetrating the silicon substrate [D11][D12]. Co-planar lines on wafers with a 0.5 um thick aluminum ground shield between the silicon dioxide and silicon showed much smaller loss than co-planar lines on wafers without the ground shield, since the aluminum ground shield blocked the electric field from the silicon substrates [D11]. Instead of the ground shield, an orthogonal grid of grounded lines placed at the oxide/bulk interface also reduced the transmission loss of on-chip interconnections [D12].

Since the co-planar line on the silicon substrate with a resistivity of 100  $\Omega$ -cm cannot be characterized using TDR measurements due to slow-wave mode propagation, Network Analyzer measurements were instead used to characterize the coplanar line.

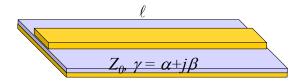
129

# 4.4. Characterization of transmission lines on low-resistivity silicon substrates using non-physical RLGC models

In Chapter 3, non-physical RLGC models for board transmission lines were developed. Board transmission lines can be represented using the characteristic impedance and propagation constant parameters. Therefore, TDR measurements can be used for characterizing board transmission lines. However, as explained in the previous section, non-physical RLGC models for board transmission lines cannot be directly applied to transmission lines containing slow-wave propagation effects. In this section, non-physical RLGC models for transmission lines with slow-wave propagation effects have been developed for characterization and simulation. First, the characteristics of board transmission lines are discussed to demonstrate that the coplanar lines on 100  $\Omega$ -cm silicon substrate cannot be represented using only characteristic impedance and propagation constant. Then, non-physical RLGC models for silicon transmission lines with slow-wave effects are extracted from NA measurements based on the non-physical RLGC models.

#### 4.4.1. Characteristics of board transmission lines

Board transmission lines are represented by characteristic impedance (Z0) and propagation constant ( $\gamma$ ), as shown in Figure 4.9.



**Figure 4.9** Transmission lines represented using Z0 and  $\gamma$  where *l* is the length.

Then, the S-parameters of the transmission line in Figure 4.9 can be represented as:

$$[S] = \frac{1}{e^{\gamma \cdot l} - \Gamma^2 e^{-\gamma \cdot l}} \begin{bmatrix} \Gamma(e^{\gamma \cdot l} - e^{-\gamma \cdot l}) & 1 - \Gamma^2 \\ 1 - \Gamma^2 & \Gamma(e^{\gamma \cdot l} - e^{-\gamma \cdot l}) \end{bmatrix}$$
(4.3)

where *I* is the length of the transmission line,  $\Gamma = (Z0-50)/(Z0+50)$ , and  $50\Omega$  is the impedance of the Network Analyzer.

#### 4.4.1.1. First observation on S11 for board transmission lines

From Equation (4.3), S11 can be simplified as:

$$S11 - \Gamma = (-\Gamma) \frac{(1 - \Gamma^2)}{1 - \Gamma^2 e^{-2\gamma \cdot l}} e^{-2\gamma \cdot l} \approx (-\Gamma)(1 - \Gamma^2) e^{-2\gamma \cdot l}$$
(4.4)

if  $|\Gamma^2 \cdot \exp(-2\gamma \cdot l)| \ll 1$ 

Equation (4.4) is a good approximation for the characteristic impedance between ~20  $\Omega$  and ~100  $\Omega$ , which corresponds to the characteristic impedance of most transmission lines used in real applications. Then, from Equation (4.4), the following two observations can be inferred:

1) S11 approximately forms a circle on the Smith chart whose center is at Z0.

2) S11 always rotates clockwise as the frequency increases.

#### 4.4.1.2. Second observation on S11 for board transmission lines

Assuming that the far end in Figure 4.9 is terminated with 50  $\Omega$ , the input impedance *Zin* at the near-end can be expressed as:

$$Zin = Z_0 \frac{50 + Z_0 \tanh(\gamma)}{Z_0 + 50 \tanh(\gamma)}$$
(4.5)

where  $Z_0$  is the characteristic impedance,  $\gamma$  is the propagation constant and *I* is the length. The input impedance *Zin* in Equation (4.5) is the impedance associated with S11

in Equation (4.3). Let us now consider the input impedance at DC. From Equation (4.5), the input impedance at DC can be expressed as:

$$Zin\_DC = Z_0(f \to 0) \frac{50 + Z_0(f \to 0) \tanh(\alpha_{dc}l)}{Z_0(f \to 0) + 50 \tanh(\alpha_{dc}l)}$$
(4.6)

where  $Z_0(f\rightarrow 0)$  is the low frequency characteristic impedance and  $\alpha_{DC}$  is the attenuation constant at DC. Then, from Equation (4.6), the following two observations can be inferred:

1) If 
$$Z_0(f \rightarrow 0) < 50 \Omega$$
,  $Z_0(f \rightarrow 0) < Zin_DC \le 50 \Omega$ 

2) If 
$$Z_0(f \rightarrow 0) > 50 \Omega$$
,  $50 \Omega \leq Zin_DC < Z_0(f \rightarrow 0)$ 

#### 4.4.1.3. Smith chart behavior of board transmission lines

In addition to the two observations on S11 for board transmission lines, observations on S12 for board transmission lines are also possible. However, since both S11 and S12 are functions of the characteristic impedance and propagation constant for board transmission lines, the observations on S11 for board transmission lines provide enough information for the characterization of board transmission lines.

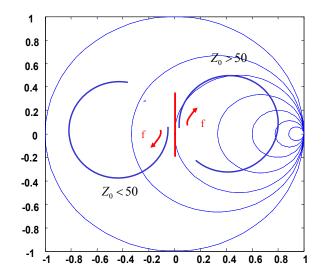
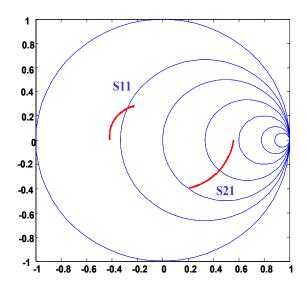


Figure 4.10 Smith-chart behavior of S11 for board transmission lines.

Then, based on the above two observations for S11, transmission lines represented using characteristic impedance and propagation constant should have a response similar to Figure 4.10. If Z0 is larger than 50  $\Omega$ , S11 should rotate clockwise around Z0 with the starting point at DC fixed at between 50  $\Omega$  and  $Z_0(f\rightarrow 0)$ . If Z0 is smaller than 50  $\Omega$ , S11 should also rotate clockwise around Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at between Z0 with the starting point at DC fixed at 50  $\Omega$  for both the cases.

#### 4.4.2. NA measurements of the co-planar line on low-resistivity silicon substrate

The co-planar line on the silicon substrate with a resistivity of 100  $\Omega$ -cm in Section 4.3 was measured using the VNA, as shown in Figure 4.11. The length of the coplanar line measured was 60 mils.



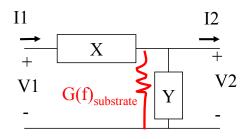
**Figure 4.11** VNA measurement of the coplanar line on 100  $\Omega$ -cm resistivity silicon substrate.

As shown in Figure 4.11, the coplanar line does not resemble the Smith-chart behavior for board transmission lines in Figure 4.10, which implies that the co-planar line cannot

be represented using just the characteristic impedance and propagation constant alone. Although S11 rotates clockwise, the starting point at low frequency is not between 50  $\Omega$  and  $Z_0(f\rightarrow 0)$ . The shift is due to the slow-wave effect. The co-planar line on the 2000  $\Omega$ cm resistivity silicon substrate in Figure 4.5 did not show the shift since it does not include the slow-wave effect. Therefore, the slow-wave effect can be extracted from the shift in the starting point at low frequencies around DC.

## 4.4.3. Non-physical RLGC models for silicon transmission lines with slow-wave propagation effects.

For extracting the slow-wave propagation effect from NA measurements, non-physical RLGC models for silicon transmission lines which include slow-wave propagation effects have been developed. Since the slow-wave propagation effect can be explained by the orthogonal loss inside silicon substrate, it can be added in parallel with the admittance of the non-physical RLGC models developed for board transmission lines, as shown in Figure 4.12. In the figure,  $G(f)_{substrate}$  represents the orthogonal ohmic loss due to silicon substrate discussed in Section 4.3.2, which can be frequency-dependent. In Figure 4.12, X and Y represent the transient behavior of board transmission lines, where X = Z0· $\gamma$  and Y =  $\gamma$ /Z0.



**Figure 4.12** Non-physical RLGC models for silicon substrate with slow-wave propagation effect.  $G(f)_{substrate}$  represents slow-wave propagation effect.

Then, non-physical RLGC parameters for a silicon substrate with slow-wave effect in Figure 4.12 can be expressed as:

$$R = real(Z0 \cdot \gamma)$$

$$L = imag(Z0 \cdot \gamma) / \omega$$

$$G = real(\gamma / Z0 + G(f)_{substrate})$$

$$C = imag(\gamma / Z0) / \omega$$
(4.7)

where  $G(f)_{substrate}$  is the per-unit-length admittance attributed to the effect of the high-loss silicon substrate. For board transmission lines,  $G(f)_{substrate}$  is negligible since metal planes are highly conductive. For co-planar lines on 2000  $\Omega$ -cm resistivity silicon substrate,  $G(f)_{substrate}$  is also negligible since the silicon substrate is close to the propagation of a good dielectric material. The RLGC model in Equation (4.7) can be simulated using the W-element tabular models in Hspice.

#### 4.4.4. Extraction of slow-wave effect from NA measurements

Based on the non-physical RLGC model for silicon transmission lines with slow-wave effect in Equation (4.7), the slow-wave effect  $G(f)_{substrate}$  can be extracted from NA measurements. Although the slow-wave effect  $G(f)_{substrate}$  can be frequency-dependent,  $G(f)_{substrate}$  has been assumed to be constant and real-valued in this dissertation. This is because it is extremely difficult to extract frequency-dependent  $G(f)_{substrate}$ . Based on the assumption, constant  $G(f)_{substrate}$  can be extracted from S11 at DC from Figure 4.11, as shown below:

$$G(f)_{substrate} = \frac{-2 \cdot S11\_DC}{l \cdot 50 \cdot (1 + S11\_DC)}$$
 [S/m] (4.8)

where *I* is the length of the measured transmission line, *S11\_DC* is S11 at DC, and 50  $\Omega$  is the VNA port2 impedance. Since the measurement in Figure 4.11 was done from 50 MHz, S11 at DC was obtained by extrapolating the low-frequency response. Based on Equation (4.8), the co-planar line on 100  $\Omega$ -cm resistivity silicon substrate had *G(f)*<sub>substrate</sub> = 20 S/m.

#### 4.4.5. Extraction of characteristic impedance and propagation constant

The characteristic impedance and propagation constant can be extracted from the VNA measurement after compensating for the slow-wave propagation effect in the extracted frequency response. Let the ABCD-parameters of the measured S-parameters in Figure 4.11 be written as:

$$\begin{bmatrix} ABCD \end{bmatrix}_m = \begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix}$$
(4.9)

Then, the transmission line parameters X and Y in Figure 4.12 can be found from the ABCD parameters using the following equations:

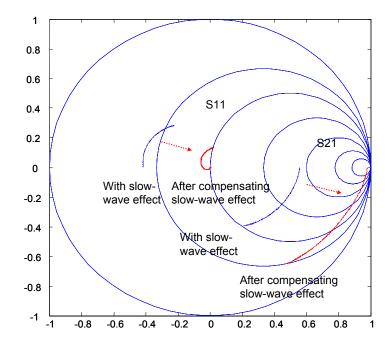
$$X = \frac{1}{l} \cdot \cosh^{-1}(A_m) \cdot \frac{B_m}{\sqrt{A_m^2 - 1}}$$

$$Y = \frac{1}{l} \cdot \cosh^{-1}(A_m) \cdot \frac{\sqrt{A_m^2 - 1}}{B_m} - G(f)_{substrate}$$
(4.10)

Since Z0 = sqrt(X/Y) and  $\gamma$ =sqrt(X·Y), the S-parameters of the coplanar line without slowwave propagation effect can be found, as shown in Figure 4.13. The compensated Sparameters satisfy the observations on S11 for board transmission lines in Section 4.4.1. Therefore, the characteristic impedance and propagation constant can be extracted from the compensated S-parameters using the method discussed in [D1][D2][D3][D4][D5]. Finally, the characteristic impedance, propagation constant and slow-wave propagation effect for the transmission lines on silicon substrates with resistivity of 100  $\Omega$ -cm can be extracted and represented as:

Z0 = 60 - 18·exp(-f/3e9) 
$$\Omega$$
  
Effective  $\varepsilon r$  = 8.2 at 10GHz (4.11)  
 $\alpha = 46/10e9 \cdot f + 14 \cdot erf(f/0.4e9)$  NP/m  
 $\beta = 2\pi \cdot f/3e8^* \text{sqrt}(\text{Effective } \varepsilon r) /m$   
 $\gamma = \alpha + j \cdot \beta$  /m

 $G(f)_{substrate} = 20$  S/m



**Figure 4.13** S-parameters of the coplanar line on 100  $\Omega$ -cm resistivity silicon substrate with and without slow-wave propagation effect.

#### 4.4.6. Model-to-hardware correlation

The extracted characteristic impedance, propagation constant and slow-wave propagation effect in Equation (4.11) were used to develop non-physical RLGC models for silicon transmission lines with slow-wave propagation effect using Equation (4.7). The RLGC parameters were extracted as:

$$R = [60 - 18 \cdot \exp(-f/3e9)] \cdot [46/10e9 \cdot f + 14 \cdot erf(f/0.4e9)] \text{ ohm/m}$$

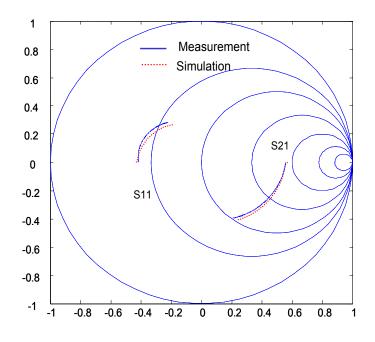
$$L = [60 - 18 \cdot \exp(-f/3e9)] / 3e8^* \operatorname{sqrt}(8.2) \qquad H /m \qquad (4.12)$$

$$G = [46/10e9 \cdot f + 14 \cdot erf(f/0.4e9)] / [60 - 18 \cdot \exp(-f/3e9)] + 20 \quad S/m$$

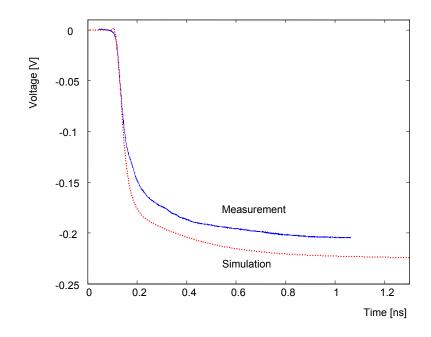
$$C = \operatorname{sqrt}(8.2) / \{3e8^* [60 - 18 \cdot \exp(-f/3e9)]\} \quad F/m$$

The simulated results are shown in Figure 4.14 and 4.15 and have been correlated with measurements. In both the time and frequency domain, the simulations show good correlation with measurements, which verifies the accuracy of the non-physical RLGC models for silicon substrate with slow-wave propagation effect.

Comparing to the RLGC parameters in Equation (4.2) for the high-resistivity silicon co-planar line in Figure 4.2, the RLGC parameters in Equation (4.12) have higher R and G values because of the thinner SiO2 thickness and slow-wave effect. In addition, the effective dielectric constant was increased from 4.9 to 8.2, as the name 'slow-wave effect' implied. It implies that for a co-planar line on 100  $\Omega$ -cm resistivity silicon substrate with the same cross-section as in Figure 4.2, the compensated RLGC parameters of the co-planar line without slow-wave effect are different from the RLGC parameters in Equation (4.2) due to slow-wave effect.



**Figure 4.14** Frequency-domain correlation between simulation and measurement for the coplanar line on 100  $\Omega$ -cm resistivity silicon substrate.



**Figure 4.15** Time-domain correlation between simulation and measurement for the coplanar line on 100  $\Omega$ -cm resistivity silicon substrate.

#### 4.5. Selection and optimization of transmission lines on silicon substrate

In this section, based on the discussions on silicon transmission lines, the silicon coplanar line for the wafer-level package test vehicle described in Chapter 1 was optimized for achieving good signal integrity.

#### 4.5.1. Fabricated silicon transmission lines

For choosing the appropriate silicon transmission line for the test vehicle, co-planar transmission lines were fabricated on 4-inch wafers using the following five silicon structures, as shown in Figure 4.16.

wafer1: 0.2um thickness Au - 2um thickness Cu - 0.2um thickness Ti -

1um thickness SiO2 on 2000  $\Omega$ -cm silicon wafer.

wafer2: 0.2um thickness Au - 3um thickness Cu - 0.2um thickness Ti -

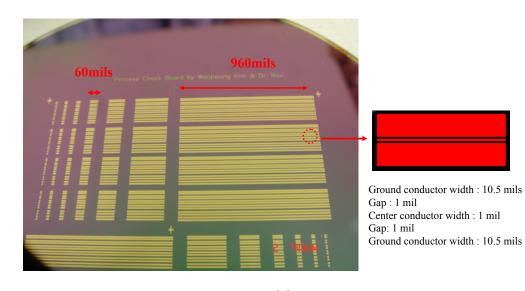
1um thickness SiO2 on 2000  $\Omega$ -cm silicon wafer.

wafer3: 0.2um thickness Au - 3um thickness Cu - 0.2um thickness Ti -

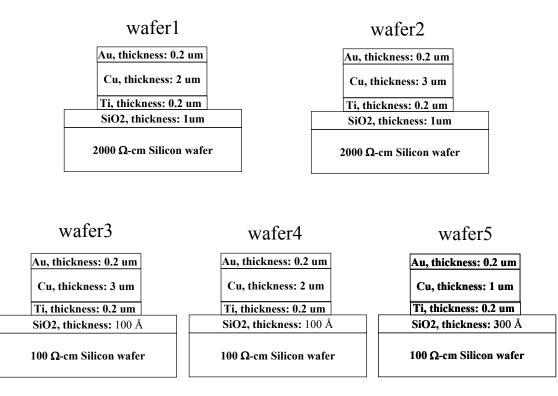
10nm thickness SiO2 on 100  $\Omega$ -cm silicon wafer.

- wafer4: 0.2um thickness Au 2um thickness Cu 0.2um thickness Ti 10nm thickness SiO2 on 100  $\Omega$ -cm silicon wafer.
- wafer5: 0.2um thickness Au 1um thickness Cu 0.2um thickness Ti 30nm thickness SiO2 on 100  $\Omega$ -cm silicon wafer.

Wafer1 and wafer2 used a high-resistivity silicon substrate with  $\rho$ =2000  $\Omega$ -cm, and wafer3, wafer4 and wafer 5 used a low-resistivity silicon substrate with  $\rho$ =100  $\Omega$ -cm. The co-planar silicon transmission lines in Figure 4.16(a) were patterned using the Au-Cu-Ti layers in Figure 4.16(b). The coplanar lines had a center conductor width of 1 mil and a gap between conductors of 1 mil. The width of each ground conductor was 10.5 mils. The coplanar lines were measured using TDR and NA for comparison. The length of the co-planar lines measured using NA was 60 mils. The longest co-planar lines had a length of 960 mils, which were used for TDR measurements.



(a)



(b)

Figure 4.16 Fabricated silicon transmission lines. (a) top view and (b) cross-section.

#### 4.5.2. Comparison using TDR measurements

TDR measurements of the co-planar lines on wafer1, 2, 3 and 4 are shown in Figure 4.17. The length of the co-planar lines was 960 mils. The far end of the co-planar lines was unterminated. Time Domain Reflectometry (TDR) having a step pulse with 30ps risetime and 250mV amplitude was used.

As shown in Figure 4.17, the TDR response for wafer3 and wafer4 are similar to lumped resistors due to slow-wave propagation effect, which implies that the transmission loss of wafer3 and wafer4 is very high. On the contrary, wafer1 and wafer2 show good time-domain response since they do not include slow-wave propagation effect. To achieve better signal integriy in the wafer-level package test vehicle, wafer1 or wafer2 should be chosen since they have lower loss. Between wafer1 and wafer2, wafer2 showed slightly larger round-trip reflection since the co-planar line on wafer2 had thicker conductors, which implied that wafer2 had a smaller loss than wafer1. Therefore, from the TDR measurements in Figure 4.17, wafer2 was chosen for the wafer-level package test vehicle.

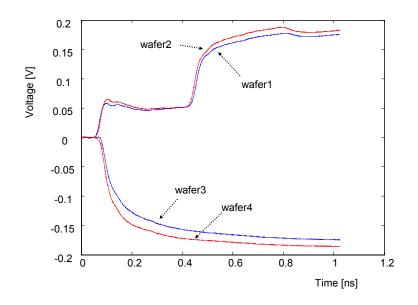


Figure 4.17 TDR measurements for the co-planar line on four silicon wafers.

#### 4.5.3. Comparison using Network Analyzer measurements

The co-planar lines used for VNA comparison had a center conductor of width 1 mil, gap of 1 mil, and length of 60 mils. The co-planar lines on the five wafers were measured using Network Analyzer from 50MHz to 10GHz, as shown in Figure 4.18 on the Smith chart. From the VNA measurements in Figure 4.18, it is clear that wafer1 and wafer2 do not include slow-wave propagation effect, but wafer3, wafer4 and wafer5 suffer from slow-wave propagation effect. Therefore, wafer1 and wafer2 had smaller loss than wafer3, wafer4 and wafer5. Between wafer1 and wafer2, since wafer2 had better time-domain response in Figure 4.17, wafer2 was finally chosen for the silicon transmission line in the wafer-level package test vehicle.

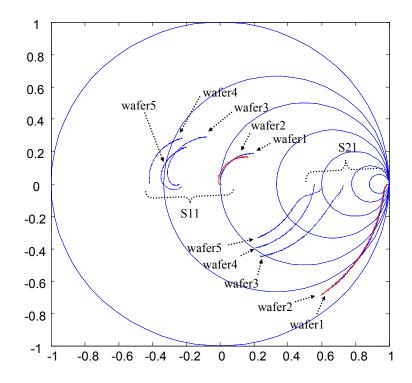


Figure 4.18 Network Analzyer measurements for the co-planar lines on five wafers.

#### 4.6. Thermal, passivation and underfill effect on signal propagation

In this section, the effect of passivation, underfill and curing on signal propagation has been discussed for silicon transmission lines. For investigating the effect, co-planar silicon lines with 60 mil length and cross-section similar to wafer2 in Figure 4.15 were fabricated and measured using a Network Analyzer.

#### 4.6.1. Thermal effect

Before and after curing, the co-planar silicon lines were measured using a Network Analyzer, as shown in Figure 4.19. In Figure 4.19, the magnitude of S21 is shown. After thermal cycling, the loss of the silicon lines was reduced. This is probably because thermal cycling removes the moisture inside the lines, making the contacts better.

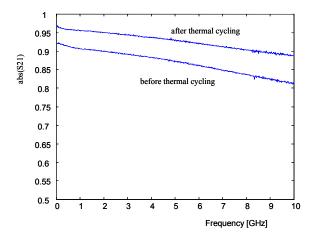


Figure 4.19 Effect of thermal cycling on S21 of silicon transmission lines.

#### 4.6.2. Passivation and Thermal effect

Three measurements were compared to investigate the effect of passivation and curing on the electrical property of silicon lines. First, the fabricated silicon lines with 60 mil length measured using a NA. Then, polyimide with 4mil thickness was spin-coated on the silicon lines and measured again. Finally, thermal cycling was applied to the silicon lines with polyimide. The magnitude of S21 of the three VNA measurements is shown in Figure 4.20. As shown in Figure 4.20, the polyimide coating increased the loss. However, similar to Figure 4.19, thermal cycling reduced the overall loss of the silicon lines.

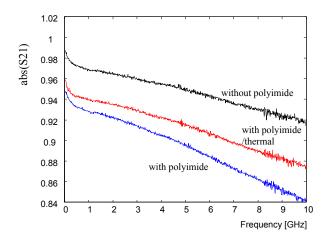


Figure 4.20 Effect of polyimide and thermal cycling on S21 of silicon lines.

#### 4.6.3. Underfill effect

The effect of underfill was investigated on the fabricated silicon lines. The underfill used had the dielectric constant and loss tangent shown in Figure 4.21, from 1Hz and 10KHz.

Frequency (Hz)	Dielectric constant	Loss factor
1	3.15	0.0032
10	3.14	0.0031
100	3.13	0.0062
1000	3.12	0.0100
10000	3.08	0.0185

Figure 4.21 Electrical characteristics of an underfill used.

In Figure 4.22, the magnitude of S21 of the silicon lines with and without the underfill is compared. As shown in Figure 4.22, the underfill material increased the loss, but the effect of the underfill was not severe since the loss of the silicon substrate was much higher than that of the underfill.

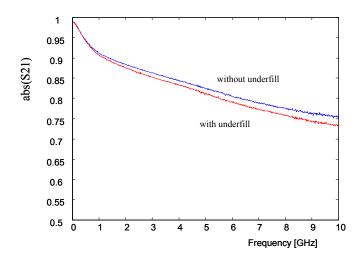


Figure 4.22 Effect of underfill on S21 of the silicon lines.

#### 4.7. Summary

In this chapter, silicon transmission lines were characterized using TDR and NA measurements. Co-planar lines on two silicon substrates with  $\rho$  = 2000  $\Omega$ -cm and  $\rho$  = 100 Ω-cm were fabricated and characterized. While co-planar lines on silicon substrate with  $\rho$  = 2000  $\Omega$ -cm does not include slow-wave propagation effect, co-planar lines on silicon substrate with  $\rho$  = 100  $\Omega$ -cm contain slow-wave propagation effect. Co-planar lines on silicon substrate with  $\rho$  = 2000  $\Omega$ -cm were characterized using the TDR characterization method described in Chapter 3. However, co-planar lines on silicon substrate with  $\rho$  = 100  $\Omega$ -cm were characterized using NA measurements since the TDR characterization method could not be applied to transmission lines including slow-wave effect. For characterizing and simulating the co-planar lines on silicon substrate containing slow-wave effect, non-physical RLGC models for silicon substrate with slowwave propagation effect were developed. Based on the non-physical RLGC models, the characteristic impedance, propagation constant and slow-wave propagation effect were extracted and simulated showing good correlation with measurements. For the silicon line in the wafer-level package test vehicle described in Chapter 1, the co-planar line on 2000  $\Omega$ -cm resistivity silicon substrate was selected with the following cross-section of the coplanar lines: 0.2um thickness Au, 3um thickness Cu, 0.2um thickness Ti and 1um thickness SiO<sub>2</sub> on 2000  $\Omega$ -cm silicon wafer.

### **Chapter 5**

### Characterization of Multi-conductor Transmission Lines

In this chapter, a TDR characterization method is described for multi-conductor package transmission lines. This method is an extension of the TDR characterization method described for single transmission lines in Chapter 3. Non-physical RLGC models for multi-conductor transmission lines have been derived for simulating the transient response using the extracted data from TDR measurements. As an example, coupled lines have been fabricated and characterized using the TDR method. The accuracy of the TDR characterization technique and non-physical RLGC models for coupled lines have been evaluated through correlation between simulations and measurements. Differential lines have also been fabricated and characterized. The method discussed has been extended to multi-conductor transmission lines including asymmetric coupled lines, (3+1)-conductor transmission lines and (64+1)-conductor transmission lines.

#### 5.1. Symmetric coupled lines

The characterization technique for coupled lines is based on the in-situ characterization technique for transmission lines explained in Chapter 3. The in-situ characterization method can be used to extract the frequency-dependent characteristic impedance and propagation constant from the TDR measurement of two-conductor transmission lines. This method has been extended to coupled lines in this section.

147

#### 5.1.1. Fabricated coupled lines

Dimensions of microstrip coupled lines fabricated at the Packaging Research Center are shown in Figure 5.1. Coupled lines were patterned on one side of an LCP (Liquid Crystal Polymer) dielectric sheet which had a thickness of 2 mils. The other side of the LCP dielectric sheet was covered by metal.

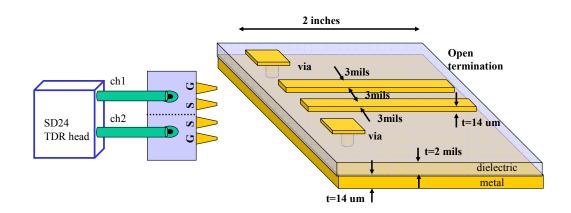


Figure 5.1 Dimensions of fabricated microstrip coupled line and measurement setup.

Vias were used to connect the ground pads to the bottom ground plane. The metal thickness was 0.5 oz. (14um) and the diameter of vias was 6 mils. The width and length of the signal conductors were 3 mils and 2000 mils, respectively. A Ground-Signal-Signal-Ground (GSSG) microprobe with a pitch of 150um from Cascade Microtech was used for TDR measurement.

#### 5.1.2. Even- and odd-mode TDR measurements

Since the fabricated microstrip coupled lines are symmetric, ch1 and ch2 of the TDR head in Figure 5.1 were used to measure the TDR waveforms for even- and odd-mode excitations. The measured even and odd-mode TDR waveforms are shown in Figure 5.2. The TDR equipment used had an amplitude of 250mV and a risetime of 30ps.

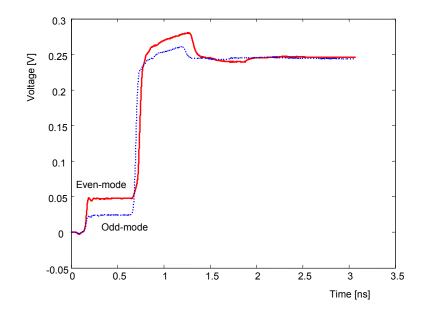


Figure 5.2 TDR measurement of the even and odd mode waveforms for the coupled line

### 5.1.3. Extraction of the even- and odd-mode characteristic impedance and propagation constant

The in-situ TDR characterization technique for single transmission lines described in Chapter 3 enables the extraction of the characteristic impedance and propagation constant of transmission lines. Hence, from Figure 5.2, the characteristic impedance and propagation constant for each mode can be extracted. In other words, the even-mode characteristic impedance and propagation constant can be extracted from the evenmode TDR measurement, and the odd-mode characteristic impedance and propagation constant can be extracted from the odd-mode TDR measurement.

Then, using the in-situ characterization method, the even-mode characteristic impedance and propagation constant were extracted from the even-mode TDR measurement as shown below:

$$ZO_{e} = 73.9 \quad \Omega$$

$$\alpha_{e} = 13/\sqrt{10e9} \cdot \sqrt{f} \quad Np/m \qquad (5.1)$$

$$Vp_{e} = 3e8/\sqrt{2.6} \quad m/s$$

149

where  $Z0_e$  is the even-mode characteristic impedance,  $\alpha_e$  is the even-mode attenuation constant, and Vp<sub>e</sub> is the even-mode effective phase velocity. The odd-mode characteristic impedance and propagation constant were also extracted from the odd-mode TDR waveform as shown below:

$$ZO_{o} = 60.8 \quad \Omega$$
  

$$\alpha_{o} = 13 / \sqrt{10e9} \cdot \sqrt{f} \quad Np / m \qquad (5.2)$$
  

$$Vp_{o} = 3e8 / \sqrt{2.3} \quad m / s$$

where Z0<sub>o</sub> is the odd-mode characteristic impedance,  $\alpha_o$  is the odd-mode attenuation constant, and Vp<sub>o</sub> is the odd-mode effective phase velocity.

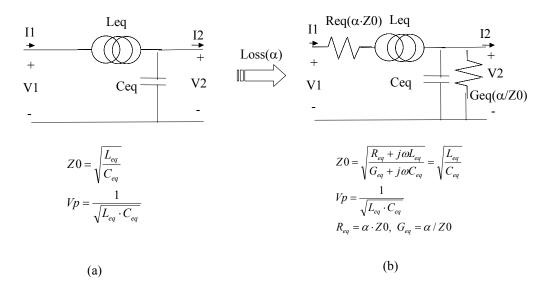
#### 5.1.4. Derivation of non-physical RLGC models for symmetric coupled lines

Non-physical RLGC models for symmetric coupled lines are derived using a procedure similar to Chapter 3. These models can be used to simulate the extracted data of the coupled line from TDR measurements.

### 5.1.4.1. Extraction procedure for non-physical RLGC models in single transmission lines

In this section, the non-physical RLGC models derived in Chapter 3 are extended to coupled lines with (n+1)-conductors. The procedure for developing non-physical RLGC models for single transmission lines in Chapter 3 has been summarized in this section. First, consider a lossless transmission line as shown in Figure 5.3(a). A small section of the lossless transmission line has the RLGC model in Figure 5.3(a) consisting of inductance and capacitance parameters. The characteristic impedance and phase velocity of the lossless line are also shown in the figure. Next, consider a lossy transmission line has the section of the lossy transmission line in Figure 5.3(b). A small section of the lossy transmission line has the non-physical RLGC model in Figure 5.3(b) after adding resistance and conductance.

Based on the derivation in Chapter 3, the characteristic impedance and phase velocity of the lossy transmission line in Figure 5.3(b) are identical to those of the lossless transmission line in Figure 5.3(a). From the characteristic impedance, the resistance and conductance in Figure 5.3(b) can be extracted.



**Figure 5.3** (a) Lossless non-physical RLGC model and (b) lossy non-physical RLGC model for single transmission line. Z0 is the characteristic impedance,  $\alpha$  is the attenuation constant in Np/m, Leq is the per-unit-length inductance, Ceq is the per-unit-length capacitance, Req is the per-unit-length resistance, and Geq is the per-unit-length conductance.

The procedure for extracting the non-physical RLGC model for single transmission lines can be summarized as follows:

- Step 1) Consider a lossless transmission line. Find the expression of the characteristic impedance and phase velocity of the lossless RLGC model in terms of the per-unit-length capacitance and inductance.
- Step 2) Obtain the general lossy RLGC model for lossy transmission lines by adding the per-unit-length resistance and conductance.

- Step 3) Substitute the per-unit-length capacitance and inductance with their associated impedance and admittance for the lossy RLGC model in the characteristic impedance expression. The associated impedance becomes Req+jω·Leq, and the associated admittance becomes Geq+jω·Ceq. Then, the expression for the characteristic impedance of the lossy transmission line can be extracted.
- Step 4) In non-physical RLGC models, the lossy and lossless transmission lines have identical expressions for characteristic impedance and phase velocity. Therefore, from the expression for the characteristic impedance of the lossy transmission line, Req =  $\alpha$ ·Z0 and Geq =  $\alpha$ /Z0, where  $\alpha$  is the attenuation constant in Np/m and Z0 is the characteristic impedance.

The four steps described above have been extended for developing non-physical RLGC models for coupled lines.

#### 5.1.4.2. Step 1: RLGC models for lossless symmetric coupled lines

Based on the non-physical RLGC model extraction procedure, the lossless RLGC model for symmetric coupled lines is shown in Figure 5.4.

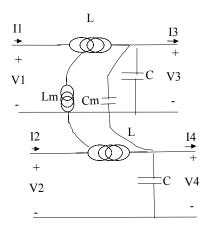


Figure 5.4 RLGC model for symmetric lossless coupled lines.

In the figure, L and C are the self inductance and capacitance, respectively, and Lm and Cm are the mutual inductance and coupling capacitance of the coupled lines, respectively. Then, the characteristic impedance and phase velocity of the lossless coupled line can be obtained using the equivalent circuits in Figure 5.5.

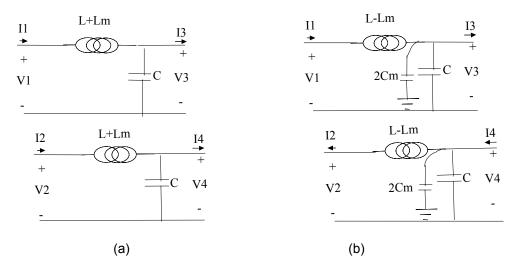


Figure 5.5 (a) Even-mode equivalent circuit and (b) odd-mode equivalent circuit for symmetric lossless coupled lines.

For the even mode excitation, since the same voltage is applied to the two signal lines, there is no electric field between the two conductors and hence the coupling capacitance is removed. In addition, since the currents of the two signal lines flow in the same direction, the magnetic fields rotate in the same direction thereby increasing the inductance, as shown in Figure 5.5(a). For the odd mode excitation, since opposite voltages are applied to the two signal lines, the coupling capacitance doubles, as shown in Figure 5.5(b). In addition, the current in the two signal lines flow in opposite directions thereby decreasing the inductance. Then, from the equivalent circuits in Figure 5.5, the characteristic impedance and phase velocity of even and odd mode excitations can be written as:

$$Z0_{e} = \sqrt{\frac{L+Lm}{C}}, Vp_{e} = \frac{1}{\sqrt{(L+Lm) \cdot C}}$$

$$Z0_{o} = \sqrt{\frac{L-Lm}{C+2Cm}}, Vp_{o} = \frac{1}{\sqrt{(L-Lm)(C+2Cm)}}$$
(5.3)

where  $Z0_e$  and  $Z0_o$  are the even- and odd-mode characteristic impedance, and  $Vp_e$  and  $Vp_o$  are the even and odd-mode effective phase velocities of lossless symmetric coupled lines, respectively.

#### 5.1.4.3. Step 2: RLGC models for lossy symmetric coupled lines

The next step is to compute the characteristic impedance of lossy coupled lines by substituting the inductance and capacitance with their associated impedance and admittance. The general coupled-line RLGC model for lossy symmetric coupled lines is shown in Figure 5.6 where R, G, Rm and Gm represent the loss in coupled lines.

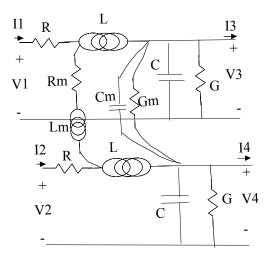


Figure 5.6 General RLGC model of symmetric lossy coupled lines.

## 5.1.4.4. Step 3: Extraction of the characteristic impedance of lossy symmetric coupled lines

By substituting the inductance and capacitance with their associated impedance and admittance in the characteristic impedance equation, the even and odd-mode characteristic impedance and phase velocity of symmetric lossy coupled lines can be written as:

$$Z0_{e} = \sqrt{\frac{(R+j\omega L) + (Rm+j\omega Lm)}{G+j\omega C}} = \sqrt{\frac{L+Lm}{C}}$$

$$Z0_{o} = \sqrt{\frac{(R+j\omega L) - (Rm+j\omega Lm)}{(G+j\omega C) + 2(Gm+j\omega Cm)}} = \sqrt{\frac{L-Lm}{C+2Cm}}$$

$$Vp_{e} = \frac{1}{\sqrt{(L+Lm) \cdot C}}$$

$$Vp_{o} = \frac{1}{\sqrt{(L-Lm)(C+2Cm)}}$$
(5.4)

where  $ZO_e$  and  $ZO_o$  are the even- and odd-mode characteristic impedance,  $Vp_e$  and  $Vp_o$  are the even- and odd-mode phase velocity, respectively.

#### 5.1.4.5. Step 4: Extraction of resistance and conductance

From Equation (5.4), the following relationships can be obtained for extracting the resistance and conductance.

$$R + Rm = \alpha_e \cdot Z0_e$$

$$G = \alpha_e / Z0_e$$

$$R - Rm = \alpha_o \cdot Z0_o$$

$$G + 2Gm = \alpha_o / Z0_o$$
(5.5)

where  $\alpha_e$  is the even-mode attenuation constant in NP/m and  $\alpha_o$  is the odd-mode attenuation constant in Np/m.

#### 5.1.4.6. Non-physical RGLC models for symmetric coupled lines

From Equation (5.3) and (5.5), using the even- and odd-mode characteristic impedances, phase velocities and losses, the non-physical RLGC model for symmetric coupled lines can be written as:

$$L = \frac{1}{2} \left\{ \frac{ZO_e}{Vp_e} + \frac{ZO_o}{Vp_o} \right\} [H/m] \qquad C = \frac{1}{ZO_e \cdot Vp_e} [F/m]$$

$$R = \frac{1}{2} \left\{ \alpha_e \cdot ZO_e + \alpha_o \cdot ZO_o \right\} [\Omega/m] \qquad G = \frac{\alpha_e}{ZO_e} [S/m]$$

$$L_m = \frac{1}{2} \left\{ \frac{ZO_e}{Vp_e} - \frac{ZO_o}{Vp_o} \right\} [H/m] \qquad C_m = \frac{1}{2} \left\{ \frac{1}{ZO_o \cdot Vp_o} - \frac{1}{ZO_e \cdot Vp_e} \right\} [F/m]$$

$$R_m = \frac{1}{2} \left\{ \alpha_e \cdot ZO_e - \alpha_o \cdot ZO_o \right\} [\Omega/m] \qquad G_m = \frac{1}{2} \left\{ \frac{\alpha_o}{ZO_o} - \frac{\alpha_e}{ZO_e} \right] [S/m]$$
(5.6)

From Maxwell's equations, L, C, Lm and Cm are the same as those of physical RLGC models for coupled lines. The *R*, *L*, *G*, *C* matrices of symmetric coupled lines can then be expressed as:

$$R = \begin{bmatrix} R & Rm \\ Rm & R \end{bmatrix}, \quad L = \begin{bmatrix} L & Lm \\ Lm & L \end{bmatrix}$$

$$G = \begin{bmatrix} G + Gm & -Gm \\ -Gm & G + Gm \end{bmatrix}, \quad C = \begin{bmatrix} C + Cm & -Cm \\ -Cm & C + Cm \end{bmatrix}$$
(5.7)

The frequency-dependent *R*, *L*, *G*, *C* matrices in Equation (5.7) can be simulated using tabular W-element models in Hspice.

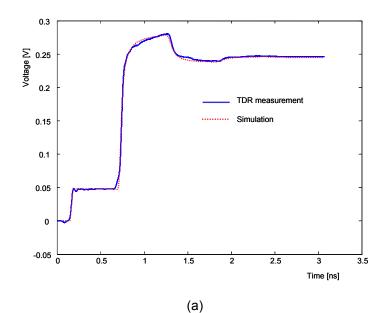
#### 5.1.5. Time-domain Model-to-Hardware correlation

The accuracy of the proposed TDR characterization method and non-physical RLGC models for coupled lines has been evaluated using TDR measurements. The measured characteristic impedance and propagation constant for symmetric coupled lines shown in Equation (5.1) and (5.2) were simulated using the non-physical RLGC model, described in Equation (5.6) and (5.7). The coupled line in Figure 5.1 had the following RLGC parameters, which were extracted directly from measurements:

L = 352.28 nH/m, C = 72.73 pF/m  
R = 
$$877.55/\sqrt{10e9} \cdot \sqrt{f}$$
  $\Omega/m$ , G= $0.176/\sqrt{10e9} \cdot \sqrt{f}$  S/m  
Lm = 44.9 nH/m, Cm = 5.27 pF/m (5.8)  
Rm =  $85.15/\sqrt{10e9} \cdot \sqrt{f}$   $\Omega/m$ , Gm =  $0.019/\sqrt{10e9} \cdot \sqrt{f}$  S/m

The simulated even- and odd-mode waveforms using Equation (5.8) have been

compared with TDR measurements in Figure 5.7. The simulation results show good correlation with the even- and odd-mode TDR measurements, demonstrating the accuracy of the extracted data and the non-physical RLGC model in Equation (5.6).



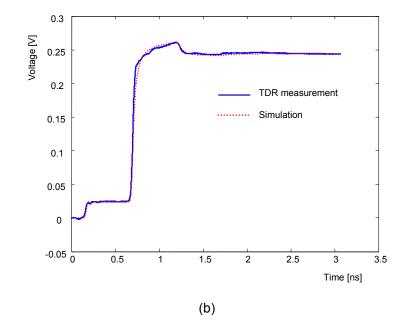


Figure 5.7 Comparison between simulation and TDR measurement for (a) evenmode and (b) odd-mode.

The extracted data in Equation (5.1) and (5.2) and the non-physical RLGC model in Equation (5.6) and (5.7) were also applied for single line excitation, as shown in Figure 5.8. With only ch1 excited using a step pulse, ch1 and ch2 were used to measure the reflected and crosstalk signals. The measured waveforms for the single line excitation have also been compared to simulations, as shown in Figure 5.9. The simulations and measurements show good correlation, further verifying the accuracy of the extracted data and non-physical RLGC model for coupled lines. The small difference in Figure 5.9(b) was due to the imperfect open termination.

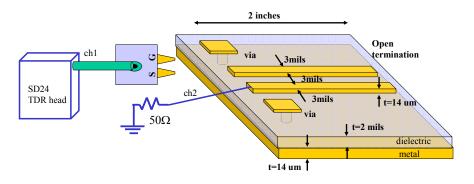
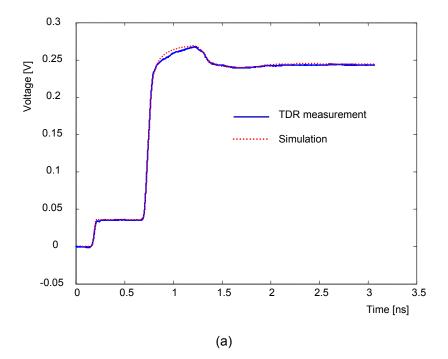
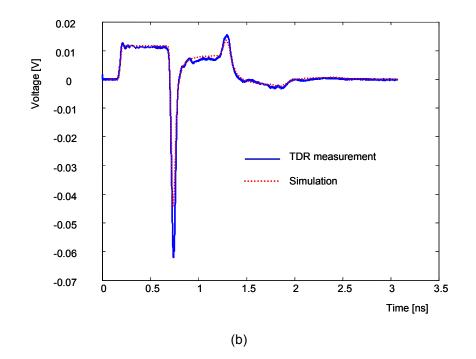


Figure 5.8 Single-line excitation of microstrip coupled lines.





**Figure 5.9** Comparison between simulations and TDR measurements for coupled line with single excitation. (a) ch1 and (b) ch2.

#### 5.1.6. Co-planar coupled lines

Co-planar coupled lines were also fabricated, measured and characterized using TDR measurements, as shown in Figure 5.10.

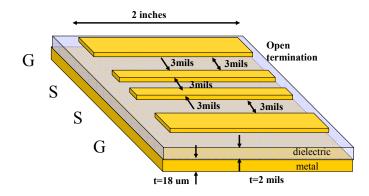


Figure 5.10 Fabricated co-planar coupled lines.

The coupled lines in Figure 5.10 do not have via connections. Instead, they have ground lines next to signal lines. The dielectric sheet was a polyimide film with 2 mils in

thickness (Upilex from UBE Industries, LTD), which has a dielectric constant of 3.2 and a loss-tangent of 0.0023. The metal thickness was 18um, the two signal conductors had a metal width of 3 mils, the gap between metal was 3 mils, and the length of coupled lines was 2 inches. The even- and odd-mode TDR measurements of the coupled line are shown in Figure 5.11. Using the in-situ TDR characterization method, the even- and odd-modes of the coupled line were characterized, which yielded the following parameters:

$$ZO_{e} = 92.2 \ \Omega$$

$$\alpha_{e} = \frac{2}{\sqrt{10e9}} \cdot \sqrt{f} + \frac{3}{10e9} \cdot f \qquad Np/m$$

$$Vp_{e} = 3e8/\sqrt{2.5} \qquad m/s$$

$$ZO_{o} = 69.4 \ \Omega$$

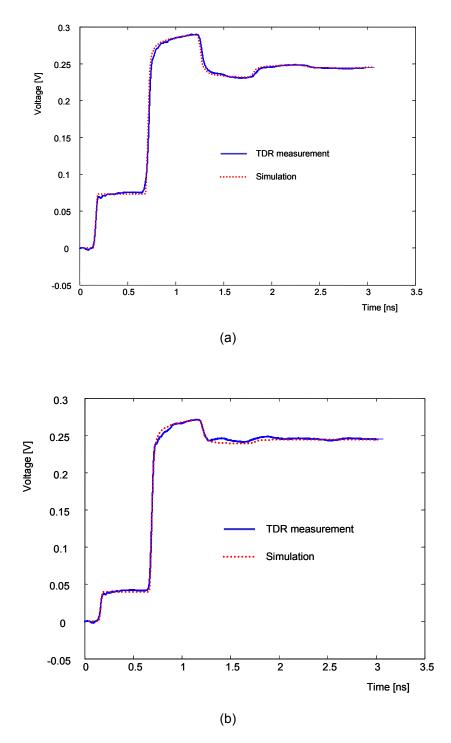
$$\alpha_{o} = \frac{1.7}{\sqrt{10e9}} \cdot \sqrt{f} + \frac{4}{10e9} \cdot f \qquad Np/m$$

$$Vp_{o} = 3e8/\sqrt{2.3} \qquad m/s$$
(5.9)

Then, using Equation (5.9) along with the non-physical RLGC model described in Equations (5.6) and (5.7), the coupled line in Figure 5.10 can be simulated using Hspice W-element Tabular models. The RLGC parameters for the co-planar lines are as shown below:

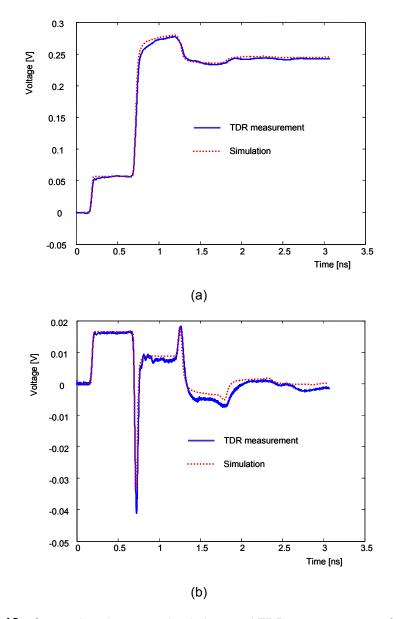
L = 418.39 nH/m, C = 57.16 pF/m  
R = 
$$151.19/\sqrt{10e9} \cdot \sqrt{f} + 277.1/10e9 \cdot f \ \Omega/m$$
 (5.10)  
G= $(2/\sqrt{10e9} \cdot \sqrt{f} + 3/10e9 \cdot f)/92.2 \ S/m$   
Lm = 67.55 nH/m, Cm = 7.84 pF/m  
Rm =  $33.21/\sqrt{10e9} \cdot \sqrt{f} - 0.5/10e9 \cdot f \ \Omega/m$   
Gm =  $0.0014/\sqrt{10e9} \cdot \sqrt{f} + 0.012/10e9 \cdot f \ S/m$ 

The simulation results have been compared to TDR measurements in Figure 5.11, showing good correlation.



**Figure 5.11** Comparison between simulations and TDR measurements for (a) the evenmode and (b) odd-mode of the coupled line in Figure 5.10.

Similar to Figure 5.8, a single line excitation was also applied to the co-planar coupled line in Figure 5.10. The measurement and simulation results have been compared in Figure 5.12. The simulation and measurement results for single line excitation also show good correlation in Figure 5.12, verifying the accuracy of the extracted data and the non-physical RLGC model for coupled lines.



**Figure 5.12** Comparison between simulations and TDR measurements of single-line excitation for the coupled line in Figure 5.10. (a) ch1 and (b) ch2.

#### 5.1.7. Non-physical RLGC models for silicon coupled lines with slow-wave mode

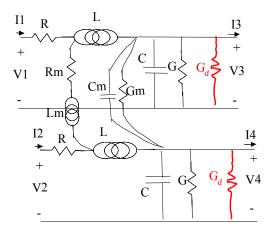
Similar to the co-planar lines on silicon substrate described in Chapter 4, the loss effect due to silicon substrate can be included in the non-physical RLGC models for coupled lines in Figure 5.6, as shown in Figure 5.13. In Figure 5.13,  $G_d$  represents the loss due to the electric field inside the silicon substrate, as explained in Chapter 4. In Figure 5.13,  $G_d$  can be frequency-dependent and complex, but a real-valued  $G_d$  showed good correlation with measurements, as described in Chapter 4 for the low resistivity silicon substrate. Then, assuming a real-valued  $G_d$ , non-physical RLGC models for symmetric coupled lines on silicon substrate can be expressed as shown in Equation (5.11). The parameters can be simulated with the RLGC matrices in Equation (5.7) using Hspice W-element Tabular models.

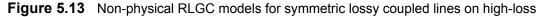
$$L = \frac{1}{2} \{ \frac{Z0_{e}}{Vp_{e}} + \frac{Z0_{o}}{Vp_{o}} \} [H/m] \qquad C = \frac{1}{Z0_{e} \cdot Vp_{e}} [F/m]$$

$$R = \frac{1}{2} \{ \alpha_{e} \cdot Z0_{e} + \alpha_{o} \cdot Z0_{o} \} [\Omega/m] \qquad G = \frac{\alpha_{e}}{Z0_{e}} + G_{d} [S/m]$$

$$L_{m} = \frac{1}{2} \{ \frac{Z0_{e}}{Vp_{e}} - \frac{Z0_{o}}{Vp_{o}} \} [H/m] \qquad C_{m} = \frac{1}{2} \{ \frac{1}{Z0_{o} \cdot Vp_{o}} - \frac{1}{Z0_{e} \cdot Vp_{e}} \} [F/m]$$

$$R_{m} = \frac{1}{2} \{ \alpha_{e} \cdot Z0_{e} - \alpha_{o} \cdot Z0_{o} \} [\Omega/m] \qquad G_{m} = \frac{1}{2} \{ \frac{\alpha_{o}}{Z0_{o}} - \frac{\alpha_{e}}{Z0_{e}} \} [S/m]$$
(5.11)





silicon substrates.  $G_d$  is the substrate loss.

#### 5.1.8. Non-physical RLGC models for asymmetric coupled lines on board

Non-physical RLGC models for asymmetric coupled lines can also be extracted using the non-physical RLGC model extraction procedure. First, consider lossless asymmetric coupled lines. The even- and odd-mode characteristic impedances and phase velocities can be expressed in terms of the capacitance and inductance. Then, using the RLGC models of lossy asymmetric coupled lines in Figure 5.14, the even- and odd-mode characteristic impedance and phase velocity of lossy asymmetric coupled lines can be obtained by replacing the inductance and capacitance with their associated impedance and admittance. Finally, the relationship between the resistance and conductance can be found from the even- and odd-mode characteristic impedances.

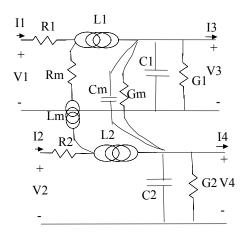


Figure 5.14 General RLGC model for asymmetric lossy coupled lines.

Then, non-physical RLGC models for lossy asymmetric coupled lines as shown in Figure 5.14 can be derived, which consist of the even- and odd-mode characteristic impedances, phase velocities and losses which can be measured using TDR measurements. The RLGC models for the asymmetric coupled lines are as shown below:

$$L1 = \frac{1}{2} \left\{ \frac{ZO_{e1}}{Vp_{e1}} + \frac{ZO_{o1}}{Vp_{o1}} \right\} [H/m] \qquad C1 = \frac{1}{ZO_{e1} \cdot Vp_{e1}} [F/m]$$

$$R1 = \frac{1}{2} \left\{ \alpha_{e1} \cdot ZO_{e1} + \alpha_{o1} \cdot ZO_{o1} \right\} [\Omega/m] \qquad G1 = \frac{\alpha_{e1}}{ZO_{e1}} [S/m]$$

$$L2 = \frac{1}{2} \left\{ \frac{ZO_{e2}}{Vp_{e2}} + \frac{ZO_{o2}}{Vp_{o2}} \right\} [H/m] \qquad C2 = \frac{1}{ZO_{e2} \cdot Vp_{e2}} [F/m]$$

$$R2 = \frac{1}{2} \left\{ \alpha_{e2} \cdot ZO_{e2} + \alpha_{o2} \cdot ZO_{o2} \right\} [\Omega/m] \qquad G2 = \frac{\alpha_{e2}}{ZO_{e2}} [S/m]$$

$$L_{m12} = \frac{1}{2} \left\{ \frac{ZO_{e1}}{Vp_{e1}} - \frac{ZO_{o1}}{Vp_{o1}} \right\} [H/m] \qquad C_{m12} = \frac{1}{2} \left\{ \frac{\alpha_{o1}}{ZO_{o1} \cdot Vp_{o1}} - \frac{1}{ZO_{e1} \cdot Vp_{e1}} \right\} [F/m] \qquad (5.12)$$

$$R_{m12} = \frac{1}{2} \left\{ \alpha_{e1} \cdot ZO_{e1} - \alpha_{o1} \cdot ZO_{o1} \right\} [\Omega/m] \qquad G_{m12} = \frac{1}{2} \left\{ \frac{\alpha_{o1}}{ZO_{o1}} - \frac{\alpha_{e1}}{ZO_{e1}} \right] [S/m]$$

$$L_{m21} = \frac{1}{2} \left\{ \frac{ZO_{e2}}{Vp_{e2}} - \frac{ZO_{o2}}{Vp_{o2}} \right\} [H/m] \qquad C_{m21} = \frac{1}{2} \left\{ \frac{\alpha_{o2}}{ZO_{o2}} - \frac{\alpha_{e2}}{ZO_{e2}} \right\} [F/m]$$

$$R_{m21} = \frac{1}{2} \left\{ \alpha_{e2} \cdot ZO_{e2} - \alpha_{o2} \cdot ZO_{o2} \right\} [\Omega/m] \qquad G_{m21} = \frac{1}{2} \left\{ \frac{\alpha_{o2}}{ZO_{o2}} - \frac{\alpha_{e2}}{ZO_{e2}} \right\} [S/m]$$

where  $ZO_{e1}$  is the port1 even-mode characteristic impedance,  $ZO_{e2}$  is the port2 evenmode characteristic impedance,  $ZO_{o1}$  is the port1 odd-mode characteristic impedance,  $ZO_{o2}$  is the port2 odd-mode characteristic impedance,  $Vp_{e1}$  is the port1 even-mode phase velocity,  $Vp_{e2}$  is the port2 even-mode phase velocity,  $Vp_{o1}$  is the port1 odd-mode phase velocity,  $Vp_{o2}$  is the port2 odd-mode phase velocity,  $\alpha_{e1}$  is the port1 even-mode attenuation constant,  $\alpha_{e2}$  is the port2 even-mode attenuation constant,  $\alpha_{o1}$  is the port1 odd-mode attenuation constant and  $\alpha_{o1}$  is the port1 odd-mode attenuation constant in NP/m. In Equation (5.12), Lm12 = Lm21 = Lm; Cm12 = Cm21 = Cm; Rm12 = Rm21 = Rm; and Gm12 = Gm21 = Gm. According to Maxwell's equations, L1, C1, L2, C2, Lm and Cm are the same as those of physical RLGC models. The *R*, *L*, *G*, and *C* matrices of lossy asymmetric coupled lines can then be expressed as:

$$R = \begin{bmatrix} R1 & Rm12 \\ Rm21 & R2 \end{bmatrix}, L = \begin{bmatrix} L1 & Lm12 \\ Lm21 & L2 \end{bmatrix}$$
$$G = \begin{bmatrix} G1 + Gm12 & -Gm12 \\ -Gm21 & G2 + Gm21 \end{bmatrix}, C = \begin{bmatrix} C1 + Cm12 & -Cm12 \\ -Cm21 & C2 + Cm21 \end{bmatrix}$$
(5.13)

The frequency-dependent *R*, *L*, *G*, and *C* matrices in Equation (5.13) can be simulated using tabular W-element models in Hspice.

# 5.2. Differential transmission lines

Differential lines are characterized using TDR measurements in this section. Differential lines are coupled lines where only the odd-mode excitation is used. Since differential lines require two conductors for each signal, differential lines are not efficient for high-density interconnection schemes. However, differential lines work well in the presence of noise [E1].

# 5.2.1. Fabricated differential lines

Dimensions of differential lines fabricated at the Packaging Research Center are shown in Figure 5.15. Differential lines were patterned on one side of an LCP (Liquid Crystal Polymer) dielectric sheet which had a thickness of 2 mils. The other side of the LCP dielectric sheet was covered by metal. The metal thickness was 0.5 oz. (14um).

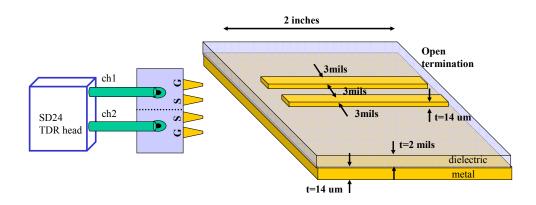
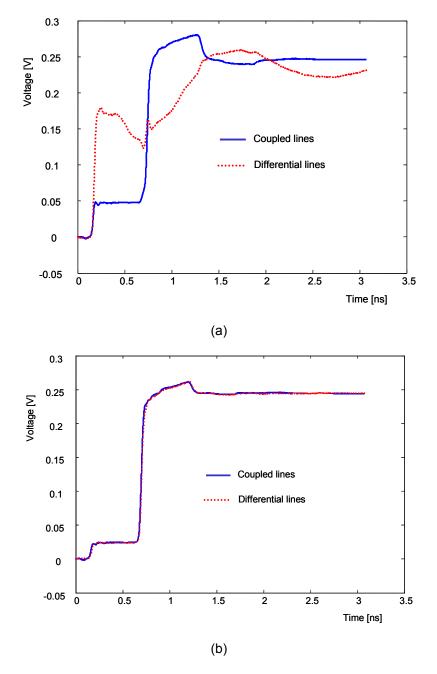


Figure 5.15 Fabricated differential lines and measurement setup.

The width and length of the signal conductors were 3 mils and 2000 mils, respectively. A GSSG microprobe with a pitch of 150um was used for measurement. The bottom metal layer was a floating metal whose electrical potential was not defined. The differential line in Figure 5.15 was fabricated with the same dimension and material as the coupled line in Figure 5.1 except for the ground pads and vias.

# 5.2.2. Even and odd mode TDR measurements

The even and odd modes of the differential line in Figure 5.16 were measured using a method similar to the coupled line measurements in Figure 5.1.



**Figure 5.16** Comparison between the coupled line in Figure 5.1 and differential line in Figure 5.15 for the (a) even-mode and (b) odd-mode.

The measured waveforms are shown in Figure 5.16 with the measured waveforms of the coupled line in Figure 5.1. For the odd mode, the differential line in Figure 5.15 shows the same waveform as the coupled line in Figure 5.2. However, for the even mode, the differential line has a very different behaviour from the coupled line. This is because the even mode of the differential line has no ground return conductor.

#### 5.2.3. Non-physical RLGC models for differential lines

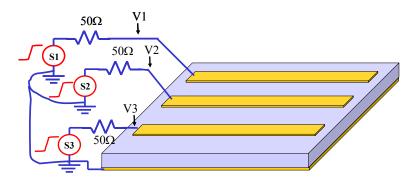
Since differential lines are coupled lines where only the odd-mode excitation is used, the non-physical RLGC models for coupled lines in Equation (5.6) and (5.7) can be also used for differential lines. Since the differential line in Figure 5.15 only uses the odd mode, the even-mode of the differential line is not used. Therefore, using the non-physical RLGC model for coupled lines in Equation (5.6), numerous non-physical RLGC models for the differential line are possible with different even modes. For example, the even mode can be made equal to the measured odd mode to reduce the number of measurements. The coupled line model in Equation (5.8) can also be used for the differential line since the odd-mode is the same. The simulation results and measurements using Equation (5.8) are shown in Figures 5.7 and Figure 5.16

While the fabricated differential line in Figure 5.15 had a bottom metal layer, differential lines without the bottom metal layer can be characterized using a method similar to the fabricated differential line. First, measure the odd mode of differential lines without the bottom metal layer and extract the characteristic impedance and propagation constant of the odd mode. Second, since the even mode of the differential lines is not used, the even mode can be assumed to be the same as the odd mode. Then, the non-physical RLGC model for the differential lines can be obtained by applying the even and odd modes to Equations (5.6) and (5.7).

168

# 5.3. Multi-conductor transmission lines

The TDR characterization method and non-physical RLGC models can be extended to general lossy (n+1)-conductor transmission lines. In this section, the characterization and modeling of general lossy (n+1)-conductor transmission lines are discussed using the example of a (3+1)-conductor transmission line. Two-conductor transmission lines represent single transmission lines which have one signal conductor and one ground plane. Three-conductor transmission lines are coupled lines which have two signal conductors above a ground plane. Similarly, (3+1)-conductor transmission lines have three signal conductors above a ground plane, and (n+1)-conductor transmission lines have n-signal conductors above one ground plane. It is important to note that the ground conductor of (n+1)-conductor transmission lines is not a floating metal, but is connected to the ground of the n signal sources. As an example, a symmetric (3+1)-conductor transmission line is shown in Figure 5.17.



**Figure 5.17** Symmetric (3+1)-conductor transmission lines.

# 5.3.1. Modes of (n+1)-conductor transmission lines

First, the modes of (n+1)-conductor transmission lines are considered for characterizing (n+1)-conductor transmission lines using TDR measurements and for developing non-physical RLGC models. The (n+1)-conductor transmission lines have

 $2^{n-1}$  modes. For example, single transmission lines have one mode, coupled lines have two modes, and (3+1)-conductor transmission lines have four modes. The modes of (3+1)-conductor transmission lines are shown in Figure 5.18. In Figure 5.18, 'e' stands for even and 'o' stands for odd mode. S1, S2 and S3 are the sources in Figure 5.17 with '+1' meaning a positive signal, and '-1' meaning a negative signal.

mode	<b>S</b> 1	S2	S3
eee	+1	+1	+1
eeo	+1	+1	-1
eoe	+1	-1	+1
e00	+1	-1	-1

Figure 5.18 Modes of (3+1)-conductor transmission lines.

# 5.3.2. TDR measurements of (n+1)-conductor transmission lines

The accurate TDR characterization of (n+1)-conductor transmission lines requires nchannel TDR equipment. Each channel represents a TDR source for (n+1)-conductor transmission lines. For example, (3+1)-conductor transmission lines require threechannel TDR equipment. Then, the 'eee' mode in Figure 5.18 can be measured using the same polarity step pulse source. The 'eeo' mode can be measured with S1 and S2 in the positive polarity and S3 in the negative polarity. The other modes can also be measured using 3-channel TDR equipment in a similar way. Among the 2<sup>n-1</sup> modes of (n+1)-conductor transmission lines, n-mode TDR measurements are required to find all the parameters of non-physical RLGC models for (n+1)-conductor transmission lines. For (3+1)-conductor transmission lines, three modes in Figure 5.18 need to be measured. Since each channel is a TDR waveform for a mode, a total of nine TDR waveforms can be measured using the three-channel TDR equipment for (3+1)- conductor transmission line.

#### 5.3.3. Extraction of the characteristic impedance and propagation constant

From each TDR waveform, the characteristic impedance and propagation constant of each mode can be extracted using the in-situ TDR characterization method described in Chapter 3. In Figure 5.19, the characteristic impedance and propagation constant of each mode is shown. In Figure 5.19,  $\gamma = \alpha + j \cdot \beta$ , where  $\alpha$  is the attenuation constant and  $\beta$  is the phase constant, and  $\beta = \omega/Vp$ , where  $\omega$  is the angular frequency and Vp is the phase velocity.

mode	S1	S2	S3
eee	$Z0_{eee1}, \gamma_{eee1}$	$Z0_{eee2}, \gamma_{eee2}$	$Z0_{eee3}, \gamma_{eee3}$
eeo	$Z0_{eeo1}, \gamma_{eeo1}$	$Z0_{eeo2}, \gamma_{eeo2}$	$Z0_{eeo3}, \gamma_{eeo3}$
eoe	$Z0_{eoe1}, \gamma_{eoe1}$	$Z0_{eoe2}, \gamma_{eoe2}$	$Z0_{eoe3}, \gamma_{eoe3}$
eoo	$Z0_{eoo1}, \gamma_{eoo1}$	$Z0_{eoo2}, \gamma_{eoo2}$	$Z0_{eoo3}, \gamma_{eoo3}$

**Figure 5.19** Characteristic impedance and propagation constant of (3+1)-conductor

# transmission lines

### 5.3.4. Non-physical RLGC models for (n+1)-conductor transmission lines

In this section, based on the non-physical RLGC model extraction procedure in Section 5.1.4.1, non-physical RLGC models for (n+1)-conductor transmission lines are developed for simulating (n+1)-conductor transmission lines.

# 5.3.4.1. Step 1: RLGC models for lossless (n+1)-conductor transmission lines

According to the non-physical RLGC model extraction procedure, lossless (n+1)conductor transmission lines can be considered fisrt. For example, the RLGC model of lossless (3+1)-conductor transmission line is shown in Figure 5.20.

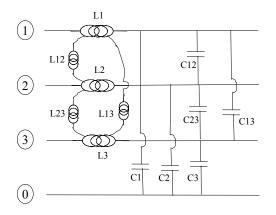


Figure 5.20 RLGC model of lossless (3+1)-conductor transmission lines.

For extracting the characteristic impedance and phase velocity of the lossless (3+1)conductor transmission line, the equivalent circuits in Figure 5.21 can be derived from the RLGC model of the lossless (3+1)-conductor transmission line in Figure 5.20.

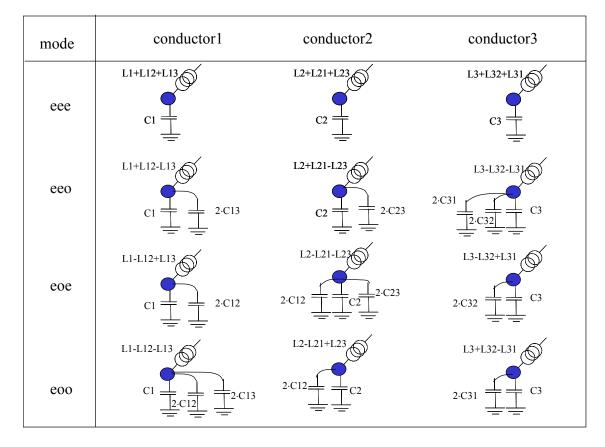


Figure 5.21 Equivalent circuits of lossless (3+1)-conductor transmission lines.

Then, from the lossless RLGC model, the characteristic impedance and phase velocity of each mode can be derived using the equivalent circuits, as shown in Figure 5.22.

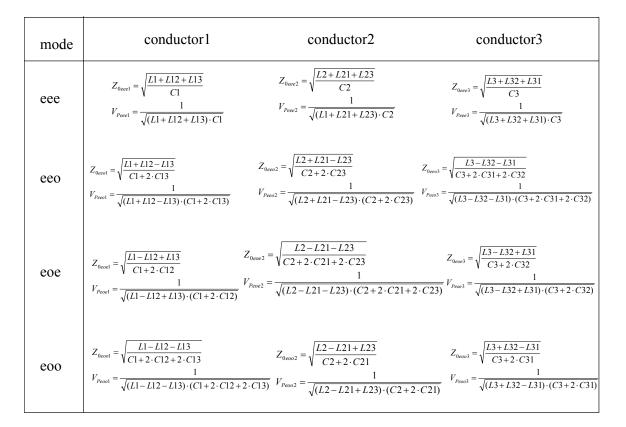


Figure 5.22 Characteristic impedances and phase velocities of lossless (3+1)-conductor

transmission lines.

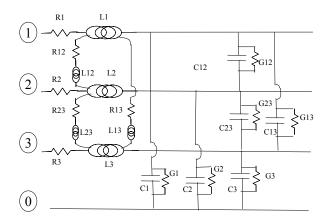


Figure 5.23 General RLGC model of (3+1)-conductor transmission lines.

# 5.3.4.2. Step 2: RLGC models for lossy (n+1)-conductor transmission lines

Next, the characteristic impedance of a lossy (n+1)-conductor transmission line can be extracted. The RLGC model of lossy (n+1)-conductor transmission lines can be obtained by inserting the resistance and conductance to the lossless RLGC model. For example, the RLGC model of lossy (3+1)-conductor transmission line is shown in Figure 5.23.

# 5.3.4.3. Step 3: Extraction of Z0 of lossy (n+1)-conductor transmission lines

The characteristic impedance of lossy (n+1)-conductor transmission line can be extracted by changing the inductance and capacitance to their associated impedance and admittance, respectively. For (3+1)-conductor transmission lines, the first three modes of Figure 5.18 can be used for extracting the non-physical RLGC model in Figure 5.23. Then, the characteristic impedance of lossy (3+1)-conductor transmission line can be expressed as:

$$\begin{aligned} Z0_{eeel} &= \sqrt{\frac{(R1+j\omega L1) + (R12+j\omega L12) + (R13+j\omega L13)}{G1+j\omega C1}} \\ Z0_{eeol} &= \sqrt{\frac{(R1+j\omega L1) + (R12+j\omega L12) - (R13+j\omega L13)}{(G1+j\omega C1) + 2 \cdot (G13+j\omega C13)}} \\ Z0_{eeol} &= \sqrt{\frac{(R1+j\omega L1) - (R12+j\omega L12) + (R13+j\omega L13)}{(G1+j\omega C1) + 2 \cdot (G12+j\omega C12)}} \\ Z0_{eeol} &= \sqrt{\frac{(R2+j\omega L2) + (R21+j\omega L21) + (R23+j\omega L23)}{G2+j\omega C2}} \\ Z0_{eeol} &= \sqrt{\frac{(R2+j\omega L2) + (R21+j\omega L21) - (R23+j\omega L23)}{(G2+j\omega C2) + 2 \cdot (G23+j\omega C23)}} \\ Z0_{eeol} &= \sqrt{\frac{(R2+j\omega L2) - (R21+j\omega L21) - (R23+j\omega L23)}{(G2+j\omega C2) + 2 \cdot (G21+j\omega C21) + 2 \cdot (G23+j\omega C23)}} \\ Z0_{eeol} &= \sqrt{\frac{(R3+j\omega L3) + (R32+j\omega L32) + (R31+j\omega L31)}{G3+j\omega C3}} \\ Z0_{eeol} &= \sqrt{\frac{(R3+j\omega L3) - (R32+j\omega L32) - (R31+j\omega L31)}{(G3+j\omega C3) + 2 \cdot (G32+j\omega C32)}} \\ Z0_{eool} &= \sqrt{\frac{(R3+j\omega L3) - (R32+j\omega L32) - (R31+j\omega L31)}{(G3+j\omega C3) + 2 \cdot (G32+j\omega C32)}} \\ Z0_{eool} &= \sqrt{\frac{(R3+j\omega L3) - (R32+j\omega L32) + (R31+j\omega L31)}{(G3+j\omega C3) + 2 \cdot (G32+j\omega C32)}} \end{aligned}$$

# 5.3.4.4. Step 4: Extraction of the resistance and conductance

From the characteristic impedance, the resistance and conductance can be extracted. For example, the following relationships can be obtained from Equation (5.14) for (3+1)-conductor transmission lines:

$R1 + R12 + R13 = \alpha_{eee1} \cdot Z0_{eee1},$	$G1 = \alpha_{eee1} / Z0_{eee1}$	
$R1 + R12 - R13 = \alpha_{eeo1} \cdot Z0_{eeo1},$	$G1 + 2 \cdot G13 = \alpha_{eeo1} / Z0_{eeo1}$	
$R1 - R12 + R13 = \alpha_{eoe1} \cdot Z0_{eoe1},$	$G1 + 2 \cdot G12 = \alpha_{eoe1} / Z0_{eoe1}$	
$R2 + R21 + R23 = \alpha_{eee2} \cdot Z0_{eee2},$	$G2 = \alpha_{eee2} / Z0_{eee2}$	(5.15)
$R2 + R21 - R23 = \alpha_{eeo2} \cdot Z0_{eeo2},$	$G2 + 2 \cdot G23 = \alpha_{eeo2} / Z0_{eeo2}$	
$R2 - R21 - R23 = \alpha_{eoe2} \cdot Z0_{eoe2},$	$G2 + 2 \cdot G21 + 2 \cdot G23 = \alpha_{eoe2} / Z0_{eoe2}$	
$R3 + R32 + R31 = \alpha_{eee3} \cdot Z0_{eee3},$	$G3 = \alpha_{eee3} / Z0_{eee3}$	
$R3 - R32 - R31 = \alpha_{eeo3} \cdot Z0_{eeo3}$ ,	$G3 + 2 \cdot G31 + 2 \cdot G32 = \alpha_{eeo3} / Z0_{eeo3}$	
$R3 - R32 + R31 = \alpha_{eoe3} \cdot Z0_{eoe3},$	$G3 + 2 \cdot G32 = \alpha_{eoe3} / Z0_{eoe3}$	

#### 5.3.4.5. Non-physical RLGC models for (n+1)-conductor transmission lines

Finally, the RLGC parameters of (n+1)-conductor transmission lines can be extracted using the relationship of characteristic impedance and phase velocity in Step 1 and Step 4. For (3+1)-conductor transmission lines, the inductance and capacitance for the (3+1)-conductor transmission lines can be extracted from Figure 5.22 as follows:

$$L1 = \frac{1}{2} \left( \frac{Z_{0ee01}}{Vp_{ee01}} + \frac{Z_{0e01}}{Vp_{ee01}} \right), \ L2 = \frac{1}{2} \left( \frac{Z_{0ee22}}{Vp_{ee22}} + \frac{Z_{0eo22}}{Vp_{eo22}} \right), \ L3 = \frac{1}{2} \left( \frac{Z_{0ee03}}{Vp_{ee03}} + \frac{Z_{0eo3}}{Vp_{ee03}} \right)$$

$$L12 = \frac{1}{2} \left( \frac{Z_{0ee01}}{Vp_{ee1}} - \frac{Z_{0eo1}}{Vp_{eo01}} \right), \ L21 = \frac{1}{2} \left( \frac{Z_{0ee02}}{Vp_{ee02}} - \frac{Z_{0eo22}}{Vp_{eo22}} \right), \ L31 = \frac{1}{2} \left( \frac{Z_{0ee03}}{Vp_{eo03}} - \frac{Z_{0eo3}}{Vp_{eo3}} \right)$$

$$L13 = \frac{1}{2} \left( \frac{Z_{0ee01}}{Vp_{ee01}} - \frac{Z_{0eo1}}{Vp_{eo01}} \right), \ L23 = \frac{1}{2} \left( \frac{Z_{0ee02}}{Vp_{ee02}} - \frac{Z_{0eo22}}{Vp_{eo22}} \right), \ L32 = \frac{1}{2} \left( \frac{Z_{0ee03}}{Vp_{eo03}} - \frac{Z_{0eo3}}{Vp_{eo3}} \right)$$

$$C13 = \frac{1}{2} \left( \frac{1}{Z_{0ee01}} \cdot Vp_{eo1}} - \frac{1}{Z_{0ee01}} \right), \ C23 = \frac{1}{2} \left( \frac{1}{Z_{0eo2}} \cdot Vp_{eo2}} - \frac{1}{Z_{0eo2}} \right), \ C31 = \frac{1}{2} \left( \frac{1}{Z_{0eo1}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo1}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo2}} \cdot Vp_{eo2}} - \frac{1}{Z_{0eo2}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo2}} \right), \ C31 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} \right), \ C32 = \frac{1}{2} \left( \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} - \frac{1}{Z_{0eo3}} \cdot Vp_{eo3}} \right)$$

From Equation (5.15), all the resistances and conductances can be extracted as follows:

$$R1 = \frac{1}{2} (\alpha_{eee1} \cdot Z0_{eee1} + \alpha_{eoe1} \cdot Z0_{eoe1}), R12 = \frac{1}{2} (\alpha_{eee1} \cdot Z0_{eee1} - \alpha_{eoe1} \cdot Z0_{eoe1})$$

$$R13 = \frac{1}{2} (\alpha_{eee1} \cdot Z0_{eee1} - \alpha_{eeo1} \cdot Z0_{eeo1}), R2 = \frac{1}{2} (\alpha_{eee2} \cdot Z0_{eee2} + \alpha_{eoe2} \cdot Z0_{eoe2})$$

$$R21 = \frac{1}{2} (\alpha_{eeo2} \cdot Z0_{eeo2} - \alpha_{eoe2} \cdot Z0_{eoe2}), R23 = \frac{1}{2} (\alpha_{eee2} \cdot Z0_{eee2} - \alpha_{eeo2} \cdot Z0_{eeo2})$$

$$R3 = \frac{1}{2} (\alpha_{eee3} \cdot Z0_{eee3} + \alpha_{eeo3} \cdot Z0_{eeo3}), R31 = \frac{1}{2} (\alpha_{eoe3} \cdot Z0_{eoe3} - \alpha_{eeo3} \cdot Z0_{eeo3})$$

$$R32 = \frac{1}{2} (\alpha_{eee3} \cdot Z0_{eee3} - \alpha_{eoe3} \cdot Z0_{eoe3})$$

$$G1 = \frac{\alpha_{eee1}}{Z0_{eee1}}, G2 = \frac{\alpha_{eee2}}{Z0_{eee2}}, G3 = \frac{\alpha_{eee3}}{Z0_{eee3}}$$

$$G12 = \frac{1}{2} (\frac{\alpha_{eoe1}}{Z0_{eee1}} - \frac{\alpha_{eee1}}{Z0_{eee1}}), G13 = \frac{1}{2} (\frac{\alpha_{eeo2}}{Z0_{eeo2}} - \frac{\alpha_{eee2}}{Z0_{eee2}})$$

$$G21 = \frac{1}{2} (\frac{\alpha_{eoe3}}{Z0_{eoe3}} - \frac{\alpha_{eoe3}}{Z0_{eoe3}}), G32 = \frac{1}{2} (\frac{\alpha_{eoe3}}{Z0_{eeo3}} - \frac{\alpha_{eee3}}{Z0_{eee3}})$$

$$G31 = \frac{1}{2} (\frac{\alpha_{eoo3}}{Z0_{eoo3}} - \frac{\alpha_{eoo3}}{Z0_{eoo3}}), G32 = \frac{1}{2} (\frac{\alpha_{eoo3}}{Z0_{eoo3}} - \frac{\alpha_{eeo3}}{Z0_{eoo3}})$$

Equation (5.16) and (5.17) are the parameters of the non-physical RLGC model of the (3+1)-conductor transmission line. The (3+1)-conductor transmission line has the R, L, G and C matrices in the following forms, which can be simulated in Hspice:

$$R = \begin{bmatrix} R1 & R12 & R13 \\ R21 & R2 & R23 \\ R31 & R32 & R3 \end{bmatrix}, L = \begin{bmatrix} L1 & L12 & L13 \\ L21 & L2 & L23 \\ L31 & L32 & L3 \end{bmatrix}$$

$$G = \begin{bmatrix} (G1+G12+G13) & -G12 & -G13 \\ -G21 & (G2+G21+G23) & -G23 \\ -G31 & -G32 & (G3+G31+G32) \end{bmatrix},$$

$$C = \begin{bmatrix} (C1+C12+C13) & -C12 & -C13 \\ -C21 & (C2+C21+C23) & -C23 \\ -C31 & -C32 & (C3+C31+C32) \end{bmatrix}$$
(5.18)

All the inductances, capacitances, resistances and conductances of the non-physical RLGC model of (n+1)-conductor transmission line can be extracted using a similar procedure. The non-physical RLGC parameters of (n+1)-conductor transmission lines can be simulated using the following matrix form in Hspice:

$$R = \begin{bmatrix} R1 & R12 & \cdots & R1n \\ R21 & R2 & \cdots & R2n \\ \vdots & & & \\ Rn1 & Rn2 & \cdots & Rn \end{bmatrix}, \quad L = \begin{bmatrix} L1 & L12 & \cdots & L1n \\ L21 & L2 & \cdots & L2n \\ \vdots & & \\ Ln1 & Ln2 & \cdots & Ln \end{bmatrix}$$

$$G = \begin{bmatrix} \sum_{k=1}^{n} G1k & -G12 & \cdots & -G1n \\ -G21 & \sum_{k=1}^{n} G2k & \cdots & -G2n \\ \vdots & & & \\ -Gn1 & -Gn2 & \cdots & \sum_{k=1}^{n} Gnk \end{bmatrix}, \quad C = \begin{bmatrix} \sum_{k=1}^{n} C1k & -C12 & \cdots & -C1n \\ -C21 & \sum_{k=1}^{n} C2k & \cdots & -C2n \\ \vdots & & & \\ -Cn1 & -Cn2 & \cdots & \sum_{k=1}^{n} Cnk \end{bmatrix}$$
(5.19)

# 5.3.5. Non-physical RLGC models for (n+1)-conductor silicon transmission line with slow-wave mode

Similar to the co-planar lines on silicon substrate in Chapter 4, the loss effect due to the silicon substrate can be included in the non-physical RLGC models for (n+1)-conductor transmission lines. For example, the non-physical RLGC model of (3+1)-conductor silicon lines with a slow-wave mode is shown in Figure 5.24. In the figure, G<sub>d</sub> represents the loss due to the slow-wave propagation effect, as explained in Chapter 4.

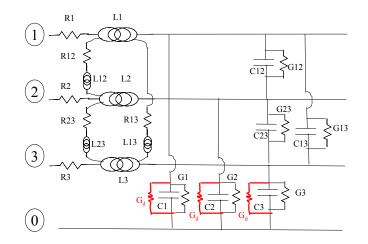


Figure 5.24Non-physical RLGC model for (3+1)-conductor silicon lines on high-loss<br/>silicon substrates.  $G_d$  represents the substrate loss.

As mentioned before,  $G_d$  can be frequency-dependent and complex, but real-valued  $G_d$  shows good correlation with measurements, similar to the low-resistivity silicon substrate in Chapter 4. Then, assuming a real-valued  $G_d$ , non-physical RLGC models for (3+1)-conductor silicon lines with slow-wave mode can be expressed as shown in Equation (5.20). The parameters can be simulated with the RLGC matrices in Equation (5.18) using Hspice W-element Tabular models.

$$\begin{split} L1 &= \frac{1}{2} \left( \frac{Z_{0eeo1}}{Vp_{eeo1}} + \frac{Z_{0eoe1}}{Vp_{eoo1}} \right), \ L2 &= \frac{1}{2} \left( \frac{Z_{0eeo2}}{Vp_{eeo2}} + \frac{Z_{0eoe2}}{Vp_{eoo2}} \right), \ L3 &= \frac{1}{2} \left( \frac{Z_{0eeo3}}{Vp_{eeo3}} + \frac{Z_{0eoo3}}{Vp_{eoo3}} \right) \\ L12 &= \frac{1}{2} \left( \frac{Z_{0eeo1}}{Vp_{eeo1}} - \frac{Z_{0eoo1}}{Vp_{eoo1}} \right), \ L21 &= \frac{1}{2} \left( \frac{Z_{0eeo2}}{Vp_{eoo2}} - \frac{Z_{0eoo2}}{Vp_{eoo2}} \right), \ L31 &= \frac{1}{2} \left( \frac{Z_{0eeo3}}{Vp_{eoo3}} - \frac{Z_{0eoo3}}{Vp_{eoo3}} \right) \\ L13 &= \frac{1}{2} \left( \frac{Z_{0eeo1}}{Vp_{eeo1}} - \frac{Z_{0eoo1}}{Vp_{eoo1}} \right), \ L23 &= \frac{1}{2} \left( \frac{Z_{0eeo2}}{Vp_{eoo2}} - \frac{Z_{0eoo2}}{Vp_{eoo2}} \right), \ L32 &= \frac{1}{2} \left( \frac{Z_{0eeo3}}{Vp_{eoo3}} - \frac{Z_{0eoo3}}{Vp_{eoo3}} \right) \\ C1 &= \frac{1}{2} \left( \frac{Z_{0eeo1}}{Vp_{eeo1}} - \frac{Z_{0eoo1}}{Vp_{eoo1}} \right), \ L23 &= \frac{1}{2} \left( \frac{Z_{0eeo2}}{Vp_{eoo2}} - \frac{Z_{0eoo2}}{Vp_{eoo2}} \right), \ L32 &= \frac{1}{2} \left( \frac{Z_{0eoo3}}{Vp_{eoo3}} - \frac{Z_{0eoo3}}{Vp_{eoo3}} \right) \\ C1 &= \frac{1}{Z0_{eeo1}} \cdot Vp_{eeo1}}, \ C2 &= \frac{1}{Z0_{eeo2}} \cdot Vp_{eeo2}}, \ C3 &= \frac{1}{Z0_{eeo3}} \cdot Vp_{eeo3}} \\ C12 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo1} \cdot Vp_{eoo1}} - \frac{1}{Z0_{eeo1} \cdot Vp_{eeo1}} \right), \ C21 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo2}} \cdot Vp_{eoo2}} - \frac{1}{Z0_{eoo2} \cdot Vp_{eoo2}} \right) \\ C13 &= \frac{1}{2} \left( \frac{1}{Z0_{eeo1} \cdot Vp_{eoo1}} - \frac{1}{Z0_{eeo1} \cdot Vp_{eeo1}} \right), \ C32 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo2}} \cdot Vp_{eoo2}} - \frac{1}{Z0_{eeo2} \cdot Vp_{eoo2}} \right) \\ C31 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} \right), \ C32 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eeo3} \cdot Vp_{eoo3}} \right) \\ C31 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} \right), \ C32 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} \right) \\ C31 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} \right), \ C32 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} \right) \\ C31 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} \right), \ C32 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} \right) \\ C31 &= \frac{1}{2} \left( \frac{1}{Z0_{eoo3} \cdot Vp_{eoo3}} - \frac{1}{Z0_{eoo3} \cdot Vp_{$$

$$R1 = \frac{1}{2} (\alpha_{eee1} \cdot Z0_{eee1} + \alpha_{eoe1} \cdot Z0_{eoe1}), R12 = \frac{1}{2} (\alpha_{eee1} \cdot Z0_{eee1} - \alpha_{eoe1} \cdot Z0_{eoe1})$$

$$R13 = \frac{1}{2} (\alpha_{eee1} \cdot Z0_{eee1} - \alpha_{eeo1} \cdot Z0_{eeo1}), R2 = \frac{1}{2} (\alpha_{eee2} \cdot Z0_{eee2} + \alpha_{eoe2} \cdot Z0_{eoe2})$$

$$R21 = \frac{1}{2} (\alpha_{eeo2} \cdot Z0_{eeo2} - \alpha_{eoe2} \cdot Z0_{eoe2}), R23 = \frac{1}{2} (\alpha_{eee2} \cdot Z0_{eee2} - \alpha_{eeo2} \cdot Z0_{eeo2})$$

$$R3 = \frac{1}{2} (\alpha_{eee3} \cdot Z0_{eee3} + \alpha_{eeo3} \cdot Z0_{eeo3}), R31 = \frac{1}{2} (\alpha_{eoe3} \cdot Z0_{eoe3} - \alpha_{eeo3} \cdot Z0_{eeo3})$$

$$R32 = \frac{1}{2} (\alpha_{eee3} \cdot Z0_{eee3} - \alpha_{eoe3} \cdot Z0_{eoe3})$$

$$G1 = \frac{\alpha_{eee1}}{Z0_{eee1}} + G_d, G2 = \frac{\alpha_{eee2}}{Z0_{eee2}} + G_d, G3 = \frac{\alpha_{eee3}}{Z0_{eee3}} + G_d$$

$$G12 = \frac{1}{2} (\frac{\alpha_{eoe1}}{Z0_{eoe1}} - \frac{\alpha_{eoe1}}{Z0_{eee1}}), G13 = \frac{1}{2} (\frac{\alpha_{eeo2}}{Z0_{eeo2}} - \frac{\alpha_{eee2}}{Z0_{eee2}})$$

$$G21 = \frac{1}{2} (\frac{\alpha_{eoo3}}{Z0_{eoo3}} - \frac{\alpha_{eoo3}}{Z0_{eoo3}}), G32 = \frac{1}{2} (\frac{\alpha_{eoo3}}{Z0_{eoo3}} - \frac{\alpha_{eoo3}}{Z0_{eoo3}})$$

#### 5.3.6. Simulation of (3+1)-conductor transmission lines

As an example, the following (3+1)-conductor transmission line in Figure 5.25 was simulated for demonstrating the stability of Equations (5.16) and (5.17). First, the inductance and capacitance were extracted using the 2D-parameter extractor in Hspice. Based on Maxwell's equations, the inductance and capacitance from the 2D-parameter extractor must be the same as those of the non-physical RLGC models.

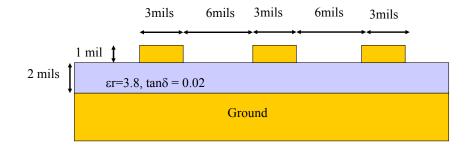


Figure 5.25 Cross-section of the simulated (3+1)-conductor transmission line.

The 2D-parameter extractor in Hspice yielded the following inductance and capacitance matrices for the (3+1)-conductor transmission line in Figure 5.25.

$$L = \begin{bmatrix} 2.98e - 7 \\ 2.60e - 8 & 2.97e - 7 \\ 6.82e - 9 & 2.60e - 8 & 2.98e - 7 \end{bmatrix} H/m$$

$$C = \begin{bmatrix} 9.86e - 11 \\ -2.73e - 12 & 9.87e - 11 \\ -4.44e - 13 & -2.73e - 12 & 9.86e - 11 \end{bmatrix} F/m$$
(5.21)

Then, the inductance and capacitance in Equation (5.21) were applied to Figure 5.22 to obtain the characteristic impedance and phase velocity of the (3+1)-conductor transmission line. In this example, the attenuation constant of the (3+1)-conductor transmission line was simulated using  $\alpha = 13/10e9$ \*f NP/m for all the attenuation constants in Equation (5.17), where f is the frequency. Then, the non-physical RLGC

model of the (3+1)-conductor transmission line in Figure 5.25 can be obtained using Equation (5.16) and (5.17) as follows:

L1 = 2.98e-7 H/m, L2 = 2.97e-7 H/m, L3 = 2.98e-7 H/m  
L12=L21=2.60e-8 H/m, L13=L31 = 6.82e-9 H/m  
L23=L32=2.60e-8 H/m (5.22)  
C1 = 95.43 pF/m, C2 = 93.24 pF/m, C3 = 95.43 pF/m  
C12=C21 = 2.73 pF/m, C13=C31=4.44 pF/m,  
C23=C32=2.73 pF/m  
R1 = 54.6 
$$\cdot$$
 (13/10e9\*f)  $\Omega$ /m, R2=54.8  $\cdot$  (13/10e9\*f)  $\Omega$ /m, R3=54.6  $\cdot$  (13/10e9\*f)  $\Omega$ /m  
R12=R21=3.3  $\cdot$  (13/10e9\*f)  $\Omega$ /m, R13=R31=0.75  $\cdot$  (13/10e9\*f)  $\Omega$ /m  
R23=R32=1.16  $\cdot$  (13/10e9\*f)  $\Omega$ /m  
G1 = 0.017  $\cdot$  (13/10e9\*f)  $\Omega$ /m, G2 = 0.016  $\cdot$  (13/10e9\*f)  $S$ /m  
G3=0.017  $\cdot$  (13/10e9\*f)  $S$ /m, G12=G21=1.1e-3  $\cdot$  (13/10e9\*f)  $S$ /m  
G13=G31=0.22e-3  $\cdot$  (13/10e9\*f) S/m, G23=G32=0.32e-3  $\cdot$  (13/10e9\*f) S/m

The (3+1)-conductor transmission line was simulated with a step source with 30ps risetime and 0.25V amplitude using the circuit in Figure 5.26.

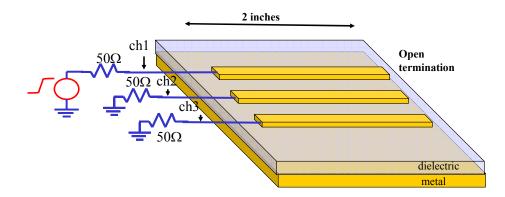


Figure 5.26 Simulated circuit for the (3+1)-conductor transmission line.

The (3+1)-conductor transmission line had open terminations, and the length was 2 inches. The simulation results are shown in Figure 5.27. The reflected signal by the (3+1)-conductor transmission line was simulated in Ch1, and the cross-talk signals were simulated in Ch2 and Ch3.

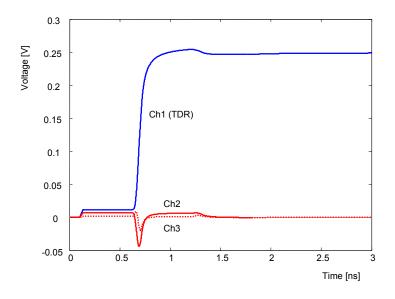


Figure 5.27 Simulated waveforms for the (3+1)-conductor transmission line in Figure 5.25.

### 5.3.7. Simulation of (64+1)-conductor transmission lines

(64+1)-conductor transmission lines are used for 64-bit parallel data or register buses in computer systems. In this section, (64+1)-conductor transmission lines are simulated after deriving non-physical RLGC models for (64+1)-conductor transmission lines based on the non-physical RLGC models extraction procedure. Since the non-physical RLGC models for (64+1)-conductor transmission lines are too complex and long, the equations are not shown. Instead, the algorithm to generate the non-physical RLGC models for (64+1)-conductor transmission lines is available in an Appendix.

The cross-section of the simulated (64+1)-conductor transmission line is shown in Figure 5.28. The inductance and capacitance of the transmission line in Equation (5.26)

were computed using the Hspice 2D parameter extractor. Mutual capacitance and inductance were considered up to two adjacent conductors, neglecting the other mutual capacitance and inductance. The loss was assumed to be similar to that of the APPE board in Chapter 3.

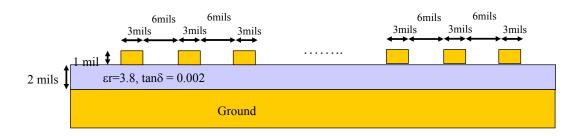


Figure 5.28 Cross-section of simulated (64+1)-conductor transmission lines.

$$L1 \approx 298 \ nH/m$$

$$L12 = 26 \ nH/m$$

$$L13 = 6.82 \ nH/m$$

$$C1 \approx 95.9 \ pF/m$$

$$C12 = 2.73 \ pF/m$$

$$C13 = 0.444 \ pF/m$$

$$\alpha = \frac{3}{\sqrt{10e^9}} \sqrt{f} \ Np/m \text{ for all modes}$$
(5.23)

In this simulation, the non-physical RLGC parameters were assumed to be the following:

$$L1 = L3 = \dots = L_n$$

$$L12 = L21 = L23 = L32 = \dots L_{n(n-1)} = L_{(n-1)n}$$

$$R1 = R3 = \dots = R_n$$

$$R12 = R21 = R23 = R32 = \dots R_{n(n-1)} = R_{(n-1)n}$$

$$C1 = C3 = \dots = C_n$$

$$C12 = C21 = C23 = C32 = \dots C_{n(n-1)} = C_{(n-1)n}$$

$$G1 = G3 = \dots = G_n$$

$$G12 = G21 = G23 = G32 = \dots G_{n(n-1)} = G_{(n-1)n}$$

The inductance and capacitance were used to compute the mode characteristic impedance of the transmission line, and the non-physical RLGC model for the (64+1)-conductor transmission line in Figure 5.28 was extracted with the attenuation constant in Equation (5.23). The RLGC matrices in Equation (5.19) consisting of the parameters in Equation (5.23) and (5.24) were extracted and simulated using W-element tabular models in Hspice.

The circuit simulated using the (64+1)-conductor transmission line and 3pF load capacitors is shown in Figure 5.29. In the figure, all the near ends of the transmission line, which were from ch1 to ch64, were terminated using 50 ohms, and all the far ends from ch65 to ch128 were terminated using 3pF capacitors. A 5GHz clock signal with a risetime of 20ps and amplitude of 1V was the source located at ch30 to excite the (64+1)-conductor transmission line with a length of 2 inches. The simulation results are shown in Figure 5.30. Figure 5.30(a) shows the near-end waveform for the 5GHz input signal, and Figure 5.30(b) shows the far-end waveform. Near-end cross-talk waveform was simulated in Ch31 and Ch32, and far-end cross-talk waveform was simulated in Ch95 and Ch96. These simulations show the stability of non-physical RLGC models, which is a major issue in the modeling of lossy multi-conductor transmission lines [E2].

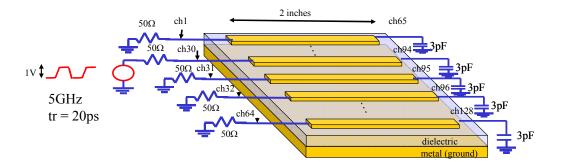
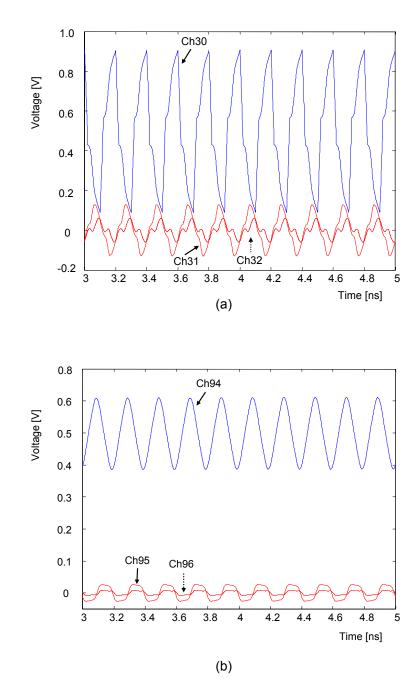


Figure 5.29 (64+1)-conductor transmission line with 3pF load capacitors.



**Figure 5.30** Simulation results of the (64+1)-conductor transmission line with 3pF load capacitors in Figure 5.29. (a) Near end and (b) far end.

# 5.3.8. Characterization of (n+1)-conductor transmission lines using two-channel TDR measurements

Since (n+1)-conductor transmission lines require n-channel TDR probes for extracting non-physical RLGC models, it is almost impossible to measure (n+1)-conductor transmission lines for  $n \ge 3$ . Since microprobes and TDR heads for two-channel TDR measurements are commercially available, a technique to characterize (n+1)-conductor transmission lines using two-channel TDR measurements has been discussed in this section. The technique has been developed under the assumption that mutual inductance and capacitance except adjacent conductors are negligible. This assumption is a good approximation for planar (n+1)-conductor transmission lines such as in Figure 5.28 since adjacent conductors block the electric fields from the remaining conductors. Since most digital systems use planar (n+1)-conductor transmission lines for 16- or 32-bit data or address buses, this approximation can be applied for high-speed interconnect design and simulation. Then, the RLGC matrices of (n+1)-conductor transmission lines in Equation (5.19) can be reduced to Equation (5.25).

$$R = \begin{bmatrix} R1 & R12 & 0 & \cdots & 0 \\ R21 & R2 & R23 & \cdots & 0 \\ 0 & R32 & R3 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & Rn \end{bmatrix}, \quad L = \begin{bmatrix} L1 & L12 & 0 & \cdots & 0 \\ L21 & L2 & L23 & \cdots & 0 \\ 0 & L32 & L3 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & Ln \end{bmatrix}$$

$$G = \begin{bmatrix} (G1+G12) & -G12 & \cdots & 0 \\ -G21 & (G2+G21+G23) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & Gn+Gn \cdot n-1 \end{bmatrix}$$

$$C = \begin{bmatrix} (C1+C12) & -C12 & \cdots & 0 \\ -C21 & (C2+C21+C23) & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & Cn+Cn \cdot n-1 \end{bmatrix}$$
(5.25)

For symmetric (n+1)-conductor transmission lines, the following assumptions are generally valid.

$$L2 = L3 = \dots = L_{(n-1)}$$

$$L12 = L21 = L23 = L32 = \dots = L_{n(n-1)} = L_{(n-1)n}$$

$$R2 = R3 = \dots = R_{(n-1)}$$

$$R12 = R21 = R23 = R32 = \dots = R_{n(n-1)} = R_{(n-1)n}$$

$$C2 = C3 = \dots = C_{(n-1)}$$

$$C12 = C21 = C23 = C32 = \dots = C_{n(n-1)} = C_{(n-1)n}$$

$$G2 = G3 = \dots = G_{(n-1)}$$

$$G12 = G21 = G23 = G32 = \dots = G_{n(n-1)} = G_{(n-1)n}$$

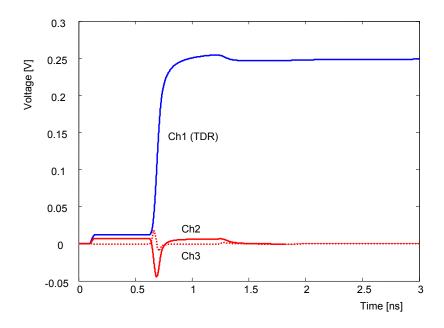
Although L1 can be slightly different from L2 for (n+1)-conductor transmission lines due to the fringing field, setting L1≈L2≈Ln is a good approximation if L12  $\leq$  L1/10. For the same reason, C1  $\approx$  C2  $\approx$  Cn, R1  $\approx$  R2  $\approx$  Rn and G1  $\approx$  G2  $\approx$  Gn. Then, L1, L12, R1, R12, C1, C12, G1, and G12 can approximately be characterized from conductors 1 and 2 with the other conductors floating, using the method for symmetric coupled lines.

The (3+1)-conductor transmission line in Figure 5.25 was simulated for comparison. The parameters in Equation (5.27) were simulated and compared to Equation (5.21). The simulation results using Equation (5.27) are shown in Figure 5.31. The simulation results in Figure 5.31 are very similar to the waveforms in Figure 5.27 implying that Equation (5.27) is a good approximation for Equation (5.21).

$$L = \begin{bmatrix} 2.97e - 7 \\ 2.60e - 8 & 2.97e - 7 \\ 0 & 2.60e - 8 & 2.97e - 8 \end{bmatrix} H/m$$

$$C = \begin{bmatrix} 95.97e - 12 \\ -2.73e - 12 & 98.7e - 12 \\ 0 & -2.73e - 12 & 95.97e - 12 \end{bmatrix} F/m$$
(5.27)

 $\alpha$  = 13/ 10e9 · f Np/m for all  $\alpha$ 



**Figure 5.31** Simulated waveforms of the (3+1)-conductor transmission line by neglecting mutual inductance and capacitance except for adjacent conductors.

#### 5.3.9. Signal integrity chart

Based on the investigation on transmission lines in this chapter, the following chart in Figure 5.32 has been obtained. The chart shows the controllability of the impedance of the corresponding structures. 'Controllable' means that electromagnetic fields are confined inside the structures and therefore the impedance of the structures can be changed by changing the dimension of the structures. On the contrary, 'uncontrollable' means that electromagnetic fields are not confined inside the structures and therefore the impedance of the structures cannot be controlled by changing the dimension of the structures. The structures with controllable impedance have better signal integrity since all the electromagnetic signals are controllable. In order to design high-speed digital systems with good signal integrity, uncontrollable structures must be avoided.

mode	Even-mode	Odd-mode (differential-mode)
Multi-conductor TL with a ground plane	controllable	controllable
Multi-conductor TL with a floating plane	uncontrollable	controllable
Multi-conductor TL without a floating plane	uncontrollable	a little controllable
Vias With ground vias	controllable	controllable
Vias Without ground vias	uncontrollable	controllable

Figure 5.32 Impedance controllability (signal integrity) chart.

The best structure for signal integrity is multi-conductor transmission lines with a ground plane, according to Figure 5.32. A ground plane is a metal plane below signal lines to which the ground of signal sources is connected. Therefore, high-speed interconnections such as processor-memory interconnect should be designed using multi-conductor transmission lines with a ground plane. If high-speed interconnections do not use even-mode propagation or if high-speed interconnections are differential lines, multi-conductor transmission lines with a floating plane show the same performance as multi-conductor transmission lines with a ground plane. A floating plane is a metal plane below signal lines to which the ground of signal sources is not connected. The differential lines with a floating plane have a little worse signal integrity than the differential lines with a floating plane since outside electromagnetic fields can induce noise. Vias can be also considered as vertical multi-conductor transmission lines. Therefore, the same explanation can also be applied to vias. To improve signal integrity, ground vias must be placed close to signal vias to form vertical transmission lines [E3][E4].

# 5.4. Summary

In this chapter, the TDR characterization technique for transmission lines described in Chapter 3 has been extended to multi-conductor transmission lines. Coupled lines were fabricated and characterized using TDR measurements yielding the even- and oddmode characteristic impedance and propagation constant for coupled lines. Nonphysical RLGC models for coupled lines were then developed and used for simulation with the extracted data from TDR measurements. The simulation showed good agreement with time-domain measurements, showing the accuracy of the extracted data and non-physical RLGC model. Differential lines were also fabricated and characterized using TDR measurements. Differential lines are coupled lines where only the odd-mode excitation is used. Non-physical RLGC models for coupled lines on silicon substrate, asymmetric coupled lines, (3+1)-conductor transmission lines and (64+1)-conductor transmission lines were derived and simulated showing good stability. Finally, the method for characterizing (n+1)-conductor transmission lines using two channel TDR measurements were discussed for planar multi-conductor transmission lines.

# **Chapter 6**

# Wafer-Level Packaging on Integrated Substrate

This chapter discusses the effect of the assembled wafer-level package and interconnect transition on gigabit data transmission. The test vehicle in Chapter 1 consisting of a coplanar silicon transmission line, two transmission lines on board and assembled wafer level package was used for evaluation. In Chapter 3, for board transmission lines, six board materials consisting of Ciba thin film, Vialux (Dupont), FR4, Hitachi MCL-LX67, Nelco N4000-12, and APPE were compared to investigate the effect of board material on signal propagation. APPE had the lowest transmission loss amongst them. In Chapter 4, silicon substrates with 100  $\Omega$ -cm and 2000  $\Omega$ -cm resistivity were compared for investigating the effect of silicon substrate on signal propagation. Silicon substrate with 100  $\Omega$ -cm resistivity had higher loss due to the slow-wave propagation effect. For assembling the wafer-level package, solder bumps with 50um diameter and 100um pitch were used, and the effect of parasitic capacitance from the solder bumps on signal propagation is investigated in this chapter. This chapter concludes that better signal integrity cannot be achieved only by using lower loss material, but also requires low parasitic capacitance for signal transmission from the chip to the board. The minimum parasitic capacitance required for data transmission has been guantified in this chapter which can lead to the optimization of the wafer level package assembly process.

190

# 6.1. Wafer-level package test vehicle

The test vehicle used in this dissertation consists of two Printed Wiring Board (PWB) transmission lines, a silicon transmission line, and solder bumps with 50um diameter and 100um pitch, as shown in Figure 6.1. The goal is to transmit a 5Gbps signal, consistent with the ITRS roadmap in 2005 for microprocessors, through the interconnection structure and receive it at the far end with minimum degradation. As discussed in Chapter 1, the PWB transmission lines used were coplanar lines with a center conductor of width 2.5 mils and conductor gap of 2.5 mils. The length of each PWB line was 2.5 cm. Various PWB materials were evaluated as the dielectric for the PWB coplanar lines, as discussed in Chapter 3.

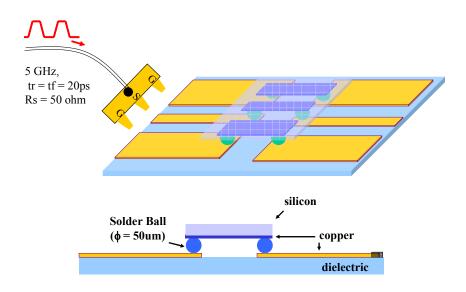


Figure 6.1 Test vehicle for wafer-level package on integrated board.

The silicon transmission lines used were also coplanar lines with a center conductor of width 1 mil, gap of 1 mil and length of 1mm. The silicon substrates with resistivity of 100  $\Omega$ -cm and 2000  $\Omega$ -cm were evaluated and compared for signal transmission in Chapter 4. The vertical dimension of the transmission line on the 2000  $\Omega$ -cm resistivity silicon

substrate had 0.2um thickness Au, 3um thickness Cu, 0.2um thickness Ti, and 1um thickness SiO2 on the silicon substrate with 500um thickness. The coplanar silicon line was patterned using the Au-Cu-Ti layers. The silicon and PWB transmission lines were connected through solder bumps with 50um diameter and 100um pitch.

# 6.2. Modeling of Solder Bumps

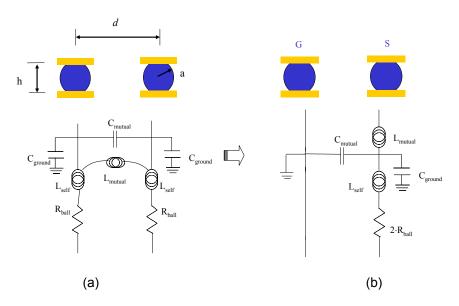
In this section, the solder bumps of the wafer-level package test vehicle in Figure 6.1 have been analytically modeled. Analytical models have been compared to HFSS (High Frequency Structure Simulator) and measurement results.

#### 6.2.1 Analytical models

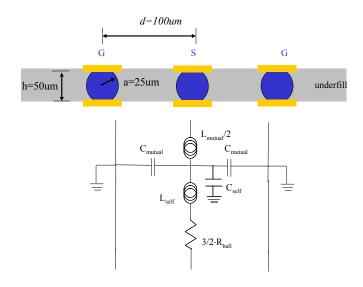
Solder bumps can be modeled as shown in Figure 6.2. The model in Figure 6.2(a) is a general equivalent circuit for two parallel solder bumps, and the model in Figure 6.2(b) is a solder bump model with ground and signal assignments. In the figure,  $L_{self}$  is the self inductance of the solder bumps, and  $C_{ground}$  is the capacitance between the solder bumps and ground.  $L_{mutual}$  and  $C_{mutual}$  are the mutual inductance and capacitance, respectively. In Figure 6.2,  $R_{ball}$  is the static resistance of each solder bump. Mutual inductance and capacitance are related to transverse electromagnetic (TEM) fields between the two solder bumps,  $L_{self}$  and  $C_{ground}$  are related to electromagnetic fields existing between each solder bump and ground. The self-capacitance of the solder bumps is  $C_{self} = C_{ground} + C_{mutual}$ . In [F1], filp-chip solder bumps with 125um diameter, 250um pitch and 75um height from Unitive Inc. have been characterized using a Network Analyzer. The solder bumps had a self-inductance of 98pH, mutual-capacitance of 7fF, self-capacitance of 2pF and inductance coupling coefficient of 0.001. Similar to the parallel solder bumps in Figure 6.2, the solder bumps of the test vehicle in Figure 6.1

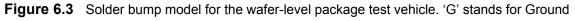
192

can be modeled as shown in Figure 6.3. The underfill in Figure 6.3 had the same property as Figure 4.21.



**Figure 6.2** Solder bump models for (a) two parallel solder bumps and (b) ground-signal solder bumps. 'G' stands for Ground and 'S' stands for Signal.





and 'S' stands for Signal.

#### 6.2.1.1 Extraction of self inductance and capacitance

The self inductance of the solder bumps in Figure 6.3 can be extracted using Bogatin's simplified formula [F2], as shown below:

$$L_{self} = 196.8 \cdot \ln(\frac{d}{a}) \cdot h \quad nH \tag{6.1}$$

where *d* is the pitch of the two solder bumps, *a* is the radius of each solder bump and *h* is the height, as shown in Figure 6.3. Then, the self inductance  $L_{self}$  in Figure 6.3 becomes 13.6 pH.

The self capacitance of the solder bumps in Figure 6.3 depends on the geometry of the solder bumps and ground. There is no general relationship between the self-capacitance and the geometry of the solder bumps except for the parallel plate capacitance relationship. In this chpater, the self-capacitance was extracted based on a previously published result on solder bumps, as discussed in [F1]. In [F1], the flip-chip solder bumps with 125um diameter and 250um pitch from Unitive Inc. had a self-capacitance of 2pF. Since the self-capacitance is proportional to area, the self-capacitance of the solder bumps with 50um diameter and 100um pitch is expected to be  $\sim 0.32$ pF.

#### 6.2.1.2 Mutual inductance and capacitance

The mutual inductance and capacitance of the solder bumps in Figure 6.3 can be modeled as a transmission line since the current flow through the solder balls is similar to a transmission line. For simplicity, the solder balls were assumed to be circular cylinders, as shown in Figure 6.4. Then, the per-unit-length capacitance between two adjacent cylinders can be calculated as [F3]:

$$C_{mutual} = \frac{\pi \varepsilon_r \cdot \varepsilon_0}{\cosh^{-1}(\frac{d}{2a})} [F/m]$$
(6.2)

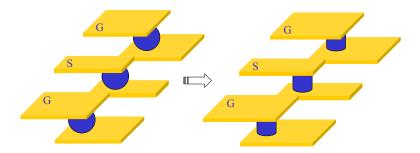


Figure 6.4 Simplification of solder bumps to cylinders.

where *a* is the radius of the cylinder, *d* is the center-to-center distance between two adjacent cylinders,  $\varepsilon_r$  is the effective permittivity of the material surrounding the cylinders, and  $\varepsilon_0$  is the permittivity of air. The total mutual capacitance of the solder bumps is  $2 \cdot C_{mutual}$ .

The per-unit-length mutual inductance can be calculated from the velocity as:

$$L_{mutual} = \frac{\varepsilon_r}{2C_{mutual} \cdot c_0^2} \left[ H / m \right]$$
(6.3)

where  $c_0$  is the speed of light in free-space and  $\varepsilon_r$  is the relative dielectric constant. Then, the mutual inductance of the solder bumps is  $L_{mutual}$ , where *h* is the length of the cylinders. Using the underfill material with  $\varepsilon_r = 3.1$ , the per-unit-length mutual capacitance in Equation (6.2) is 65.477 pF/m. Then, the per-unit-length mutual inductance in Equation (6.3) is 263 nH/m. Therefore, the mutual inductance of the solder bumps in Figure 6.3 is 13.15pH (= 263 nH/m \* 50 um). The mutual capacitance of the solder bumps in Figure 6.3 is 6.55 fF (= 65.477 pF/m \*2 \* 50um). The static resistance of the solder bump is ~ 7.5 m $\Omega$ , assuming solder bumps have 10% conductivity of copper. The inductance in Equation (6.3) does not depend on the material surrounding the solder balls, but depends on the distance between adjacent solder balls. Placing the ground path closer to the signal path reduces the mutual inductance of the interconnection.

#### 6.2.1.3 Analytical solder bump model for the wafer-level package test vehicle

Hence, after modifying the model in Figure 6.3, the solder bumps can be represented using an equivalent circuit as:

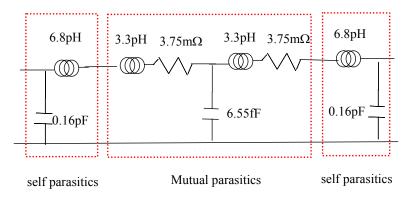


Figure 6.5 Analytical model for the solder bumps with 50um diameter and 100um pitch in the wafer-level package test vehicle.

### 6.2.2 VNA Measurement

As shown in Figure 6.6, 100um diameter solder bumps were fabricated and characterized using a Vector Network Analyzer to extract the parasitics. A package transmission line fabricated using Nelco N4000-13 material was used for measurement of the solder bumps and de-embedded for extracting the response of the solder bumps. The de-embedding was based on two line measurements, as discussed in [F4][F5]. The other end of the solder bumps was shorted using an on-chip conductor, as shown in Figure 6.6. The co-planar package transmission line had a center conductor width of 5 mils and a gap between metal lines of 4 mils. The solder bumps had a diameter of 100um and pitch of 200um.

In Figure 6.7, the imaginary part of the input impedance for the solder bumps is shown along with the frequency response of a 47.7 pH inductor. According to Equation (6.1), the 100um diameter solder bumps have a self inductance of 27.28 pH. The mutual

inductance is 26.3 pH based on Equations (6.2) and (6.3). Then, the calculated total inductance is 40.43 pH. The extracted inductance in Figure 6.7 from VNA measurements is close to the calculated total inductance, which validates Equations (6.1), (6.2) and (6.3).

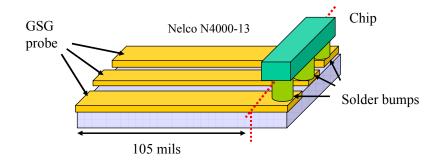
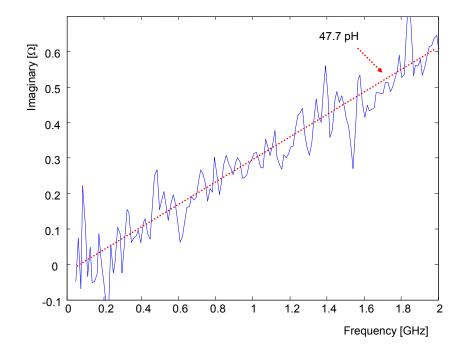


Figure 6.6 Measurement test vehicle for the characterization of solder bumps with 100um diameter and 200um pitch.



**Figure 6.7** Imaginary part of the measured input impedance of the solder bumps with 100um diameter and 200um pitch.

#### 6.2.3 Modeling using HFSS

3D simulations using HFSS (High Frequency Structure Simulator) [F6] were also used to verify the accuracy of the inductance and capacitance values extracted in Figure 6.5. The solder bumps with 50um diameter and 100um pitch were simulated with different heights. With the far end of the solder bumps shorted as in Figure 6.6, the input impedance was calculated using HFSS. Then, the inductance was extracted from the imaginary part of the input impedance, as shown in Figure 6.8.

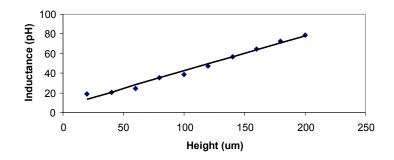


Figure 6.8 Solder bump inductance extracted from HFSS.

The inductance in Figure 6.8 can be approximated as:

$$L = 6.6253 + 0.3558 * h[um] [pH]$$
(6.4)

where h is the height of the solder bumps in um. Since the constant value 6.6253 pH does not change with the height of the solder bumps, it is the inductance of the shorting metal used to connect the solder bumps together. Then, for 50 um height bumps in the test vehicle, the estimated inductance of solder bumps from HFSS was 17.79 pH, based on Equation (6.4). This value is smaller than the inductance predicted by the analytical model, which was 20.2 pH. This would be because HFSS calculates the external inductance, while the analytical model includes the internal inductance as well.

# 6.3 Simulation of Test vehicle

In this section, the wafer-level package test vehicle in Figure 6.1 was simulated using board and silicon transmission lines characterized in Chapter 3 and Chapter 4, respectively. Two configurations were simulated for comparison, namely the best and worst configurations. In terms of transmission loss, the best configuration consisted of the APPE and 2000  $\Omega$ -cm resistivity silicon transmission lines, and the worst configuration consisted of the FR4 and 100  $\Omega$ -cm resistivity silicon transmission lines. The solder bump model in Figure 6.5 was used for the simulation. The goal of this simulation was to differentiate the two structures in terms of signal integrity.

#### 6.3.1 100 $\Omega$ -cm resistivity silicon substrate, FR4 and solder bumps

For the worst configuration, the FR4 transmission line and 100  $\Omega$ -cm resistivity silicon transmission line were selected from Chapter 3 and Chapter 4 for the simulation of the test vehicle, as shown in Figure 6.9. The simulated FR4 transmission line had the following non-physical RLGC parameters:

R = 
$$88 \cdot (7/10e9 \cdot f)$$
 ohm/m  
L = 425 nH /m (6.5)  
G =  $(7/10e9 \cdot f)/88$  S/m  
C = 54.9 pF/m

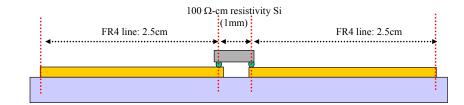
The coplanar line on silicon substrate with a resistivity of 100  $\Omega$ -cm had the following non-physical RLGC parameters:

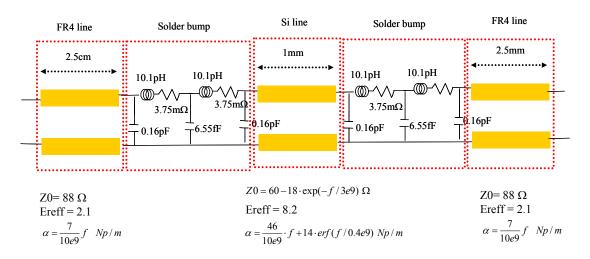
$$R = [60 - 18 \cdot \exp(-f/3e9)] \cdot [46/10e^9 \cdot f + 14 \cdot erf(f/0.4e^9)] \text{ ohm/m}$$

$$L = [60 - 18 \cdot \exp(-f/3e9)]/3e8^* \operatorname{sqrt}(8.2) \qquad H /m$$

$$G = [46/10e^9 \cdot f + 14 \cdot erf(f/0.4e^9)]/[60 - 18 \cdot \exp(-f/3e^9)] + 20 \quad S/m$$

$$C = \operatorname{sqrt}(8.2) / \{3e8^* [60 - 18 \cdot \exp(-f/3e^9)]\} \quad F/m$$
(6.6)



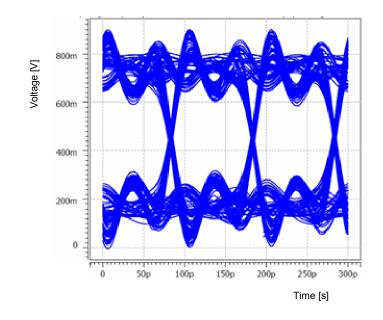


**Figure 6.9** Equivalent model for FR4 and  $100\Omega$ -cm resistivity silicon test vehicle.

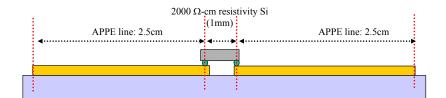
Then, the worst configuration in Figure 6.9 was simulated, yielding the eye-diagram shown in Figure 6.10 for 5GHz digital signals with 20ps risetime and 2V amplitude. The output impedance of the 5GHz digital signals was assumed to be 50 ohms. The far end of the test vehicle was terminated with the characteristic impedance of the board transmission line. The eye-diagram in Figure 6.10 was simulated at the far end using Hspice.

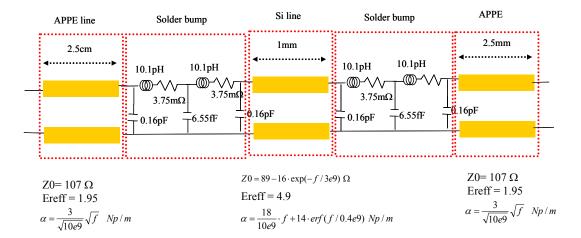
#### 6.3.2 2000 $\Omega$ -cm resistivity silicon substrate, APPE and solder bumps

For the best configuration, the APPE transmission line and 2000  $\Omega$ -cm resistivity silicon transmission were selected from Chapter 3 and Chapter 4, respectively, as shown in Figure 6.11. For the solder bumps, the solder bump model in Figure 6.5 was used.



**Figure 6.10** Simulated eye-diagram for FR4 and  $100\Omega$ -cm resistivity silicon test vehicle.





**Figure 6.11** Equivalent model for the APPE and  $2000\Omega$ -cm resistivity silicon test vehicle.

The simulated APPE transmission line had the following non-physical RLGC parameters:

R = 
$$107 \cdot [3/\sqrt{10e9} \cdot \sqrt{f}]$$
 ohm/m  
L = 498 nH/m  
G =  $[3/\sqrt{10e9} \cdot \sqrt{f}]/107$  S/m  
C = 43.5 pF/m

The coplanar line on silicon substrate with a resistivity of 2000  $\Omega$ -cm had the following non-physical RLGC parameters:

$$R = [89 - 16 \cdot \exp(-f/3e9)] \cdot [18/10e9 \cdot f + 14 \cdot erf(f/0.4e9)] \quad ohm/m$$

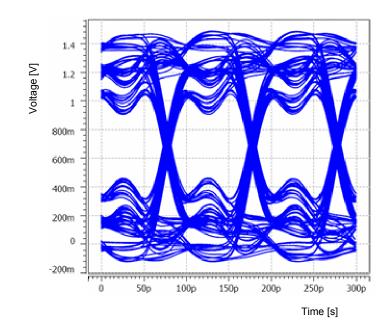
$$L = [89 - 16 \cdot \exp(-f/3e9)]/3e8^* \operatorname{sqrt}(4.9) \qquad H/m \qquad (6.8)$$

$$G = [18/10e9 \cdot f + 14 \cdot erf(f/0.4e9)]/[89 - 16 \cdot \exp(-f/3e9)] \quad S/m$$

$$C = \operatorname{sqrt}(4.9) / \{3e8^* [89 - 16 \cdot \exp(-f/3e9)]\} \quad F/m$$

Then, the best configuration in Figure 6.11 was simulated yielding the eye-diagram shown in Figure 6.12 for 5GHz digital signals with 20ps risetime and 2V amplitude. The output impedance of the 5GHz digital signals was 50 ohms. The far end of the test vehicle was terminated with the characteristic impedance of the board transmission line. The eye-diagram in Figure 6.12 was simulated at the far end using Hspice.

It was expected that the APPE-2000 $\Omega$ -cm configuration in Figure 6.9 would have much better eye-diagrams than the FR4-100 $\Omega$ -cm configuration in Figure 6.11 since the APPE- 2000  $\Omega$ -cm configuration had much lower loss. However, as shown in Figure 6.10 and 6.12, the APPE-2000  $\Omega$ -cm configuration does not show better eye-diagrams. It is mainly because of the capacitance of the solder bumps.



**Figure 6.12** Simulated eye-diagram for APPE and  $2000\Omega$ -cm resistivity silicon test vehicle.

## 6.3.3 Effect of solder bump capacitance

To evaluate the effect of the solder bump capacitance, smaller solder bumps with 35um diameter and 100um pitch were considered in this section. In Figure 6.13, the analytical model for solder bumps with 35um diameter and 100um pitch extracted using Equations (6.1), (6.2) and (6.3) is shown. The total capacitance of the solder bumps is about half the capacitance of the solder bumps with 50um diameter and 100um pitch, while the total inductance of the solder bumps is similar. Then, the equivalent circuit for the best configuration using solder bumps with 35um diameter and 100um pitch in Figure 6.14 was simulated for the same 5GHz digital signals, as shown in Figure 6.15. The simulated eye-diagram in Figure 6.15 has much better eye-opening than Figure 6.12.

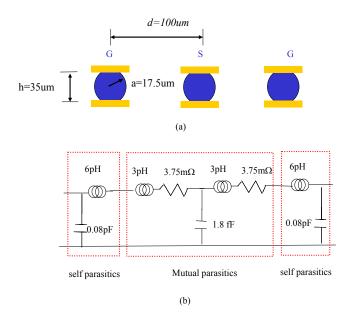
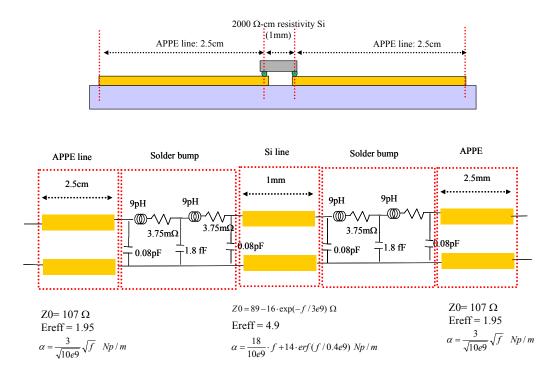
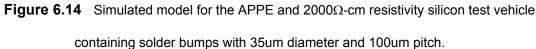
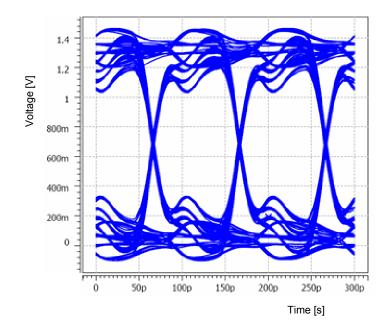


Figure 6.13 (a) Solder bumps with 35um diameter and 100um pitch and (b) their analytical

model.





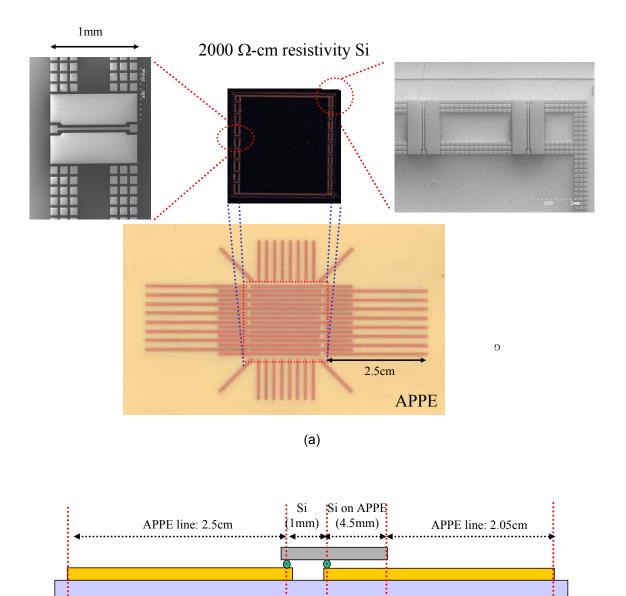


**Figure 6.15** Simulated eye-diagram of APPE and 2000Ω-cm silicon test vehicle containing solder bumps with 35um diameter and 100um pitch.

From the above simulations, it can be concluded that better signal integrity cannot be achieved only by using lower loss material, but also requires low parasitic capacitance for signal transmission from the chip to the board. The maximum parasitic capacitance required for 5GHz digital signal transmission is about 0.16pF in Figure 6.14, which can be achieved using solder bumps with 35um diameter and 100um pitch. However, the required capacitance can be increased with better characteristic impedance matching.

#### 6.4 Fabrication of Test vehicle

The wafer-level package test vehicle in Figure 6.1 was fabricated as shown in Figure 6.16 and tested in this section. The fabricated test vehicle is a little different from Figure 6.1 due to problems with assembly. In the assembled test vehicle, Si wafer covered by  $SiO_2$  was extended onto the APPE line, as shown in Figure 6.16.



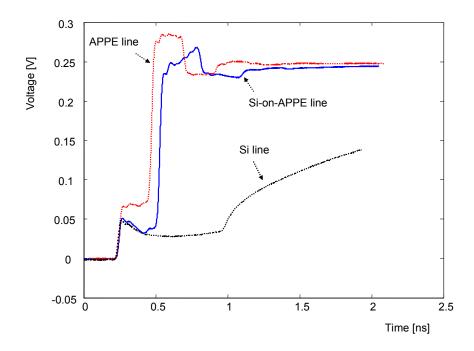
(b)

Figure 6.16 Assembled wafer level package test vehicle. (a) top view and (b) cross-section.

# 6.4.1. Extraction of equivalent circuits

The TDR measurements of the APPE line, Si-on-APPE line and Si line for the assembled test vehicle in Figure 6.16 are shown in Figure 6.17. The measured APPE coplanar line in Figure 6.17 had a center-conductor width of 2.5 mils, a gap between

metal of 2.5 mils, a APPE substrate thickness of 1mm, a length of 2.5cm. The Si coplanar line had a center-conductor width of 1 mil, a gap between metal of 1 mil, a silicon resistivity of 2000  $\Omega$ -cm covered by 1um thickness SiO<sub>2</sub>, and a length of 960 mils. The Si-on-APPE line is the APPE co-planar line covered by 2000 $\Omega$ -cm resistivity silicon wafer with 1um thickness SiO<sub>2</sub>. The dimension of the Si-on-APPE line was the same as that of the APPE line.



**Figure 6.17** TDR measurements of the APPE line, Si-on-APPE line and Si line for the assembled test vehicle in Figure 6.16.

Then, from the TDR measurements in Figure 6.17, the APPE coplanar line in the assembled test vehicle was extracted using non-physical RLGC models as:

Z0 = 92 
$$\Omega$$
  
Effective  $\varepsilon r$  = 1.8 (6.9)  
 $\alpha = 3/\sqrt{10e^9} \cdot \sqrt{f}$  NP/m

Similarly, the Si-on-APPE line in the assembled test vehicle was extracted as:

Z0 = 76-12·exp(-f/3e9) 
$$\Omega$$
  
Effective  $\varepsilon r$  = 2.8 (6.10)  
 $\alpha = 5 / \sqrt{10e^9} \cdot \sqrt{f}$  NP/m

and the Si line in the assembled test vehicle was extracted as:

Z0 = 76-12·exp(-f/3e9) 
$$\Omega$$
  
Effective  $\varepsilon r = 4.9$  (6.11)  
 $\alpha = \frac{18}{10e9} \cdot f + 14 \cdot erf(f/0.4e9)$  NP/m

The APPE and 2000  $\Omega$ -cm resistivity line parameters in Equation (6.9) and (6.11) were a little different from the parameters in Chapter 3 since the assembled lines were heated at 210° for ~10s during the assembly process. The assembled test vehicle can now be modeled as shown in Figure 6.18.

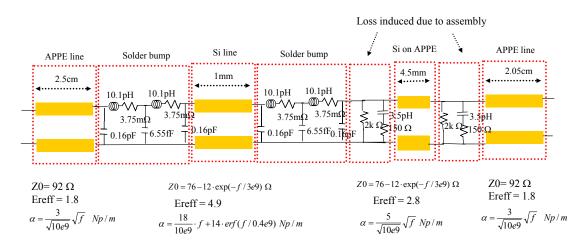
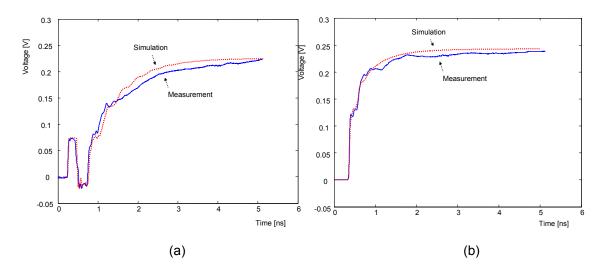


Figure 6. 18 Extracted model of the assembled wafer-level package test vehicle.

In the model in Figure 6.18, due to problems with assembly, additional loss was included as  $2K\Omega$  resistors in parallel with the Si-on-APPE line. This resistance was estimated from the TDR measurement of the assembled test vehicle in Figure 6.19. This was caused by the interaction between solders on the APPE coplanar line during the assembly process.

The extracted model in Figure 6.18 was verified by comparing its TDR/TDT simulation waveforms to measurements, as shown in Figure 6.19. The solid line in Figure 6.19(a) was measured using TDR with the far end open in the assembled test vehicle. The dotted line in Figure 6.19(a) was simulated using the extracted model in Figure 6.18. Figure 6.19(b) shows the comparison between the TDT measurement and simulation. The simulations and measurements show good agreement.

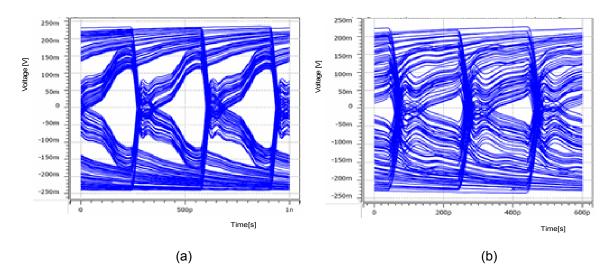


**Figure 6.19** Model-to-hardware correlation for the assembled test vehicle. (a) TDR measurement and simulation with far end open and (b) TDT measurement and simulation.

#### 6.4.2. Eye-diagram simulation

Eye-diagrams were simulated using the extracted model in Figure 6.18 at 3Gbps and 5Gbps data rates, as shown in Figure 6.20. The binary random source had a peak-topeak amplitude of 1V, 30ps risetime, and 10ps jitter with 50  $\Omega$  source output impedance. The far end of the extracted model in Figure 6.18 was terminated with the characteristic impedance of the board transmission line. The eye-diagrams in Figure 6.20 were simulated at the far end of the test vehicle.

As shown in Figure 6.20, the eye-diagrams do not have sufficient eye-opening for 3Gbps and 5Gbps data transmission. Therefore, the fabricated test vehicle cannot be used for either 3Gbps and 5Gbps signal transmission due to the following two reasons. The first reason is due to problem with the assembly process that created a loss ( $2K\Omega$  resistor in Figure 6.18). The second reason is due to the Si-on-APPE line in Figure 6.18, which increases the capacitance of the transmission line. The Si-on-APPE line caused the mismatch in characteristic impedance between the Si-on-APPE line and APPE line. However, these two problems can be solved by enhancing the assembly process and redesign of the APPE line on the substrate.



**Figure 6.20** Simulated eye-diagrams for the assembled wafer-level package test vehicle in Figure 6.16 at (a) 3Gbps and (b) 5Gbps data rates.

#### 6.4.3. Enhancement of the assembly process

The assembly process caused a loss equivalent to a  $2K\Omega$  resistor in Figure 6.18. After enhancing the assembly process, the loss of  $2K\Omega$  would be removed. Then, the eye-diagram of the assembled test vehicle becomes much better at 5Gbps data rate, as shown in Figure 6.21.

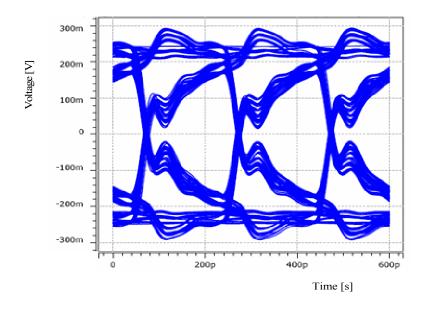


Figure 6.21 Eye-diagram at 5Gbps data rate for the test vehicle with proper assembly process.

#### 6.4.4 Redesign of the test vehicle

The eye-diagram in Figure 6.21 is still not sufficient for 5Gbps data transmission using the test vehicle, in spite of the proper assembly process. It is because of the impedance mismatch between the Si-on-APPE line and APPE line in Figure 6.16. More improvement can be achieved by changing the characteristic impedance of the APPE line to match the characteristic impedance of the Si-on-APPE line in the fabricated test vehicle, as shown in Figure 6.22. If the characteristic impedance of the APPE line is 64  $\Omega$ , the eye-diagram of the test vehicle becomes better, as shown in Figure 6.23. The 64 ohm characteristic impedance of the coplanar APPE line can be implemented using a center-conductor width of 2.5 mils, metal gap of 1 mil with a metal thickness of 9um on 1mm thick APPE board. However, the dimensions are difficult to fabricate using board fabrication process. Using a metal thickness of 35um (1 oz.) on 1mm thick APPE board,

the 64 ohm characteristic impedance can also be achieved using a center-conductor width of 2.5 mils and metal gap of 1.5 mils. The silicon transmission line is the same as discussed earlier on 2000  $\Omega$ -cm resistivity silicon substrate (Figure 6.16), and the solder bumps with 50um diameter and 100um pitch can be used.

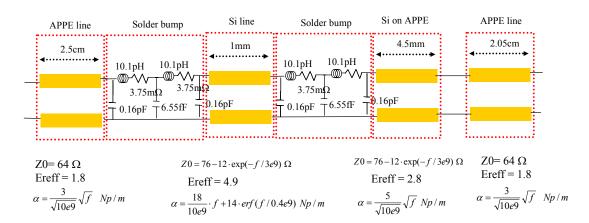


Figure 6.22 Equivalent circuit for the re-designed wafer-level package test vehicle.

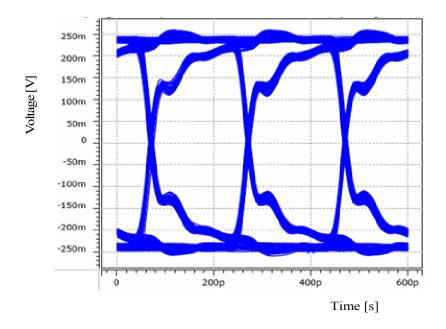


Figure 6.23 Simulated eye-diagram at 5Gbps data rate for the re-designed test vehicle.

In Section 4.3, the minimum capacitance of the solder bumps was estimated to be ~0.16pF for 5Gbps data transmission. However, even with solder bumps of 50um diameter and 100um pitch which correspond to a capacitance of 0.32pF, the eye-diagram shows good eye-opening in Figure 6.23. This is because of the better impedance matching between transmission lines.

#### 6.5. Design procedure for the wafer-level package test vehicle

From the above simulations and measurements of the wafer-level package test vehicle, the following design procedure has been recommended for the design of the wafer-level package on integrated board:

- First of all, characteristic impedance matching between board and silicon transmission lines should be first considered. Good impedance matching can reduce the effect of parasitic capacitance on transmitted signals.
- Next, parasitic capacitance in wafer-level package on integrated board should be kept minimum. Since signal-line bendings can induce parasitic capacitance [F7][F8][F9], minimum number of signal bendings must be used. Especially, rightangle bendings should be avoided. Instead, use 45 degree angle bendings.
- 3) Finally, after the consideration of impedance matching and parasitic capacitance, low-loss board and silicon materials should be considered for better signal integrity. If low-loss board and silicon material are used with a high parasitic capacitance, the capacitance will limit the overall performance regardless of the low-loss board and silicon material.

#### 6.6. Summary

In this chapter, we investigated the effect of assembled wafer-level package, silicon substrate and board material, and material interfaces on gigabit data transmission using the wafer-level package test vehicle. Two configurations for the test vehicle were compared, namely the FR4 board/100 $\Omega$ -cm resistivity silicon substrate wafer level package test vehicle and the APPE board/2000 $\Omega$ -cm resistivity silicon substrate WLP test vehicle. From the eye-diagram simulations of these two test vehicles, it was concluded that better signal integrity cannot be achieved only by using lower loss material, but also requires low parasitic capacitance for signal transmission from the chip to the board. In addition, the proper design procedure for achieving signal integrity in the wafer level package test vehicle is 1) first, design transmission lines with better impedance matching and 2) achieve smaller parasitic capacitance. Since the assembly process caused an unexpected loss equivalent to  $2K\Omega$  resistors in the assembled test vehicle, the wafer-level package test vehicle is being re-assembled using the proper assembly process.

# Chapter 7

# **Conclusion & Future Work**

In this dissertation, we have proposed TDR-based methods that enable gigabit data transmission in both the IC and package. The wafer-level package on an integrated board has been investigated using the TDR-based methods for gigabit data transmission in both the IC and package.

First, the need for TDR measurements in digital systems has been explained in Chapter 1. It has been shown that digital signal response to a system can be translated into a step pulse response to the system. The importance of the low frequency spectrum of the step pulse response has been described using the frequency spectrum of step pulses.

Second, the Short-Open-Load-Line calibration for TDR measurements has been proposed in Chapter 2 to extract frequency-domain information from TDR measurements. It has been shown that the uncertainty of TDR with ±1.5ps drift is lower than common Network Analyzers at frequencies below ~2GHz, but higher at frequencies >2GHz, which means that TDR is more accurate at frequencies below ~2GHz than VNAs for one-port measurements. For inductors and microwave filters, the accuracy of the SOLL calibration has been compared to NA measurements.

Third, the frequency-dependent characteristic impedance and propagation constant of package transmission lines have been extracted from TDR measurements using the Short-Open-Load-Line calibration in Chapter 3. Non-physical RLGC models for package transmission lines have been developed for simulating the extracted data from TDR measurements in Chapter 3. The accuracy of the extracted data and non-physical RLGC models has been verified by comparing simulations to measurements.

Fourth, silicon transmission lines have been characterized using TDR and NA measurements in Chapter 4. The slow-wave effect in silicon transmission lines has been extracted and modeled from NA measurements. Non-physical RLGC models for silicon transmission lines with the slow-wave effect have been proposed for simulating the extracted data from TDR and NA measurements. The accuracy of the extracted data and non-physical RLGC models for silicon transmission lines has been verified by showing good agreement between simulations and measurements in the time and frequency domains.

Fifth, coupled lines and differential lines have been characterized using TDR measurements in Chapter 5. Non-physical RLGC models for coupled lines have been developed for simulating the extracted data from TDR measurements. The accuracy of the extracted data and non-physical RLGC models for coupled lines has been verified by showing good correlation between simulations and measurements.

Sixth, non-physical RLGC models for multi-conductor transmission lines have been proposed showing excellent stability in Chapter 5. For example, lossy (3+1)-conductor transmission lines and (64+1)-conductor transmission lines have been simulated showing excellent stability.

Finally, the effect of the parasitic capacitance of packages on gigabit data transmission has been investigated in the wafer-level package test vehicle. The solder bumps with 50um diameter and 100um pitch have been analytically modeled. It has been shown that better signal integrity in gigabit data transmission cannot be achieved only by using lower loss material, but also requires a smaller parasitic capacitance at the same time. Although the maximum parasitic capacitance for the fabricated wafer-level

216

package test vehicle has been ~0.16pF for 5Ghz digital signal propagation, the effect of the parasitic capacitance can be reduced by designing silicon and package transmission lines with similar characteristic impedance.

Based on the discussions in this dissertation, the following two recommendations for designing wafer-level packages on an integrated board have been drawn for gigabit data transmission in both the IC and package. First, a smaller difference in the characteristic impedance of board and silicon transmission lines yields better signal integrity. Hence, board and silicon transmission lines need to be designed to have the same characteristic impedance. Second, reducing the parasitic capacitance of solder bumps yields better signal integrity. Since smaller solder bumps have smaller parasitic capacitance, solder bumps need to be fabricated as small as possible. If the parasitic capacitance is high, the mismatch in the characteristic impedance should be small for gigabit data transmission. If the mismatch in the characteristic impedance is high, the parasitic capacitance can limit the maximum operating frequency of wafer-level package on integrated board regardless of the board and silicon loss.

Based on the above conclusions, the following areas of research are appropriate as an extension to the methods described in this dissertation:

- Re-design of the wafer-level package test vehicle: Based on the above conclusions in this dissertation for wafer-level packages on integrated boards, the wafer-level package test vehicle can be re-designed for higher gigabit data transmission.
- 2. **Microstrip-type wafer-level package test vehicle:** The assembled wafer-level package test vehicle consisted of co-planar transmission lines. However, since microstrip lines are more practical transmission lines, the consideration of

217

microstrip-type wafer-level package test vehicles is important for practical applications.

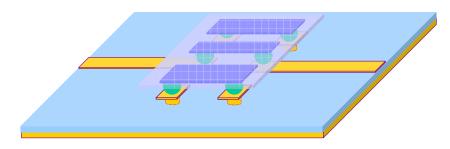


Figure 7.1 Microstrip-type wafer-level package test vehicle.

3. Wafer-level package test vehicle including integrated circuits: The final wafer-level package test vehicles will be test vehicles including integrated circuits for demonstrating chip-to-chip gigabit data transmission.

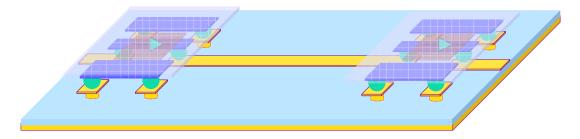


Figure 7.2 wafer-level package test vehicle including integrated circuits.

## Appendix A. Simulation of (64+1)-conductor transmission lines

An automated Matlab code was written for simulating (64+1)-conductor transmission lines, which consisted of 'Gen\_RLGCmodel\_generation\_file.m' and 'insert\_dot.m.' The Matlab code generated the following two Matlab files: 'main\_NPRLGC\_generation.m' and 'sub\_NPRLGC\_generation.m.' These two files included the non-physical RLGC model of (64+1)-conductor transmission lines. The resistance, inductance, conductance and capacitance of (64+1)-conductor transmission lines can be changed in 'main\_NPRLGC\_generation.m'. Then, 'main\_NPRLGC\_generation.m' was executed in Matlab. The output of the execution was 'NPRLGC\_65\_conductorline.dat,' which included the W-element tabular model for (64+1)-conductor transmission lines. The resistance tabular model for generation.m' The W-element model can be simulated in Hspice. The codes can be applied for generating non-physical RLGC models of any (N+1)-conductor transmission lines for N≥2.

### A.1. Gen\_RLGCmodel\_generation\_file.m

clear all close all

```
N=64: %number of signal conductor lines
fprintf(' Generating (%d+1)-conductor line Non-physical RLGC model... \n', N);
fprintf(' Please execute main_NPRLGC_generation.m later... \n');
count = 0;
for jj=1:N
 S='Z0 mode'; cc = num2str(jj); S = strcat(S,cc);
                                            S = strcat(S, ' ');
 for kk=1:N
   aaa = num2str(kk);
                      Sa = strcat(S,aaa);
   S1=sprintf('syms %s;',Sa);
                            S2=sprintf('Z0(jj,kk)= %s;',Sa);
   eval(S1);
              eval(S2);
 end
end
count = 0;
for jj=1:N
 S='Vp mode'; cc = num2str(jj);
                             S = strcat(S,cc);
                                            S = strcat(S, ' ');
```

```
for kk=1:N
                      Sa = strcat(S.aaa);
   aaa = num2str(kk);
   S1=sprintf('syms %s;',Sa);
                           S2=sprintf('Vp(jj,kk)= %s;',Sa);
   eval(S1);
              eval(S2);
  end
end
count = 0:
for jj=1:N
  S='alpha mode':
                cc = num2str(jj); S = strcat(S,cc); S = strcat(S,' ');
 for kk=1:N
   aaa = num2str(kk);
                      Sa = strcat(S,aaa);
   S1=sprintf('syms %s;',Sa);
                           S2=sprintf('alpha1(jj,kk)= %s;',Sa);
   eval(S1):
              eval(S2);
  end
end
for jj=1:N
  aaa = sprintf('%d',jj); S = strcat('L ',aaa);
 for ii=1:N
   aa = sprintf('%d',ii);
                     S1 = strcat(S,aa);
   Sc=sprintf('syms %s;',S1);
                          Sd=sprintf('L(jj,ii)= %s;',S1);
   eval(Sc);
              eval(Sd);
 end
end
for jj=1:N
 aaa = sprintf('%d',jj); S = strcat('C ',aaa);
 for ii=1:N
   aa = sprintf('%d',ii);
                      S1 = strcat(S,aa);
   Sc=sprintf('syms %s;',S1);
                           Sd=sprintf('C(jj,ii)= %s;',S1);
   eval(Sc);
              eval(Sd);
 end
end
for jj=1:N
 aaa = sprintf('%d',jj); S = strcat('R ',aaa);
 for ii=1:N
   aa = sprintf('%d',ii);
                      S1 = strcat(S.aa);
   Sc=sprintf('syms %s;',S1);
                          Sd=sprintf('R(jj,ii)= %s;',S1);
   eval(Sc);
            eval(Sd);
 end
end
for jj=1:N
 aaa = sprintf('%d',jj); S = strcat('G ',aaa);
 for ii=1:N
   aa = sprintf('%d',ii);
                      S1 = strcat(S,aa);
   Sc=sprintf('syms %s;',S1);
                           Sd=sprintf('G(jj,ii)= %s;',S1);
   eval(Sc);
              eval(Sd);
 end
```

# end

```
matrix number = ones(N,N);
for ii=1:N
 for i = 1:N
   if jj == N-ii+2
    matrix number(ii,jj) = -1;
   end
 end
end
%matrix mode numbers, eeeee
L_matrix_total = zeros(N,N,N);
for kk=1:N
 for ii=1:N
   for jj=1:N
    if matrix number(kk,ii) == matrix number(ii,jj)
      if kk == jj
        L_matrix(ii,jj) = 1;
      else
      L matrix(ii,jj) = 1;
      end
     else
       L matrix(ii,jj) = -1;
     end
   end
  end
 L_matrix_total(:,:,kk) = L_matrix;
end
R matrix total = L matrix total;
C matrix total = zeros(N,N,N);
for kk=1:N
 for ii=1:N
   for jj=1:N
    if matrix number(kk,ii) == matrix number(ii,jj)
      if kk == ji
        C matrix(ii,jj) = 1;
      else
       C_{matrix(ii,jj)} = 0;
      end
     else
       C matrix(ii,jj) = 2;
     end
   end
  end
 C_matrix_total(:,:,kk) = C_matrix;
end
```

```
G matrix total = C matrix total;
capacitance extraction = 1./(Z0.*Vp);
inductance extraction = Z0 ./ Vp;
resistance extraction = alpha1.*Z0;
conductance extraction = alpha1 ./Z0;
for kk = 1:N
  L extracted(:,kk) = inv(L matrix total(:,:,kk))*inductance extraction(:,kk);
  C extracted(:,kk) = inv(C matrix total(:,:,kk))*capacitance extraction(:,kk);
  R_extracted(:,kk) = inv(R_matrix_total(:,:,kk))*resistance_extraction(:,kk);
  G_extracted(:,kk) = inv(G_matrix_total(:,:,kk))*conductance_extraction(:,kk);
  over_Z0_Vp(:,kk) = C_matrix_total(:,:,kk)*C(kk,:).';
  Z0 over Vp(:,kk) = L matrix total(:,:,kk)*L(kk,:).';
  alpha ZO(:,kk) = R matrix total(:,:,kk)*R(kk,:).';
  alpha over Z0(:,kk) = G matrix total(:,:,kk)*G(kk,:).';
end
L extracted = L extracted.';
C extracted = C extracted.';
R extracted = R extracted.';
G_extracted = G_extracted.';
Z0 Vp = 1 / \text{over } Z0 Vp;
Z0 2 = Z0_Vp .* Z0_over_Vp;
Z0_extracted = sqrt(Z0_2);
Vp_2 = Z0_Vp ./ Z0_over_Vp;
Vp extracted = sqrt(Vp 2);
alpha 2 = alpha Z0 .* alpha over Z0;
alpha extracted = sqrt(alpha 2);
syms Gd
Gd matrix = Gd^*eye(N);
G extracted = G extracted + Gd matrix;
R spice = R extracted;
L_spice = L_extracted;
for ii=1:N
  for jj=1:N
    if ii == ji
      C_spice(ii,jj)=sum(C_extracted(ii,:));
    else
      C spice(ii,jj)=-C extracted(ii,jj);
    end
  end
```

```
end
```

```
for ii=1:N
  for jj=1:N
    if ii == ji
      G spice(ii,jj)=sum(G extracted(ii,:));
    else
       G spice(ii,jj)=-G extracted(ii,jj);
    end
  end
end
for jj=1:N
  aaa = sprintf('%d',jj);
                       S = strcat('Cspice ',aaa);
  for ii=1:N
    aa = sprintf('%d',ii);
                           S1 = strcat(S,aa);
    Sc=sprintf('syms %s;',S1);
                                 Sd=sprintf('Cspice(jj,ii)= %s;',S1);
    eval(Sc);
                 eval(Sd);
  end
end
for jj=1:N
  aaa = sprintf('%d',jj);
                       S = strcat('Gspice ',aaa);
  for ii=1:N
    aa = sprintf('%d',ii);
                           S1 = strcat(S.aa);
    Sc=sprintf('syms %s;',S1);
                                 Sd=sprintf('Gspice(jj,ii)= %s;',S1);
    eval(Sc);
                 eval(Sd);
  end
end
fid = fopen('main NPRLGC generation.m','w');
fprintf(fid, freg = logspace(0, 11, 200); \n');
fprintf(fid, freq = [0 freq]; \n \n');
fprintf(fid, 'L11 = 2.977e-7*ones(size(1:length(freg))); \%\%H/m \n');
fprintf(fid, 'L12 = 2.600e-8*ones(size(1:length(freg))); \%\%H/m \n');
fprintf(fid, 'L13 = 6.820e-9*ones(size(1:length(freq))); %%H/m \n');
fprintf(fid, 'C11 = (9.86e-11 - 2.73e-12 - 4.43e-13)*ones(size(1:length(freg))); %%F/m \n');
fprintf(fid, 'C12 = 2.73e-12*ones(size(1:length(freq))); %%F/m \n');
fprintf(fid, 'C13 = 4.43-13*ones(size(1:length(freq))); %%F/m \n');
fprintf(fid, 'alpha all mode = 0*(0.3*erf(freg/0.6e9)+0.8/10e9*freg) + 13/1e10 * freg +
0.001: \n \n'):
fprintf(fid, 'Gd = 0; \n \);
fprintf(fid,'\n');
for ii = 1:N
  for jj =1:N
    if ii == ii
      fprintf(fid, '%s = %s; \n', char(L(ii, jj)), 'L11');
    elseif abs(ii-jj) == 1
      fprintf(fid, '%s = %s; \n', char(L(ii, jj)), 'L12');
```

```
elseif abs(ii-jj) == 2
      fprintf(fid, '%s = %s; \n', char(L(ii, jj)), 'L13');
    else
      fprintf(fid, '%s = %s; \n', char(L(ii, jj)), '0');
    end
  end
end
fprintf(fid,'\n');
for ii = 1:N
  for jj =1:N
    if ii == ji
      fprintf(fid, '%s = %s; \n', char(C(ii, jj)), 'C11');
    elseif abs(ii-jj) == 1
      fprintf(fid, '%s = %s; \n', char(C(ii,jj)), 'C12');
    elseif abs(ii-jj) == 2
      fprintf(fid, '%s = %s; \n', char(C(ii, jj)), 'C13');
    else
      fprintf(fid, '%s = %s; \n', char(C(ii,jj)), '0');
    end
  end
end
fprintf(fid,'%%%%%%%%%generate Z0 parameters %%%%%%%% \n\n');
fprintf(fid,'\n');
for ii = 1:N
  for ii =1:N
    fprintf(fid,'%s = %s; \n',char(Z0(ii,jj)),insert_dot(Z0_extracted(ii,jj)));
  end
end
fprintf(fid,'\n');
for ii = 1:N
  for jj =1:N
    fprintf(fid,'%s = %s; \n',char(Vp(ii,jj)),insert dot(Vp extracted(ii,jj)));
  end
end
%%%%%%% \n\n');
fprintf(fid,'\n');
for ii = 1:N
  for ii =1:N
    fprintf(fid,'%s = %s; \n',char(alpha1(ii,jj)),'alpha all mode');
  end
end
fprintf(fid, '\n \n');
fprintf(fid,'sub_NPRLGC_generation(');
```

```
fprintf(fid,'freq, %s, %s, %s ',char(Z0(1,1)),char(Vp(1,1)),char(alpha1(1,1)));
for ii=1:N
  for jj=1:N
    if ii == 1 & jj == 1
    else
       fprintf(fid,',%s, %s, %s',char(Z0(ii,jj)),char(Vp(ii,jj)),char(alpha1(ii,jj)));
    end
  end
end
fprintf(fid,',Gd');
fprintf(fid,'); \n');
fclose(fid);
%%%%%%%%%%%generate sub generation file%%%%%%%
fid = fopen('sub NPRLGC generation.m','w');
fprintf(fid,'function []=sub_NPRLGC_generation(');
fprintf(fid,'freq, %s, %s, %s ',char(Z0(1,1)),char(Vp(1,1)),char(alpha1(1,1)));
for ii=1:N
  for jj=1:N
    if ii == 1 & jj == 1
    else
       fprintf(fid,',%s, %s, %s',char(Z0(ii,jj)),char(Vp(ii,jj)),char(alpha1(ii,jj)));
    end
  end
end
fprintf(fid,',Gd');
fprintf(fid,'); \n');
fprintf(fid,'%%%%%%%%%%%%%%generate L parameters %%%%%%%% \n\n');
fprintf(fid,'\n');
for ii = 1:N
  for jj =1:N
    fprintf(fid,'%s = %s; \n',char(L(ii,jj)),insert dot(L extracted(ii,jj)));
  end
end
fprintf(fid,'\n');
for ii = 1:N
  for jj =1:N
    fprintf(fid,'%s = %s; \n',char(Cspice(ii,jj)),insert dot(C spice(ii,jj)));
  end
end
fprintf(fid,'\n');
for ii = 1:N
  for jj =1:N
```

```
fprintf(fid,'%s = %s;\n',char(R(ii,jj)),insert dot(R extracted(ii,jj)));
  end
end
fprintf(fid,'\n');
for ii = 1:N
  for ii =1:N
    fprintf(fid,'%s = %s; \n',char(Gspice(ii,jj)),insert dot(G spice(ii,jj)));
  end
end
fprintf(fid,'%%%%%%%%%%R, L, G, C input for W-element %%%% \n');
fprintf(fid,'\n');
fprintf(fid, 'Rinput=[ freg" ');
for kk =1:N
  for ii = 1:kk
    fprintf(fid,' %s" ', char(R(kk,ii)));
  end
end
fprintf(fid,']; \n');
fprintf(fid, 'Linput=[ freq" ');
for kk =1:N
  for ii = 1:kk
    fprintf(fid,' %s" ', char(L(kk,ii)));
  end
end
fprintf(fid,']; \n');
fprintf(fid, 'Ginput=[ freq" ');
for kk =1:N
  for ii = 1:kk
    fprintf(fid,' %s" ', char(Gspice(kk,ii)));
  end
end
fprintf(fid,']; \n');
fprintf(fid, 'Cinput=[ freq" ');
for kk =1:N
  for ii = 1:kk
    fprintf(fid,' %s" ', char(Cspice(kk,ii)));
  end
end
fprintf(fid,']; \n');
fprintf(fid, '\n');
```

```
fprintf(fid,' fid = fopen("NPRLGC_%d_conductorline.dat","w"); \n',N+1);
```

fprintf(fid, 'fprintf(fid,".MODEL NPRLGC\_%d\_conductor W MODELTYPE=TABLE N=%d LMODEL=Imod\_%d CMODEL=cmod\_%d RMODEL=rmod\_%d GMODEL=gmod\_%d \\n \\n");', N+1,N,N+1,N+1,N+1);

```
fprintf(fid,'\n');
fprintf(fid, 'fprintf(fid,".MODEL Imod %d sp N=%d SPACING=NONUNIFORM
VALTYPE=REAL INTERPOLATION=SPLINE \\n"); \n',N+1,N);
fprintf(fid, 'fprintf(fid,"+ EXTRAPOLATION=LINEAR INFINITY= "); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=2:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid, "%%10.5e ",Linput(length(freg),iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'fprintf(fid,"+ DATA=(%%d,", length(freq)); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid, "%%10.5e ",Linput(1,iii)); \n');
for intf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n'):
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid, 'for kkk = 2:length(freg) \n');
fprintf(fid,'\t fprintf(fid, "+ "); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid,"%%10.5e ",Linput(kkk,iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'end \n');
fprintf(fid,'fprintf(fid,"+ ) \\n \\n" ); \n');
```

```
fprintf(fid.'\n'):
fprintf(fid, 'fprintf(fid,".MODEL cmod_%d sp N=%d SPACING=NONUNIFORM
VALTYPE=REAL INTERPOLATION=SPLINE \\n"); \n',N+1,N);
fprintf(fid, 'fprintf(fid,"+ EXTRAPOLATION=LINEAR INFINITY= "); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=2:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid,"%%10.5e ",Cinput(length(freq),iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'fprintf(fid,"+ DATA=(%%d,", length(freg)); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid,"%%10.5e ",Cinput(1,iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid, 'for kkk = 2:length(freq) \n');
fprintf(fid,'\t fprintf(fid, "+ "); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid, "%%10.5e ",Cinput(kkk,iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'end \n');
fprintf(fid,'fprintf(fid,"+ ) \\n \\n" ); \n');
fprintf(fid,'\n');
```

```
fprintf(fid, 'fprintf(fid,".MODEL rmod %d sp N=%d SPACING=NONUNIFORM
VALTYPE=REAL INTERPOLATION=SPLINE \\n"); \n',N+1,N);
fprintf(fid, 'fprintf(fid,"+ EXTRAPOLATION=LINEAR INFINITY= "); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=2:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid, "%%10.5e ",Rinput(length(freg),iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'fprintf(fid,"+ DATA=(%%d,", length(freg)); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid, "%%10.5e ",Rinput(1,iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid, 'for kkk = 2:length(freq) \n');
fprintf(fid,'\t fprintf(fid, "+ "); \n');
fprintf(fid, 'fprintf(fid, "( "); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid,''%%10.5e '',Rinput(kkk,iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 \& iii \sim = 1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'end \n');
fprintf(fid,'fprintf(fid,"+ ) \\n \\n" ); \n');
fprintf(fid,'\n');
fprintf(fid, 'fprintf(fid,".MODEL gmod %d sp N=%d SPACING=NONUNIFORM
VALTYPE=REAL INTERPOLATION=SPLINE \\n"); \n',N+1,N);
fprintf(fid, 'fprintf(fid,"+ EXTRAPOLATION=LINEAR INFINITY= "); \n');
```

```
fprintf(fid, 'fprintf(fid, ''( ''); \n');
fprintf(fid, 'for iii=2:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid,''%%10.5e '',Ginput(length(freq),iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 \& iii \sim 1 \langle n' \rangle;
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'fprintf(fid,"+ DATA=(%%d,", length(freg)); \n');
fprintf(fid, 'fprintf(fid, ''( ''); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid, "%%10.5e ",Ginput(1,iii)); \n');
fprintf(fid, '\t if rem(iii, 15) == 1 & iii \sim=1 \n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid, 'for kkk = 2:length(freq) \n');
fprintf(fid,'\t fprintf(fid, "+ "); \n');
fprintf(fid, 'fprintf(fid, ''( ''); \n');
fprintf(fid, 'for iii=1:length(Rinput(1,:)) \n');
fprintf(fid, '\t fprintf(fid, "%%10.5e ",Ginput(kkk,iii)); \n');
fprintf(fid, '\ tif rem(iii, 15) == 1 \& iii \sim = 1 \ n');
fprintf(fid, '\t \t fprintf(fid,"\\n"); \n');
fprintf(fid, '\t \t fprintf(fid,"+ "); \n');
fprintf(fid, ' \t end \n');
fprintf(fid, 'end \n');
fprintf(fid, 'fprintf(fid,") \\n"); \n');
fprintf(fid,'end \n');
fprintf(fid,'fprintf(fid,"+ ) \\n \\n" ); \n');
fprintf(fid,'\n fclose(fid);');
```

fclose(fid);

#### A.2. insert\_dot.m

```
function [BB] = insert_dot(AAA)
AA = char(AAA);
length_AA = length(AA);
count = 0;
for kk=1:length_AA
    count = count+1;
    if AA(kk) == '/' | AA(kk) == '*' | AA(kk) == 'A'
        BB(count) = '.';
        count = count+1;
        BB(count) = AA(kk);
    else
        BB(count) = AA(kk);
    end
end
```

# A.3. Hspice input file

# Appendix B. VNA characterization of transmission lines

The characteristic impedance and propagation constant of transmission lines can be extracted using two transmission lines, as shown in Figure B.1. The two transmission lines have the same physical dimensions with different length. In this analysis, the left parasitics are assumed to be symmetric to the right unknown parasitics since they have the same pad transitions.

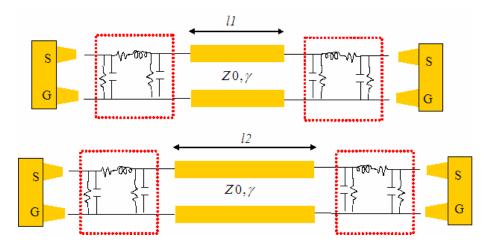


Figure B.1 Two transmission-line measurements for the characterization of transmission lines using Network Analyzers.

Then, Figure B.1 can be expressed in the ABCD parameter's form as follows:

$$\begin{bmatrix} a & b \\ c & (1+bc)/a \end{bmatrix} \begin{bmatrix} \cosh(\gamma \cdot l1) & Z0 \cdot \sinh(\gamma \cdot l1) \\ \frac{1}{Z0} \sinh(\gamma \cdot l1) & \cosh(\gamma \cdot l1) \end{bmatrix} \begin{bmatrix} (1+bc)/a & b \\ c & a \end{bmatrix} = \begin{bmatrix} Ma1 & Mb1 \\ Mc1 & Md1 \end{bmatrix} = M1$$
(B.1)  
$$\begin{bmatrix} a & b \\ c & (1+bc)/a \end{bmatrix} \begin{bmatrix} \cosh(\gamma \cdot l2) & Z0 \cdot \sinh(\gamma \cdot l2) \\ \frac{1}{Z0} \sinh(\gamma \cdot l2) & \cosh(\gamma \cdot l2) \end{bmatrix} \begin{bmatrix} (1+bc)/a & b \\ c & a \end{bmatrix} = \begin{bmatrix} Ma2 & Mb2 \\ Mc2 & Md2 \end{bmatrix} = M2$$
(B.2)

where  $\begin{bmatrix} a & b \\ c & (1+bc)/a \end{bmatrix}$  is the error box of the left side parasitics  $\begin{bmatrix} (1+bc)/a & b \\ c & a \end{bmatrix}$  is the error box of the right side parasitics

and *a*, *b*, and *c* are the components of the unknown parasitics. M1 and M2 are the ABCD parameters converted from measured S-parameters. Z0 is the characteristic impedance and  $\gamma$  is the propagation constant. According to [1], the propagation constant  $\gamma$  can be easily extracted using the following equation without knowing the unknown parasitics, *a*, *b*, *c*.

$$Tr(M1 M2^{-1}) = 2\cosh(\gamma(l2-l1))$$
 (B.3)

where *Tr* is the trace defined as the sum of diagonal elements.

Compared to the propagation constant, the characteristic impedance extraction is not easy because it is not always possible. In Equation (B.1) and (B.2), there exist only 3 independent equations for 4 unknown variables such as a, b, c, and Z0. For extracting Z0, therefore, one variable among a, b, and c must be assumed to be known. For example, a = 1 was used in [2][3]. Consequently, in order to extract Z0, the circuit models for the unknown parasitics are limited to models producing only two variables in their ABCD parameters. Symbolic Math in Matlab can be used to solve Equation (B.1) and (B.2) generating accurate results.

Pad deembedding is for extracting the pad parasitics such as *a*, *b* and *c* in Figure B.1. Once if the characteristic impedance and propagation constant of the transmission line is found, general pad de-embedding is possible using Equation (B.1) and (B.2) since there are three independent equations and three unknown variables.

# References

[A1] International Technology Reoadmap for Semiconductors, http://public.itrs.net.

- [A2] R. R. Tummala, *Fundamentals of Microsystems Packaging*, McGraw-Hill: New York, 2001.
- [A3] C.-Y. Chung, W. Shi, and A. Waizman, "Achieving 3.2 Gb/s, 400MTS AGTL+ IO through robust power delivery design with minimal package size," *DesignCon 2002*.
- [A4] Intel, Intel Pentium 4 Processor 423 Pin Socket (PGA423) Design Guideline, 2000.
- [A5] Intel Applcation note AP-577, <u>An introduction to Plastic Pin Grid Array (PPGA)</u> <u>Packaging</u>, June 1997.
- [A6] Jinseong Choi, <u>Modeling of Power Supply Noise in Large Chips using the Finite</u> <u>Difference Time Domain Method</u>, Thesis (Ph. D), School of Electrical and Computer Engineering, Georgia Institute of Technology, 2003.
- [A7] L. Ritchey, "How poor packaging kills good PCB designs," EE Design *Exclusive Features* (eedesign.com), Jan. 2004.
- [A8] W. Kim and et al., "Electrical Design of Wafer Level Package on Board for Gigabit Data Transmission," 5<sup>th</sup> Electronics Packaging Technology Conference, Dec. 2003.
- [A9] T.K.Sakar, Z.A. Maricevic J., B. Zhang, A. R. Djordjevic, "Evaluation of Excessive Inductance and Capacitance Of Microstrip Junction," IEEE Trans. Microwave Theory and Tech., vol. 42, pp. 1095-1097, June 1994.
- [A10] P.L. Werner and R. Mittra, "A new technique for the Extraction of SPICE-type Equivalent Circuits from Measured or Computed S-Parameters of Microstrip Components and Discontinuities," IEEE 6th Electrical Performance of Electronic Packaging, pp. 70-73, Oct. 1997.
- [A11] J.-M. Jong and V.K. Tripathi, "Time-Domain Characterization of Interconnect Discontinuities in High-Speed Circuits," IEEE Trans. Advanced Packaging, vol. 15, pp. 497-504, Aug. 1992.
- [A12] I. Novak, "Lossy Power Distribution Networks With Thin Dielectric Layers and/or Thin Conductive layers," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp. 353-360, Aug. 2000.
- [A13] J.M. Hobbs, et al., "Simultaneous Switching Noise Suppression for High Speed Systems Using Embedded Decoupling," *Proceedings of 2001 Electronic Components and Technology Conference*, May 2001.

- [A14] R. H. Bowles and R. Charbonneau, "An overview of the NCMS embedded capacitance project," in *Proc. NCMS Embedded Capacitance Conf.*, Tempe, AZ, Feb. 2000.
- [A15] R. Carlson, S.Krakauer, R. Monnier, V. Van Duzer, and R. Woodbury," Sampling oscillography," Hewlett-Packard Applications Note 36, Nov. 1959.
- [A16] "Pulse reflection measurement of transmission line impedance and discontinuities," in-house publication, Tektronix, 1962.
- [A17] "Time domain reflectometry," Hewlett-Packard Applications Note 62, 1964.
- [A18] A.S. Farber and C.W.Ho, "Wide-band network characterization by Fourier Transformation of time-domain measurements," IEEE Journal of Solid-State Circuits, vol. 4, pp. 231-235, Aug. 1969.
- [A19] M.F.Iskander and M.A.K. Hamid, "A Time-Domain Technique for Characterizing Leaky Coaxial Cables," MTT-S international Microwave Symposium Digest, vol. 77, pp. 151-154, Jun. 1977.
- [A20] J. Mar, "A time-domain method of measuring transistor parameters," IEEE Journal of Solid-State Circuits, Vol. 6, Issue: 4, pp. 223-226, Aug. 1971.
- [A21] D. Schaubert, "Application of Prony's method to time-domain reflectometer data and equivalent circuit synthesis," IEEE Trans. Antennas and Propagation, Vol. 27, pp.180-184, Mar. 1979
- [A22] J.C.Toscano, A. Elshabini-Riad, S.M. Riad and A.Y. Al-Mazroo, "Wide-band characterization of multilayer thick film structures using a time-domain technique," IEEE Trans. Instrumentation and Measurement, vol. 38, pp. 515-520, Apr. 1989.
- [A23] J.-M. Jong and V.K. Tripathi, "Time-domain characterization of interconnect discontinuities in high-speed circuits," IEEE Trans. Components, Hybrids, and Manufacturing Technology, vol. 15, pp. 497-504, Aug. 1992.
- [A24] V.K. Tripathi, J.B.Rettig and L.Hayden, "Characterization of multiple coupled interconnection lines from time domain measurement," IEEE VLSI Multilevel Interconnection Conference, pp. 416-418, Jun. 1990.
- [A25] V.K. Tripathi and N. Orhanovic, "Time domain characterization of dispersive dissipative interconnects," 1992 Electrical Performance of Electronic Packaging, pp. 167-170, Apr. 1992.
- [A26] K.M. Fidanboylu, S.M. Riad and A. Elsahbini-Riad, "A new time-domain approach for determining the complex permittivity using stripline geometry," IEEE Trans. Instrumentation and Measurement, vol. 39, pp. 940-944, Dec. 1990.
- [A27] R. Nozaki and T.K. Bose, "Broadband complex permittivity measurements by timedomain spectroscopy," IEEE Trans. Instrumentation and Measurement, vol. 39, pp. 945-951, Dec. 1990.

- [A28] K.M. Fidanboylu, S.M. Riad and A. Elshabini-Riad, "An enhanced time domain approach for dielectric characterization using stripline geometry," IEEE Trans. Instrumentation and Measurement, vol. 41, pp. 132-136, Feb. 1992.
- [A29] Hewlett-Packard, "Improving Time Domain Network Analysis for use with HP54120 Digitizing Oscilloscope and TDR," Hewlett Packard Note 62-1, 1988.
- [A30] T. Dhaene, L. Martens, P. Degraeuwe and D. Zutter, "Improved time-domain characterization of high-speed interconnection structures," 1992 Electrical Performance of Electronic Packaging, pp. 142-144, Apr. 1992.
- [A31] J.A.Valdmanis, G. Mourou, and C.W. Gabel,"Picosecond electro-optic sampling system," Appl. phys. Lett., vol. 41, pp. 211-212, Aug. 1982.
- [A32] W. Su and S.M. Riad, "Calibration of time domain network analyzers," IEEE Trans. Instrumentation and Measurement, vol. 42, pp. 157-161, Apr. 1993.
- [A33] T. Dhaene, L. Martens, and D. Zutter, "Calibration and normalization of time domain network analyzer measurements," IEEE Trans. Microwave Theory and Techniques, vol. 42, pp. 580-589, Apr. 1994.
- [A34] P. Ferrari, G. Angenieux and B. Flechet, "A complete calibration procedure for time domain network analyzers," IEEE MTT-S international Microwave Symposium Digest, pp. 1451-1454, June 1992.
- [A35] L.A. Hayden and V.K. Tripathi, "Calibration methods for time domain network analysis," IEEE Trans. Microwave Theory and Tech., vol. 41, pp. 415-420, March 1993.
- [A36] P. Ferrari and G. Angenieux, "Calibration of a time-domain network analyzer: a new approach," IEEE Trans. Instrumentation and Measurement, vol. 49, pp.178-187, Feb. 2000.
- [A37] R. B. Marks, L. A. Hayden, J. A. Jargon, and F. Williams, "Time domain network analysis using the multiline TRL calibration," 44th ARFTG Conference Digest, pp. 47-55, Dec. 1-2, 1994.
- [A38] D. C. DeGroot and R. B. Marks, "Optimizing time-domain network analysis," 46th ARFTG Conference Digest, pp. 19-28, Nov. 30-Dec. 1, 1995.
- [A39] J.M. Jong, V.K. Tripathi, L.A. Hayden and B. Janko, "Lossy interconnect modeling from TDR/T measurements," IEEE 3rd Topical Meeting on Electrical Performance of Electronic Packaging, pp. 133-135, Nov. 1994.
- [A40] J. A. Jargon and M.D. Janezic, "Measuring complex permittivity and permeability using time domain network analysis," IEEE MTT-S International Microwave Symposium Digest, pp. 1407-1410, Jun. 1996.
- [A41] R.D. Lutz, A. Tripathi, V.K. Tripathi, and T. Arabi, "Accurate characterization of board level interconnects for high performance systems," IEEE 6th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 171-174, Oct. 1997.

- [A42] J. Letosa, et al., "Performance limits in TDR technique by Monte Carlo simulation," IEEE Trans. Magnetics, vol. 32, pp. 958-961, May 1996.
- [A43] D.C. DeGroot and J.A. Jargon, "Long term stability in a calibrated time-domain network analyzer," Proc. 1998 Measurement Science Conference, 1998.
- [A44] N.G. Paulter, "Long-term repeatability of a TDR-based printed wiring board dielectric constant measurement system," IEEE Trans. Instrumentation and Measurement, vol. 47, pp. 1469-1473, Dec. 1998.
- [A45] N.G.Paulter, "An Assessment on the Accuracy of Time-Domain Reflectometry for Measuring the Characteristic Impedance of Transmission Lines," IEEE Trans. Instrum. Meas., vol. 50, No. 5, pp. 1381-1388, Oct. 2001.
- [A46] P. Ferrari and G. Angenieux, "A simulation technique for the evaluation of random error effects in time-domain measurement systems," IEEE Trans. Instrumentation and Measurement, pp. 665-671, Jun. 2001.
- [A47] J.-M. Jong, B. Janko and V.K. Tripathi, "Time-domain characterization and circuit modeling of a multilayer ceramic package," IEEE Trans. Comonents, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, vol. 19, pp. 48-56, Feb. 1996.
- [A48] H. Zhu, A.R. Hefner Jr., J.-S. Lai, "Characterization of power electronics system interconnect parasitics using time domain reflectometry," IEEE Trans. Power Electronics, vol. 14, pp. 622-628, Jul. 1999.
- [A49] A. Tripathi and V. K. Tripathi, "Characterization and modeling of multiple coupled lines in an inhomogeneous medium from time-domain reflection measurements," IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications, Vol. 47, pp. 1191-1201, Aug. 2000.
- [A50] S. Pannal and M. Swaminathan, "Extraction of S-Parameters from TDR/TDT Measurements using Rational Functions," IEEE 54th Automatic RF Techniques Groupp (ARFTG) Conference Digest, pp. 45-52, Dec. 1999.
- [A51] M. Swaminathan and S. Pannala and T. Roy, "Extraction of frequency dependent transmission line parameters using TDR/TDT measurements," 2001 Instrumentation and Measurement Technology Conference, pp. 1726-1730, May. 2001.
- [A52] N. Na, K. Choi and M. Swaminathan," Characterization of embedded resistors for high frequency wireless applications," 1998 Radio and Wireless Conference, pp. 117-120, Aug. 1998.
- [A53] V.K. Tripathi, J.B. Rettig and L. Hayden, "Characterization of multiple coupled interconnection lines from time domain measurement," IEEE Seventh International VLSI Multilevel Interconnection Conference, pp. 415-418, Jun. 1990.

- [A54] D.F. Williams, J.E. Rogers, and C.L. Holloway, "Multiconductor transmission line characterization: Representations, approximations, and accuracy," IEEE Trans. Microwave Theory Tech., vol. 47, pp. 403-409, Apr. 1999.
- [A55] M. Sung, et al., "An efficient crosstalk parameter extraction method for high-speed interconnection lines," IEEE Trans. Advanced Packaging, vol. 23, pp. 148-155, May 2000.
- [A56] D. A. Smolyansky and S.D. Corey, "Computing Self and Mutual Capacitance and Inductance using even and Odd TDR measurements," IEEE Electrical Performance of Electronic Packaging, pp. 117-122, Oct. 2002.
- [A57] J.C. Tippet and R.A. Speciale, "A Rigorous Technique for Measuring the Scattering Matrix of a Multiport Device with a 2-port Network Analyzer," IEEE Trans. Microwave Theory and Tech., Vol. 30, pp. 661-666, May 1982.
- [A58] H. Dropkin, "Comments on 'A Rigorous Technique for Measuring the Scattering Matrix of a Multiport Device with a 2-port Network Analyzer'," IEEE Trans. Microwave Theory and Tech., vol. 31, pp. 79-81, Jan. 1983.
- [A59] S. Sercu and L. Martens, "Characterizing N-port Packages and Interconnections with a 2-port Network Analyzer," IEEE 6<sup>th</sup> Topical Meeting on Electrical Performance of Electronic Packaging, pp. 163-166, Oct. 1997.
- [A60] D.E. Bockelman and W. R. Eisenstadt, "Combined differential and common-mode scattering parameters: Theory and simulation," IEEE Trans. Microwave Theory and Tech., vol. 43, pp. 1530-1539, July 1995.
- [A61] <u>A Guide to Better Vector Network Analyzer Calibrations for Probe-Tip</u> <u>Measurements</u>, Technical Brief, Cascade Microtech, 1994.
- [A62] J.V. Butler, D.K. Rytting, M.F. Isakander, R.D. Pollard and M. Vanden Bossche, "16-term error-model and calibration procedure 16-term error-model and calibration procedure for on-wafer network analysis measurements," IEEE Trans. Microwave Theory and Tech., vol. 39, pp. 2211-2217, Dec. 1991.
- [A63] S. Sercu and L. Martens, "Experimental Circuit Model Generation of Non-uniform Coupled Mutli-conductor Structures," IEEE 1997 MTT-S Digest, pp. 1781-1784, 1997.
- [A64] L. Martens and S. Sercu, "Parameter extraction for circuit models of electronic packages without optimization," IEEE Electrical Performance of Electronic Packaging, pp. 71-74, Oct. 1999.
- [A65] Avant!, Star-Hspice Manual, Release 2001. 2, pp. 18-27, 2001.
- [B1] P. Ferrari and G. Angenieux, "Calibration of a time-domain network analyzer: a new approach," IEEE Trans. Instrumentation and Measurement, vol. 49, pp.178-187, Feb. 2000.

- [B2] P.Ferrari and G. Angenieux, "simulation technique for the evaluation of random noise effects in Time-domain measurement systems." IEEE Trans. Instrum. Meas., vol. 50, No. 3, pp. 665-671, June 2001.
- [B3] T. Dhaene, L. Martens, and D. Zutter, "Calibration and normalization of time domain network analyzer measurements," IEEE Trans. Microwave Theory and Techniques, vol. 42, pp. 580-589, Apr. 1994.

[B4] Agilent PNA Series Microwave Network Analyzers Data Sheet, 2003.

- [B5] D.F. Williams, C.M. Wang, and U. Arz, "An optimal multiline TRL calibration algorithm," 2003 Int. Microwave Symp. Dig., pp. 1819-1822, June 10-12, 2003.
- [B6] W. Su and S.M. Riad, "Calibration of time domain network analyzers," IEEE Trans. instrumentation and Measurement, vol. 42, pp. 157-161, Apr. 1993.
- [B7] S. Dalmia, et al., "Design of inductors in organic substrates for 1-3GHz wireless applications," Proceedings of the International Microwave Symposium, May 2002.
- [B8] A.M. Niknejad and R.G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's," IEEE Journal on Solid-State Circuits, vol. 33, No. 10, pp. 1470-1481, Oct. 1998.
- [B9] J.M. Hobbs, et al., "Development and characterization of embedded thin-film capacitors for mixed signal applications on fully organic system-on-package technololgy," RAWCON, pp. 201-204, 2000.
- [C1] S. P. Thomson, *The life of Lord Kelvin*, Chelsea Pub. Co., London, 1976.
- [C2] L. Cohen, Heaviside's Electrical Circuit Theory, McGRAW-Hill Inc., New York, 1928.
- [C3] R. A. Chipman, Schaum's outline of Theory and Problems of Transmission Lines, McGraw-Hill Book Co., ch. 6, 1968.
- [C4] A. E. Kenelly, F. A. Laws and P. H. Pierce, "Experimental Researches on Skin Effect in Conductors," Transactions A. I. E. E., pp. 1971, 1915.
- [C5] H. A. Wheeler, "Formulas for the Skin Effect," Proc. IRE, vol. 30, pp. 412-424, Sep. 1942.
- [C6] R. Schinzinger and P. A. A. Raura, Conformal Mapping: Methods and Application, Elsevier Science Pub. B. V., 1991.
- [C7] Y. Eo and W. R. Eisenstadt, "High-speed VLSI interconnect modeling based on Sparameters measurement," IEEE Trans. Comp. Hybrids. Manuf. Techn., vol. 16, pp. 555-562, Aug. 1993.
- [C8] T. M. Winker, L. S. Dutta, and H. Grabinski, "An accurate determination of the characteristic impedance of lossy lines on chips based on high frequency S-

parameter measurements," IEEE Multi-Chip Module Conference, pp. 190-195, Feb. 1996.

- [C9] D. F. Williams, U. Arz, and H. Grabinski, "Accurate characteristic impedance measurement on silicon," IEEE MTT-Symposium Digest, pp. 1917-1920, 1998.
- [C10] D. F. Williams and B. K. Alpert, "Characteristic impedance of microstrip on silicon," 1999 Electrical Performance of Electrical Packaging, pp. 181-184, 1999.
- [C11] G. Carchon, W. De Raedt, and B. Nauwelaers, "Accurate transmission line characterization on high and low-resistivity substrates," IEEE 2001 MTT-Symposium, pp. 1539-1542, 2001.
- [C12] D. F. Williams, U. Arz, and H. Grabinski, "Characteristic-impedance measurement error on lossy substrates," IEEE Microwave and Wireless Components Lett., vol. 11, pp. 299-301, Jul. 2001.
- [C13] S. Vandengerghe, et al., "Characteristic impedance extraction using calibration comparison," IEEE Trans. Microwave Theory and Techniques, vol. 49, pp. 2573-2579, Dec. 2001.
- [C14] M. Lee and S. Nam, "An accurate broadband measurement of substrate dielectric constant," IEEE Microwave and Guided Wave Lett., vol. 6, pp. 168-170, Apr. 1996.
- [C15] Deutsch, A.; Scheuermann, M.R.; Arjavalingam, G.; Kneller, L.; Tam, J.K.; Surovic, C.W.; "Characterization of resistive transmission lines to 70 GHz with ultrafast optoelectronics," IEEE Microwave and Guided Wave Letters, Volume: 3 Issue: 3, Mar 1993, Page(s): 75 -77
- [C16] W. Kim, S. H. Lee, M. Swaminathan and R. Tummala, "Robust Extraction of the Frequency-Dependent Characteristic Impedance of Transmission Lines using One-Port TDR Measurements", 10th Topical Meeting on Electrical Performance of Electronic Packaging, Massachusetts, pp. 113-116, Oct. 2001.
- [C17] D.F. Williams, U.Arz, and H. Grabinski, "Accurate characteristic impedance measurement on silicon," in IEEE MTT-S Symp., pp. 1917-1920, June 1998.
- [C18] Avant!, Star-Hspice Manual, Release 2001. 2, pp. 18-27, 2001.
- [D1] W.R. Eisenstadt and Y. Eo, "S-Parameter-Based IC Interconnect Transmission Line Characterization," IEEE Trans. Components, Hybrids, and Manufacturing Tech., Vol. 15, pp. 483-490, Aug. 1992.
- [D2] D.F. Williams, U. Arz and H. Grabinski, "Accurate characteristic impedance measurement on silicon," IEEE MTT-S International Microwave Symposium Digest, pp. 1917-1920, Jun. 1998.
- [D3] Y. Eo and W. R. Eisenstadt and J. Shim, "S-Parameter-Measuremetn-Based High-Speed Signal Transient Characterization of VLSI Interconnects on SiO2-Si Substrate," IEEE Trans. Advanced Packaging, Vol. 23, No. 3, pp. 470-479, Aug. 2000.

- [D4] G. Carchon and B. Nauwelaers, "Accurate transmission line characterization on high and low-resistivity substrates," IEE Proceedings-Microwaves, Antennas and Propagation, vol. 148, pp. 285-290, Oct. 2001.
- [D5] M. Lee and S. Nam, "An accurate broadband measurement of substrate dielectric constant," IEEE Microwave and Guided Wave Lett., vol. 6, pp. 168-170, Apr. 1996.
- [D6] H. Hasegawa, M. Furukawa and H. Yanai, "Properties of Microstrip Line on Si-SiO2 System," IEEE Trans. Microwave Theory and Tech., vol. 19, pp. 869-881, Nov. 1971.
- [D7] R.A. Lawton and W.T. Anderson, "Two-layer dielectric microstrip line structure: SiO2 On Si and GaAs on Si: modeling and measurement," IEEE Trans. Microwave Theory and Tech., vol. 36, pp. 785-789, Apr. 1988.
- [D8] A. Weisshaar, H. Lan and A. Luoh, "Accurate closed-form expressions for the frequency-dependent line parameters of on-chip interconnects on lossy silicon substrate," IEEE Trans. Advanced Packaging, Vol. 25, pp. 288-296, May 2002.
- [D9] W. Kim, et al., "Electrical Design of Wafer Level Packaging on Board for Gigabit Data Transmission," Electronics Packaging Technology Conference, 2003.
- [D10] J. Mao, M. Swaminathan, J. Libous and D. O'Connor, "Effect of Substrate Resistivity on Switching Noise in On-chip Power Distribution Network," 2003 Electrical Performance of Electonic Packaging, Oct. 2003.
- [D11] B. Kleveland, et al., "Exploiting CMOS Reverse Interconnect Scaling in Multigigahertz Amplifier and Oscillator Design," IEEE Journal of Solid-State Circuits, Vol. 36, No. 10, pp. 1480-1488, Oct. 2001.
- [D12] R. D. Lutz, V. K. Tripathi and A. Weisshaar, "Enhanced Transmission Characteristics of On-Chip Interconnects with Orthogonal Gridded Shield," IEEE Trans. Advanced Packaging, Vol. 24, No. 3, pp. 288-293, Aug. 2001.
- [E1] W.J. Dally and J.W. Poulton, Digital Systems Engineering, Cambridge University Press: USA, 1998.
- [E2] S. Sercu and L. Martens, "Experimental Circuit Model Generation of Non-uniform Coupled Mutli-conductor Structures," IEEE 1997 MTT-S Digest, pp. 1781-1784, 1997.
- [E3] T. Neu, "Designing controlled-impedance vias," EDN magazine *designfreature* (EDN.com), October 2003, pp. 67-72.
- [E4] L. Tsang and D. Miller, "Coupling of Vias in Electronic Packaging and Printed Circuit Board Structures with Finite Ground Plane," IEEE Trans. Advanced Packaging, Vol. 26, No. 4, pp. 375-384, Nov. 2003.
- [F1] G.A. Rinne and P.D. Rranzon, "The Parasitic Reactances of Flip Chip Solder Bumps," Unitive case studies, Unitive Inc.

- [F2] Bagatin and Eric, <u>Electrical Principles of Microelectronics Packaging</u>, Raychm Corporation, San Jose, CA, 1988, pp. 121.
- [F3] L.C. Shen and J.A. Kong, <u>Applied Electromagnetism</u>, Thrid Edition, PWS Publisking Company: Boston, 1995.
- [F4] M. Lee and S. Nam, "An accurate broadband measurement of substrate dielectric constant," IEEE Microwave and Guided Wave Lett., vol. 6, pp. 168-170, Apr. 1996.
- [F5] D.F. Williams, U.Arz, and H. Grabinski, "Accurate characteristic impedance measurement on silicon," in IEEE MTT-S Symp., pp. 1917-1920, June 1998.
- [F6] Ansoft Corp., HFSS, <u>http://www.ansoft.com</u>.
- [F7] T.K.Sakar, Z.A. Maricevic J., B. Zhang, A. R. Djordjevic, "Evaluation of Excessive Inductance and Capacitance Of Microstrip Junction," IEEE Trans. Microwave Theory and Tech., vol. 42, pp. 1095-1097, June 1994.
- [F8] P.L. Werner and R. Mittra, "A new technique for the Extraction of SPICE-type Equivalent Circuits from Measured or Computed S-Parameters of Microstrip Components and Discontinuities," IEEE 6th Electrical Performance of Electronic Packaging, pp. 70-73, Oct. 1997.
- [F9] J.-M. Jong and V.K. Tripathi, "Time-Domain Characterization of Interconnect Discontinuities in High-Speed Circuits," IEEE Trans. Advanced Packaging, vol. 15, pp. 497-504, Aug. 1992.

Publications (2000-) at Gatech

- [1] <u>Woopoung Kim</u>, M. Swaminathan and Y.L.Li,"Extraction of frequency-dependent characteristic impedance of transmission lines using TDR measurements",
- 3<sup>rd</sup> Electronics Packaging Technology Conference 2000, pp.191-197, Dec. 2000.

[2] S. Dalmia, W. Kim, S. Min, M. Swaminathan, V. Sundaram, F. Liu, G. White

- and R. Tummala,"Design and Analysis of High Q-Inductors for MCM-L Technology", *Proceedings of the International Microwave Symposium*, Phoenix, Arizona, May 2001.
- [3] M. Swaminathan, <u>W. Kim</u> and I. Novak, "Measurement Problems in High-Speed Networks", *Proceedings of the IEEE Instrumentation and Measurement Technology Conference*, State of the Art Lecture, pp. 1339 - 1346, Budapest, Hungary, May 2001.
- [4] <u>W. Kim</u>, S. Dalmia and M. Swaminathan, "Extraction of Frequency-Dependent Properties of Embedded Inductors Using TDR Measurements", *Proceedings of the* 5th IEEE Workshop on Signal Propagation on Interconnects, Cavallino – Venice, Italy, May 2001.
- [5] S. Chun, J. Choi, S. Dalmia, <u>W. Kim</u> and M. Swaminathan, "Capturing Via Effects in Simultaneous Switching Noise Simulation", *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, pp. 1221-1226, Montreal, Canada, Aug. 2001.
- [6] <u>W. Kim</u>, S. H. Lee, M. Swaminathan and R. Tummala, "Robust Extraction of the Frequency-Dependent Characteristic Impedance of Transmission Lines using One-Port TDR Measurements", 10th Topical Meeting on Electrical Performance of Electronic Packaging, Massachusetts, pp. 113-116, Oct. 2001.
- [7] S. Min, S. Lee, <u>W. Kim</u>, S. Dalmia and M. Swaminathan, "Design, fabrication, measurements, and modeling of embedded inductors in laminated technology", *Proceedings of the InterPACK 2001*, Kauai, Hawaii, July 2001.
- [8] J. H. Kim, et al, "Electromagnetic modeling and hardware measurements of simultaneous switching noise in high speed systems", *Proceedings of the International Symposium on Electromagnetic Compatibility*, Vo1. 2, May 2002.
- [9] <u>W. Kim</u> and M. Swaminathan, "Validity of non-physical RLGC models for simulating lossy transmission lines", *Proceedings of the Interantional Symposium on Antenna and Propagation Society*, Vol.3, May 2002.
- [10] <u>W. Kim</u>, S. H. Lee, M. Swaminathan and R. R. Tummala, "Simulation of eyediagrams on lossy transmission lines using extracted data from 1-port TDR measurements", *Proceedings of the 6<sup>th</sup> IEEE Workshop on Signal Propagation on Interconnects*, May 2002.

- [11] <u>W. Kim</u>, S. H. Lee, M. Swaminathan and R. R. Tummala, "Determination of propagation constants of transmission lines using 1-port TDR measurements", 59<sup>th</sup> *ARFTG conference*, June 2002.
- [12] S.H. Lee, et al," High performance spiral inductors embedded on organic substrates for SOP applications", Microwave Symposium Digest, 2002 IEEE MTT-S International, Volume: 3, Page(s): 2229 -2232, June 2002.
- [13] S. Dalmia, et al, "Design of inductors in organic substrates for 1-3GHz wireless applications", *Proceedings of the International Microwave Symposium*, May 2002.
- [14] J. M. Hobbs, et al, "Development and characterization of embedded thin-film capacitors for mixed signal applications on fully organic system-on-package technology", 2002 IEEE Radio and Wireless Conference (RAWCON), Aug. 2002.
- [15] <u>Woopoung Kim</u>, Sung-Hwan Min, Suna Choi, and Madhavan Swaminathan, "Measurement-based Modeling and Test Methodology for Integrated Substrates", 60<sup>th</sup> ARFTG conference, Dec. 2002
- [16] <u>Woopoung Kim</u> and Madhavan Swaminathan, "Simulation of lossy package transmission Lines Using Extracted Data from One-port TDR Measurements," *Submitted to IEEE Trans. Adavanced Packaging.*
- [17] R. Doraiswami, et al., "Advances in Fine Pitch Lead Free Assembly Process," IEEE 53th Electronics and Component Technology Conference, pp. 834-839, 2003.
- [18] <u>Woopoung Kim</u> and et al., "Electrical Design of Wafer Level Package on Board for Gigabit Data Transmission," 5<sup>th</sup> Electronics Packaging Technology Conference, 2003.
- [19] J. Mao, et al., "Electromagnetic Modeling of Switching Noise in On-chip Power Distribution Networks," 8<sup>th</sup> International Conference and Workshop on Electromagnetic Interference and Compatibility, Dec. 2003.

[20] <u>Woopoung Kim</u>, R. Madhavan, and M. Swaminathan, "Interconnects Modeling and Design for high speed information and communication," *Invited to PIERS2004 in Pisa, Italy, Mar. 2004.* 

[21] <u>Woopoung Kim</u>, et al., "Effect of Wafer Level Packaging, Silicon Substrate and Board Material on Gigabit Board-Silicon-Board Data Transmission," 54<sup>th</sup> Electronic Components and Technology Conference, pp. 150-159, Dec. 2003.

Publications (1998 - 2000) at KAIST

[1] Woonghwan Ryu, Myung-Jin Yim, Seungyoung Ahn, Junho Lee, <u>Woopoung Kim</u>, Kyung-Wook Paik, and Joungho Kim, " High-Frequency SPICE Model of Anisotropic Conductive Film Flip-Chip Interconnections Based on a Genetic Algorithm ", IEEE Transactions on Advanced Packaging, Vol. 23, No. 3, September 2000, p542-545

- [2] Jongjoo Lee, Heeseok Lee, <u>Woopoung Kim</u>, Jaehoon Lee, and Joungho Kim, "Suppression of Coupled-Slotline Mode on CPW Using Air-Bridges Measured by Picosecond Photoconductive Sampling," IEEE Microwave and Guided Wave Letters, Vol. 9, No. 7, July 1999, pp. 265~267
- [3] <u>Woopoung Kim</u>, "Waveform Reconstruction of Photoconductive Switch using Minimum Phase Retrieval Algorithm," Appl. Phys. Lett., vol. 73, No.1, p7, 1998

[Conference]

- [1] <u>Woopoung Kim</u>, Jongjoo Lee and Joungho Kim, "Photoconductive Sampling Using Phase RetrievalAlgorithm," International Topical Workshop on Contemporary Photonics Technologies, 1998, January, Tokyo, Japan, p233.
- [2] Heeseok Lee, Jongjoo Lee, <u>Woopoung Kim</u>, Jaehoon Lee and Joungho Kim, "Farfield Pattern of Photoconductive Dipole Antenna using Finite-Difference Time-Domain Method," 5th International Workshop on Femtosecond Technology, 1998, February, Tsukuba, Japan, p129.
- [3] <u>Woopoung Kim</u>, Heeseok Lee and Joungho Kim, "In-situ Retrieval and Display of Femtosecond Optical Pulses and Picosecond Electrical Pulses," Ultrafast Phenomena Conference, 1998, July, Germany, p72-73.
- [4] Jaehoon Lee, Heeseok Lee, <u>Woopoung Kim</u>, Jongjoo Lee and Joungho Kim, "Characterization of > 100 GHz Devices Using Photoconductive Pump and Probe Measurement," IEEE Lasers and Electro-Optic Society 1998 Annual Meeting, Orlando, December, 1998, p225-226.
- [5] Heeseok Lee, Jongjoo Lee, <u>Woopong Kim</u>, Jaehoon Lee and Joungho Kim, " Design of Optimum Terahertz Transient Response using Finite-difference Time-Domain (FDTD) Method," IEEE Lasers and Electro-Optic Society 1998 Annual Meeting, Orlando, December, 1998. p221-222.
- [6] Jaehoon Lee, Heeseok Lee, <u>Woopoung Kim</u>, Jongjoo Lee and Joungho Kim, " > 100 GHz Time Domain Measurement Using photoconductive Sampling," accepted to The Sixth IEEE International Conference on Terahertz Electronics, United Kingdom, September, 1998, p204- 207.
- [7] Heeseok Lee, <u>Woopoung Kim</u>, Jongjoo Lee, Jaeyoung Ryu, and Joungho Kim, "Picosecond Pulse Scattering of Highly-Polarized Electromagnetic Wave Measured by Photoconductive Sampling," CLEO/Pacific Rim '99, August 1999, p793-794, Seoul, Korea.
- [8] <u>Woopoung Kim</u>, Jaeyoung Ryu, Heeseok Lee, and Joungho Kim, " A Novel Time Domain Picosecond Sampling System for Non-contact Characterization of Liquids, Semiconductors, and Metals," CLEO/Pacific Rim '99, August 1999, p791-792, Seoul, Korea.
- [9] Heeseok Lee, Jongjoo Lee, <u>Woopoung Kim</u>, Jaeyoung Ryu and Joungho Kim, "Picosecond Time-Domain Characterization of Millimeter-Wave Antenna Using Fiber-Coupled Photoconductive Probe Antenna," '99 Korea-China Joint Symposium on Semiconductor Physics and device Applications, Sept.13, 1999. Daeduk, Korea.

p57-59.

- [10] Seungyoung Ahn, Woonghwan Ryu, Myung-Jin Yim, Junho Lee, Young-Doo Jeon, <u>Woopoung Kim</u>, Kyung-Wook Paik, and Joungho Kim, "Over 10GHz Equivalent Circuit Model of ACF Flip-chip Interconnect using Ni-filled Ball and Au-coated polymer balls," Proceedings of 24 th IEEE/CPMT International Electronics Manufacturing Technology Symposium, Austin Convention Center, Austin, USA, pp. 421-425, Oct. 1999.
- [11] Joungho Kim, Jongjoo Lee, Heeseok Lee, <u>Woopoung Kim</u> and Jaeyoung Ryu, "Picosecond Time-Domain Photoconductive Sampling Method For Measuring Guided and Free-Space Pulse Propagation," 8 th Topical Meeting on Electrical Performance of Electronic Packaging, October, 1999, San Diego, CA.
- [12] H.Lee, J.Ryu, W.Kim, Joungho.Kim, "Verification of Picosecond Sampling for Electromagnetic Transient Scattering Experiment in Terahertz Spectrum Region," 7 th IEEE International Conference on Terahertz Electronics, Nov. 1999, p272-275, Nara, Japan.
- [13] J.Ryu, W.Kim, H.Lee, Joungho Kim, "Compact Terahertz Imaging System Using Near-Field Probe," 7 th IEEE International Conference on Terahertz Electronics, Nov. 1999, p81-84, Nara, Japan.
- [14] Seungyoung Ahn, Woonghwan Ryu, Myung-Jin Yim, Junho Lee, Young-Doo Jeon, Woopoung Kim, Kyung-Wook Paik, and Joungho Kim, "Comparison of Ni-filled Balls and Au-coated Polymer Balls in High-Frequency Application of ACF Flip-Chip Joint", APACK99, Symposium on Advances in packaging), p353-356, Singapore, Dec. 1999.

## Awards & Patents

- [1] S. Dalmia, S. HwanMin, <u>W. Kim</u> and M. Swaminathan, ``High Q Inductors in MCML Technology", Invention Disclosure # 2409, Date: Dec. 13, 2000.
- [2] <u>W. Kim</u>, S. H. Lee and M. Swaminathan, "Robust Extraction of the Frequency-Dependent Characteristic Impedance of Transmission Lines Using One Port TDR Measurements", Invention Disclosure # 2518, Date: July 17, 2001.

## VITA

## **Personal Details**

Name: Address: E-mail: Nationality: Marital Status: Sex:	Woopoung Kim 20435 Via Paviso, Apt: # F21 Cupertino, CA 95014 <u>yousu@ieee.org</u> South Korea Single Male
Education 2000-present	<ul> <li>Georgia Institute of Technology, Atlanta, Georgia USA</li> <li>Ph.D. in School of Electrical Engineering</li> <li>Concentrations: Applied Electromagnetism, High-speed system design</li> <li>Advisor: Dr. Madhavan Swaminathan</li> </ul>
1999	<ul> <li>Korea Advanced Institute of Science and Tech., Taejon, South Korea</li> <li>Ph.D. course in Electrical Engineering</li> <li>♦ Concentrations: Applied Electromag., THz short pulse phenomena</li> <li>♦ Advisor: Dr. Joungho Kim</li> </ul>
1997-1999	<ul> <li>Korea Advanced Institute of Science and Tech., Taejon, South Korea M.S. in Electrical Engineering</li> <li>Concentrations: Applied Electromag., THz short pulse phenomena</li> <li>Thesis: Time domain picosecond pulse sampling system for non-contact characterization of liquids, semiconductors, and metals</li> <li>Advisor: Dr. Joungho Kim</li> </ul>
1990-1997	<ul> <li>Korea Advanced Institute of Science and Tech., Taejon, South Korea</li> <li>B.S. in Electrical Engineering</li> <li>Concentrations: Electromagnetism, circuits, VLSI</li> <li>Military Service, South Korea (1991-1993)</li> </ul>