Physical Design of Optoelectronic System-on-a-Chip/Package Using Electrical and Optical Interconnects: CAD Tools and Algorithms

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Physical Design of Optoelectronic System-on-a-Chip/Package Using Electrical and Optical Interconnects: CAD Tools and Algorithms

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Dedicated to

my father, Sun-Kyu Seo, my mother, In-Hee Song,

my sister, Min-Jung Seo, my brother-in-law, Doo-Hyun Kim, my nephew, Yun-Geun Kim,

my brother, Chung-Hyeon Seo, my sister-in-law, Young Ra,

my wife, Jiwon Park

and

my son, Jonathan H. Seo

for their love, encouragement and belief.

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ABBREVIATIONS

CAD	Computer-Aided Design, xii
MCNC	Microelectronics Center of North Carolina, xvii
GSRC	Gigascale Systems Research Center, xvii
SoC	System-on-a-Chip, 3
SoP	System-on-a-Package, 3
NP	Nondeterministic Polynomial, 4
VLSI	Very Large Scale Integration, 6
VCSEL	Vertical Cavity Surface-Emitting Laser, 7
MOSIS	Metal Oxide Semiconductor Implementation System, 7
FSIM	Free-Space Interconnected Module, 8
I/O	Input and Output, 8
MCM	Multi-Chip Module, 8
FSOI	Free-Space Optical Interconnect, 8
SIA	Semiconductor Industry Association, 9
BCB	Benzocyclobutene, 11
DSM	Deep-Sub Micron, 15
CMOS	Complementary Metal Oxide Semiconductor, 20
TE	Transverse Electric, 61
MOCS	Method of Optical Centroid Searching, 62
ITRS	International Technology Roadmap for Semiconductors, 80
EDA	Electronic Design Automation, 81
EMI	Electromagnetic Interference, 81

SUMMARY

Current electrical systems are faced with the limitation in performance by the electrical interconnect technology determining overall processing speed. In addition, the electrical interconnects containing many long distance interconnects require high power to drive. One of the best ways to overcome these bottlenecks is through the use of optical interconnect to limit interconnect latency and power.

This research explores new computer-aided design (CAD) algorithms for developing optoelectronic systems. These algorithms focus on place and route problems using optical interconnections covering system-on-a-chip design as well as system-on-a-package design. In order to design optoelectronic systems, optical interconnection models are developed at first. The CAD algorithms include optical interconnection models and solve place and route problems for optoelectronic systems. The microelectronics center of north Carolina (MCNC) and gigascale systems research center (GSRC) benchmark circuits are used to evaluate these algorithms.

CHAPTER 1

INTRODUCTION

Current electrical systems are faced with the limitation in performance by the electrical interconnect technology determining overall processing speed. In addition, the electrical interconnects containing many long distance interconnects require high power to drive. One of the best ways to overcome these bottlenecks is through the use of optical interconnect to limit interconnect latency and power.

In 2000, D. A. B. Miller codified the physical advantages of optical interconnect over electrical interconnect [1]. Some possible practical advantages of optical interconnects are described in below.

Table 1. Possible practical advantages of optical interconnects

Advantage	Description
Design simplification	• No electromagnetic wave phenomena • No distance and frequency dependence
Architecture	• Large numbers of long high-speed connections • 2D interconnect architecture
Timing	• Predictable signal timing and no timing skew
Other physical advantage	• Power savings • High interconnect density

Because of the above advantages, optical interconnects could increase overall performance of electrical packages, and reduce the crosstalk, power consumption and signal latency. Due to the lack of computer-aided design (CAD) algorithms/tools in optics, it necessitates the development of new CAD algorithms/tools for emerging technologies such as optical interconnect.

1.1 Problem Statement

This dissertation explores four issues, which are module placement, electrical and optical interconnect modeling, interconnection routing, and optimization algorithm.

1.1.1 Module Placement

Module placement is a crucial step in physical design cycle because it determines the performance of chips, boards or packages. A good placement provides less area and increases the performance [2].

Module placement problem is generally related to routing problem. However, a poor placement cannot be improved by high quality routing. Therefore, placement phase is a very critical step in physical design cycle.

The objective of module placement problem is to construct a layout which provides the locations of all blocks, routes all nets and minimizes the total layout area if given size of each fixed blocks and netlists. The detailed objective for designing high performance systems is to minimize the total delay of the system by minimizing the total lengths of the

critical paths. It is usually performed by minimizing the length of the longest nets. This optimization is known as the *performance-driven placement optimization*.

1.1.2 Interconnect Modeling

In this dissertation, routing phase has to be able to deal with both electrical and optical interconnects. It leads to a new problem which is when, where and how to use optical interconnects as a replacement of electrical interconnects. In order to identify the problem, a comparison model which satisfies the system requirement is required.

For the optoelectronic system-on-a-chip, free-space optical interconnect technology is adopted. To design and analyze the system-on-a-chip (SoC) performance, two comparison models are made in terms of speed performance and energy cost.

Optical waveguide interconnect technology is used to design the optoelectronic system-on-a-package (SoP). To design and analyze the system-on-a-package performance, a comparison model for signal delay time is made and a bending loss model is also made for minimizing the signal power loss in optical waveguide at bends.

1.1.3 Interconnect Routing

After module placement phase, the exact location of module blocks and pins are determined. Using the region which is not occupied by the modules, nets are routed. This process is called *routing* [2].

The objective of the routing problem is to minimize the total interconnect length while using routing regions and completing all the interconnections. The interconnect routing should meet the timing budget of the systems.

Besides routing the interconnects among modules, special routing which is an optical clock routing is also explored in this dissertation.

1.1.4 Optimization Algorithm

The place and route problems are optimization problems as known as a nondeterministic-polynomial (NP) problem. It translates that the problems cannot be solved with deterministic algorithms in polynomial time. Therefore, heuristic algorithm such as simulated annealing or genetic algorithm is used for solving the NP problems.

The problems of heuristic algorithm are the performance vs. the optimization time. Due to heuristic approach, the algorithms often converge to a local minimum which is far from the optimum solution. In order to avoid it, a modified algorithm is usually used.

The optimization time is also becoming a critical issue because the problem size is getting bigger and bigger nowadays. To meeting time-to-market, design time should be minimized. In physical design process, all the stages, partitioning, floorplanning, placement, global routing, detailed routing, compaction and verification, are iteratively performed until meeting the required specification of the system. Thus, the optimization time should be minimized while remaining the optimization performance.

1.2 History of the problem

In this section, the origin and history of both optical interconnect technology and place and route problem are presented.

1.2.1 Optical Interconnection

C. Chappe first invented the optical telegraph in 1791. This served as the starting point for optical communication systems. The fusion of optics and atomic physics began with J. Fraunhofer in 1818. N. Niepce invented photography in 1826 and C. Wheatstone invented stereoscopy in 1832 respectively and they are the first products of imaging systems. In 1870, J. Tyndall demonstrated that light could be guided in a water jet [3]. However, the idea of a communication system based on the propagation of light through circular dielectric waveguides was considered from the mid-1960s, albeit some theoretical studies were performed in the early years of the present century [3], [4].

The first optical data storage and retrieval system has been developed by J. L. Baird in 1925. In 1928, N. Bohr presented the development of quantum mechanics and the principle of wave-particle duality of light and matter. R. K. Luneburg identified the final mathematical identification of optics with electromagnetics in 1944. In 1948, D. Gabor invented holography [3].

During 1960s, the semiconductor diode laser had been developed. This was the starting point that tried to use optics in digital computation and led to the rapid

development of optical communication systems. As the conclusion of the first demonstration, optical devices could not substitute for transistors in general computing machines because they consumed too much power [5]. However, the ideas of optics for communication were conceived at that time. From the mid 1970s to the late 1980s, the optical switching was paid attention because optical switch could be much faster than any electrical transistor [6]. This is still valid because nonlinear optics can make logic devices much faster than any electrical devices. In the early 1980s, quantum well structures were enhanced and this led to further interest in semiconductor optical switching devices.

In 1984, J. W. Goodman proposed ideas of optical interconnection of very large scale integration (VLSI) electronics [7]: index-guided, unfocused free-space and focused free-space optical interconnect. In index-guided optical interconnect, two types of waveguides, optical fibers and optical waveguides integrated on a suitable substrate, can be used. The two optical interconnect technologies provide a compact and planar packaging of the global optical clock distribution without diffractive components. In unfocused free-space optical interconnect, the optical signals carrying the clock signals broadcast to the entire electronic chip. Because detectors are located in the same distance at the focal point of the lens, there is no clock skew. A focused free-space optical clock distribution uses a holographic optical element. The holographic optical element acts as a complex grating. They were the actual start of the field of optical interconnects.

The quantum-confined Stark effect was discovered in III-V semiconductor quantum wells in 1984 [8]. This effect was important for optical computing and optical

interconnects because of the allowance of low energy devices, the possibility of 2D interconnected modulator or switch and the capability of large arrays of devices. The very important devices, vertical cavity surface-emitting lasers (VCSELs), were developed [9] and demonstrated [10] in the late 1980s. The first demonstration which VCSEL was electrically pumped was successfully made at room temperature. VCSELs became very interested practical devices, especially for low-cost optical fiber connections. Moreover, they become candidate devices for optical interconnects to silicon chips.

In 1988, B. D. Clymer and J. W. Goodman presented the skew properties of an array of optical transimpedence receivers associated with a hologram-based focused free-space optical clock distribution [11]. The test circuit used 3μm Metal Oxide Semiconductor Implementation System (MOSIS) technology with 18 optical receivers.

P. J. Delfyett, et al, introduced the mode-locked operation of a semiconductor laser system as a jitterless timing source [12]. They demonstrated the optical clock distribution of 1024 separate ports utilizing optical fibers. The total accumulated timing jitter was less than 12ps.

An optomechanical configuration has been conceived [13] that is far less complex than any current approach in 1994. Implementing a Fourier-plane-based interconnect with an arbitrary degree of space variance, it comprises only two component aggregates requiring mutual alignment in free space. Connections among such free-space interconnected modules (FSIMs) are effected over waveguide ribbons in a natural fashion obeying the principles of hierarchical interconnections: all signals leave chips on the

same physical transport medium, in this case through the optical array input and output (I/O) apertures to free-space modes. Use of a mechanically compliant medium (ribbons) decouples system scaling from free-space alignment requirements.

A prototype 3D optoelectronic neural network was implemented in 1994 [14]. It was composed of a 16-node input, 4-neuron hidden, and a single-neuron output layer. The prototype used high-speed optical interconnects for fan-out and mixed-signal VLSI circuits for fan-in. In 1997, S. P. Levitan, et al, developed "Chatoyant", a mixed-signal CAD tool for performing end-to-end system simulations of free space interconnection systems [15]. Chatoyant was able to analyze optical, electrical, and mechanical trade-offs. The prototype system for intra multi-chip module (MCM) interconnects was built in 1999 [16]. This system supported 48 independent free-space optical interconnect (FSOI) channels using 8 lasers and detectors. All chips were integrated on a ceramic substrate with three silicon chips.

A board-level free-space optical clock distribution system implemented with substrate mode hologram was presented by J. H. Yeh, et al in 1995 [17]. The system used an H-tree clock distribution to avoid clock skews. With 622MHz clock signal, 36ps of timing jitter and less than 10ps of clock skew were achieved.

In 1998, Y. Li, et al, reported board-level large bandwidth optical clock distributions with fanout of 128 on a printed circuit board using silica and polymer optical fibers [18]. The result showed the multi Gbps bandwidth capability.

A multi-GHz optical clock distribution on a Cray T-90 supercomputer multi-processor board is presented in 1999 [19]. The optical clock signal is distributed to 48 fanout points on $14.5\times27cm^2$ printed wiring board through a polyimide optical waveguide organized as an H-tree structure.

M. Forbes, et al, presented three different types of approaches for optoelectronic interconnects between VLSI chips [20]: fibre-ribbons, planar waveguides and free-space optics. This paper pointed out the limitations of electrical interconnect and the advantages of optical interconnect.

The 2002 Semiconductor Industry Association (SIA) roadmap update [21] shows the substantial problems of electrical interconnects on silicon chips. Off-chip long distance interconnections suffer in performance. It is proposed to replace such interconnections with optical interconnect to mitigate specific interconnect performance issues.

Optical connections between individual computer systems are now available. N. Savage anticipated that optical interconnection would be introduced in the computer to connect circuit boards within 2-5 years [22] and connect chips within 5-10 years. Optical interconnects will be feasible in 15 years for on-chip interconnects.

1.2.2 Place and Route

In this dissertation, the place and route problem is considered as a combined problem. This approach has been researched and has produced some useful results. In 1983, M.

Burstein and S. J. Hong presented a placement algorithm to interleave routing in a gate array system [23]. W. Dai and E. S. Kuh presented an algorithm for simultaneous floor planning and global routing for hierarchical building-block layout in 1987 [24]. P. R. Suaris and G. Kedem presented an algorithm for a quadrisection based combined place and route scheme for standard cell in 1989 [25]. In the same year, J. Cong presented an algorithm for pin assignment associated with global routing [26]. J. Rose developed a parallel global routing algorithm for standard cells which route multiple nets in parallel by relaxing data dependencies in 1990 [27].

In 1990, J. Garbers, *et al*, developed a hierarchical placement procedure based on routing and timing information [28]. This algorithm is based on min-cut method. After every cut which guides the subsequent cell partitioning, global routing and timing analysis is performed. In 1993, S. Sutanthavibul, E. Shargowitz and R. Lin presented an adaptive timing-driven placement for high performance VLSI chips [29]. J. Xu, P. Guo and C. Cheng presented an algorithm for cluster refinement for block placement in 1997 [30]. The algorithm is to minimize the chip size and interconnection wire length for mixed macro-cell and standard-cell. In 1997, C. J. Alpert, *et al*, revisited quadratic placement [31].

1.3 Key Contributions

The goal of this dissertation is to develop computer-aided design algorithms for optoelectronic systems utilizing optical interconnect technology. In order to achieve the

goal, the works are divided into four main parts, which are interconnection modeling, place and route, optical clock routing and adaptive optimization algorithm.

1.3.1 Interconnection Modeling

We have modeled two types of optical interconnects. Firstly, we modeled electrical interconnect and free-space optical interconnect in terms of speed performance and energy cost. Free-space optical interconnect uses VCSEL as an optical signal transmitter and shows the superiority to electrical interconnect. However, electrical interconnect is dominant if the interconnect length is less than 3cm from the energy cost point of view.

Secondly, we modeled optical waveguide interconnect in terms of power losses in optical waveguide at bends. The result of bending loss with specific fabrication parameters is curve-fitted with Boltzmann function to specify to our CAD tool. The parameters which are used in this dissertation are taken from a real fabrication parameter [32]. They are 1μm Benzocyclobutene (BCB) as a core layer, SiO_2 as a cladding layer, 1μm waveguide thickness and a wavelength of 1.3μm. The BCB index of refraction is 1.537 at a wavelength of 1.3μm and the SiO_2 index of refraction is 1.45 at a wavelength of 1.3μm [32]. The result is only for a single-mode operation. The analytical regression model for the bending loss of optical waveguide tells that the result is saturated over 240μm bending radius of optical waveguide. It translates that the bending loss is negligible over 240μm bending radius. For the simulations, the minimum bending radius of optical waveguide is assumed to be 100μm.

The signal propagation speed in optical waveguide interconnect is dominant over one in electrical interconnect once the interconnect length is over 2.4cm.

1.3.2 Place and Route

A new approach to designing high performance optoelectronic SoC utilizing free-space optical interconnect and SoP utilizing optical waveguide interconnect is developed.

The results for optoelectronic SoC show that more than 55% improvement in overall SoC speed and more than 11% saving in total energy consumption are obtained through the optimization process with the use of free-space optical interconnects. This translates to improve the overall SoC performance by a factor of over 1.5.

The result for optoelectronic SoP shows that more than 21% improvement in SoP performance is obtained through the use of optical waveguide interconnects.

1.3.3 Optical Clock Routing

Optical clock distribution network eliminates the disadvantages of electrical clock distribution such as clock skew, timing jitter, etc. Moreover, it allows no limitations on the maximum frequency of modulation of an optical signal.

We presented a new approach to optimized clock routing using optical waveguide. The results are very encouraging and show that less than 26.1psec in signal timing skew is obtained for a signal flight time of 614.38psec. This translates that the signal timing

skew can be neglected (< 4%). For optical power consumption, about 15% reduction is also obtained over clock nets routed with existing (optical) methods.

1.3.4 Hybrid Optimization

In this dissertation, two types of optimization algorithms were used for simultaneous place and route, which are a genetic algorithm and a simulated annealing to compare the performance of optimization due to the parameter size of optimization problem. As a result, a genetic algorithm is faster than simulated annealing even though the optimization performance of simulated annealing is slightly better than that of a genetic algorithm.

Therefore, in order to increase the optimization performance of a genetic algorithm, we applied two more different variations to a genetic algorithm. The first one is called "Steady-state genetic algorithm." It is basically producing better children in the next generation. Therefore, if the children are not better than their parents, the children should be then discarded in the next population.

The second one is called "Hybrid genetic algorithm." It adopted "Force-directed algorithm" to crossover function in a genetic algorithm. Force-directed algorithm models the input graph as a system of forces and tries to find a minimum energy configuration of this system. Even though this hybrid genetic algorithm is much faster than a generational genetic algorithm, however, it converges to a local minimum in some cases.

1.4 Summary of Dissertation

The next six chapters of this dissertation discuss the models for comparison of electrical and optical interconnects and the CAD algorithms to optimizing both module placement and routing of electrical and optical interconnects using the optical interconnect models. Chapter 2 presents comparison models between electrical and optical interconnects in terms of speed performance and energy cost. Using the comparison models, chapter 3 presents CAD algorithms to design optoelectronic system-on-a-chip utilizing free-space optical interconnects. Chapter 4 presents a power loss model for optical waveguide interconnect and a signal delay model for comparison between electrical and optical waveguide interconnects. Chapter 5 presents new CAD algorithms to design optical clock distribution network using optical waveguide interconnect technology. Chapter 6 presents CAD algorithms to design optoelectronic system-on-a-package using optical waveguide interconnect technology. The final chapter, Chapter 7, summarizes the results of this dissertation and discusses future work. The appendix provides the results of Chapter 6 with GSRC benchmark circuits.

CHAPTER 2

MODELING OF FREE-SPACE OPTICAL INTERCONNECT

2.1 Introduction

VLSI feature size scaling is now up to deep-sub micron (DSM). As the scaling technology has been developed, it has brought unexpected phenomena, such as intolerable wire resistance and capacitance, skin effect, ground bounce, etc. As a result, long electrical interconnects become the key issues for determining the performance of VLSI systems. In order to overcome these bottlenecks, a new technology has been sought for several decades and optical interconnect technology has been suggested as a substitution technology for long electrical interconnection.

However, optical interconnect technology has its own limitations, such as requirement of additional components, which are optical signal transmitter and receiver, signal transformation cost from electrical to optical and voltage incompatibility. Therefore, it is required that identifies the superiority between electrical and optical interconnects and determines which technology should use where.

There are lots of efforts that try to identify the superiority of optical interconnection as a substitution of electrical interconnection. In 1988, M. R. Feldman, *et al*, presented the comparison between optical and electrical interconnects based on power and speed consideration. G. I. Yayla, *et al*, reported a similar analysis, but expanded analysis in many ways about ten years later [34]. This chapter presents a comparison model between electrical and optical interconnects in terms of speed performance and energy cost using G. I. Yayla's circuit models.

2.2 Interconnect Models

Basically, both an electrical and an optical interconnects are composed of three main parts which are a transmitter, a signal transmission medium and a receiver. Figure 1 shows the off-chip electrical interconnection scheme with a fan-out of N. The model consists of a transmitter chip which is followed by a superbuffer, the off-chip conductor, the receiver chips along the conductor and a parallel termination resistor R_T.

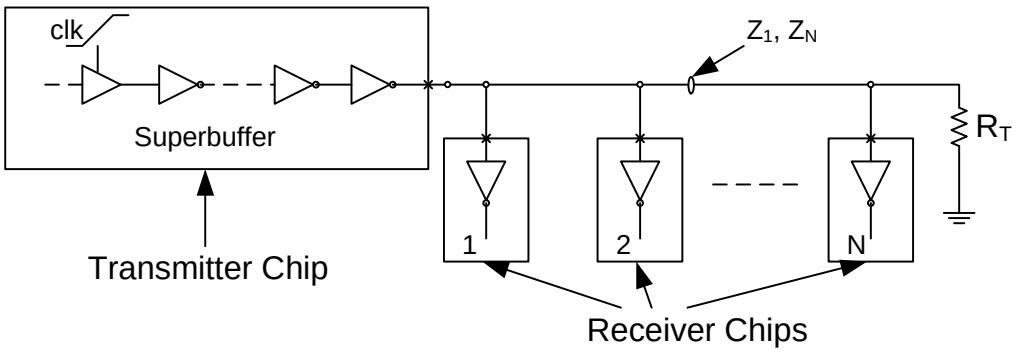


Figure 1. Model of off-chip electrical interconnection with fan-out

In this chapter, free-space optical interconnect technology is only considered. The optical signal is traveling through the air. It translates that only the optical signal transmitter and the optical signal receiver should be modeled because the refractive index in the air is almost 1.

The integration configuration for free-space optical substrate module is shown in Figure 2. On the silicon substrate, VCSEL and photodetector array is bonded based upon flip-chip technology. On the optical substrate, there is a microoptical substrate which carries focal-plane diffractive elements.

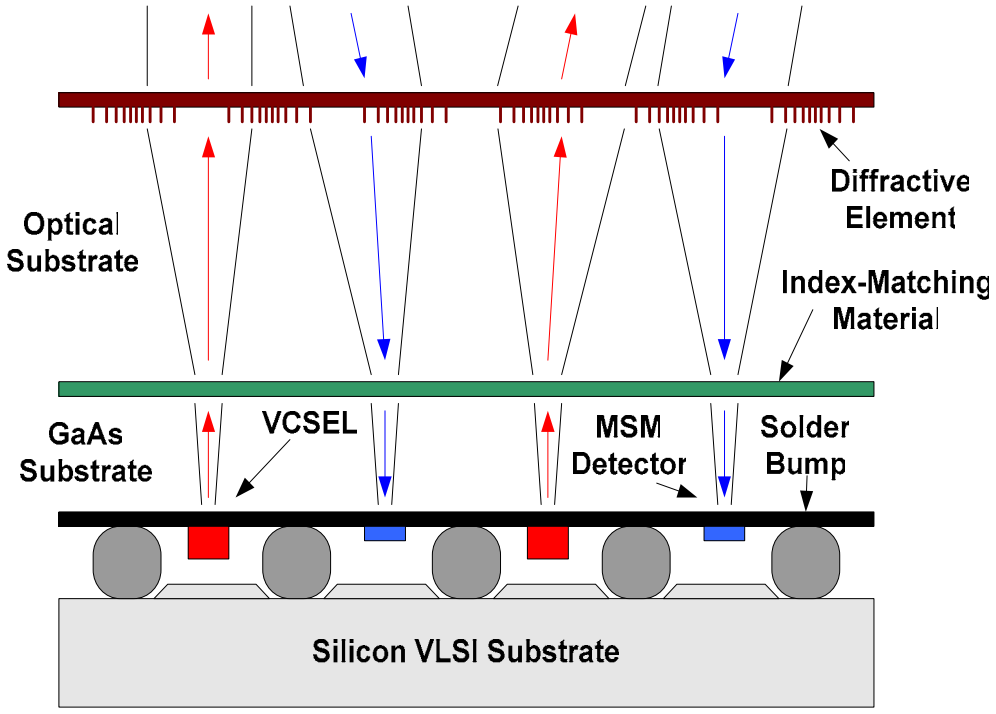


Figure 2. Integration configuration for free-space optical substrate module

In this research, VCSEL is considered as an optical signal transmitter. The optical signal transmitter model includes a transmitter, a transmitter driver and a superbuffer and is shown in Figure 3.

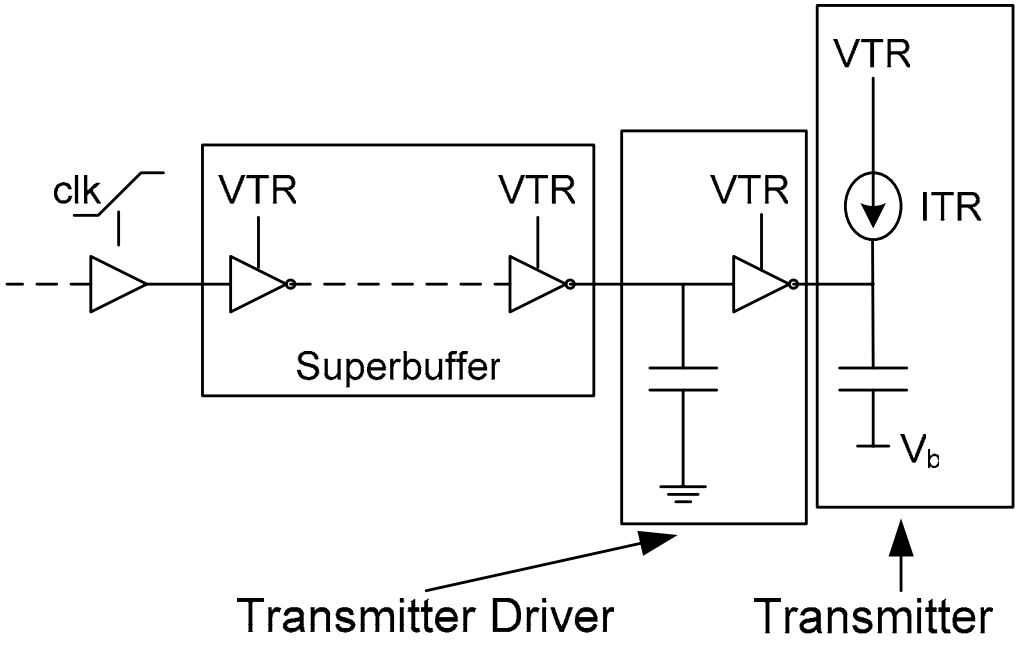


Figure 3. Model of an optical signal transmitter

Figure 4 shows the optical signal receiver model. The model consists of a photodiode, a thresholding current source, clamping diodes and an inverter. The clamping diodes limit the voltage swing and an inverter amplifies the photodiode output signal and restores the logic.

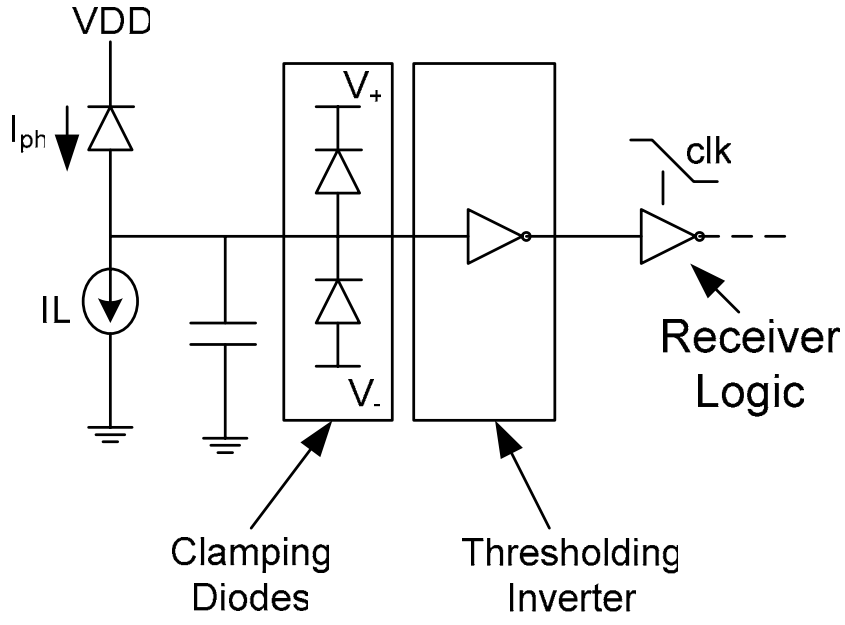


Figure 4. Model of an optical signal receiver

However, there are several assumptions to allow to use the above interconnect models.

- Interconnect length and fan-out are considered as independent variables.

- Large-scale digital computing systems using dense interconnections are only considered.
- Analog fan-in is not considered.
- Synchronous communication is assumed as the communication protocol.
- Static complementary metal oxide semiconductor (CMOS) logic design with rail-to-rail voltage swings is assumed.
- The scaling analysis of VLSI technology is not included, but 0.5 micron CMOS technology is used.
- Non-return to zero type of communication is assumed.
- A photodiode output voltage swing of 330mV is assumed, which is approximately equal to the transition width of a CMOS inverter transfer characteristic for 3.3V power supply voltage in 0.5μm CMOS.
- The interconnection conductor is assumed to be lossless.

2.3 Speed Performance Model

Using the above interconnect models, G. I. Yayla, *et al*, reported comparison results between electrical interconnect and free-space optical interconnect in 1998 from the speed performance and energy cost point of view. From the comparison results, the speed performance of both off-chip electrical interconnections and free-space optical interconnections are extracted and compared. Figure 5 shows interconnect length versus speed performance for electrical and optical interconnect obtained through regression

modeling using the exponential decay function, which produces exponential curve. The comparison models were obtained from G. I. Yayla's paper.

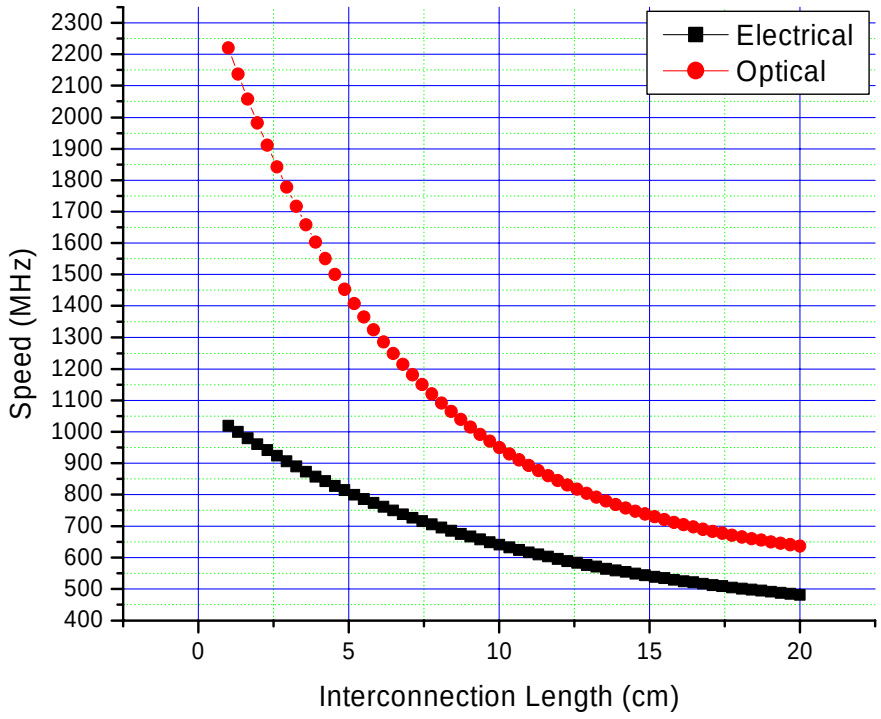


Figure 5. Regression models for speed performance

According to the above graph, optical interconnect is always dominant over electrical interconnect from the speed performance point of view.

The speed regression model is expressed by,

$$Speed = a + b \cdot e^{-x/c} \qquad (1)$$

The coefficients of the models are shown in Table 2.

Table 2. Coefficients for speed regression model

Coefficient / Interconnect	*a*	*b*	*c*
Optical	557.56	1952.58	6.23
Electrical	393.19	693.82	9.70

The CAD tool, which will be introduced in chapter 3, can accommodate any prescribed model for speed performance of electrical versus optical interconnect. Cases where optical sensor delays dominate the performance of optical interconnect can easily be accommodated into the proposed CAD framework.

2.4 Energy Cost Model

The original comparison data of the energy cost for both electrical and optical interconnects is obtained from G. I. Yayla's paper. The comparison data were curve-fitted by polynomial function, which produces cubic curve.

The results are shown in Figure 6.

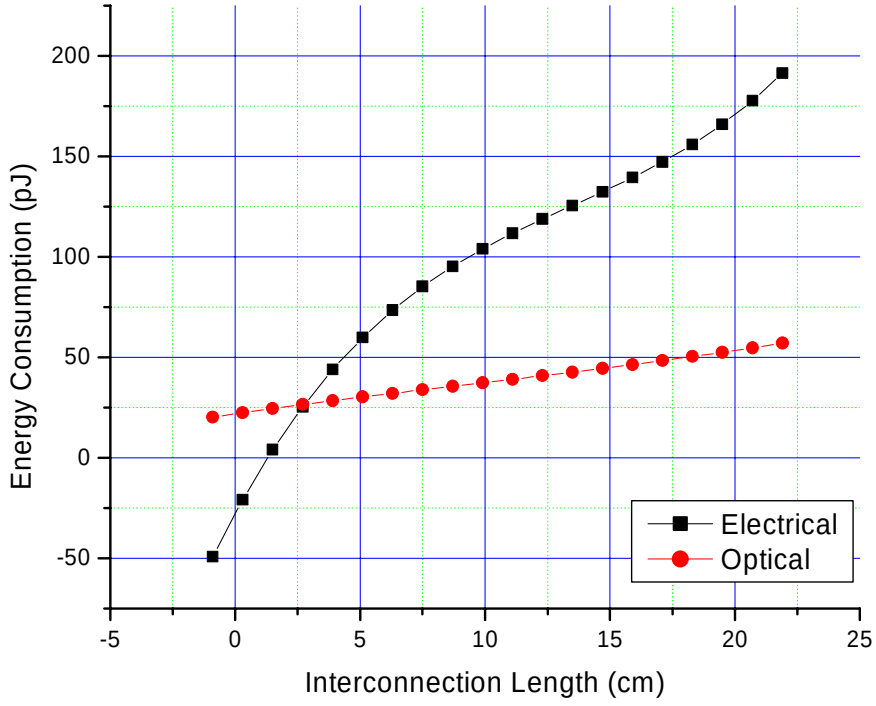


Figure 6. Regression models for energy consumption

Figure 6 reveals that optical interconnect is superior to electrical interconnect if interconnect length is longer than 3cm. Thus, the CAD algorithm does not replace electrical interconnect with optical interconnect if the interconnect length is shorter than 3cm.

The energy cost model can be written as,

$$Energy = a + bx + cx^2 + dx^3 \qquad (2)$$

The coefficients of the models are shown in Table 3.

Table 3. Coefficients for energy regression model

Coefficient / Interconnect	*a*	*b*	*c*	*d*
Optical	21.93	1.77	-0.03	0.001
Electrical	-27.56	22.84	-1.28	0.032

2.5 Summary

In this chapter, we have modeled electrical interconnect and free-space optical interconnect in terms of speed performance and energy cost. Free-space optical interconnect uses VCSEL as an optical signal transmitter and shows the superiority to electrical interconnect. However, electrical interconnect is dominant if the interconnect length is less than 3cm from the energy cost point of view.

Even though G. I. Yayla's models rather have several limitations and out-of date, but the models presents very broad comparison models between electrical and free-space optical interconnects.

In the next chapter, a new approach to designing optoelectronic system-on-a-chip using the speed performance and energy cost models will be presented.

CHAPTER 3

DESIGN OF SYSTEM-ON-A-CHIP USING FREE-SPACE OPTICAL INTERCONNECT

Flexible free-space optical interconnect architectures are currently being developed for low latency, low power, interconnection among on-chip, off-chip processor and memory elements to facilitate implementation of multi GHz clock multiprocessor. This requires replacing interconnects longer than a few *mm* with optical links based on Vertical Cavity Surface-Emitting Laser (VCSEL), resulting in minimized latency and reduced power and volume [13].

In this chapter, we propose a new gigascale optoelectronic system-on-a-chip architecture utilizing free-space optical interconnect technology and develop computer-aided design (CAD) algorithms to achieve maximal use of on-chip electrical and optical interconnect resources by optimal assignment of a subset of nets to free-space optical interconnections.

3.1 Introduction

At high speeds, electrical interconnections suffer from the problems of capacitive loading, mutual crosstalk, reflection, switching noise, clock skew, power consumption,

timing jitter, etc. In contrast, optical interconnections offer advantages such as high bandwidth, negligible mutual crosstalk, high speed, low power consumption, low timing jitter, etc. The use of optical interconnects is expected to increase packaging densities, interconnection bandwidth and chip speeds, and reduce crosstalk, power and chip latency.

In 1984, J. W. Goodman proposed optical interconnection of very large scale integration (VLSI) electronics [7]: intra-chip data communications and inter-chip data communications. They were the actual start of the field of optical interconnects. A prototype 3D optoelectronic neural network was implemented in 1994 [14]. It was composed of a 16-node input, 4-neuron hidden, and a single-neuron output layer. The prototype used high-speed optical interconnects for fan-out and mixed-signal VLSI circuits for fan-in. In 1997, S. P. Levitan, et al, developed "Chatoyant", a mixed-signal CAD tool for performing end-to-end system simulations of free space interconnection systems [15]. Chatoyant was able to analyze optical, electrical, and mechanical trade-offs. The prototype system for intra MCM interconnects was built in 1999. This system supported 48 independent free-space optical interconnect (FSOI) channels using 8 lasers and detectors. All chips were integrated on a ceramic substrate with three silicon chips.

M. Forbes, et al, presented three different types of approaches for optoelectronic interconnects between VLSI chips [20]: fibre-ribbons, planar waveguides and free-space optics. This paper points out the limitations of electrical interconnect and the advantages of optical interconnect.

The 2002 Semiconductor Industry Association (SIA) roadmap update [21] shows the substantial problems associated with electrical interconnects on silicon chips. Off-chip long distance interconnections suffer in performance. It is proposed to replace such interconnections with optical interconnect to mitigate specific interconnect performance issues.

Optical connections between individual computer systems are now available. N. Savage anticipated that optical interconnection would be introduced in computers to connect circuit boards within 2-5 years [22] and connect chips within 5-10 years. Optical interconnects will be feasible in 15 years for on-chip interconnects.

In this chapter, we introduce GOETHE (Generic Opto-Electronic system design THEurgist), a CAD tool for physical placement and routing of interconnections in System-on-a-Chip (SoC) utilizing free-space optical interconnect technology.

GOETHE determines which of the interconnects are routed electrically and which are routed optically without exceeding the routing capacity of the optical interconnect while minimizing total electrical interconnect length. Free-space optical interconnect technology is suitable for routing on-chip interconnects using an optical interconnect layer [7]. Data throughput between modules could be enhanced through the use of free-space optical interconnect by a factor of a thousand [22].

This research discusses the design of the circuit on silicon substrate and its interaction with the optical substrate and the architecture of SoC interconnection with free-space optical substrate that is discussed in this chapter is shown in Figure 7.

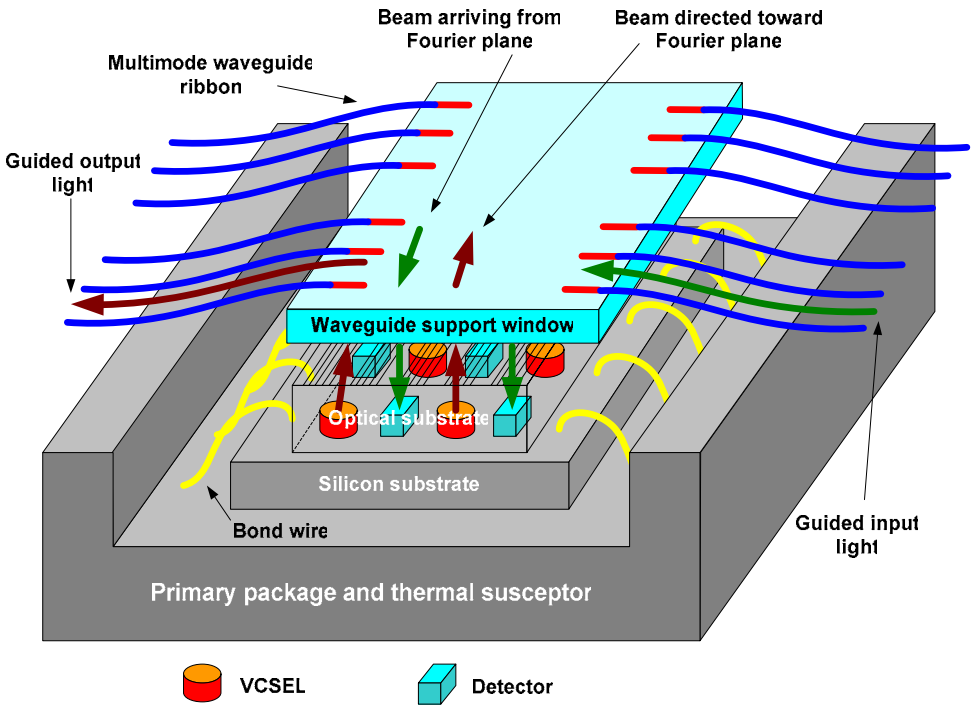
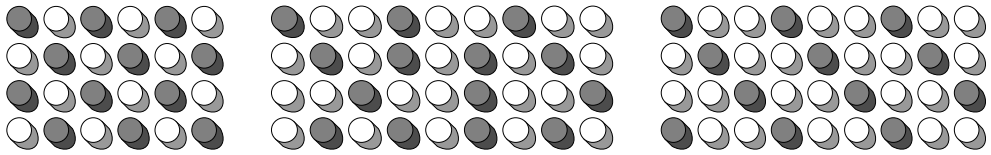


Figure 7. Optomechanical configuration in the neighborhood of the substrate.

3.2 Assumption

All module shapes are assumed to be rectangular-shaped. Pins are assigned into module periphery. A set of netlists are generated randomly for a specified number of modules. It is also assumed that the SoC operations are pipelined and that all module data transfers are buffered.

In this chapter, three arrangements of optical sensors are considered (see Figure 8). The gray circles represent transmitters and the white circles represent receivers.



(a) (b) (c)

Figure 8. Three different sensor arrangements

In the horizontal and vertical directions, the patterns of Figure 8 are repeated up to the size of a SoC. However, any regular sensor arrangements of transmitter-receiver configurations can be specified as an input to GOETHE. Therefore, it is possible to experiment with different sensor arrangements of transmitter-receiver configurations so that determines which gives the best performance.

3.3 Optimization Algorithms

The optimization goals are as follows:

- *Given*: The preliminary locations of all modules and netlists and the arrangements of optical sensors in the VCSEL array.
- *Determine*: The optimal placement of all modules.

- *Such that (optimization criteria)*: (a) total electrical interconnect length is minimized and (b) the utilization of the optical routing capacity is maximized.

The optimization algorithm consists of a *placement and routing* and a *module compaction* step. These are described in Section 3.3.1 and 3.3.3.

3.3.1 Placement and Routing

Genetic Algorithm is employed in order to optimize placement of modules and routing of electrical and optical interconnects simultaneously. There are three steps to find the best placement of modules which gives minimum routing cost.

First of all, *population* is generated as a group of many random orders of modules. The number of populations is one of the inputs to GOETHE. These orders are stored as a sequence of numbers. Second, two better groups which are called parents in the population and combine them to create two new solutions which are called children using *Crossover*. During crossover, a random point is picked in the parents' sequences and switched every number in the sequence after that point. When the placement of modules is changed, the sequence of the longest interconnects is also changed.

However, the crossover sometimes may not work because the population is represented by a sequence of numbers. An example is shown below [35].

Parent 1	1 2 3 4 5 **6 7 8 9**
Parent 2	8 7 6 3 2 **5 4 9 1**
Child 1	1 2 3 4 5 **5 4 9 1**
Child 2	8 7 6 3 2 **6 7 8 9**

Figure 9. An example that crossover operation does not work

To resolve this phenomenon, *partially matched crossover* is employed which is shown in Figure 10.

Parent 1	1 **2 3 4 5** 6 7 8 9
Parent 2	8 7 6 **3 2 5 4** 9 1
Child 1	1 **3 2 5 4** 6 9 8 7
Child 2	8 7 6 **2 3 4 5** 9 1

Figure 10. Partially matched crossover

Finally, modules are rotated to random orientation during *Mutation.*

The above operations may not reproduce good parents to better children. Therefore, if the children are not better than their parents, the children should be then discarded in the population. This decision is made by total routing cost (see Figure 14).

The algorithm attempts to replace long electrical interconnects with optical interconnects in the sequence of interconnect length. However, the breakpoint which electrical interconnect can be replaced with optical interconnect should be determined because electrical interconnects is still dominant over optical interconnects for very short distance interconnect (< 3cm). It is described in Chapter 2.

The following operations are the overall goals of the optimization.

- Maximization of the utilization of the optical routing capacity.
- Minimization of the length of the critical (longest) electrical interconnects.
- Minimization of the total electrical interconnect length.

If an input port of one module is to be routed to an output port of another module optically, then the input port and the output port must first be routed electrically to the nearest receiver and transmitter respectively. The cost of routings electrically from I/O ports to the sensors is included in the total cost of the electrical interconnect routing.

Figure 11 shows GOETHE layout after the optimization with 16 modules. The right window layout is an optimized layout of the one shown in the left window.

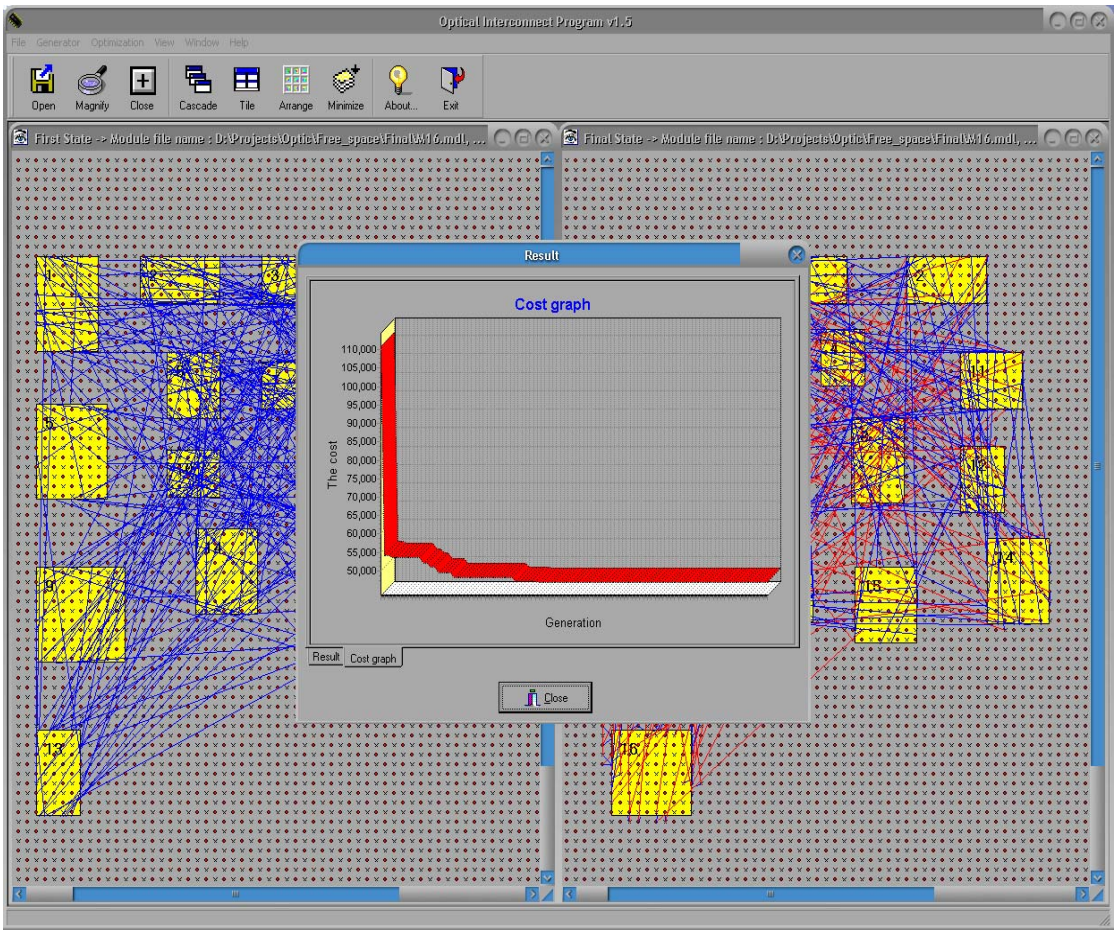


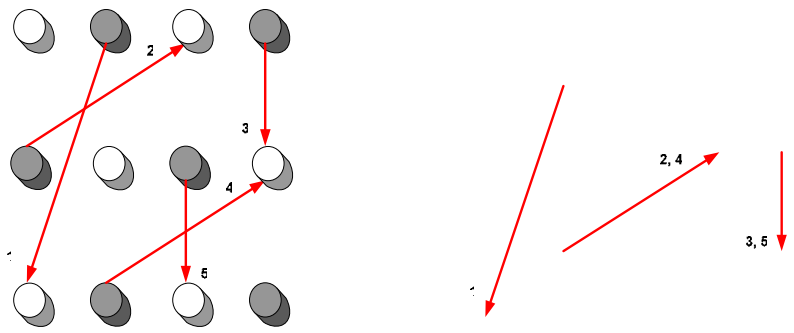
Figure 11. GOETHE layout with optimization

3.3.2 Optical Routing Capacity

The physical length of optical interconnect does not matter. This is different from electrical interconnects. The optical routing capacity is determined by the number of

optical directions in which signals have to be routed [13]. It turns out that due to the manner in which the diffraction grating of Figure 2 is fabricated, the optical routing capacity depends upon the number of optical directions rather than upon the number of physical routings of optical interconnects. Thereby, the number of optical directions that the optical substrate can support is one of the inputs to the optimization tool, GOETHE.

Figure 12(a) shows the physical routing of signals in the optical substrate. The gray circles represent transmitters and the white circles represent receivers. Figure 12(b) shows optical vectors that the routing configuration of Figure 12(a) reduces to. All parallel optical directions in Figure 12(a) trim down to a single optical vector in Figure 12(b).



(a) (b)

Figure 12. Optical vectors in Fourier plane

3.3.3 Module Compaction

The regions between modules are called *channels*. At the beginning of the optimization process, GOETHE places modules with distance of wiring capacity. Then, virtual vertical direction lines are placed in the channels. The number of horizontal electrical interconnects crossing the vertical direction line for each channel is calculated. From this calculation, a difference between the wiring capacity and the wiring density which we call *Ridge*, is formed. The *Compression-Ridge method* is applied to delete the Ridge region [2]. This method is consecutively introduced in the horizontal direction.

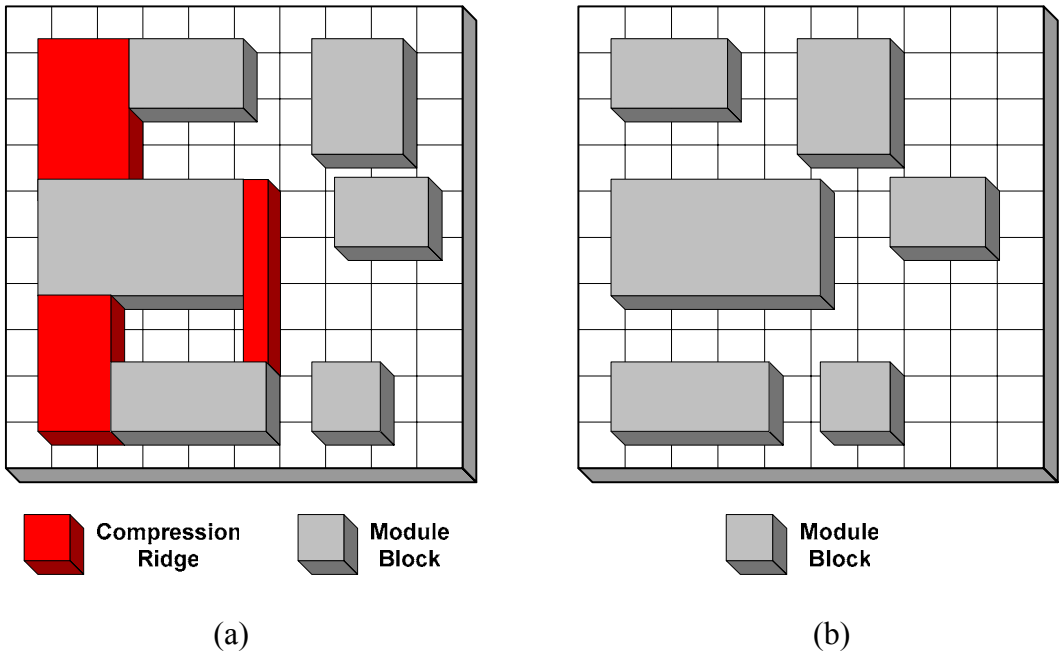


Figure 13. Compression-Ridge Method

3.3.4 Cost Function

The cost function for the optimization is described in Figure 14. It is composed of the electrical interconnect cost and the optical interconnect cost. The first term includes the electrical interconnect length due to all the electrical interconnect plus the interconnect length contributions due to the electrical interconnects to all transmitters and receivers which are occupied by optical interconnects. *Manhattan distance* is employed to calculate the electrical interconnect length.

$$Cost = \sum \left(Electrical\ interconnect\ length \right) + w\left(1 - \frac{v}{D} \right)$$

where
w = Weight factor for optical cost
v = The number of optical vectors in current layout
D = The maximum number of optical directions that the optical substrate can accommodate

Figure 14. The cost function

The second term represents the optical interconnect cost. It attempts to minimize the unutilization of the optical routing capacity – note that at each step of the algorithm the longest interconnects are replaced with optical interconnect. w is the weight factor for the optical cost and is set to be 100 in this research. It turns out that the optical cost is the percentage of the unutilization of the optical routing capacity.

3.3.5 Pseudo Code for Optimizer

The pseudo code for a genetic algorithm [37] with the objective of minimizing the total routing cost in a SoC is as follows:

Algorithm 3.1. Genetic Algorithm

```
1.  Generate modules and netlists;
2.  Generate population; // Section 3.3.1
3.  Set the generation number;
4.  for (each  generation) {
5.      Partially matched crossover; // Section 3.3.1 – Swap modules
6.      Module compaction; // Section 3.3.3 - Find the optimal module placement
7.      Mutation; // Section 3.3.1 - Rotate modules
8.      Module compaction; // Section 3.3.3 - Find the optimal module placement
9.      Evolution; // Section 3.3.4 - Optimize the total routing cost
10. }
11. Calculate speed improvement; // Section 2.3
12. Calculate energy saving; // Section 2.4
13. Save result files;
```

Figure 15. Pseudo code for genetic optimizer

During *evolution*, the algorithm makes total cost minimal.

3.4 Results and Analysis

In this section, we present experimental results of the optimization achieved by using GOETHE. All algorithms are implemented in C++.

3.4.1 A Simulation Result

As mentioned in Section 3.2, a set of netlists was generated randomly for a specified number of modules. For comparison of overall SoC performance, cases with 9, 16, 25, 36 and 49 modules were simulated and a case of 36 modules is shown in this section. For the all simulations, the dimension of SoCs is set to be $10 \times 10 cm^2$.

Figure 16 shows the graph for the cost reduction versus the number of generations of the genetic optimizer with 36 modules and 1000 netlists. In this simulation, the optical routing capacity was 300.

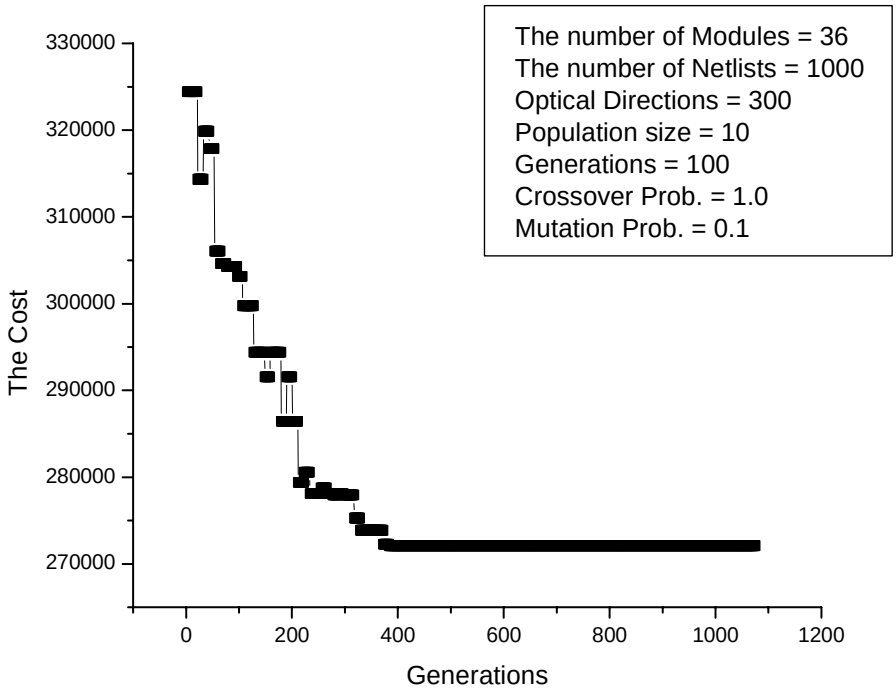


Figure 16. The cost graph

The result shows about 20% saving in the electrical cost which is given in Figure 14. About 99.7% of optical routing capacity is occupied.

Table 4 shows reductions in interconnect length for the different sensor distributions of Figure 8 with 36 modules and 1000 netlists. For the simulations, optical routing capacity was 500.

Table 4. Comparison with different sensor distributions

Arrangement	% of wires converted to optical links	% reduction in longest wire length	% reduction of total cost	No. of optical directions
(a)	50	60	69	495
(b)	48	52	65	475
(c)	43	47	62	428

Figure 17, Figure 18 and Figure 19 show an example of the optimization performed by GOETHE. The blue lines represent electrical interconnects and the red lines represent optical interconnects.

Figure 17 shows a layout and description of all the interconnects at the beginning of the optimization process.

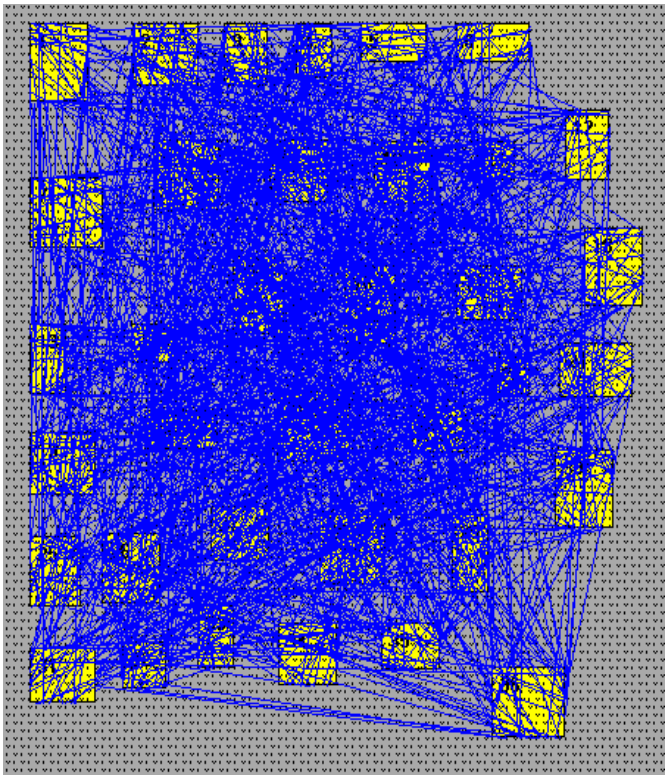


Figure 17. Placement and routing before optimization

Figure 18 shows only the optical interconnects at the end of the optimization.

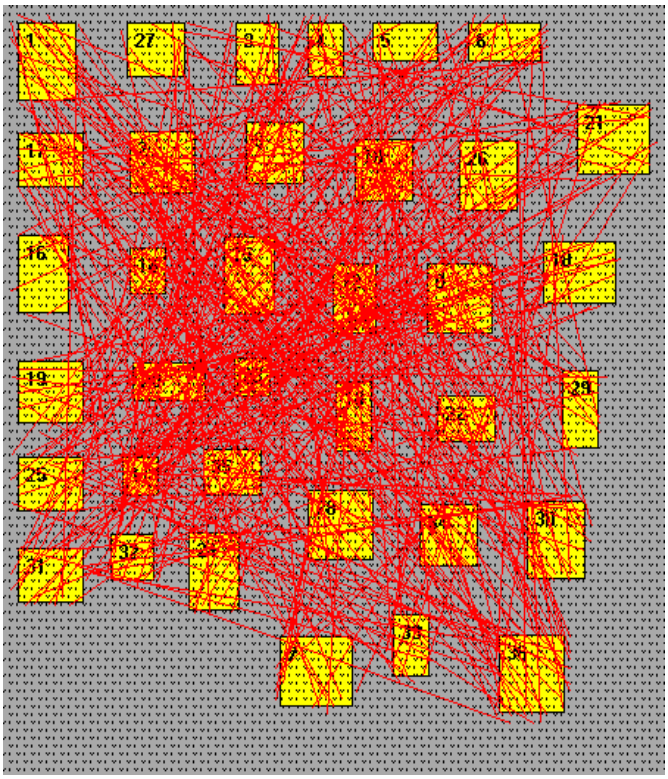


Figure 18. Optical routing after optimization

The electrical interconnects at the end of the optimization are shown in Figure 19.

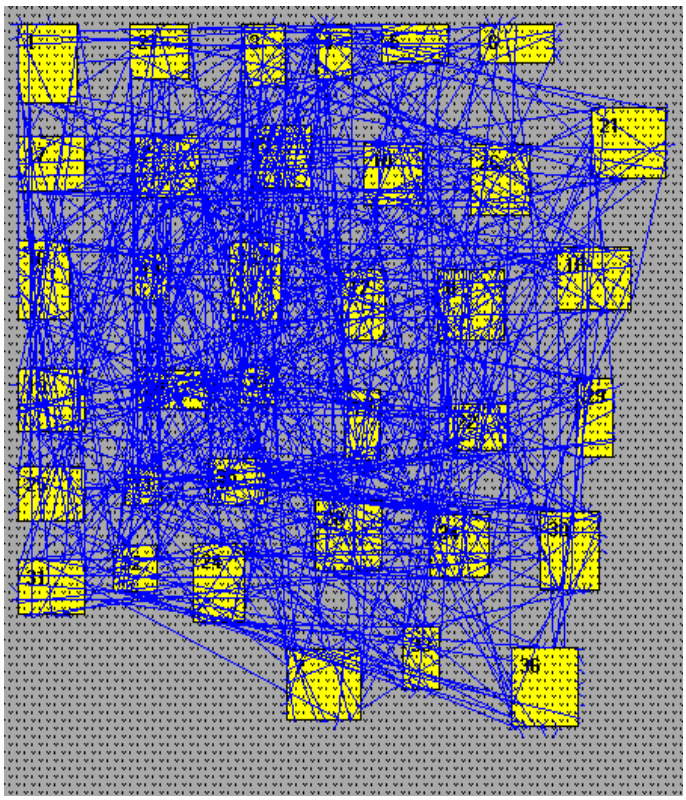


Figure 19. Electrical routing after optimization

3.4.2 Speed and Energy Issues

In this section, we evaluate the SoC speed improvement and energy saving with 9, 16, 25, 36 and 49 modules.

The graph for the percentage improvement of overall SoC speed vs. the number of optical vectors with various numbers of modules is shown in Figure 20.

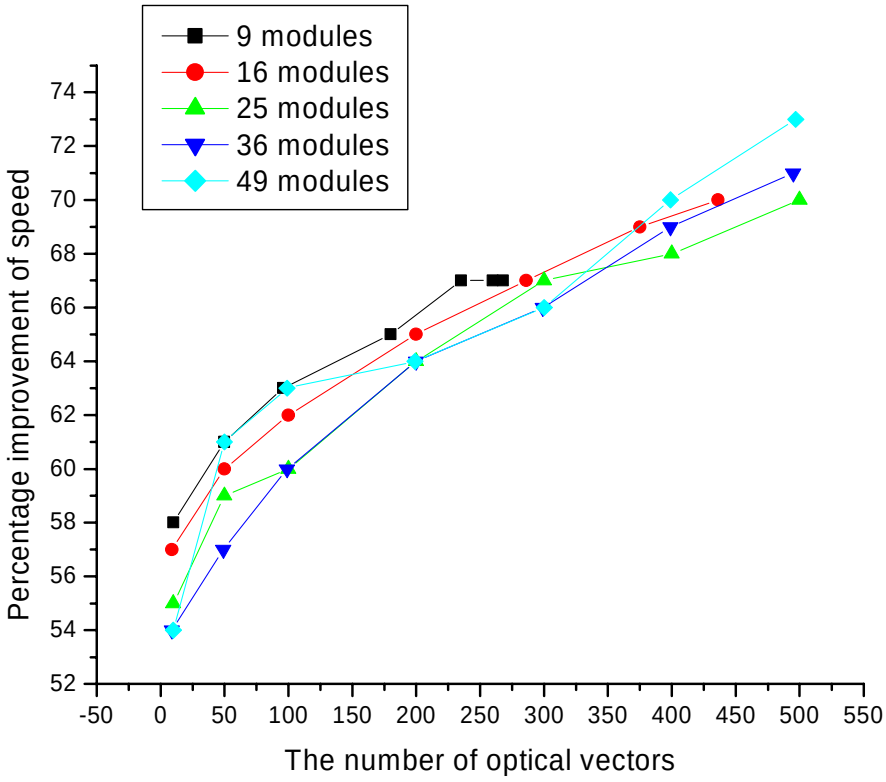


Figure 20. The graph for speed improvement vs. optical directions with various numbers of modules

The results are very encouraging and show that more than 54% improvement in chip speed can be obtained through the use of optical interconnects.

Figure 21 shows the graph for the percentage saving of energy consumption vs. the number of optical vectors with 9, 16, 25, 36 and 49 modules.

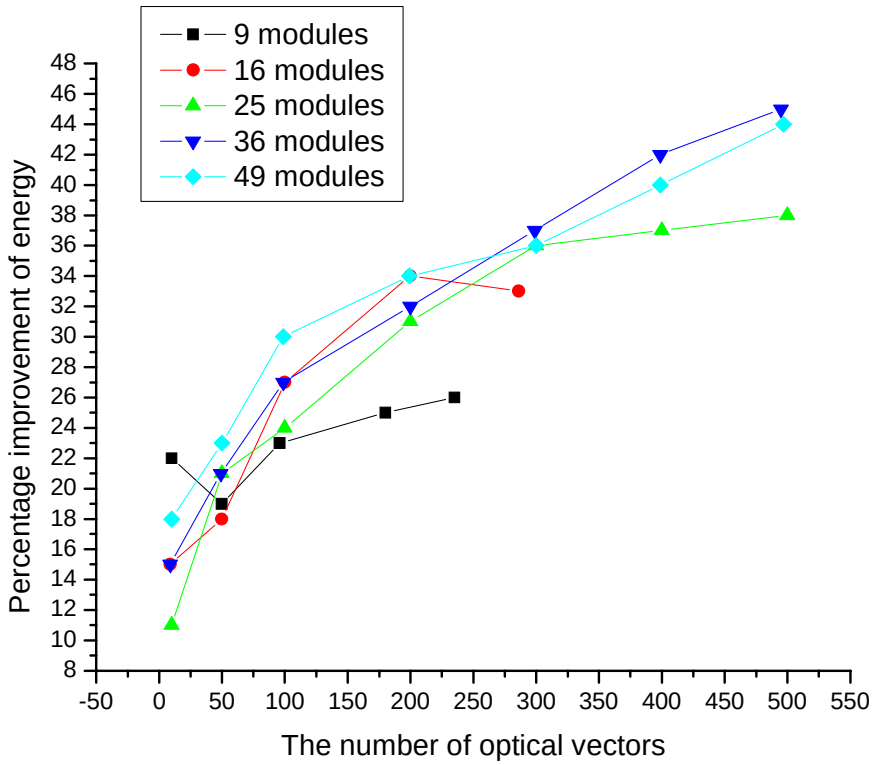


Figure 21. The graph for energy saving vs. optical directions with various numbers of modules

In cases of 9 and 16 modules, the best results are with 235 and 200 optical interconnects respectively.

Table 5 shows results for optimization performed with 9, 16, 25, 36 and 49 modules against different number of optical directions supported by optical substrate. The table

entries show the number of optimized optical vectors which must be less than the number of optical directions, the percentage saving in total energy consumption and the percentage improvement in overall SoC speed.

Table 5. The percentage improvement of energy consumption and speed with the different number of optical directions

No. of module \ Optical direction		10	50	100	200	300	400	500
9	Optical vector	10	50	96	180	235	260	268
	Energy (%)	22	19	23	25	26	20	15
	Speed (%)	58	61	63	65	67	67	67
16	Optical vector	9	50	100	200	286	375	436
	Energy (%)	15	18	27	34	33	31	26
	Speed (%)	57	60	62	65	67	69	70
25	Optical vector	9	49	100	199	300	396	489
	Energy (%)	11	21	24	31	36	37	38
	Speed (%)	55	59	60	64	67	68	70
36	Optical vector	9	49	99	200	299	399	495
	Energy (%)	15	21	27	32	37	42	45
	Speed (%)	54	57	60	64	66	69	71
49	Optical vector	10	50	99	199	300	399	497
	Energy (%)	18	23	30	34	36	40	44
	Speed (%)	54	61	63	64	66	70	73

3.5 Summary

In this research, a new approach to high performance SoC utilizing free-space optical interconnect was described. The results show that more than 55% improvement in overall SoC speed and more than 11% saving in total energy consumption are obtained through the optimization process with the use of free-space optical interconnects. This translates to improve the overall SoC performance by a factor of over 1.5.

CHAPTER 4

MODELING OF OPTICAL WAVEGUIDE INTERCONNECT

4.1 Introduction

In the previous chapters, the free-space optical interconnect technology for optoelectronic system-on-a-chip has been discussed. This chapter describes the modeling of optical waveguide interconnection for optoelectronic system-on-a-package. The proposed model can be applied directly to a CAD tool for designing optoelectronic system-on-a-package utilizing optical waveguide interconnection. In order to utilize optical interconnection to system-on-a-package, two major loss terms should be taken into account, which are inherent optical waveguide losses and optical waveguide bending loss. Inherent optical waveguide losses, which include scattering losses, material absorption losses and waveguide structural imperfection losses, are determined by a fiber scanning method [32]. Optical waveguide bending losses are considered as the power loss at each waveguide bends. Using real fabrication parameters, optical waveguide bending losses can be modeled with Boltzmann function. Finally, this chapter presents the comparison of electrical and optical interconnections by calculating clock signal timing skew.

4.2 Inherent Optical Waveguide Losses

In optical waveguide, inherent optical waveguide losses, which include scattering losses, material absorption losses and waveguide structural imperfection losses, are directly proportional to its material and its structure. From the physical design point of view, the losses are related to the path length from a location of an optical signal input to a receiver. Therefore, the optical network layout algorithm minimizes the path length using as a large bending radius for each bends in the optical waveguides as possible with the restriction that there is no cross-over among optical waveguides. For evaluation, the propagation loss is set to be 0.36dB/cm at a wavelength of 1.3μm measured by a fiber scanning method [32]. However, the splitting loss of optical waveguide is assumed to be negligible in this dissertation. As a reference, B. Bihari, *et al* show that the splitting loss is reduced to 0.4dB per splitter in their experiments [19].

4.3 Optical Waveguide Bending Losses

Figure 22 shows that a fundamental guided mode wavefront is traveling in an optical waveguide.

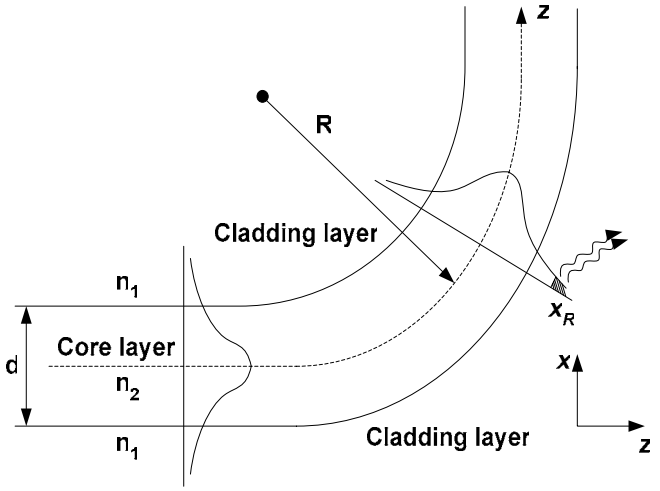


Figure 22. Bending loss derivation

When the mode passes through the bent optical waveguide, tangential velocity of the mode in a cladding layer, $v_{tan}=R(d\theta/dt)$ will exceed the velocity of light. Thus, the portion of the evanescent field tail x_R cannot stay in phase and splits away from the guided mode and radiates into a cladding layer.

The rate of total power loss along z can be described by,

$$-\frac{dP_m(z)}{dz} = \alpha_m P_m(z) \tag{3}$$

where α_m is the proportionality constant.

From Equation (3), the guided power for m^{th} mode can be written as,

$$P_m(z) = P_{0,m} e^{-2\alpha_m z} \tag{4}$$

where $P_{0,m}$ is the incident power for m^{th} mode and $z=\pi R/2$.

The α_m can be easily derived by calculating radiating aperture [38].

$$\alpha_m = C_1 e^{-2C_2 R} \tag{5}$$

where C_1 and C_2 are constants.

Therefore, Equation (4) is a function of bending radius of optical waveguide. The result of bending loss with specific fabrication parameters is curve-fitted with Boltzmann function to specify to our CAD tool shown in Figure 23.

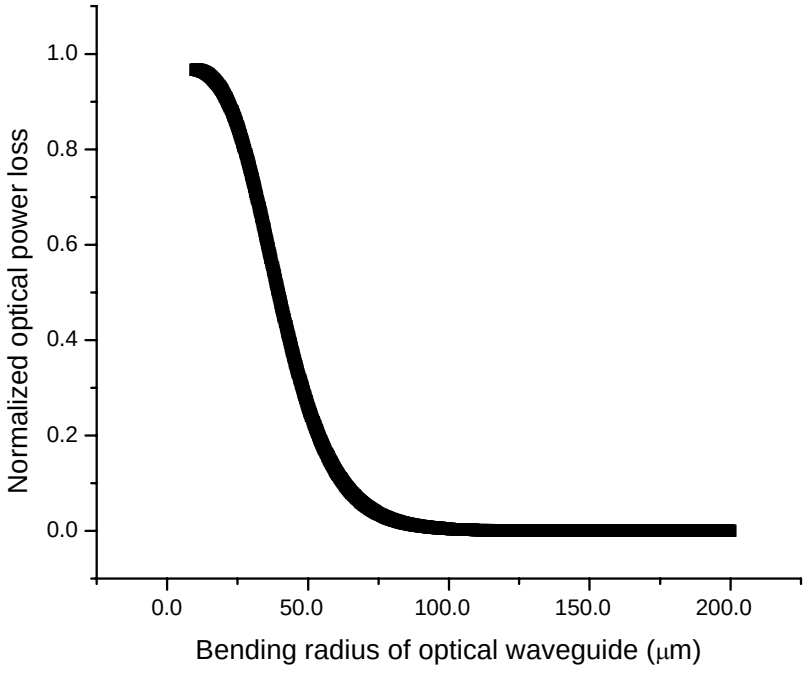


Figure 23. The normalized optical power loss

The parameters which are used in this chapter are taken from real fabrication parameters [32]. They are 1μm Benzocyclobutene (BCB) as a core layer, SiO_2 as a cladding layer, 1μm waveguide thickness and a wavelength of 1.3μm. The BCB index of refraction is 1.537 at a wavelength of 1.3μm and the SiO_2 index of refraction is 1.45 at a wavelength of 1.3μm [32]. The result is only for a single-mode operation. The analytical regression model for the bending loss of optical waveguide is shown in Equation (6).

$$\text{Bending Loss} = [1.0508/(1+e^{(\text{radius}-4\times10^{-5})/10^{-5}})] + 9.9\times10^{-4} \qquad (6)$$

Equation (6) tells that the result is saturated over 240μm bending radius of optical waveguide. It translates that the bending loss is negligible over 240μm bending radius. For the simulations, the minimum bending radius of optical waveguide is assumed to be 100μm. The lossless tight bending is only feasible with a high contrast optical waveguide like in [32]. In 1998, P.G. Kik and A. Polman also claimed the bending radius could be as small as 50μm for a high contrast waveguide such as an Al_2O_3 core with an SiO_2 cladding(Δn=0.20) [33]. They have shown that a 3cm long waveguide can be roll-up on an area of only 1mm for such a system.

4.4 Clock Signal Timing Skew Calculation

The effective refractive index of TE_0 mode in the dielectric waveguide is about 1.537. c is the speed of light in free-space. n is effective refractive index. λ is 1.3μm. $dn/d\lambda$ is approximately calculated with conventional BCB material, which is 3022 family [39].

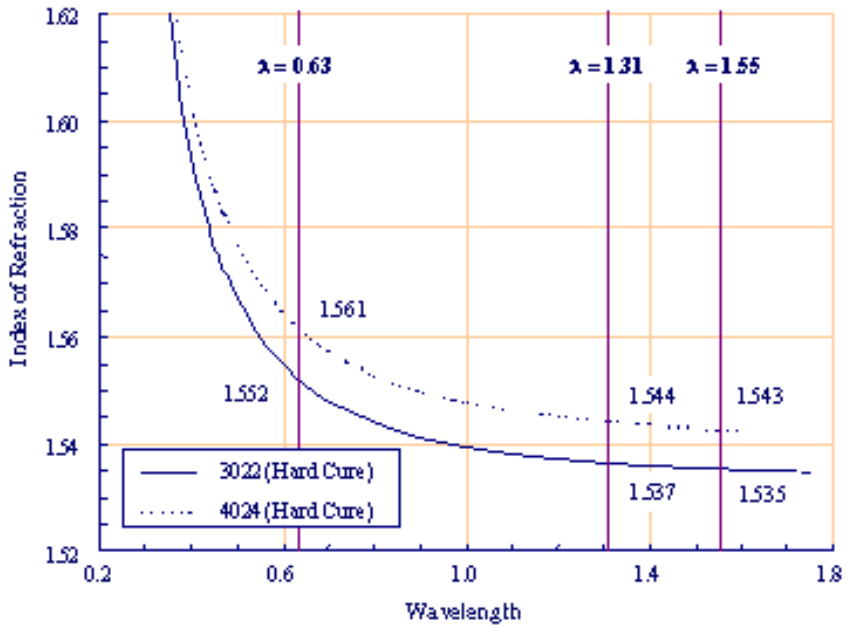


Figure 24. Index of refraction as a function of wavelength for photo BCB (4024-40) and non-photo BCB (3022-46) after curing at 250°C for 60 minutes

v_g is the group velocity of the guided mode in the material with an ideal monochromatic optical source.

$$\upsilon_g = c\left[n - \lambda\frac{dn}{d\lambda}\right]^{-1} \approx 1.93675\times10^8\,(\mathrm{m/s}) \tag{7}$$

Thus, delay $d_{optical}$ is

$$d_{optical} = \frac{x}{\upsilon_g} = \frac{x}{1.93675\times10^8}(\mathrm{sec}) \tag{8}$$

where x = (a path length – the shortest path length).

However, the delay $d_{electrical}$ in electrical interconnection is

$$d_{electrical} = \frac{x}{c/5} = \frac{x}{0.6\times10^{8}}(\sec) \qquad (9)$$

because the signal propagation speed for repeatered global electrical interconnections can be assumed to be approximately c/5 [40].

In order to minimize clock skew, our CAD algorithm finds the optimal bending radius with the assumptions that are made in Section 4.2. This implies that path lengths are minimized and clock skews are also minimized with a given partitions and routing.

4.5 Summary

The result of bending loss with specific fabrication parameters is curve-fitted with Boltzmann function. The parameters which are used in this chapter are taken from a real fabrication parameter [32]. The result is only for a single-mode operation. The analytical regression model for the bending loss of optical waveguide is shown in Equation (6). Equation (6) tells that the result is saturated over 240μm bending radius of optical waveguide. It translates that the bending loss is negligible over 240μm bending radius. For the simulations, the minimum bending radius of optical waveguide is assumed to be 100μm.

According to Section 4.4, the signal propagation speed in optical waveguide interconnect is dominant over one in electrical interconnect once the interconnect length is over 2.4cm.

CHAPTER 5

DESIGN OF OPTICAL CLOCK DISTRIBUTION NETWORKS USING OPTICAL WAVEGUIDE INTERCONNECT

5.1 Introduction

Due to increasing levels of integration and sophistication in packaging technologies, the problem of routing electrical control and synchronization signals to the various subsystems of the package has assumed great significance. These control and synchronization signal networks, such as the clock distribution networks discussed in this chapter, have to be designed very carefully in order to maximize the performance of the assembled electronic package while minimizing manufacturing costs. Specifically, for clock distribution, the skew of the clock signal from the source to the various destination points must be minimized in order to maximize the electrical performance of the package. In addition, overall power consumption must be minimized. These stringent design requirements necessitate the development of new computer-aided design (CAD) algorithms for emerging technologies such as optical interconnect.

C. Chappe first invented the optical telegraph in 1790. This served as the starting point for optical communication systems. In 1870, J. Tyndall demonstrated that light could be guided in a water jet. However, the idea of a communication system based on the propagation of light through circular dielectric waveguides was considered from the mid-1960s, albeit some theoretical studies were performed in the early years of the present century [3], [4].

In 1984, J. W. Goodman suggested three optical clock distribution approaches [7]: unfocused free-space, focused free-space and index-guided optical interconnect. Free-space optical interconnect technology is suitable for routing on-chip interconnects using an optical interconnect layer. Special lenses and diffraction gratings are employed to route signals optically from point on the silicon die to another. This chapter discusses a new approach to optimal routing of clock signals using index-guided optical interconnect. This employs advanced technology in which optical waveguides are directly integrated into the package substrate. The approach provides a compact and planar packaging of the global optical clock distribution.

A multi-GHz optical clock distribution on a Cray T-90 supercomputer multi-processor board is presented in 1999 [17]. The optical clock signal is distributed to 48 fanout points on $14.5\times27\text{cm}^2$ printed wiring board through a polyimide optical waveguide organized as an H-tree structure.

The 2002 Semiconductor Industry Association (SIA) roadmap update shows the substantial problems associated with electrical interconnects in silicon chips [21]. Off-chip long distance interconnections suffer in performance. It is proposed to replace such interconnections with optical interconnect to migrate specific interconnect performance issues. In this chapter, we develop a new CAD algorithm that finds an optimal clock routing network and a best optical data input location for the network utilizing optical waveguide technology. Figure 25 shows "***BOSS***" (Board-level Optical clock Synthesis and Simulator tool) layout with two simulation results of symmetric 64-fanout. The right window layout is an optimized layout of the layout shown on the left window.

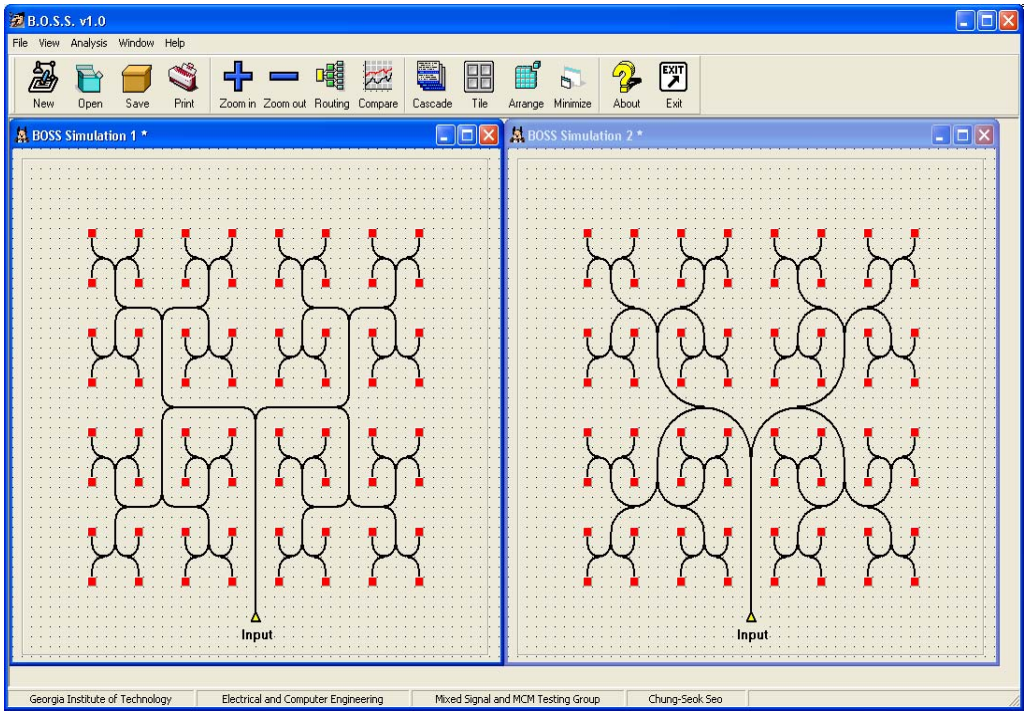


Figure 25. BOSS layout with a symmetric structure simulation

5.2 Problem Statement

The integration configuration of an optical clock routing on system-on-a-package (SOP) substrate that is discussed in this chapter is shown in Figure 26. This H-tree optical clock structure consists of three 1-to-2 optical power splitters.

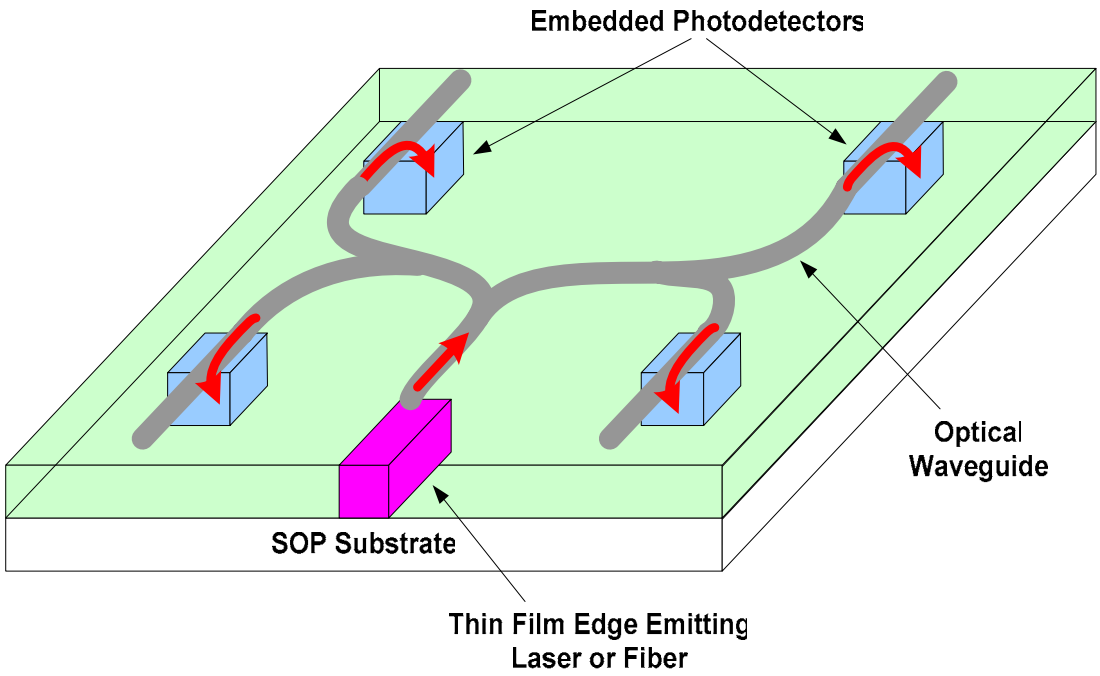


Figure 26. Integration configuration for high-speed optical clock distribution using embedded optoelectronics

In this chapter, we design clock distribution networks using optical waveguide interconnections instead of electrical interconnections. In designing such networks, the performance of the clock distribution networks needs to be minimized. This performance

is determined by bending losses in the optical waveguide as well as signal skews introduced by different lengths of the interconnect. Therefore, two major losses were considered and modeled in Chapter 4, which are optical waveguide bending losses and inherent optical waveguide losses. Using the loss models, we develop a new CAD algorithm that finds the optimal clock routing network and a best optical data input location for the network utilizing optical waveguide technology in Section 5.3.

5.3 Optimization Algorithms

The optimization goals are as follows:

- *Given*: The locations of all the terminal points (detectors) to which the clock signal is to be routed optically.
- *Determine*: (a) The location of the clock signal transmitter on the printed wiring board and (b) the optimal layout of the optical waveguides from the transmitter to each of the detectors.
- *Such that (optimization criteria)*: (a) clock signal skew is minimized and (b) bending and propagation losses due to the optical waveguides are minimized.

The optimization algorithm consists of a *layout partitioning step*, a *waveguide routing step* and a *calibration step for the location of optical data input*.

The flowchart of the optimization process is shown in Figure 27.

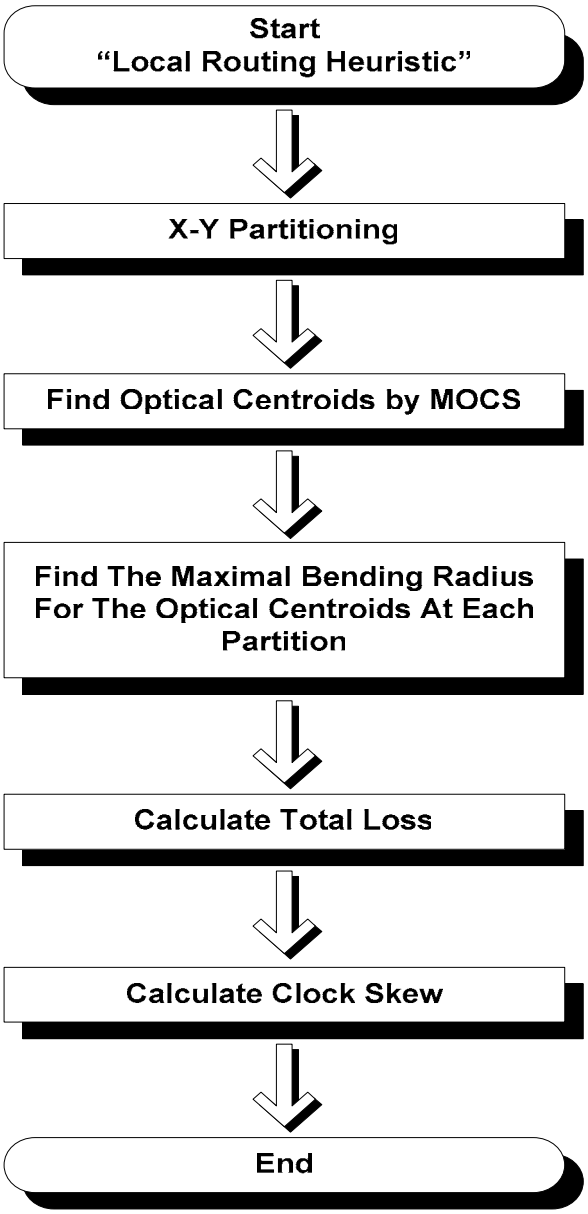


Figure 27. Overall flow of optical clock routing

5.3.1 Design Assumptions

It is assumed that different combinations of L-shaped waveguides (90˚ bent L-shape) are used to construct the optimal optical routing network. Each L-shaped interconnect is able to have a different radius of curvature. This provides flexibility of design as opposed to the use of a rigid H-tree structure. The optical waveguide is assumed to be Transverse Electric (TE) field polarized with single mode operation. It is also assumed that there is an isolation layer between electrical and optical substrate to avoid signal-absorption. The final layout is a 1-to-2^x fanout structure where x>1. This means that the system is a single clock system and the number of detectors on board is 2^x where x>1.

From the viewpoint of signal transmission latency, optical interconnection has three types of latencies: transmitter latency, the signal flight time latency and receiver latency. In this chapter, the latencies in the optical transmitter and the optical receiver are not considered. However, it is reported that they are less than 100psec respectively in recent publication [41].

5.3.2 Layout Partitioning

The X-Y partition algorithm is used [42] to group two detectors as one group, so that we can utilize 1-to-2 optical power splitter and find its "optical centroid" (see Section 5.3.3) in the later clock routing phase. The board B is partitioned into two subregions, B_L and B_R with equal number of detectors. The subregions B_L and B_R are then partitioned in the orthogonal direction. Alternating x- and y-direction partitioning is recursively performed until there are two detectors in each subregion.

The algorithm is illustrated in Figure 28.

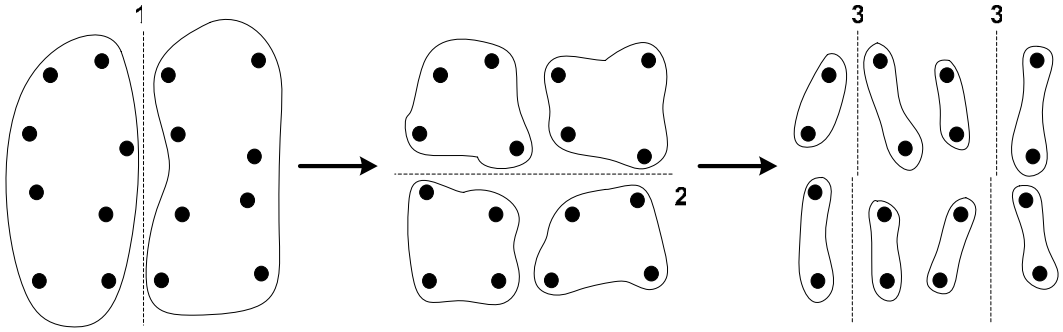


Figure 28. X-Y partition algorithm

5.3.3 Optical Clock Routing

For clock distribution, the skew of the clock signal from the source to the various destination points must be minimized in order to maximize the electrical performance of a package. Exact zero skew algorithms using Elmore delay model have been developed for electrical clock routing [43-45].

For optical clock distribution, a new algorithm which we call *the Method of Optical Centroid Searching (MOCS)* is developed. The basic idea of the MOCS algorithm is to minimize the path length difference from the transmitter to any of the detectors by finding "optical centroid" based upon Manhattan Geometry. These optical centroids represent points in the layout grid that are *equidistant* from all other points in the same layout partition at each step of the recursive layout partitioning process. Hence, there are as many optical centroids as there are recursive calls in the layout partitioning algorithm.

In order to feed all the detectors corresponding to a layout partition, the signal feeding the detectors is fanned out to the detectors or other optical centroids at the optical centroid corresponding to the partition. The MOCS algorithm is illustrated in Figure 29.

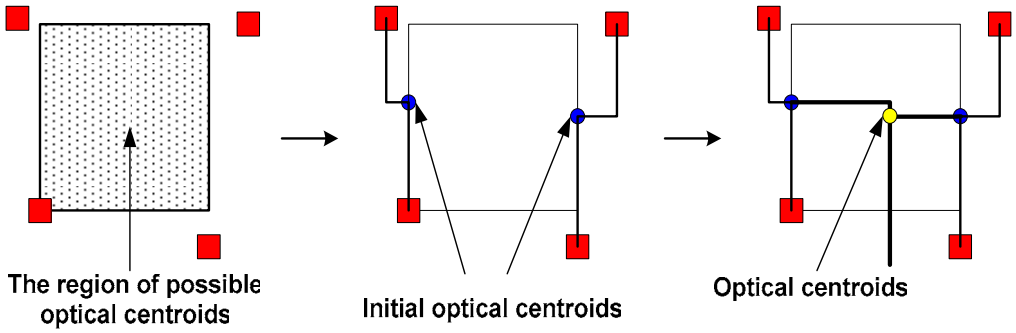


Figure 29. The method of optical centroid searching

Let C be a set of 4 optical centroids. It is assumed that 4 detectors are initially set as the first optical centroids.

$$C(x) = \{c_x(i) \mid c_x(i) \text{ is centroid sorted in x-direction}\}$$

$$C(y) = \{c_y(i) \mid c_y(i) \text{ is centroid sorted in y-direction}\}$$

where $i = (1,2,3,4)$.

The next optical centroids of C are located in region R_C.

$$R_C = \{x, y \mid (c_x(2) \le x \le c_x(3)) \cap (c_y(2) \le y \le c_y(3))\}$$

Let C_L, C_R, C_T and C_B be initial optical centroids and C_M be the next optical centroid which is a yellow dot in Figure 29. Let PL_L, PL_R, PL_T and PL_B be path lengths

from the left, right, top and bottom optical centroid to the detectors on the left, right, top and bottom side.

The pseudo code for recursive MOCS is given in Figure 30. This MOCS is recursively introduced until there is only one optical centroid after searching.

Algorithm 5.1. Method of Optical Centroid Searching

```
1.  for (all the segments by X-Y partitioning ) {
2.      decide waveguide proceeding direction;
3.      if (waveguide proceeding direction is up or down) {
4.          abs_height = abs(C_L(y) –C_R(y));
5.          difference = abs(PL_L–PL_R);
6.          PL_1 = PL_L; PL_2 = PL_R; C_1 = C_L(y); C_2 = C_R(y);
7.      } else {
8.          abs_height = abs(C_T(x)-C_B(x));
9.          difference = abs(PL_T–PL_B);
10.         PL_1 = PL_T; PL_2 = PL_B; C_1 = C_T(x); C_2 = C_B(x);
11.     }
12.     if (PL_1 > PL_2) {
13.         if ((down and C_1 < C_2) or (up and C_1 > C_2)) {
14.             d_1 = C_1 – abs_height; d_2 = C_2 –difference;
15.         }
16.         else if ((down and C_1 >= C_2) or (up and C_1 <= C_2))  {
17.             d_1 = C_1; d_2 = C_2 –difference+ abs_height;
18.       }
```

Figure 30. Pseudo code for MOCS algorithm

```
19.         else if ((left and C1 < C2) or (right and C1 > C2)) {
20.             d1 = C1; d2 = C2 –difference– abs_height;
21.         }
22.         else {
23.             d1 = C1+ abs_height; d2 = C2 –difference;
24.         }
25.     else {
26.         if ((down and C1 < C2) or (up and C1 > C2)) {
27.             d1 = C1+difference– abs_height; d2 = C2;
28.         }
29.         else if ((down and C1 >= C2) or (up and C1 <= C2)) {
30.             d1 = C1+difference; d2 = C2+ abs_height;
31.         }
32.         else if ((left and C1 < C2) or (right and C1 > C2)) {
33.             d1 = C1+ abs_height; d2 = C2 –difference;
34.         }
35.         else {
36.             d1 = C1; d2 = C2– difference –abs_height;
37.         }
38.     }
39.     leng_diff = (d2 – d1)/2;
40.     if (waveguide proceeding direction is up or down) {
41.         CM(x) = x1 + leng_diff;
42.         if (C1 < C2) CM(y) = C2;
43.         else CM(y) = C1;
44.     }
```

Figure 30. Pseudo code for MOCS algorithm (Continued)

```
45.     else {
46.         C_M(y) = y1 + leng_diff;
47.         if (C_1 < C_2) C_M(x) = C_2;
48.         else C_M(x) = C_1;
49.     }
50. Find_optical_centroid( );
51. }
52. Find the best location of an optical data input (Section 5.3.4);
```

Figure 30. Pseudo code for MOCS algorithm (Continued)

For routing, any optical waveguide cannot cross any other optical waveguide or any detector to avoid inducing significant power loss caused by a discontinuity at the intersection.

5.3.4 Optical Data Input Location

As mentioned earlier, the system designed in this chapter is a single clock system. BOSS provides layouts of 1-to-2^x fanout (x>1). The optical data input location is determined at the end of routing through the MOCS (Method of Optical Centroid Searching) algorithm. The x coordinate is same as the last optical centroid and the y coordinate is the bottom of the board.

5.3.5 Local Routing Heuristic

For each optical centroid, the maximum bending radius is different. Examples of a local routing stage with different bending radii are shown in Figure 31.

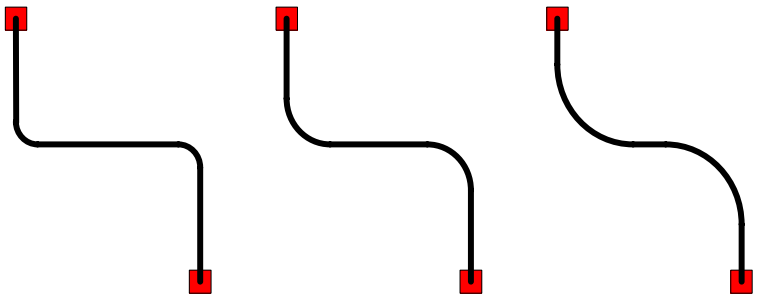


Figure 31. Example layout with different bending radii

Different bending radii of the optical interconnect cause a length difference between optical data input point and the detector location. This results in signal timing skew. Thereby, bending radii of all waveguides corresponding to the n^{th} stage of recursion are all identical to avoid signal timing skew. The n^{th} stage of recursion in Figure 30 corresponds to a local layout of the optical waveguides from a centroid (*local centroid*) to other centroids (*sub-centroids*) or a set of detectors. For routing from a local centroid to a sub-centroid, the ideal choice is to pick a waveguide layout with the largest bending radius. This minimizes bending losses. However, use of interconnect with different bending radius (see Figure 31) can cause timing skews between the various signal paths. Thus, all waveguides are routed using the smallest bending radius (of the

largest for each interconnect) over all the interconnects from the local centroid to all the sub-centroids. This is called the *local routing heuristic*.

The pseudo code for local routing heuristic is as follows:

Algorithm 5.2. Local Routing Heuristic

```
1. X-Y partitioning (Section 5.3.2);
2. Find_optical_centroid( ) (Figure 29);
3. for (each partition) {
4.     Find the maximal bending radius for the optical centroids
       at each partition;
5.     bending radius = the smallest bending radius among the
       optimal bending radii of each stage;
6. }
7. Calculate total loss (Section 4.2 and 4.3);
8. Calculate delay (Section 4.4);
```

Figure 32. Pseudo code for local routing heuristic

5.4 Results and Analysis

5.4.1 Preliminary Result

The preliminary result for a 4-fanout structure is shown in Figure 33.

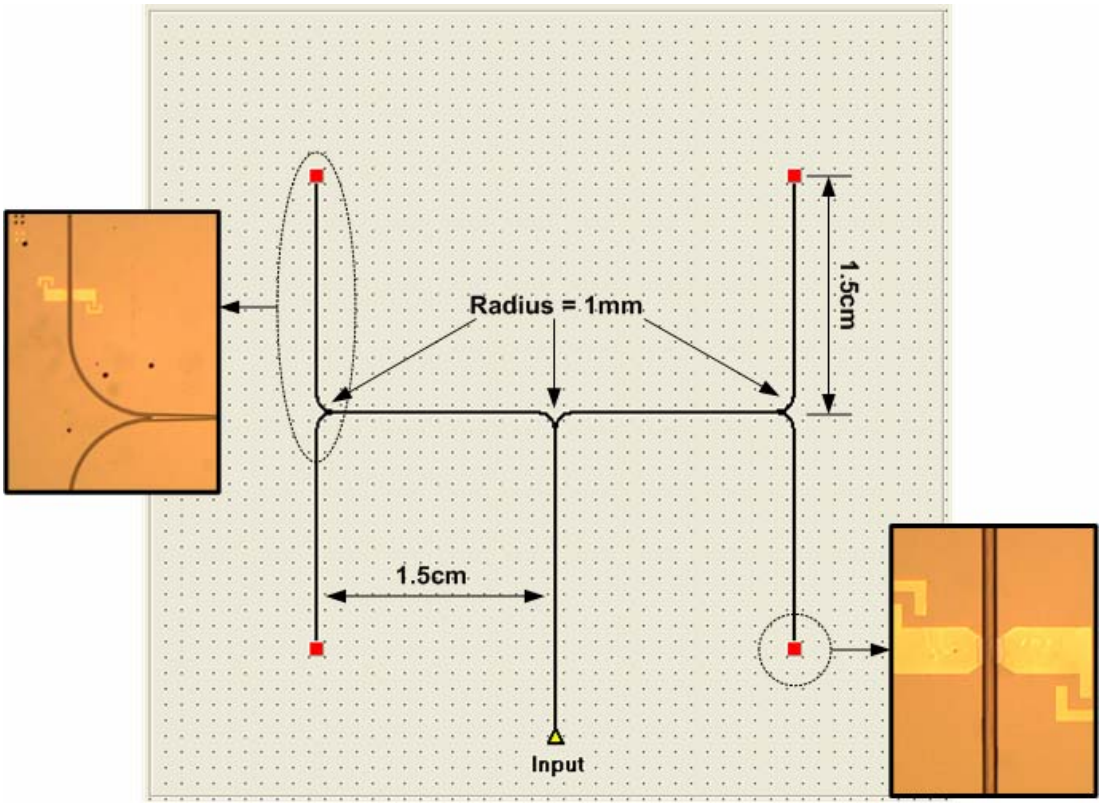


Figure 33. 1-to-4 H-tree structure layout with two enlarged microphotographs of fabrication

This design was designed using BOSS and fabricated. Two microphotographs corresponding to the fabricated Inverted-Metal Semiconductor Metal (I-MSM)

photodetectors embedded in the BCB (Benzocyclobutene) polymer waveguide on the SiO_2/Si substrate are also shown in Figure 33. The dimension of the board is $5\times5cm^2$. The bending radii of the optical waveguides are respectively 1mm.

5.4.2 Symmetric Structure

An H-tree system with fanout of 256 has been designed. Figure 34 shows the layout before optimization. The dimension of the board is $10\times10cm^2$ and the bending radius is 1.5mm. The length between detectors is 6mm in the x- and y-directions. The optimized layout of Figure 34 is shown in Figure 35 through the use of waveguides with different bending radii.

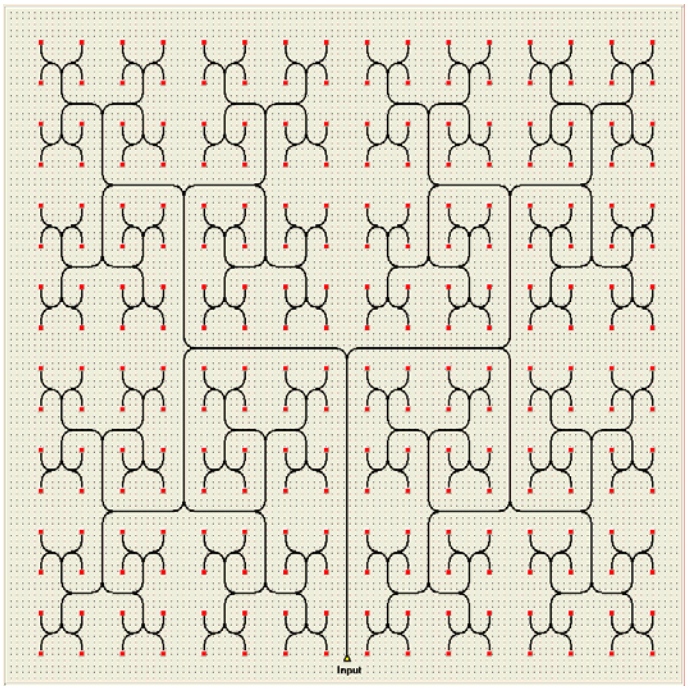


Figure 34. Symmetric clock routing of fanout 256 before optimization

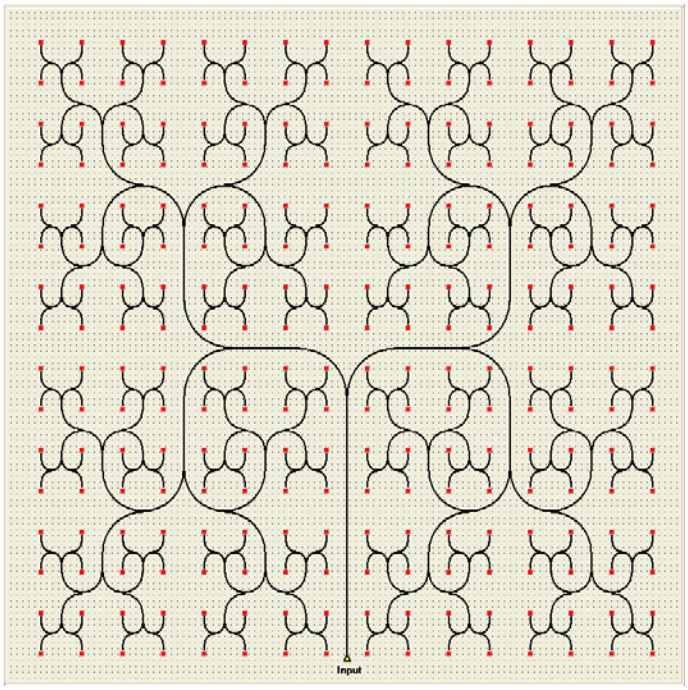


Figure 35. Symmetric clock routing of fanout 256 after optimization

This was carefully designed to avoid waveguide-crossing. The bending radii of each stage from a detector to an optical data input are 1.5, 1.5, 3, 3, 6, 6, 7 and 7mm.

The total loss of the longest path from an optical data input to a detector due to changing bending radius is calculated and shown in Figure 36.

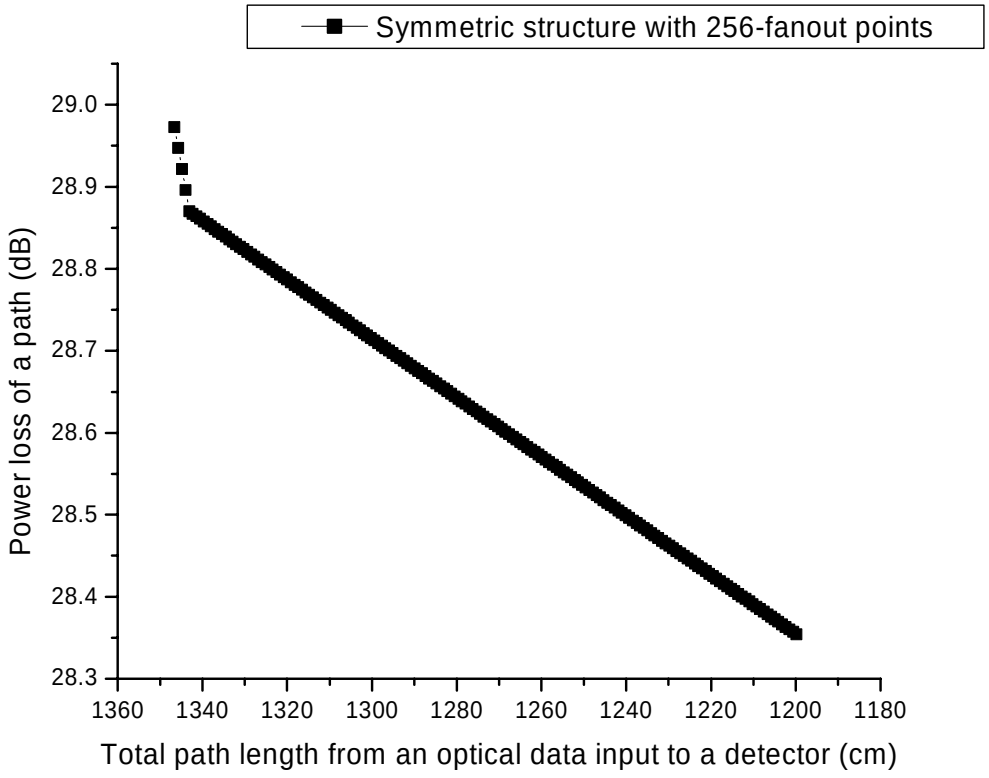


Figure 36. The reduction graph of total optical power loss of the longest path from an optical data input to a photodetector

The total loss includes the bending loss of optical waveguide, the propagation loss and the splitting loss described in Chapter 4. The maximum power saving after optimization is about 15%.

5.4.3 Asymmetric Structure

With the new L-shaped optical waveguide, BOSS can design asymmetric structures while finding the best location of the optical data input.

Figure 37 shows an asymmetric clock routing of fanout 64 utilizing the proposed MOCS algorithm (see Section 5.3.3) with L-shape optical waveguide. The dimension of the board is $5\times5cm^2$. Each bending radius is 200μm. Through the use of different bending radii, the layout of Figure 37 is optimized and results in the layout of Figure 38.

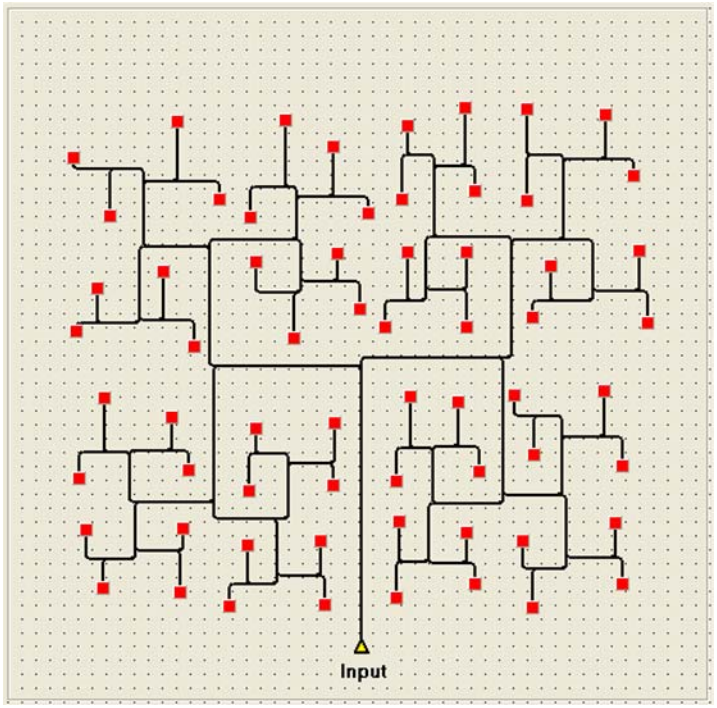


Figure 37. Asymmetric clock routing of fanout 64 before optimization

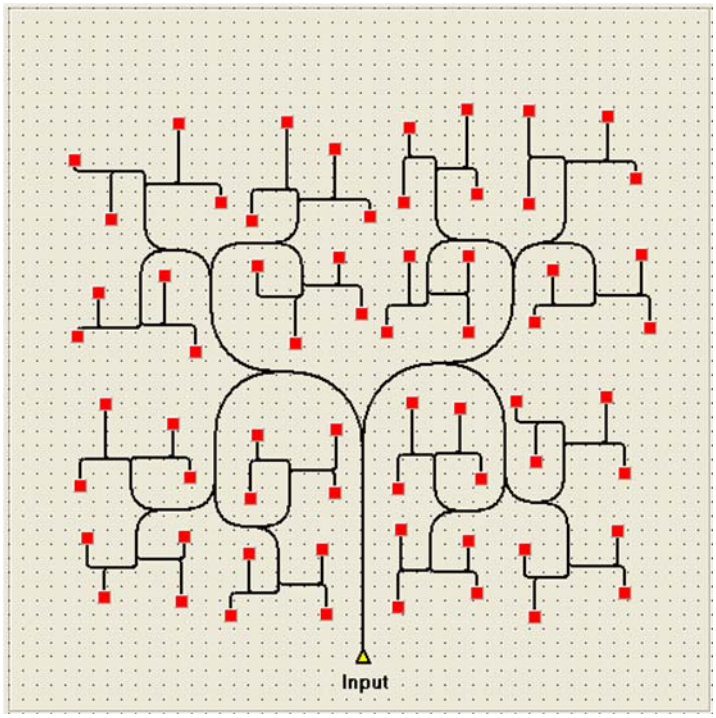


Figure 38. Asymmetric clock routing of fanout 64 after optimization

The bending radii of each stage from a detector to an optical data input are 0.2, 0.2, 1.5, 1.8, 4.2, and 5.0mm.

Another asymmetric clock routing of fanout 256 is designed in Figure 39. The layout is very similar to the H-tree structure. The dimension of the board is $10\times10cm^2$. Each bending radius is 400μm. Figure 40 is an optimized version of Figure 39 with different bending radii - note that no additional timing skew is introduced in Figure 40 as opposed to Figure 39.

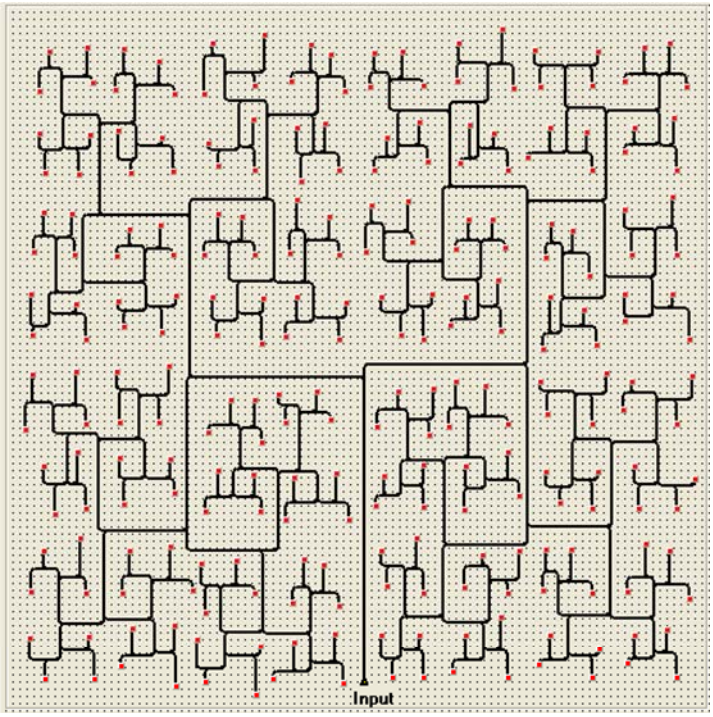


Figure 39. Asymmetric clock routing of fanout 256 before optimization

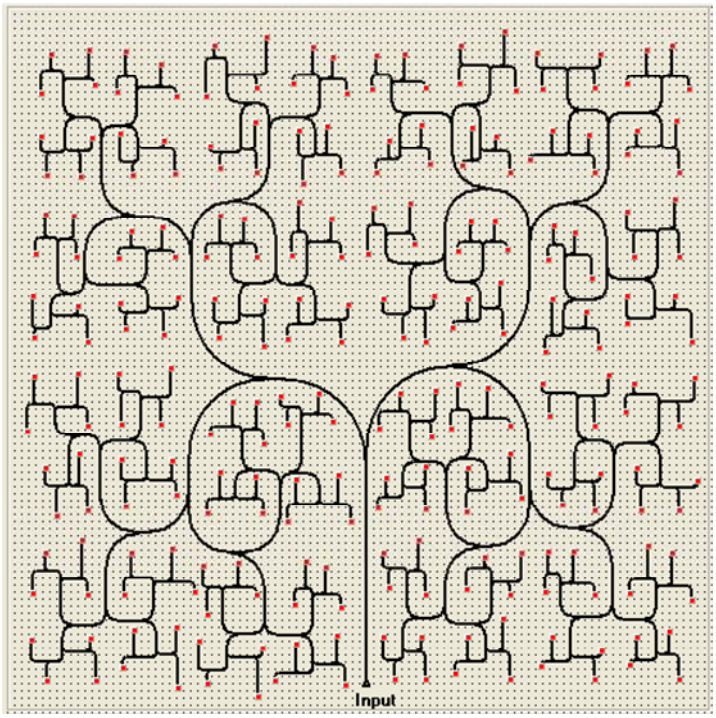


Figure 40. Asymmetric clock routing of fanout 256 after optimization

The bending radii of each stage from a detector to an optical data input are 0.4, 0.4, 1.5, 1.5, 4.8, 5.4, 10.8 and 11.6mm.

5.4.4 Optical Power Loss and Signal Timing Skew

Table 6 shows the total power loss along the longest path for each bending stage. As described earlier, the bending loss exceeded 240μm bending is negligible. That is the reason the results don't seem to be affected by the bending loss.

Table 6. Power loss along the longest path for each stage (dB)

Structure \ Stage		1	2	3	4	5	6	7	8
Symmetric	16	3.82	7.12	10.3	13.9	N/A	N/A	N/A	N/A
	64	3.84	7.12	10.3	13.4	16.5	20.1	N/A	N/A
	256	4.58	8.34	11.7	15.0	18.2	21.4	24.4	27.6
Asymmetric	64	3.99	7.90	11.2	14.3	17.4	21.0	N/A	N/A
	256	4.61	8.39	11.9	15.2	18.5	21.6	24.6	27.8

Table 7 shows minimum, maximum, average signal timing skew and the maximum time of signal flight along the longest path for different structures.

Table 7. Signal timing skew along the longest path

Structure \ Skew		Minimum (psec)	Maximum (psec)	Average (psec)	Time of flight (psec)
Symmetric	16	0	0	0	163.91
	64	0	0	0	240.16
	256	0	0	0	599.89
Asymmetric	64	7.5	7.5	1.28	255.82
	256	23.9	26.1	3.48	614.38

The maximum signal timing skew is about 26.1psec when the time of signal flight is 614.38psec. This result implicates that signal timing skew in the simulation structures is negligible (< 4%). For the same structure with electrical interconnections based on Equation (9), the signal timing skew is about 87.43psec.

5.5 Summary

We have presented a new approach to optimized clock routing using optical waveguide. The results are very encouraging and show that less than 26.1psec in signal timing skew is obtained for a signal flight time of 614.38psec. This translates that the signal timing

skew can be neglected (< 4%). For optical power consumption, about 15% reduction is also obtained over clock nets routed with existing (optical) methods.

CHAPTER 6

DESIGN OF OPTOELECTRONIC SYSTEM-ON-A-PACKAGE USING OPTICAL WAVEGUIDE INTERCONNECT

6.1 Introduction

Since the 1980s, the rate of improvement in terms of wire length reduction is only 5-10% every 2-3 years based on International Technology Roadmap for Semiconductors (ITRS) report [21]. It translates that it takes about 10 years for 30% wire length reduction. About 30% wire length reduction could be obtained when we improve CMOS process technology, for instance, from 0.13μm to 0.10μm. However, the technology improvement costs around a few billion dollars. If taking into account time-to-market together, the overall cost of 30% wire length reduction will be tremendous.

Recently, C. Chang, *et al*, reported comparison results about optimality and scalability of existing placement algorithms [46]. The results basically indicate that about 30% wire length reduction could be achieved using a new approach of placement of chips. Therefore, the development of a new optimization algorithm instead of the improvement

of physical process technology could achieve the same improvement with less time-consuming.

According to ITRS [21], Electronic Design Automation (EDA) roadmap and MEL-ARI OPTO Technology roadmap [47], optical interconnection is believed to be introduced to enhance the performance of current electrical system-on-a-package because bandwidth demands are increasing and electrical interconnection is faced with the physical bottlenecks, such as capacitive loading, mutual crosstalk, reflection, switching noise, clock skew, power consumption, timing jitter, etc. On the contrast, optical interconnection has attractive features such as high bandwidth, invulnerability to electromagnetic interference (EMI), negligible mutual crosstalk, high speed, low power consumption, low timing jitter, etc.

M. Forbes, et al, presented three different types of approaches for optoelectronic interconnects between VLSI chips [20]: fibre-ribbons, planar waveguides and free-space optics. This paper pointed out the limitations of electrical interconnects and the advantages of optical interconnects.

However, optoelectronic system-on-a-package cannot be designed by current physical computer-aided design (CAD) tools because such tools cannot deal with electrical and optical interconnections simultaneously. Moreover, there are no publication yet which presents physical design process of optoelectronic system-on-a-package until now. Hence we need a new optimization algorithm to design and optimize current electronic system-on-a-packages utilizing optical waveguide technology. Eventually, it is

believed that the system performance will be improved by a factor of a thousand once optical interconnections are introduced.

In this chapter, we develop a CAD tool for physical design of optoelectronic system-on-a-package using optical waveguide interconnects. Figure 41 shows the integration configuration of optical data path routing on a system-on-a-package (SOP) substrate.

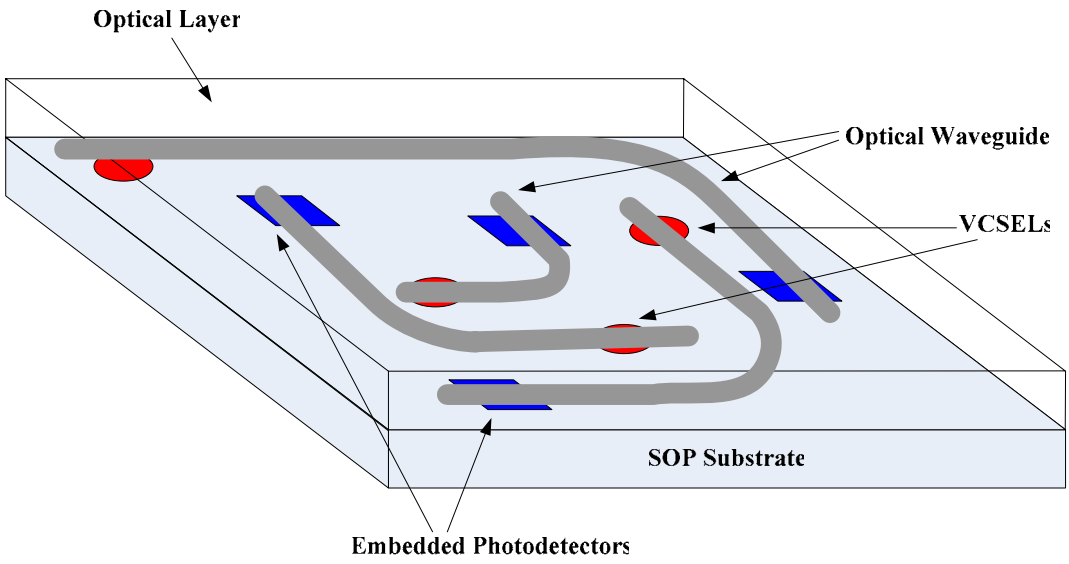


Figure 41. Integration configuration for high-speed optical data path routingon a SOP substrate using enbedded optoelectronics

The major objective of this chapter is to develop a new algorithm for placement of modules on a SOP substrate and routing of electrical and optical interconnect utilizing optical waveguide technology. A new approach to placement of modules on a SOP

substrate and routing electrical and optical interconnects will maximize the overall performance of optoelectronic system-on-a-package.

Figure 42 shows GHOST (Genetic High-performance Optoelectronic System design Tool) layout with two simulation results. The left window figure is an area-driven optimized layout and the right window figure is an interconnect-driven optimized layout.

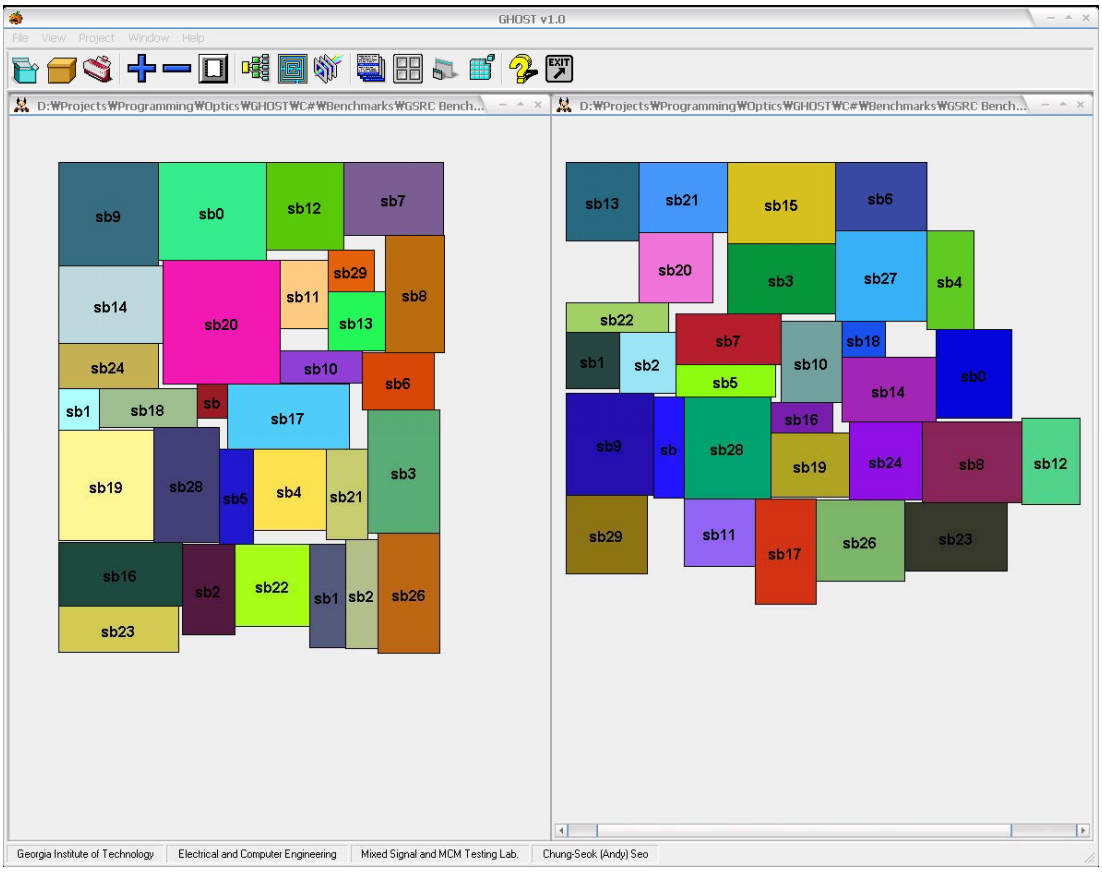


Figure 42. GHOST layout

6.2 Problem Statement

The fundamental problem is to place modules and route electrical and optical interconnects on a SOP substrate. The problem consists of three issues: module placement, assignment of a subset of interconnects to optical interconnects, and optical waveguide and electrical routing. The three issues are mentioned in Section 6.3, 6.4 and 6.5.

In this chapter, a simulated annealing and a hybrid genetic algorithms are employed for simultaneously optimizing the module block placement and routing problems. Pseudo codes for the algorithms are shown in Figure 43 and Figure 44.

Algorithm 6.1. Simulated Annealing

```
1.  Initialize temperature and placement;
2.  While (temperature > final temperature) {
3.      While(inner_loop_criterion is FALSE) {
4.          Perturbation;
5.          Cost = Placement_and_Routing(Sequence-Pair);
6.          If (Cost is not Acceptable) Reject;
7.          Calculate the next temperature;
8.      }
9.  }
10. Display the result;
```

Figure 43. The pseudo code for the simulated annealing

Algorithm 6.2. Hybrid Genetic Algorithm

```
1.  Initialize module locations;
2.  Initial placement(for all modules);
3.  samecost = 0;
4.  best cost = old cost = Area of initial placement;
5.  for (int i=0; ((i < iteration)&&(samecost < stop)); i++)
6.  {
7.       generate random probability;
8.      if (probability > xoverprob) Force Directed Crossover();
9.      Mutation();
10.     cost = Placement();
11.     if (cost < bestcost)
12.     {
13.         Keep the child; bestcost = cost;
14.     }
15.     else if (cost > oldcost)
16.     {
17.         Reject the child; cost = oldcost;
18.     }
19.     oldcost = cost;
20.     if (oldcost == bestcost) samecost++;
21.     else samecost = 0;
22.     Generate next population;
23. }
```

Figure 44. Hybrid genetic algorithm for optimization of module placement and routing of electrical and optical interconnects

Only different part of the hybrid genetic algorithm from a general genetic algorithm is "crossover." We call this algorithm "Hybrid genetic algorithm" because force directed algorithm is applied to crossover function. When randomly generated probability is greater than the crossover probability, every vector forces among modules are calculated. According to the vector forces, module placement is executed. The hybrid genetic algorithm dramatically reduces the simulation time, but often converges to a local minimum. In order to avoid falling into a local minimum, the force directed crossover function is switched with a general crossover function from time to time.

The optimization process is composed of three steps: (a) Module block placement, (b) Partition of electrical and optical interconnects and (c) Routing of electrical and optical interconnects. The three steps are discussed in following sections (Section 6.3, 6.4 and 6.5).

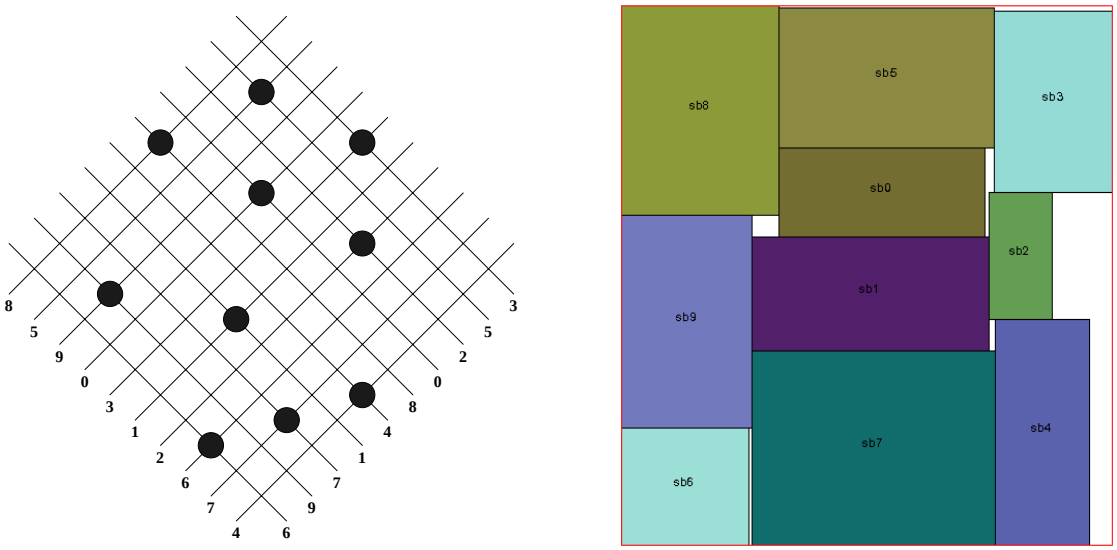
6.3 Block Placement Algorithm Based on Sequence Pair

There are several representations for the block placement. In this chapter, we use sequence pair representation because it is efficient for general non-slicing structures [49]-[51].

A sequence pair is a pair of sequence of *n* blocks. Figure 45(a) shows a 45 degree oblique grid which is constructed by a sequence pair (S_1, S_2) and Figure 45(b) shows the block placement which is constructed by the oblique grid. In sequence pair (S_1, S_2), each pair of blocks has the following relationship.

$$(<\ldots S_{1a}\ldots S_{1b}\ldots>, <\ldots S_{1a}\ldots S_{1b}\ldots>);\ S_{1a} \text{ is left } S_{1b} \qquad (10)$$

$$(<\ldots S_{1b}\ldots S_{1a}\ldots>, <\ldots S_{1a}\ldots S_{1b}\ldots>);\ S_{1a} \text{ is below } S_{1b} \qquad (11)$$



(a) (b)

Figure 45. An example of GSRC benchmark circuits: (a) 45 degree oblique grid of a sequence pair ((8 5 9 0 3 1 2 6 7 4), (6 9 7 1 4 8 0 2 5 3)), (b) Block representation by a sequence pair in (a)

In this chapter, we use Sequence-Pair representation by longest common subsequence computation which is proposed by X. Tang, *et al* [49]. The pseudo code for the algorithm is shown in Figure 46.

Algorithm 6.3. Block Placement Algorithm

```
1.  Clear Array.of Lx;
2.  Clear Array of Ly;
3.  for (int i=0; i<Number_of_Blocks; i++)
4.  {
5.      y_bk = x_bk = i;
6.      x_bk_index = Array.IndexOf(x_bk);
7.      y_bk_index = Array.IndexOf(y_bk);
8.      X[x_bk] = Lx[x_bk_index];
9.      Y[y_bk] = Ly[y_bk_index];
10.     tempX = Block_Size_X[x_bk];
11.     tempY = Block_Size_Y[y_bk];
12.     totX = X[x_bk] + tempX;
13.     totY = Y[y_bk] + tempY;
14.     for (int j=x_bkindex; ((j<Number_of_Blocks)&&(totX>Lx[j])); j++)
15.         Lx[j] = totX;
16.     for (int k=y_bkindex; ((k<Number_of_Blocks)&&(totY>Lx[k])); k++)
17.         Ly[k] = totY;
18. }
19. Return Lx and Ly;
```

Figure 46. Block placement algorithm based on sequence pair representation by longest common subsequence computation

6.4 Partition of Electrical and Optical Interconnects and Routing of Electrical Interconnect

The signal flight time $f_{electrical}$ in electrical interconnection is

$$f_{electrical} = \frac{L}{c/5} = \frac{L}{0.6\times10^{8}}(\sec) \qquad (12)$$

where L is a path length and , c is the speed of light in free-space, because the signal propagation speed for repeatered global electrical interconnections can be assumed to be approximately c/5 [40]. With the Equation (12), the breakpoint which optical waveguide interconnect dominates over electrical interconnect can be calculated from the viewpoint of the signal flight time.

There are several publications which reported the latencies in the optical transmitter and the optical receiver. It is reported that they are less than 20psec respectively in recent publication [32]. If taking into account the latencies, the breakpoint which optical waveguide interconnect is dominant over electrical interconnect is around 2.4cm.

With the breakpoint, we determine whether a topological interconnect is routed electrically or optically. Clearly, this partitioning depends on the placement of modules on the SoP substrate. The CAD tool attempts to route the longest interconnects optically if the interconnects' lengths are longer than the breakpoint length.

6.5 Optical Data Path Routing

Optical data path routing is the single-layer routing problem [2]. Although the fundamental problem in general single-layer problem is to determine if all the interconnects can be routed or not, a slight change is adopted. In this chapter, we attempt to replace electrical interconnects with optical interconnects as many as possible. However, any optical waveguide cannot cross any other optical waveguide or any detector to avoid inducing significant power loss caused by a discontinuity at the intersection. Therefore, if an optical interconnect cross any other optical interconnect, the optical interconnect is left as an electrical interconnect. This is the only difference from the single-layer routing problem.

Figure 47 shows the optical data path routing algorithm based on maze routing algorithm.

Algorithm 6.4. Optical Data Path Routing Algorithm

```
1.  Set Breakpoint where optical interconnect is dominant over
    electrical interconnect;
2.  Sort the electrical interconnect by their lengths;
3.  i = 0;
4.  Make two grids in the memory;
5.  Place optical transmitters and receivers in grid 1;
6.  while (interconnect_Length[i] >= Breakpoint) {
7.      condition_1 = Find_Nearest_Transmitter();
8.      condition_2 = Find_Nearest_Receiver();
9.      if (condition_1 == true)&&(condition_2 == true)) {
10.         condition_3 = Optical_Path_Forward_Routing(i);
11.         if (condition_3 == true) {
12.             Optical_Path_Back_Trace(i);
13.             Make_Optical_Bendings(i);
14.         }
15.         Make_Grid_2_Zero();
16.     }
17.     i++;
18. }
19. Minimize_Number_Bending(for all optical interconnects);
20. Maximize_Bending_Radius(for all optical interconnects);
```

Figure 47. Optical data path routing algorithm based on maze routing algorithm

First of all, all the electrical interconnects are sorted by their lengths. Longest electrical interconnects are about to be replaced because they are the keys to determine the performance of SOPs.

Second of all, a nearest optical transmitter from the electrical output port and a nearest optical receiver from the electrical input port are sought. If they are found, the electrical interconnect can be replaced with optical interconnect based on maze routing algorithm which are shown in Figure 48 and Figure 49.

Algorithm 6.5. Optical Data Path Forward Routing Algorithm

```
1.  path_exist = false;
2.  Grid[original_x, original_y] = 1;
3.  tempX = original_x;
4.  tempY = original_y;
5.  while (path_exist == false)
6.  {
7.      x = tempX; y = tempY; z = Grid[x, y];
8.      if (!path_exist) explore(x+1, y); // East
9.      if (!path_exist) explore(x-1, y); // West
10.     if (!path_exist) explore(x, y+1); // South
11.     if (!path_exist) explore(x, y-1); // North
12. }
13. return path_exist;
```

Figure 48. Optical data path forward routing algorithm

Algorithm 6.6. Optical Data Path Back Trace Algorithm

```
1.  index = 0;
2.  retrace = Grid[targetX, targetY];
3.  if (retrace > 2) {
4.     x = targetX; y = targetY;
5.     Route[index].X = targetX; Route[index].Y = targetY;
6.     while (retrace > 1) {
7.           if (Grid[x+1, y] == (retrace-1)) {
8.                 x++; retrace--; index++;
9.                 Route[index].X = x; Route[index].Y = y;
10.          }
11.          else if (Grid[x-1, y] == (retrace-1)) {
12.                x--; retrace--; index++;
13.                Route[index].X = x; Route[index].Y = y;
14.          }
15.          else if (Grid[x, y+1] == (retrace-1)) {
16.                y++; retrace--; index++;
17.                Route[index].X = x; Route[index].Y = y;
18.          }
19.          else if (Grid[x, y-1] == (retrace-1)) {
20.                y--; retrace--; index++;
21.                Route[index].X = x; Route[index].Y = y;
22.          }
23.    }
24. }
```

Figure 49. Optical data path back trace algorithm

Next, bending direction should be determined. In this algorithm, there are eight types of bending direction, which are from left to up, from left to down, from right to up, from right to up, from up to left, from up to right, from down to left and from down to right. It helps to layout after optimization process. The algorithm is shown in Figure 50.

Algorithm 6.7. Optical Interconnect Bending Determination Algorithm

```
// Bending_Direction
// 'A' : LEFT -> UP
// 'B' : RIGHT -> UP
// 'C' : LEFT -> DOWN
// 'D' : RIGHT -> DOWN
// 'E' : DOWN -> RIGHT
// 'F' : UP -> RIGHT
// 'G' : DOWN -> LEFT
// 'H' : UP -> LEFT
1.  opticalnets.Location[NumOpticalNets].X = Route[index].X;
2.  opticalnets.Location[NumOpticalNets].Y = Route[index].Y;
3.  NumOpticalNets++; // Number of Optical nets
4.  index = number of bending;
5.  while (index > 1) {
6.     index--;
7.     if ((Route[index].X == Route[index-1].X)&&(Route[index].Y ==
    Route[index+1].Y)) { // A ~ D
8.           opticalnets.Location[NumOpticalNets].X = Route[index].X;
9.           opticalnets.Location[NumOpticalNets].Y = Route[index].Y;
10.          if (Route[index].X > Route[index+1].X) { // Left ->
```

Figure 50. Pseudo code for determining each bending radius of optical interconnects

```
11.                 if (Route[index].Y > Route[index-1].Y) // -> Up
12.                         Bending.Direction[NumOpticalNets] = 'A';
13.                 else // -> Down
14.                         Bending.Direction[NumOpticalNets] = 'C';
15.         }
16.         else if (Route[index].X < Route[index+1].X){  // Right ->
17.                 if (Route[index].Y > Route[index-1].Y) // -> Up
18.                         Bending.Direction[NumOpticalNets] = 'B';
19.                 else // -> Down
20.                         Bending.Direction[NumOpticalNets] = 'D';
21.         }
22.         opticalnets.Radius[NumOpticalNets] = 1;
23.         NumOpticalNets++;
24. }
25. else if ((Route[index].Y == Route[index-1].Y)&&(Route[index].X ==
            Route[index+1].X)) { // E ~ H
26.         opticalnets.Location[NumOpticalNets].X = Route[index].X;
27.         opticalnets.Location[NumOpticalNets].Y = Route[index].Y;
28.         if (Route[index].Y > Route[index+1].Y) {  // Up ->
29.                 if (Route[index].X < Route[index-1].X) // -> Right
30.                         Bending.Direction[NumOpticalNets] = 'F';
```

Figure 50. Pseudo code for determining each bending radius of optical interconnects (Continued)

```
31.                 else // -> Left
32.                         Bending.Direction[NumOpticalNets] = 'H';
33.         }
34.         else if (Route[index].Y < Route[index+1].Y) { // Down ->
35.                 if (Route[index].X < Route[index-1].X) // -> Right
36.                         Bending.Direction[NumOpticalNets] = 'E';
37.                 else // -> Left
38.                         Bending.Direction[NumOpticalNets] = 'G';
39.         }
40.         opticalnets.Radius[NumOpticalNets] = 1;
41.         NumOpticalNets++;
42.   }
43. }
44. opticalnets.Location[NumOpticalNets].X = Route[index-1].X;
45. opticalnets.Location[NumOpticalNets].Y = Route[index-1].Y;
46. opticalnets.NumOpticalNets++;
```

Figure 50. Pseudo code for determining each bending radius of optical interconnects (Continued)

Finally, number of bending is minimized and bending radius is maximized. However, the two minimization and maximization processes are also optimization problems. It translates that they require other optimization algorithms and take long time to simulate. Therefore, the two processes are roughly optimized in the simulation.

In Section 4.3, the minimum bending radius of optical waveguide which doesn't have bending loss is around 100μm. During routing optical waveguide interconnects, bending radius should be at least 100μm and the number of optical waveguide bending should also be minimized.

6.6 Results and Analysis

The CAD tool is written in C# under .NET environment. For the simulation, 16 GSRC and 5 MCNC benchmark circuits were used.

Figure 51 shows a layout with 50 modules after area-driven optimization process.

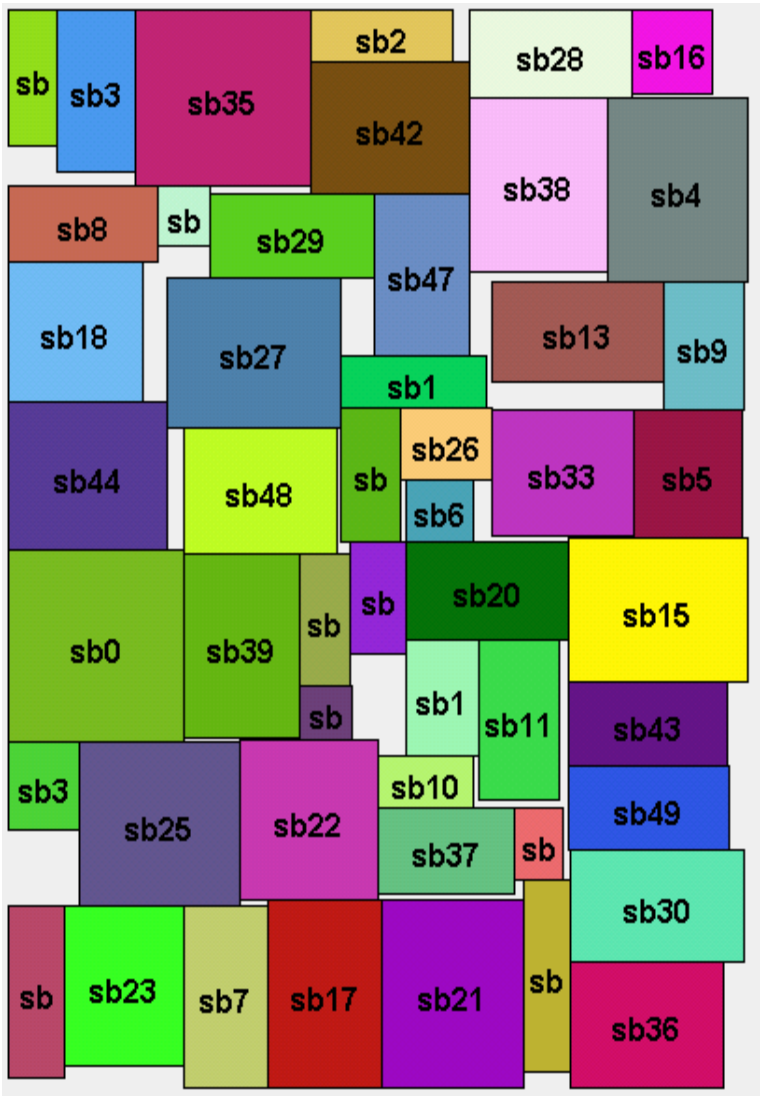


Figure 51. GSRC benchmark circuit with 50 modules after area-driven optimization

Figure 52 shows a layout with 50 modules after interconnect-driven optimization process. Compared to Figure 51, Figure 52 layout area is larger because it is optimized by total interconnect lengths.

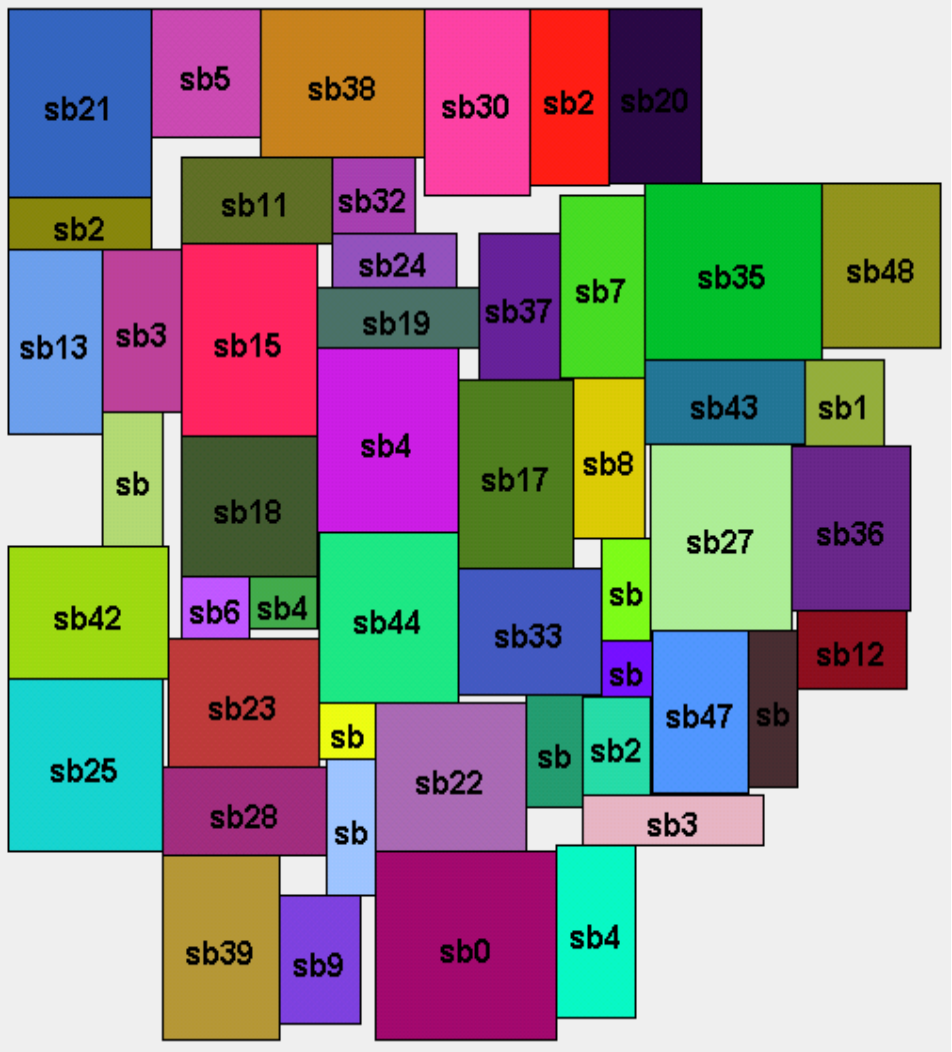


Figure 52. GSRC benchmark circuit with 50 modules after interconnect-driven optimization

Table 8 shows the optimized areas by area- and interconnect-driven optimization. Table entries show the name of the benchmark circuit, system-on-a-package area after area- and interconnect-driven optimization. Comparing with the results in GSRC and MCNC benchmark suites, GHOST provides very competitive results.

Table 8. Simulation results for optimized area by area and total interconnect length

Benchmark	Module name	Area	
		Area-driven	Interconnect-driven
GSRC	n10a	228492	255788
	n10b	233120	264948
	n10c	233859	280630
	n30a	219480	259011
	n30b	209836	239805
	n30c	235626	275423
	n50a	208314	254430
	n50b	215058	242554
	n50c	213744	237500

Table 8. Simulation results for optimized area by area and total interconnect length (Continued)

Benchmark	Module name	Area	
		Area-driven	Interconnect-driven
GSRC	n100a	191376	223826
	n100b	171210	191281
	n100c	181753	210271
	n200a	187264	222717
	n200b	188190	212604
	n200c	183480	204422
	n300	291720	369148
MCNC	ami33	1210770	1536444
	ami49	37632000	39841650
	apte	47078460	51291955
	hp	9144576	10209025
	xerox	20415409	21765946

Table 9 shows results for routing optimization using optical waveguide interconnects. Table entries show the name of the benchmark circuit, the replacement percentage of electrical interconnects with optical interconnects and the percentage improvement in overall performance of system-on-a-package. More than 21% improvement of SOP performance can be achieved using optical interconnects.

Table 9. Simulation results after using optical interconnects

Benchmark	Module name	Optical interconnect (%)	Performance improvement (%)
GSRC	n10a	11.1	24
	n10b	17.2	27
	n10c	15.2	21
	n30a	19.1	23
	n30b	15.0	26
	n30c	13.2	22
	n50a	9.0	31
	n50b	12.2	32
	n50c	10.3	35

Table 9. Simulation results after using optical interconnects (Continued)

Benchmark	Module name	Optical interconnect (%)	Performance improvement (%)
GSRC	n100a	8.4	50
	n100b	9.0	55
	n100c	7.6	58
	n200a	5.8	61
	n200b	6.5	58
	n200c	4.6	54
	n300c	8.9	67
MCNC	ami33	17.0	42
	ami49	11.2	79
	apte	20.4	89
	hp	10.4	50
	xerox	9.0	52

According to the result, using optical interconnect as a substitute of electrical interconnect provides the overall performance improvement of the SOP.

Optimized MCNC benchmark circuits are shown below.

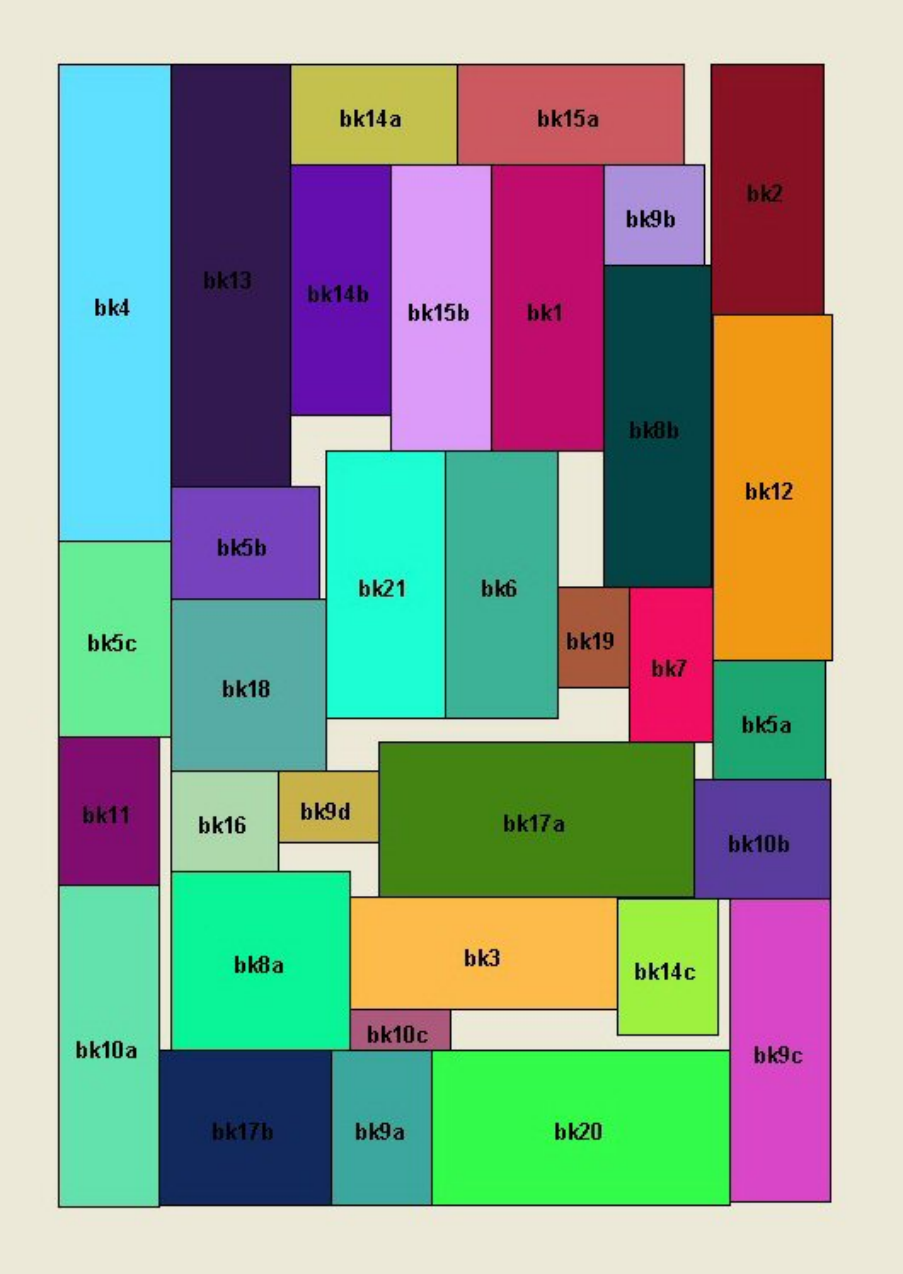


Figure 53. Optimized placement for Ami33 benchmark circuit

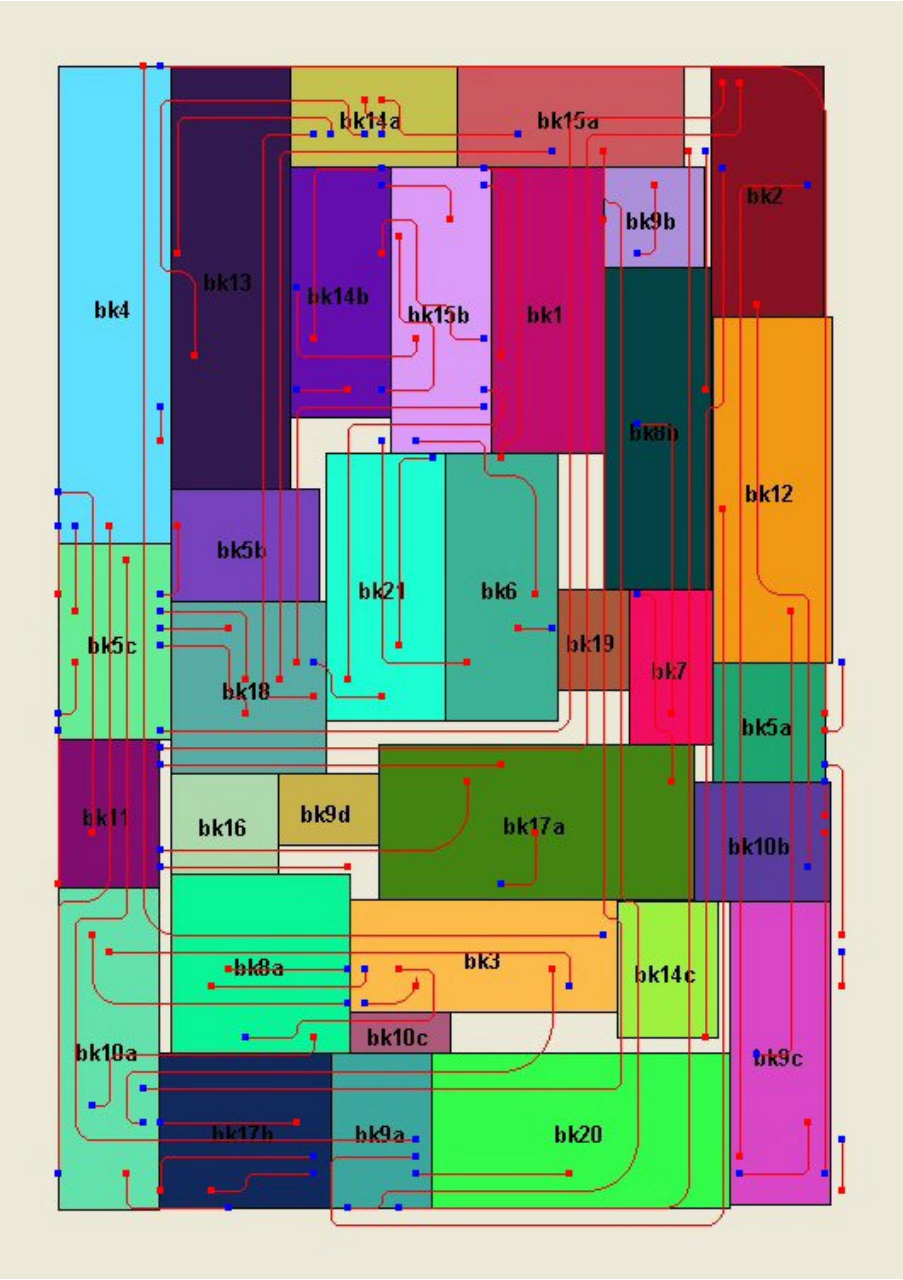


Figure 54. Optimized placement and optical waveguide routing for Ami33 benchmark circuit

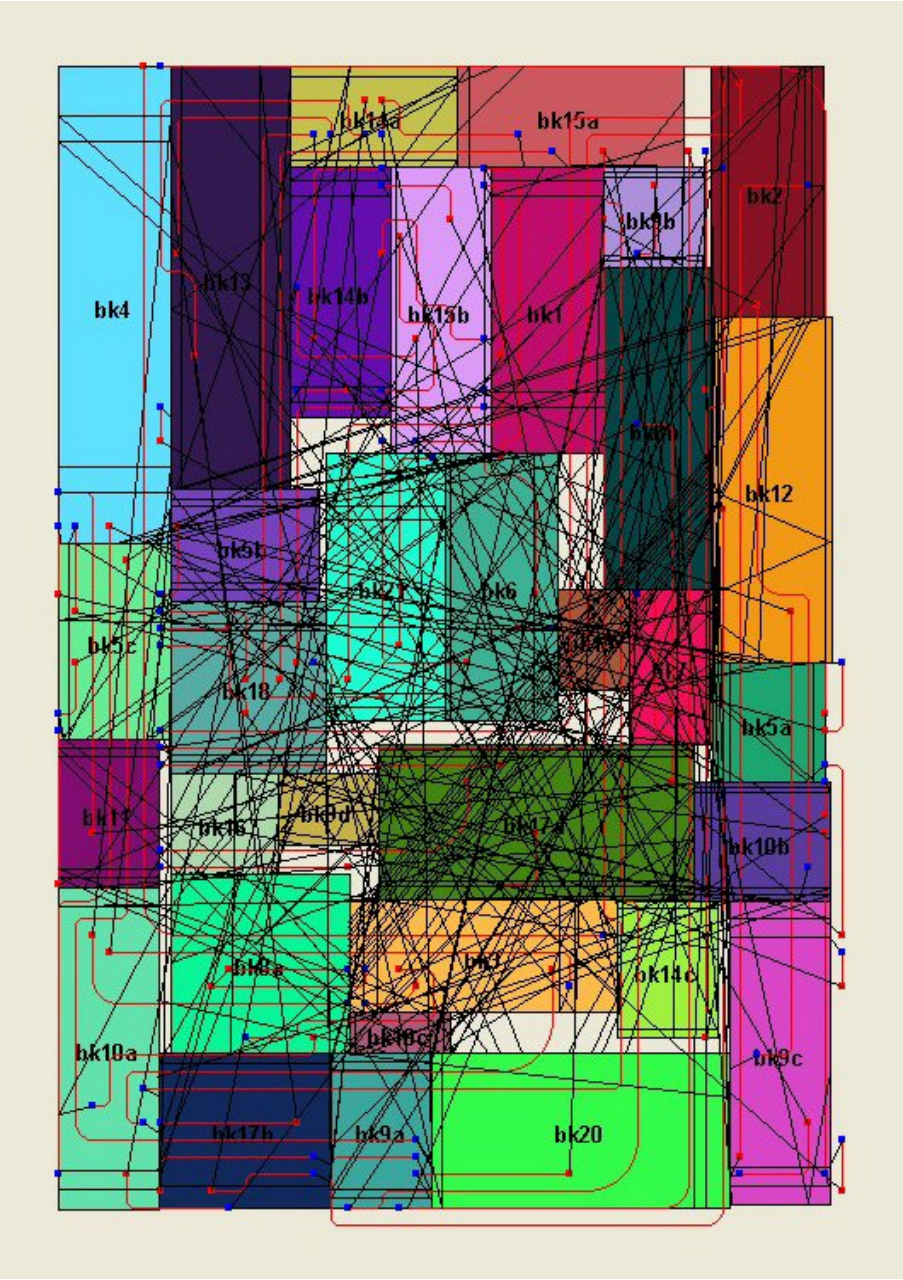


Figure 55. Optimized placement and both electrical and optical waveguide routing for Ami33 benchmark circuit

Figure 56. Optimized placement for Ami49 benchmark circuit

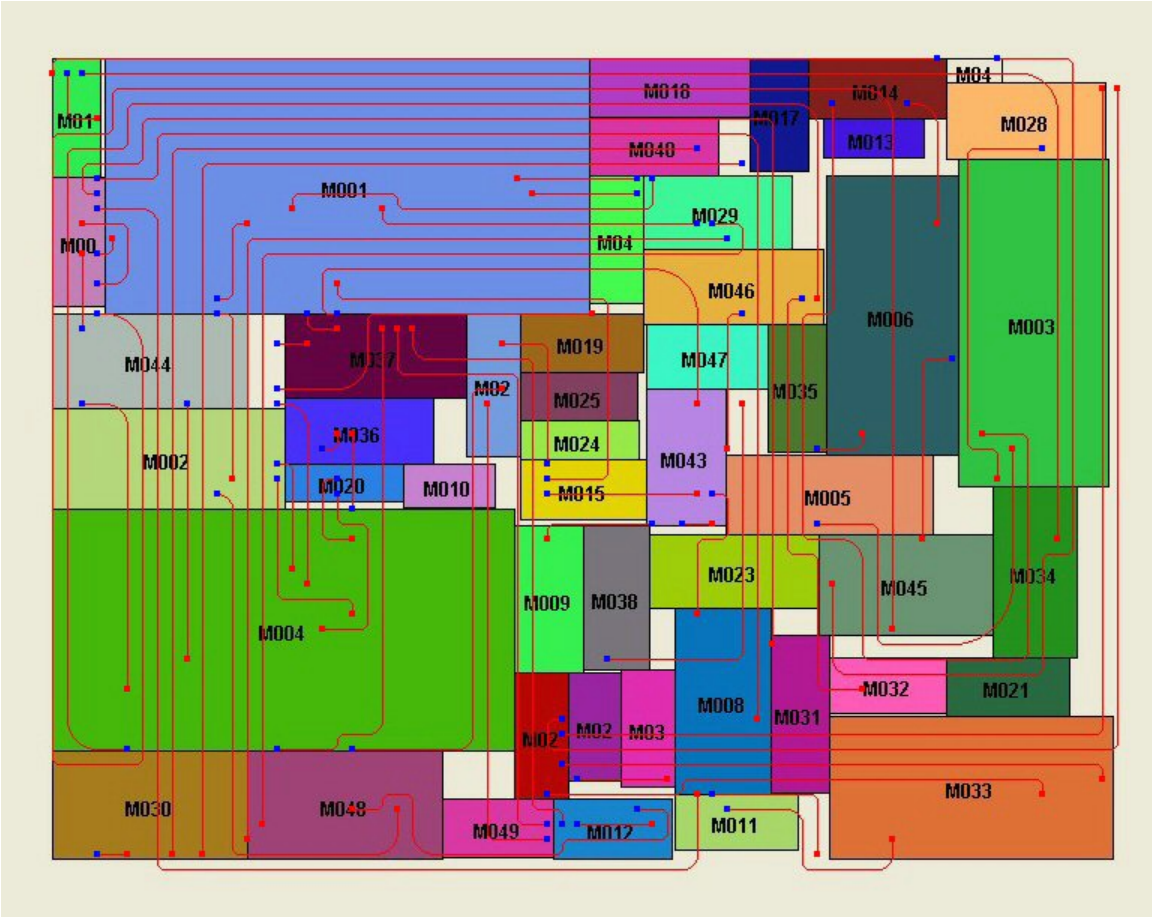


Figure 57. Optimized placement and optical waveguide routing for Ami49 benchmark circuit

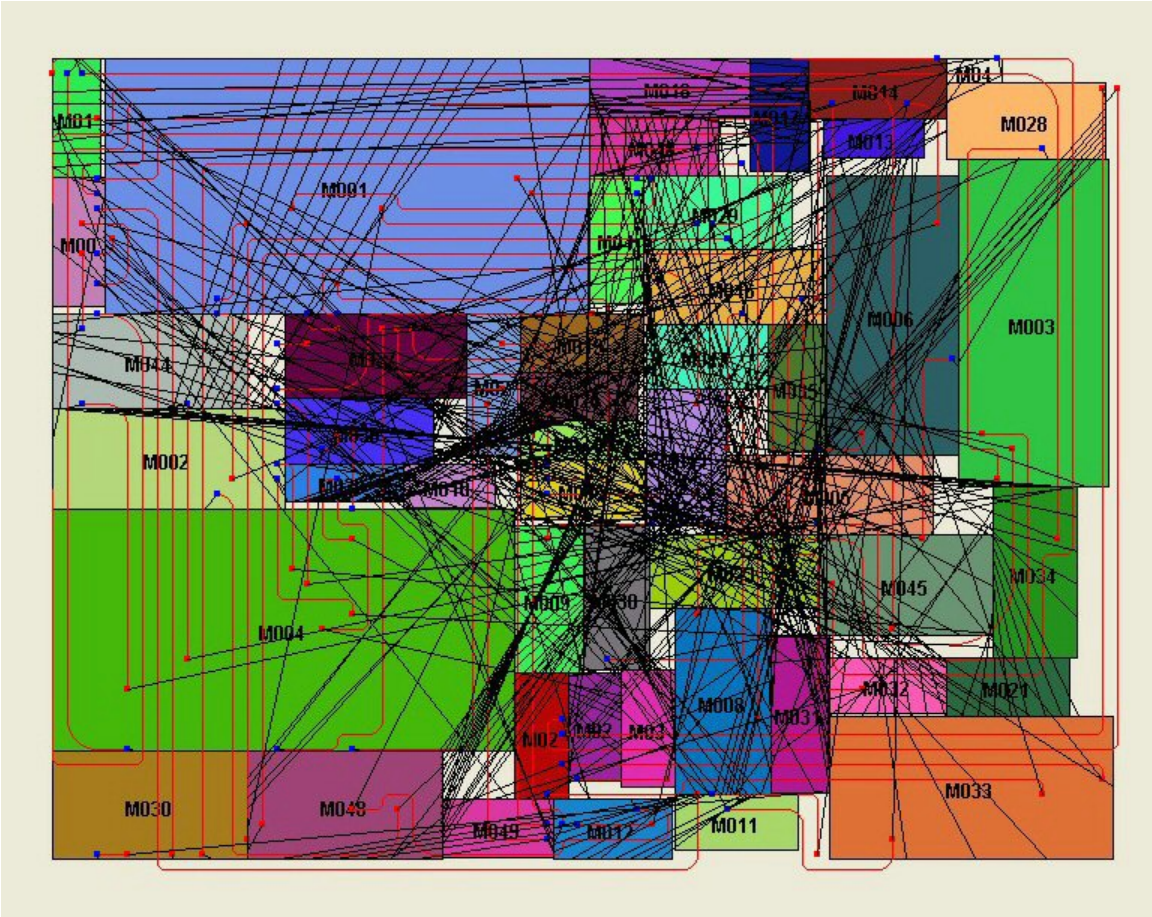


Figure 58. Optimized placement and both electrical and optical waveguide routing for Ami49 benchmark circuit

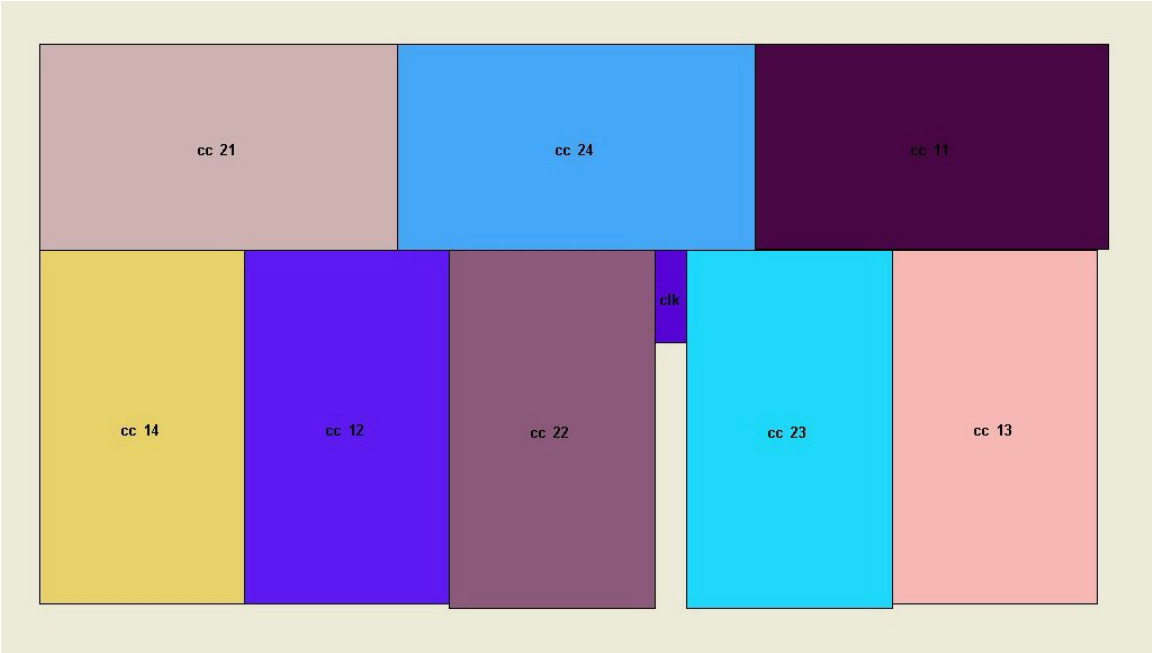


Figure 59. Optimized placement for Apte benchmark circuit

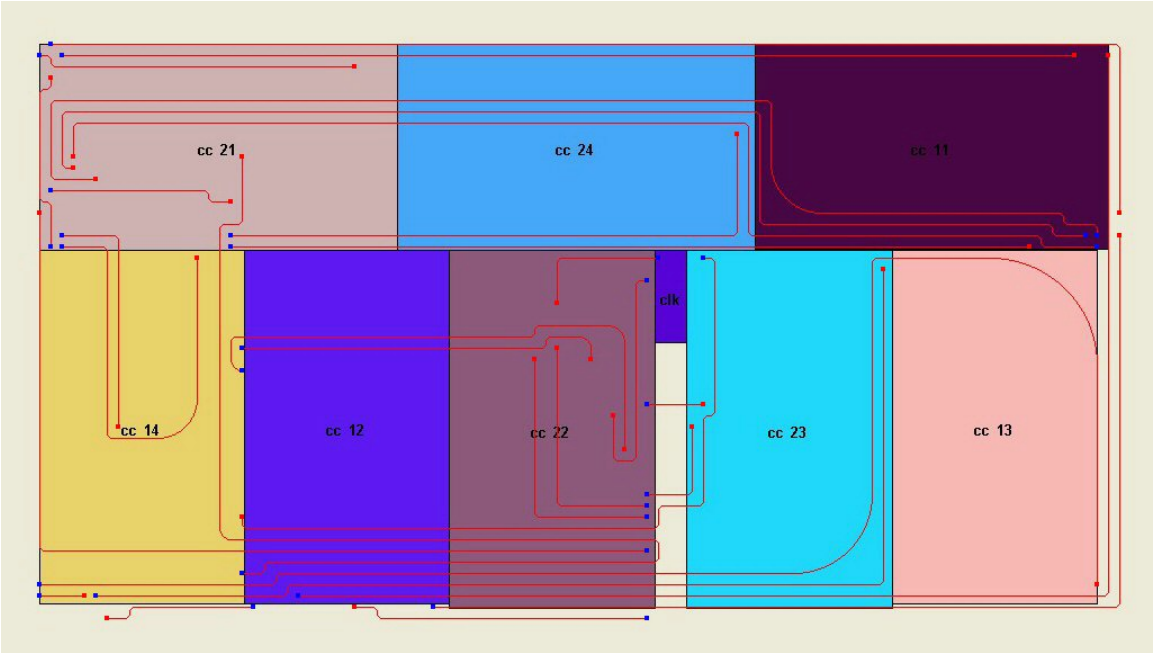


Figure 60. Optimized placement and optical waveguide routing for Apte benchmark circuit

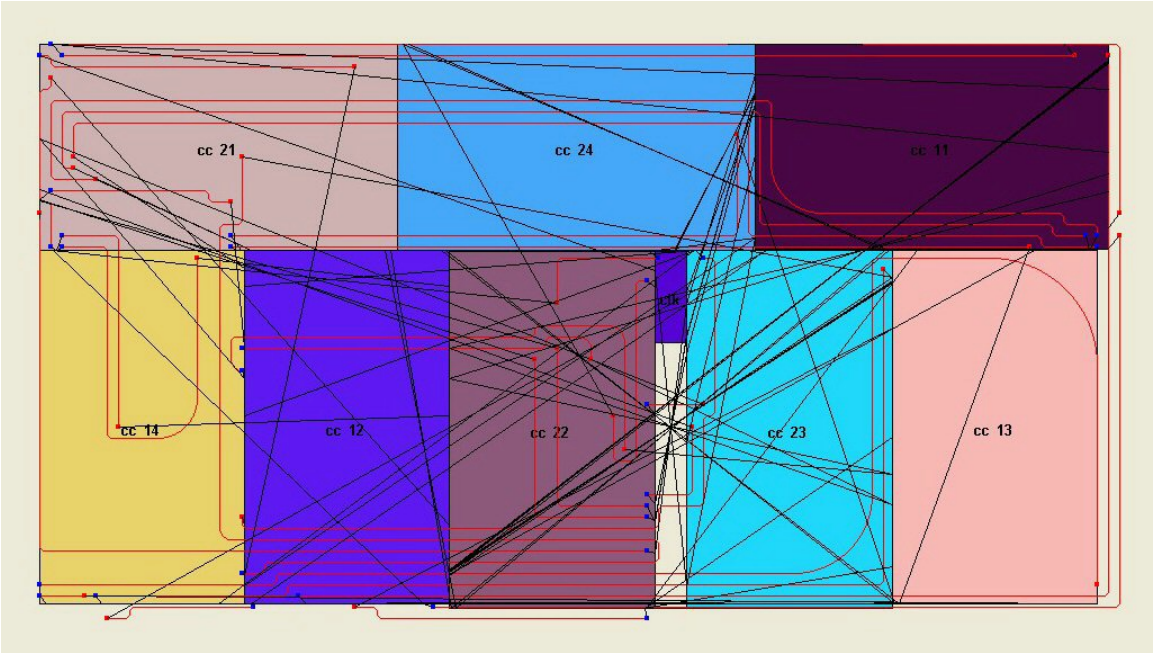


Figure 61. Optimized placement and both electrical and optical waveguide routing for Apte benchmark circuit

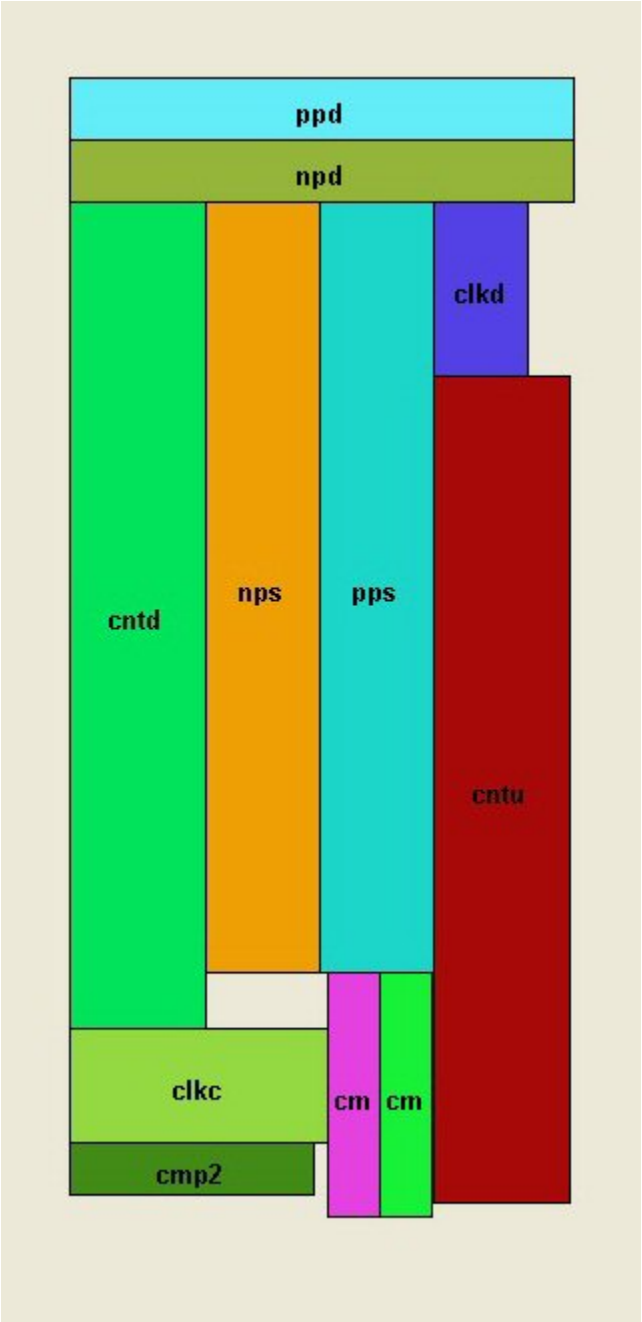


Figure 62. Optimized placement for Hp benchmark circuit

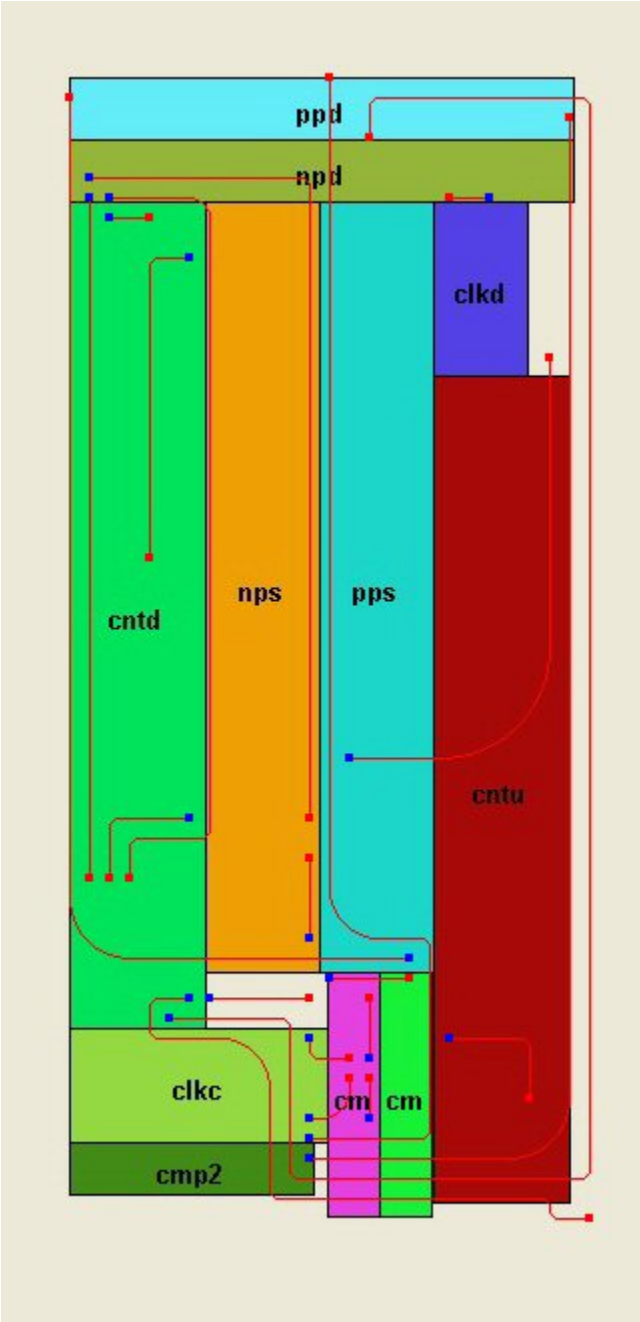


Figure 63. Optimized placement and optical waveguide routing for Hp benchmark circuit

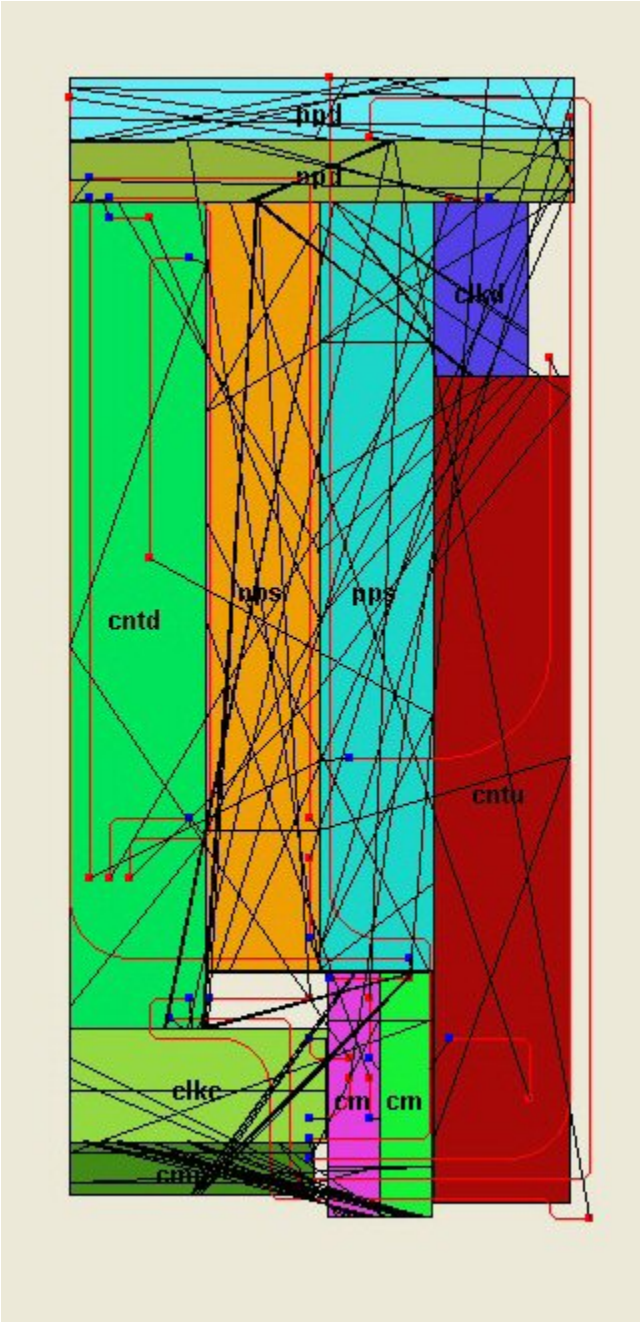


Figure 64. Optimized placement and both electrical and optical waveguide routing for Hp benchmark circuit

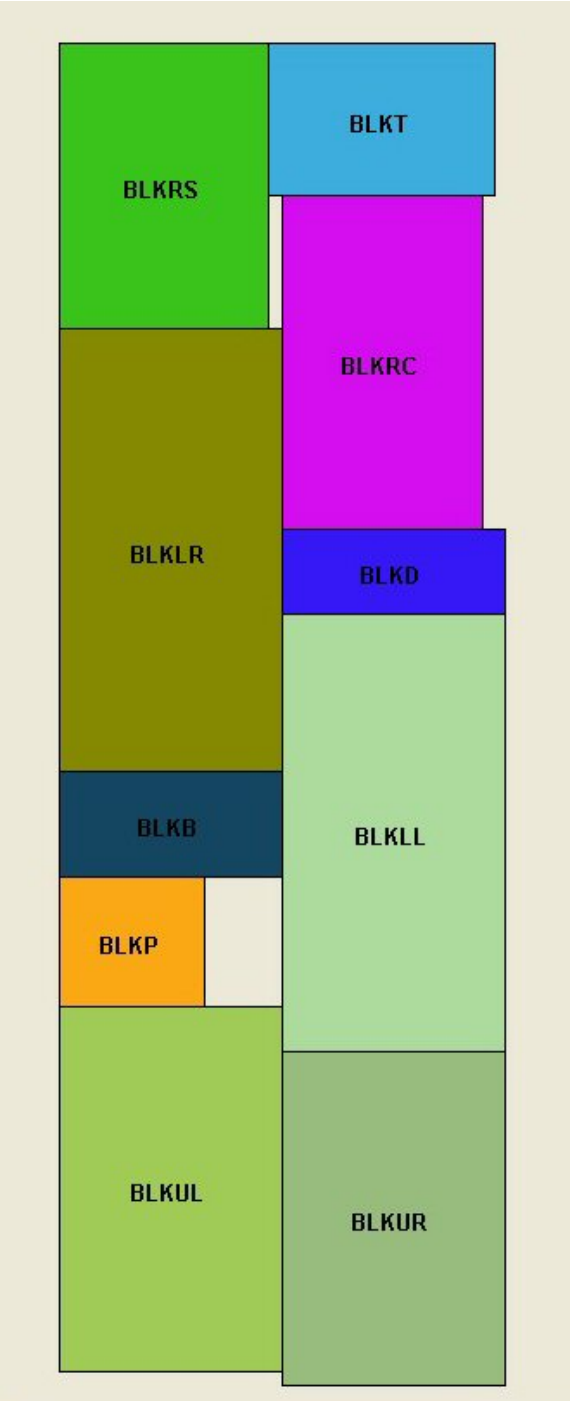


Figure 65. Optimized placement for Xerox benchmark circuit

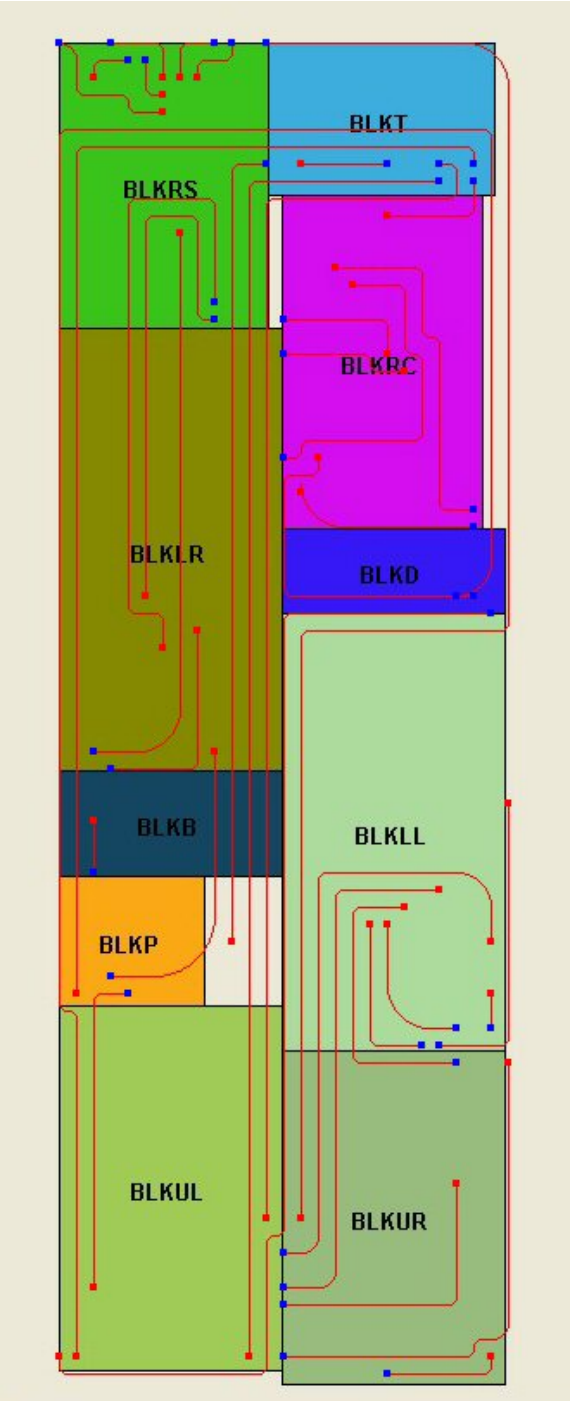


Figure 66. Optimized placement and optical waveguide routing for Xerox benchmark circuit

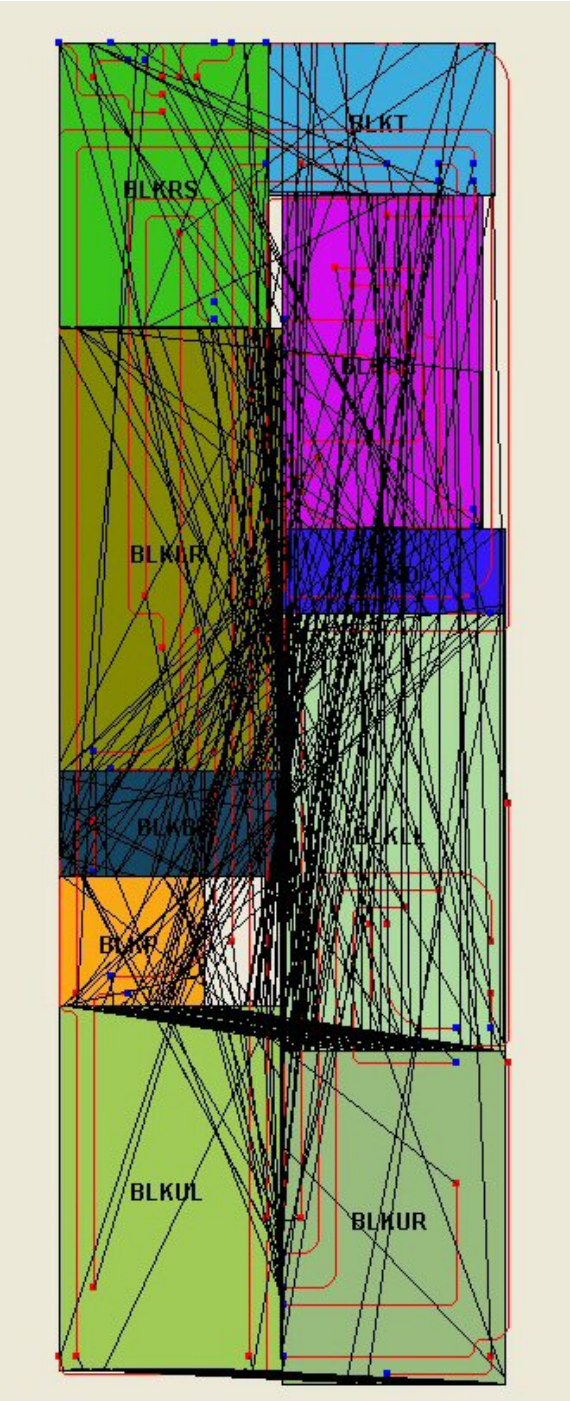


Figure 67. Optimized placement and both electrical and optical waveguide routing for Xerox benchmark circuit

6.7 Summary

In this chapter, we present a new approach to designing optoelectronic system-on-a-package using optical waveguide interconnect. The results show that more than 21% improvement of the SOP performance is obtained using a hybrid genetic algorithm.

Optical interconnect technology is still immature to replace all electrical interconnects because of incompatibility with current electrical technology, signal transformation issues, cost issues, etc. However, optical interconnect technology is a remarkable technology to break through the limitations of electrical interconnect.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

The goal of this dissertation was to develop optical interconnection models and new CAD algorithms using the models for designing optoelectronic systems. Using the constructed models of electrical and optical interconnects, the optoelectronic systems was successfully designed using new CAD algorithms.

Electrical interconnect and free-space optical interconnect for designing SoC have been modeled from the speed and energy consumption point of view. According to the models, free-space optical interconnect is dominant over electrical interconnect for both speed and energy consumption once the interconnect length is over 3cm. Therefore, the CAD tool which takes care of place and route tries to convert electrical interconnects which is longer than 3cm to optical interconnects while optimizing module placement. For the place and route, steady-state genetic algorithm, which keeps better solution in the next generation, is used. As results, more than 55% improvement in overall SoC speed and more than 11% saving in total energy consumption are obtained through the optimization process with the use of free-space optical interconnects. This translates to improve the overall SoC performance by a factor of more than 1.5.

To expand chip or module-level design to board or package-level, optical waveguide interconnect was introduced and modeled. Different from free-space optical interconnect, optical waveguide interconnect has some other consideration, such as inherent optical waveguide losses and optical waveguide bending loss. By deriving the field distribution inside optical waveguide, below equation is obtained by applying a real fabrication parameters.

$$\text{Bending Loss} = [1.0508/(1+e^{(\text{radius}-4\times10^{-5})/10^{-5}})]+9.9\times10^{-4}$$

Additionally, inherent optical waveguide losses are directly obtained by measuring optical waveguide losses using a fiber scanning method. The losses, which include scattering losses, material absorption losses and waveguide structural imperfection losses, are 0.36dB/cm at a wavelength of 1.3μm [32]. However, the splitting loss of optical waveguide is assumed to be negligible in this dissertation. As a reference, B. Bihari, *et al* show that the splitting loss is reduced to 0.4dB per splitter in their experiments. Using this loss model, the design automation algorithm which constructs the optical clock distribution network was developed. It basically minimizes all the path length and minimizes the length differences of each paths so that clock signal flight time is minimized and clock signal skew is minimized. The results show that less than 26.1psec in signal timing skew is obtained for a signal flight time of 614.38psec. This translates that the signal timing skew can be neglected (< 4%). For optical power consumption, about 15% reduction is also obtained over clock nets routed with existing (optical) methods.

Finally, high-performance optoelectronic system-on-a-package is designed utilizing above optical waveguide loss model. In this research, a simulated annealing and a hybrid genetic algorithms are employed for simultaneously optimizing the module block placement and routing problems. Block placement algorithm is based on Sequence-pair algorithm which produces minimum area with compacting modules. Optical data path routing is the single-layer routing problem. Although the fundamental problem in general single-layer problem is to determine if all the interconnects can be routed or not, a slight change is adopted. In this chapter, we attempt to replace electrical interconnects with optical interconnects as many as possible. However, any optical waveguide cannot cross any other optical waveguide or any detector to avoid inducing significant power loss caused by a discontinuity at the intersection. Therefore, if an optical interconnect cross any other optical interconnect, the optical interconnect is left as an electrical interconnect. This is the only difference from the single-layer routing problem. This algorithm is based on maze routing algorithm with minimizing both optical waveguide bending losses and the number of bends in optical waveguide. As the optimization result, more than 47% improvement in the performance of optoelectronic systems is obtained through the use of optical waveguide interconnects.

7.2 Future Work

The demand of high-performance system-on-a-chip/package will increase the need for another emerging interconnect technology other than electrical interconnects. This

dissertation presented new methodologies to design high-performance optoelectronic systems with the proposed models which compared electrical interconnect with optical interconnect from the speed and power consumption point of view.

In this dissertation, it is assumed that the models extracted from papers and a textbook are correct. However, it may not be correct if considering CMOS feature size scaling. As the feature scales down to deep-sub microns (DSM), many unexpected factors come up. In order to design optoelectronic system with DSM technology, those factors should be taken into account.

For place and route algorithm, the objective of this dissertation is either speed maximization or area minimization. However, there are several other optimization problems, such as power minimization, noise reduction, heat sink, etc. These optimization problems should be considered in the future.

APPENDIX A

SIMULATION RESULTS FOR GSRC BENCHMARK

This appendix includes the results of Chapter 6 with GSRC benchmark circuits.

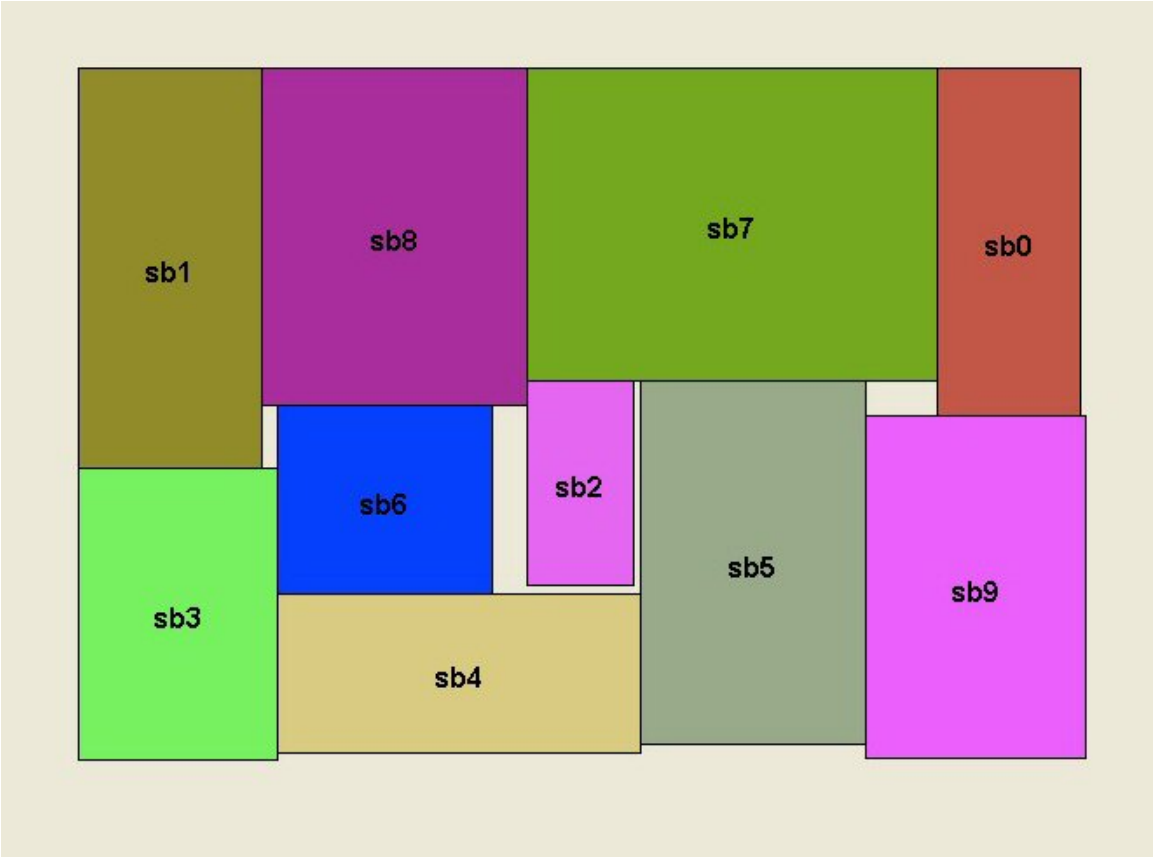


Figure 68. Optimized placement for n10a benchmark circuit

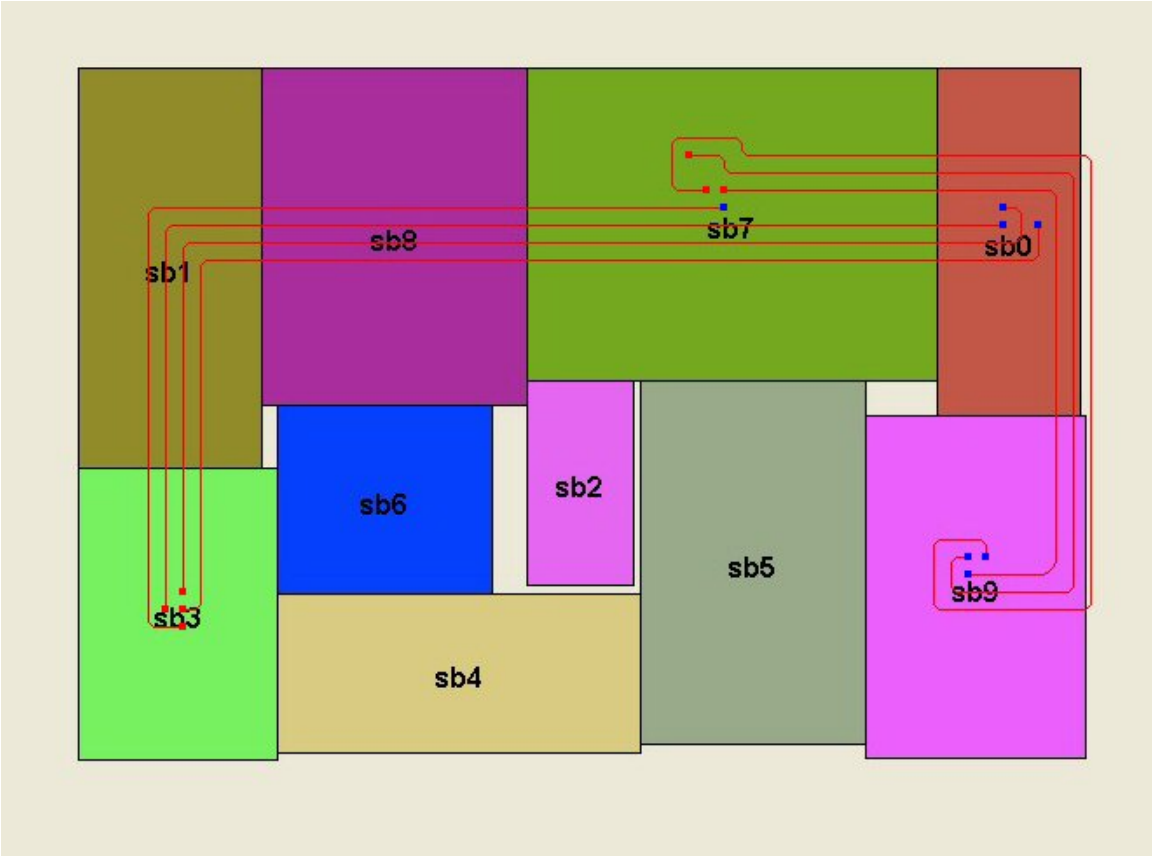


Figure 69. Optimized placement and optical waveguide routing for n10a benchmark circuit

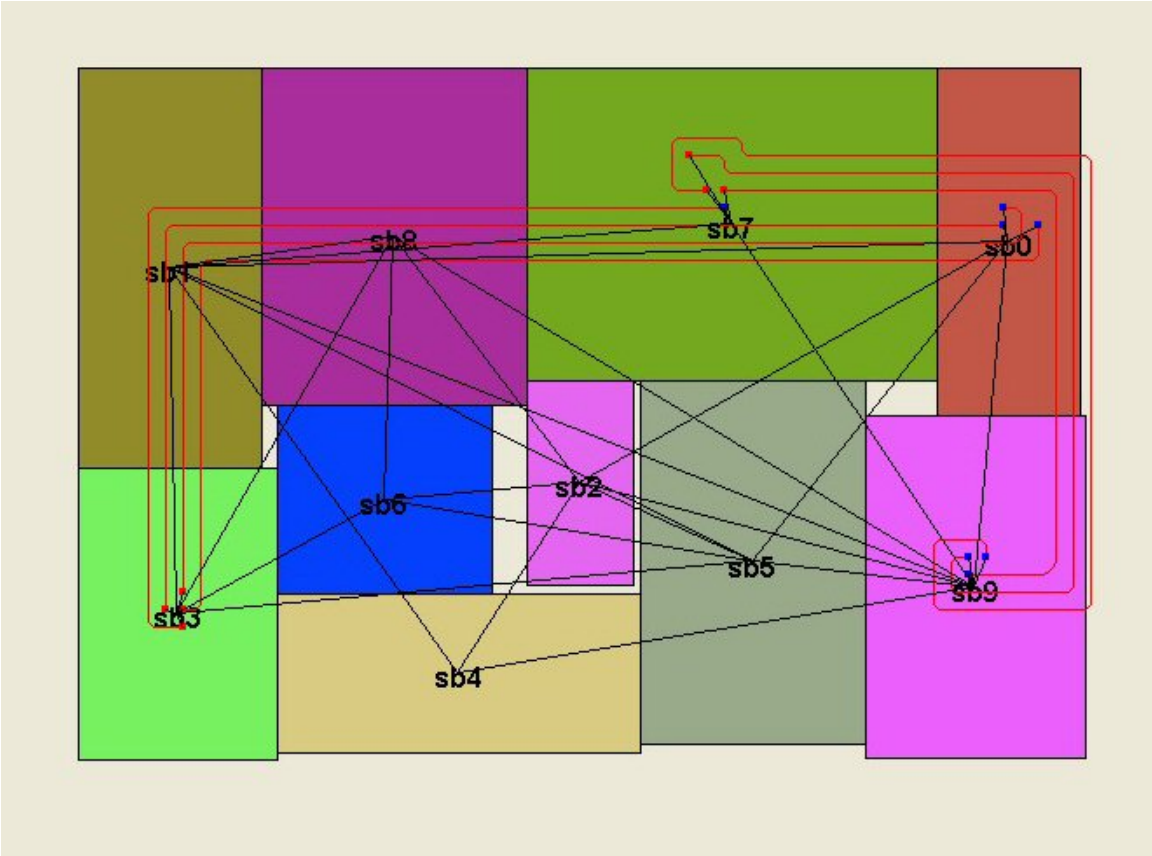


Figure 70. Optimized placement and both electrical and optical waveguide routing for n10a benchmark circuit

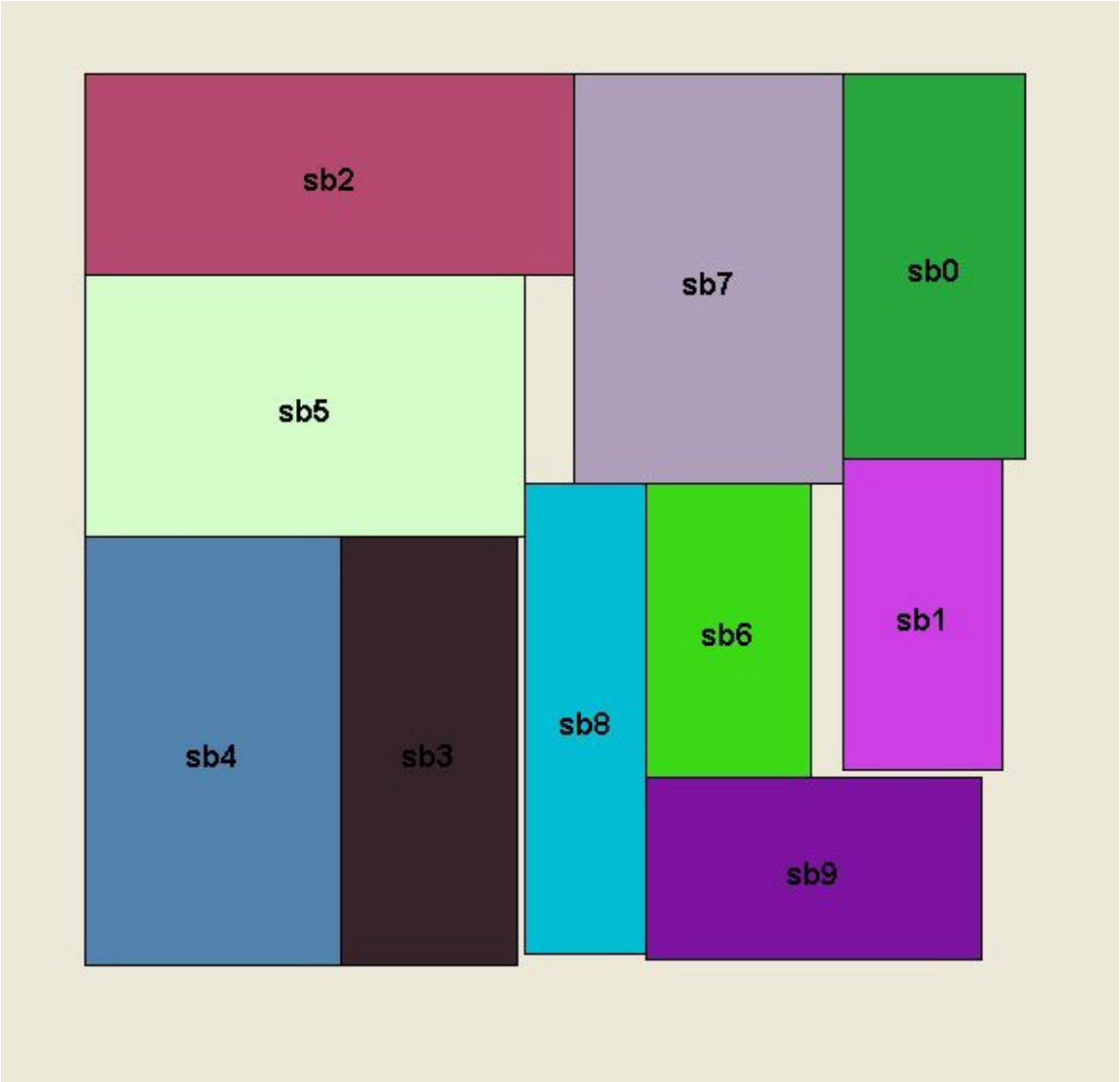


Figure 71. Optimized placement for n10b benchmark circuit

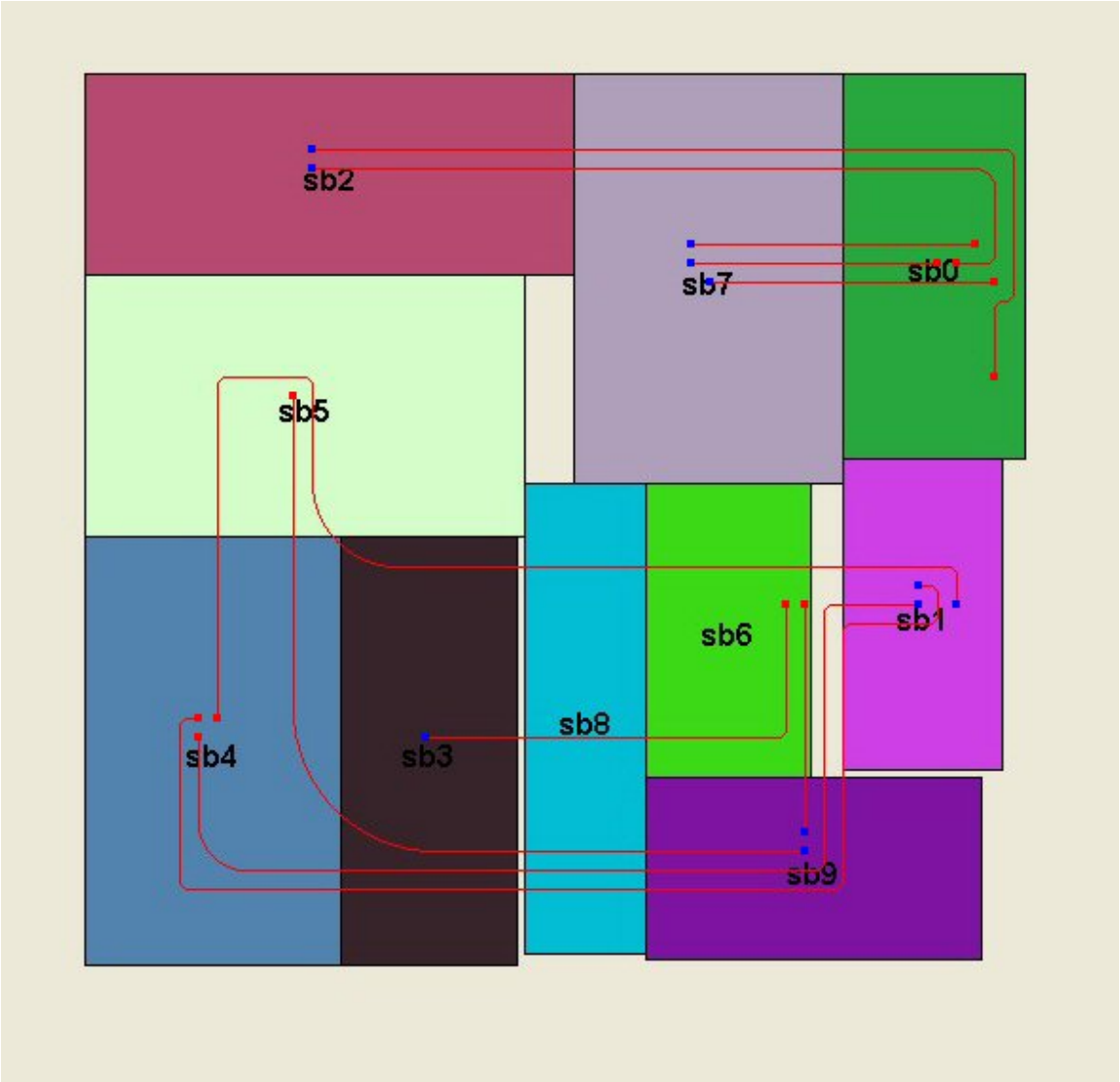


Figure 72. Optimized placement and optical waveguide routing for n10b benchmark circuit

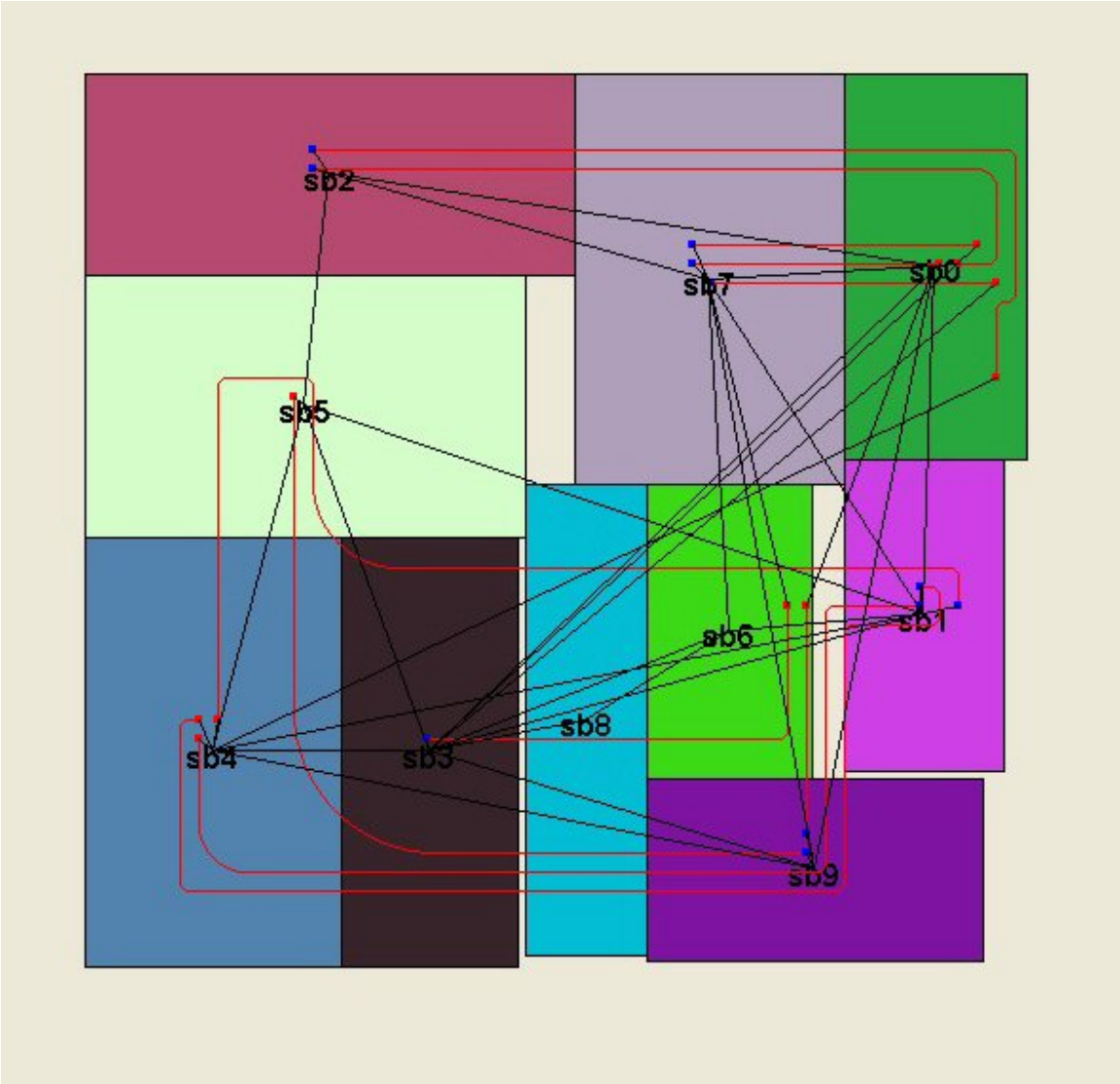


Figure 73. Optimized placement and both electrical and optical waveguide routing for n10b benchmark circuit

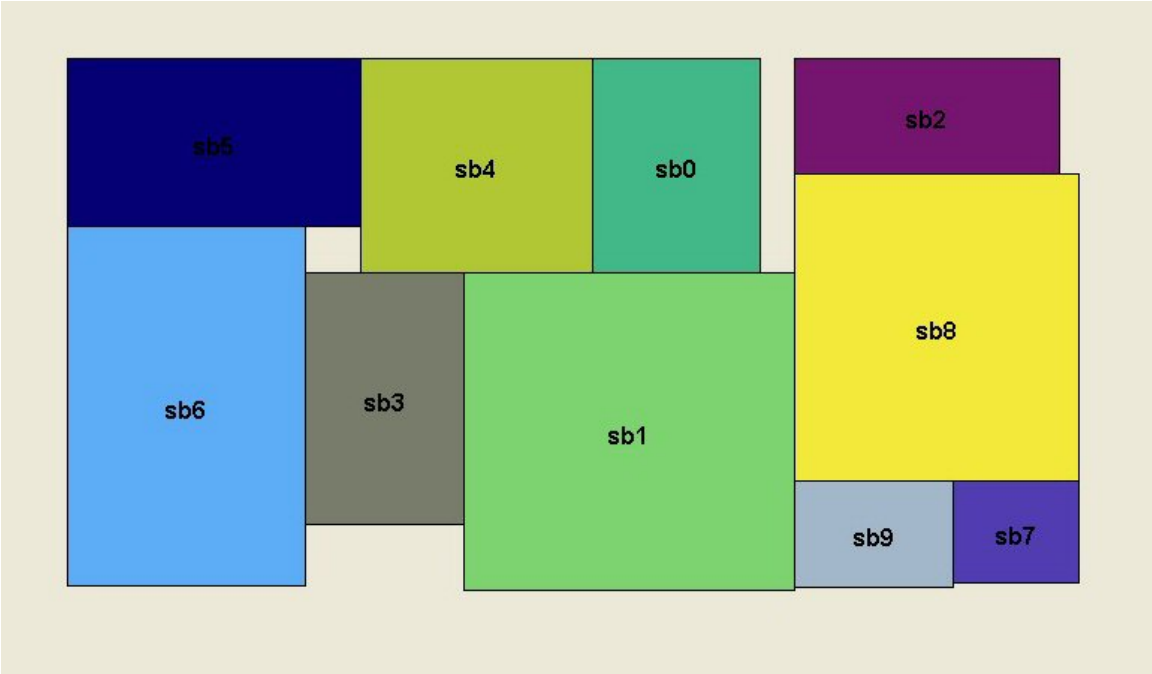


Figure 74. Optimized placement for n10c benchmark circuit

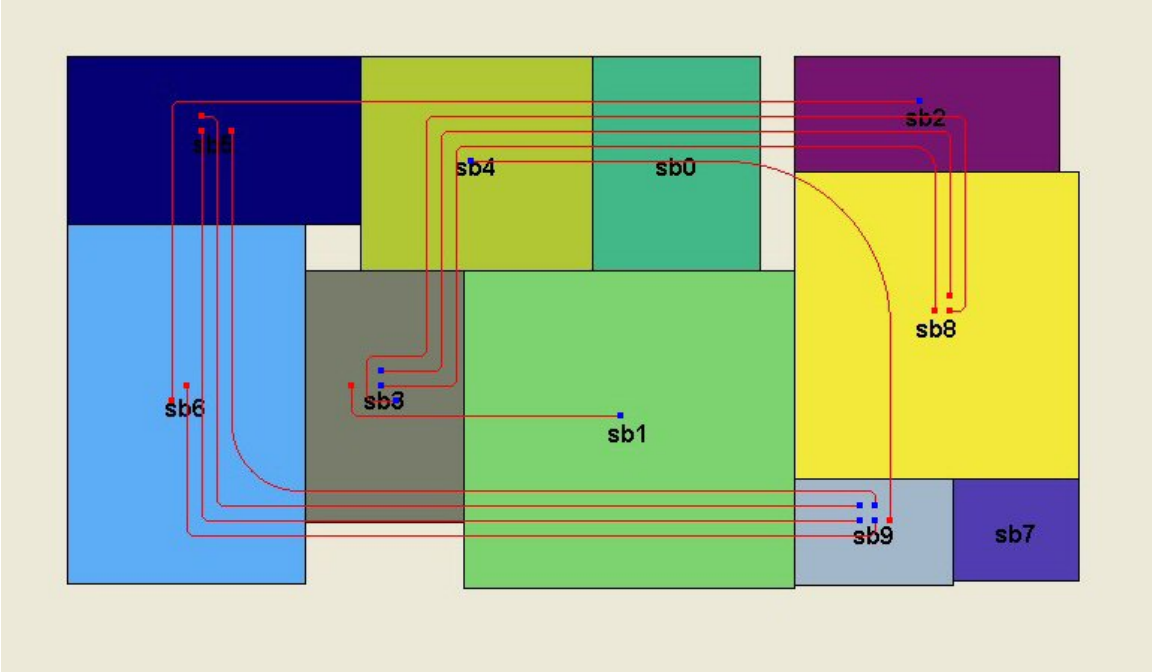


Figure 75. Optimized placement and optical waveguide routing for n10c benchmark circuit

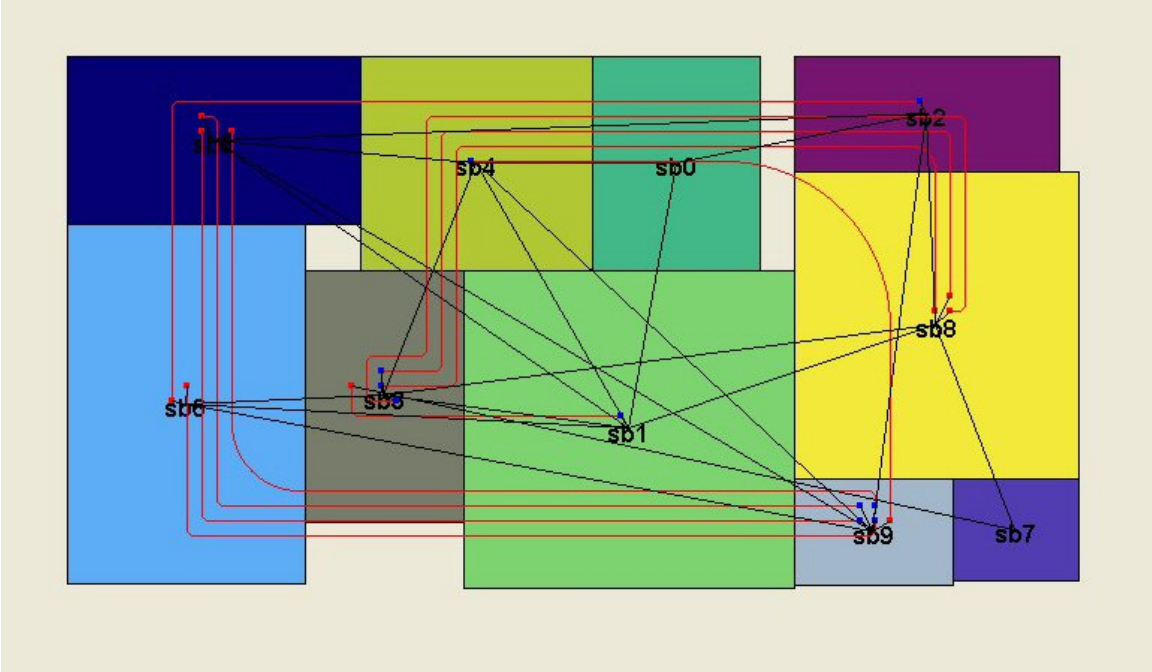


Figure 76. Optimized placement and both electrical and optical waveguide routing for n10c benchmark circuit

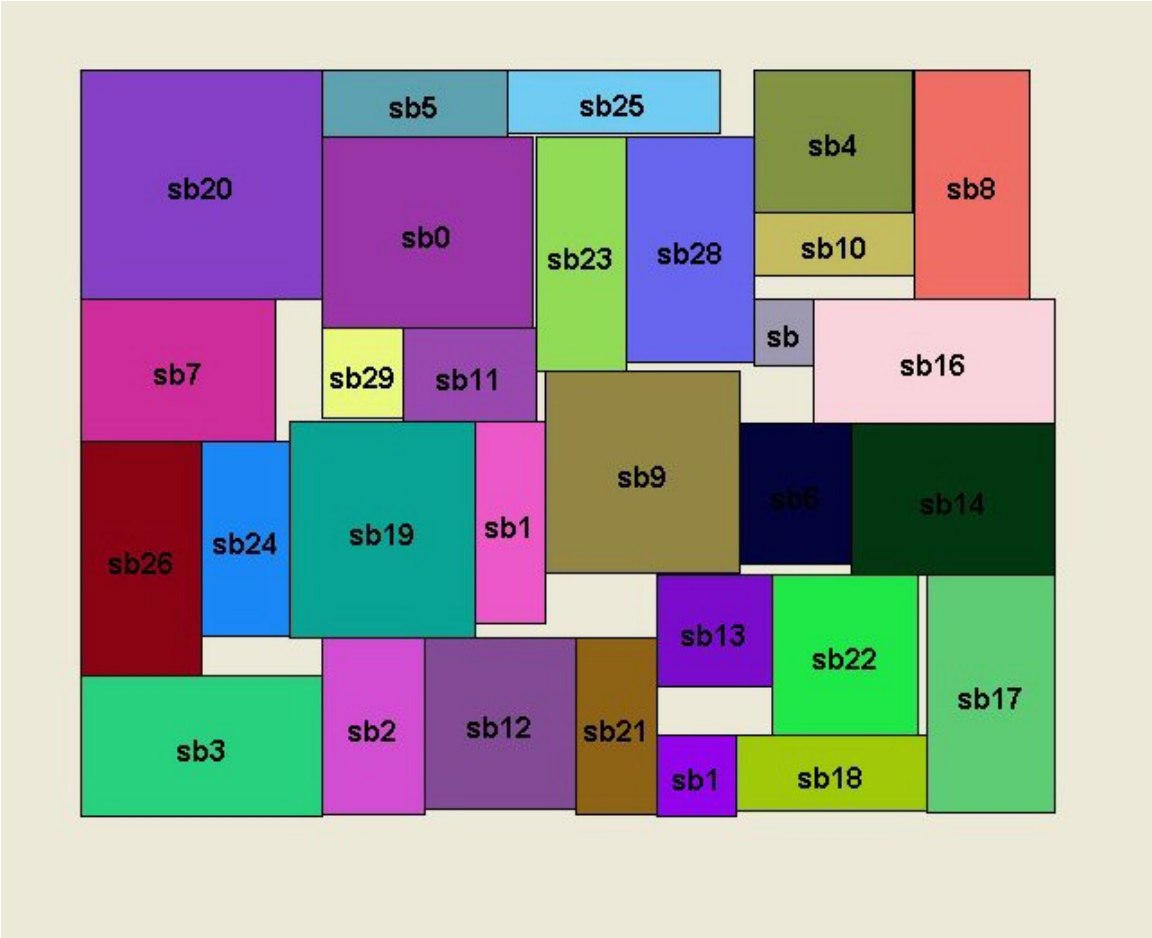


Figure 77. Optimized placement for n30a benchmark circuit

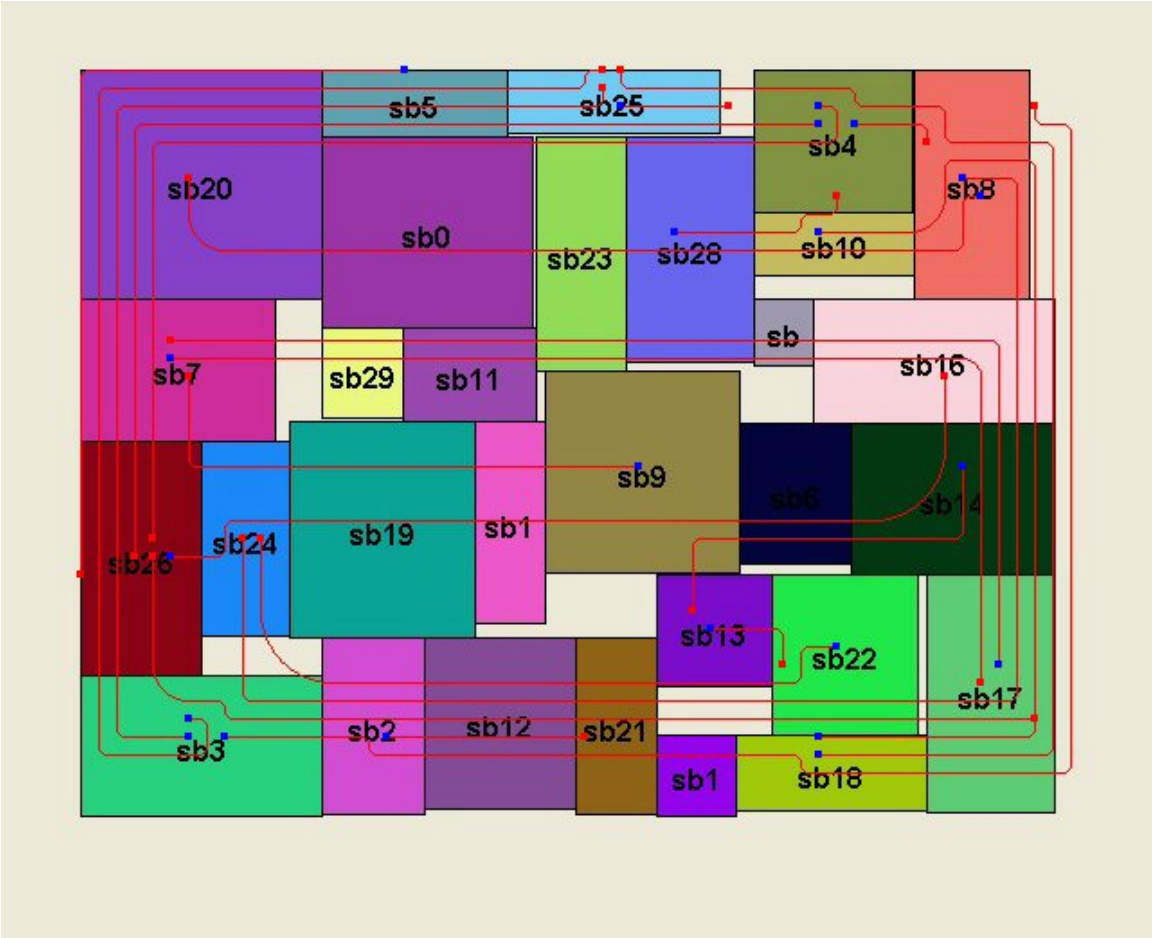


Figure 78. Optimized placement and optical waveguide routing for n30a benchmark circuit

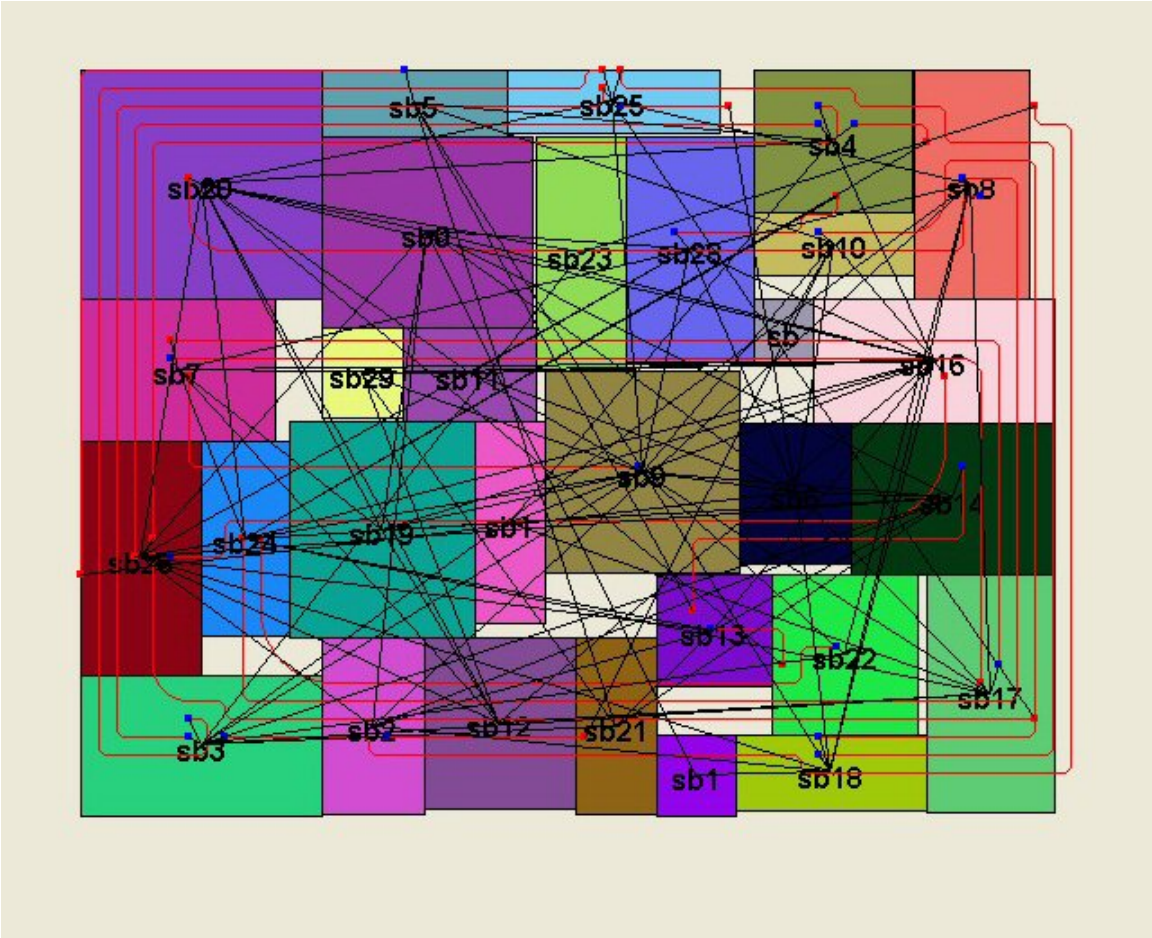


Figure 79. Optimized placement and both electrical and optical waveguide routing for n30a benchmark circuit

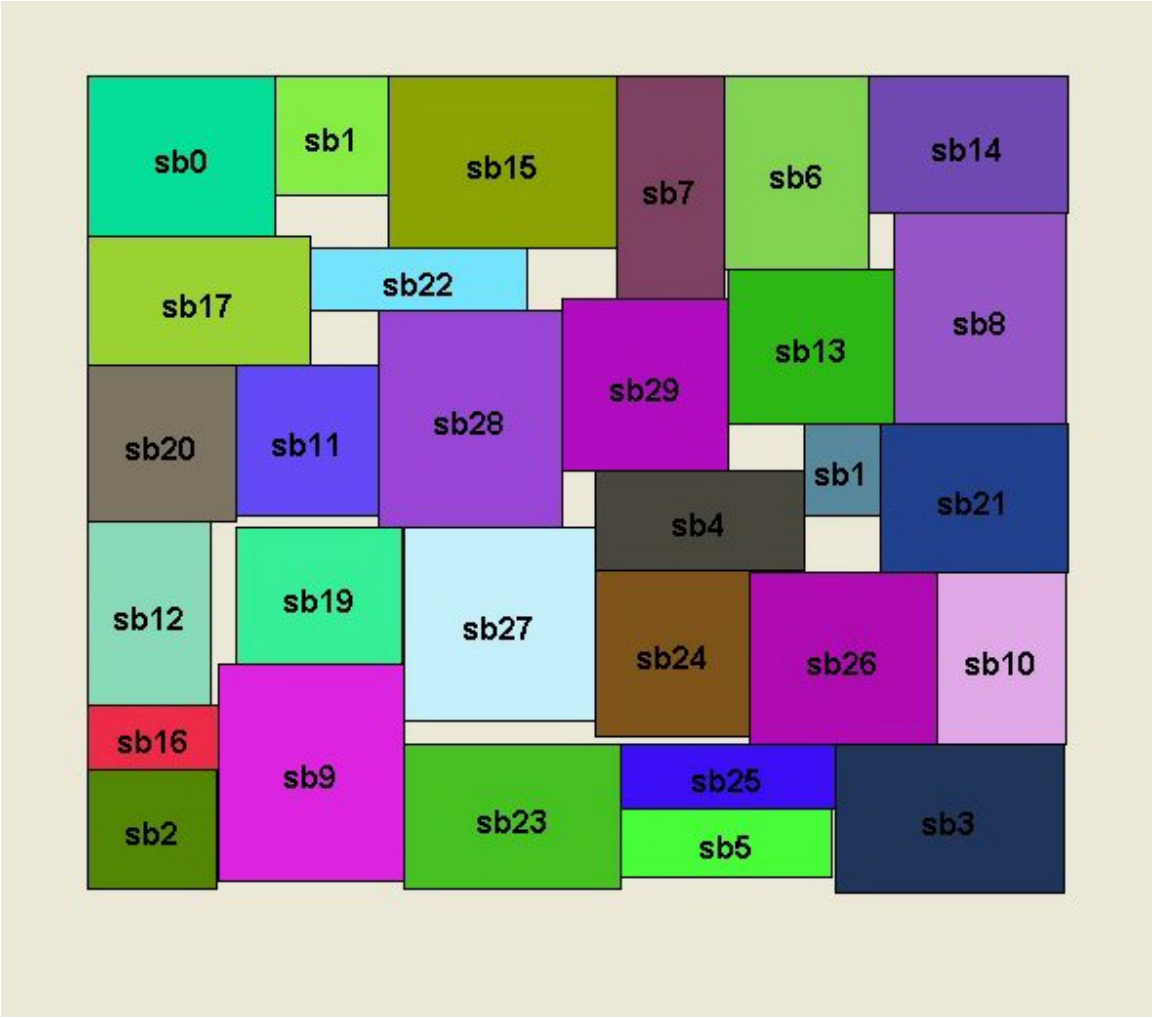


Figure 80. Optimized placement for n30b benchmark circuit

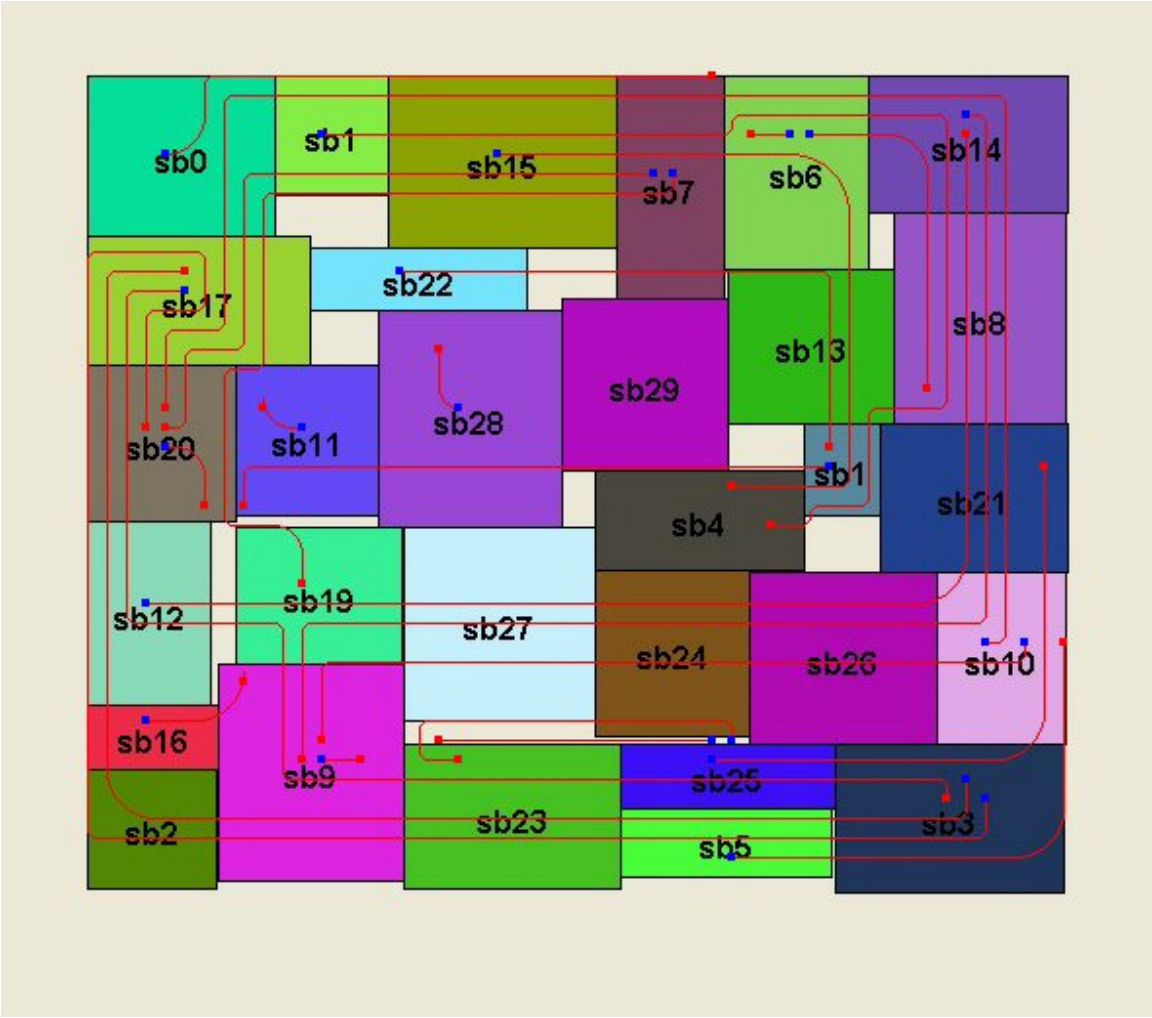


Figure 81. Optimized placement and optical waveguide routing for n30b benchmark circuit

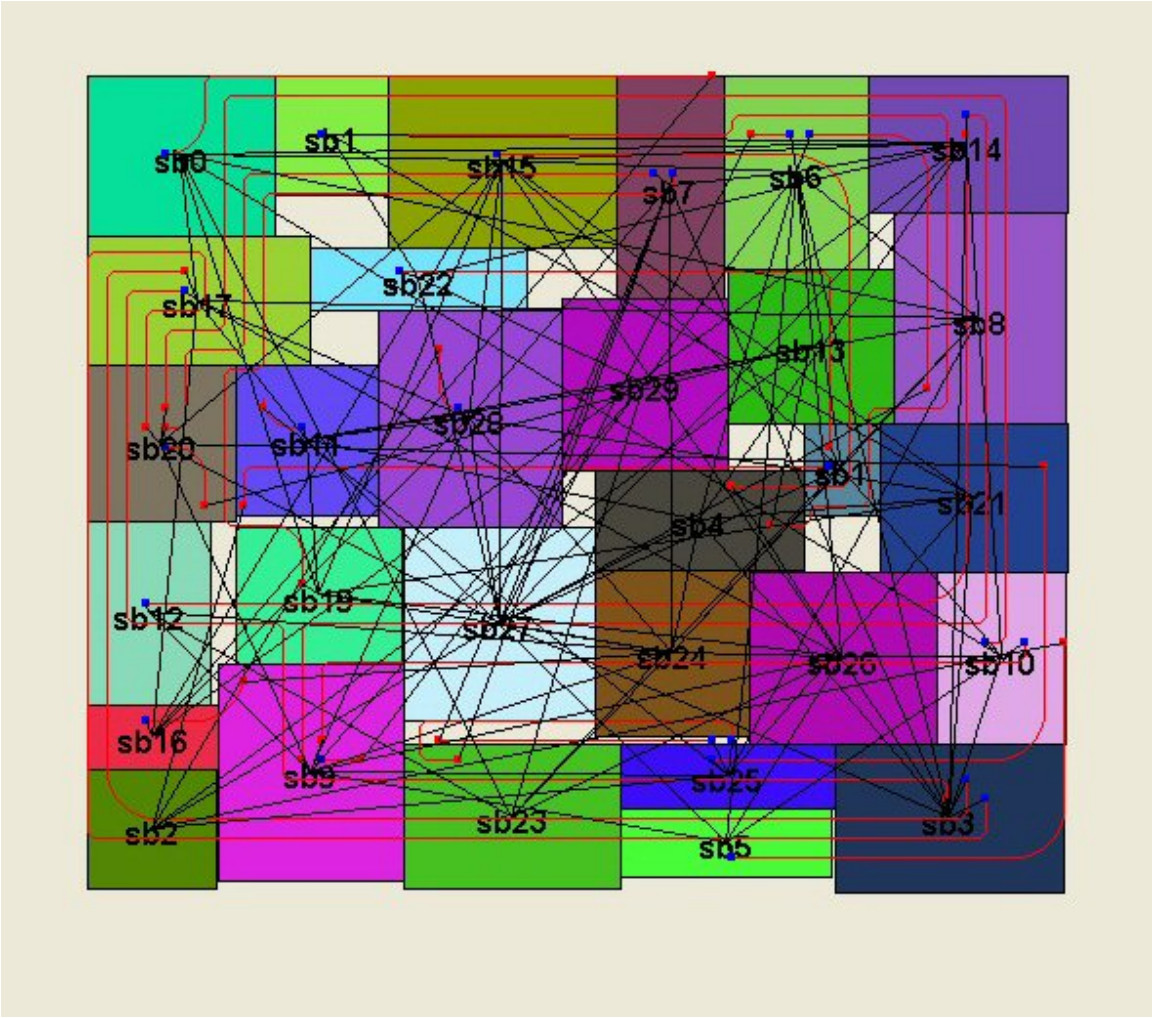
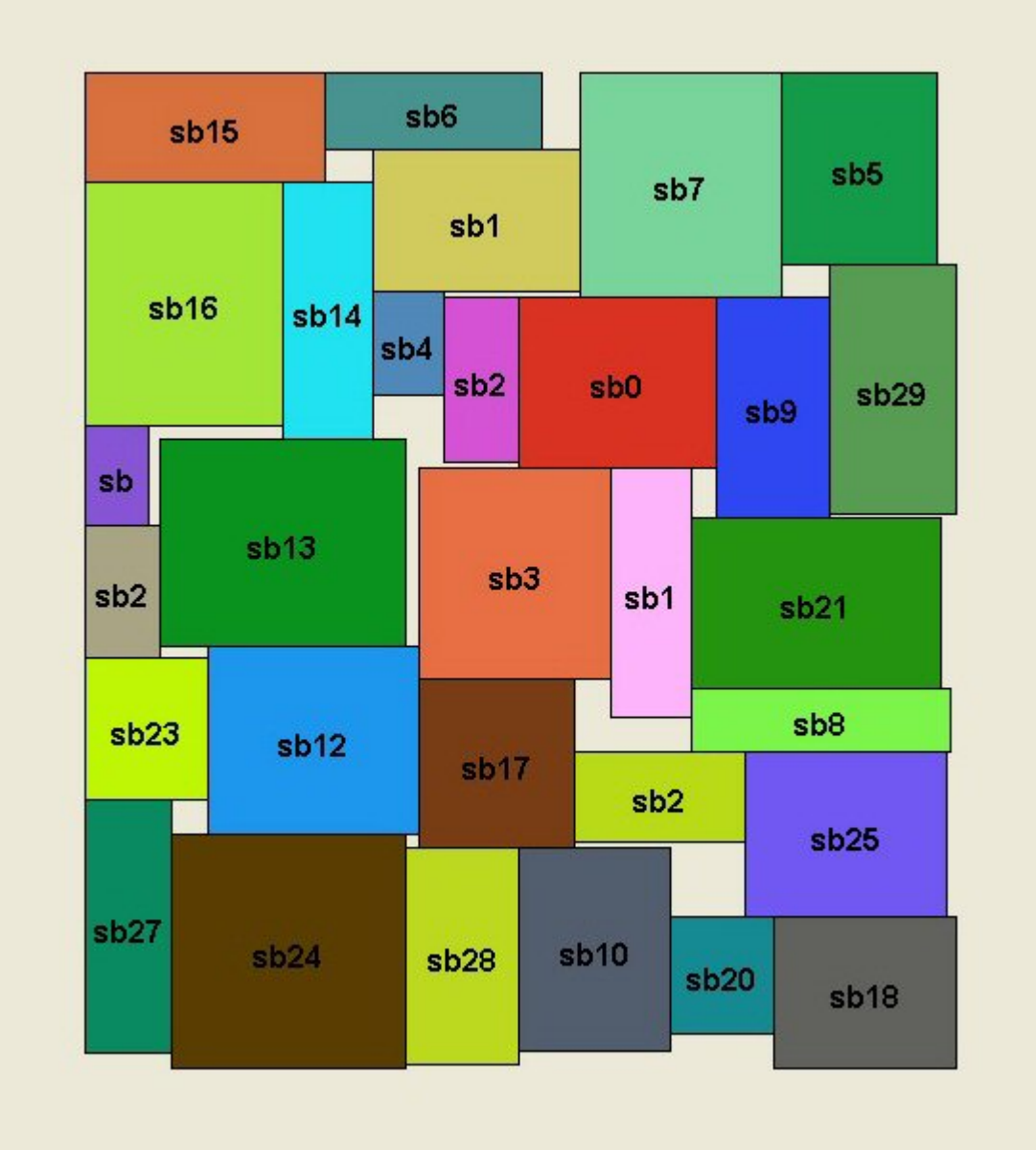


Figure 82. Optimized placement and both electrical and optical waveguide routing for n30b benchmark circuit



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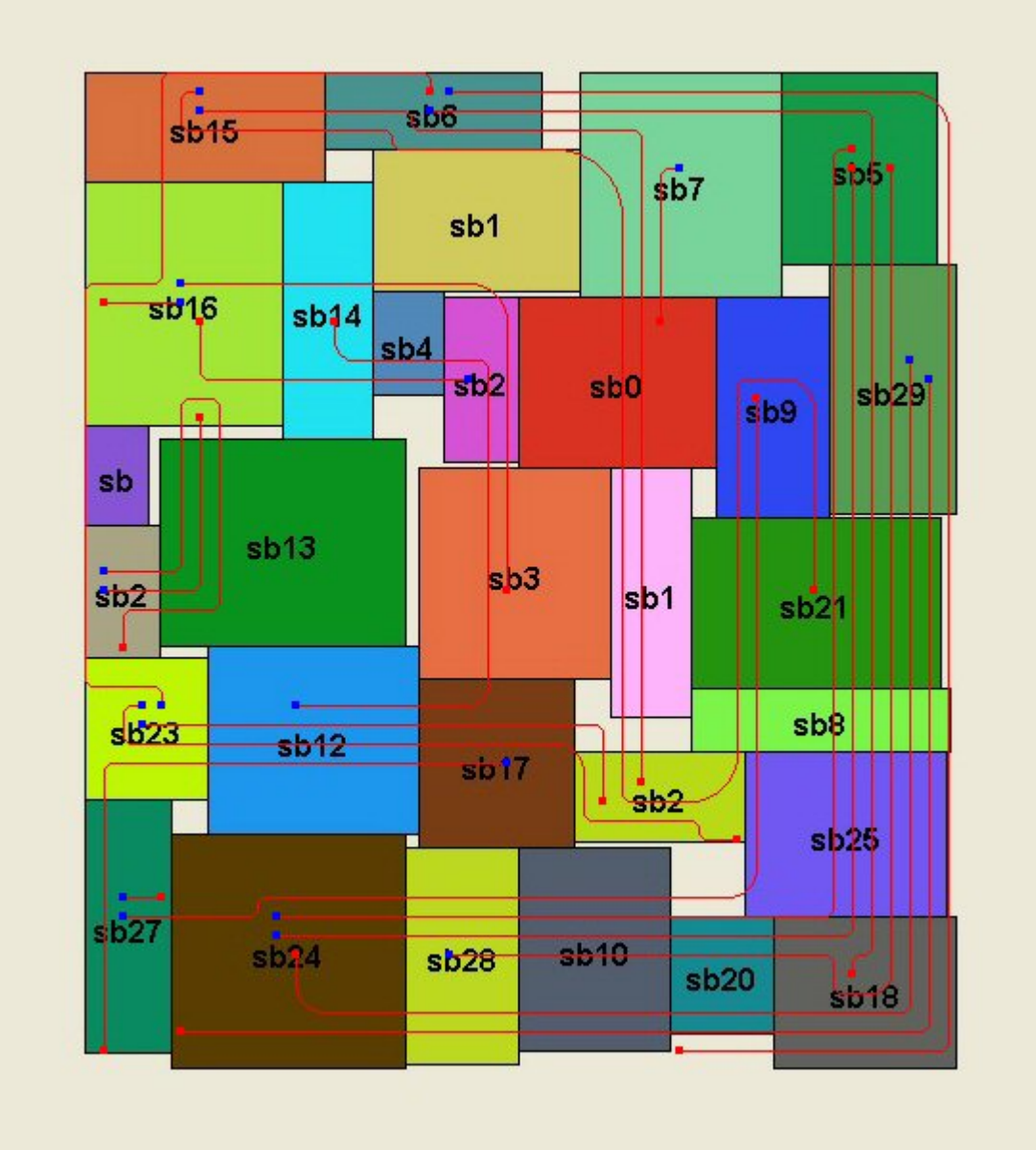


Figure 84. Optimized placement and optical waveguide routing for n30c benchmark circuit

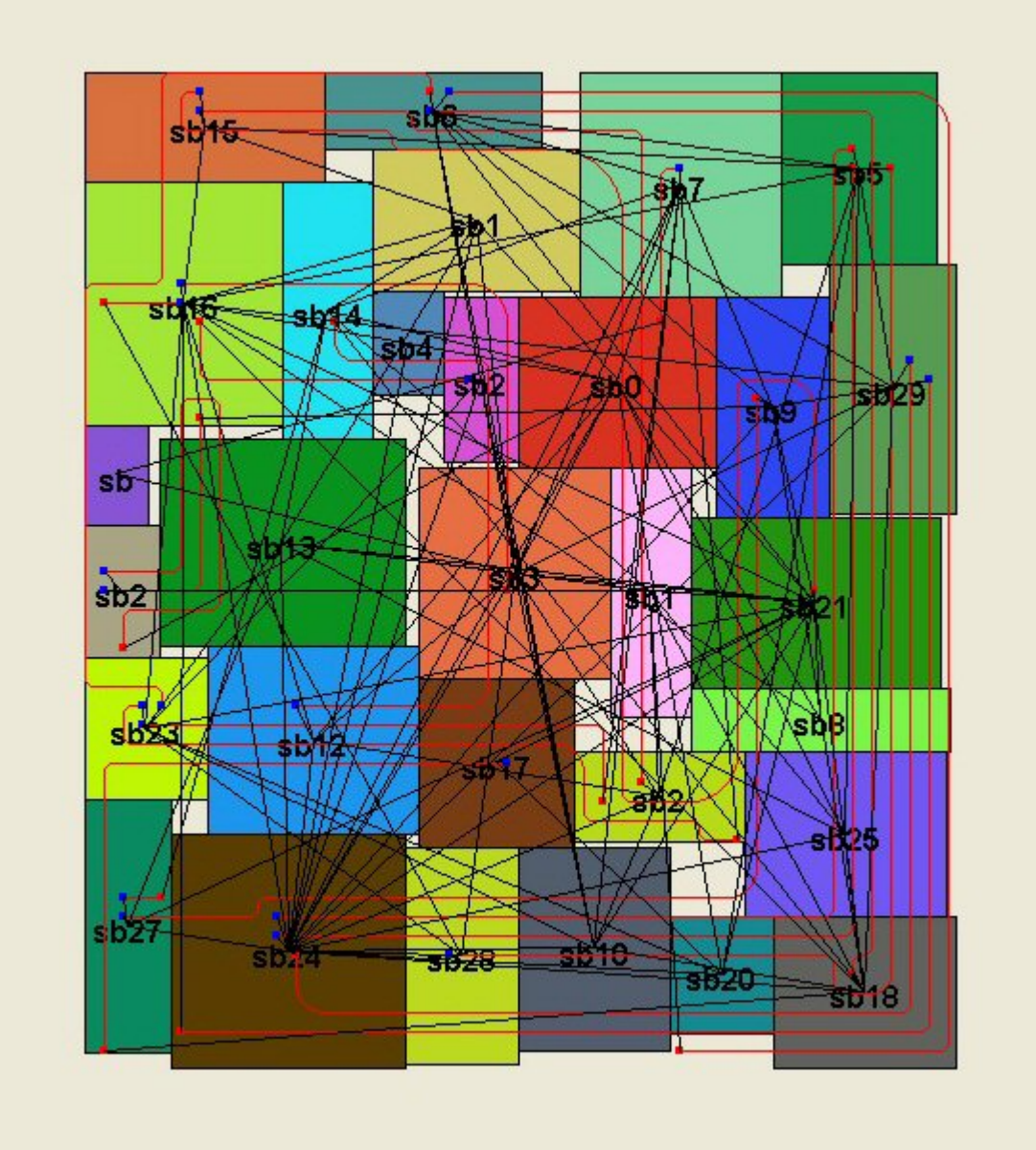


Figure 85. Optimized placement and both electrical and optical waveguide routing for n30c benchmark circuit

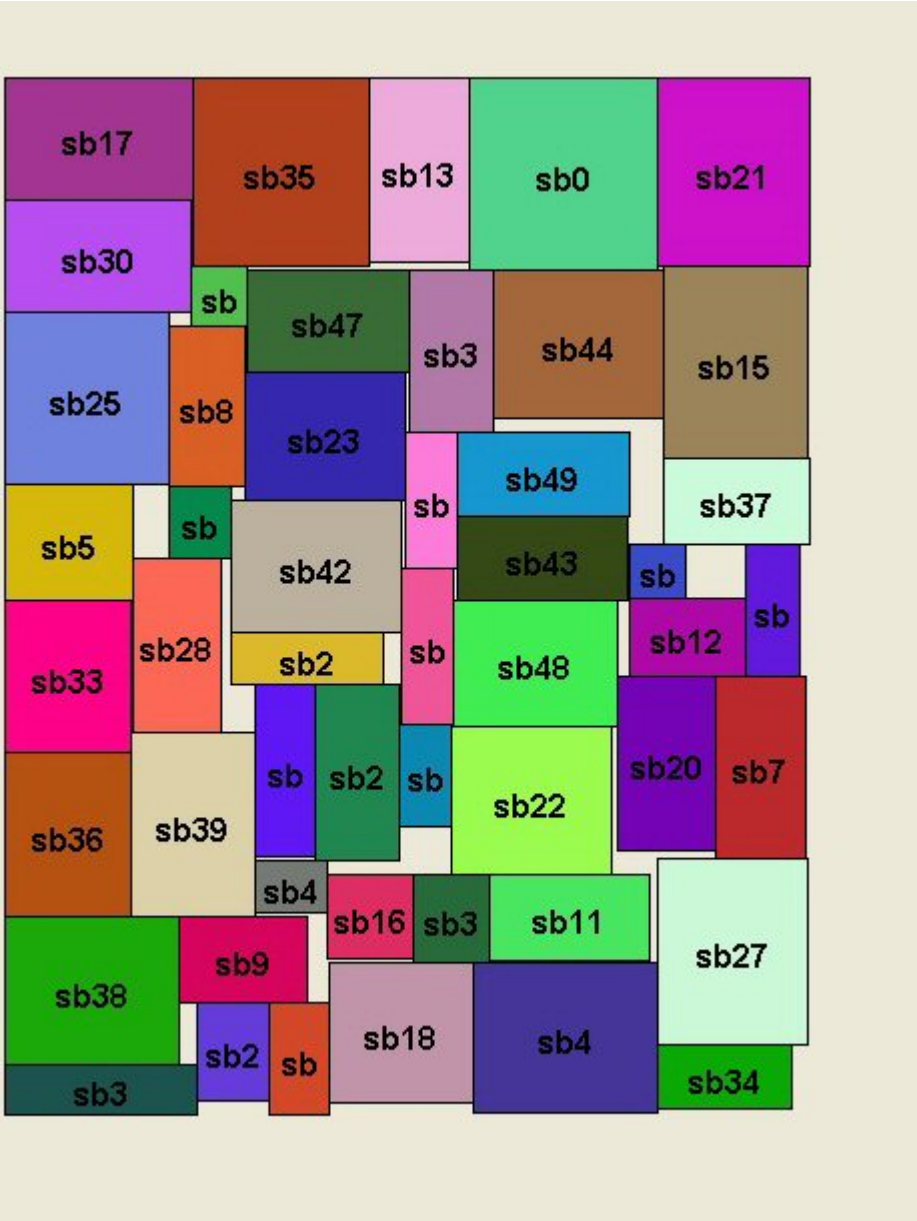


Figure 86. Optimized placement for n50a benchmark circuit

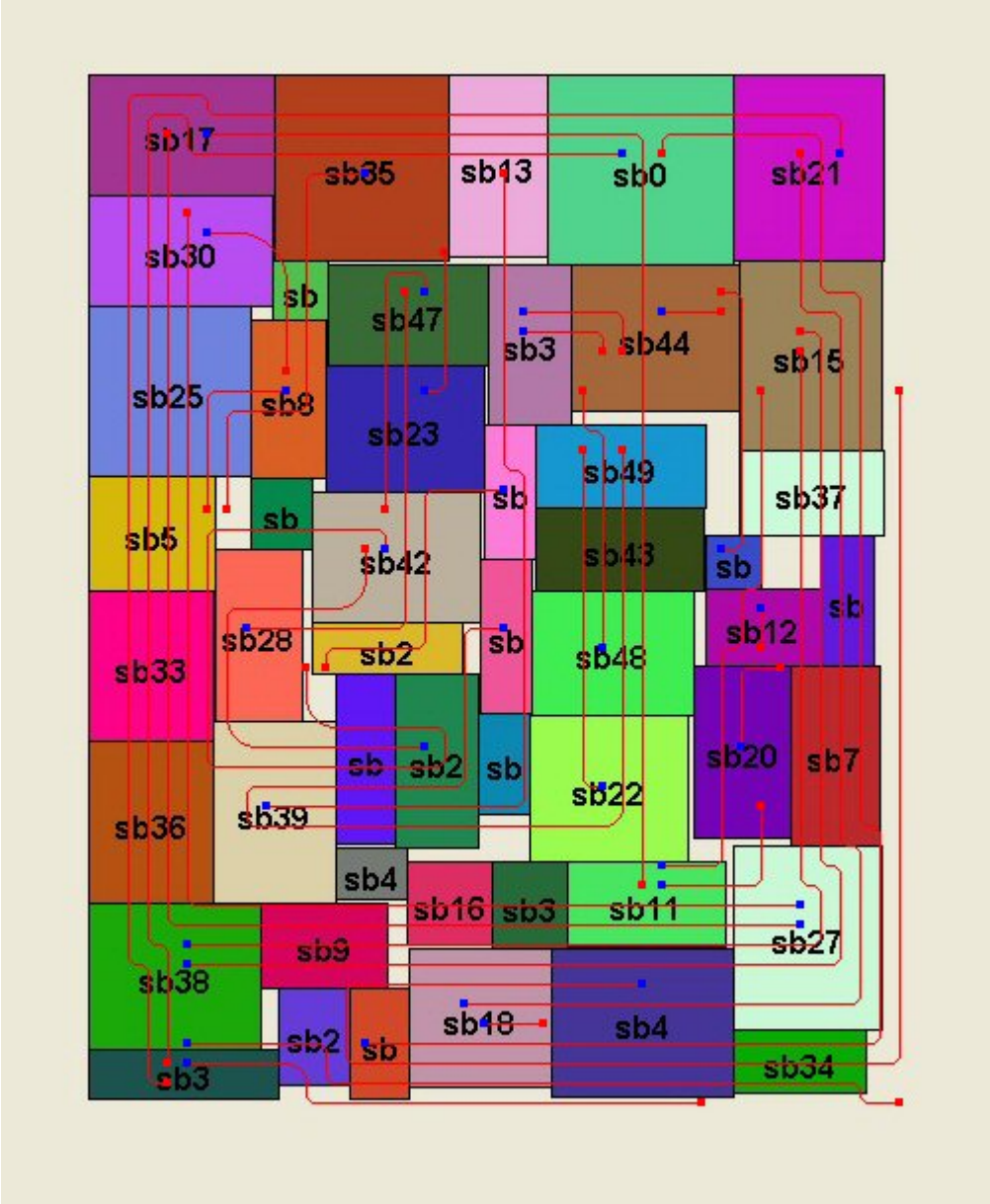


Figure 87. Optimized placement and optical waveguide routing for n50a benchmark circuit

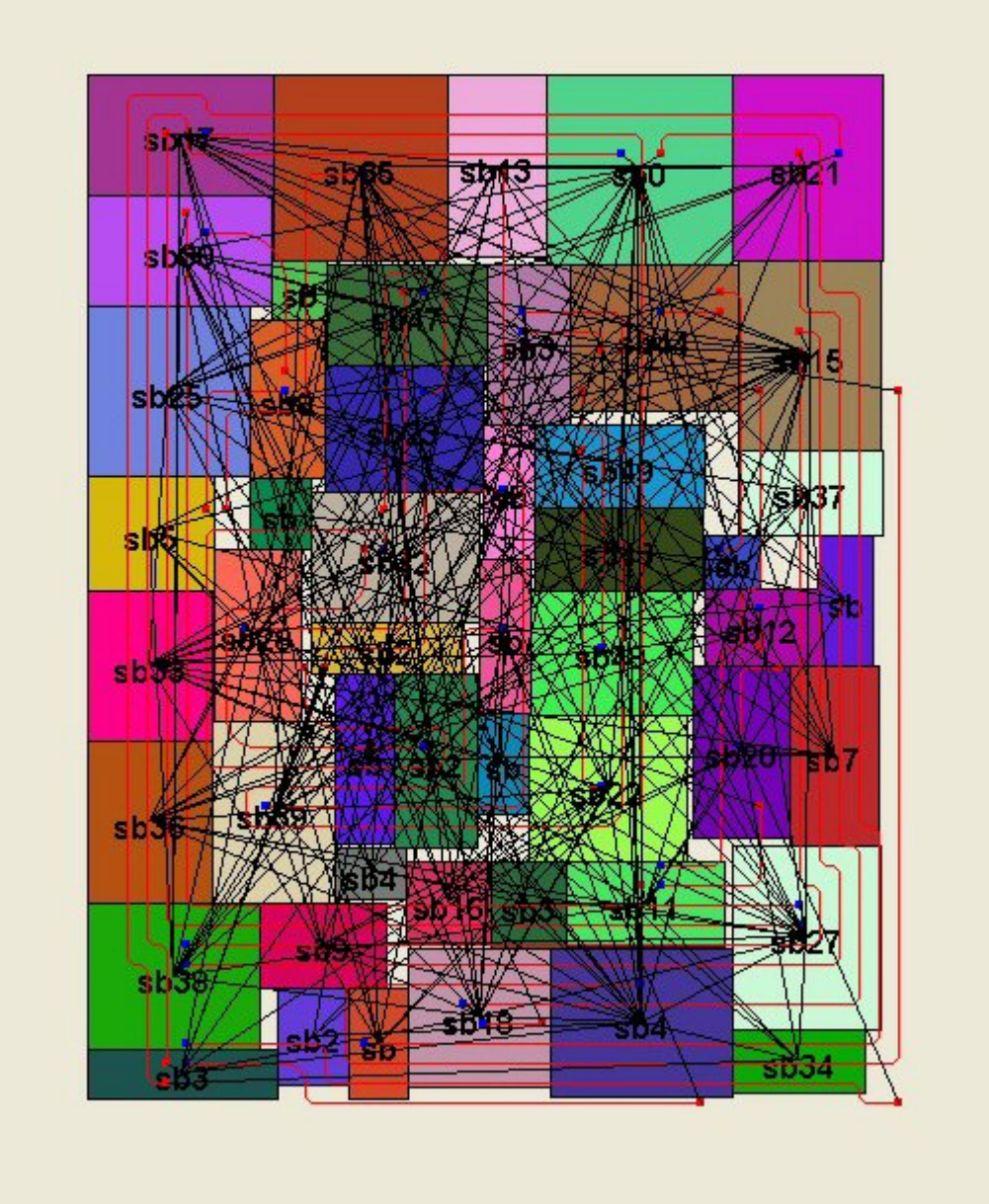


Figure 88. Optimized placement and both electrical and optical waveguide routing for n50a benchmark circuit

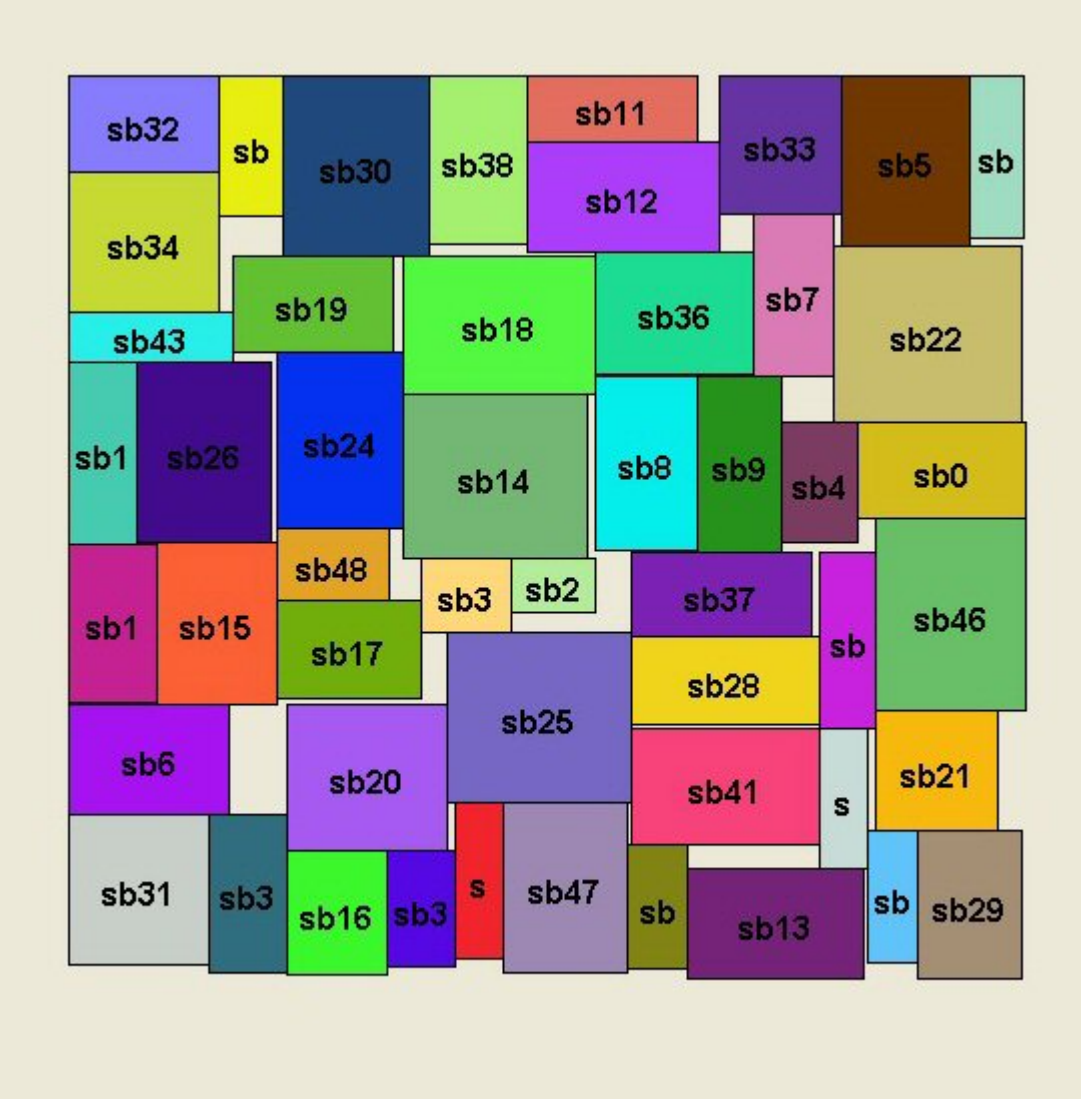


Figure 89. Optimized placement for n50b benchmark circuit

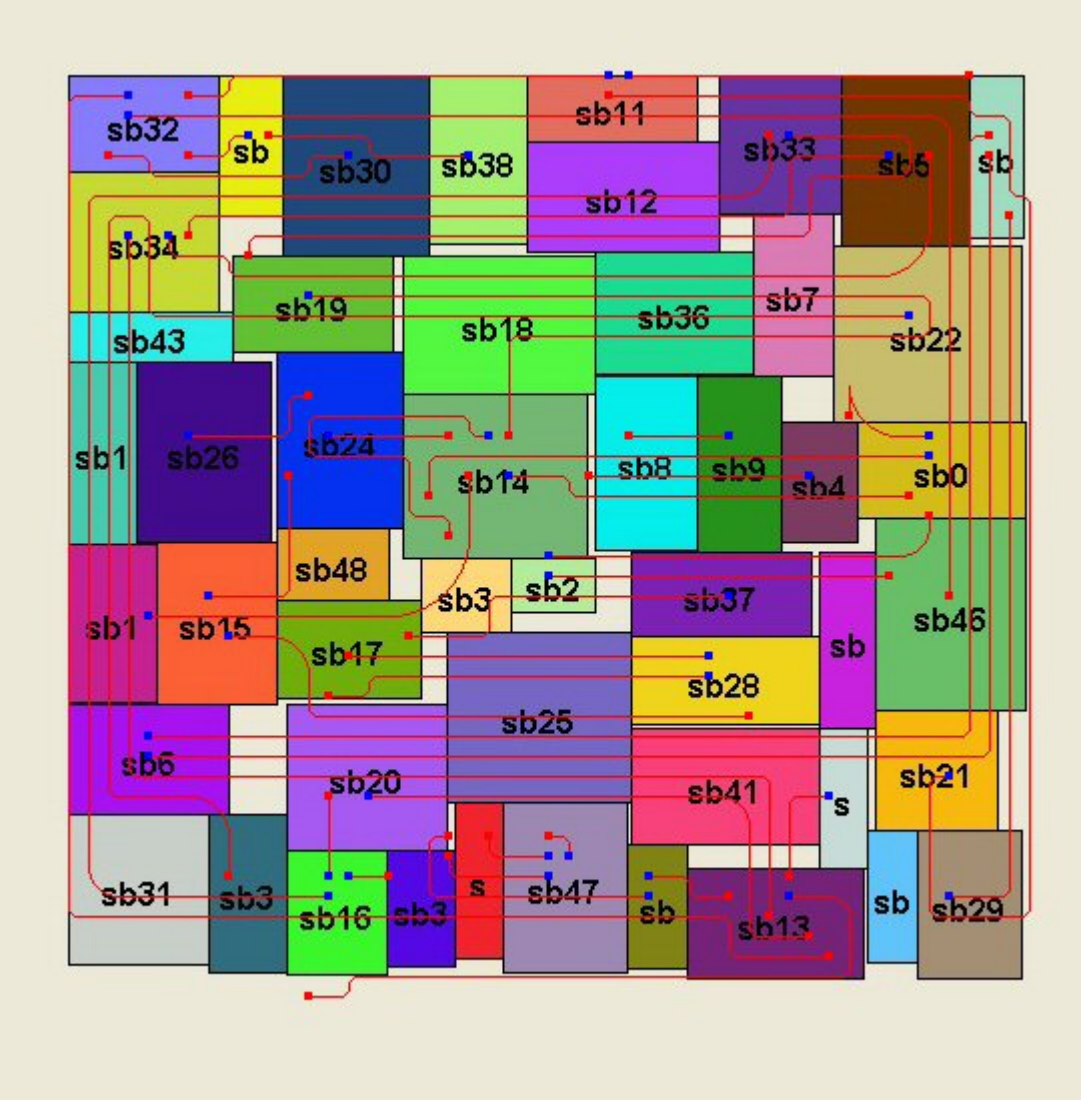


Figure 90. Optimized placement and optical waveguide routing for n50b benchmark circuit

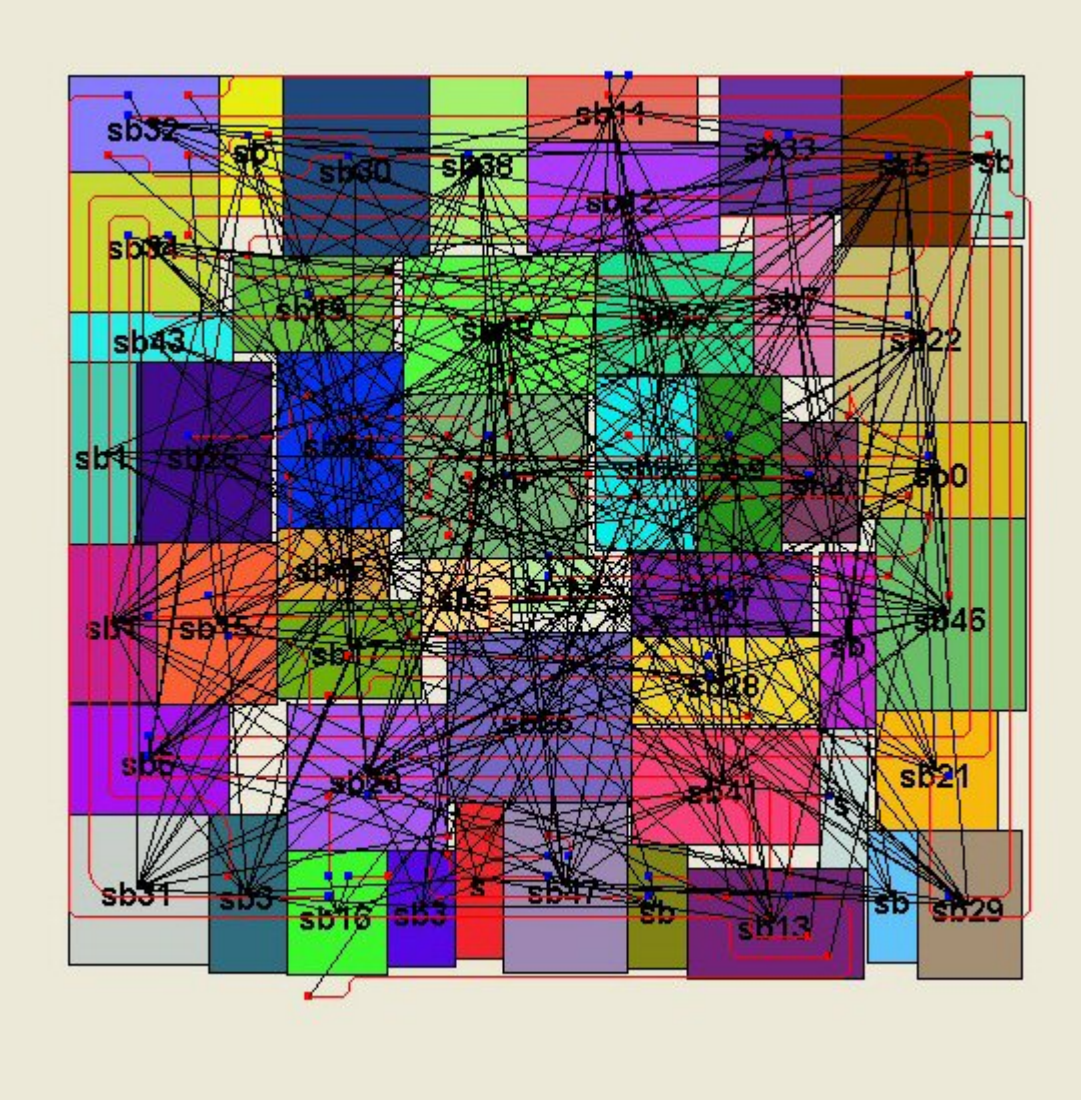


Figure 91. Optimized placement and both electrical and optical waveguide routing for n50b benchmark circuit

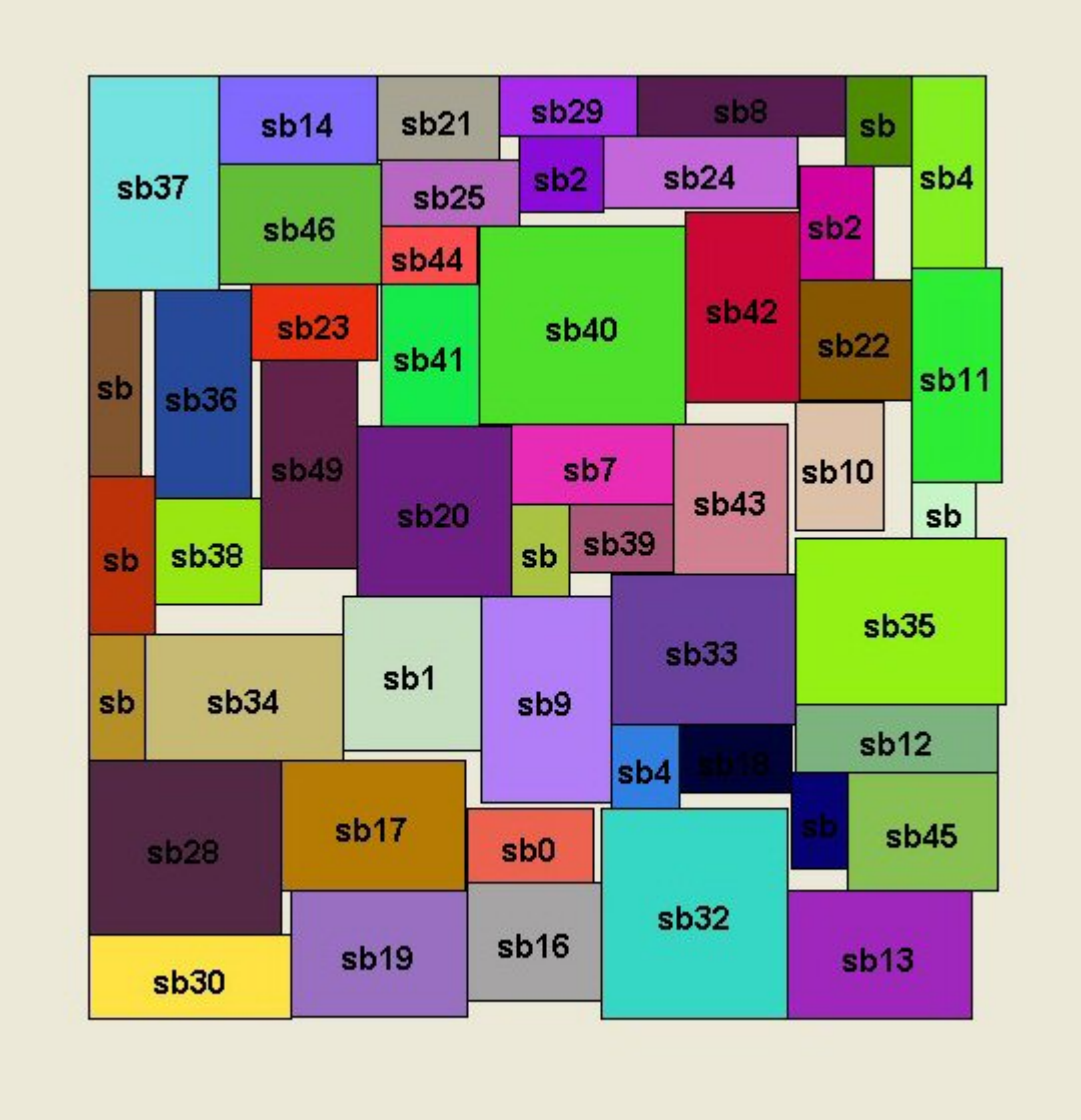


Figure 92. Optimized placement for n50c benchmark circuit

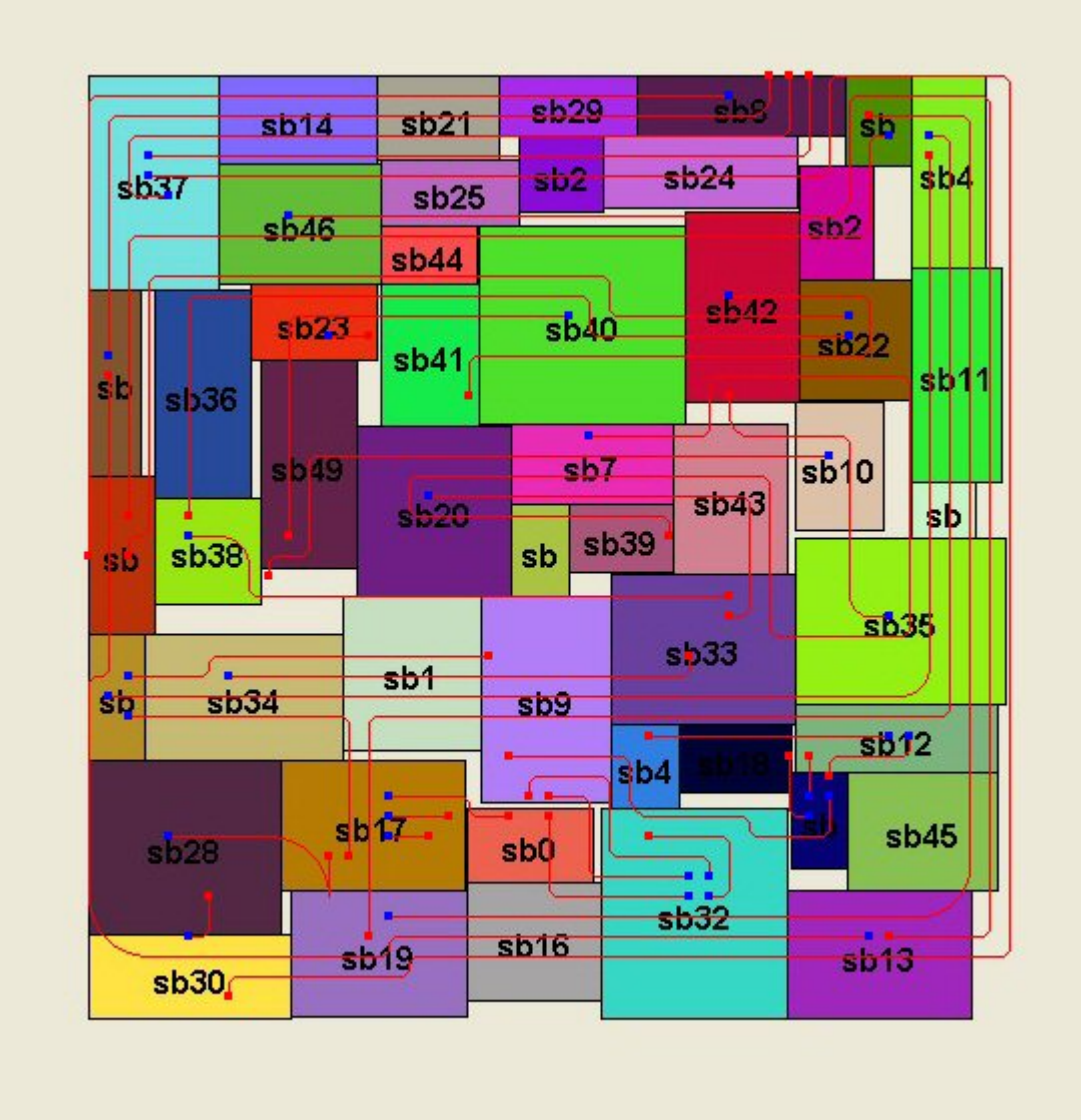


Figure 93. Optimized placement and optical waveguide routing for n50c benchmark circuit

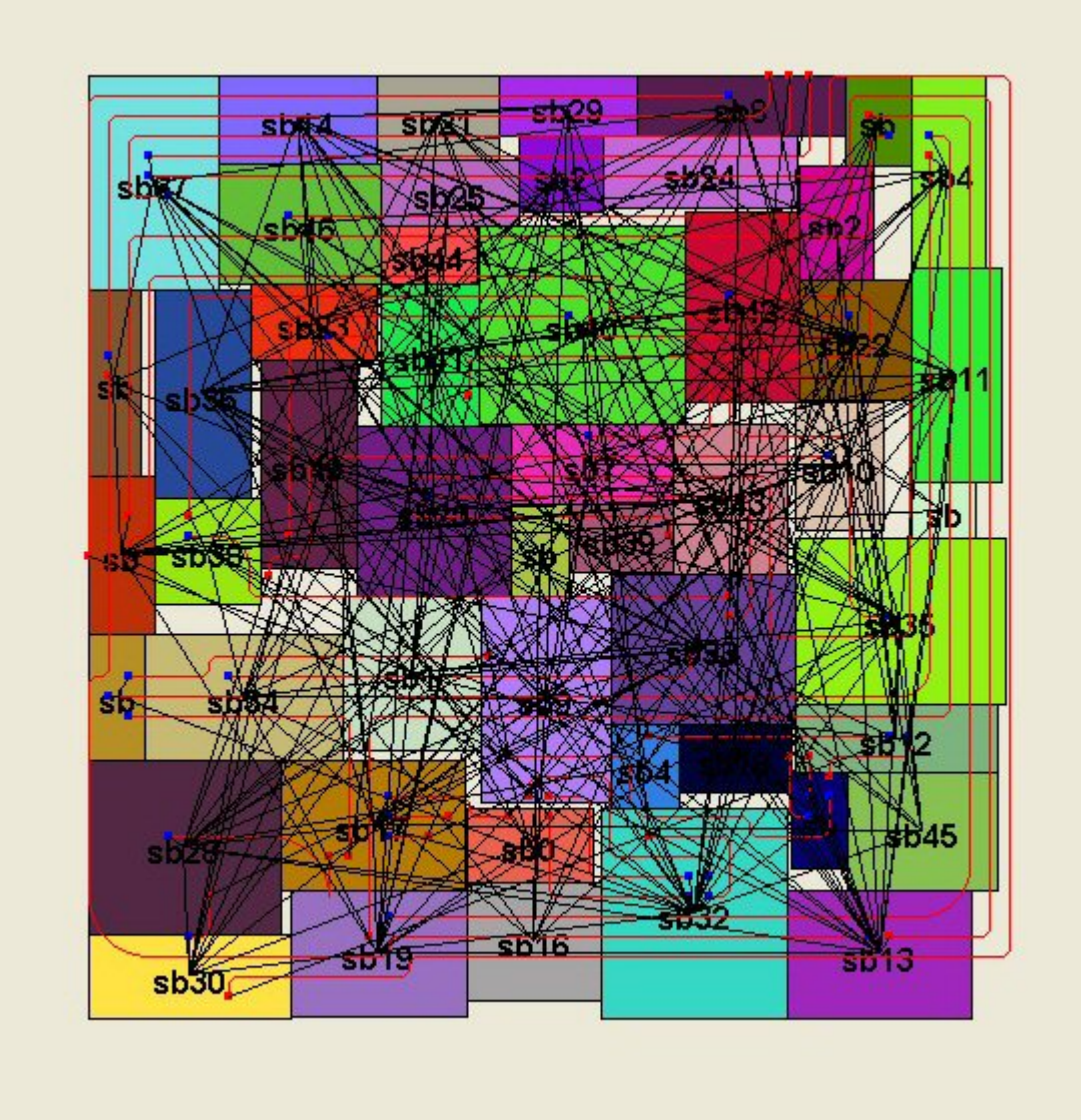


Figure 94. Optimized placement and both electrical and optical waveguide routing for n50c benchmark circuit

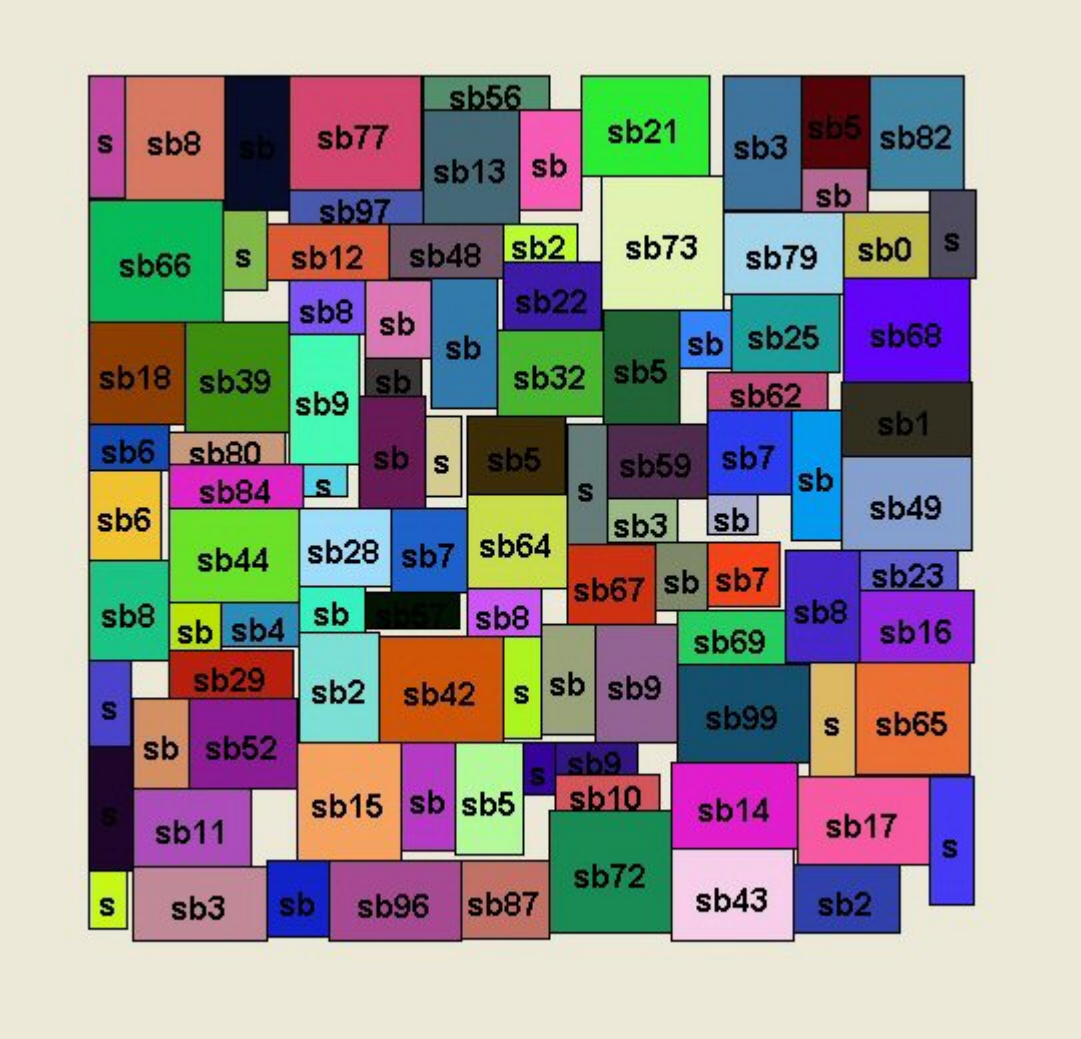


Figure 95. Optimized placement for n100a benchmark circuit

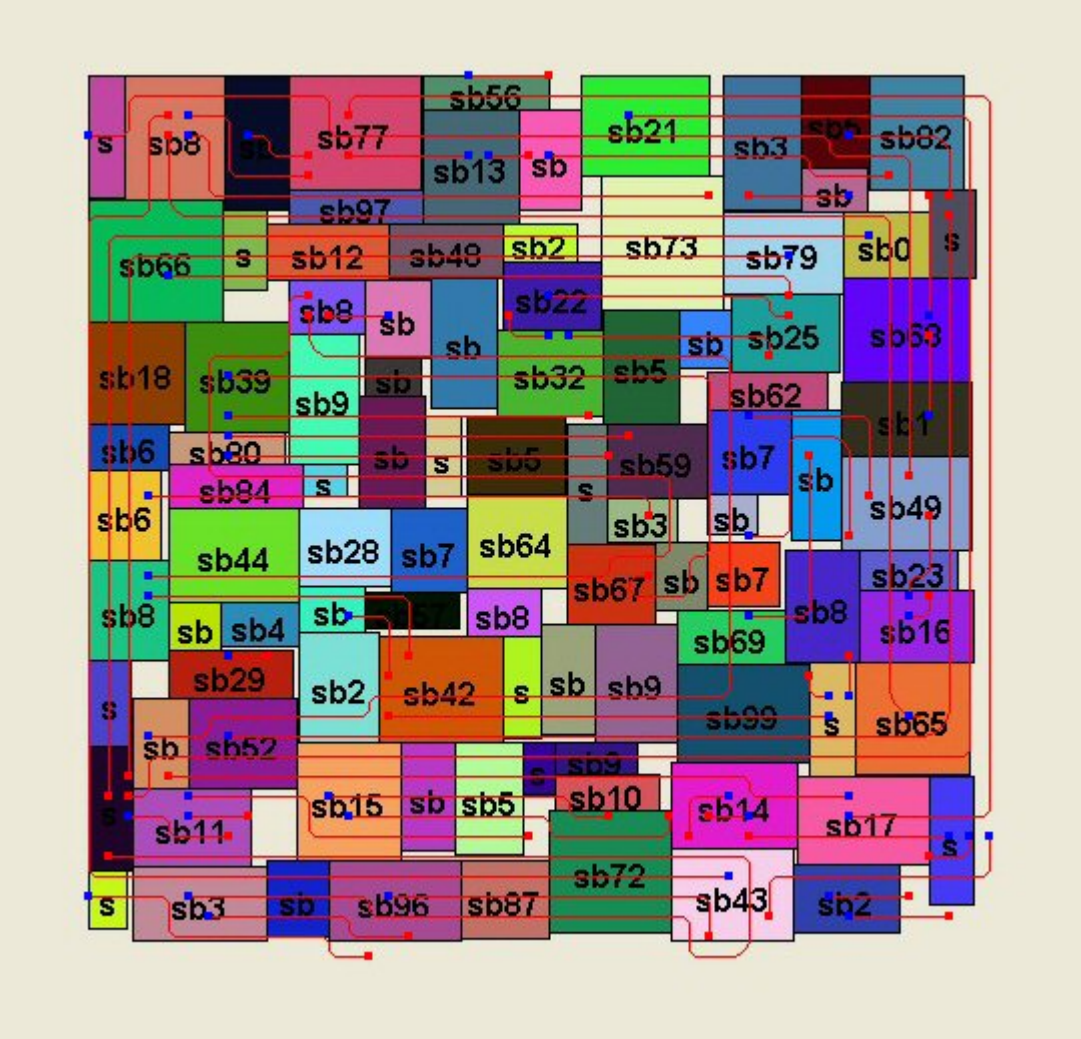


Figure 96. Optimized placement and optical waveguide routing for n100a benchmark circuit

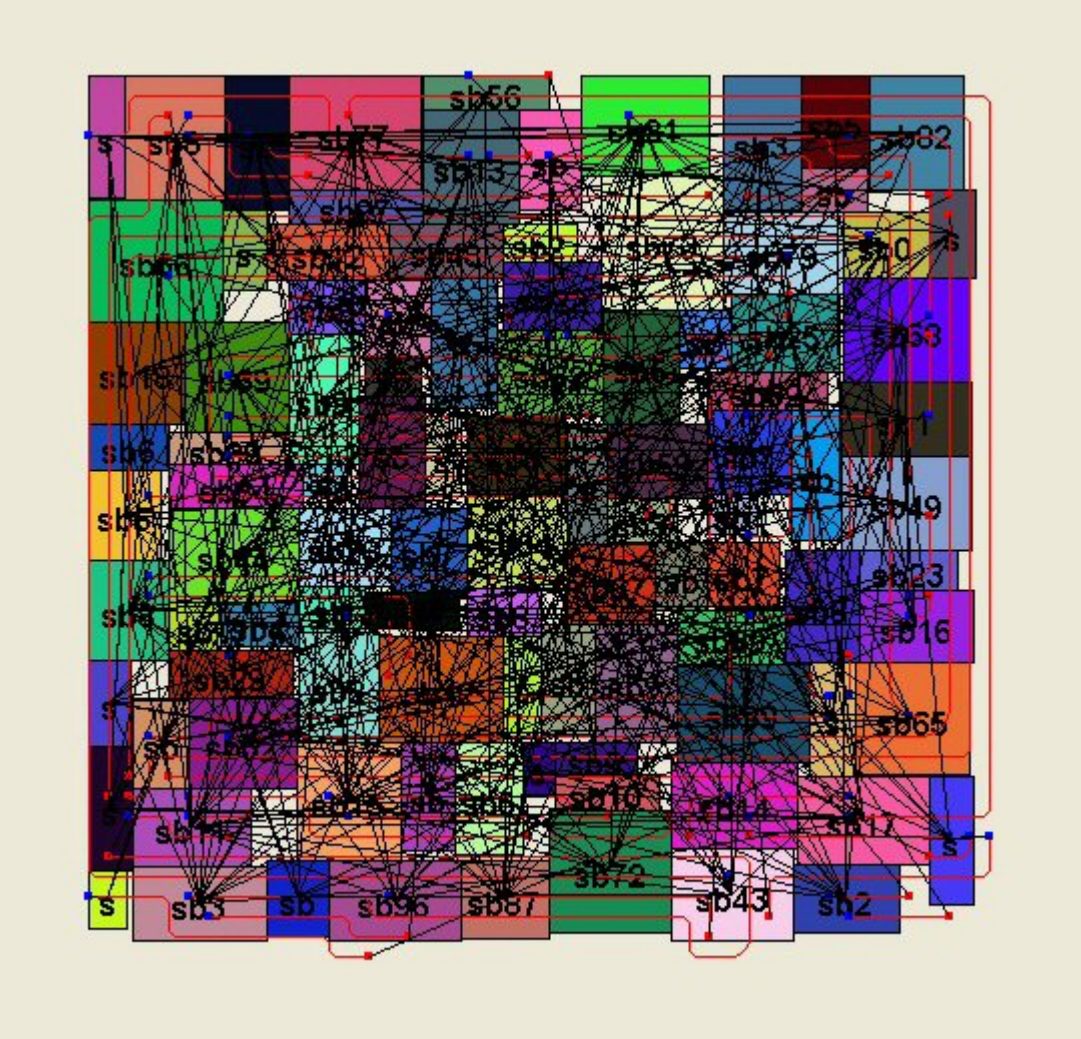


Figure 97. Optimized placement and both electrical and optical waveguide routing for n100a benchmark circuit

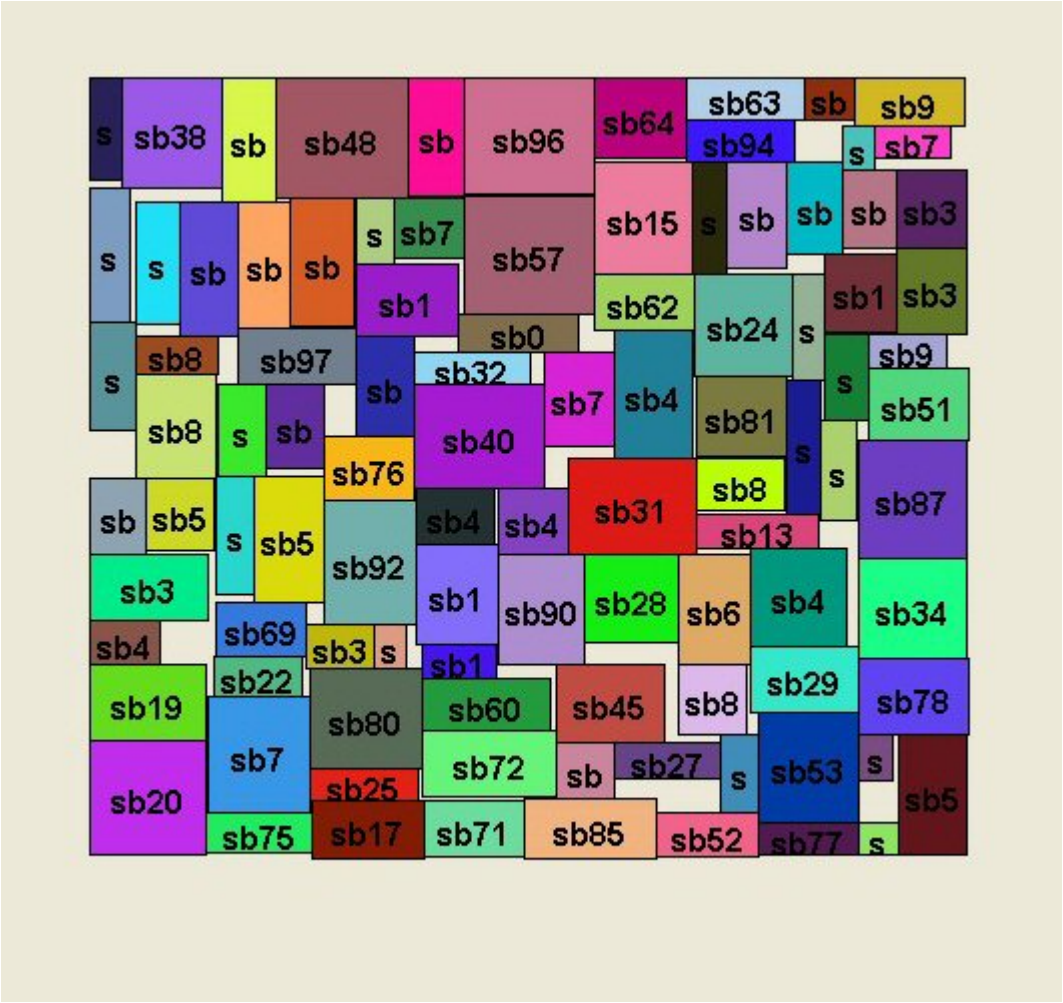


Figure 98. Optimized placement for n100b benchmark circuit

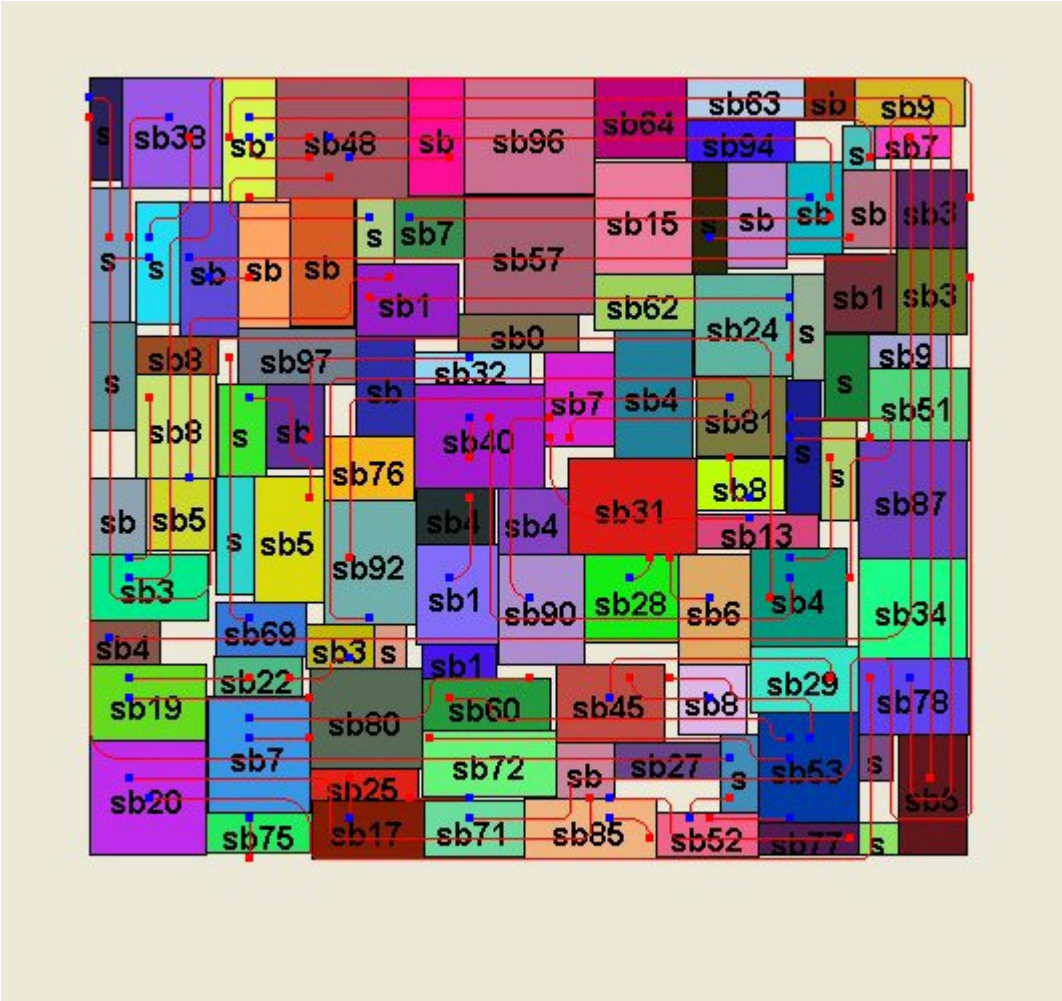


Figure 99. Optimized placement and optical waveguide routing for n100b benchmark circuit

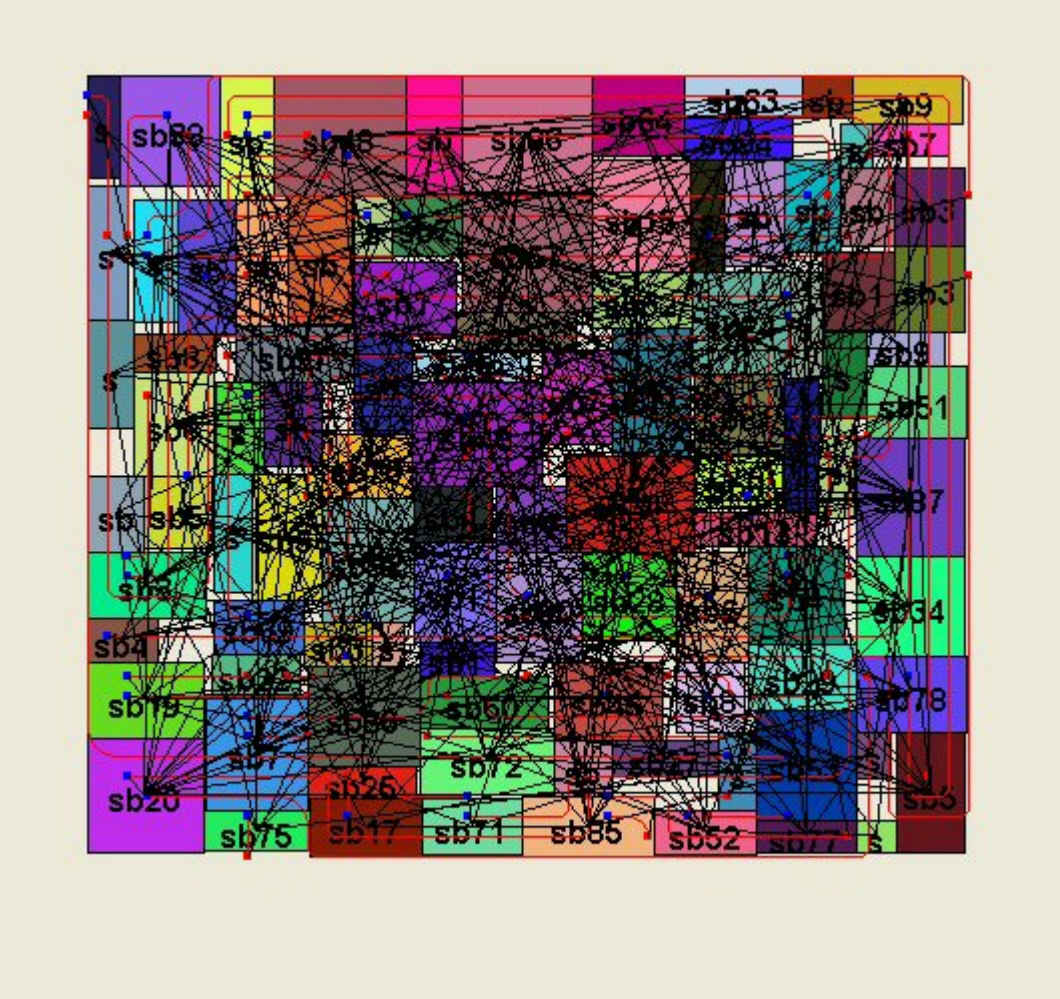
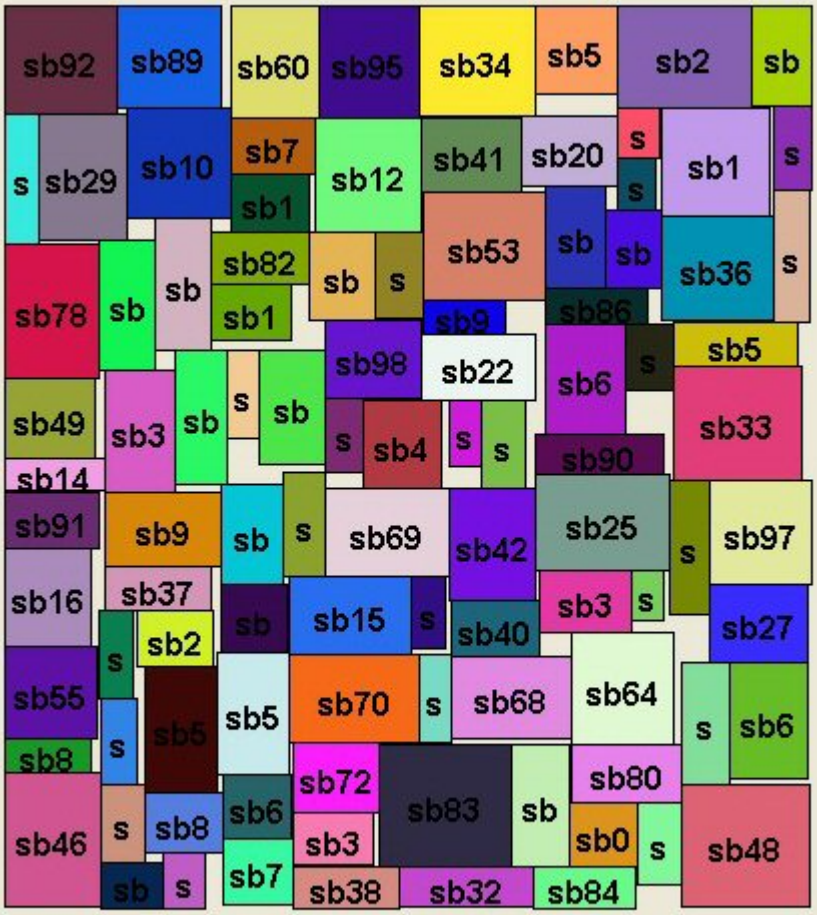


Figure 100. Optimized placement and both electrical and optical waveguide routing for n100b benchmark circuit



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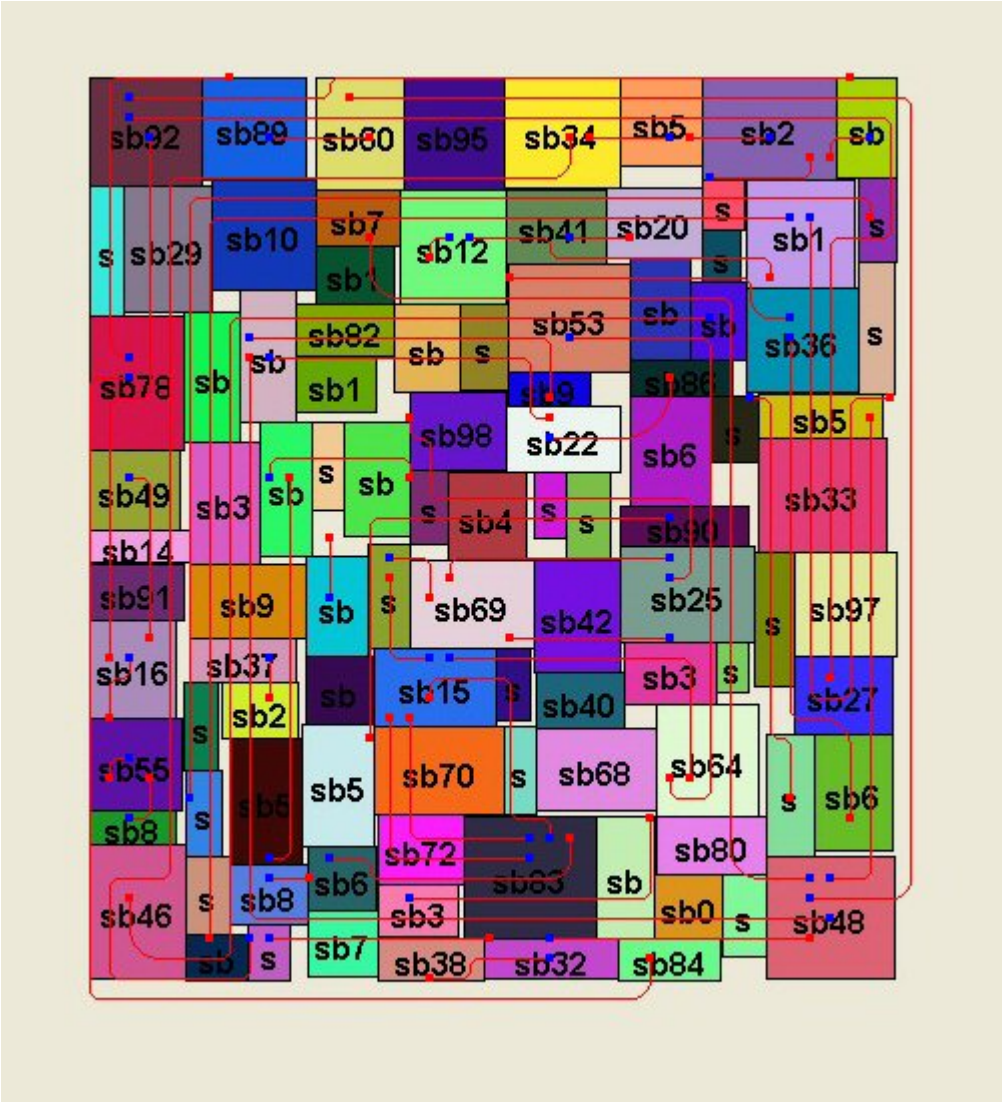

Figure 102. Optimized placement and optical waveguide routing for n100c benchmark circuit

Figure 103. Optimized placement and both electrical and optical waveguide routing for n100c benchmark circuit

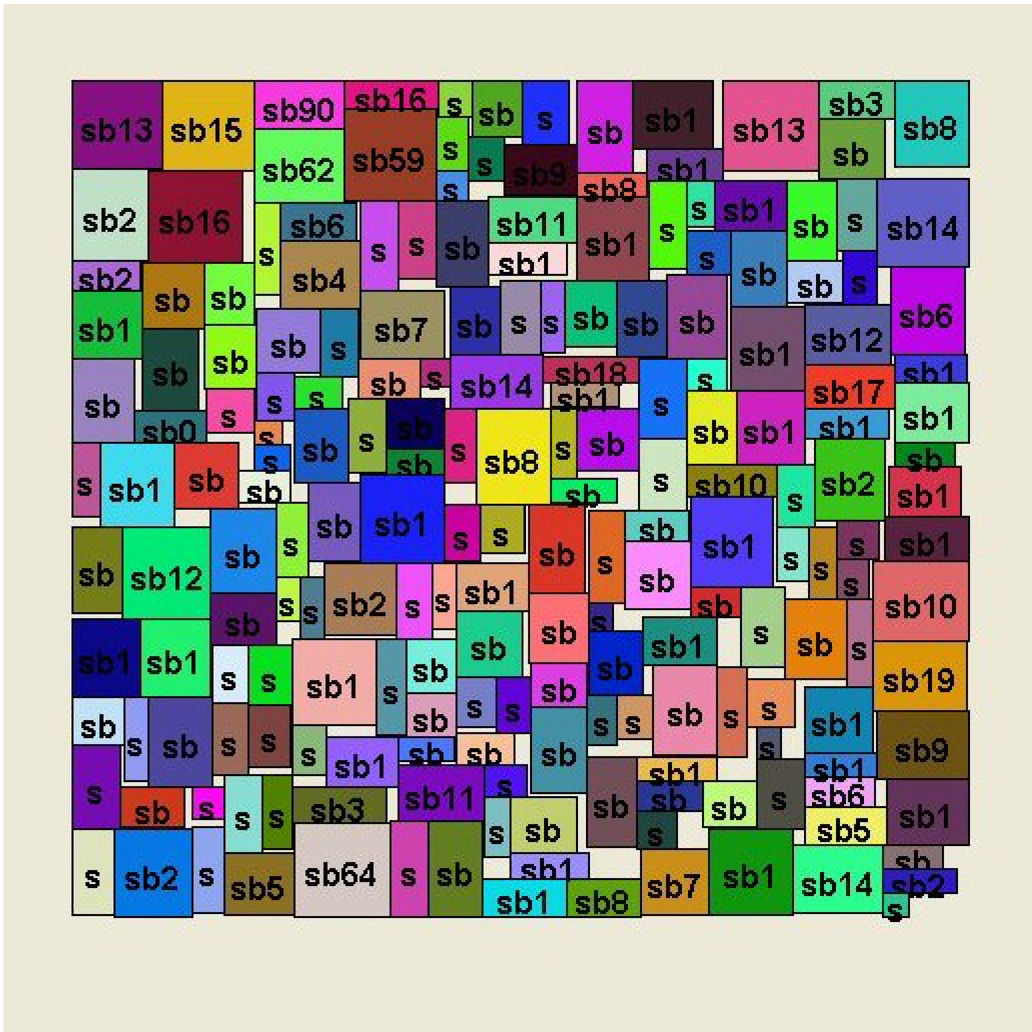

Figure 104. Optimized placement for n200a benchmark circuit

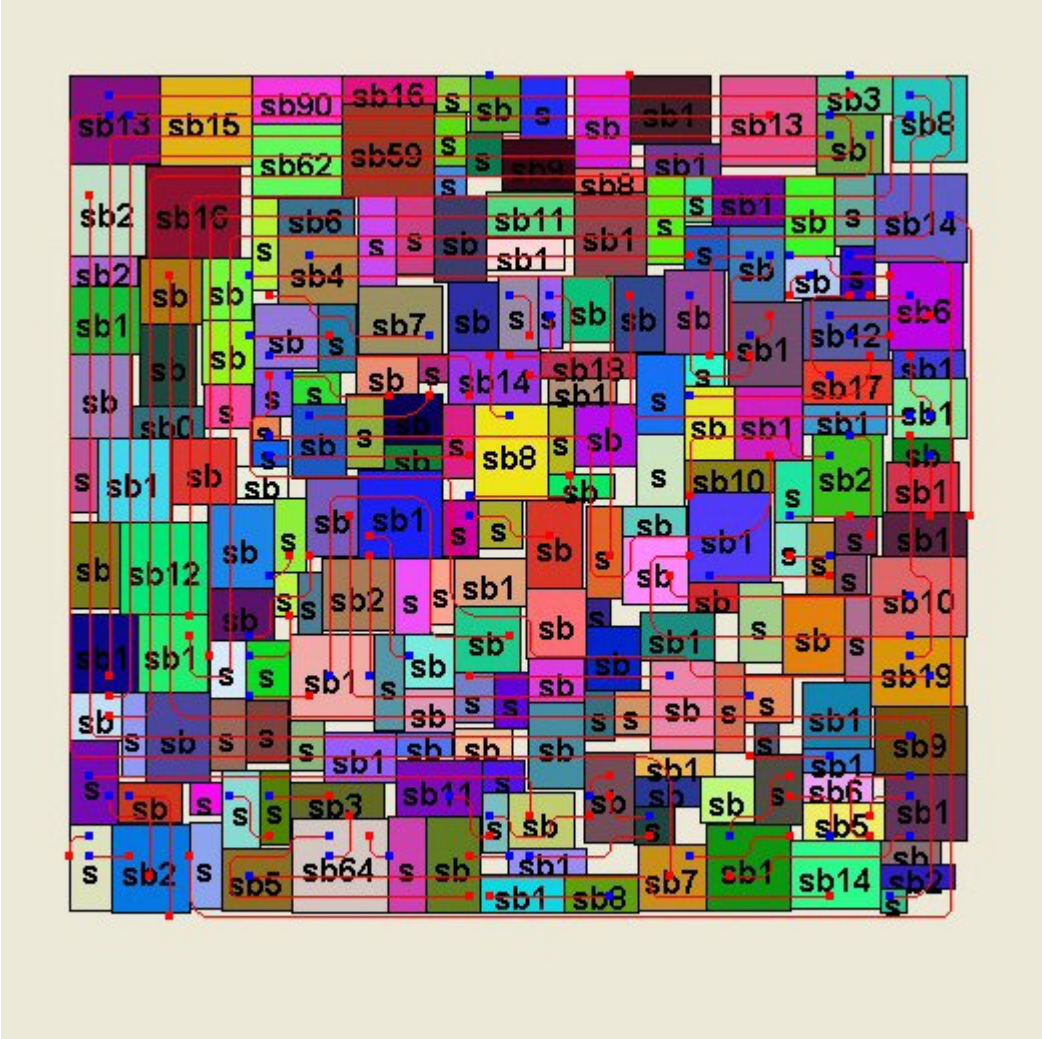

Figure 105. Optimized placement and optical waveguide routing for n200a benchmark circuit

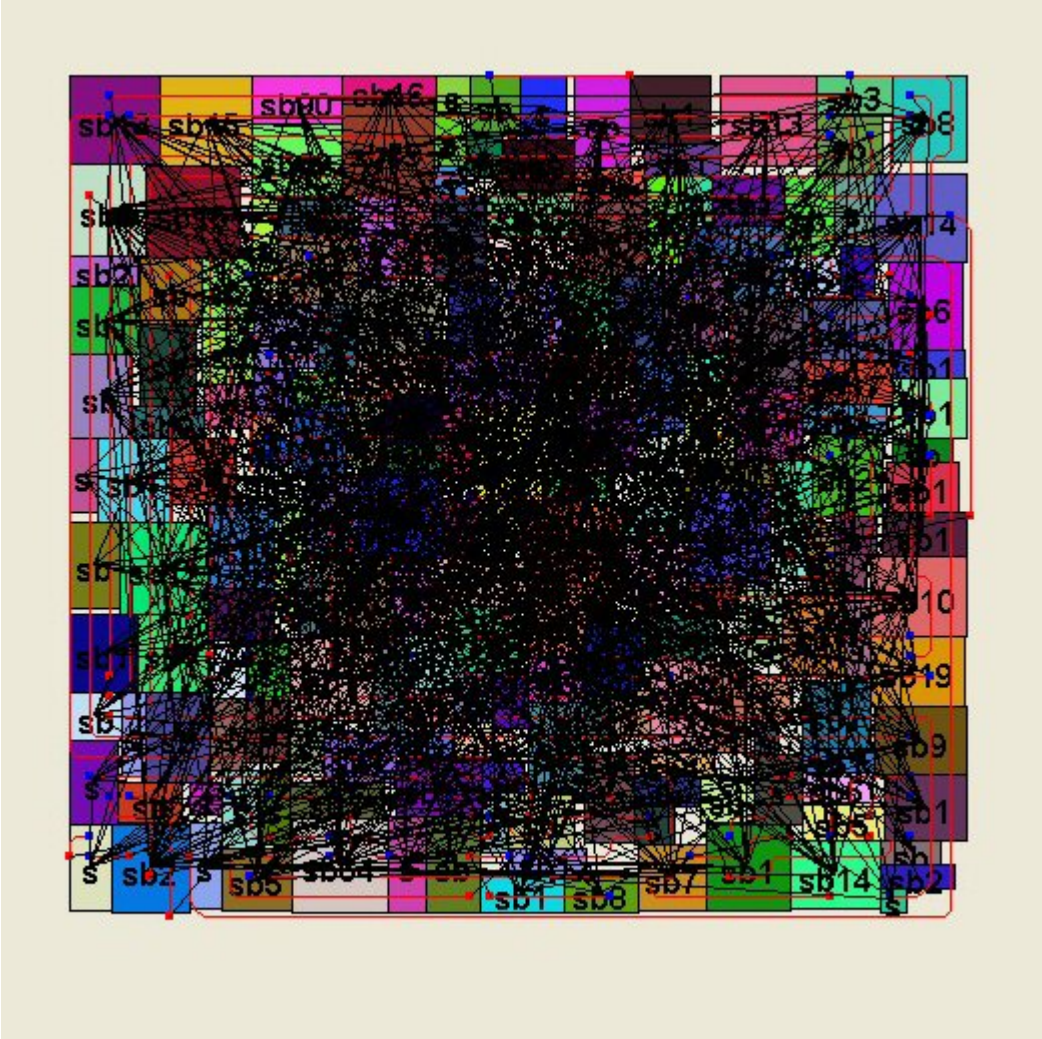

Figure 106. Optimized placement and both electrical and optical waveguide routing for n200a benchmark circuit

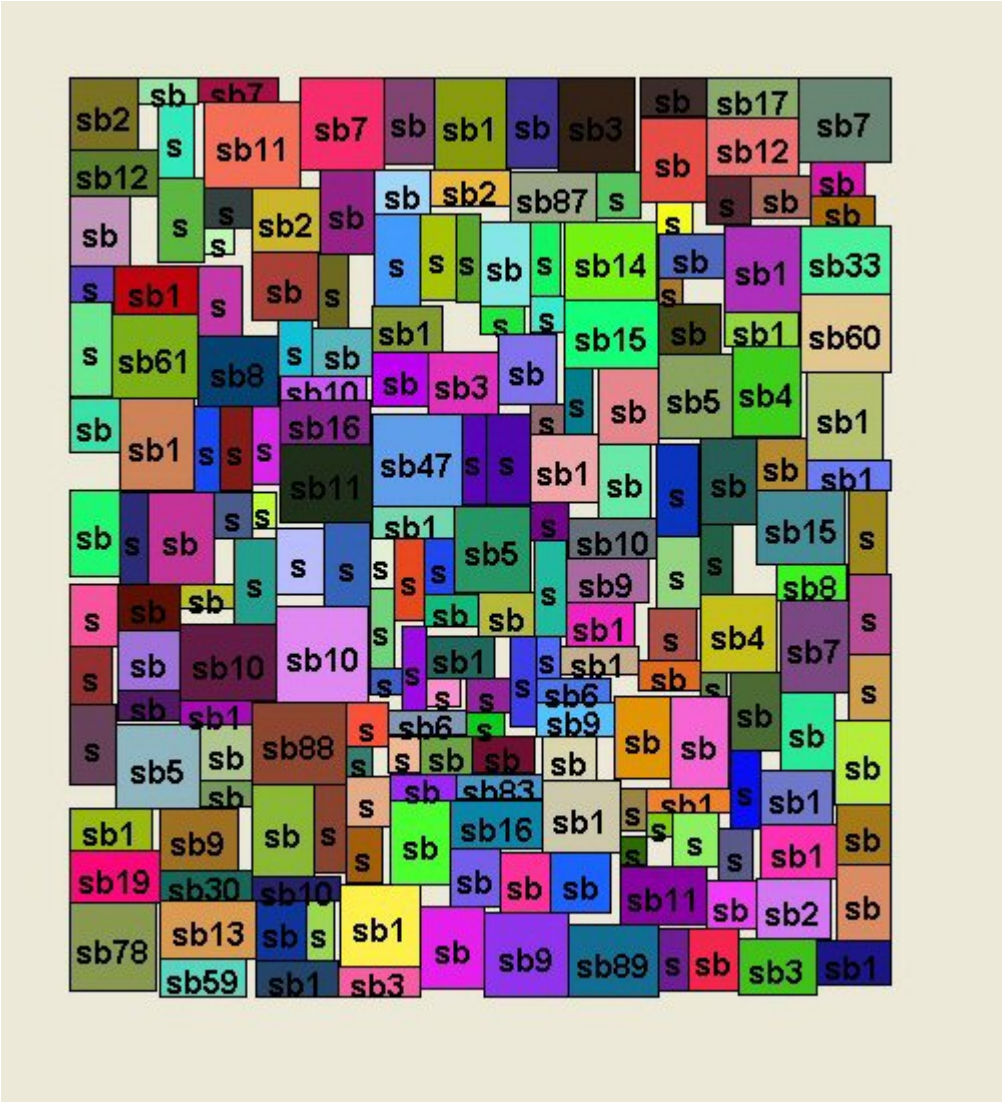

Figure 107. Optimized placement for n200b benchmark circuit

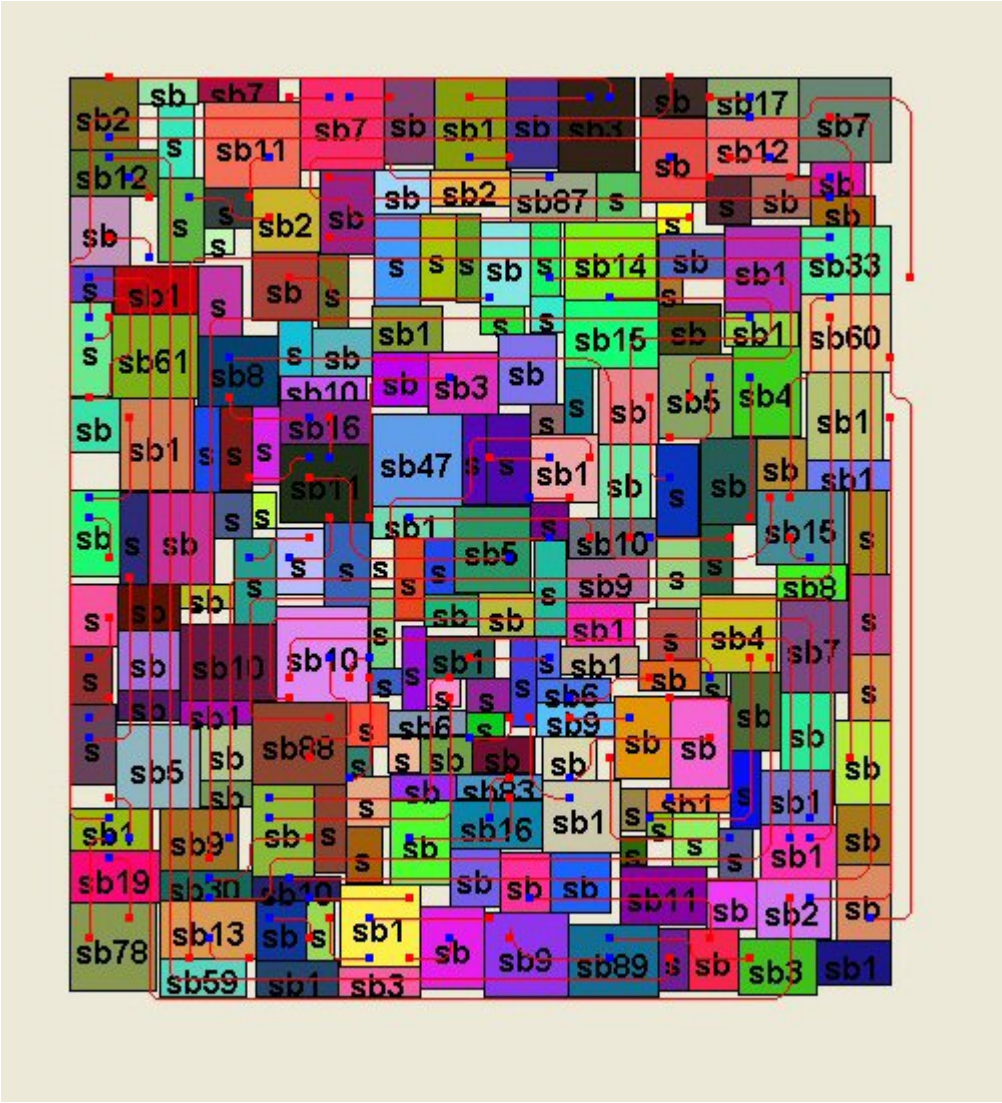

Figure 108. Optimized placement and optical waveguide routing for n200b benchmark circuit

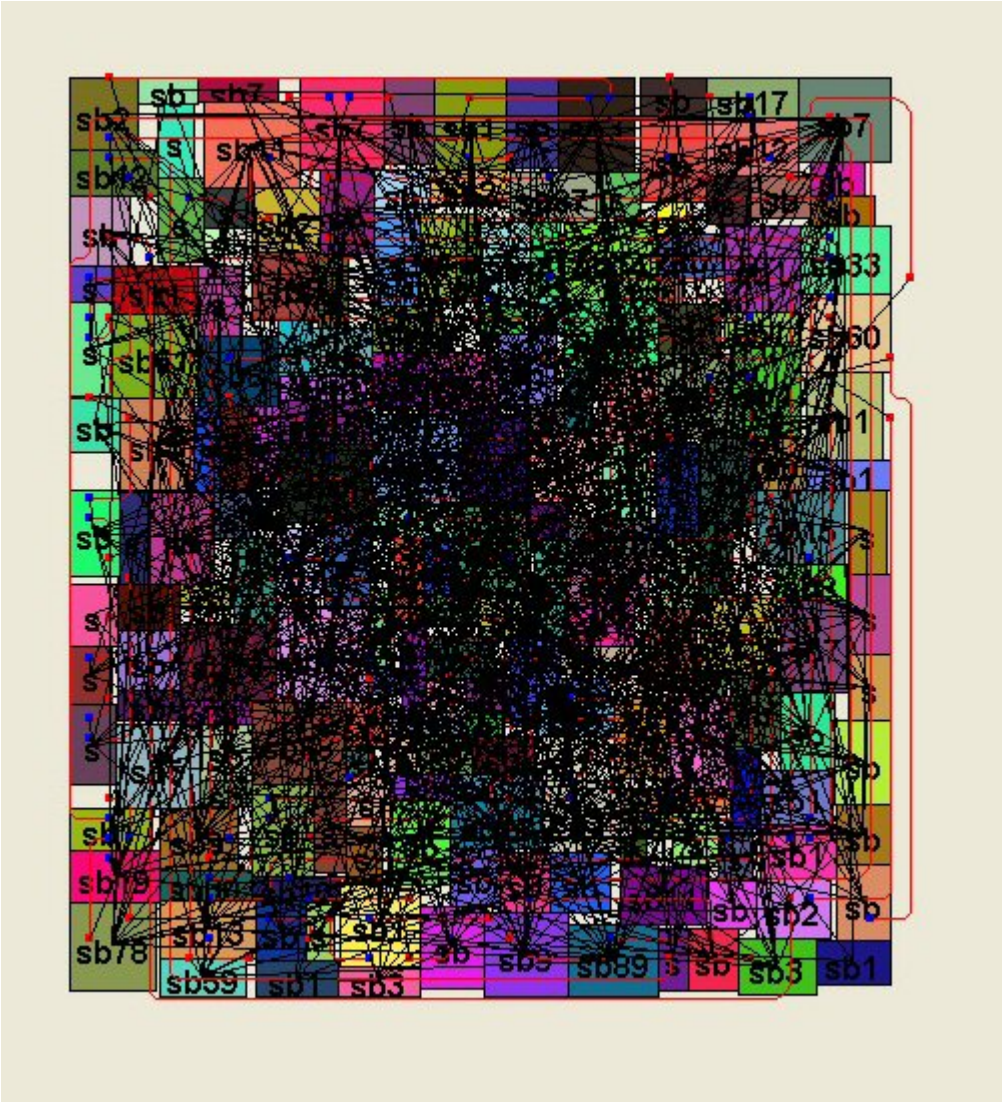

Figure 109. Optimized placement and both electrical and optical waveguide routing for n200b benchmark circuit

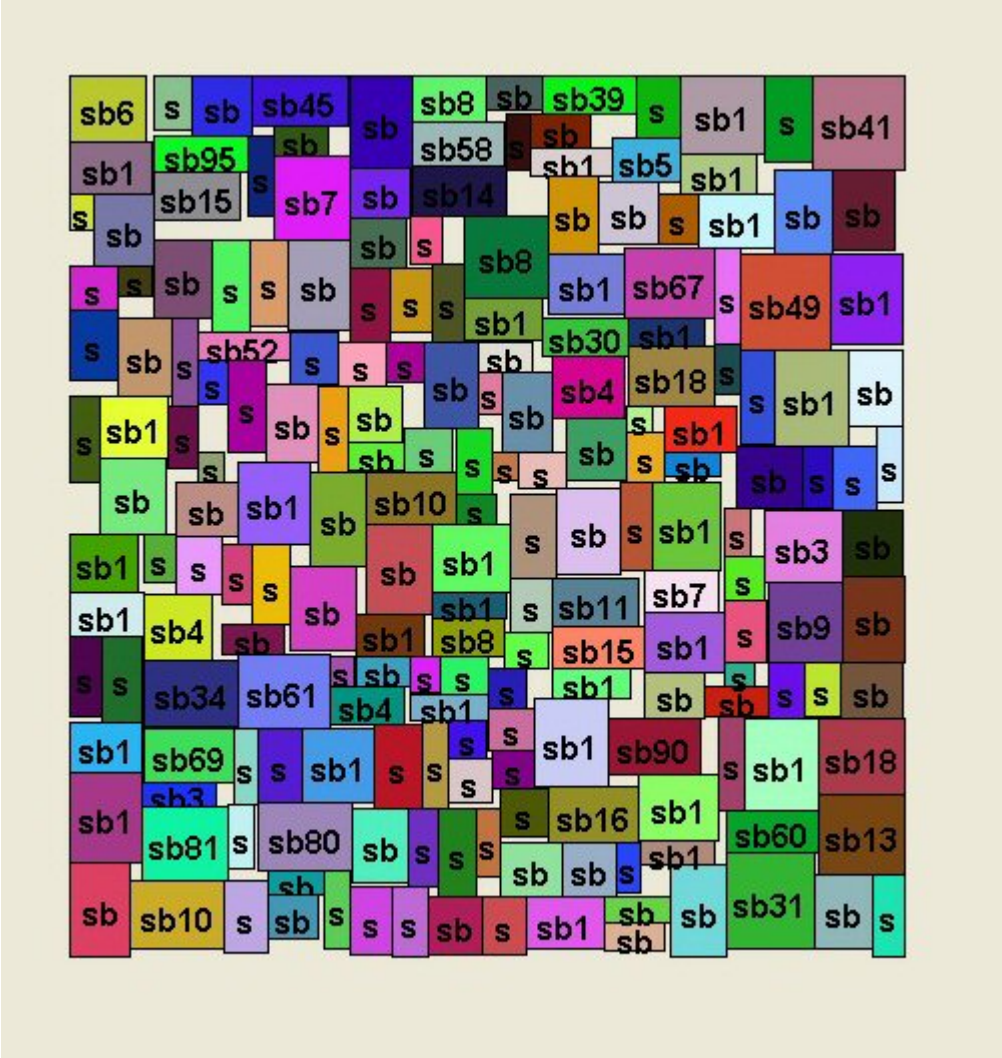

Figure 110. Optimized placement for n200c benchmark circuit

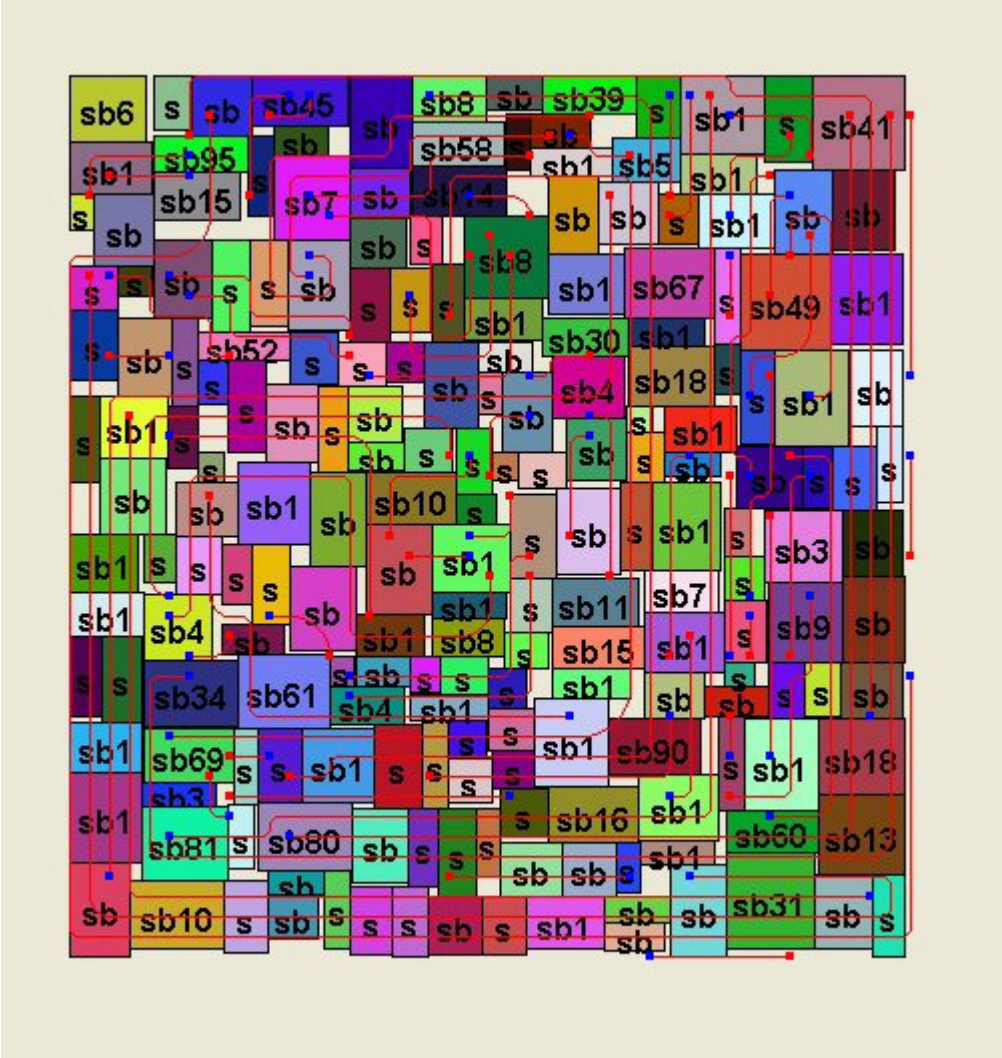

Figure 111. Optimized placement and optical waveguide routing for n200c benchmark circuit

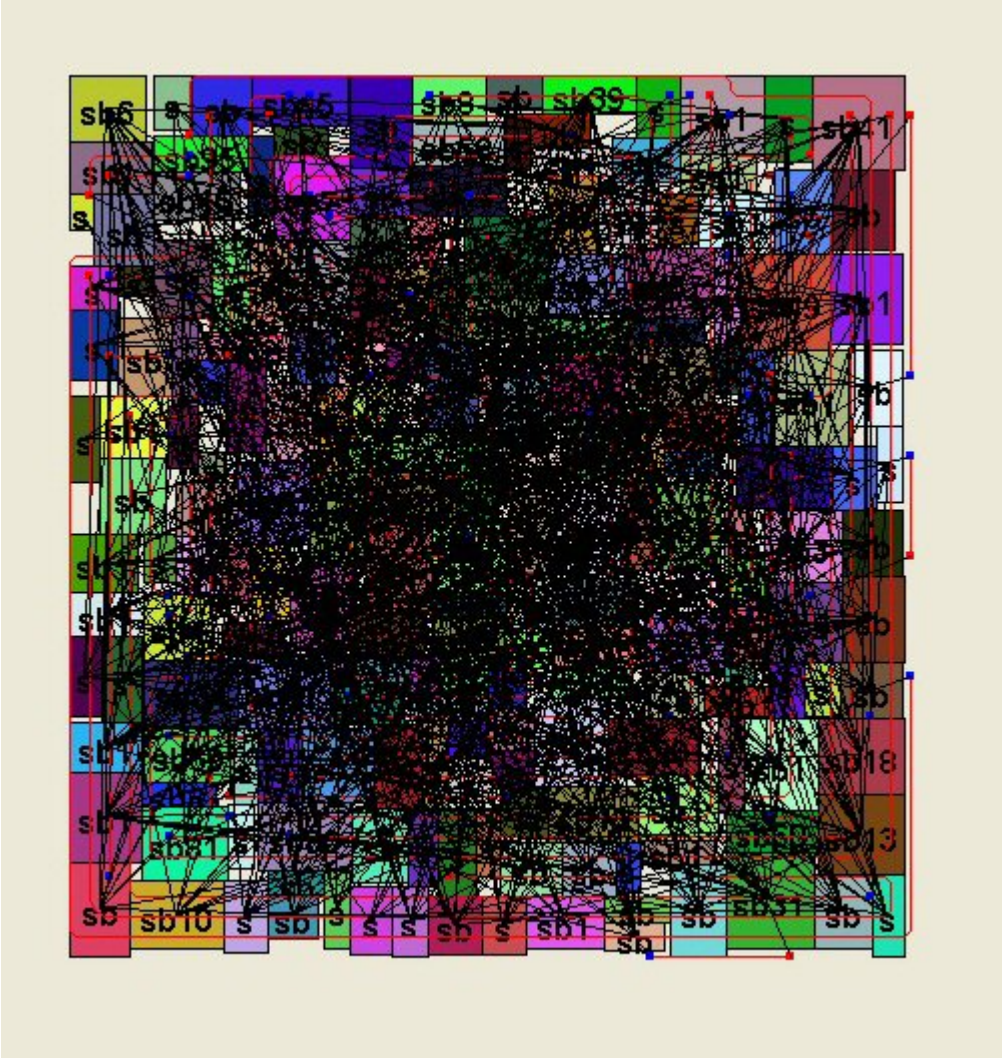

Figure 112. Optimized placement and both electrical and optical waveguide routing for n200c benchmark circuit

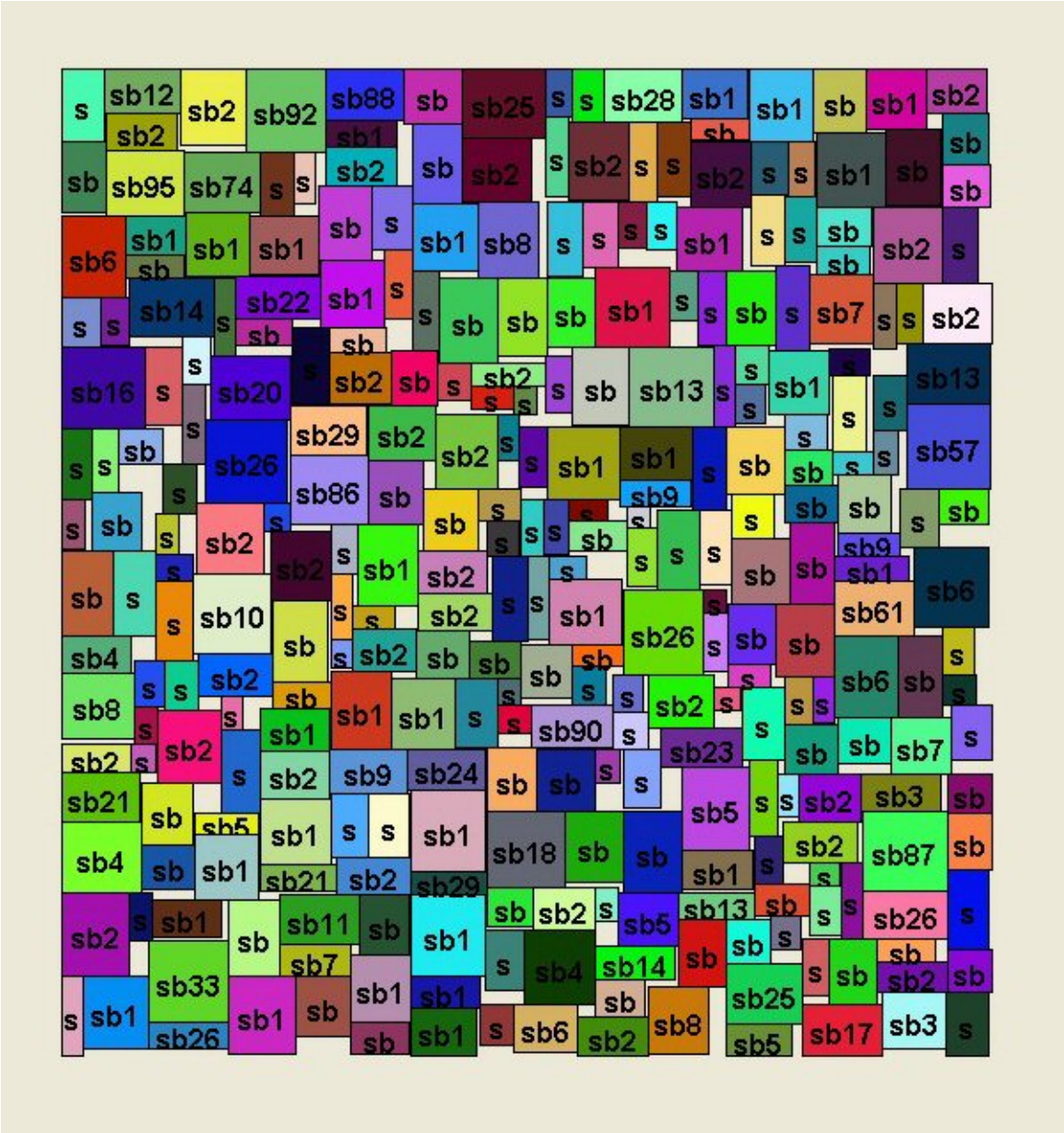

Figure 113. Optimized placement for n300 benchmark circuit

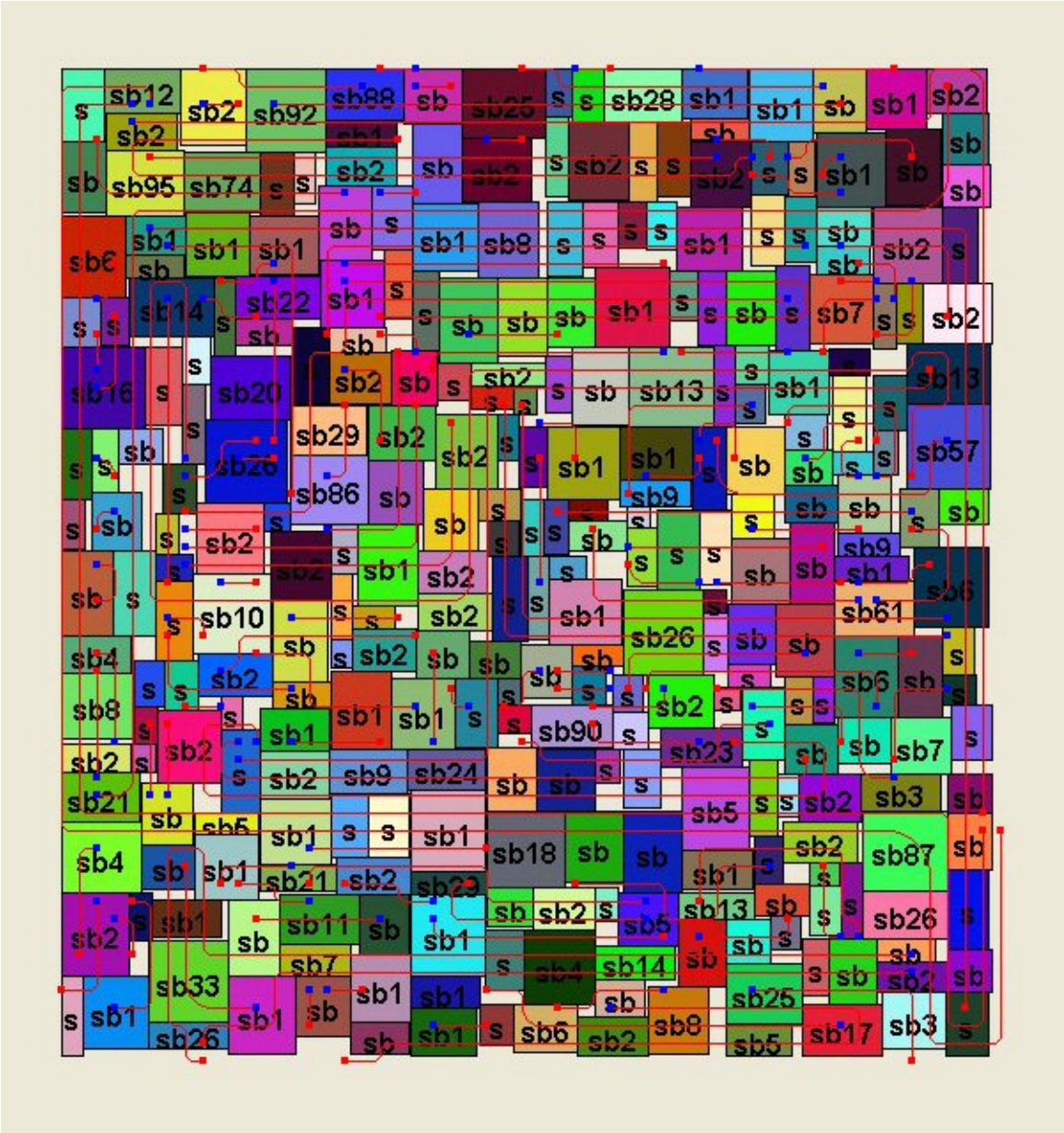

Figure 114. Optimized placement and optical waveguide routing for n300 benchmark circuit

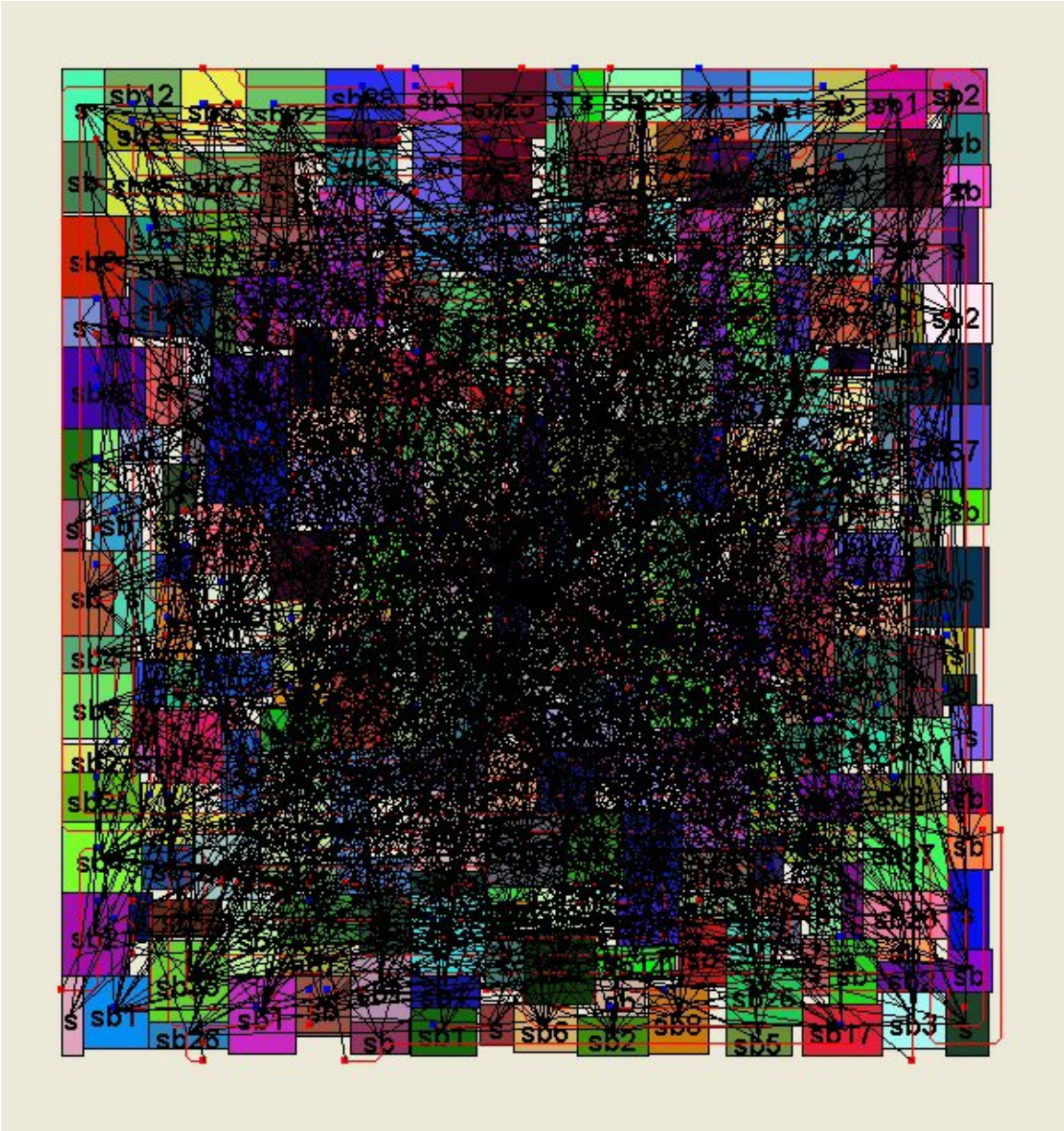

Figure 115. Optimized placement and both electrical and optical waveguide routing for n300 benchmark circuit

APPENDIX B

PUBLICATION GENERATED

[1] **Chung-Seok(Andy) Seo,** Abhijit Chatterjee and Nan M. Jokerst, "*Physical design of optoelectronic system-on-a-package: A CAD tool and algorithms*", Submitted to ISQED 2005.

[2] **Chung-Seok (Andy) Seo** and Abhijit Chatterjee, "*Efficient Routing of Board-Level Optical Clocks for Ultra High-Speed Systems*," pp. 1310-1317, IEICE Trans. On Fundamentals, 2004.

[3] **Chung-Seok (Andy) Seo**, Abhijit Chatterjee and Nan M. Jokerst, "*Physical Design of Optoelectronic System-on-a-Package Using Optical Waveguide Interconnects*," pp. 29-34, ECTC, 2004.

[4] **Chung-Seok (Andy) Seo**, Abhijit Chatterjee, Sang-Yeon Cho and Nan M. Jokerst, "*Design and Optimization of Board-Level Optical Clock Distribution Network for High-Performance Optoelectronic System-on-a-Packages*," pp. 292-297, GLSVLSI, 2004.

[5] **Chung-Seok (Andy) Seo**, Abhijit Chatterjee and Timothy J. Drabik, "*Optically Interconnected Intelligent RAM Multiprocessor: Gigascale Opto-IRAM*," pp. 256-260, CATA, 2004.

[6] **Chung-Seok (Andy) Seo** and Abhijit Chatterjee, "*Optimization of Board-Level H-tree Optical Clock Distribution*," pp. 609-611, ITC-CSCC, 2003.

[7] **Chung-Seok (Andy) Seo** and Abhijit Chatterjee, "*Free-Space Optical Interconnect for High-Performance MCM Systems*," pp. 294-298, IWSOC, 2003.

[8] **Chung-Seok Seo**, Abhijit Chatterjee and Timothy J. Drabik, "*Wiring Optimization for Propagation Delay and Reduced Power Consumption in Multichip Modules with Free-Space Optical Interconnect*," pp. 1-6, ECTC, 2003.

[9] Jaemin Shin, **Chung-Seok Seo**, Ananth Chellappa, Martin Brook, Abhijit Chatterjee and Nan M. Jokerst, "*Comparison of Electrical Interconnect and Optical Interconnect*," pp. 1067-1072, ECTC, 2003.

[10] **Chung-Seok Seo** and Abhijit Chatterjee, "*A CAD Tool for System-on-Chip Placement and Routing with Free-Space Optical Interconnect*," pp. 24-29, ICCD, 2002.

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[7] J. W. Goodman, F. J. Leonberger, S. Y. Kung, and R. A. Athale, "Optical interconnections for VLSI systems," Proc. IEEE, col. 72, no. 7, pp. 850-866, Jul. 1984.

[8] D. A. Miller, *et al*, "Bandedge electro-absorption in quantum well structures: The quantum confined stark effect," Phys. Rev. Letter, vol. 53, pp. 2173-2177, 1984.

[9] H. Soda, *et al*, "GaInAsP-InP surface emitting injection-lasers," Jpn. J. Appl. Phys., vol. 18, pp. 2329-2330, 1979.

[10] J. L. Jewell, *et al*, "Low-threshold electrically pumped vertical-cavity surface-emitting microlasers," Electron. Letter, vol. 25, pp. 1123-1124, 1989.

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