Comprehensive Assessment of Fault-Resilient Schemes Based on Energy Storage Integrated Modular Converters for AC-DC Conversion Systems

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Abstract—Due to the scalability and flexibility of various modular power electronic converters, integrating split energy storage components (such as batteries and supercapacitors) is feasible and attractive. This paper investigates the operational and economic characteristics of different ac/dc fault-resilient schemes using energy storage integrated modular converters in ac-dc conversion applications. Based on the topological features between the energy storage system (ESS) and the ac and/or dc system, four energy storage based modular converter deployment schemes are presented. Through a case study, operational performance including fault isolation and power compensation under extreme ac/dc fault conditions are verified using time-domain simulation. System losses are evaluated, whereas detailed design considerations, major component usage and estimated capital costs are articulated. The four schemes are compared and selection guidelines are presented. In general, the schemes with independent ESSs would be preferable for such ac-dc conversion applications due to their high operational flexibility.

Index Terms—AC-DC power conversion, energy storage, modular converters, system faults.

I. Introduction

Energy storage systems (ESSs) are promising and critical in construction, regulation and reinforcement of various electric systems. For power systems, ESSs are participating in power flow management, transient disturbance elimination, and peak power shaving [1]–[3]. For electrified transportation, advanced vehicles, ships and aircraft need effective ESSs to improve controllability and performance [4], [5].

With fast response and desirable controllability, batteries and supercapacitors are mainstream among stationary energy storage technologies [3]. However, any mismatch of voltage or power rating between the available storage modules and various electric systems may jeopardize security, stability, and efficiency. Also, compatible operation of the storage elements requires effective management systems for monitoring, controlling and fault-tolerance. Thus, although different energy cell management systems have made series-connected cell strings applicable [6]–[8], massive energy storage integration into medium and high voltage systems remain challenging for renewable energy utilization and power system security.

In ac grid applications, the energy storage integrated STATCOM has been implemented with a modular multilevel converter (MMC) and centralized dc-bus supercapacitors; it can provide both frequency and voltage supports to the tied ac grid [9]. Rather than centralized integration, modular converter topologies with floating power electronic submodules (SMs) enable scalable and reliable ESS construction at different power and voltage levels. The method of integrating split energy storage elements (ESEs) into the cascaded H-bridge (CHB) has been proposed in [10], where essential design considerations, grid-tied control systems and voltage balancing have been investigated and verified in [11]–[19].

For ESS deployment in dc systems, topologies adopting half-bridge SMs or other types for dc systems have been investigated in [20]–[24]. Also, dual-stage transformer-based dc-dc converters can be used, whereas galvanic isolation improves dc fault ride-through capability [25]–[27].

Another influential ESS type based on MMC was proposed in [28], where power flow can be regulated flexibly among the connected ac and dc grids, and the integrated energy storage components. The MMC is a suitable candidate to integrate bulk dc power systems with energy storage in order to mitigate power fluctuation of massive renewable sources [29], [30]. This configuration can also be used as a transient power conditioner and electric motor drive [31]–[33]. The MMC with energy storage requires systematic internal regulation, which is articulated in [34]–[37]. To isolate dc faults, inner SMs can be full-bridge (FB) based, hybrid and/or other types [38]–[40].

In terms of ESS functionality, recent publications generally aim to provide back-up active and reactive power within ac networks for frequency/voltage management and system dispatch, where half-bridge (HB) MMC and CHB-based ESSs (modelled as controllable ac voltage sources) have been mainly assessed [41]–[44]. For ESS equipment, losses calculation, reliability comparison and energy storage management are the main focus as in [41], [44], [45]. It has been gradually and widely recognized that modular converters are able to provide better scalable, reliable and controllable integration schemes.

Power converter resiliency against faults, which cause fluctuated and even disrupted power transfer, is essential for system stability, reliability and security. The feature of zero-crossing current facilitates ac system protection and instantaneous power theory enables mature ac fault ride-through technologies for voltage source converters (VSCs) [46], [47]. Although dc-fault ride-through with modular converters transformed into the STATCOM is widely accepted as in [48], dc-fault resiliency of ESS-based systems is not discussed in depth. Also, dc fault isolation, as reported, depends highly on extensive utilization of fully-controllable semiconductors, such as using hybrid dc circuit breakers (DCCBs) or MMCs at medium and high voltage levels [40], [49]. As shunt-connected ESSs add extra power converters in parallel with the original ac-dc conversion system, more power

compensation than the rated can be provided for their connected system; however, they cannot participate in fault isolation of the ac-dc conversion stage. Also, to fulfil both ac and dc side power support during dc and ac faults respectively, both ac and dc shunt ESSs are required, leading to higher capital costs. Therefore, the major research gap is that the performance and configuration of different ESS-based ac-dc conversion systems with the ac/dc fault resilient feature have not been assessed and compared.

This paper investigates energy storage integrated modular converter deployment with improved system fault resiliency in bidirectional ac-dc conversion applications. Four energy storage integrated converter schemes which are able to ride-through both ac and dc side faults are presented. A case study with detailed design is used for assessment. Time-domain simulations are given to verify the fault-resilient capability in both ac and dc fault cases. System normal operation losses are evaluated. Also, essential design aspects, component usage and capital cost are articulated and compared. Based on the case study, key characteristics and selection guidelines are given.

The paper is organized as follows. Section II presents fundamentals of constructing modular converters and four system schemes with basic operation characteristics. Section III evaluates different schemes based on a case study, including simulation verification, losses calculation, ESE design, component usage and cost estimation. Section IV concludes the study.

II. MODULAR CONVERTERS AND SYSTEM SCHEMES

Topologically, the fault-resilient ac-dc conversion system is based on various energy storage integrated modular converters, which are constructed using different energy storage components, semiconductor switches and passive components. This section will present the basic ESE configuration, modular chain structure, and four fault-resilient schemes.

A. Energy Storage Elements (ESEs)

Depending on operational circumstances and performance requirements, the ESE which is to be integrated is constructed by the main storage component such as battery, supercapacitor or the combination, and the auxiliary circuit. Two major design aspects, namely, voltage rating (mainly related to normal operation) and current profile (mainly related to safety, aging and performance degradation), should be considered. Proper circuits within the ESE that interface the energy storage component and the main power electronic modules are usually suggested as shown in Fig. 1. The passive circuit in Fig. 1(a) is simple in terms of design and operation [50]–[53]. However, the targeted SM is required to have the same voltage rating as the main storage component, hence SM voltage variation exists
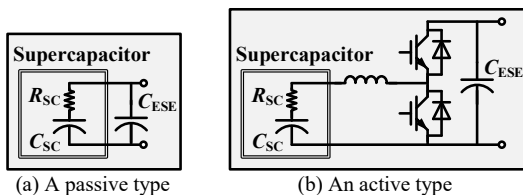
depending on the energy storage component SoC. If the ESS is used for periodic power applications (such as ac systems), the interfacing circuit is suggested to attenuate the ac components in order to reduce current ripple stresses on the main storage component [51]. To obtain the controllable ESE output voltage, different active circuits have been investigated in [35], [54]–[58], where the most usual practice is using the bidirectional dc-dc converter, as the example in Fig. 1(b). This method introduces a new degree of freedom in terms of configuration, optimization and control, but increases semiconductor usage, cost and design complexity [59], [60].

B. Modular Converter Chain Structure

The basic principle of building the modular converter is to match the connected system by synthesizing ac and/or dc voltages using modular chains constructed by unipolar and/or bipolar SMs [61]. Using modulation techniques for multilevel converters such as pulse width or nearest level modulation, the chain can generate high-quality waveforms and present high modularity, redundancy and scalability.

ESEs are usually integrated into the converter chains in a full and equal manner, featuring unified design, operation and control. The ESEs can also be partially integrated into the converter chains. For example, the MMC with energy storage proposed in [62] is implemented by the partially rated storage method within one MMC arm. Different methods of asymmetrical ESE integration into MMC arms/legs have been analyzed in [63]. However, in order to utilize the stored energy of ESE-based SMs, additional arm current manipulation is involved causing larger distortion and/or higher current peaks. Although all these operation approaches are feasible for modular chains and modular converter based ESSs in general, the partial integration is just a trade-off between voltage (lower voltage due to partially-used SMs) and current (higher current due to harmonics injection) ratings, while the overall required power rating cannot be compromised. Therefore, for simplicity, this study assumes that the ESEs are integrated into the targeted modular chain/converter in a consistent and identical way.

IGBT-based HB, FB and mixed-bridge (MB, a combination of HB and FB SMs) chains are typical choices for modular converter construction and split ESE integration, as shown in Fig. 2. Chains A and B consist of HBs without and with ESEs respectively. These HB-based chains can only be safely used in a dc system, while it generates dc power in steady state. The FB chain (Chain-C) is mainly for ac systems with an ac output
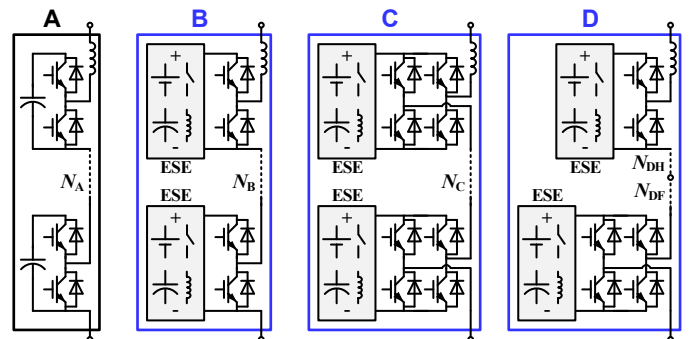

Fig. 1. Two typical ESE implementations.

(a) A passive type   (b) An active type

Fig. 2. Modular chains A, B, C and D for modular converter construction.

(a) ES-HB-MMC with DCCBs (Scheme-I)

(b) ES-MB-MMC (Scheme-II)

(c) HB-MMC with AC-Series ESS (Scheme-III)

(d) HB-MMC with DCCBs and DC-Shunt ESS (Scheme-IV)

Fig. 3. Energy storage based system schemes with ac and dc fault resiliency.

modular feature of the MB-MMC can be utilized to integrate ESEs, thus, the energy storage based MB-MMC (ES-MB-MMC). This scheme represents a typical trade-off between dc-fault resiliency and semiconductor usage (operation losses). In this study, HB and FB SM numbers (N_{DH} and N_{DF}, respectively) within Chain-D are assumed to be equal [40].

3) Scheme-III: The scheme diagram is shown in Fig. 3(c), where the conventional HB-MMC based on Chain-A operates for normal ac-dc conversion, and in its ac side, a series-deployed ESS (AC-Series ESS) constructed by Chain-C is used and can be activated to synthesize ac voltage and compensate power during faults [64]. To minimize conduction losses, the AC-Series ESS can be bypassed in normal operation cases similar to the DCCB (with a disconnector and auxiliary IGBTs) [65].

4) Scheme-IV: As illustrated in Fig. 3(d), the Chain-A based HB-MMC also offers the simplest topology for ac-dc conversion. In the HB-MMC dc side, a DC-Shunt ESS (Chain-B) is deployed to provide dc power support [22]; whereas DCCBs are used to ensure fast dc fault isolation and ESS normal operation [49]. The DC-Shunt ESS output current can be controlled to smooth system dc-side current, and ESEs can

TABLE I
PARAMETERS OF AC-DC CONVERSION SCENARIO

Items	Values	Items	Values
Rated power	20 MW	AC system frequency (f_0)	50 Hz
DC voltage (V_{DC})	20 kV	AC L-L rms voltage (V_{AC})	11 kV
DC line inductance	200 μH	AC transformer (Y/Δ) ratio	11:10
DC line resistance	100 mΩ	AC transformer inductance	0.18 pu
DC line capacitance	100 nF	AC transformer resistance	0.01 pu

TABLE II
PARAMETERS OF SCHEMES I-IV AS THE BENCHMARK

Schemes	Items	Values
Scheme-I	DCCB breaking time	2 ms
	DCCB disconnector closed resistance	1 mΩ
	Chain-B inductance & resistance	0.15 pu, 0.01 pu
	ESE SM No. per Chain-B (N_B)	40
	ESE SM rated voltage (V_{ESE})	500 V
	ESE supercapacitor series and parallel No.	188, 24
	ESE capacitor (C_{ESE})	26.7 mF (40 ms)
Scheme-II	Chain-D inductance & resistance	0.15 pu, 0.01 pu
	ESE SM No. per Chain-D (N_{DH}, N_{DF})	20, 20
	ESE SM rated voltage (V_{ESE})	500 V
	ESE supercapacitor series and parallel No.	188, 24
	ESE capacitor (C_{ESE})	26.7 mF (40 ms)
Scheme-III	HB-MMC SM No. per Chain-A (N_A)	40
	HB-MMC SM capacitance	26.7 mF (40 ms)
	Chain-A inductance & resistance	0.15 pu, 0.01 pu
	Bypassing disconnector breaking time	2 ms
	Bypassing disconnector on-state resistance	1 mΩ
	ESE SM No. per FB Chain-C (N_C)	20
	ESE SM rated voltage (V_{ESE})	500 V
	ESE supercapacitor series and parallel No.	188, 96
	ESE capacitor (C_{ESE})	106.7 mF (40 ms)
Scheme-IV	DCCB breaking time	2 ms
	DCCB disconnector closed resistance	1 mΩ
	HB-MMC SM No. per Chain-A (N_A)	40
	HB-MMC SM capacitance	26.7 mF (40 ms)
	Chain-A inductance & resistance	0.15 pu, 0.01 pu
	ESE SM No. per FB Chain-B (N_B)	40
	ESE SM rated voltage (V_{ESE})	500 V
	ESE supercapacitor series and parallel No.	188, 144
	ESE capacitor (C_{ESE})	20 mF (5 ms)
	Chain-B filtering inductance	1 mH

power; also, it has full protection ability if used in a dc system. The MB chain (Chain-D), determined by the ratio of HB and FB SMs, is generally deployed in a dc system with limited protection capability. The ESE management system is implemented by the combination of ESE internal monitoring and regulating circuits and the chain-level control over typical factors such as the average state-of-charge (SoC), power flow, etc. For all chains, redundancy is applicable and faulty SMs can be bypassed and removed from the main power conversion process.

C. Fault-Resilient Schemes

Using the previously discussed modular chains A to D, four viable modular converter based schemes can be constructed to interconnect the dc and ac systems (S_{DC} and S_{AC}, respectively), with ac and dc fault resilient capabilities, as in Fig. 3.

1) Scheme-I: The schematic diagram is shown in Fig. 3(a). Based on the Chain-B, an energy storage based HB-MMC (ES-HB-MMC) can operate for ac-dc conversion and provide power support for ac and dc sides [28]. The DCCBs can ensure fast dc fault isolation [49].

2) Scheme-II: As shown in Fig. 3(b), FB SMs within the Chain-D enable dc fault isolation without DCCBs, and inherent
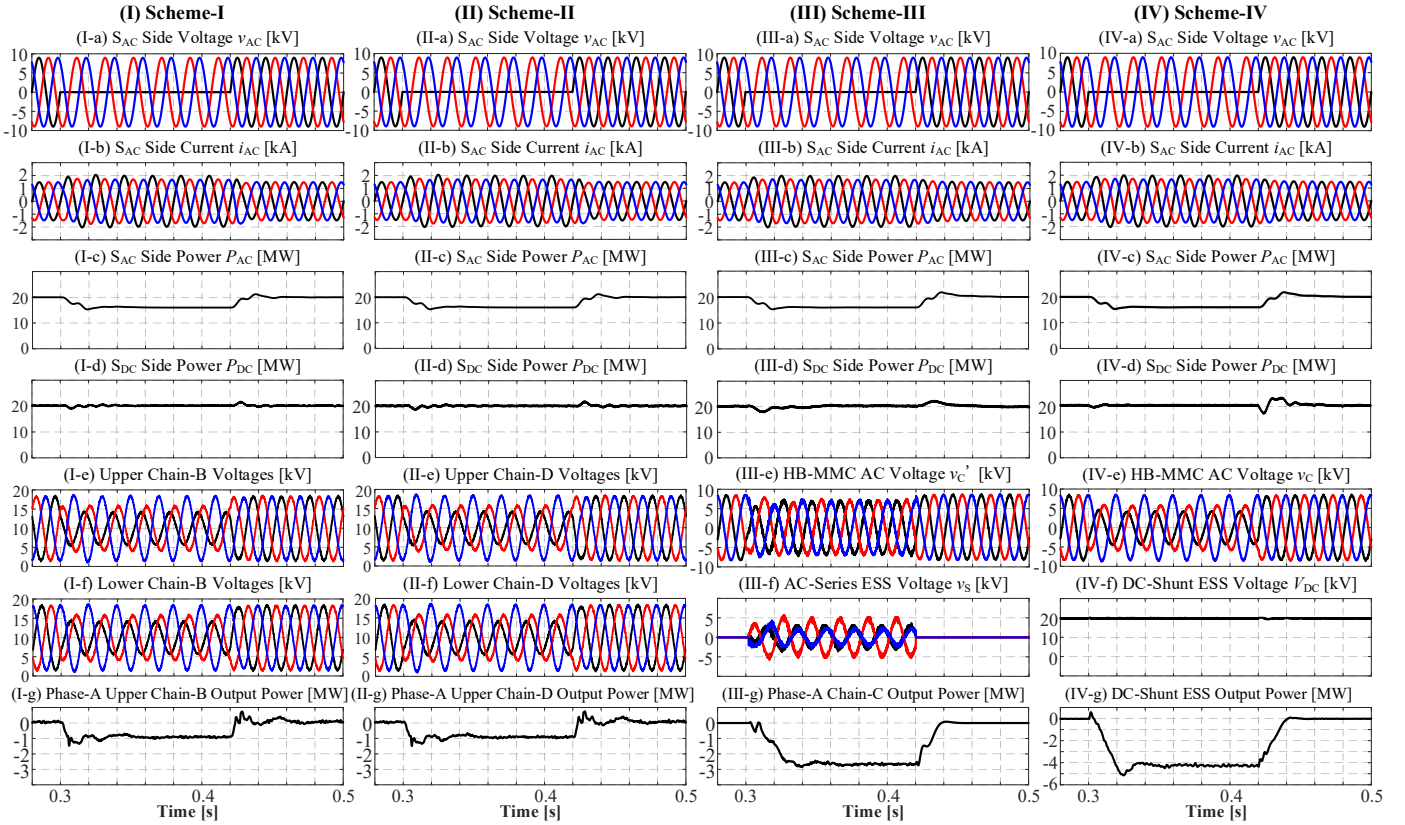
Fig. 4. AC-Fault resiliency of schemes I-IV.

be flexibly blocked in dc fault cases before the DCCBs are open.

III. CASE STUDY

The performance of the presented schemes will be evaluated, in terms of fault resiliency, operation losses and realistic ESE configurations. Then, practical-oriented component usage, cost estimation and related design considerations will be given.

A. Benchmark

Major parameters of the targeted ac-dc conversion system are given in Table I, where four schemes are configured to achieve both ac-dc conversion and enhance system ac/dc fault resiliency using the energy storage. Normally, systems operate to deliver 1pu active power from the S_{DC} to S_{AC} (defined as the positive direction) with unity power factor.

Detailed parameters of the schemes are given in Table II. The modular converters, DCCB, and ac bypassing circuits are assumed to be realized by the Infineon IGBT (FF1400R12IP4 [66]), with the PWM frequency at $40f_0$. The basic ESE is assumed to be implemented with parallel connection of the Maxwell supercapacitor (BCAP0100 P270 S07 [67]) and conventional electrolytic capacitors C_{ESE}, considering the basic operation requirements, power ratings, and voltage/current constraints. For clarity, ESEs are directly connected into the modular converter SMs without more semiconductor-based circuitry herein. This ESE configuration, as shown in Fig. 1(a), represents the simplest and generic type, which has been

reported as applicable for both ac and dc ESSs [16], [18], [19], [23]. For all the studied schemes, the ESE stored energy is configured the same. In order to compensate the lost/disrupted power during both extreme ac and dc fault events, the overall power rating of the integrated ESS should be the same as the rated power of the ac-dc conversion system.

B. Time-Domain Simulation

MATLAB/Simulink-based models are used to validate the resiliency of the studied schemes against faults. System performance is presented in this subsection.

1) AC-Side Fault

A nearby single phase to ground solid short circuit fault, which is the most common ac fault type with partial power interruption, is used to verify the effectiveness of ac fault resiliency. System performance of the schemes in the ac fault case is shown in Fig. 4. The S_{AC} fault occurs at 0.3 s and lasts for 120 ms as shown in Fig. 4 I-IV(a). The VSC ac-side current is controlled to avoid over-current; whereas the rated ac-side power injection is affected, as in Fig. 4 I-IV(b) and (c). For schemes I and II, ES-HB-MMC and ES-MB-MMC are able to store the power that cannot be injected into S_{AC}, dc powers from S_{DC} exhibit negligible interruption, see Fig. 4 I-II(d)-(g). For Scheme-III, the operation of the HB-MMC and AC-Series ESS achieves near constant dc-side power flow during the fault, with minor power variation while switching its state, as displayed in Fig. 4 III(d)-(f). The AC-Series ESS absorbs the extra dc power, as shown in Fig. 4 III(g). For Scheme-IV, although the HB-
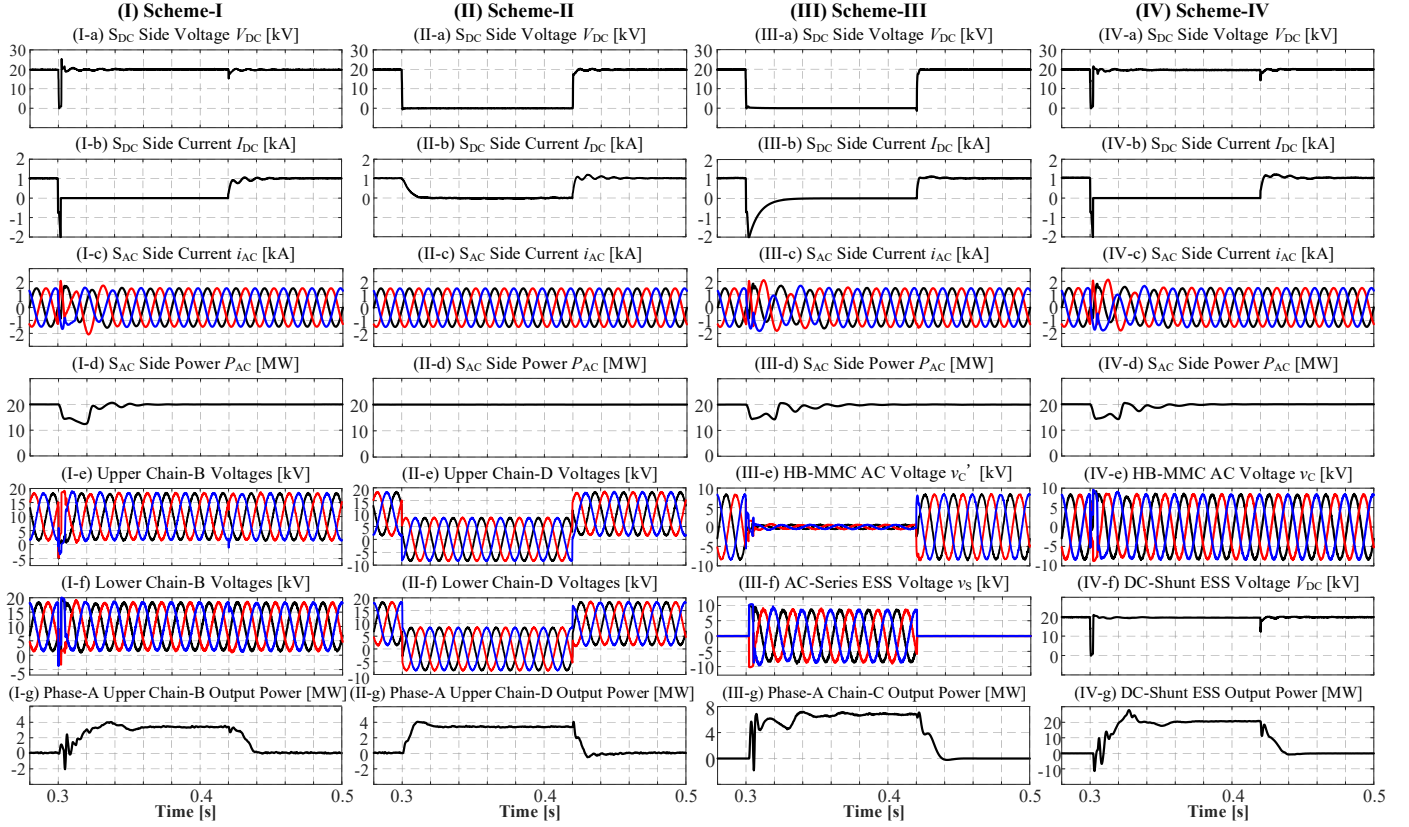
Fig. 5. DC-Fault resiliency of schemes I-IV.

MMC reduces dc power consumption due to the ac fault, the DC-Shunt ESS is activated to ensure unaffected dc-side voltage (and current), as displayed in Fig. 4 IV(c)-(f). This is achieved by sinking the extra dc power, see Fig. 4 IV(g). All schemes attain normal operation when the fault is cleared.

2) DC-Side Fault

A pole-to-pole solid short circuit fault in S_{DC}, with all power disrupted, represents the most severe system fault case in the ac-dc conversion system. Then, the (properly-sized) energy storage within the conversion system is required to provide rated power for the normal ac side, therefore, S_{AC} security can be significantly increased. Fig. 5 shows system performance during the dc fault which occurs at 0.3 s and is cleared at 0.42 s. In Scheme-I, although the ES-HB-MMC SMs are blocked, fault current (from both dc and ac sides) flows into the fault site through the dc line; DCCBs isolate the faulty section after 2 ms, see Fig. 5 I(a) and (b). The ac-side current is temporarily uncontrolled and normal power flow is affected, see Fig. 5 I(c). After the dc fault is blocked, the ES-HB-MMC is able to synthesize voltage to maintain ac current and dc-terminal voltage using the MMC ac and dc loops, and to provide power for the ac-side after a short stabilization period, as shown in Fig. 5 I(d)-(g). The ES-HB-MMC attains the original operation when the dc fault is cleared. In Scheme-II, the ES-MB-MMC can isolate its ac side and the faulty dc side with the Chain-D, with its dc terminal dropping and dc current decaying, see Fig. 5 II(a), (b), (e) and (f). During the dc fault, the ac currents are tightly controlled and the ac power transfer is maintained

smoothly using the Chain-D, as shown in Fig. 5 II(c), (d) and (g). The dc-link pole-to-pole voltage of the HB-MMC in Scheme-III drops due to the dc fault, and dc current flows from the ac to dc side in the first 2 ms and drops in one cycle, with the HB-MMC arms bypassed and AC-Series ESS chains activated (bypassing disconnectors are switched off in 2 ms), see Fig. 5 III(a) to (c). Then, the AC-Series ESS synthesizes ac-side voltage, controls ac current, and compensates S_{AC} power, while the HB-MMC arms are bypassed. The ac power transfer is stabilized after 3-4 cycles, see Fig. 5 III(c)-(g). Normally, the DC-Shunt ESS SMs in Scheme-IV can be blocked, and when the fault occurs, the HB-MMC in Scheme-IV suffers from the fault for a short duration. This is similar to Scheme-I, as shown in Fig. 5 IV(a) and (b). After the DCCB fault isolation, HB-MMC retains its operation by synthesizing ac voltage and controlling ac current, thereby injecting power into S_{AC}, see Fig. 5 IV(c)-(e). The DC-Shunt ESS can generate dc voltage and provide the required dc current/power, as shown in Fig. 5 IV(f) and (g). As schemes III and IV adopt the same conventional HB-MMC configuration and control, ac grid side dynamics are basically the same, with minor differences due to the active power sources.

C. Normal Operation Losses

System long-term operation efficiency should be quantified, which is critical for system operator capital interests. Therefore, this subsection assesses major component steady-state losses of the benchmark schemes during normal operation.

The modular converter based systems involve complicated operation and a large number of switches. Some basic and reasonable approximations/assumptions for the losses estimation are [68], [69]: 1) The power converter operates with constant dc voltage/current and sinusoidal ac voltage/current; 2) The MMC modulation signal is sinusoidal; 3) Losses are equally distributed among ESEs/SMs/arms/phases, ac bypassing circuits, or DCCBs; 4) Switch characteristics, under typical conditions, can be linearly and piecewise represented; 5) Supercapacitor operating condition is as the initial and the typical ESR_{DC} is used as the internal resistance; and, 6) Other passive components, such as capacitors, snubbers, and reactors, are not considered.

In generally, forward conduction voltage drops V_{CE} (and V_D) of the IGBT (and its diode) can be represented as [70]:

$$V_{CE} \approx V_{CE0} + R_1 i_C \qquad (1)$$
$$V_D \approx V_{D0} + R_2 i_D \qquad (2)$$

where, V_{CE0}, V_{D0}, R_1 and R_2 are constants based on the piecewise characteristics under typical conducting conditions in [66]; and i_C and i_D are the corresponding device currents in different devices/schemes, such as the equivalent SM switch currents, dc currents (for DCCBs) and ac currents (for ac bypassing circuits). The switching energy losses of the IGBT turn-on, turn-off and diode (E_{Ton}, E_{Toff} and E_D respectively) can also be linearly represented as:

$$E_{Ton} \approx (K_{Ton} i_C)(V_T / V_{T0}) E_{Ton0} \qquad (3)$$
$$E_{Toff} \approx (K_{Toff} i_C)(V_T / V_{T0}) E_{Toff0} \qquad (4)$$
$$E_D \approx (K_D i_D)(V_T / V_{T0}) E_{D0} \qquad (5)$$

where, V_{T0}, K_{Ton}, K_{Toff}, K_D, E_{Ton0}, E_{Toff0} and E_{D0} are nominal constants and typical results of the switching losses tests obtained from datasheet [66]; variables i_C, i_D and V_T indicate the current and voltage conditions during switching.

For the studied schemes, major components to be considered are as follows:

1) Modular Converter IGBTs: Due to the same ac-dc conversion scenario, the MMC arm currents are the same in all schemes, with a dc component ($\frac{1}{3}I_{DC}$) plus a first-order ac component ($\frac{1}{2}i_{AC}$); whereas the modulation index (with the magnitude being about 81.65% in this case) is also the same. Thus, conduction losses can be estimated by integrating the product of switch conduction current and voltage, using (1) and (2), based on the approach in [70]. The time-averaged switching losses of the switch (IGBT on/off states and diode off state) are calculated based on (3)-(5), as in [71]. Under normal operating conditions, SMs of the AC-Series ESS in Scheme-III can be bypassed [64], and the DC-Shunt ESS in Scheme-IV can be blocked [26]; therefore, negligible losses are incurred.

2) ESEs and ESSs: ESEs within the SMs of schemes I and II serve as energy buffers even during normal operation, leading to partial charge and discharge losses. For the passive circuit based ESE of the benchmark, the ac current through the supercapacitor (capacitive plus resistive impedance), which is in parallel with the conventional capacitor (one capacitive impedance), can be calculated using the Kirchhoff's rules when the ESE is conducting currents (shared by the capacitor and supercapacitor [72]). Hence, the losses due to supercapacitor internal resistance can be estimated by obtained current rms

TABLE III
MAJOR COMPONENT LOSSES OF SCHEMES I-IV IN THE NORMAL OPERATION

Schemes	Items	Losses [kW]	Percentage
Scheme-I	DCCBs	14.80	2.9%
	ES-HB-MMC IGBTs (conduction)	195.90	39.0%
	ES-HB-MMC IGBTs (switching)	2.54	0.5%
	ES-HB-MMC ESEs (63 mΩ Each)	288.59	57.5%
	Total	**501.83**	100%
Scheme-II	ES-MB-MMC IGBTs (conduction)	299.82	50.7%
	ES-MB-MMC IGBTs (switching)	2.54	0.4%
	ES-MB-MMC ESEs (63 mΩ Each)	288.59	48.8%
	Total	**590.95**	100%
Scheme-III	HB-MMC IGBTs (conduction)	195.90	93.1%
	HB-MMC IGBTs (switching)	2.54	1.2%
	AC-Series ESS bypassing circuits	11.99	5.7%
	AC-Series ESS SMs (bypassed)	0	0%
	AC-Series ESS ESEs (bypassed)	0	0%
	Total	**210.43**	100%
Scheme-IV	DCCBs	14.80	6.9%
	HB-MMC IGBTs (conduction)	195.90	91.9%
	HB-MMC IGBTs (switching)	2.54	1.2%
	DC-Shunt ESS SMs (blocked)	0	0%
	DC-Shunt ESS ESEs (blocked)	0	0%
	Total	**213.24**	100%

values at f_0 and $2f_0$. ESEs within the AC-Series and DC-Shunt ESSs in schemes III and IV respectively, do not participate in power conversion nor energy storage under normal operating conditions, while supercapacitor leakage current is negligible.

3) DCCBs (Schemes I and IV) and AC Bypassing Circuits (Scheme-III): For the four schemes during normal ac-dc conversion, dc (I_{DC}) and ac (i_{AC}) side currents are the same. Also, in the closed/bypassing status, the DCCB and ac bypassing circuit have the same circuitry configuration with series connection of two IGBTs and a disconnector [49], [65]. Hence, IGBT conduction losses are the same as above and the disconnector can be considered as a resistor.

Summarized normal operation losses results of the studied schemes are shown in Table III, from which the estimated normal operation efficiencies (with the previous major component considered) are 97.49%, 97.05%, 98.95% and 98.93% respectively. For schemes I and II, about half the total losses are caused by continuously charging and discharging the ESE during normal ac-dc conversion. Also, Scheme-II has higher losses than the HB-MMC based counterpart (Scheme-I), mainly due to the FB SMs conduction losses of Chain-D. Schemes III and IV show similarly high efficiencies as their ESS parts are either bypassed or blocked under normal operating conductions, which would be desirable for long-term efficiency.

D. ESE Configuration Analysis

Based on the loss assessment, ESE configuration considerations for different schemes are now discussed.

1) Schemes I and II

The losses of schemes I and II reveal that directly connecting the main storage components into the main MMC results in high power losses due to the continuous ESEs ac current conduction. The ESE loss results are highly dependent on the shunt-connected conventional capacitor (larger capacitance leads to lower supercapacitor losses). However, the 40 ms

TABLE IV
COMPONENT USAGE AND CAPITAL COST OF SCHEMES I-IV

Schemes	Parts	Major Components	Amount [pcs]	Price [$/pcs]	Cost [k$]	Percentage	Total Cost [k$]
Storage	ESEs	Supercapacitor cell	1082.9k	2.5	2707	100%	2707
Scheme-I	DCCB	$IGBT_1$	84	700	58.8	6.6%	884.8
		Disconnector	2	5000	10	1.1%	
	ES-HB-MMC (6 Chain-B)	Arm inductor (2.3 mH)	6	20000	120	13.6%	
		$IGBT_1$	480	700	336	38.0%	
		ESE capacitor (26.7 mF)	240 (800 kJ)	500 (150 $/kJ)	120	13.6%	
		ESE dc-dc converter dc inductor (0.8 mH)	240	800	192	21.7%	
		ESE dc-dc converter $IGBT_2$	480	100	48	5.4%	
Scheme-II	ES-MB-MMC (6 Chain-D)	Arm inductor (2.3 mH)	6	20000	120	12.2%	984.0
		$IGBT_1$	720	700	504	51.2%	
		ESE capacitor (26.7 mF)	240 (800 kJ)	500 (150 $/kJ)	120	12.2%	
		ESE dc-dc converter dc inductor (0.8 mH)	240	800	192	19.5%	
		ESE dc-dc converter $IGBT_2$	480	100	48	4.9%	
Scheme-III	HB-MMC (6 Chain-A)	Arm inductor (2.3 mH)	6	20000	120	13.6%	883.2
		$IGBT_1$	480	700	336	38.0%	
		SM capacitor (26.7 mF)	240 (800 kJ)	500 (150 $/kJ)	120	13.6%	
	AC-Series ESS (3 Chain-C)	$IGBT_1$	240	700	168	19.0%	
		ESE capacitor (106.7 mF)	60 (800 kJ)	2000 (150 $/kJ)	120	13.6%	
		AC bypassing $IGBT_1$	6	700	4.2	0.5%	
		AC bypassing disconnector	3	5000	15	1.7%	
Scheme-IV	DCCBs	$IGBT_1$	84	700	58.8	8.0%	733.8
		Disconnector	2	5000	10	1.4%	
	DC-Shunt ESS (1 Chain-B)	$IGBT_1$	80	700	56	7.6%	
		Filtering inductor (1 mH)	1	18000	18	2.5%	
		ESE capacitor (20 mF)	40 (100 kJ)	375 (150 $/kJ)	15	2.0%	
	HB-MMC (6 Chain-A)	Arm inductor (2.3 mH)	6	20000	120	16.4%	
		$IGBT_1$	480	700	336	45.8%	
		SM capacitor (26.7 mF)	240 (800 kJ)	500 (150 $/kJ)	120	16.4%	

conventional capacitor storage time constant is usual practice and larger conventional capacitance would be undesirable. In order to obtain smoother ESE current, other passive types to filter low order current and conduct dc current can be used, but they are also unacceptably costly and bulky [30], [51].

Therefore, from the perspective of voltage output and loss minimization, the adoption of actively-controlled circuits such as bidirectional dc-dc converters may be necessary for schemes I and II [33], [59]. Taking the benchmark as an example and using the ESE design shown in Fig. 1(b), the rated power of one ESE (with an assumed 250 V rated voltage) in schemes I or II is 20 MW/240 = 83.3 kW and the ESE dc current rating is 330 A. This means that each MMC SM should be equipped with a dc inductor (to boost the voltage and smooth the current) and two IGBTs (Infineon IGBT FZ400R12KE4 adopted with low switching losses at 5 kHz [73]). To achieve ±10% current ripple, the approximate dc converter inductance is calculated to be 0.8 mH. With the active interface, the normal operating efficiency of Scheme-I could be near the same as those of schemes III and IV, whereas Scheme-II would be the lowest due to the use of Chain-D, according to the results in Table III.

2) Schemes III and IV

Due to the activation/deactivation mechanism adopted for the AC-Series ESS in Scheme-III, the previously advanced ESE configurations for long-term losses minimization could be avoided. When the ESS operates during faults, its SMs and ESEs carry converter ac-side currents, and this should be considered for ESS sizing as discussed in [64].

With dc output (no ac voltage/current) and simple control (no ac-related measurement/manipulation), the ESE configuration of the DC-Shunt ESS in Scheme-IV is straightforward. Therefore the ESE conventional capacitor (C_{ESE}), only for high-frequency oscillation suppression, can be reduced as in the benchmark in Table II.

For schemes III and IV with direct connection of supercapacitors/batteries and SMs, the converter chain output voltage variation caused by the SoC change of the energy storage components might be a concern. Usually, the operational component voltage range should be specified to avoid ESE overdischarge and ESS malfunction. For example, battery charge and discharge cut-off voltages should be obeyed; whereas supercapacitor voltage is required to be within its absolute maximum and minimum operational voltages. Thus, the synthesized voltage can be flexibly compensated/adjusted by the independent SMs and controllable modulation index.

E. Component Usage and Cost Estimation

In an effort to present a more practical investigation, this subsection evaluates the component usage and capital cost of the studied schemes based on the benchmark results and ESE design. Then, selected representative cost aspects will be specifically compared to analyze scheme characteristics in terms of investment.

Table IV shows the results of major component usage and cost estimation without considering redundancy, interfacing transformer, auxiliary and protective circuits. All costs are assumed to be linearly proportional to the usage with fixed prices. For all schemes, the amount of deployed supercapacitors (with 394.7 MJ storage capacity) is the same, and energy storage cost would be highly dependent on the energy capacity (duration of the ESS utilization). The price is estimated given
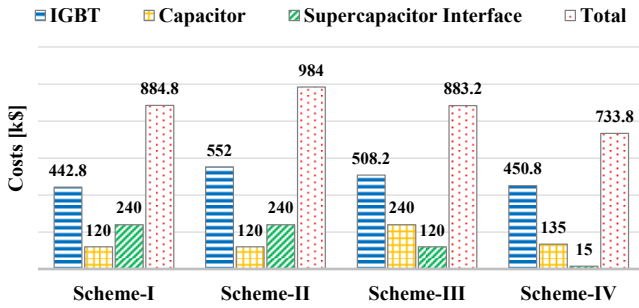
Fig. 6. Comparison of representative costs of the studied schemes.

high volume. The IGBT$_1$ (FF1400R12IP4) is used to construct the main modular converters, DCCBs and ac bypassing circuits [66]; whereas the IGBT$_2$ (FZ400R12KE4) is used for the dc-dc converter within ESEs in schemes I and II [73]. The mechanical disconnector price is estimated given the ratings and margin [74]. The capacitor and inductor prices are estimated according to [75]–[77], considering price reduction and design margins. Main observations for each scheme are as follows:

1) Scheme-I: The DCCB accounts for less than 10% of Scheme-I total cost, while modular converter IGBT$_1$ costs nearly 40% of the total cost. The use of a dc-dc converter within each SM leads to a high percentage (about 25%) of total cost.

2) Scheme-II: The FB SMs in Chain-D results in significantly increased investment on semiconductors (more than half the total). Similarly, the dc-dc converter takes 25% of the total.

3) Scheme-III: Although the HB-MMC is the main portion, the cost for extra semiconductors and capacitors of the AC-Series ESS is high (more than 30%), due to the adopted FB SMs for three-phase ac deployment.

4) Scheme-IV: The costs for the HB-MMC and DCCBs are the same as any conventional design; however, the use of the DC-Shunt ESS results in a small amount of HB SMs semiconductors and ESE conventional capacitors. Nevertheless, a high-current dc filtering reactor is needed, which increases the cost.

Fig. 6 compares selected key costs of the studied schemes. Scheme-II has the highest cost for IGBTs (including IGBT$_1$ and IGBT$_2$) due to the FB SMs and dc-dc converters. The second highest IGBT-costing scheme is Scheme-III, due to its dual-stage structure. As schemes I and II have only one modular converter (conventional ac-dc MMC), the conventional capacitor usage/cost is the lowest. However, the adoption of the dc-dc converter results in higher costs for interfacing the energy storage components. Although the costs for supercapacitor interface is avoided, more capacitors are used in Scheme-III. Nevertheless, more reactive power (ac voltage) support for S_{AC} can be provided with Scheme-III, which may justify the high investment on capacitors [65]. Scheme-IV shows the lowest investment on both capacitive storage and supercapacitor interface due to its dc-side ESS deployment. Basically, with a large number of IGBTs (for FB SMs and dc-dc converters), the highest total cost is required by Scheme-II, which is followed by Scheme-I. Scheme-III, with a dual-stage structure, has a similar total cost to Scheme-I. Comparatively, Scheme-IV features the lowest cost in total.

F. Summarized Analysis and Generic Discussion

Based on the case study, this subsection presents summarized analysis and instructive guidelines on the studied schemes in terms of several critical aspects.

1) Fault Resiliency Capability

In general, all schemes are able to significantly enhance system ac and dc fault resiliency with both essential fault isolation and uninterruptable power support. With DCCBs, schemes I and IV might be more effective for dc fault clearance, however performance and reliability of the fast mechanical disconnector would be the main concern. An alternative ac bypassing solution using static switches for Scheme-III is presented in [64], where thyristors are used. For schemes II and III, additional semiconductors would optionally be used to generate negative dc voltage, thereby further enhancing clearance ability.

2) Energy Storage Integration

Although highly dependent on the storage capacity, supercapacitor cost is high but is projected to be continually decreasing, indicating a challenging but promising prospect of such massive ESS applications. Also, for critical systems, the cost can be justified by the significant improvement in system security and resiliency.

The storage integration approaches, either using passive or active circuits, should be articulated. Schemes I and II necessitate active interface from the perspective of operating efficiency and component lifetime. However, the cost and size of the converter system increases significantly. Independent ESSs in schemes III and IV allow passive circuits, but the ESS output voltage would vary widely if using less energy storage components, which should be specifically defined/sized. Specifically, Scheme-IV allows the lowest circuit design and component usage for the split energy storage using batteries or supercapacitors due to its dc nature. However, for all schemes, certain cost trade-off between power electronic systems and energy storage components exists.

3) Operation Efficiency

Comparatively, schemes I, III and IV achieve similarly high operation efficiency under normal ac-dc conversion conditions due to the use of the HB-MMC. Scheme-II cannot avoid the trade-off between high steady-state losses and dc-fault resilient capability.

4) Capital Cost

Overall, Scheme-II has the highest cost. Costs of schemes I and III are similar. However, Scheme-III can contribute to ac system regulation with both active power and voltage support, thus, a case-by-case cost investigation should be conducted. Scheme-IV is the most cost-effective choice among the studied schemes for such energy storage applications, mainly due to its independent dc-side ESS deployment.

IV. Conclusion

This paper investigated four fault-resilient schemes I-IV of integrating split energy storage components into modular converters in ac-dc conversion applications. A comprehensive assessment based on a case study was presented. First, time-domain simulations were used to illustrate performance of bespoke features in both asymmetrical-ac and dc fault cases. Then, system losses in normal operation cases were estimated, which indicates that the energy storage components are prohibitively connected into the main ac-dc MMC SMs without an active interfacing circuit in schemes I and II. Thus, ESE design suggestions for all schemes were articulated. Hence, component usage and capital cost of the four schemes were assessed. Comparatively, although all schemes offer fault resiliency features, operation losses and capital cost could be different depending on the ESS integration, whereas a trade-off between low component usage (cost) and low ESE operation losses emerges. It could be observed that schemes with ESEs integrated into the main ac-dc MMC (schemes I and II) involve certain coupled configuration/operation between ac-dc conversion and energy storage; whereas schemes with independent ESSs (III and IV) enable a more flexible energy storage deployment arrangement. Preferably, schemes with independent ESSs are more suitable for massive energy storage applications. The findings in this paper could be used for ESS deployment in various ac/dc conversion systems to improve security.
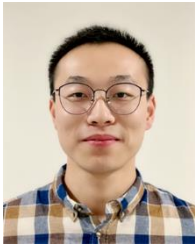
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