UNIVERSITAT POLITÈCNICA DE CATALUNYA

Design of a 16-bit 50-kHz Low-Power SC Delta-Sigma Modulator for ADC in 0.18um CMOS Technology

MASTER THESIS

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Abstract

A general purpose 16 Bits Σ-Δ modulator ADC for double precision audio 50 kHz bandwidth, targeted for Low-power operation, involving no additional digital circuit compensation, no bootstrapping techniques and resistor-less topologies, and relaying on Switched Capacitor Σ-Δ modulator topologies for robust operation and insensitivity to process and temperature variations, is presented in this work.

Designed in a commercial 180 nm technology, the whole circuit static current is calculated in 620 μA with a nominal voltage supply of 1.8 V, performing a Schreier FOM of 174.16 dB. This outstanding state-of-the-art forseen FOM is achieved by the use of architectural and circuital Low-power techniques. At the architectural level a single loop Low-distortion topology with the optimum order and coefficients have been chosen, while at circuit level very novel OTA based on Variable Mirror Amplifiers allows an efficient Class-AB operation.

Specially optimized switched variable mirror amplifiers with a novel design methodology based on Bottom-up approach, allows faster design stages ensuring feasable circuit performance at architectural level without the need of large iterative simulations of the complete SC Σ-Δ modulator. Simulation results confirms the complete optimization process and the metioned advantages with respect to the tradicional approach.

KEY WORDS- *16 Bits, 50 kHz, Low-Power, Low-Distortion, No boostrapping, Switched Capacitor Σ-Δ modulator.*

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Chapter 1

Introduction

Technological advancement and growing demands for electronic devices with advanced features is currently driving the smart sensing portable devices. In current times smart sensors are an integral part of most of the handled electronics devices, automotive and biomedical equipment, between others, that offers advanced features.

Data converters play a crucial role inside this aspect by covering the essential need of connecting the physical or analog world, with the digital world of electronics. A direct consequence of it, is a raising interest in pushing the ADCs performance, increasing the resolution and speed of conversion while reducing the power consumption and the manufacturing cost.

Smart sensor applications usually requires for low bandwidth input signals with medium to high resolution data conversions and low power consumptions. Σ-Δ modulators are a common choice in smart sensors, providing an efficient way to implement high-performance ADCs without stringent matching requirements or calibration, at expenses of increasing the oversampling ratios. Besides, Σ-Δ modulators robustness and resolution allows the integration in a wide variety of applications.

1.1 ADC Fundamentals

ADCs perform two basic fundamental operations: discretization in time and discretization in amplitude. These two functions are illustrated in Fig.1.1. The first operation of the ADCs is to discretize in time, or sample the input signal. Normally, the input signal is sampled at uniformly spaced times, at a given sampling frequency f_s, resulting in samples separated by one sampling period T_s. The result from this sampling process are impulses at each sampling time kT_s. Moreover, the sampling process limits the input signal frequency and imposes the speed requirement of the ADC.

The second operation described is the discretization in amplitude of the sampled signal, which limits the input signal accuracy and therefore the resolution of the ADC. In the operation, the ADC approximates the input signal amplitude of each sample with one of a finite number of possible values. Because the output of the ADC can only take a finite number of output values, the sampled amplitude can be represented by a digital code.

The number of discrete values M which the ADC can produce at the output determines the resolution usually expressed in number of bits N:

$$N = \log_2(M) \tag{1.1}$$

Another parameter related to the amplitude discretization is the quantization step Δ which is determined by Eq. 1.2 and represents the distance between adjacent levels. The size of the quantization step Δ depends on the full scale of the input signal ($V_{min} < V < V_{max}$) and the number of bits.

$$\Delta = \frac{V_{max} - V_{min}}{2^N} \tag{1.2}$$

As consequence of the finite number of output values in a converter, errors into the digital representation of the analog input are introduced.

These errors are called quantization errors Q_ϵ and are illustrated in Fig.1.2. The range of the quantization error in normal operation is $-\Delta/2 < Q_\epsilon < \Delta/2$, and usually is considered to have a uniform probability density function within its range. Because of that, the quantization error can be modelled as an additive white noise source, as shown in Fig.1.2a, while the power spectral density (PSD) in the range $[-f_s/2$ to $f_s/2]$ is given by

$$S_E(f) = \frac{1}{f_s}[\frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 \cdot de] = \frac{\Delta}{12 f_s} \tag{1.3}$$

Two main groups of ADCs can be classified depending on the relationship between the sampling frequency f_s and the bandwidth (BW) of the input signal to be considered. The first group are named Nyquist ADCs and their sampling frequencies follows the Nyquist theorem, where f_s is chosen to be equal to twice the signal bandwidth. While the second group are the Oversampling ADCs in which the sampling frequency is higher than the previous case. The idea behind is to crease the sampling frequency in order to trade it off with a significant reduction of the quantization noise.

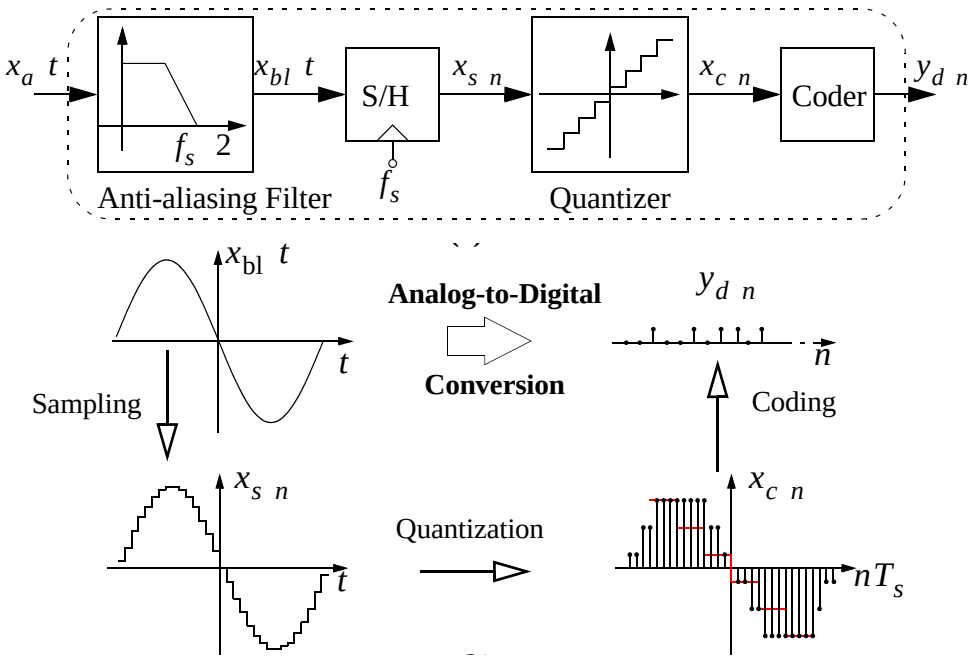
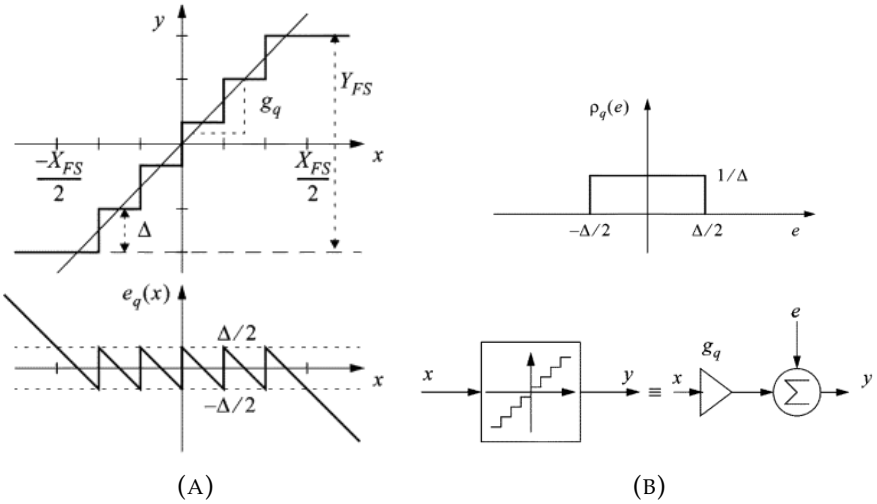


FIGURE 1.1: ADC basic block diagram and Analog-to-Digital conversion process.

Fig.1.2b represents the equivalent Quantizer block diagram, including the quantizator intrinsic gain g_q and quantization error as an input. This block is latter used in the extraction of the modulator transfer functions.



(A) (B)

FIGURE 1.2: (*A*) 6-level quantizer characteristic and its quantization error, (*B*) equivalence of the quantizer block diagram with its simplified linear model accounting for the injection of a uniformly distributed white noise.

1.2 ADC architectures

The vast majority of ADC architectures used nowadays have been discovered and published between the 40s and 60s [12]. Improvements in technology and in the optimization processes have made possible to increase the performance.

The ADC could be classified in terms of resolution, speed of conversion, mode of operation, internal structure, input/output type of signal, power consumption and others. The list provided below reflects what is traditionally known for each type of ADC, however must not be taken "as is" since research on this field is still very active, making the following distinctions more and more blurry. In the following list the converters are classified in terms of speed of conversion (form low to high speed of conversion versus the achievable resolution):

- **Integrating ADC** ⇒ Integration ADCs are characterized for having a low speed of conversion and a high resolution. The idea behind this topology as the name suggest is the integration of the signal during a period of time by means of a capacitor and discharging the mentioned capacitor at a constant rate until is completely discharged. At that point knowing the two times and the value of the voltage reference, is possible to know the value of the input signal. The simplicity of this architecture makes them attractive for instrumental applications and digital acquisition systems in which the speed of conversion is not a must.

- Σ-Δ **ADC** $\Rightarrow$ These ADCs are suited for low-mid conversion speeds and high resolution applications. These converters are based on two concepts, one is the oversampling and the other is the in-band noise shaping. The oversampling imposes a drawback in the frequency of the input signal and therefore in the speed of conversion. Resolutions of 14 to 20 bits are possible to be achieved with this architecture.

- **SAR ADC** $\Rightarrow$ The Successive Approximation Register (SAR) ADC is suited for medium to high resolutions, with speed in the range of few mega-samples per second. The typical resolution achieved ranges between 8 to 16 bits maintaining a low power consumption and a great noise figure. It is typical to use SAR ADC in portable electronics and data acquisition systems.

- **Pipeline ADC** $\Rightarrow$ Pipeline ADCs are used in applications with medium to high speed of conversion and resolutions between 6 to 16 bits. It also has a good relation between speed-resolution-consumption which is well suited for communication systems, image sensors and digital video systems between others.

- **Flash ADC** $\Rightarrow$ Is the fastest ADC topology and it is used in high bandwidth applications. Its main drawback is power consumption, resolution and manufacturing cost. In fact, this type of ADC relies solely on the matching of electrical parameters that need to be trimmed (one device at time) to accomodate for acceptable resolution. For this reason they are normally used in oscilloscopes, radars, satellites and other applications in which the speed of conversion is a must. There is a topology in between the pipeline and the flash, called Half-Flash which obtains a good relation between cost, speed and resolution which makes them more competitive in signal processing applications.

1.3 State-of-the-art ADCs

Monolithic ADCs integration has evolved following a Moore-like law over nearly four decades [12], thanks to the continuously increasing effort of the research community. ADC performance has shown a remarkable improvement in many key parameters with respect to the early days implementations. Low-power and small chip area are often pursued to allow the ADC to be part of a larger system-on-chip (SoC). This trend has evolved from the early days in which the major achievement was to implement a full converter in a single die with a modest speed and resolution and a high power consumption.

From a designer point of view it is crucial to understand the rate of performance and the roadmap of the different ADCs in other to be able to make the best topology election for each application. Several authors have presented works that blend the evolution surveys and derivations of theoretical physical limits to various degrees.

Historically, one of the most widely cited surveys is the Walden survey[35], which is one of the pioneers and includes scientific and commercial ADC references from 1978 to 2008. Nowadays, the Murmann survey is usually referenced [16]. This survew is continuously updated and analyses ADC performance trends with a focus on energy per sample and signal to noise and distortion ratio (SNDR). There are also other surveys based on different analysis of the ADC performance [11] [15] [3] and different points of view [7].

Figure 1.3 compares the conversion region achieved by the state-of-the-art oversampling ADCs with the one achieved by Nyquist ADCs. The figure was collected from [24] and the data used in this graph is obtained from the Murmann survey [16].

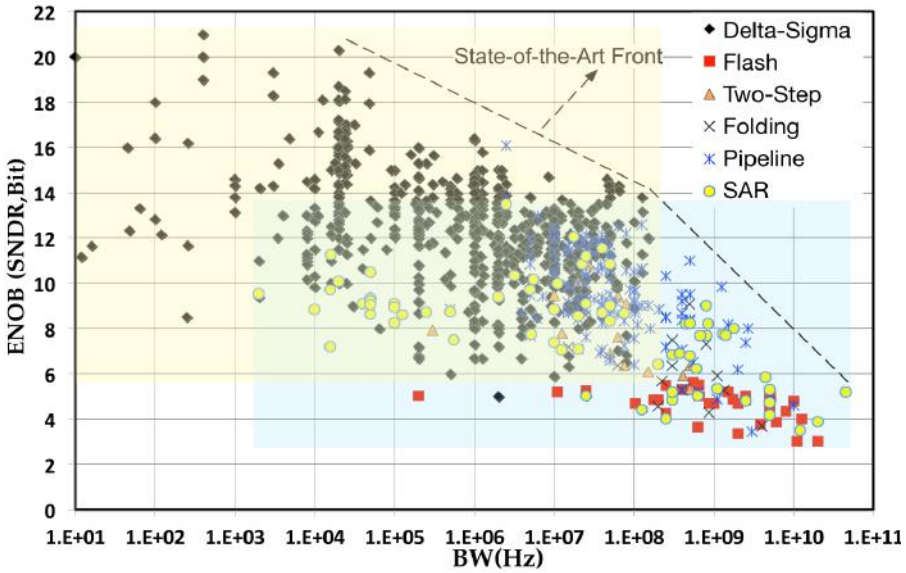


FIGURE 1.3: Murmann survey of ADC performance: representation on the ENOB versus signal bandwidth plane.

The figure 1.3 shows a space map of the different basic ADCs topologies pointed in terms of resolution in bits and speed in Hertz. From the state-of-the-art, oversampling ADCs as Σ-Δ ADCs, have been proved to be used in high resolution and wide frequency (from hundreds of Hertz to hundreds of megahertz) applications. While Nyquist ADCs are more competitive in high frequency applications and medium resolutions.

It is necessary to introduce a third variable not reflected in Fig.1.3, which is the power consumption. In general it is possible to increase the data conversion speed at expenses of higher current consumption, i.e. two different points in Fig.1.3 can be equal in term of state-of-the-art. For this reason, the energy per conversion is normally used and expressed as $E_j = Power/f_s$. A way to include these three parameter is by means of figures of merit (FOM). Figure of merit are expressions which uses a combination of the most important parameters to obtain a value that could be used in a comparation.

In the case of ADCs there are two main FOMs which are the Walden FOM [35] and the Schreier FOM [26]. The Walden FOM is given by

$$FOM_{Walden} \equiv \frac{P}{2 \cdot BW \cdot 2^{ENOB}} \tag{1.4}$$

where P is the static power consumption and the $ENOB$ is the effective number of bits, which is derived from the SNDR expressed in dB, and defined as

$$ENOB \equiv \frac{SNDR(dB) - 1.76}{6.02} \tag{1.5}$$

The main drawback with respect this FOMs is a bias towards low-power medium resolution designs rather than high resolution, and thus benefits from CMOS technology scaling. In other words, more FOM is gained by decreasing the power P rather than increasing the resolution $ENOB$, because Eq.1.4 does not correctly describe the trade-off between power and resolution in the ADCs.

The second FOM is the Schreier FOM which is described as

$$FOM_{Schreier} \equiv SNDR + 10\log(\frac{BW}{P}) \tag{1.6}$$

This FOM is preferred for comparing high resolution ADCs limited by thermal noise. Finally Fig.1.4 represents the space map of the different ADCs with the lines representing the Schreier and Walden FOMs.

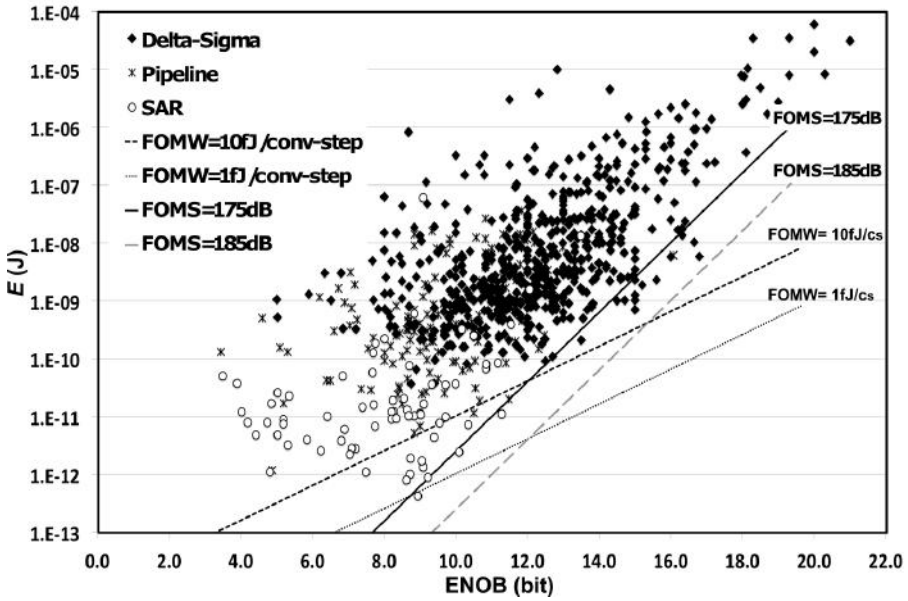


FIGURE 1.4: Murmann survey of ADC performance: representation on the energy-per-conversion versus the ENOB.

1.4 Σ-Δ ADC

The next subsections are focused to explain the basics of the Sigma-Delta operation and a brief description of the main topologies used.

1.4.1 Σ-Δ Modulation Basics

Σ-Δ ADCs are based on two concepts, one is the oversampling and the other one is the noise shaping [26][24][12]. All the architectures explained above except for Σ-Δ are also known as Nyquist ADCs, because the conversion rate follows the Nyquist theorem in which the sampling frequency f_s is two times the input signal bandwidth. Increasing the f_s above the Nyquist frequency f_{NY}, allows for the quantization noise to be reduced, since the same amount of quantization noise is spread over a wider frequency range, i.e. wider than the signal bandwidth. Ideally, the out-of-band noise power can be removed by filtering, leaving the in-band noise level signicantly lower. The ratio between both frequencies (f_s and f_{NY}) is called the oversampling ratio (OSR).

$$OSR = f_s/f_{NY} = f_s/(2 \cdot BW) \tag{1.7}$$

The in-band noise power calculated for low-pass signals as function of the OSR is shown in Eq.1.8.

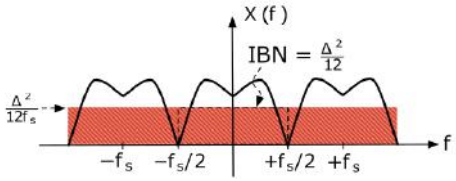
$$P_E = \int_{-BW}^{BW} S_E(f) \cdot df = \frac{\Delta^2}{12 \cdot OSR} \tag{1.8}$$

Therefore based in Eq.1.8 the in-band noise is reduced as the OSR increases. The effect is illustrated in Fig.1.5b, as the OSR is increased the in-band noise spreads along higher frequencies reducing the amount of noise inside the band of interest. With this phenomena the P_E is reduced by 3 dB each time the OSR is doubled which implies a gain of 0.5 Bits.

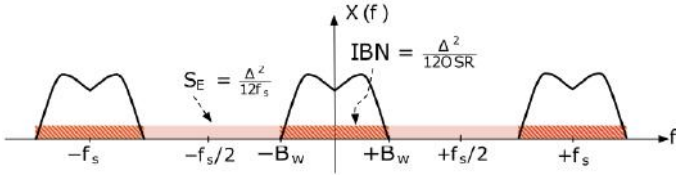
The other concept behind Σ-Δ ADCs is the noise shaping, which is used to further increase the accuracy by filtering the quantization noise in such a way that most of its power lies outside the signal band.

A graphical example is shown in Fig.1.5c, in which it is possible to appreciate how the in-band noise is rejected to higher frequencies, differently to the mere oversampling that does not modify the shape of the noise power spectral density.

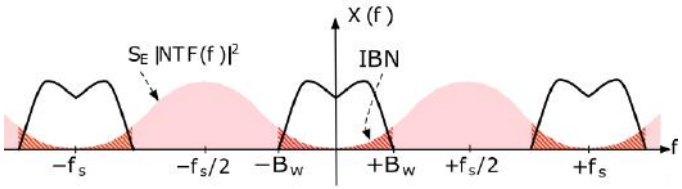
To implement this shift of noise power from low-to-high frequencies the signal undergoes a modulation which can be understood by looking at the basic Σ-Δ block diagram presented in Fig.1.6. This figure shows the main components used in a single loop feedback topology, which in this case are a low pass filter and a linear model of the quantizer.



(A) In-band noise representation on a Nyquist-rate ADC.



(B) OSR effect on the in-band noise.



(C) OSR effect and noise shaping on the in-band noise.

FIGURE 1.5: In-band noise power representations in three different cases: Nyquist-rate ADC, oversampled ADC and oversampled with noise shaping ADC.

Since the circuit processes samples of the input signal, in can be analyzed in the discrete time transformed domain as $X(z)$ and the output $Y(z)$. The quantization error in the linear model of the quantizer is represented by $E(z)$ and g_q is the quantizer gain.

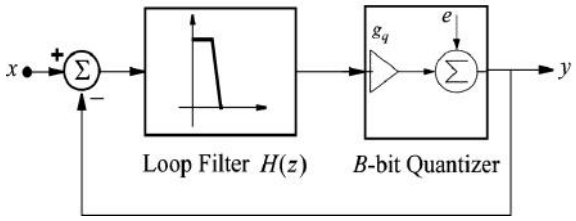


FIGURE 1.6: Basic single loop Σ-Δ Modulator block diagram.

From the block diagram of Fig.1.6 the signal and noise transfer function is calculated in Eq.1.9.

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E(z) \tag{1.9}$$

where signal transfer function ($STF(z)$) and noise transfer function is ($NTF(z)$). They are given by

$$STF(z) = \frac{g_q H(z)}{1 + g_q H(z)}; NTF(z) = \frac{1}{1 + g_q H(z)}; \tag{1.10}$$

If the loop filter is designed in such a way that $|H(z)| \to \infty$ inside the band of interest, the $STF(z) = 1$ and the $NTF(z) = 0$. This means that the signal can pass through the system without attenuation or distortion while the noise is rejected inside the band. However in practice it is not possible to completely reduce the quantization error due to gain limitations in the loop filter. Assuming an ideal $NTF(z) = (1 - z^{-1})^L$, where L is the loop order, the in-band shaped power noise is calculated by

$$P_Q = \int_{-BW}^{BW} \frac{\Delta^2}{12 f_s} |NTF(f)|^2 \cdot df = \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1) OSR^{2L+1}} \tag{1.11}$$

assuming the following susbtitution of the $NTF(f)$

$$NTF(f) = NTF(z)|_{z=e^{j2\pi f/fs}} \tag{1.12}$$

In Eq.1.11, both effects oversampling and noise shaping are combined, showing a higher in-band noise reduction with the OSR than the previous Eq.1.8, which did not include the noise shaping effect. Therefore, Σ-Δ ADCs are able to take advantage of this combined effect that shows a higher reduction of the in-band noise and also enables a higher resolution.

From Fig.1.6, y is a modulated signal in the digital domain representing the analog discrete time (DT) of x. To complete the ADC conversion process, its high frequency spectral component must be eliminated and its rate must be shifted down to the Nyquist rate, corresponding to the Nyquist frequency of the input signal. This operation is performed in the digital domain by the so called decimator filter, which together with the modulator, composes the complete ADC Block. The analysis and the implementation of the decimator filter is out the scope of this work, the interested reader may reference [26].

1.4.2 CT and DT Σ-Δ Modulation

From the operation point of view Σ-Δ ADCs are classified in continuous time (CT) and discrete time (DT). The difference between them is the location of the sample and hold system (S/H). If the sampling operation is performed outside the Σ-Δ loop then the modulator is classified as DT Σ-Δ, and if its performed inside the loop the Σ-Δ is classified as CT. Fig.1.7 illustrates both topologies showing the position of the S/H system.

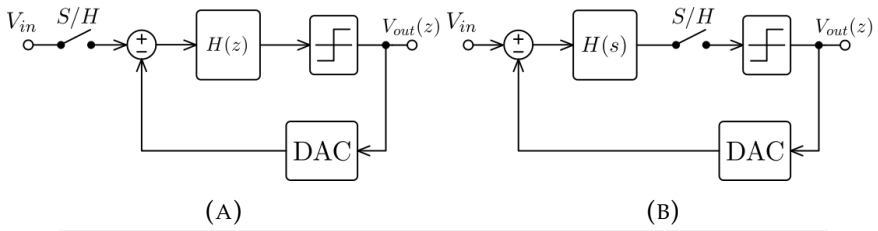


FIGURE 1.7: Discrete time (A) and Continuous time (B) Σ-Δ modulators block diagram.

DT realizations relying on switched-capacitor SC, present low sensitivity to clock jitter and higher robustness against process, supply-voltage and temperature (PVT) variations, mainly due to the linearity of integrated capacitors and matching-based design methodologies. Otherwise, the main drawbacks present in DT implementations are related to bandwidth limitations and the use of sampling switches which introduces non-linearites. SC implementation rely on almost complete settling of the OpAmps which happens to be at several time-constants. As the clock frequency increases this could be unfeasable from the OpAmp bandwidth point of view. CT implementations relax this aspect.

CT modulators based on active-RC and gm-C implementations have been introduced as an alternative for implementing loop filters for high bandwidth applications. Another positive aspect that makes this topology attractive is the built-in anti-aliasing filter and the absence of sampling errors. Besides these advantages, CT modulators are very sensitive to clock jitter, and also to PVT variations. Special attention must be paid to excessive loop delays in the feedback DAC to avoid instability problems.

For all these reasons DT Σ-Δ ADCs are preferred when a robust solution is needed.

1.4.3 Classification of Σ-Δ Modulators

Multiple efforts have been made in continuously increasing Σ-Δ modulators performance during the past decades, resulting in a number of different techniques:

- **Low order Σ-Δ vs High order Σ-Δ** $\Rightarrow$ One simple way to obtain higher resolutions is to increase the order of the loop filter by adding more stages in series. In practice there are limitations in the order due to stability problems because of the path delays created in each new stage added [24][26]. Practically the order of the loop filter is less than a fifth-order.

- **Single-Loop Σ-Δ vs MASH Σ-Δ** $\Rightarrow$ As explained above stability problems arise when using high order simple-loop Σ-Δ. The problem in part can be solved by selecting the adequate scaling coefficients, but assuming a significant reduction of DR compared with an ideal Σ-Δ modulator. An alternative approach to obtain high order Σ-Δ avoiding instability problems is found in the number of quantizers. Σ-Δ modulators employing only one quantizer are called single-loop, whereas those employing several quantizers are often named MASH (multiple-stage noise shaping) or cascade Σ-Δ modulators. MASH modulators consist of N stages of Σ-Δ modulators, in which each stage remodulates a scaled version of the quantization error generated in the preceding one. All the outputs of the cascaded stages are processed conveniently in the digital domain by subtraction. MASH architectures gives the chance to increase the order and therefore the resolution, but at the cost of increasing the complexity of the design. Mismatch errors between different system blocks must be avoided in order to maintain the benefits explained.

In practice, for high resolution the effective order of the shaping is not achieved due to noise imperfect cancellation, causing lower shaped noise to leak in the final output.

- **Single-bit Σ-Δ vs Multi-bit Σ-Δ** $\Rightarrow$ Another approach is the use of multi-bit topologies[9][17][18] instead of the classical single bit DAC [31][28][36]. Increasing the number of bits in the quantizer not only increases the SNR but also the loop stability allowing the use of higher loop coefficients. However, since multi-bit DAC from the feedback loop is directly connected to the input of the Σ-Δ modulator, any non-linearity in the DAC can not be distinguished from the input signal and will be present at the output. Therefore, special attention to non-linearity and accuracy during the DAC design must be taken. Dynamic element matching (DEM) techniques are commonly used to tackle this problem, but they require extra circuitry representing an increase in area, power consumption and complexity. Single bit classical architectures in its counterpart don't require this extra circuitry which makes them more suitable for high linearity applications.

1.5 Objectives

The purpose of this thesis is focused on the realization of a Low-power 16 Bits Σ-Δ Modulator with a bandwidth of 50 kHz. The resulting modulator from the design process is intended to be part of an IP that could be reused in different designs, for this reason the bandwidth and the resolution requirements are high enough to cover a wide variety of applications.

The frame work of this master thesis tries to continue exploring new different ways of designing Σ-Δ modulators, taking as a start point a previous work done in the same research group by Stepan Sutula et. al.[32]. Many aspects of the design flow, from the architectural up to the circuital level will be revised, corrected and optimized in this work, giving degrees of freedom to explore the design space as well as to take decisions following a different path.

The previous work done by Sutula et. al. [32] [30] consist on a 4 order non-bootstraped feedforward single-bit Σ-Δ Modulator with Class-AB single stage switched VMAs [33], which consumes 7.9 mW and obtains 96.6 dB of SNDR from real measurements without using any calibration or analog tuning, and a Schreier FOM of 164.6 dB.

The objectives this thesis aims to achieve are declared in the next lines.

- Contribute to the development of a platform for high-level modelling based on open source software.
- Using the High level models implemented in an open source software, to explore the possibility of using a lower loop order, oversampling ratio and a different number of the quantizer bits (from 1 to 1.5), while maintaining the same performance and stability behaviour.
- Search for optimization methods focused in Bottom-up design flows instead of the Top-down classical approach [34], trying to reduce simulation times and increasing the design efficiency.

- Mapping the physical implementation to a 180 nm 1P6M technology from Xfab, including triple MiM [1] capacitors which allows a significant area reduction, with respect to the previously used technology (UMC 180 nm single MiM).
- Continuing exploring the benefits of using the different types of Class-AB switched Variable Mirror Amplifier (SVMA) introduced in [32]. Increasing the Class-AB coefficient while reducing as much as possible the power consumption.

The performance requirements of the Σ-Δ Modulator are summarized in table 1.1.

Modulator architecture	Single-loop Feed-forward
Bandwidth	50 kHz
Over Sampling Ratio	128
Input signal fullscale	>2 V p-to-p differential
Target SNDR peak	16 Bits
Circuit level characteristics	Switched Capacitors, Switched OpAmp, Non-bootstrapping, No analog calibration, Resistor-less

TABLE 1.1: Initial specifications and characteristics of the Σ-Δ Modulator of this thesis.

1.6 Design methodologies

In order to handle the increasing complexity of analog and mixed-signal IC design, a clear definition of a hierarchical design flow is essential. Despite the advances made during the last decades, the design automation tools in analog domain cannot support the complete design process[10].

Since then and specially in the case of Σ-Δ Modulator, the intervention of a designer with a complete systematic design method and a series of customized tools are required.

Traditionally, analog circuit design has been done following two systematic design flows, Top-down and Bottom-up. Top-down methodologies can be defined as the natural way to approach a complex design. Defining the requirements needed and spending time in developing system-level models and verification environments before planing the sub-blocks division and starting the simulations.

Bottom-up flow methodologies decompose the design in different sub-blocks, which constitute a simple and independent design units. Setting the requirements of each individual block, the transistor level design can be done in parallel by several design teams. Each block is verified as a standalone unit against the specifications and integrated with the rest of

[1] Metal Insulator Metal (MiM) capacitors are implemented using the parasitic capacitance between two conductors on a metal layer. Several metal layers are connected in parallel by vias, forming a vertical metal wall or mesh which increases the capacitance density (capacitance per unit area of silicon chip)

individuals as a system. Verification of the overall system is performed to ensure the correct behaviour of the final design.

Σ-Δ Modulator design procedures traditionally use Top-down methodologies[34]. But in the case of this work both techniques are used in combination to improve the design procedures and also to reduce the simulation times. The synthesis procedure together with the software environments, followed in this work are schematically shown in Fig.1.8.

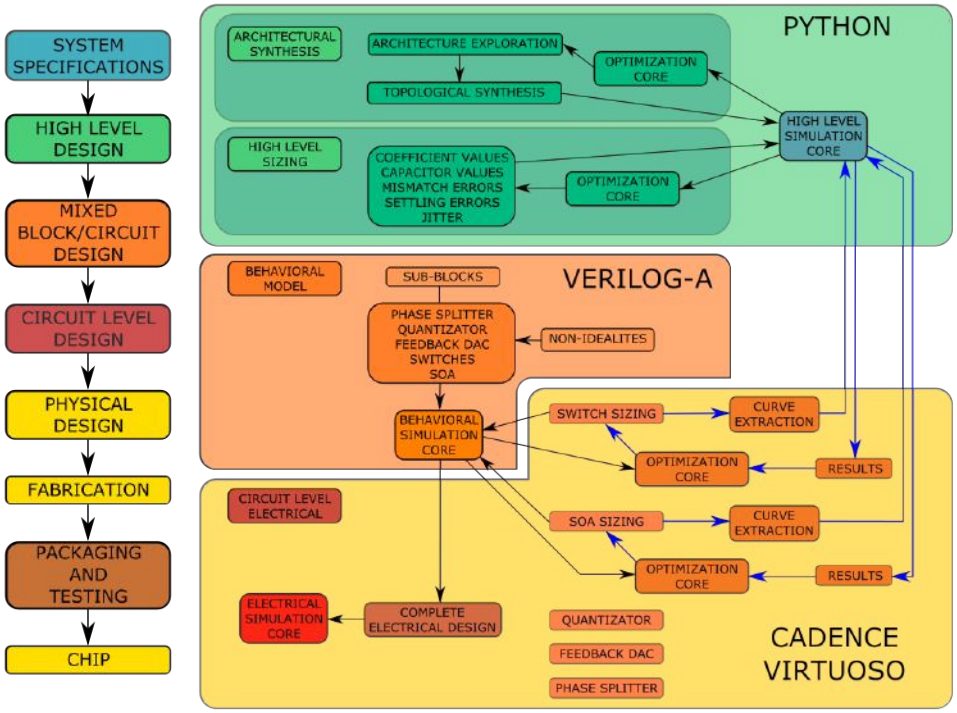


FIGURE 1.8: Design flow diagram adopted in this work. Design tasks have been mapped to their respective design environment.

Different functions are performed in each individual block shown in the synthesis procedure. The description of each stage is presented in the next list.

- **System specifications** $\Rightarrow$ Is the first phase of the design and includes all the requirements imposed in the design. At this stage topological or architectural solutions to be used in the next stage are discussed.
- **High level design** $\Rightarrow$ It has the main task to calculate the different equations in discrete time domain for a quite large number of clock cycles, since, as described in the previous sections, the Σ-Δ Modulation operates an oversampling over the original signal bandwidth.

  Includes the different theoretical models used in the architectural synthesis and also the performance and verification tests. Behavioural simulation programs such as Matlab Simulink [25] are normally used. But in this work following an open source solution Python proves to be a good candidate. Therefore, the high level simulation core is coded using a friendly distribution of Python which includes all the necessary to compile on the fly the written code.

In the case of this work, the optimization core block represents the analytical function done by a designer taking the proper design decisions based on simulation results. While the High level simulation core contains the different functions used to simulate the different Σ-Δ Modulator topologies.

The design flow in first place explores the different topologies selected during the system specification and confirms the expected behaviour. After the candidates are synthesised and simulated using the simulation core the next step is to test the robustness against coefficient mismatch, jitter, settling errors and feedback DAC reference errors. A re-evaluation of the different coefficients selected is possible if the requirements are not satisfied.

- **Mixed Block/Circuit Design** $\Rightarrow$ Cadence Verilog-A represents the intermediate step point between the high level simulations and the circuit level design [8]. Is the link between the numerical simulations done in Python and the electrical simulations in Cadence. Verilog-A is a behavioural kind of language used in electrical simulations to describe the behaviour of any analog or digital block. Verilog-A is simulated in the same environment as the circuit level design using Cadence virtuoso.

  Classically, the Σ-Δ Modulator is divided in different blocks following the indications of Top-down methodologies. Each independent block is described using Verilog-A to form the complete system. When the hole system is described, the next step is to start simulating.

  The main optimization and tests during the design are done in the mixed/signal stage by substituting each block by its circuit level counterpart and maintaining the rest of blocks in Verilog-A. Therefore, the block of interest is optimized while the rest remains ideal i.e. with a negligible contribution to the non-idealities and linearity of the circuit.

  The simulations performed in this part are less time consuming than substituting all the blocks with the transistor level designs. But are high enough to represent a drawback in the optimization process. For this reason in the next point an alternative to the classical approach is presented.

- **Circuit level design** $\Rightarrow$ The transistor level design of each individual block selected in the previous stage is simulated and optimized in this stage. As explained above, the classical approach begins by substituting the previous ideal block by its real counterpart maintaining ideal views in the rest of blocks.

  The new approach represented in Fig.1.8 using blue lines, is mainly based on the electrical extraction of the main characteristics in form of curves, based on a reduced schematic and on short full-electrical transient simulations. The curves can be passed to the high level models and used to evaluate the block performance by doing lengthy simulations in terms of numer of clock cycles.

The simulation time is drastically reduced allowing the evaluation of different solutions in a short period of time. Therefore the optimization process is fessable using the proposed method. This Bottom-up method is also compatible with the traditional design flow of using Verilog-A as an intermediate point.

- **Physical Design** ⇒ The circuit level design represents the characteristics and disposition of each component. In order to be able to manufacture the design the components are converted to its geometrical representations separating each material or process in a different layer.

  The first step inside the layout is the floorplaning which consist in the division of the chip into small blocks. The process of identifying each structure and the connection requirements is essential to meet the available space without losing performance.

  The following step consist in the placement of each component inside the blocks defined in the floorplaning. The position of the different components is a key point to avoid future problems of performance and routing conflicts.

  After the routing a design verification is performed to ensure the correct behaviour of the final design. Different verification test are used to ensure the layout compliance with all the technological requirements (Design Rule Checking DRC), the consistency with the original netlist (Layout vs Schematic LVS) and with all the electrical requirements (Electrical Rule Checking ERC).

- **Fabrication** ⇒ The final design is send to the factory to start the manufacturing process. Normally the foundry uses its own verification tools to ensure the design is able to be processed. After confirming the viability of the design the order start the process.

- **Packaging and testing** ⇒ Represents the last step in the fabrication process and consist in the encapsulation of the silicon wafer to a supportive case which prevents physical damage and corrosion. The encapsulation or package not only supports the silicon but also allows to stablish the electrical contacts between the IC and a circuit board.

  The testing compromises all the steps and elements used as a test vehicle to prove the expected performance.

- **Chip** ⇒ Finally after the achievement of all the different stages the design is completed in the shape of a chip.

The present work covers almost all the stages of the design but others are sorted due to time constrains. The sorted stages are the captions shown in Fig.1.8 filled in yellow.

1.7 Structure of the Work

This thesis is organized in 6 chapters.

- Chapter 2: Measurements

Real measurements across temperature with Σ-Δ modulator designed presented in [32] [30]. Robusness comprovation and extraction of conclusion used during the former design process.

- Chapter 3: High level Σ-Δ modelling

High level Σ-Δ modulator modelling of the different topologies selecting the best candidate after performing robustness and optimization tests.

- Chapter 4: Circuit level design

Transistor level description of each individual block that comforms the complete Σ-Δ modulator.

- Chapter 5: Simulation results

Description of the novel optimization process followed during the design. Explanation and optmization of the different SVMA candidates used in the complete Σ-Δ modulator system. Simulation results presentation including corners.

- Chapter 6: Conclusions

Review of the different design steps, conclusions and future work.

Chapter 2

Measurements

As already stated in the first chapter of this work, the starting point was the design presented in [32] [30] developed within the ICAS group at IMB-CNM. Since only few proof of concept measurements were previously performed, a good starting point for this work can be the measurement against temperature variations of the previous design chip. Avoiding the large fabrication cycle required for microelectronics manufacturing and allowing to gain a valuable experience for the new design, as well as on the experimental characterization of sigma-delta ADCs such as the one designed in this work. Therefore, the current section is intended to show how Σ-Δ Modulator performance is measured demonstrating the robustness against variations in temperature.

2.1 Σ-Δ performance metrics

In Σ-Δ modulators different performance metrics based on dynamic measurements are used, rather than static measurements used low-frequency Nyquist ADCs. The metrics are obtained from the frequency domain representation of the time-domain digital output sequence. An example of a typical output spectrum and its main characteristics is illustrated in Fig.2.1.

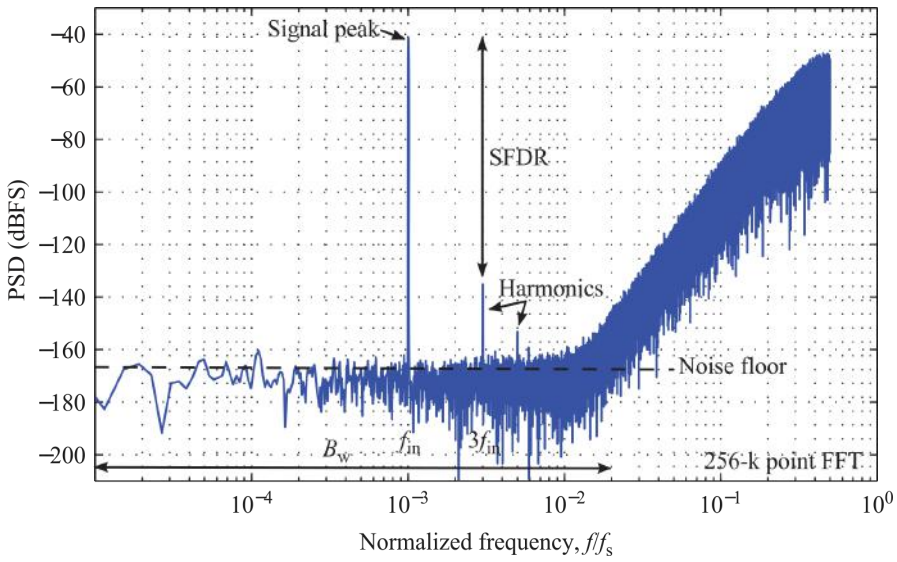


FIGURE 2.1: Typical Σ-Δ Modulator power spectral density with performance metrics.

The most important measures extracted from the output spectrum are collected in the following list and illustrated in Fig.2.2:

- **Signal-to-noise-ratio (SNR)** ⇒ The SNR is the ratio of the input signal power to the noise power measured inside the band (IBN), accounting only for the modulator linear performance without the in-band power associated to harmonics of the input signal. The maximum SNR a converter can achieve is called the peak signal-to-noise-ratio (SNR_p).

$$SNR(dB) = 10 \cdot \log_{10}(\frac{P_{signal}}{IBN}) \tag{2.1}$$

- **Signal-to-noise-and-distortion-ratio (SNDR)** ⇒ The SNR is the ratio of the input signal power to the total noise power measured inside the band (IBN). Accounting for all the possible harmonics present at the Σ-Δ modulator output. The maximum SNDR a converter can achieve is called the peak signal-to-noise-and-distortion-ratio ($SNDR_p$).

- **Dynamic Range (DR)** ⇒ The DR is the ratio between the maximum input signal power which can be applied without a significant performance degradation and the minimum detectable input signal power. Assuming a 3 dB of drop from the SNR peak as a significant performance degradation. From Eq.1.11 and Eq.2.1 the DR expression in dB as function of the loop order L, the number of bits B and the oversampling ratio OSR is obtained as follows

$$DR(dB) = 10 \cdot \log_{10}(\frac{3(2^B - 1)^2(2L + 1)OSR^{2L+1}}{2\pi^{2L}}) \tag{2.2}$$

  In Practice when the Σ-Δ modulator performance is assessed, the DR is obtained from the evaluation of the SNDR plot as function of the input signal amplitude, represented in Fig.2.2.

- **Effective number of Bits (ENOB)** ⇒ Similar to the given expression for an ideal Nyquist ADC (Eq.1.5), there is an expression established for Σ-Δ modulators, where the ENOB can be defined as the number of bits needed for an ideal Nyquist ADC to achieve the same DR as the Σ-Δ ADC

$$ENOB = \frac{DR(dB) - 1.76}{6.02} \tag{2.3}$$

- **Overload Level (OL)** ⇒ The overload level is the relative input where the SNR decreases by 3 dB from the SNR peak

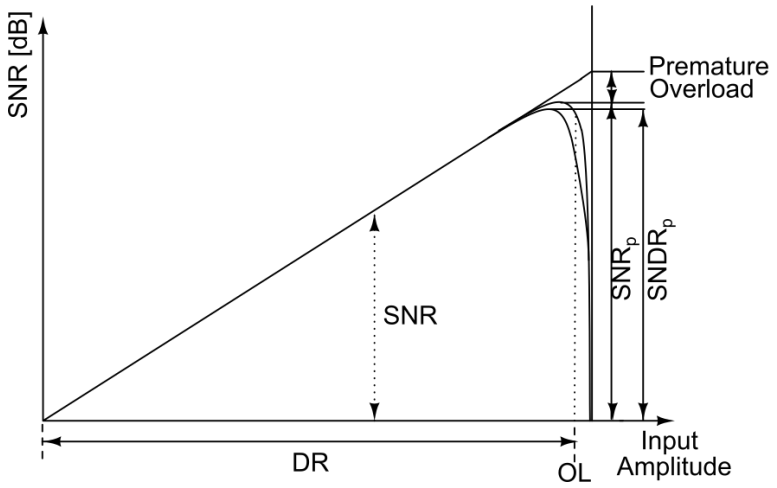


FIGURE 2.2: Graphical representation of the most important performance metrics of Σ-Δ ADC.

As observed in Fig.2.2, the SNDR plot versus the input signal amplitude offers a wide variety of relevant information about the final performance of the designed Σ-Δ modulator. Among all these different metrics the most important parameter is the peak SNDR which gives the instantanious resolution for the maximum amplitude allow by the modulator. Generally the DR which is the horizontal measurement of the converter resolution takes very similar values to the peak SNDR since the SNDR versus input amplitude is typically a linear function with unitary slope.

2.2 Σ-Δ Modulator expected Performance

The previous work done by Sutula et.al.[32] [30] consists in a 4th order 50 kHz bandwidth non-bootstrapped single-bit Σ-Δ Modulator, which obtains experimental 96.6 dB of SNDR operating at 1.8 V and consuming 7.9 mW. Simulation results (Table.2.1) for the full set of technology and temperature corners of the fabricated Σ-Δ Modulator exhibit a very low sensitivity.

	Slow	**Typical**	**Fast**
-40 °C	110.2 dB	109.2 dB	109.2 dB
27 °C	110.6 dB	111.3 dB	110.7 dB
80 °C	110.7 dB	109.3 dB	109.6 dB

TABLE 2.1: Σ-Δ Modulator SNDR simulated under process and temperature variations.

However, the post-layout simulations for the typical process show a substantial drop of the SNDR down to 103 dB. Therefore, lower SNDR value and tendency with the temperature is expected in the real measurements. Furthermore, the design of [32] lacks of on-chip decoupling capacitors which contributes to degrade even mode the SNDR.

2.3 Σ-Δ Test Vehicle

The Test Vehicle is used as interface between the chip and the external equipment needed to measure the design performance. This platform includes the circuitry that generates all the voltage and current references and also the interface used to capture the bit-stream from the Σ-Δ Modulator.

The same prototype board of [32] was used here, however all the cable connections have been revised and enhanced to avoid as much as possible distortion and noise coupling deriving from the cables themselves.

Clear limitations are evident at this point, however a fast prototyping was preferred over a dedicated PCB design in order to accomplish with time limitations.

2.3.1 Test Vehicle Equipment

Different equipments have been used during the measurements, this subsection tries to summarize their main characteristics including a brief description of their use in the measurements.

- **Input Signal Generator (SRS DS360)** $\Rightarrow$ The SRS DS360 is a function generator which is able to generate a differential sinusoidal wave while maintaining low-noise (1 μV) and low-distortion levels (below -100 dB) which at the end limits the measured resolution to 16 Bits. Is also possible to select the output impedance between a series of fixed values, allowing the matching impedance between the equipment and the input of the chip.

  In the case of study the frequency of the input signal is selected to 13.6 kHz and the amplitude to -2 dB of the modulator input full scale (dBFS). The selected values are the same as the ones used during the simulations.

- **Clock Generator (TTI TG5011)** $\Rightarrow$ The TTI TG5011 is a high frequency function generator with rise and fall times bellow 8 ns and low-jitter specifications (0.5 ns RMS). It also allows the selection of the amplitude, offset, duty cycle and the frequency in steps of 1 μHz. The output impedance is fixed to 50 Ω.

  In the case of study the frequency of the clock signal is selected to 13.6 MHz with an amplitude of 1.8 V and 0.9 V of offset. The square clock signal is selected to have a 50% Duty cycle.

- **Power Supply (TTI EX354T)** $\Rightarrow$ The TTI EX354T is a conventional triple output power supply with two trimmed outputs and a fixed one. All the outputs have adjustable current limiters with a maximum current capability of 4A.

  The selected power supply is trimmed to 5 V. The rest of voltage references are obtained on-board using commercial step-down voltage regulators.

- **Interface between PC and Chip (DE0-nanoII)** $\Rightarrow$ DE0-NanoII is a development and educational board designed by TerAsic which contains all the necessary to start a FPGA project.

The current version used includes an Altera Cyclone III FPGA module and the USB Blaster needed to program the Cyclone III. Quartus II web is used as the programming environment.

The DE0-nanoII board is used to capture the bit-stream from the Σ-Δ Modulator and send the data to the PC when is required.

2.3.2 Test Vehicle Board

The main function of the board is to hold the DIP 16 package where the chip is contained and to establish all the electrical connections to the external equipments. As explained before all the voltage references are also generated on-board to avoid possible noise injection through the wires.

The board is also shielded by a metallic box to reduce electromagnetic interference when performing the measurements. The board and the metallic case are shown in Fig.2.3.

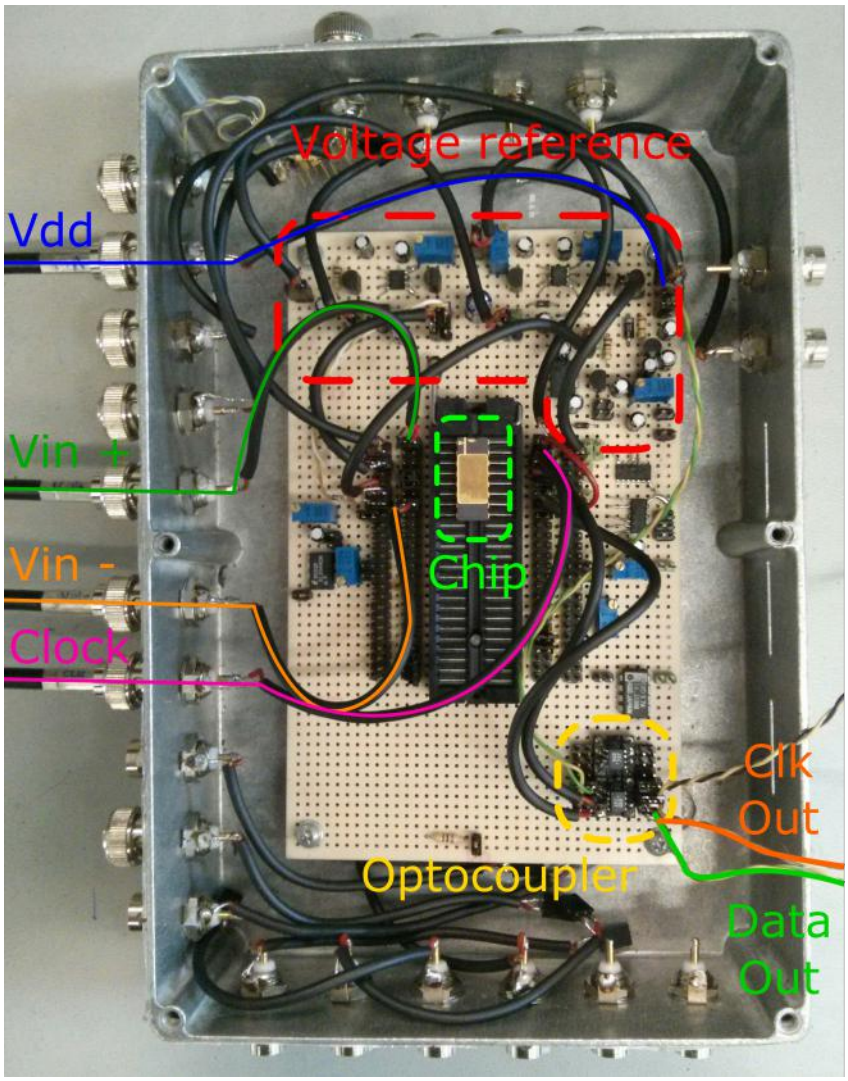


FIGURE 2.3: Test vehicle board of the Σ-Δ ADC of [32].

The different connections between the external devices and the board are drawn in the image. The series of potentiometers are used to adjust the final voltage supplied by the step-down regulators. Moreover, all voltage references are filtered using capacitors with different sizes to avoid noise and perturbations to be injected in the modulator. Both digital outputs from the Σ-Δ Modulator are connected to optocouplers to separate the acquisition system from the board.

2.3.3 Test Vehicle Software

The setup used also includes a software stage running in the PC to send the correct commands and receive the packed data-stream. A routine written in Python is used as a post-processing tool and FPGA control software, requesting at a given rate the packed data-stream.

Most of the written code to form the High Level Simulator Core (Fig.1.8) is used in the post-processing to extract the PSD and the SNDR. The routines needed for communicating with the FPGA are included in the standard packages installed by the Anaconda distribution of Python[5].

The software continuously requests data from the FPGA at a pace set by the user (1 second in this specific case) and plots the results almost instantly. Wrong results due to changes in the conditions or lost of synchronization are automatically discarded, while the rest are saved.

Figure 2.4 shows the PSD-spectrum resulting from the post-processing Python script. The SNDR is also calculated and reported in the title of the plot.

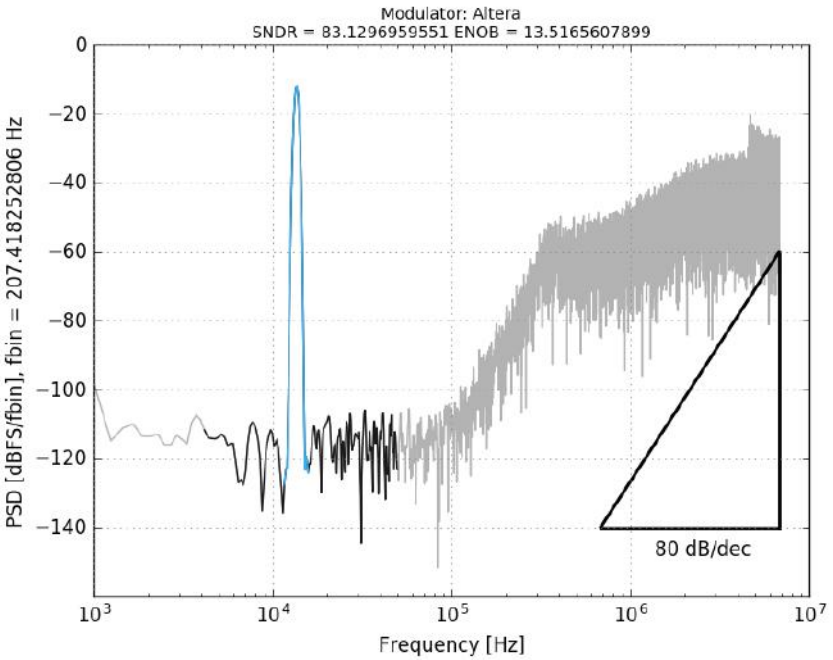


FIGURE 2.4: Σ-Δ Modulator PSD measurement of the Σ-Δ ADC of [32].

2.4 Σ-Δ Modulator Measurements

The aim of the measurements is to compare the deviation with temperature presented in Table 2.1 with experimental data obtained from the real operation of the previous Σ-Δ Modulator design. Following this aim an environmental test chamber is required to modify the Σ-Δ Modulator temperature.

The selected chamber (Dycometal CCK -40/81) allows to change the temperature and the humidity at the same time using a PID controller. The range of temperature variation is compressed between -40 °C and 80 °C. While the humidity range is situated between 15% and 98%. The chamber also includes two wall feedthroughs to connect the test vehicle board with the equipment situated outside the chamber.

2.4.1 Measurement Procedure

The procedure used to measure tries to reduce as much as possible all the external noise sources to guarantee the correct function of the modulator and also to improve the results. The following steps describes the procedure used during the measurements.

1. Temperature setpoint selection to the next value while maintaining a low humidity level (<20%).

2. Waiting for the temperature to be established at the correct value. In heating mode the temperature is increased 3 °C per minute, while in cooling mode the rate is -1 °C per minute.

3. After the value is established the temperature control is disconnected. By disconnecting the temperature control, all the pumps and mechanical systems are automatically switched off, reducing the electromagnetic noise generated by the chamber itself.

   Concerning the stability of the temperature, the chamber is able to retain the temperature at the correct value during al least 15 minutes. In the case of the humidity, it is more difficult to retain a low value due to the feedthroughs.

4. Starting the measurement software to capture the bit-stream from the Σ-Δ Modulator . The measure time is about 10 min, enough to guarantee, that the measurement is taken at the right temperature.

5. Switching on the temperature control to the next setpoint and wait 5 minutes to reduce the humidity level before the new temperature is reached.

2.5 Measurement Results

Following the previous procedure a range between -40 °C and 80 °C is measured in 10 °C steps. The first sweep consist on rising up the temperature to reduce the presence of humidity in the walls of the chamber. After heating

up with a low humidity setpoint the chamber is cooled down while taking measurements at each step point. The post processing results obtained from the measurements are summarized in Table 2.2.

The measurements are performed with a lower input signal amplitude (-12 dBFS) than the selected in the simulations. For this reason the SNDR value is significantly lower with respect to the simulations.

The results obtained shows a low deviation against temperature variations inside the range of -20 °C to 50 °C. Outside this range other problems not related with the Σ-Δ Modulator performance arises bringing bad results. Conclusions about the obtained results are presented in the next section.

Temperature	SNDR	% Deviation
-40 °C	80.03 dB	-3.75 %
-30 °C	82.06 dB	-1.31 %
-20 °C	81.59 dB	-1.87 %
-10 °C	83.15 dB	0.02 %
0 °C	82.74 dB	-0.49 %
10 °C	83.25 dB	0.12 %
20 °C	83.13 dB	0 %
30 °C	83.75 dB	0.72 %
40 °C	83.83 dB	0.81 %
50 °C	84.81 dB	1.99 %
60 °C	86.95 dB	4.57 %
70 °C	87.42 dB	5.13 %
80 °C	87.86 dB	5.68 %

TABLE 2.2: Σ-Δ Modulator SNDR measurements across temperature.

2.6 Discussion

At this point some partial conclusion may be drawn. Post layout simulations assessed a resolution of 103 dBFS. However, as already stated in [32] a further degradation was detected on the physical chip probably due to the lack of proper on-chip decoupling capacitors, resulting in a SNDR of 96.6 dB.

The measurements presented here are performed with a lower input signal amplitude (-12 dBFS) than the selected in the simulations, for a more convenient test setup under temperature variations. For these reasons the SNDR value resulted lower then the simulated value.

Σ-Δ Modulator robustness against temperature variations inside the range of -10 °C to 40 °C have been proved trough real measurements. Out of this range of temperatures other problems related with the test vehicle board appear to increase the noise floor level and distortion, reducing the measured resolution of the modulator and increasing the deviation above the expected value obtained in the simulations.

These effects can be produced by a list of factors which should be taken in consideration in the following designs:

- The connections between the input ports and the board are made with single in-line pin sockets. The problems turns with the variation of the contact resistance due to the position of the cable which produces a change in the contact area. The described effects are translated in distortion, reducing the final SNDR value.

  A possible solution is to weld the cable directly as close as possible to the input.

- Another effect related to the inputs is the length and symmetry of the cables used for the differential inputs. The length should be as short as possible maintaining a symmetry in length between the differential inputs. The state of the cable and the welding are also a key factor to ensure no distortion.

- The use of prototyping boards is an important step for proving the concept. But for accurate results PCB must be developed to eliminate external couplings of distortion and noise.

  Using a PCB allows to ensure symmetry between inputs, to separate more efficiently electrical domains, to eliminate the tin and/or cable paths and to reduce the antenna effects leading a significant reduction in the noise floor.

- Another important improvement which is related to the design technology is the use of on-chip decoupling capacities. The triple MiM capacities allow the use of higher capacitor values with less area consumption than the previous design technology.

- Because of the use of the feedthroughs to connect the inside board and the external equipment, the chamber at certain temperatures below 0 °C is not capable to maintain the humidity setpoint. Resulting in the appearance of ice crystals at the exposed surfaces of the board, affecting therefore, the internal connections and the final performance. The solution could be the fabrication of a silicone plug attached to cables.

All this points are a valuable information which the only way to be acquired is by means of practical testing of a real chip. The conclusions are also taken into account in the design developed in this work.

Chapter 3

High level Σ-Δ modelling

High level modelling is the starting point in any Σ-Δ modulator design, because solving a system of difference equations is much faster and easier than simulating a complex system in the electrical domain.

As shown in Table 3.1, multiple evaluations of an ideal model with different parameters are possible in a short period of time. Therefore, it is feasable to explore all the different topologies and its optimal solutions at a high level of abstraction.

	High Level	**Verilog-A**	**Cadence Schematic**
Time	30 seconds	1-2 Hours	4 days

TABLE 3.1: Σ-Δ Modulator simulation time comparison on 12 GHz/24 CPUs x86_64 machine.

The most important part in the high level modelling is including step-by-step different modules trying to enhance the approximation between the ideal model and a real modulator. Having good behavioural models is a key point to increase the efficiency of the design methodology and the optimization of the design.

The first step in the high level modelling is the block diagram extraction of the different Σ-Δ topologies discussed during the System Specification stage. The block diagram along with the transfer function represents the behavioural model of each architecture. At this point the mathematical description of each modulator is ready to be used in the simulation software.

Proprietary simulation programs such as Matlab Simulink [25] are normally used in the Σ-Δ ADCs design. But in the case of this work, a friendly and open source Python distribution called Anaconda[5] has been chosen.

Python is then used in the High level modelling to define the modulator behaviour described by its transfer function and also to analyse all the data generated during the simulation. Following the diagram of Fig.3.1 a simple and functional model is described.

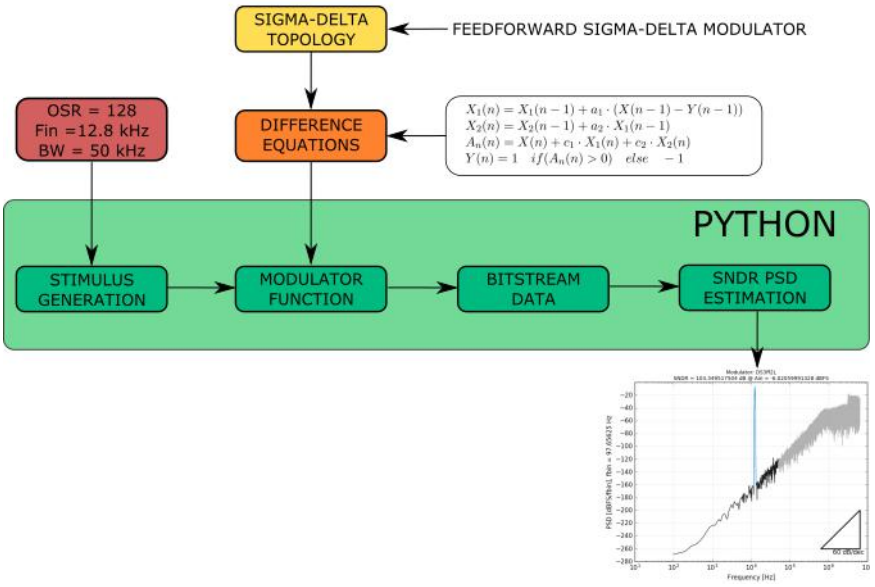


FIGURE 3.1: Design flow of High level modulator implementation.

As presented in the following sections many non-ideal effects modelling circuit-specific issues are easily included in the Python code.

3.1 Σ-Δ modulator topologies

In this work a Switched Capacitor Σ-Δ modulator is addressed. For this topology a single loop architecture was preferred over MASH architecture to avoid noise leakage problems. Single loop modulators come with a variety of different flavours. In the next two subsections two different implementations will be presented. The former, has an historical value by itself and helps introducing the practical implementation of high order noise shaping together with an example of python code. The latter is a state of art modulator topology which features low distortion and low power capabilities and constitute the chosen topology for the work presented here.

3.1.1 Distributed feedback Σ-Δ modulator

Distributed feedback topology is one of the most common Σ-Δ modulator architectures used during the past decades. It responds to the needs of increasing the low shaping, and consequently, the resolution given by first-order Σ-Δ modulators. Besides, the first-order Σ-Δ modulator suffers from tonal behaviour, dead zone input range[26].

The simplest way to avoid these problems consists of replacing the quantizer inside the loop with a nested 1st-order Σ-Δ modulator. When this operation is done L-times the result is a L-th order modulator, including L number of integrators before the quantizer and multiple feedback signals.

It has to be observed that each integrator, represented as an $H(z)$ block is pre-scaled by a coefficient $a_1 ... a_L$. This coefficient is positive and non zero, and usually less than one for the sake of stability.

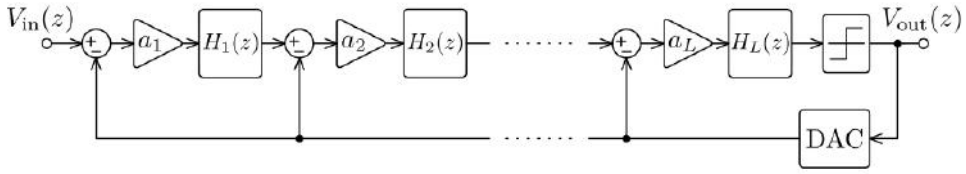


FIGURE 3.2: L-th order distributed feedback Σ-Δ Modulator.

Assuming the second-order distributed feedback modulator of Fig.3.3, the transfer function is deducted from the intermediate states as follows.

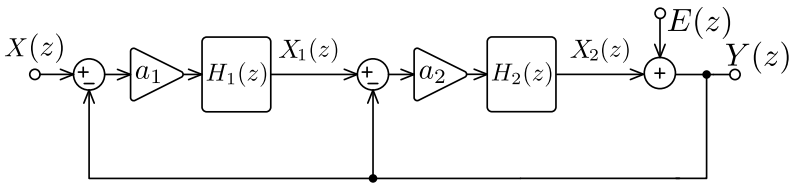


FIGURE 3.3: 2^{nd} order distributed feedback Σ-Δ Modulator.

Following the same approximation explained in Chapter 1, the Quantizer is substituted by a linear block providing the summation of the quantization error $E(z)$.

Note that, the system now has a multiple input fed respectively by $X(z)$ and $E(z)$. The output sequence is represented by $Y(z)$ and the output of each integrator is given by its state variable, $X_1(z)$ and $X_2(z)$ respectively for the first and the second integrator. The system of equations can be neatly written as shown in the following lines.

$$\begin{cases} X_1(z) = a_1 H(z) \cdot (X(z) - Y(z)) \\ X_2(z) = a_2 H(z) \cdot (X_2(z) - Y(z)) \\ Y(z) = X_2(z) + E(z) \end{cases} \tag{3.1}$$

Eq.3.1 can be easily translated to the following Python code:

```
for k in range(0, nsamples):
    X1[k] = X1[k - 1] + a1*(X[k - 1] - Y[k - 1])
    X2[k] = X2[k - 1] + a2*(X1[k - 1] - Y[k - 1])
    Y[k] = 1 if X2[k] >= 0 else -1
```

It is worth noting that the Python code provided above does not make any approximation on the quantizer, so its non-linear effects on the modulator are already included. Developing the algebra of Eq.3.1 the following expression is obtained.

$$Y(z) = \underbrace{\frac{a_1 a_2 H^2(z)}{1 + a_2 H(z) + a_1 a_2 H^2(z)}}_{STF(z)} X(z) + \underbrace{\frac{1}{1 + a_2 H(z) + a_1 a_2 H^2(z)}}_{NTF(z)} E(z) \tag{3.2}$$

Assuming an integrator transfer function $H(z) = z^{-1}/(1 - z^{-1})$, the $STF(z)$ and $NTF(z)$ are calculated as follows

$$\begin{cases} STF(z) = a_1 a_2 \cdot z^{-2}/D(z) \\ NTF(z) = a_1 a_2 \cdot (1 - z^{-1})^2/D(z) \end{cases} \tag{3.3}$$

where $D(z) = (1 + a_1 a_2) - (2 - a_2)z^{-1} + (1 + a_2)z^{-1}$.

Taking the numerator terms in Eq.3.3, apart from a gain factor represented by $a_1 a_2$, it is possible to observe that the input is delayed by two samples (z^{-2}), while the quantization error $E(z)$ is shaped by the desired term $(1-z^{-1})$ to the power of two, corresponding to the second order shaping.

Analysing the effects of $D(z)$ and provided that the modulator is stable for $a_1 = a_2 = 0.5$, $D(z)$ can be calculated as

$$D(z) = \frac{3}{2}(\frac{5}{6} - z^{-1} + z^{-2}) \rightarrow Z_p = \frac{1}{2} \pm j\sqrt{\frac{7}{12}} \tag{3.4}$$

The z-domain poles Z_p map directly to the frequency domain using the transformation $e^{j\omega T_s} = cos(\omega T_s) + jsin(\omega T_s) = z$.

$$\omega_p = \frac{1}{T_s}(\frac{\pi}{3} \pm sin^{-1}\sqrt{\frac{7}{12}}) \tag{3.5}$$

From the Bode-plot point of view this corresponds to the second order prototype polynomial:

$$(\frac{s}{\omega_0})^2 + 2\xi(\frac{s}{\omega_0}) + 1 \tag{3.6}$$

Where $f_0 = 2\pi\omega_0$ is the corner frequency and ξ is the damping factor.

$$\begin{cases} \dfrac{f_0}{f_s} = \dfrac{1}{2\pi}\sqrt{(\dfrac{\pi}{3})^2 + (sin^{-1}\sqrt{\dfrac{7}{12}})^2} \approx 0.22 \\ \xi = \dfrac{\pi}{3}\dfrac{1}{\sqrt{(\dfrac{\pi}{3})^2 + (sin^{-1}\sqrt{\dfrac{7}{12}})^2}} \approx 0.77 \end{cases} \tag{3.7}$$

Indicating that the frequency response is almost flat up to $1/5$ of the sampling frequency. Considering that the practical oversampling ratio values are in the order of 8 times or even much more higher, $D(z)$ can be considered to hold for a constant value of $3/2$ in all the signal bandwidth.

Using the Python code for Eq.3.1, the first simulation cycle and the density of states, at each integrator output is obtained (Fig.3.4). The density of states brings a valuable information about the level occupation at the output of each integrator and consequently the output range needed for each OpAmp implementing the integrator block.

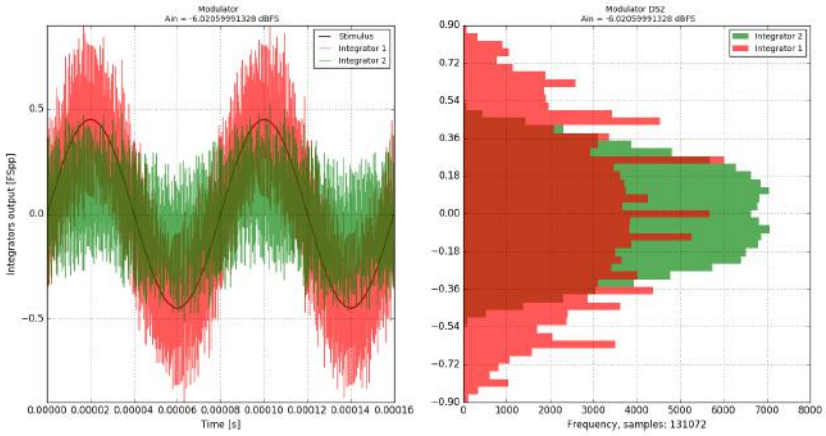


FIGURE 3.4: Transient simulation and signal distortion at integrator outputs for a 2^{nd} order distributed feedback Σ-Δ modulator.

3.1.2 Feedforward Σ-Δ modulator

Feedforward Σ-Δ Modulators are first introduced in [27] to attain to low power and low distortion modulators.

The idea behind this topology is to transfer the input signal and part of the subsequent intermediate states directly to the input of the quantizer. Avoiding the input signal to pass through the integrators chain, eliminates the distortion produced by non-linear OpAmp gain, Slew-rate and other related effects. As a consequence the integrators only process the quantization error which is much smaller than the input amplitude, increasing the ability to handle large signals without overloading the quantizer.

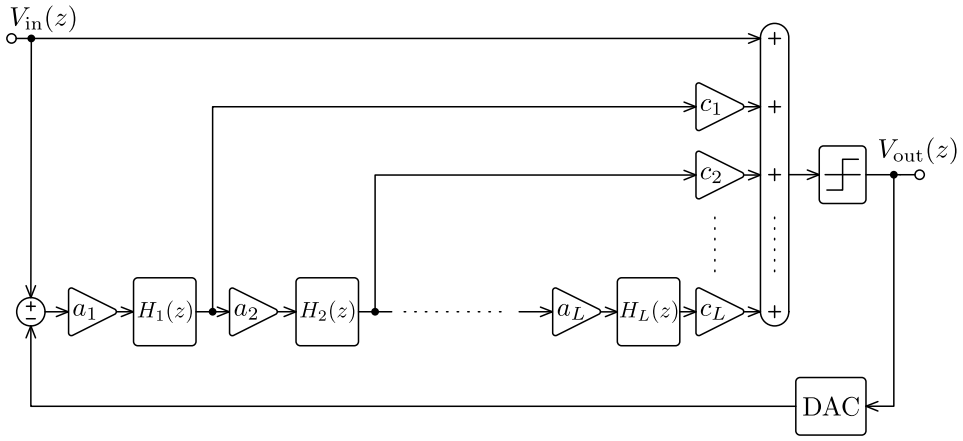


FIGURE 3.5: L-th order Feedforward Σ-Δ Modulator.

Following the same criteria used for the distributed feedback modulator the transfer function from a second order modulator (Fig.3.6) is deducted and presented in Eq.3.8.

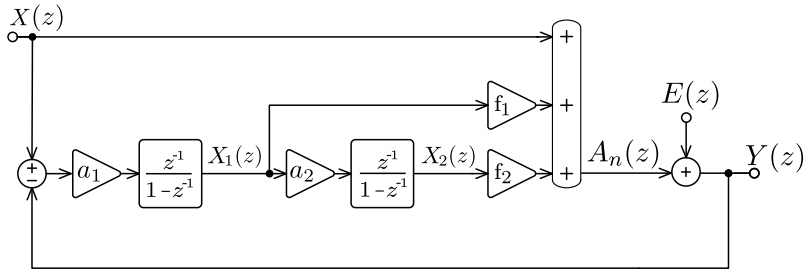


FIGURE 3.6: 2^{nd} order Feedforward Σ-Δ Modulator.

The equation describing the system in Fig.3.6 are:

$$\begin{cases} X_1(z) = a_1 H(z) \cdot (X(z) - Y(z)) \\ X_2(z) = a_2 H(z) X_1(z) \\ Y(z) = X(z) + f_1 \cdot X_1(z) + f_2 \cdot X_2(z) + E(z) \end{cases} \tag{3.8}$$

Which results in

$$\begin{cases} STF(z) = 1 \\ NTF(z) = \dfrac{(1 - z^{-1})^2}{1 - (2 - f_1 a_1) z^{-1} + (1 - f_1 a_1 + f_2 a_1 a_2) z^{-2}} \end{cases} \tag{3.9}$$

The $STF(z) = 1$ confirms the signal is transferred without distortion while quantization noise is now processed by the integrators. Again, the $NTF(z)$ states for a second order shaping at the numerator and it has a denominator that can accommodate for a convenient transfer function by tuning the loop coefficients a_1, a_2, a_3, f_1, f_2 and f_3.

In terms of density of states at the integrator outputs (Fig.3.7), it is appreciated a significant reduction which leads to a relaxation of linearity requirements at the output stages of the OpAmps and also in the power consumption.

The following code are used to implement the modulator behavioural model in Python.

```
for k in range(0, nsamples):
    X1[k] = X1[k - 1] + a1*(X[k - 1] - Y[k - 1])
    X2[k] = X2[k - 1] + a2*X1[k - 1]
    An[k] = X[k] + f1*X1[k] + f2*X2[k]
    Y[k] = 1 if An[k] >= 0 else -1
```

The new line ($A_n(n)$) added in the code above represents the summation of the different feedforward signal connected to the quantizer input. Comparing the simulation results from Fig.3.4 and Fig.3.7, is it possible to clearly see the difference in the density of states and the overload levels.

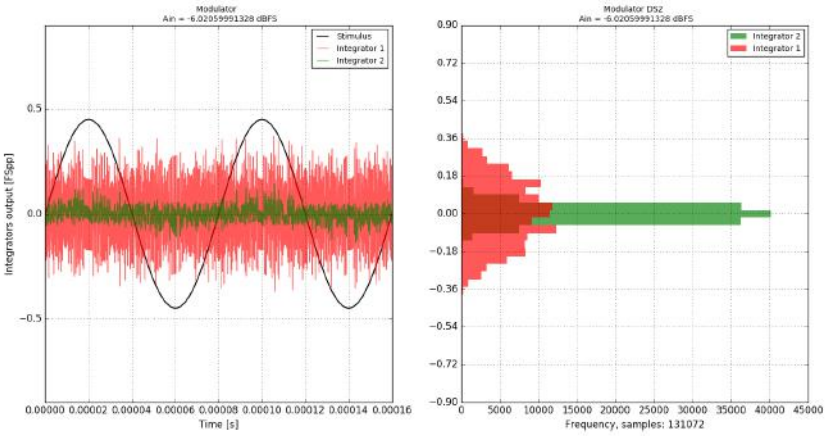


FIGURE 3.7: Transient simulation and signal distortion at integrator outputs for a 2^{nd} order feedforward Σ-Δ modulator.

3.2 Σ-Δ Modulator Topology Election

The advantages of the Feedforward Σ-Δ Modulator which makes the difference over the traditional Σ-Δ Modulator are described below:

- Only one feedback path instead of the multiple paths used in the traditional modulator
- Reduced sensitivity to the building block non-idealities, because the input signal is transferred directly at the quantizer input
- Reduced internal signal swing and power consumption, as consequence of the processed quantization error which is much smaller than the input amplitude.

At this point the Feedforward Σ-Δ Modulator Topology is selected to be implemented in the frame work of this master thesis.

The next steps described in this section consist in the selection of the different parameters to achieve a resolution of 16 Bits corresponding to a SNDR of 98.1 dB, while maintaining as low as possible the complexity and power consumption. The mentioned parameters are the over sampling ratio (OSR), the modulator order L and the number of levels of the quantizer Q_L. The selection of Q_L is restricted to 2 or 3 levels. Both values can be practically implemented without the need of Dynamic Element Matching (DEM) digital circuit in the DAC which would broaden the design time and introduce more power consumption. The considered OSR values have been also restricted to a power of two in order not to complicate the decimator filter design. This is considered to be a good practice, since it greatly simplifies the post-processing digital hardware contributing to a global low-power mixed-signal design.

All the different simulations are performed using the high level developed code, following the flow shown in Fig.3.1. Simulations have been performed in order to extract the SNDR peak of each configuration, results are summarized in Table. 3.2.

		OSR			
		64	128		
Modulator Order	**L = 3**	85 dB	107 dB	$\mathbf{2Q_L}$	**Quantizer levels**
		98 dB	122 dB	$\mathbf{3Q_L}$	
	L = 4	92 dB	121 dB	$\mathbf{2Q_L}$	
		102 dB	129 dB	$\mathbf{3Q_L}$	

TABLE 3.2: SNDR peak value for various Σ-Δ Modulator configurations, considered in this work.

Results in Table 3.2 are taken from literature [37] and have been resimulated in order to double check the Python code with published results.

It can be observed that the only case of OSR = 64 complying with the target resolution is $L = 4$ and $Q_L = 3$, while all the cases of OSR = 128 perform well and are all possible candidates.

Having a lower OSR is attractive since it implies a reduced switching activity, involving also the digital part. Unfortunately the case of $L = 4$ and $Q_L = 3$ provides very few dBs of margin, respect to the targeted performance, in this case less than 4 dB, so the choice of this particular case would not be considered a sage design choice. In fact, the SNDR calculated here accounts only for the quantization noise and distortion without taking into account all the unavoidable circuit non-idealities. The latter would easily erode the SNDR safe margin.

On the OSR = 128 side, a very high SNDR figure is assessed. However, the cases performing a SNDR larger than 120 dB ($L = 4$ or $Q_L = 3$), come with extra circuit complexity which are not fit for this application.

Finally the best trade-off is found in the $L = 3$, $Q_L = 2$ and OSR = 128 case, which provides the simplest hardware implementation while guaranteeing an SNDR margin of almost 9 dB. This means, in practice, that the final SNDR is allowed to be determined by other physical effects, which in the common design practice is the K_BT/C noise for SC implementation of the modulator presented in this work and described in the next chapter.

Finally, an advice should be taken into account before continuing with the design process. The physical realization using switched OpAmps (SOA) implies the correct selection of the different phases in which each integrator works. This aspect, which accounts for circuit level implementation of the modulator is explained in detail in Chapter 4.1. The following tests and simulations are all performed using the updated Σ-Δ modulator models with the correct integrator expressions, as indicated in Fig.3.8.

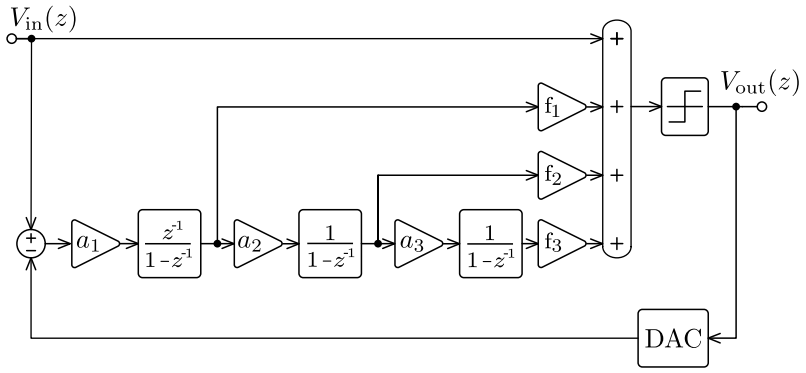


FIGURE 3.8: Block diagram of the 3^{rd} order feedforward Σ-Δ modulator developed in this work.

3.3 Coefficient Optimization

Generally speaking, a process of optimization normally implies the definition of a cost function which is to be minimized with respect some variables and under further constrains. In the case of a Σ-Δ modulator the architecture robustness, the coefficient viability and the sensitivity of the system are variables and constrains used during the optimization which are difficult to be summarized in a cost function[14][19][38][37]. In this work, a manual selection process from a pool containing multiple solutions with multidimensional outputs is preferred, because many design aspects such as circuit complexity or mismatch sensitivity can not be easily or univocally translated into a cost function. Here is where design experience plays a crucial role of taking important decisions about design alternatives.

For this reason a Grid Search is performed, adjusting the step size to minimize the number of simulations while maintaining a good relation between points. The simulation times of the behavioural model is low enough to allow the simulation of a high number of points. The selected grid implies the simulation of 22500 points which represent 62.5 hours.

All the possible candidates are selected following the following criteria

1. **SNDR Peak value $\geq$ 107 dB** $\Rightarrow$ The list is automatically sorted by SNDR. However this is not the most important selection criteria.
2. **SNDR Peak value position** $\Rightarrow$ The SNDR peak in terms of input signal amplitude should be as close as possible to the fullscale value, taking advantage of the whole Σ-Δ modulator operation range. To understand the importance of this point it must be noted that the input full scale will be proportional to the feedback DAC electrical fullscale. Usually the same capacitor implementing the input sampler also provides the feedback path of the modulator.

   Intuitively, the fullscale of the DAC should be greater than the input signal fullscale to provide a sample-by-sample sufficient feedback without driving the modulator to saturation. If, as usual, the resolution is limited by K_BT/C noise, the SNDR will be proportional to C and the DAC fullscale to the power of two.

However, this simple picture is worsened by the non-linear effects of the modulator itself which for a given DAC fullscale, turns to be unstable if the same fullscale is applied to the input. In fact, the input fullscale should be kept lower for stable operation of the modulator. In order to preserve the SNDR, the designer is forced to either increase the DAC fullscale or to increase the C value.

Nevertheless, the DAC fullscale cannot freely increase and in any case exceed the power supplies of the circuit. In practice, these values are even lower due to the unavoidable switch distortion. When the maximum DAC fullscale is reached, the only way to increase the SNDR is by enlarging C which translates directly to power consumption. A good choice for low power design is then, to choose a proper set of coefficients which allows for higher input signal before the modulator start to produce severe distortion.

3. **Coefficient value** $\Rightarrow$ Integrator coefficients with higher values are more interesting because allows the use of lower sampling capacitance values. This is crucial at the input stage where the higher capacitance value is used to reduce the Thermal noise.

   This aspect can be clarified recalling that a SC integrator is circuital identical to a SC amplifier with the difference that the feedback capacitor is never reset, assuming as a consequence, the role of the integrating capacitor. In this circuit the integrator coefficient is given by the ratio of the sampling capacitor over the integrating capacitor

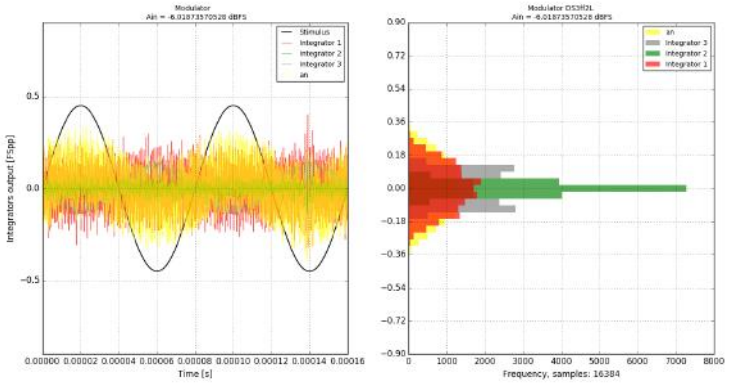
   It is now evident that smaller integrator coefficient will translate, for a fixed K_BT/C noise driven the sampling capacitor, to a larger integrating capacitor. This one is directly connected at the output of the OpAmp, demanding consequently, more current capability and resulting in more power consumption.

   The maximum values of the coefficients are related to the loop stability. There is no solid theory which allows to predict analytically which are these limits, so simulations are needed to validate the proper operation of the loop. All the sets of coefficients that produces instabilities in the modulator are discarded.

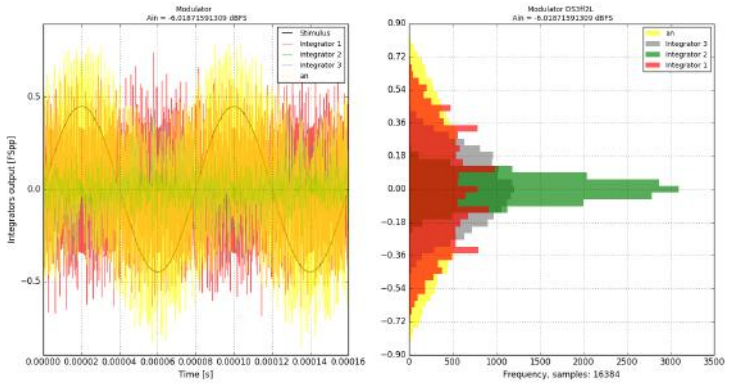
Position	$\mathbf{a}_1$	$\mathbf{a}_2$	$\mathbf{a}_3$	$\mathbf{f}_1$	$\mathbf{f}_2$	$\mathbf{f}_3$	$\mathbf{SNDR}_{peak}$	$\mathbf{A}_{in}@SNDR_{peak}$
1	0.2	0.2	0.2	1	1	3	111.13 dB	-5.19 dBFS
2	0.2	0.2	0.1	1	1	6	111.13 dB	-5.19 dBFS
3	0.1	0.2	0.5	3	1	2.5	111.01 dB	-4.43 dBFS
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
285	0.5	0.2	0.5	1	1	1	107.71 dB	-4.43 dBFS

TABLE 3.3: Extracted output samples of the Grid search algorithm.

Among all the possible candidates that fulfil the 3 choice criteria described above, a very practical choice is for candidate that implements $f_1 = f_2 = f_3 = 1$. As will be shown in the next chapter, this choice greatly simplifies the implementation of the passive adder in front of the quantizer and it guarantees the lowest attenuation possible avoiding demanding requirements on the quantizer offset and noise.



(A) Simulation results of candidate number 1



(B) Simulation results of candidate number 285

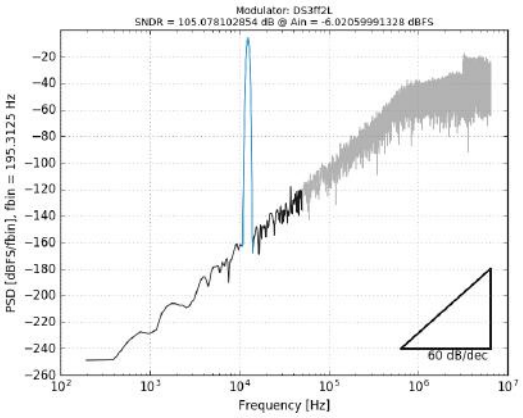
FIGURE 3.9: Transient simulations and state variables distribution for two different candidates of the grid search algorithm.

For all the above reason the candidate in position 285 is selected. The main drawback with selecting a large a_1 is the occupancy levels of the first integrator spreading to large voltage (See Fig.3.9a versus Fig.3.9b). This translates at circuit level on wider output range performing OpAmps, but as will be demonstrated in the next chapter, where the circuits are presented and analysed, this does not represent a critical factor.

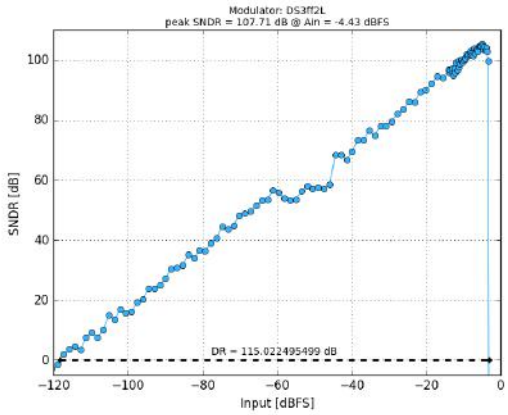
Position	$\mathbf{a}_1$	$\mathbf{a}_2$	$\mathbf{a}_3$	$\mathbf{f}_1$	$\mathbf{f}_2$	$\mathbf{f}_3$	$\mathbf{SNDR}_{peak}$	$\mathbf{A}_{in}@SNDR_{peak}$
285	0.5	0.2	0.5	1	1	1	107.71 dB	-4.43 dBFS

TABLE 3.4: Selected set of coefficients for the 3^{rd} order Σ-Δ Modulator of this work.

Fig.3.10 together with the occupancy levels shown in 3.9b, represents the simulation results obtained from the high level simulations. From this point the rest of robustness test performed in the following sections uses the coefficient of Table.3.4.



(A) Σ-ΔM PSD-spectrum.



(B) Σ-ΔM simulated SNR vs Vin.

FIGURE 3.10: High level simulation results of 3^{rd} order Σ-Δ modulator model of this work.

3.4 Mismatch robustness test

Small variations in the characteristics of identically designed devices occur during the manufacturing process of integrated circuits. These mismatches result in gain coefficient variations with respect to those defined during the high-level design, compromising the expected stability and performance.

Therefore it is interesting to verify the modulator robustness against coefficient variations using the behavioural simulations.

The proposed test consists in the evaluation of all the different possible combinations between minimum and maximum values of each coefficient for a given worst-case coefficient mismatch $\epsilon_{Mismatch}$. For a third order Σ-Δ Modulator with 6 coefficients, 64 different cases must be considered. Using the example of a second order Σ-Δ Modulator the 16 different cases are listed in Table 3.5 for the sake of clarity.

The test performs a $\epsilon_{Mismatch}$ sweep simulating all the different combinations and saving the worst SNDR result for each $\epsilon_{Mismatch}$ step point. Fig.3.11 plots the results of this sweep for the high level modulator model with the correct coefficients selected in the previous section(Table 3.4).

Robustness against coefficient mismatch up to 11.5% have been proved from the high level simulation results. The expected variation from a typical capacitor mismatch error in a practical SC Σ-Δ Modulator is much lower than the simulated results. Therefore, the selected set of coefficients ensure the correct modulator function.

Case	a_1	a_2	f_1	f_1
0	a_1	a_2	f_1	f_2
1	$a_{1,min}$	$a_{2,min}$	$f_{1,min}$	$f_{2,min}$
2	$a_{1,max}$	$a_{2,min}$	$f_{1,min}$	$f_{2,min}$
3	$a_{1,min}$	$a_{2,max}$	$f_{1,min}$	$f_{2,min}$
4	$a_{1,max}$	$a_{2,max}$	$f_{1,min}$	$f_{2,min}$
5	$a_{1,min}$	$a_{2,min}$	$f_{1,max}$	$f_{2,min}$
6	$a_{1,max}$	$a_{2,min}$	$f_{1,max}$	$f_{2,min}$
7	$a_{1,min}$	$a_{2,max}$	$f_{1,max}$	$f_{2,min}$
8	$a_{1,max}$	$a_{2,max}$	$f_{1,max}$	$f_{2,min}$
9	$a_{1,min}$	$a_{2,min}$	$f_{1,min}$	$f_{2,max}$
10	$a_{1,max}$	$a_{2,min}$	$f_{1,min}$	$f_{2,max}$
11	$a_{1,min}$	$a_{2,max}$	$f_{1,min}$	$f_{2,max}$
12	$a_{1,max}$	$a_{2,max}$	$f_{1,min}$	$f_{2,max}$
13	$a_{1,min}$	$a_{2,min}$	$f_{1,max}$	$f_{2,max}$
14	$a_{1,max}$	$a_{2,min}$	$f_{1,max}$	$f_{2,max}$
15	$a_{1,min}$	$a_{2,max}$	$f_{1,max}$	$f_{2,max}$
16	$a_{1,max}$	$a_{2,max}$	$f_{1,max}$	$f_{2,max}$

TABLE 3.5: Gain coefficients generated for the mismatch sensitivity test.

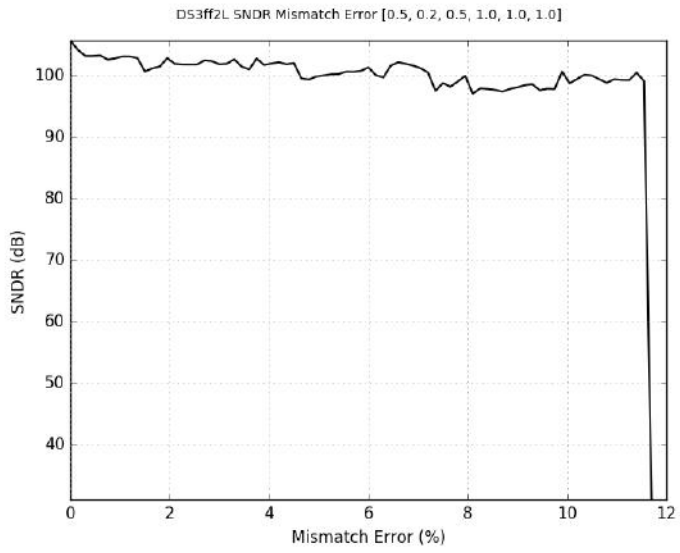


FIGURE 3.11: Mismatch coefficient test results.

3.5 Settling robustness test

The settling error at the integrators output is produced by several non-idealities present in the OpAmp, such as open loop gain, Slew-rate, limited Bandwidth and other related effects.

This error is modelled using the high level simulation flow (Fig.1.8) and is treated as a random noise which contributes directly at the output of the integrators.

Using the same second order feedforward Σ-Δ modulator presented in the first section of this chapter, the mathematical description added to the high level model is shown in Eq.3.10.

$$\begin{aligned} X_1(n) &= X_1(n-1) + a_1 \cdot (X(n-1) - Y(n-1)) + V_e(n) \\ X_2(n) &= X_2(n-1) + a_2 \cdot X_1(n-1) + V_e(n) \\ A_n(n) &= X(n) + c_1 \cdot X_1(n) + c_2 \cdot X_2(n) \\ Y(n) &= 1 \quad if(A_n(n) > 0) \quad else \quad -1 \end{aligned} \tag{3.10}$$

Where the $V_e(n)$ is the settling error random noise signal generated with a uniform distribution between -ϵ_{sett} and 0.

Simulation results presented in Fig.3.12, determine the maximum settling error ϵ_{sett} allowed at the output of the integrators. To comply with the specifications a maximum 0.02% settling error ϵ_{sett} is allowed. This top-down design methodology has been used in [30] as well in many other references [37][38] to stablish the requirements on the OpAmps from a high level model. However, as it will be explained in the next chapters, this work uses a novel bottom-up approach, which starts from practical and feasible values of circuit performances, extracting a set of characteristics with the aim to map them to the high level models. At this point a high level model is composed including circuital details allowing for a fast validation of the system.

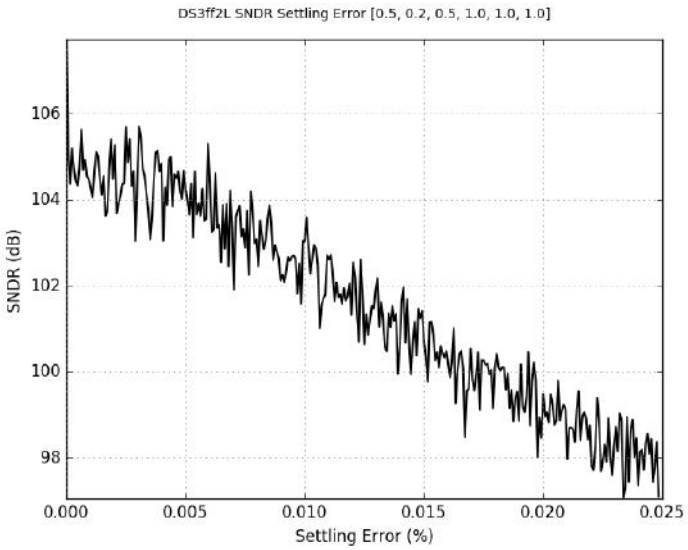


FIGURE 3.12: SNDR degradation as function of the integrator settling error.

3.6 Clock jitter robustness test

Discrete-time Σ-ΔMs are affected by errors during the sampling of the input signal due to timing uncertainties in the clock phases that control de SC operation.

The clock jitter effect is mainly limited to a sampling uncertainty of the input signal Δt. Because timing uncertainties during the integrator phase only causes an extra error to be added to the integrator settling error and their influence can be neglected in practice.

Sampling time uncertainty causes a non-uniform sampling of the modulator input signal that results in an increase in the in-band noise power. However, Σ-ΔM exhibit larger tolerance to clock jitter than Nyquist converters, because the in-band noise is reduced by the modulator OSR[24].

$$P_{Jitter} = \frac{\overline{V_s^2}}{8} \cdot \frac{(2\pi \cdot BW \cdot \sigma_{Jitter})^2}{OSR} \tag{3.11}$$

where P_{Jitter} is the resulting in-band power injected at the sampling input due to clock jitter , V_s^2 the maximum input signal power and σ_{Jitter} the standard deviation of the timing uncertainty.

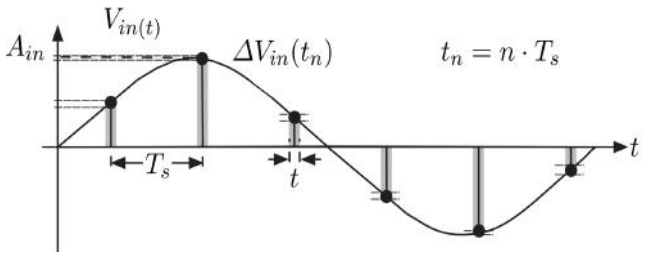


FIGURE 3.13: Graphical representation of a non-uniform sampling of a sinusoidal signal due to clock jitter.

Fig. 3.13, illustrates the non-uniform sampling process of the input signal due to time uncertainties Δt in the clock phases. It can be seen in this representation how the horizontal uncertainties Δt reflects to the vertical uncertainties ΔV_{in} at the nominal sampling times t_n. This allows, from an algorithmic point of view to maintain a uniform sampling and model of clock jitter effect directly on the amplitudes. It can be easily shown that the ΔV_{in} error relates to the Δt through the derivative of the input signal $v_{in}(t)$[25]. The Python code used to model this effect is listed as follows:

```
#Sinusoidal input waveform generator
t, Vin = stimulus_sin(InputAmplitude, fin, fck, ncycles)
nsamples = len(stim)
Vin_aux = np.zeros(nsamples)
#normal distribution
Delta = np.random.normal(0,Delta_Jitter,nsamples)

for p in range(0,nsamples):
    Vin_aux[p] = (Vin[p] - Vin[p - 1])*Delta[p]
    Vin[p] = Vin[p] + Vin_aux[p]
```

Clock jitter simulation results in Fig. 3.14, shows how the resolution is maintained until a $1 \cdot 10^{-3} \cdot Ts$ is reached and how the SNDR decreases as the clock jitter is increased. A maximum $5 \cdot 10^{-3} \cdot Ts$ clock jitter is allowed to comply with the 16 Bits target.

This result a valuable information for the clock generator to be designed on chip if a SoC solution is needed, or for the clock generator used during the laboratory measurements.

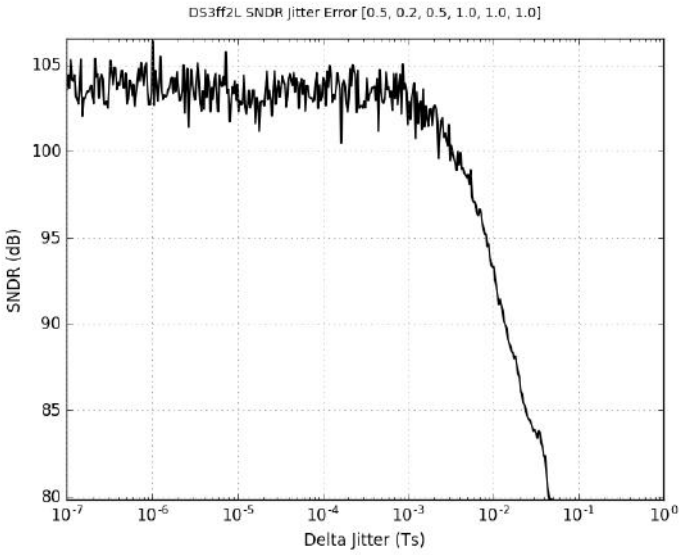


FIGURE 3.14: Clock Jitter test results.

3.7 Reference noise robustness test

Reference noise test aims to simulate the error introduced by variations in the feedback reference voltages. These variations are directly introduced in the input systems increasing the in-band noise level and affecting the final performance. As in the case of the clock jitter, the reference noise only affect the input stage in which the feedback is performed.

From the high level point of view the variations introduced in the references are modelled using a normal distribution. The Python code used to model this effect is listed as follows:

```
#normal distribution used in the reference error
RefInc = np.random.normal(0,Error_reference*0.5*fullscalepp,nsamples)

for k in range(0, nsamples):
    X1[k] = X1[k - 1] + (X[k - 1] - Y[k - 1] + RefInc[k])
    X2[k] = X2[k - 1] + a2*X1[k - 1]
    X3[k] = X3[k - 1] + a3*X2[k - 1]
    An[k] = X[k] + f1*X1[k] + f2*X2[k] + f3*X3[k]
    Y[k] = 1 if An[k] >= 0 else -1
```

During the simulation the worst SNDR value is saved at each error reference ϵ_{ref} step. Simulation result for ϵ_{ref} ranging from $1 \cdot 10^{-6}$ to $1\%FS$ are presented in Fig.3.15.

The response remains constant until it reaches a point ($10^{-3}\%FS$) in which starts decreasing. In order to comply with the required specifications a maximum variation of $5 \cdot 10^{-3}\%FS$ is allowed. These considerations should be taken into account during the package and testing stage, as well as during the eventual design of the SoC references.

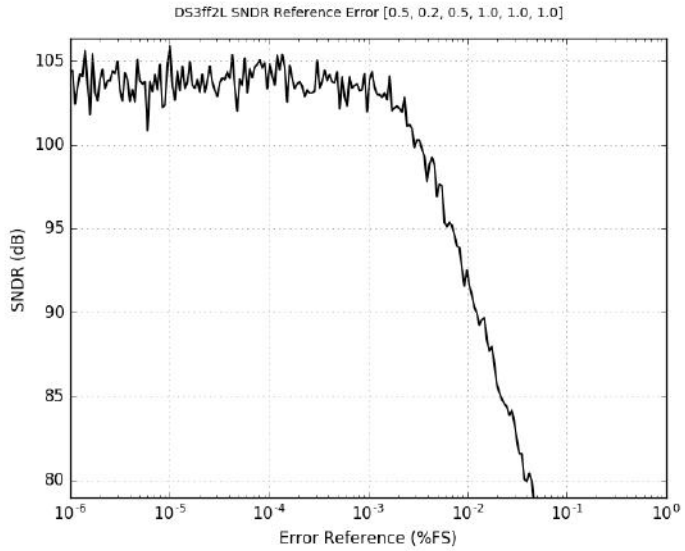


FIGURE 3.15: Reference noise test results.

3.8 Thermal noise

The overall noise contribution in the in-band noise is dominated by the first integrator. The capacitors in the SC sampler acts as a filter of the thermal noise produced by the switch resistance. For this reason, the thermal noise budget determines the minimum value of the sampling capacitor.

The total in-band noise power injected by the thermal noise (K_BT/C) does not depend on the equivalent switch resistor, but on the sampling capacitor C_s, the OSR and the absolute temperature T. For a fully differential implementation, the input capacitor values is[26]:

$$C_{s1} = \frac{2k_BT}{\overline{V_n^2} \cdot OSR} \tag{3.12}$$

Here, $\overline{V_n^2}$ is the maximum allowed noise power:

$$\overline{V_n^2} = \frac{\overline{V_s^2}}{10^{(SNDR_m)/10}} \tag{3.13}$$

where $\overline{V_s^2}$ is the maximum signal power and $SNDR_m$ is the required SNDR value with a certain safe margin. The sampling capacitor of the first stage is calculated following Eq.3.12, while the following sampling stages can be scaled down according to[20]:

$$C_{si} = C_{s1} \frac{\pi^{2i-1}}{OSR^{2i-2}(2i-1)} \prod_{k=2}^{i} \frac{1}{a_{k-1}^2} \tag{3.14}$$

Values obtained with Eq.3.14 represent the minimum sampling capacitor needed to comply with the thermal noise suppression specifications. But other related effects such as technological deviations in the capacitors may require the use of higher capacitance values.

In these cases the only consequence to a higher capacity value is related with the power consumption. As explained before there is an important trade-off between the capacity values and the power consumption requirements. High capacitance values implies more current to move the charge between capacitors, while low capacity values presents less current consumption, but higher sensitivity to thermal noise.

The final capacitor values selected are summarized in the next table.

Capacitance	Value	Capacitance	Value	Capacitance	Value
				Cff_0	0.5 pF
C_{s1}	5 pF	C_{in1}	10 pF	Cff_1	0.5 pF
C_{s2}	0.5 pF	C_{in2}	2.5 pF	Cff_2	0.5 pF
C_{s3}	0.5 pF	C_{in3}	1 pF	Cff_3	0.5 pF

TABLE 3.6: Capacitor sizing for the SC Σ-ΔM.

Fig.3.16 shows the output spectrum of the SC Σ-ΔM with and without thermal noise using the same sampling frequency f_s and -6dB_{FS} 12.8 kHz sinusoidal input for both cases.

The expected noise rejection form the sampling capacitor is confirmed by the high level K_BT/C noise simulation, thus ensuring the correct capacitor sizing.

It can also be observed how the sampling thermal noise increases the noise floor in the low frequency portion of the spectrum. But for high frequencies or approximately above the bandwidth point the spectrum is preserved.

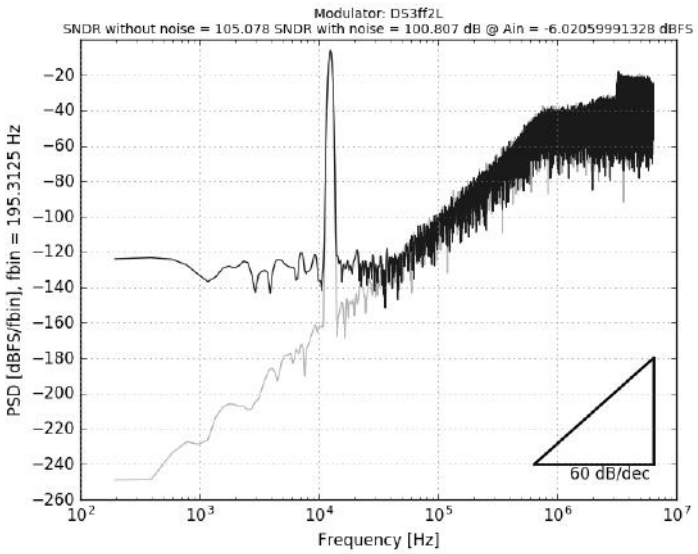


FIGURE 3.16: High level PSD-spectrum with (Grey) and without (Black) thermal noise.

Chapter 4

Circuit level design

High level models and test simulations are conveniently used to verify the Σ-Δ modulator correct behaviour and to efficiently map the electrical specification in the circuit level design. At that stage the modulator is still modelled at a system level, but some electrical quantities have been derived from the high level sizing. The circuit-level implementation of the 3^{rd} order SC Σ-Δ modulator is presented in this chapter, together with the explanation of its working principle.

The design process presented here, comprises a series of successive steps in which the high level models and simple ad-hoc circuit schematics are blended together to achieve an accurate, and yet fast, design which reserves only for the final verification the simulation of the whole Σ-Δ modulator at electrical level.

4.1 Switched Capacitor Σ-Δ Modulator

Fig.4.2 represents the SC fully-differential circuit implementation of the Σ-Δ modulator. The arrangement of the different clock phases to maintain the correct behaviour is a key point in the physical realization.

For the chosen third-order modulator a phase problem may arise from the use of switched OpAmps, which operates only in a determined phase of the clock cycle. This issue can be understood from the following argument. Typically in switched OpAmp configurations, stages operates in an interleaved fashion in such way that when the leading stage is active, the following is switched Off and vice versa. This responds to the switched OpAmp operating mode, where each OpAmp is periodically switched Off for power saving. In a typical two-phase clock this allows for a power savings up to 50%.

If the same principle is applied to the third order modulator of interest, as well for any odd-order modulator, this would drive the loop to instability due to an extra half delay necessary in the feedback DAC.

To make it clearer, consider the 3^{rd} order modulator of Fig.4.1, in which stage 1 and 3 are On, owning the first semi-cycle ($PhaseA$), while stage 2 operates during the second half of the clock cycle ($PhaseB$), respecting the classic interleaved switched OpAmp operation. In this case the Quantizer is forced to decide at the end of $phaseA$, just before the third stage is switched Off. This implies that the feedback DAC sample is ready to be used at the very beginning of $phaseB$, however the stage 1 is Off during this phase and cannot process it until $phaseA$ comes again. This can be accommodated easily, by using a flip-flop which holds the Quantizer state, for the half cycle needed to realign again with the active phase of the first stage.

Nevertheless, this half delay placed in the feedback path would dramatically change the loop filter transfer function invalidating the Σ-Δ modulator and its shaping properties.

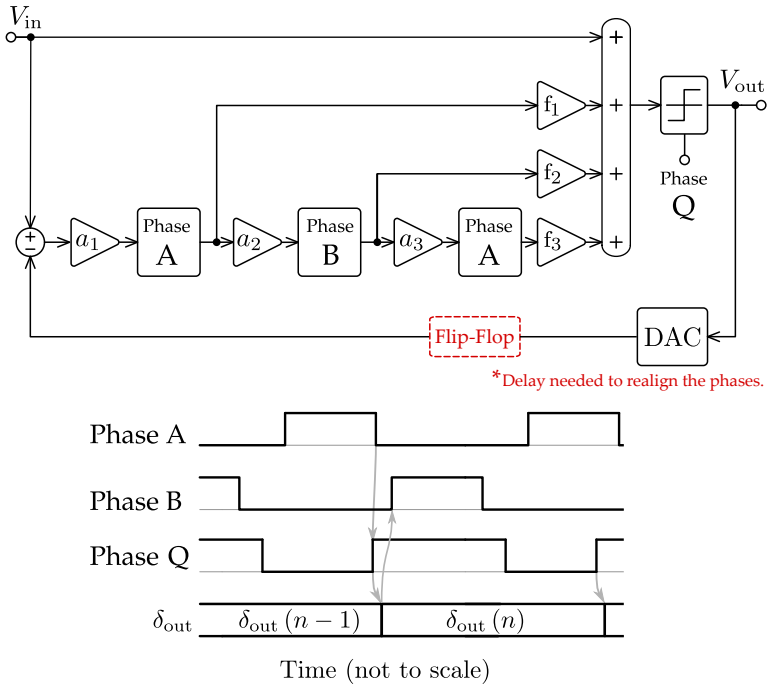


FIGURE 4.1: Interleaved operation of switched OpAmps in a 3^{rd} order Σ-Δ Modulator. This implementation modifies the loop transfer function in a way that make the modulator dysfunctional. It is shown here for illustration purposes.

A solution based on clock divisions in which each SOA is successively activated at a time is presented in [4]. In this case this solution can be accommodated by using a three phase clock, where each phase activates one stage at time. However, it would require faster time responses from the switched OpAmp, which translates in higher power consumption.

Here a different and novel approach is present to solve this problem allowing the use of two phase clock. The solution is depicted in Fig.4.2, where it is evident that SVMA2 (Stage 2) and SVMA3 (Stage 3) are operated simultaneously. The charge stored in the C_{s2} capacitors is immediately transferred to C_{in3} thanks to the combined action of SVMA2 and SVMA3. A sign inversion is now needed in the signal path, which is implemented by simply crossing the connection at the SVMA3 input. Now the quantizer can operate at the end of the second semi-cycle and deliver the sample at the beginning of the first semi-cycle when the first stage is On. By doing so, the half delay in the feedback path is removed and the desired loop filter transfer function is preserved.

Fig.4.2 shows more detail over the clock phases. Practical clock splitting comprises four phases, two of them for the NMOS switches and the rest for the PMOS switches, which are non-overlapped to avoid charge sharing in the actual SC implementation. Referring to the explanation given before, phase 3 and 4 map to $phaseA$ while phase 1 and 2 map to $phaseB$. A detailed description of the phase splitter is given in the following section.

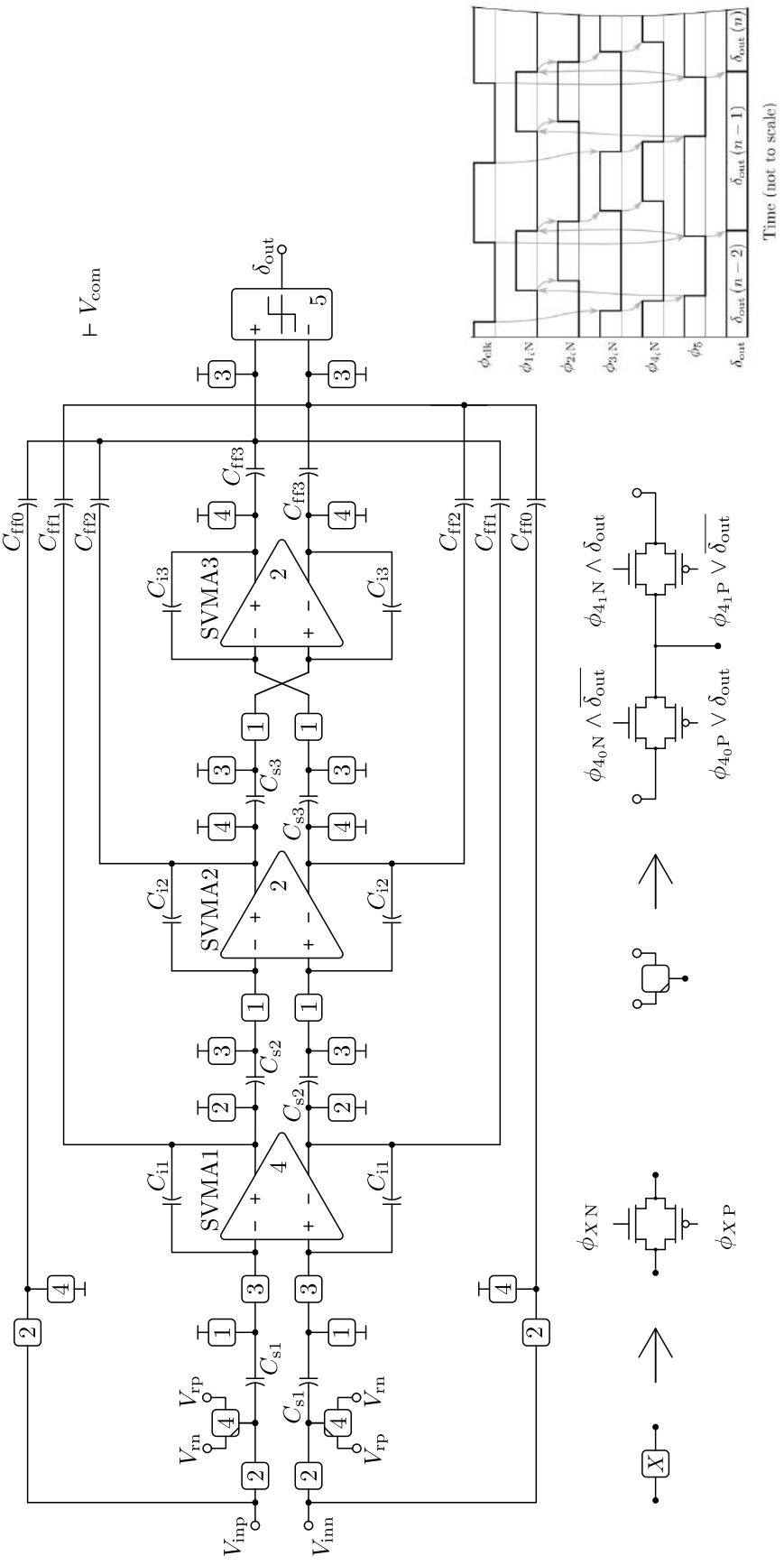


FIGURE 4.2: 3^{rd} order Σ-ΔM SC based on switched OpAmps. Here the switched OpAmps blocks are labelled as SVMA accounting for the switched variable mirror amplifiers.

An apparent discrepancy of the circuit presented in Fig.4.2 with the high level modulator of Fig.3.8 may rise, due to the fact that switched OpAmp based integrator is represented by the following transfer function $H(z) = z^{-1/2}/(1-z^{-1})$ instead of $H(z) = z^{-1}/(1-z^{-1})$. However a simple transformation described in Fig.4.3 can be used when a cascade of switched OpAmp integrators are considered.

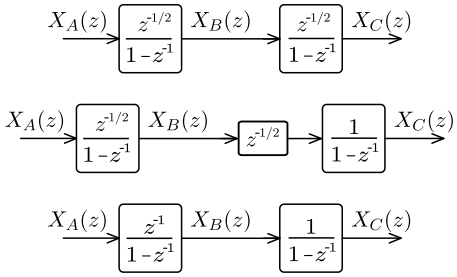


FIGURE 4.3: Rearrangement of half delays in a cascade of two half delay integrators.

The switches in Fig.4.2 are implemented using complementary transmission gates, avoiding bootstrapping techniques operating at supply levels higher than the nominal voltage of its CMOS technology, which at the end suppose shortening the device life. Special attention is paid in the input signal switches, which are one of the main distortion sources due to the high supported signal swing. The switch design process is discussed in Chapter 5.2.

All the different capacitors are derived from K_BT/C noise specifications using the expression presented in Chapter 3.8, to ensure the expected noise suppression inside the loop. The first sampling capacitor must be carefully sized and the rest can be scaled down proportionally to the corresponding ratios(Eq.3.14). The selected technology includes MiM capacitors with higher capacitance value per square micrometer, reducing the amount of area designed for the Table. 3.6 capacitors.

Feedforward signals from the intermediate states are summed by means of a simple passive capacitive divider. This solution attain to Low-power operation and avoids the DC current consumption of OpAmps based active adders. As introduced before, the modulator operation is defined in two different phases, aiming the separation of the sampling and integration process at each stage. This allows the integrators SVMAs to be switched off at different times and halving the power consumption.

The first operation phase illustrated in Fig.4.4 represents the input signal sampling process and its injection to the passive feedforward adder. While the SVMAs 2 and 3 are activated to process the quantization error and transfer its output to the same adder. At the end of the process, depending on the adder input signal, the quantizer changes its internal state and applies the corresponding feedback voltage for the next phase.

Fig.4.5 shows the second operation phase in which the first SVMA is activated to perform the charge redistribution and the quantizer feedback subtraction. At the same time, the next stage sampling process is completed. Charge injection from the output of the second integrator to the feedforward adder is also done during this phase.

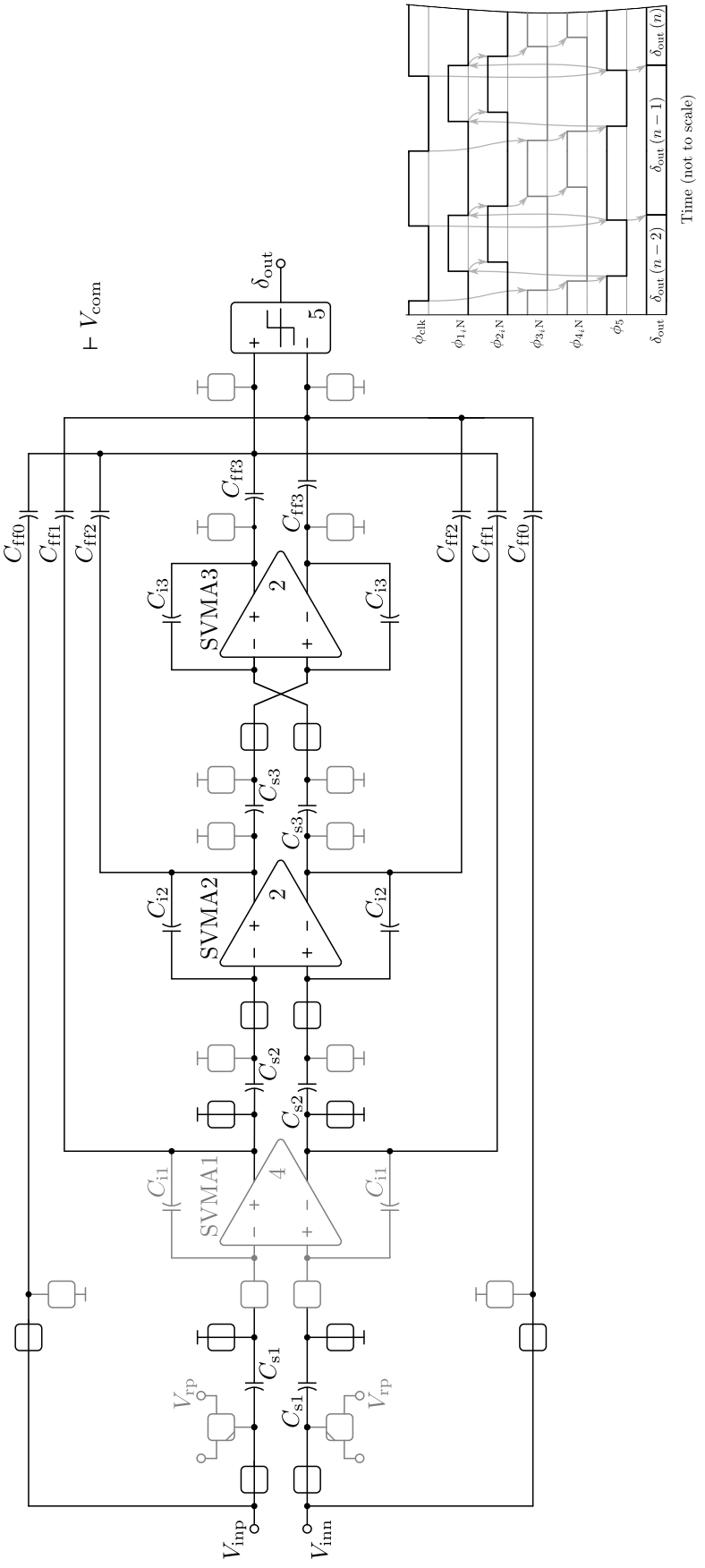


FIGURE 4.4: Σ-ΔM SC-switched OpAmp schematic during ϕ_{1-2}.

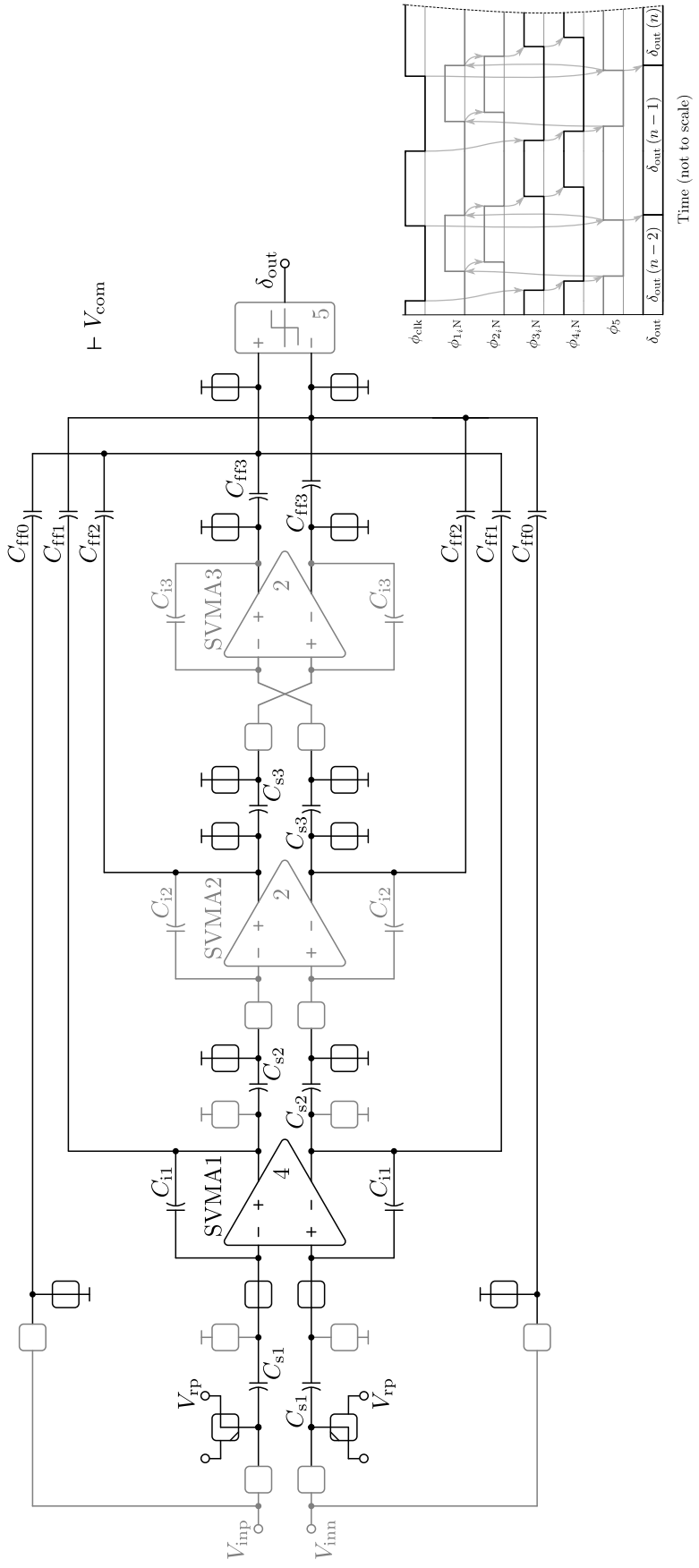


FIGURE 4.5: Σ-ΔM SC-switched OpAmp schematic during ϕ_{3-4}.

4.2 Modulator building blocks

In the following subsections the various blocks composing the modulator are described. These blocks are the phase splitter, a single bit quantizer and finally the SVMA which is the more important block of the whole modulator.

4.2.1 Phase Splitter

The phase splitter is in charge of generating the specific phases used to control the different processes inside the modulator. These processes involve the control of the different switches, SVMAs and the quantizer present in the topology. For this reason counterpart phases and its delayed versions are generated to control the complementary switches avoiding charge injection problems.

The generated control sequence of Fig.4.7, also ensures the synchronization between non-overlapped phases and the correct opening of the right-handed switches of the sampling capacitors C_{1-3} before their left-handed counterparts[38] to avoid input signal dependent charge injection and, as consequence, distortion.

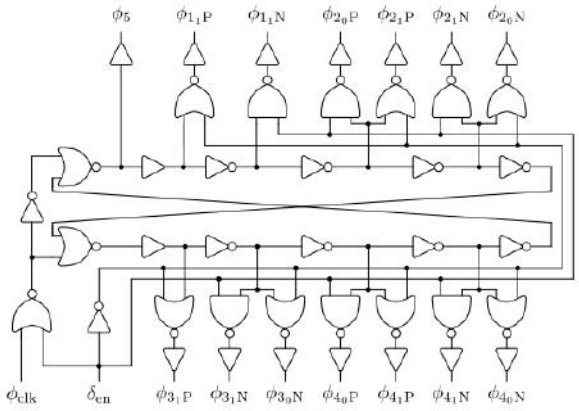


FIGURE 4.6: Σ-ΔM phase generator.

The clock generator employs the enable pin δ_{en} to force a determined position of all the phases during the initialization state, pre-charging all the different nodes to a known voltage. After the initialization, the process begins with the first half cycle phase ϕ_1 and its delayed version ϕ_2. In this phases the switches are configured to perform the following operations, as illustrated in Fig.4.4.

- First integrator input signal sampling operation into C_{s1}.
- Integration operation in the second and third stages.
- Summation operation of the feedforward signals(Input signal, second and third stage).

The phase ϕ_5 triggers the quantizer operation capturing its input signal slightly before the end of ϕ_1, thus updating the feedback voltage value before the next half cycle period.

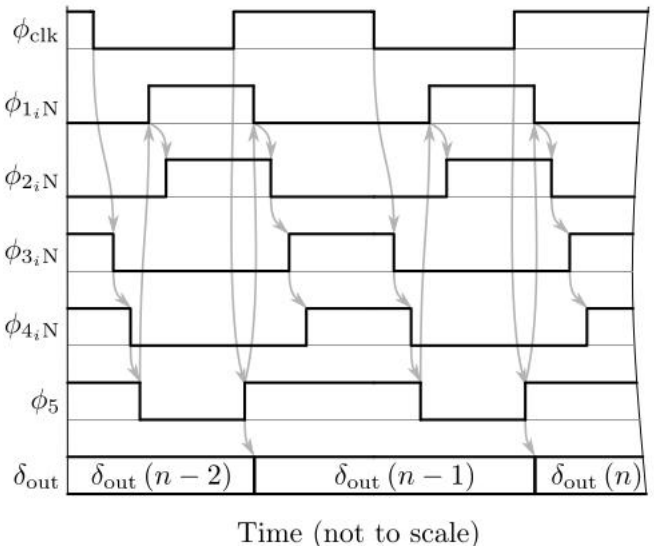


FIGURE 4.7: Σ-ΔM operation chronogram.

Phases ϕ_3 and its delayed copy ϕ_4 represent the second half period illustrated in Fig.4.5. In this phase the configured switch disposition performs the following processes.

- C_{ff0}, C_{ff2}, C_{ff3} and C_{s3} are discharged.
- Integration operation in the first stages and feedback subtraction.
- Second integrator sampling operation into C_{s2}.
- Summation operation of the feedforward signals(First stage).

4.2.2 Single-bit Quantizer

For single-bit Σ-ΔM, the quantizer requirements are relaxed as the systematic offset and the non-idealities in this stage are largely suppressed[37] by the feedback loop action, allowing the use of simple quantizer structures with negligible static power consumption.

Single bit quantizer realizations are mainly based on dynamic comparators and SR flip-flops to hold the result[41][22]. Fig.4.8, illustrates the selected architecture of the quantizer.

The quantizer operation is determined by both half periods of ϕ_5. Starting when ϕ_5 is at the first half period (low level state) the nodes V_{tn} and V_{tp} are pre-charged to the power supply voltage V_{dd}, while nodes V_{bn} and V_{bp} are discharged to ground because transistors $MI1$ and $MI2$ are in cut off region.

In the second half period, when ϕ_5 is at high voltage state the current through $MI1$ and $MI2$ starts flowing discharging the associated capacitances in nodes V_{tn} and V_{tp}. At that moment depending on the $MD3$ and $MD4$ gate voltages a difference in the current flow between branches is created. These difference is amplified when one of the V_{bn} or V_{bp} nodes reaches one threshold voltage V_{th} increasing the difference and forcing the latching effect in the output nodes.

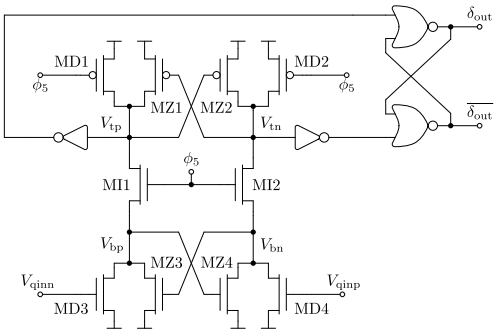


FIGURE 4.8: Σ-Δ modulator single bit quantizer.

The analog outputs V_{tn} and V_{tp} are translated to the digital domain by means of inverters. The SR flip-flop is then used to hold the output values and avoid possible errors due to false triggering. Fig.4.9 shows the different node waveforms and how they behave when ϕ_5 is activated by a rising pulse.

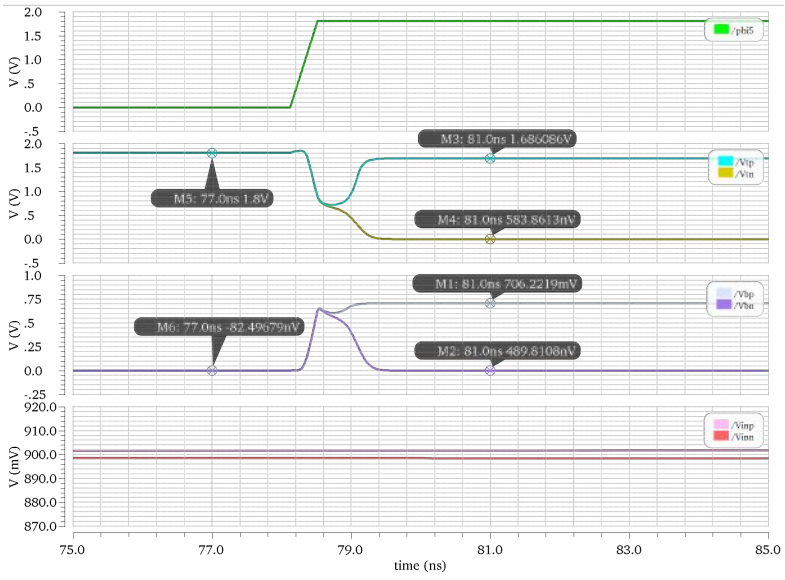


FIGURE 4.9: Σ-Δ modulator single bit quantizer waveform representation.

4.2.3 Switched Variable-Mirror Amplifiers

Low power SC Σ-ΔM requires robust OpAmp circuits capable of managing high peak currents produced during the switching phases but, at the same time, consuming very low DC currents when their current capability is not needed. OpAmp operating in Class-AB seems a promising way to control peak currents while maintaining a low static current consumption. Multiple Class-AB OpAmps realizations are reported in the literature[39][21][13], exhibiting different approaches and trade-offs.

A new Class-AB family of variable current mirror amplifiers (VMA) is presented in [33], reporting interesting improvements and features which makes them a good solution for SC Σ-ΔM.

With respect to other OpAmp topologies, such as [39][21][13] the solution of [33] generates all the Class-AB current in the output transistors only i.e. power is delivered only to the load without influencing the bias of the internal branches. Furthermore it exhibits a very low sensitivity to both technology and temperature deviations. Thanks to the proposed topology, Class-AB peaks are fully invested in the output transistors only. Apart from the inherent power saving, this single-stage solution avoids current and area overheads associated to compensation techniques needed in multistage designs.

4.2.3.1 Switched Variable-Mirror Amplifiers principle of operation

The proposed VMA architecture illustrated in Fig.4.10, starts from a basic fully-differential architecture with two complementary differential pairs. The use of two distinct input transconductors allows to split the input signal in two paths for separate Class-AB control of NMOS and PMOS output transistors.

The boxed part in the same figure represents the dynamic current mirrors which constitutes the core of the OpAmp. They can be understood as fully-differential voltage-controlled (V_{cp} and V_{cn}) non-linear current amplifiers (I_{oNp}/I_{iNp} and I_{oNn}/I_{iNn}), which adapt their gain dynamically and symmetrically depending on operation point thanks to the cross-coupled partial positive feedback.

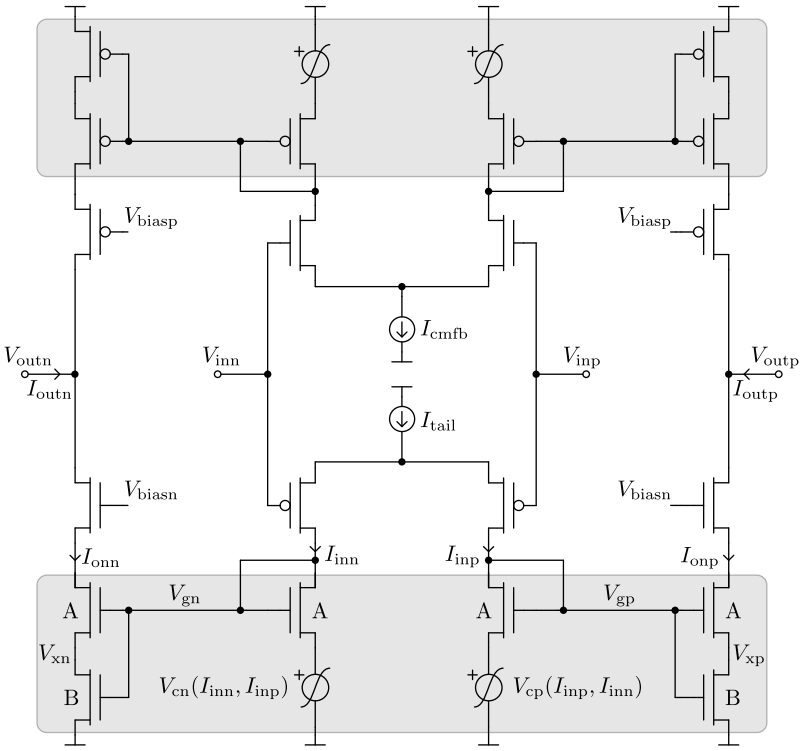


FIGURE 4.10: General architecture of the proposed VMA[33].

Eq.4.1 represent the different operating zones which are also qualitatively illustrated in Fig.4.11.

$$\begin{cases} I_{outp} > 0 & V_{cp} > V_{xp} & I_{oNp} \gg I_{iNp} \\ I_{outp} \equiv 0 & V_{cp} \equiv V_{xp} & I_{oNp} \equiv I_{iNp} \equiv I_{tail}/2 \\ I_{outp} < 0 & V_{cp} < V_{xp} & I_{oNp} \ll I_{iNp} \end{cases} \tag{4.1}$$

As noted in Fig.4.10 the internal core of the dynamic current mirror always operates in Class-A, with the consequent benefits in terms of dynamic-to-static power consumption. When high current peaks are demanded the output transistors are the ones in charge of draining the required Class-AB current.

Fig.4.11 represents qualitatively the final structure behaviour when the current requirements changes, showing how the structure behaves as a Class-A architecture when the differential input currents are low enough, while providing the Class-AB boosting when large currents are needed.

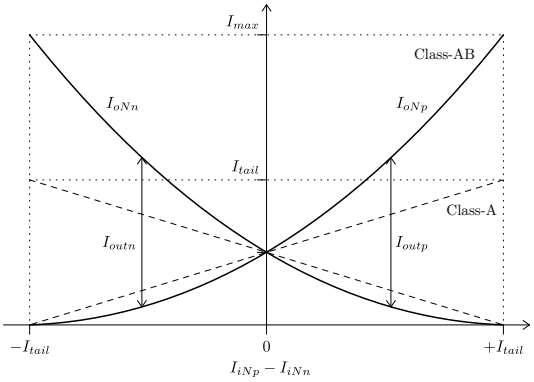


FIGURE 4.11: Qualitative large-signal Class-AB operation[33].

The I_{cmfb} current source in Fig.4.10 accounts for the output common mode regulation which can be implemented in a very standard way. In the design of [33] the output branches are provided with folded cascode transistor to improve the open-loop voltage gain.

4.2.3.2 Switched Variable-Mirror Types

From the dynamic current mirror two different solutions are possible to implement the dynamic current mirror. The first one is called Type 1 and is presented in Fig.4.12. It is based on a cross-coupled matched pair which introduces the amount of positive feedback responsible of the Class-AB behaviour. To prevent the complete OpAmp from latching, an additional C-sized crossed transistor is incorporated providing some amount of negative feedback. Optimum balance between positive and negative feedback can be simply achieved by matching ratios B and C. The gate voltage V_{bias} required for the C-sized transistors is directly obtained from the matches composite active load biased at I_{tail}.

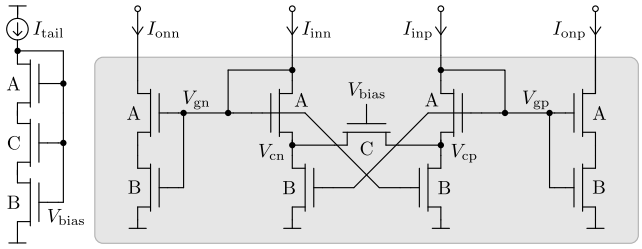


FIGURE 4.12: Type 1 Class-AB current amplifier[33].

The second Class-AB circuit proposal for the boxed parts in Fig.4.10, basically replaces the C-sized crossed transistor by two split counterparts. This is referred to be the Type 2. The negative feedback generation needed is guaranteed and the V_{bias} voltage required in the Type 1 avoided. This can suppose a reduction in the power consumption as two I_{tail} are suppressed from the circuit. However, it is also true that a proportional reduction in the current value to bias the active load is possible in order to bring closer both topologies in term of consumption.

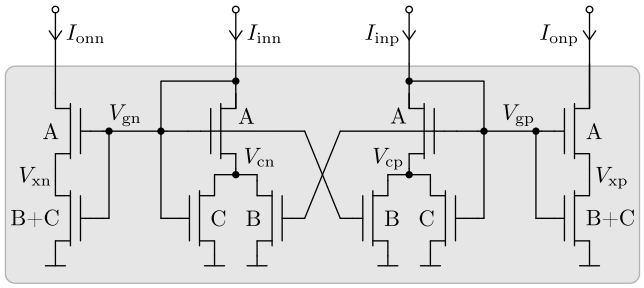


FIGURE 4.13: Type 2 Class-AB current amplifier[33].

For both types, a proper selection of A, B and C values allows a wide range of Class-AB modulation indexes in all regions of operation. The Class-AB modulation index is defined as the ratio between the maximum current drived by the output transistors and the tail value selected in the differential pairs. An unified expression for both types of SVMAs and different transistor regions of operations is reported in [33] and presented in Eq.4.2.

$$K_{AB} = \frac{I_{max}}{I_{tail}} \simeq \frac{1 + \frac{A}{C}}{1 + \frac{A}{B+C}} \rightarrow if A = B + C \rightarrow K_{AB} \simeq 1 + \frac{B/C}{2} \tag{4.2}$$

A practical approach is to set the A coefficient to be the $B+C$, in this way the degrees of freedom are reduced and the design task is easily achieved. Analytical expressions showing no technological and temperature dependency are developed and discussed in [33]. In the case of this work the robustness of the different topologies is proved by the simulation results presented in the next chapter.

4.2.3.3 Switched Variable-Mirror SC implementation

The switched OpAmp implementation of the VMA, called SVMA, requires from certain modifications that does not affect the behaviour described above. These modifications are basically the addition of different switches to convert the topology into a switched variable mirror amplifier SVMA. They also include the CMFB circuit in charge of the output common mode voltage. Fig.4.14 represents both On/Off SVMA operation phases.

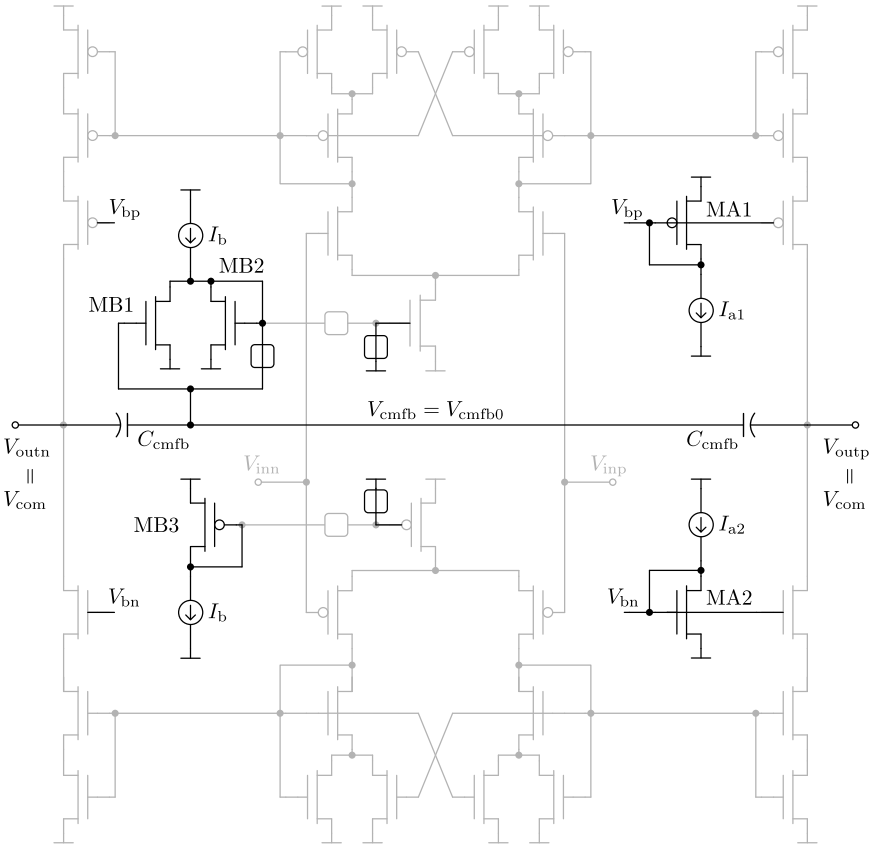
During the Off phase illustrated in Fig.4.14a, the tails of both differential pairs are connected to the corresponding rail stopping current flow through the structures. This allows a 50% of power reduction with respect a non-switched VMA.

Another important point is related to the CMFB operation circuit. In this phase following the chronogram of Fig.4.7 the differential outputs of the integrators are tied to the common mode voltage V_{cm}(Fig.4.4). At the same time transistor $MB1$ and $MB2$ from the CMFB are wired to the middle point formed by the C_{cmfb} capacitors. The diode connection of $MB1$ and $MB2$ generates a voltage difference between the output value and middle point. This difference allows the capacitors to be charged at a certain point in which the current from both $MB1$ and $MB2$ transistors are the same.

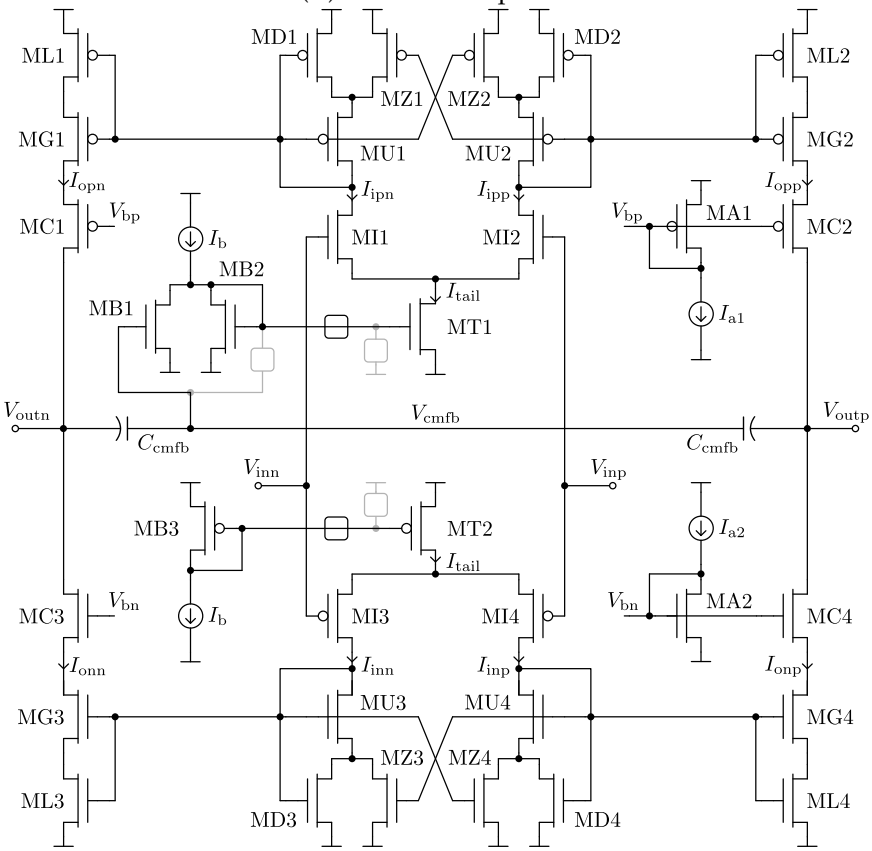
When the SVMA are switched On the tails of the differential pairs are connected to the corresponding mirrors, allowing the current to flow trough the different branches.

Regarding the CMFB, the middle point connection of $MB2$ is opened and directly wired to the tail transistor $MT1$. The other $MB1$ middle connection is maintained and the CM voltage constantly sensed using the C_{cmfb} capacitors. If a variation in the CM voltage is observed the $MB1$ changes its current affecting the $MB2$ polarization, which in turn adjust the current flowing trough the tail re-adjusting the outputs voltage.

Finally, each SVMA will be designed and simulated independently aiming to achieve the lowest current consumption while maintaining the expected requirements. The design process and simulation results are introduced in detail in the next chapter.



(A) SVMA in off phase.



(B) SVMA in on phase.

FIGURE 4.14: SVMA schematic during off phase (A) and on phase (B).

Chapter 5

Circuit optimization and simulation results

Each individual block defined during the circuit level design is simulated and optimized to achieve the required performance. The simulation results and the optimization process followed during this stage of the transistor level design is described in this chapter. Finally, simulation results from the complete system are performed to confirm the expected behavior from the design methodology proposed in this work.

5.1 Simulation Testbench

During the simulation and optimization process a reduced testbench of the complete system described in Chapter 4 is used. The proposed testbench in Fig.5.1, includes all the boundary conditions imposed by the complete system, but reducing the complexity and hence the simulation time. It reproduces the same operating conditions of each integrator stage inside the modulator. Switches and the SVMA is operated alike to reproduce the same transient behaviour. The differential input (V_{inn_i}, V_{inn_i}) is fixed for each transfer operated by the integrator.

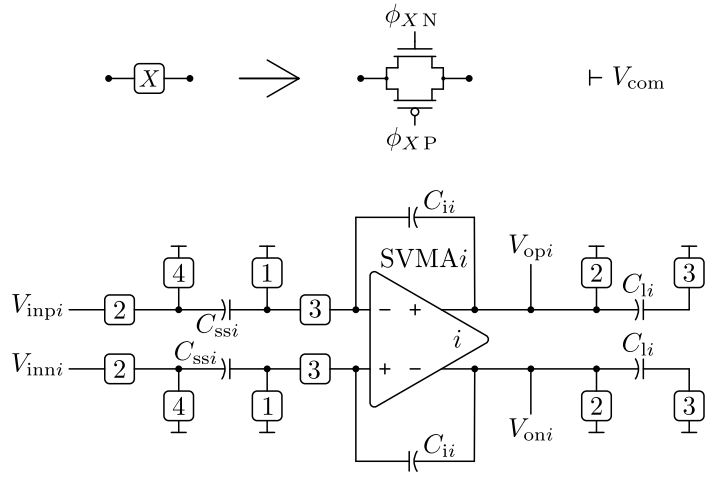


FIGURE 5.1: Reduced Testbench schematic used in the optimization processes.

The equivalent capacitors shown in Fig.5.1 depend on the stage to be designed. Therefore, C_{ss_i} and C_{i_i} corresponds respectively to the C_{s_i} and C_{in_i} value of the former stage to be optimized.

In the case of the first and second stage C_{li} capacitor corresponds to the sum of the current stage feedforward capacitor C_{ff_i} and the following sampling capacitor C_{s_i}, while in the third is equal to the feedforward capacitor C_{ff3}. Table 5.1 summarizes the different values at each stage.

Parameter	1^{st} Stage	2^{nd} Stage	3^{rd} Stage
C_{ssi}	5 pF	10 pF	1 pF
C_{ii}	0.5 pF	2.5 pF	1 pF
C_{li}	0.5 pF	1 pF	0.5 pF

TABLE 5.1: Capacitor values used in Fig.5.1.

Depending on the part of the circuit to be studied different views of the same block are used, changing between ideal and transistor level block. This allows the separation of the different contributions to the final results achieved.

At this point, the aim is to stablish a relation between the electrical characteristic that describes the circuit of Fig.5.1, and the high level simulation model. One way to achieve this, is by introducing input signal dependent integrator gain parameter in the high level model which will be dependent on the different limitation imposed by the transistor level blocks. Therefore, a parametric sweep varying the differential input amplitude is performed while acquiring the differential output waveform.

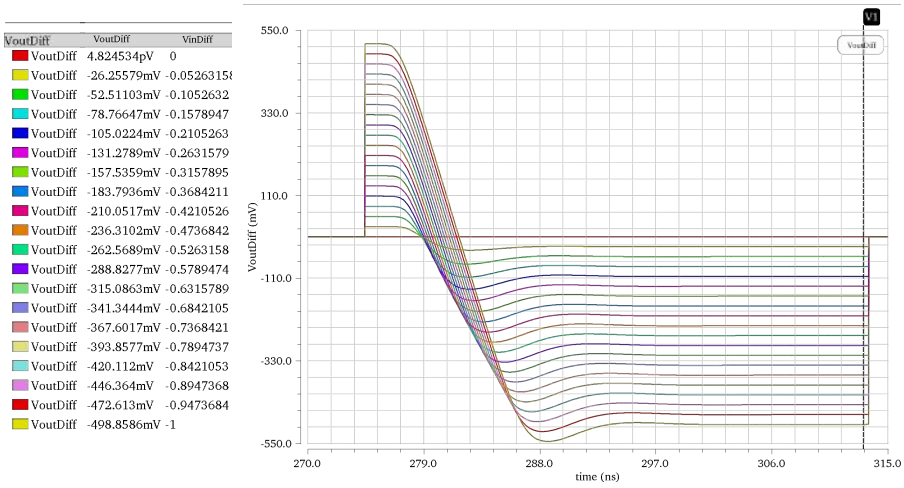


FIGURE 5.2: Differential output voltage waveforms during the integration phase for input differential voltage ranging from 0 to -1 V.

An example is illustrated in Fig.5.2, which shows the differential output wave obtained during the integration phase. The marker in the figure indicates the point in which the signal must be ready to be acquired by the next stage. All the different values between input and output are displayed in the left part of the figure. Fig.5.3 represents the relation between the differential input and output voltage.

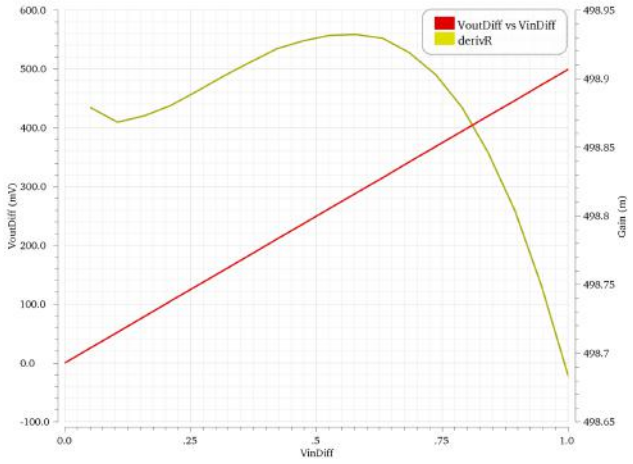


FIGURE 5.3: Differential output voltage (Red) and its derivative (Yellow) representation obtained from Fig.5.2.

The slope of the differential output voltage represents the gain as function of the differential input voltage. This gain representation only allows for a qualitative overview of the structure behaviour. The performance is assessed by means of the high level simulation extracting by interpolation the charge-transfer characteristic curve.

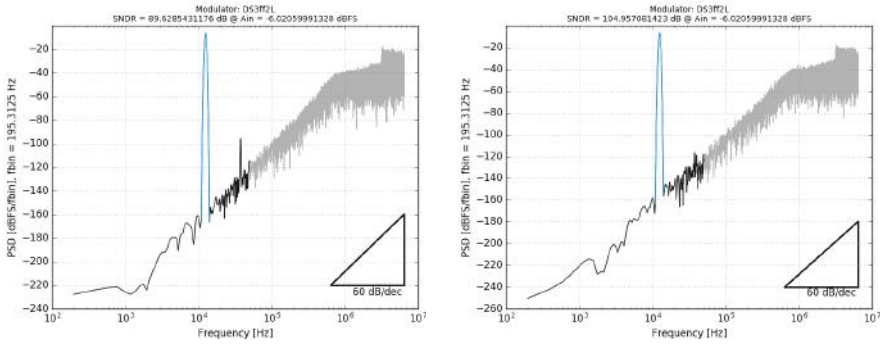
A Cubic spline interpolation is used, other interpolation methods such as polynomial fit has been also tried, but they result to be not numerically stable as the cubic spline interpolation, which forces the resulting functions to pass through the different points ensuring no numerical errors are generated from the interpolation process.

The following code shows the simple Python implementation of this feature:

```
#Spline interoplation
FitC1T = interpolate.splrep(VinDiff, VoutDiff, s=0)

for k in range(0, nsamples):
    #First coefficient a1 subtituted by spline interpolation method.
    X1[k] = X1[k - 1] + interpolate.splev((X[k - 1] - Y[k - 1]), FitC1T,
    der=0)
    X2[k] = X2[k - 1] + a2*X1[k - 1]
    X3[k] = X3[k - 1] + a3*X2[k - 1]
    An[k] = X[k] + f1*X1[k] + f2*X2[k] + f3*X3[k]
    Y[k] = 1 if An[k] >= 0 else -1
```

Fig.5.4, illustrates two different simulation results obtained with the method mentioned above. In the case of Fig.5.4a the distortion generated by the transistor level block is appreciable reducing the expected resolution. After modifying the design parameters a new simulation result is obtained and represented in Fig.5.4b.



(A) (B)

FIGURE 5.4: High level simulation results for two design cases of Fig.5.1. In (A) is evident an harmonic distortion in the spectral density due to non-linearity of the charge transfer characteristic curve. (B) represents a better design choice where the harmonic distortion is more attenuated.

5.2 Switches

Switches in SC Σ-ΔM topologies are a fundamental part in the design process, because all the signals are driven trough them. Therefore, non-idealities present in the switches are directly injected in the signal paths causing the distortion and noise level to increase reducing the final resolution.

All the switches used in SC Σ-ΔM are based on pass-gates, where the NMOS and PMOS are parallel connected and driven at their respective gate by complementary digital signals. The most important design specification of CMOS switches are the on-resistance R_{on}. The R_{on} value ideally is supposed to remain constant for all signal levels, but in practice the R_{on} have a non-linear behaviour. This non-linear characteristic depends on the switch polarization conditions, which are mainly affected by the voltage to be transmitted. This is a potential source of harmonic distortion to be avoided. Also, the clock feedtrough, charge injection and leakage of the switches suppose a source of harmonic distortion, affecting the expected resolution.

Special attention must be paid for sizing the switches of the first stage, because any non-linearity originated at the input sampler will not be shaped by the loop and will appear directly at the output.

The on-resistance R_{on} and its non-linearities, can be reduced by increasing the aspect ratio W/L of both transistors, but the area and consequently the gate-to-drain-source parasitic capacitances arises, supposing a problem when the external capacities are of the same or similar value as the parasitic ones. Since the signal driving the gate has a large swing, its coupling with the useful signal may result intolerable if the parasitic capacitance is too high. Therefore, there is a trade-off between maximum value of R_{on} that can be tolerated and the drain-source parasitic capacitances, that are in turn conditioned by the value of capacitor used in the SC branches.

The rest of stages are scaled down to fit with the required noise suppression chain and therefore lower switch sizes are normally used.

The optimization process attains all the non-linear effects and simulates the different switches in a reduced testbench of Fig.5.1 which contains the same boundary conditions as the complete system.

5.2.1 Switches optimization process

Not all the switches have the same relevance inside the SC modulator. To explain this a reduced version of the first stage is presented in Fig.5.5.

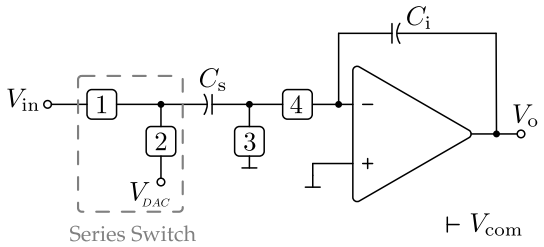


FIGURE 5.5: SC Σ-Δ modulator first stage schematic showing relevant issues regarding the sampler switches.

As explained before, the R_{on} value is ideally supposed to be constant but in reality it changes depending on the NMOS/PMOS polarization. Taking this fact into account, it is then easy to understand which switches are going to suffer the most from this variation.

Switch number one in Fig.5.5, supports the highest voltage swing in the circuit, changing its polarization and therefore its R_{on} value depending on the input signal voltage. This series switch is a source of distortion to be avoided by a proper sizing during the design.

The design strategy adopted here chooses L to be small enough for speed while, at the same time, checking its R_{off} to be adequate to avoid important signal leakage in the OFF state. In this design $L = L_{min}$ proved to be acceptable in this regard. Then, a trade-off for W has been reached, because larger W allows better linearity and speed, up to the point that the clock injection and feedtrough effect begin to appear.

Sizing of switches 1 and 2 are identical to dynamically compensate for the latter effects. Since they are operated in a complementary fashion, the charge released or coupled to 1 when its channel is destroyed, is immediately absorbed by 2 when its channel is created. The same technique allows for switch 3 and 4 to share the same geometry.

Luckily, bootstrapping techniques operating at supply levels higher than the nominal voltage values of its CMOS technology which at the end suppose shortening the device life and an increase in the yield, proved not to be necessary for the input switches, so they have been avoided.

Switch number two is also considered a series switch as the DAC feedback voltage is connected to one terminal. But is not that critical in this design thanks to the fact that the voltage varies between only two fixed points of inverse polarity, being a two level DAC design.

Switch three is connected to the virtual ground which operates in a near zero voltage variation, while switch number four is connected to the common mode voltage V_{com}. Both switches with one terminal connected to a fixed voltage do not represent a critical issue to be considered during the

design, apart from introducing too much delay in the charge transfer, however this can be accommodated easily with moderate size of W.

In the second and third integration stage illustrated in Fig.5.6, the series switches are replaced by switched OpAmps, which ensures linearity thanks to its very low output impedance. Therefore, the switches from these stages can be scaled down by the same factor used in the capacitances, from the sizing obtained in the first stage.

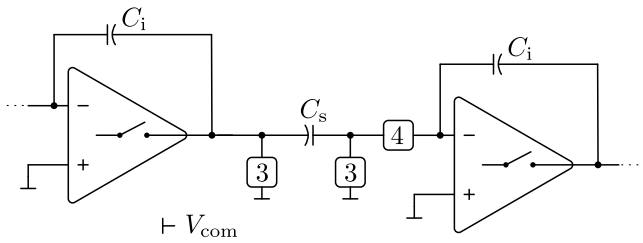


FIGURE 5.6: SC Σ-Δ modulator second and third stage schematic illustrating the switched OpAmp action on the switching scheme.

To study the impact of the switches alone, the SVMA of Fig.5.1 is substituted here by a VerilogA model. The design process start from left to right substituting the ideal switches by transistor level blocks. In this case, a minimum length L_{min} allowed by the technology is used for both NMOS/PMOS transistor while the $W_p = 3 \cdot W_n$ is hold to equalize the different charge mobilities between NMOS and PMOS devices.

5.3 Switched Variable Mirror Amplifier

The former section represents the design process and the results obtained from the most important block of SC Σ-Δ modulator. A poor design of this block could lead in a failure during the modulator operation, reducing the expected resolution or even creating instabilities that force the system to stop modulating.

5.3.1 Design space and alternatives

The SVMA schematic circuit from Fig.4.14 can be separated in four main blocks, the dynamic current mirrors which depends on the selected SVMA Type, the input differential pairs, the cascodes and finally the current mirrors used in the tail of the differential pairs. Each individual block performs a different function and has different design rules.

The dynamic current mirrors are sized to maintain transistors A in saturation and B in ohmic region, while ensuring enough room for the differential pair to work properly. As explained in Chapter 4.2.3.2, the Class-AB coefficient K_{AB} depends on geometrical proportion between transistors A, B and C, defined for all regions of MOS operation by Eq.4.2. During the design process a practical assumption consistent on $A = B + C$ and $C = 1$, for both SVMAs is taken to reduce the number of degrees of freedom.

Cascode transistors in the output branches can be added to improve the open-loop voltage gain. The optimum biasing of these stacked devices for maximum output full-scale can be easily obtained from [2].

Current mirrors from the differential pairs tails are polarized in strong inversion [6], ensuring a correct current copy while maintaining a low drain-source voltage.

Finally the differential pair inversion coefficient IC is set to be one, which is considered a good rule of thumb. Qualitatively, if it is considered a $IC \geq 10$ (strong inversion) current can be always reduced and the width W widened for a target gm. Since a single-pole OTA stage the pole itself is determined by the ratio of gm over the capacitive load C_L, it means that for a target bandwidth, the current can be reduced and so the power, when the pair is operated in strong inversion.

For very wide devices, the gm approaches the theoretical limit of $I_D/\eta U_T$, where η is the sub-threshold slope factor and $U_T = K_A T/q$ is the thermal voltage. In this case where $IC \leq 1/10$ (weak inversion), the input capacitance C_{IN} may eventually dominate over the sampling capacity C_s and introduce a critical signal dependent attenuation on the desired integrator coefficient:

$$a_i = \frac{C_s}{C_{Feedback} + C_{IN}(V_{in})} \tag{5.1}$$

To compensate for this, the designer may increase C_s and $C_{Feedback}$, but at the expense of more power required to drive larger capacitors.

In this case the beneficial effect on low frequency noise, in having large input devices is not needed since the OpAmp is configured as an integrator, meaning that its input-referred-noise is first order shaped.

The above discussion proves that setting the operation region of the differential pair to be in moderate inversion ($IC = 1$) is the best suited solution for low-power design.

Observing the state-of-the-art described in Chapter 1.3, in can be concluded that in order to get close to the boundary defined by Schreier [26], it is necessary to scale down the static power consumption. The previous design [33] presents an I_{tail} current in the order of 1.2 mA for the first stage, and in the case of this work a first current reduction to 200 μA is achieved. Also, the output cascode transistors implemented in the previous work implies the addition of more current branches biasing the cascode transistors and also a reduction in the output swing.

At this point of the work, it is questioned the cascode implementation as an additional part to increase the open loop-gain aiming to achieve the expected resolution. Therefore, all the possible candidates are the combination between both SVMA types and the use of output cascode.

Table 5.2, summarizes the simulation results for all the possible SVMA combinations with a Class-AB index equal to 6. The results presented are obtained from the optimization process described above, and also from individual testbenches used to obtain the differential and common mode gains and phases.

	Cascode	Differential		CMFB		Optimization
		Gain	Phase Margin	Gain	Phase Margin	SNDR
Type1	No	54.37 dB	55.36 °	49.47 dB	82.15 °	104.62 dB
	Yes	74.66 dB	53.67 °	80.73 dB	80.95 °	105.08 dB
Type2	No	55.72 dB	49.42 °	50.74 dB	84.95 °	105.25 dB
	Yes	81.59 dB	49.62 °	81.18 dB	81.71 °	103.18 dB

TABLE 5.2: SVMA candidates performance for $K_{AB} = 6$ and $I_{tail} = 200\mu A$.

The transient simulation results obtained from the four combinations, with the optimization process explained above, present a low deviation between them and also with the high level results. This makes clear that the addition of the output cascodes in both topologies increases the differential and common mode gain, but this increment is not necessary as the SNDR results achieved are the same. Therefore, the cascode is discarded in this work allowing the reduction of the current consumption while increasing the output voltage swing.

5.3.2 Slew rate and linear relaxation

In [33] both transient regimes where analyzed in a simplified way by trating them as independent design parameters. The slew rate was derived directly from the current capability, while the linear relaxation was derived from the OpAmp bandwidth. Both parameters can be mapped then to a bias current and a Class-AB modulation index, which represent the real design parameters to be optimized. In practice, both parameters are related to each other in a way that a modification of one parameter may affect both the slew rate and the relaxation time.

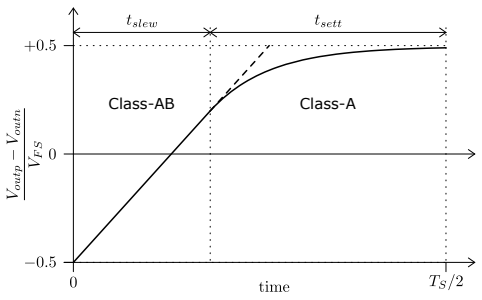


FIGURE 5.7: Qualitative transient response of the VMA differential output voltage.

Fig.5.7, illustrates qualitatively the differential output voltage response of a general SVMA structure. The displayed waveform corresponds to the second half period in which the charge stored in the sampling capacitor C_s is transferred to the integrator capacitor C_{in}, thanks to the action of the SVMA acting as a charge pump. From this transient response, two regions are differentiated in the figure. The first one corresponds to the slewing regime in which the output voltage rate of change is determined by SVMA slew-rate (SR).

Here the current capability is determined by Class-AB operation of the SVMA. The second part corresponds to the relaxation regime limited by the small-signal time constant of the single stage acting as a Class-A topology.

Increasing the Class-AB index, the slew-rate of the SVMA increases, moving the transition between regions to the left, shortening the slewing time and therefore increasing the relaxation time.

However, it can be shown that increasing the K_{AB} coefficient also have an effect on the bandwidth itself, since it lowers the parasitic pole associated to the Class-AB mirror of Fig.4.10.

Although an accurate small signal analysis may be carried on, attention must be paid to the fact that a transition is performed during the transients of Fig.5.8 making the small signal approximation only marginally valid.

One phenomenon which turns to be important at this stage, but poorly modelled by a small signal analysis, is the overshoot occurring eventually, at the end of the slew rate regime. When an overshoot occurs, it is interpreted as an excess of Class-AB, since the Class-AB control was not fast enough to reduce its action. In this case, the designer can either increase the total bias current in order to make it faster, but at an expense of power, or decrease the K_{AB} coefficient down to a value that avoids this overshoot. The second choice is evidently preferable while the relaxation time is minimally affected, allowing for a good settling characteristic. Nevertheless, if the total bias current is too low, the settling may result too poor, regardless of the K_{AB} value, so in this case an increase of power consumption is unavoidable. This aspect is evident specially for low values of differential input voltage $V_{in_{DIFF}}$, where the OTA practically never enters the slew rate regime and Class-AB action is not present.

From a visual point of view, the characteristic of Fig.5.8 and Fig.5.9 must present a good aspect for both at low and high values of $V_{in_{DIFF}}$. In practice, a good trade-off is reached for moderate overshoots present only for high values of $V_{in_{DIFF}}$, such as depicted in Fig.5.13.

5.3.3 SVMA Type 1 Optimization

The optimization process begins with a reduction of the I_{tail} current to 150 μA and the K_{AB} to 4, from the results in Table 5.2. The simulation results are shown in Fig.5.8.

This first simulation gives a SNDR of 97.65 dB, which is much lower than the previous results from Table 5.2. Evaluating the waveforms qualitatively it is possible to observe a large relaxation time and the absence of overshooting.

The relaxation time is related to the bandwidth, which in this case seems good enough to allow a further reduction in the tail current I_{tail}. But a problem may arise related to the capability of the system to supply current during the slewing mode, reducing the relaxation time and also emphasizing the effect of the bandwidth reduction. For this reason, the K_{AB} is first increased to 8 and after that a reduction in the I_{tail} is evaluated.

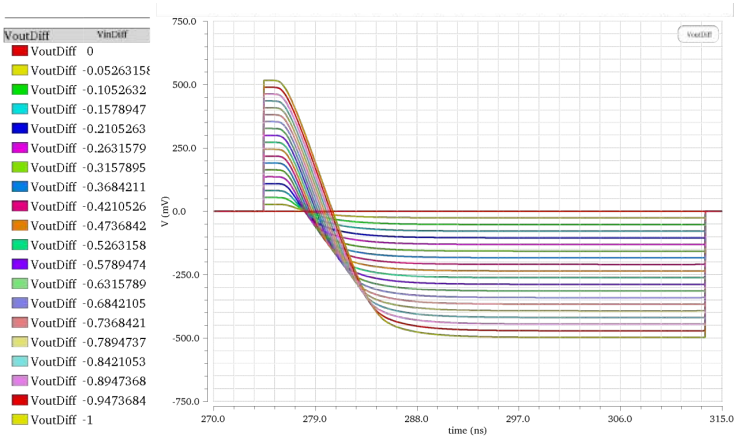


FIGURE 5.8: Type 1 differential output voltage waveform with $K_{AB} = 4$ and $I_{tail} = 150\mu A$.

From the new $K_{AB} = 8$ coefficient, the resulting SNDR is 99.85 dB which is higher than the previous value. Note also the appearance of overshooting and the increase in the relaxation time, as consequence of a higher slew-rate. A new simulation in which the K_{AB} is reduced to an intermediate value of 6 is performed, seeking the optimal value of SNDR.

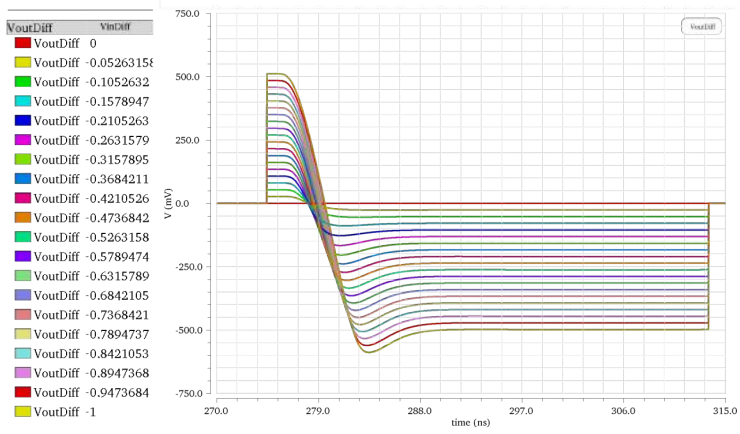


FIGURE 5.9: Type 1 differential output voltage waveform with $K_{AB} = 8$ and $I_{tail} = 150\mu A$.

The simulation results with $K_{AB} = 6$ provide higher a SNDR value up to 100.68 dB, while reducing the overshoot observed in Fig.5.9. The first part of increasing the Class-AB coefficient is achieved with a significant increment of the SNDR. Now is time to reduce the tail current, for this reason a current sweep to find the limits in terms of current is illustrated in Fig.5.10.

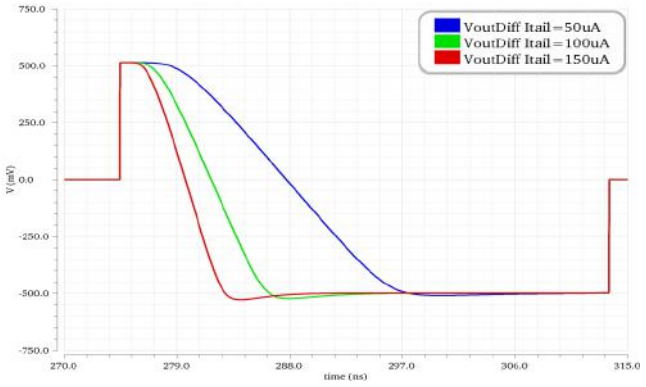


FIGURE 5.10: Type 1 differential output voltage waveforms for a fixed Vin_{DIFF} step of 1 V and I_{tail} equal to 150, 100 and 50 μA.

With this K_{AB} coefficient is it possible to observe that the lowest I_{tail} value must be higher than 50 μA, because the BW and slew-rate are severely affected, preventing the output from reaching the expected final value. For this reason a new different current value of 75 μA together with the 100 μA is simulated.

The SNDR obtained are 100.43 dB and 98.70 dB for a I_{tail} of 100 μA and 75 μA respectively. The SNDR variation from 100 μA to 150 μA is negligible. At this point a lower current value is achieved, but at least two more simulations are needed with different K_{AB} values to confirm the current limit is reached. The results for both $K_{AB} = 4$ and $K_{AB} = 8$, together with the previous results are summarized in Table 5.3.

		I_{tail}		
		$75\mu A$	$100\mu A$	$150\mu A$
K_{AB}	4		99.08 dB	97.65 dB
	6	98.70 dB	100.43 dB	100.68 dB
	8		99.22 dB	99.85 dB

TABLE 5.3: Type 1 explored design space.

First of all is important to notice the robustness of the SVMA against huge variations in the tail current and in the geometrical sizing of the structure. Ensuring the expected 16 Bits of resolution even when this parameters (I_{tail} and K_{AB}) vastly differs from the optimal solution found with the optimization method described in this chapter.

5.3.4 SVMA Type 2 Optimization

Type 2 SVMA topology optimization process starts with the same parameters used for Type 1 ($I_{tail} = 150\mu$A and the $K_{AB} = 4$). Aiming is to achieve at least the same current consumption obtained by type 1 in the previous section, the first simulation results with Type 2 are shown in Fig.5.11.

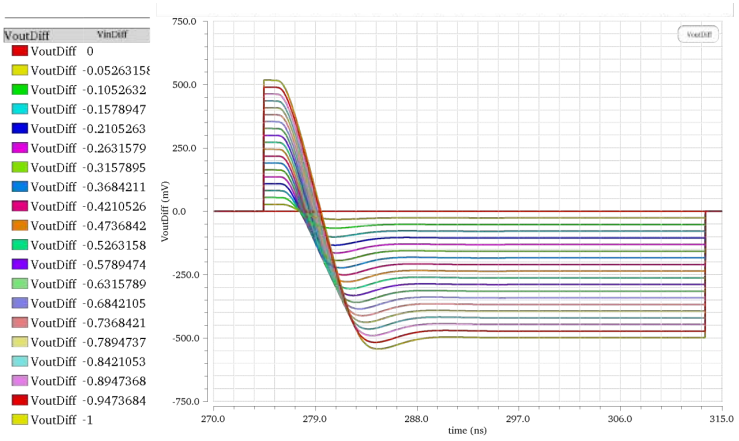


FIGURE 5.11: Type 2 differential output voltage waveform with $K_{AB} = 4$ and $I_{tail} = 150\mu A$.

In this case, in contrast with the previous type simulation results, the former topology presents more overshooting in the output signal while maintaining a large relaxation time. The SNDR is also higher reaching a value of 100 dB.

In the type 1 case, the K_{AB} coefficient was increased, to have more current capability, and from this new point the total bias current was reduced. In this case the K_{AB} coefficient to 3, obtaining a reduction of the SNDR to 98 dB is obtained. From this point, to increase the SNDR to the previous 100 dB, the current must be increased. To confirm this assumption a current of 170 μA while maintaining the same K_{AB} equal to 3 is simulated, obtaining 99.88 dB of SNDR. This result reinforces the idea explained before about the close relationship between both regions of operation (slewing and relaxation).

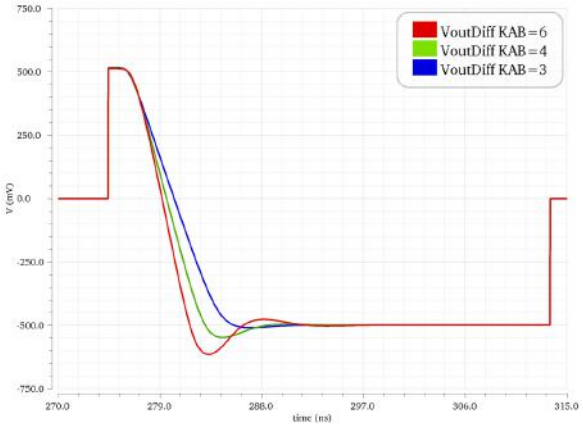


FIGURE 5.12: Type 2 differential output voltage waveforms for a fixed Vin_{DIFF} step of 1 V with I_{tail} of 150 μA and K_{AB} equal to 3, 4 and 6.

Fig.5.12, represents the differential output voltage for three K_{AB} coefficient values. Illustrating how for higher K_{AB} coefficients the bandwidth of the system is reduced, increasing the relaxation time due to the less dumping effect on the second part of the transient. The contrary happens with the lowest K_{AB} value, in which the slewing time is increased but the output stabilizes smoothly.

Following the optimization process and confirming after simulation different K_{AB} values with the same current that the K_{AB} coefficient is at the correct point. It is time to reduce the tail current by the same amount used in the type 1. For I_{tail} currents of 100 μA and 75 μA, the SNDR obtained is 104 dB and 102.6 dB respectively. With the intention to reduce even further the current consumption a final simulation using a tail current of 50 μA is performed obtaining a huge drop to 46 dB. Simulation results from the optimal solution found by the optimization process are shown in Fig.5.13. Is it possible to observe overshooting but the stabilization time and the transient dynamics fit with the modulator requirements.

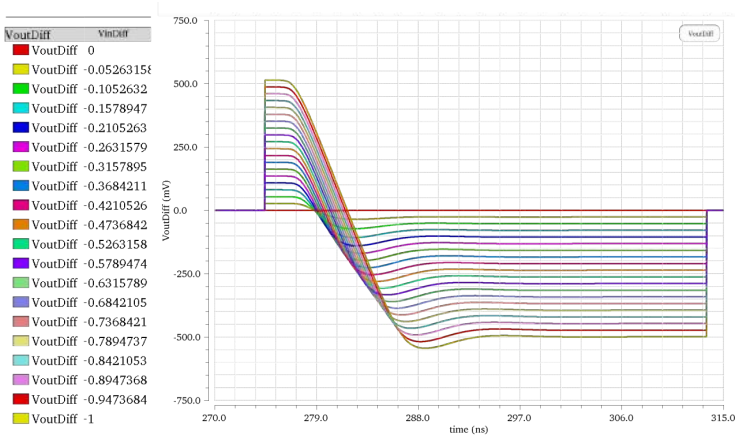


FIGURE 5.13: Type 2 differential output voltage waveform with $K_{AB} = 4$ and $I_{tail} = 100\mu A$.

All the simulation performed during the optimization process are summarized in Table 5.4.

		I_{tail}			
		$50\mu A$	$75\mu A$	$100\mu A$	$150\mu A$
K_{AB}	3			98 dB	99.8 dB
	4	46 dB	102.6 dB	104 dB	100.71 dB
	6			75 dB	99.1 dB

TABLE 5.4: Type 2 explored design space.

As in the previous topology it is important to note the robustness of the modulator against variations in the current and in the sizing of the different blocks. Ensuring in all the cases the expected 16 Bits of resolution. In this case the selected candidate is the one with $K_{AB} = 4$ and $I_{tail} = 100\mu A$, even when there is another candidate presenting less current consumption it is appreciated to maintain the design with a certain security margin, taking advantage of the robustness.

5.3.5 2^{nd} and 3^{rd} SVMA stages

The second and third SVMA stages are less critical to be designed than the first stage, because the errors introduced are one and two orders shaped respectively. These effect allows to scale down both SVMA circuits depending on the equivalent capacity C_{eq} seen by the SVMA at the output. The equivalent capacity is calculated from Eq.5.2.

$$C_{eq} = \frac{C_s \cdot C_{in}}{C_s + C_{in}} + C_L \tag{5.2}$$

Where the C_L is the sum of the next stage sampling capacity and the former stage feedforward capacity. With the exception of the third stage in with C_L equals to C_{ff3}. Table 5.5 presents the equivalent capacitance C_{eq} and the scale down factors applied to the current and also to the transistor level sizing.

	C_{eq}	Scale Factor	Type 1 and 2 Current
SVMA 1	4 pF	-	100 μA
SVMA 2	1.42 pF	$\sim$1/3	35 μA
SVMA 3	0.83 pF	$\sim$1/5	20 μA

TABLE 5.5: 2^{nd} and 3^{rd} SVMA stages scale down.

Simulation results of the 2^{nd} and 3^{rd} SVMA stages for both types confirms the expected performance, allowing the design process to continue with the SC Σ-Δ modulator electrical simulations.

5.4 SC Σ-ΔM electrical simulations

This section includes the simulation results of the complete system with the transistor level SVMAs designed above. Due to time restrictions it was not possible to include all the transistor levels blocks such as the switches and the single bit quantizer. The selection of the final topology to be implemented is decided in terms of static current consumption. Table 5.6 presents the simulated current consumption of the modulator. The values have been extracted by means of transient simulation applying -6 dBFS at the input, so the total consumption accounts both the static and the signal dependent power consumption.

	Total Current
Type 1	795 μA
Type 2	643 μA

TABLE 5.6: Simulated dynamic current consumption of each SC Σ-ΔM implemented for both SVMA types.

As explained before in Chapter 4.2.3.2, type 1 requires from an additional bias to polarize correctly the C transistors in charge of the negative feedback (Fig.4.12). But in the case of this work the current flowing trough each stack of transistors is supposed to be of the same value as I_{tail}. In fact, this is not necessary because a proportional scaled down version of

this stack can be used. Therefore, the contribution to the final power consumption of type 1 will be reduced and comparable to the expected from type 2.

Is important to note the static current of the single bit quantizer is not considered because of the latching operation with nule static current consumption allowed by the selected topology[41].

In this work type 2 is selected to be implemented following the current consumption criteria explained above. But as the steps to follow for the complete SC Σ-Δ modulator simulation are fulfilled for both topologies, the PSD-spectrum and SNDR results for type 1 (Fig.5.14a) and type 2 (Fig.5.14b) are presented.

Assuming 16 Bits or what is the same a SNDR values of 98.1 dB, the Schreier FOM for the modulator based on type 2 SVMAs, can be calculated taking into account the static current estimated in the Table 5.6.

$$FOM_{Schreier} \equiv 98.1dB + 10\log(\frac{50kHz}{643\mu A \cdot 1.8V}) = 174.45dB \tag{5.3}$$

With a conservative approach a theoretical Schreier FOM of 174.45 dB is achieved.

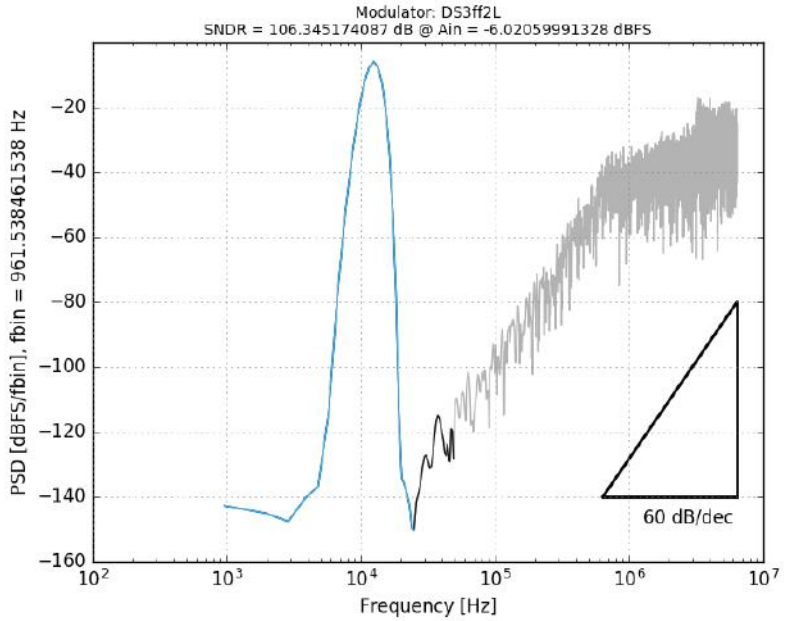
Simulation results from Fig.5.14 shows the expected SNDR value and also confirms the viability of the novel design methodology based on a Bottom-up approach. Reducing the simulation time from 7 days to 20 minutes, while guaranteeing the correct behaviour of the SVMAs, and relieving the simulation of the complete system as the last step in the validation.

Finally, simulations across corners with the selected Type 2 topology are performed and presented in Table 5.7

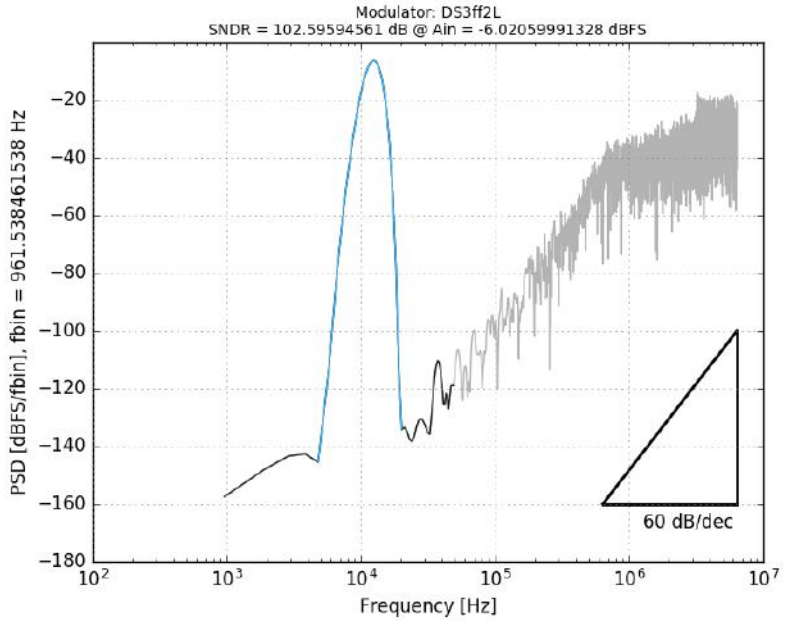
	Type 2
Typ	103.08 dB
Wp	101.25 dB
Wo	101.90 dB
Wz	101.52 dB
Ws	98.34 dB

TABLE 5.7: SC Σ-ΔM Type 2 simulation across corners.

Simulation results across corners shows a low deviation between the typical case and almost all the worst cases. Worst-speed corner present the highest SNDR drop, but, strictly from a numerical point of view, it still complies with the resolution requirements fixed in this work, even if no room is left for any safe margin. This drop in the SNDR is caused by the third harmonic distortion, but the final resolution including thermal noise is suppose to maintain the same SNDR value, as the effect from distortion and noise can be considered to be uncorrelated.



(A) Type 1 SC Σ-ΔM electrical simulation.



(B) Type 2 SC Σ-ΔM electrical simulation.

FIGURE 5.14: SC Σ-ΔM electrical simulations (Cadence), which represents 7 days of computing for 16 cycles with the ideal versions of the quantizer and the switching network, versus the maximum of 20 minutes spent in the bottom-up approach (simplified Cadence testbench and Python code simulation).

Chapter 6

Conclusions

6.1 Conclusions

A high-resolution 16-bits and double audio bandwidth (50 kHz) Σ-Δ modulator ADC design, targeted for low-power operation, is presented in the framework of this master thesis. The CMOS modulator is based on a switched-capacitor topology and a novel switched variable mirror amplifier, for robust operation and insensitivity to both process and temperature variations. The design process comprises the achievement of the following objectives stated in Chapter 1.5:

- The development of a high-level simulation platform using the non-proprietary software Python, implementing all the necessary modulator models and testing the most important system-level parameters. This design tool allows the selection of the best suited modulator architecture, loop order and coefficients values to achieve the required dynamic-range performance. Furthermore, the same environment can be also used to include the circuit-level details in the high-level simulations for fast prototyping and design, which is necessary in the optimization process described in Chapter 5.

- Exploration of the robustness and performance of the new family of Class-AB switched Variable Mirror Amplifier (SVMA) introduced in [32].

- Reduction in one order of magnitude of the current consumption with respect to [32] and finding the optimal CMOS circuit sizing with respect to current consumption. The optimization of SVMAs was done with a novel design methodology based on bottom-up approach, which ensures feasible circuit performance at architectural level without the need of large iterative simulations of the complete SC Σ-Δ modulator.

- Reduction of almost three order of magnitude of the simulation times with respect to the traditional approach and relaying the complete SC Σ-Δ modulator simulation to a final verification step.

- Schematic design of the SC Σ-Δ modulator in a commercial 180-nm triple MiM-capacitor standard CMOS technology, obtaining a static power consumption of 643 μA with a nominal voltage supply of 1.8 V. The provisional, estimated Schreier FOM of 174,16 dB, outstands the current state-of-the-art Σ-Δ modulators reported in literature, and it

is achieved by the use of architectural and circuital low-power techniques. In this sense, analog calibration, complex digital circuit post-processing, bootstrapping and resistors have been avoided, in favour of a robust low-cost circuit implementation.

6.2 Future work

Due to time limitation imposed by the framework of this master thesis, some few task are still required in order to complete the CMOS design of the Σ-Δ modulator circuit. These steps are declared in the following list:

- The quantizer, although simple in this design, has to be still tested inside the complete Σ-Δ loop.
- Study the possibility to use a modular design for various SVMAs, present in all the stages of the modulator, using parallel realizations of the same layout SVMA cell.
- Design of the full-custom mixed-signal CMOS layout, both floorplan and block level.
- Perform all the post-layout simulation and verifications before sending the design to the foundry.

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